

Compal Confidential

JFWXX Schematics Document

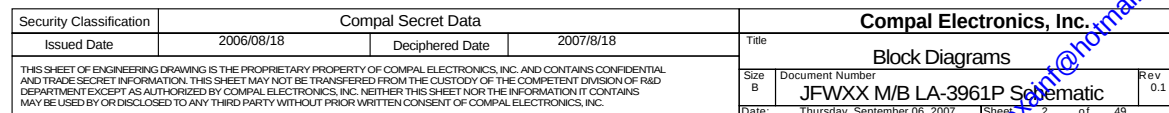
Intel Merom Processor with SiSM672MX + DDRII + SiS968 + SiS307LV

2007 - 09 - 06

REV: 0.3

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				JFWXX M/B LA-3961P Schematic	
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Model Name : JFWXX
File Name : LA-3961P



Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS (Actual +0.9V)	0.9V switched power rail for DDR terminator	ON	ON	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

PROJECT ID Table

	PROJECT_ID
14W	R424 (Pull low)
15W	NA (Internal Pull High)

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
CARD BUS CB1410	AD20	2	C,D
1394+Cardreader	AD22	0	G,H

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADI ADM1032	1001 100X b
EEPROM(24C16/02)	1010 000X b	NVIDIA NB8X	

EC SM Bus2 address

ICH8M SM Bus address

Device	Address
Clock Generator (ICS9LPRS325AKLFT_MLF72)	1101 001Xb
DDR DIMM0	1010 000Xb
DDR DIMM1	1010 010Xb

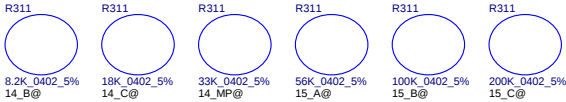
SKU ID Table

Vcc	3.3V +/- 5%
Ra	100K +/- 5%

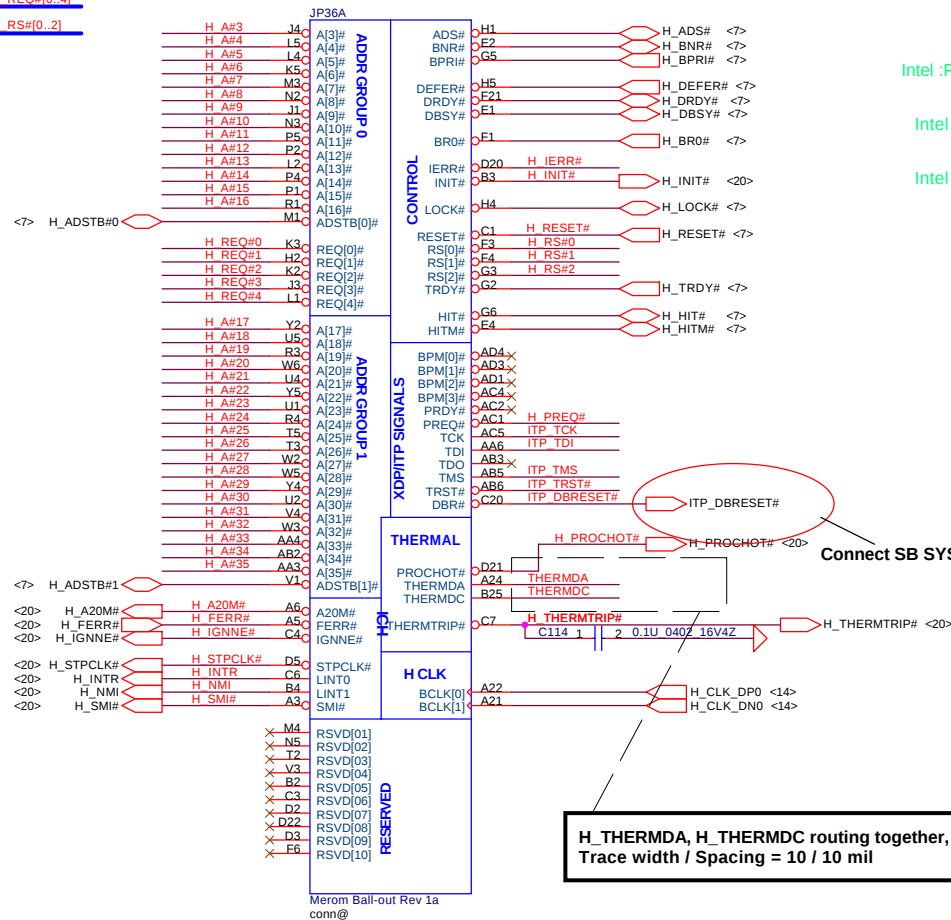
Ra~ R312

Rb~ R311

Board ID	Rb	VAD_BID Min	VAD_BID typ	VAD_BID Max	Rb BOM Structure
0	0	0 V	0 V	0 V	14_A@
1	8.2K +/- 5%	0.217 V	0.250 V	0.288 V	14_B@
2	18K +/- 5%	0.439 V	0.503 V	0.575 V	14_C@
3	33K +/- 5%	0.721 V	0.819 V	0.926 V	14_MP@
4	56K +/- 5%	1.054 V	1.185 V	1.325 V	15_A@
5	100K +/- 5%	1.489 V	1.650 V	1.819 V	15_B@
6	200K +/- 5%	2.019 V	2.200 V	2.386 V	15_C@
7	NC	3.135V	3.300 V	3.465 V	15_MP@



<7> H_A# [3..35] H_A# [3..35]
 <7> H_REQ# [0..4] H_REQ# [0..4]
 <7> H_RS# [0..2] H_RS# [0..2]

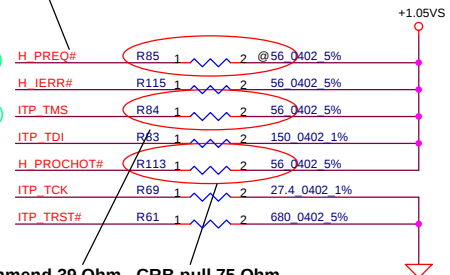


H_THERMDA, H_THERMDC routing together,
 Trace width / Spacing = 10 / 10 mil

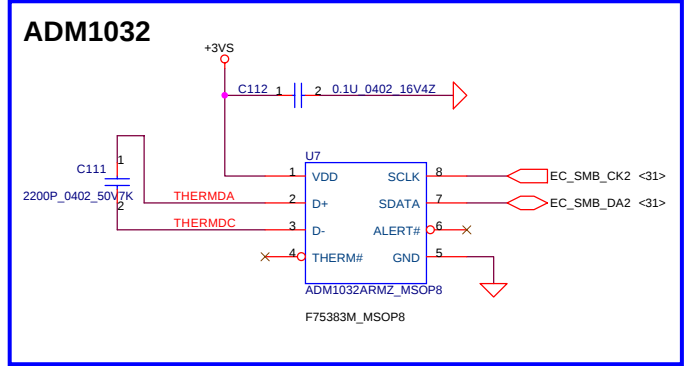
Trace length must short

Place close to CPU within 500mil

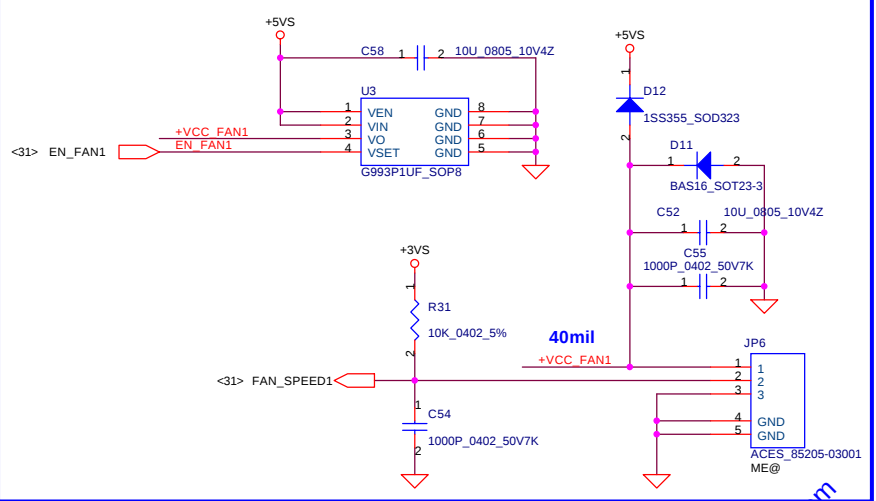
Intel : Pull-up 56ohm (Un-Mount) SIS : Pull-up 56ohm (Mount)
 Intel : Pull-up 56ohm (Mount) SIS : Pull-up 54.9ohm (Mount)
 Intel : Pull-up 56ohm (Mount) SIS : Pull-up 75ohm (Mount)



Checklist recommend 39 Ohm CRB pull 75 Ohm



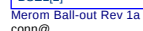
FAN1 Conn



CPU to SB interface



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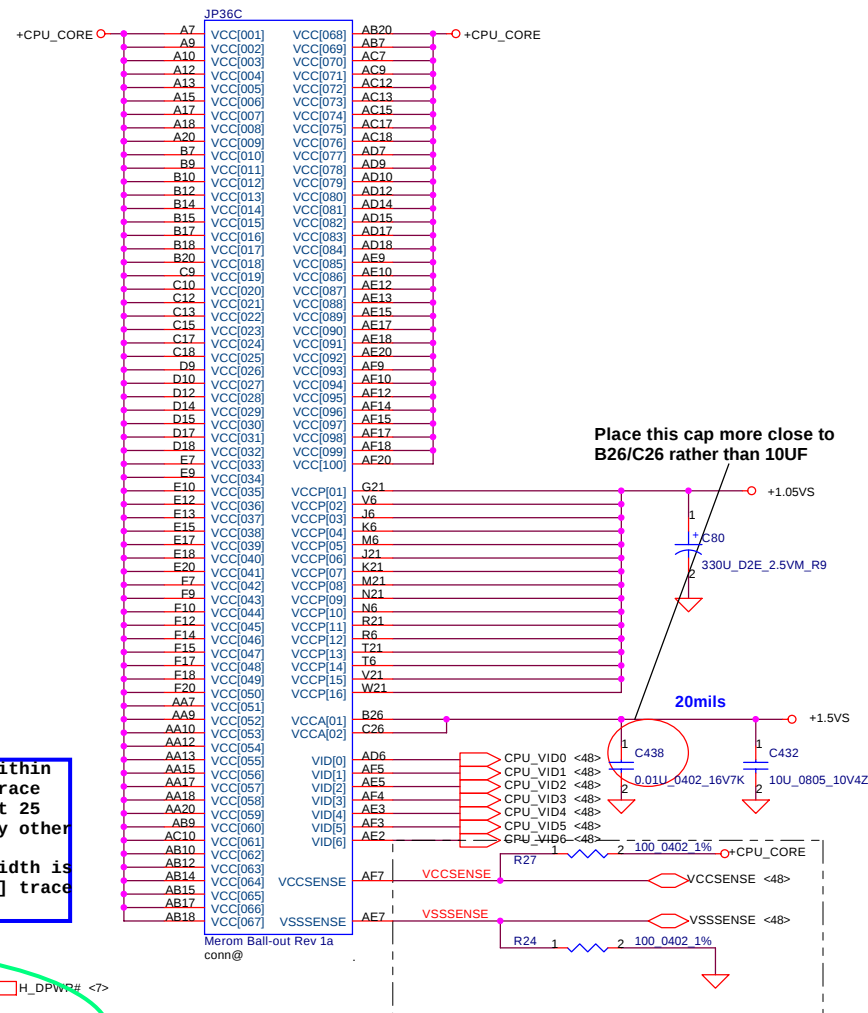


CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1
200	0	1	0



length match within 25 mils.
the trace width/space/other is
/7/25.

Close to CPU pin
within 500mils.



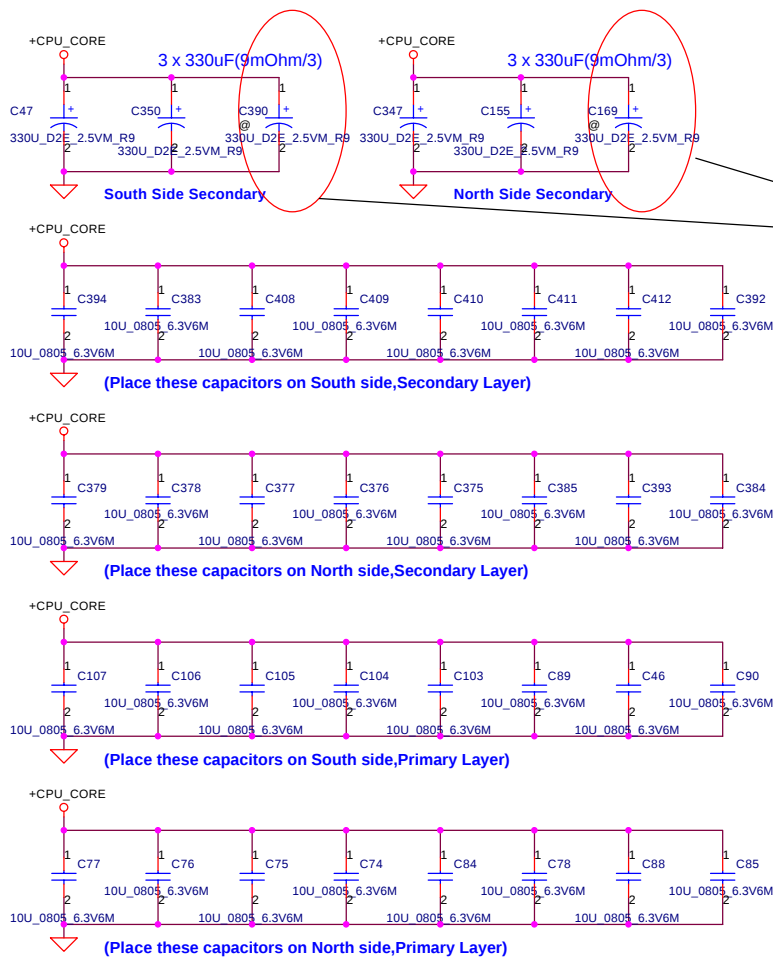
Place this cap more close to B26/C26 rather than 10UF

20mils

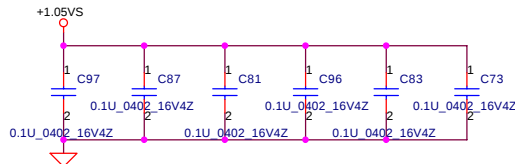
		Compal Electronics, Inc.	
		Title Merom (2/3)	
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JP36D			
A4	VSS[001]	VSS[082]	P6
A8	VSS[002]	VSS[083]	P21
A11	VSS[003]	VSS[084]	P24
A14	VSS[004]	VSS[085]	R2
A16	VSS[005]	VSS[086]	R5
A19	VSS[006]	VSS[087]	R22
A23	VSS[007]	VSS[088]	R25
AF2	VSS[008]	VSS[089]	T1
B6	VSS[009]	VSS[090]	T4
B8	VSS[010]	VSS[091]	T23
B11	VSS[011]	VSS[092]	T26
B13	VSS[012]	VSS[093]	U3
B16	VSS[013]	VSS[094]	U6
B19	VSS[014]	VSS[095]	U21
B21	VSS[015]	VSS[096]	U24
B24	VSS[016]	VSS[097]	V2
C5	VSS[017]	VSS[098]	V5
C8	VSS[018]	VSS[099]	V22
C11	VSS[019]	VSS[100]	V25
C14	VSS[020]	VSS[101]	W1
C16	VSS[021]	VSS[102]	W4
C19	VSS[022]	VSS[103]	W23
C2	VSS[023]	VSS[104]	W26
C22	VSS[024]	VSS[105]	Y3
C25	VSS[025]	VSS[106]	Y6
D1	VSS[026]	VSS[107]	Y21
D4	VSS[027]	VSS[108]	Y24
D8	VSS[028]	VSS[109]	AA2
D11	VSS[029]	VSS[110]	AA5
D13	VSS[030]	VSS[111]	AA8
D16	VSS[031]	VSS[112]	AA11
D19	VSS[032]	VSS[113]	AA14
D23	VSS[033]	VSS[114]	AA16
D26	VSS[034]	VSS[115]	AA19
E3	VSS[035]	VSS[116]	AA22
E6	VSS[036]	VSS[117]	AA25
E8	VSS[037]	VSS[118]	AB1
E11	VSS[038]	VSS[119]	AB4
E14	VSS[039]	VSS[120]	AB8
E16	VSS[040]	VSS[121]	AB11
E19	VSS[041]	VSS[122]	AB13
E21	VSS[042]	VSS[123]	AB16
E24	VSS[043]	VSS[124]	AB19
F5	VSS[044]	VSS[125]	AB23
F8	VSS[045]	VSS[126]	AB26
F11	VSS[046]	VSS[127]	AC3
F16	VSS[047]	VSS[128]	AC6
F19	VSS[048]	VSS[129]	AC8
F2	VSS[049]	VSS[130]	AC11
F22	VSS[050]	VSS[131]	AC14
F25	VSS[051]	VSS[132]	AC16
G4	VSS[052]	VSS[133]	AC19
G1	VSS[053]	VSS[134]	AC21
G23	VSS[054]	VSS[135]	AC24
G26	VSS[055]	VSS[136]	AD2
H3	VSS[056]	VSS[137]	AD5
H6	VSS[057]	VSS[138]	AD8
H21	VSS[058]	VSS[139]	AD11
H24	VSS[059]	VSS[140]	AD13
J2	VSS[060]	VSS[141]	AD16
J5	VSS[061]	VSS[142]	AD19
J22	VSS[062]	VSS[143]	AD22
J25	VSS[063]	VSS[144]	AD25
K1	VSS[064]	VSS[145]	AE1
K4	VSS[065]	VSS[146]	AE4
K23	VSS[066]	VSS[147]	AE8
K26	VSS[067]	VSS[148]	AE11
L3	VSS[068]	VSS[149]	AE14
L6	VSS[069]	VSS[150]	AE16
L21	VSS[070]	VSS[151]	AE19
L24	VSS[071]	VSS[152]	AE23
M2	VSS[072]	VSS[153]	AE26
M5	VSS[073]	VSS[154]	A2
M22	VSS[074]	VSS[155]	A2
M25	VSS[075]	VSS[156]	AF6
N1	VSS[076]	VSS[157]	AF8
N4	VSS[077]	VSS[158]	AF11
N23	VSS[078]	VSS[159]	AF13
N26	VSS[079]	VSS[160]	AF16
P3	VSS[080]	VSS[161]	AF19
	VSS[081]	VSS[162]	AF21
		VSS[163]	A25
			AE25

Merom Ball-out Rev 1a
conn@

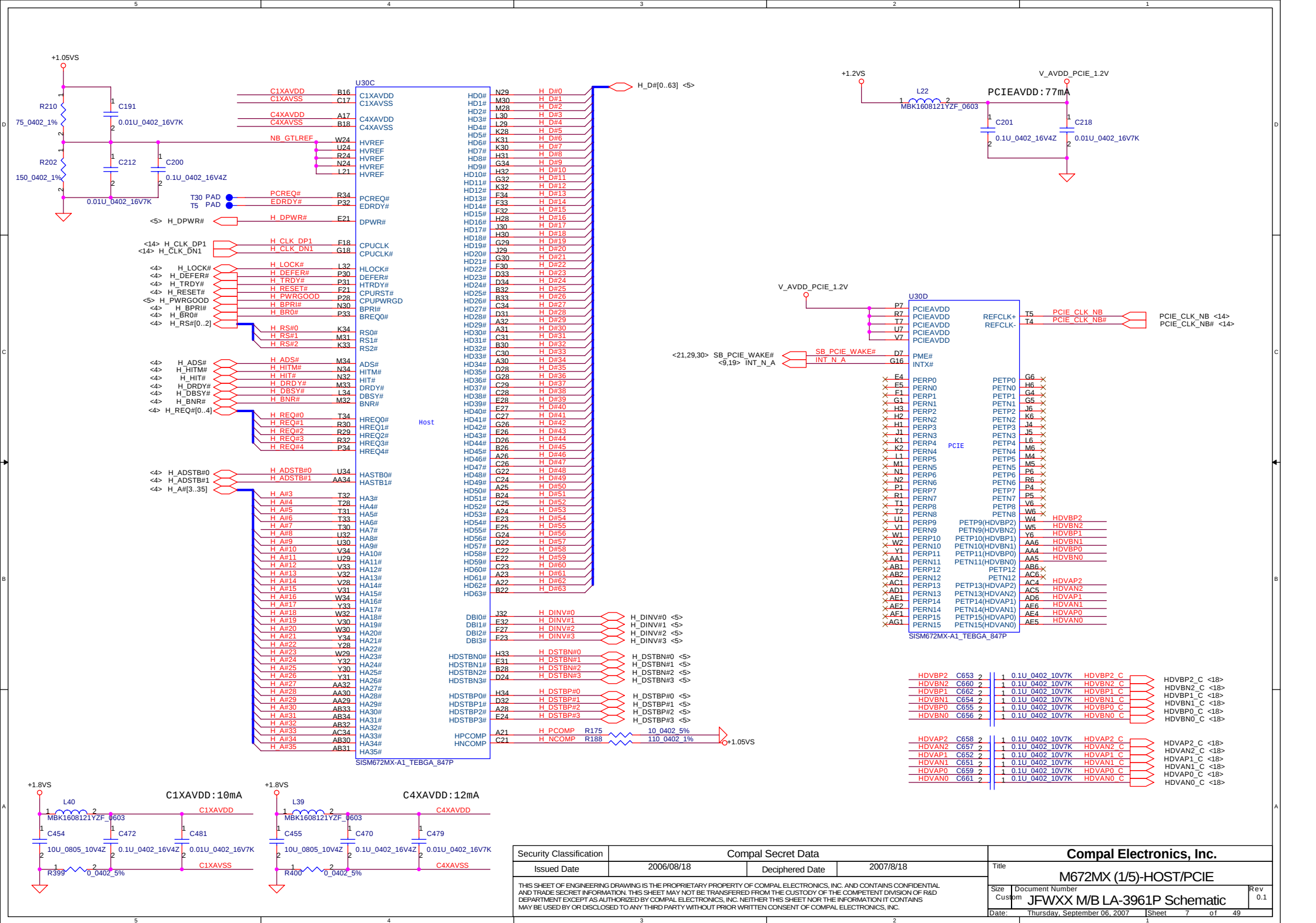


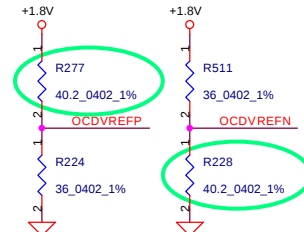
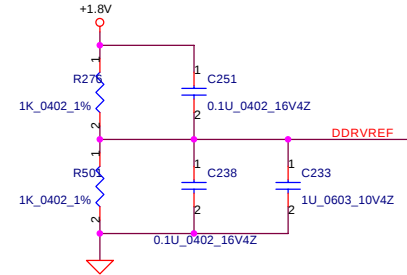
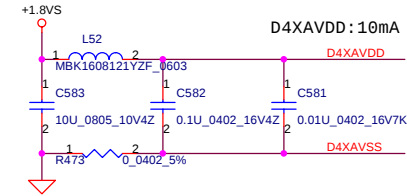
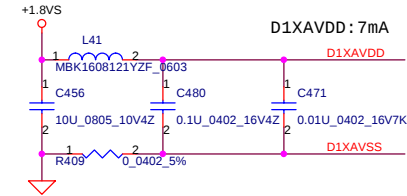
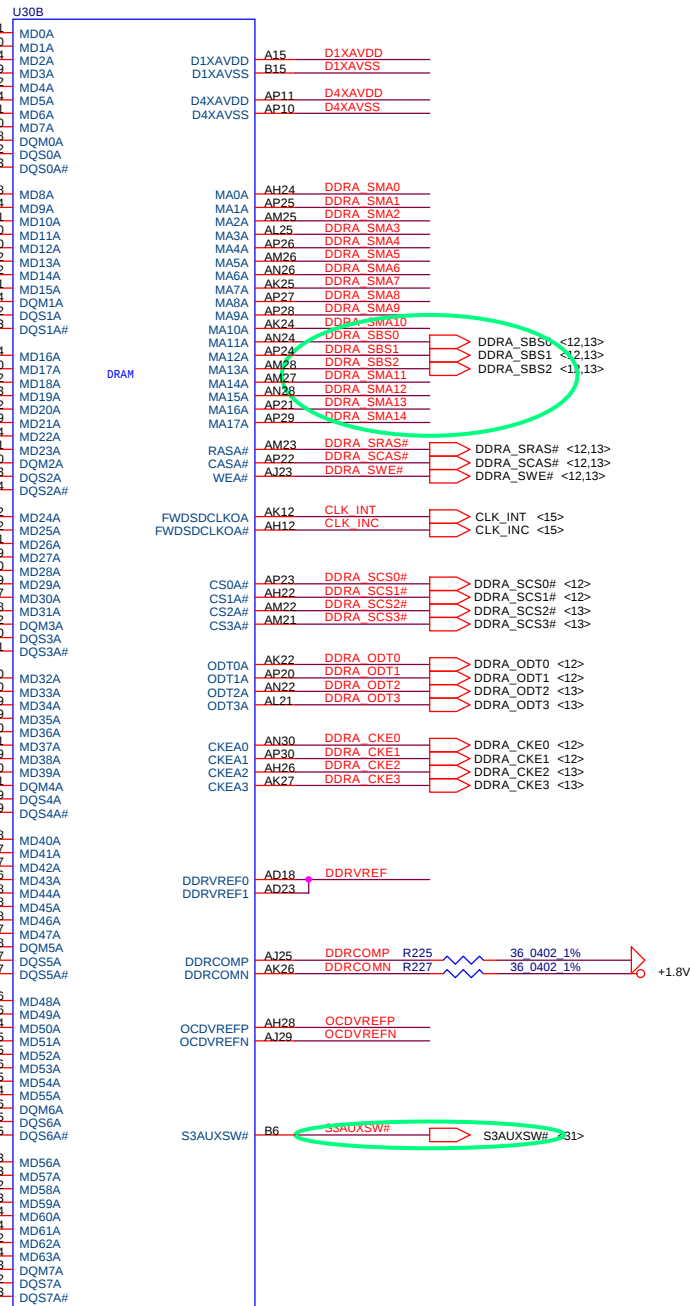
+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP, Polymer	6X330uF	9m ohm/6	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32
	32X10uF	3m ohm/32	0.6nH/32



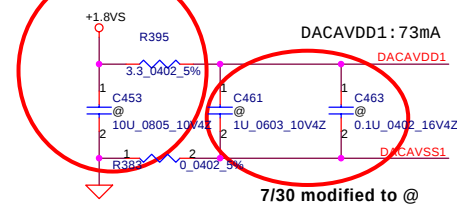
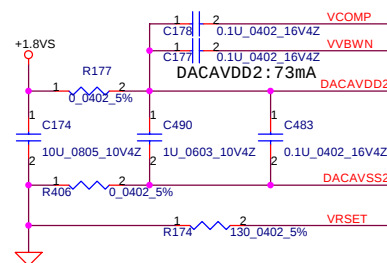
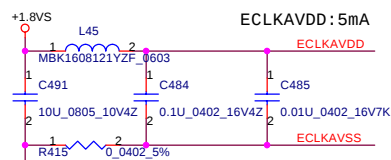
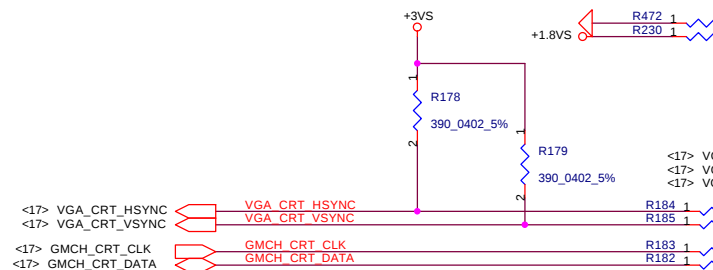
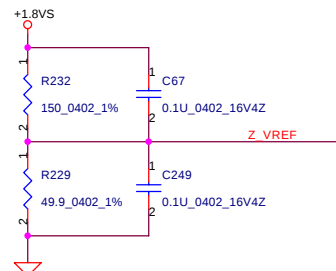
CRB no stuff. Reserved!

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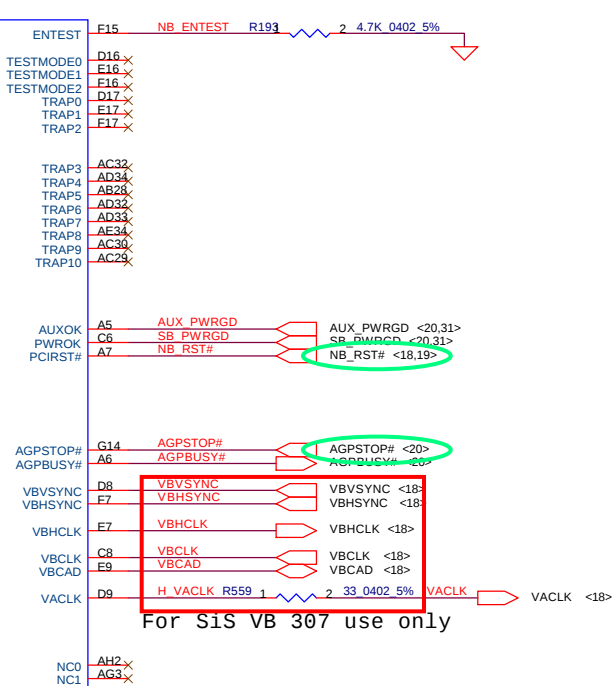
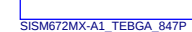
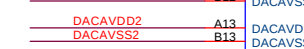
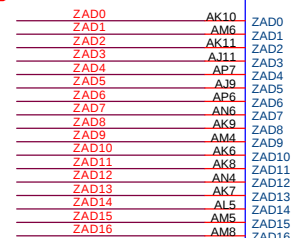




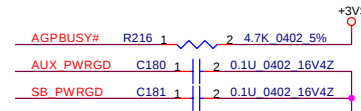
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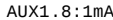
DACAVDD1 Spec.
Voltage : 1.5V +/- 5%
Current : 100mA



For SiS VB 307 use only

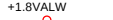


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				Size	Rev
				Custom	0.1
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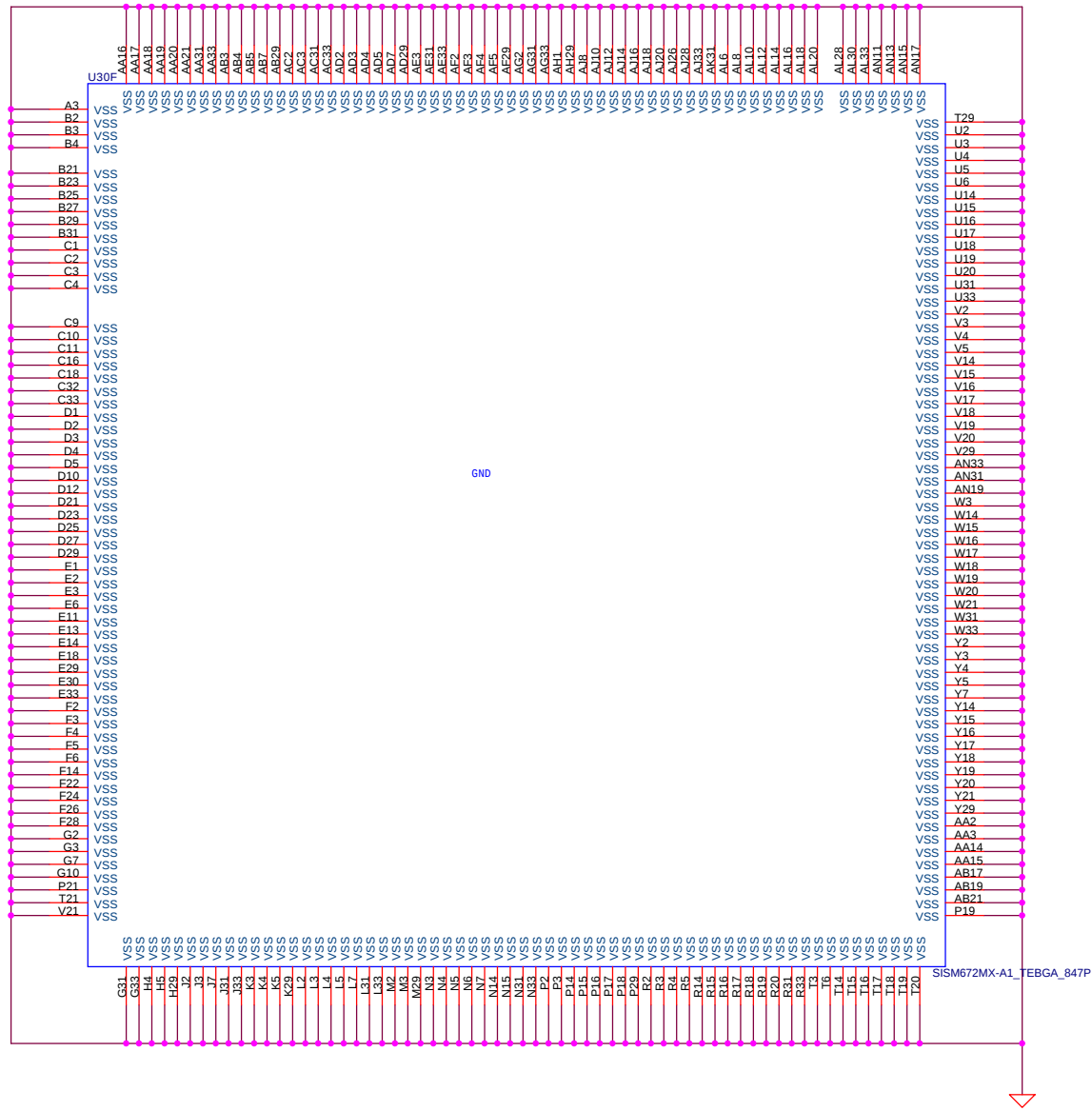


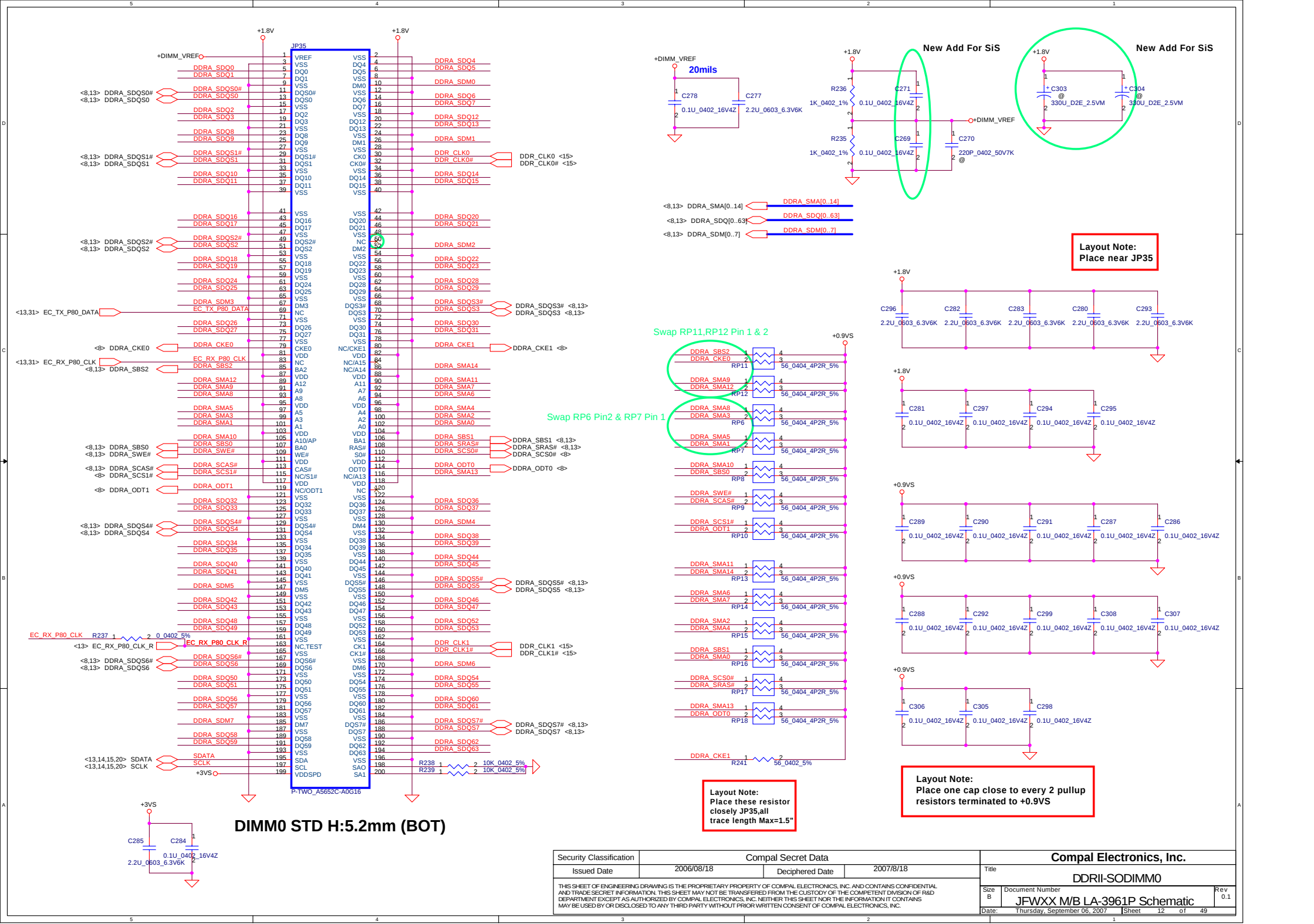
The diagrams show the following capacitor configurations:

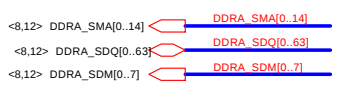
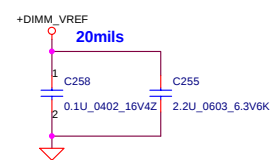
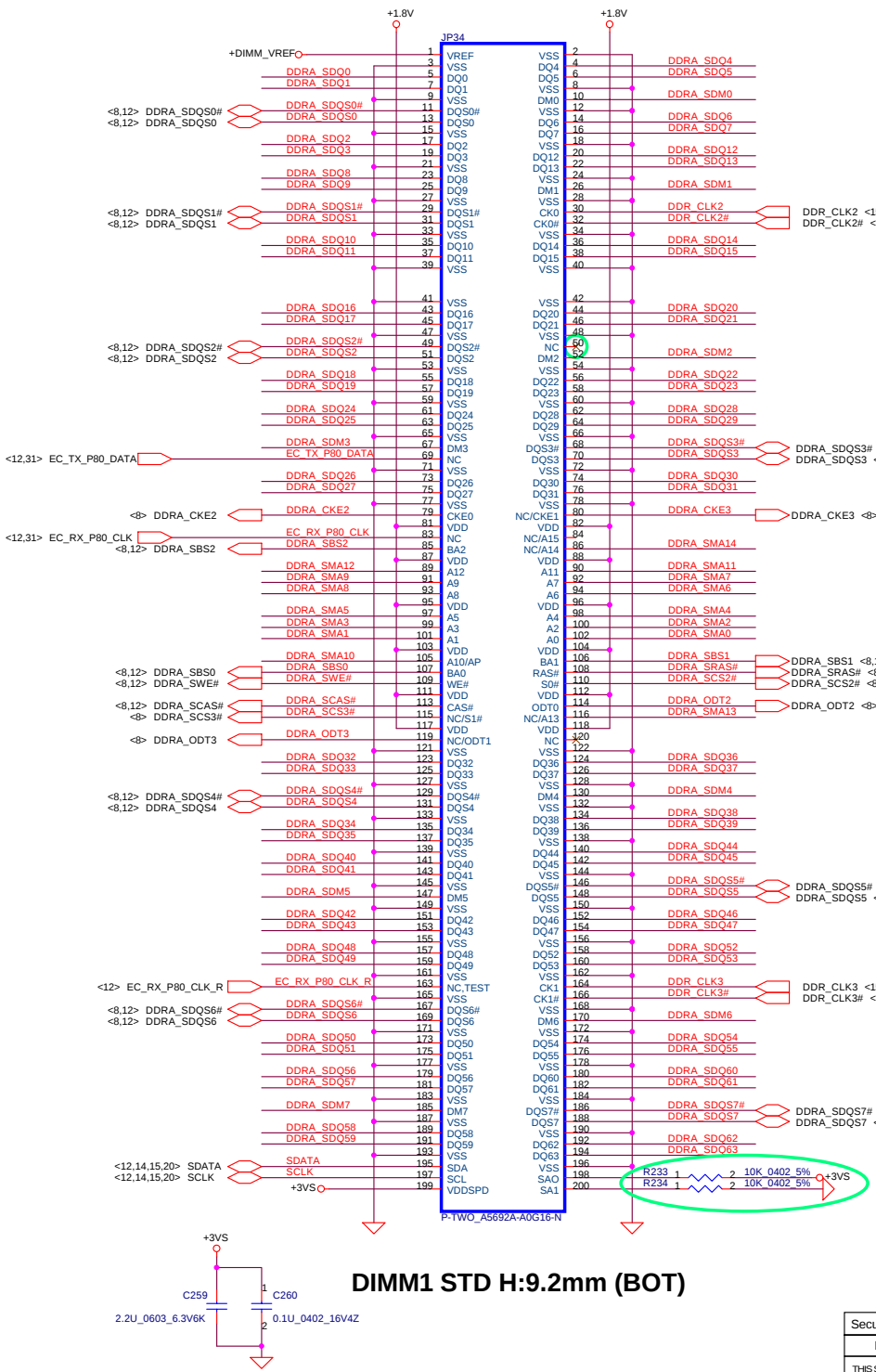
- +1.8V:** A series of six capacitors in parallel: C230 (0.1U 0402 16V4Z), C231 (0.1U 0402 16V4Z), C235 (1U 0603 10V4Z), C223 (1U 0603 10V4Z), C237 (4.7U 0805 10V4Z), and C236 (4.7U 0805 10V4Z).
- +1.2VS:** A series of six capacitors in parallel: C226 (0.1U 0402 16V4Z), C209 (0.1U 0402 16V4Z), C213 (1U 0603 10V4Z), C220 (1U 0603 10V4Z), C196 (4.7U 0805 10V4Z), and C242 (4.7U 0805 10V4Z).
- +1.8VALW:** A single capacitor C190 (1U 0603 10V4Z) in parallel with ground.
- +1.2VALW:** A single capacitor C182 (1U 0603 10V4Z) in parallel with ground.
- +1.8VS:** A series of three capacitors in parallel: C198 (0.1U 0402 16V4Z), C221 (1U 0603 10V4Z), and C193 (1U 0603 10V4Z).
- +1.2VS:** A series of three capacitors in parallel: C197 (0.1U 0402 16V4Z), C240 (1U 0603 10V4Z), and C234 (1U 0603 10V4Z).
- +1.05VS:** A series of three capacitors in parallel: C188 (0.1U 0402 16V4Z), C179 (1U 0603 10V4Z), and C184 (1U 0603 10V4Z).



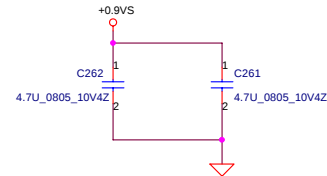
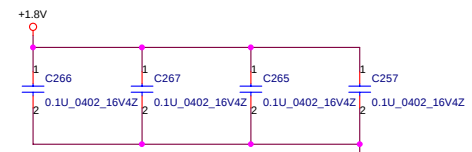
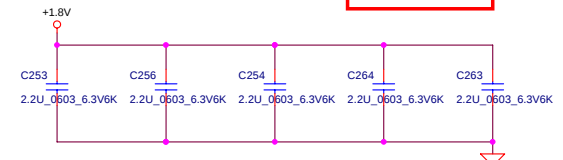
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	M672MX (4/5)-POWER	
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				Cusom	JFWXX M/B LA-3961P Schematic	0.1
				Date:	Thursday, September 06, 2007	Sheet 10 of 49







Layout Note:
Place near JP34



Layout Note:
Place these resistor
closely JP34,all
trace length Max=1.5"

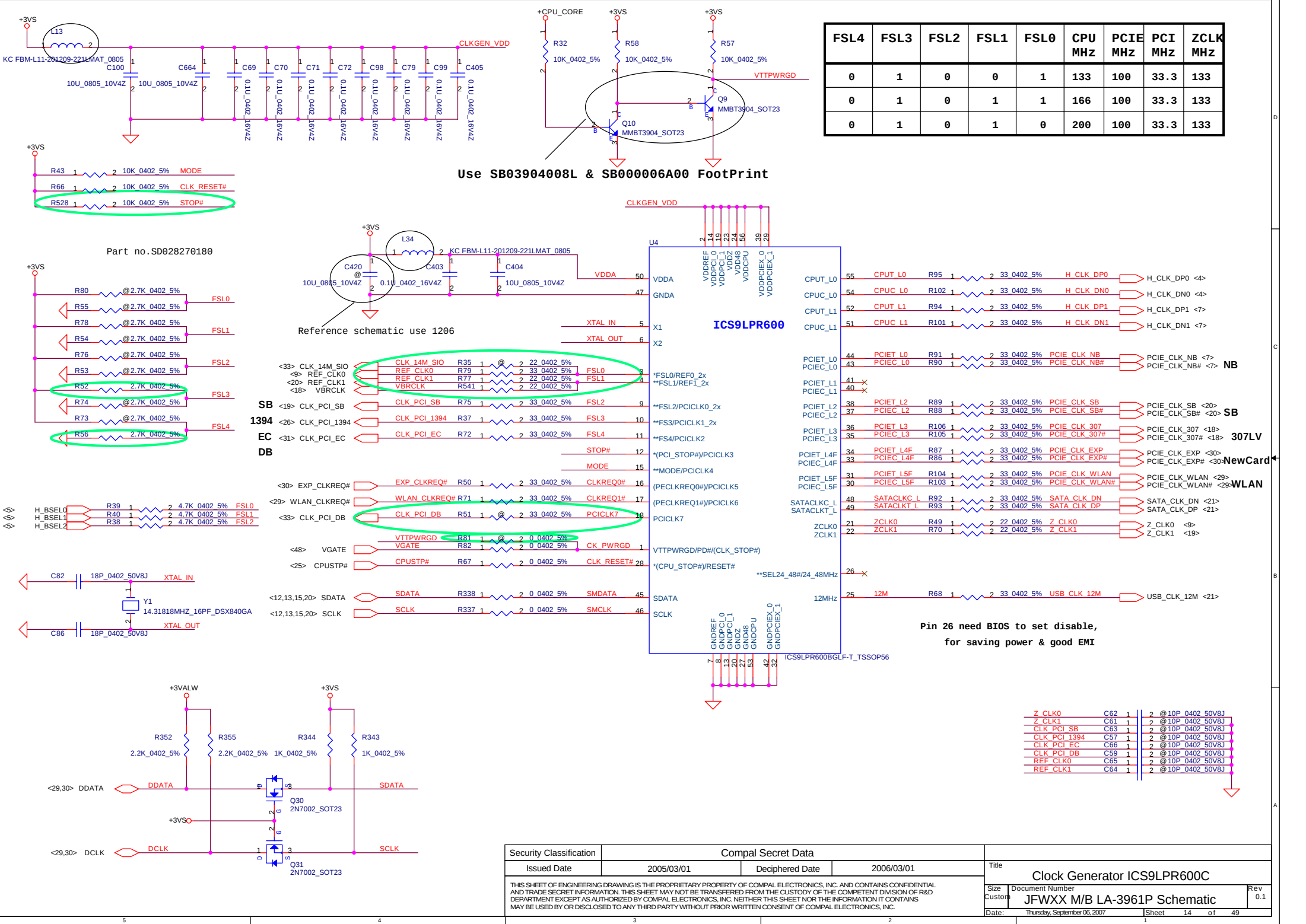
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS

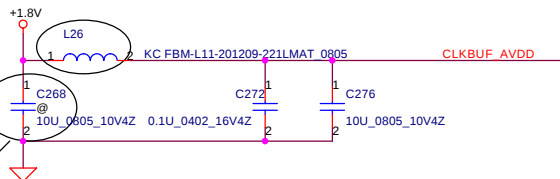
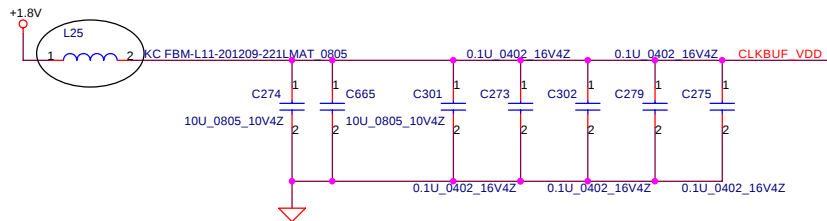
DIMM1 STD H:9.2mm (BOT)

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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	
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Size B	Document Number	JFWXX M/B LA-3961P Schematic		Rev 0.1	
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FSL4	FSL3	FSL2	FSL1	FSL0	CPU MHZ	PCIE MHZ	PCI MHZ	ZCLK MHZ
0	1	0	0	1	133	100	33.3	133
0	1	0	1	1	166	100	33.3	133
0	1	0	1	0	200	100	33.3	133

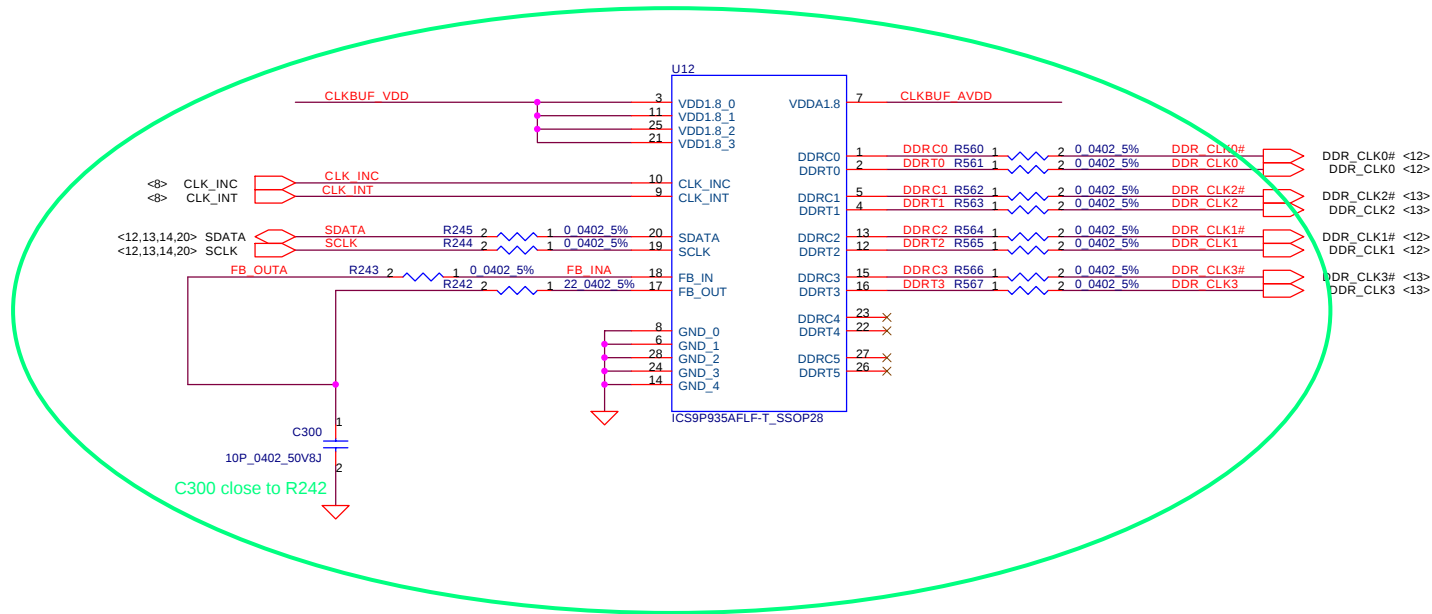
Use SB03904008L & SB000006A00 FootPrint





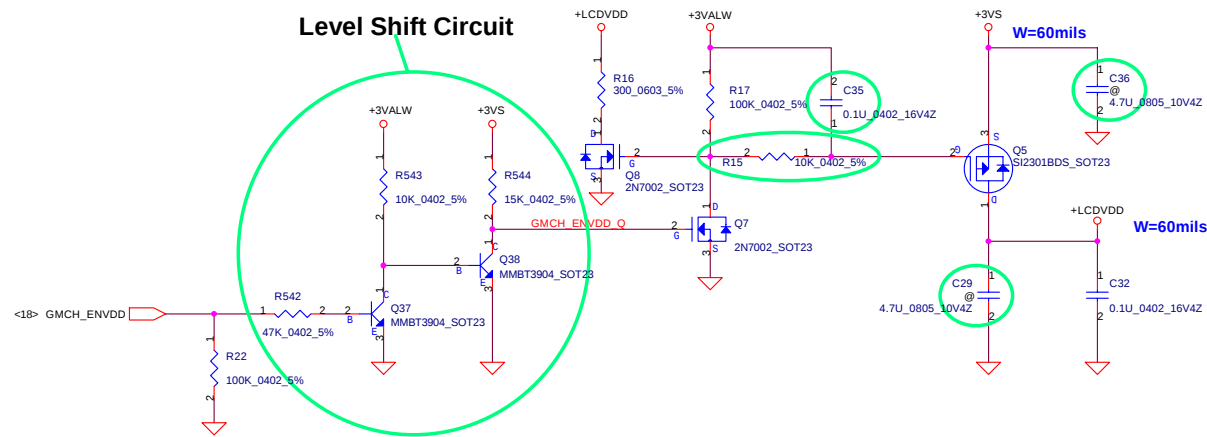
Reference schematic use 1206

Horizontal rotate

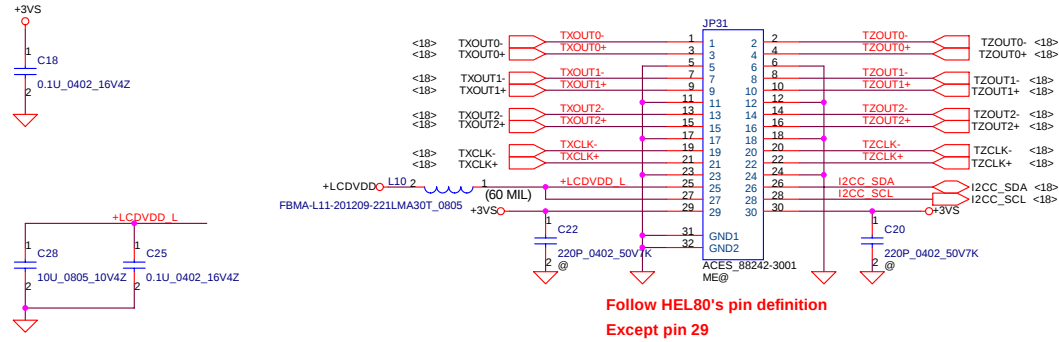


Security Classification		Compal Secret Data		Title	
Issued Date	2005/03/01	Deciphered Date	2006/03/01	Clock Buffer ICS9P935	
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				Date: Thursday, September 06, 2007	Rev 0.1
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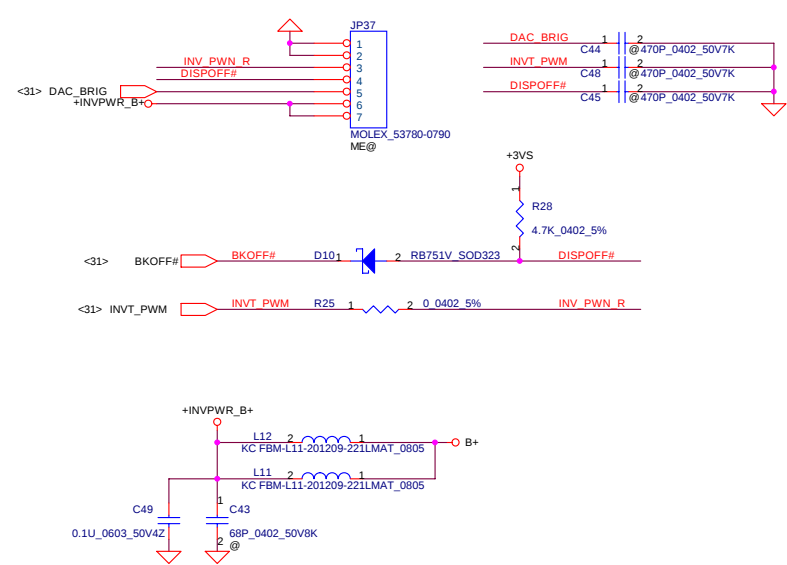
LCD POWER CIRCUIT



LCD/PANEL BD. Conn.

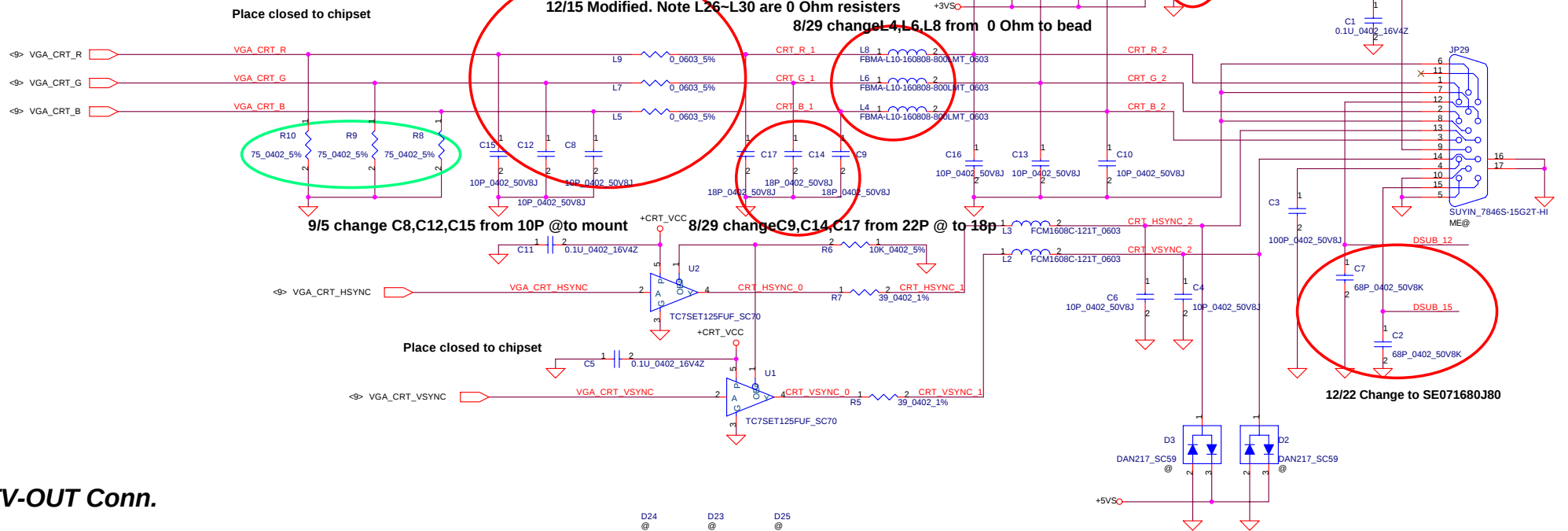


INVERTER Conn.

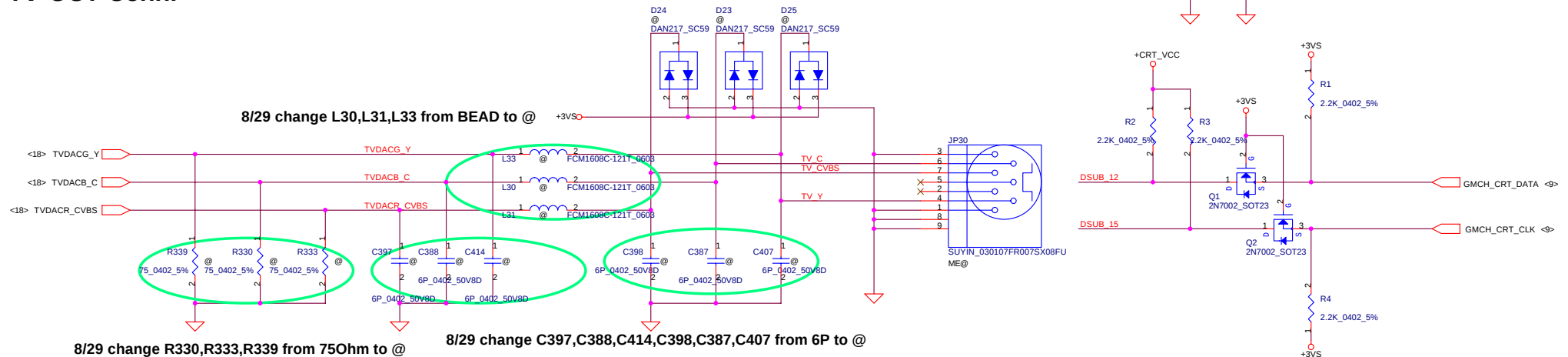


Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title		
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Size B	Document Number	JFWXX M/B LA-3961P Schematic			Rev	0.1
Date:	Thursday, September 06, 2007	Sheet	16	of	49	

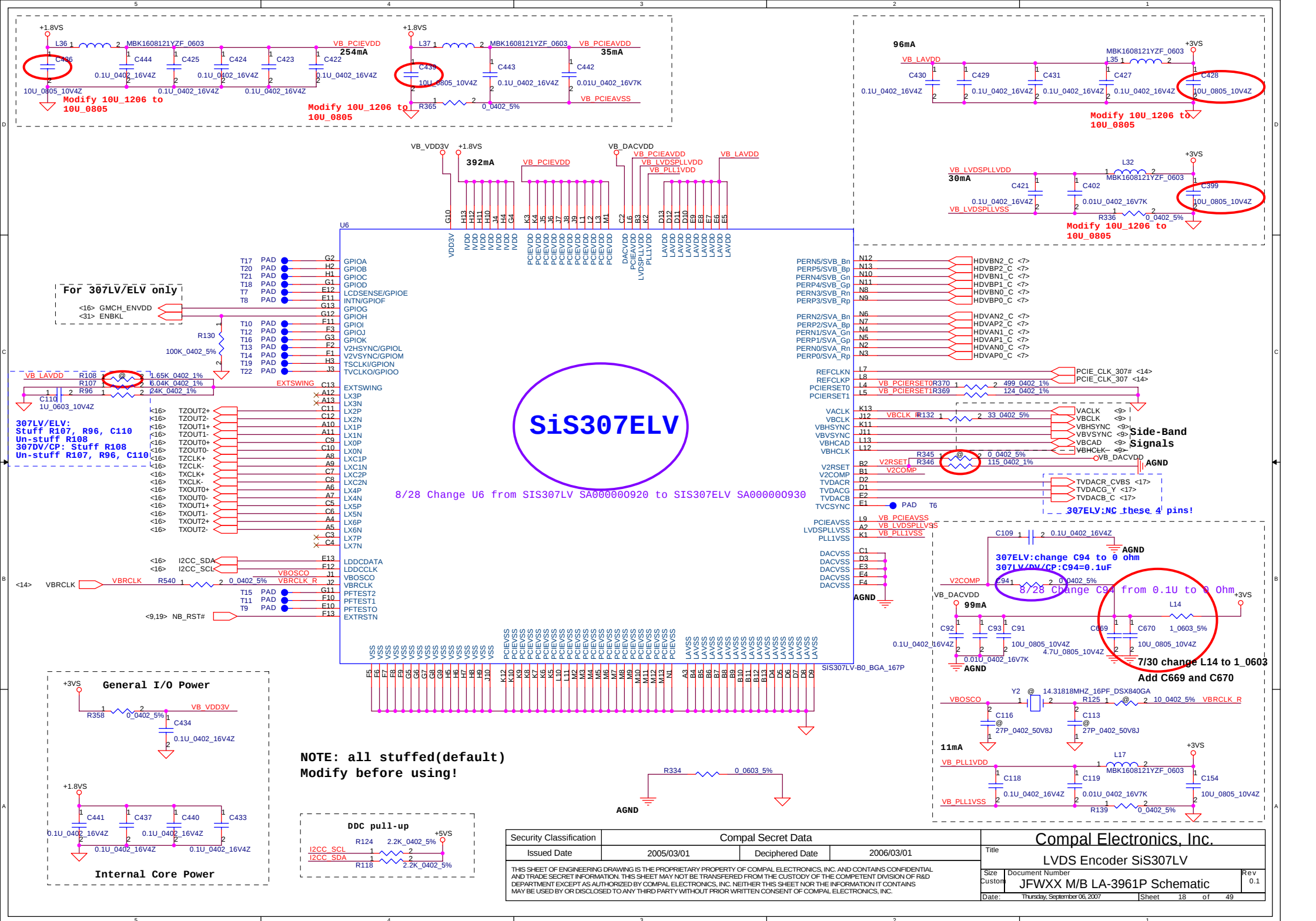
CRT Connector

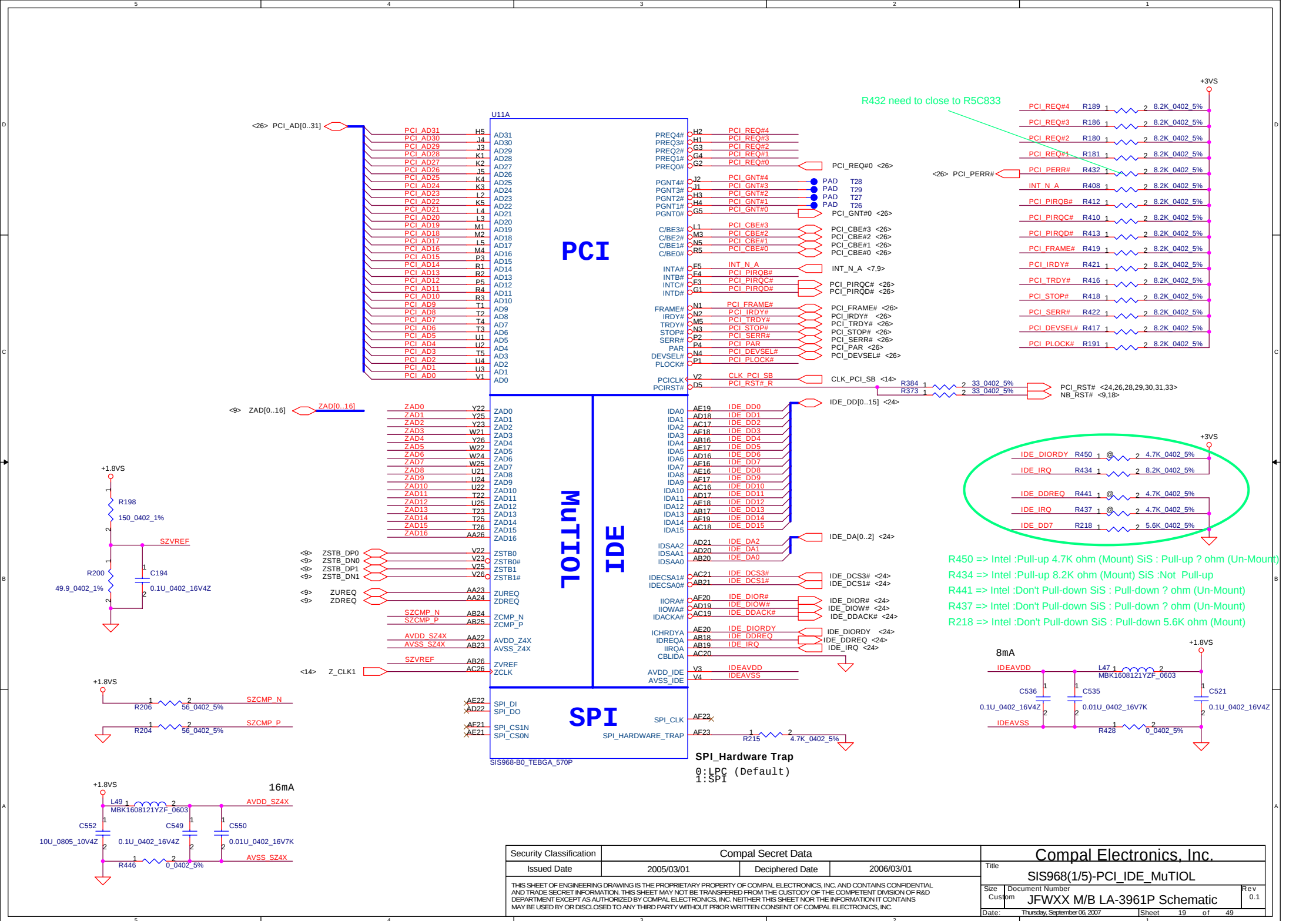


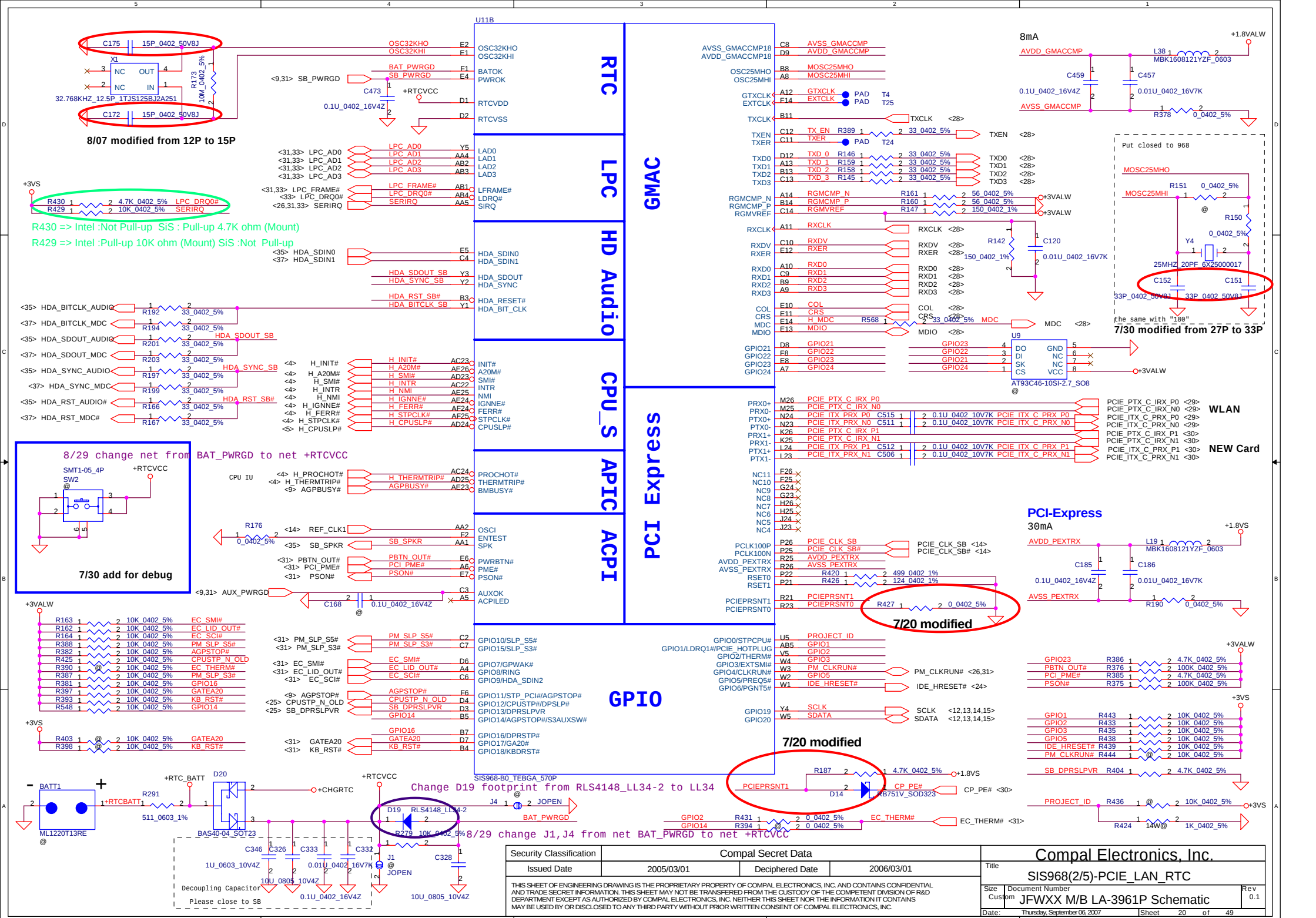
TV-OUT Conn.

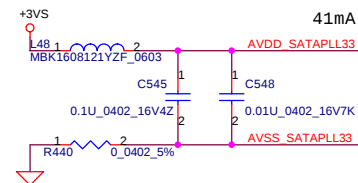


Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2006/08/18				Title			
				Deciphered Date				CMT & TV-OUT Connector			
				2007/8/18				Size B			
								Document Number			
								JFWXX M/B LA-3961P Schematic			
								Rev 0.1			
								Date: Thursday, September 06, 2007			
								Sheet 17 of 49			

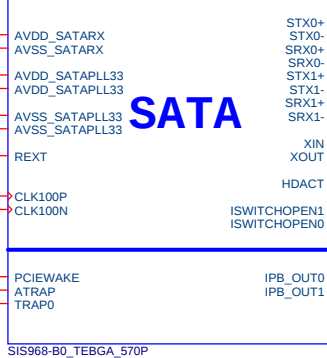
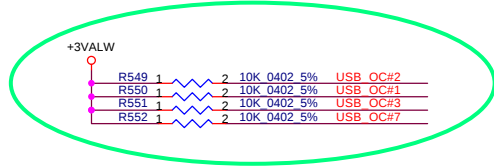




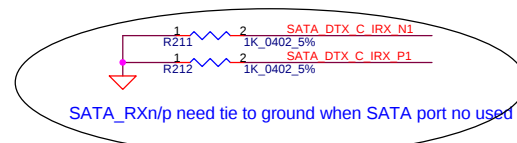




+3VALW
 R549 1 2 10K 0402 5% USB OC#2
 R550 1 2 10K 0402 5% USB OC#1
 R551 1 2 10K 0402 5% USB OC#3
 R552 1 2 10K 0402 5% USB OC#7



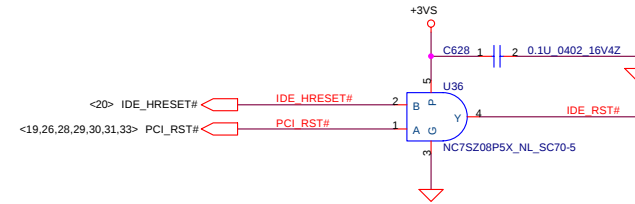
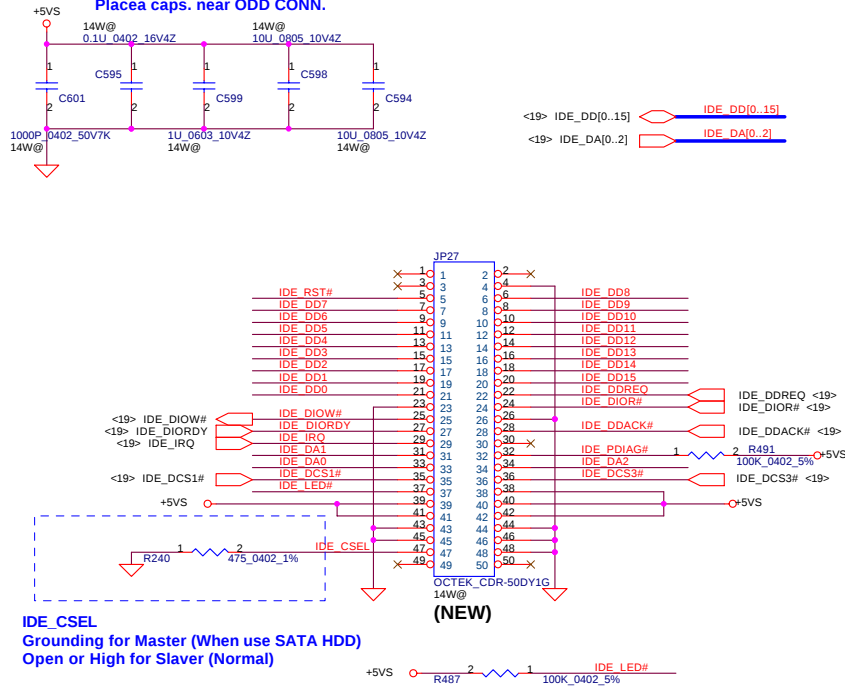
SATA



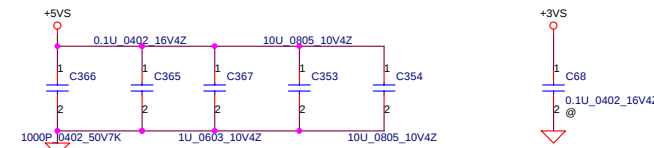
Security Classification		Compal Secret Data		Compal Electronics, Inc. Title SIS968(3/5)-USB_SATA	
Issued Date	2005/03/01	Deciphered Date	2006/03/01	Size	Document Number
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14W ODD Conn.

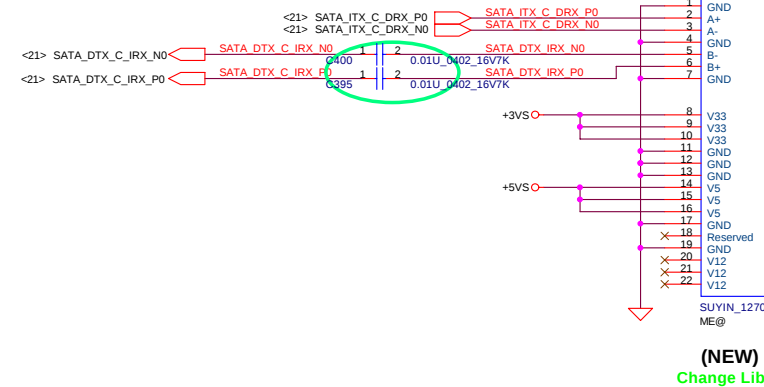
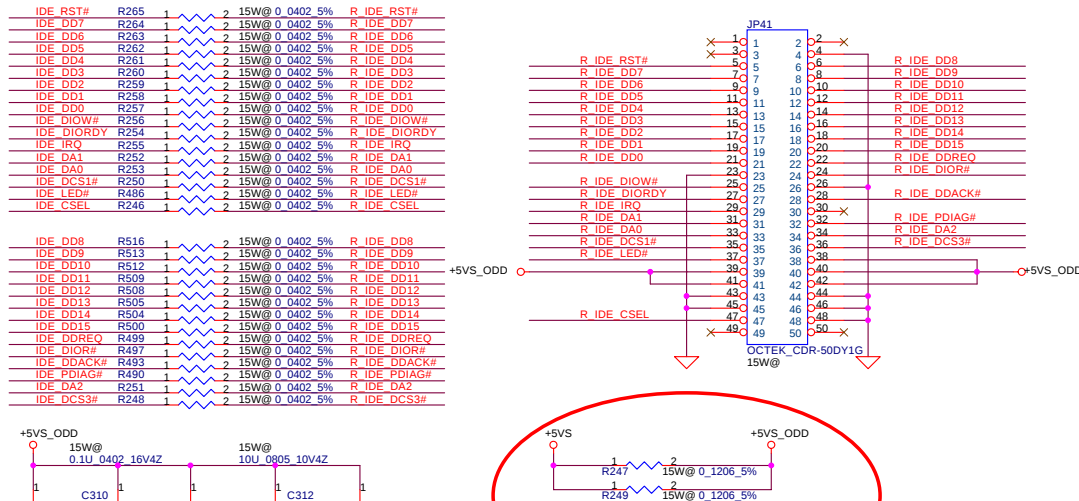
Placea caps. near ODD CONN.



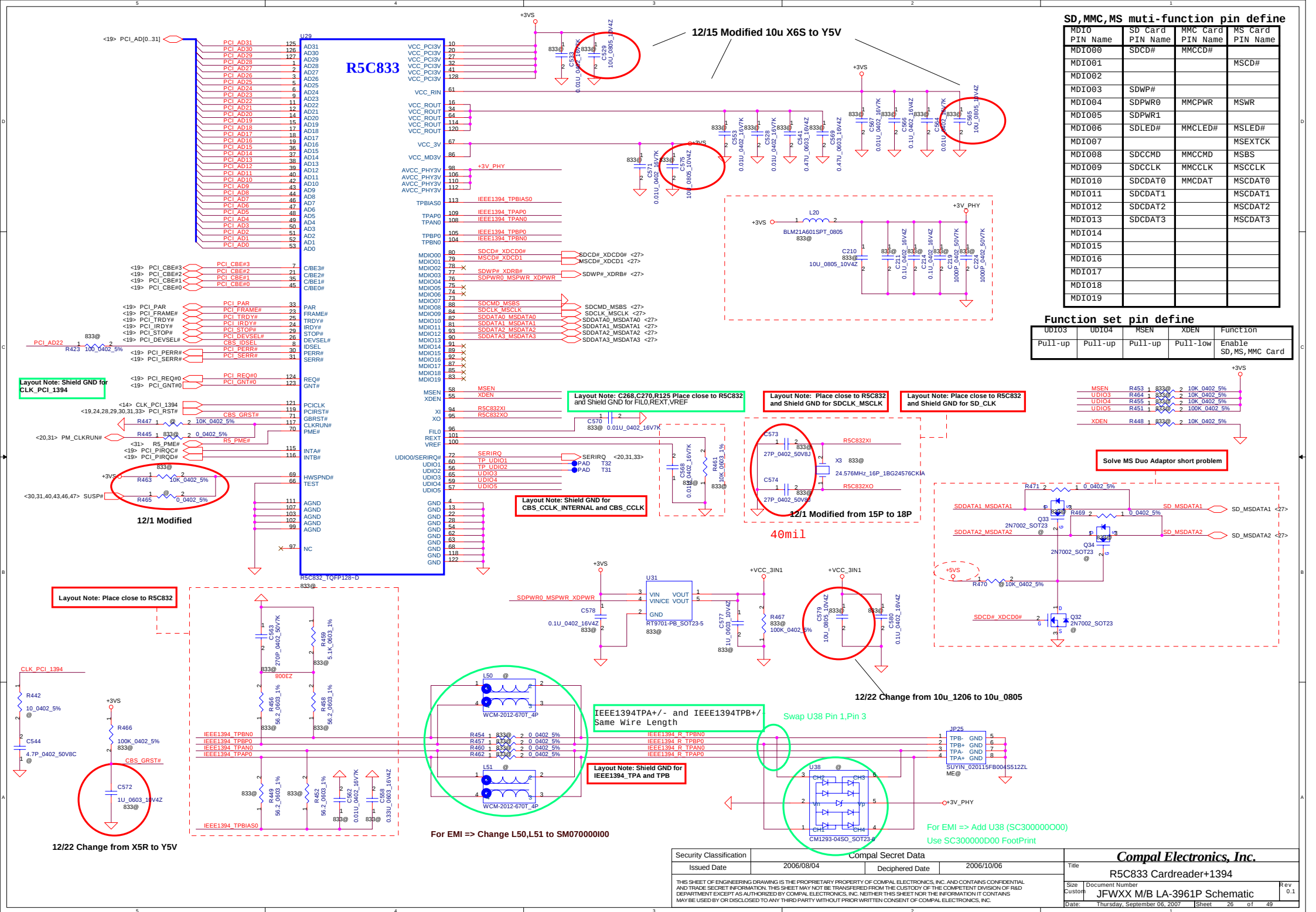
SATA HDD Conn.



15W ODD Conn.

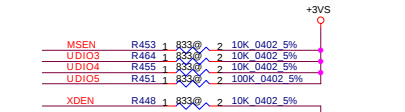


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Issued Date	2006/08/18	Deciphered Date	2007/8/18	HDD & ODD Connector	
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				JFWXX M/B LA-3961P Schematic	
				Date:	Thursday, September 06, 2007
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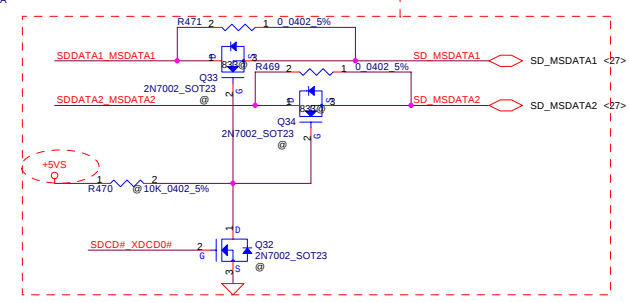


SD, MMC, MS multi-function pin define			
MDIO PIN Name	SD Card PIN Name	MMC Card PIN Name	MS Card PIN Name
MDIO00	SDCD#	MMCD#	MSCD#
MDIO01			
MDIO02			
MDIO03	SDWP#		
MDIO04	SDPWR0	MMCPWR	MSWR
MDIO05	SDPWR1		
MDIO06	SDLED#	MMCLD#	MSLED#
MDIO07			
MDIO08	SDCCMD	MMCCMD	MSBS
MDIO09	SDCLK	MMCLK	MSCCLK
MDIO10	SDCDAT0	MMCDAT	MSCDAT0
MDIO11	SDCDAT1		MSCDAT1
MDIO12	SDCDAT2		MSCDAT2
MDIO13	SDCDAT3		MSCDAT3
MDIO14			
MDIO15			
MDIO16			
MDIO17			
MDIO18			
MDIO19			

Function set pin define				
UDIO3	UDIO4	MSEN	XDEN	Function
Pull-up	Pull-up	Pull-up	Pull-low	Enable SD, MS, MMC Card



Solve MS Duo Adaptor short problem



12/22 Change from 10u_1206 to 10u_0805

Swap U38 Pin 1, Pin 3

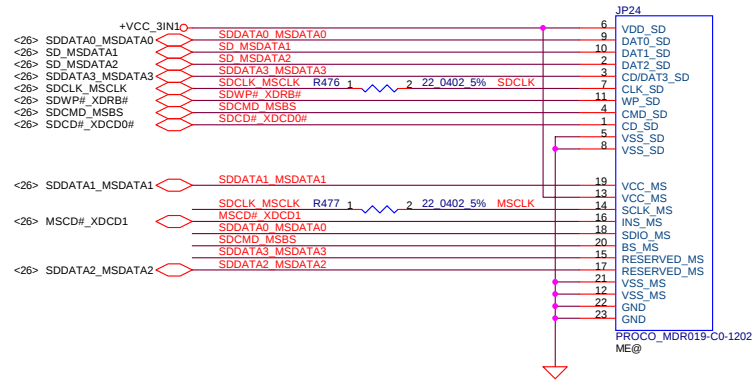
IEEE1394TPA+/- and IEEE1394TPB+/- Same Wire Length

Layout Note: Shield GND for IEEE1394_TPA and TPB

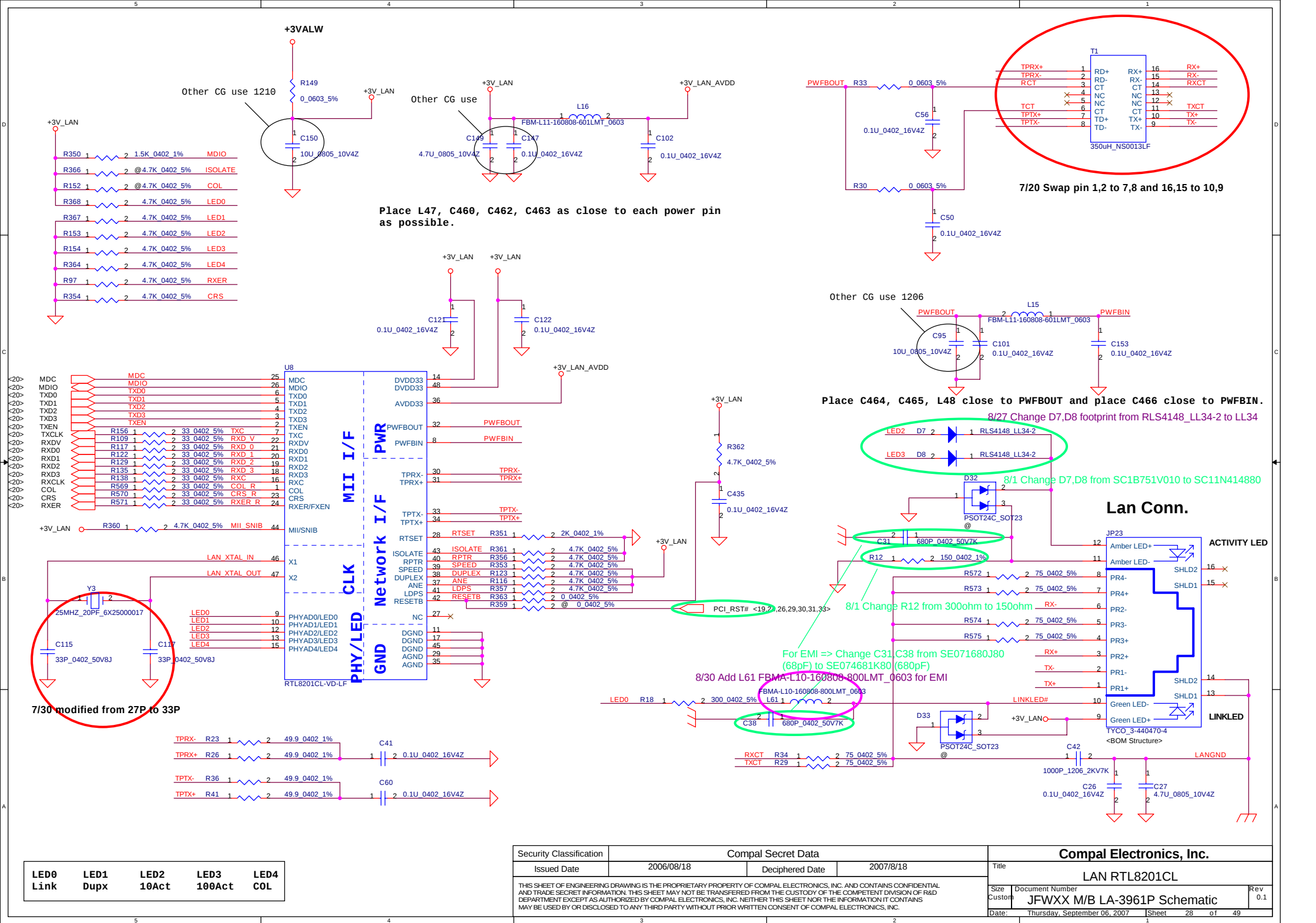
For EMI => Change L50, L51 to SM070000000

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Title			
R5C833 Cardreader+1394			
Size	Document Number	Rev	
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3 in 1 Card Reader

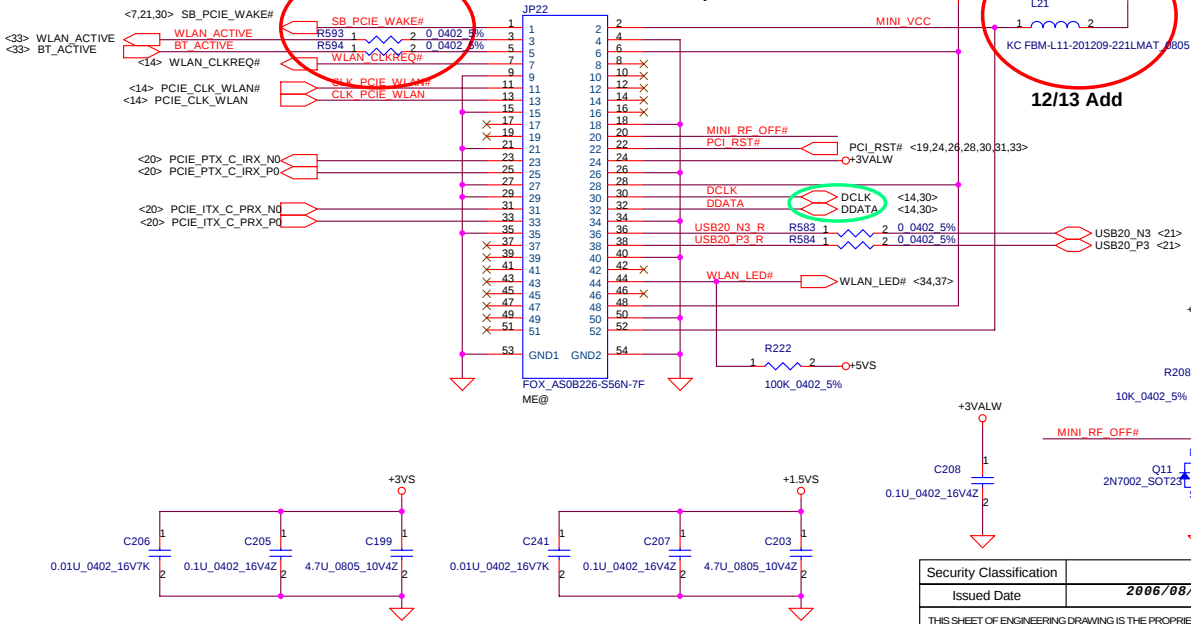


Security Classification		Compal Secret Data		Title	
Issued Date	2006/08/04	Deciphered Date	2006/10/06	3 IN 1 CardReader Conn.	
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				Custom	JFWXX M/B LA-3961P Schematic
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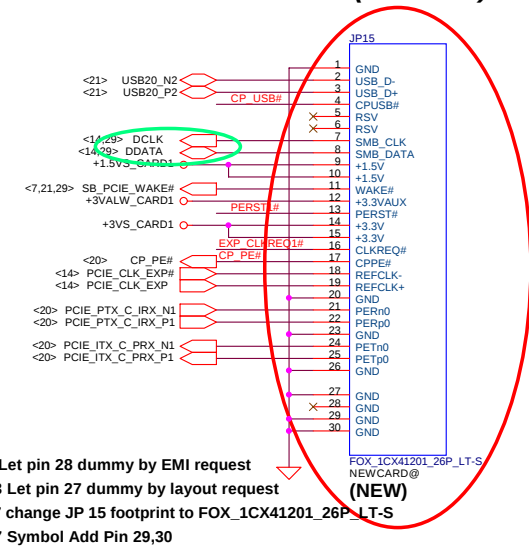
Mini-Express Card for WLAN

8/31 Add R593 connect net WLAN_ACTIVE to JP22 pin3
8/31 Add R594 connect net BT_ACTIVE to JP22 pin5



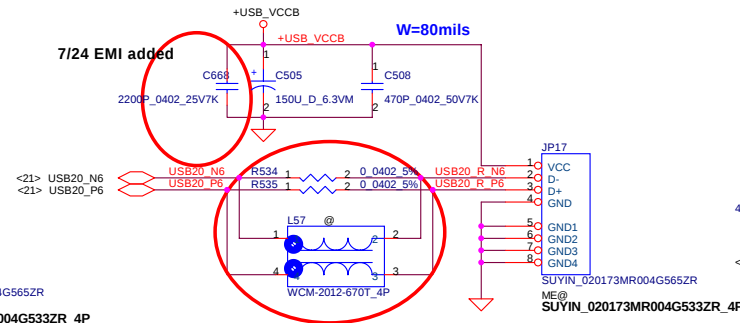
Security Classification		Compal Secret Data		Title	
Issued Date		2006/08/05		Deciphered Date	
		2007/08/05		Size	
				Document Number	
				JFWXX M/B LA-3961P Schematic	
				Rev	
				0.1	
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New Card Socket (Left/TOP)

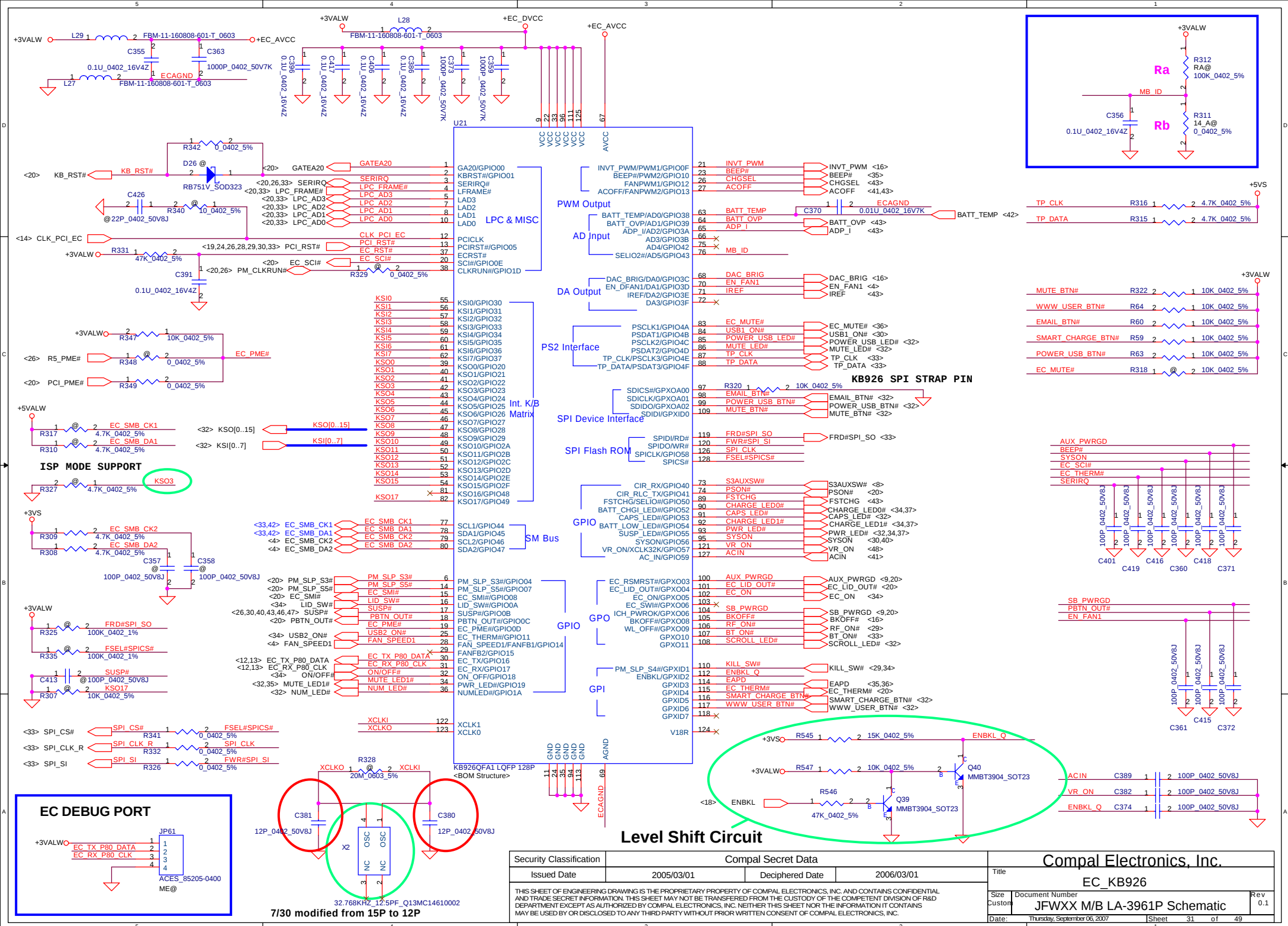


04/17 Symbol Add Pin 29,30

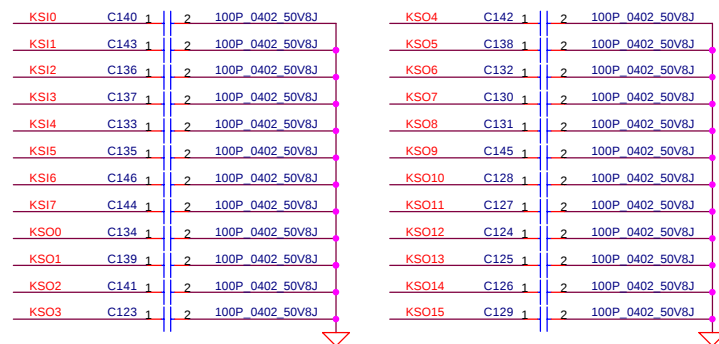
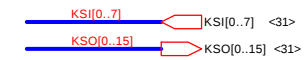
USB CONN. 2



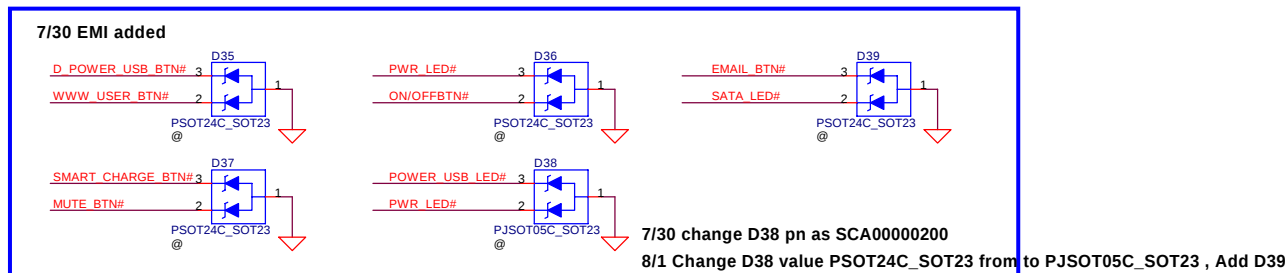
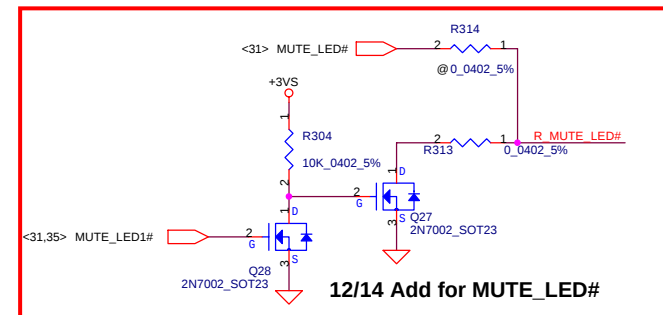
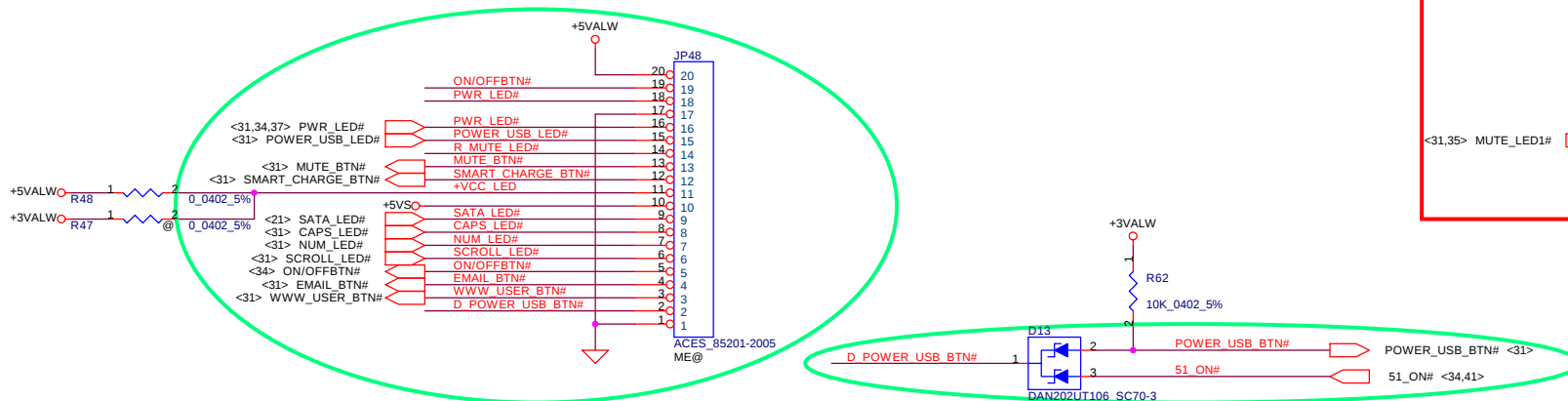
Security Classification		Compal Secret Data		Compal Electronics, Inc.			
Issued Date		2006/08/18		Deciphered Date		2007/8/18	
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				NewCard & USB Connector			
				Size B	Document Number		
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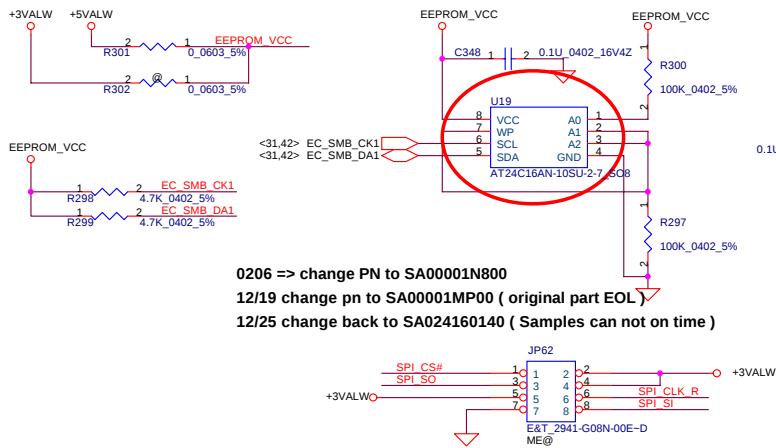
INT KBD Conn.



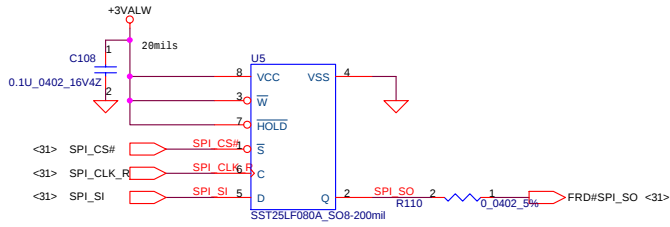
Switch Board Conn.



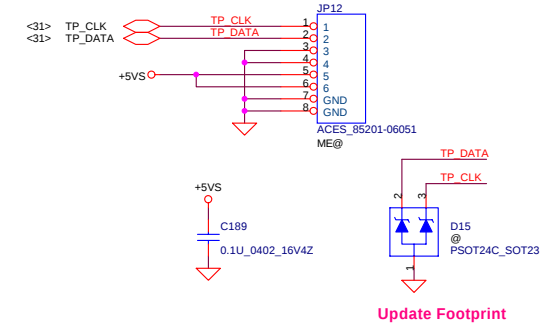
Security Classification		Compal Secret Data		Compal Electronics, Inc.			
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title KB /SW Conn.			
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				B		JFWXX M/B LA-3961P Schematic	0.1
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8M SPI ROM



To TP/B Conn.

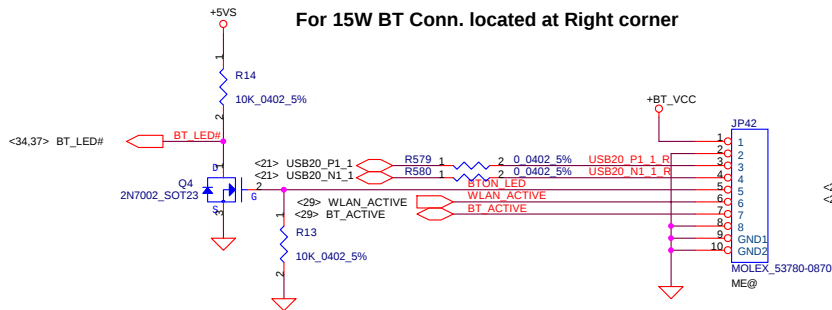


Bluetooth Conn.

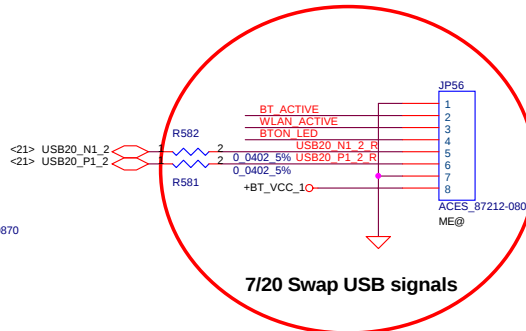
Need to check BT pin definition again!

9/20 modified this block

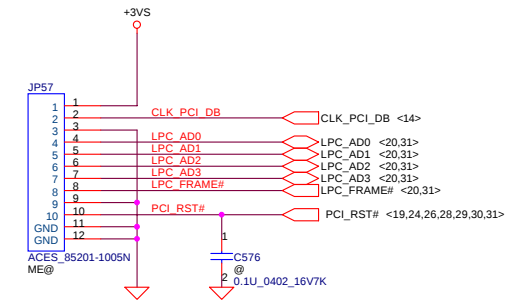
For 15W BT Conn. located at Right corner



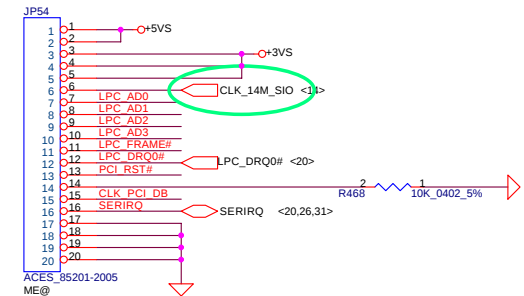
For 14W BT Conn. located at Left corner



FOR LPC DEBUG PORT

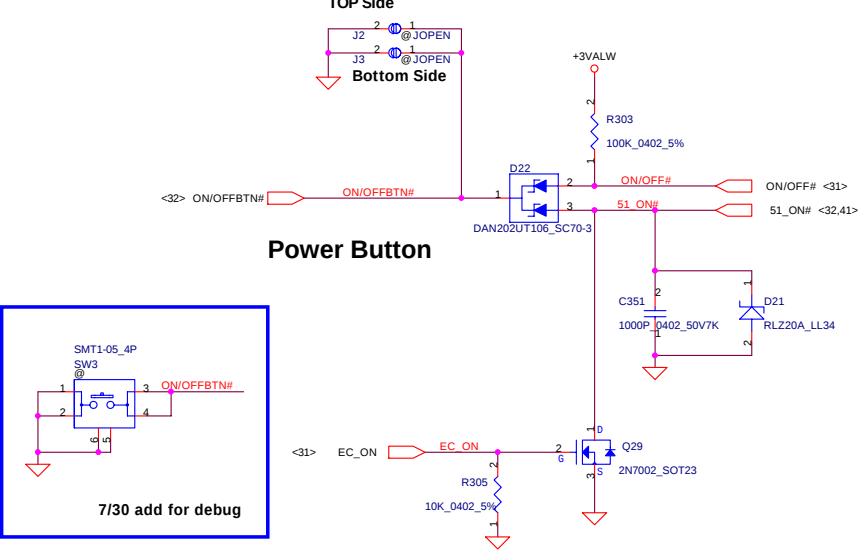


FOR LPC SIO DEBUG PORT

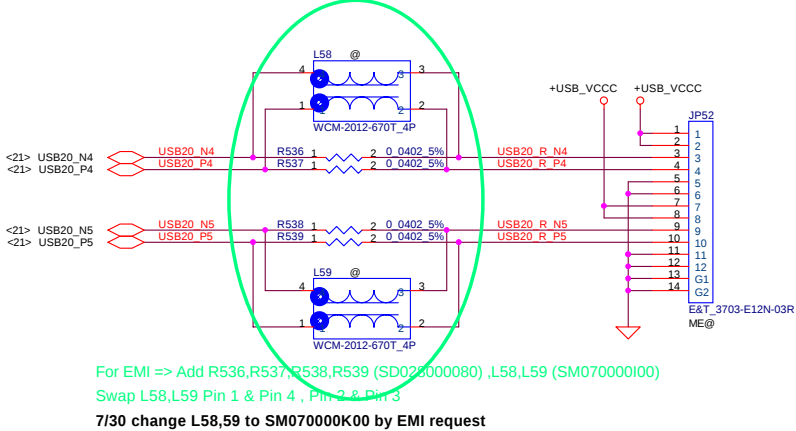


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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title		
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Size	B	Document Number	JFWXX M/B LA-3961P Schematic	Rev	0.1	
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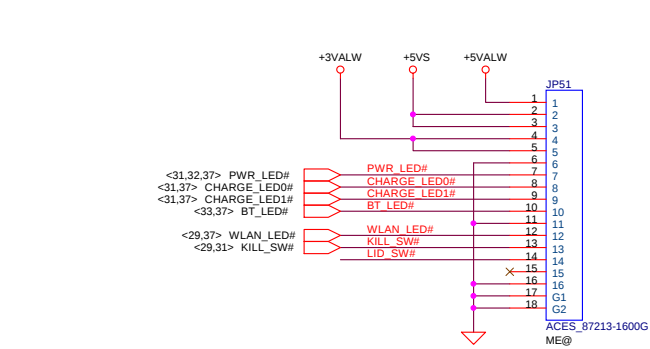
ON/OFF switch



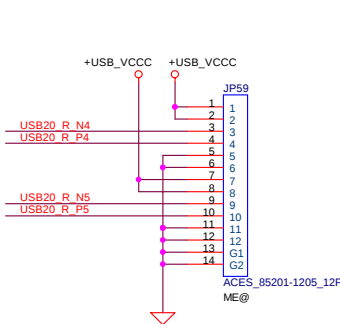
For JFW01 IO Conn.



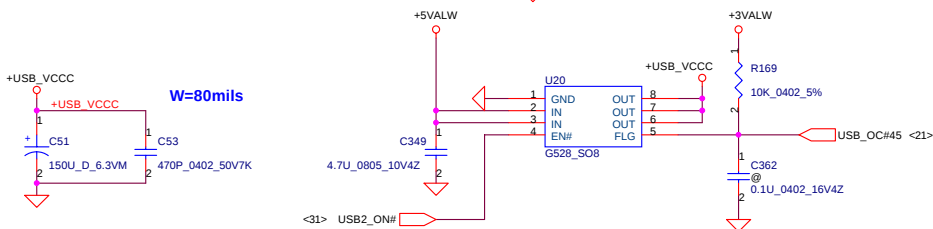
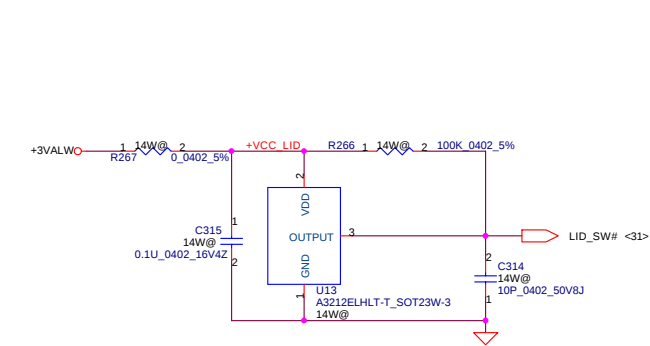
Front LED Board



For JFW91 IO Conn.

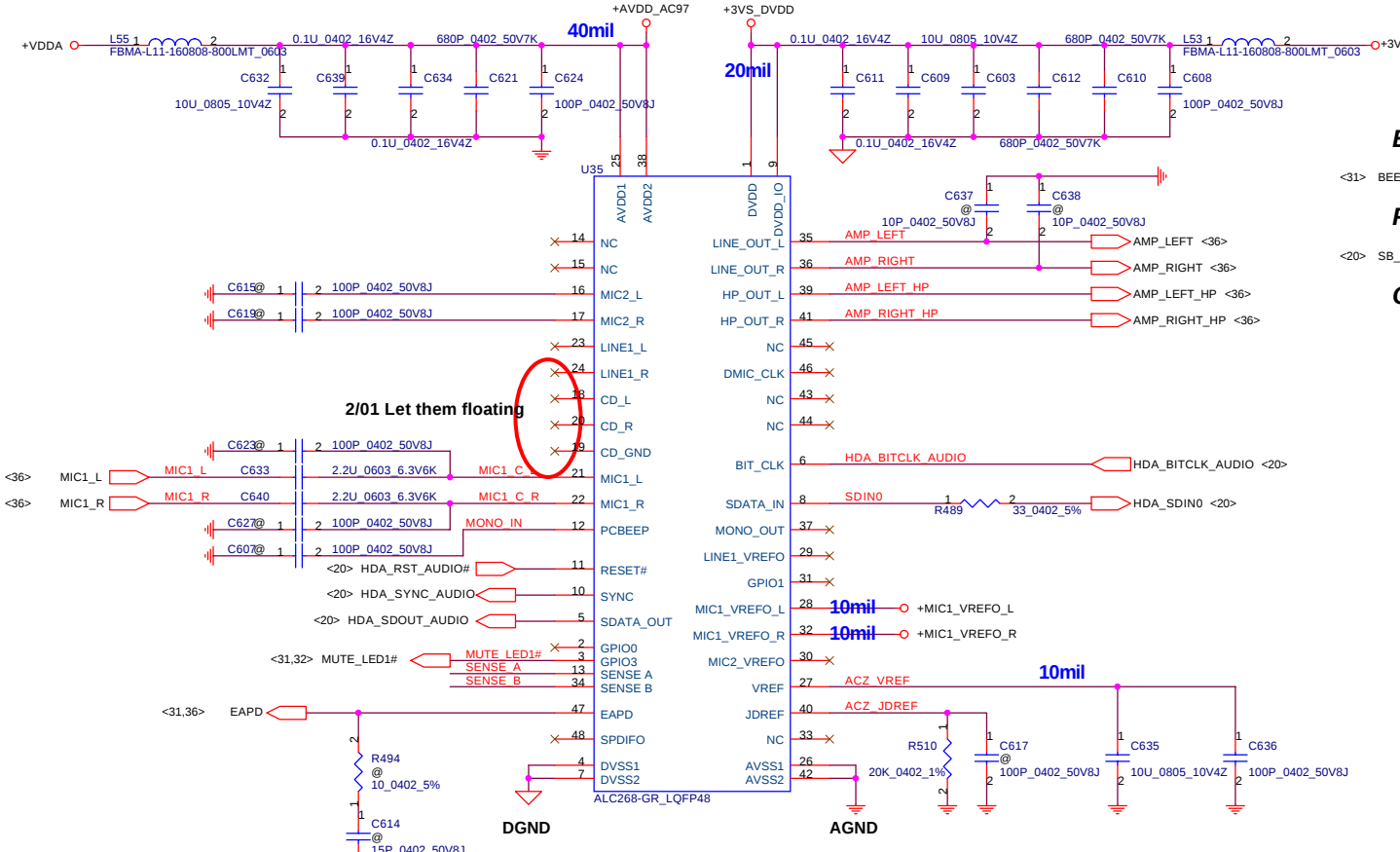


Lid Switch



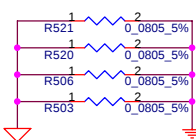
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2006/08/18				Deciphered Date			
2007/8/18				Title				PWROK/LID/Front/IO Board			
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HD Audio Codec



Sense Pin	Impedance	Codec Signals	Funncion
SENSE A / B	39.2K	PORT-A (PIN 39, 41)	HP
	20K	PORT-B (PIN 21, 22)	MIC
	10K	PORT-C (PIN 23, 24)	LINE IN
SENSE B	5.1K	PORT-D (PIN 35, 36)	LINE Out
	39.2K	PORT-E (PIN 14, 15)	HP
	20K	PORT-F (PIN 16, 17)	MIC
	10K	PORT-G (PIN 43, 44)	LINE IN
	5.1K	PORT-H (PIN 45, 46)	LINE Out

Moat Bridge

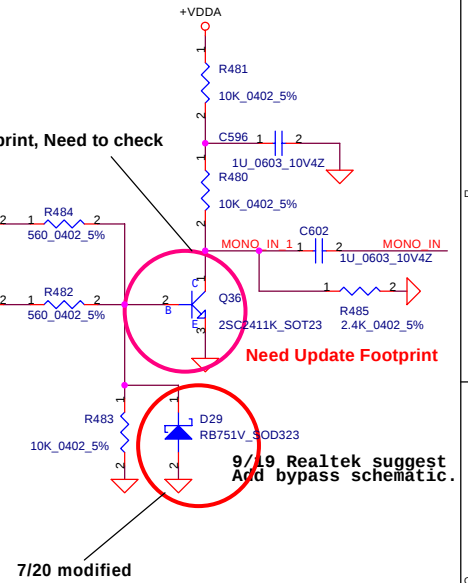


9/22 Update footprint, Need to check

EC Bleep

PCI Bleep

CardBus Bleep

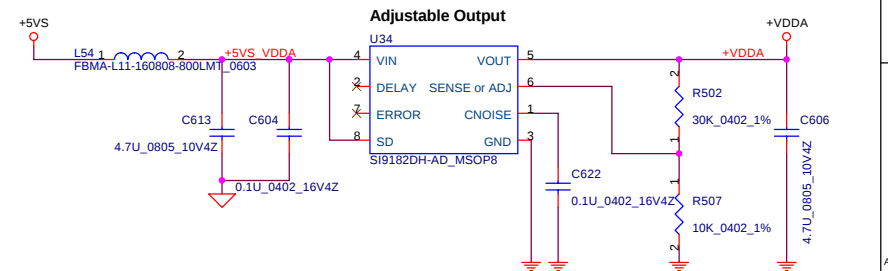


Need Update Footprint

9/19 Realtek suggest And bypass schematic.

7/20 modified

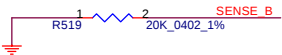
Regulator for CODEC



SENSE FOR Ext. Mic.



SENSE FOR Solo Int. Mic.



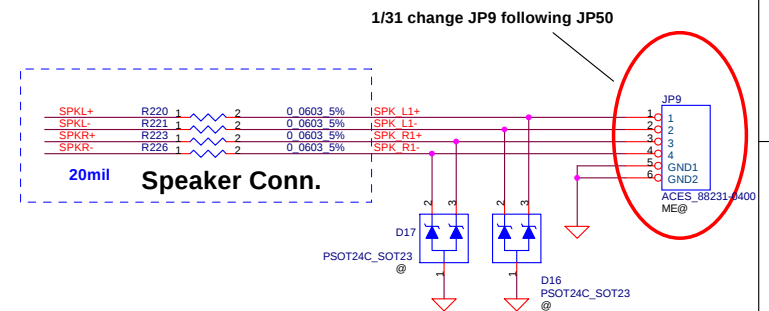
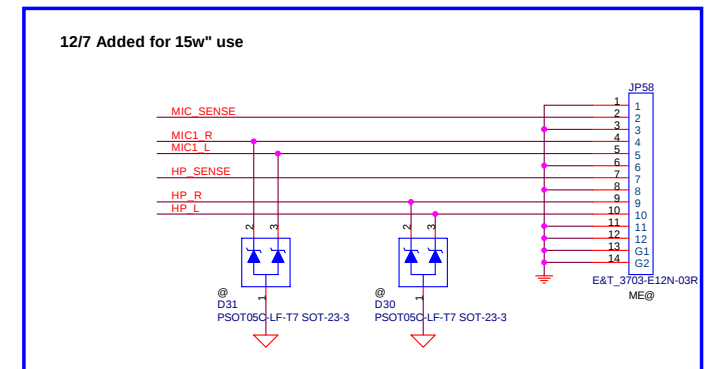
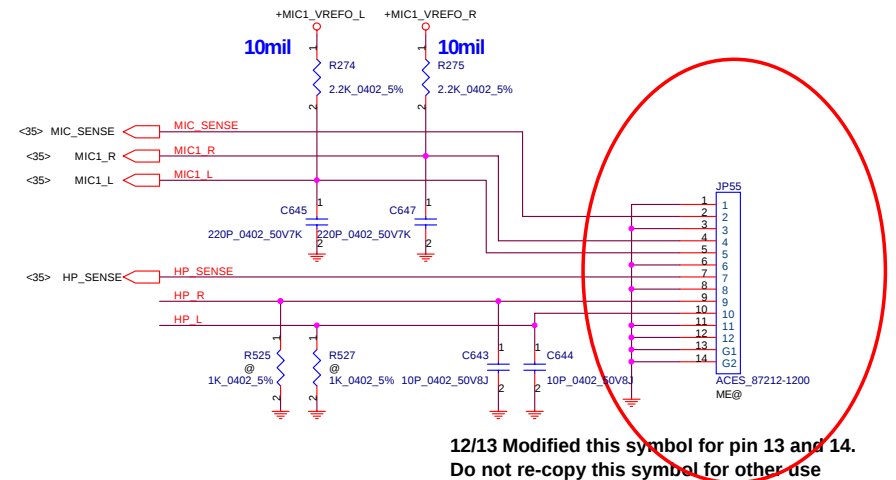
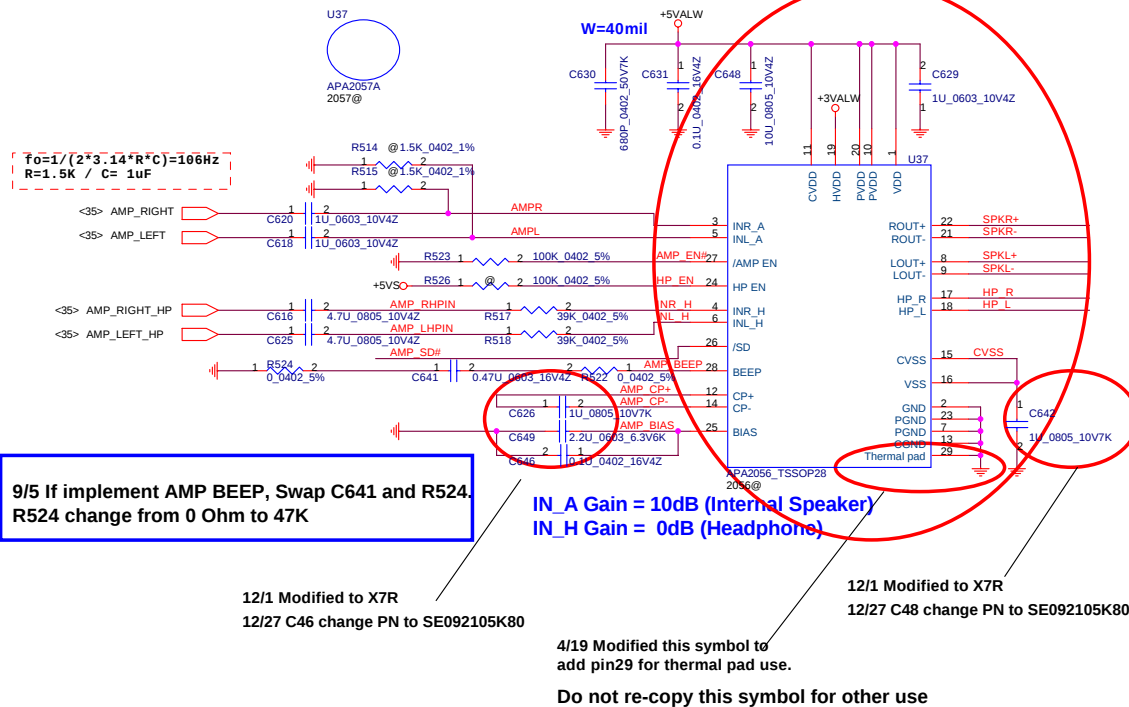
SENSE FOR HP



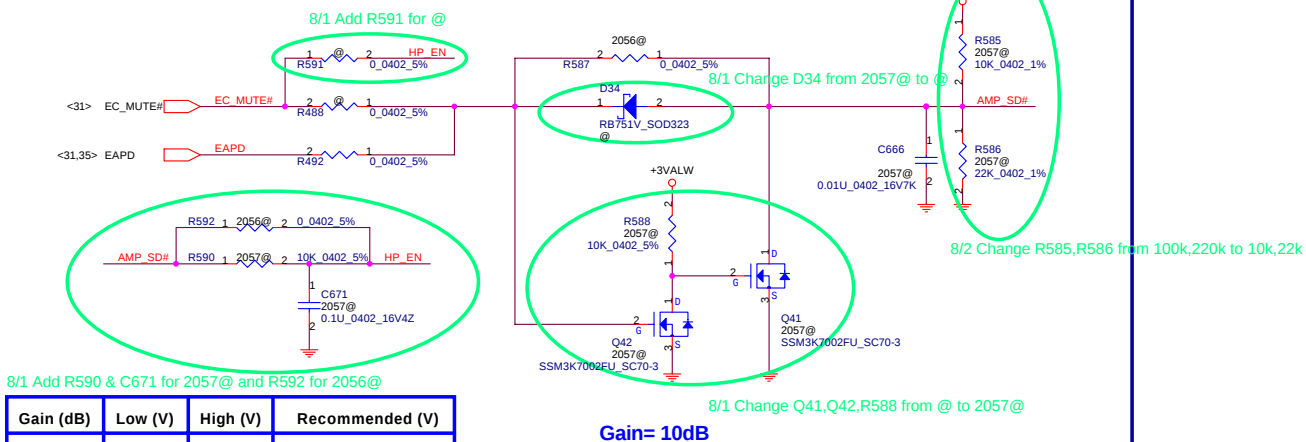
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APA2056 SPK/HP Amplifier

7/20 Add U37 for APA2057A SA00001QD00



7/20 Add below circuit for APA2057 gain tuning use



Gain (dB)	Low (V)	High (V)	Recommended (V)
10	3.45	3.51	3.48
11	3.56	3.62	3.59
12	3.68	3.73	3.70
13	3.80	3.85	3.82
15	4.02	4.07	4.05

+5VALW assume equal 5.1V
10 dB ---> $5.1 \times 220 / 320 = 3.5$

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[illegible]

9/3 change R531,C30,R191,R201,R578 from CAM@ to mount

For EMI => Add L60 (SM070000I00)

7/30 change L60 to SM070000K00 by EMI request

For EMI => Change D9 from SC300000100 to SC300000P00

LED1

R269 14W@
4.3K_0402_5%

+5VALW 1 2

HT-191NB_LED0603
14W@

PWR_LED# <31,32,34>

LED3

R272 14W@
3.3K_0402_5%

+5VALW 1 2

HT-297UD/CB_LED3/AMB0603
14W@

Amber 3

Blue 1

CHARGE_LED0# <31,34>

CHARGE_LED1# <31,34>

Blue&Amber

LED2

R270 14W@
3.3K_0402_5%

+5VS 1 2

HT-297UD/CB_LED2/AMB0603
14W@

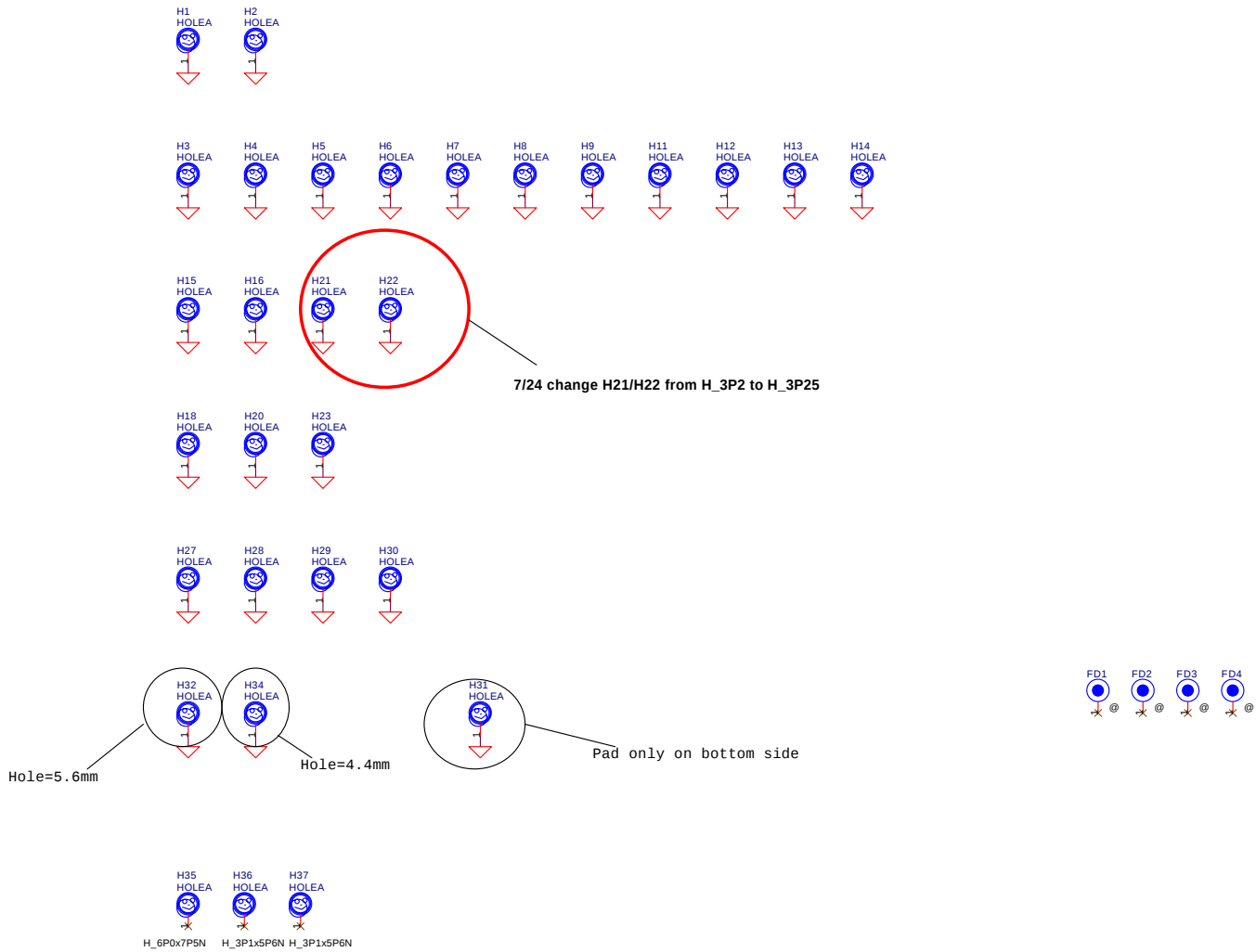
Amber 3

Blue 1

BT_LED# <33,34>

WLAN_LED# <29,34>

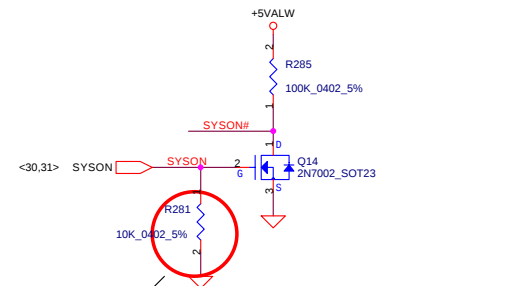
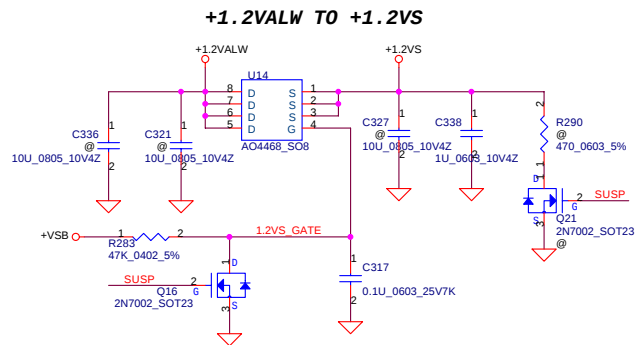
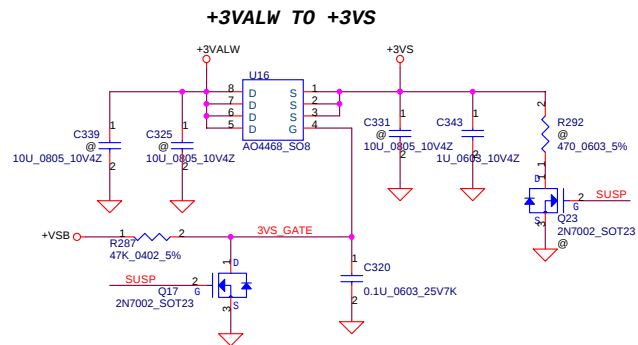
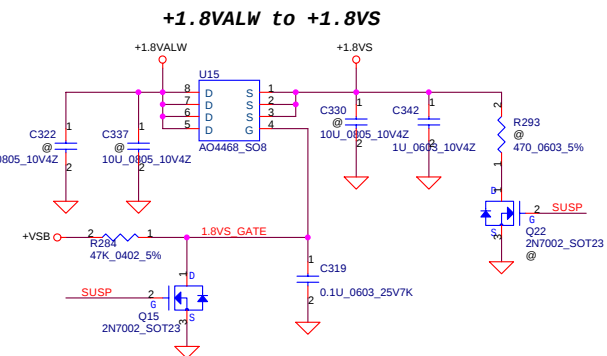
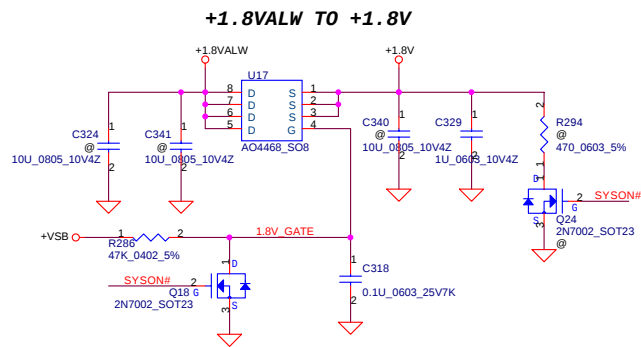
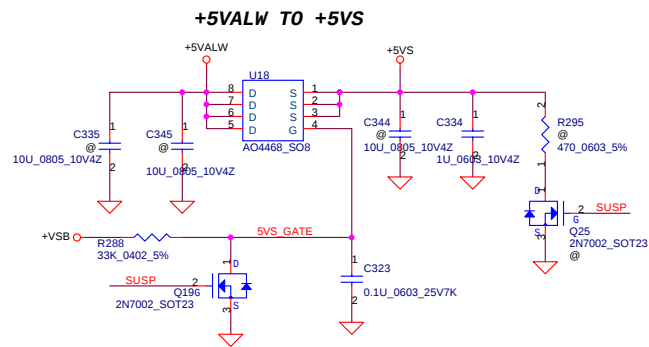
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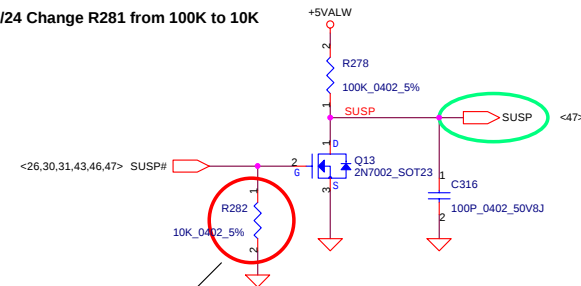
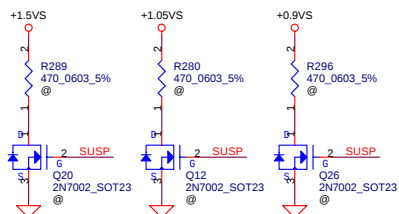
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7/24 Change R281 from 100K to 10K



3/14 Change R16 from 100K to 10K

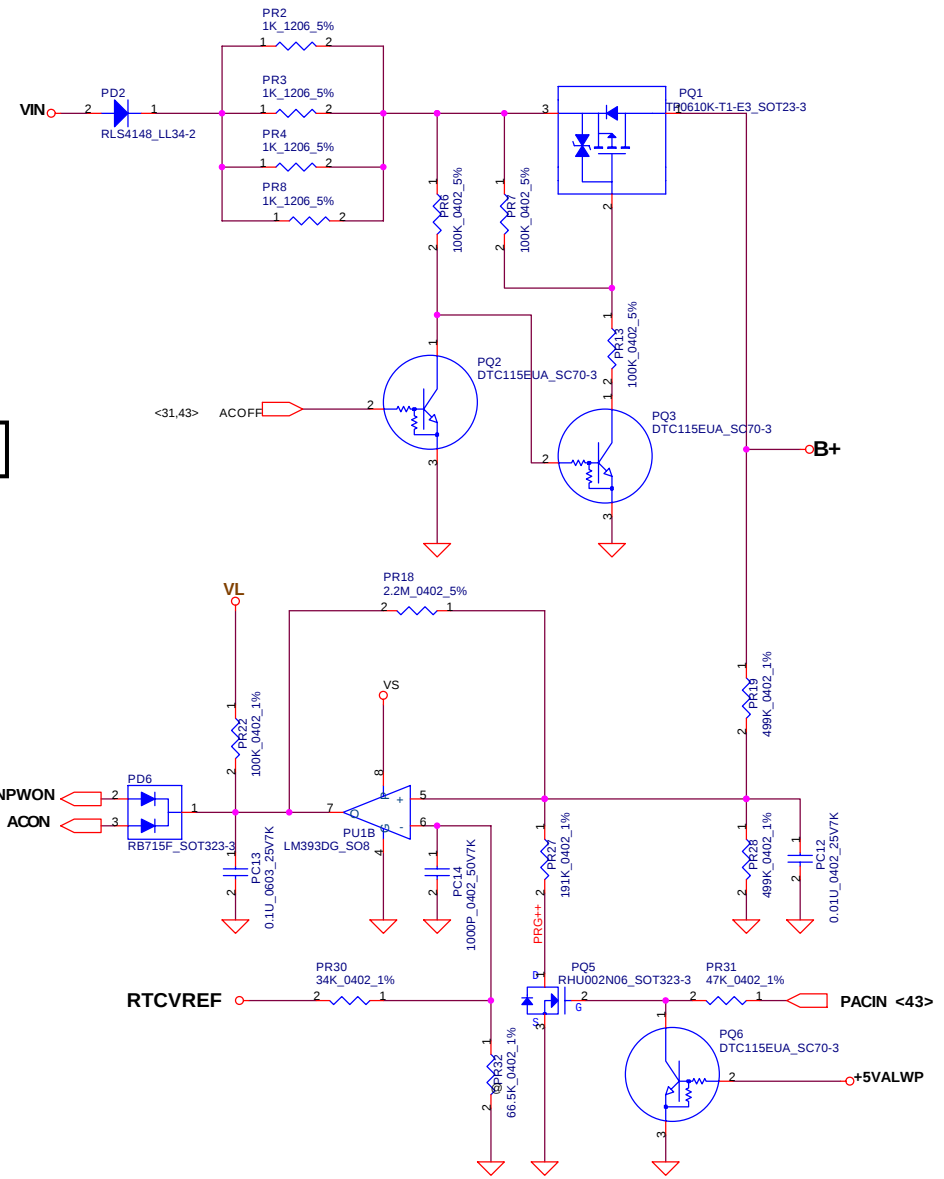
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Vin Detector
High 18.764
Low 17.745

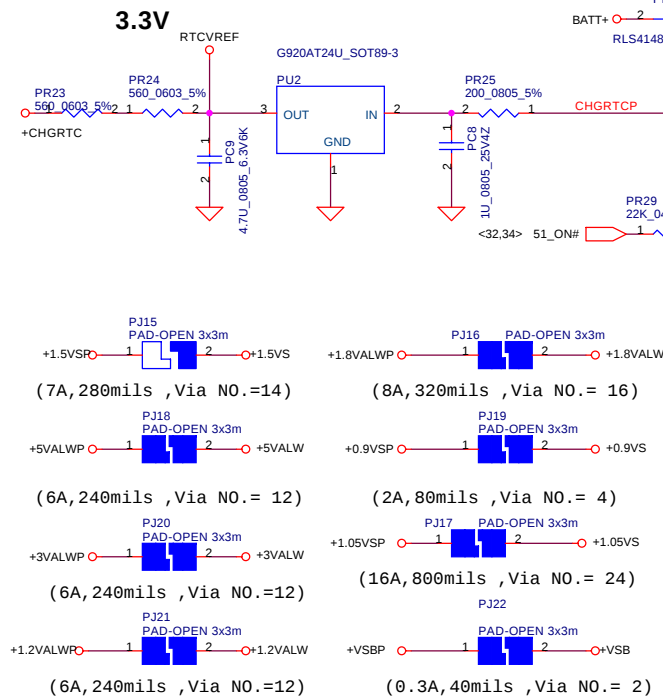
High	18.764	17.901	17.063
Low	17.745	16.9	16.03

	Precharge detector		
	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

	Precharge detector		
	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

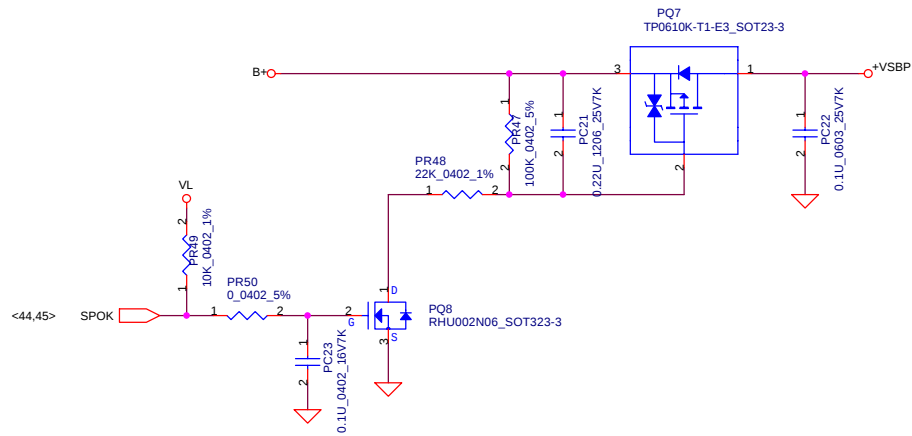
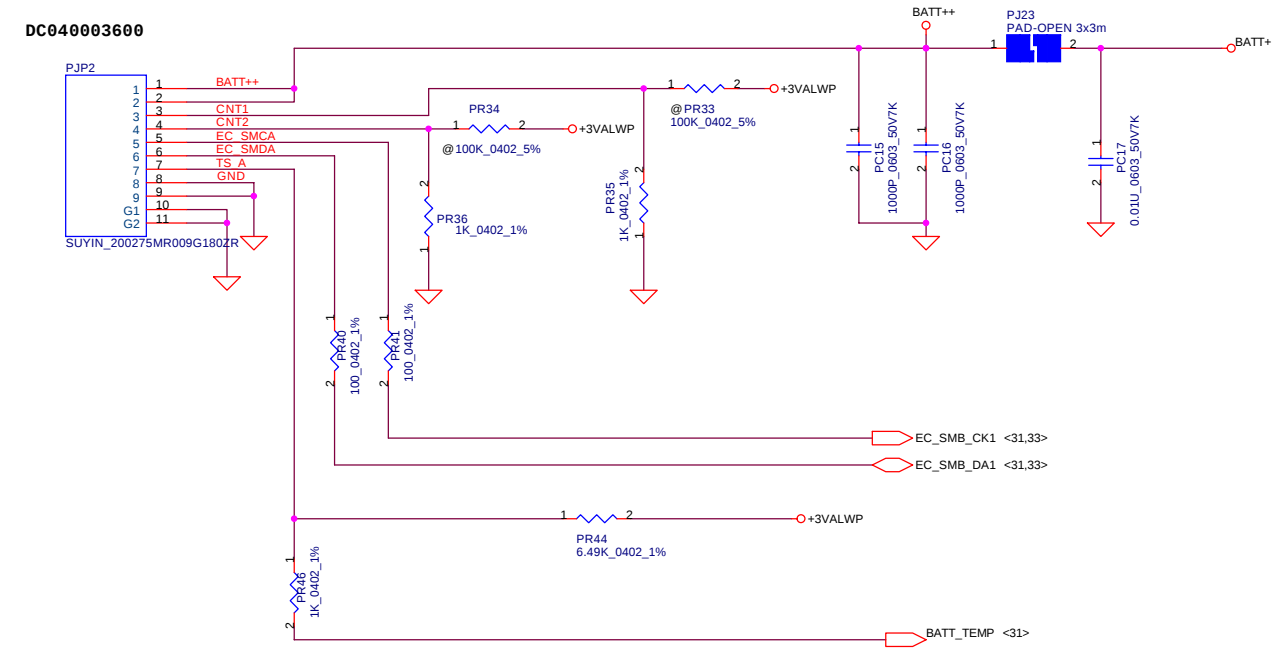


PACIN <43>



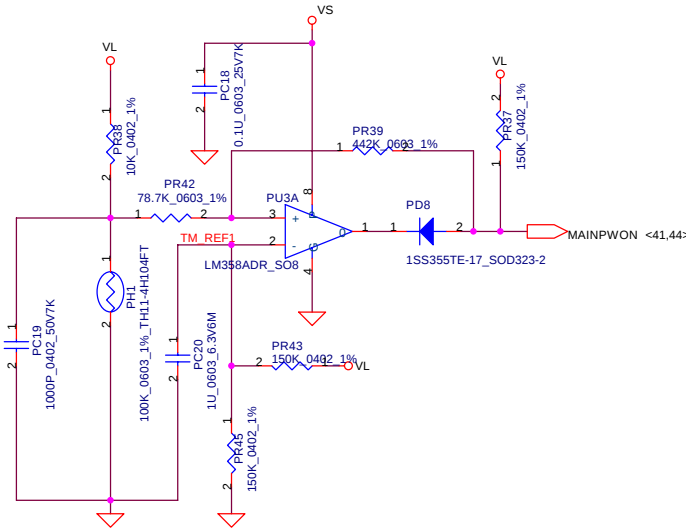
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DC040003600



2/16 Change to 89 degree C for thermal request

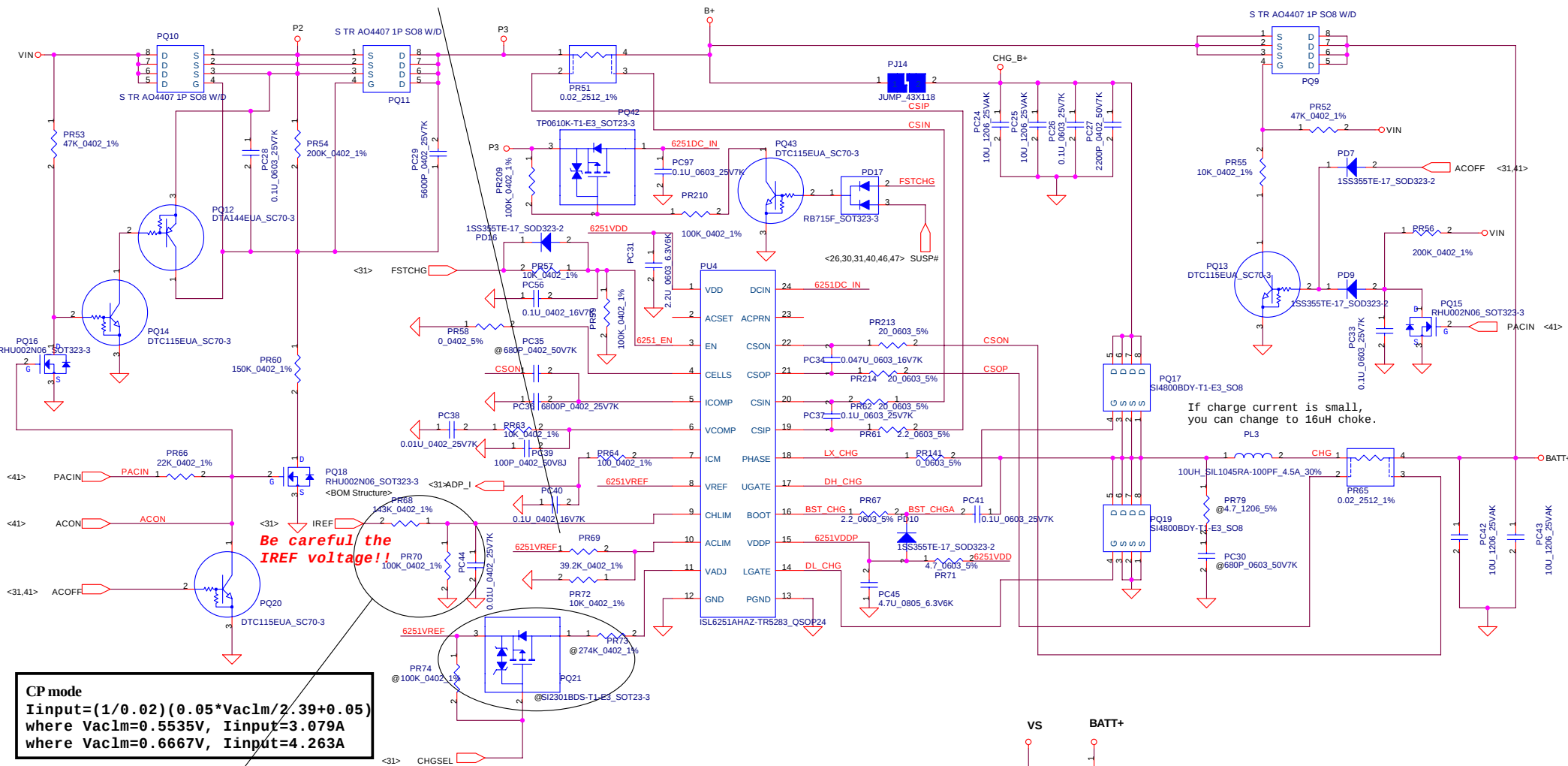
PH1 under CPU botten side :
CPU thermal protection at 85 degree C
Recovery at 70 degree C



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65W, Iadapter=0~3.42A, Current sense=0.02ohm, PR74=39.2K, CP=3.079A

ADP_I = 19.9*Iadapter*Rsense



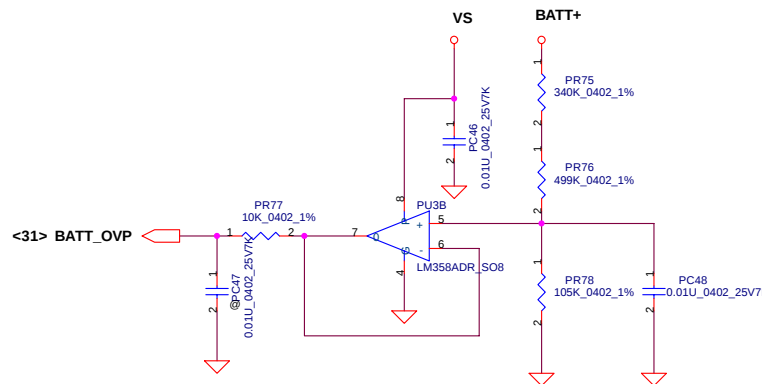
Be careful the IREF voltage!!

CP mode
 $I_{input} = (1/0.02)(0.05 \cdot V_{ac1m}/2.39 + 0.05)$
 where $V_{ac1m} = 0.5535V$, $I_{input} = 3.079A$
 where $V_{ac1m} = 0.6667V$, $I_{input} = 4.263A$

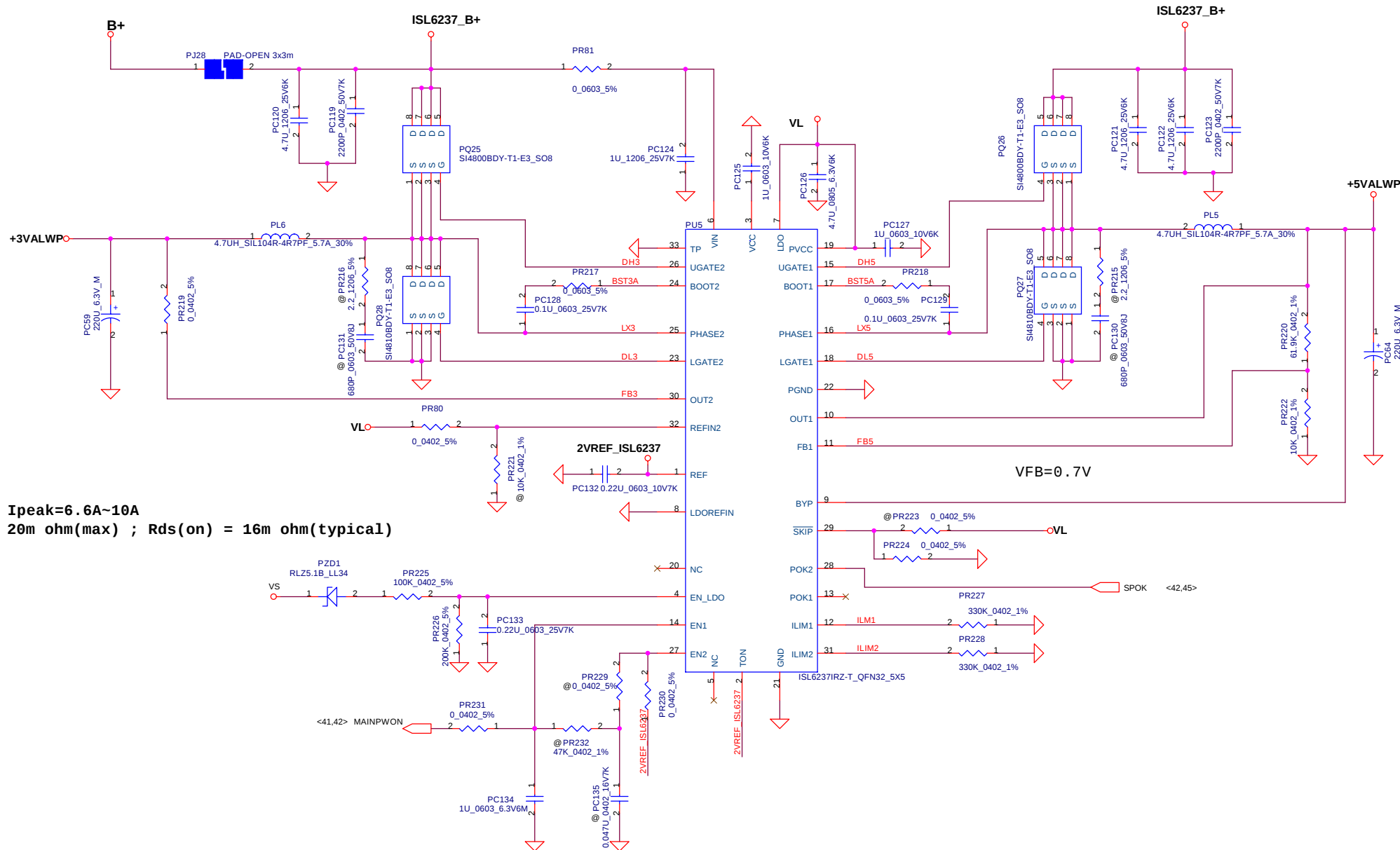
CC=0.6~3.4A
 $V_{CHLM} = 0.24V \sim 1.36V$
 $I_{REF} = 0.972 \cdot I_{charge}$
 $I_{REF} = 0.5832V \sim 3.3V$

If this area float, Charge voltage is 4.2V/cell

BATT Type	Charging Voltage (0x15)	CHGSEL	CV mode
2800mAH 3S pack	13050mV	LOW	12.90V
Normal 3S LI-ON Cells	12600mV	HIGH	12.60V



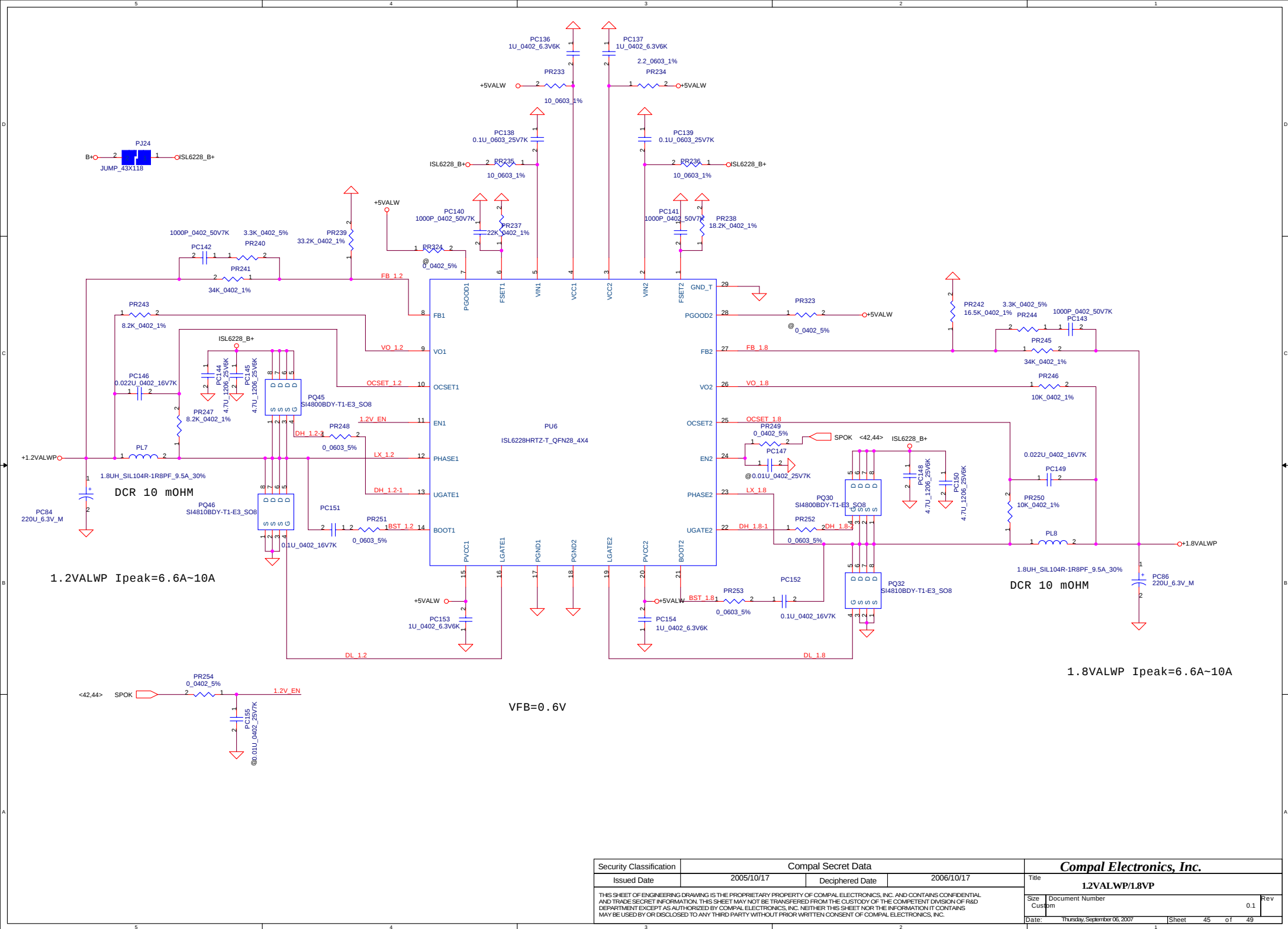
OVP voltage :
 LI-3S : 13.50V -- BATT-OVP=1.5V
 BATT-OVP=0.111*BATT+

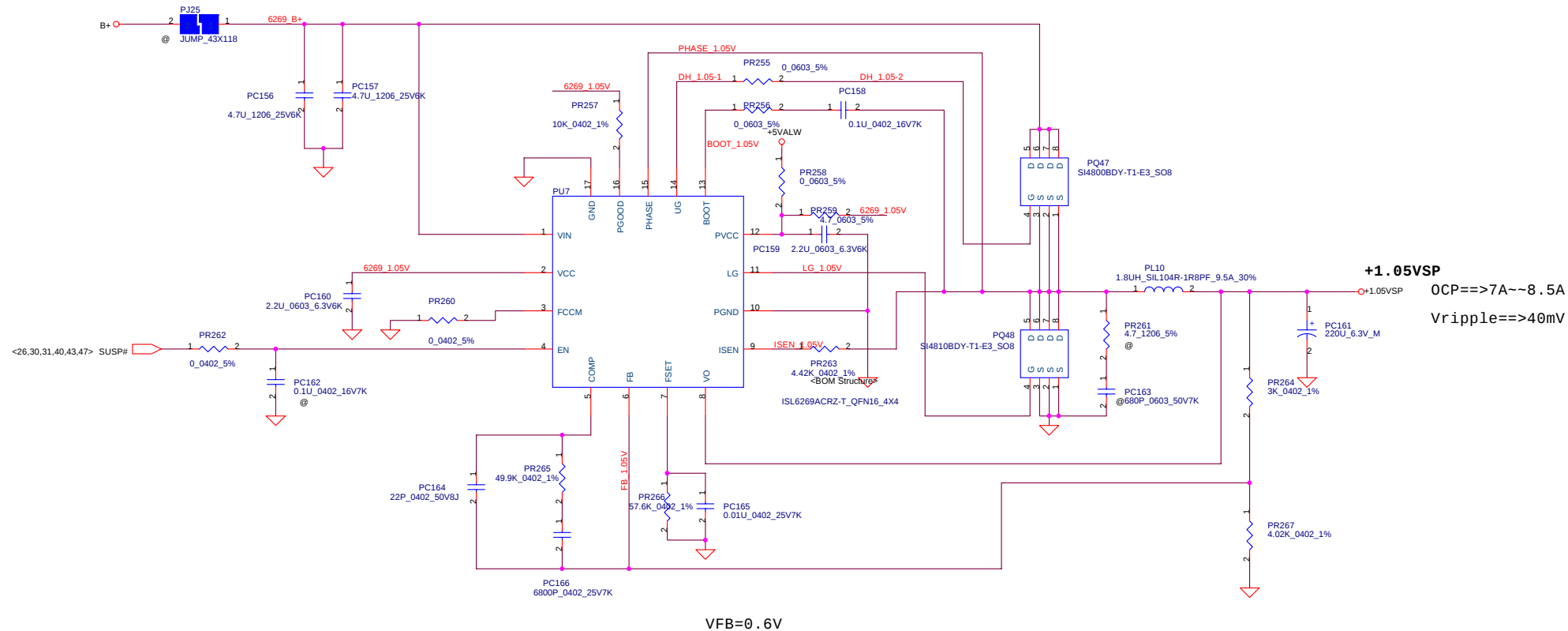


3.3VALWP Ipeak=6.6A~10A
Rds(on) = 20m ohm(max) ; Rds(on) = 16m ohm(typical)

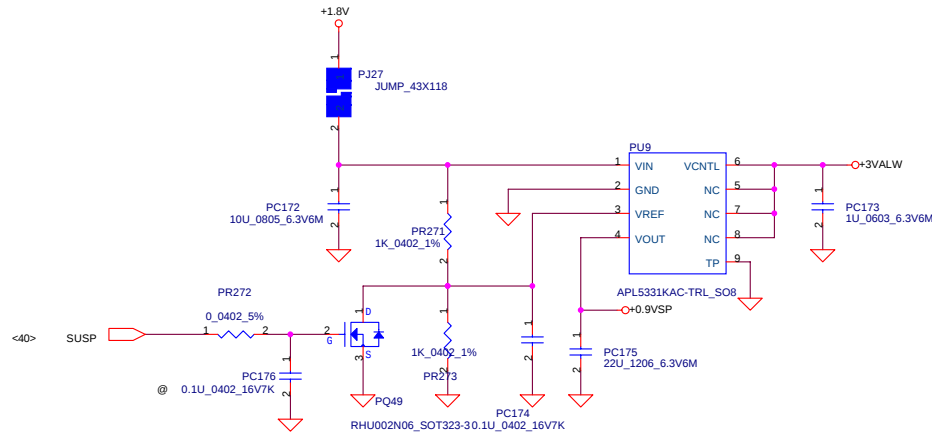
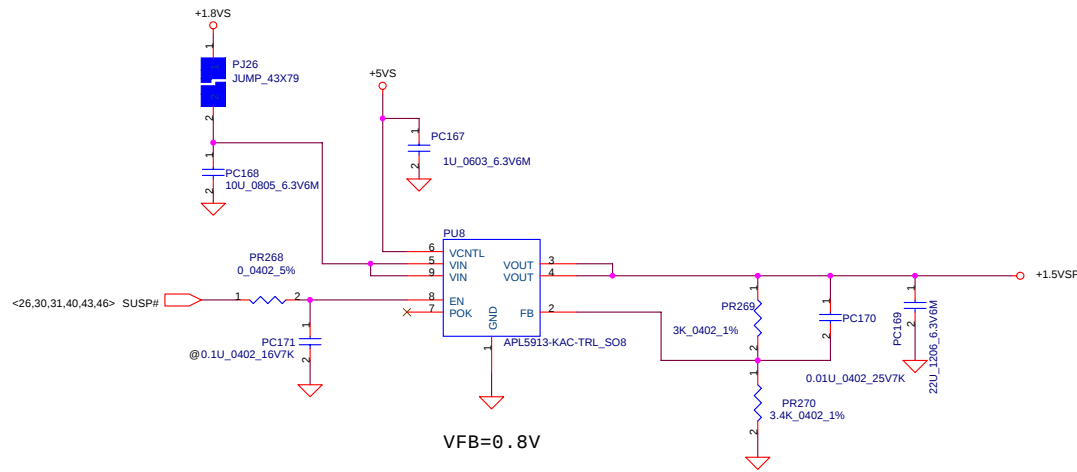
5VALWP Ipeak=6.6A~10A
Rds(on) = 20m ohm(max) ; Rds(on) = 16m ohm(typical)

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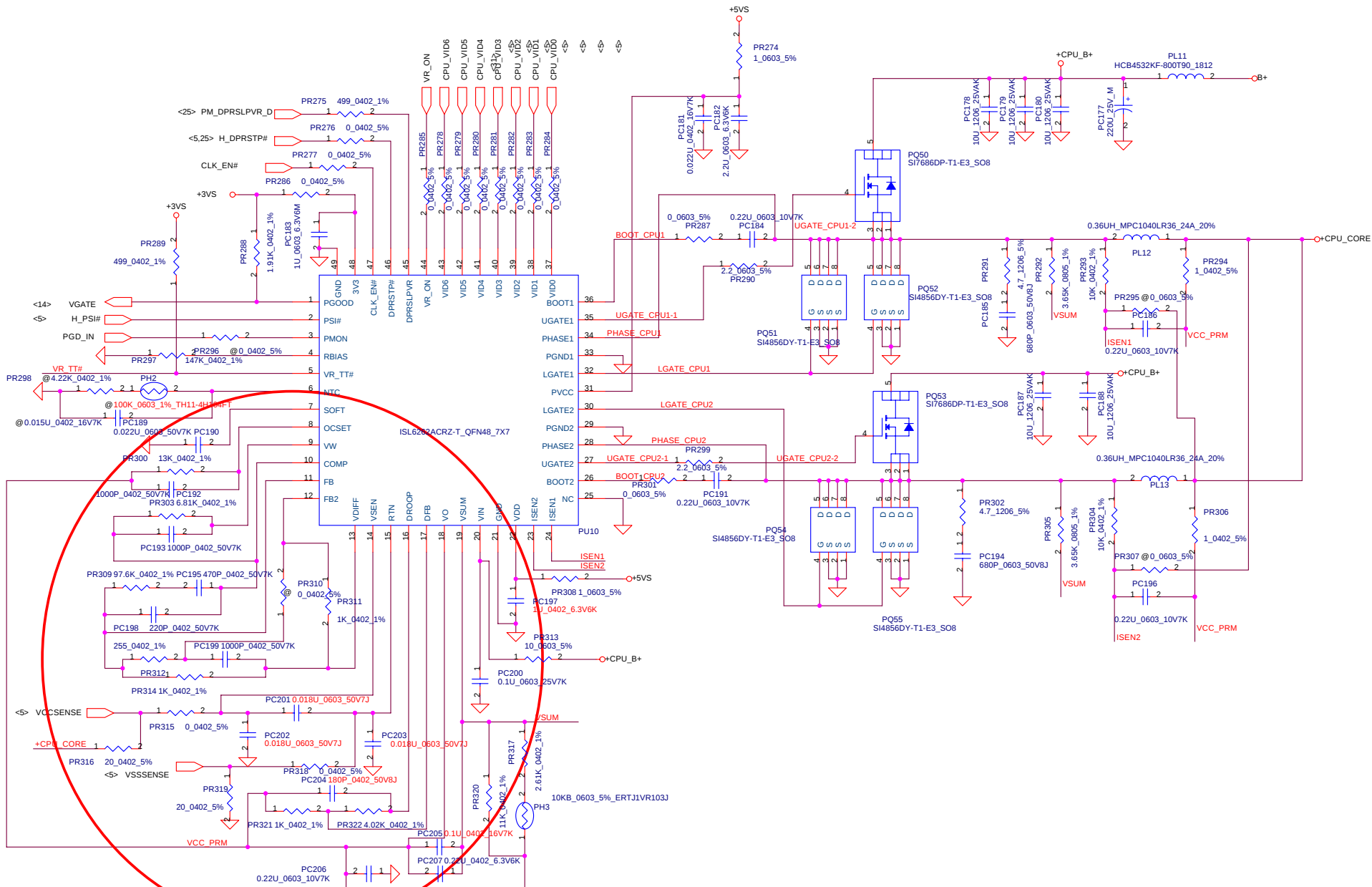




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