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P. Leader	Check by	Design by

PCB P/N: 1P-106A100-40SB

Project Code & Schematics Subject: MS80 Main Board

FOXCONN HON HAI PRECISION IND. CO., LTD.
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Title: *Index Page*

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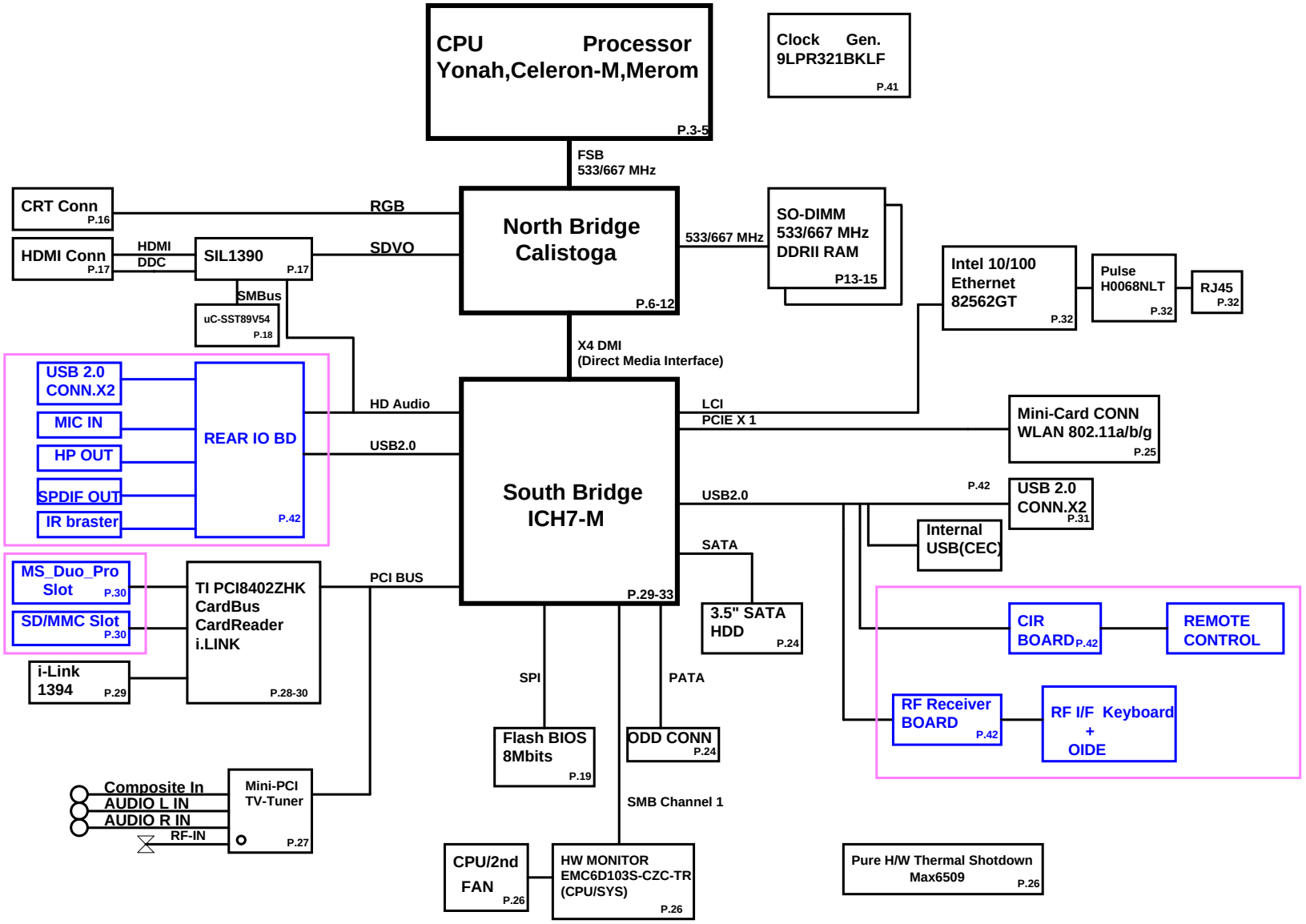
MS80 Bolck diagram



SYSTEM DC/DC
SC411MLTRT P.35

INPUTS	OUTPUTS
DC_OUT	+5VALW
DC_OUT	+3VALW

SYSTEM DC/DC
MAX8743 P.36

INPUTS	OUTPUTS
DC_OUT	+1_5VRUN
	+1_05VRUN

DDRII DC/DC
SC486 P.37

INPUTS	OUTPUTS
DC_OUT	+1_8VSUS
	+0_9VRUN

CPU DC/DC
ISL6262
P.38

INPUTS	OUTPUTS
DC_OUT	VHCORE

HDD DC/DC
MAX8546 P.40

INPUTS	OUTPUTS
DC_OUT	+12VRUN

MAX1616
P.34

INPUTS	OUTPUT
DC_IN	MAX1616_LDO

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: *Block Diagram (All)*		
Size: C	Document Number: MS80-1-04	Rev: 0.1
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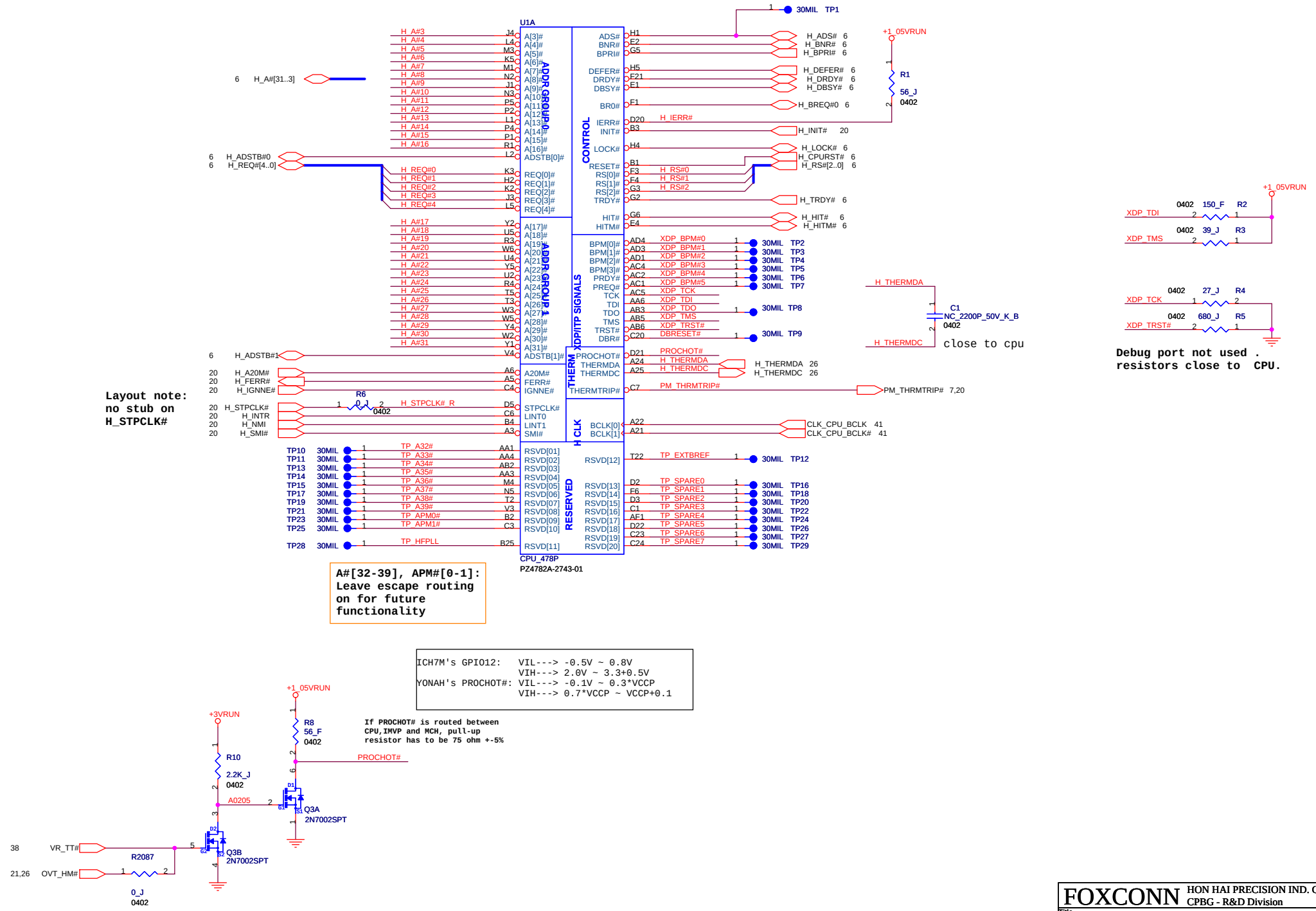

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	Yonah (HOST BUS) 1/3
Size A3	Document Number MS80-1-04 Rev 0.1
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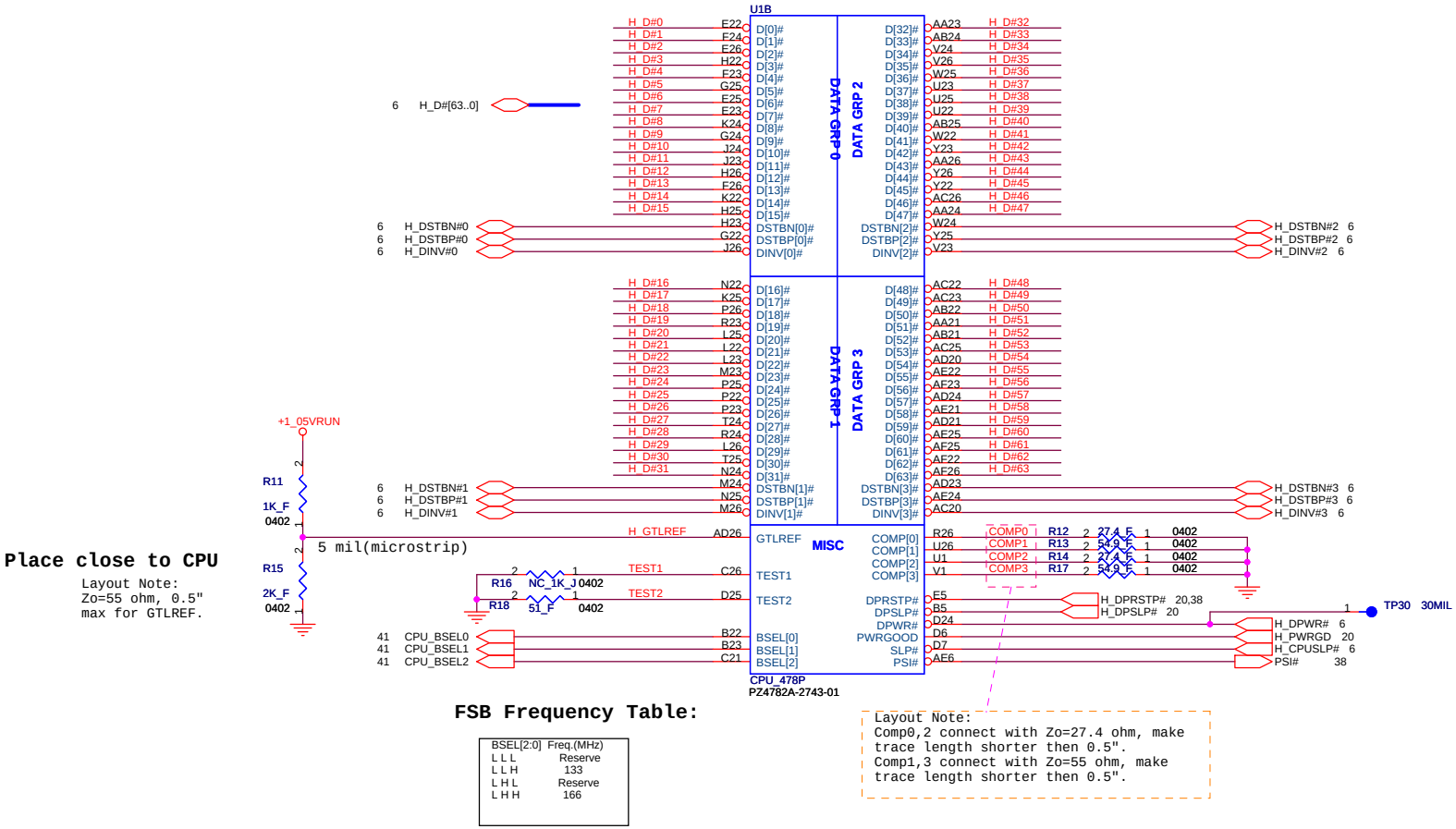

Place close to CPU

Layout Note:
Zo=55 ohm, 0.5"
max for GTLREF.

FSB Frequency Table:

BSEL[2:0]	Freq.(MHz)
L L L	Reserve
L L H	133
L H L	Reserve
L H H	166

Layout Note:
Comp0,2 connect with Zo=27.4 ohm, make trace length shorter then 0.5".
Comp1,3 connect with Zo=55 ohm, make trace length shorter then 0.5".

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Title: *Yonah (HOST BUS) 2/3*

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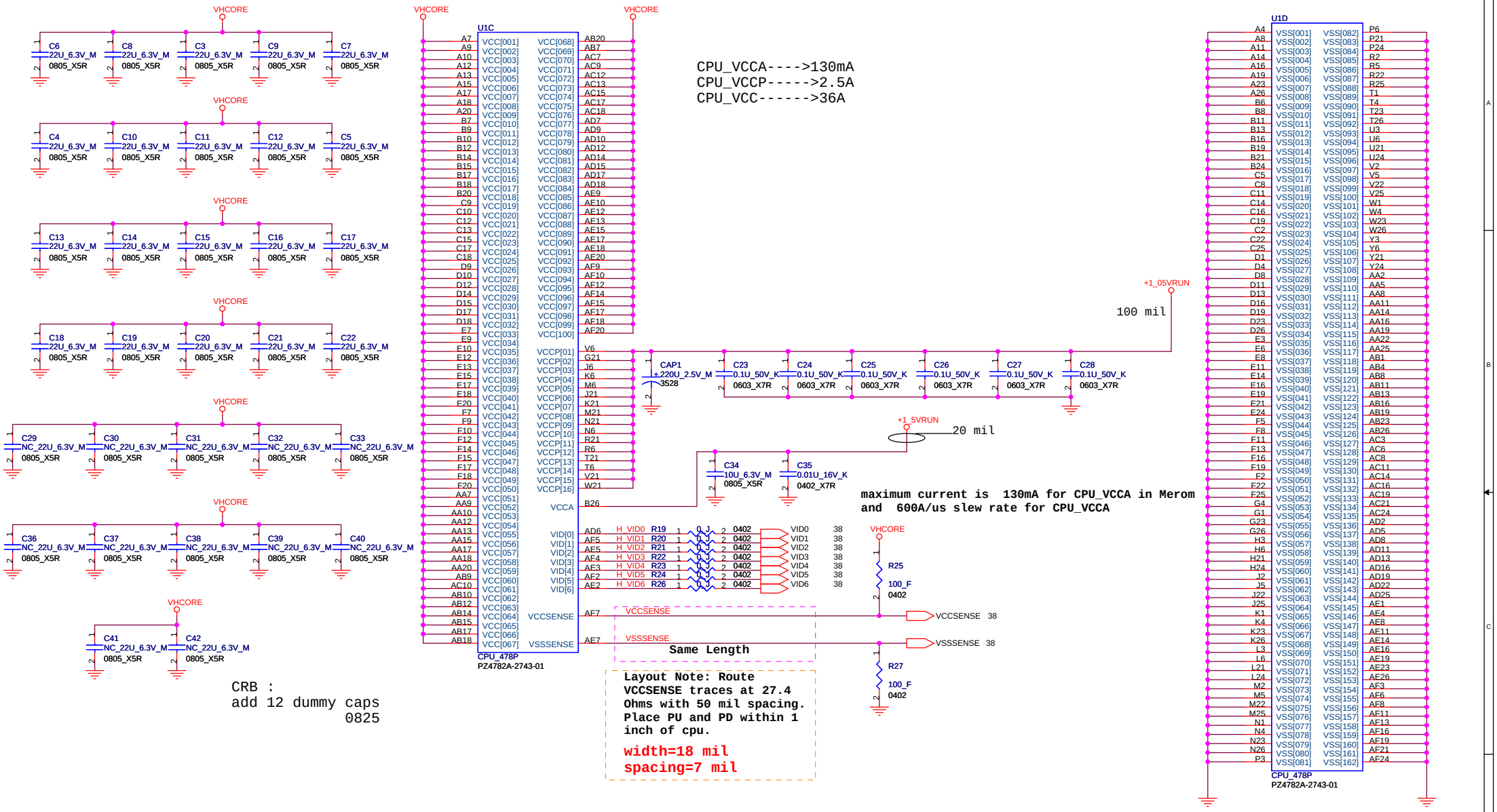

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	Yonah (POWER/GROUND) 3/3	
Size A3	Document Number MS80-1-04	Rev 0.1
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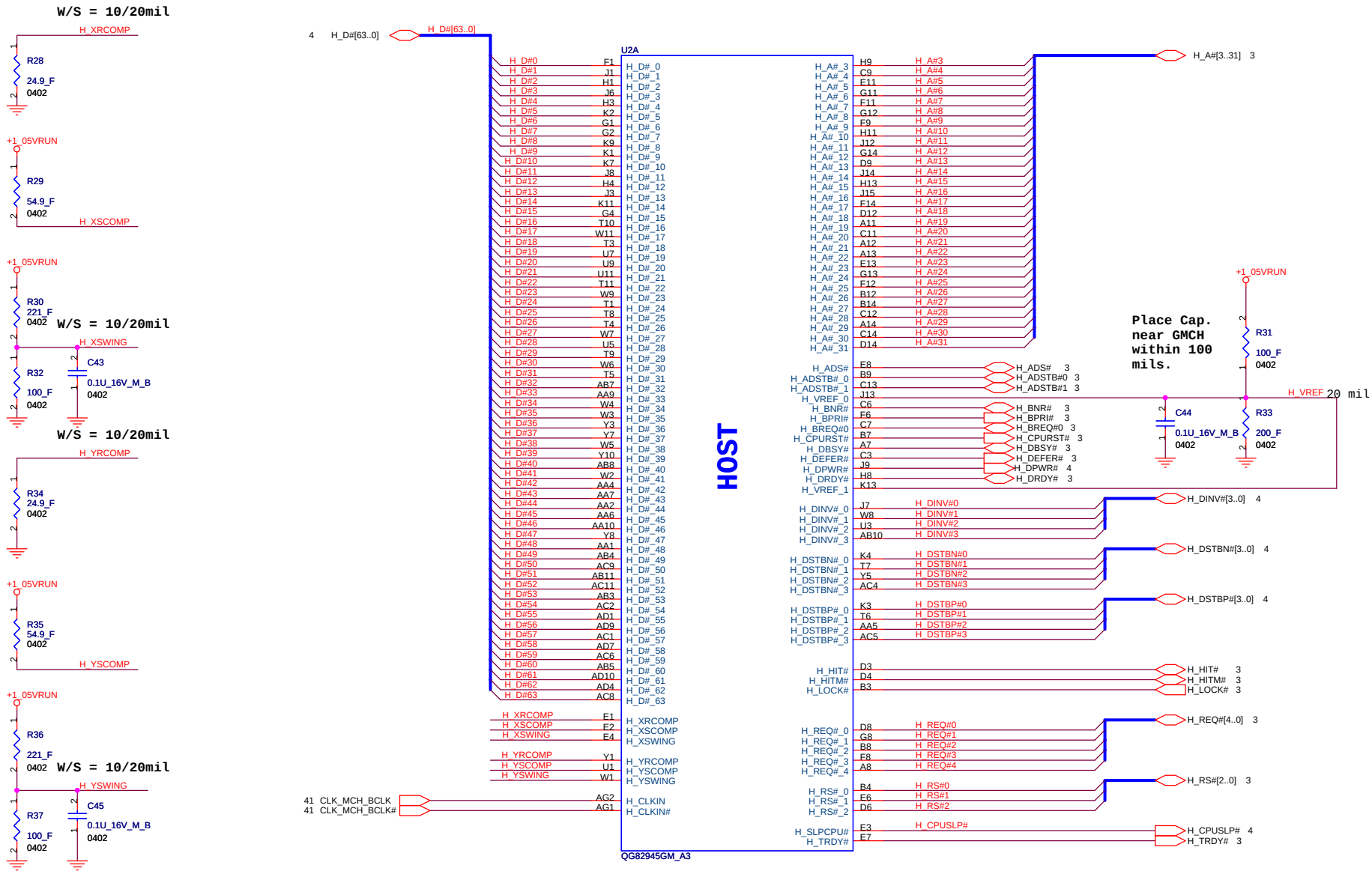
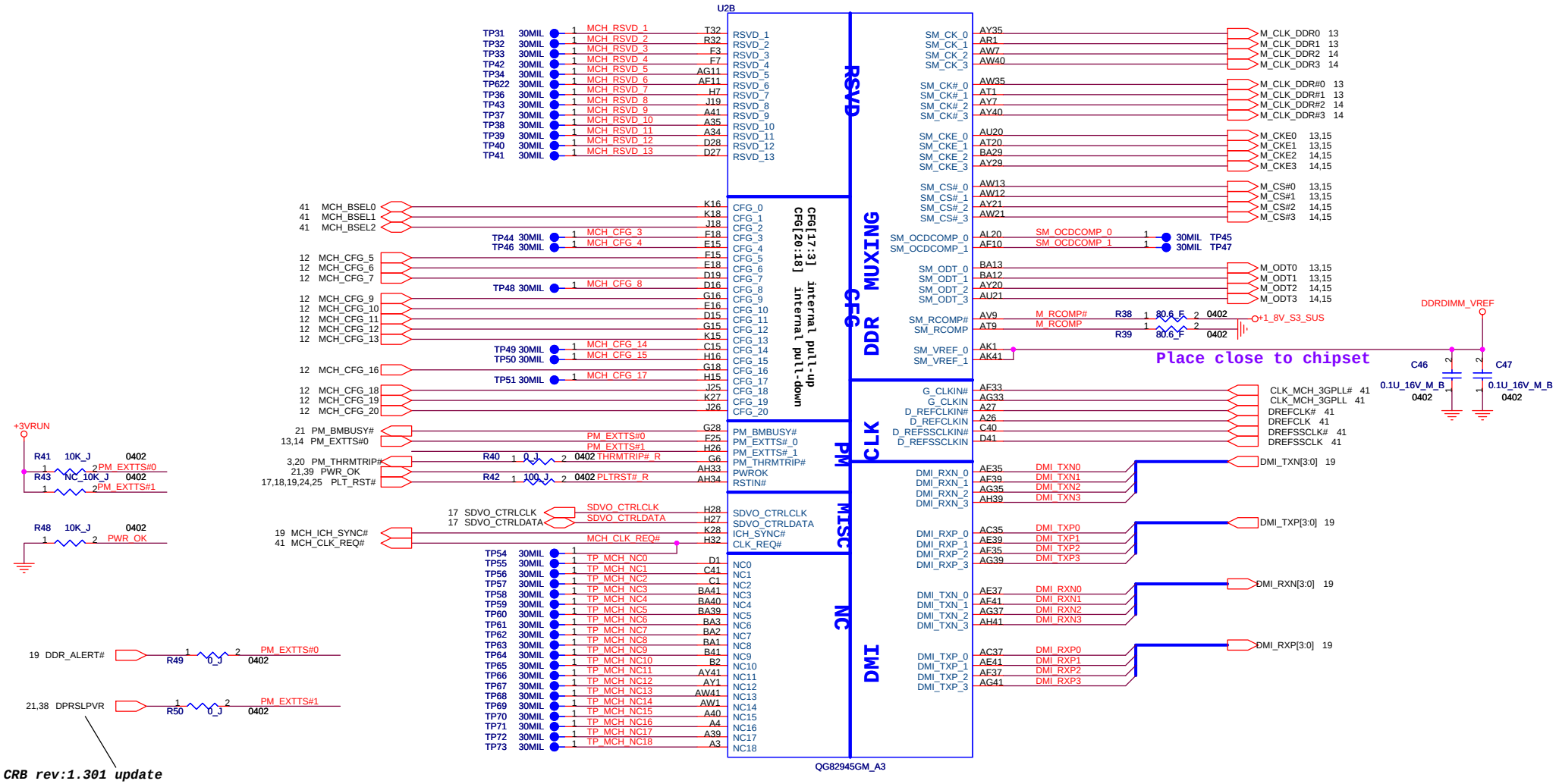


FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title	CALISTOHA (HOST)		
Size A3	Document Number MS80-1-04		Rev 0.1
Date: Tuesday, October 17, 2006	Sheet 6 of 44		



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	CALISTOGA (DMI) 2 of 7
Size A3	Document Number MS80-1-04
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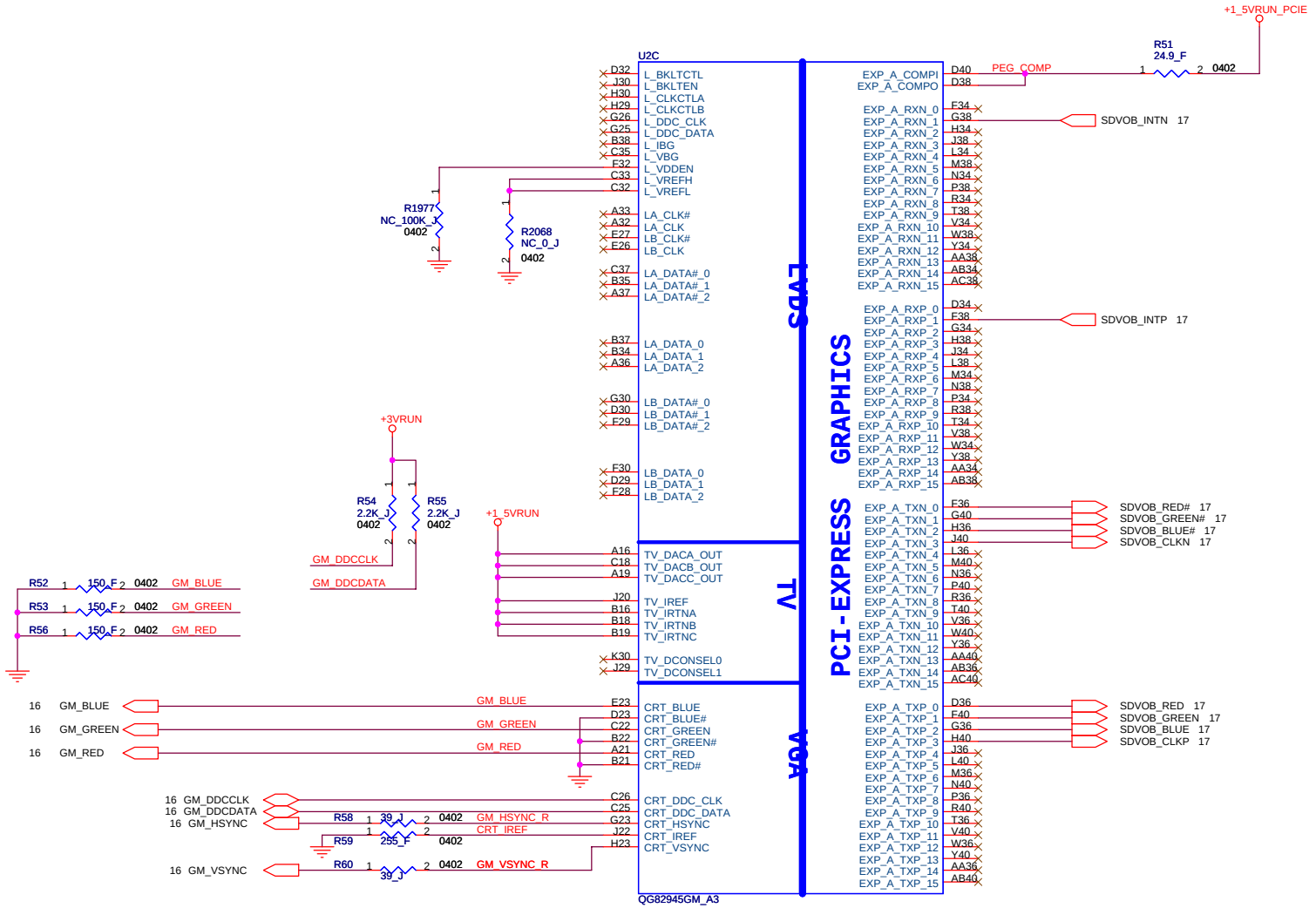

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	CALISTOGA (GRAPHIC) 3 of 7
Size A3	Document Number MS80-1-04 Rev 0.1
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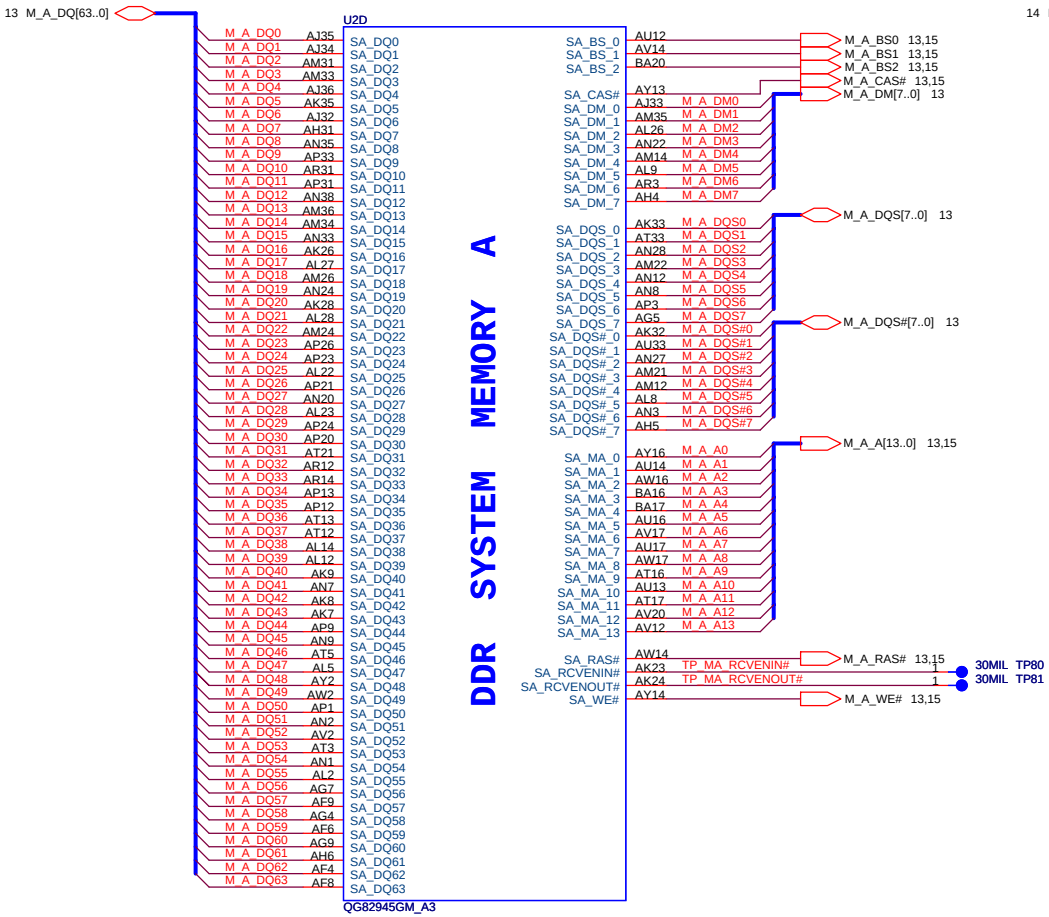

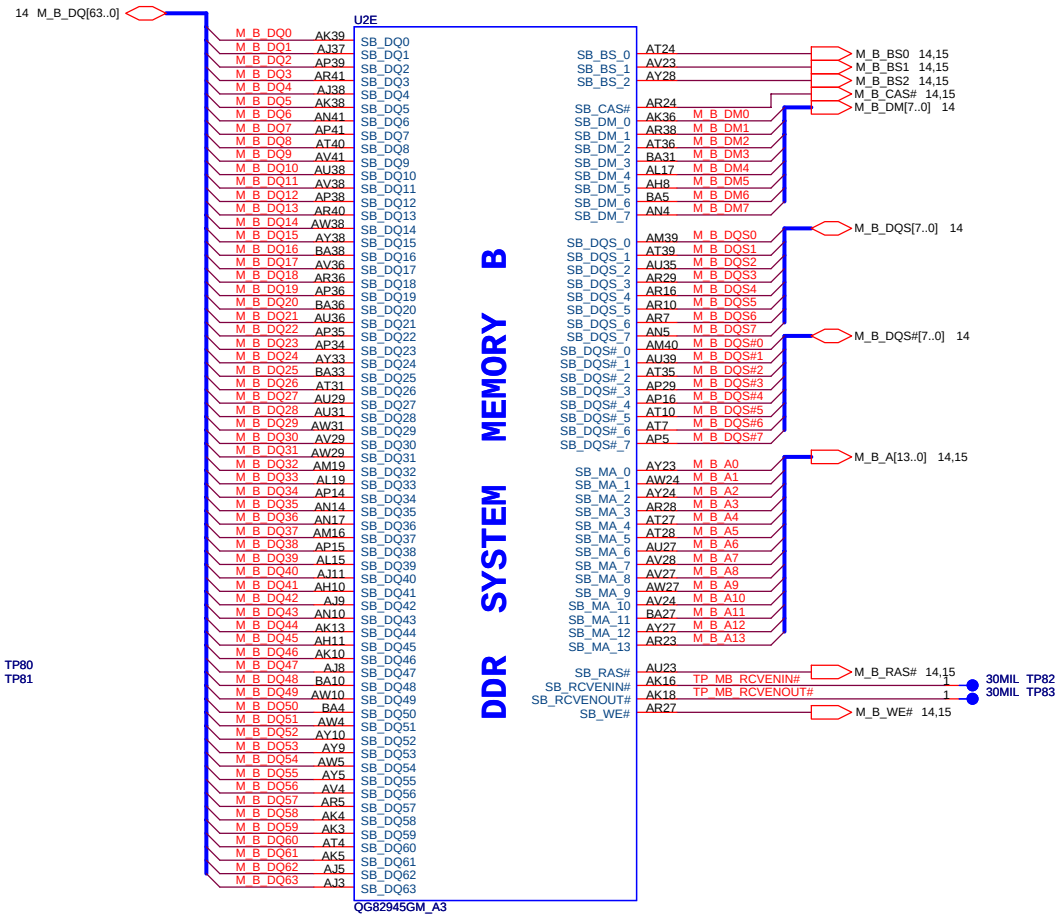

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: CALISTOGA (DDRII) 4 of 7		
Size: A3	Document Number: MS80-1-04	Rev: 0.1
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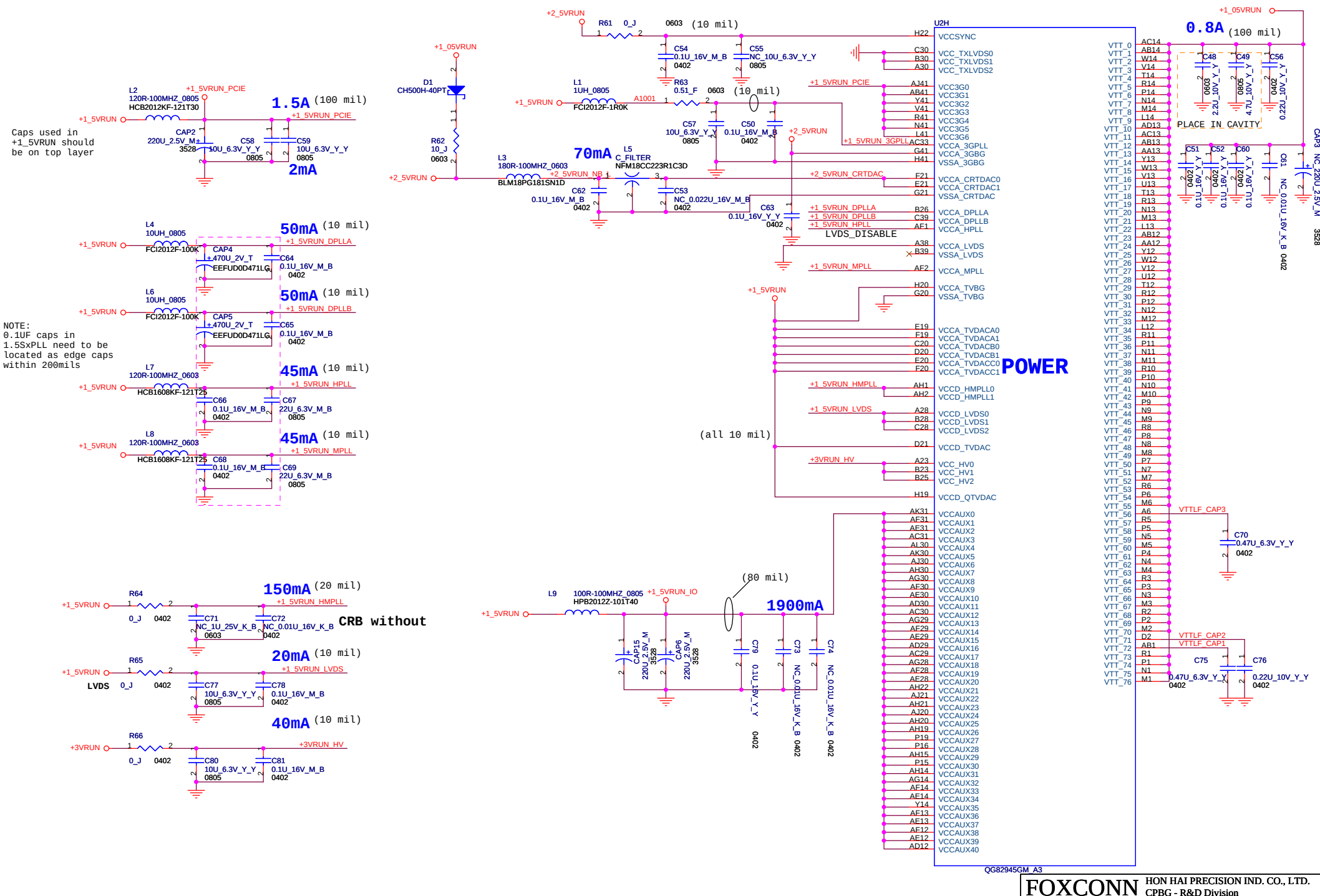

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Title: CALISTOGA(POWER,VCC) 5 of 7

Size: A3 | Document Number: MS80-1-04 | Rev: 0.1

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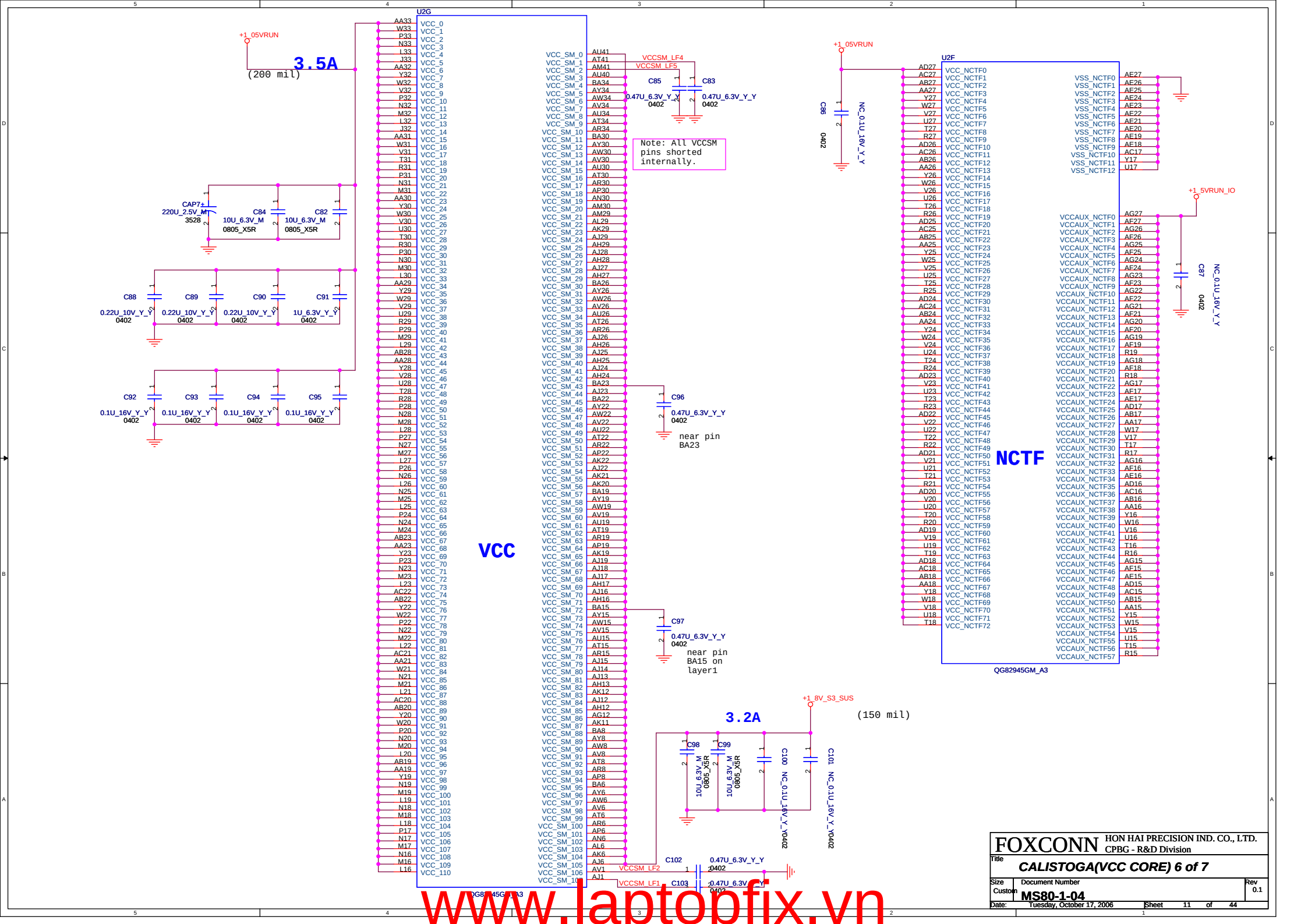

FOXCONN HON HAI PRECISION IND. CO., LTD.
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Title: CALISTOGA(VCC CORE) 6 of 7

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7 MCH_CFG_5 — 1 — 30MIL TP84

MCH_CFG_5	Low = DMIx2 High = DMIx4

7 MCH_CFG_6 — 1 — 30MIL TP85

MCH_CFG_6	Low = Moby Dick High = Calistoga

DDR2 select (default high)

7 MCH_CFG_7 — 1 — 30MIL TP87

MCH_CFG_7 (CPU Strap)	Low = RSVD High = Mobile Yonah processor

7 MCH_CFG_9 — 1 — 30MIL TP89

MCH_CFG_9 (PCIE Graphics Lane)	Low = Reverse Lane High = Normal operation

For layout convenience

7 MCH_CFG_10 — 1 — 30MIL TP90

MCH_CFG_10 (HOST PLL VCC SELECT)	Low = RESERVED High = MOBILITY

7 MCH_CFG_11 — 1 — R67 NC_2.2K_J 0402 — 2

MCH_CFG_11 (PSB 4x CLK ENABLE)	Low = Reserved High= Calistoga

7 MCH_CFG_12 — 1 — 30MIL TP92
7 MCH_CFG_13 — 1 — 30MIL TP93

MCH_CFG_[13:12] (XOR/ALLZ)	00=Partial Clock Gating Disable 01=XOR Mode Enable 10=All-Z Mode Enable 11=Normal Operation(Default)

7 MCH_CFG_16 — 1 — 30MIL TP94

MCH_CFG_16 (FSB Dynamic ODT)	Low = Dynamic ODT Disabled High = Dynamic ODT Enable

MCH_CFG_18 (VCC_CORE Select)	Low = 1.05V(default) High = 1.5V

7 MCH_CFG_18 — 1 — 30MIL TP86

MCH_CFG_19 (DMI LANE REVERSAL)	Low = Normal(default) High = LANES REVERSED

7 MCH_CFG_19 — 1 — 30MIL TP88

MCH_CFG_20 (PCIe Backward Interpoerability mode)	Low = Only SDVO or PCIE x1 is operational (defaults)) High = SDVO and PCIE x1 are operating simultaneously via the PEG port

7 MCH_CFG_20 — 1 — 30MIL TP91

Layout Noe:
Location of all MCH_CFG strap resistors needs to be close to trace to minimize stub

Check CALISTOGA version , after A2 version , if systec can't boot up then NC the pull low R

U2I

AC41	VSS_0		VSS_97	AK34	
AA41	VSS_1		VSS_98	AG34	
W41	VSS_2		VSS_99	AF34	
T41	VSS_3		VSS_100	AE34	
P41	VSS_4		VSS_101	AC34	
M41	VSS_5		VSS_102	C34	
J41	VSS_6		VSS_103	AW33	
F41	VSS_7		VSS_104	AV33	
AV40	VSS_8		VSS_105	AR33	
AP40	VSS_9		VSS_106	AE33	
AN40	VSS_10		VSS_107	AB33	
AK40	VSS_11		VSS_108	Y33	
AJ40	VSS_12		VSS_109	V33	
AH40	VSS_13		VSS_110	T33	
AG40	VSS_14		VSS_111	R33	
AF40	VSS_15		VSS_112	M33	
AE40	VSS_16		VSS_113	H33	
B40	VSS_17		VSS_114	G33	
AY39	VSS_18		VSS_115	F33	
AW39	VSS_19		VSS_116	D33	
AV39	VSS_20		VSS_117	B33	
AR39	VSS_21		VSS_118	AH32	
AN39	VSS_22		VSS_119	AG32	
AJ39	VSS_23		VSS_120	AE32	
AC39	VSS_24		VSS_121	AE32	
AB39	VSS_25		VSS_122	AC32	
AA39	VSS_26		VSS_123	AB32	
Y39	VSS_27		VSS_124	G32	
W39	VSS_28		VSS_125	B32	
V39	VSS_29		VSS_126	AY31	
T39	VSS_30		VSS_127	AV31	
R39	VSS_31		VSS_128	AN31	
P39	VSS_32		VSS_129	AJ31	
N39	VSS_33		VSS_130	AG31	
M39	VSS_34		VSS_131	AB31	
L39	VSS_35		VSS_132	Y31	
J39	VSS_36		VSS_133	AB30	
H39	VSS_37		VSS_134	E30	
G39	VSS_38		VSS_135	AT29	
F39	VSS_39		VSS_136	AN29	
D39	VSS_40		VSS_137	AB29	
AT38	VSS_41		VSS_138	T29	
AM38	VSS_42		VSS_139	N29	
AH38	VSS_43		VSS_140	K29	
AG38	VSS_44		VSS_141	G29	
AF38	VSS_45		VSS_142	E29	
AE38	VSS_46		VSS_143	C29	
C38	VSS_47		VSS_144	B29	
AK37	VSS_48		VSS_145	A29	
AH37	VSS_49		VSS_146	BA28	
AB37	VSS_50		VSS_147	AW28	
AA37	VSS_51		VSS_148	AU28	
Y37	VSS_52		VSS_149	AP28	
W37	VSS_53		VSS_150	AM28	
V37	VSS_54		VSS_151	AD28	
T37	VSS_55		VSS_152	AC28	
R37	VSS_56		VSS_153	W28	
P37	VSS_57		VSS_154	J28	
N37	VSS_58		VSS_155	E28	
M37	VSS_59		VSS_156	AP27	
L37	VSS_60		VSS_157	AM27	
J37	VSS_61		VSS_158	AK27	
H37	VSS_62		VSS_159	J27	
G37	VSS_63		VSS_160	G27	
F37	VSS_64		VSS_161	F27	
D37	VSS_65		VSS_162	C27	
AY36	VSS_66		VSS_163	B27	
AW36	VSS_67		VSS_164	AN26	
AN36	VSS_68		VSS_165	M26	
AH36	VSS_69		VSS_166	K26	
AG36	VSS_70		VSS_167	F26	
AF36	VSS_71		VSS_168	D26	
AE36	VSS_72		VSS_169	AK25	
AC36	VSS_73		VSS_170	P25	
C36	VSS_74		VSS_171	K25	
B36	VSS_75		VSS_172	H25	
BA35	VSS_76		VSS_173	E25	
AV35	VSS_77		VSS_174	D25	
AR35	VSS_78		VSS_175	A25	
AH35	VSS_79		VSS_176	BA24	
AB35	VSS_80		VSS_177	AU24	
AA35	VSS_81		VSS_178	AL24	
Y35	VSS_82		VSS_179	AW23	
W35	VSS_83				
V35	VSS_84				
T35	VSS_85				
R35	VSS_86				
P35	VSS_87				
N35	VSS_88				
M35	VSS_89				
L35	VSS_90				
J35	VSS_91				
H35	VSS_92				
G35	VSS_93				
F35	VSS_94				
D35	VSS_95				
AN34	VSS_96				

VSS

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U2J

AT23	VSS_180		VSS_273	J11	
AN23	VSS_181		VSS_274	D11	
AM23	VSS_182		VSS_275	B11	
AH23	VSS_183		VSS_276	AV10	
AC23	VSS_184		VSS_277	AP10	
W23	VSS_185		VSS_278	AL10	
K23	VSS_186		VSS_279	AJ10	
J23	VSS_187		VSS_280	AG10	
F23	VSS_188		VSS_281	AC10	
C23	VSS_189		VSS_282	W10	
AA22	VSS_190		VSS_283	U10	
K22	VSS_191		VSS_284	BA9	
G22	VSS_192		VSS_285	AW9	
F22	VSS_193		VSS_286	AR9	
E22	VSS_194		VSS_287	AH9	
D22	VSS_195		VSS_288	AB9	
A22	VSS_196		VSS_289	Y9	
BA21	VSS_197		VSS_290	R9	
AV21	VSS_198		VSS_291	G9	
AR21	VSS_199		VSS_292	E9	
AN21	VSS_200		VSS_293	A9	
AL21	VSS_201		VSS_294	AG8	
AB21	VSS_202		VSS_295	AD8	
Y21	VSS_203		VSS_296	AA8	
P21	VSS_204		VSS_297	U8	
K21	VSS_205		VSS_298	K8	
J21	VSS_206		VSS_299	C8	
H21	VSS_207		VSS_300	BA7	
C21	VSS_208		VSS_301	AV7	
AW20	VSS_209		VSS_302	AP7	
AR20	VSS_210		VSS_303	AL7	
AM20	VSS_211		VSS_304	AJ7	
AA20	VSS_212		VSS_305	AH7	
K20	VSS_213		VSS_306	AF7	
B20	VSS_214		VSS_307	AC7	
A20	VSS_215		VSS_308	R7	
AN19	VSS_216		VSS_309	G7	
AC19	VSS_217		VSS_310	D7	
W19	VSS_218		VSS_311	AG6	
K19	VSS_219		VSS_312	AD6	
G19	VSS_220		VSS_313	AB6	
C19	VSS_221		VSS_314	Y6	
AH18	VSS_222		VSS_315	U6	
P18	VSS_223		VSS_316	N6	
H18	VSS_224		VSS_317	K6	
D18	VSS_225		VSS_318	H6	
A18	VSS_226		VSS_319	B6	
AY17	VSS_227		VSS_320	AV5	
AR17	VSS_228		VSS_321	AE5	
AP17	VSS_229		VSS_322	AD5	
AM17	VSS_230		VSS_323	AY4	
AK17	VSS_231		VSS_324	AR4	
AV16	VSS_232		VSS_325	AP4	
AN16	VSS_233		VSS_326	AL4	
AL16	VSS_234		VSS_327	AJ4	
J16	VSS_235		VSS_328	Y4	
F16	VSS_236		VSS_329	U4	
C16	VSS_237		VSS_330	R4	
AN15	VSS_238		VSS_331	J4	
AM15	VSS_239		VSS_332	F4	
AK15	VSS_240		VSS_333	C4	
N15	VSS_241		VSS_334	AY3	
M15	VSS_242		VSS_335	AW3	
L15	VSS_243		VSS_336	AV3	
B15	VSS_244		VSS_337	AL3	
A15	VSS_245		VSS_338	AH3	
BA14	VSS_246		VSS_339	AG3	
AT14	VSS_247		VSS_340	AF3	
AK14	VSS_248		VSS_341	AD3	
AD14	VSS_249		VSS_342	AC3	
AA14	VSS_250		VSS_343	AA3	
U14	VSS_251		VSS_344	G3	
K14	VSS_252		VSS_345	AT2	
H14	VSS_253		VSS_346	AR2	
E14	VSS_254		VSS_347	AP2	
AV13	VSS_255		VSS_348	AK2	
AR13	VSS_256		VSS_349	AJ2	
AN13	VSS_257		VSS_350	AD2	
AM13	VSS_258		VSS_351	AB2	
AL13	VSS_259		VSS_352	Y2	
AG13	VSS_260		VSS_353	U2	
P13	VSS_261		VSS_354	T2	
E13	VSS_262		VSS_355	N2	
D13	VSS_263		VSS_356	J2	
B13	VSS_264		VSS_357	H2	
AY12	VSS_265		VSS_358	F2	
AC12	VSS_266		VSS_359	C2	
K12	VSS_267		VSS_360	AL1	
H12	VSS_268				
E12	VSS_269				
AD11	VSS_270				
AA11	VSS_271				
Y11	VSS_272				

VSS

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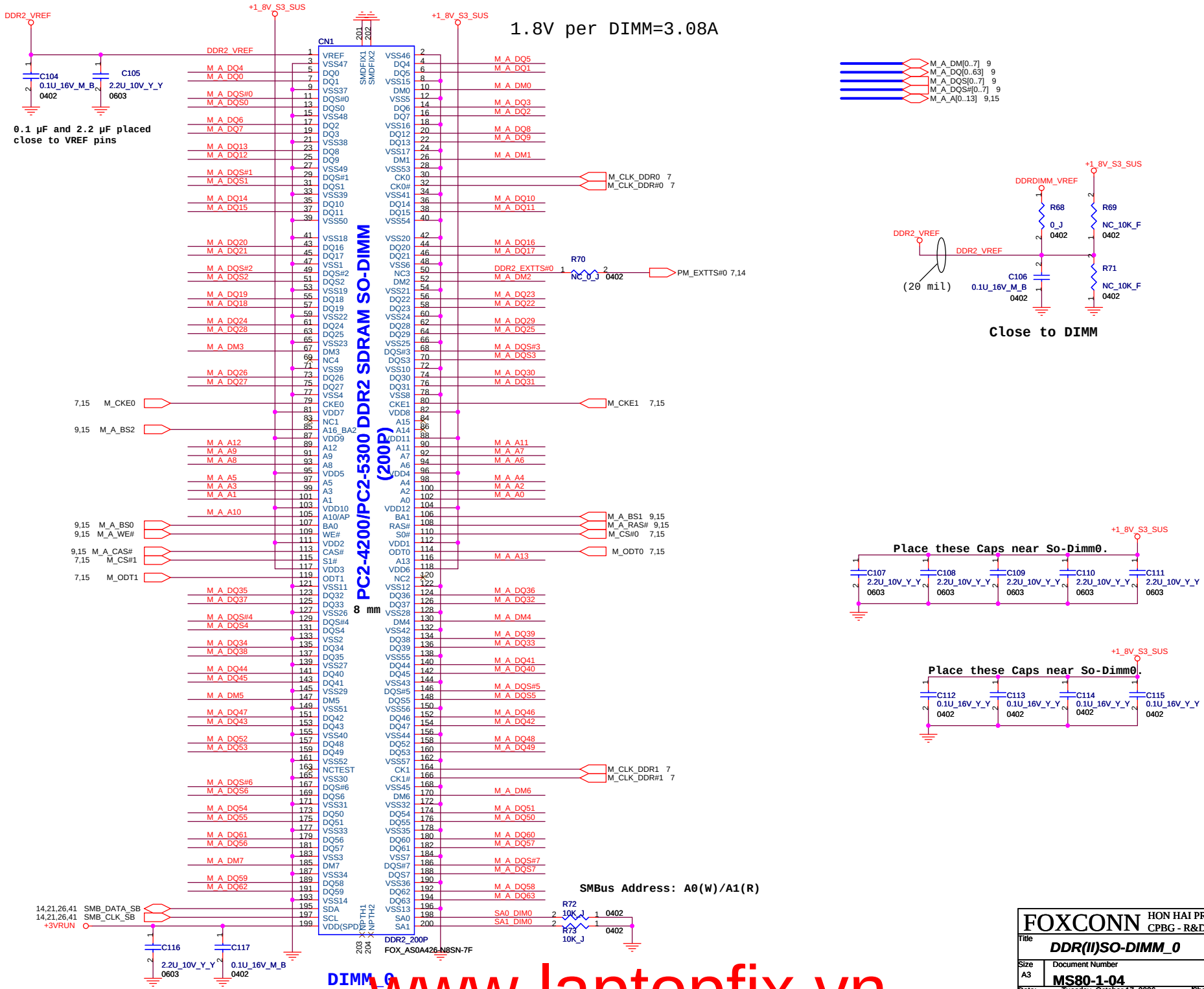
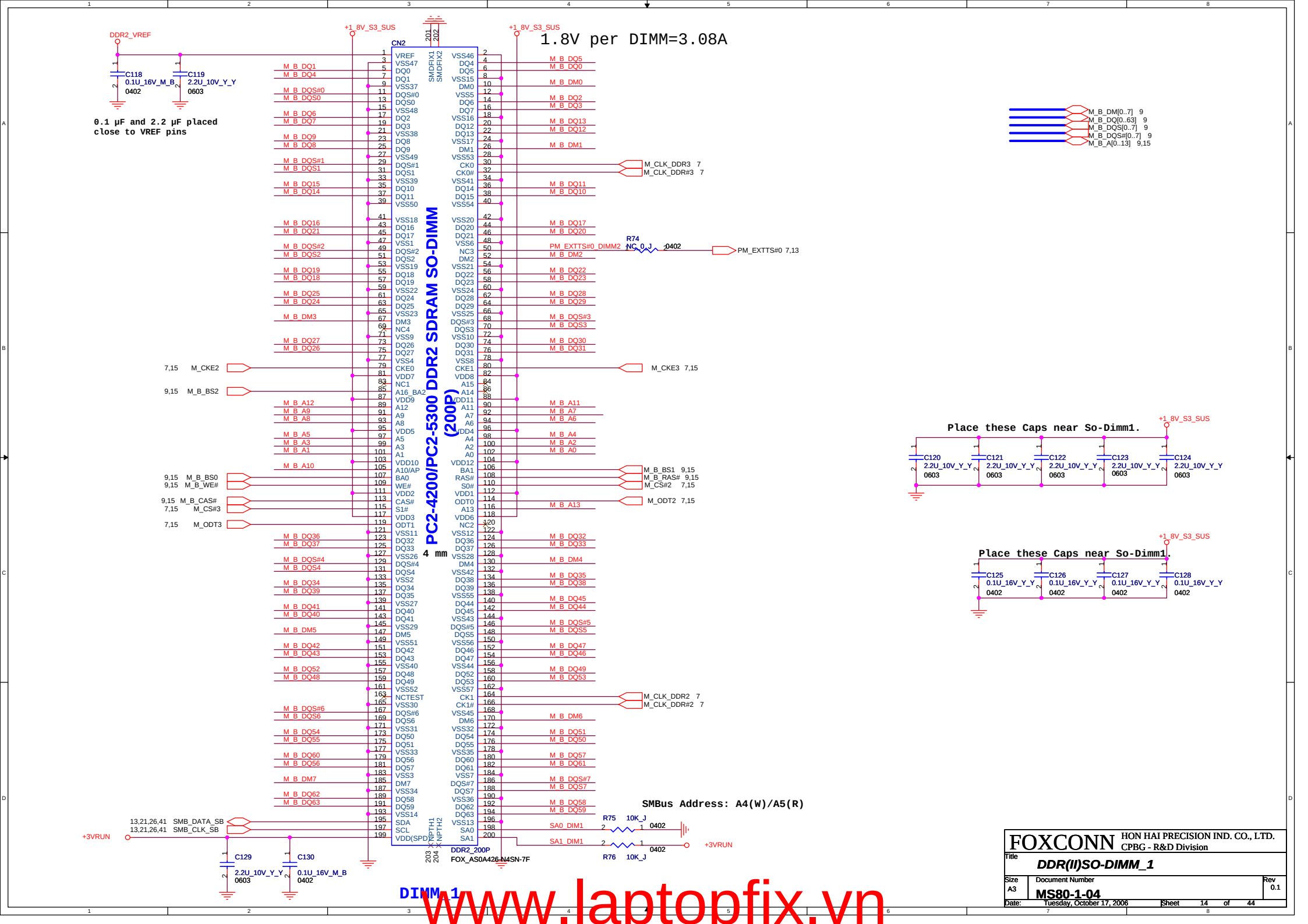

1.8V per DIMM=3.08A
CN1
PC2-4200/PC2-5300 DDR2 SDRAM SO-DIMM (200P)
8 mm
DDR2_200P
FOX_AS0A426-N8SN-7F
DIMM_0
0.1 µF and 2.2 µF placed close to VREF pins
SMBus Address: A0(W)/A1(R)
Close to DIMM
Place these Caps near So-Dimm0.
Place these Caps near So-Dimm0.
(20 mil)
FOXCONN
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
DDR(II)SO-DIMM_0
MS80-1-04
Tuesday, October 17, 2006
www.laptopfix.vn


1.8V per DIMM=3.08A
DDR2_VREF
C118 0.1U_16V_M_B 0402
C119 2.2U_10V_Y_Y 0603
0.1 µF and 2.2 µF placed close to VREF pins
+1_8V_S3_SUS
CN2
PC2-4200/PC2-5300 DDR2 SDRAM SO-DIMM (200P)
4 mm
DDR2_200P
FOX_AS0A426-N4SN-7F
M_B_DM[0..7] 9
M_B_DQ[0..63] 9
M_B_DQS[0..7] 9
M_B_DQS#[0..7] 9
M_B_A[0..13] 9,15
M_CLK_DDR3 7
M_CLK_DDR#3 7
M_CLK_DDR2 7
M_CLK_DDR#2 7
R74 NC_0_J 0402
PM_EXTTS#0_DIMM2
PM_EXTTS#0 7,13
M_CKE2 7,15
M_CKE3 7,15
M_B_BS2 9,15
M_B_BS0 9,15
M_B_WE# 9,15
M_B_CAS# 9,15
M_CS#3 7,15
M_ODT3 7,15
M_B_BS1 9,15
M_B_RAS# 9,15
M_CS#2 7,15
M_ODT2 7,15
Place these Caps near So-Dimm1.
C120 2.2U_10V_Y_Y 0603
C121 2.2U_10V_Y_Y 0603
C122 2.2U_10V_Y_Y 0603
C123 2.2U_10V_Y_Y 0603
C124 2.2U_10V_Y_Y 0603
Place these Caps near So-Dimm1.
C125 0.1U_16V_Y_Y 0402
C126 0.1U_16V_Y_Y 0402
C127 0.1U_16V_Y_Y 0402
C128 0.1U_16V_Y_Y 0402
SMBus Address: A4(W)/A5(R)
13,21,26,41 SMB_DATA_SB
13,21,26,41 SMB_CLK_SB
+3VRUN
R75 10K_J 0402
R76 10K_J 0402
SA0_DIM1
SA1_DIM1
C129 2.2U_10V_Y_Y 0603
C130 0.1U_16V_M_B 0402
DIMM_1
FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
Title DDR(II)SO-DIMM_1
Size A3
Document Number MS80-1-04
Rev 0.1
Date: Tuesday, October 17, 2006
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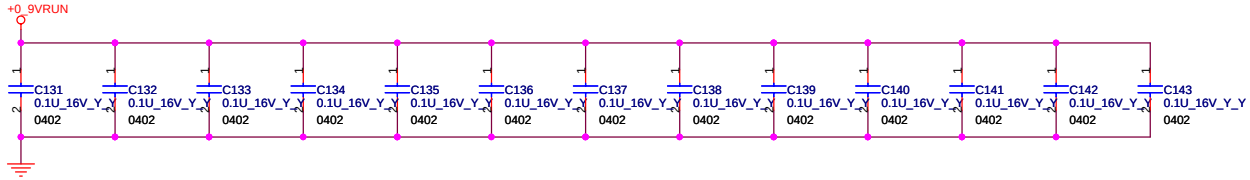
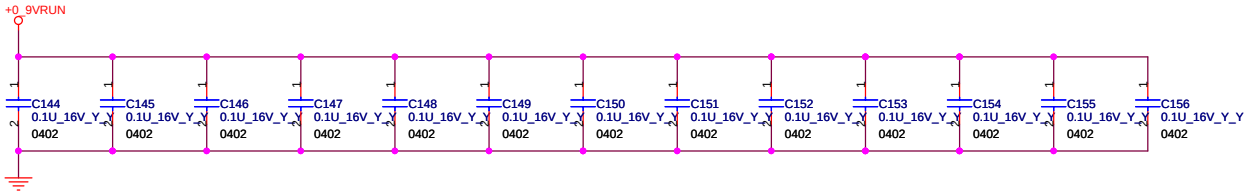
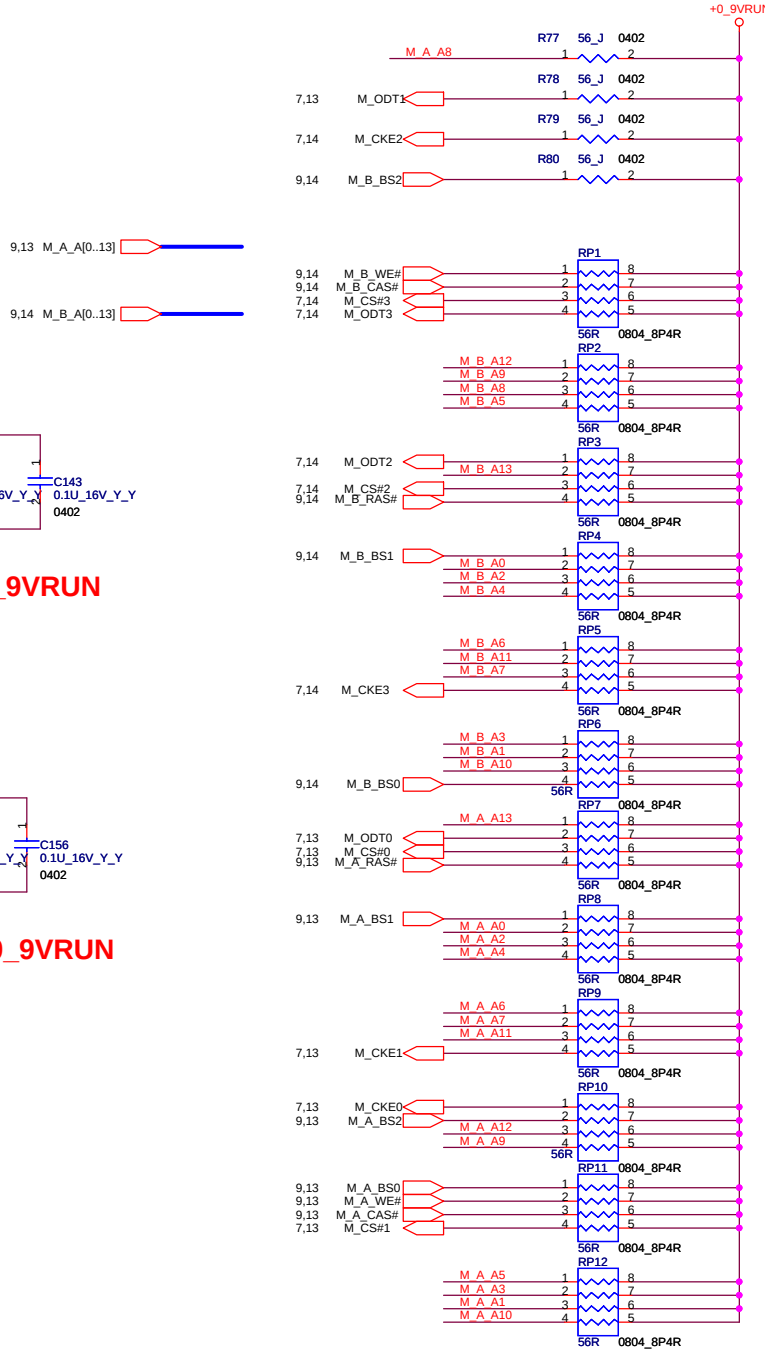


Layout note: Place 1 cap close to every 1 R-pack terminated to +0_9VRUN



Layout note: Place 1 cap close to every 1 R-pack terminated to +0_9VRUN

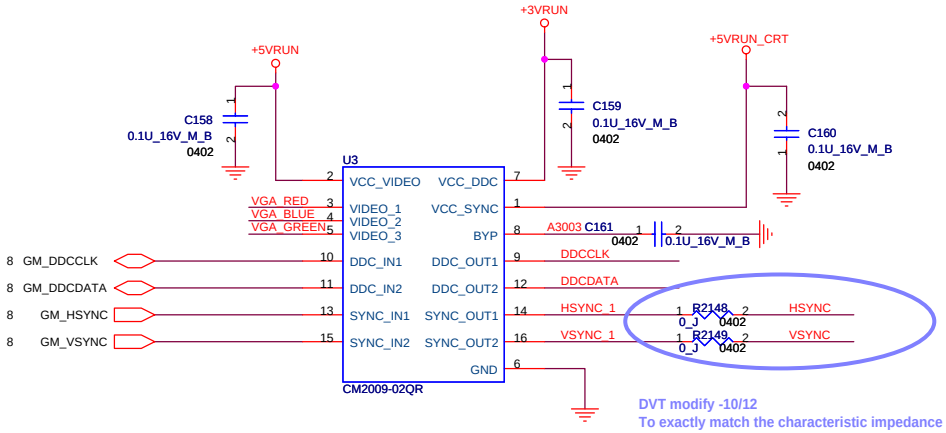


FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

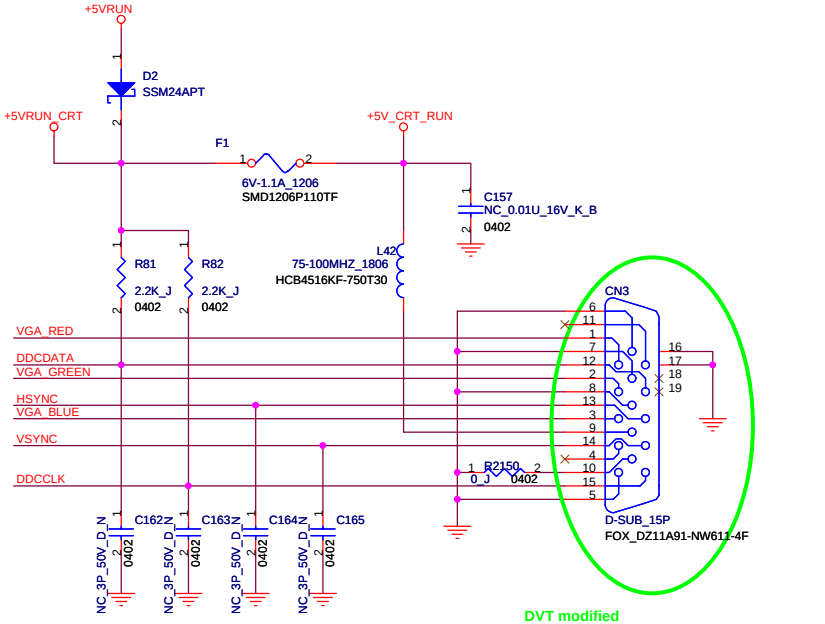
Title: ***DDR(II)Termination***

Size	Document Number	Rev
A3	**MS80-1-04**	0.1

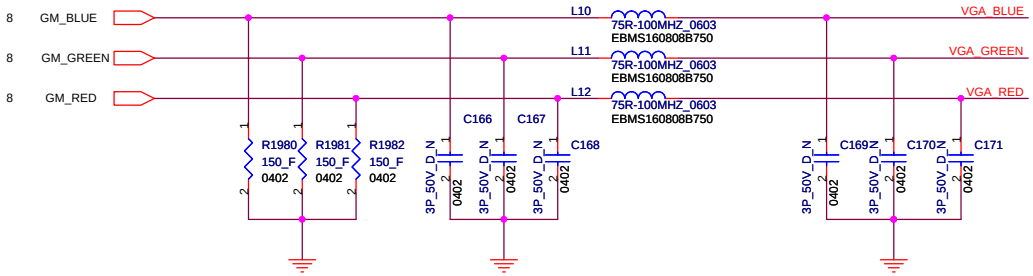
Date: Tuesday, October 17, 2006 Sheet 15 of 44



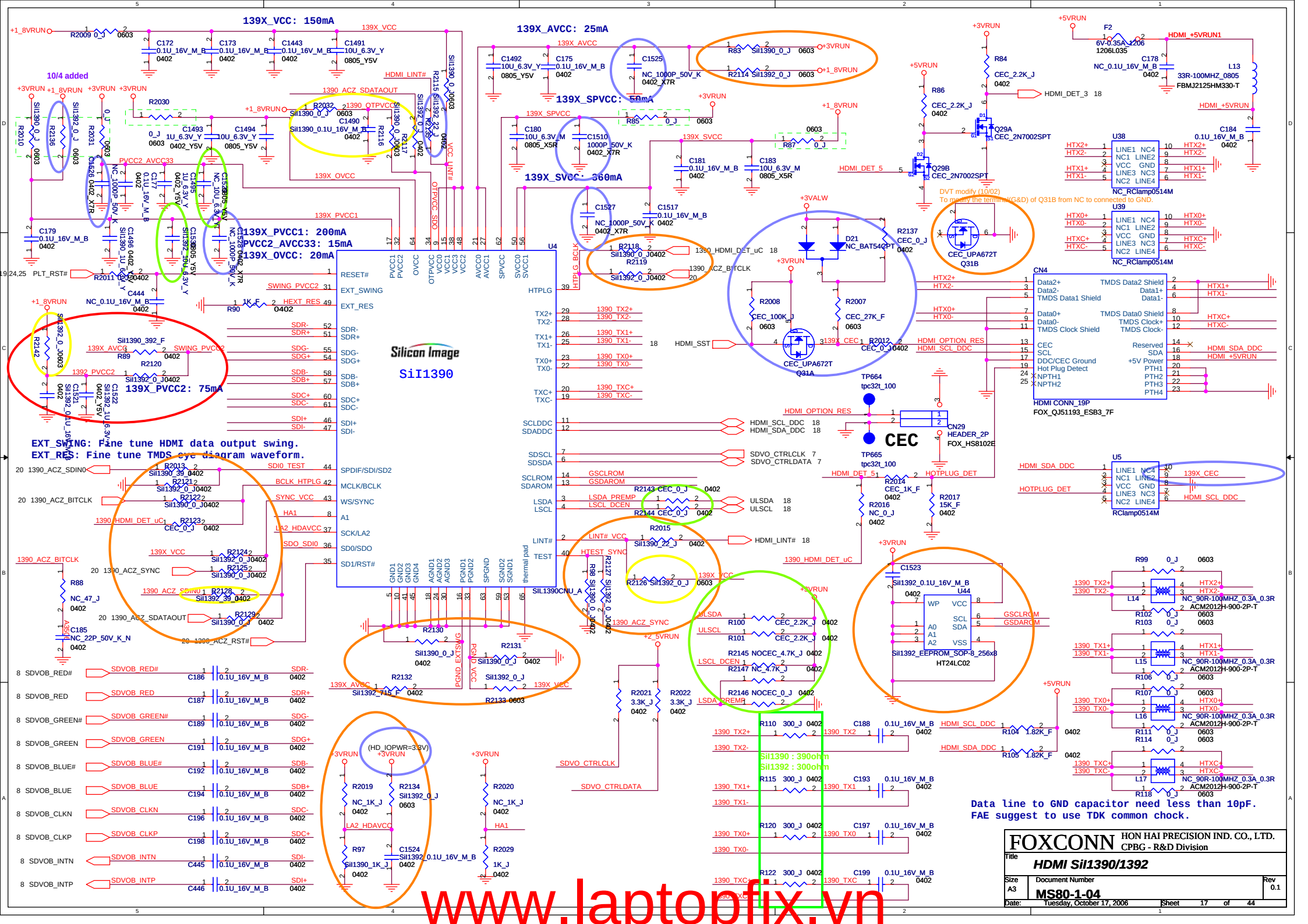
DVT modify -10/12
To exactly match the characteristic impedance of the SYNC lines , added this 2pcs series resistor for fine tune.



DVT modified
Connector color changed
Pin10 connected to GND for SONY SPEC



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: CRT		
Size: A3	Document Number: MS80-1-04	Rev: 0.1
Date: Tuesday, October 17, 2006	Sheet 16 of 44	


139X_VCC: 150mA
139X_AVCC: 25mA
139X_SPVCC: 50mA
139X_SVCC: 360mA
139X_PVCC1: 200mA
PVCC2_AVCC33: 15mA
139X_OVCC: 20mA
139X_PVCC2: 75mA
10/4 added
Silicon Image
SiI1390
EXT_SWING: Fine tune HDMI data output swing.
EXT_RES: Fine tune TMDS eye diagram waveform.
CEC
DVT modify (10/02)
To modify the terminal(G&D) of Q31B from NC to connected to GND.
Data line to GND capacitor need less than 10pF.
FAE suggest to use TDK common chock.
Sii1390 : 390ohm
Sii1392 : 300ohm
(HD_IOPWR=3.3V)
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FOXCONN
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
HDMI Sii1390/1392
MS80-1-04
Tuesday, October 17, 2006
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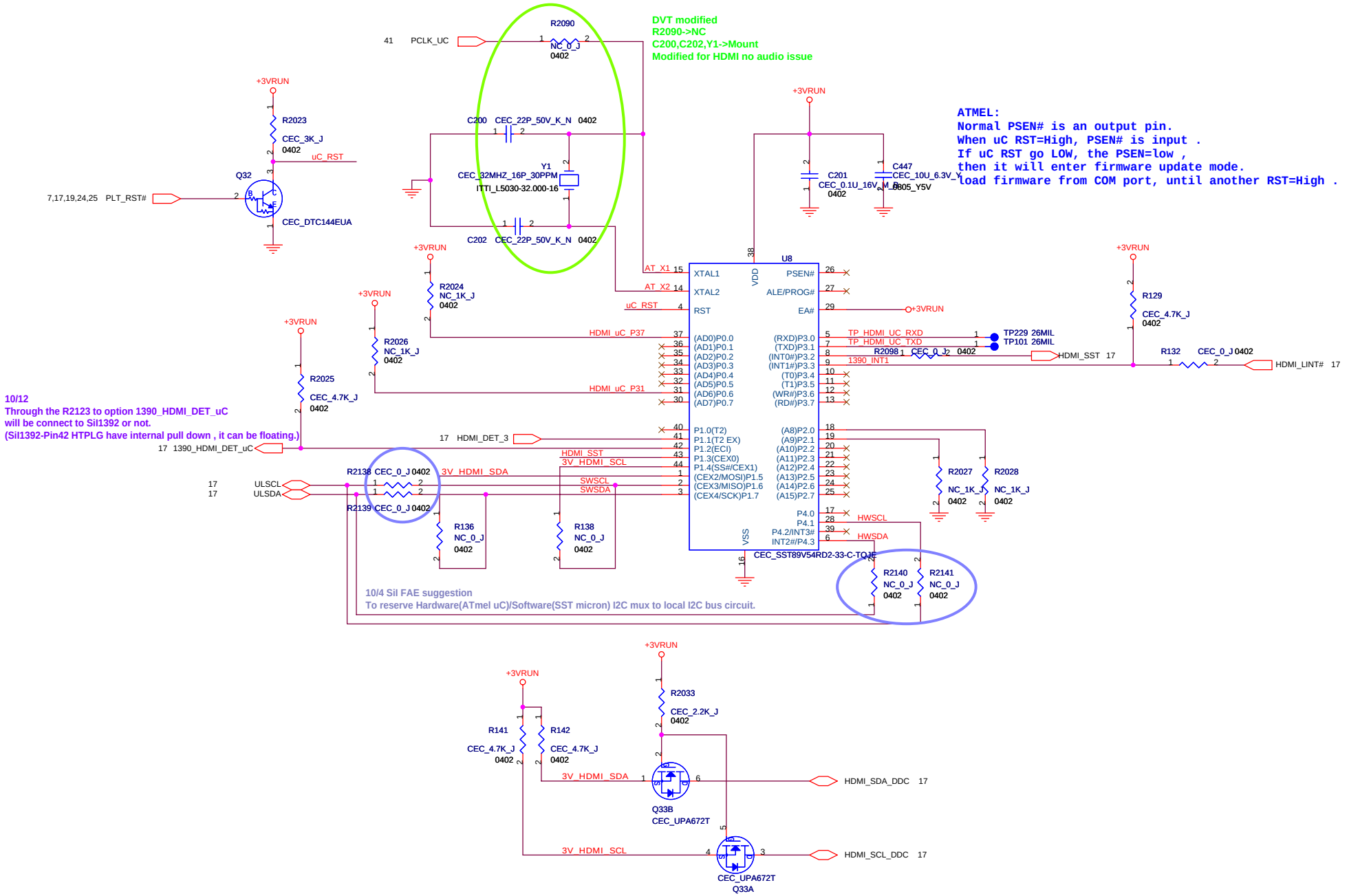

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: HDMI MICROCONTROLLER

Size: A3 | Document Number: MS80-1-04 | Rev: 0.1

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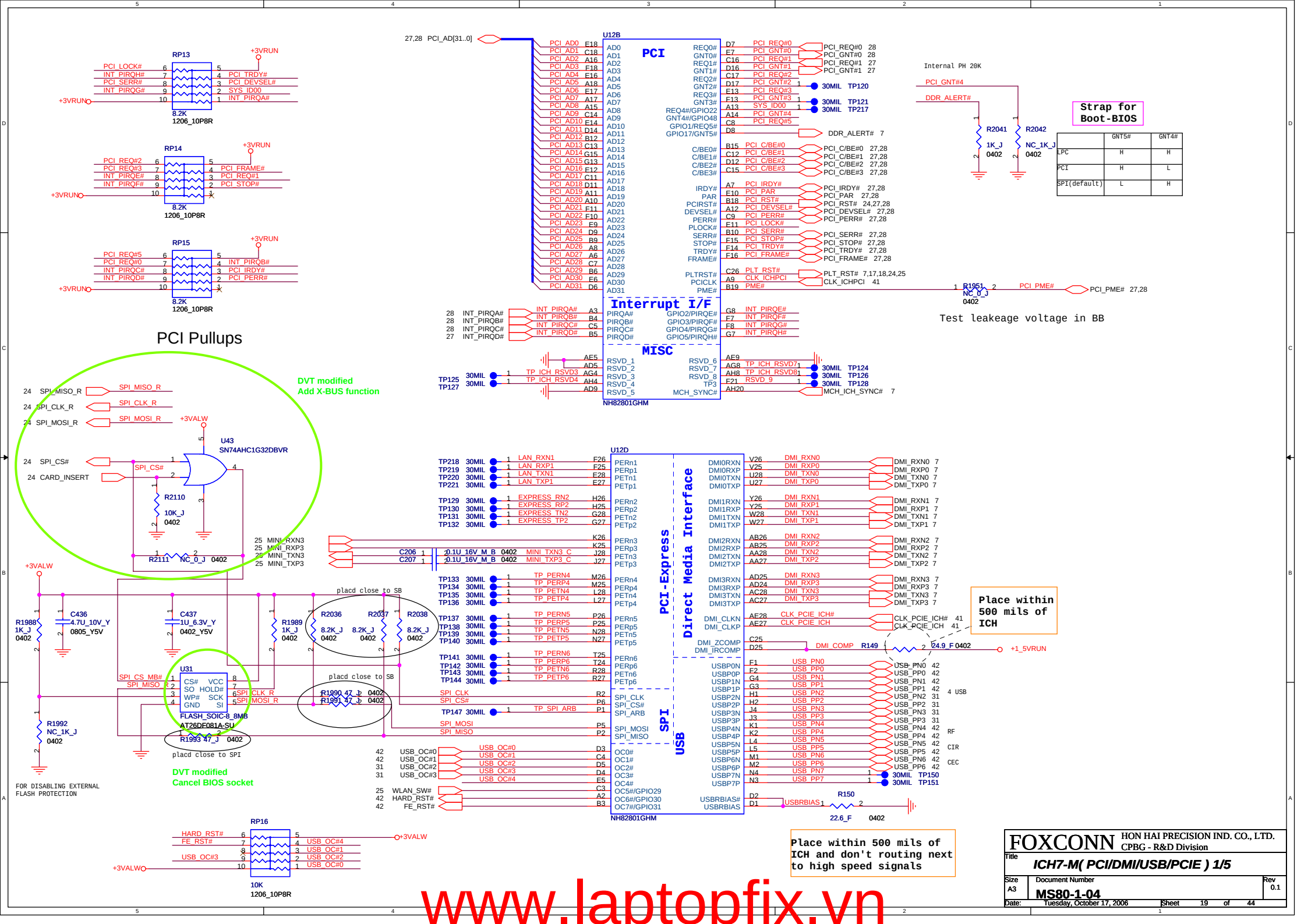
PCI Pullups
RP13
RP14
RP15
RP16
8.2K
1206_10P8R
10K
PCI_LOCK#
INT_PIRQH#
PCI_SERR#
INT_PIRQG#
PCI_TRDY#
PCI_DEVSEL#
SYS_ID00
INT_PIRQA#
PCI_REQ#2
PCI_REQ#3
INT_PIRQE#
INT_PIRQF#
PCI_FRAME#
PCI_REQ#1
PCI_STOP#
PCI_REQ#5
PCI_REQ#0
INT_PIRQC#
INT_PIRQD#
INT_PIRQB#
PCI_IRDY#
PCI_PERR#
+3VRUN
U12B
PCI
Interrupt I/F
MISC
NH82801GHM
27,28 PCI_AD[31..0]
Internal PH 20K
PCI_GNT#4
DDR_ALERT#
R2041
R2042
1K_J
NC_1K_J
0402
Strap for Boot-BIOS
GNT5#
GNT4#
LPC
PCI
SPI(default)
R1951
NC_0_J
PCI_PME#
Test leakeage voltage in BB
DVT modified
Add X-BUS function
U43
SN74AHC1G32DBVR
SPI_MISO_R
SPI_CLK_R
SPI_MOSI_R
SPI_CS#
CARD_INSERT
R2110
10K_J
R2111
NC_0_J
MINI_RXN3
MINI_RXP3
MINI_TXN3
MINI_TXP3
C206
C207
0.1U_16V_M_B
MINI_TXN3_C
MINI_TXP3_C
U12D
PCI-Express
Direct Media Interface
SPI
USB
NH82801GHM
C436
4.7U_10V_Y
0805_Y5V
C437
1U_6.3V_Y
0402_Y5V
R1988
R1989
R2036
R2037
R2038
8.2K_J
placd close to SB
U31
FLASH_SOIC-8_8MB
AT26DF081A-SU
SPI_CS_MB#
SPI_MISO
SPI_CLK_R
SPI_MOSI_R
R1990 47_J
R1991 47_J
R1993 47_J
R1992
NC_1K_J
placd close to SPI
FOR DISABLING EXTERNAL FLASH PROTECTION
DVT modified
Cancel BIOS socket
HARD_RST#
FE_RST#
USB_OC#3
R150
22.6_F
Place within 500 mils of ICH
Place within 500 mils of ICH and don't routing next to high speed signals
FOXCONN
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
ICH7-M(PCI/DMI/USB/PCIE) 1/5
MS80-1-04
Rev 0.1
Tuesday, October 17, 2006
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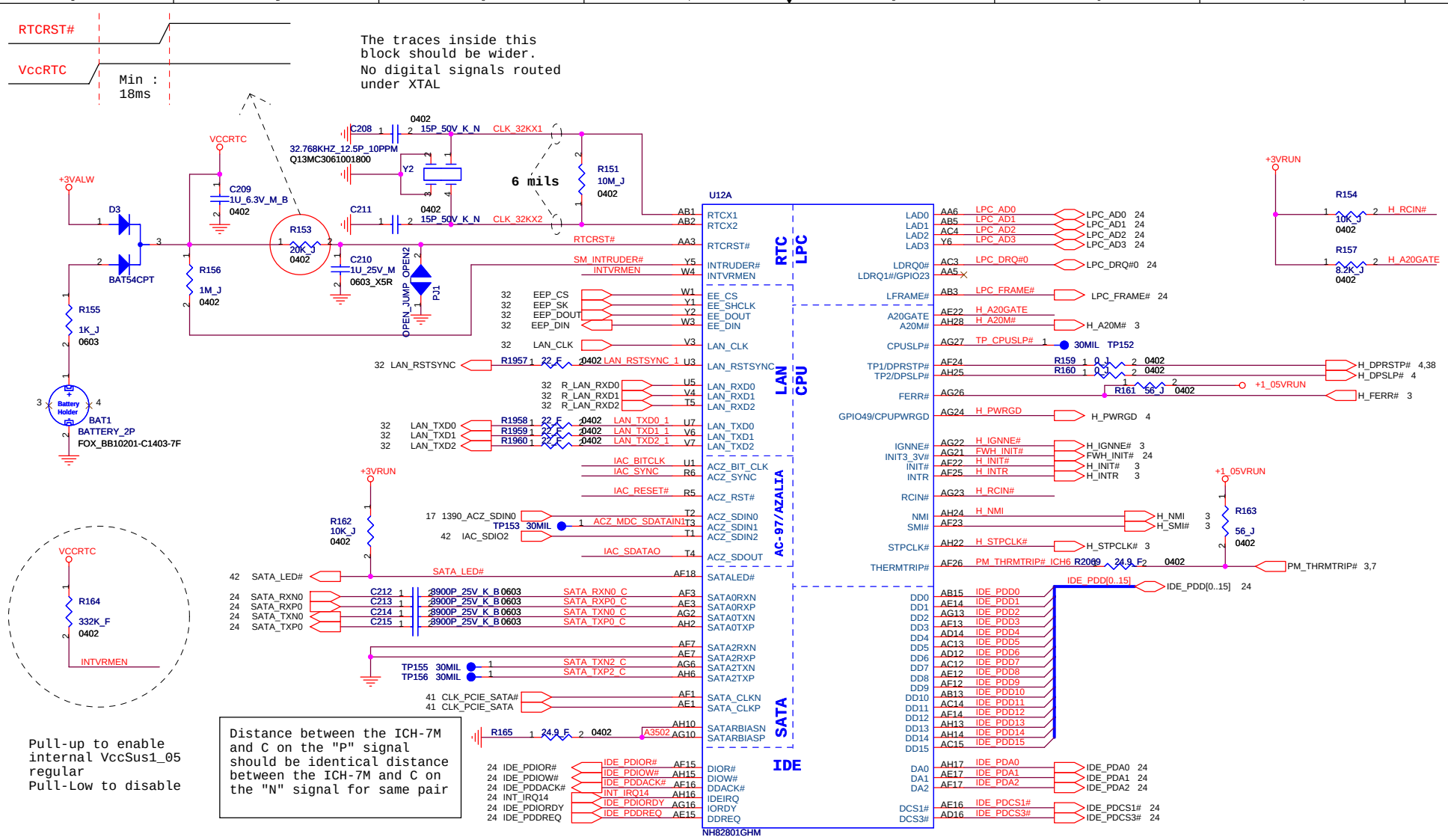

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	ICH7-M(LPC,IDE,SATA) 2/5
Size A3	Document Number MS80-1-04
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Date:	Tuesday, October 17, 2006
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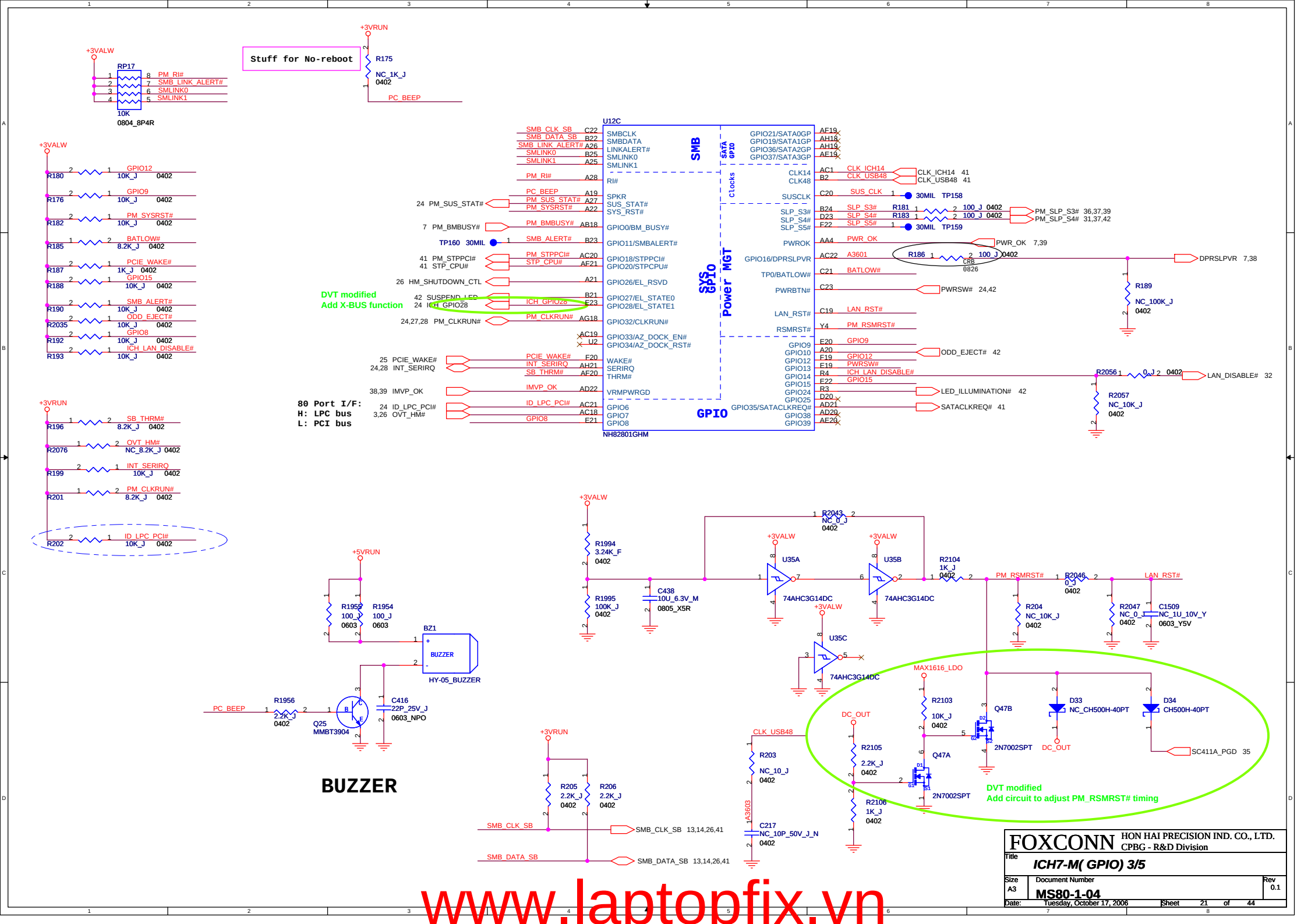

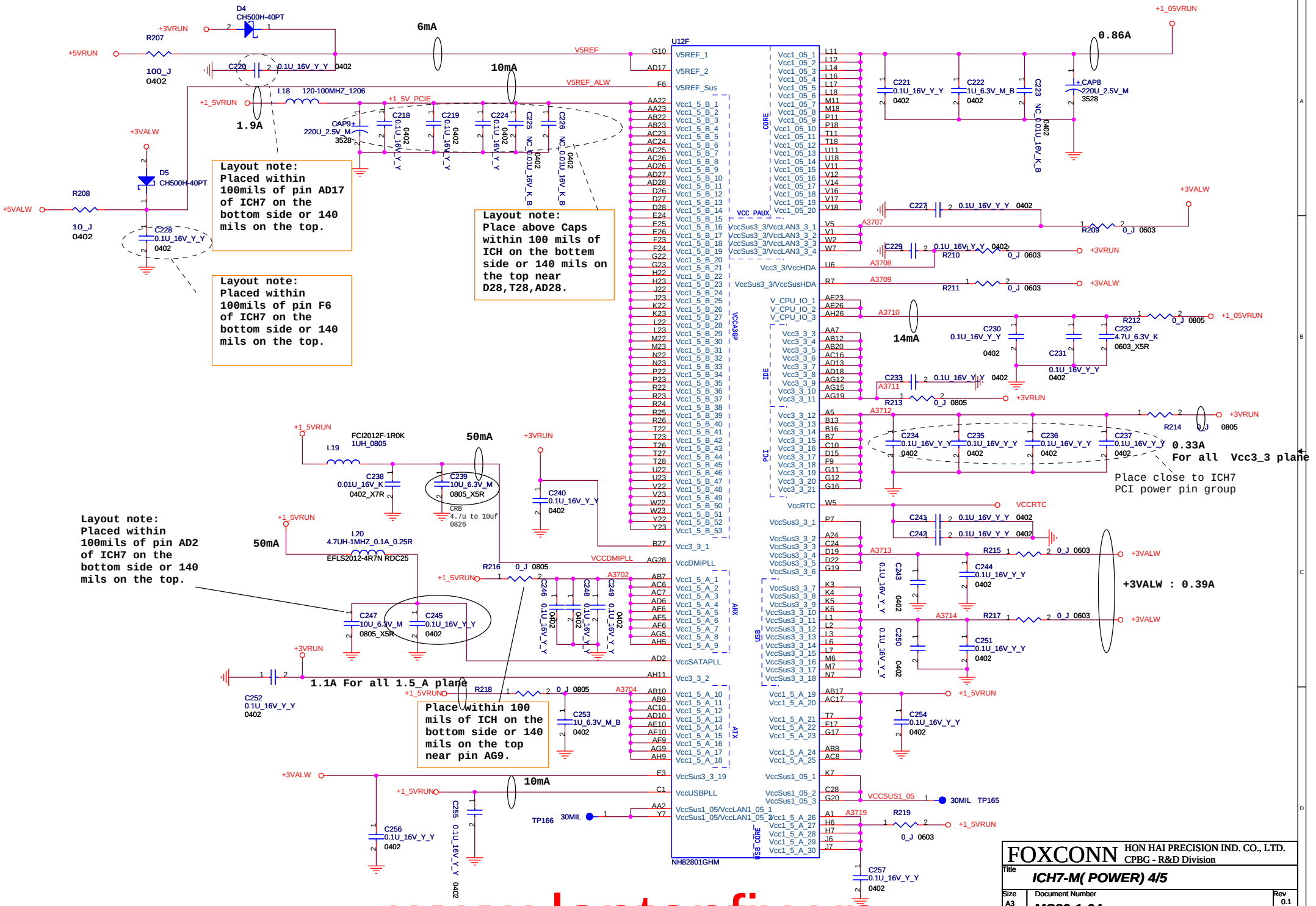

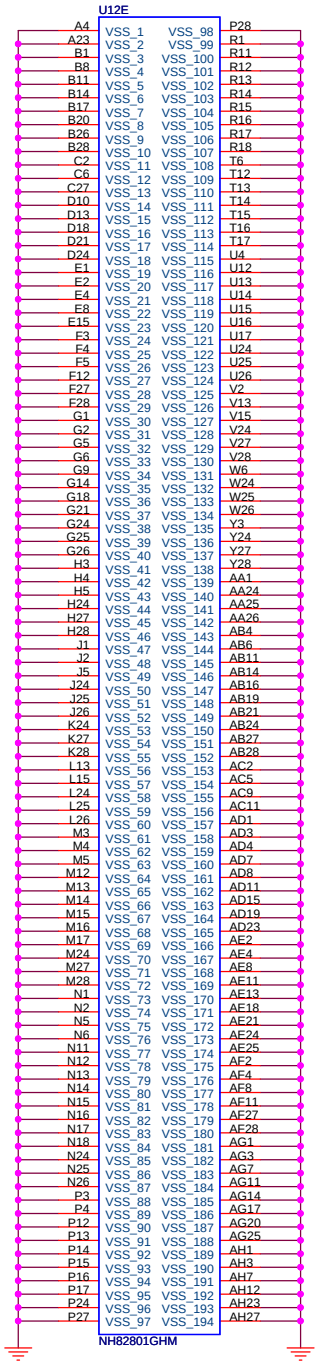

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: *ICH7-M(GND) 5/5*

Size: A3 | Document Number: **MS80-1-04** | Rev: 0.1

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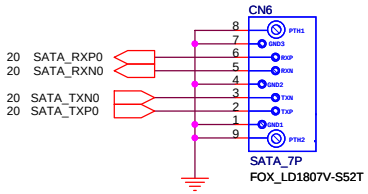
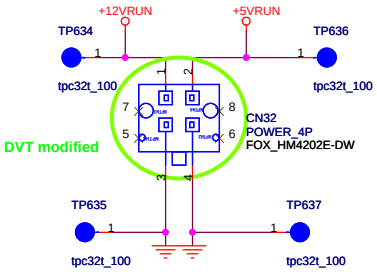
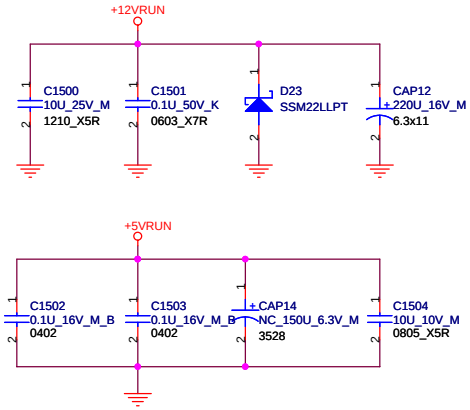
SATA HDD CONN

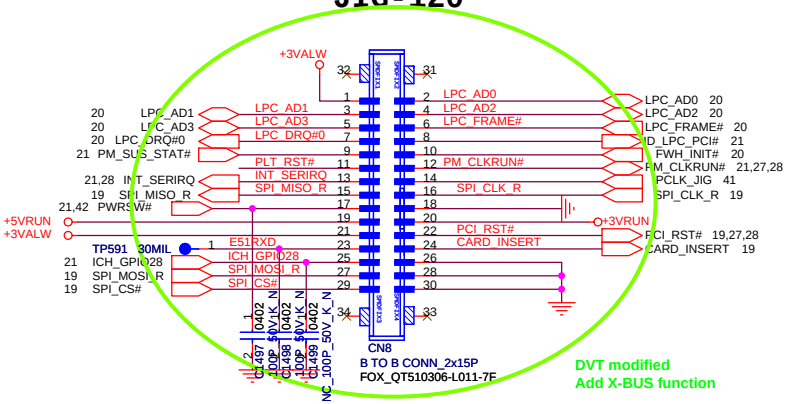


SATA HDD PWR

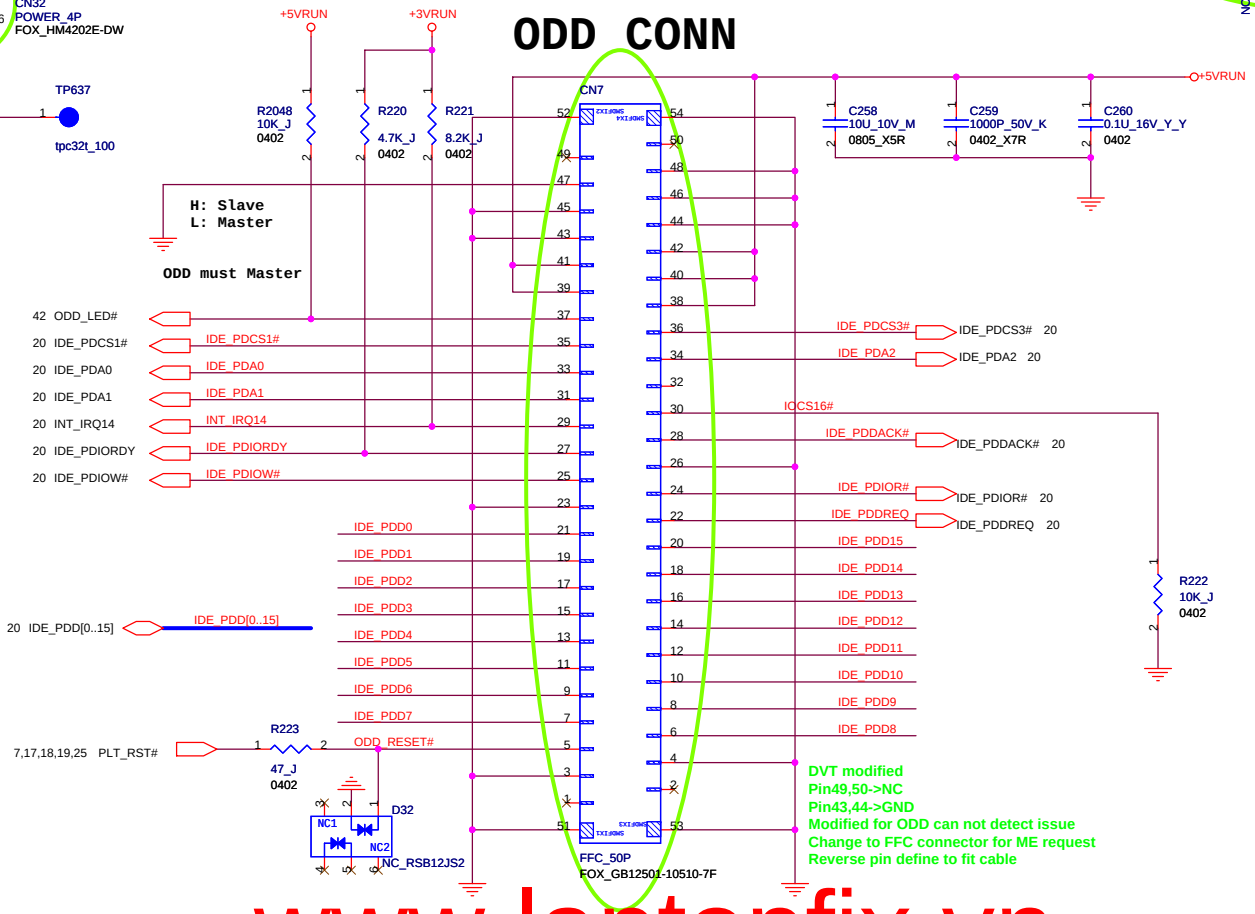




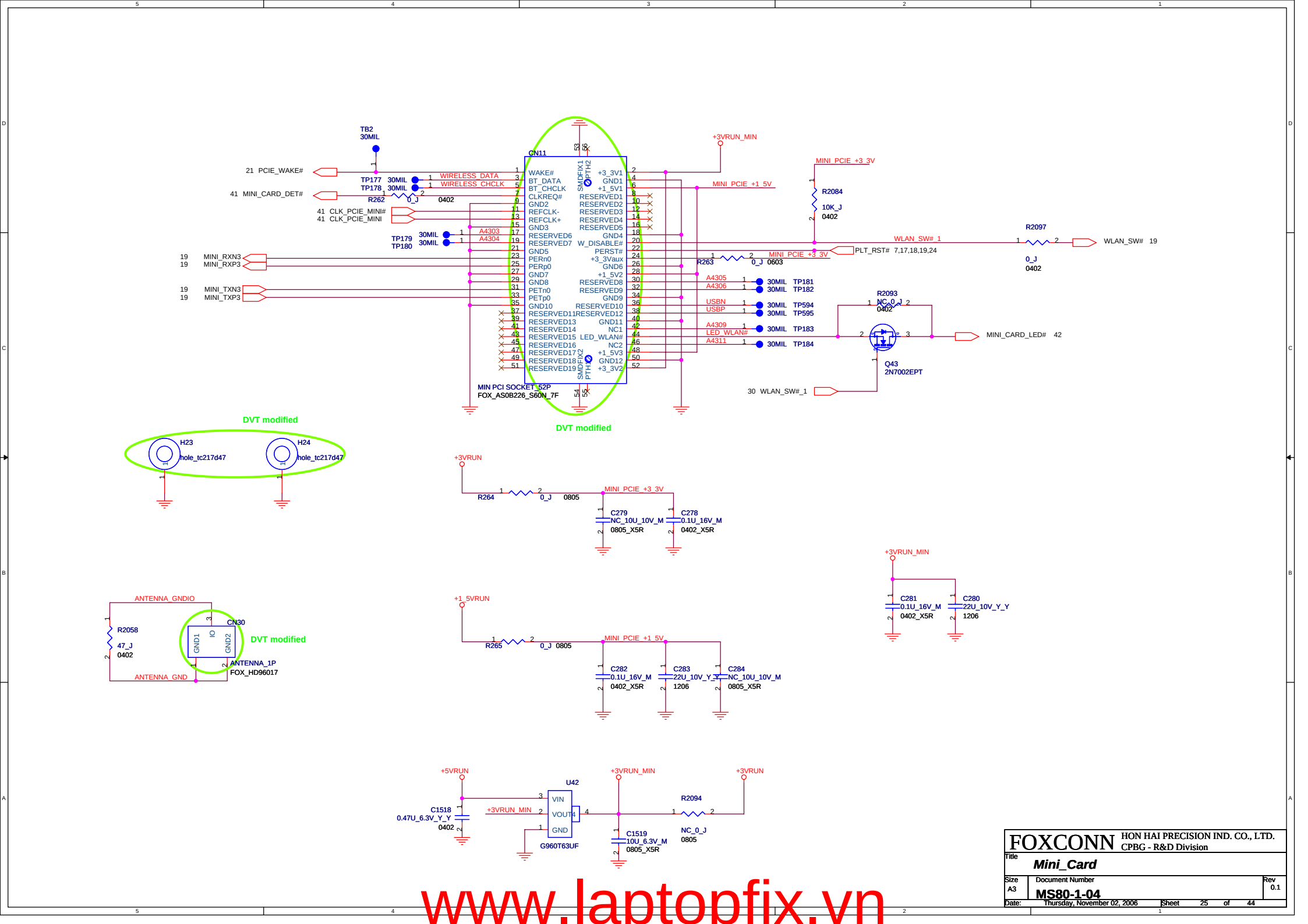
JIG-120



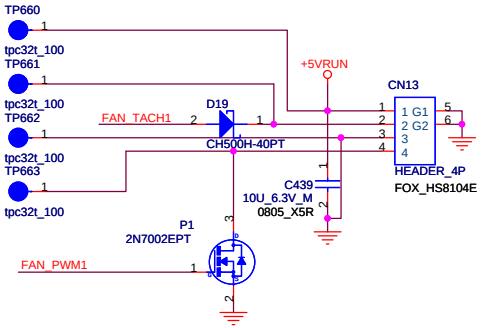
ODD CONN



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	SATA HDD/CD-ROM/DEBUGPORT	
Size A3	Document Number MS80	Rev 0.1
Date: Wednesday, October 18, 2006	Sheet 24 of 44	

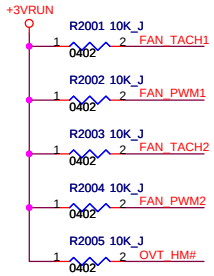


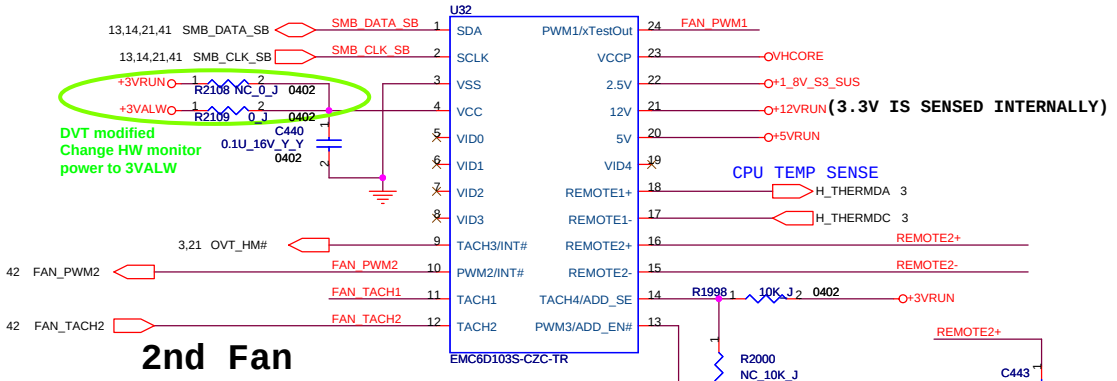
FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	*Mini_Card*
Size A3	Document Number **MS80-1-04** Rev 0.1
Date: Thursday, November 02, 2006	Sheet 25 of 44



CPU FAN CONN

CHECK PIN DEFINITION WITH THERMAL TEAM





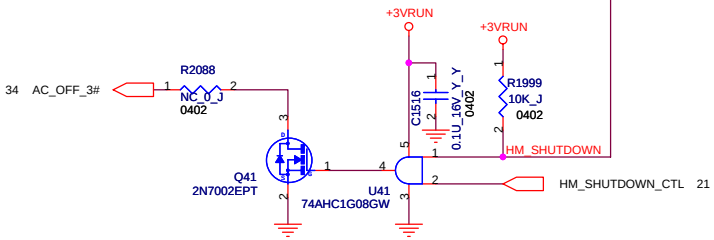
DVT modified
Change HW monitor power to 3VALW

(3.3V IS SENSED INTERNALLY)

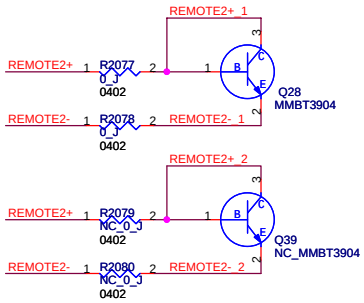
CPU TEMP SENSE

2nd Fan

HW MONITOR

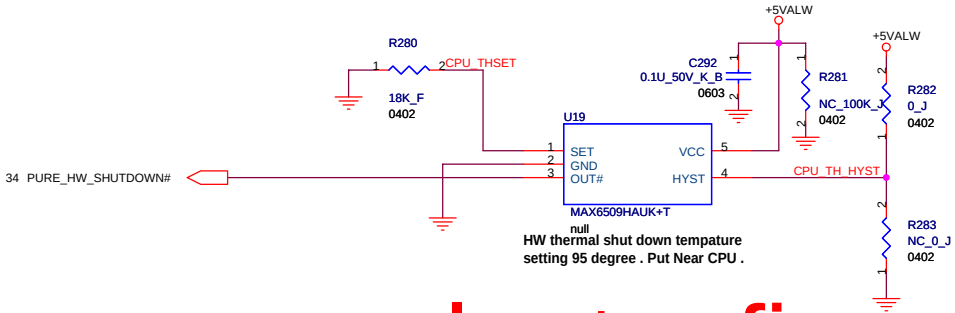


SYSTEM TEMP SENSE



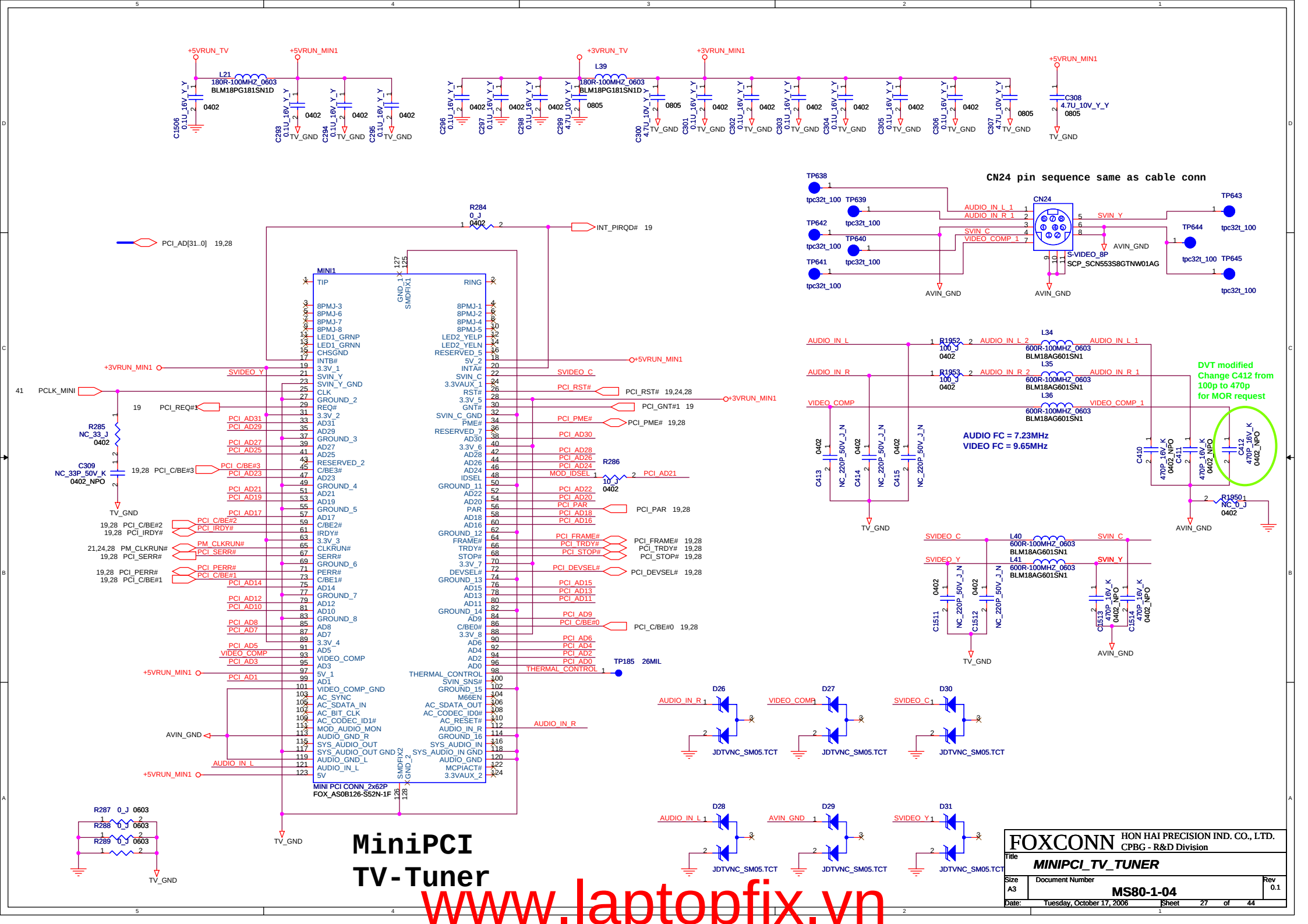
For 0 degaree to +125 degree
Rset(kohm)=[(8.3793 x 10000)/T]-211.3569+[(1.2989 x 100000)/ T x T]
T=kelvin temperature

HW THERMAL PROTECTION



HW thermal shut down tempature setting 95 degree . Put Near CPU .

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	HWMONITOR/FAN/HWPROTECT	
Size A3	Document Number MS80-1-04	Rev 0.1
Date: Tuesday, October 17, 2006	Sheet 26 of 44	


+5VRUN_TV
+5VRUN_MIN1
L21
180R-100MHZ_0603
BLM18PG181SN1D
+3VRUN_TV
+3VRUN_MIN1
L39
CN24 pin sequence same as cable conn
S-VIDEO_8P
SCP_SCN553S8GTNW01AG
MINI1
MINI PCI CONN_2x62P
FOX_AS0B126-S52N-1F
MiniPCI
TV-Tuner
DVT modified
Change C412 from
100p to 470p
for MOR request
AUDIO FC = 7.23MHz
VIDEO FC = 9.65MHz
JDTVNC_SM05.TCT
FOXCONN
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
MINIPCI_TV_TUNER
MS80-1-04
Tuesday, October 17, 2006
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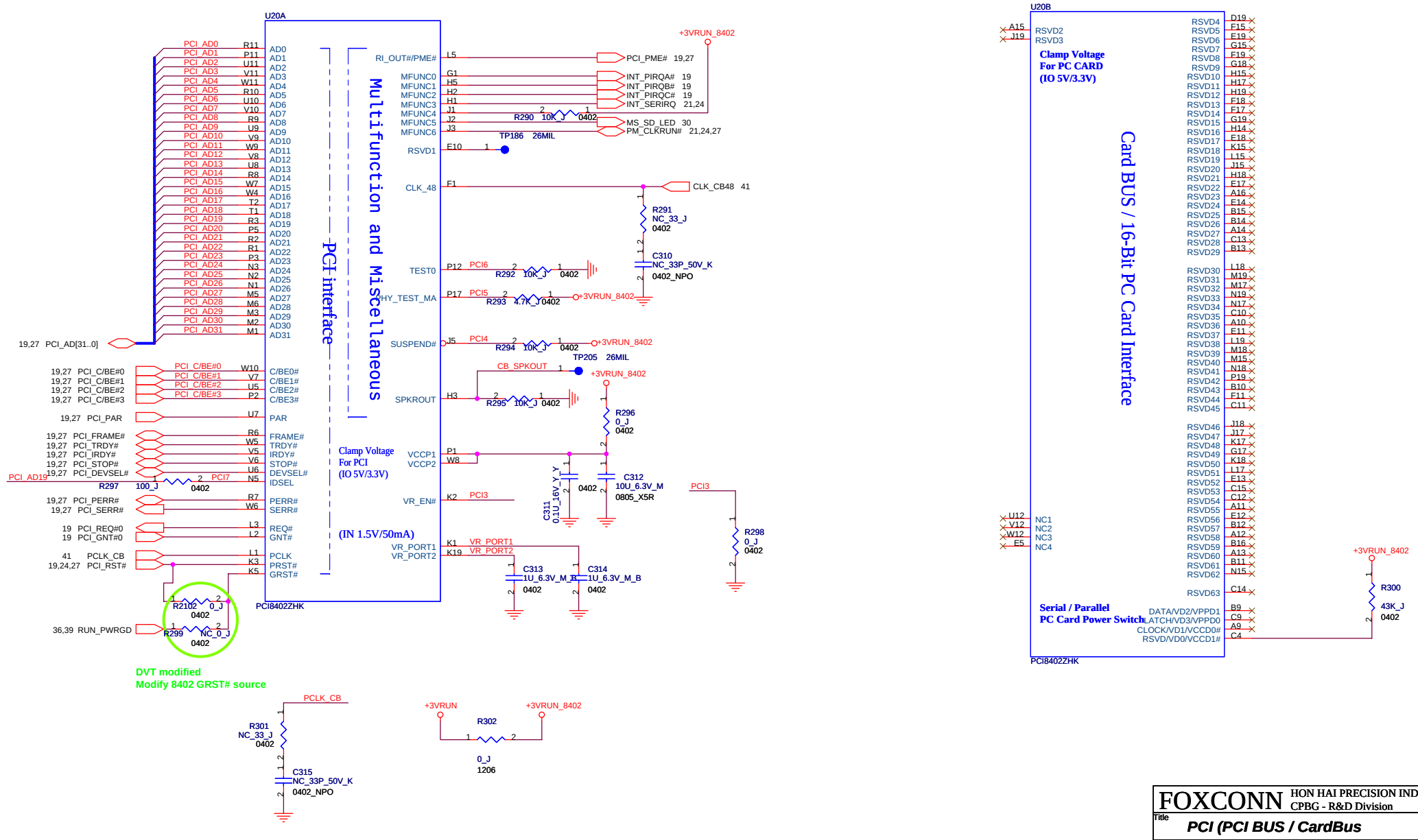
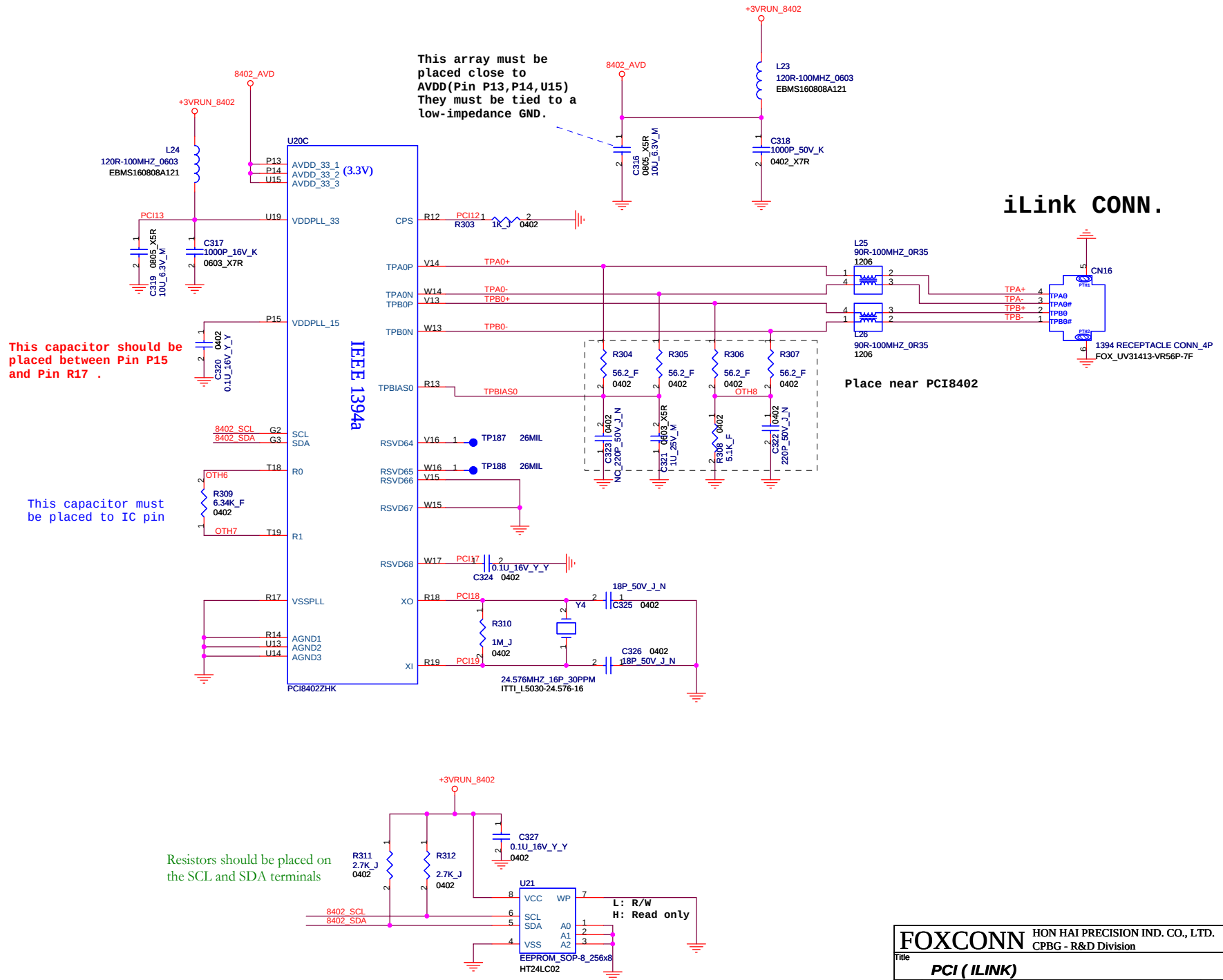
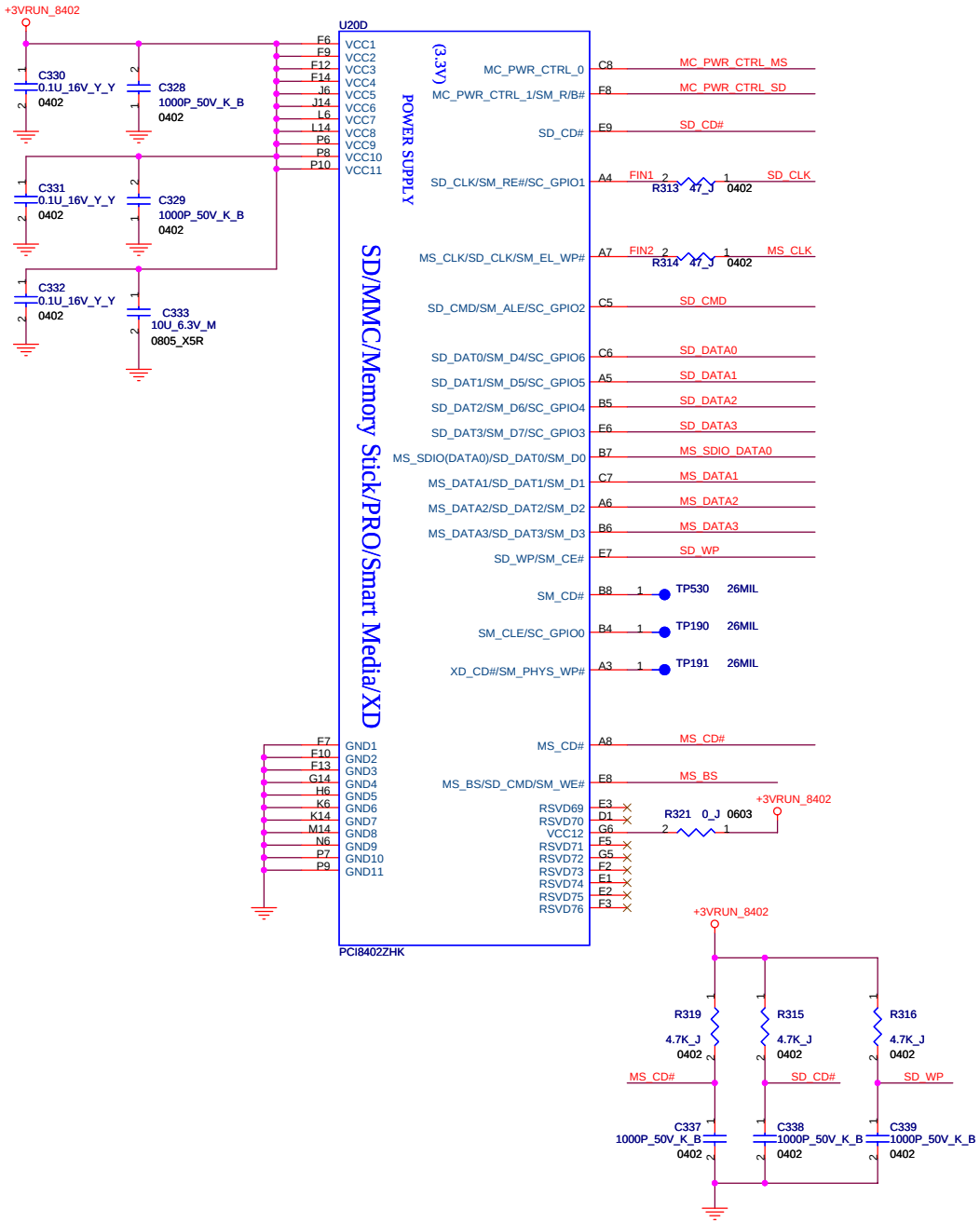
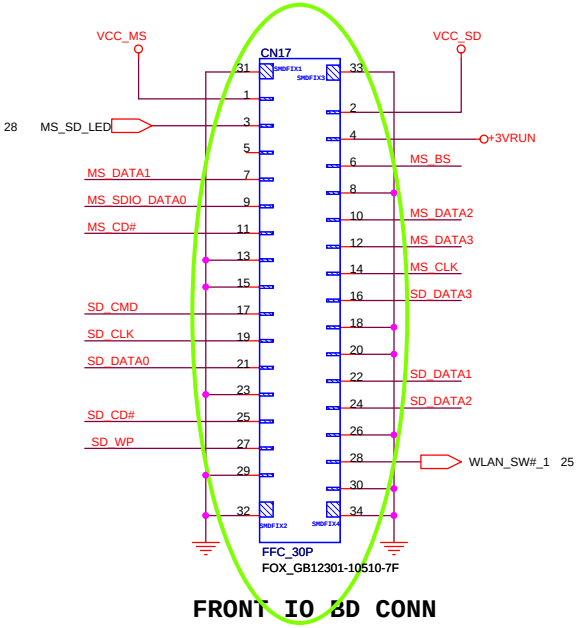


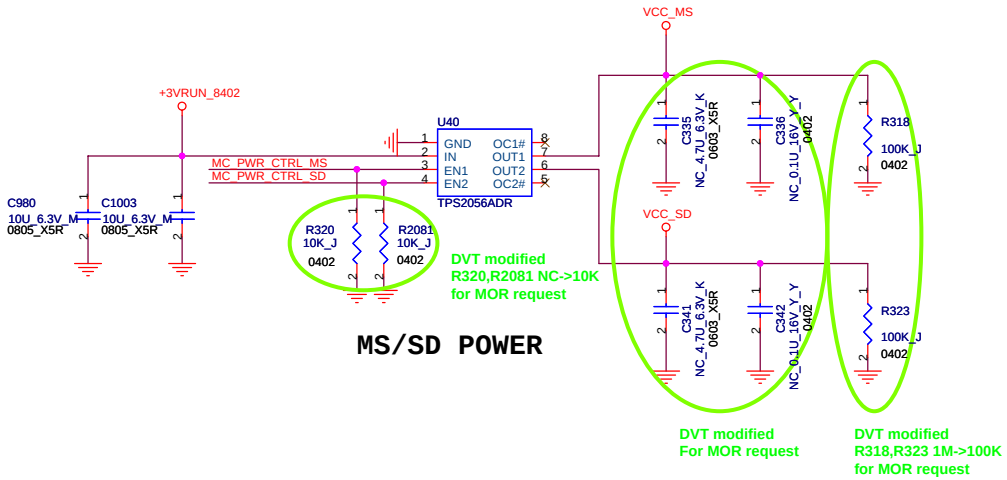
FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	PCI (PCI BUS / CardBus
Size A3	Document Number MS80-1-04
Rev	0.1
Date: Tuesday, October 17, 2006	Sheet 28 of 44



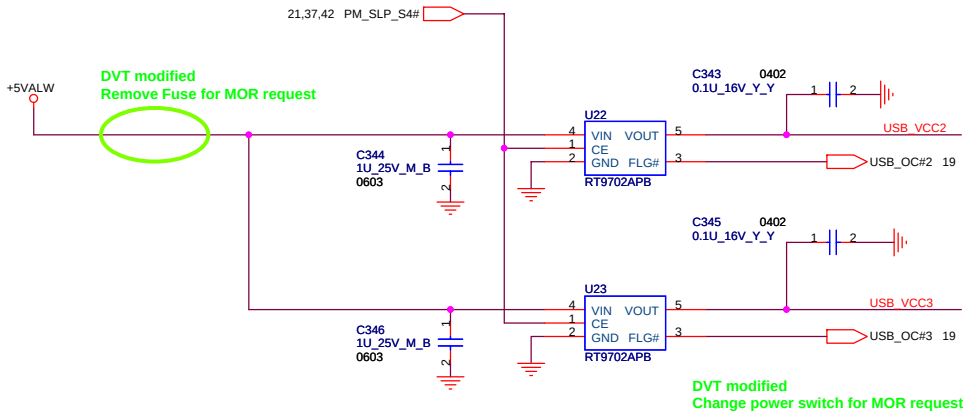
FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	PCI (ILINK)
Size A3	Document Number MS80-1-04
Rev	0.1
Date: Tuesday, October 17, 2006	Sheet 29 of 44



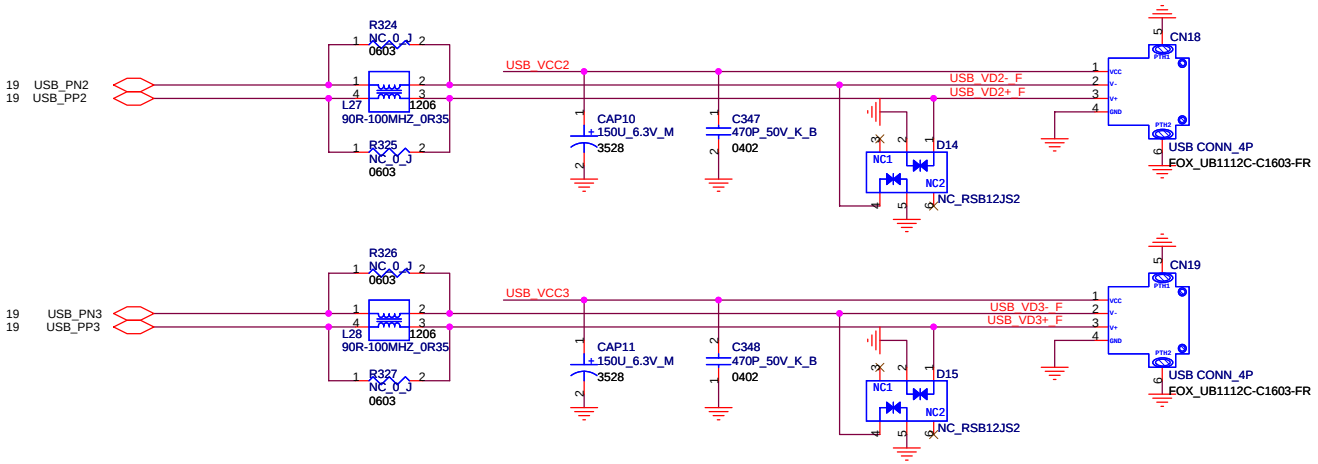




FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	PCI (MS-DUO/SD)	
Size A3	Document Number MS80-1-04	Rev 0.1
Date: Tuesday, October 17, 2006	Sheet 30 of 44	

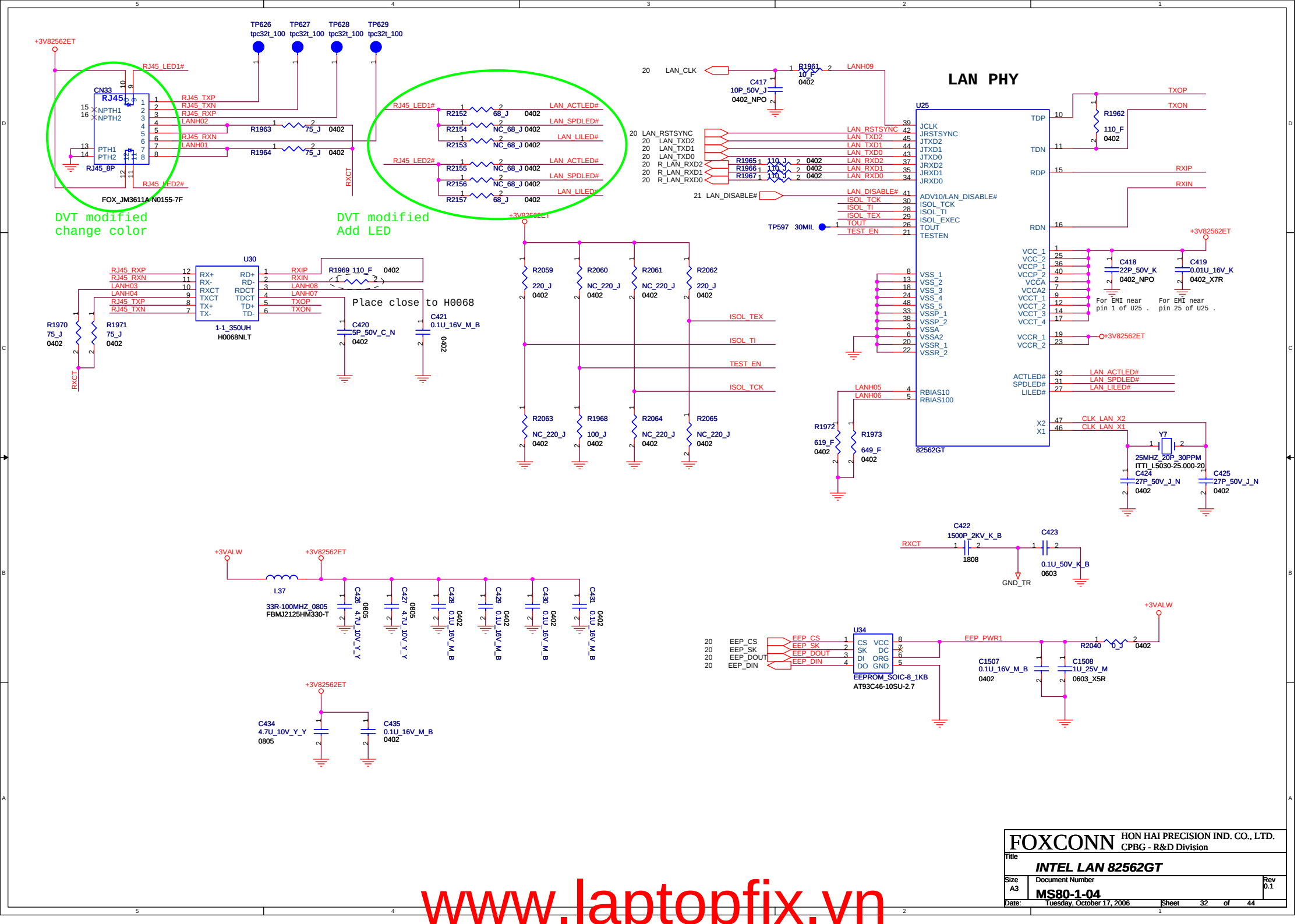


USB Power Switch



USB

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	*USB2.0*	
Size A3	Document Number MS80-1-04	Rev 0.1
Date: Tuesday, October 17, 2006	Sheet 31 of 44	


LAN PHY
DVT modified
change color
DVT modified
Add LED
Place close to H0068
FOX_JM3611A-N0155-7F
RJ45_8P
1-1_350UH
H0068NLT
82562GT
EEPROM_SOIC-8_1KB
AT93C46-10SU-2.7
25MHZ_20P_30PPM
ITTI_L5030-25.000-20
33R-100MHZ_0805
FBMJ2125HM330-T
For EMI near pin 1 of U25 .
For EMI near pin 25 of U25 .
FOXCONN
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
INTEL LAN 82562GT
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Tuesday, October 17, 2006
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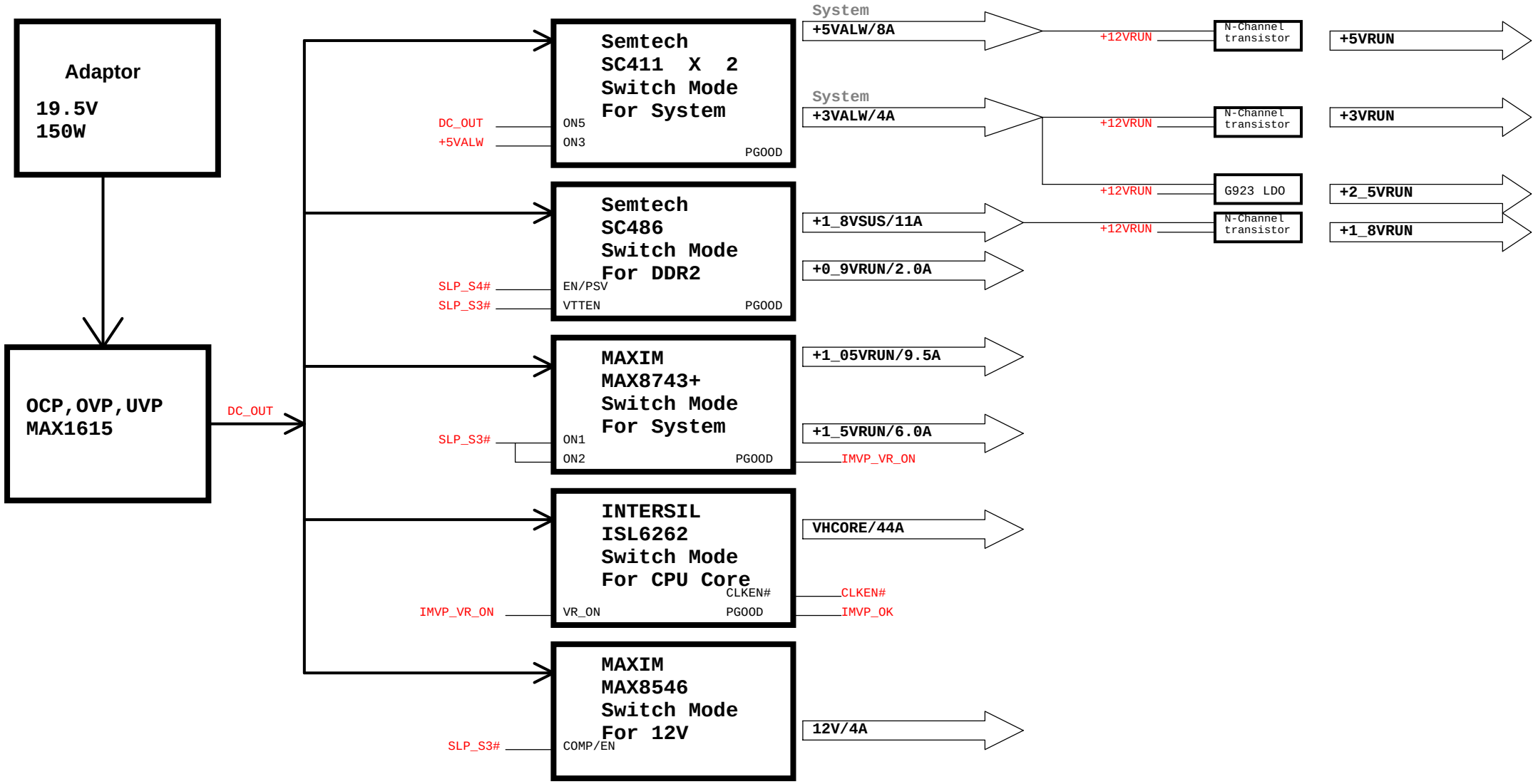
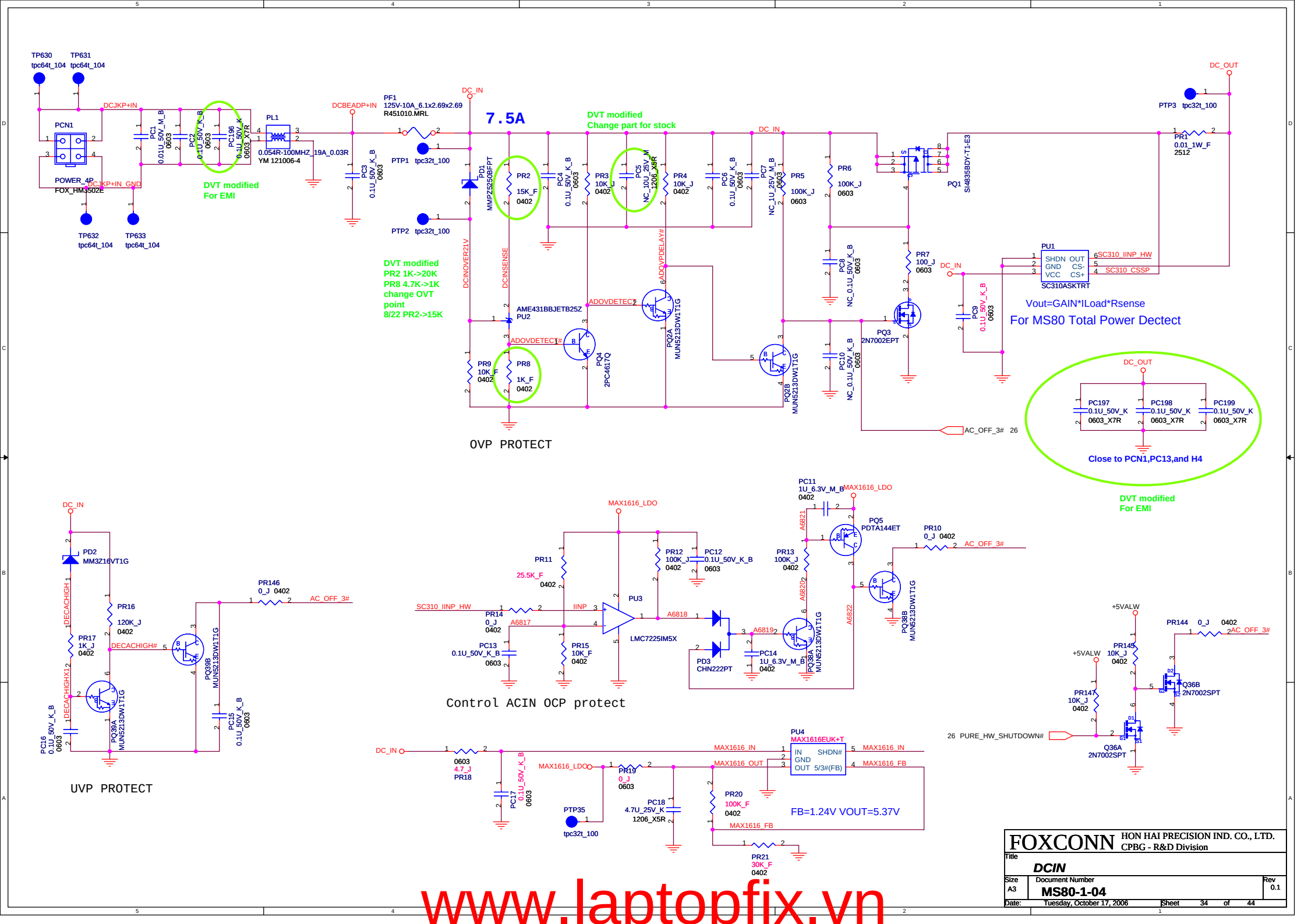
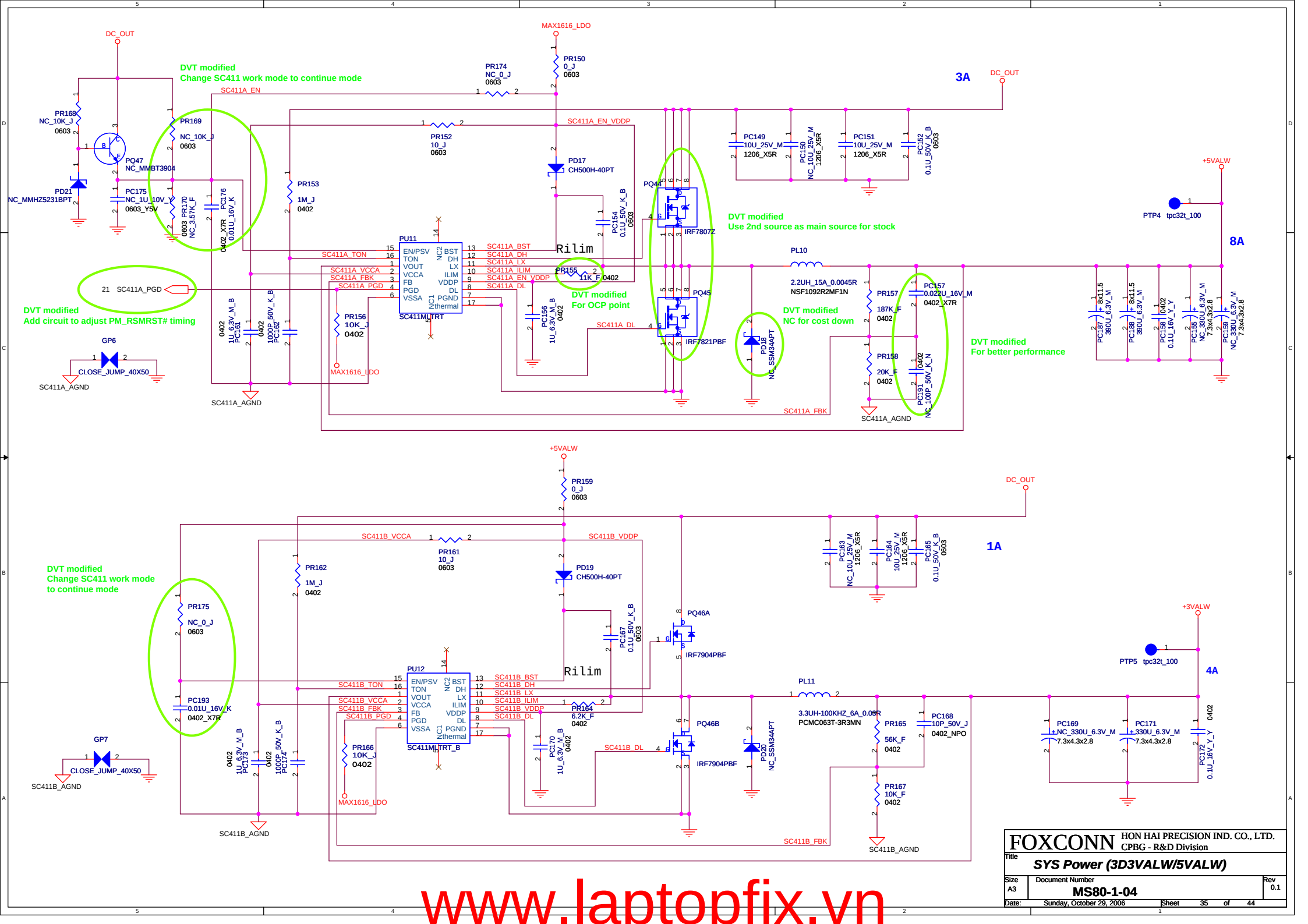
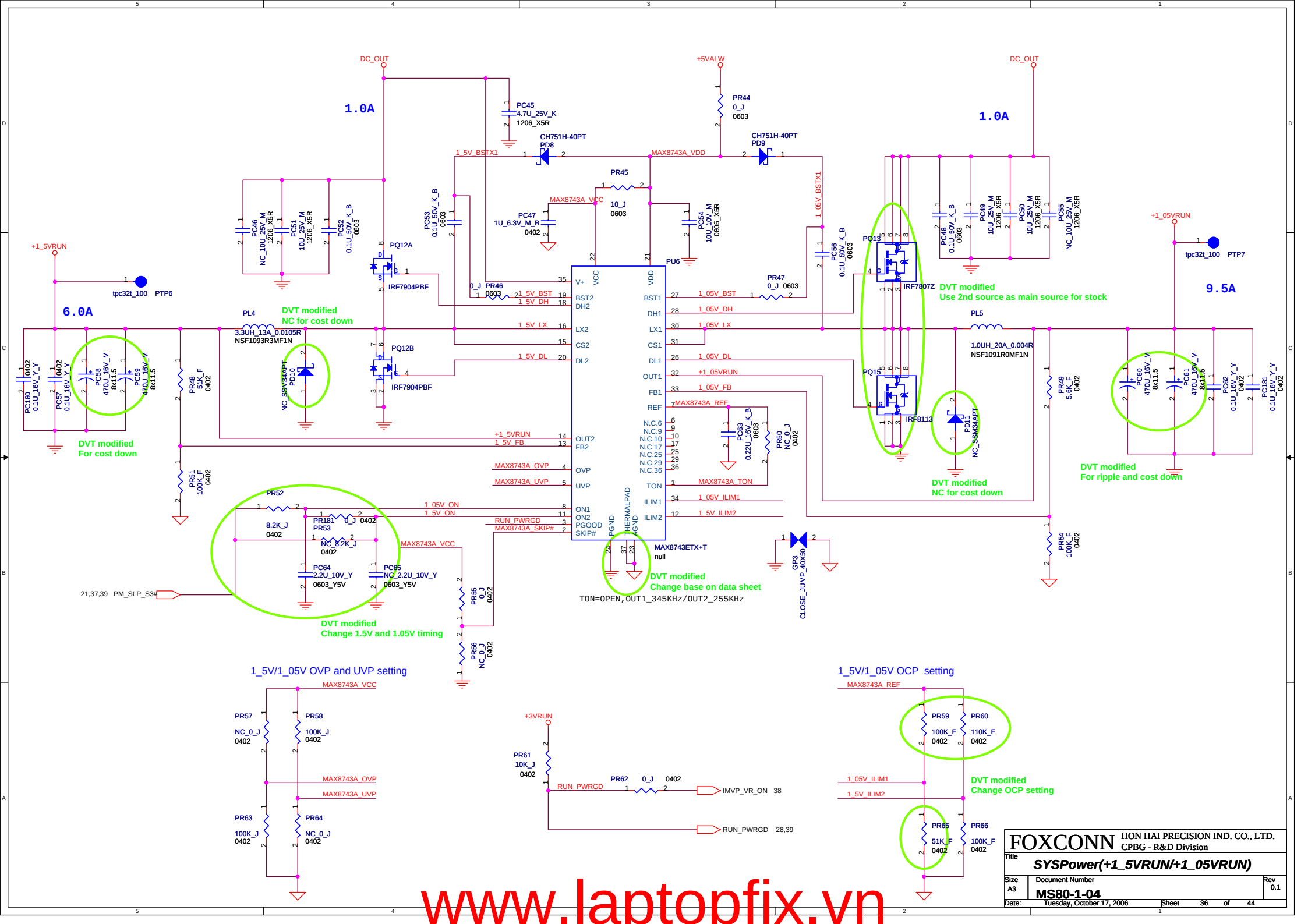


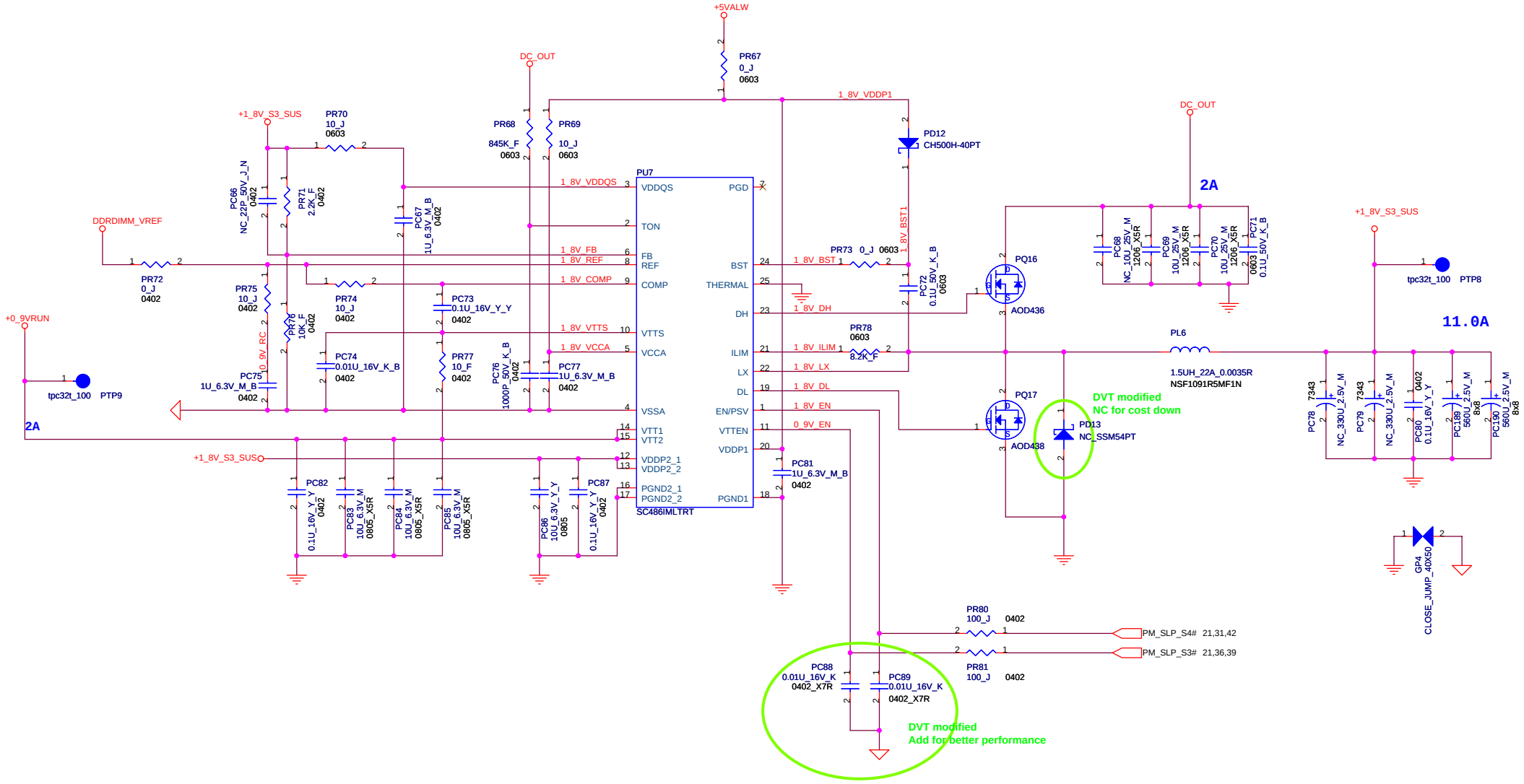
FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: *Power Design Diagram-ZG*		
Size: A3	Document Number: MS80-1-04	Rev: 0.1
Date: Tuesday, October 17, 2006	Sheet 33 of 44	



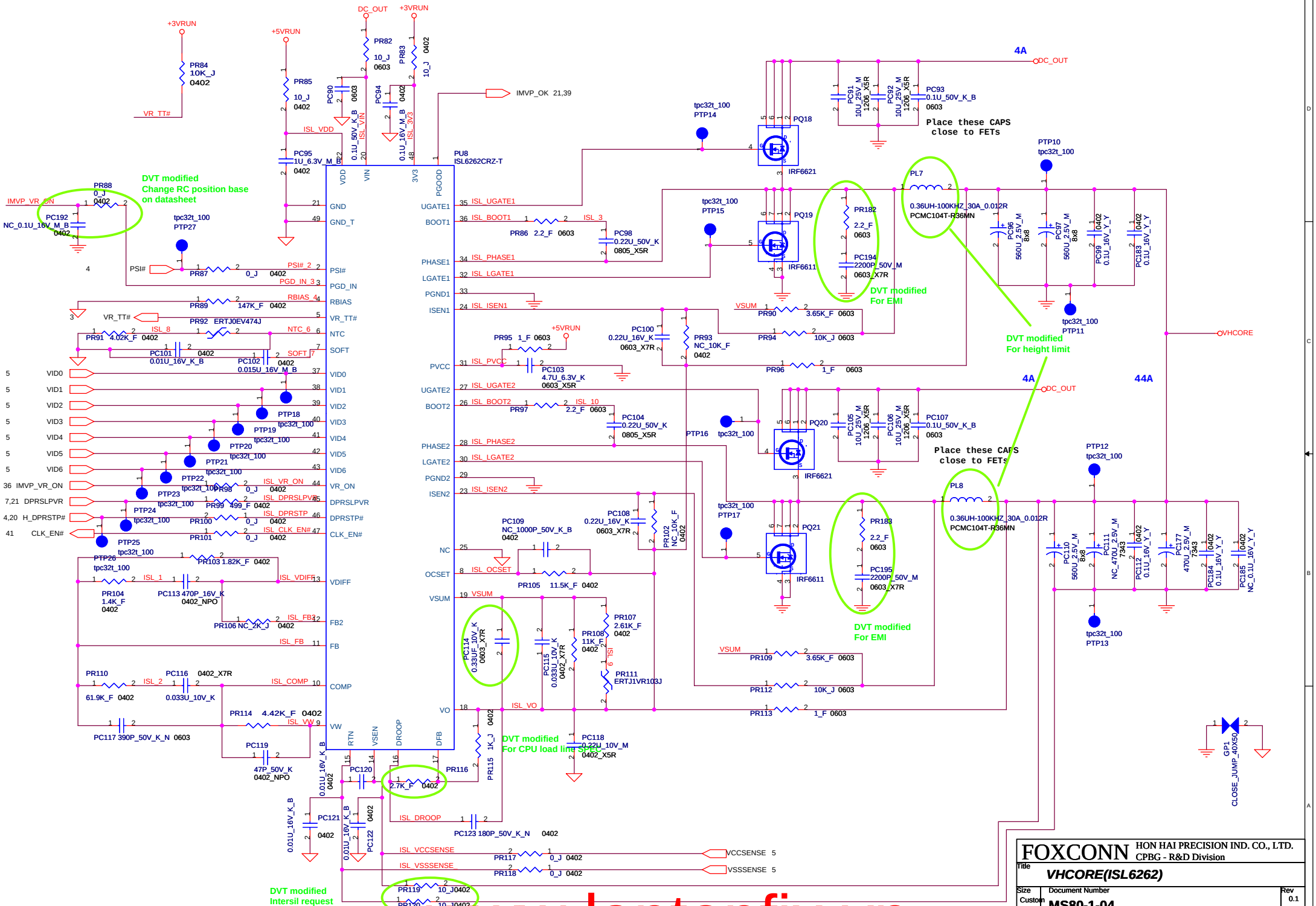
FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	DCIN	
Size A3	Document Number MS80-1-04	Rev 0.1
Date: Tuesday, October 17, 2006	Sheet 34 of 44	







FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	DDR2Power(+1_8V_S3_SUS/+0_9VRUN)	
Size A3	Document Number MS80-1-04	Rev 0.1
Date: Tuesday, October 17, 2006	Sheet 37 of 44	



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Title: VHCORE(ISL6262)

Size: Custom | Document Number: MS80-1-04 | Rev: 0.1

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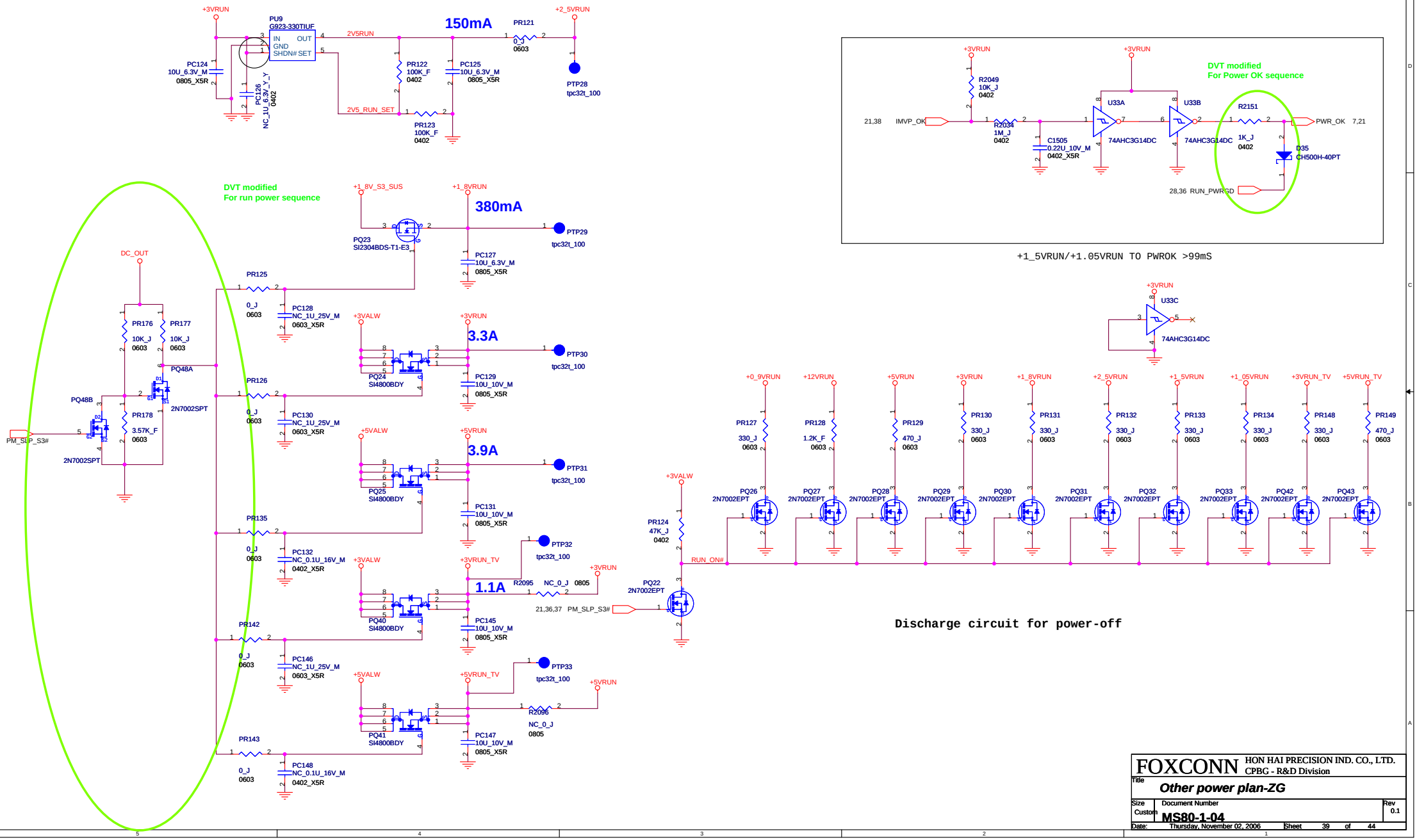
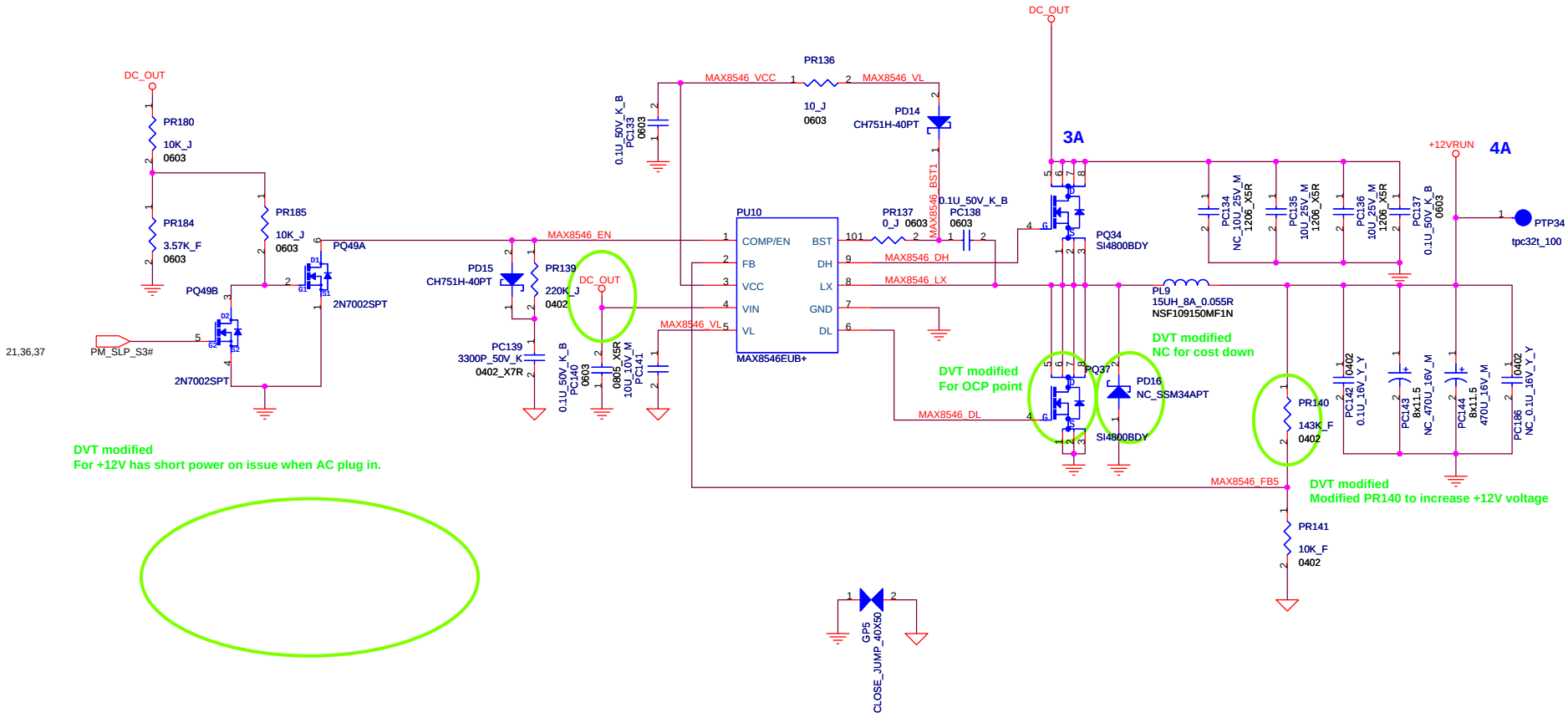
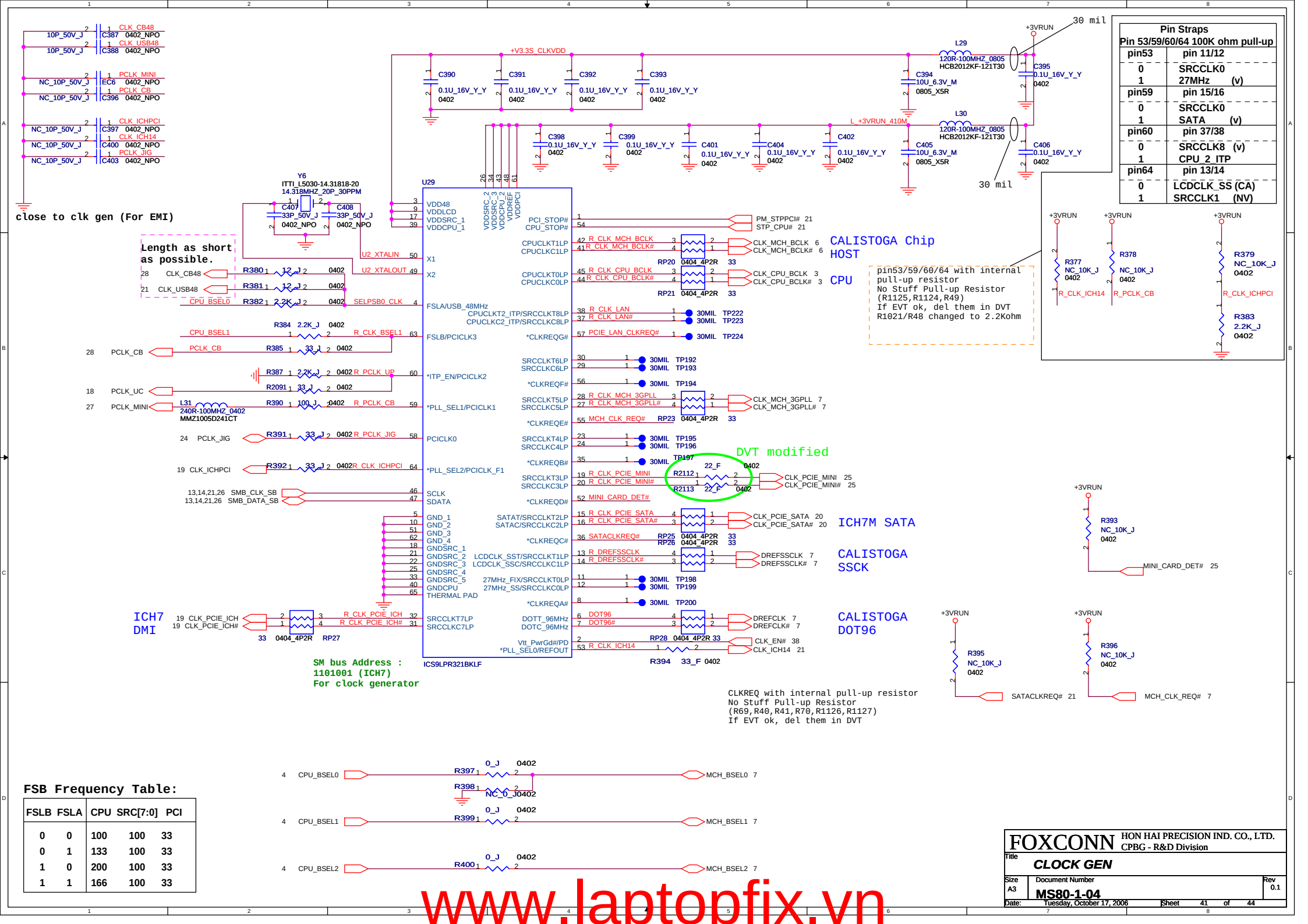




FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	*+12VRUN POWER(MAX8546)*	
Size A3	Document Number **MS80-1-04**	Rev 0.1
Date: Tuesday, October 17, 2006	Sheet 40 of 44	



Pin Straps Pin 53/59/60/64 100K ohm pull-up	
pin53	pin 11/12
0	SRCCLK0 27MHz (v)
1	
pin59	pin 15/16
0	SRCCLK0 SATA (v)
1	
pin60	pin 37/38
0	SRCCLK8 (v)
1	CPU_2_ITP
pin64	pin 13/14
0	LCDCLK_SS (CA)
1	SRCCLK1 (NV)

FSB Frequency Table:

FSLB	FSLA	CPU	SRC[7:0]	PCI
0	0	100	100	33
0	1	133	100	33
1	0	200	100	33
1	1	166	100	33

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	CLOCK GEN
Size A3	Document Number MS80-1-04 Rev 0.1
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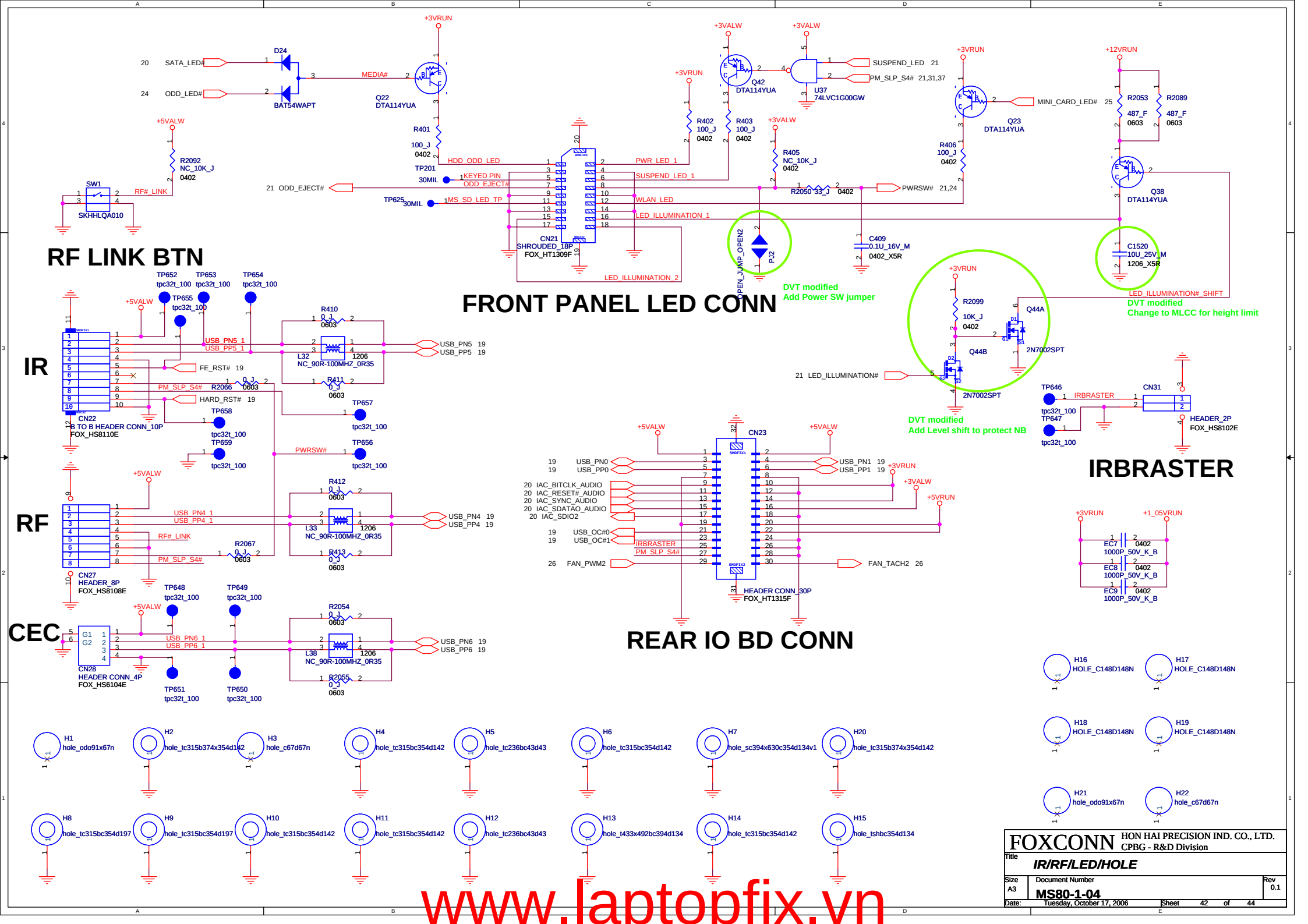
RF LINK BTN
FRONT PANEL LED CONN
IR
RF
CEC
REAR IO BD CONN
IRBRASTER
DVT modified
Add Power SW jumper
DVT modified
Change to MLCC for height limit
DVT modified
Add Level shift to protect NB
FOXCONN
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
Title
IR/RF/LED/HOLE
Size
A3
Document Number
MS80-1-04
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0.1
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HISTORY
REV.: 0.10 (2006/07/18)

0718
P19,P21 change ODD_EJECT# from GPIO5 to GPIO10
P21 change SUSPEND_LED# from GPIO8 to GPIO25
P21 delete GPIO9 SB_RST#
P19 add GPIO17 as DDR_ALERT#

change thermal policy
P34,P3 delete PR173,Q35A,Q35B,PR171,PR172 and connect OVT_HM# to VR_TT# by adding R2087
P26,P21 add R2088,Q41,U41,C1516 and HM_SHUTDOWN_CTL(GPIO26) for thermal policy

P27 add R287,R288,R289 for TV_GND

0719
P13-15 swap DDR signals for layout]
P42 change R2052,R2053,R2082,R2083 from 0ohm to 150 ohm
P42 connect CN22,CN27 pin4 to PM_SLP_S4# for anykey wake up in S3
P42 update H4,H5,H7,H10,H11,H15 for ME
P42 change R401,R407,R406 to 100ohm
P39 change PC132,PC148 to 0.1u_16v
P39 change PR148 to 330ohm
P21 change SUSPEND_LED from GPIO 25 to GPIO27
P42 add Q42 and change U37 to 74LVC1G00GW for SUSPEND LED

0720
P42 delete R2052,R2082,R2083,Q40 ;add CAP16 for ILLUMINATION LED
P38 reserve PC177 for VHCORE
P31 change F3 to PTTC SMD1206P110TF
P26 change D19 from 1N4148 to CH500H-40PT for Vf

0721

Vendor review
P17 (1)delete D21,D22,R2018 and short,change Q31 to UPA672 for avoid capacitance effect 500pf for DDC bus
(2)NC U5,U38,U39 pin3 for capacitance concern
(3)change R110,R115,R120,R122 to 390 ohm
P18 (1)R2023 changed from 1K to 3K
(2)Q33A,Q33B changed from 2n7002 to UPA672T for capacitance concern

BOM modify for common parts
P26 U41 change to 74AHC1G08GW.125
P21 change Q25 to MMBT3904(SECOS)
P26 change Q28,Q39 to MMBT3904(SECOS)
P35 change PQ47 to MMBT3904(SECOS)
P40 cahnge PC139 to 3300P YAGEO
P39 change R2034 to 10M_J TA-I
P21 change R1956 to 2.2k_J 0402
P17 R2007,R2008 change to 27K_F 0603
P17 R104,R105 change to 1.82k_F 0402
P3 change R2 to 150_F
P3 update R1
P15 update R77,R78,R79,R80
P20 update R163,R161

P37 delete PR79 for duplicate with GP4
P42 change R2053 to 931_F and add R2089 for power rating
P6-12 change U2 to 12-0G82945-A300

0724
P41,P18 add R2090,R2091 for 33M clk input of microp from clk gen path
P40 dummy PC134,PC143 by power team
P42 swap L38,L32,L33(mirror veritical) for Layout
p35 change PL11 to 4.7U-100KHZ_5.5A_0.04R(CYNTEC)
P28 change U20A pinJ2 to High active
P42 MS/SD LED move to FIO BOARD, CN21 pin 11 change to test pad
P25 connect WLAN_SW# to CN11 pin20
P18 connect P1.3 to INT0# by customer from vendor suggestion
P26 change CN13(fan) define to pin1~4 +5VRUN,TACH, GND,PWM by thermal team9(compatible with old models)

0725
P35 change PD19,PD20 to SSM34APT and dummy PD20 by power team
P24 update CN17 symbol and vendor P/N
P42 add SW1,R2092 for RF LINK BUTTON
P21 GPIO30 connect to HARD_RST#,GPIO 31 connect to FE_RST#

0726
P17 add C1517,D21 by vendor suggestion
P19 GPIO29 connect to WLAN_SW# for TE
P42 mount CN28

0727
P21 GPIO7 connect to OVT_HM#,NC R2076 for OS shutdown
P38 dummy PC111,mountPC177 by power team
P37 change PC78,PC79 to 560U_2.5V_M (lower hight parts) for layout
P35 change PC169,PC171 to 330U_6.3V_M (NEC) (lower height) for layout
P36 Add PC181 for power ripple noise (for dip caps)
P38 Add PC183,PC184,PC185 for power ripple noise (for dip caps)
P40 add PC186 for power ripple noise (for dip caps)

0728
P38 change PC108 to 0.22u_16V_K 0603 size by power team
P35 change PC155,PC159,PC160 to 330U_6.3V_M ,SMD by power team(semtech)
P37 change PC78,PC70 to 330U_2.5V_M by power team(semtech)
P36 change PQ12 to IRF7904(PQ12A),change PQ14 to IRF7904(PQ12B)

0731
wlan power ldo
(1)add C1518,c1519,U42,by customer request for Intel module susceptibility to ripple noise
(2)MINI_PCIE_+3_3V change to +3VRUn source
wlan led
P25 add Q43,R2093 by customer for avoid LED_WLAN# abnormal behavior from wlan module
P35 remove PC160 by power team

0801
P35 add PC191 by power team(vendor suggestion)
P36 NC PR50 by power team
P38 add PC192 by power team
P35 change PR155 to 16K_F,change PR164 o 6.2K_F for ocp
P36 change PR59 to 110K_F ,PR60 to 68K_F for OCP
P42 add EC7,EC8,EC9 for cpu,nb clk cross moat
P39 add R2095,R2096 for cost down
P25 (1)add R2094 for cost down,
(2)add R2097 by customer request
P17 change R2008 to 100K_J by customer

0803
P18 add R2098 by vendor suggestion
P42 change H13,H14 by ME

0804
P17 change CN29 to HS8102 cause of HS6102 not available

0816
P40 change PR140 from 140K to 143K to increase +12V voltage
P38 change PR119,PR120 from NC to 10ohm for intersil request
P30 change R320,R2081 from NC to 10K,change R318 from 1M to 100K for MOR request to avoid SD/MS issue
P34 change PR2 from 1K to 20K,change PR8 from 4.7K to 1K to change OVP point
P35 change PR155 from 16K to 11K for adjusting OCP point
P36 change PR59 from 110K to 100K,change PR65 from 100K to 51K PR60 from 68K to 110K for adjusting OCP point
P40 change PQ37 from SI4892DYT to SI4800BDY for OCP
P42 add Q44 for level shift of LED_ILLUMINATION#
P40 change PD16 from SSM34APT to NC for cost down
P36 change PD10,PD11 from SSM34APT to NC for cost down
P37 change PD13 from SSM54PT to NC for cost down
P35 change PD18 from SSM34APT to NC for cost down

0817
P24 CN7 Pin49,50->NC;Pin43,44->GND; for ODD can not detect issue
P18 R2090->NC,C200,C202,Y1->Mount; for HDMI no audio issue
P35 PQ44,PQ45 use 2nd source as main source for stock
P36 PQ13,PQ15 use 2nd source as main source for stock

0822
P35 PR169,PR170 change to NC to change SC411 work mode to continue mode
P34 PR2 20K->15K for OVP point change

0905
P42 Add PJ2(Power SW jumper for TE request
P19 Cancel BIOS socket(U31) and add BIOS chip
P28 PCI8402 GRST# signal change to PCIRST# for can not program GUID issue
P36 Change 1.5V and 1.05V timing for power good glitch issue
P21,35 Add circuit to adjust PM_RSMRST# timing
P26 Change HW monitor power to 3VALW

0918
P35 PC176 change from 0.1u to 0.01u for Mode change to continue
Add PR175(NC_0ohm) and PC193(0.01u) for mode change
Change PC157 to 22nF and NC PC191 for better performance
P37 Add PC88,PC89 for better power performance
P38 Change PR88,PC192 position base on datasheet
Change PR116,PC114 for CPU load line SPEC
Change PL7,PL8 for height limit
P39 Change enable circuit or run power sequence
P40 Change for +12V power sequence
P36 Change PC60,PC61, add PC147 for ripple and cost down
Change PC58,PC59 for cost down
ALL input 1210 MLCC(PC5,149,150,151,163,164,46,51,49,50,55,68,69, 70,91,92,105,106,134,135,136) change to 1206 with 1210 pad

0919
P31 USB power switch changed for MOR request

0921
P42 Del CAP16 and Add C1520 for height limit

0925
P19,21,24 Add X-BUS function on JIG connector

0926
PCN1,CN32,CN29,CN24,CN25,CN13,CN28,CN31,CN22 Add test point
P25 Modified WLAN connector and terminator type for mechanical
P16 CN3 change D-SUB conn color for ME requirement
P32 CN25 change RJ45 conn color for ME requirement
P24 CN32 change to HM4202E-DW for ME requirement

0927
P27 CN24 change to SCN553S8GTNW01AG for ME requirement

0928
H2, H7, H13, H15, H20 change screw hole footprint for ME requirement

1002
P37 PC88 pin2 and PC89 pin2 change connection to GND_SC486 in order to improve 1.8V unstable for power requirement.
P38 Remove PR182,PR183,PR184,PR185 to release layout space.
P41 Change CLK_PCIE_MINI damping resistor from 33ohm to 22ohm for signal quality improvement.

1004
P17 Modify for sil1390 and sil1392 co-design.
P18 Add R2138,R2139,R2140,R2141 to connect I2C bus for FAE recommended.
P39 U33 change to Schmitt trigger part for MOR requirement.
P40 Remove PR179,PR180,add 12V_EN for power requirement.
P40 Del MAX8546_DC net and connect DC_OUT for PU10 VIN.

1005
P17 Modified Sil139X circuit
P21 Add D35 on PowerOK signal for ICH sequence timing

1009
P17 Modified Sil139X circuit
P34 Add PC196,197,198,199 for EMI
P38 Add PR182,PR183 PC194,PC195 for EMI

1010
P24 ODD CONN(CN7)change to FFC and pin swaped for ME
P30 Front IO board CONN(CN7)change type for ME request
C335,336,341,342 change to NC for MOR request

1011
P34 Change DC_IN test point size

1013
P16 CRT CONN(CN3) pin10 connect to GND according to SONY SPEC
P27 C412 change from 100p to 470p for MOR request
P30 R323 change to 100K for MOR request
P31 Remove USB power fuse for MOR request
P39 Add R2151 for PWR_OK sequence

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Title: History

Size	Document Number	Rev
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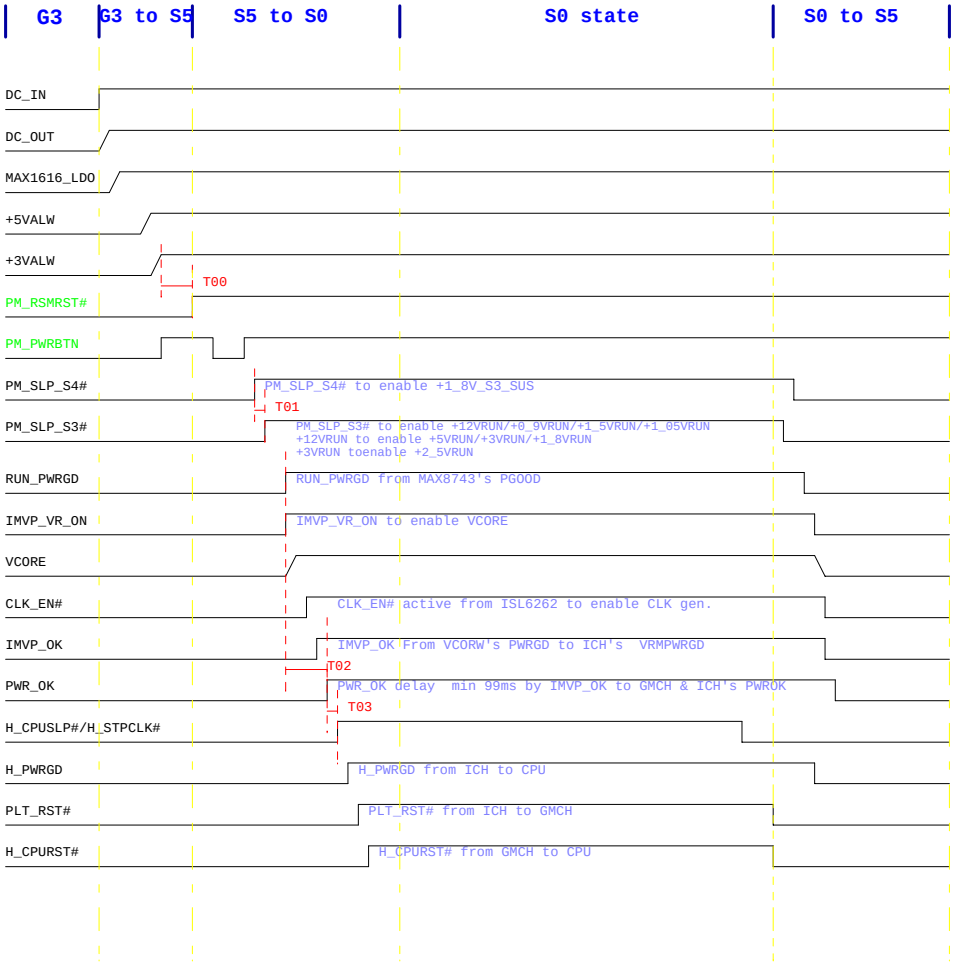
MS80 Power On Sequerce Timing

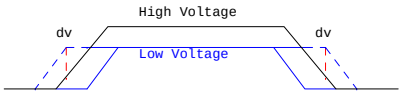
Version : 0.0
Modified date : 8/11/2006



T00 : (Min 10ms) ALW power supply to PM_RSMRST# at least 10ms (Please refer to ICH7 EDS of t204 timing)
T01 : (1 - 2 RTCCLK) PM_SLP4# to PM_SLP3# (Please refer to ICH7 EDS of t234 timing)
T02 : (Min 99ms) RUN_PWRGD to IMVP_OK (Please refer to ICH7 EDS of t214 timing)
T03 : (Max 50ns) PWR_OK active to H_CPUSLP# and H_STPCLK#

Remark: (Item1,2,3 add Diode; Item4,5,6 add dischage circuit; Item7 for implement TV)
SPEC please refer to Intel 16981 15.4 GMCH/ICH7M Platform Power -up Requirements)

1. V5REF(+5VRUN) -> +3VRUN, dt:0.7mV
2. V5REF_SUS(+5VALW) -> +3VALW, dt:0.7mV
3. +2.5VRUN -> GMCH_VCC(1.05V), dt:0.7mV
4. +1_5VRUN -> +GMCH(1.05V), dt:0.7mV
5. +3.3VRUN -> +2_5VRUN, dt:0.3mV
6. +3.3VRUN -> +5VRUN (VccLAN), dt:0.3mV
7. +3_3VRUN -> +1_5VRUN(TV), dt:0.7mV



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Title: Power Sequence

Size: C | Document Number: MS80-1-04 | Rev: 0.1

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