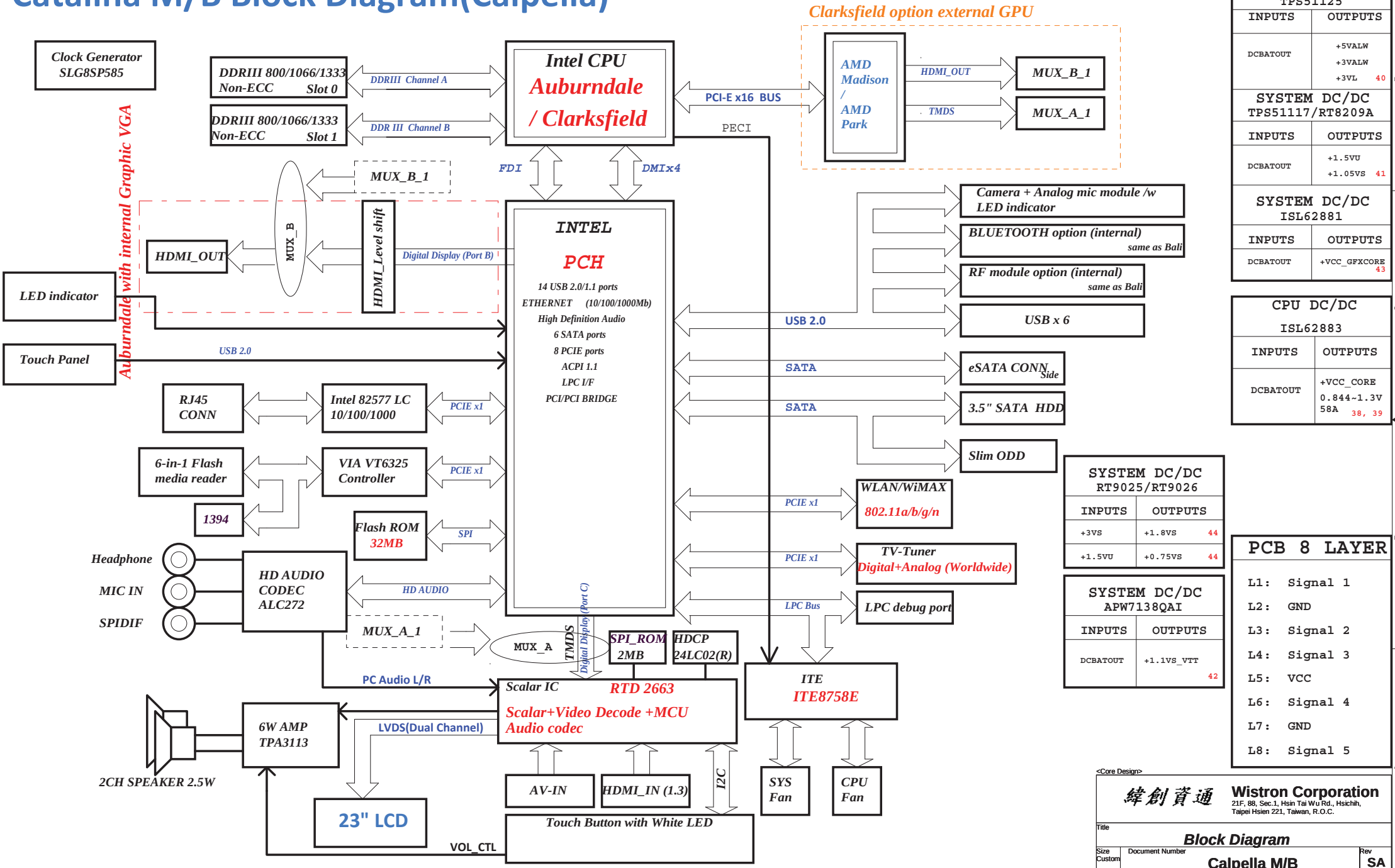
Catalina M/B Block Diagram(Calpella)



SYSTEM DC/DC TPS51125	
INPUTS	OUTPUTS
DCBATOUT	+5VALW +3VALW +3VL 40

SYSTEM DC/DC TPS51117/RT8209A	
INPUTS	OUTPUTS
DCBATOUT	+1.5VU +1.05VS 41

SYSTEM DC/DC ISL62881	
INPUTS	OUTPUTS
DCBATOUT	+VCC_GFXCORE 43

CPU DC/DC ISL62883	
INPUTS	OUTPUTS
DCBATOUT	+VCC_CORE 0.844~1.3V 58A 38, 39

SYSTEM DC/DC RT9025/RT9026	
INPUTS	OUTPUTS
+3VS	+1.8VS 44
+1.5VU	+0.75VS 44

SYSTEM DC/DC APW7138QAI	
INPUTS	OUTPUTS
DCBATOUT	+1.1VS_VTT 42

PCB 8 LAYER	
L1:	Signal 1
L2:	GND
L3:	Signal 2
L4:	Signal 3
L5:	VCC
L6:	Signal 4
L7:	GND
L8:	Signal 5

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Block Diagram

Size: Custom | Document Number: Calpella M/B | Rev: SA

Date: Tuesday, April 06, 2010 | Sheet 1 of 59

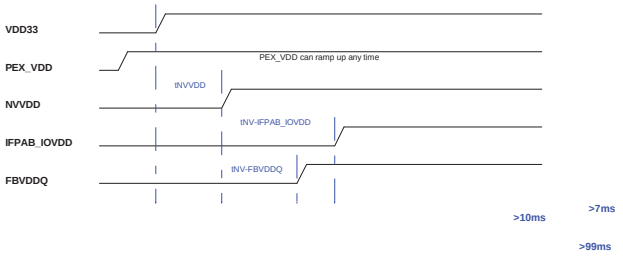
Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	**PCI-Express Configuration Select**	**1:** Single PCI-Express Graphics **0:** Bifurcation enabled	1
CFG[7]	**Reserved - Temporarily used for early Clarksfield samples.**	**Clarksfield (only for early samples pre-ES1)** - Connect to GND with 3.01K Ohm/5% resistor **Note:** Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

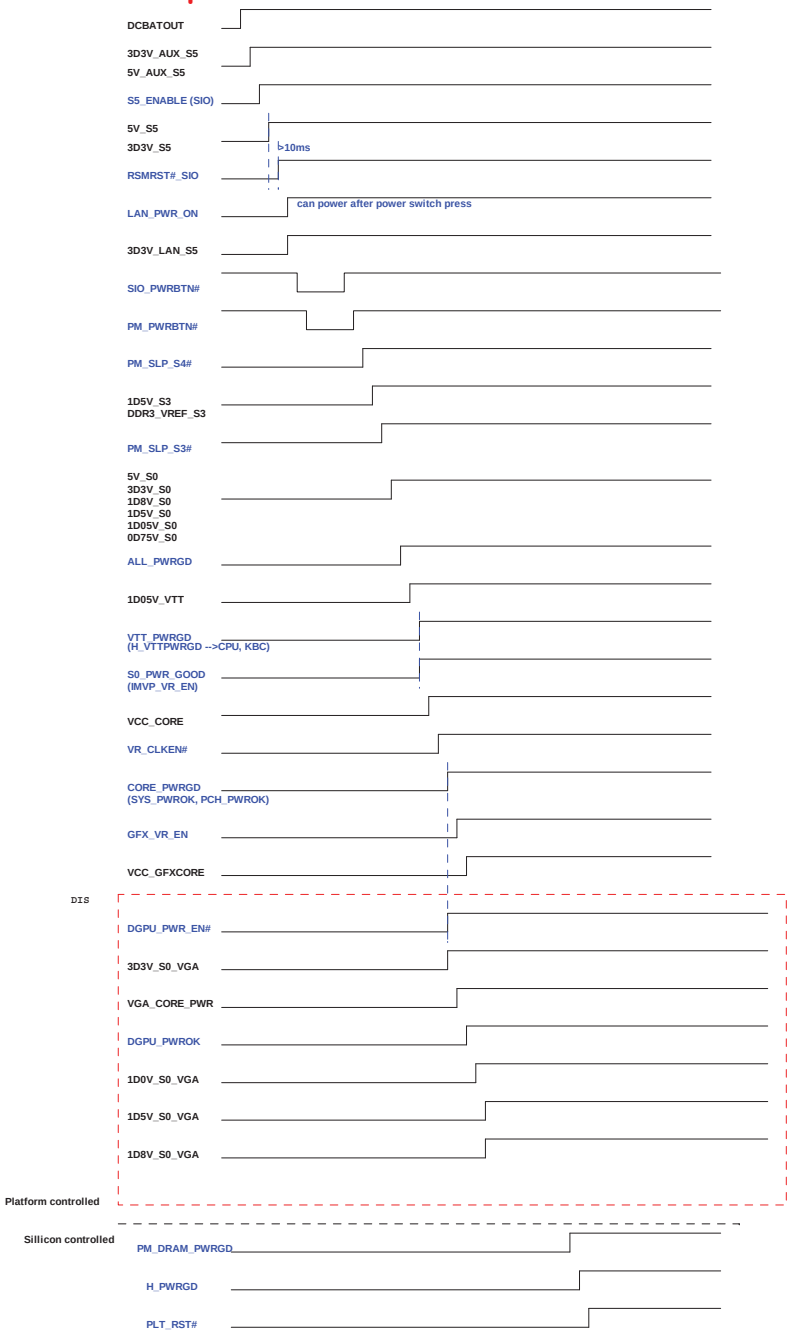
PCH Strapping

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled**
GNT0#, GNT1#	**Default (SPI):** Left both GNT0# and GNT1# floating. No pull up required. **Boot from PCI:** Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	**Default - Internal pull-up.** **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	**Default:** Do not pull low. **Disable ME in Manufacturing Mode:** Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	**Enable iTPM:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor **Disable iTPM:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Danbury:** Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	**Low (0):** Flash Descriptor Security will be overridden. **High (1) :** Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

N11M-GE Power Sequence



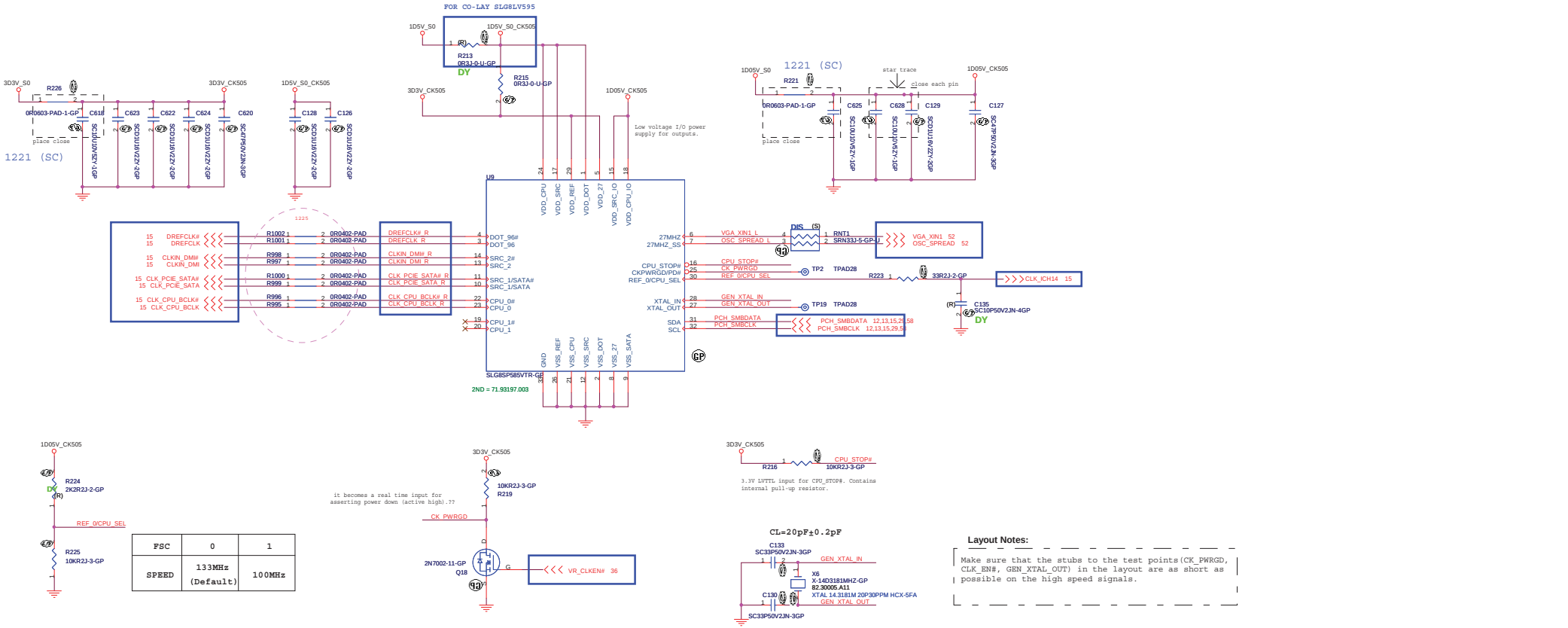
Power Sequence



<Variant Name>

Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title	<Title>	
Size A2	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, April 06, 2010	Sheet 2 of 59	



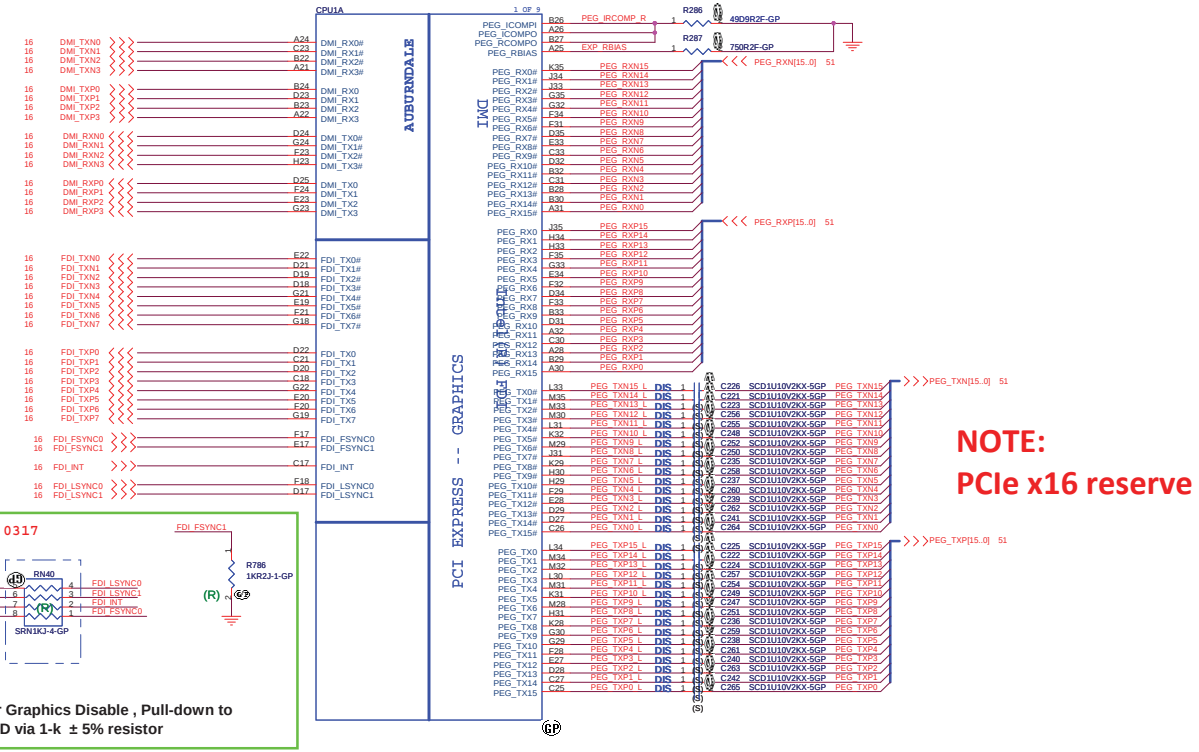
FSC	0	1
SPEED	133MHz (Default)	100MHz

Layout Notes:

Make sure that the stubs to the test points (CK_PWRGD, CLK_EN#, GEN_XTAL_OUT) in the layout are as short as possible on the high speed signals.

<variant_name>

緯創資通	Wistron Corporation 21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih, Taipei Hsien 221, Taiwan, R.O.C	
Title: Ali Mountain		
Size: A2	Document Number: CK505_SLG8SP585	Rev: <RevCode>
Date: Tuesday, April 06, 2010	Sheet 3 of 59	



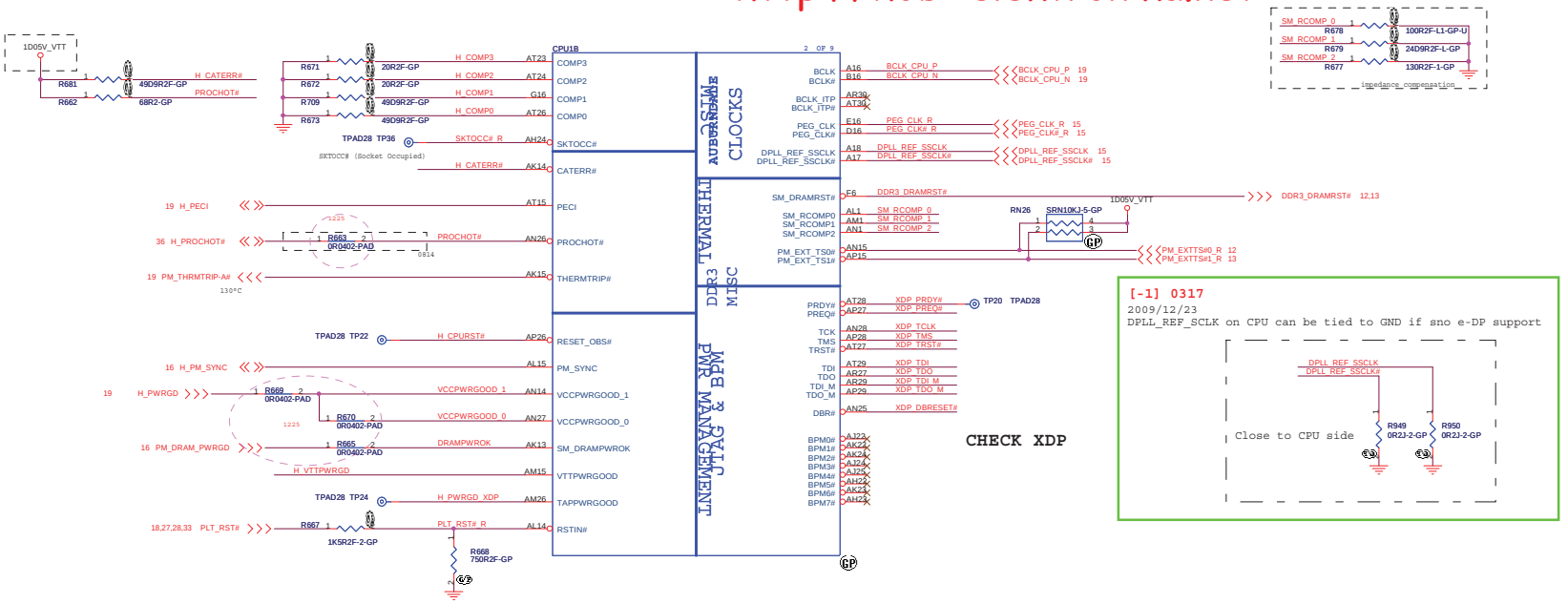
NOTE:
PCIe x16 reserve

62.10040.611
2nd = 62.10055.321

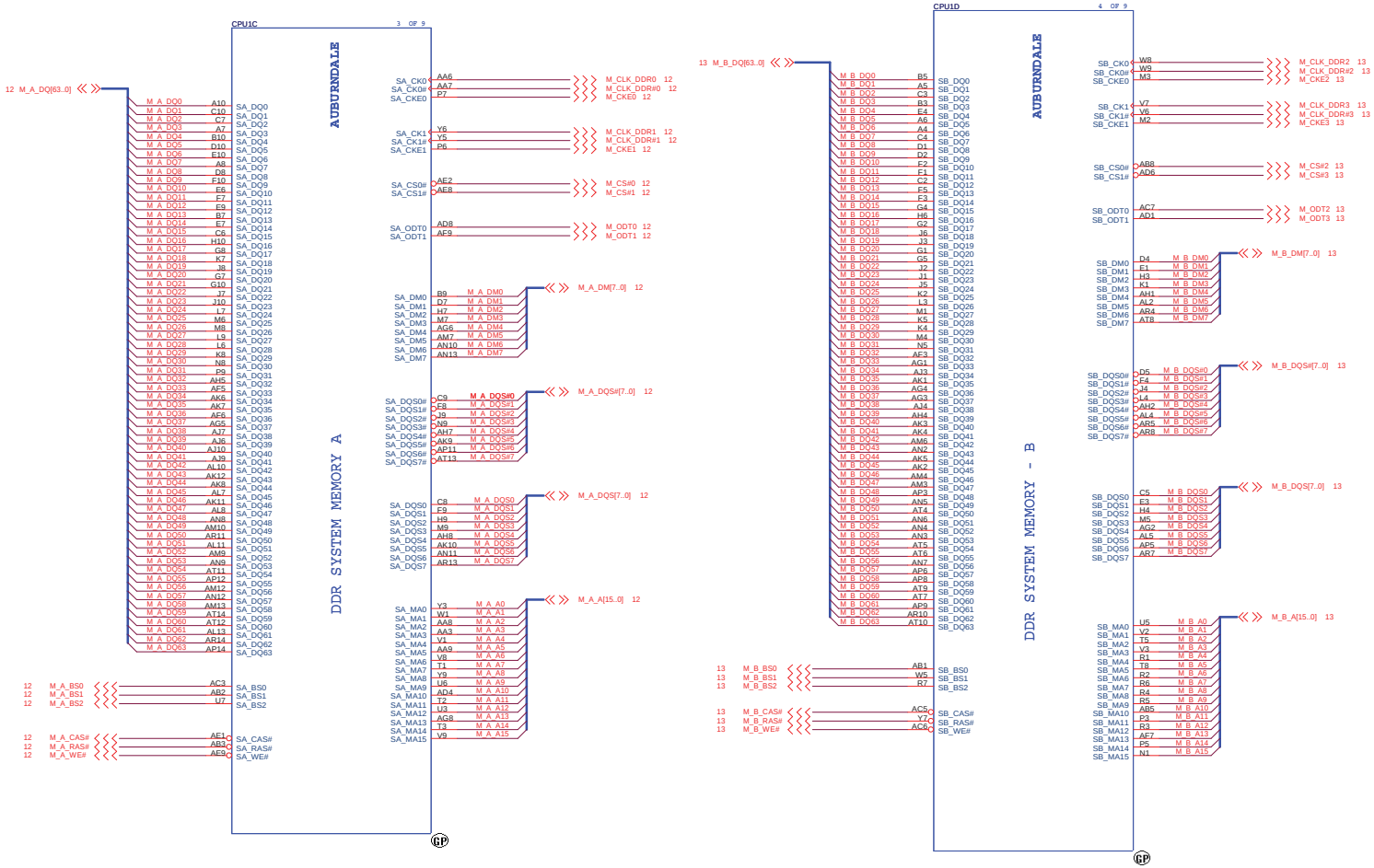
<Variant Name>

Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title		
<Title>		
Size: A2	Document Number: <Doc>	Rev: <RevCode>
Date: Tuesday, April 06, 2010	Sheet 4 of 59	



http://hobi-elektronika.net/



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(3/7)

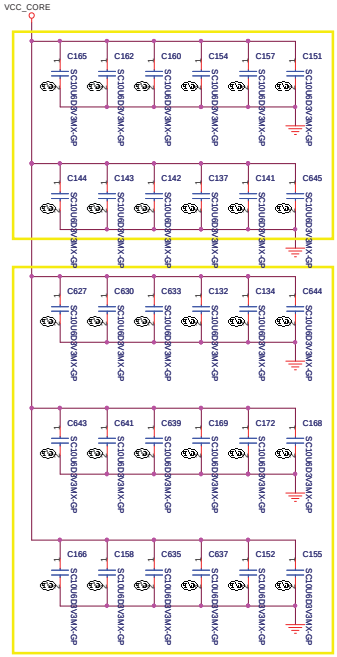
Size: A2 | Document Number: Catalina | Rev: SA

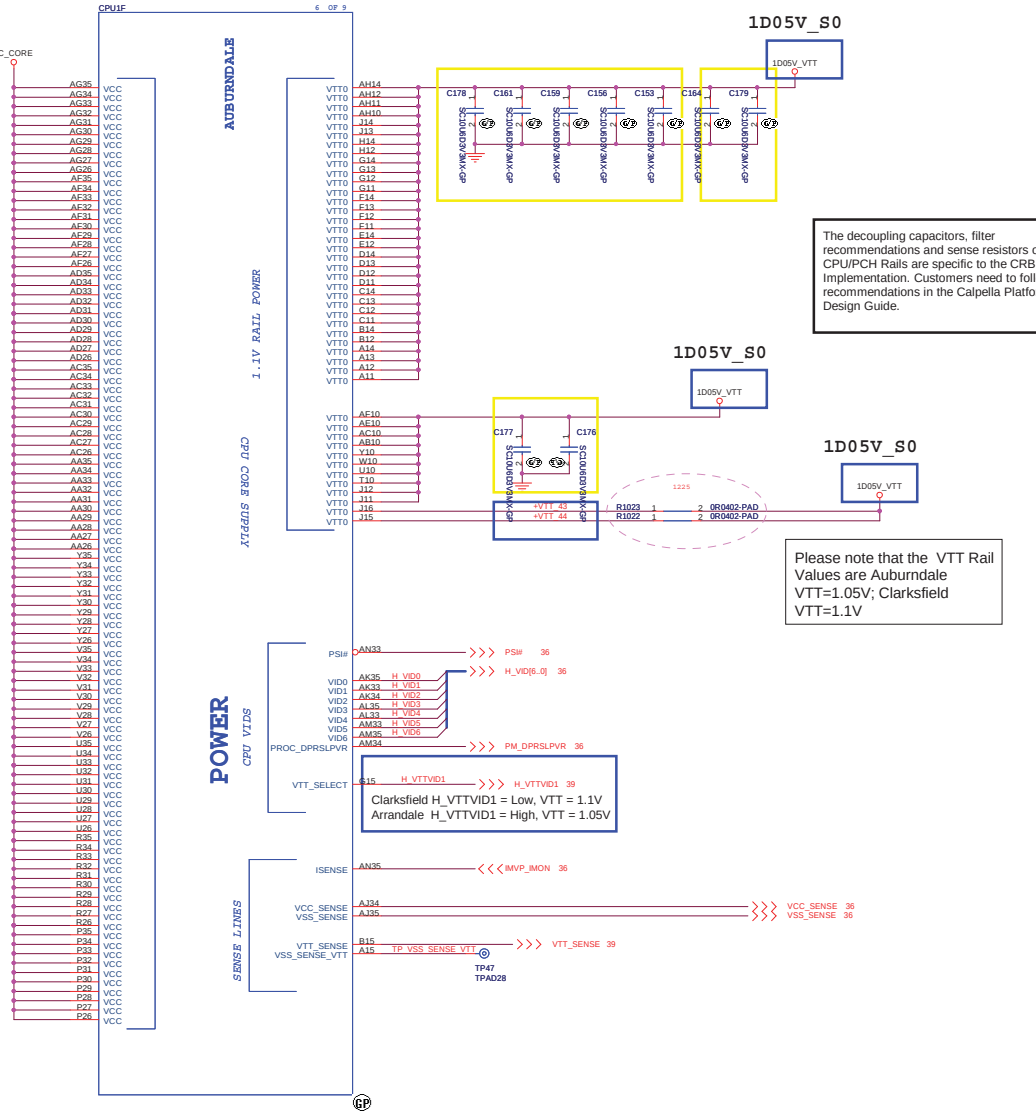
Date: Tuesday, April 06, 2010 | Sheet 6 of 59

30pcs : 10uF 6.3V X5R

PROCESSOR CORE POWER

48A -->Arrandale





The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

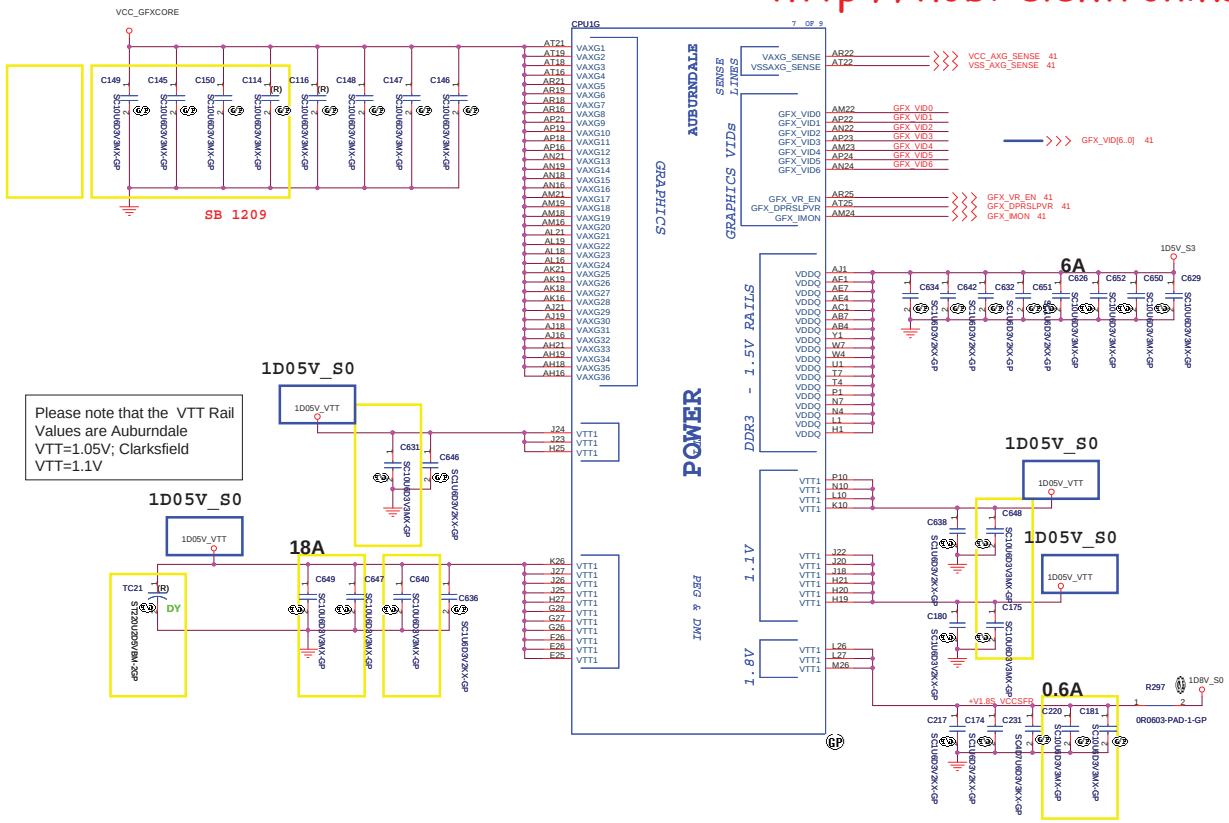
Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V

Clarksfield H_VTTVID1 = Low, VTT = 1.1V
Arrandale H_VTTVID1 = High, VTT = 1.05V

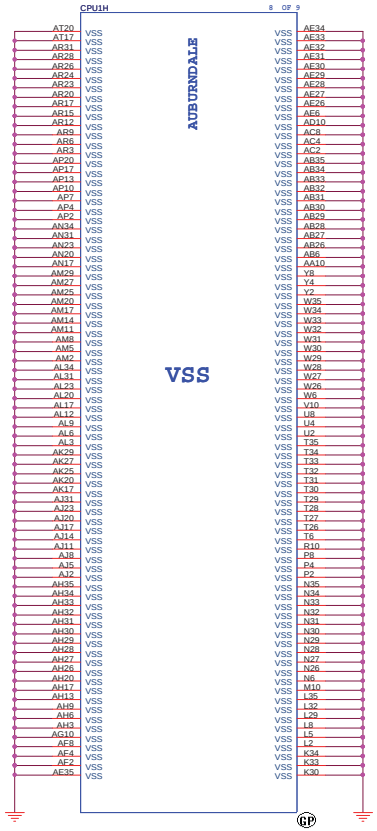
<Variant Name>

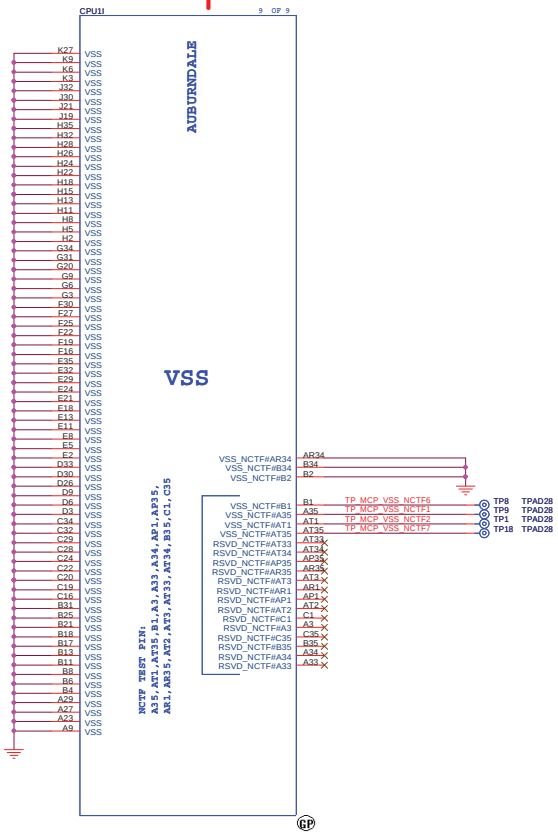
緯創資通 Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title <Title>
Size A2 | Document Number <Doc> | Rev <RevCode>
Date: Tuesday, April 06, 2010 | Sheet 7 of 59



<Variant Name>
緯創資通 Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih, Taipei Hsien 221, Taiwan, R.O.C
Title <Title>
Size A2 | Document Number <Doc> | Rev <RevCode>
Date: Tuesday, April 06, 2010 | Sheet 8 of 59





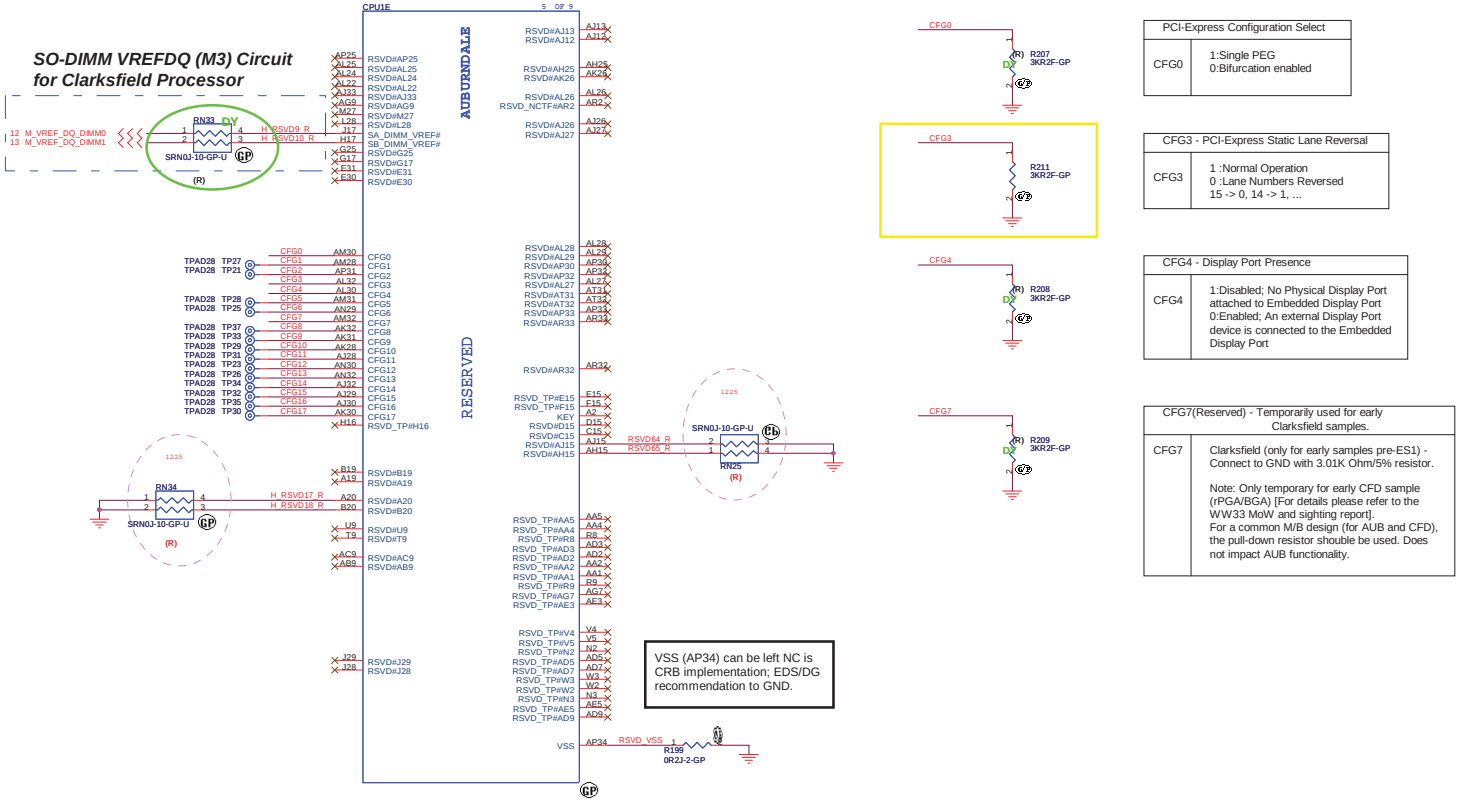
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(6/7)

Size: A2 | Document Number: Catalina | Rev: SA

Date: Tuesday, April 06, 2010 | Sheet 9 of 59



PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor shoulde be used. Does not impact AUB functionality.

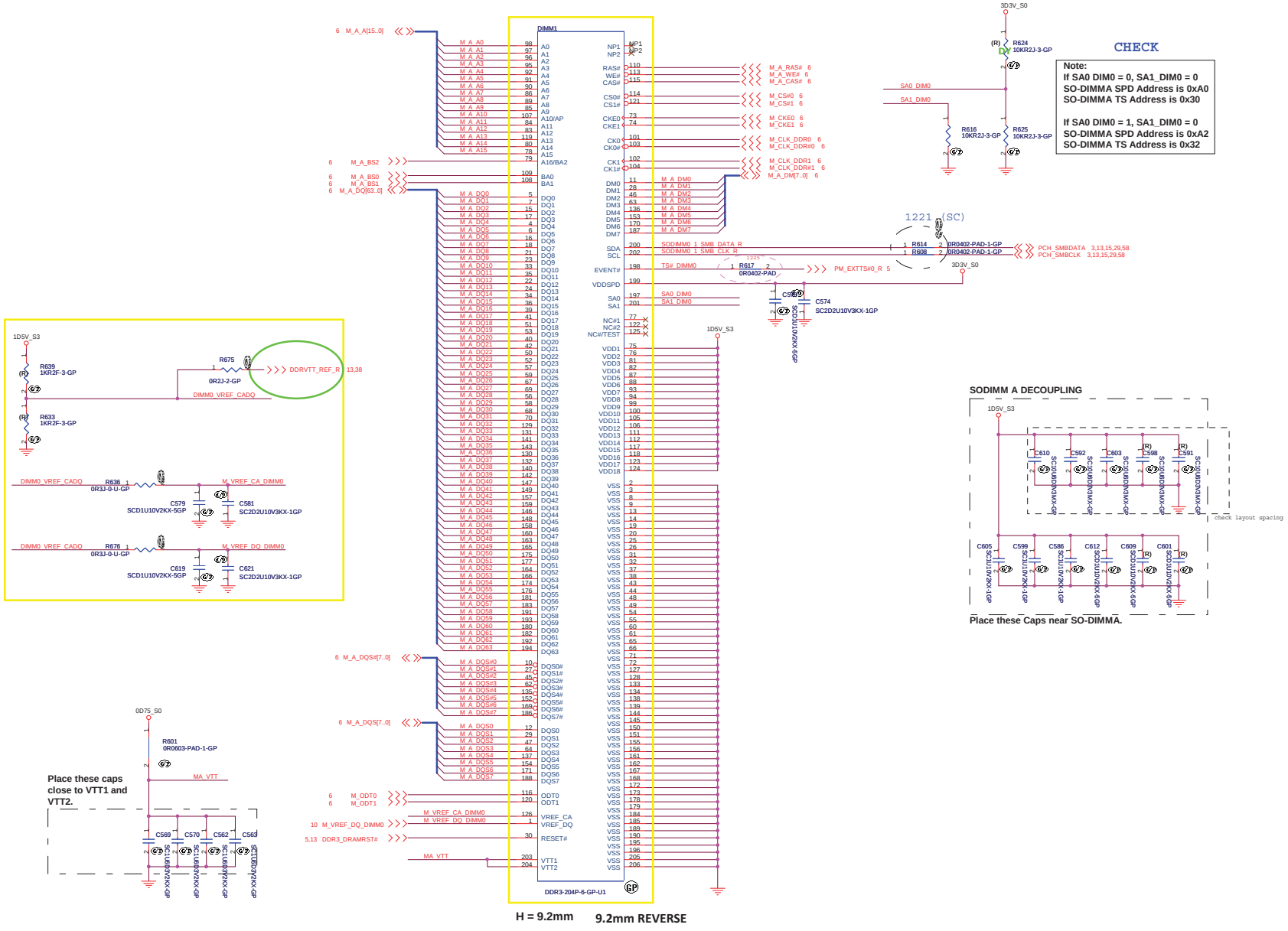
<core_design><Core Design></core_design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(7/7)

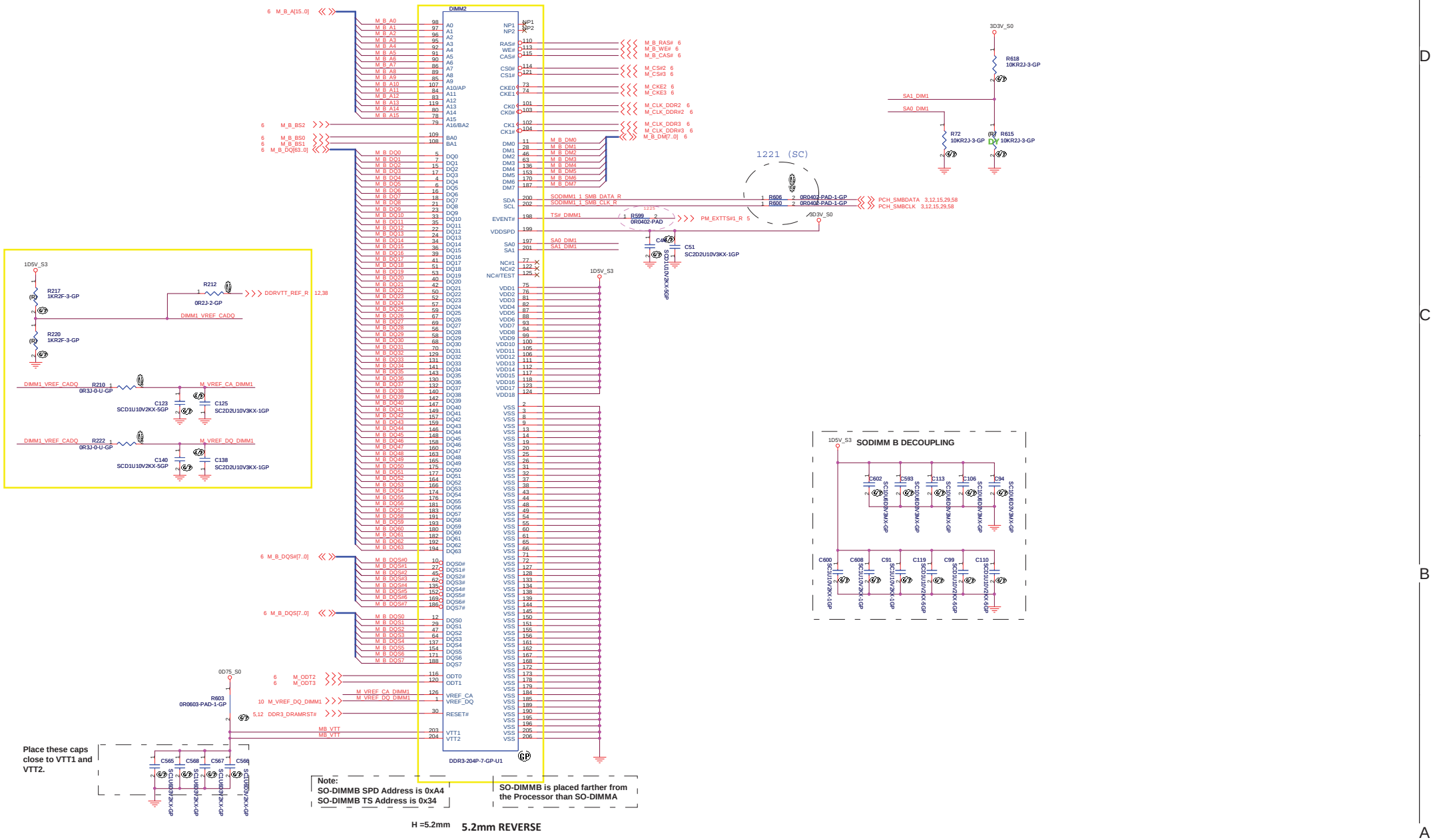
Size: A2 | Document Number: Catalina | Rev: SA

Date: Tuesday, April 06, 2010 | Sheet 10 of 59



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	DIMM1
Size	A2
Document Number	Catalina
Rev	SA
Date	Tuesday, April 06, 2010
Sheet	12 of 59

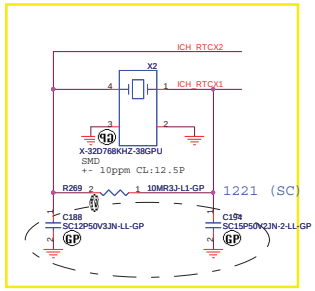


<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

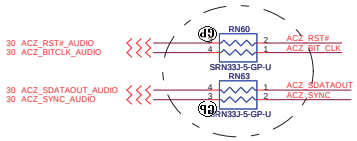
Title: DIMM2

Size	Document Number	Rev
A2	Catalina	SA

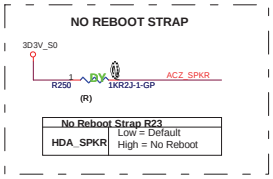
Date: Tuesday, April 06, 2010 Sheet 13 of 59

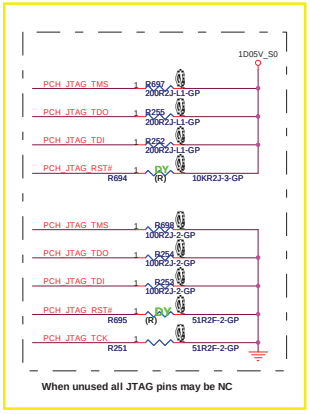


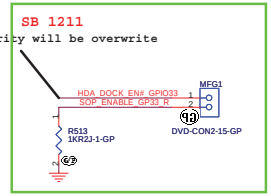
0127 (1A)

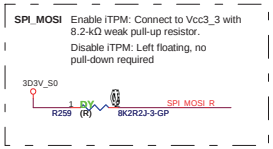


If Sample low ,the flash descriptor security will be overwrite



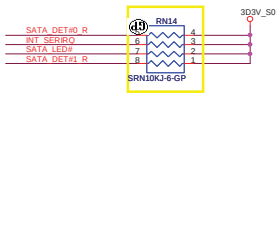






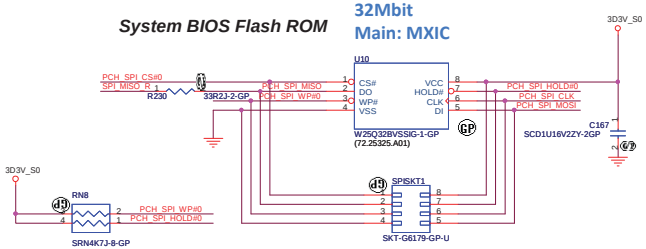
0126 (1A)

integrated VccSus1_05,VccSus1_5,VccCL1_5	
INTVRMEN	High=Enable Low=Disable
integrated VccLan1_05VccCL1_05	
LAN100_SLP	High=Enable Low=Disable



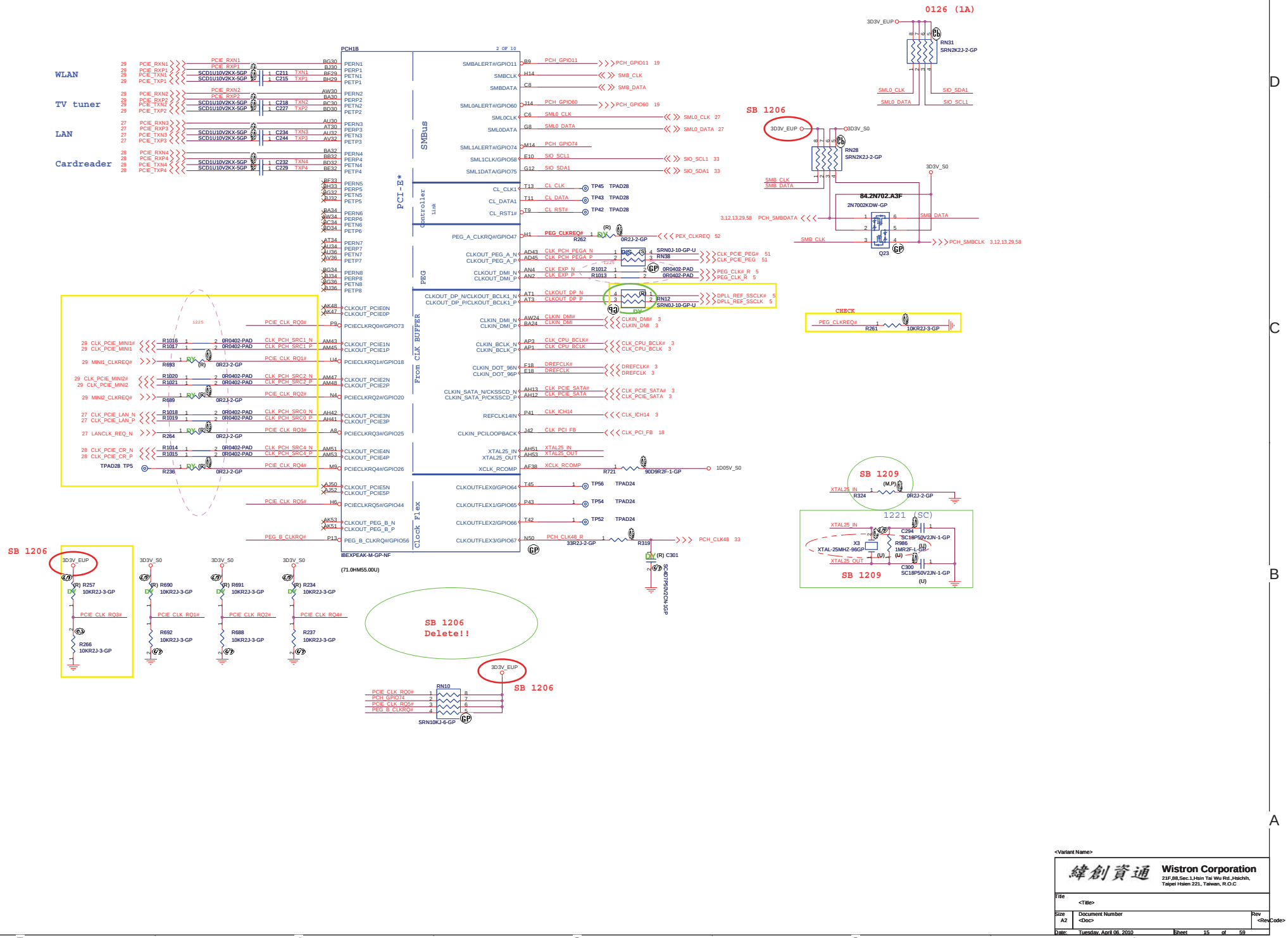
CHECK PIN Define

System BIOS Flash ROM 32Mbit Main: MXIC



<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

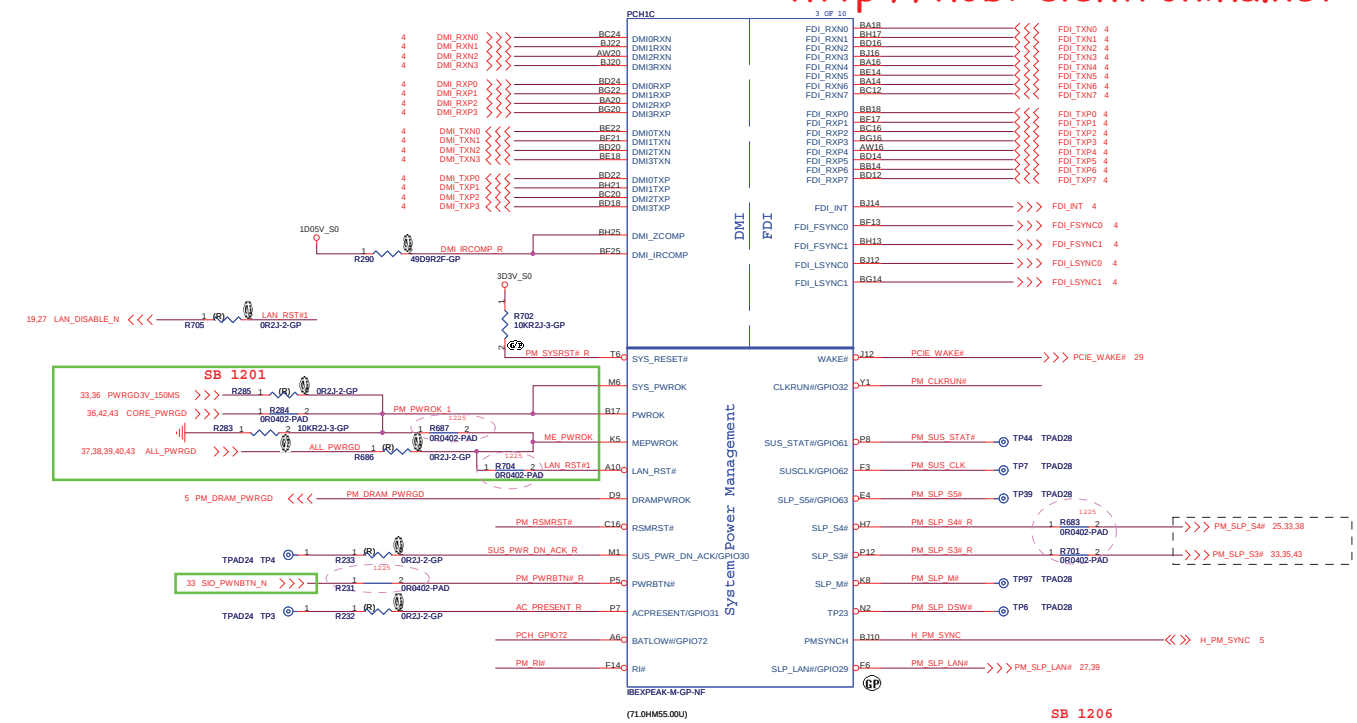
Title: PCH(1/9)
Size: A2 | Document Number: Catalina | Rev: SA
Date: Tuesday, April 06, 2010 | Sheet 14 of 59

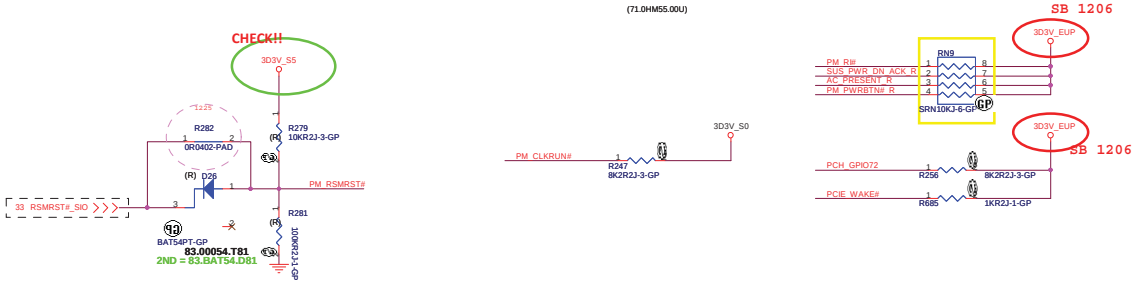


<Variant Name>

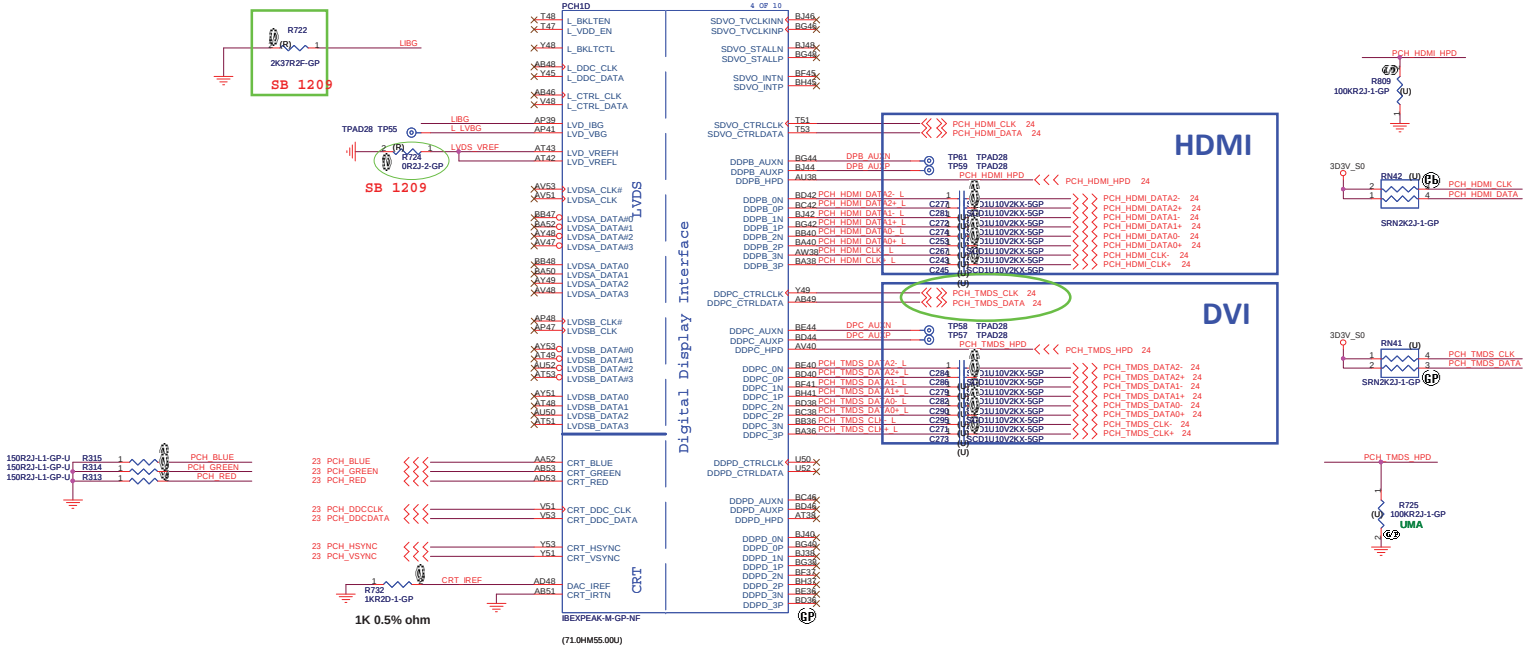
緯創資通 Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title: <Title>
Size: A2 | Document Number: <Doc> | Rev: <RevCode>
Date: Tuesday, April 06, 2010 | Sheet 15 of 59





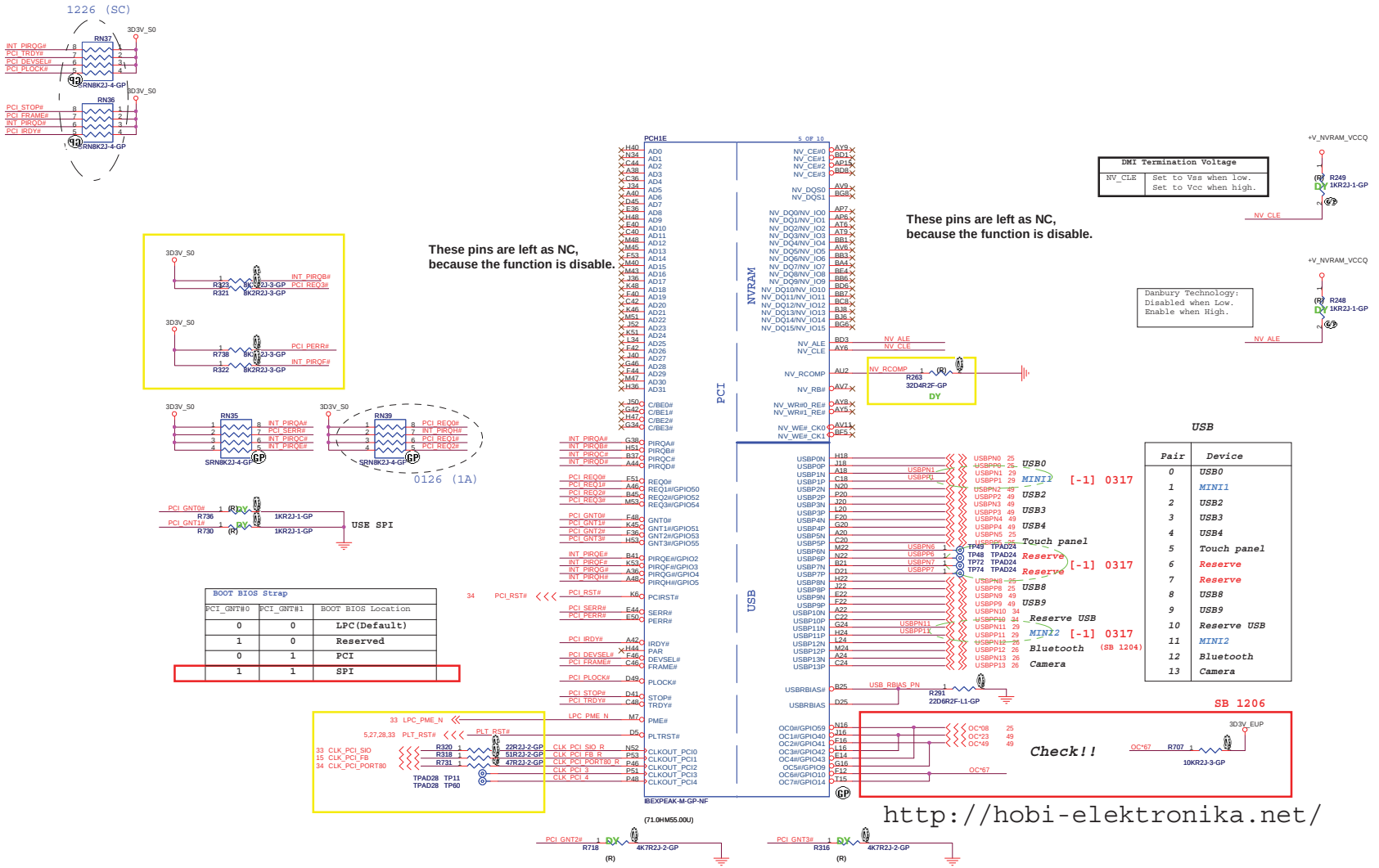
<Variant Name>
Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C
Title <Title>
Size A2 | Document Number <Doc> | Rev <RevCode>
Date: Tuesday, April 06, 2010 | Sheet 16 of 59



<Variant Name>

緯創資通 Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title	<Title>	
Size A2	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, April 06, 2010	Sheet 17 of 59	



<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH(5/9)
Size: A2 | Document Number: Catalina | Rev: SA
Date: Tuesday, April 06, 2010 | Sheet 18 of 59

GPIO8 has a weak[20K] internal pull up.
No need to have external pull down/up.
GPIO8 pin set to high at reset.

GPIO15 has a weak[20K] internal pull down.
No need to have external pull up/down.
GPIO 15 pin is set to low at reset.
Low : ME Crypto TLS with no confidentiality
High : ME Crypto TLS with confidentiality

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator,
should not place external pull down.

SB 1206

0126 (1A)

[-1] 0401

PCH1F

IBEXPEAK-M-GP-NF

(71.0HM55.00U)

Placed Within 2" from PCH

MB_ID1	MB_ID0	
0	0	UMA
0	1	MADISON
1	0	PARK

Header color: RED

Clear CMOS by GPIO

1-2	NORMAL(DEFAULT)
2-3	CLR CMOS

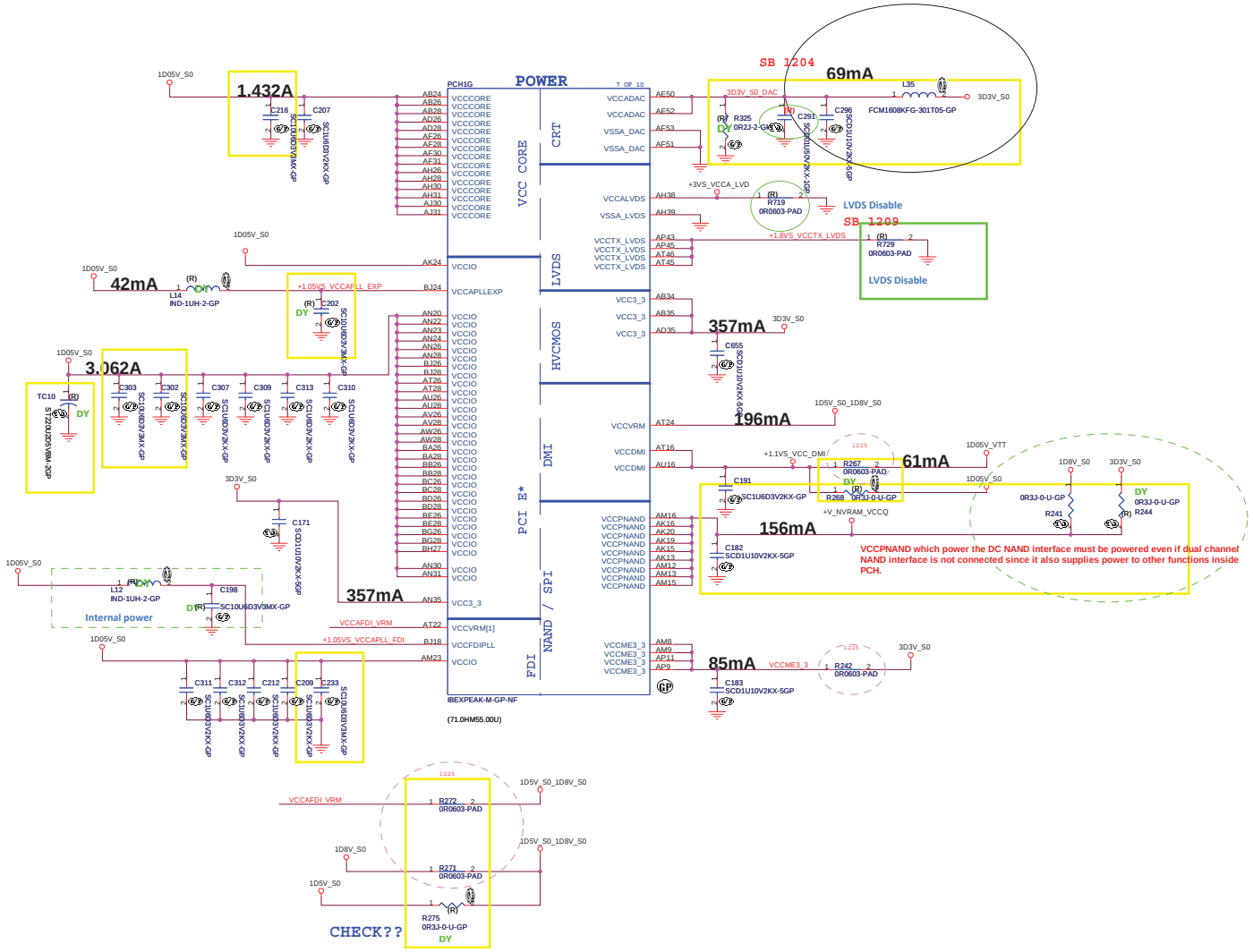
<Variant Name>

Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title: <Title>

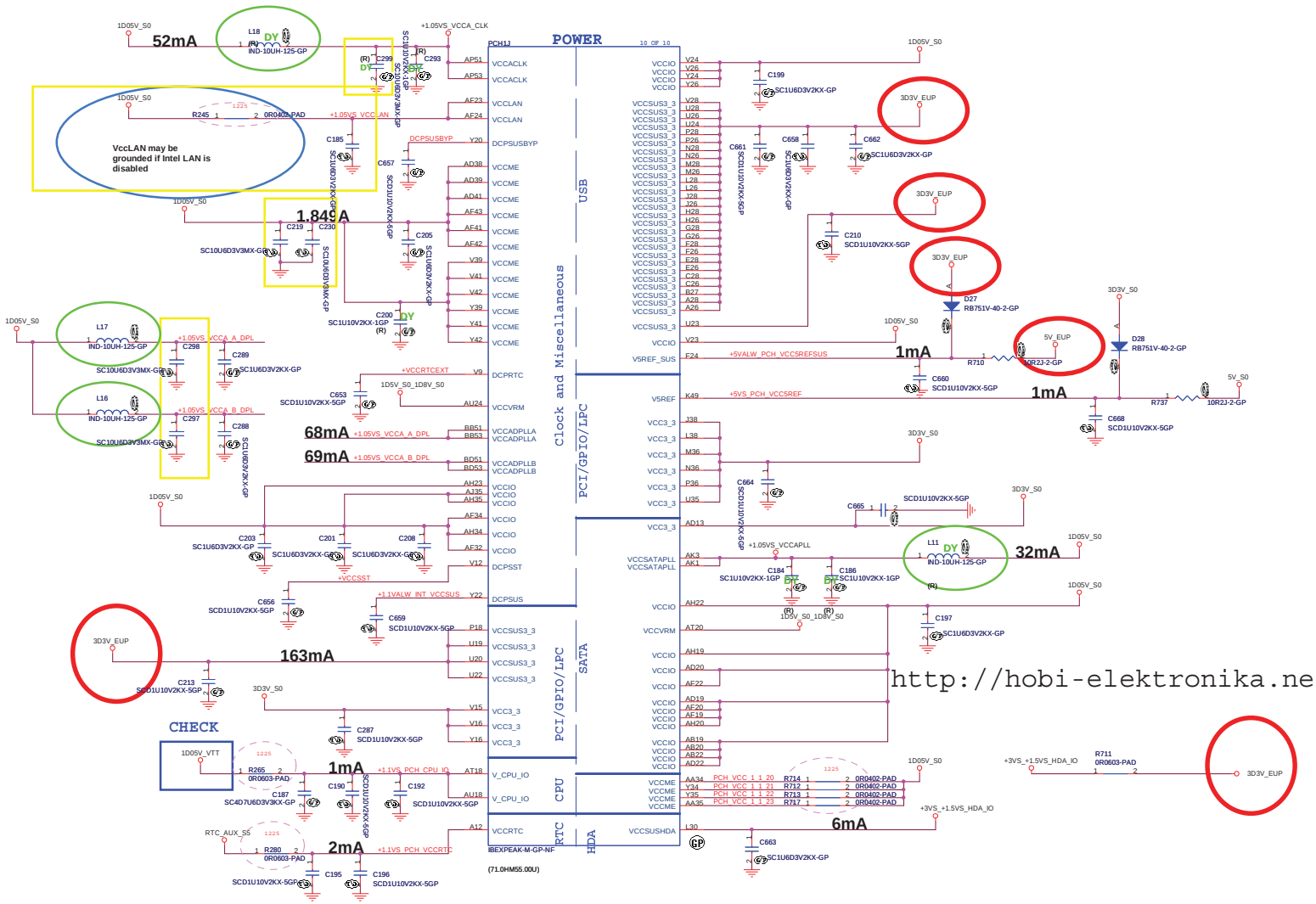
Size: A2 | Document Number: <Doc> | Rev: <RevCode>

Date: Tuesday, April 06, 2010 | Sheet 19 of 59



<variant_name>

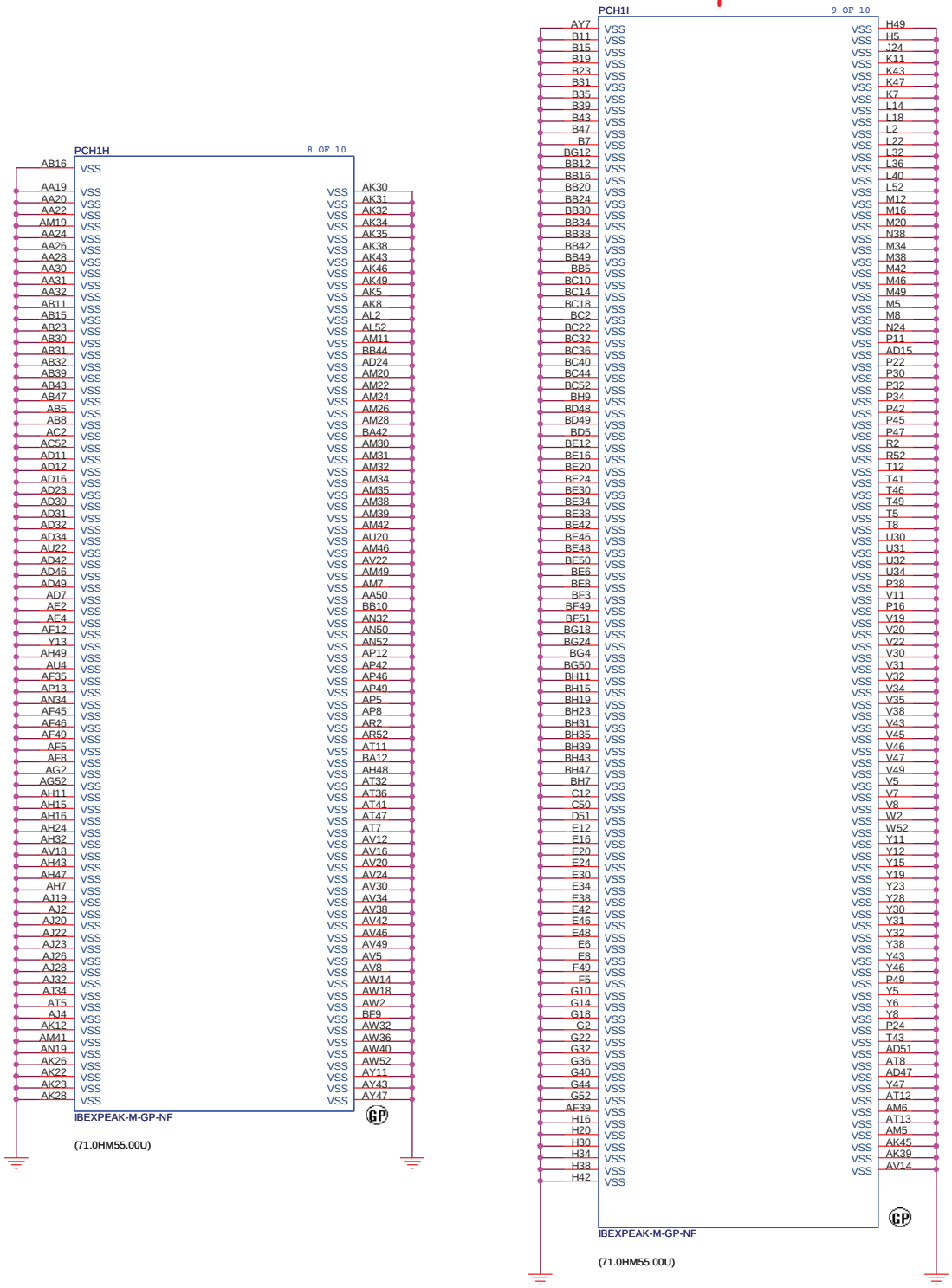
緯創資通 Wistron Corporation 21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih, Taipei Hsien 221, Taiwan, R.O.C		
Title: <Title>		
Size: A2	Document Number: <Doc>	Rev: <RevCode>
Date: Tuesday, April 06, 2010	Sheet 20 of 59	



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	PCH(8/9)	
Size A2	Document Number Catalina	Rev SA
Date: Tuesday, April 06, 2010	Sheet 21 of 59	



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PCH(9/9)***

Size	Document Number	Rev
A3	**Catalina**	**SA**

Date: Tuesday, April 06, 2010 Sheet 22 of 59

CRT header for debug

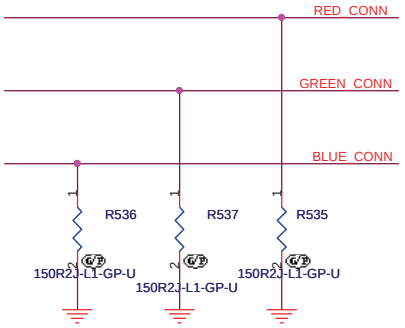
http://hobi-elektronika.net

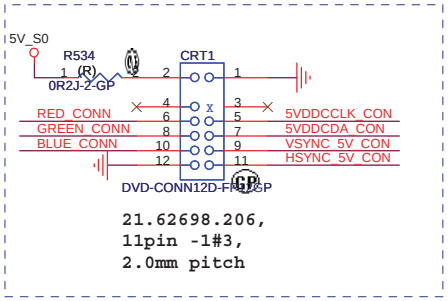
From PCH

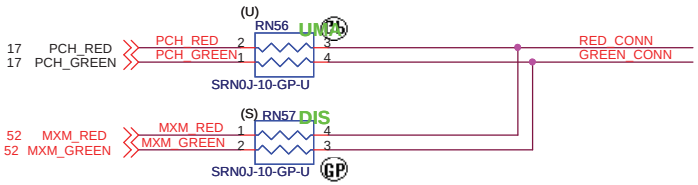
17 PCH_HSYNC
17 PCH_VSYNC
17 PCH_DDCCLK
17 PCH_DDCDATA
17 PCH_RED
17 PCH_GREEN
17 PCH_BLUE

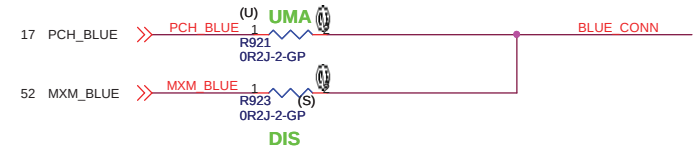
From MXM

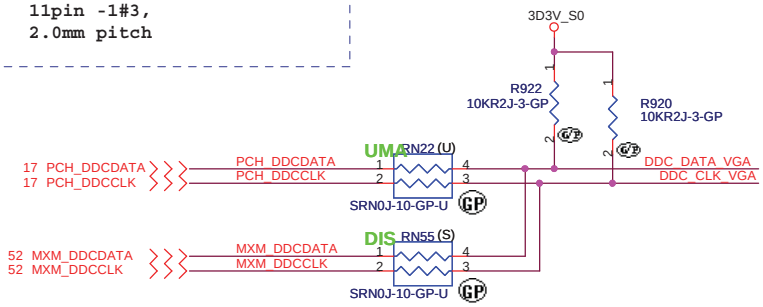
52,58 MXM_HSYNC
52,58 MXM_VSYNC
52 MXM_DDCDATA
52 MXM_DDCCLK
52 MXM_RED
52 MXM_GREEN
52 MXM_BLUE

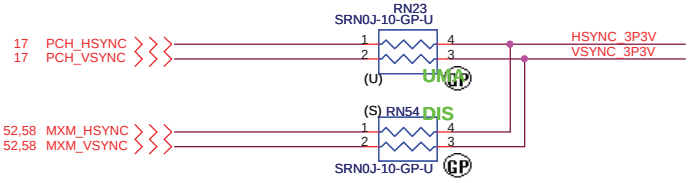


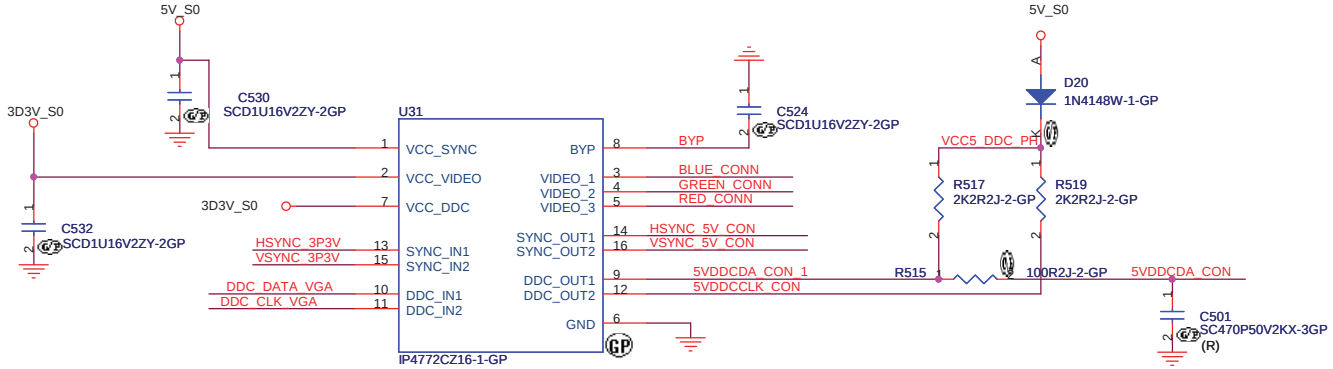












<Core Design>

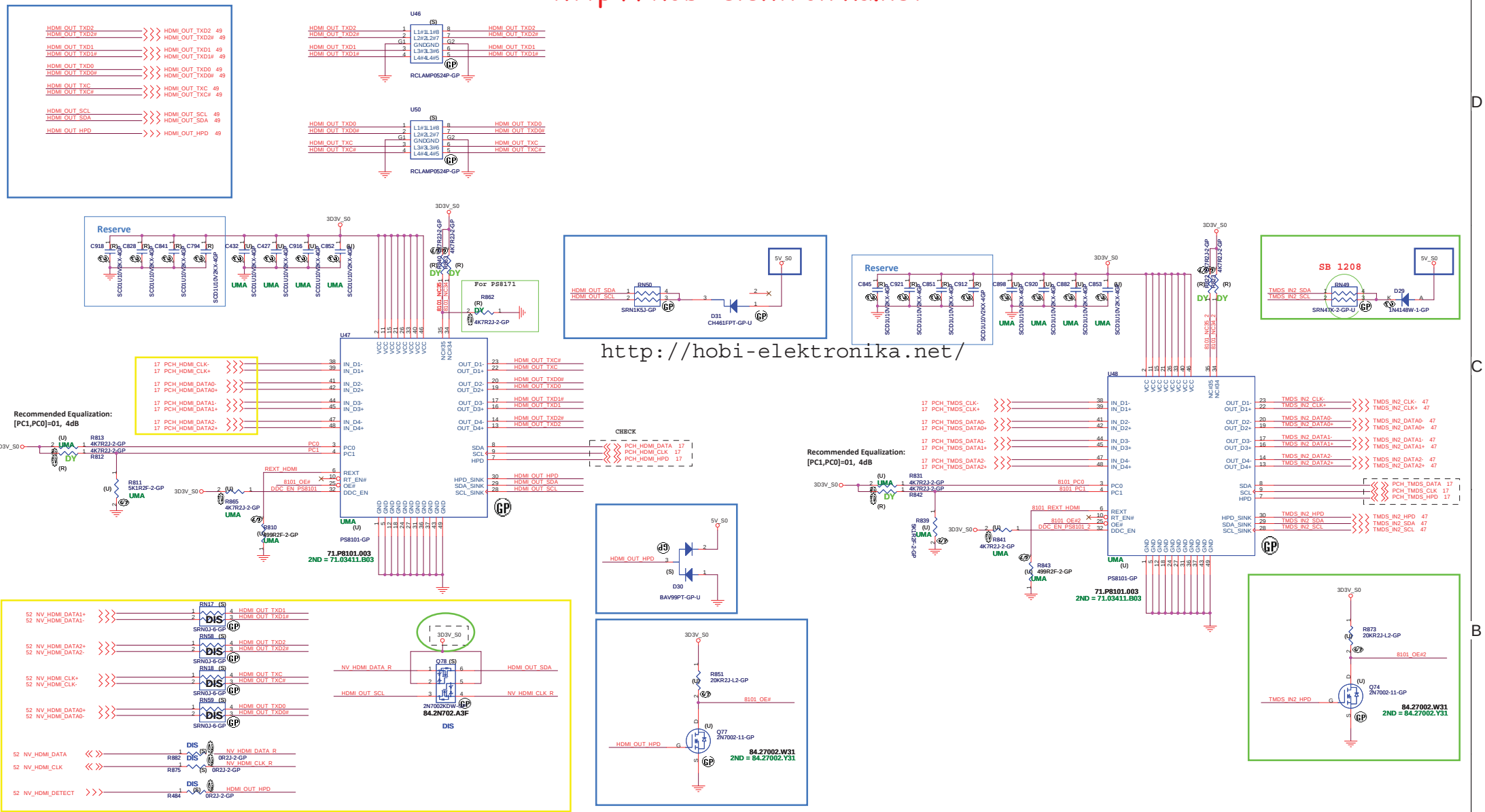
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **VGA header**

Size	Document Number	Rev
B	Catalina	SA

Date: Tuesday, April 06, 2010 Sheet 23 of 59

CHECK UMA AND DIS !!



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI OUT

Size: A2 | Document Number: Catalina | Rev: SA

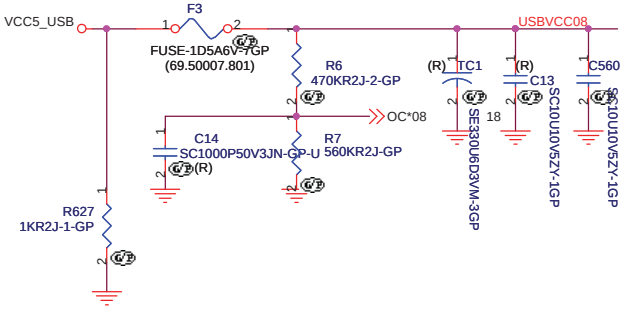
Date: Tuesday, April 06, 2010 | Sheet 24 of 59

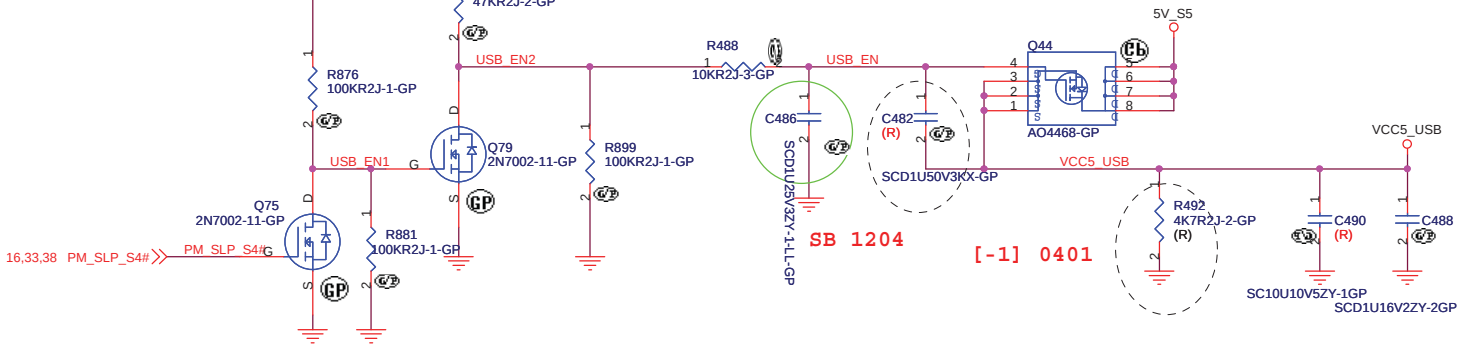
USB PORT Side 2 USB PORT (0/1)

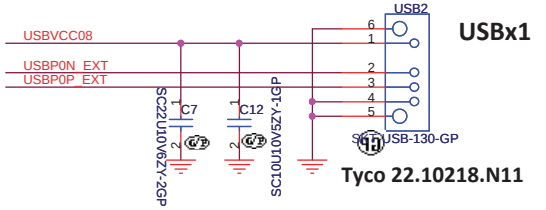
5V_S5 --> VCC5_USB

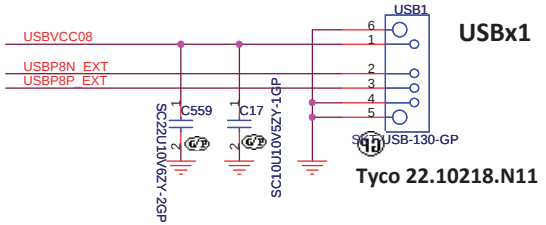
USB Power

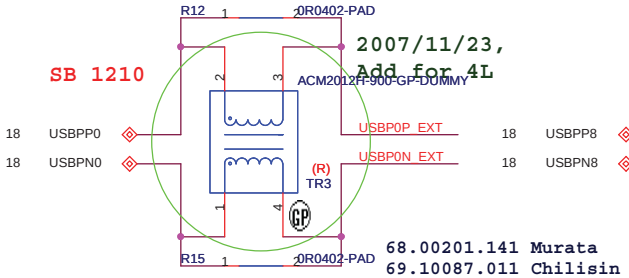
Use 69.50007.801 (Littelfuse)

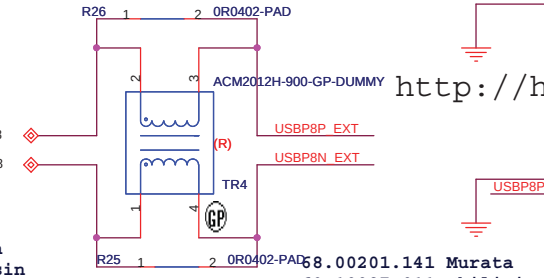


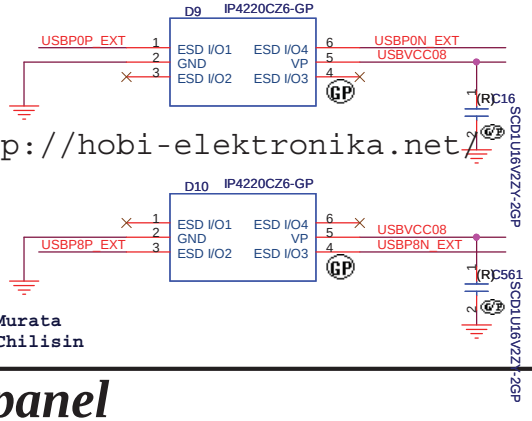




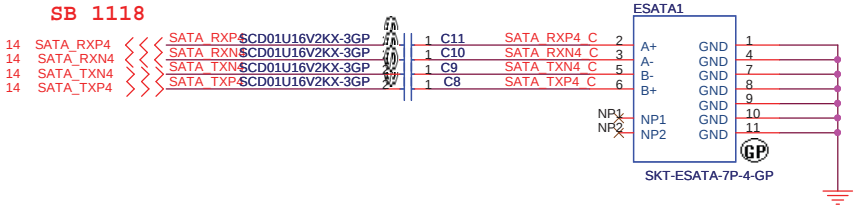




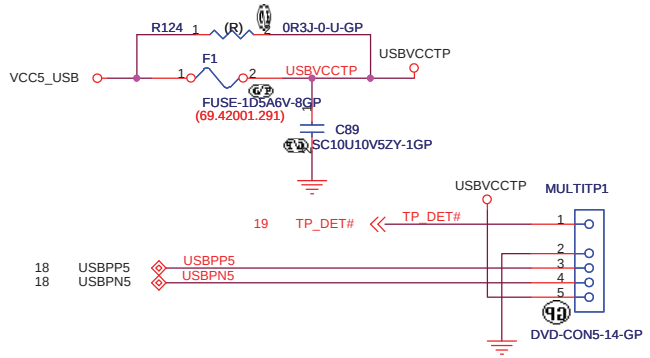




eSATA PORT



Touch panel



<Core Design>

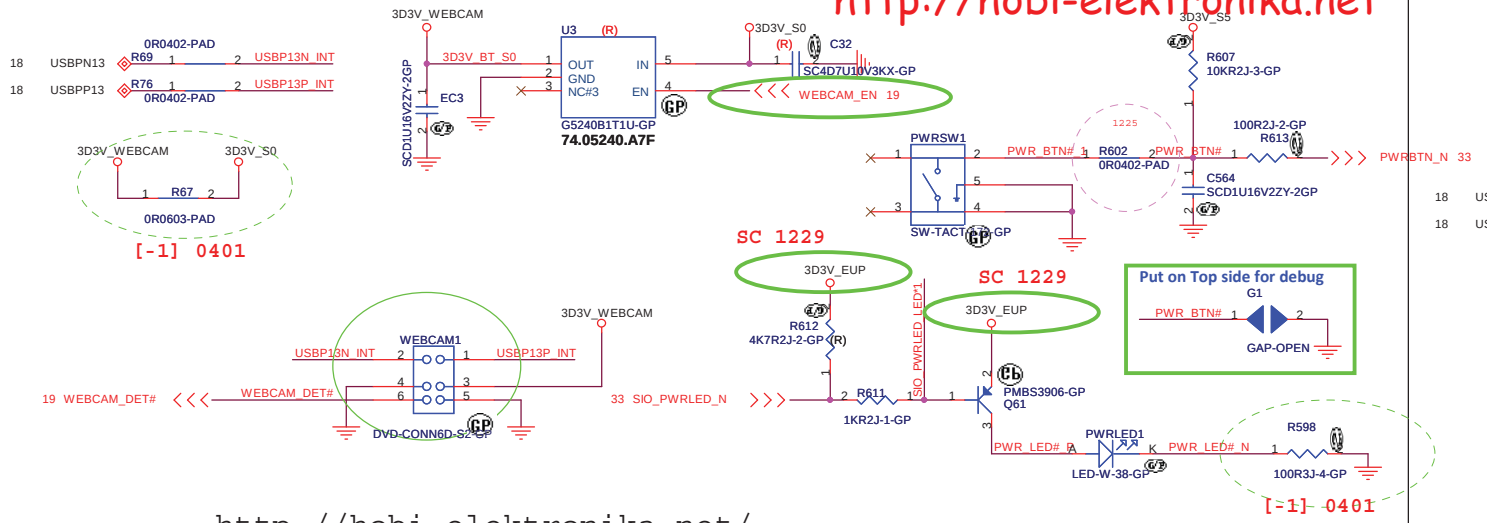
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB IO/eSATA/TP

Size	Document Number	Rev
B	Catalina	SA

Date: Tuesday, April 06, 2010 Sheet 25 of 59

CAMERA

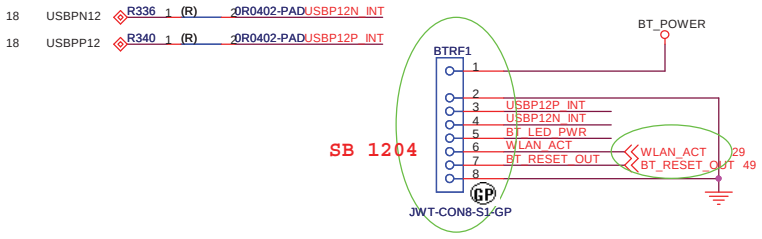


RF->Wireless KB/MS

REMOVE!!

SB 1204

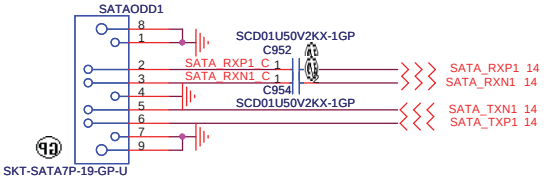
Blue tooth



CD-ROM CONNECTOR

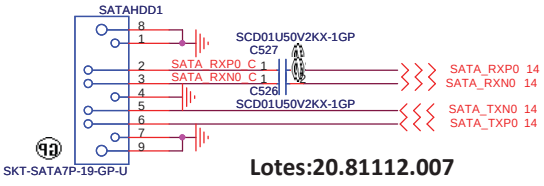
Check HD power(+12V) and connector type

Check connection!!



MAIN HDD Connector

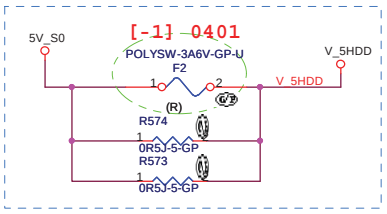
Check connection!!

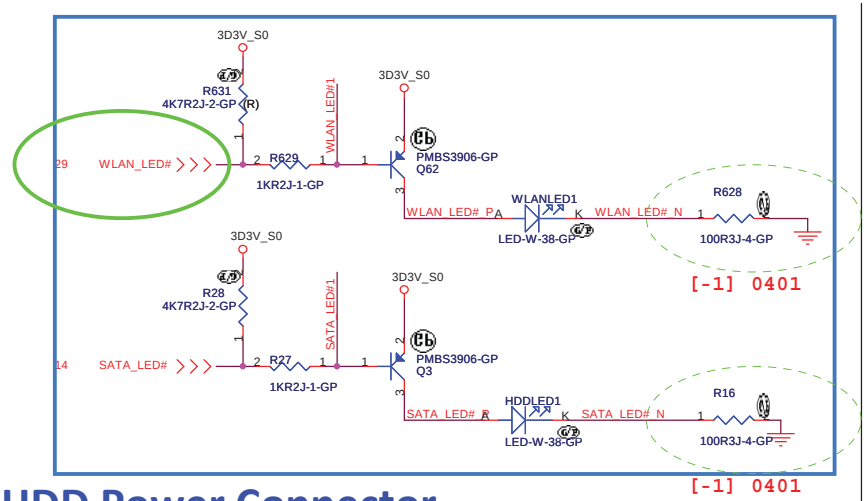


Black

Lotes:20.81112.007

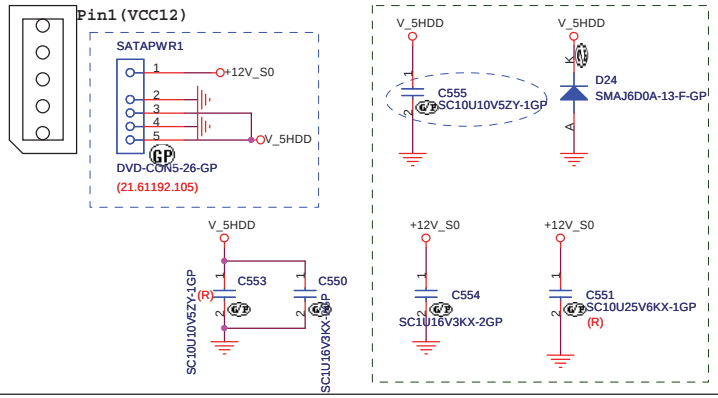
Molex: 20.80618.007



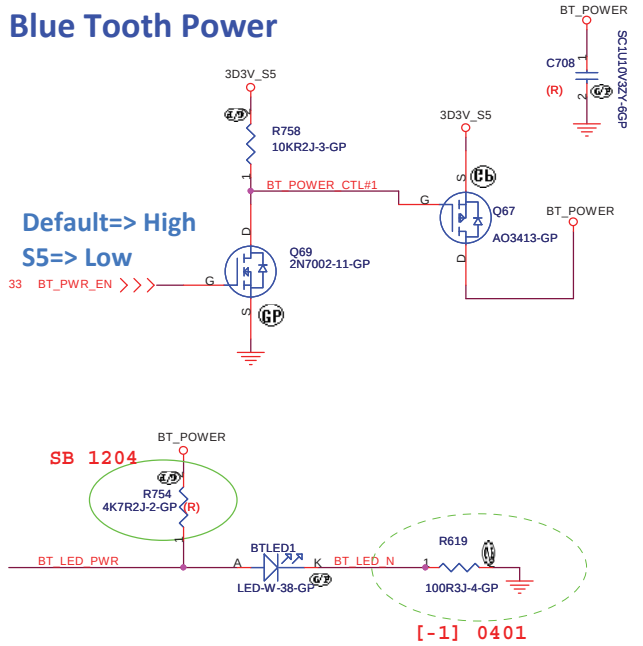


HDD Power Connector

Layout: Please put them together



Blue Tooth Power



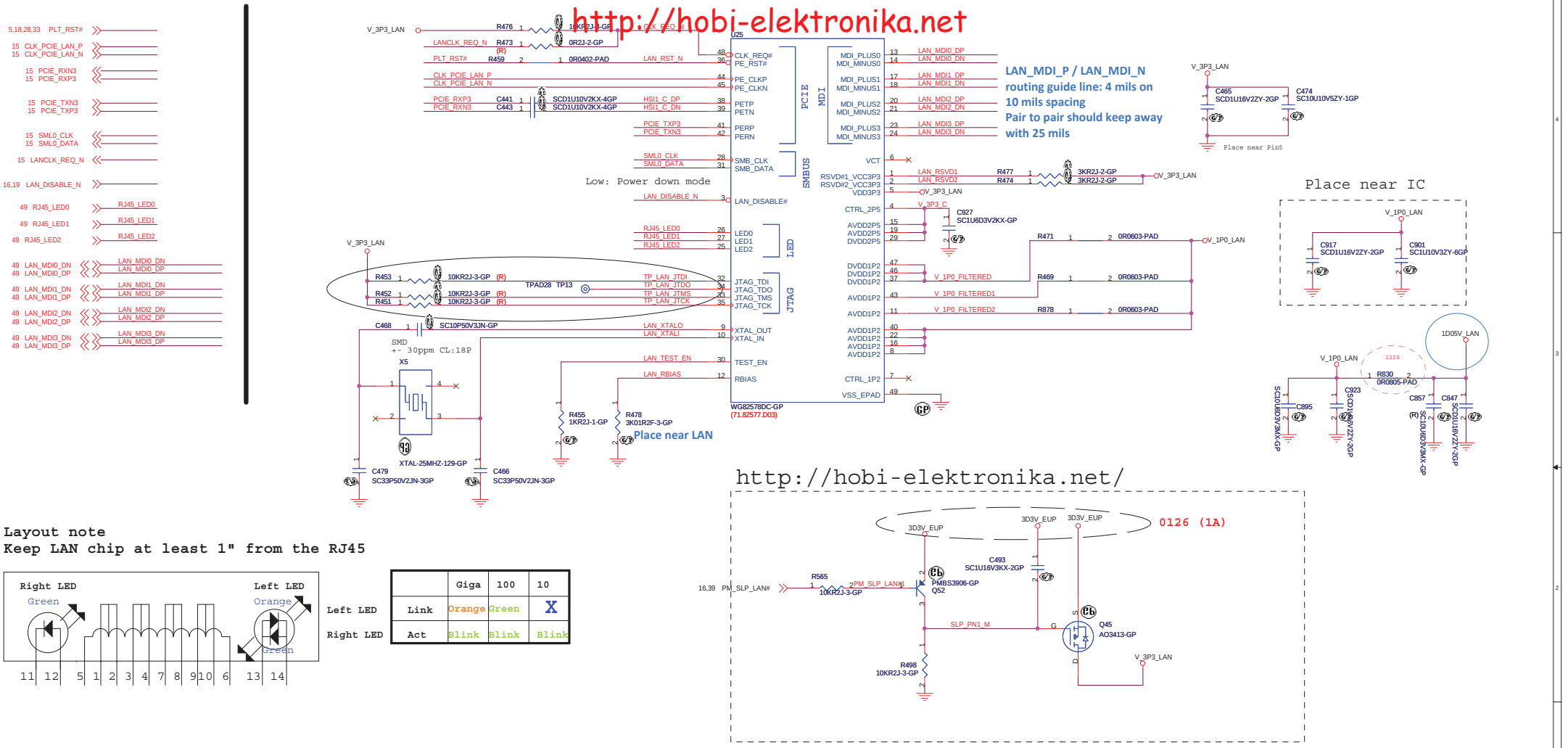
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **HDD/ODD IF+USB device**

Size: A3 | Document Number: **Catalina** | Rev: **SA**

Date: Tuesday, April 06, 2010 | Sheet 26 of 59



Layout note
Keep LAN chip at least 1" from the RJ45

	Giga	100	10
Left LED Link	Orange	Green	X
Right LED Act	Blink	Blink	Blink

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: INTEL Gb LAN-WG82577LC

Size: Custom | Document Number: Catalina | Rev: SA

Date: Tuesday, April 06, 2010 | Sheet 27 of 59

15 CLK_PCIE_CR_P
15 CLK_PCIE_CR_N
15 PCIE_RXP4
15 PCIE_RXN4
15 PCIE_TXP4
15 PCIE_TXN4
5,18,27,33 PLT_RST#

From VT6325 Internal LDO

Layout: Close to VT6325

Layout: Close to Card connector

VIA VT6325

Pin17 is floating

Disable EEPROM function	Mount 4.7kohm
EEPROM Enable	Unmount

1221 (SC)

1394 port Common Choke

Close to FIRE1

TR1 ACM2012H-900-GP-DUMMY (R)
TR2 ACM2012H-900-GP-DUMMY
69.10087.011 Chilisin
28.00201.141 Murata

Front 4pin SB 1210

If using 6pin CONN, please separate shielding GND and signal GND.

XCPS Definition:
For 6pin type of 1394, mount 11kohm res to +12V.
For 4pin type, unmount 11kohm res.
Both of type need mount 1kohm to GND.

Near the chip

CLOSE TO connector

SB 1204

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

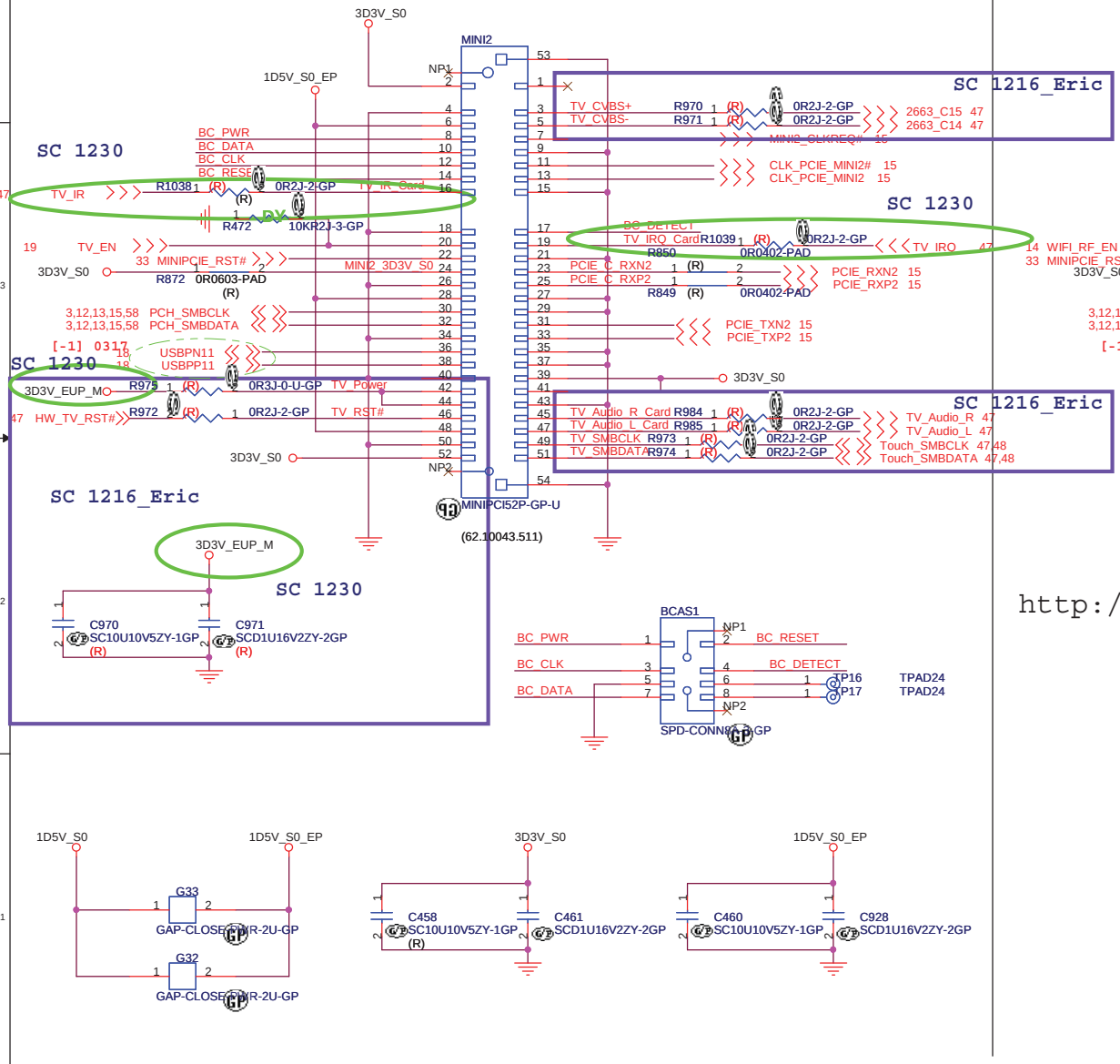
Title: VT6325 1394/CARD READER

Size	Document Number	Rev
C	Catalina	SA

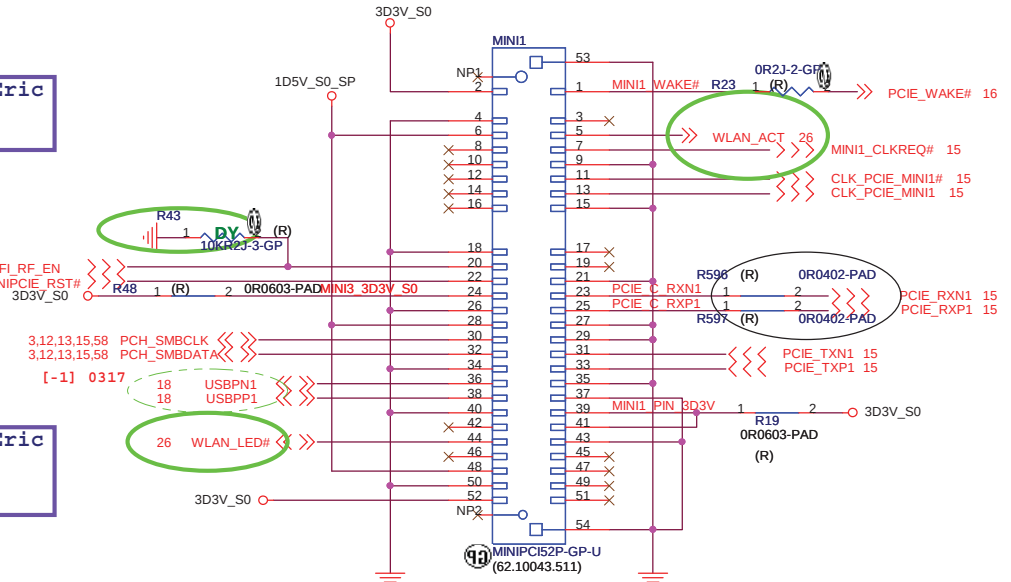
Date: Tuesday, April 06, 2010 Sheet 28 of 59

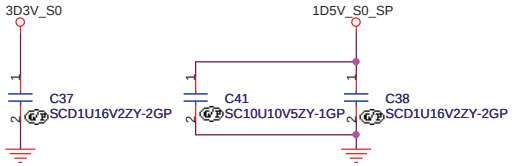
Mini PCI-E Connector

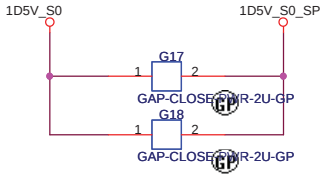
TV-TUNER Card



Wireless Card(Present support EP/SP)







<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINI CARD CONN(1/2) .

Size	Document Number	Rev
B	Catalina	SA

Date: Tuesday, April 06, 2010 Sheet 29 of 59

To PCH

14 ACZ_RST#_AUDIO >> ACZ_RST#_AUDIO
14 ACZ_SYNC_AUDIO >> ACZ_SYNC_AUDIO
14 ACZ_SDATAIN0 >> ACZ_SDATAIN0
14 ACZ_BITCLK_AUDIO >> ACZ_BITCLK_AUDIO
14 ACZ_SDATAOUT_AUDIO >> ACZ_SDATAOUT_AUDIO
14 ACZ_SPKR >> ACZ_SPKR

MIC JK IN

32 MIC_R_JACK >> MIC_R_JACK
32 MIC_L_JACK >> MIC_L_JACK

SPDIF

49 SPDIF << SPDIF

Jack Detect

32 MIC_IN_JD >> MIC_IN_JD
32 HP_OUT_JD >> HP_OUT_JD

AMP mute logic use

32 EAPD# << EAPD#

Put near Pin38

near codec

SB 1209

AUDIO OUT TO SCALAR

32 PC_AUDIO_L << PC_AUDIO_L
32 PC_AUDIO_R << PC_AUDIO_R

U2

REALTEK
ALC272
(LQFP-48)

ALC272-GR/GP

SB 1209
DELETE!!

SPDIF OUT

[-1] 0317

EXT_MIC

MIC_R_JACK 32
MIC_L_JACK 32

48 HP_DET_MUTE#

14 ACZ_SPKR

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO CODEC-ALC272

Size: Custom | Document Number: Catalina | Rev: SA

Date: Tuesday, April 06, 2010 | Sheet 30 of 59

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserve*

Size	Document Number	Rev
B	Catalina	SA

Date: Tuesday, April 06, 2010 Sheet 31 of 59

HP JACK (14/15)

Cehck Jack Spec

MIC IN

30 MIC_L_JACK
30 MIC_R_JACK

HP OUT

30 ALC272_HP_OUT_L → ALC272_HP_OUT_L
30 ALC272_HP_OUT_R → ALC272_HP_OUT_R

JACK DETECT

30 MIC_IN_JD → MIC_IN_JD
30 HP_OUT_JD → HP_OUT_JD

30 EAPD# → EAPD#

47,48 TPA3113_SD# → TPA3113_SD#

LINE OUT to Scalar

30 PC_AUDIO_R → PC_AUDIO_R
30 PC_AUDIO_L → PC_AUDIO_L

47 PC_AUDIO_R_C → PC_AUDIO_R_C
47 PC_AUDIO_L_C → PC_AUDIO_L_C

HP OUT

SB 1209 DELETE!!

5V_EUP
AUD_AGND
MUTE_LO#
MUTE_LO*
R65 10KR2J-3-GP
R70 4K7R2J-2-GP
Q8 PMBS3906-GP
R10 1KR2J-1-GP
R8 100R2J-2-GP
R9 100R2J-2-GP
R11 1KR2J-1-GP
ALC272_HP_OUT_L
ALC272_HP_OUT_R
Impedance=60 ohm
L3 FCM1608KF-1-GP
L4 FCM1608KF-1-GP
HP_OUT_L_C
HP_OUT_R_C
HP_OUT_JD
C1 SC100P50V2JN-3GP (R)
C5 SC100P50V2JN-3GP
C6 SC100P50V2JN-3GP
D1 (R) MLVG0402SR005BP-GP
D2 (R) MLVG0402SR005BP-GP
HPOUT1 AUDIO-JK132-GP
D6 AZ2025-02S-GP
R22 4K7R2J-2-GP
R21 4K7R2J-2-GP
Q2 PMBS3904-1-GP
Q1 PMBS3904-1-GP
ALC272_MUTE
R64 100KR2J-1-GP
D25 1N4148W-1-GP
R46 10KR2J-3-GP
Q6 PMBS3904-1-GP
EAPD#
R84 10KR2J-3-GP
Q9 MMBT3904-7-F-GP (R)
TPA3113_SD#

If use: 83.02025.0A1

FRONT MIC JACK (21/22)

MIC IN

MIC_L_JACK
MIC_R_JACK
Impedance=60 ohm
L1 FCM1608KF-1-GP
L2 FCM1608KF-1-GP
MIC_IN_L_JK
MIC_IN_R_JK
MIC_IN_JD
C4 SC100P50V2JN-3GP (R)
C2 SC100P50V2JN-3GP
C3 SC100P50V2JN-3GP
D4 (R) MLVG0402SR005BP-GP
D3 (R) MLVG0402SR005BP-GP
MICJK1 AUDIO-JK132-GP
D5 AZ2025-02S-GP

If use: 83.02025.0A1

Speaker Out (35/36) Placement Near Scalar

PC_AUDIO_R
PC_AUDIO_L
R605 0R0402-PAD
R604 0R0402-PAD
C572 SC22U6D3V5MX-2GP
C571 SC22U6D3V5MX-2GP
PC_AUDIO_R_1
PC_AUDIO_L_1
PC_AUDIO_R_C
PC_AUDIO_L_C
near codec
near codec

SB 1209
SB 1209
SC 1226

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO HP_JK/ MIC_JK

Size: A3 | Document Number: Catalina | Rev: SA

Date: Tuesday, April 06, 2010 | Sheet 32 of 59

Fan Controller

34 CPU_FAN_TACH1 — CPU_FAN_TACH1
34 CPU_FAN_PWM1 — CPU_FAN_PWM1
34 SYS_FAN_TACH1 — SYS_FAN_TACH1
34 SYS_FAN_PWM1 — SYS_FAN_PWM1

Please check it's pull-high location

LPC interface

14,34 LPC_LFRAME# — LPC_LFRAME#
14,34 LPC_LAD0 — LPC_LAD0
14,34 LPC_LAD1 — LPC_LAD1
14,34 LPC_LAD2 — LPC_LAD2
14,34 LPC_LAD3 — LPC_LAD3
19 KBRCIN# — KBRCIN#
19 KA20GATE — KA20GATE
18 CLK_PCI_SIO — CLK_PCI_SIO
5,18,27,28 PLT_RST# — PLT_RST#
14 INT_SERIRQ — INT_SERIRQ

15 PCH_CLK48 — PCH_CLK48
16 RSMRST#_SIO — RSMRST#_SIO
35,44,47 SIO_PSON_N — SIO_PSON_N
16,36 PWRGD3V_150MS — PWRGD3V_150MS
26 SIO_PWRLED_N — SIO_PWRLED_N
16 SIO_PWNBTN_N — SIO_PWNBTN_N
26 PWRBTN_N — PWRBTN_N
18 LPC_PME_N — LPC_PME_N
16,35,43 PM_SLP_S3# — PM_SLP_S3#
16,25,38 PM_SLP_S4# — PM_SLP_S4#
16,36,42,43 CORE_PWRGD — CORE_PWRGD
52 GPU_DPLUS — GPU_DPLUS
52 GPU_DMINUS — GPU_DMINUS
51,52 PLT_RST_ATI# — PLT_RST_ATI#

1228 (SC)
47 SOUT1 — SOUT1
47 SIO_SIN1 — SIO_SIN1
[-1] 0317

BT_PWR_EN R759 10KR2J-3-GP
SIO_PSON_N R787 10KR2J-3-GP
RSMRST# SIO R782 4K7R2J-2-GP
LPC_PME_N R785 4K7R2J-2-GP
SIO_PWRLED_N R789 4K7R2J-2-GP
SIO_PWNBTN_N R784 4K7R2J-2-GP

3D3V_S0
SRN10KJ-6-GP
RN44 (R)
LPC_LAD3 LPC_LAD2 LPC_LAD1 LPC_LAD0
SRN10KJ-5-GP
RN43
LPC_LFRAME# KBRCIN#
INT_SERIRQ R756 1KR2J-1-GP
KA20GATE R762 1KR2J-1-GP (R)
PWRGD3V_150MS R709 1KR2J-1-GP
MINIPCIE_RST# R45 1KR2J-1-GP

1226 (SC)

KA20GATE R1052 680R2J-3-GP
[-1] 0406

3D3V_S0
RN45
RTS1_N SOUT1 DTR1_N RI1_N
SRN10KJ-6-GP
47 SIO_SIN1 — SIO_SIN1
[-1] 0317

5V_S0
RN46
SIO_MCLK SIO_MDAT SIO_KCLK SIO_KDAT
SRN2K2J-2-GP

3D3V_EUP
L37 FCM1608KFG-301T05-GP
Q70 2N7002-11-GP
SIO_PSON_N
AVCC3
C724 SCD1U16V2ZY-2GP
C712 SC22U6D3V5MX-2GP
R760 330R3J-L-GP

Install N-Mos and Current-Limit
Resistor when in S5 for power-saving.

SuperIO Power-Save

AVCC3 SIO_VIN1
SIO_VIN4 SIO_VIN5 SIO_VIN6 HWM_REF GPU_DPLUS
AVCC3 VIN1 VIN4 VIN5 VIN6 VIN7 TMPIN1

0126 (1A)
R764 0R0402-PAD
VTT_PWRGD 5,35,39

GPU_DPLUS C756 SC2200P50V3KX-LGP GPU_DMINUS
HWM_REF C772 SC1U16V3ZY-GP
SIO_GND

U43
64-LQFP
IT8758E-GP

CTS1# 3VSB FAN_TAC1 FAN_CTL1 FAN_TAC2/GP52 FAN_CTL2/GP51 GNDD 5VSB_CTRL GP21 GP20 CIRTX1 PCIRST2#/GP11 3VSB VCORE LRESET SERIRQ
TMPIN2 TSD- GNDA RSMRST#/CIRRX1/GP55 PCIRST3#/GP10 MCLK/GP56 MDAT/GP57 KCLK/GP60 KDAT/GP61 3VSBSW#/GP40 PWRGD3_150MS SUSC#/GP53 PSON#/GP42 PANSHW#/GP43 PME#/GP54 PWRON#/GP44
SYS_TEMP_HDD GPU_DMINUS RSMRST#_SIO PLT_RST_ATI# SIO_MCLK SIO_MDAT SIO_KCLK SIO_KDAT SIO_PWRLED_N PWRGD3V_150MS PM_SLP_S4# SIO_PSON_N PWRBTN_N LPC_PME_N SIO_PWNBTN_N
LFRAME# LAD0 LAD1 LAD2 LAD3 KRST# PCICLK CLKIN GNDSI 5VSB_DIAMDTSI_D PCHSM_C/PECI/AMDTSI_C 3VSB VBAT 3V_5V SUSB#

0126 (1A)

3D3V_S5
C713 SCD1U16V2ZX-2GP
34 CPU_FAN_TACH1 — CPU_FAN_TACH1
34 CPU_FAN_PWM1 — CPU_FAN_PWM1
34 SYS_FAN_TACH1 — SYS_FAN_TACH1
34 SYS_FAN_PWM1 — SYS_FAN_PWM1
SIO_EUP_EN
26 BT_PWR_EN — BT_PWR_EN
PC_SYNC_INT# R
29 MINIPCIE_RST# — SIO_IRTX / MINIPCIE_RST#
PLT_RST# INT_SERIRQ

[-1] 0402
TPAD28 TP53 R1030 0R2J-2-GP (R) PC_SYNC_INT# R

C740 SCD1U16V2ZX-2GP
SB 1201
C709 SCD022U16V2KX-3-LL-GP

If without use these pins, Please pull-up. Don't let it floating
1.Pin 54:VIN3/ATXPG
2.Pin 32:SUSB#
3.Pin 23/ Pin 58/ Pin 60/ Pin 62
4.Pin55 need 2.8V

Note:use EUP function:Pin32/Pin33/Pin34/Pin37/Pin39/Pin45 pull high to SYS_3VSB.

If not use PECI, pin 27 28 could be configured as SMBus.

G30 GAP-CLOSE-PWR

LPC_LFRAME# LPC_LAD0 LPC_LAD1 LPC_LAD2 LPC_LAD3 KBRCIN# KA20GATE CLK_PCI_SIO PCH_CLK48
15 SIO_SDA1 — SIO_SDA1
15 SIO_SCL1 — SIO_SCL1

PM_SLP_S3# R1049 4K7R2J-2-GP 3VSB_DET
RTC_AUX_S5 3D3V_EUP
C746 SCD1U16V2ZY-2GP
C751 SCD1U16V2ZY-2GP
[-1] 0317

Layout Note:
The trace between IT8758(Pin25) & oscillator (output) must Thicken and Shorten. In addition to that, the trace spacing must broaden.

SuperIO power monitoring inputs
Please set R value depend on what you need.

SIO_VIN1 — R771 6K8R2F-2-GP — 5V_S0
C743 SCD1U16V2ZY-2GP — R766 10KR2F-2-GP
SIO_GND
SIO_VIN4 — R767 10KR2F-2GP — 1D5V_S3
C741 SCD1U16V2ZY-2GP
SIO_GND
SIO_VIN5 — R775 2HM_V_1P1 — G28 GAP-CLOSE-PWR — 1D05V_S0
C747 SCD1U16V2ZY-2GP
SIO_GND
SIO_VIN6 — R776 2HM_V_CPU — G29 GAP-CLOSE-PWR — VCC_CORE
C754 SCD1U16V2ZY-2GP
SIO_GND

SuperIO power monitoring inputs

HWM_REF — R783 7K68R2F-GP (R) — SYS_TEMP_HDD
SC 1216_Eric
TP14 TPAD28
TP38 TPAD28
Near Together
SIO_GND

Placement Near Venting Hole

SYS_TEMP_HDD — R235 0R0402-PAD — SYS_TEMP_VENTING
C761 SC2200P50V3KX-LL-GP
GPU_DMINUS — R238 0R0402-PAD — SYS_TEMP_VENTING_G
Q22 PMBS3904-1-GP
SB 1201
CAP close to ITE8758

[-1] 0401
R1026 0R0805-PAD
R744 (R) 0R5J-5-GP
Q65 AO3413-GP
5V_S5 — 5V_EUP
EuP Controller signal
R757 100KR2J-1-GP
C706 SCD1U16V2ZY-2GP
Q92 AO3413-GP (R)
5V_EUP_M
R755 10KR2J-3-GP
5V_EUP_EN# — 5V_EUP_EN# G
SC 1226
C704 SC1U10V3ZY-6GP
5V_EUP — 5V_EUP_M
R1028 (R) 0R5J-5-GP
3D3V_S5
R947 10KR2J-3-GP
Q66 2N7002-11-GP
SB 1210
SIO_EUP_EN
5VSB_CTRL(EUP control)
High : Enable (default)
LOW : Disable (EUP Enable)
SC 1226

[-1] 0401
R1027 0R0805-PAD
R752 (R) 0R5J-5-GP
Q64 AO3413-GP
3D3V_S5 — 3D3V_EUP
EuP Controller signal
R753 100KR2J-1-GP
C701 SCD1U16V2ZY-2GP
Q90 AO3413-GP (R)
3D3V_EUP_M
R751 10KR2J-3-GP
3V_EUP_EN# — 3V_EUP_EN# G
SC 1226
C702 SC1U10V3ZY-6GP
3D3V_EUP — 3D3V_EUP_M
R1029 0R5J-5-GP (R)
Q68 2N7002-11-GP
SIO_EUP_EN
SB 1210
SC 1226

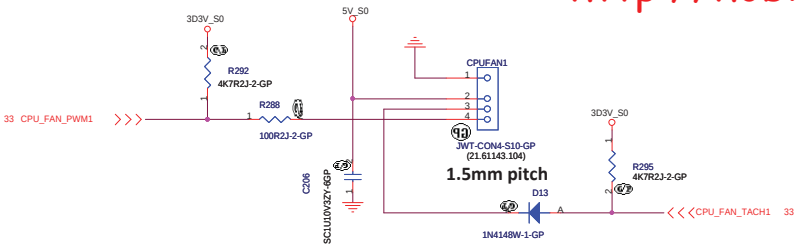
http://hobi-elektronika.net/

3D3V_EUP
R794 47KR2J-2-GP (R)
PM_SLP_S3# 2 — Q71 PMBS3904-1-GP (R)
PWRGD3V_150MS — Q72 PMBS3904-1-GP (R)
16,35,43 PM_SLP_S3# — PM_SLP_S3# — R778 10KR2J-3-GP (R) — PM_SLP_S3# 1

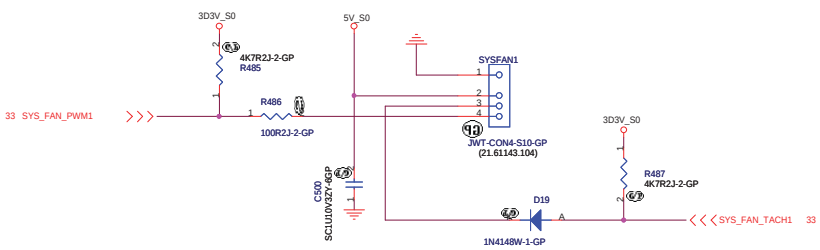
<Core Design>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	SIO ITE8758
Size C	Document Number: Catalina — Rev: SA
Date: Tuesday, April 06, 2010	Sheet 33 of 59

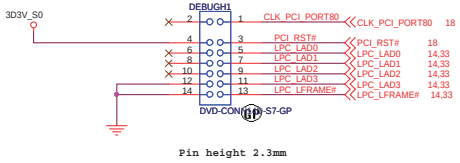
CPU FAN



MXM_SYS_FAN

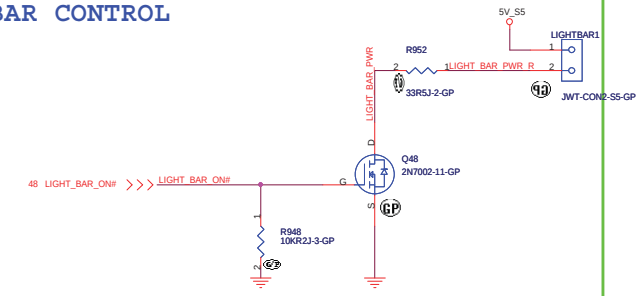


LPC DEBUG PORT

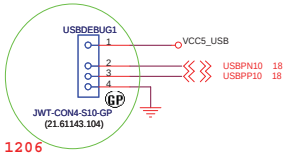


Pin height 2.3mm

LIGHT BAR CONTROL

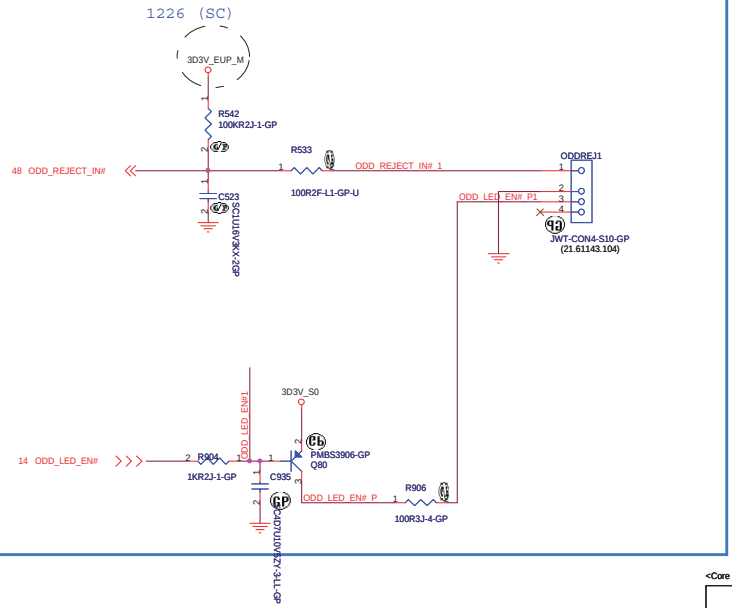


USB RESERVE



SB 1206

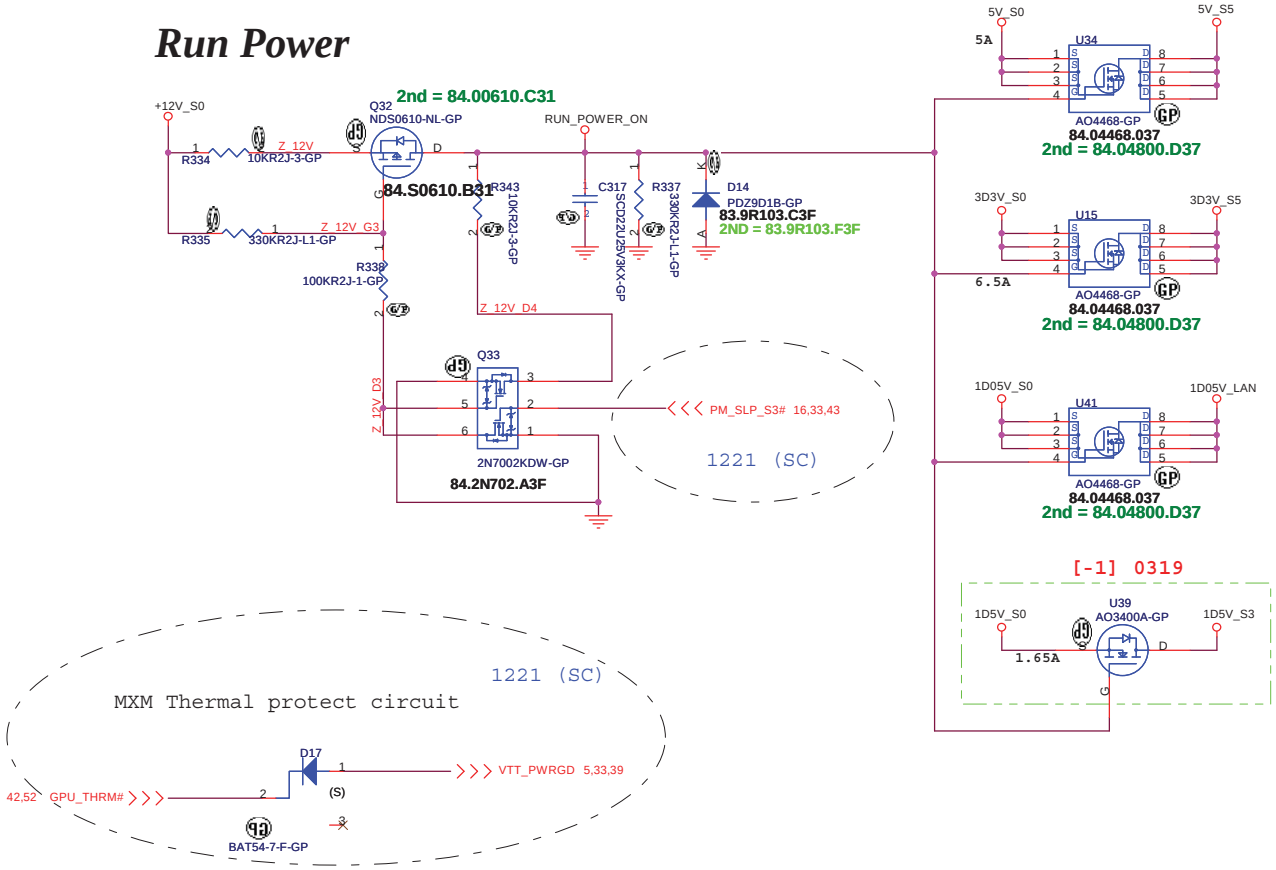
ODD REJECTION

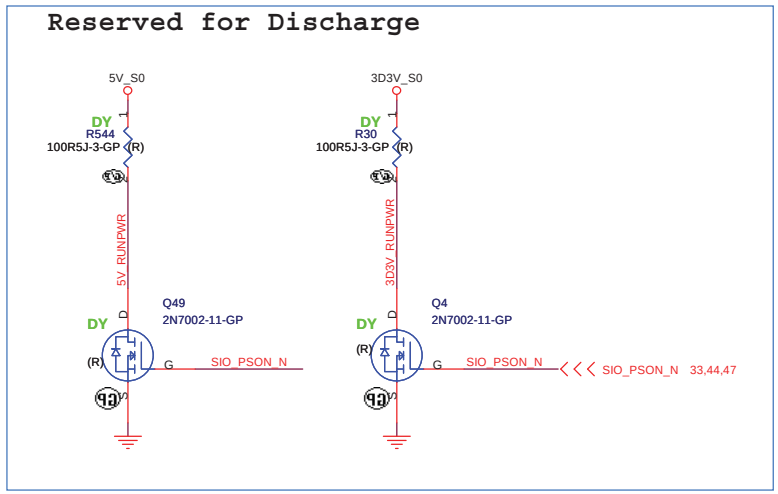


<Core Design>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: Fan control		
Size: C	Document Number: Catalina	Rev: SA
Date: Tuesday, April 06, 2010	Sheet 34 of 59	

Run Power





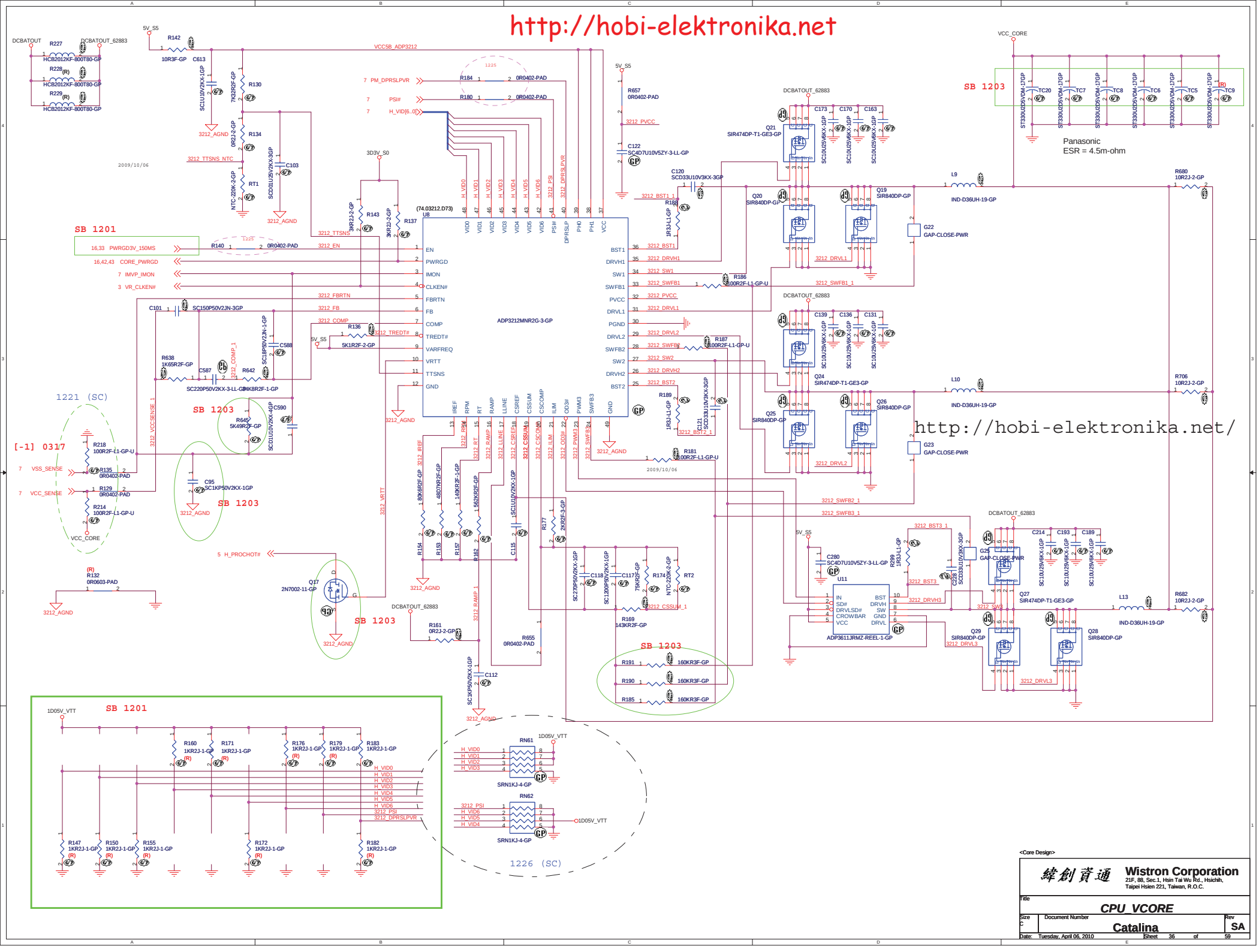
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

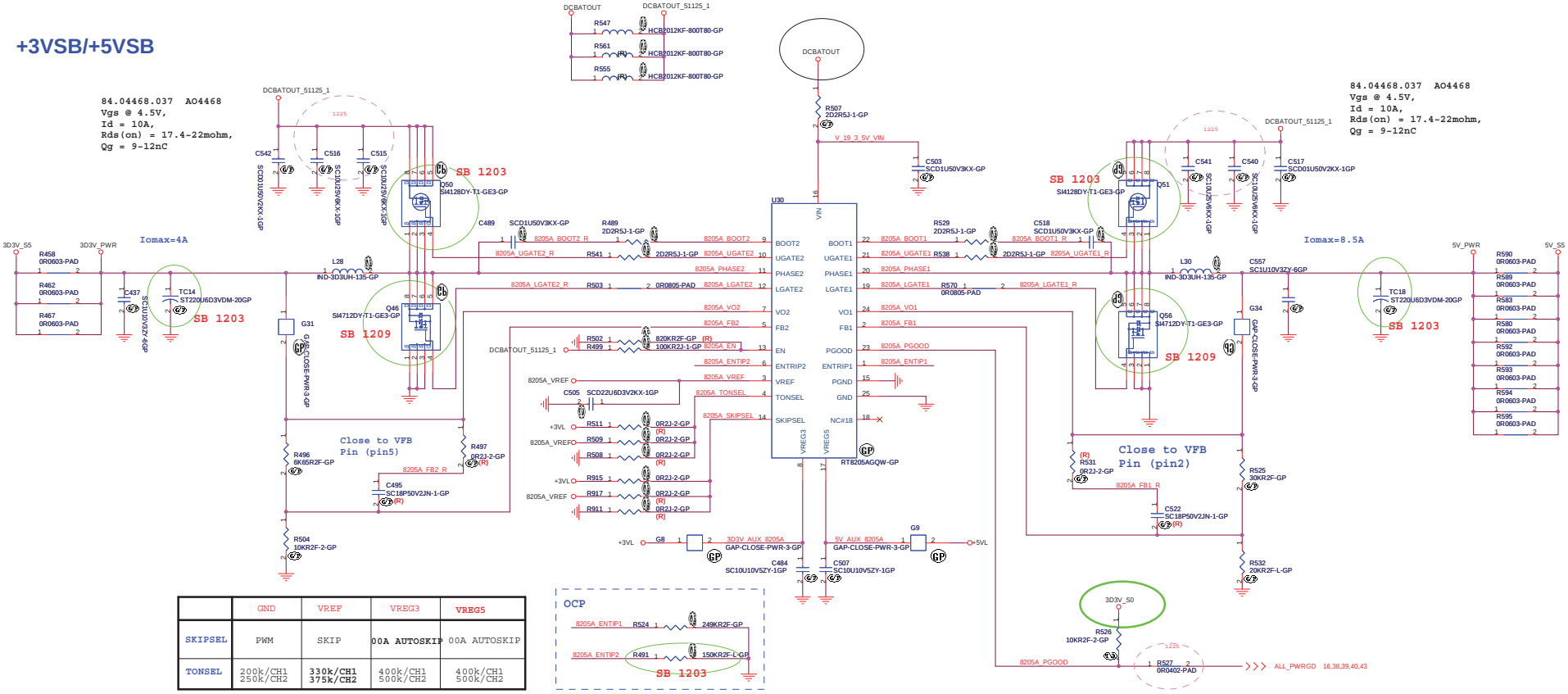
Title: Run Power

Size	Document Number	Rev
A3	Catalina	SA

Date: Tuesday, April 06, 2010 Sheet 35 of 59



+3VSB/+5VSB



	GND	VREF	VREG3	VREG5
SKIPSEL	PWM	SKIP	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	330k/CH1 375k/CH2	400k/CH1 500k/CH2	400k/CH1 500k/CH2

<Core Design>

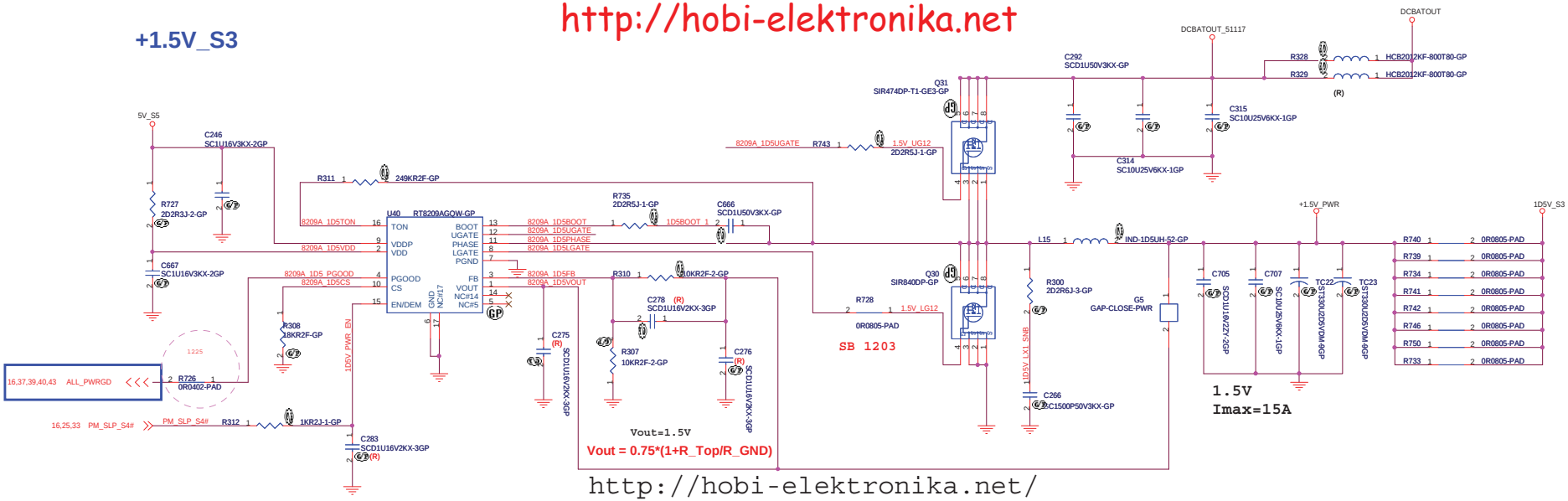
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8205A 3V&5V

Size: A2 | Document Number: Catalina | Rev: SA

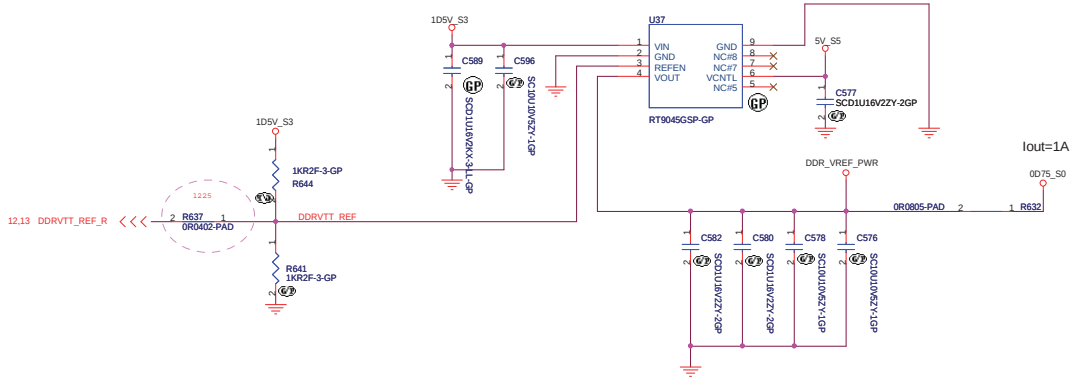
Date: Tuesday, April 06, 2010 | Sheet 37 of 59

+1.5V_S3



http://hobi-elektronika.net/

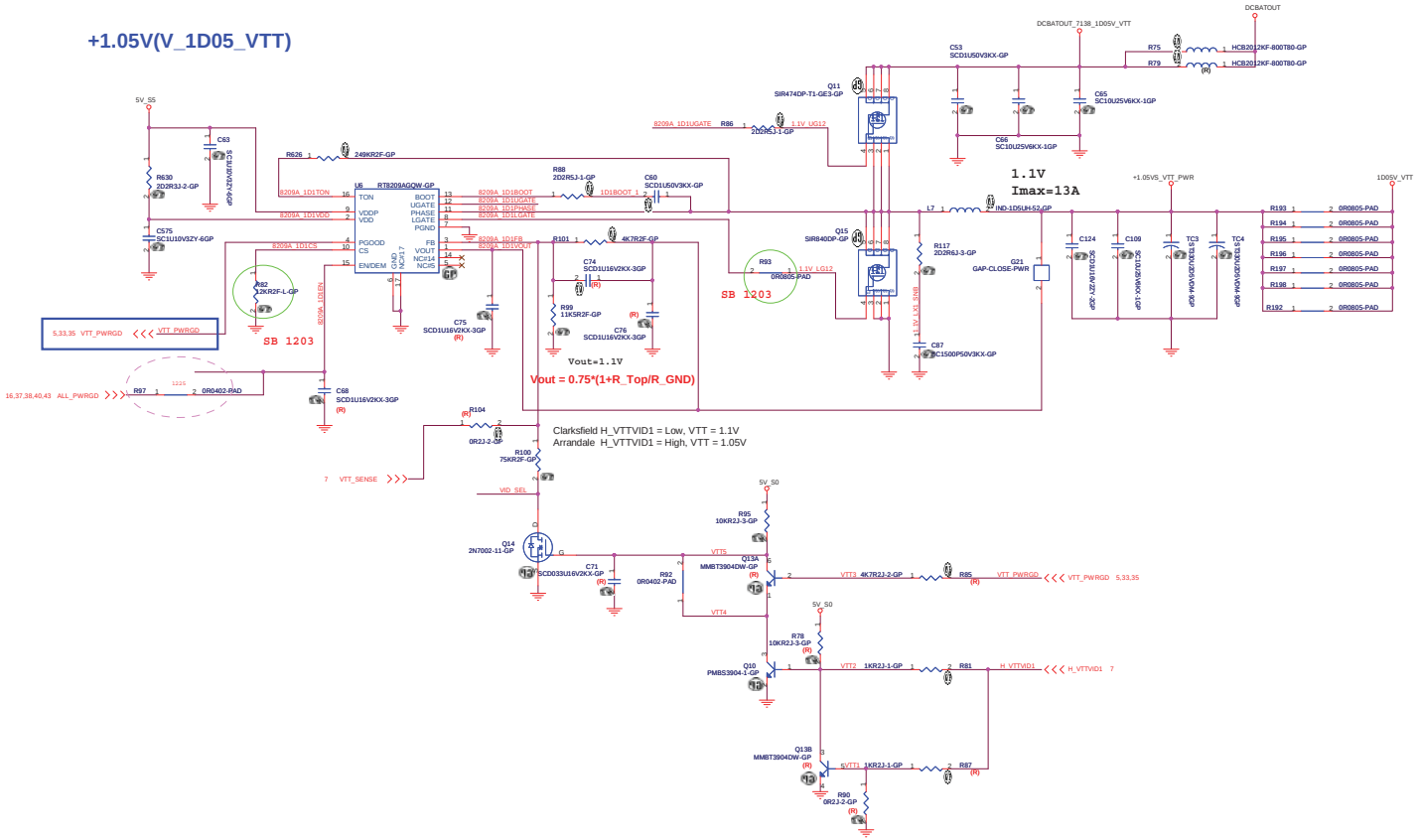
+0.75V_MEM_VTT



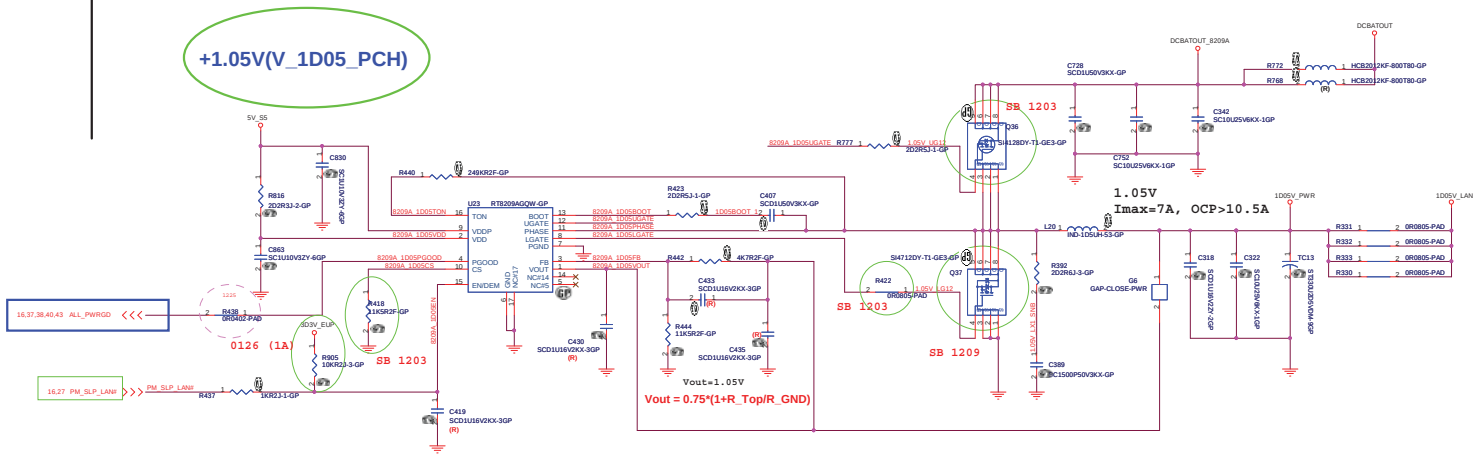
<Core Design>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	+1.5V/+0.75V	
Size: C	Document Number: Catalina	Rev: SA
Date: Tuesday, April 06, 2010	Sheet 38 of 59	

+1.05V(V_1D05_VTT)



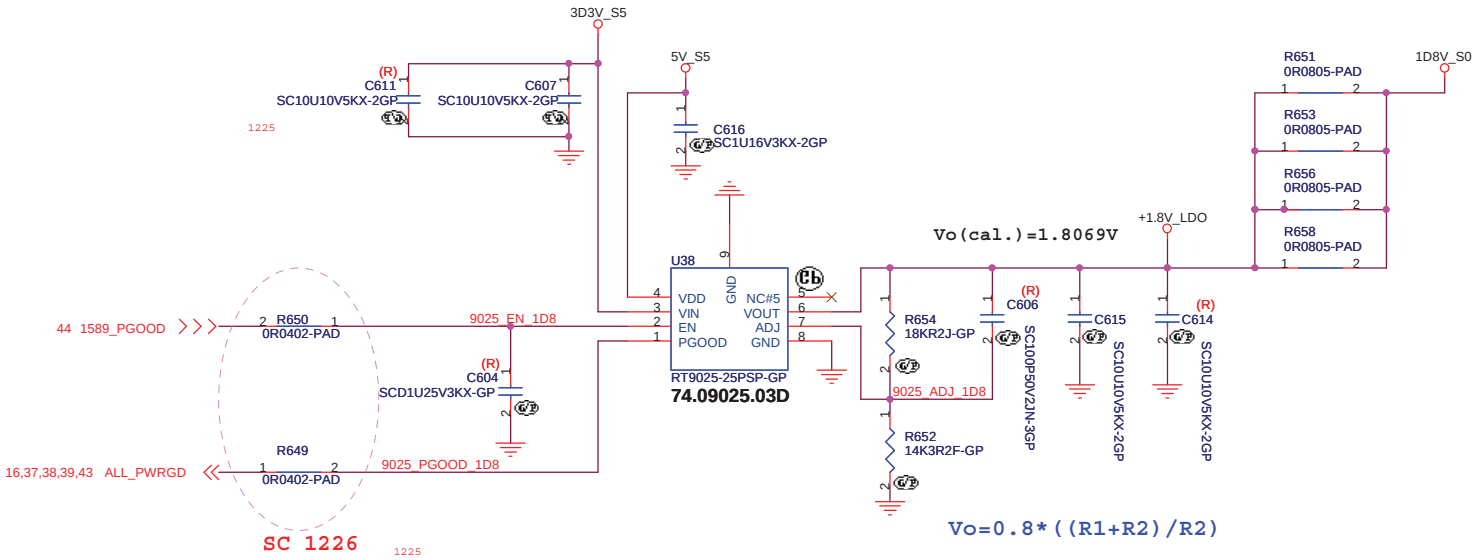
+1.05V(V_1D05_PCH)



<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

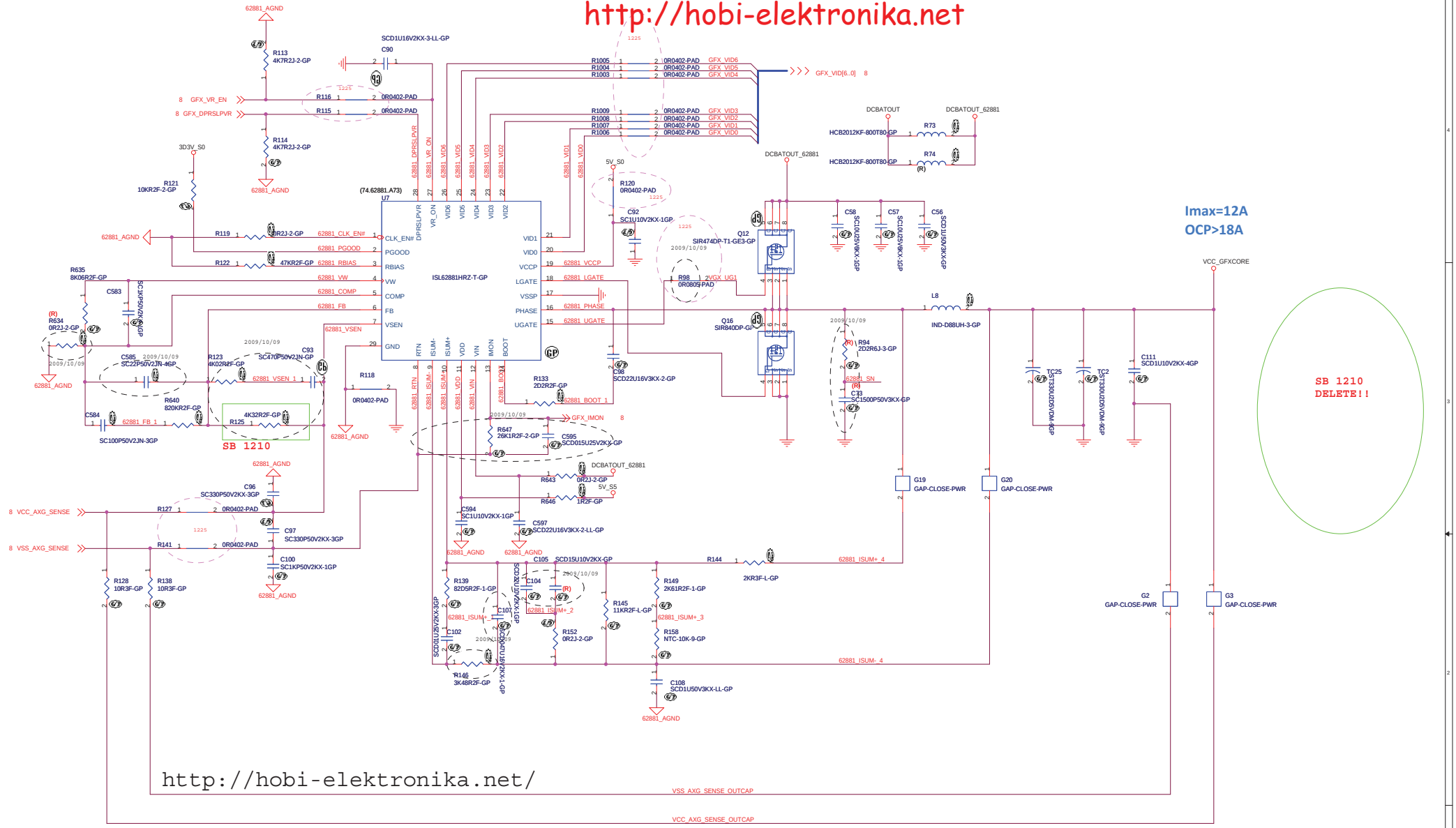
Title: V_1P1_VTT/ V_1P05_PCH
Size: Custom | Document Number: Catalina | Rev: SA
Date: Tuesday, April 06, 2010 | Sheet 39 of 59

1D8V_S0 (RT9025)



<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: 1D8V POWER		
Size: B	Document Number: Catalina	Rev: SA
Date: Tuesday, April 06, 2010	Sheet 40 of 59	



<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***GFX_Vcore***
Size: C	Document Number: **Catalina**
Rev: SA	
Date: Tuesday, April 06, 2010	Sheet 41 of 59

For GPU Core and GPIO15/20 relationship as below:

VID1(GPIO20)	VID0(GPIO15)	Core
0	0	1.22V
0	1	1.02V
1	0	1.12V
1	1	0.92V

0.9V~1.2V@20A
OCP>30A

VGA power sequence modify!!

SB 1209

SB 1209

SB 1201

SB 1201

SB 1201

SB 1201

[Park] R412=30.9k
[Madison] R412=28k

[-1] 0317

<Core Design>

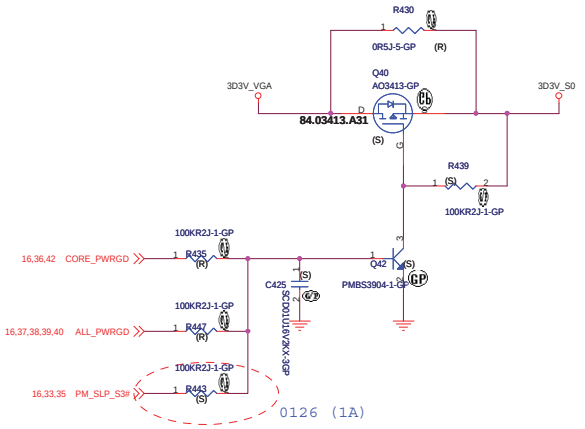
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

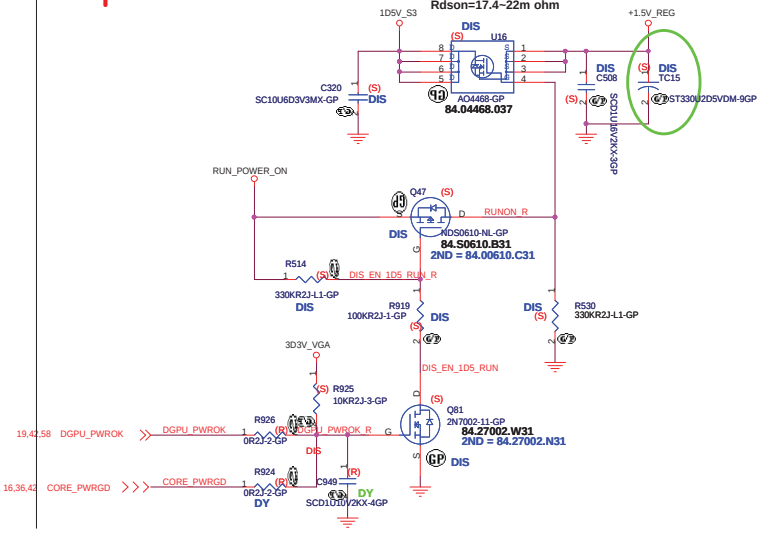
Title: MXM_GFX_Vcore

Size: C | Document Number: Catalina | Rev: SA

Date: Tuesday, April 06, 2010 | Sheet 42 of 59

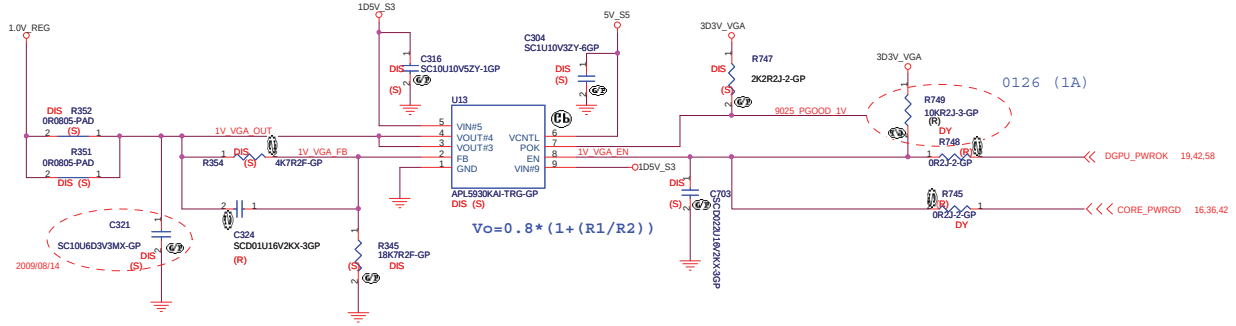
3D3V_S0 to 3D3V_DELAY Transfer





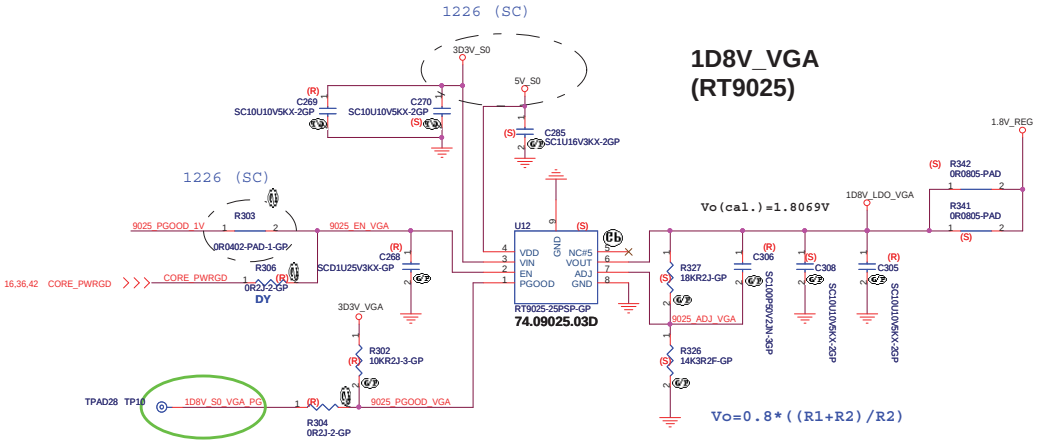
Iout=1.5A

Vout= 1V_VGA



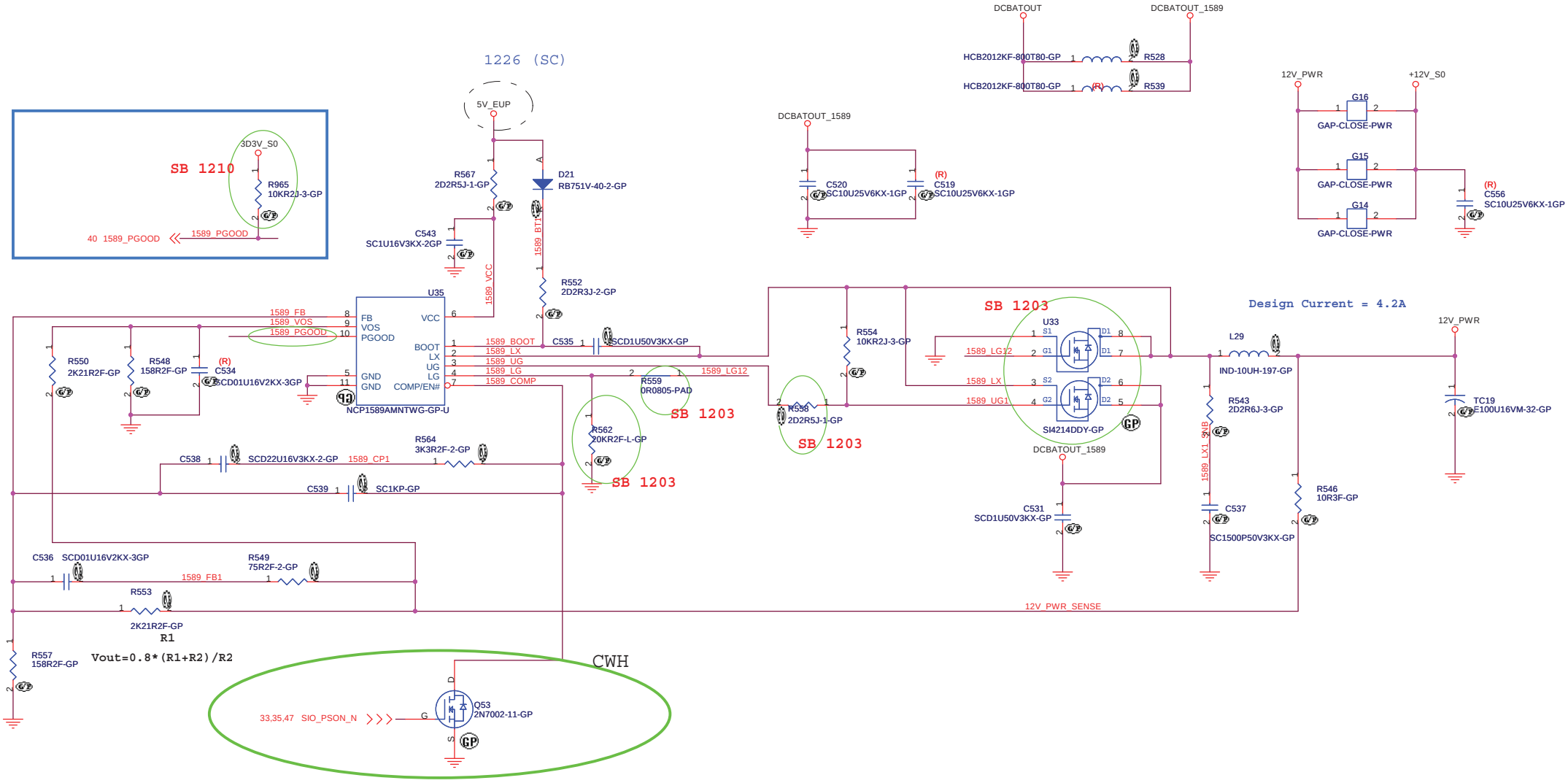
1226 (SC)

1D8V_VGA (RT9025)



<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**1.8V_REG/1V_PCIE**
Size C	Document Number: **Catalina**
Rev	SA
Date: Tuesday, April 06, 2010	Sheet 43 of 59

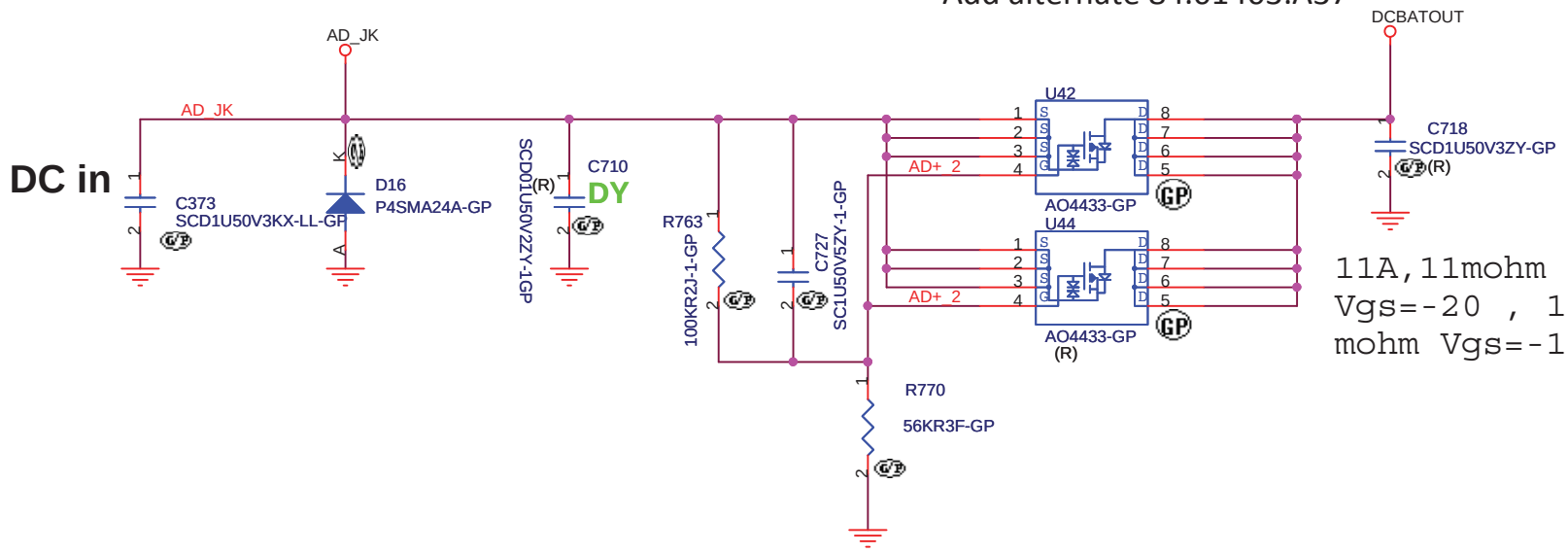


<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***+12V***
Size: Custom	Document Number: **Catalina**
Rev	**SA**
Date: Tuesday, April 06, 2010	Sheet 44 of 59

Adaptor in to generate DCBATOUT

Add alternate 84.01403.A37



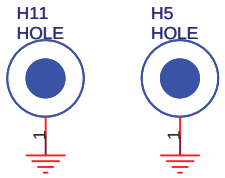
11A,11mohm <14mohm
Vgs=-20 , 14mohm <18
mohm Vgs=-10

<Core Design>

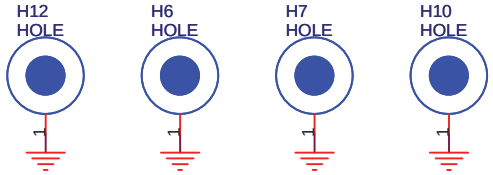
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

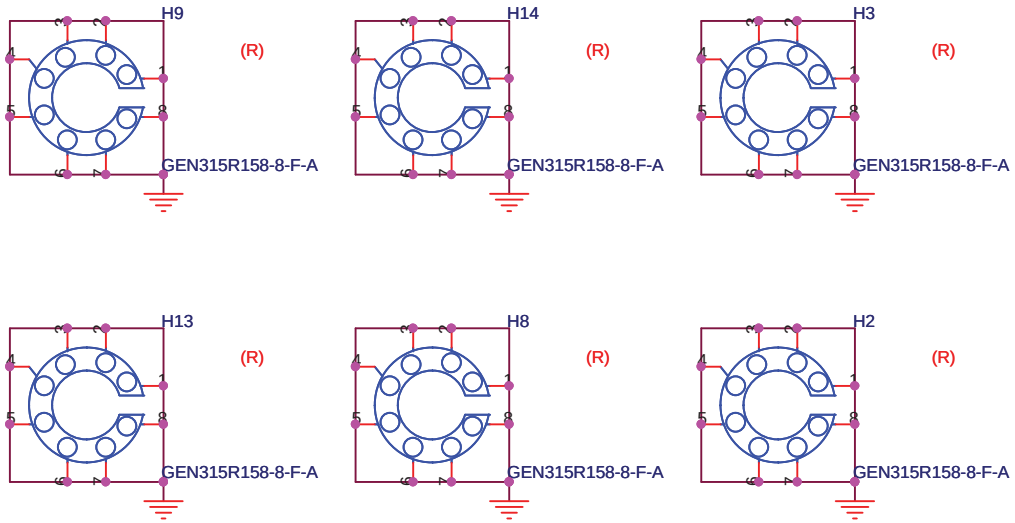
Title	***DC IN***	
Size A4	Document Number **Catalina**	Rev **SA**
Date: Tuesday, April 06, 2010	Sheet 45 of 59	

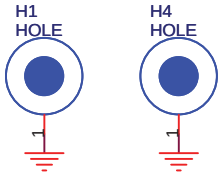
Mini PCIE holder



FAN holder



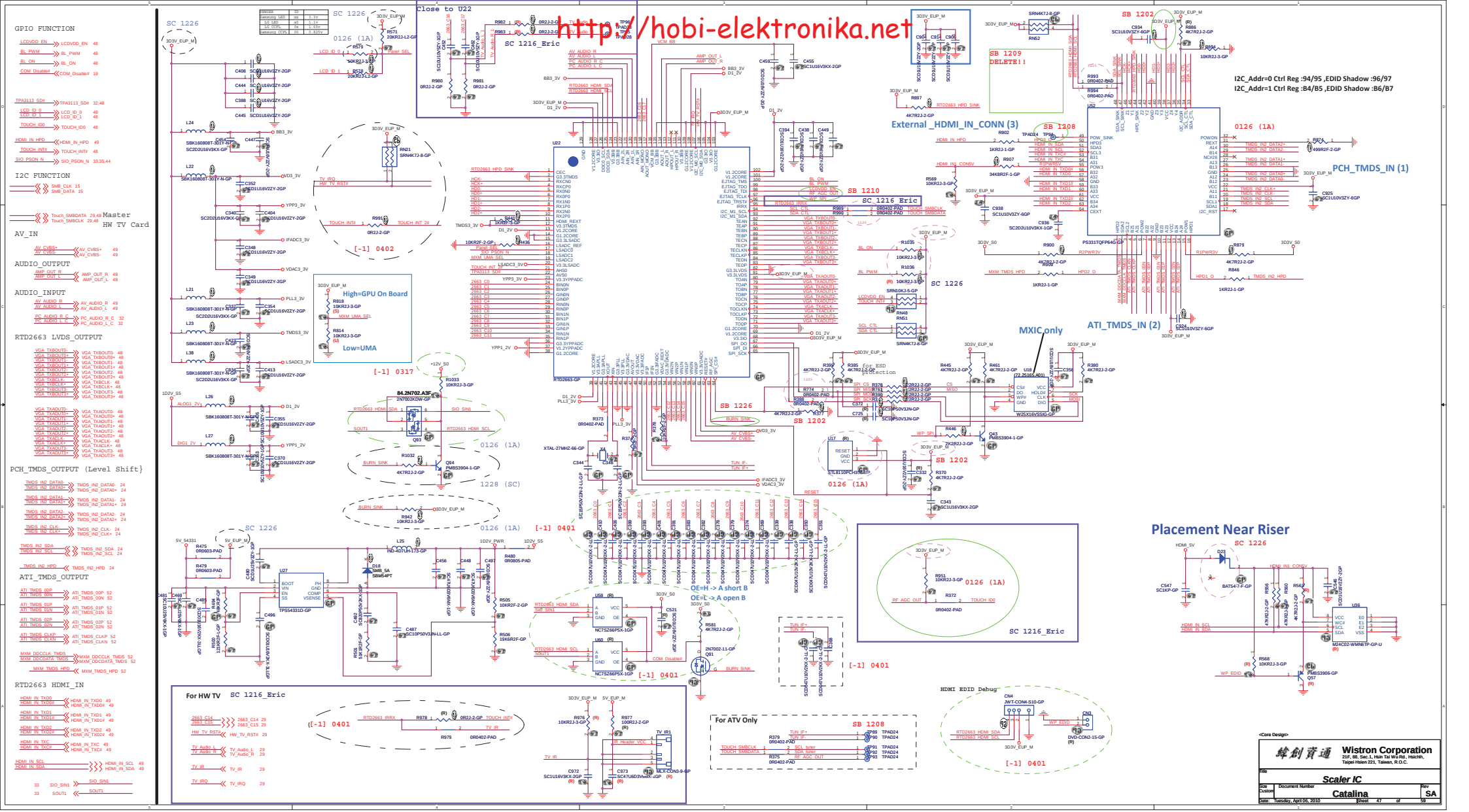




<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Screw hole***		
Size: A4	Document Number: **Catalina**	Rev: **SA**
Date: Tuesday, April 06, 2010	Sheet 46 of 59	


http://hobi-elektronika.net
GPIO FUNCTION
I2C FUNCTION
Master
HW TV Card
AV_IN
AUDIO_OUTPUT
AUDIO_INPUT
RTD2663 LVDS_OUTPUT
PCH_TMDS_OUTPUT (Level Shift)
ATI_TMDS_OUTPUT
RTD2663 HDMI_IN
SC 1226
SC 1216_Eric
Close to U22
External _HDMI_IN_CONN (3)
PCH_TMDS_IN (1)
ATI_TMDS_IN (2)
MXIC only
SB 1209
DELETE!!
I2C_Addr=0 Ctrl Reg :94/95 ,EDID Shadow :96/97
I2C_Addr=1 Ctrl Reg :B4/B5 ,EDID Shadow :B6/B7
High=GPU On Board
Low=UMA
[-1] 0402
[-1] 0317
[-1] 0401
1228 (SC)
Placement Near Riser
For HW TV
For ATV Only
HDMI EDID Debug
Wistron Corporation
Scaler IC
Catalina

Touch Key

TOUCH_INT#
L: Touch any key
H: Normal

BT_RESET_IN# (Mechical Key)
L: RESET_BT
H: Normal

BT_RESET_OUT
L: BT_RESET_IN#
H: BT_RESET

BL_CTL_OFF
Power ON: High (Default)
Touch: Low/High/Low...

LIGH_BAR_ON
LIGH BAR Off : High (Default)
Touch: Low/High/Low...

0126 (1A)

H: Enable
L: Disable

High: Enable
Low: Disable

[-1] 0401

Low: Enable
High: Disable

High: Enable
Low: Disable

Odd: channel A
Even: channel B

+19V_S5_INV Power

INVERTER BOARD CONNECTOR

Internal Speaker x 2

[-1] 0319

SB 1204
SB 1208

SB 1202

SB 1210

SC 1226

LPF for fc(-3dB)=500Hz

The PLIMIT circuit sets a limit on the output peak-to-peak voltage. The limiting is done by limiting the duty cy to fixed maximum value. This limit can be thought of as a "virtual" voltage rail which is lower than the sup connected to PVCC. This "virtual" rail is 4 times the voltage at the PLIMIT pin. This output voltage can be usec calculate the maximum output power for a given maximum input voltage and speaker impedance.

$$P_{OUT} = \frac{\left(\frac{R_L}{R_L + 2 \times R_S} \times V_P\right)^2}{2 \times R_L}$$ for unclipped power

Where:
R_S is the total series resistance including $R_{DS(on)}$, and any resistance in the output filter.
R_L is the load resistance.
V_P is the peak amplitude of the output possible within the supply rail.
$V_P = 4 \times$ PLIMIT voltage if PLIMIT < $4 \times V_P$
P_{OUT} (10%THD) = $1.25 \times P_{OUT}$ (unclipped)

Table 2. PLIMIT Typical Operation

TEST CONDITIONS ()	PLIMIT VOLTAGE	OUTPUT POWER (W)	OUTPUT VOLTAGE AMPLITUDE (V_{P-P})
PVCC=24V, Vin=1Vrms, RL=8Ω, Gain=20dB	1.62	5	14
PVCC=24V, Vin=1Vrms, RL=8Ω, Gain=20dB	1.86	5	14.8
PVCC=12V, Vin=1Vrms, RL=8Ω, Gain=20dB	1.76	5	15

SHUTDOWN	TPA3111D2
L (0V~0.8V)	SHUTDOWN
H (2V ~ VDD)	ACTIVE

GAIN1	GAIN0	GAIN (dB)
0	0	20
1	0	26
0	1	32
1	1	36

<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PANEL OUTPUT & AMP
Size: Custom | Document Number: Catalina | Rev: SA
Date: Tuesday, April 06, 2010 | Sheet 48 of 59

REAR USB

18 USBPN2
18 USBPP2
18 USBPN3
18 USBPP3
18 USBPN4
18 USBPP4
18 USBPN9
18 USBPP9

LAN

27 RJ45_LED0 → RJ45_LED0
27 RJ45_LED1 → RJ45_LED1
27 RJ45_LED2 → RJ45_LED2

27 LAN_MDI0_DN → LAN_MDI0_DN
27 LAN_MDI0_DP → LAN_MDI0_DP
27 LAN_MDI1_DN → LAN_MDI1_DN
27 LAN_MDI1_DP → LAN_MDI1_DP
27 LAN_MDI2_DN → LAN_MDI2_DN
27 LAN_MDI2_DP → LAN_MDI2_DP
27 LAN_MDI3_DN → LAN_MDI3_DN
27 LAN_MDI3_DP → LAN_MDI3_DP

HDMI OUT

HDMI_OUT_TXD2 → HDMI_OUT_TXD2 24
HDMI_OUT_TXD2# → HDMI_OUT_TXD2# 24
HDMI_OUT_TXD1 → HDMI_OUT_TXD1 24
HDMI_OUT_TXD1# → HDMI_OUT_TXD1# 24
HDMI_OUT_TXD0 → HDMI_OUT_TXD0 24
HDMI_OUT_TXD0# → HDMI_OUT_TXD0# 24
HDMI_OUT_TXC → HDMI_OUT_TXC 24
HDMI_OUT_TXC# → HDMI_OUT_TXC# 24
HDMI_OUT_SCL → HDMI_OUT_SCL 24
HDMI_OUT_SDA → HDMI_OUT_SDA 24
HDMI_OUT_HPD → HDMI_OUT_HPD 24

HDMI IN

HDMI_IN_TXD2 → HDMI_IN_TXD2 47
HDMI_IN_TXD2# → HDMI_IN_TXD2# 47
HDMI_IN_TXD1 → HDMI_IN_TXD1 47
HDMI_IN_TXD1# → HDMI_IN_TXD1# 47
HDMI_IN_TXD0 → HDMI_IN_TXD0 47
HDMI_IN_TXD0# → HDMI_IN_TXD0# 47
HDMI_IN_TXC → HDMI_IN_TXC 47
HDMI_IN_TXC# → HDMI_IN_TXC# 47
HDMI_IN_SCL → HDMI_IN_SCL 47
HDMI_IN_SDA → HDMI_IN_SDA 47
HDMI_IN_HPD → HDMI_IN_HPD 47

AV IN

47 AV_CVBS+ → AV_CVBS+
47 AV_CVBS- → AV_CVBS-
47 AV_AUDIO_R → AV_AUDIO_R
47 AV_AUDIO_L → AV_AUDIO_L

19.5V IN

AD_JK — RISER1 — AD_JK

V_3P3_LAN

HDMI_OUT_TXD2 / HDMI_OUT_TXD2# — LAN_MDI3_DN / LAN_MDI3_DP
HDMI_OUT_TXD1 / HDMI_OUT_TXD1# — LAN_MDI2_DN / LAN_MDI2_DP
HDMI_OUT_TXD0 / HDMI_OUT_TXD0# — LAN_MDI1_DN / LAN_MDI1_DP
HDMI_OUT_TXC / HDMI_OUT_TXC# — LAN_MDI0_DN / LAN_MDI0_DP
HDMI_OUT_SCL — RJ45_LED0
HDMI_OUT_SDA — RJ45_LED1
HDMI_OUT_HPD — RJ45_LED2
HDMI_IN_TXD2 / HDMI_IN_TXD2# — SPDIF → SPDIF 30
HDMI_IN_TXD1 / HDMI_IN_TXD1# — USBPP2 / USBPN2 — VCC5_USB
HDMI_IN_TXD0 / HDMI_IN_TXD0# — USBPP3 / USBPN3
HDMI_IN_TXC / HDMI_IN_TXC# — USBPP4 / USBPN4 — VCC5_USB
HDMI_IN_SCL — USBPP9
HDMI_IN_SDA — USBPN9
HDMI_IN_HPD
AV_CVBS- / AV_CVBS+
AV_AUDIO_R → OC*49 18
AV_AUDIO_L — BT_RESET_IN# → OC*23 18
RISER_DET# → RISER_DET# 19

5V_S0 — C463 SCD1U16V2ZY-2GP — GP

5V_S0 — R490 0R0603-PAD — 5V_SPDIF → 5V_SPDIF

HDMI_5V

SWAP

MLX-CONN98-4R1 GP

SB 1210

(R) R356 0R0402-PAD

EC5 — (R) SCD1U16V2ZY-2GP

AVIN_AGND

AVIN_AGND

U51 (R) RCLAMP0524P-GP

HDMI_IN_TXC# / HDMI_IN_TXC
HDMI_IN_TXD0# / HDMI_IN_TXD0
L1#1L1#8 / L2#2L2#7 / GNDGND / L3#3L3#6 / L4#4L4#5
G1 G2

U53 (R) RCLAMP0524P-GP

HDMI_IN_TXD1# / HDMI_IN_TXD1
HDMI_IN_TXD2# / HDMI_IN_TXD2
L1#1L1#8 / L2#2L2#7 / GNDGND / L3#3L3#6 / L4#4L4#5
G1 G2

BT_POWER

C525 SCD1U16V2ZY-2GP (R)

U32 SNAHC1G14DBVR-GP (R)
NC#1 VCC A GND Y
BT_RESET_OUT → BT_RESET_OUT 26

R551 4K7R2J-2-GP

R1045 (R) 22R2J-2-GP

BT_RESET_IN#

R1044 0R0402-PAD C533 SCD1U10V2KX-5GP (R)

R89 4K7R2J-2-GP

Q85 PMBS3906-GP

R1042 1K5R2F-2-GP

R1043 100R2J-2-GP

R545 10KR2J-3-GP

C976 SCD1U10V2KX-5GP

0126 (1A)

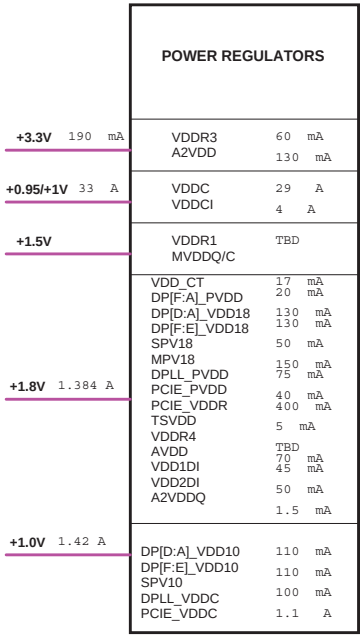
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Riser slot

Size	Document Number	Rev
C	Catalina	SA

Date: Tuesday, April 06, 2010 Sheet 49 of 59



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI_Power rail

Size: C | Document Number: Catalina | Rev: SA

Date: Tuesday, April 06, 2010 | Sheet 50 of 59

PCI_E x16

4 PEG_TXP[15..0]
PEG_TXP0 PEG_TXP1 PEG_TXP2 PEG_TXP3 PEG_TXP4 PEG_TXP5 PEG_TXP6 PEG_TXP7 PEG_TXP8 PEG_TXP9 PEG_TXP10 PEG_TXP11 PEG_TXP12 PEG_TXP13 PEG_TXP14 PEG_TXP15

4 PEG_TXN[15..0]
PEG_TXN0 PEG_TXN1 PEG_TXN2 PEG_TXN3 PEG_TXN4 PEG_TXN5 PEG_TXN6 PEG_TXN7 PEG_TXN8 PEG_TXN9 PEG_TXN10 PEG_TXN11 PEG_TXN12 PEG_TXN13 PEG_TXN14 PEG_TXN15

4 PEG_RXP[15..0]
PEG_RXP0 PEG_RXP1 PEG_RXP2 PEG_RXP3 PEG_RXP4 PEG_RXP5 PEG_RXP6 PEG_RXP7 PEG_RXP8 PEG_RXP9 PEG_RXP10 PEG_RXP11 PEG_RXP12 PEG_RXP13 PEG_RXP14 PEG_RXP15

4 PEG_RXN[15..0]
PEG_RXN0 PEG_RXN1 PEG_RXN2 PEG_RXN3 PEG_RXN4 PEG_RXN5 PEG_RXN6 PEG_RXN7 PEG_RXN8 PEG_RXN9 PEG_RXN10 PEG_RXN11 PEG_RXN12 PEG_RXN13 PEG_RXN14 PEG_RXN15

15 CLK_PCIE_PEG#
15 CLK_PCIE_PEG
CLK_PCIE_PEG#
CLK_PCIE_PEG

52 ATI_RST#
ATI_RST#

U21A 1 OF 8

PCI EXPRESS INTERFACE

PEG_TXP0	AA38	PCIE_RX0P	PCIE_TX0P	Y33	PEG_T_TXP0	DIS	1	C699	SCD1U10V2KX-4GP	PEG_RXP0
PEG_TXN0	Y37	PCIE_RX0N	PCIE_TX0N	Y32	PEG_T_TXN0	DIS	1	C700	SCD1U10V2KX-4GP	PEG_RXN0
PEG_TXP1	Y35	PCIE_RX1P	PCIE_TX1P	W33	PEG_T_TXP1	DIS	1	C673	SCD1U10V2KX-4GP	PEG_RXP1
PEG_TXN1	W36	PCIE_RX1N	PCIE_TX1N	W32	PEG_T_TXN1	DIS	1	C674	SCD1U10V2KX-4GP	PEG_RXN1
PEG_TXP2	W38	PCIE_RX2P	PCIE_TX2P	U33	PEG_T_TXP2	DIS	1	C687	SCD1U10V2KX-4GP	PEG_RXP2
PEG_TXN2	V37	PCIE_RX2N	PCIE_TX2N	U32	PEG_T_TXN2	DIS	1	C688	SCD1U10V2KX-4GP	PEG_RXN2
PEG_TXP3	V35	PCIE_RX3P	PCIE_TX3P	U30	PEG_T_TXP3	DIS	1	C675	SCD1U10V2KX-4GP	PEG_RXP3
PEG_TXN3	U36	PCIE_RX3N	PCIE_TX3N	U29	PEG_T_TXN3	DIS	1	C676	SCD1U10V2KX-4GP	PEG_RXN3
PEG_TXP4	U38	PCIE_RX4P	PCIE_TX4P	T33	PEG_T_TXP4	DIS	1	C689	SCD1U10V2KX-4GP	PEG_RXP4
PEG_TXN4	T37	PCIE_RX4N	PCIE_TX4N	T32	PEG_T_TXN4	DIS	1	C690	SCD1U10V2KX-4GP	PEG_RXN4
PEG_TXP5	T35	PCIE_RX5P	PCIE_TX5P	T30	PEG_T_TXP5	DIS	1	C677	SCD1U10V2KX-4GP	PEG_RXP5
PEG_TXN5	R36	PCIE_RX5N	PCIE_TX5N	T29	PEG_T_TXN5	DIS	1	C678	SCD1U10V2KX-4GP	PEG_RXN5
PEG_TXP6	R38	PCIE_RX6P	PCIE_TX6P	P33	PEG_T_TXP6	DIS	1	C691	SCD1U10V2KX-4GP	PEG_RXP6
PEG_TXN6	P37	PCIE_RX6N	PCIE_TX6N	P32	PEG_T_TXN6	DIS	1	C694	SCD1U10V2KX-4GP	PEG_RXN6
PEG_TXP7	P35	PCIE_RX7P	PCIE_TX7P	P30	PEG_T_TXP7	DIS	1	C679	SCD1U10V2KX-4GP	PEG_RXP7
PEG_TXN7	N36	PCIE_RX7N	PCIE_TX7N	P29	PEG_T_TXN7	DIS	1	C680	SCD1U10V2KX-4GP	PEG_RXN7
PEG_TXP8	N38	PCIE_RX8P	PCIE_TX8P	N33	PEG_T_TXP8	DIS	1	C695	SCD1U10V2KX-4GP	PEG_RXP8
PEG_TXN8	M37	PCIE_RX8N	PCIE_TX8N	N32	PEG_T_TXN8	DIS	1	C692	SCD1U10V2KX-4GP	PEG_RXN8
PEG_TXP9	M35	PCIE_RX9P	PCIE_TX9P	N30	PEG_T_TXP9	DIS	1	C681	SCD1U10V2KX-4GP	PEG_RXP9
PEG_TXN9	L36	PCIE_RX9N	PCIE_TX9N	N29	PEG_T_TXN9	DIS	1	C682	SCD1U10V2KX-4GP	PEG_RXN9
PEG_TXP10	L38	PCIE_RX10P	PCIE_TX10P	L33	PEG_T_TXP10	DIS	1	C693	SCD1U10V2KX-4GP	PEG_RXP10
PEG_TXN10	K37	PCIE_RX10N	PCIE_TX10N	L32	PEG_T_TXN10	DIS	1	C696	SCD1U10V2KX-4GP	PEG_RXN10
PEG_TXP11	K35	PCIE_RX11P	PCIE_TX11P	L30	PEG_T_TXP11	DIS	1	C683	SCD1U10V2KX-4GP	PEG_RXP11
PEG_TXN11	J36	PCIE_RX11N	PCIE_TX11N	L29	PEG_T_TXN11	DIS	1	C684	SCD1U10V2KX-4GP	PEG_RXN11
PEG_TXP12	J38	PCIE_RX12P	PCIE_TX12P	K33	PEG_T_TXP12	DIS	1	C697	SCD1U10V2KX-4GP	PEG_RXP12
PEG_TXN12	H37	PCIE_RX12N	PCIE_TX12N	K32	PEG_T_TXN12	DIS	1	C698	SCD1U10V2KX-4GP	PEG_RXN12
PEG_TXP13	H35	PCIE_RX13P	PCIE_TX13P	J33	PEG_T_TXP13	DIS	1	C669	SCD1U10V2KX-4GP	PEG_RXP13
PEG_TXN13	G36	PCIE_RX13N	PCIE_TX13N	J32	PEG_T_TXN13	DIS	1	C670	SCD1U10V2KX-4GP	PEG_RXN13
PEG_TXP14	G38	PCIE_RX14P	PCIE_TX14P	K30	PEG_T_TXP14	DIS	1	C685	SCD1U10V2KX-4GP	PEG_RXP14
PEG_TXN14	F37	PCIE_RX14N	PCIE_TX14N	K29	PEG_T_TXN14	DIS	1	C686	SCD1U10V2KX-4GP	PEG_RXN14
PEG_TXP15	F35	PCIE_RX15P	PCIE_TX15P	H33	PEG_T_TXP15	DIS	1	C672	SCD1U10V2KX-4GP	PEG_RXP15
PEG_TXN15	E37	PCIE_RX15N	PCIE_TX15N	H32	PEG_T_TXN15	DIS	1	C671	SCD1U10V2KX-4GP	PEG_RXN15

CLOCK

CLK_PCIE_PEG	AB35	PCIE_REFCLKP	
CLK_PCIE_PEG#	AA36	PCIE_REFCLKN	
	AJ21	NC#AJ21	
	AK21	NC#AK21	
PWRGOOD_ATI	AH16	PWRGOOD	
PLT_RST1# M92 1	AA30	PERST#	

CALIBRATION

		PCIE_CALRP	Y30	1 R790	1K27R2F-L-GP
		PCIE_CALRN	Y29	1 R792	2KR2F-3-GP

1.0V_REG

SB 1202

R821 10KR2J-3-GP

ATI_RST# 1 R353 2 0R0402-PAD PLT_RST1# M92 1

C325 SC47P50V2JN-3GP

MADISON-PRO-GP

(M71.MDSON.M03, P71.0PARK.M05)

33,52 PLT_RST_ATI# PLT_RST_ATI# 1 R344 2 ATI_RST# 0R0402-PAD

[-1] 0401

<Core Design>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	ATI_Mad_PCIE
Size C	Document Number: Catalina — Rev: SA
Date: Tuesday, April 06, 2010	Sheet 51 of 59

HSYNC/VSYNC are transmitted on TX0P/M_DP[A, C]2P/N,
TX3P/M_DP[B, D]2P/N, TXOUT_L0P/N_DPE2P/N,
or TXOUT_U0P/N_DPF2P/N (Blue) channel during blank

MxM HDMI OUT

NV_HDMI_CLK+ 24
NV_HDMI_CLK- 24
NV_HDMI_DATA0+ 24
NV_HDMI_DATA0- 24
NV_HDMI_DATA1+ 24
NV_HDMI_DATA1- 24
NV_HDMI_DATA2+ 24
NV_HDMI_DATA2- 24
NV_HDMI_CLK
NV_HDMI_DATA
NV_HDMI_CLK 24
NV_HDMI_DATA 24
NV_HDMI_DETECT
NV_HDMI_DETECT 24

MxM VGA OUT

MXM_RED — MXM_RED 23
MXM_GREEN — MXM_GREEN 23
MXM_BLUE — MXM_BLUE 23
MXM_DDCCLK — MXM_DDCCLK 23
MXM_DDCDATA — MXM_DDCDATA 23
MXM_HSYNC — MXM_HSYNC 23,58
MXM_VSYNC — MXM_VSYNC 23,58

GPIOS

58 GPIO6
58 GPIO1
GPIO2
58 GPU_SMBDAT
58 GPU_SMBCLK
58 GPIO5
58 GPIO8
58 GPIO9
58 GPIO11
58 GPIO12
58 GPIO13
58 GPIO22
58 GENERICC
42 AMD_GPIO15 — AMD_GPIO15
42 AMD_GPIO20 — AMD_GPIO20
15 PEX_CLKREQ — PEX_CLKREQ

OTHERS

H2SYNC 58
V2SYNC 58

DVPDATA [3:0]
Hynix-H5TQ1G63BFR-12C (800MHz)
Samsung-K4W1G1646E-HC12 (800MHz)

09/09/28
Must be tied high if not used.

Layout notice:
It should be place near HDMI connector

HDMI

TMDS to Scalar

VGA

SB 1202
09/09/28
A 3-K external pull-up (3.3 V) is required if an external BIOS ROM chip is used.

SERIAL EEPROM 512K/1M
A 256MB MEMORY APERTURE SIZE
CAN BE DEFINED USING A SEPARATE ROM OR STRAPPING

09/09/28
delete
do not need LVDS

PLACE VREFG DIVIDER AND CAP CLOSE TO ASIC

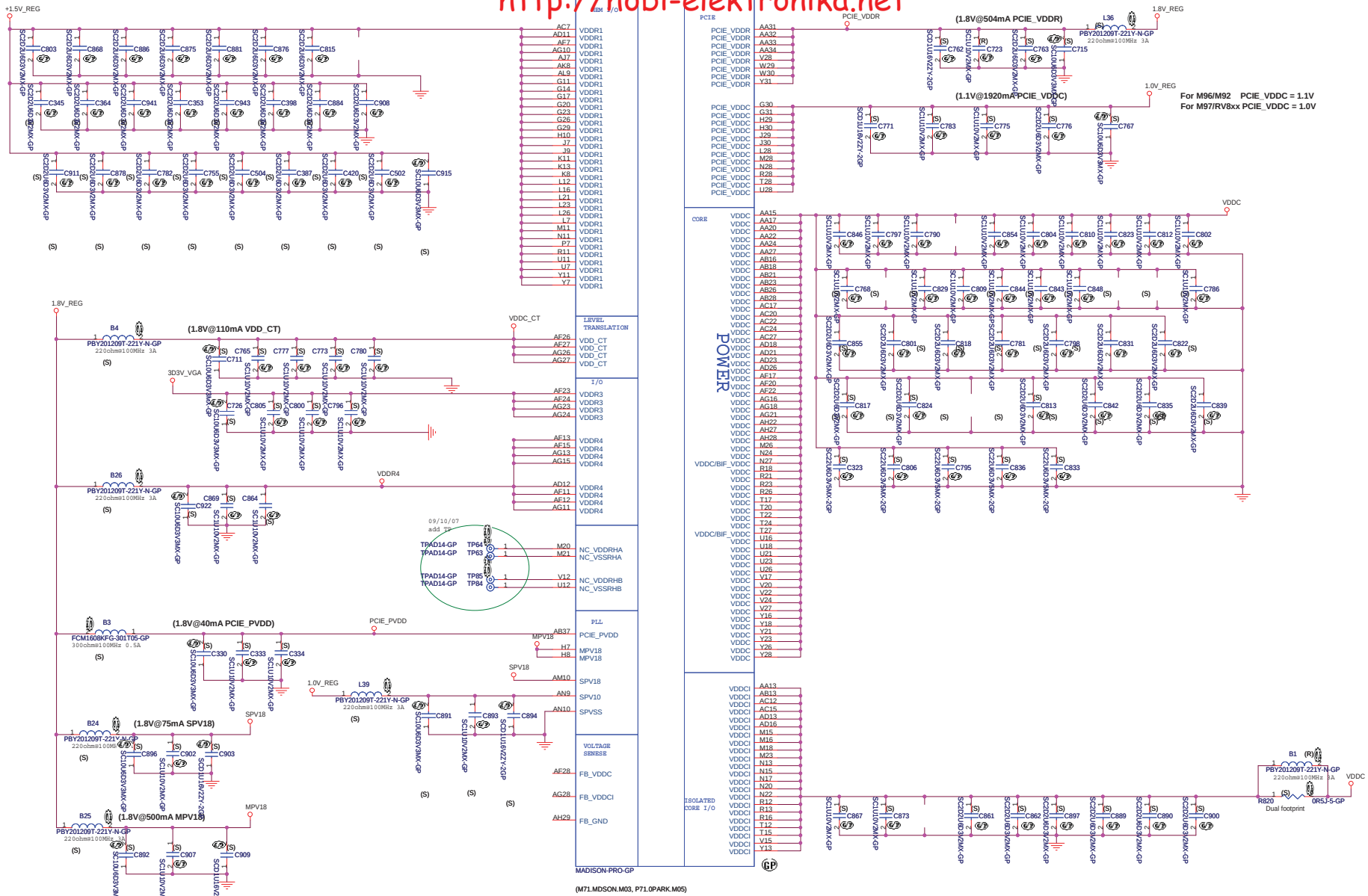
0126 (1A)

(1.8V@150mA DPLL_PVDD)
(1.1V@300mA DPLL_VDDC)
(1.8V@15mA TSVDD)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI Mad IO
Size: D
Document Number: Catalina
Rev: SA
Date: Tuesday, April 06, 2010
Sheet 52 of 59



BACO
needed??

<Core Design>

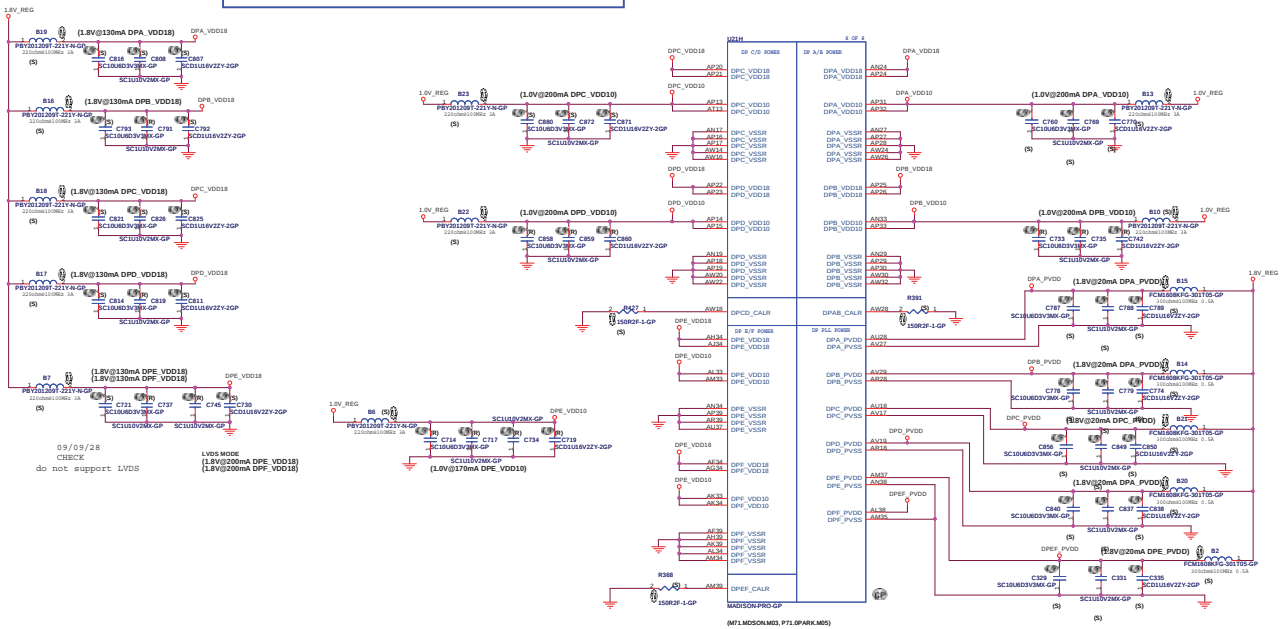
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

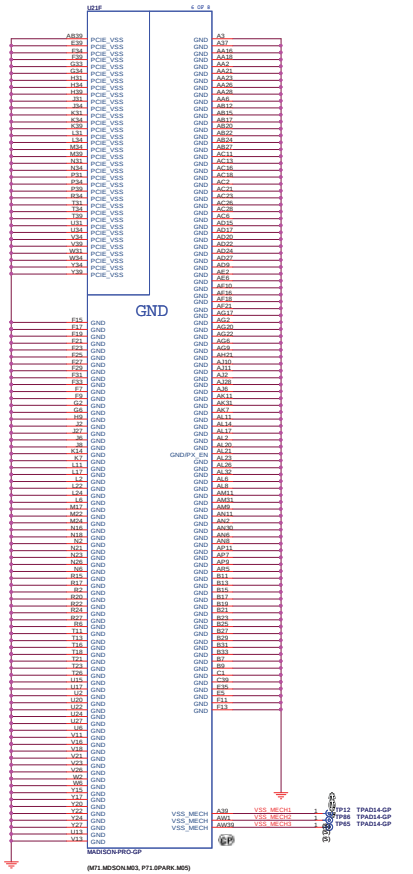
Title: ATI_Mad_POWER

Size	Document Number	Rev
C	Catalina	SA

Date: Tuesday, April 06, 2010 Sheet 53 of 59

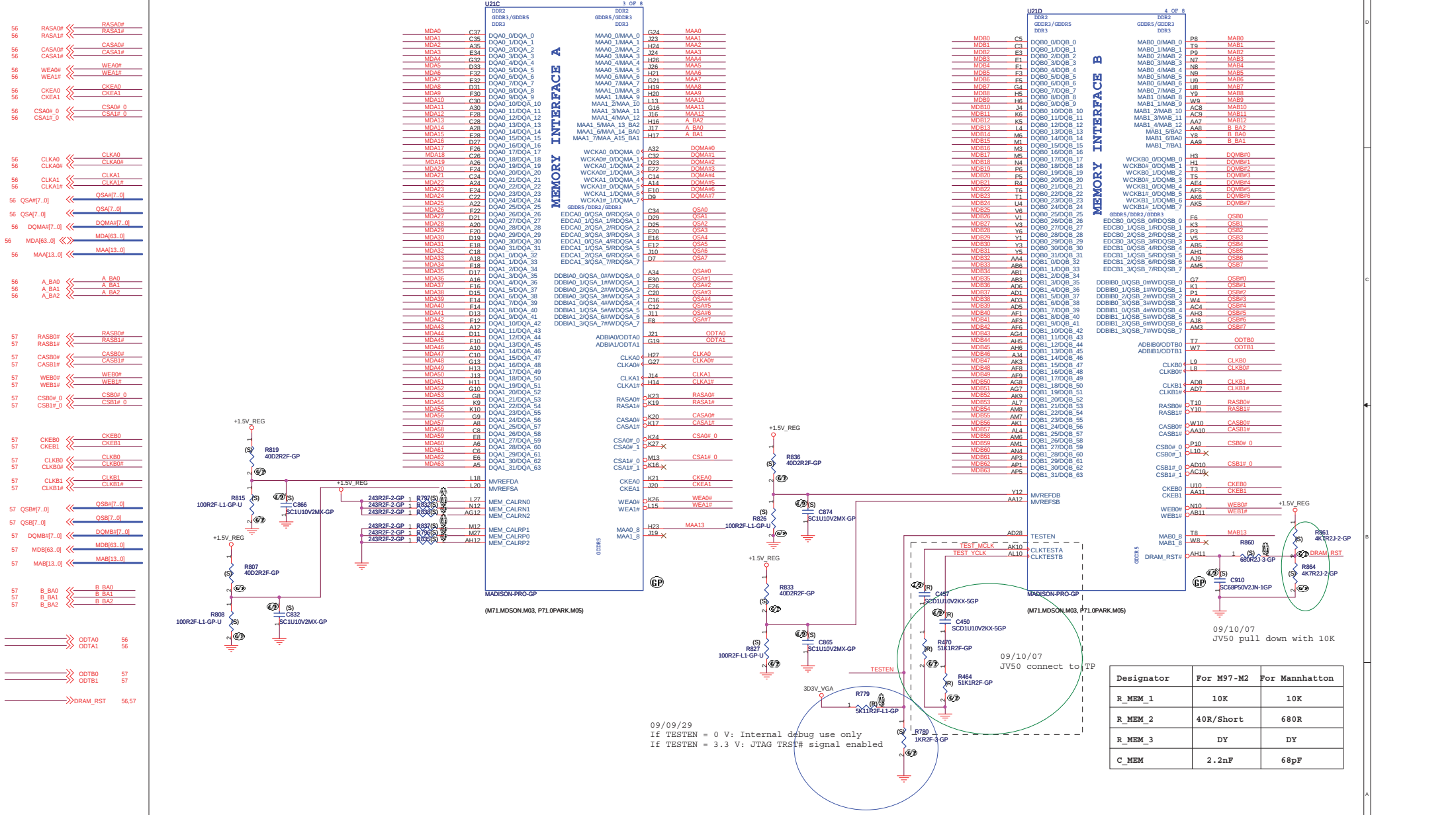
09/09/28
For dual-link TMDS, the associated power supply rails can
share the filters/decoupling capacitors.
We use single HDMI, share or ?
need check!





<Core Design>

蜂創資通	Wistron Corporation	
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	ATI DP POWER	
Size: D	Document Number: Catalina	Rev: SA
Date: Tuesday, April 06, 2010	Sheet 54 of 59	



Designator	For M97-M2	For Mannhatton
R_MEM_1	10K	10K
R_MEM_2	40R/Short	680R
R_MEM_3	DY	DY
C_MEM	2.2nF	68pF

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

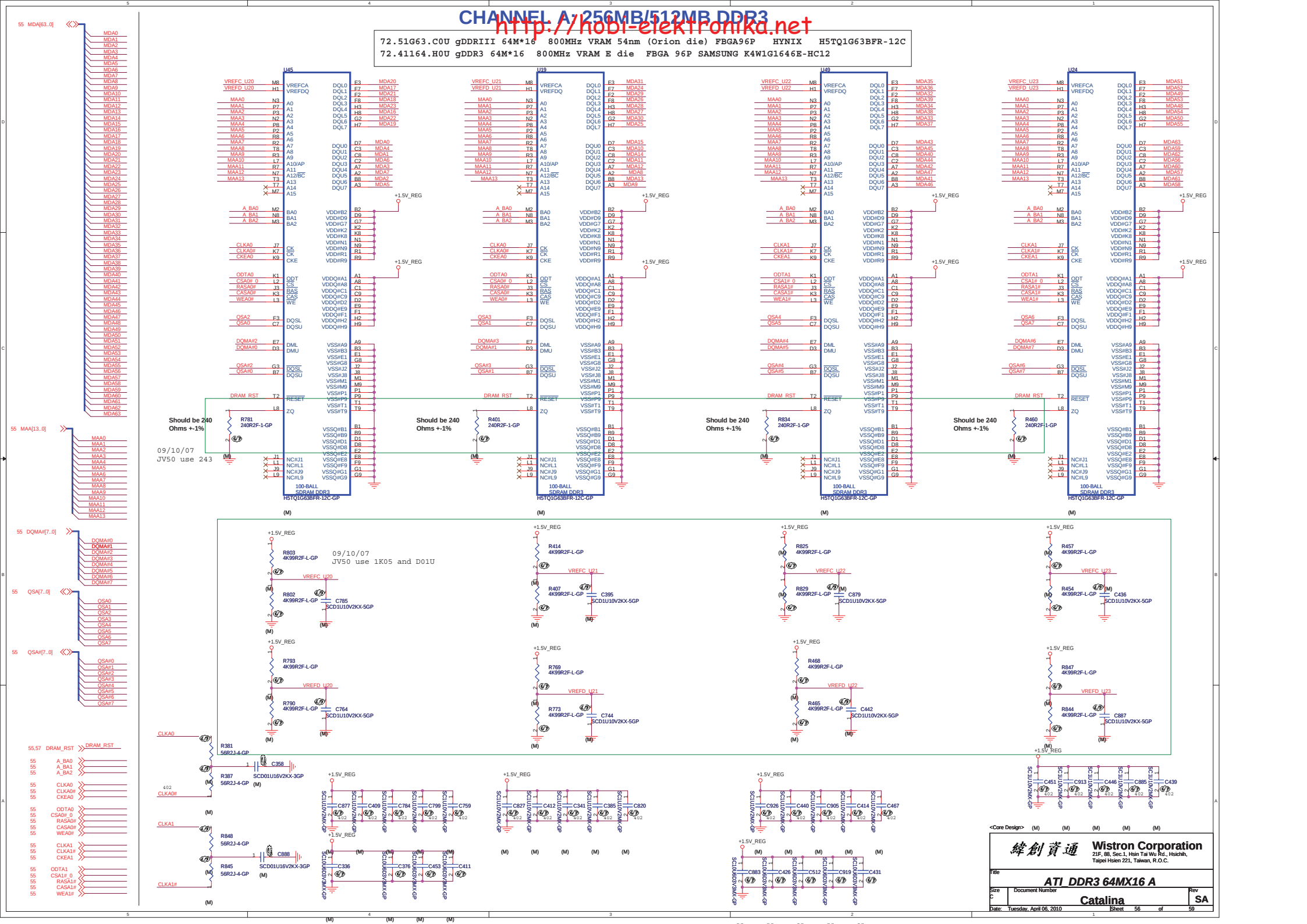
Title: ATI_Mad_MEMORY

Size: C | Document Number: Catalina | Rev: SA

Date: Tuesday, April 06, 2010 | Sheet 55 of 59

CHANNEL A: 256MB/512MB DDR3

72.51G63.C0U gDDRIII 64M*16 800MHz VRAM 54nm (Orion die) FBGA96P HYNIX H5TQ1G63BFR-12C
72.41164.H0U gDDR3 64M*16 800MHz VRAM E die FBGA 96P SAMSUNG K4W1G1646E-HC12



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

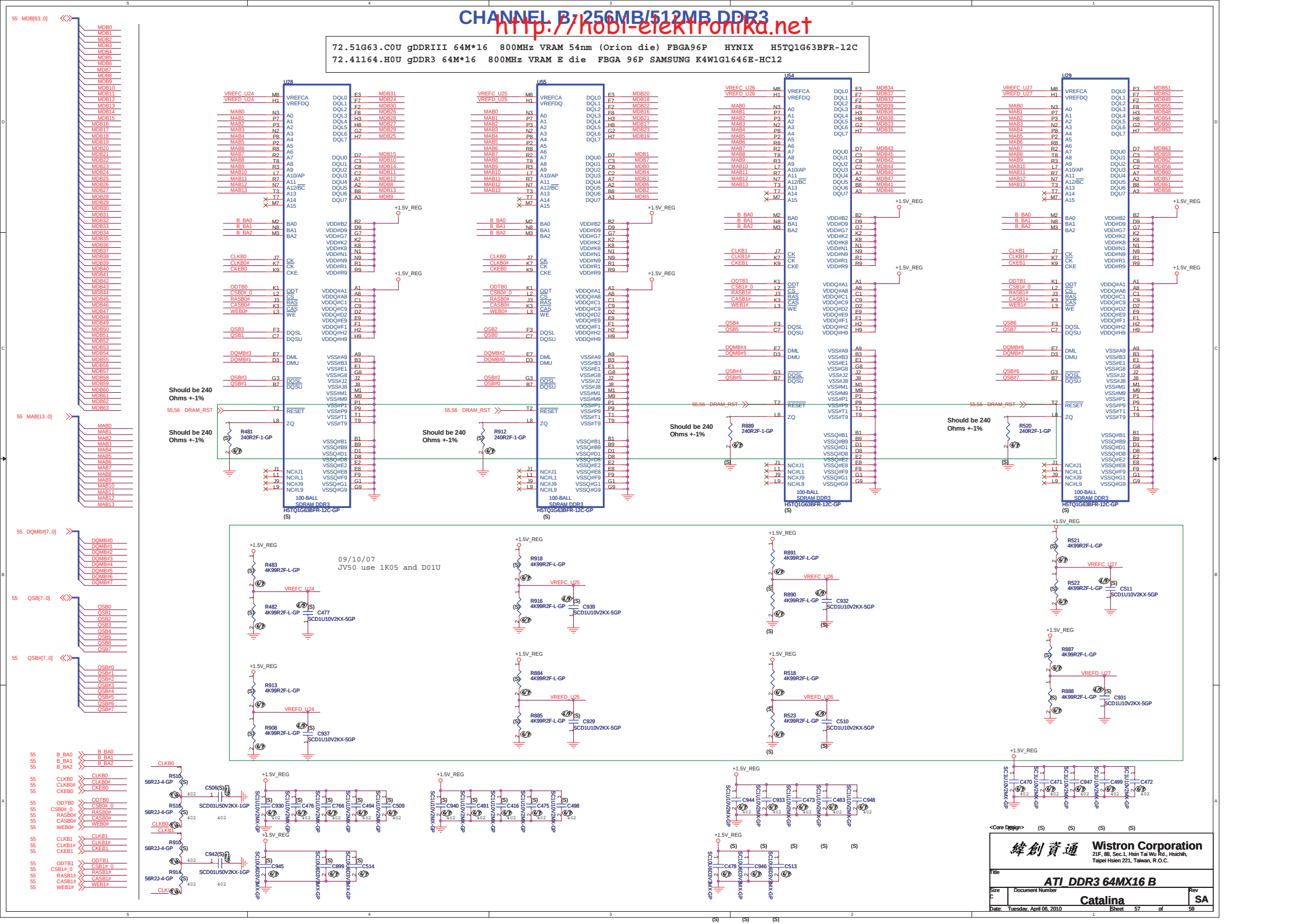
Title: ATI_DDR3 64MX16 A

Size: C | Document Number: Catalina | Rev: SA

Date: Tuesday, April 06, 2010 | Sheet 56 of 59

CHANNEL B: 256MB/512MB DDR3

72.51G63.C0U gDDRIII 64M*16 800MHz VRAM 54nm (Orion die) FBGA96P HYNIX H5TQ1G63BFR-12C
72.41164.H0U gDDR3 64M*16 800MHz VRAM E die FBGA 96P SAMSUNG K4W1G1646E-HC12



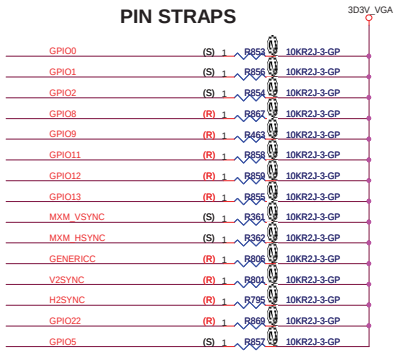
52 GPIO0
52 GPIO1
52 GPIO2
52 GPIO8
52 GPIO9
52 GPIO11
52 GPIO12
52 GPIO13
23,52 MXM_VSYNC
23,52 MXM_HSYNC
52 GENERICC
52 V2SYNC
52 H2SYNC
52 GPIO22
52 GPIO5

13,15,29 PCH_SMBCLK
13,15,29 PCH_SMBDATA

19,42,43 DGPU_PWROK

52 GPU_SMBCLK
52 GPU_SMBDAT

PIN STRAPS



	Manufacturer	Part Number	Size	CONFIG[2:0]
STRAP	ST Microelectronics	M25P05A	512 kbit	100

		HSYNC VSYNC
STRAP	Audio for both DisplayPort and HDMI.	11
	Audio for DisplayPort and HDMI if dongle is detected	10

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	1
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED	1
BIF_CLK_PM_EN	GPIO8	BIF_CLK_PM_EN	0
BIF_VGA DIS	GPIO9	VGA ENABLED	0
BIF_RX_PLL_CALIB_BP	GPIO21	BIF_RX_PLL_CALIB_BP	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	1
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	1 0 0
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
SMS_EN_HARD	H2SYNC		0
CCBYPASS	GENERICC		0
AUD[1]	HSYNC	built-in HDMI connector	1
AUD[0]	VSYNC	Audio functiuon present	1

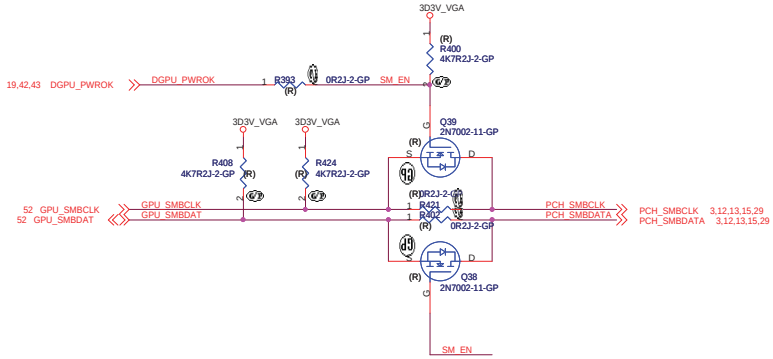
AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO_28_TDO GPIO21_BB_EN



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI_THERM & STRAPS

Size: C | Document Number: Catalina | Rev: SA

Date: Tuesday, April 06, 2010 | Sheet 58 of 59

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserve

Size	Document Number	Rev
C	Catalina	SA

Date: Tuesday, April 06, 2010 Sheet 59 of 59