GM/PM45 Block Diagram

Project code:
PCB P/N : 08124
REVISION : -1 2008/12/18

Database: XX.XXXXX.XXX
Database PCB:
Revision:

PCB STACKUP 8L

TOP	
GND/PWR	
L3-signal	
PWR	
GND/PWR	
L6-signal	
GND	
BOTTOM	

SYSTEM DC/DC TPS51120 43	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5

SYSTEM DC/DC TPS51124 44	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 1D05V_S0

CLK GEN.
ICS 9LPRS365 3

INTEL Mobile CPU
Penryn
Penryn SV Processor
FSB:800 or 1066 MHz
4, 5, 6, 7

HOST BUS 800/1066MHz

DDRIII Slot1 15,16 — 800/1066MHz
DDRIII Slot2 15,16 — 800/1066MHz

Cantiga
AGTL+ CPU I/F
DDR Memory I/F
INTEGRATED GRAHPICS
LVDS, CRT I/F
71.CNTIG.00U
8,9,10,11,12,13,14

PCIex16 — MXM card NV 50 — LVDS — LCD Panel 20
LVDS — LCD Panel 20

DMI 400MHz

ICH9M
6 PCIe ports
PCI/PCI BRIDGE
ACPI 1.1
4 SATA
High Definition Audio
LPC I/F
Serial Peripheral I/F
71.ICH9M.00U
22,23,24,25

Touch Switch 37

PCIex1:
- LAN GIGA Lan BCM5784M 33 — Riser — RJ45 34
- Jmicron JMB380 1394/Card reader 29 — 1394 30
- Jmicron JMB380 1394/Card reader 29 — 4 in 1 card reader 30 — Antenna in
- Mini PCI-E Card 31 — USB 1port — TV tuner card
- Mini PCI-E Card 32 — USB 1port — WLAN Card — Antenna

AZALIA — Codec ALC272 35
- MIC In
- SPDIF Head Phone

OP AMP TPA3007D1 36 — INT.WOOFER
OP AMP TPA3121 36 — INT.SPKR

USB:
- USB Header 1port 27 — Web Cam+ Mic Array 28
- USB Header 1port 27 — Blue Tooth Module 28 — Antenna
- Riser Rear — USB 2 Port 34 — USB 2 Port 34
- Side — USB 1Port x2 27

SPI I/F — BIOS W25X160-VSS 40

SATA — HDD 28
SATA — ODD 28
LPC BUS — SIO SMSC SCH-5147 38
- CPU Fan 26
- SYS Fan 26
- PS/2 KB/MS 26 — Optional

CPU DC/DC ADP3208A 46	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

LT72

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Title: *Block Diagram*
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ICH9M

PIN NAME	POWER WELL	USAGE	AFTER PLTRST	Notes	P/H&P/D	Default value
GPIO0	MAIN	PM_BMBUSY#	GPI			High
GPIO1	MAIN	LPC_SMI*	GPI	Input:LPC SMI Event Input(Low active) Open Drain		High
GPIO2	MAIN	IRQE#	GPI			High
GPIO3	MAIN	IRQF#	GPI			High
GPIO4	MAIN	IRQG#	GPI			High
GPIO5	MAIN	IRQH#	GPI			High
GPIO6	MAIN	Touch_INT_SB	GPI	H: Normal, L:Enable		High
GPIO7	MAIN	CDR_REFECT_SB	GPI	H: Normal, L:Enable CDR_REFECT_TOUCH		High
GPIO8	RESUME		GPO			High
GPIO9	RESUME	NO	Native(WOL_EN)	check		High
GPIO10	RESUME	NO	GPI			High
GPIO11	RESUME	OCP#	Native(SMBALERT#)			High
GPIO12	RESUME	NO	GPO			Low
GPIO13	RESUME	NO	GPI			High
GPIO14	RESUME	NO	GPI			High
GPIO15						
GPIO16	MAIN	DPRSLPVR	Native(DPRSLPVR)	H: Enable Internal PD 20K		Low
GPIO17	MAIN		GPI	GPO		High
GPIO18	MAIN		GPO	H: Enable		High
GPIO19	MAIN	Wireless LAN_EN	GPO			High
GPIO20	MAIN		GPO	Internal PD 20K (Can't PU)		High
GPIO21	MAIN	TV_EN	GPO			High
GPIO22	MAIN		OD			High
GPIO23	MAIN	NO	Native(LDRQ1#)	Internal PD 20K		High
GPIO24	RESUME		GPI			Low
GPIO25						
GPIO26	RESUME					Low
GPIO27	RESUME		GPO			Low
GPIO28	RESUME		GPO			Low
GPIO29	RESUME	OC*45	Native(OC5#)			High
GPIO30	RESUME	OC*6	Native(OC6#)			High
GPIO31	RESUME	OC*7	Native(OC7#)			High
GPIO32						
GPIO33	HDA_DOCK_EN#		GPO	Internal PU 20K		High
GPIO34	MAIN	NO	GPO			Low
GPIO35	MAIN		GPO			Low
GPIO36	MAIN	MXM_DET	GPI	H: no MXM, L: MXM on		High
GPIO37	MAIN	USB_CAM_EN	GPO	CAMERA_EN L: Enable		High
GPIO38	MAIN	PCB_VER0	OD			High
GPIO39	MAIN	PCB_VER1	OD			High
GPIO40	RESUME	OC*01	Native(OC1#)			High
GPIO41	RESUME	OC*23	Native(OC2#)			High
GPIO42	RESUME	OC*23	Native(OC3#)			High
GPIO43	RESUME	OC*45	Native(OC4#)			High
GPIO44	RESUME	OC*8	Native(OC8#)			High
GPIO45	RESUME	OC*9	Native(OC9#)			High
GPIO46	RESUME	OC*10	Native(OC10#)			High
GPIO47	RESUME	OC*11	Native(OC11#)			High
GPIO48	MAIN	PCB_VER2	GPI			High
GPIO49	MAIN	SB_INVERTER_EN#	GPO	L: Teenah/ NC: Catiga chipset Internal PU 20K		High
GPIO50	MAIN	(REQ1#)	Native(REQ1#)			High
GPIO51	MAIN	NO (GNT1#)	Native(GNT1#)	Internal PU 20K		High
GPIO52	MAIN	(REQ2#)	Native(REQ2#)			High
GPIO53	MAIN	NO (GNT2#)	Native(GNT2#)	Internal PU 20K		High
GPIO54	MAIN	(REQ3#)	Native(REQ3#)			High
GPIO55	MAIN	NO (GNT3#)	Native(GNT3#)	Internal PU 20K		High
GPIO56	RESUME	NO	GPI			Low
GPIO57	RESUME	CMOS_IN	GPI		-1A add	High
GPIO58	RESUME	NO	GPI	Internal PU 20K		High
GPIO59	RESUME	OC*01	Native(OC0#)			High
GPIO60	RESUME	NO	Native(LINKALERT#)			Low
GPIO61						
GPIO62						
GPIO63						

SCH 5147

GPIO #	Usage	Notes	IN POWER	OUT POWER	VCC POR	VTR POR
GP10	BAT_INH_MXM	BAT_INH H: AC , L:BAT no use MXM 05/06	N/A	MAIN (VCC)		
GP11	PLTRST#		N/A	AUX (VTR)		
GP12	PLTRST#		N/A	AUX (VTR)		
GP13	PLTRST#		N/A	AUX (VTR)		
GP14	PLTRST#		N/A	AUX (VTR)		
GP15	Thermal Trip		N/A	MAIN (VCC)	OUT.OD	OUT.OD.High
GP16			N/A	AUX (VTR)		OUT.OD.High
GP17		LAN_EN	N/A	AUX (VTR)		OUT.OD.High
GP20			AUX (VTR)	MAIN (VCC)		In
GP21	KB		AUX (VTR)	MAIN (VCC)		
GP22	KB		AUX (VTR)	MAIN (VCC)		
GP27			AUX (VTR)	AUX (VTR)		In
GP32	MS		AUX (VTR)	MAIN (VCC)		
GP33	MS		AUX (VTR)	MAIN (VCC)		
GP36			AUX (VTR)	MAIN (VCC)		In
GP37			AUX (VTR)	MAIN (VCC)		In
GP40			AUX (VTR)	AUX (VTR)		
GP41			AUX (VTR)	AUX (VTR)		
GP42			AUX (VTR)	AUX (VTR)		In
GP43			AUX (VTR)	MAIN (VCC)		In
GP50			AUX (VTR)	AUX (VTR)		In
GP51			AUX (VTR)	AUX (VTR)		In
GP52	Dual Core/Qual Core		AUX (VTR)	AUX (VTR)		In
GP53			AUX (VTR)	AUX (VTR)		In
GP54			AUX (VTR)	AUX (VTR)		In
GP55			AUX (VTR)	AUX (VTR)		In
GP56			AUX (VTR)	AUX (VTR)		In
GP57			AUX (VTR)	AUX (VTR)		In
GP60		SUBWOOFER_CTL	AUX (VTR)	AUX (VTR)		OUT.OD.Low
GP61			AUX (VTR)	AUX (VTR)		OUT.OD.Low

ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01:SPI, 10:PCI, 11:LPC
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister.

PCI Routing

page 17

	IDSEL	INT	REQ	GNT
no	no	G:CARDBUS B:1394 F:Flash Media D:SD Host	0	0

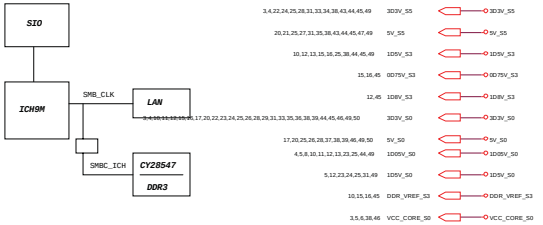
PCIE Routing

LANE1	Lan
LANE2	JMICRON380
LANE3	MiniCard TV
LANE4	MiniCard WLAN

USB Table

USB Pair	Device
0	USB0
1	USB1
2	USB2
3	USB3
4	USB4
5	USB5
6	WIRELESS
7	BT
8	CAMERA
9	miniPCI-E
10	miniPCI-E
11	

SMBus



Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) 1=**The iTPM Host Interface is disalbed(default)**
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality (default)**
CFG9	PCIE Graphics Lane	**0 = Reverse Lanes,15->0,14->1 ect..** 1= Normal operation(Default):Lane Numbered in order
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1= Disabled (default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) **11 = Disabled (default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation(Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port** 1 = PCIE is operational (Default) Note: PCIE is operational and the device operting simultaneously via the PEG port
SDVO_CTRLDATA	SDVO Present	**0 =No SDVO Card Present (Default)** 1 = SDVO Card Present
check L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG/12/CFG13 straps can be enabled at any time.

ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 355845 Rev.2.2 page 99

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 10K
DPRSLPVR/GPIO16	PULL-DOWN 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

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Title: Table of Content

Size	Document Number	Rev
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SRC0,SRC2

SRC1,SRC4

27select: Pin24,25
1: 27M
0:SRC
27select: Pin20,21
1: SRC
0:96M
SRC/ITP select: Pin53,54
0:SRC
1:ITP
0: allow overclocking
1: not allow overclocking

** FS*: internal PL

CK_PWRGD: 3.3V LVTTL input pin that is a level sensitive strobe used to latch the FSLA, FSLB, FSLC,SRC-5_EN, ITP_EN,TME or iAMT entry/exit.

For wireless performance

Solder Thermal Pad to GND add min 4 vias

ICS9LPRS365BKLFT-GP-U

Frequency Table

FS_C	FS_B	FS_A	CPU	SRC	PCI	DOT	REF	USB
Bit2	Bit1	Bit0	(MHz)	(MHz)	(MHz)	(MHz)	(MHz)	(MHz)
0	0	0	266.66	100.00	33.33	96.00	14.318	48.00
0	0	1	133.33	100.00	33.33	96.00	14.318	48.00
0	1	0	200.00	100.00	33.33	96.00	14.318	48.00
0	1	1	166.66	100.00	33.33	96.00	14.318	48.00
1	0	0	333.33	100.00	33.33	96.00	14.318	48.00
1	0	1	100.00	100.00	33.33	96.00	14.318	48.00
1	1	0	400.00	100.00	33.33	96.00	14.318	48.00
1	1	1	200.00	100.00	33.33	96.00	14.318	48.00

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Title: Clock generator ICS-9LPRS365

Size: Custom | Document Number: Bali | Rev: -1

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SB 8/6 Layout Lib
62.10079.001=>
(Old) BGA479-SKT-9-U1H199
(New) BGA479-SKT-9-U2H203

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

Quad Core Option

8/18 SB Modify

-1 CPU socket change to 62.10053.571

QuadCore

Layout Note:
Route H_THERMDA and H_THERMDC on same layer w/ 10 mil trace & 10 mil spacing. Route away from noise sources with ground guard tracks on each side.

Layout note: Z0=50 ohm, 0.5" max for GTLREF

Layout note:
Comp0,2 connect with Zo=27.4ohm, make trace length shorter than 0.5".
Comp1,3 connect with Zo=55ohm, make trace length shorter than 0.5".

XDP FOR QUAD CORE CPU

Need check!!

R462: Use 1.91K in Topology2, 1.74K for Topology1.

CPU	F8
DC	GND
QC	Floating

CPU	Auto Detect
DC	3D3V_S5
QC	GND

CPU	QC/DC
DC	3D3V_S5
QC	GND

1G86D Truth Value Table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

CPU_CONT	KBC
1	RSMRST# KEEP LOW AND POWER LED FLASH
0	RSMRST# AND POWER LED NORMALLY

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Title: Penryn(1/3)-AGTL+/XDP
Size: Custom | Document Number: Bali | Rev: -1
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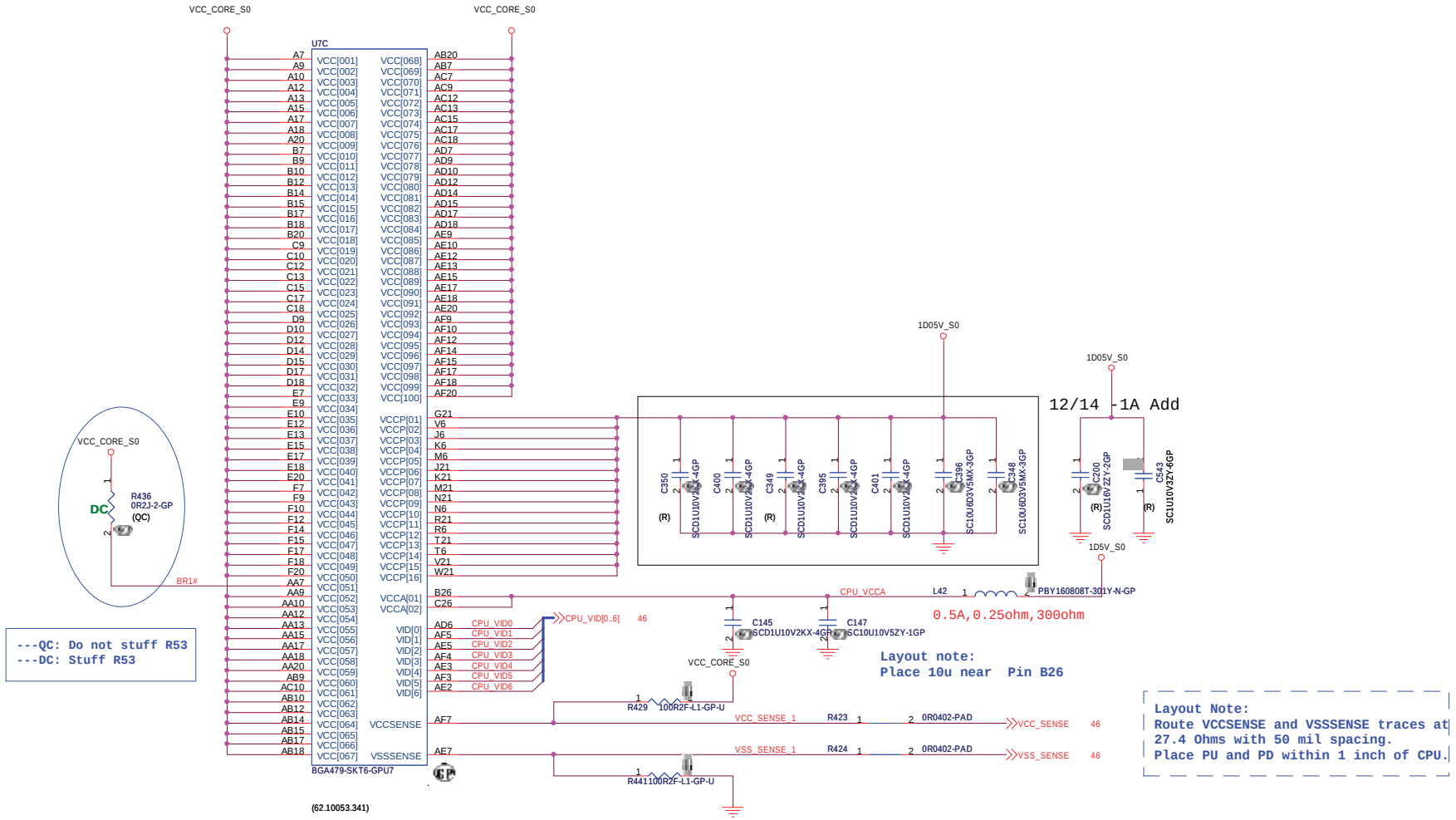

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Title: Penryn(2/3)-AGTL+/PWR

Size	Document Number	Rev
A3	Bali	-1

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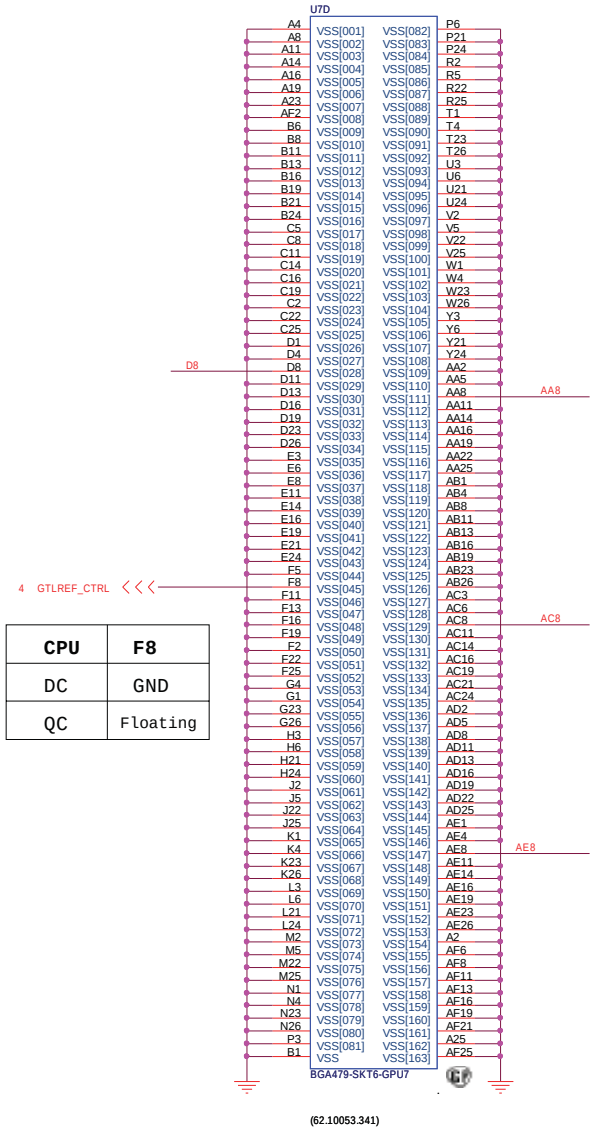
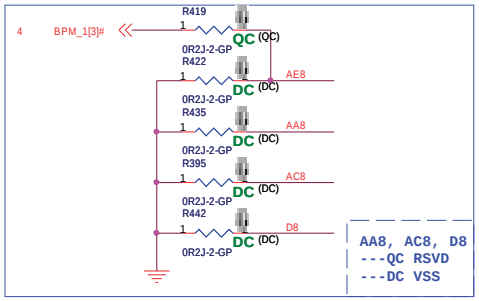
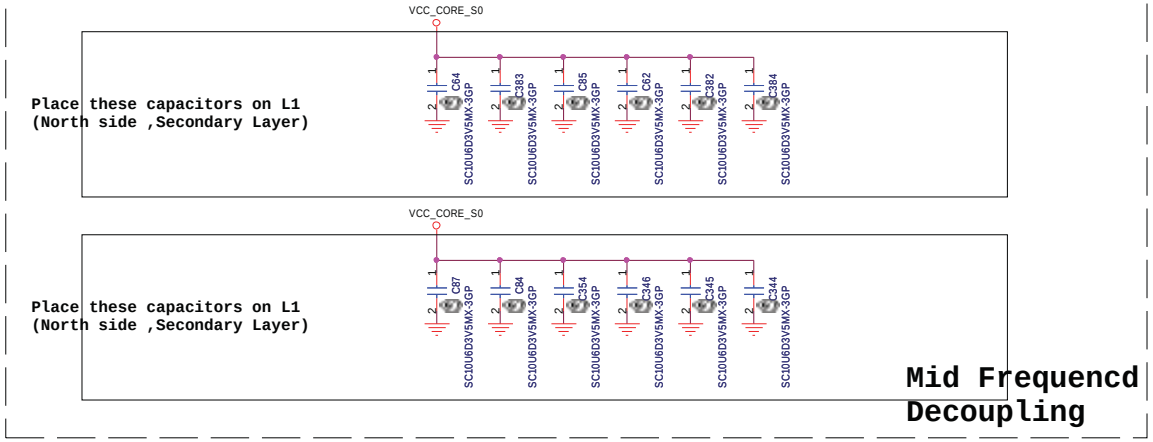
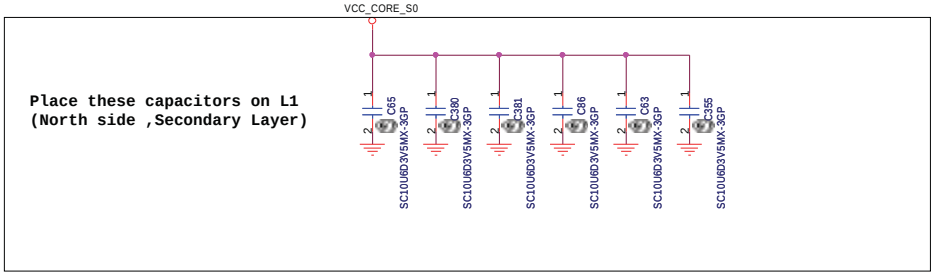
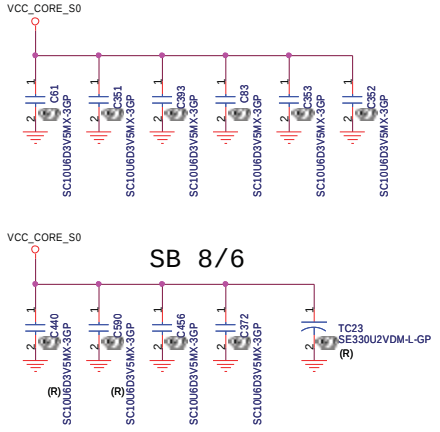


CPU	F8
DC	GND
QC	Floating









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Title: Penryn(3/3)-GND&Bypass

Size	Document Number	Rev
A3	Bali	-1

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ITP Connector

Remove

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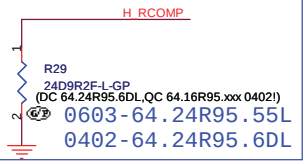
Title: *Penryn(3/3)-GND&Bypass*

Size	Document Number	Rev
B	Bali	SA

Date: Friday, February 13, 2009 Sheet 7 of 52

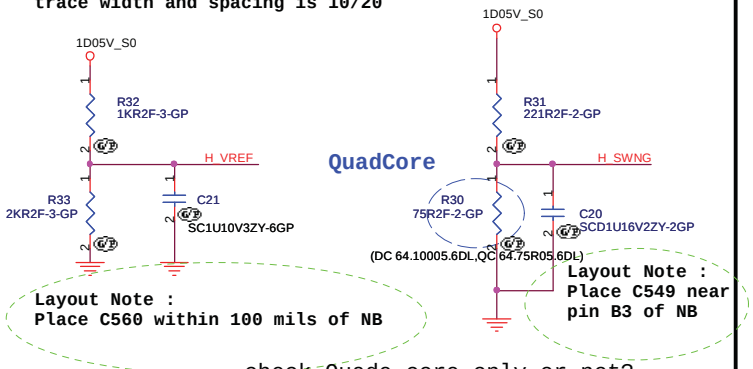
Layout note:
Trace should be 10-mil wide
with 20-mil spacing

QuadCore



check Quade core only or not?

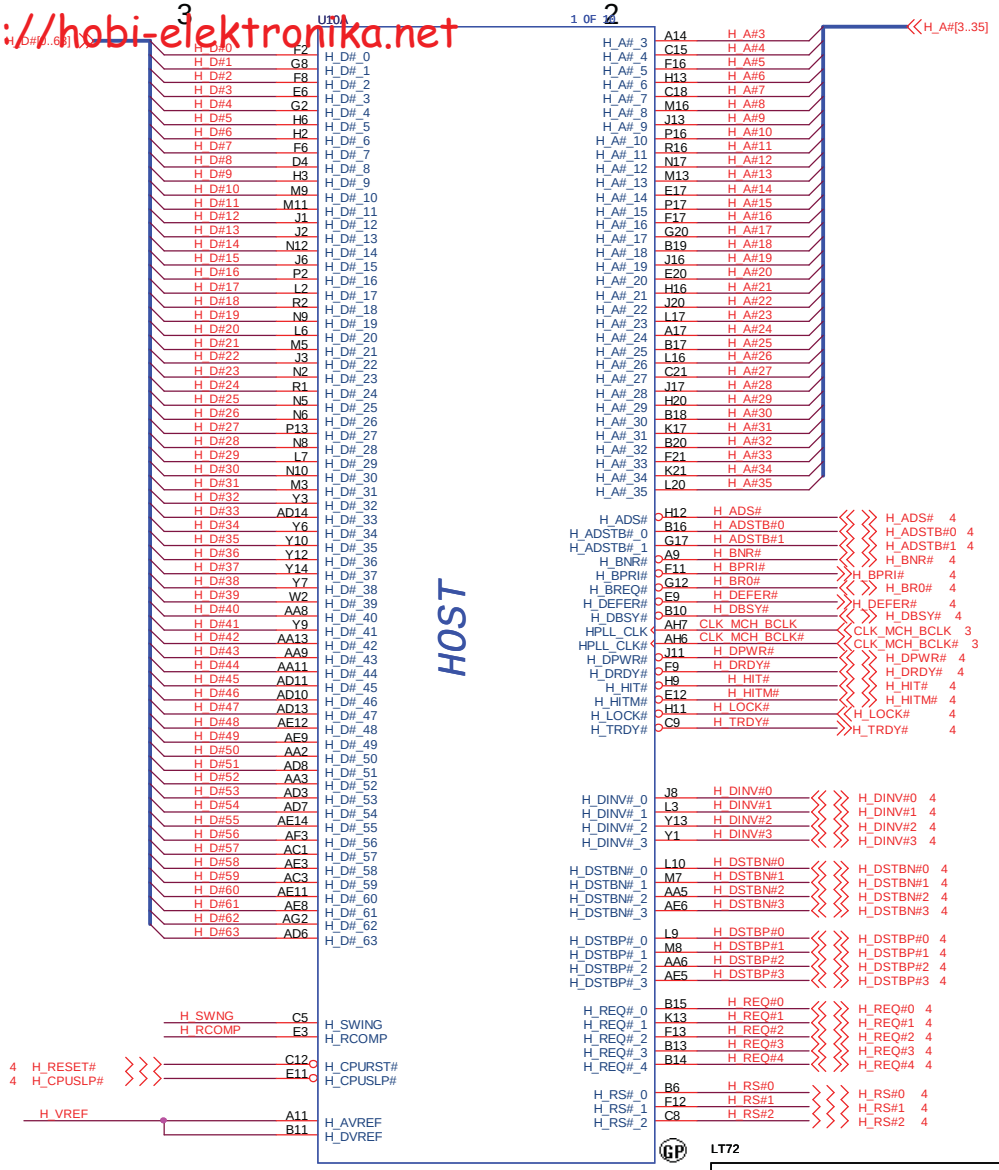
Layout Note :
H_RCOMP / H_VREF / H_SWNG
trace width and spacing is 10/20



Layout Note :
Place C560 within 100 mils of NB

Layout Note :
Place C549 near
pin B3 of NB

check Quade core only or not?



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Title: CANTIGA(1/7): HOST I/F

Size	Document Number	Rev
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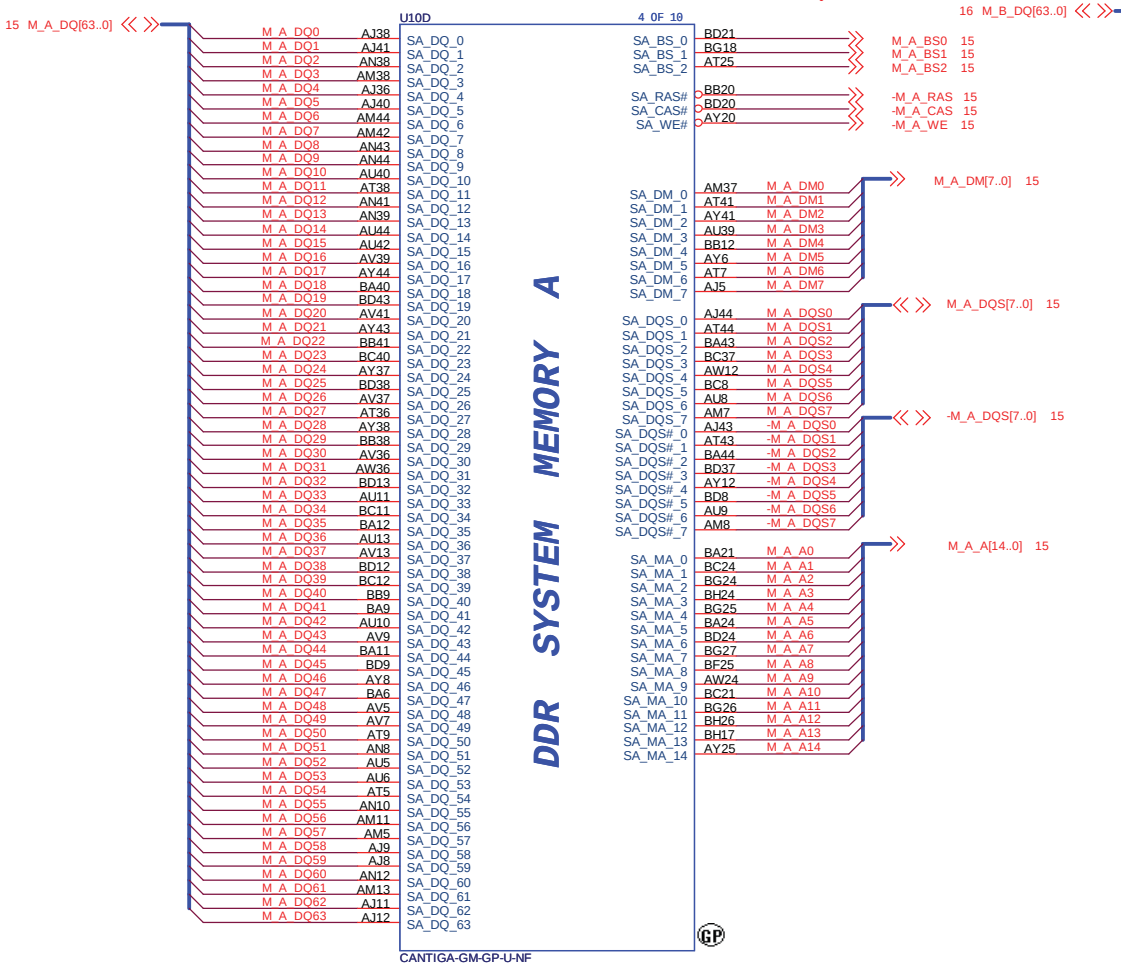
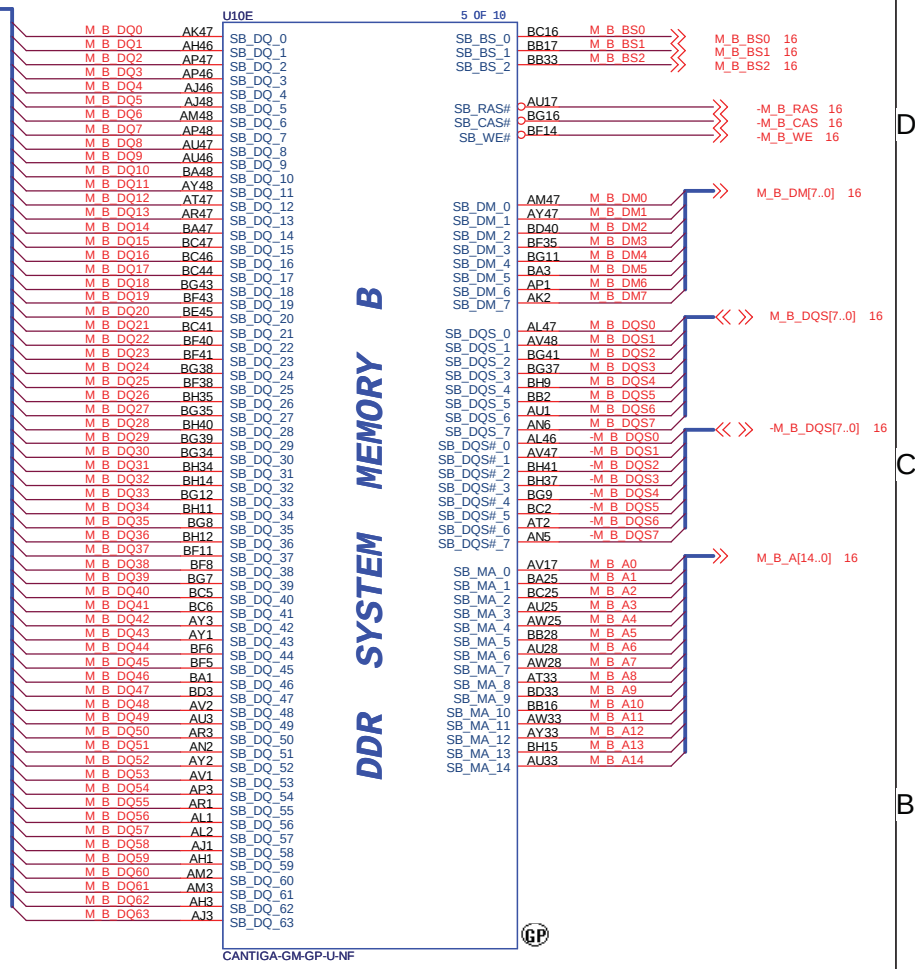
Date: Friday, February 13, 2009 Sheet 8 of 52





LT72

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CANTIGA(2/7)-DDR3 A/B CH***

Size	Document Number	Rev
B	Bali	-1

Date: Friday, February 13, 2009 Sheet 9 of 52

ME DEBUG PORT PIN OUT TABLE

RESERVED#AL34	ME_JTAG_TCK
RESERVED#AK34	ME_JTAG_TDI
RESERVED#AN35	ME_JTAG_TDO
RESERVED#AM35	ME_JTAG_TMS

CFG5 : DMIx2
CFG6 : iTPM
CFG7 : ME Crypto
CFG9: PCIE STD& REV
CFG16 : FSB Dynamic ODT
CFG19 : DMI Lane reversal
CFG20 : DP concurrent
CFG[17:3]:internal pullup
CFG[20:18]:internal pulldown

U10B — 2 OF 10

RSVD
DDR CLK/ CONTROL/COMPENSATION
CLK
DMI
CFG
GRAPHICS VID
PM
ME
MISC
NC
HDA

PCI-E reverse:Low

part number error!

check 1.5 or 1.05V Power GD

SB 0111/08

check

12/12
-1C Modify

08/06
R484 delete

Remove 6/17

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CANTIGA-GM-GP-U-NF

(71.0GM47.00U)

(64.20005.6DL)

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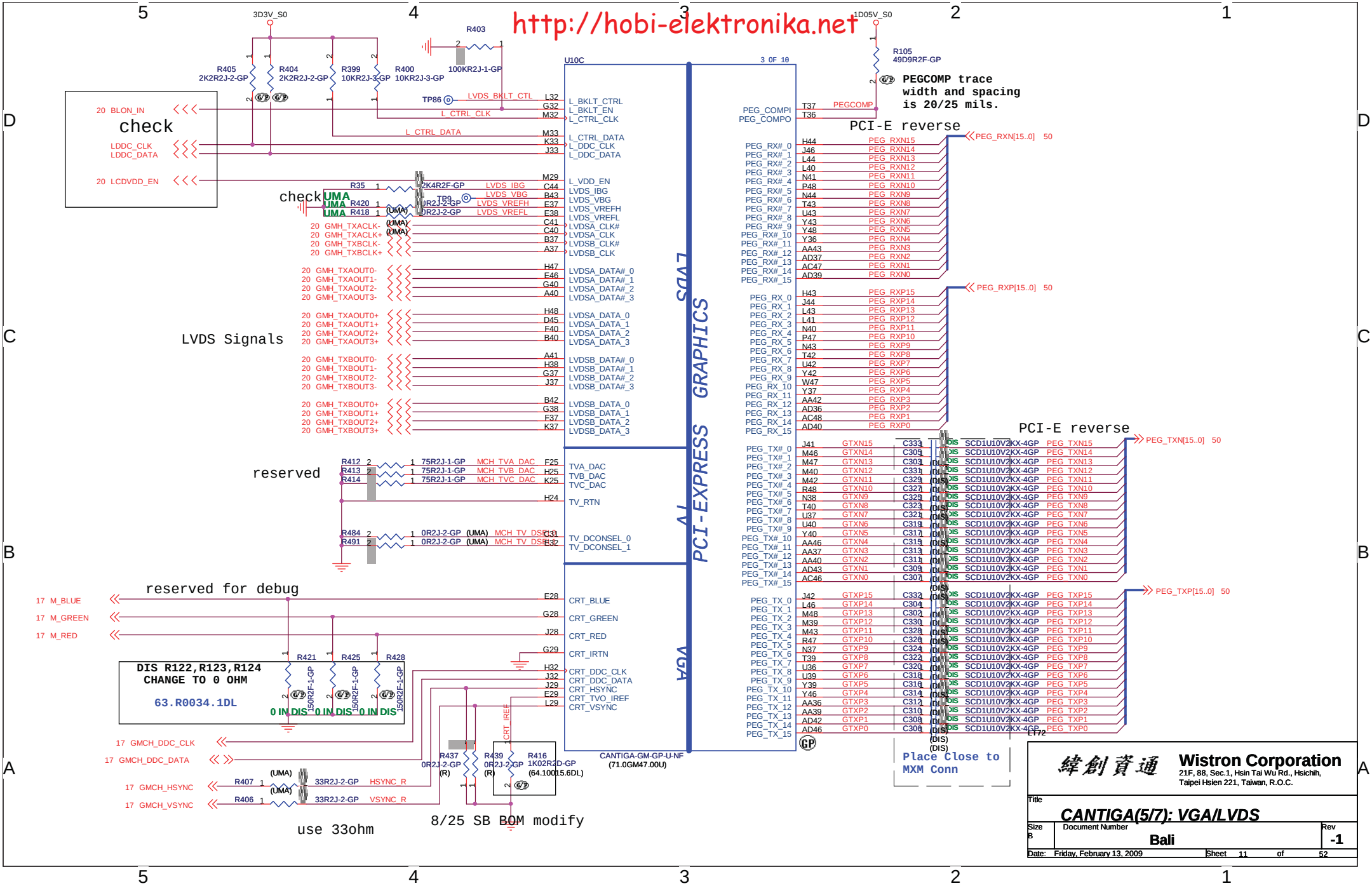
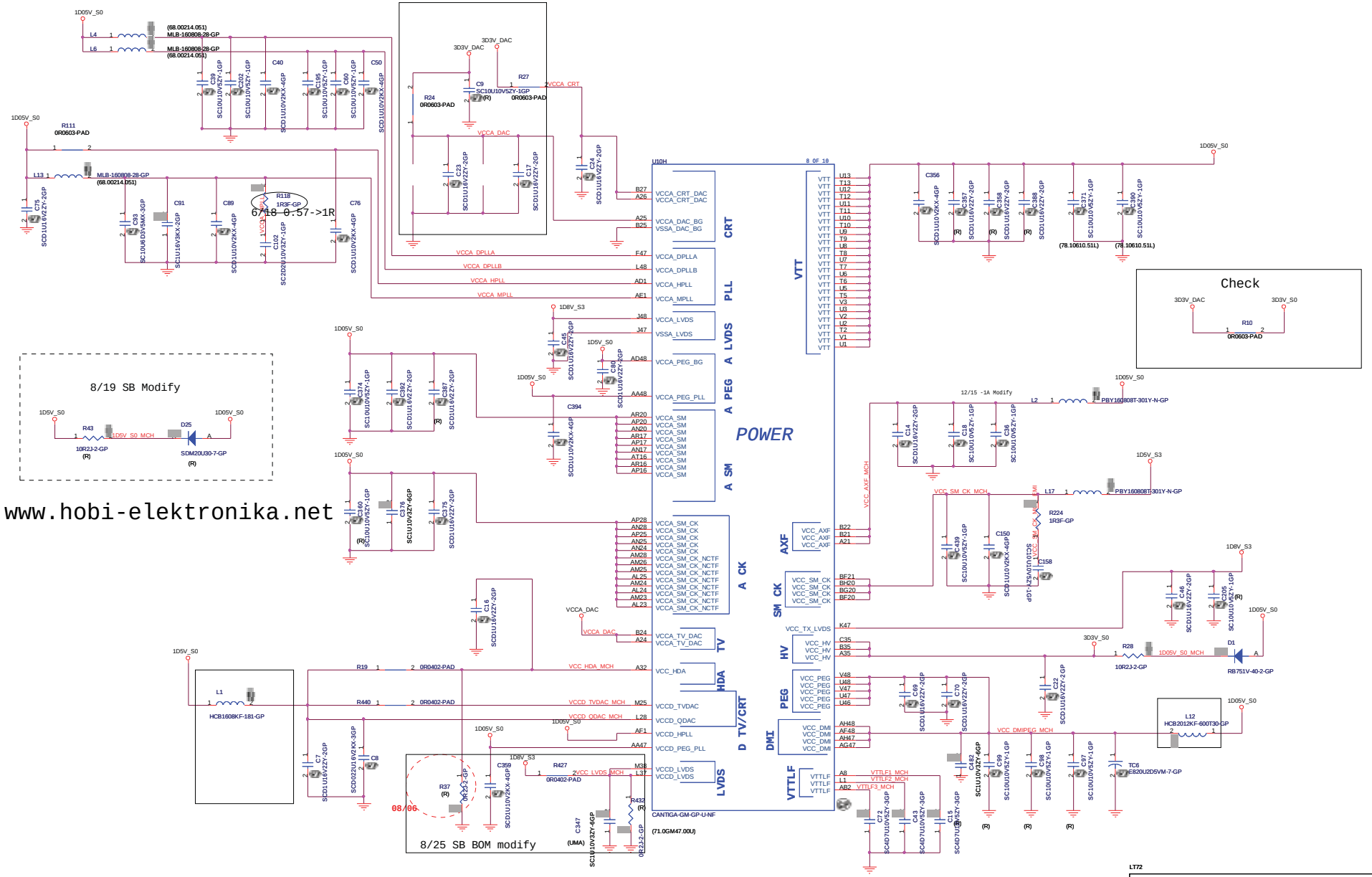
Taipei Hsien 221, Taiwan, R.O.C.

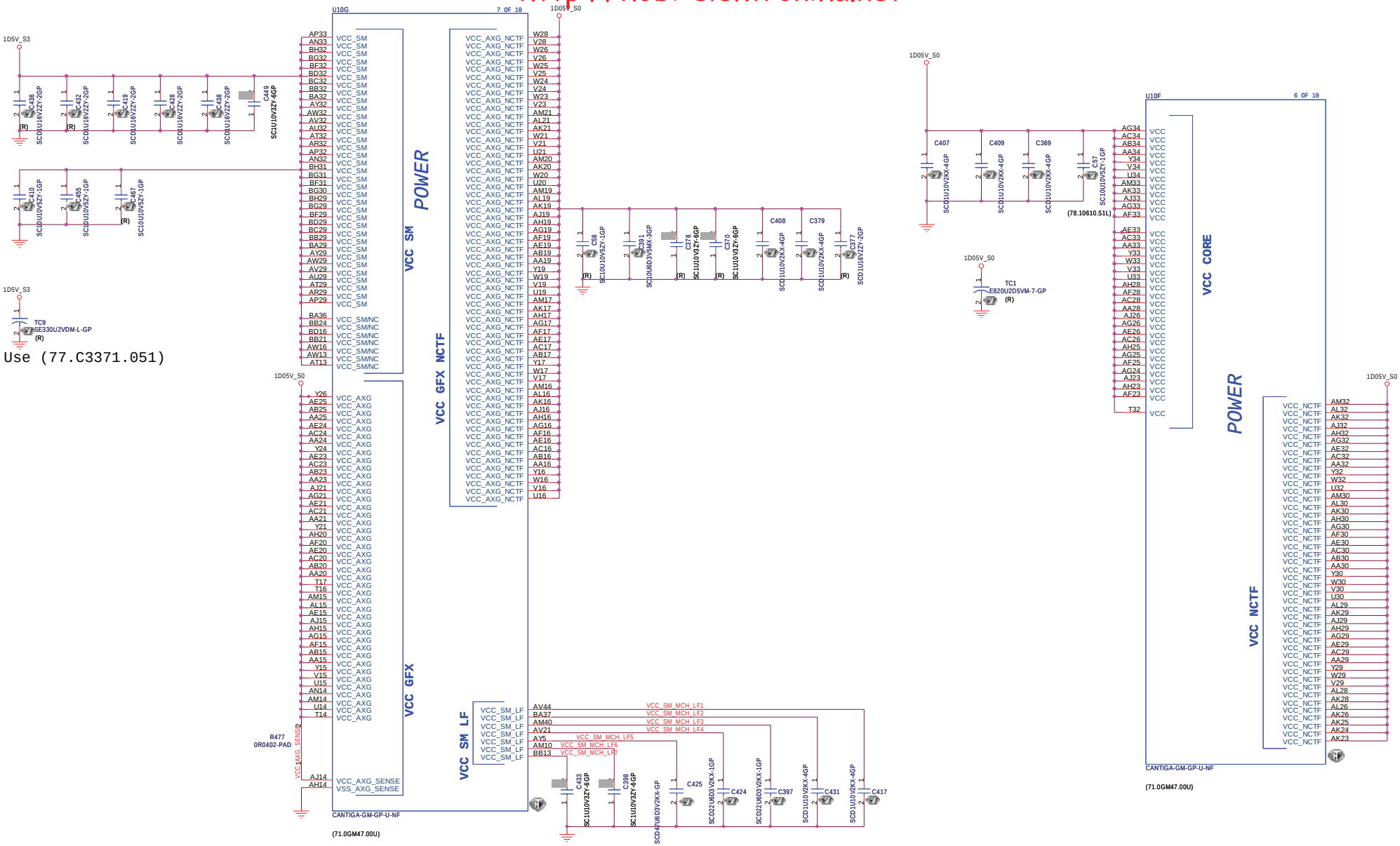
Title: CANTIGA(3/7):DMI/PM/CFG/GF

Size: Custom | Document Number: Bali | Rev: -1

Date: Friday, February 13, 2009 | Sheet 10 of 52

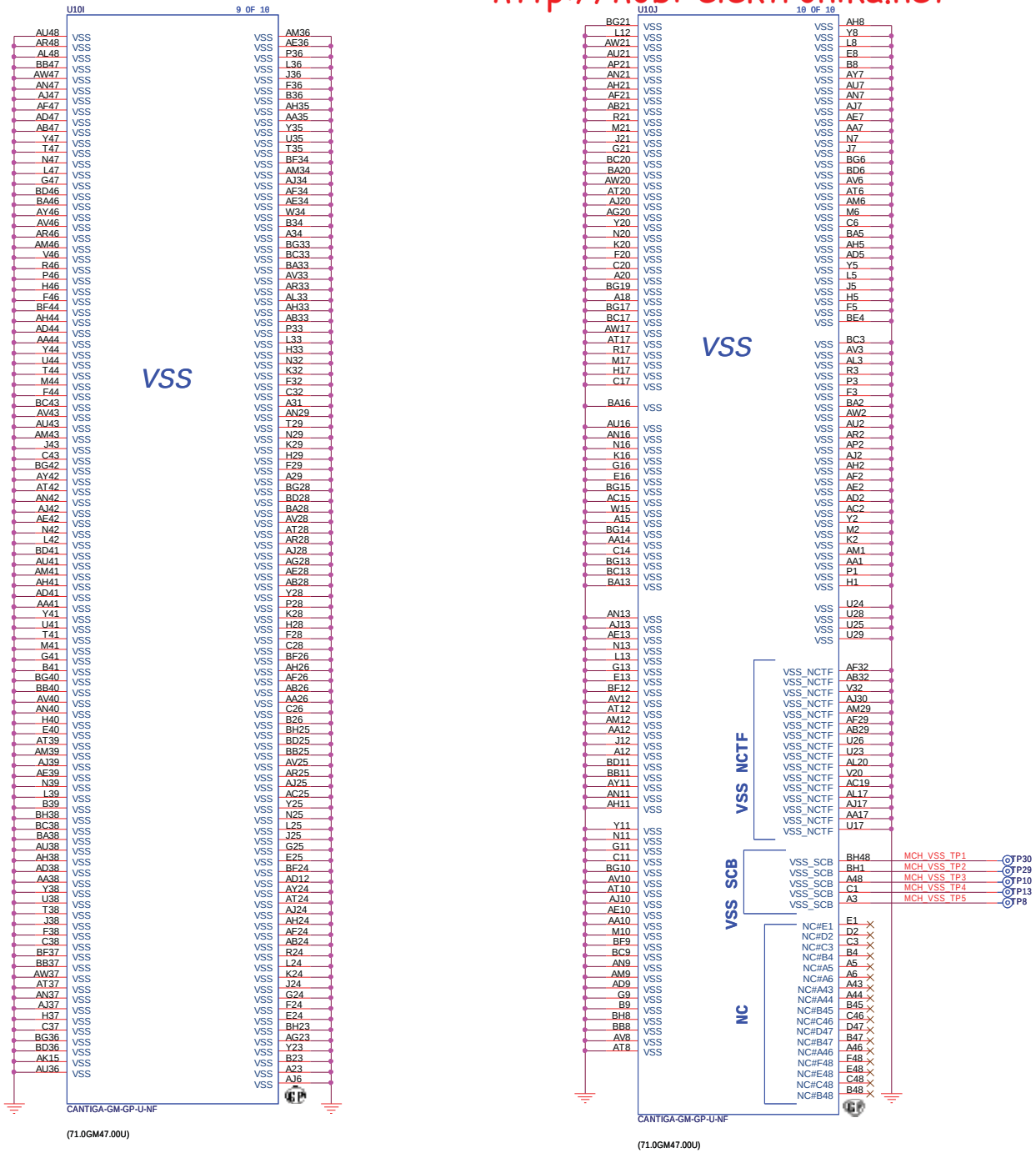






LT72

緯創資通	**Wistron Corporation**
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***CANTIGA(6/7)-PWR2***
Size: Custom	Document Number: **Bali**
Rev	**-1**
Date: Friday, February 13, 2009	Sheet 13 of 52



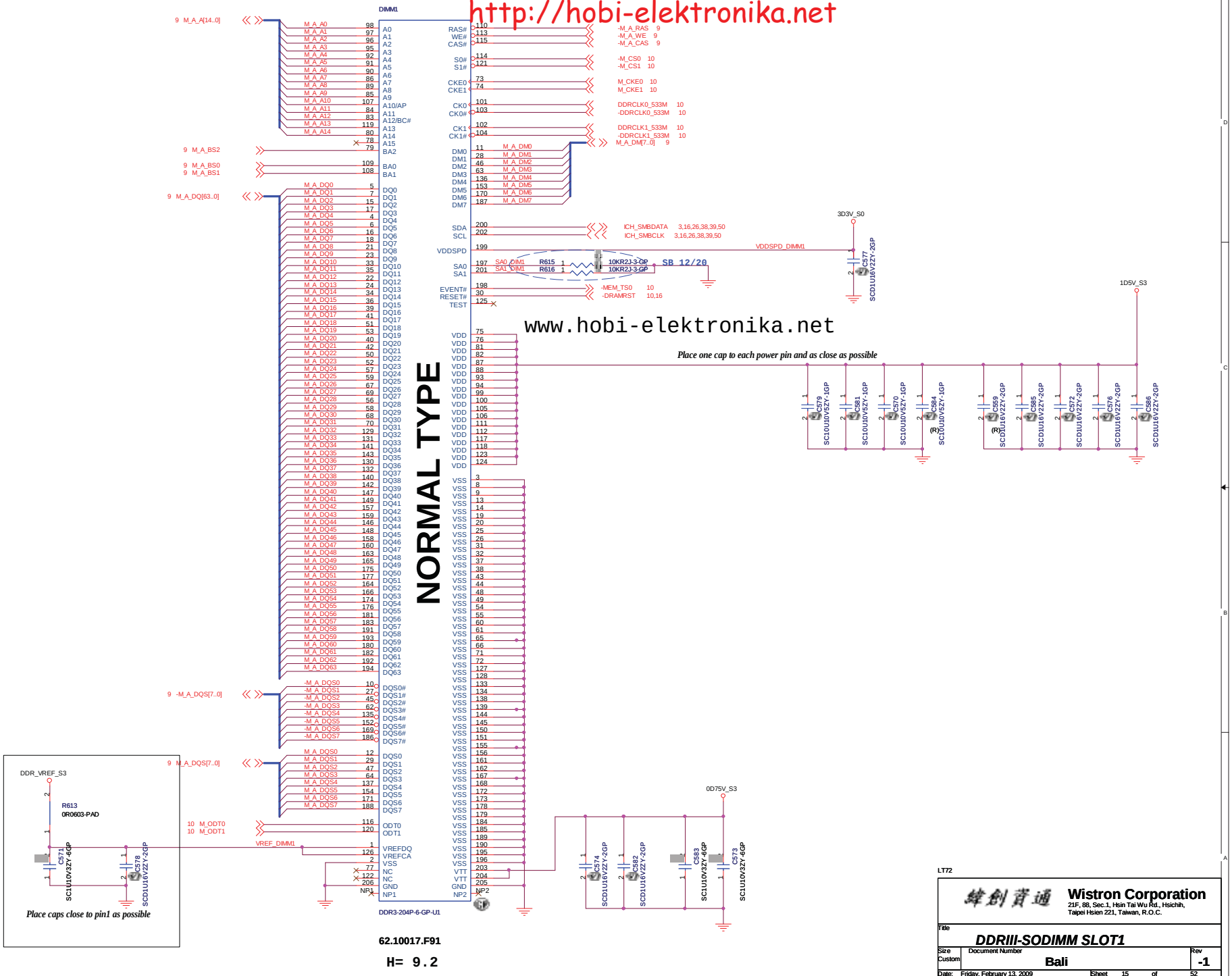
LT72

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CANTIGA(7/7): GND

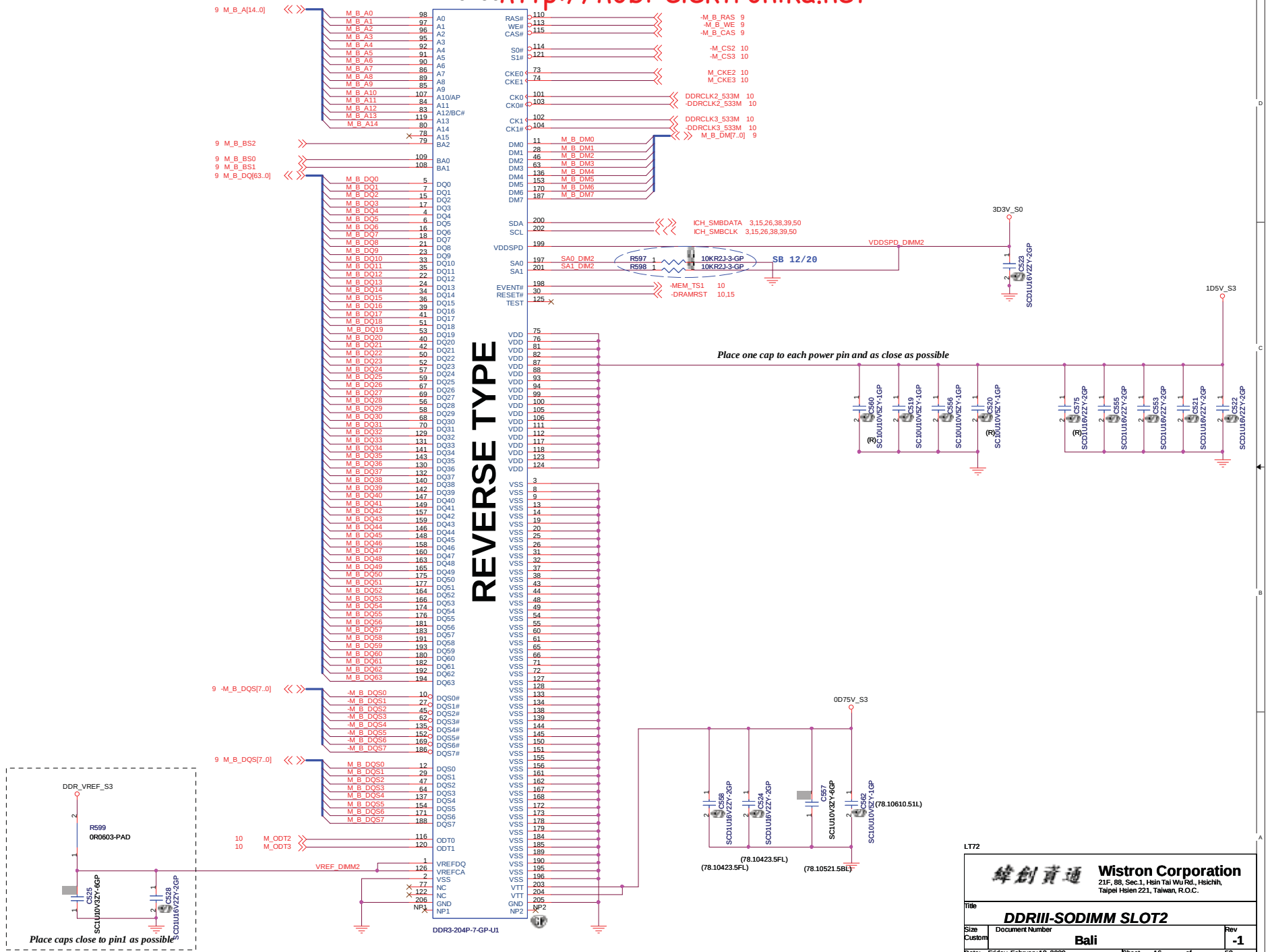
Size	Document Number	Rev
A3	Bali	-1

Date: Friday, February 13, 2009 Sheet 14 of 52



LT72

蜂創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***DDRIII-SODIMM SLOT1***	
Size: Custom	Document Number: **Bali**	Rev: **-1**
Date: Friday, February 13, 2009	Sheet 15 of 52	



LT72

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDRIII-SODIMM SLOT2**

Size	Document Number	Rev
Custom	Bali	-1

Date: Friday, February 13, 2009 Sheet 16 of 52

CRT I/F & CONNECTOR

20070615 Change VGA header for debug propose

8/6 Modify. Mirror connection and Key 1

-1A Modify the connector

11/12 -1B

JWT new: 21.61024.108

Layout Note:
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Layout Note:
Place these resistors close to the CRT-out connector

22ohm

68.00084.A11 Change to 68.00143.111
09/24

SB 0111/08

check

check pullhigh

Modify in -2A

LT72

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT Connector

Size: B | Document Number: Bali | Rev: -1

Date: Friday, February 13, 2009 | Sheet 17 of 52

Naming convention –
  Please confirm if Bali MB is "L-IGM45" ------It's true.
Paste location?-------------------------------------
  Place character string "L-IGM45" in silk-screen layer and Easy to observe position of PCB.
don't paste it with lable paper.

Location Box for P/N+Head Code+FRU Number -------
      please follow lenovo SPEC about size,after the assembly,the Box is advantageous for the scanning the position.
Please provide this number rule information---------
          Please follow lenovo SPEC.

Remove

Location Box for MAC Address -------------------------
       Please lay aside nearby P/N Box, does not affect to the P/N lable scanning position.
Please provide MAC information--------------------
          Lenovo does not supply this information, after needing ODM supplier apply and assign it to use.

Label for LC ERP No.; (A label with 8 digits' Arabic number) ---------
This Lable with 11s lable(P/N+HC+ FRU) the identical lable, now was also already unable to provide the information,
the interior needs to discuss.only reserve Box(itme 2).
Please provide this number rule information---------
          the number need apply from lenovo system,needs the internal
          discussion.

LT72

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Taipei Hsien 221, Taiwan, R.O.C.

Title	VGA IN(1/2)-RGB IN	
Size B	Document Number Bali	Rev -1
Date: Friday, February 13, 2009	Sheet 18 of 52	

Remove

LT72

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

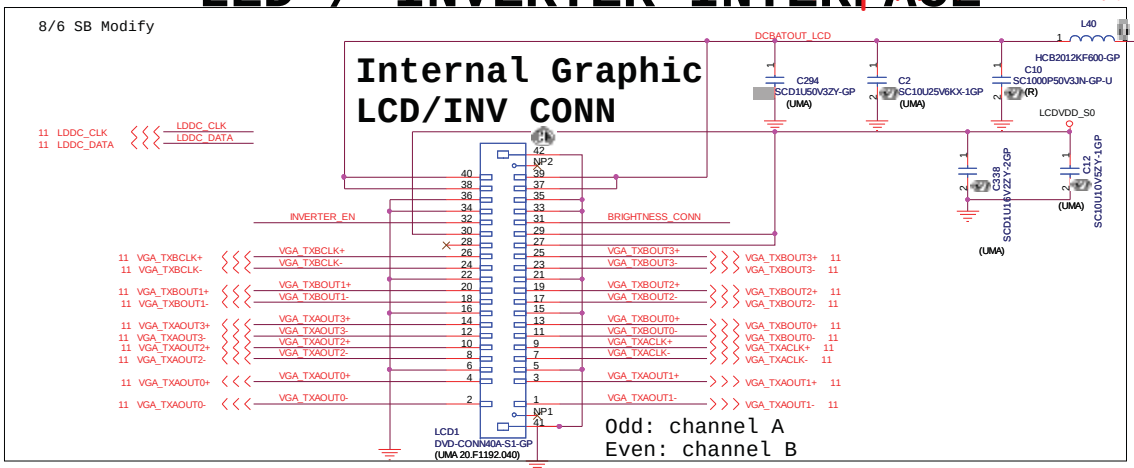
Title

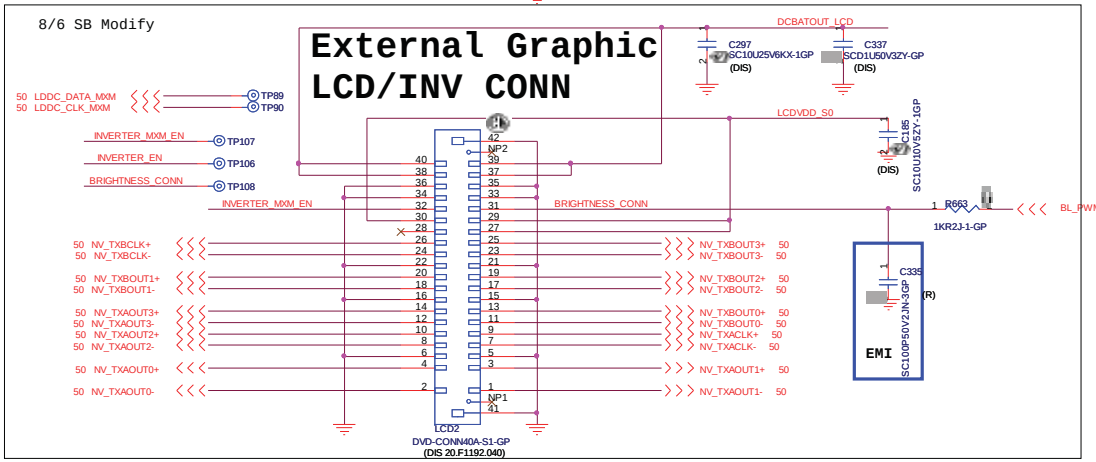
VGA IN(2/2)-NT68665H

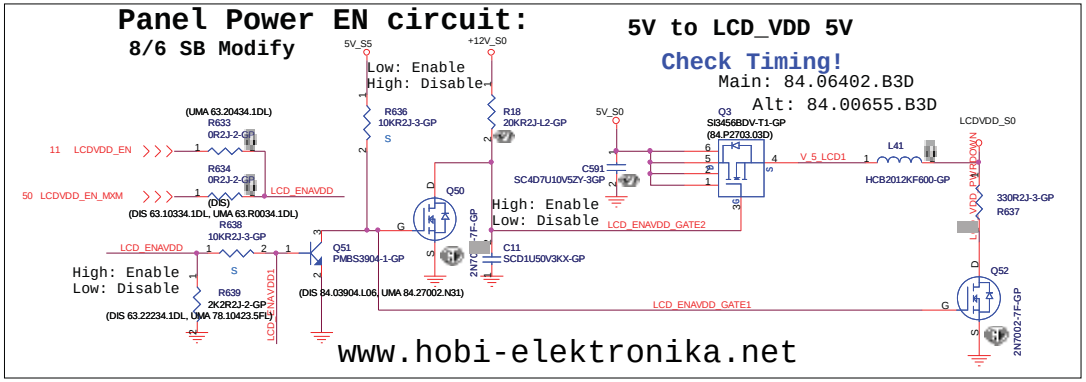
Size	Document Number	Rev
B	Bali	-1

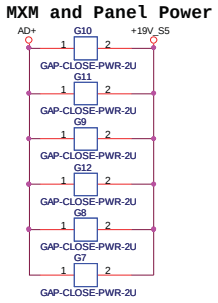
Date: Friday, February 13, 2009 Sheet 19 of 52

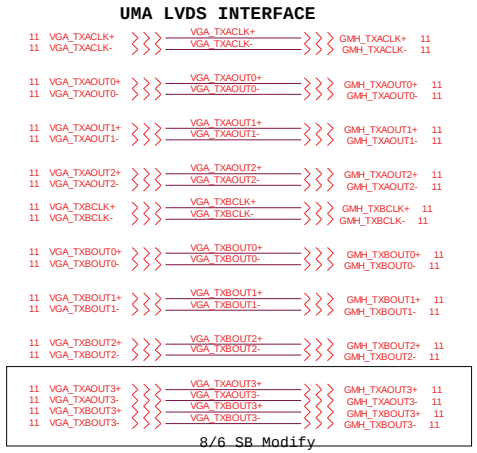
LED / INVERTER INTERFACE

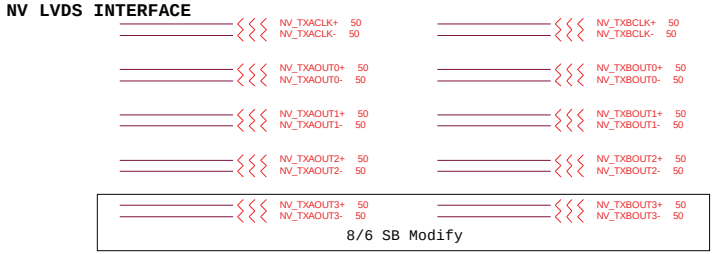


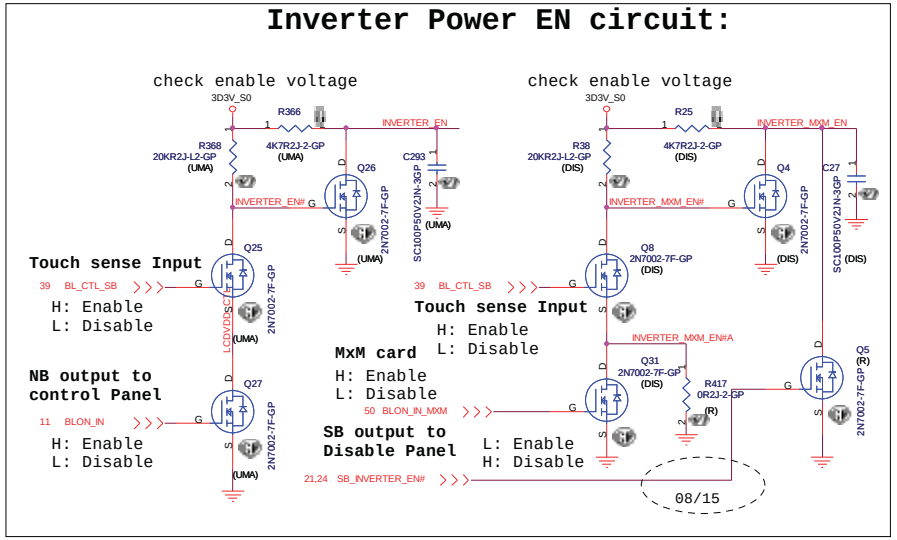












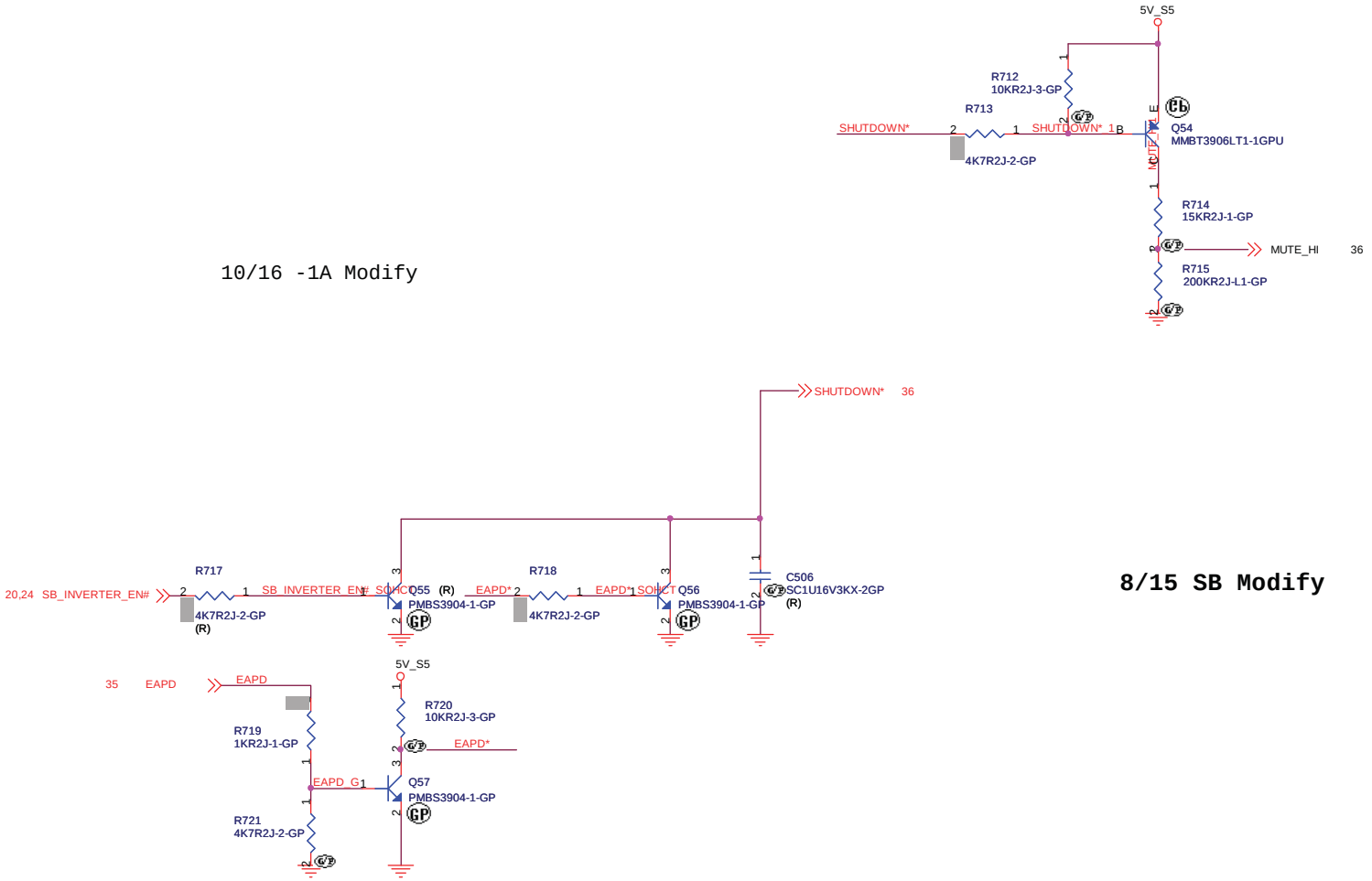
LT72

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: LCD/Inverter Connector		
Size: Custom	Document Number: Bali	Rev: -1
Date: Friday, February 13, 2009	Sheet 20 of 52	

10/2 -1A Unmount

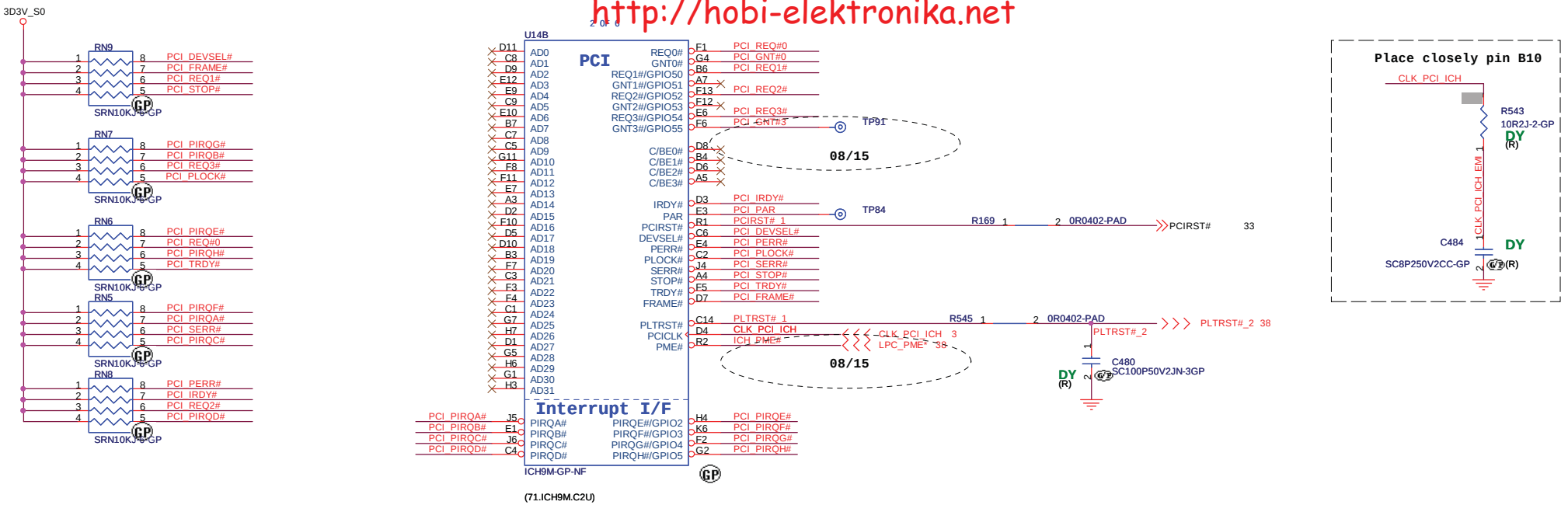
10/16 -1A Modify

8/15 SB Modify

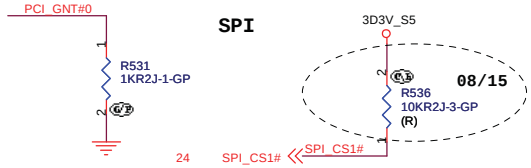


LT72

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: **MUTE**		
Size: B	Document Number: Bali	Rev: -1
Date: Friday, February 13, 2009	Sheet 21 of 52	



Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *



A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enable High= Default *

Remove

LT72

緯創資通 Wistron Corporation
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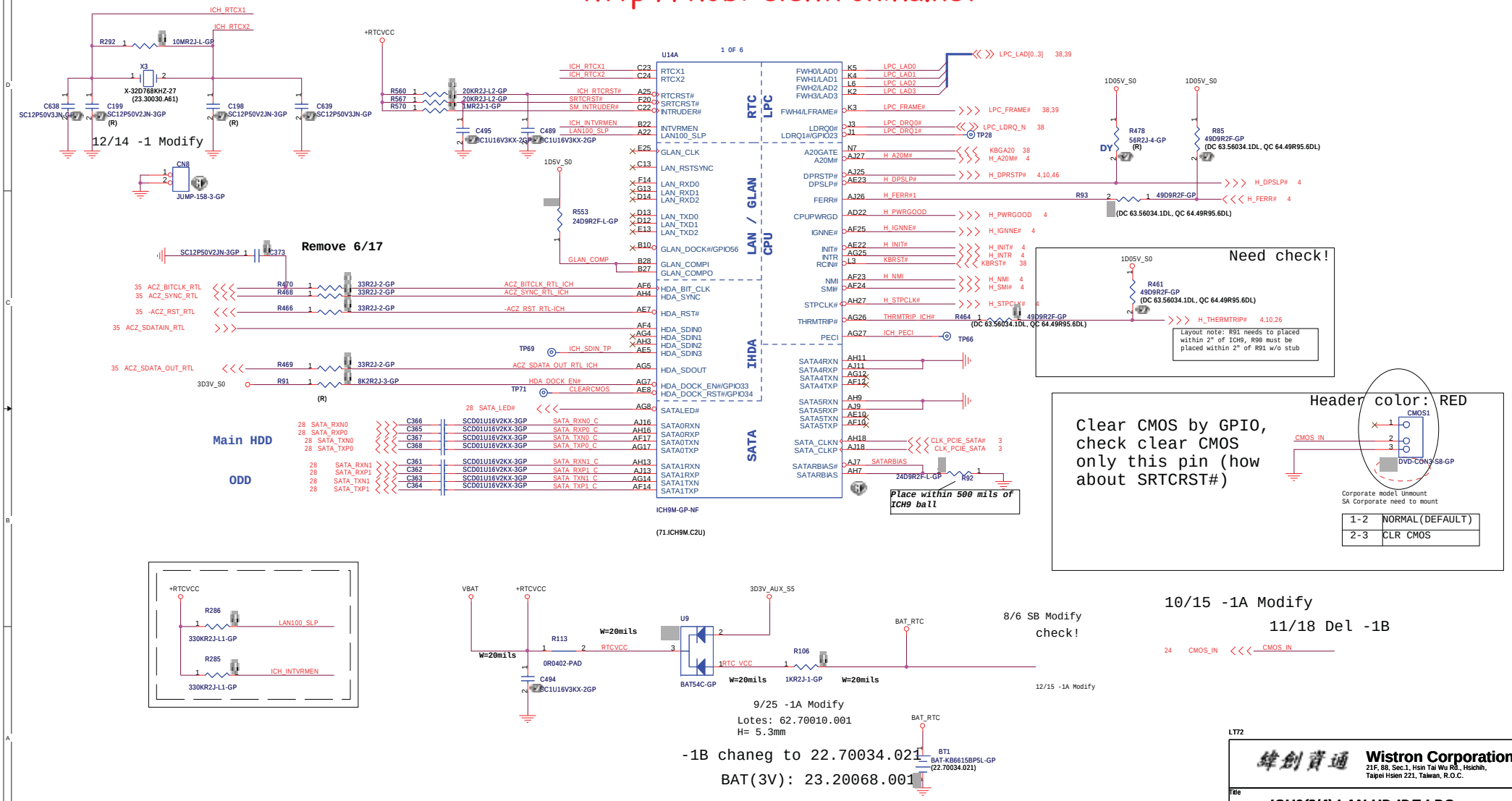
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH9(1/4)-PCI/INT

Size	Document Number	Rev
Custom	Bali	-1

Date: Friday, February 13, 2009 Sheet 22 of 52



No Reboot Strap	
SPKR	LOW = Defaule High=No Reboot

Check SPK

Remove to SIO

3 OF 6

4 OF 6

08/15

10/2 -1A Modify

check PL 10K !

8/28 SB BOM change

10/15 -1A Modify

8/6 SB Remove

11/12 -1B

8/28 SB BOM change

8/6 SB Modify

SB 0110/08

8/6 SB modify

Mini Card 1

Mini Card 2

1394/Card reader

Check LAN

12/14 -1 Remove

12/14 -1 Modify

-1A 10/13 change

USB2x1 Rear

USB2x1 Rear

PCI-Ex1 1

CAMERA 10/13 -1A Modify

WIRELESS KB/MS

PCI-Ex1 210/13 -1A Modify

BT

9/30 -1A Modify

USB1x2 Side

H: no MXM, L: MXM on

Low: Normal
High:Low Power

PCB_VER0	PCB_VER1	PCB_VER2	M/B
0	0	0	SA
0	0	1	SB
0	1	0	-1A
0	1	1	-1B
1	0	0	-1
1	0	1	-2A

GPIO49 should be pulled down to GND only when using Teenah. When using Cantiga, this ball should be left as No Connect.

Signals must NOT float if they are not being used
OC [11:0]# are not 5-V tolerant. OC [11:0]# may optionally be used as GPIOs

Wistron Corporation
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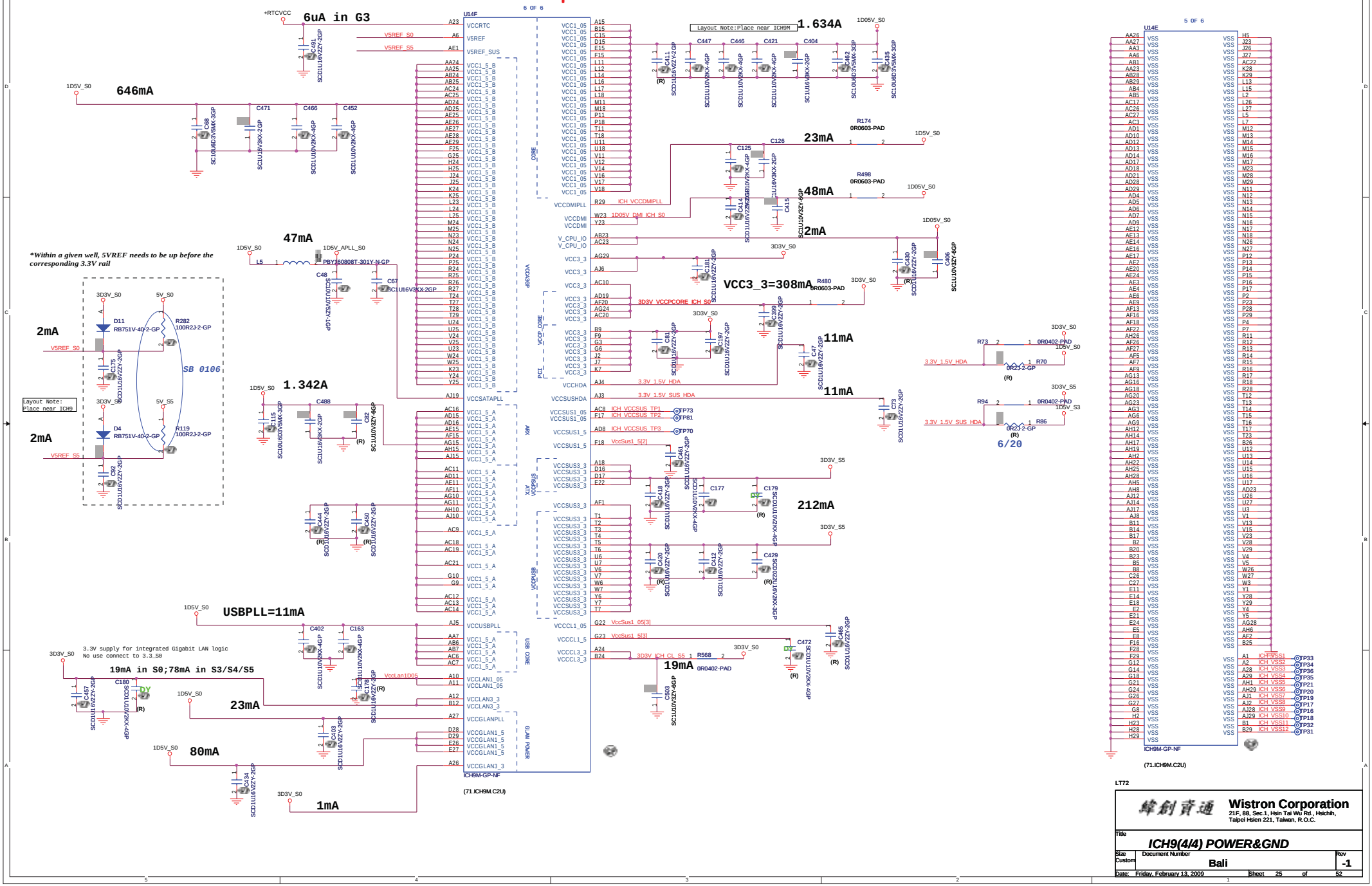
Title: ICH9(3/4) PM,USB,GPIO

Size: Custom | Document Number: Bali | Rev: -1

Date: Friday, February 13, 2009 | Sheet 24 of 52



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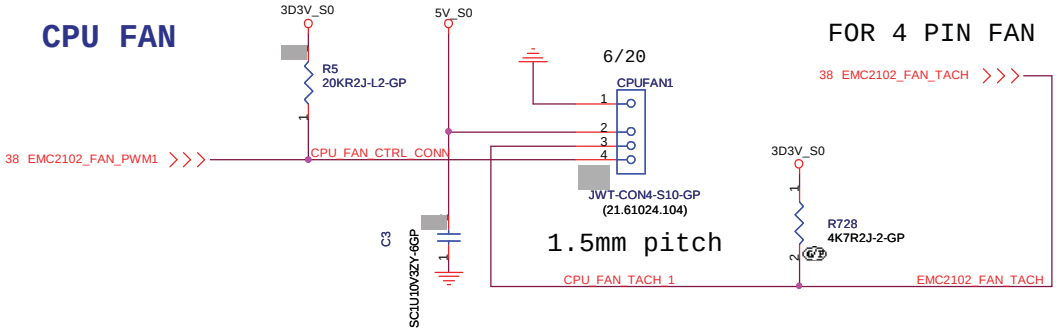
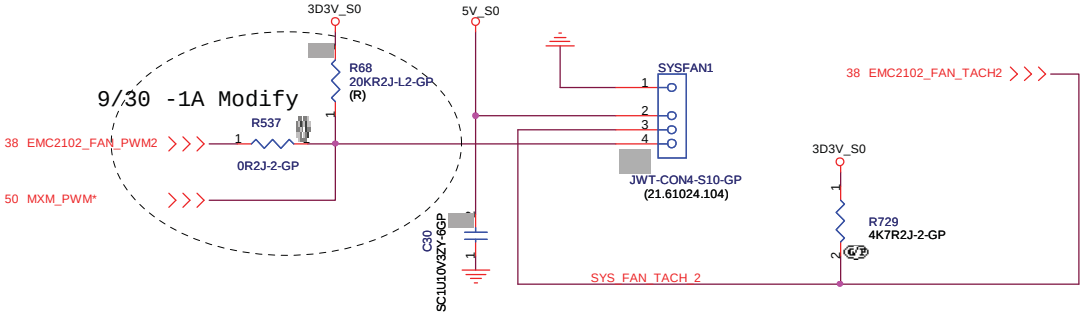
CPU FAN

FOR 4 PIN FAN



8/19 SB Modify

MXM_SYS FAN

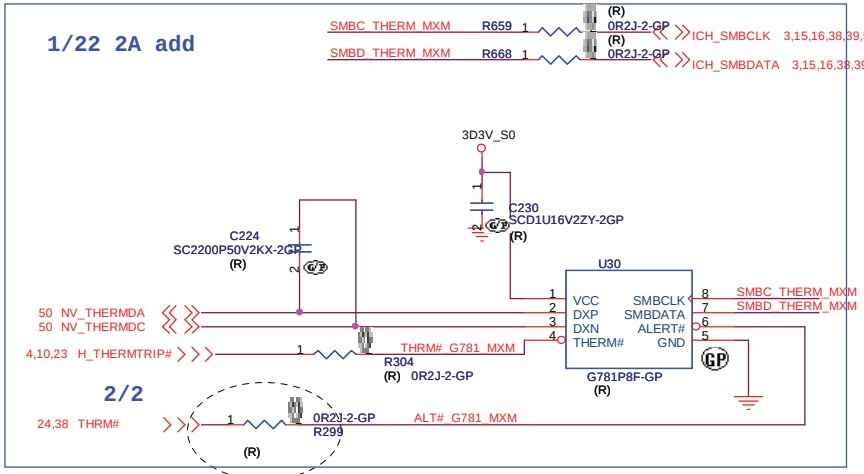


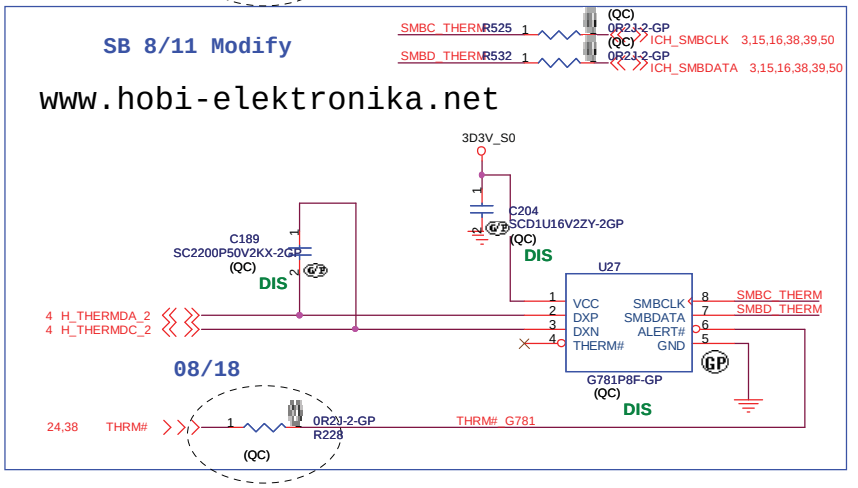
8/19 SB Modify

08/18

Remove MxM card thermal detect IC

Remove thermal circuit





LT71 DIS BOM

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *Thermal/Fan Controllor EMC2102*		
Size: B	Document Number: Bali	Rev: SB
Date: Friday, February 13, 2009	Sheet 26 of 52	

USB PORT

Check USB power switch
power switch S5 OFF

Need check this block
-1A 10/13 change

DCBATOUT_51120
R456 15KR2J-1-GP
USB_PW_CONTROL1
Q38 MMBT3906LT1-1GPU
C385 SCD1U50V3KX-GP
USB_PW_CONTROL
R471 330KR2J-L1-GP
R457 330KR2J-L1-GP
GATE_5V
USB_PW_CONTROL2
R451 100KR2J-1-GP
R467 10KR2J-3-GP
USB2_PW_CONTROL5
USB_PW_CONTROL3
USB1_PW_CONTROL4

Check status
38 USB_SB_PWR_CRL
R447 20KR2J-L2-GP (R)
24,28,38,44,45,49 PM_SLP_S5#
R445 20KR2J-L2-GP
Q35 2N7002-7F-GP
PMBS3904-1-GP
Q36
9/30 -1A Modify

5V_S5
VCC5_USB
U37 AO4468-GP
Need check! Vgs=+/-20V

USB Power

Use 69.50007.801 (Littelfuse)
9/25 Del L23

VCC5_USB
F1 FUSE-1D5A6V-TGP (69.50007.801)
R258 470KR2J-2-GP
OC*01
C164 SC1000P50V3JN-GP-U (R)
R250 560KR2J-GP
R237 1KR2J-1-GP
C144 SC22U10V6ZY-2GP
C210 SC10U10V6ZY-1GP
C231 SC10U10V6ZY-1GP
USBVCC01
24

Side 4 USB PORT (0/1)
04/04/2006

IP4220CZ6-GP
USBP0P_EXT
USBP1P_EXT
ESD I/O1
GND
ESD I/O2
ESD I/O4
VP
ESD I/O3
USBP0N_EXT
USBVCC01
USBP1N_EXT
D10
C244 SCD1U16V2ZY-2GP (R)

USBx1
USB2
8/11 Add
C226 C208 C207 SC10U10V6ZY-1GP
SKT-USB-130-GP
Tyco 22.10218.N11

USBx1
USB1
C154 C142 SC10U10V6ZY-1GP
SKT-USB-130-GP

R564 20R0402-PAD
TR4 (R)
24 USB_PP0
24 USB_PN0
USBP0P_EXT
USBP0N_EXT
ACM2012H-900-GP-DUMMY
R563 20R0402-PAD
2007/11/23,
Add for 4L
68.00201.141 Murata
69.10087.011 Chilisin

R552 20R0402-PAD
TR3 (R)
24 USB_PP1
24 USB_PN1
USBP1P_EXT
USBP1N_EXT
ACM2012H-900-GP-DUMMY
R547 20R0402-PAD
68.00201.141 Murata
69.10087.011 Chilisin

Remove 6/17

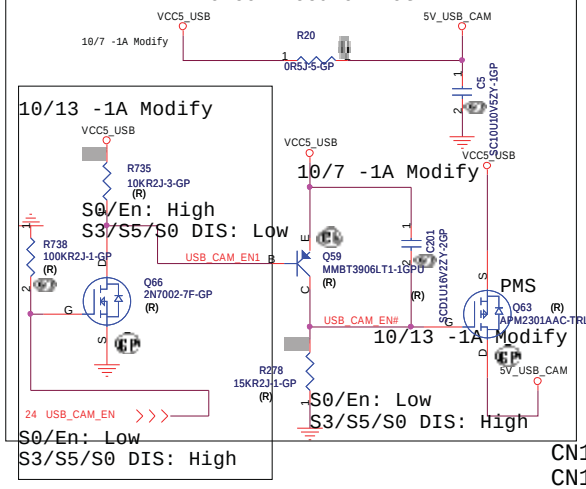
LT72

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

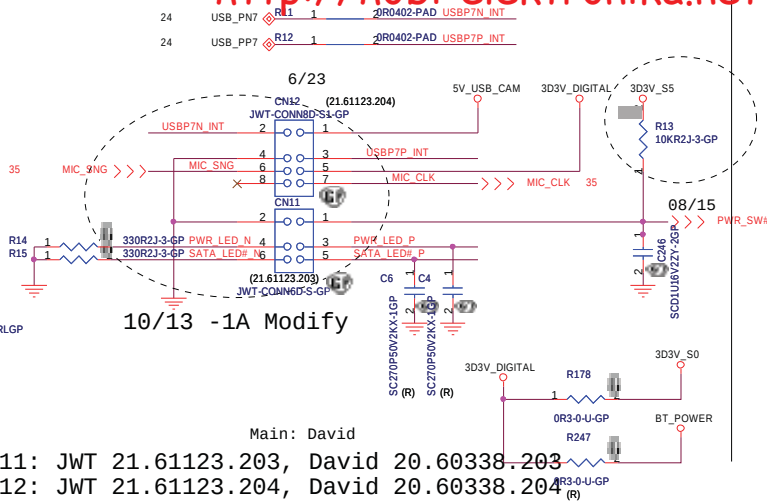
Title: USB I/O
Size: B
Document Number: Bali
Rev: -1
Date: Friday, February 13, 2009
Sheet 27 of 52

5V to 5V_USB_CAM

check need or not



CAMERA

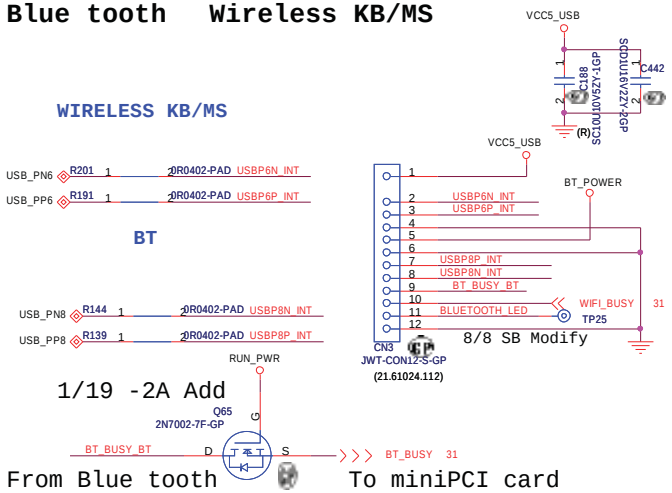


Main: David

CN11: JWT 21.61123.203, David 20.60338.203

CN12: JWT 21.61123.204, David 20.60338.204

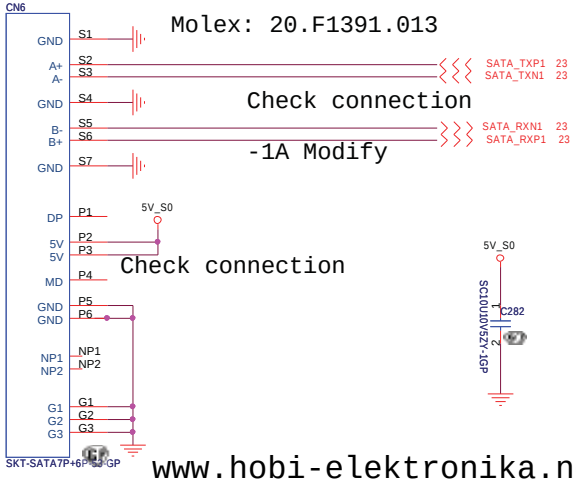
Blue tooth Wireless KB/MS



CD-ROM CONNECTOR

Check HD power(+12V) and connector type

9/25 -1A Modify



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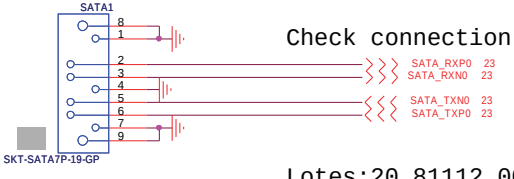
MAIN HDD Connector

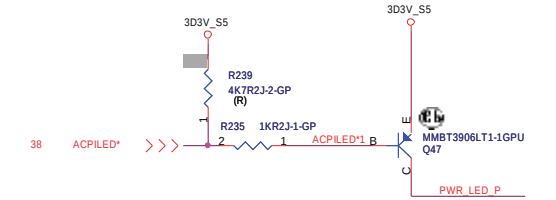


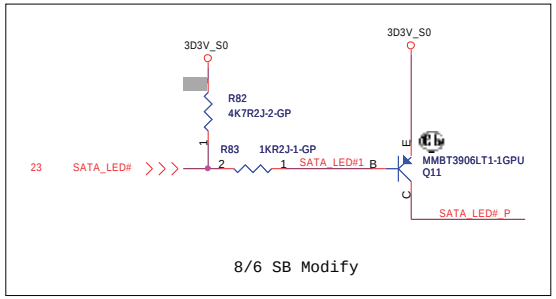
9/25 -1A Modify

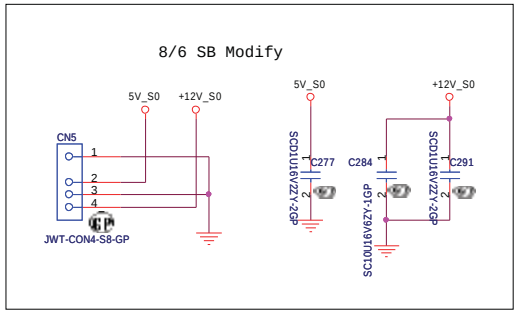
Black

Lotes:20.81112.007

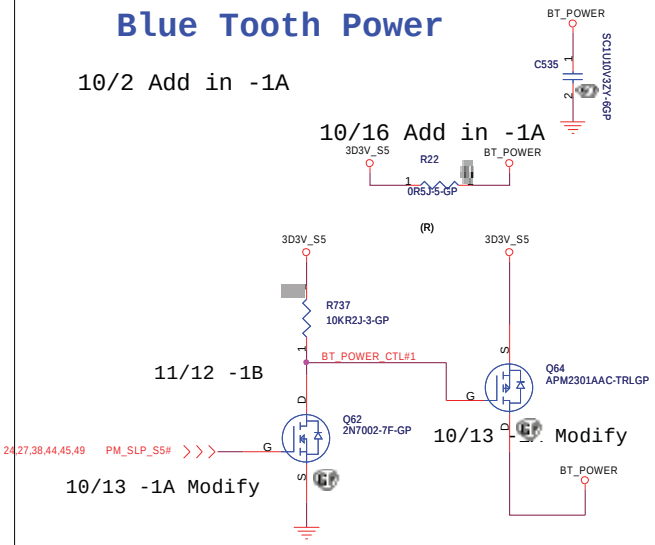
Molex: 20.80618.007







Blue Tooth Power



PM_SLP_S5#
S3/S0: High
S5: Low

SLP_S5*_INV
S3/S0: High
S5: Low

BT_POWER_CTL#1
S3/S0: Low
S5:High

BT_POWER
S3/S0: 3.3V
S5: 0V

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Title: HDD/CDROM		
Size: A3	Document Number: Bali	Rev: -1
Date: Friday, February 13, 2009	Sheet 28 of 52	

+3V3 and +1V8 Source power must disable at S3 mode

Decouple capacitors
1394 Differential Pairs = 110 Ohm

Power Circuit Trace Width: 40 mil (Min.)
Power plane or Power shape is more better

8/6 SB Add Check

8/19 SB Add

Create power(CR1_PCTLN) from Jmicon chip

Note:
R133 use 0805 type and over 20 mils trace width on both side (CR1_PCTLN & CR1_POWER)

LED remove

For Debug circuit remove 2008.06.13

Card Reader power circuit

TREXT trace width/length: 12mil/< 250mil

MDIO Single End = 50 Ohm

Close to JMB38x pins (<500mil)

71.00380.003 verB

For D3E Mode remove

2008.06.13

D3E support (From Ver.B)

Note:
1. Add Q3 & Delete R135, if JMB38x Power domain is different to SB chip
2. Delete Q3 & Add R135, if JMB38x Power domain is same as SB chip

Add 6 via hole to ground plane

QFN-48

For D3E support via Side-Band (From Ver.B)
For D3E Mode remove
2008.06.13

PCIe Differential Pairs = 100 Ohm

Card Reader Pull High/Low Resistors

Card Reader Connector

BIOS Note:
Clock to JMB38x must always turn on, no matter any system power state

PREXT trace width/length: 12mil/< 250mil

Check Pin13,14,15,16,17,20 function

reserve 10Kohm pull-low to GND?for MDIO7 (for EEPROM use).

H:on-board, L:on Add-in card
H:CR1_PCTLN high active,L:CR1_PCTLN low active
(MDIO12 is no use in MP version IC)
H:CR1_LEDN high active,L:CR1_LEDN low active

Power-On strapping setting

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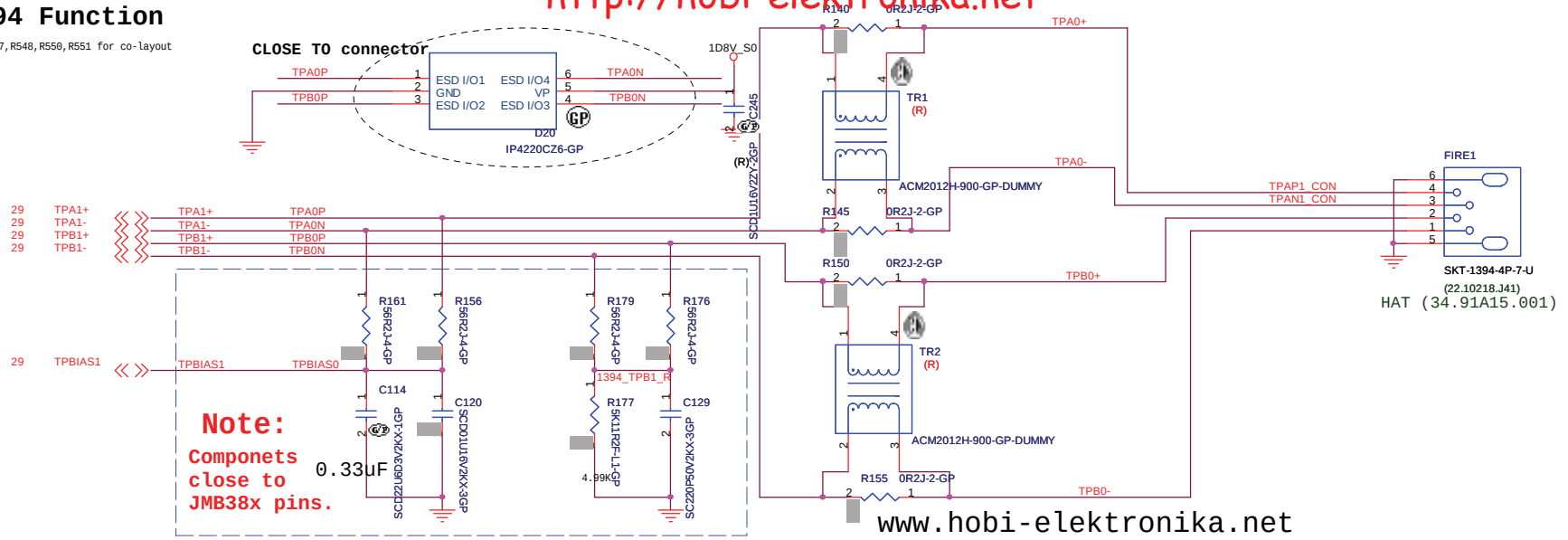
Title: Jmicron380	
Size: B	Document Number: Bali	Rev: SB
Date: Friday, February 13, 2009	Sheet 29 of 52	

1394 Function

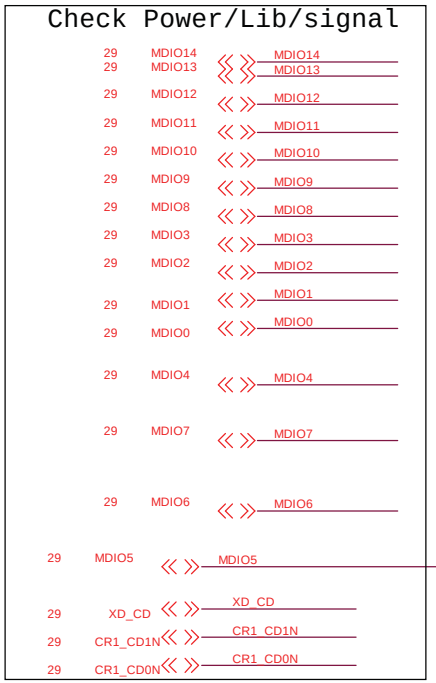
Reserve R547,R548,R550,R551 for co-layout

CLOSE TO connector

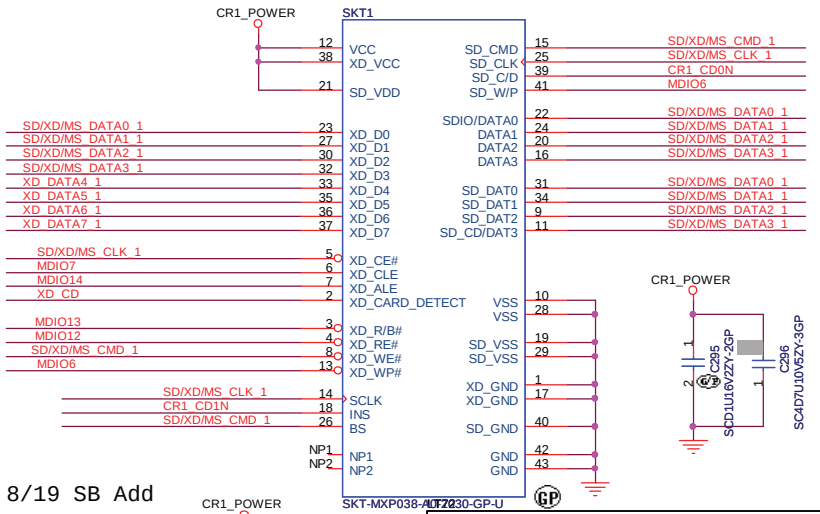
Choke / 0 Ohm Co-layout



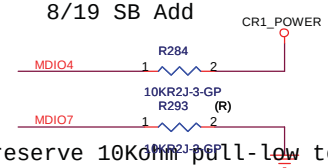
Check Power/Lib/signal



4 in 1 Card reader



8/19 SB Add



reserve 10Kohm pull-low to GND?for MDIO7 (for EEPROM use).

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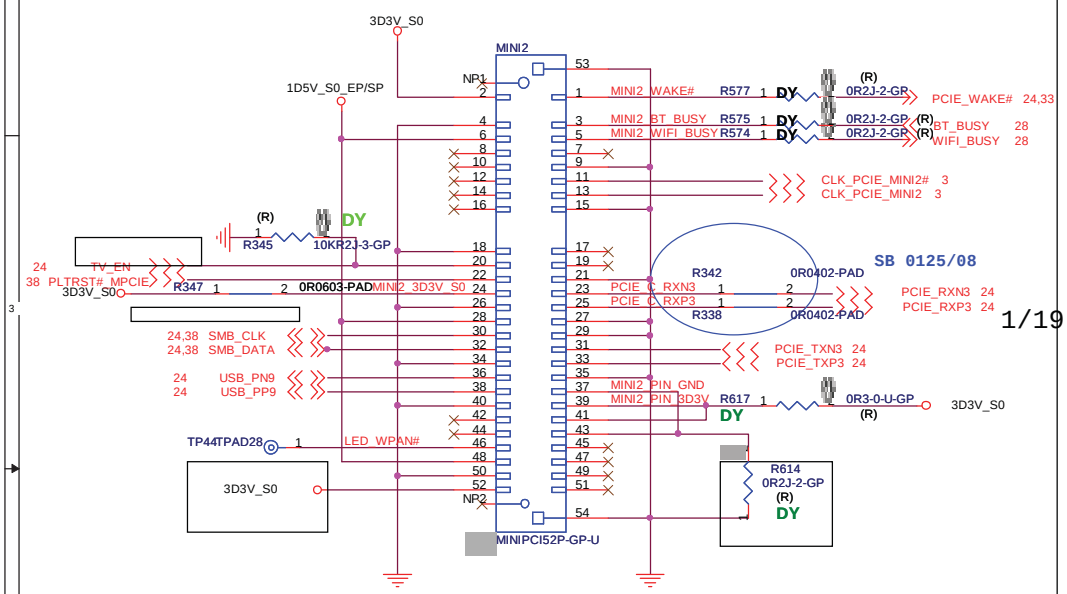
Title	R5C832/IEEE1394/SD/BT	
Size: B	Document Number: Bali	Rev: -1
Date: Friday, February 13, 2009	Sheet 30 of 52	

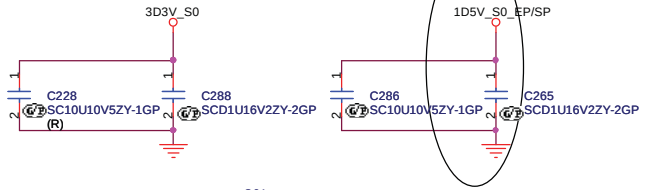
Mini PCI-E Connector

WWAN/TV-TUNER

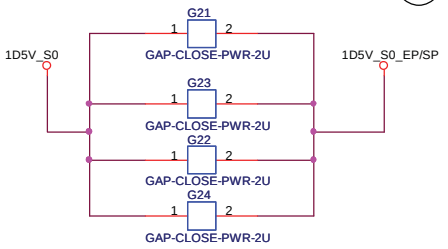


1/19 -2A change

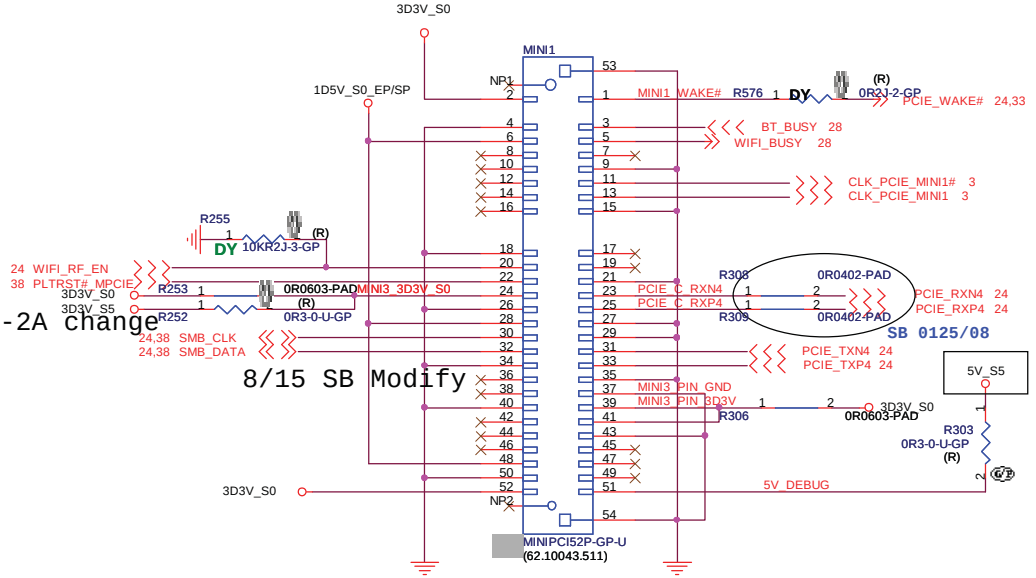
8/15 SB Modify



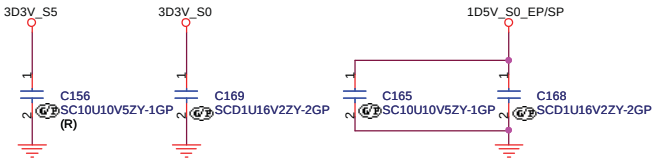
8/6 SB Remove



Wireless Card(Present support EP/SP)



Tyco 1759544-1 (62.10043.511)



8/6 SB Remove

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Title: MINI CARD CONN(1/2) .

Size	Document Number	Rev
B	Bali	-1

Date: Friday, February 13, 2009 Sheet 31 of 52

Remove

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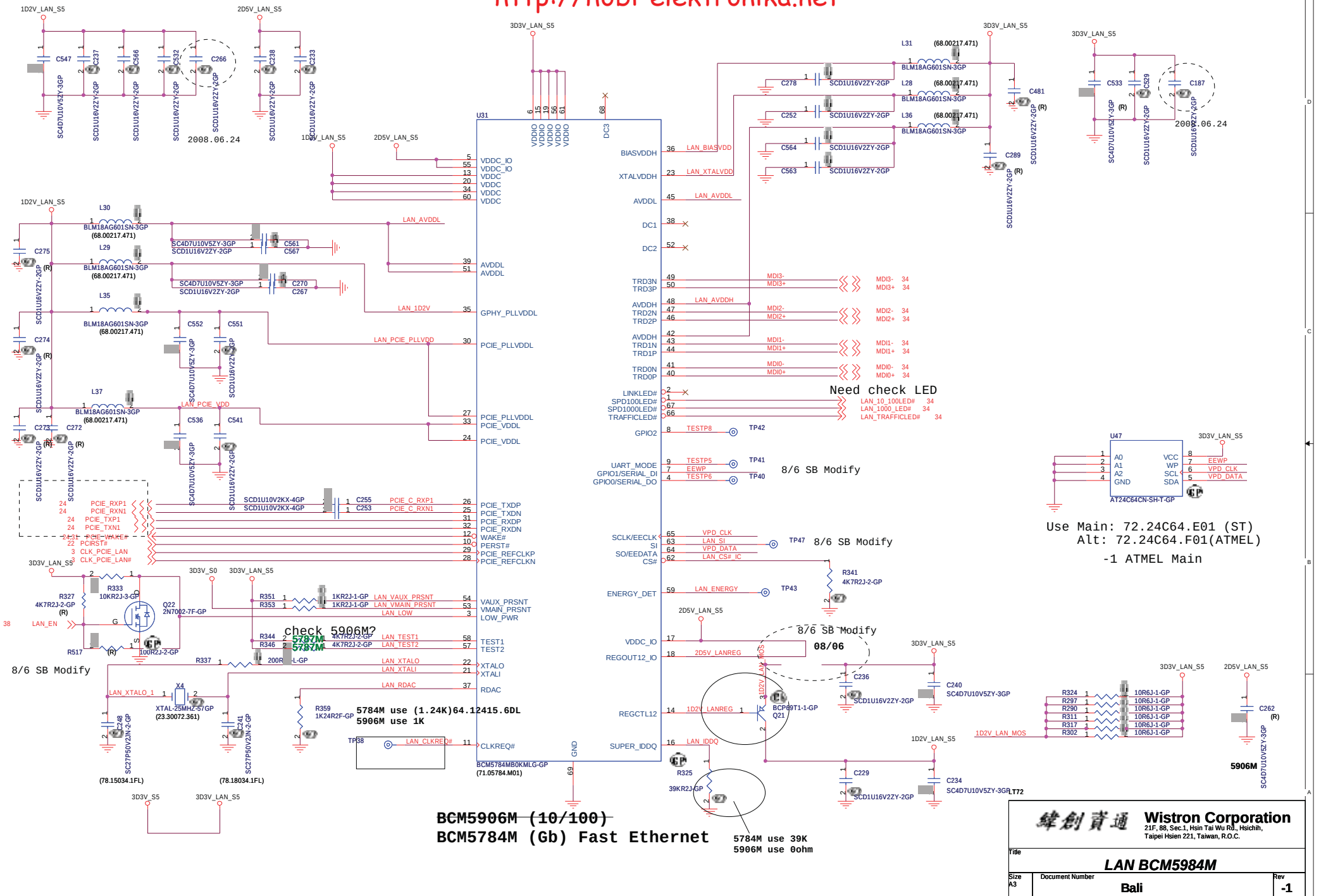
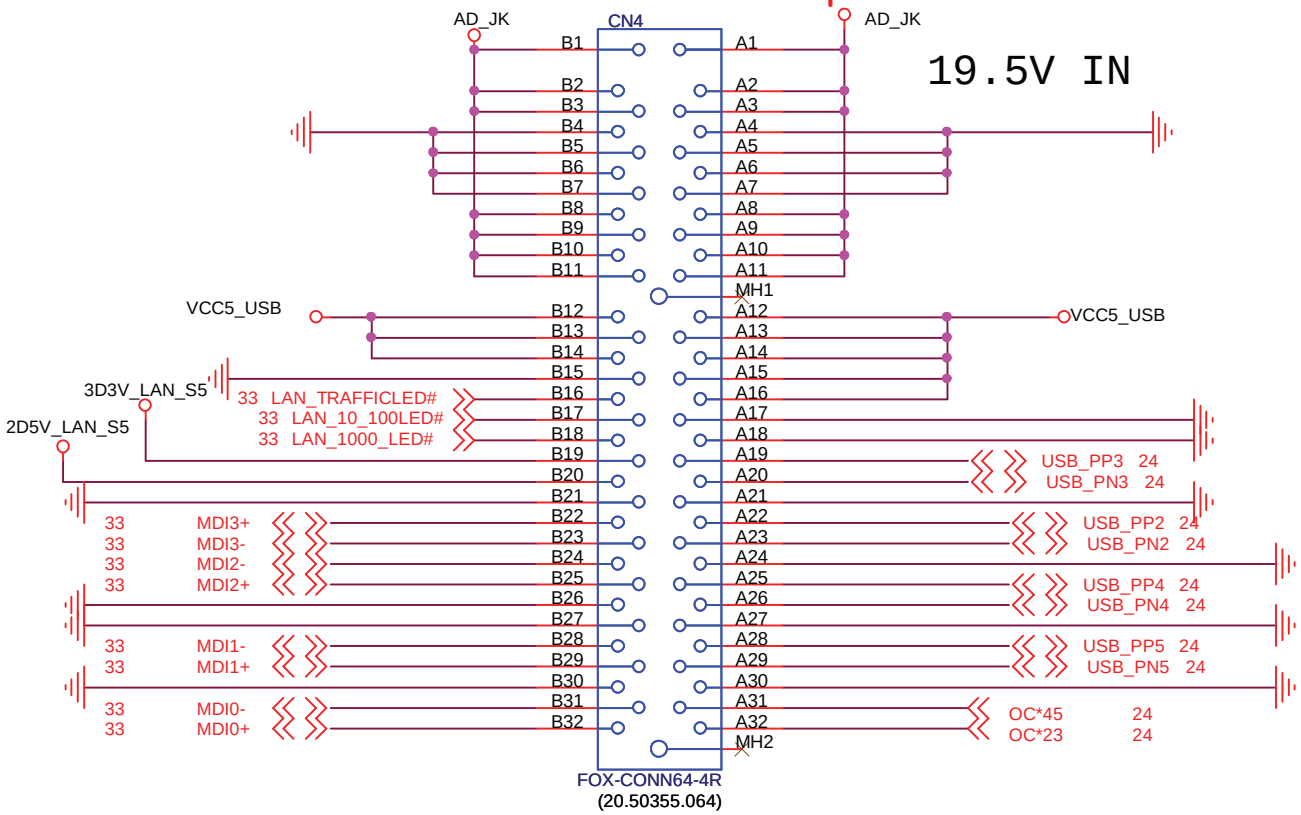
Title: MINIPCIE Robson		
Size: B	Document Number: Bali	Rev: SB
Date: Friday, February 13, 2009	Sheet 32 of 52	





Lotes: 20.50355.064
Tyco: (20.50246.064)

10/100M Lan Transformer

RJ45+RJ11=>
cheange Riser
Card

New Card =>
cheange to
Page 32

LT72

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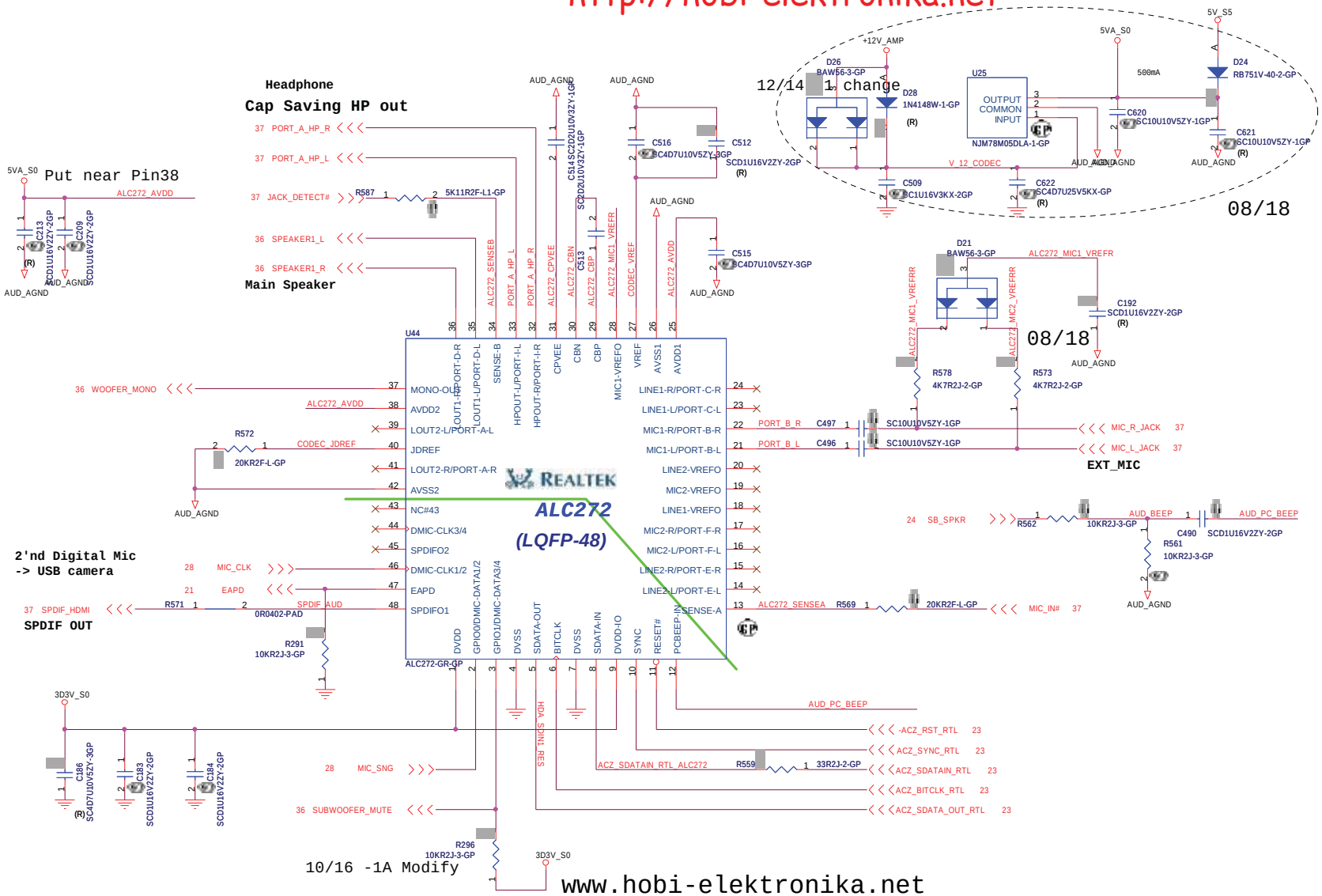
Title: ***Riser***		
Size: A	Document Number: **Bali**	Rev: **-1**
Date: Friday, February 13, 2009	Sheet 34 of 52	



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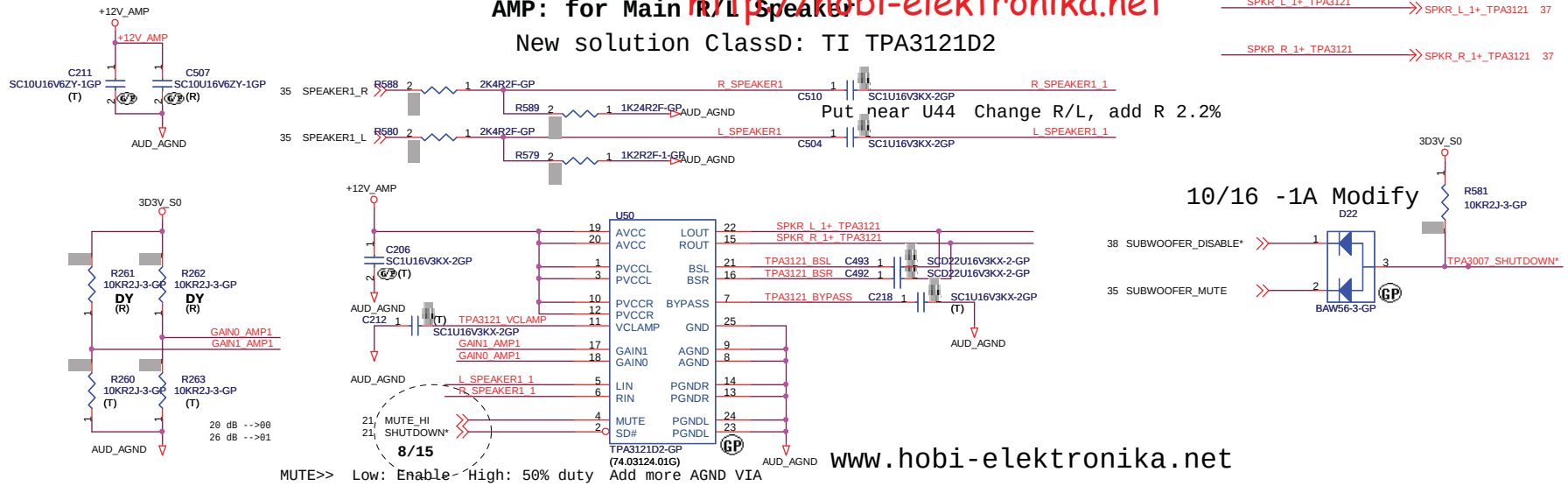
Title	AUDIO CODEC-ALC272
Size A3	Document Number: Bali
Rev	SB
Date: Friday, February 13, 2009	Sheet 35 of 52

AMP: for Main R/L Speaker

New solution ClassD: TI TPA3121D2

Put near U44 Change R/L, add R 2.2%

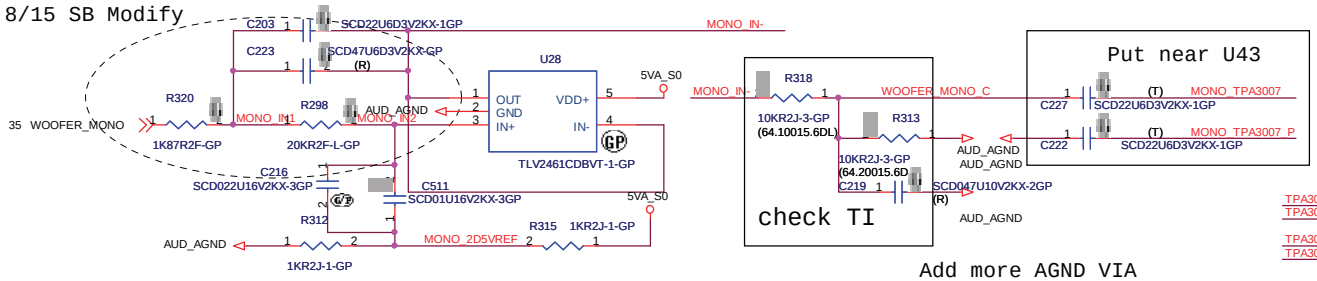
10/16 -1A Modify



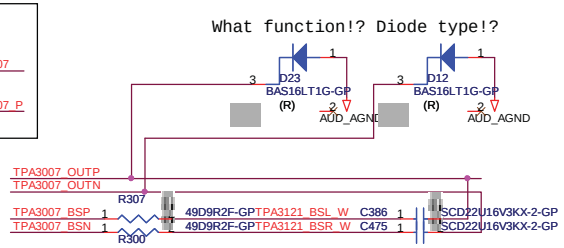
MUTE>> Low: Enable High: 50% duty Add more AGND VIA

www.hobi-elektronika.net

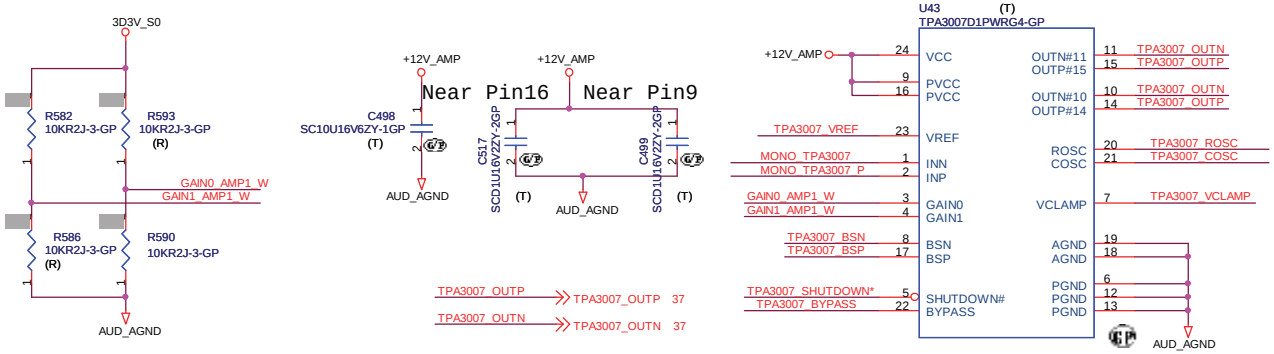
8/15 SB Modify

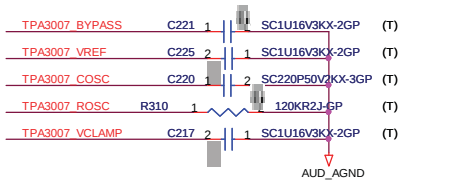


What function!? Diode type!?

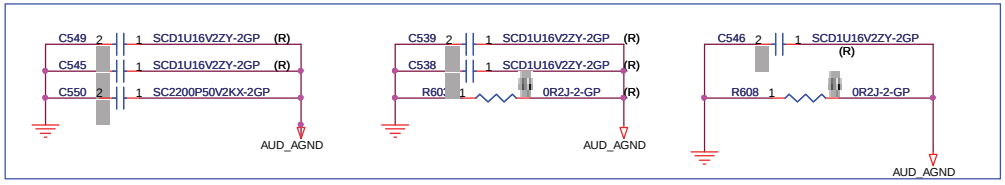


Add more AGND VIA





Speaker1_L FSOV 1.122V
Speaker1_R FSOV 1.107V
Woofer_MONO FSOV 1.089V



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Title: AUDIO AMP/SPEAKER

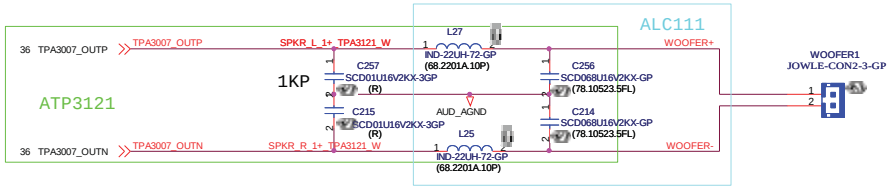
Size: Custom | Document Number: BAli | Rev: SB

Date: Friday, February 13, 2009 | Sheet 36 of 52

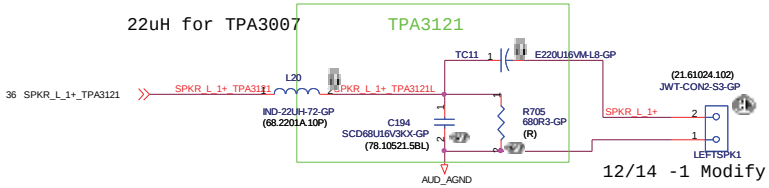
Sub Woofer

22uH for TPA3007
8.2uH for ALC111

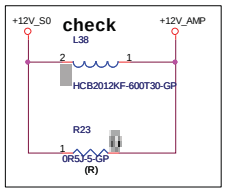
-1A change and need modiry in
-1B(78.10523.5FL)0402



22uH for TPA3007



12/14 -1 Modify



10uH for ALC111
68.22010.20B Youth
68.2201A.10P Chilism
68.2201A.10N Tai-Tech

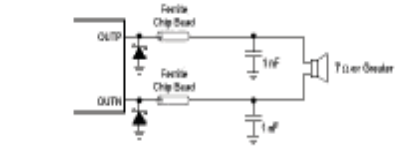


Figure 16. Typical Ferrite Chip Bead Filter (Chip bead example: Fair-Rite 2512067007Y3)

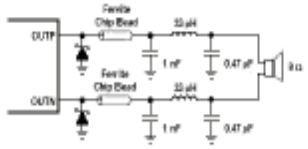
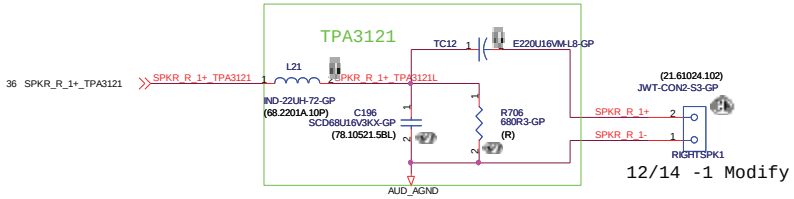


Figure 17. Typical LC Output Filter for 8-Ω Speaker, Cutoff Frequency of 41 kHz

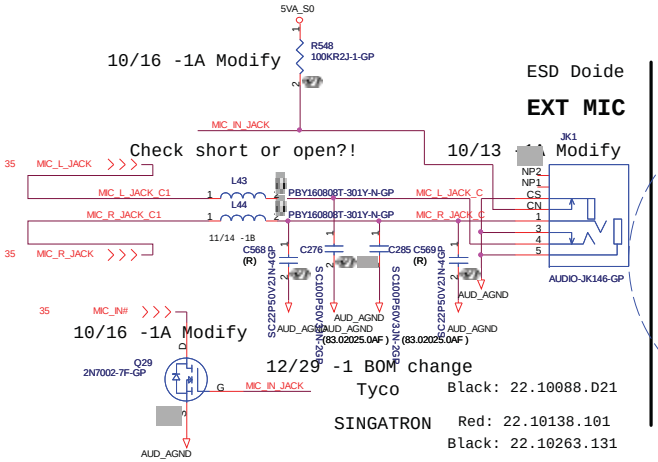
22uH
68.22010.20B YOUTH (remove)
68.2201A.10P Chilisin
68.2201A.10N TAI-TECH

220uF
CHEMICON 09.2271D.L16
SANYU 09.2271D.L13
Rubycon 09.2271D.J8L



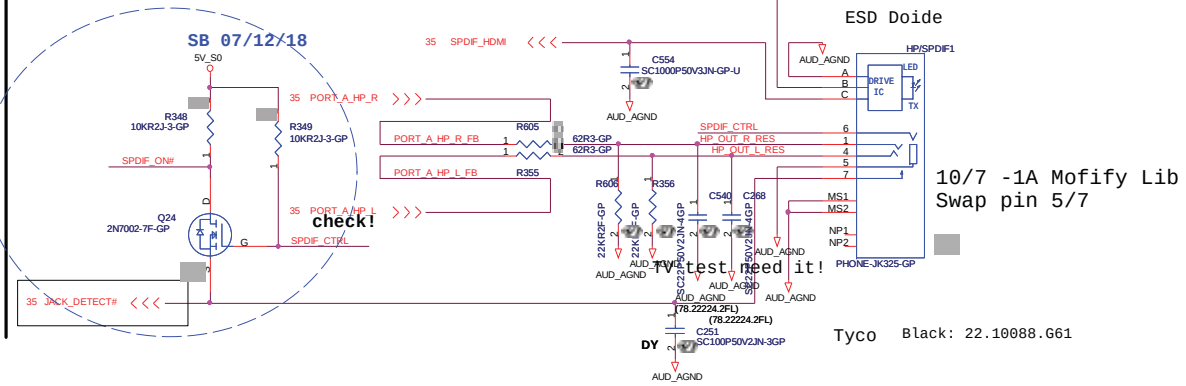
12/14 -1 Modify

10/16 -1A Modify

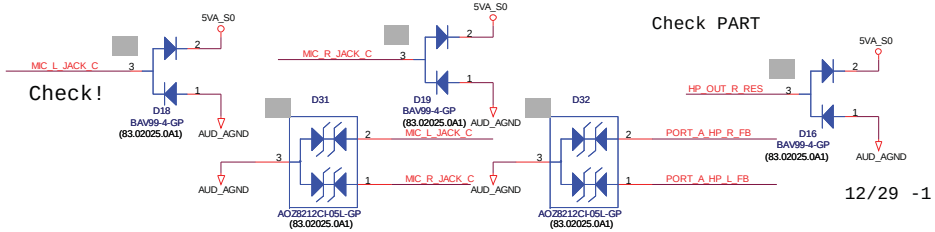


HP_OUT/ LINE_OUT

Power on S0



10/7 -1A Mofify Lib
Swap pin 5/7



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Title: AUDIO HP_JK/ MIC_JK/SUBWOF

Size	Document Number	Rev
Custom	Bali	SB

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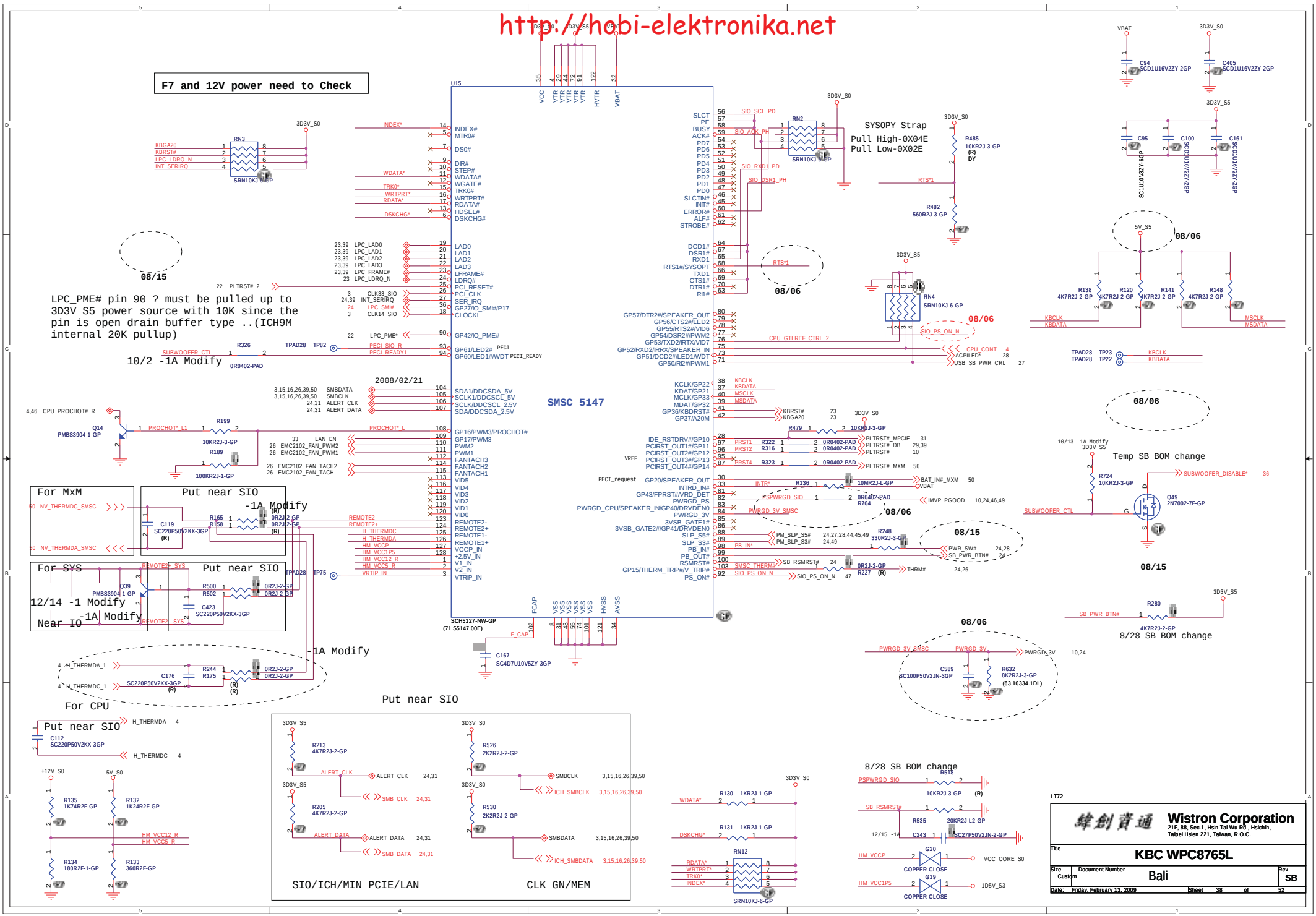


Touch button

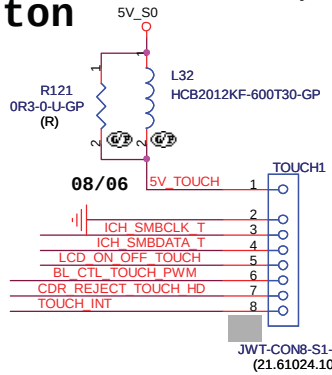
9/25 -1A Modify

LCD_ON_OFF_TOUCH
Power ON: High
Touch: Low/Hihg/Low...

BL_CTL_TOUCH_PWM
PWM duty for Inverter Board

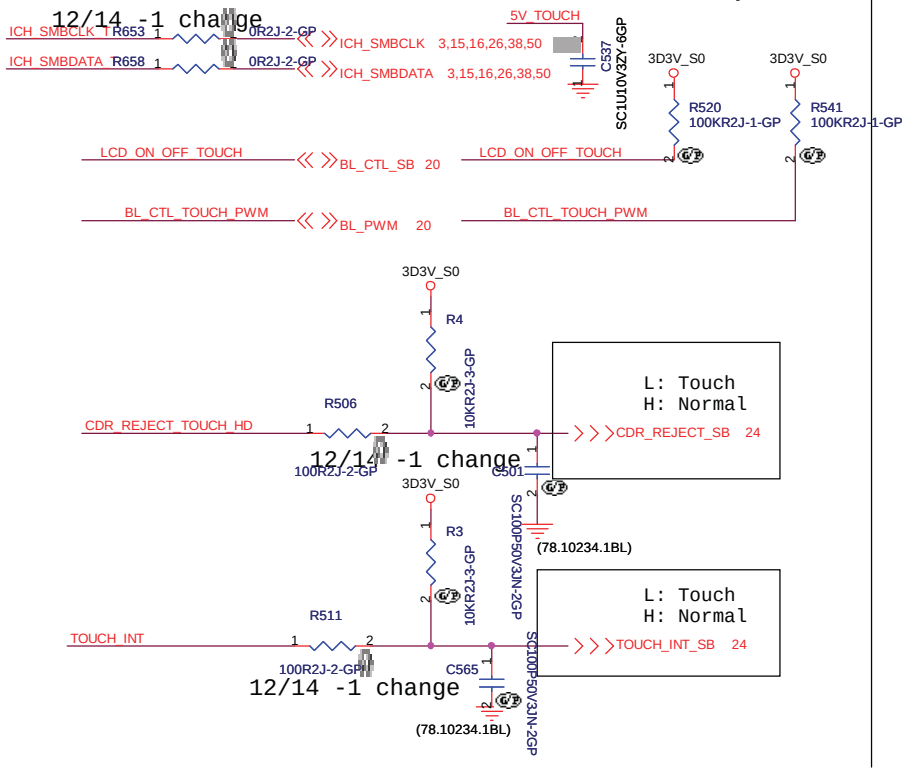
CDR_REFECT_TOUCH_HD
L: Touch
H: Normal

TOUCH_INT
L: Touch any key
H: Normal



9/25 -1A Modify

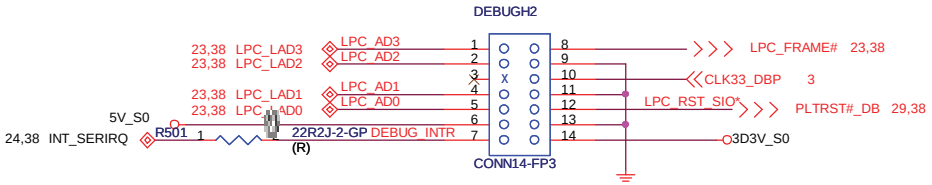
12/14 -1 change



12/14 -1 change

12/14 -1 change

debug header

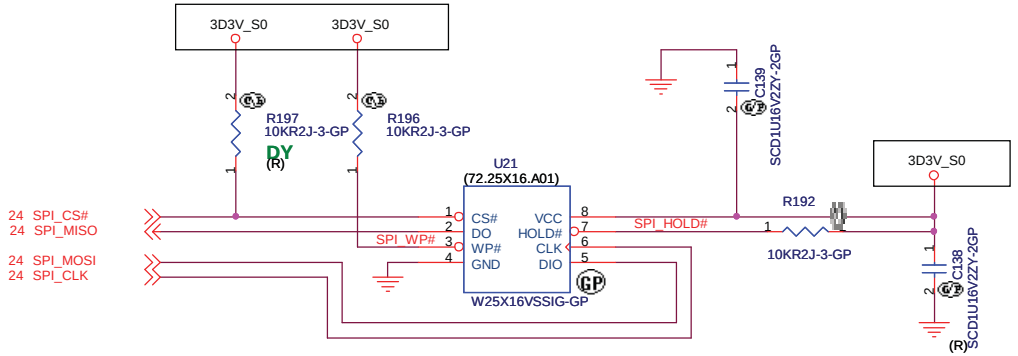


(Main 21.62704.207(low) Alt 21.62582.207(high))

21.62704.207
David HEAD ML
2R14P(-1#6)ST
14452360
(high2.56+4mm)

SPI ROM for System & KBC

SPI Socket: 62.10089.011



1. Main Source: 72.25X16.A01(Winbond 16Mb)
2. 2nd Source: 72.25165.A01 (MXIC 16Mb)
3. 3ns source: 72.25016.A01 (SST -50 16MB)
72.25016.D01 (SST-75 16Mb)

12/14 -1 Remove BIOS socket

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Title: ***Keyboard /Touch Pad***

Size	Document Number	Rev
Custom	Bali	-1

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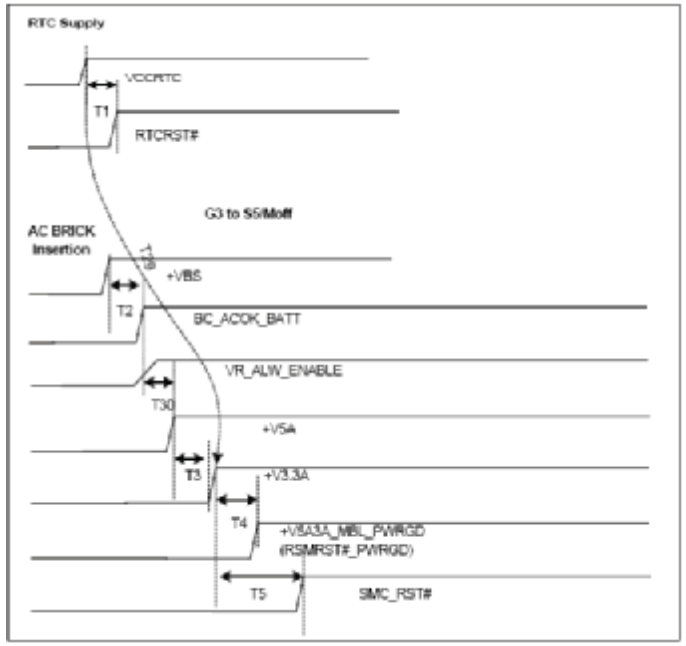
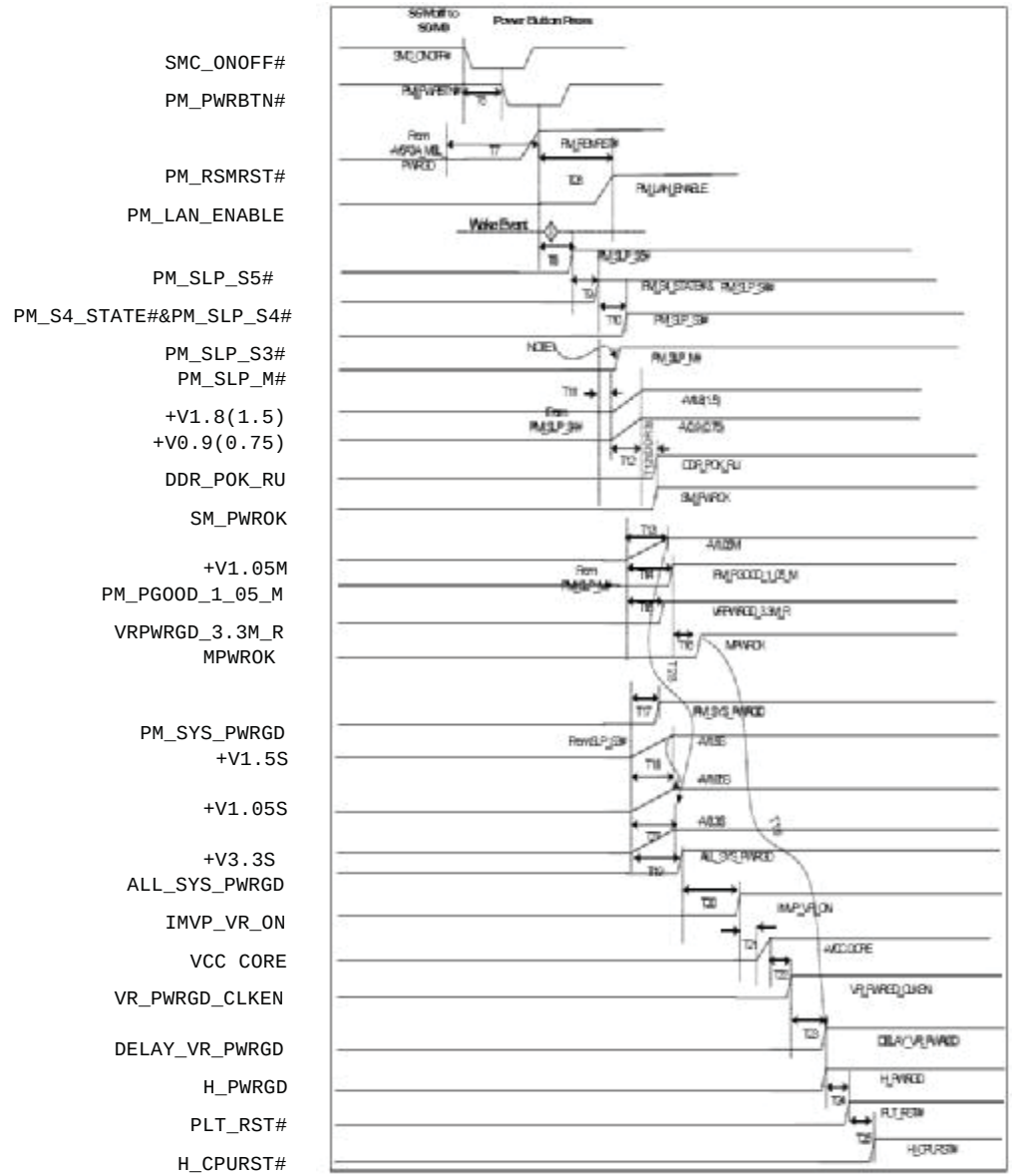
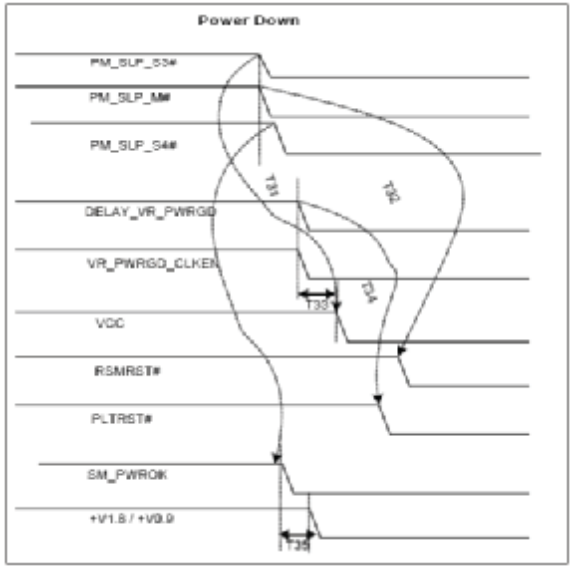
Standby Power ON



Power ON



Power DOWN



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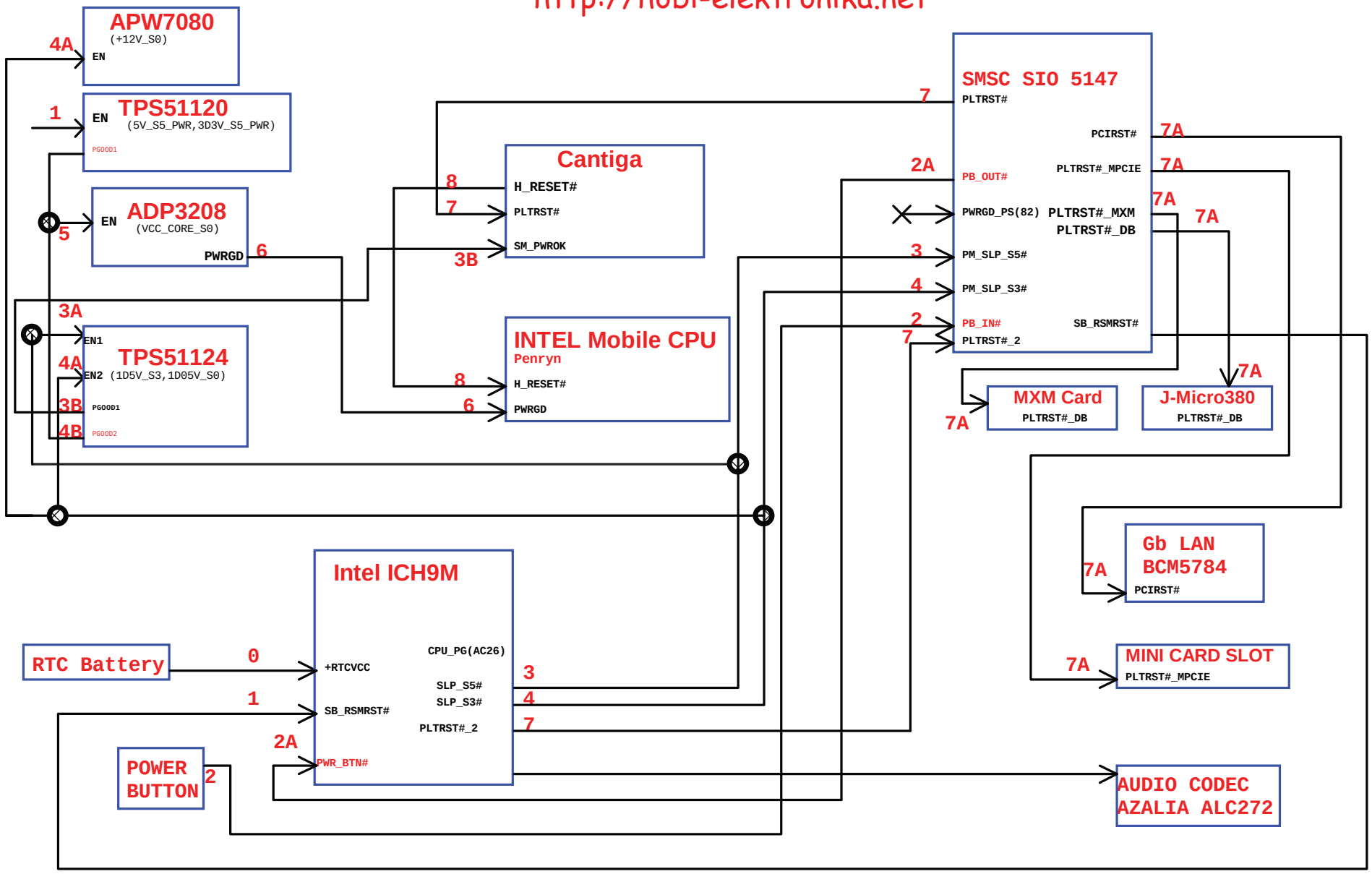
Title: G-sensor / SPI / LEDs		
Size: Custom	Document Number: Bali	Rev: SA
Date: Friday, February 13, 2009	Sheet 40 of 52	



RESET/POWER GOOD MAP

PGOOD(39)

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Title: FWH and Debug

Size: Custom | Document Number: Bali | Rev: SA

Date: Friday, February 13, 2009 | Sheet 41 of 52

CPU_CORE
ADP3207A

H_VID0
H_VID1
H_VID2
H_VID3
H_VID4
H_VID5
H_VID6

VID Setting
VID0(I / 1.05V)
VID1(I / 1.05V)
VID2(I / 1.05V)
VID3(I / 1.05V)
VID4(I / 1.05V)
VID5(I / 1.05V)
VID6(I / 1.05V)

Output Signal
PGOOD(OD / 3.3V) → VGATE

Output Power
VCC_CORE_PWR(O) → VCC_CORE_S0(Imax=55A)

PWR_GD

Input Signal
VR_ON (I / 3.3V)

VCC_SENSE
VSS_SENSE

Voltage Sense
VSEN
RTN(I / Vcore)

DCBATOUT
5V_S0
3D3V_S0

Input Power
VCC(I)
VCC(I)
VCC(I)

3.3V/5V
TPS51120

S5PWR_ENABLE
S5PWR_ENABLE
DCBATOUT_51120

Input Signal
51120_EN2 FOR 3.3V
51120_EN1 FOR 5.0V
VIN

Output Signal
PGOUT(OD / 5V) → Pull High (3D3V)

DCBATOUT_51120
5V_S5

Input Power
VIN
REG5V_IN(I / 5V)

Output Power
5V(O) → 5V (6A)
3D3V(O) → 3D3V (6A)

1D8V_S3
G966

3D3V_S5
5V_S5
PM_SLP_S5#

VIN
VCNTL
S3
VOUT → 1D8V_S3 (300mA)

DDR_0D75V_S3
TPS51100

1D5V_S3
5V_S5
DDR_VREF_S0_EN

VIN
VCNTL
S3
VOUT → 0D75V_S3 (1A)

1D5V/1D05V
TI TPS51124

S5PWR_ENABLE
PM_SLP_S5#

Input Signal
EN1 (I / 3.3V)
EN2 (I / 3.3V)

Output Signal
PG1(OD / 1D8V) → 1D5_S3_PG
PG2(OD /2D5V) → 1D05_S0_PG

Input Power
DCBATOUT
5V_S5
V+
VCC (I / 5V)

Output Power
1D05V(O) → 1D05V_S0 (20A)
1D8V(O) → 1D5V_S3 (10A)

Charger
MAX8725

CHARGE_OFF
BT_TH
BAT+SENSE
BT_SCL_5
BT_SDA_5
FLASH_GPIO1
FLASH_GPIO2
AC_IN
AD+

Input Signal
CLS (I / 3.3V)
THM (I / 3.3V)
BATT (I / 3.3V)
SCL (IO / 5V)
SDA (IO / 5V)
RESET#/PB5 (I/5V)
PB0/MOSI/AIN0
PB0/MOSI/AIN0

Input Power
DCIN (I)

Output Signal
LDO (O / 5.4V) → AD_IN
XTAL2/PB4 (O/5V) → CHARGE_LED#
XTAL1/PB3 (O/5V) → BL2#

Output Power
VCC (O) → DCBATOUT
VCC (O) → BT+

Adapter

AD_OFF
5V_AUX_S5

Input Signal (I)
Output Signal (O) → AD_IN

Input Power
VCC(I)
VCC(I)

Output Power
VCC(O) → AD+

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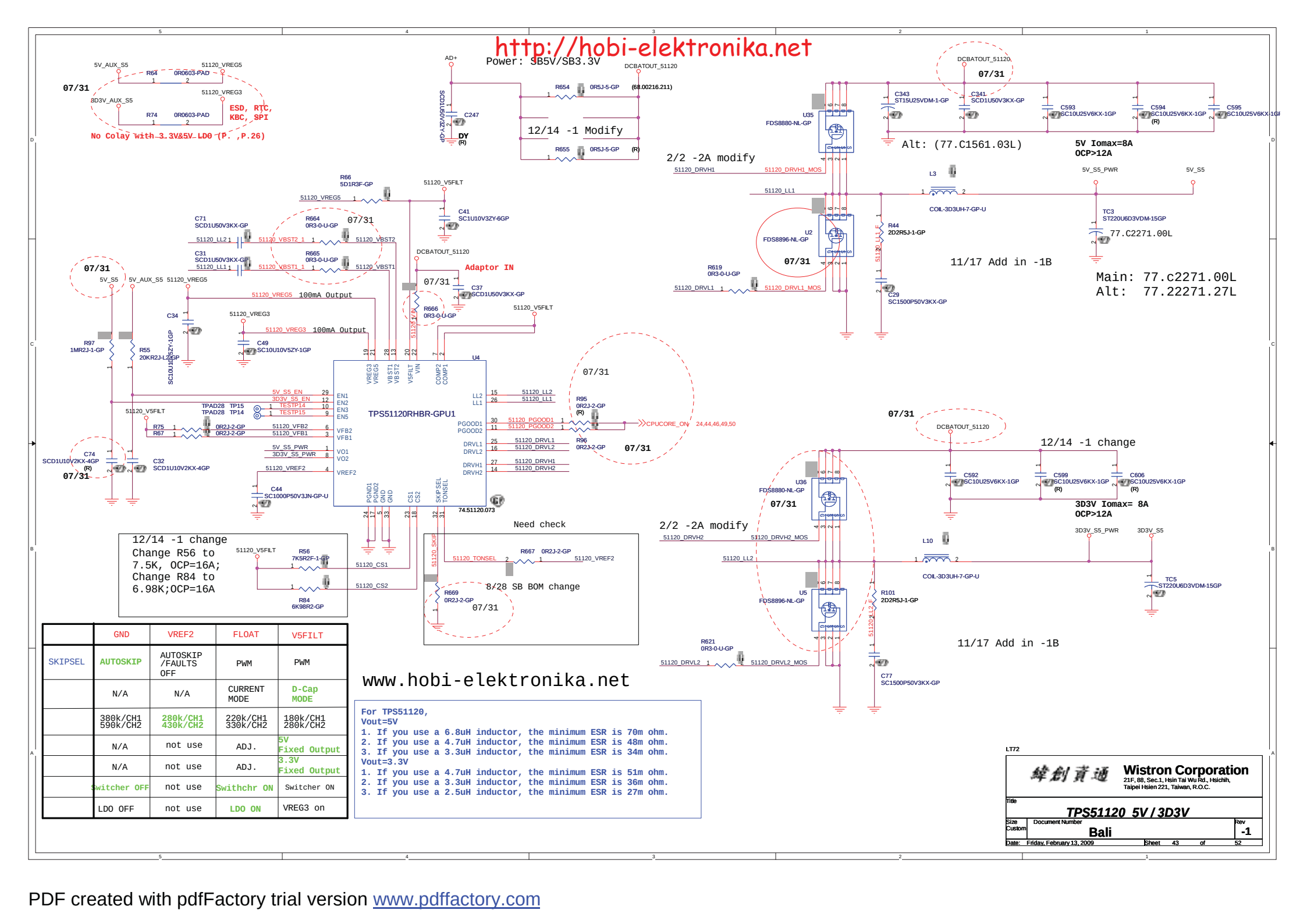
Title: POWER BLOCK DIAGRAM

Size: A3 | Document Number: Bali | Rev: Bali

Date: Friday, February 13, 2009 | Sheet 42 of 52



	GND	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP /FAULTS OFF	PWM	PWM
	N/A	N/A	CURRENT MODE	D-Cap MODE
	380k/CH1 590k/CH2	280k/CH1 430k/CH2	220k/CH1 330k/CH2	180k/CH1 280k/CH2
	N/A	not use	ADJ.	5V Fixed Output
	N/A	not use	ADJ.	3.3V Fixed Output
	Switcher OFF	not use	Swithchr ON	Switcher ON
	LDO OFF	not use	LDO ON	VREG3 on

For TPS51120,
Vout=5V
1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.
Vout=3.3V
1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

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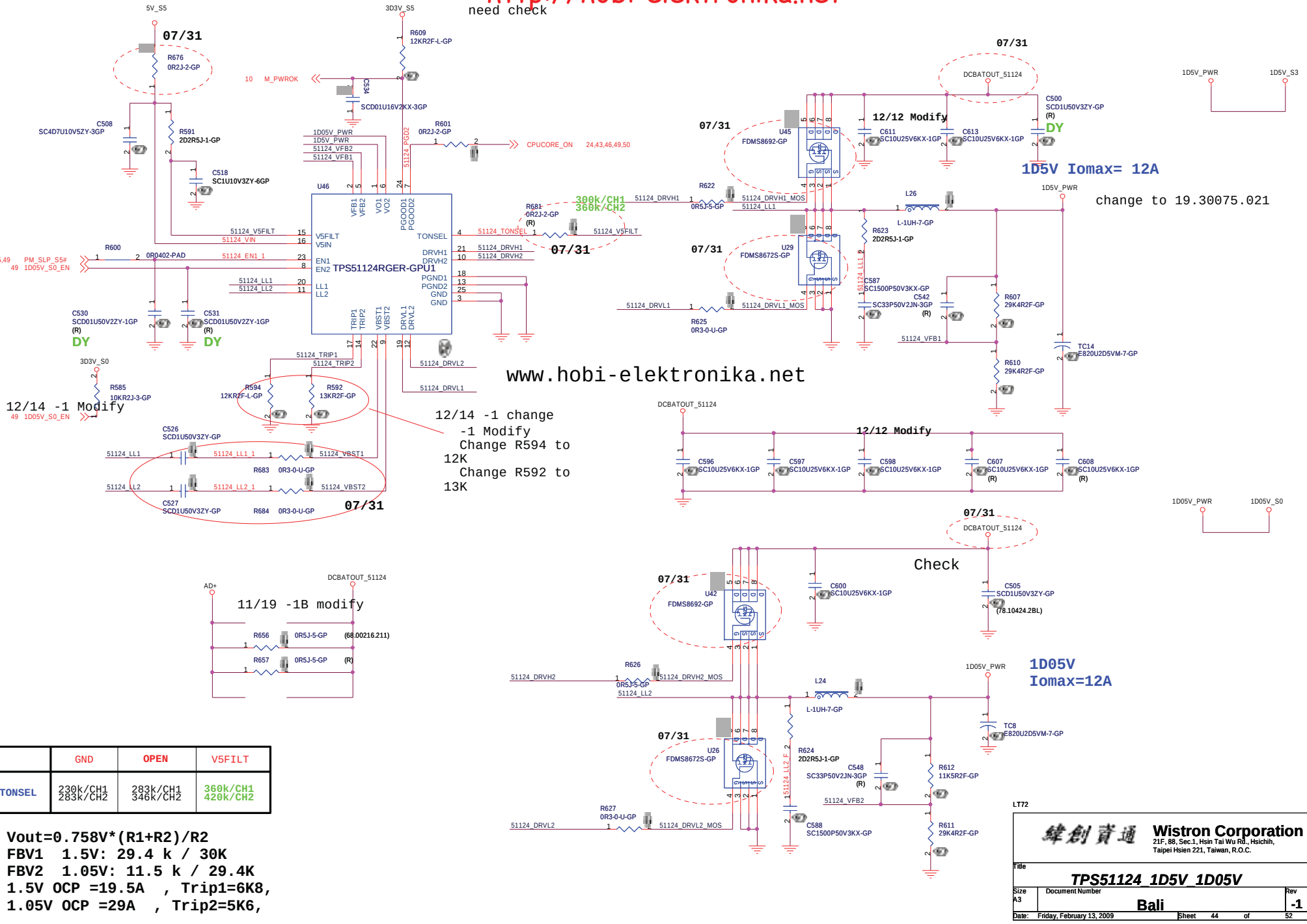
Title: TPS51120 5V / 3D3V

Size: Custom | Document Number: Bali | Rev: -1

Date: Friday, February 13, 2009 | Sheet 43 of 52

need check



	GND	OPEN	V5FILT
TONSEL	230k/CH1 283k/CH2	283k/CH1 346k/CH2	360k/CH1 420k/CH2

Vout=0.758V*(R1+R2)/R2
FBV1 1.5V: 29.4 k / 30K
FBV2 1.05V: 11.5 k / 29.4K
1.5V OCP =19.5A , Trip1=6K8,
1.05V OCP =29A , Trip2=5K6,

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Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51124_1D5V_1D05V

Size	Document Number	Rev
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Date: Friday, February 13, 2009 Sheet 44 of 52

9/25 -1A Remove

1D8V_S3_5336 — 1D8V_S3

3D3V_S5 -> 1.8V_S3
1D8V
Iomax=300mA

3D3V_S5, C624 SCD1U16V2ZY-2GP (R), R725 1KR2F-3-GP, R726 1KR2F-1-GP, C625 SCD1U16V2ZY-2GP (R), C623 SC4D7U10V5ZY-3GP, APL5331_REF, 1D8V_S3_5336, **1D8V/300mA**, U52 (74.05336.031) APL5331KAC-TRLGP (VIN, GND, VREF, VOUT, NC#8, NC#7, VCNTL, NC#5), C626 SC10U10V5ZY-1GP, 5V_S5, C544 SCD1U16V2ZY-2GP

5V_S5, R727 10KR2J-3-GP, SLP_S5*_INV, APL5331_REF, Q58 2N7002-7F-GP, Q61 2N7002-7F-GP, 24,27,28,38,44,49 PM_SLP_S5#

PM_SLP_S5#
S3/S0: High
S5: Low

SLP_S5*_INV
S3/S0: Low
S5:High

S3/S0: EN
S5: Low

0D75V
Iomax=1A

5V_S5, C292 SC1U10V3ZY-6GP, U34 TPS51100DGQ-1-GP (VIN, S5, GND, S3, VTTREF, VDDQSNS, VLDOIN, VTT, PGND, VTTSNS), 1D5V_S3, C290 SC10U10V5ZY-1GP, 0D75V_PWR, 0D75V_S3, R362 0R2J-2-GP, R363 0R2J-2-GP, R361 (R) 0R2J-2-GP, 24,27,28,38,44,49 PM_SLP_S5#, 49 PM_SLP_S3_1#, 5110_PMSLPS4#, 5110_PMSLPS3#, DDR_VREF_S3, C283 SCDU16V2ZY-2GP, C280 SC10U10V5ZY-1GP (R), C287 SC10U10V5ZY-1GP (R), C281 SC10U10V5ZY-1GP

DY

U22 **0518** APL1117VC-GP (ADJ/GND, OUT, IN)

check current
3D3V -> 1.8V

3D3V_S0, C146 SC10U10V5ZY-1GP (R), C149 SCD1U16V2ZY-2GP, VCC3_3SBREF, 1D8V_S0, **0518**, R242 120R3F-L-GP, R257 54D9R2F-L1-GP, C166 SC10U10V5ZY-1GP

9/25 -1A Add

1D8V_1084, R45 0R5J-5-GP (R), 1D8V_S0

U48 APL1084GC-TRL-GP (R) (ADJ, VOUT, VIN)

07/31

3D3V_S0, 1D8V_1084, Need check, 1D8V_1084_APL1084, C616 SC10U10V5ZY-1GP (R), APL1084_ADJ, R697 120R3F-L-GP (R), R698 54D9R2F-L1-GP (R), C614 SC10U10V5ZY-1GP (R), C615 SC10U10V5ZY-1GP (R)

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Title: ***LDO 1D8V / 0D75V***

Size	Document Number	Rev
A3	Bali	-1A

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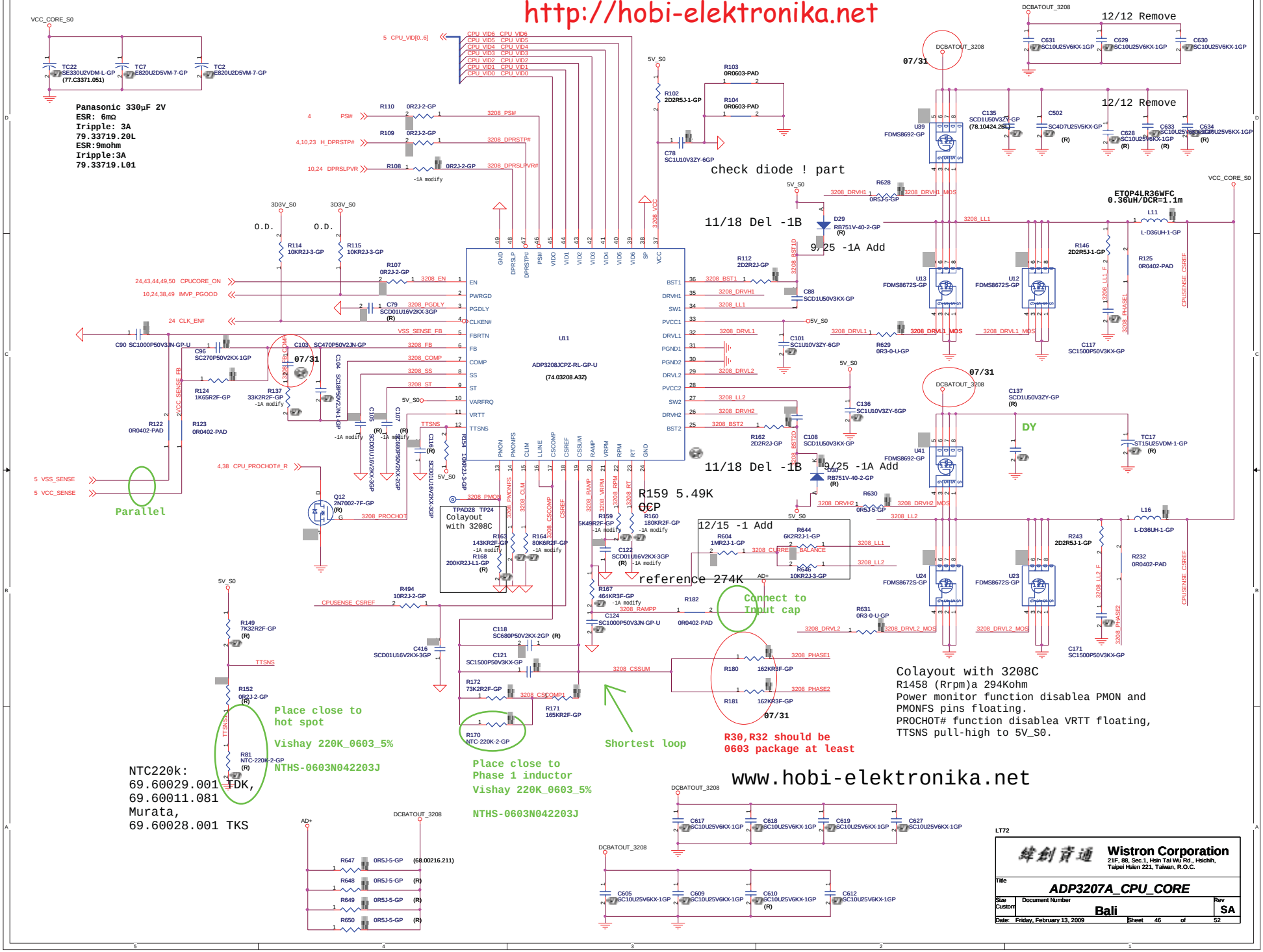
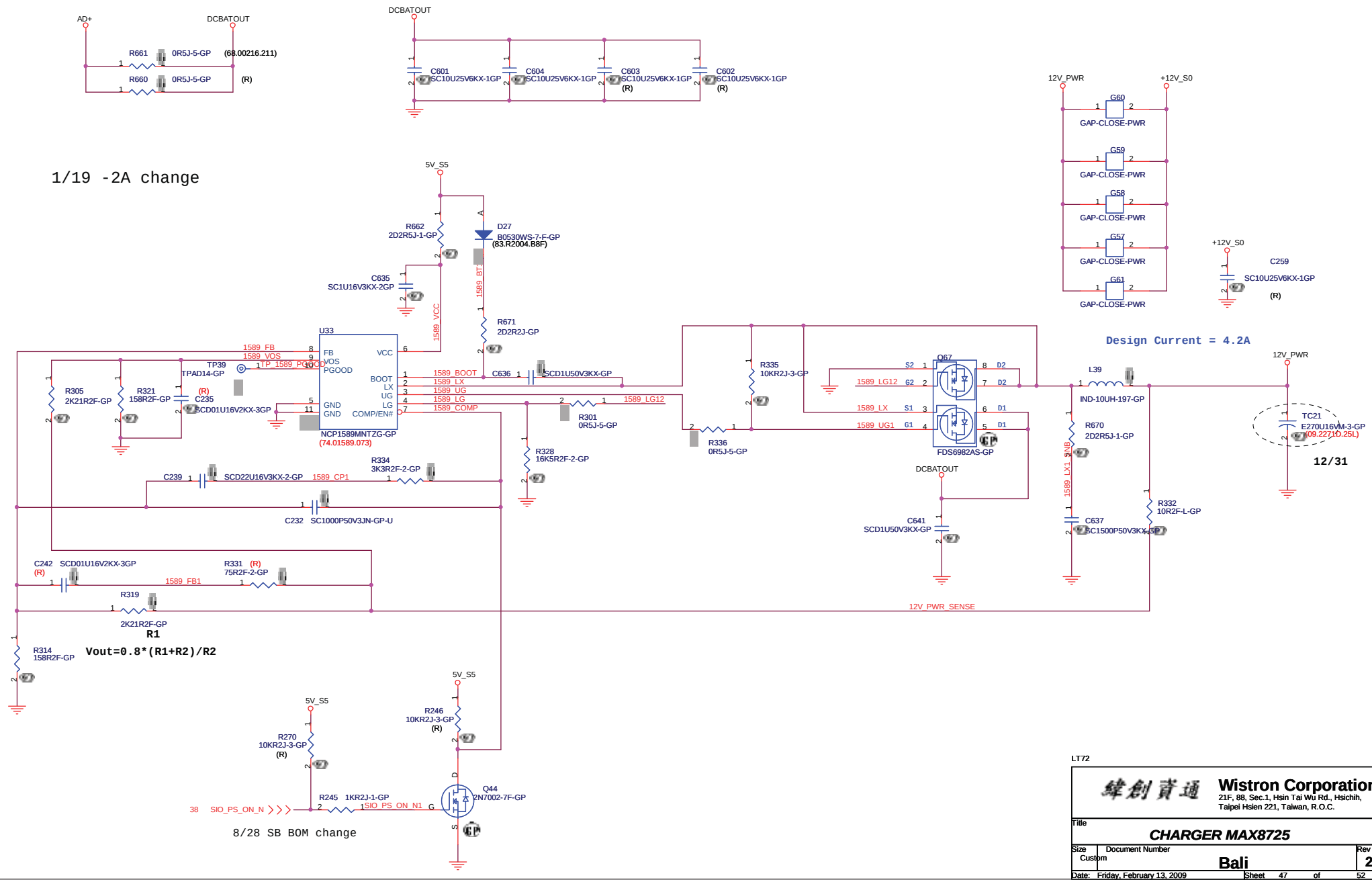
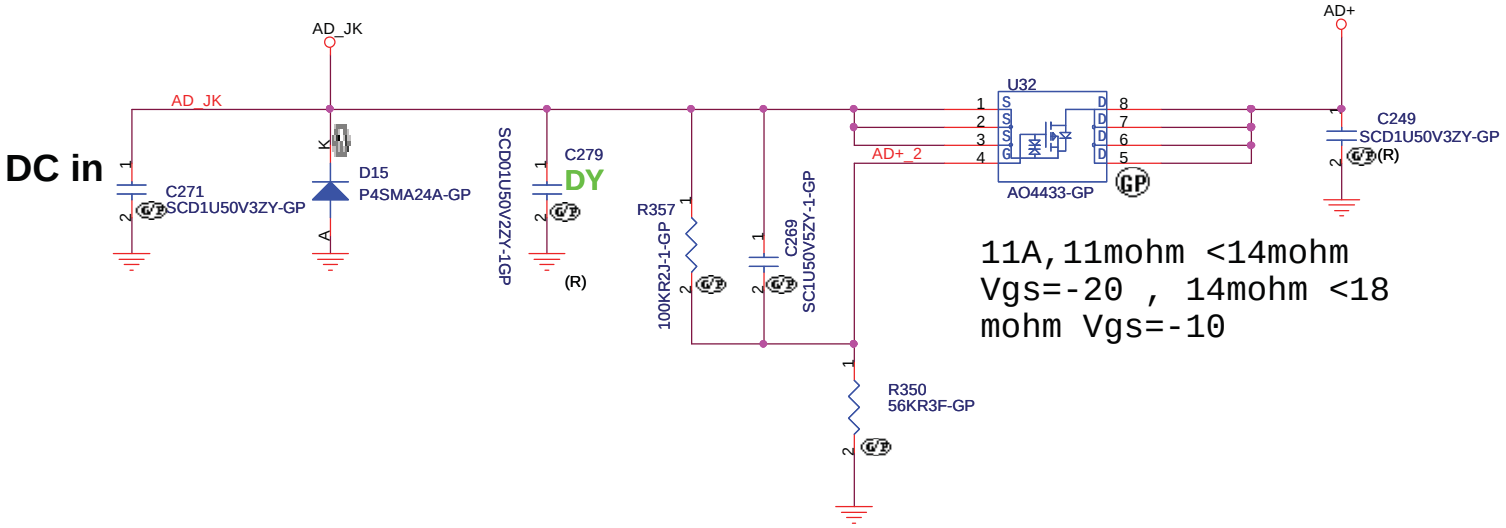
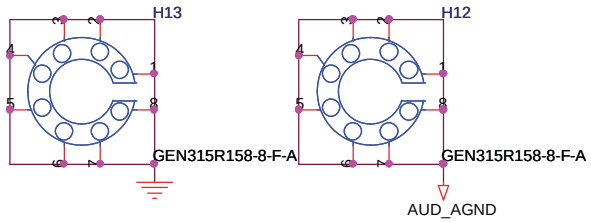


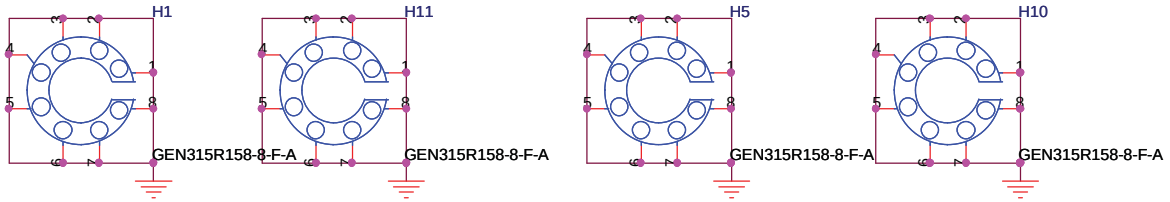


Adaptor in to generate DCBATOUT

Add alternate 84.01403.A37







緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ADT&BATT CONN		
Size: A4	Document Number: Bali	Rev: SA
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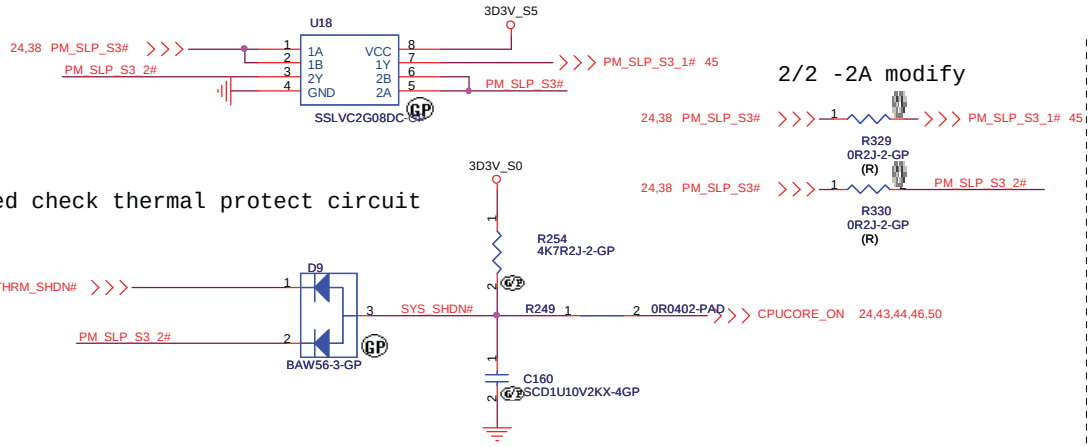
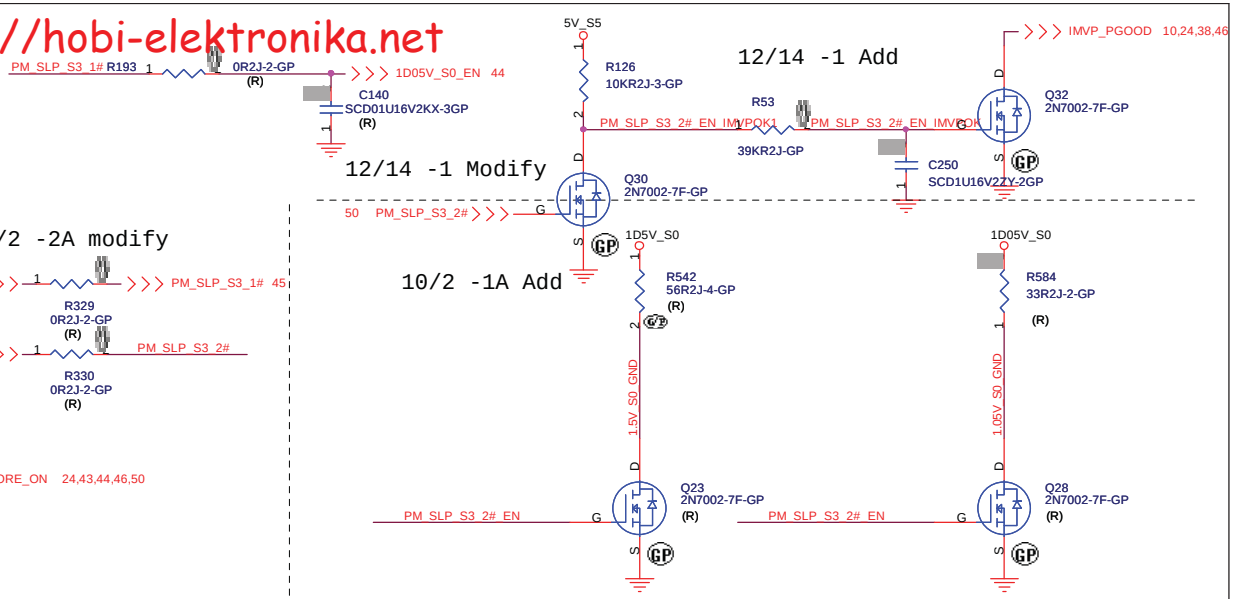
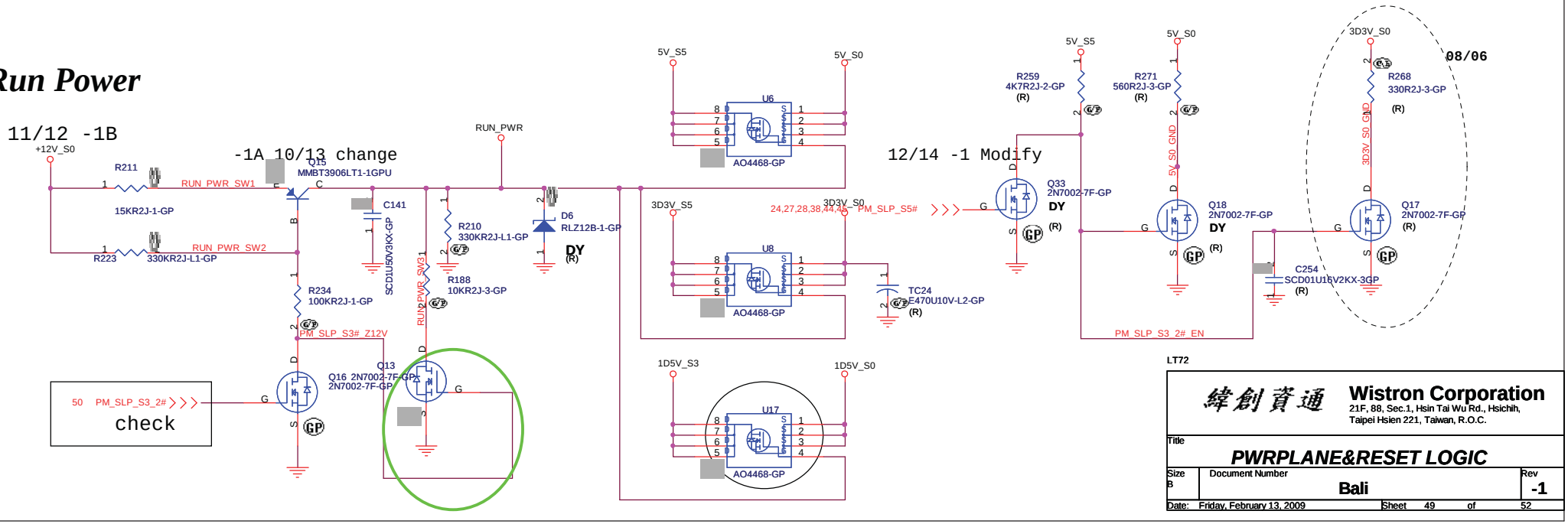
Reset Logic

need modify for DT thermal protect





Run Power



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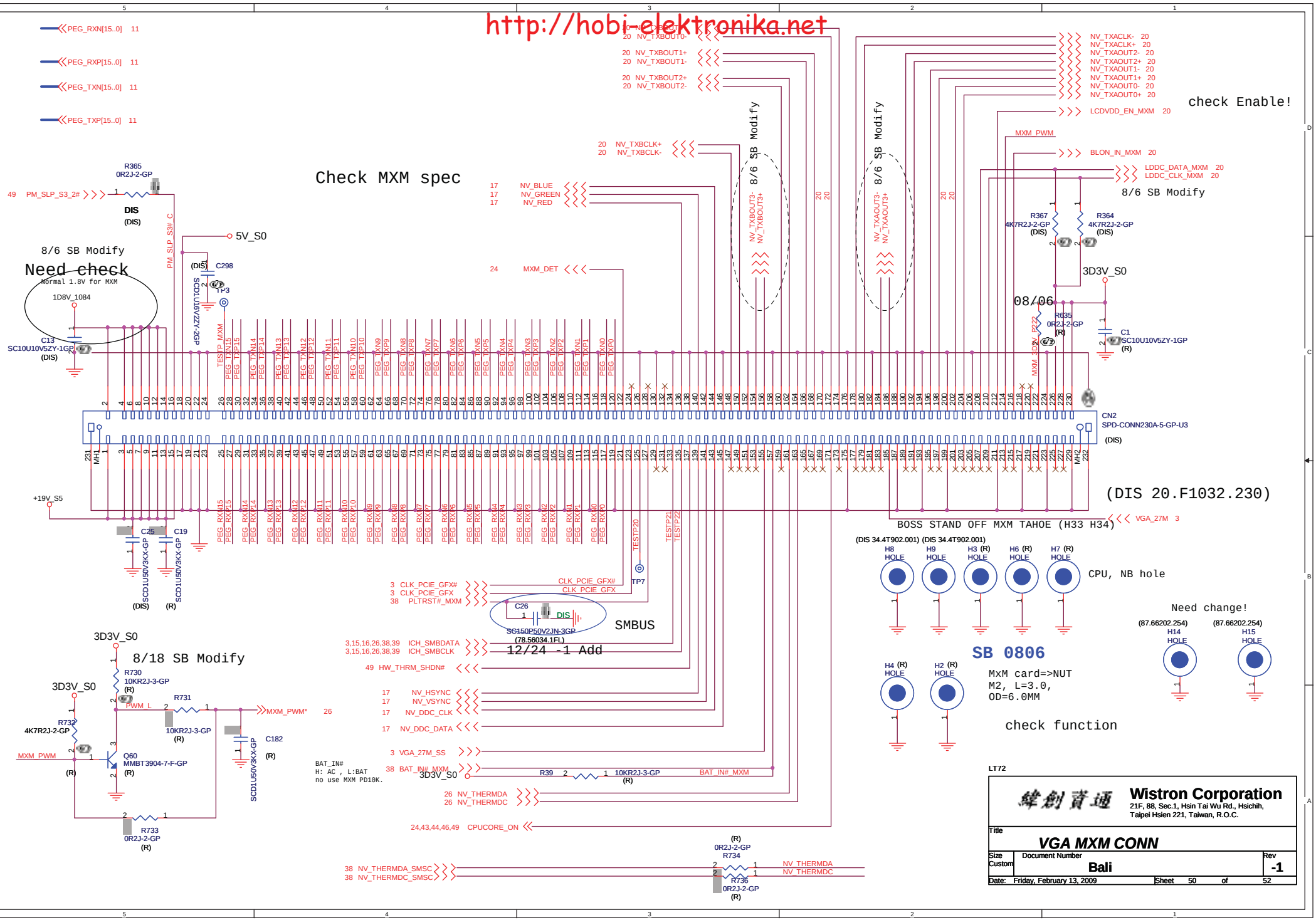
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***PWRPLANE&RESET LOGIC***	
Size B	Document Number **Bali**	Rev **-1**
Date: Friday, February 13, 2009	Sheet 49 of 52	



Vendor check	Result	RD check	Source	Schmeatic	
			NB	O	01_BLOCK DIAGRAM
			NB	Δ	02_Table of Content
ICS ?	Modify ICS 6/25,26		New	O	03_Clock Gen CY28647->Realtek (need check solution)
			NB	O	04_Penryn(1/3)-AGTL+
Intel (1)First FB 6/23	Modify in 6/24		NB	O	05_Penryn(2/3)-PWR
			NB	O	06_Penryn(3/3)-GND&Bypass
			NB	O	07_Penryn(4/4)-XDP PORT
			NB	O	08_Cantiga(1)-HOST I/F
			NB	O	09_Cantiga(2)-DDR3 A/B CH
			NB	O	10_Cantiga(3)-DMI/PM/CFG
			NB	O	11_Cantiga(4)-VGA/LVDS/TV
			NB	O	12_Cantiga(5)-PWR1
			NB	O	13_Cantiga(6)-PWR2
			NB	O	14_Cantiga(7)-GND
			NB	O	15_DDRIII-SODIMM SLOT1
			NB	O	16_DDRIII-SODIMM SLOT2
		YAMA		O	17_CRT CONN-> No need
		remove			18_VGA IN(1/2)-RGB IN->No need
		remove			19_VGA IN(2/2)-NT68665H->No nee
		NB/NEW		O	20_LCD CNN/ Lid SW
		remove			21_HDMI->no need
			NB	O	22_ICH9(1/4)-PCI /INT
			NB	O	23_ICH9(2/4) LAN/HD/IDE/LPC/RTC
	Modify in 6/20		NB	O	24_ICH9(3/4) PM,USB,GPIO
			NB	O	25_ICH9(4/4) POWER&GND
			New	O	26_THERMAL EMC2102-> Fan
			New	O	27_USB I/O / Modem
			New	O	28_HD/CDROM I/F+USB device
JM380 6/19	Modify 6/20		New	O	29_R5C833/PCI(1/2)-> Jmicon Solution
			New	O	30_R5C833/IEEE1394/SD/BT(2/2)
			NB	O	31_MINI CARD CONN(1,2)
		remove			32_New Card
Lan 6/26	Modify 6/26		New	Δ	33_LAN_BCM5906M Need check Spec
			New	O	34_LAN/New Card->Riser Card
Realtek 6/20,23	Modify 6/22,24		New	O	35_AUDIO CODEC ALC888S-> ALC262
			New	O	36_AUDIO AMP/Speaker Need check Amplify
TI 6/18-24	Modify 6/25		New	O	37_AUDIO HP_JK/ MIC_JK/SUBWOF Need check Amplify
SMSC 6/20	Modify 6/27		New	O	38_KBC WPCE8765C-> SIO
			New	O	39_KB /TP /Lanuch Board
				No	40_CIR / SPI ROM / LEDs-> Power Sequence
				No	41_SWITCHs / DEBUG-> Reset
		NB/New		No	42_Power Block Diagram
TI 6/17	Modify 6/18		NB	O	43_PW_5V_S5/3V_S5(TPS51120)
			NB	O	44_PW1D05V_S0/1D5V_S3(TPS51124)
			NB	O	45_LDO 1D8V/0D75V
ON 6/17	Modify 6/18		NB	Δ	46_PW_CPU_CORE(ADP3207A)
TI 6/25	Modify 6/24-25		New	O	47_CHARGER MAX8725-> +12V
			NB	V	48_AD / BATT CONN
			NB	Δ	49_PWR PLANE & RESET LOGIC
			NB	O	50_VGA MXM CONN
			New	O	51_SMALL BD CONN->check List
			New	V	52_LVDS SWITCH->Power Map

Check MxM spec: OK

V finish

O most
Δ half

X not yet

No no change

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Title: SMALL BD CONN

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