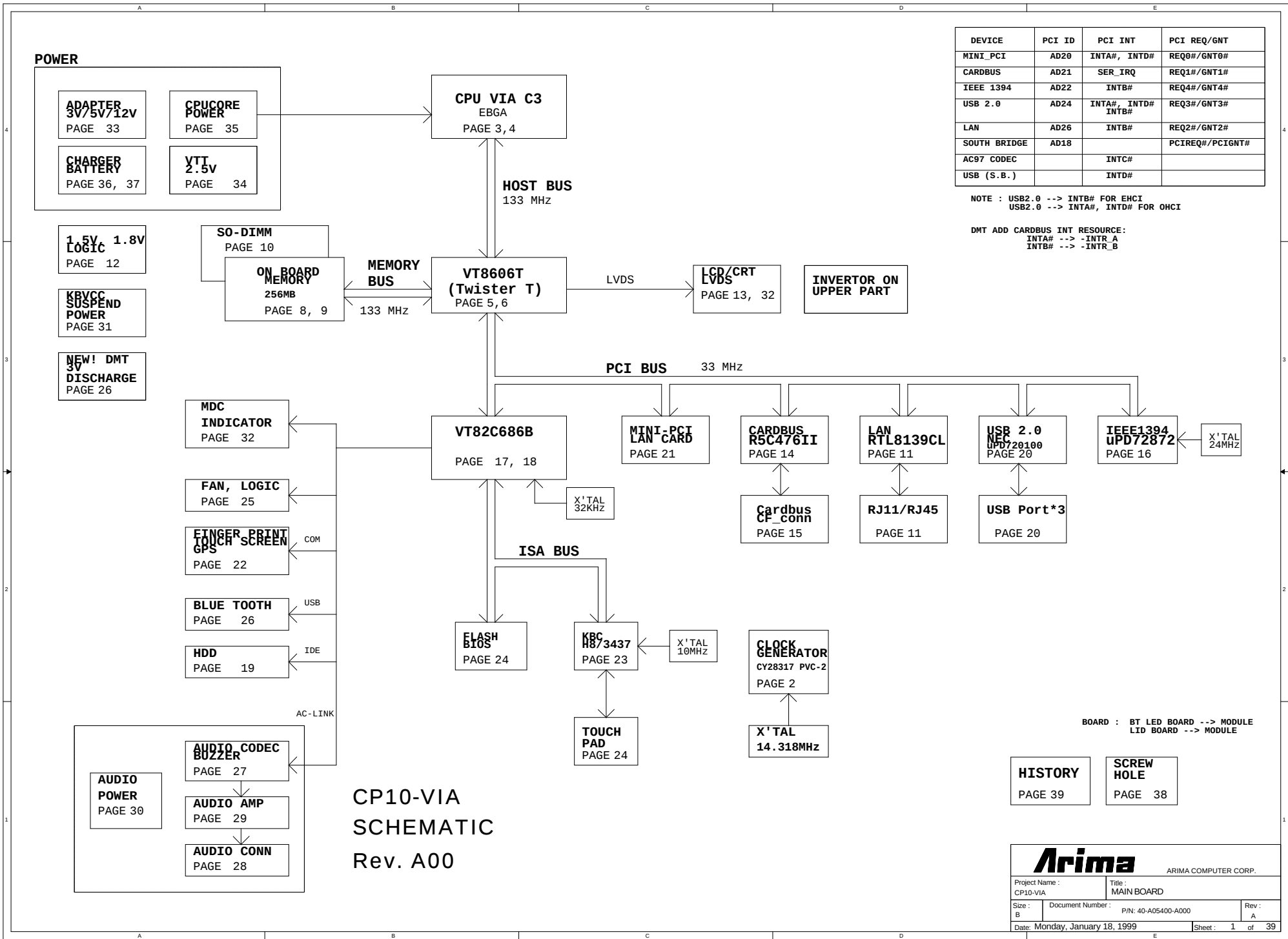
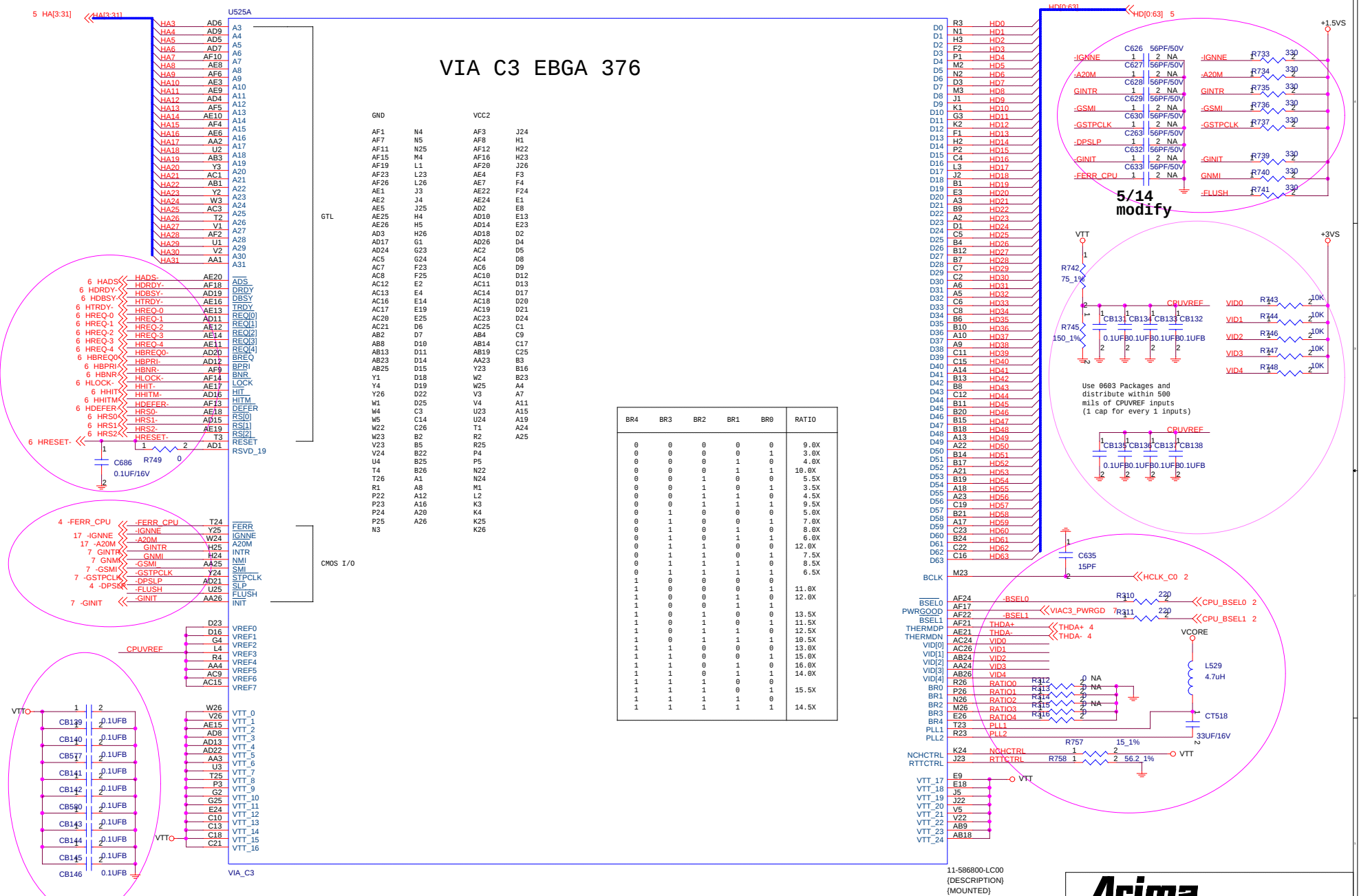
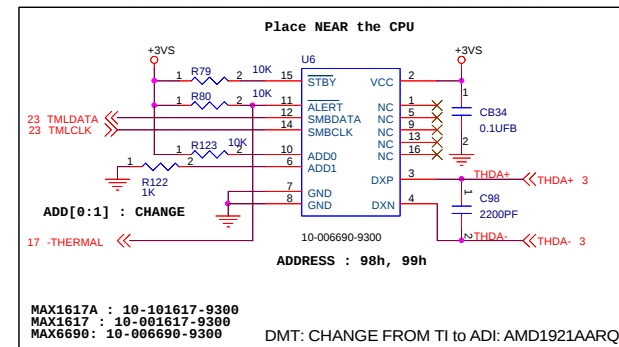
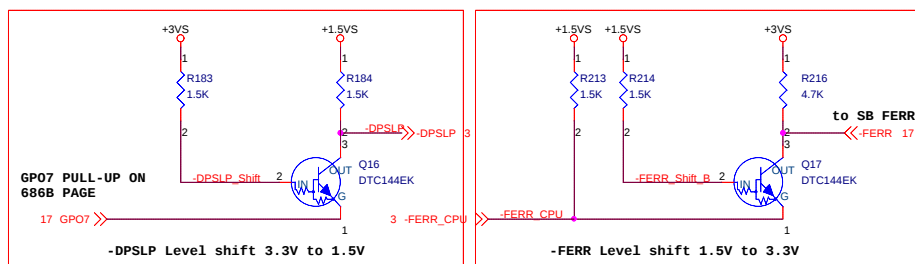
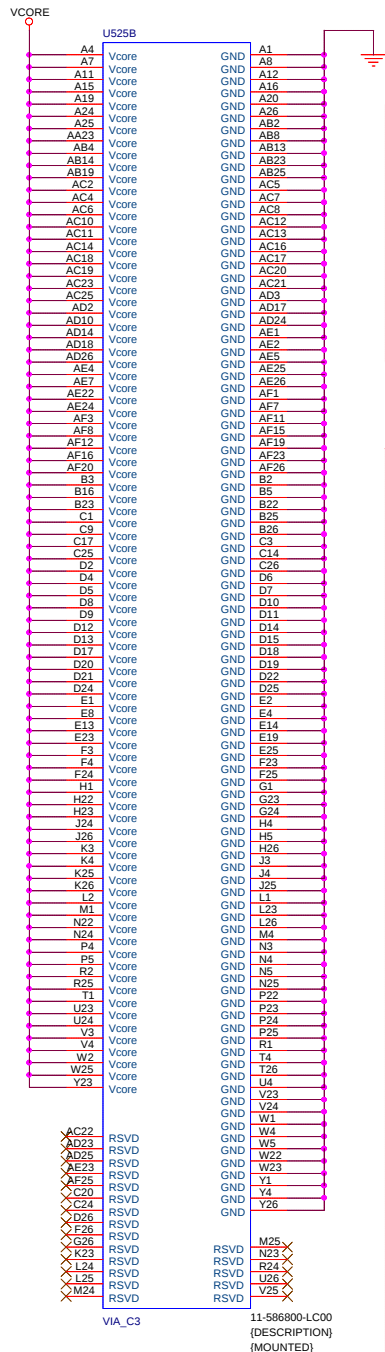
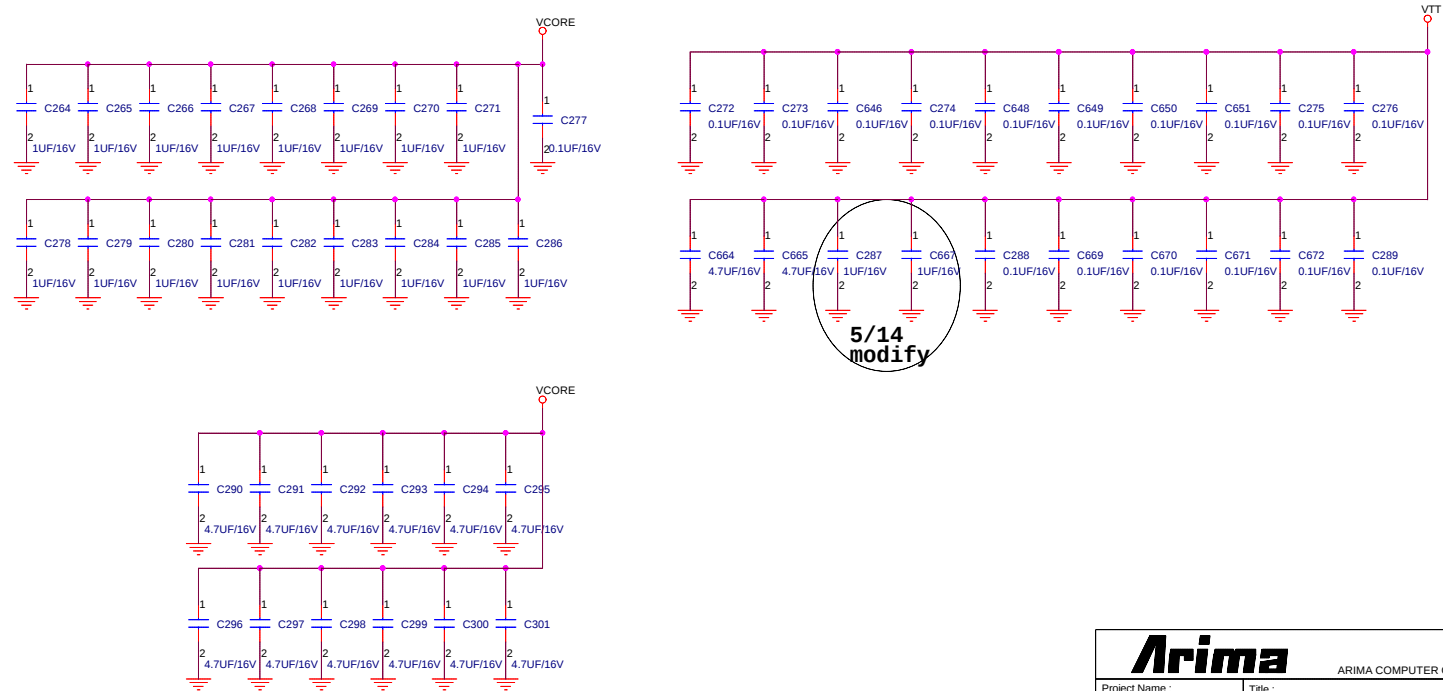








CPU DECOUPLING

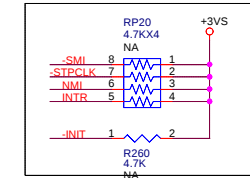
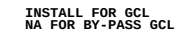
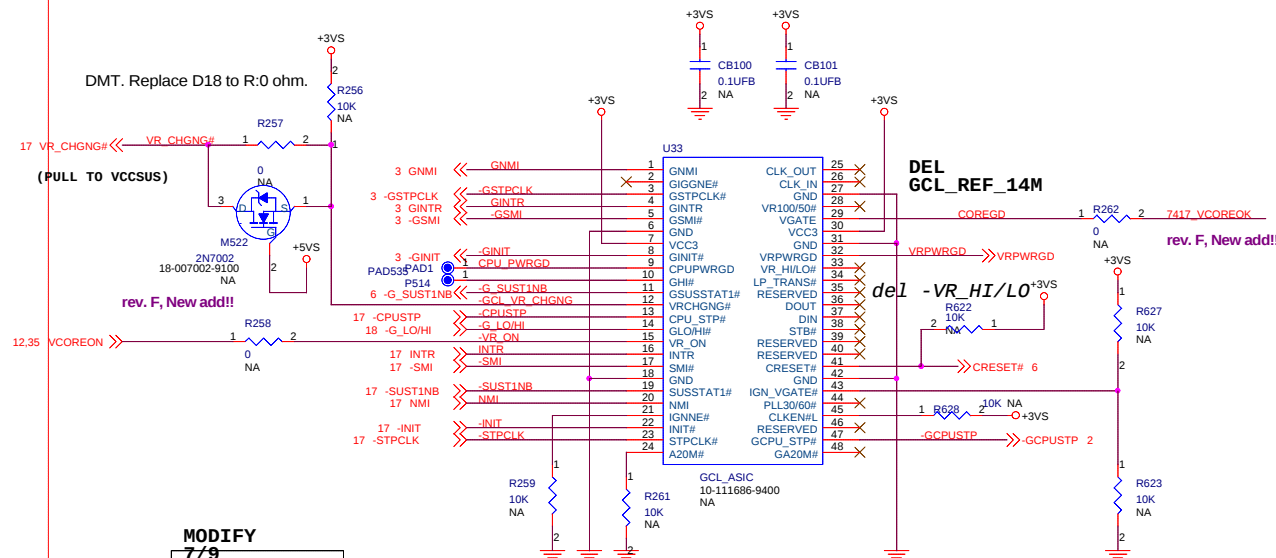


Arima

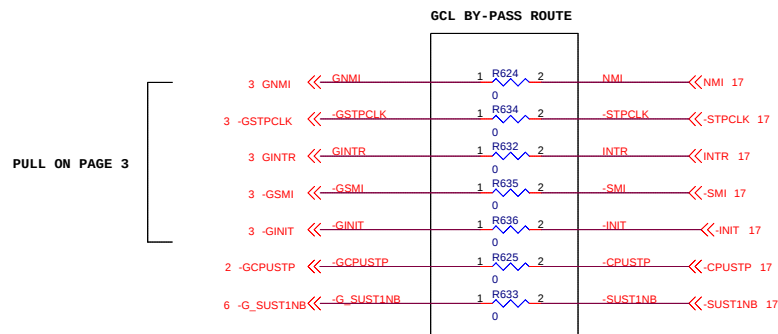
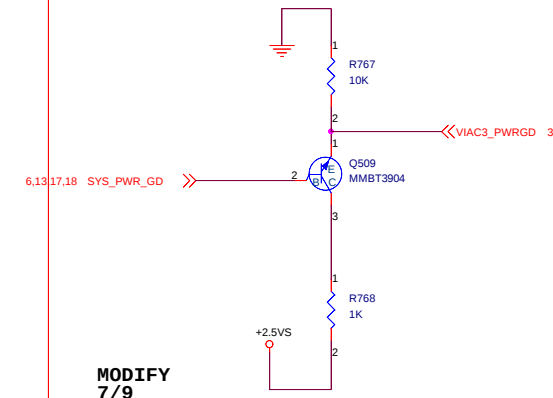
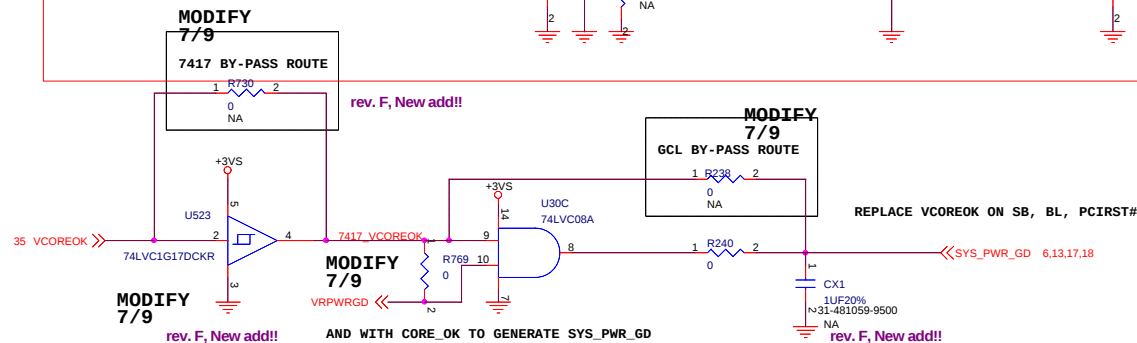
ARIMA COMPUTER CORP.

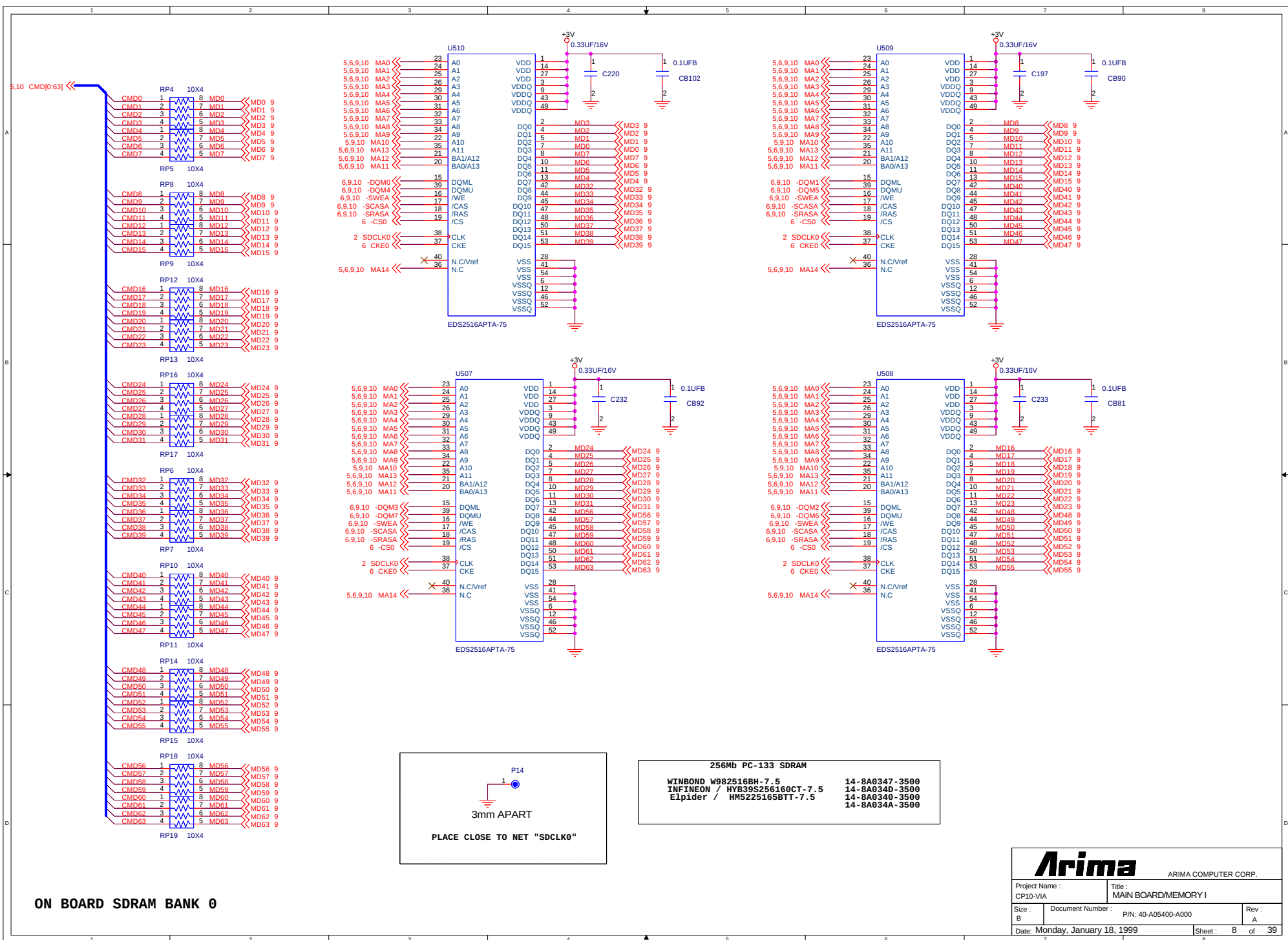
Project Name : CP10-VIA		Title : MAIN BOARD/CPU II	
Size : B	Document Number :	P/N: 40-A05400-A000	Rev : A
Date: Monday, January 18, 1999		Sheet: 4 of 39	

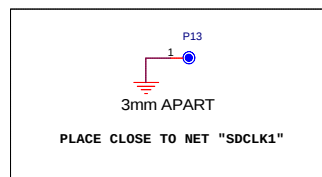
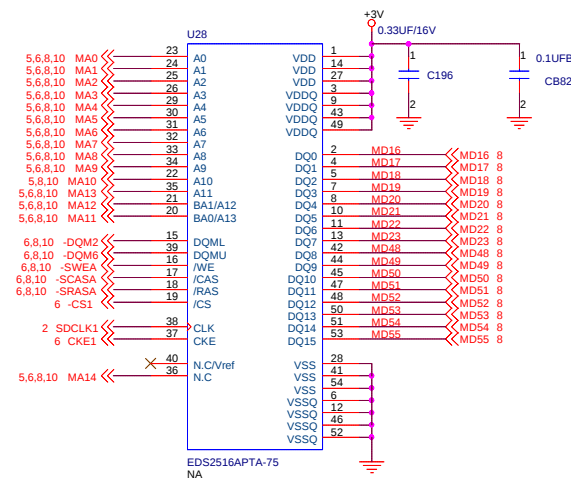
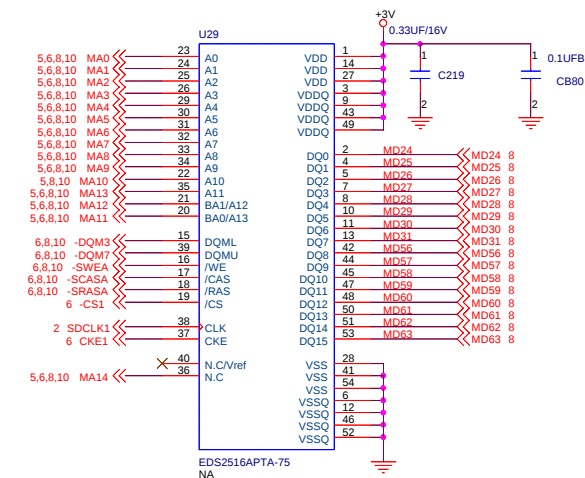
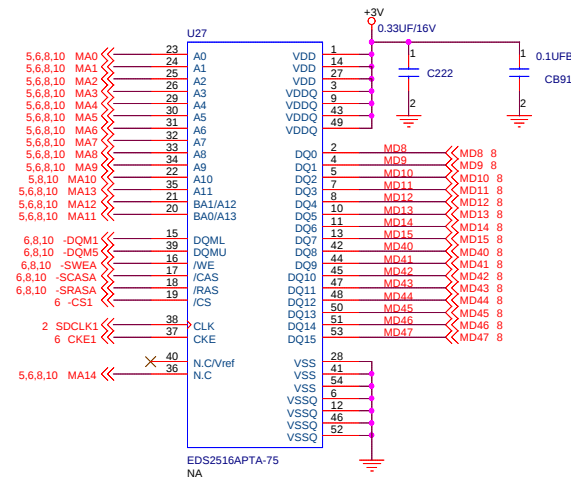
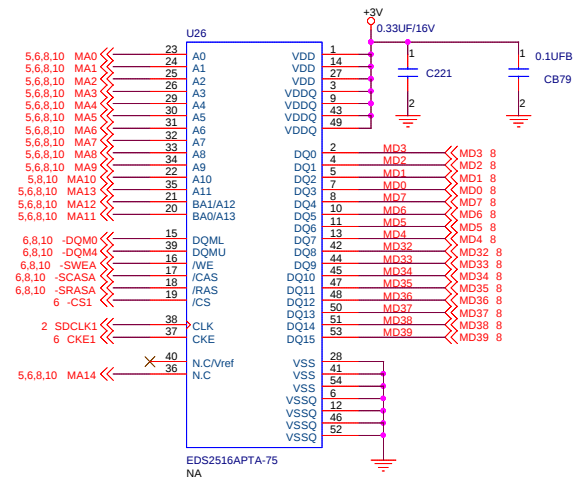
FOR VIA CPU GCL NA



```
Del CPU_PWRGD
AND VCOREOK
SELECT 7/9
```

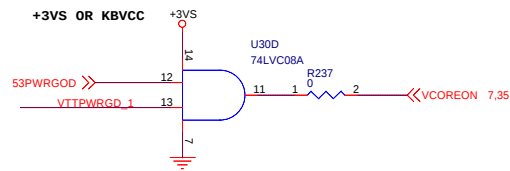




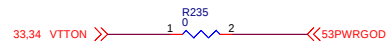


ON BOARD SDRAM BANK 1

Arima		ARIMA COMPUTER CORP.	
Project Name : CP10-VIA		Title : MAIN BOARD/MEMORY II	
Size : B	Document Number : P/N: 40-A05400-A000	Rev : A	
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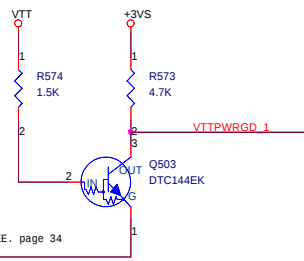


(LCX)



FROM DC/DC

del GMUXSEL AND -DPSLP_PWR

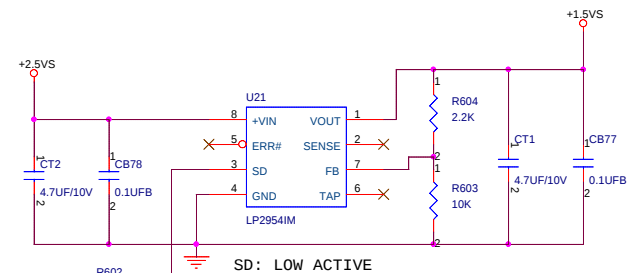


VTPWRGD PULL-UP ON MAX1715EE, page 34
2.34 VTPWRGD

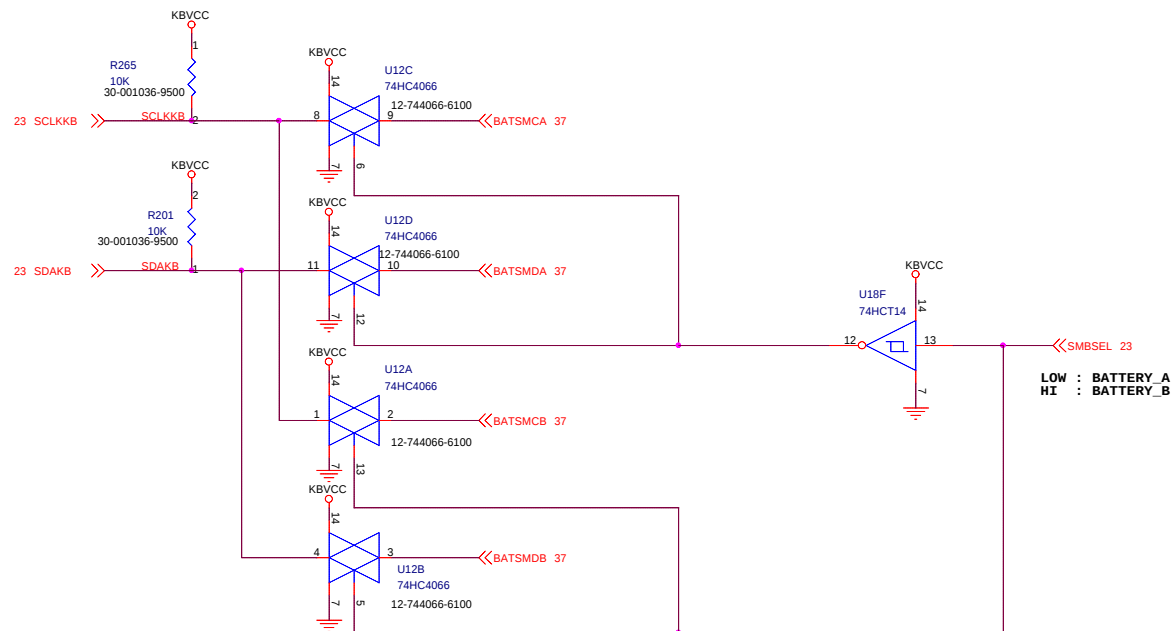
DMT MODIFY LIST:

- ADD 0 OHM IN 53PWRGOD AND VTPWRGD
- ADD VTPWRGD LEVEL SHIFT SCHEMATIC

POWER GOOD



SD: LOW ACTIVE



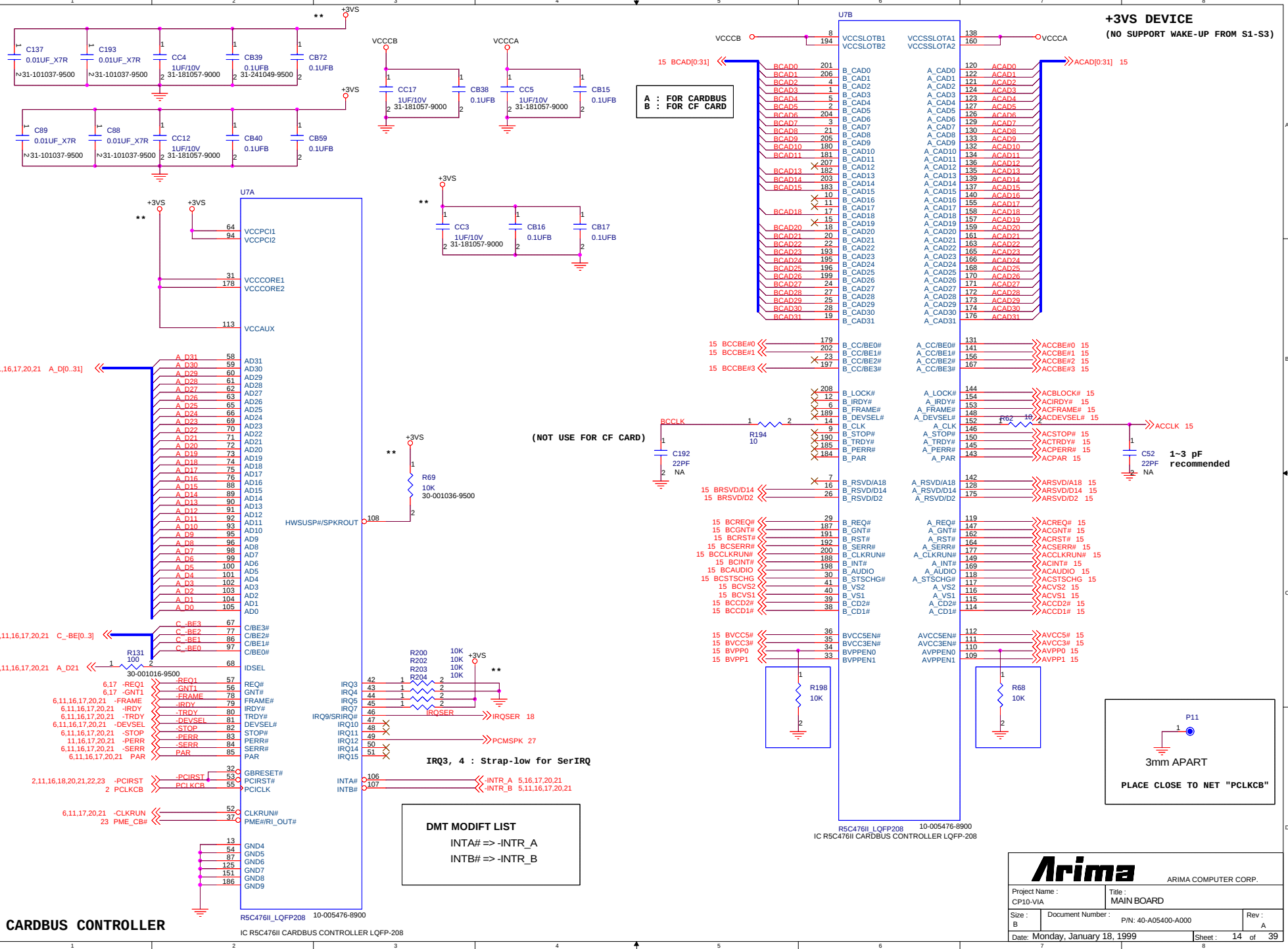
LOW : BATTERY_A
HI : BATTERY_B

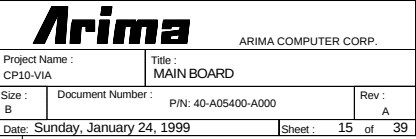
IRT: MERGER U12 & U23 (REMOVE U23)

U23A => U12A

U23B => U12B

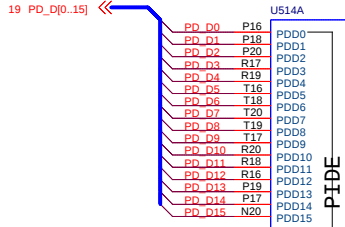
Arima		ARIMA COMPUTER CORP.	
Project Name :	CP10-VIA	Title :	MAIN BOARD/POWERGOOD LOGIC
Size :	B	Document Number :	P/N: 40-A05400-A000
Date:	Monday, January 18, 1999	Rev :	A
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		ARIMA COMPUTER CORP.	
Project Name : CP10-VIA		Title : MAIN BOARD	
Size : B	Document Number :	P/N: 40-A05400-A000	Rev : A
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+3VS/+5VS, VCCSUS



PIDE

AUDIO & GAME

CD-ROM REMOVED

SB

PM

PCI

MONITOR

VT82C868B

10-782686-8700

10-782686-8700

10-782686-8700

10-782686-8700

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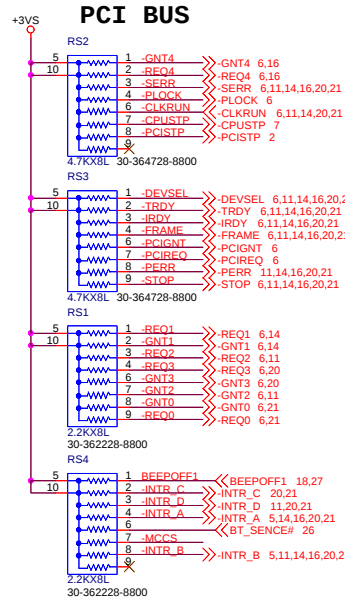
10-782686-8700

10-782686-8700

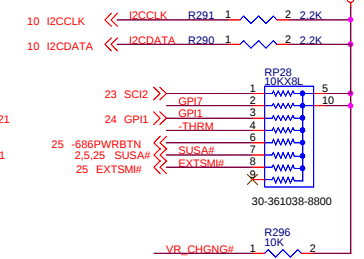
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10-782686-8700

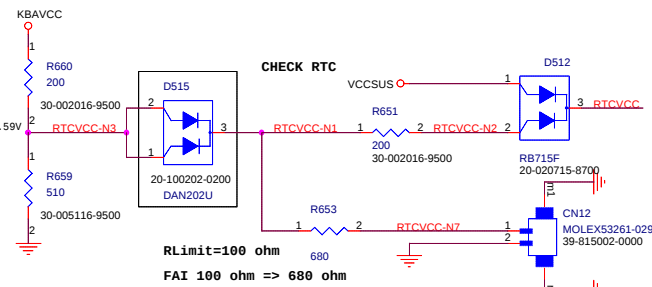
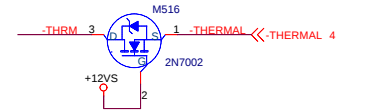
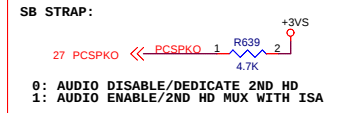
PCI BUS



SUSPEND POWER PLANE:
PWRGD, RSMRST#, PWRBTN#, SMBCLK, SMBDATA,
SUSCLK, SUS#A, SUS#B, SUS#C, SUSST1#, GP11,
GP12, GP13, GP15, GP16, GP17, GP00.



DMT. Change R295 from 10k to NA.

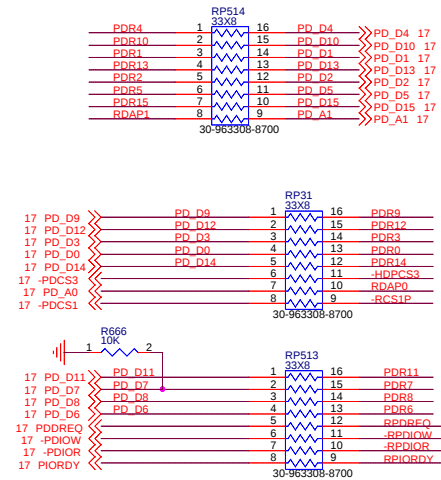
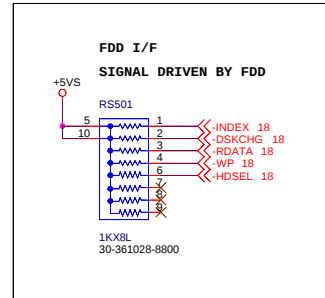
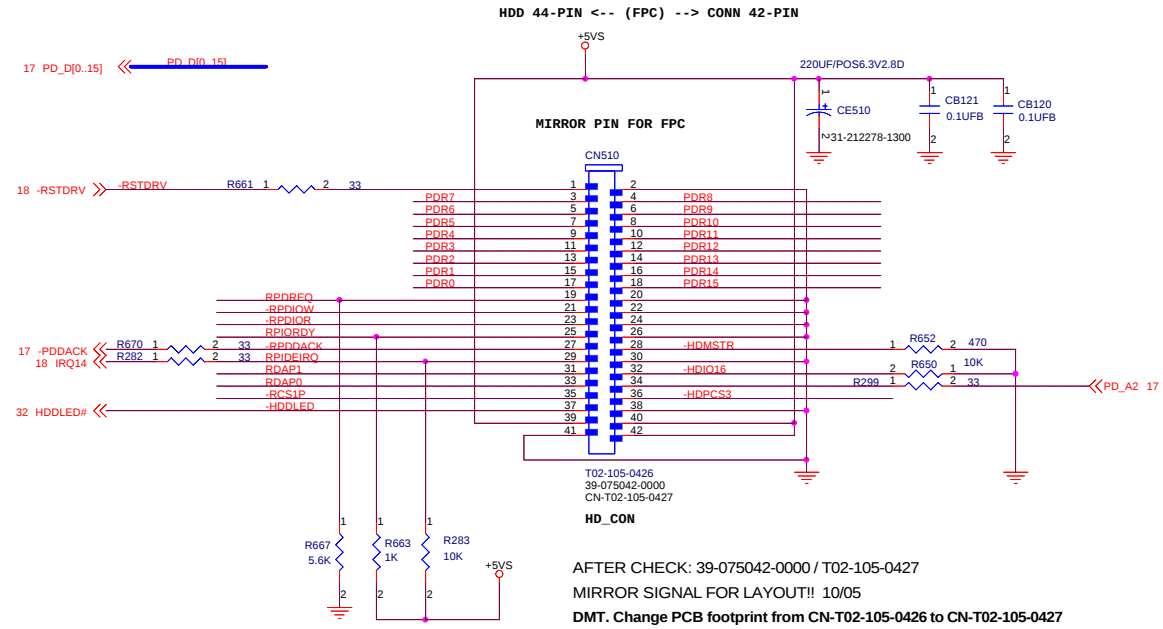


Arima		ARIMA COMPUTER CORP.	
Project Name :	CP10-VIA	Title :	MAIN BOARD
Size :	B	Document Number :	P/N: 40-A05400-A000
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SOUTH BRIDGE 1/2



HDD PIN DEFINE			
1 : RESET	2 : GND		
3 : D7	4 : D8		
5 : D6	6 : D9		
7 : D5	8 : D10		
9 : D4	10 : D11		
11 : D3	12 : D12		
13 : D2	14 : D13		
15 : D1	16 : D14		
17 : D0	18 : D15		
19 : GND	20 : (KEY)		
21 : REQ	22 : GND		
23 : IOW	24 : GND		
25 : IOR	26 : GND		
27 : IORDY	28 : MASTER		
29 : DACK	30 : GND		
31 : IRQ	32 : ID16		
33 : A1	34 : PDIAG		
35 : A0	36 : A2		
37 : CS1	38 : CS3		
39 : DASP(LED)	40 : GND		
41 : SV	42 : SV		
43 : GND	44 : NC		



IDE CONNECTORS

Arima		ARIMA COMPUTER CORP.	
Project Name : CP10-VIA		Title : MAIN BOARD	
Size : B	Document Number : P/N: 40-A05400-A000	Rev : A	
Date: Monday, January 18, 1999		Sheet : 19	of 39

+3VS DEVICE

1. SUPPORT S1 WAKE-UP ONLY, NO
NEED TO SUPPORT S3 WAKE-UP

2.11.14.16.18.21.22.23 -PCIRST << 1
DAP202U
20-100202-0100

6.11.14.16.17.21 C_BE3
6.11.14.16.17.21 C_BE2
6.11.14.16.17.21 C_BE1
6.11.14.16.17.21 C_BE0

6.11.14.16.17.21 PAR
6.11.14.16.17.21 -FRAME
6.11.14.16.17.21 -IRDY
6.11.14.16.17.21 -TRDY
6.11.14.16.17.21 -STOP
5.11.14.16.17.21 A_D24
6.11.14.16.17.21 -DEVSEL
6.17 -REQ3
6.17 -GN13
11.14.16.17.21 -PERR
6.11.14.16.17.21 -SERR

2 PCLK_USB20 << 2
6.11.14.17.21 -CLKRUN << 2

23 USB20_PME# << 2
18 USB_SMI# << 2

DO NOT SUPPORT LEGACY !

5.14.16.17.21 -INTR_A << 1
17.21 -INTR_C << 1

OHCI-2

11.17.21 -INTR_D << 1
5.11.14.16.17.21 -INTR_B << 1

OHCI-1

USB2.0

DMT use 48MHz!!

48M/30M SEL

ENABLE OHCI1
DISABLE OHCI2

IRT: COMMON CHOKE - MOUNTED

DVT to DMT:
VBBRST0: SYS_PWR_GD => -PCIRST
CHANGE -OC#

FAI: Those PAD are for ATE

WHEN SET TO DISABLE EEPROM, PIN
"SRCLK" AND "SRDAT" BECOME OUTPUT
MODE.

CLOSE TO "PCLK_USB20" &
"USB_48MHZ"

Arima

ARIMA COMPUTER CORP.

Project Name : CP10-VIA		Title : MAIN BOARD	
Size : B	Document Number :	P/N: 40-A05400-A000	Rev : A
Date: Monday, January 18, 1999		Sheet: 20	of 39

A B C D E

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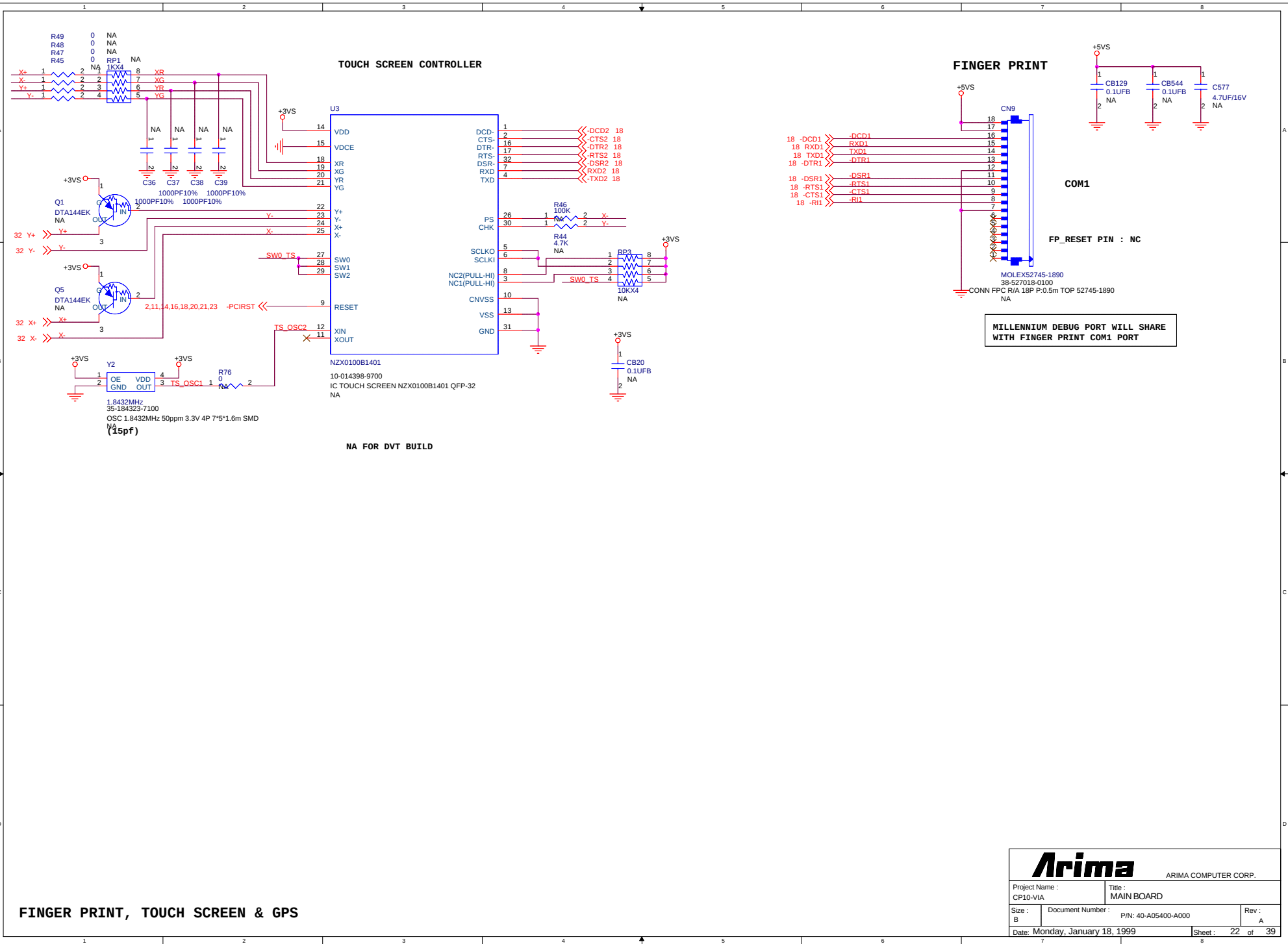
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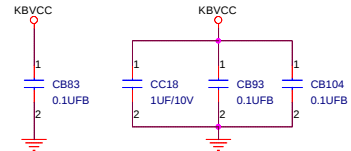
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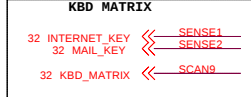


IRT: KBVCC to KBVCC

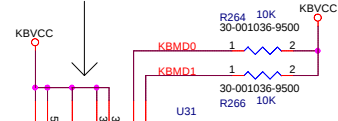


FAI CHANGE POWER SOURCE.

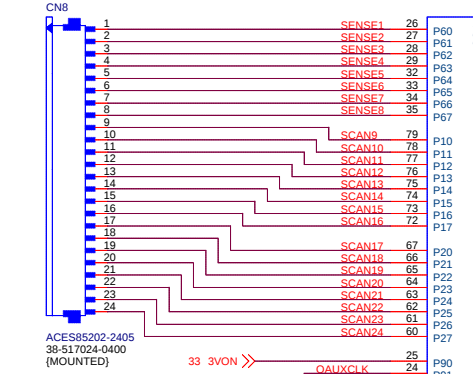
PIN36, 37 change from KBVCC to KBVCC



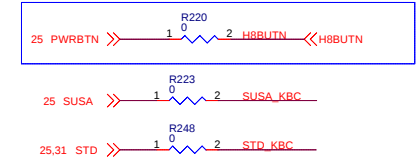
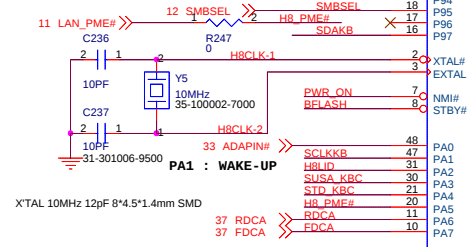
LONG TRACE as one RESISTER



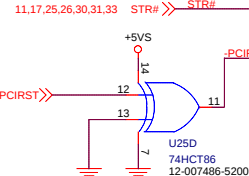
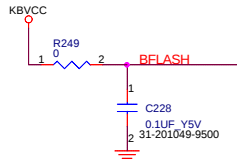
*** KEYBOARD CONNECTOR ***



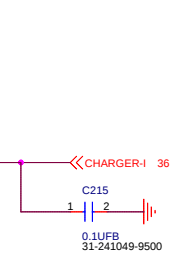
P96=GPI or clock output



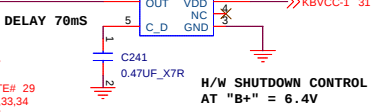
H8



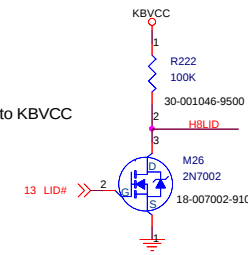
DMT NEW CHANGE!



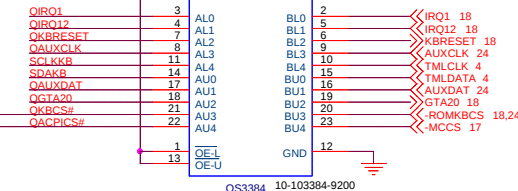
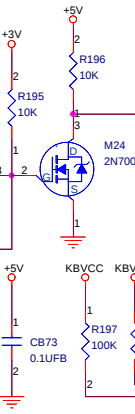
P41 : (FAN2 REMOVE)



H/W SHUTDOWN CONTROL AT "B+" = 6.4V

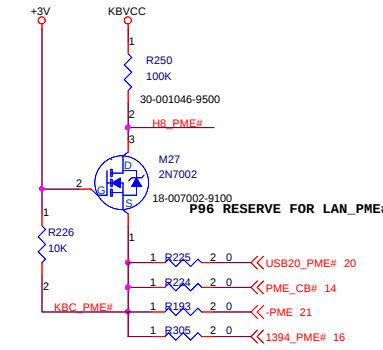
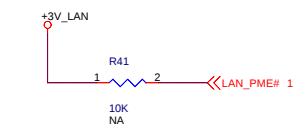


IRT: KBVCC to KBVCC

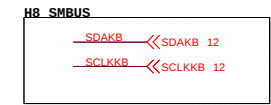


KB : PS2/ KBD
AUX1 : PS2/MOUSE

DMT modify: LAN_PME# pull to +3V_LAN



FAI: Add 1394's PME



PULL UP ?

P96 OUTPUT SHOULD BE CLOCK FUNCTION, CAN NOT BE GPO.
PAB - PA7 AND P6B - P67 ARE AND TOGETHER FOR INTERRUPT.
P9B - P92 = IRQB - IRQ2

Arima

ARIMA COMPUTER CORP.

Project Name : CP10-VIA

Title : MAIN BOARD

Size : B

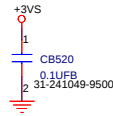
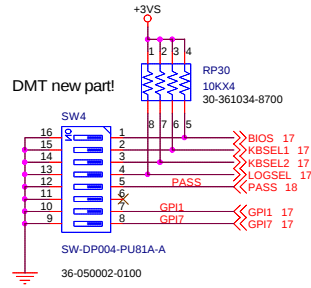
Document Number : P/N: 40-A05400-A000

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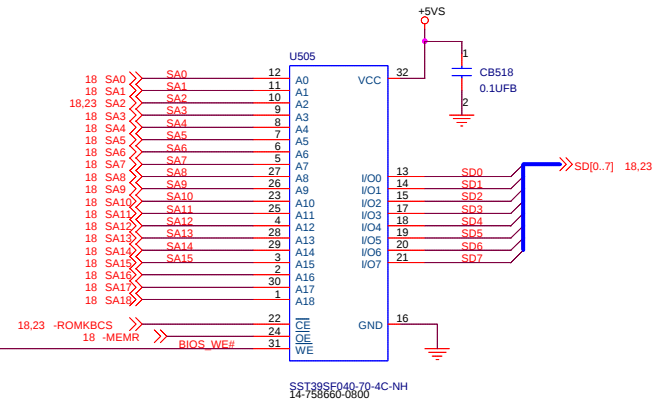
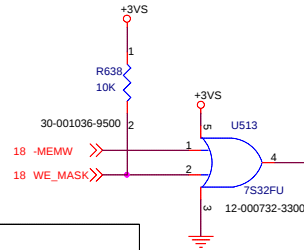
Rev: A

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PLCC : FLASHROM
 14-758660-0800 : SST39SF040-70-4C-NH
 14-758667-1100 : WINBOND W29C040P-90
 14-75866H-1100 : MX29F004TQC-90



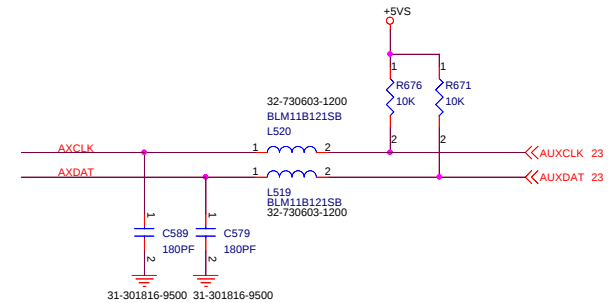
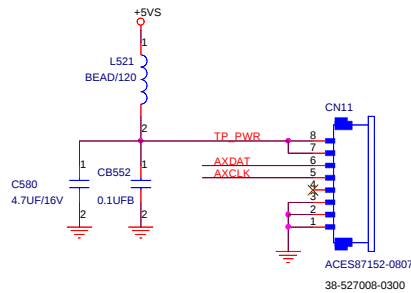
GP11 = Finger Print Detect



WILL CHANGE TO IC DIRECTLY MOUNTED
 AFTER MASS PRODUCTION.

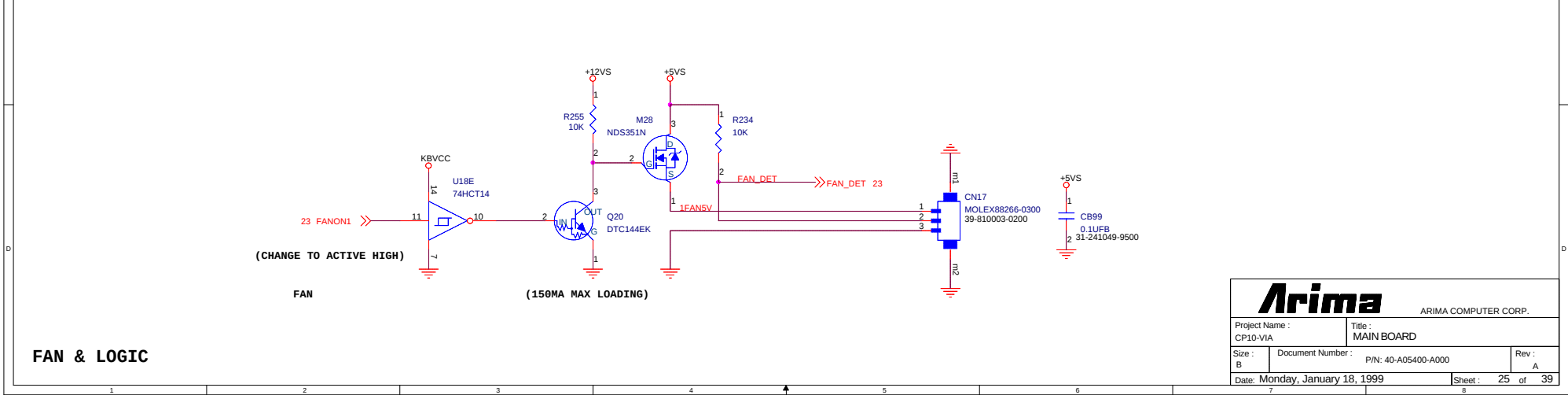
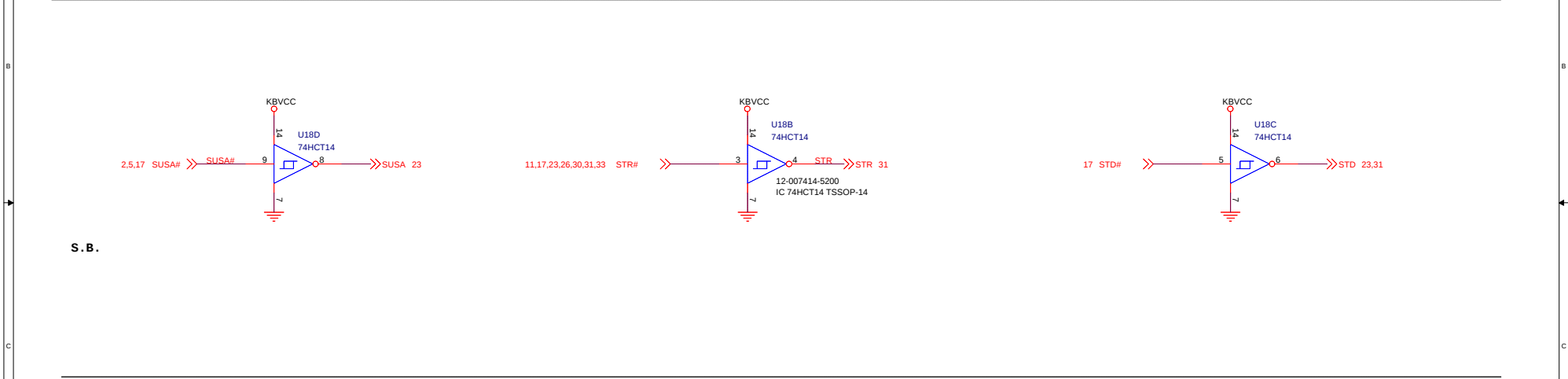
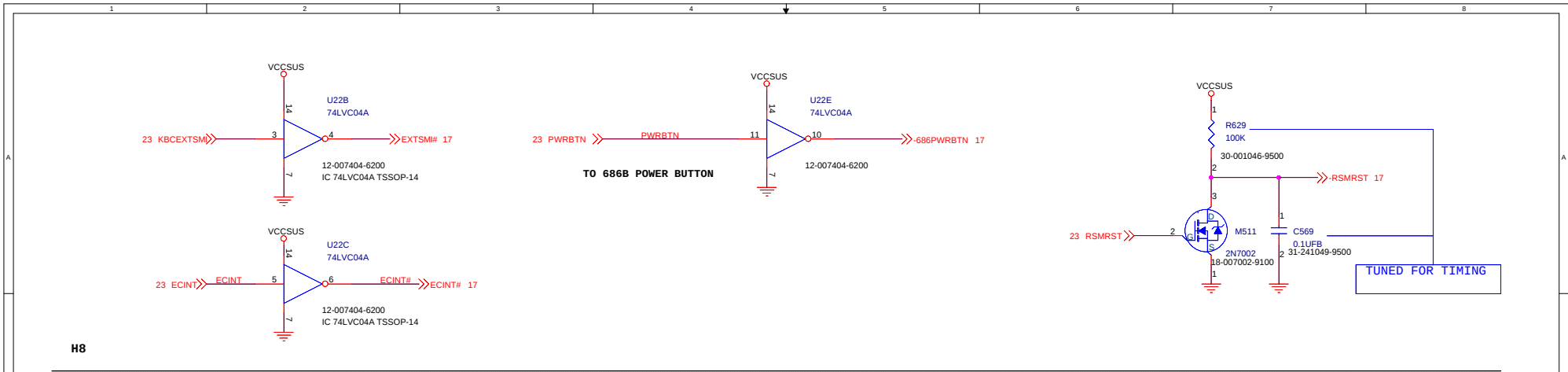
SW4-1: BIOS BOOT BOLCK	OFF: Normal; ON: Enable
SW4-2: KEYBOARD SEL-1	OFF = Japan Keyboard
SW4-3: KEYBOARD SEL-2	OFF = Japan Keyboard
SW4-4: LOGO SELECT	OFF: NEC logo; ON: PACKBELL logo
SW4-5: PASSWORD	OFF: Disable; ON: Overwrite Password
SW4-6: NA	
SW4-7: FINGER PRINT DETECT	OFF: No Finger Print; ON: Finger Print Function
SW4-8: GPI / RESERVE	OFF: Lavia (Consumer); ON: VersaPro (Commercial)

DMT MODIFT LIST
 ADD 8 POLES DIP SW



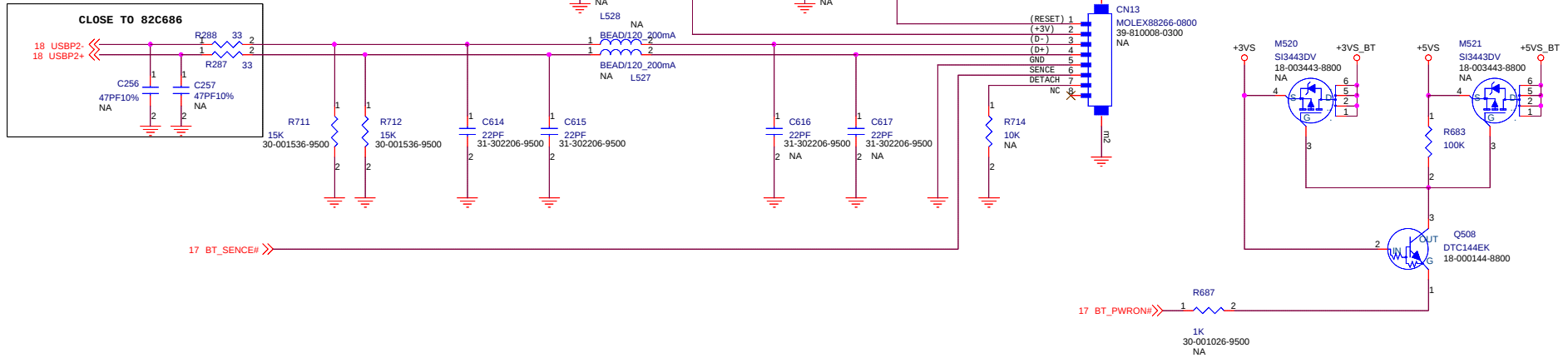
BIOS & TOUCHPAD

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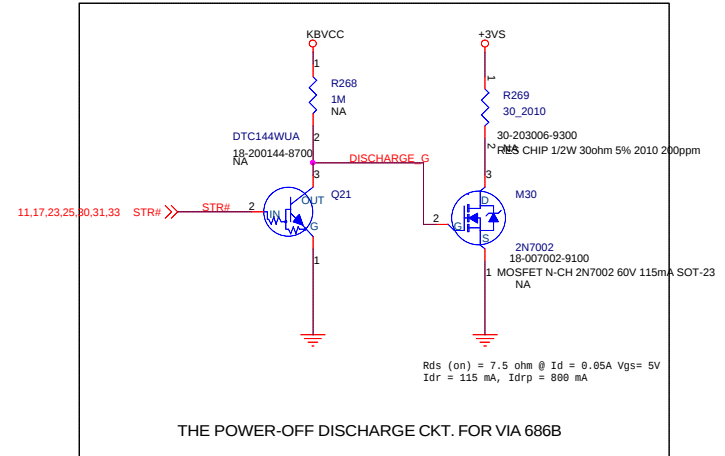
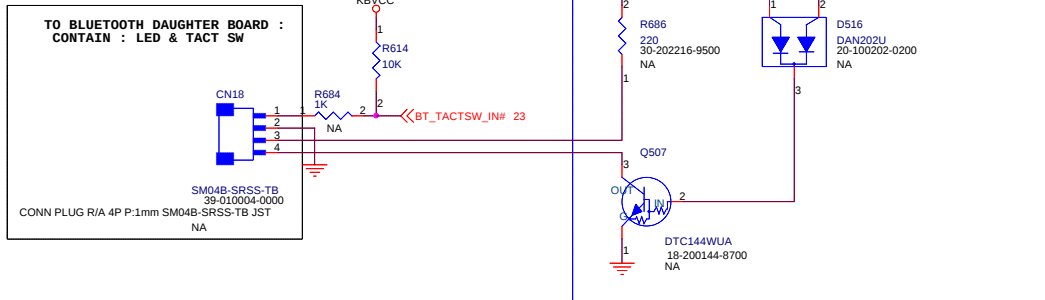


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*** CELLULAR / BT CONNECTOR ***



FAI Change from JST to ACES



FOR DMT. NEW! 3V DISCHARGE CKT.
FOR FAI.REMOVE.

BLUETOOTH and 3V DISCHARGE CKT.

Arima			
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CHANGE TO AD1886A !!

FOR COMP SIDE (TOP SIDE)

30-910045-00 FOR A-CURVE
30-910043-00 FOR C-CURVE

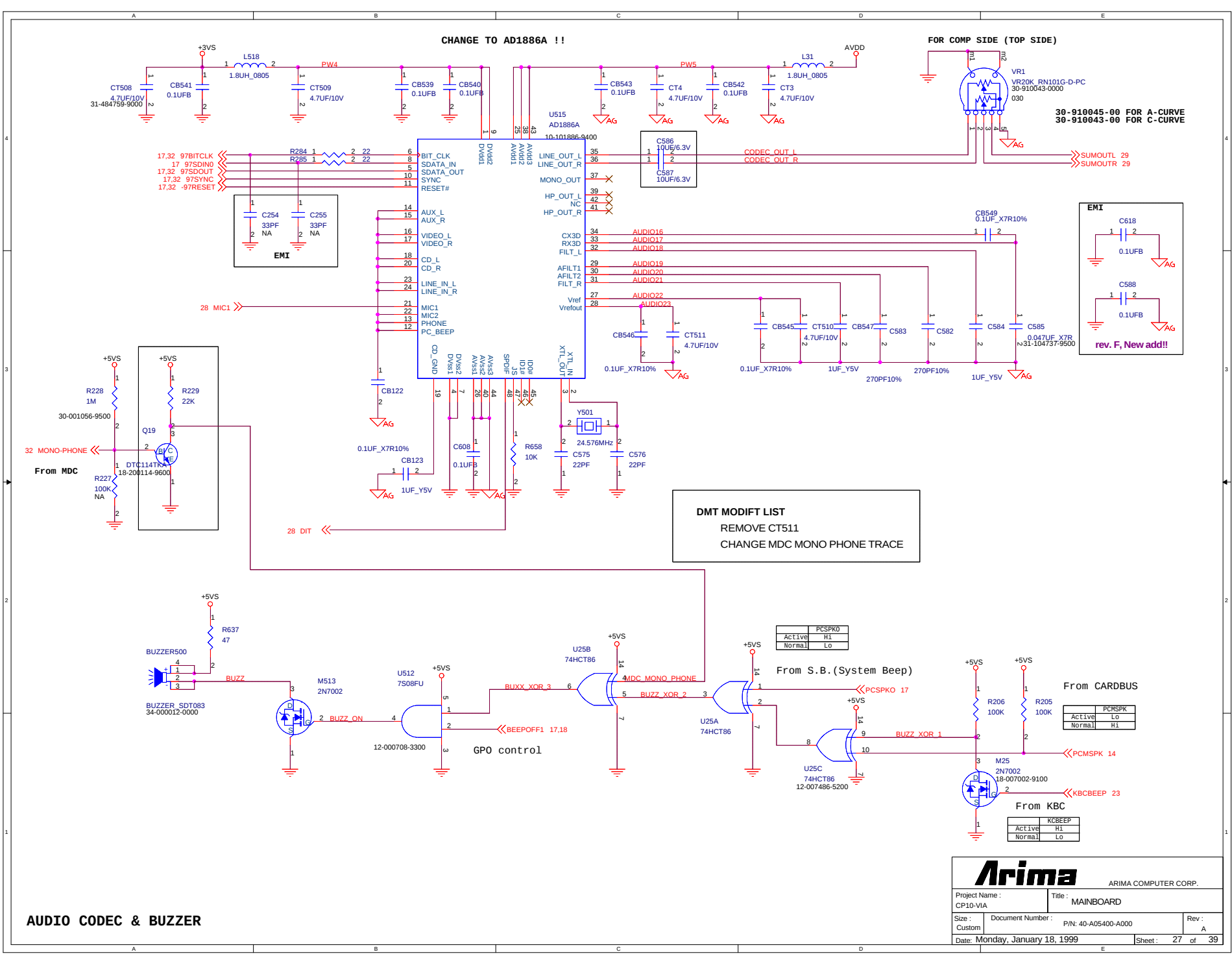
EMI
C618 0.1uFB
C588 0.1uFB
rev. F, New add!!

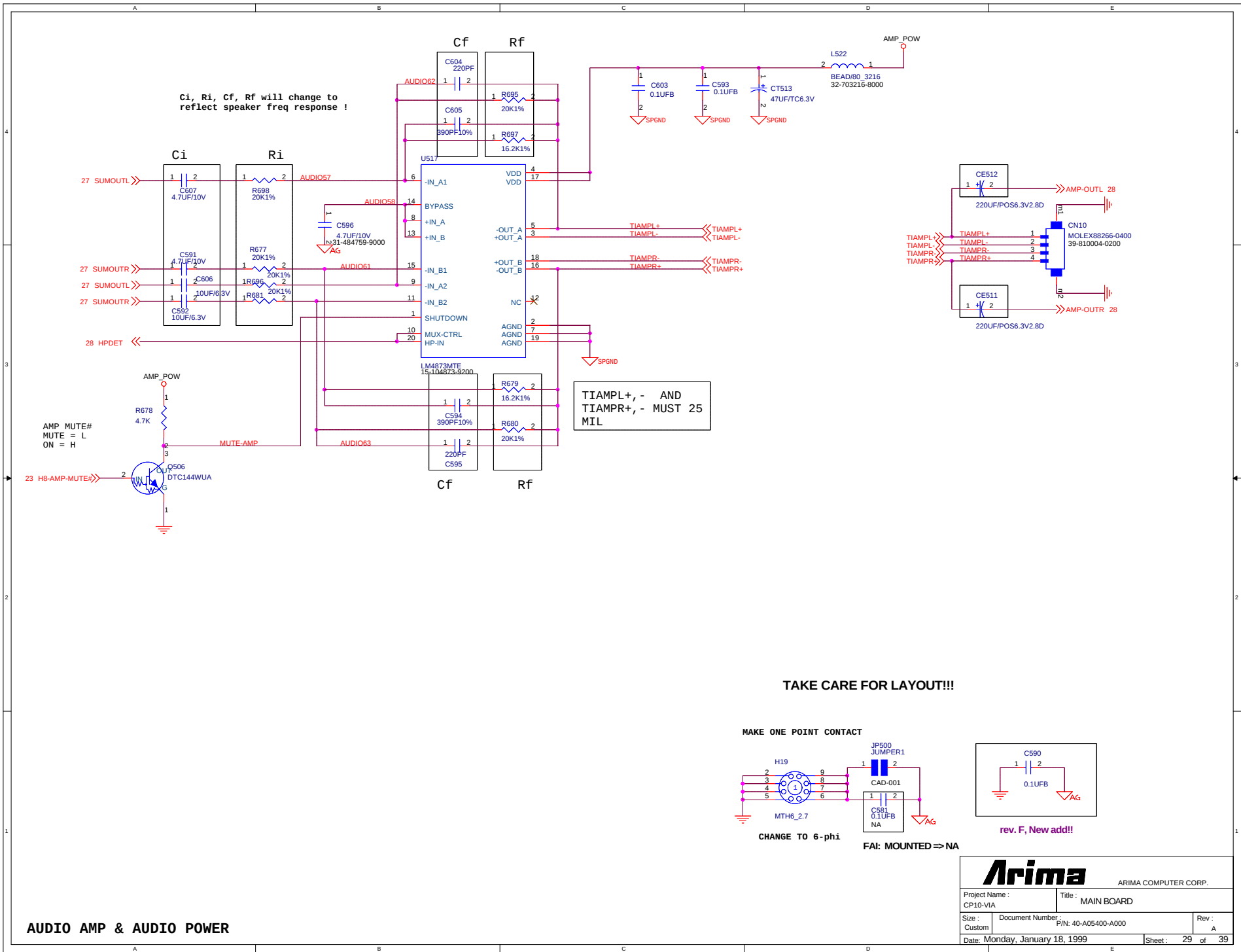
DMT MODIFT LIST
REMOVE CT511
CHANGE MDC MONO PHONE TRACE

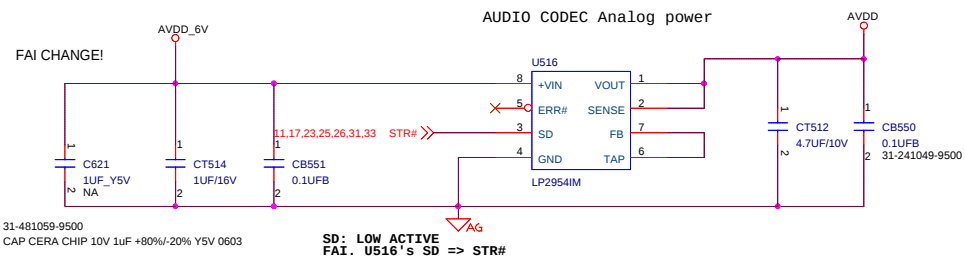
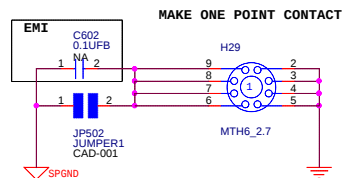
AUDIO CODEC & BUZZER



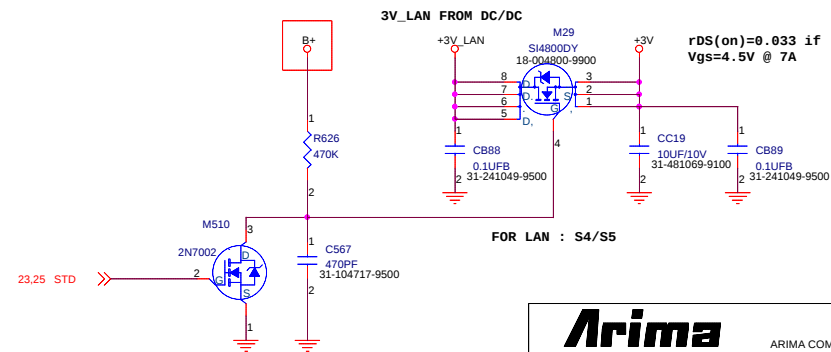
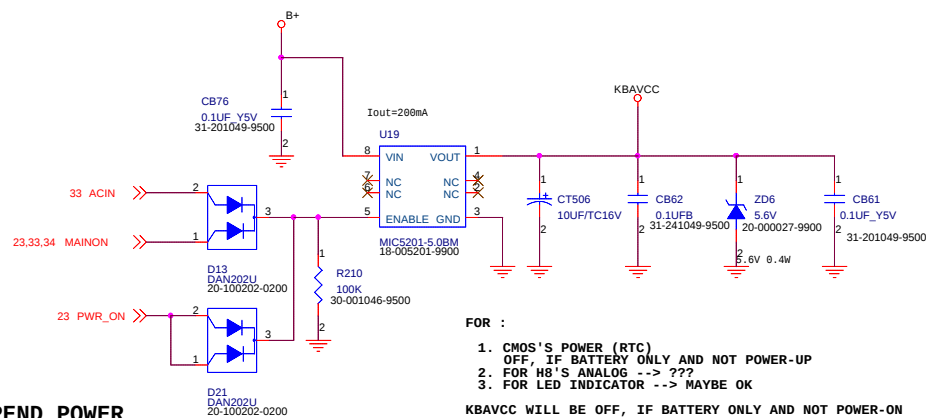
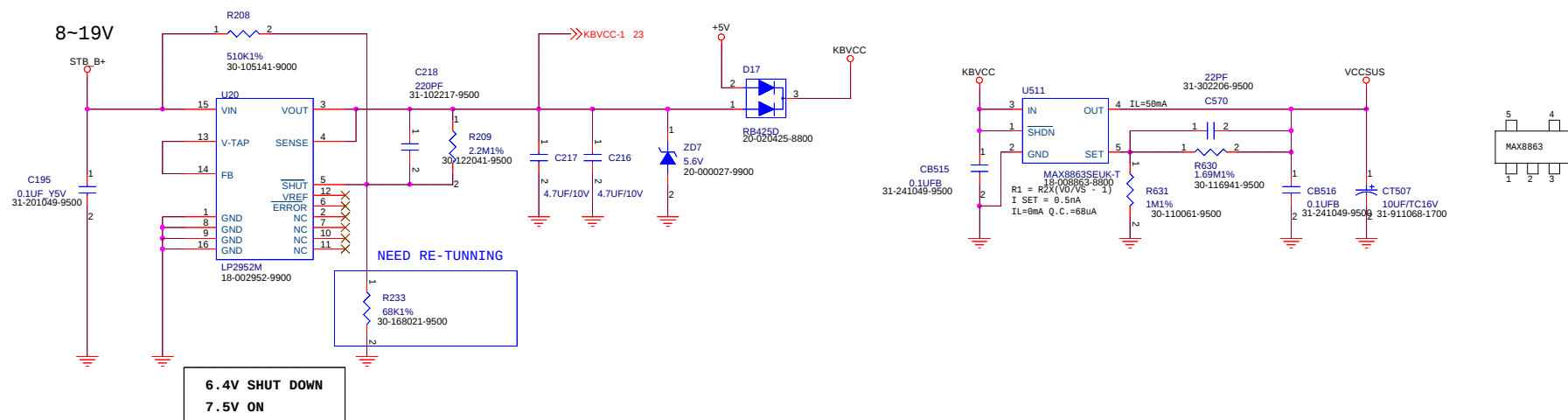
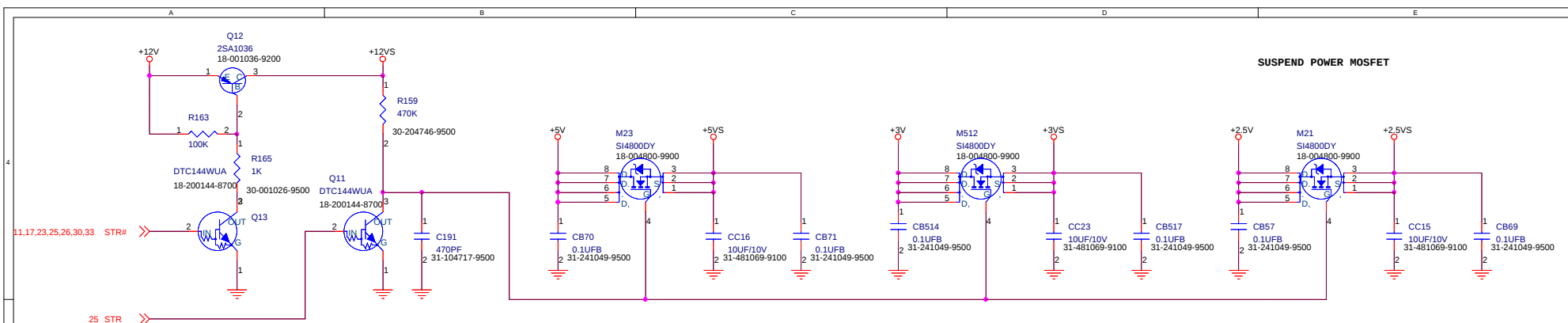
ARIMA COMPUTER CORP.
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 Title : MAINBOARD
 Size : Custom
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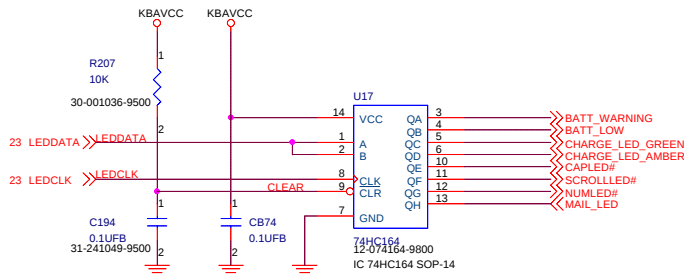


		ARIMA COMPUTER CORP.	
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Size : B	Document Number : P/N: A0-A05400-A000		Rev : A
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		ARIMA COMPUTER CORP.	
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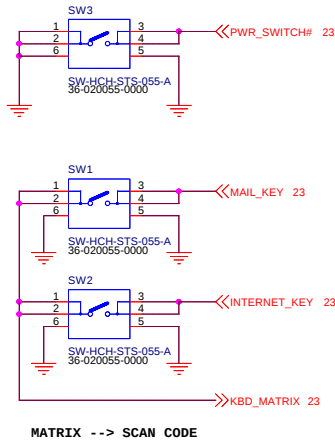
KBAVCC POWER



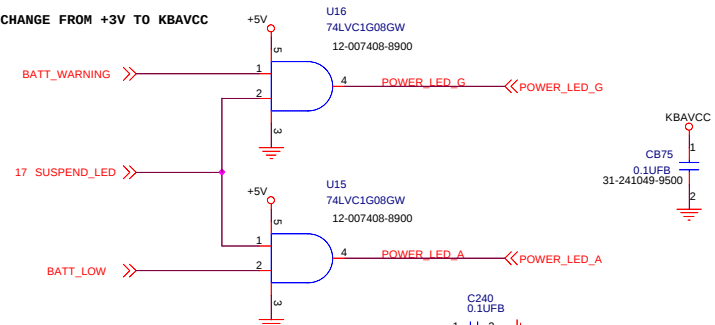
INDICATOR

DMT MODIFT LIST
 SW1-6 => GND
 SW2-6 => GND
 SW3-6 => GND

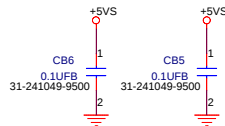
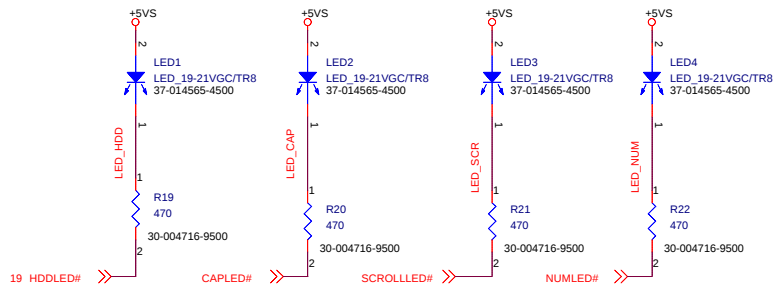
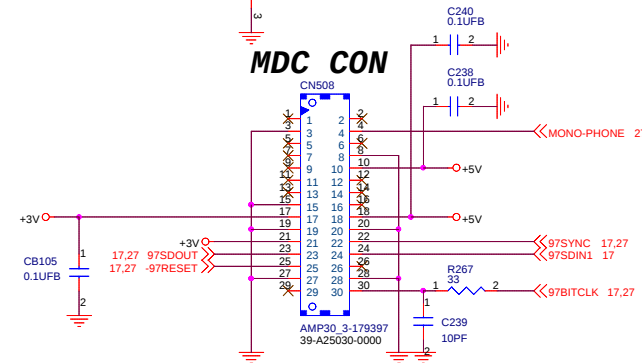
POWER SWITCH AND SHORT KEY



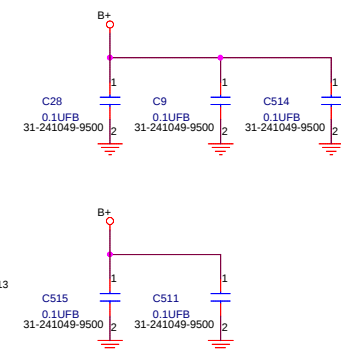
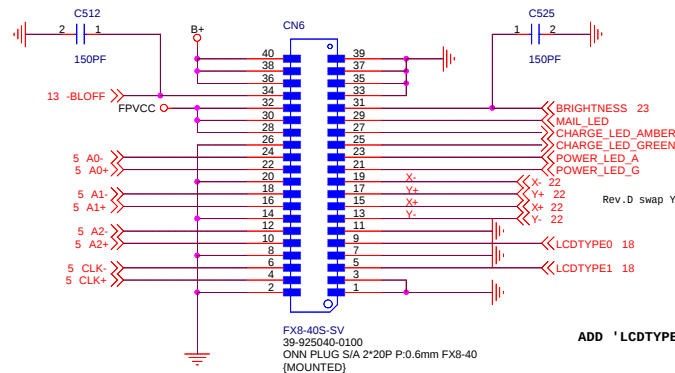
CHANGE FROM +3V TO KBAVCC



MDC CON



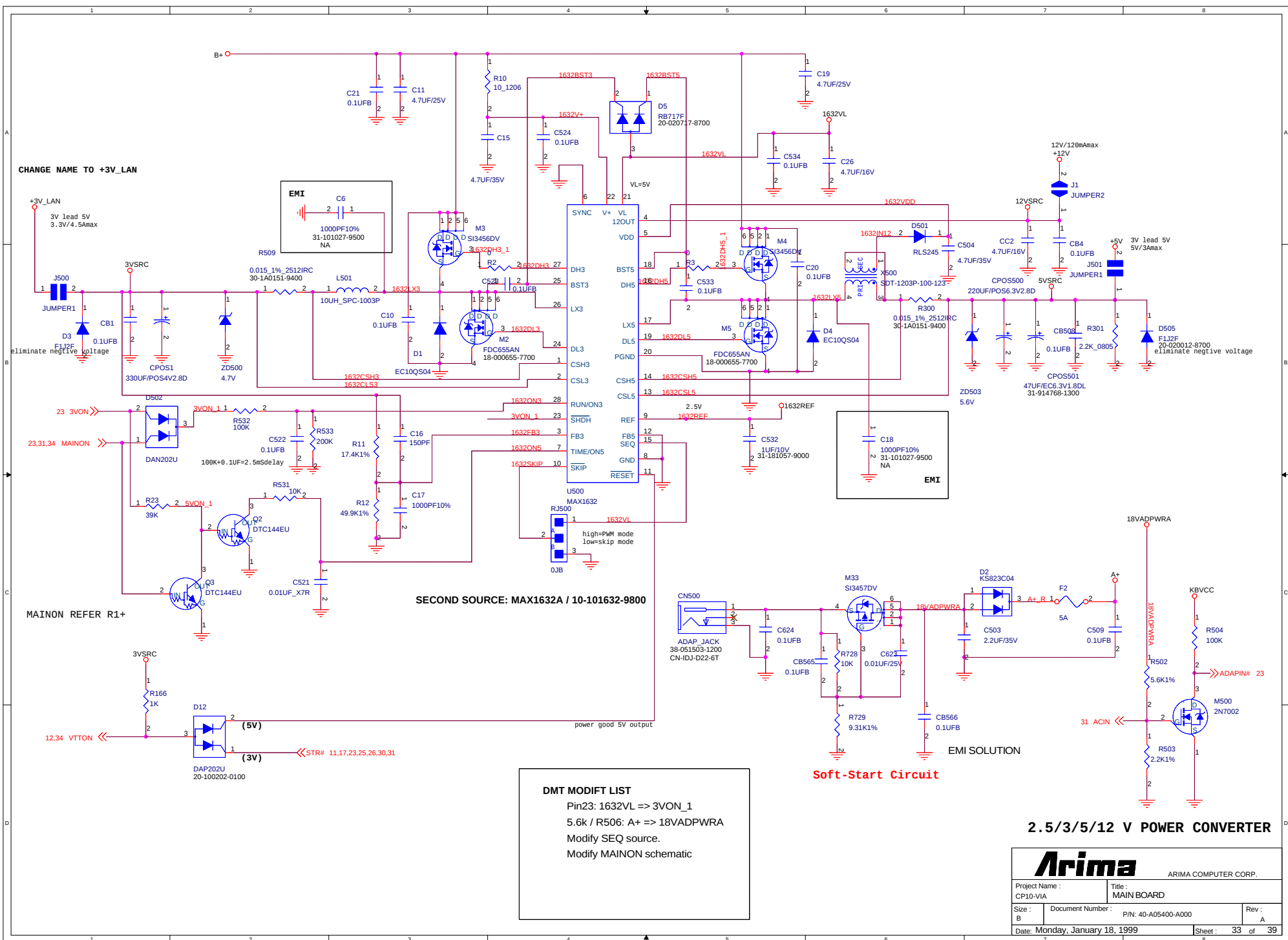
RE-ASSIGN PIN FOR FPC - 8/25



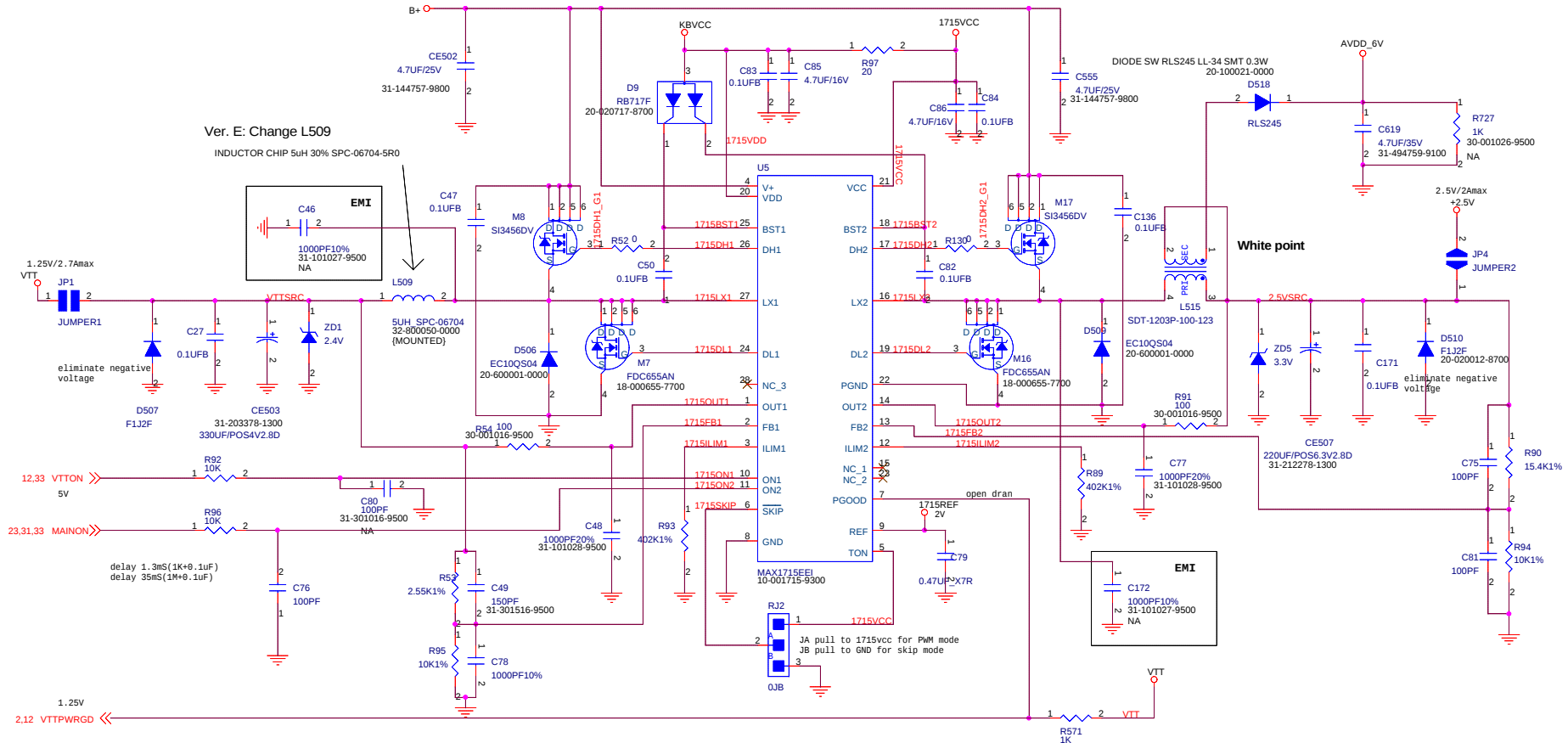
LED, LVDS I/F & MDC

ADD 'LCDTYPE2" PIN ON 8/28

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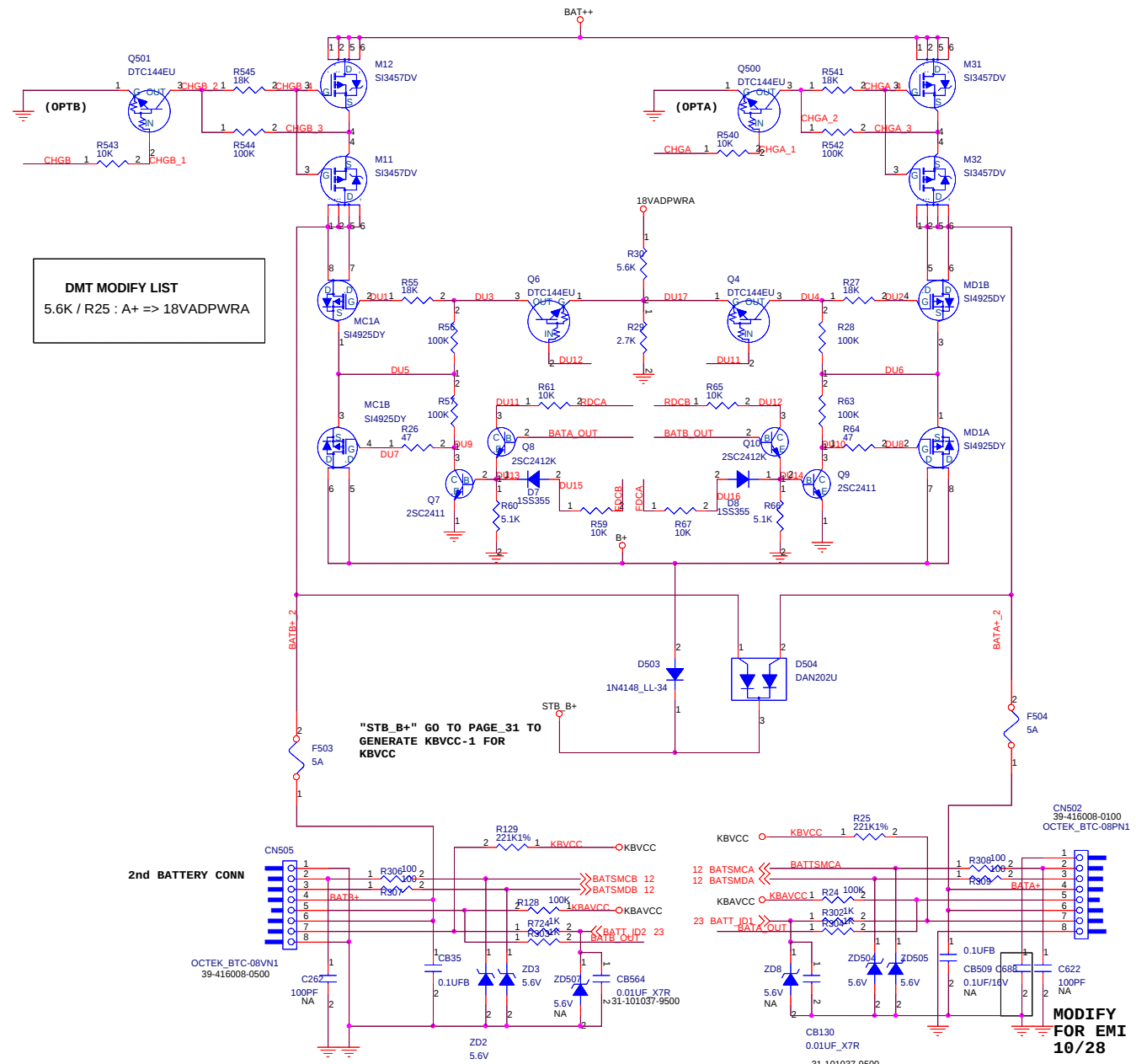
Ver. E: Change L509
INDUCTOR CHIP 5uH 30% SPC-06704-SR0



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23 RDCB >> RDCB
 23 FDCB >> FDCB
 23 RDCA >> RDCA
 23 FDCA >> FDCA
 23,36 CHGB >> CHGB
 23,36 CHGA >> CHGA

DMT MODIFY LIST
 5.6K / R25 : A+ => 18VADPWRA

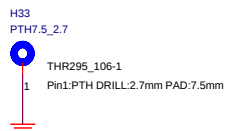
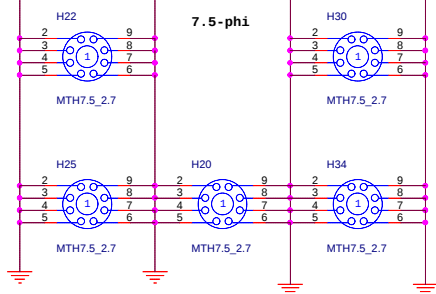
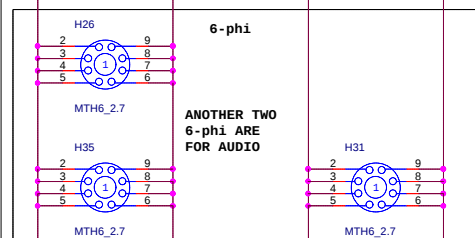
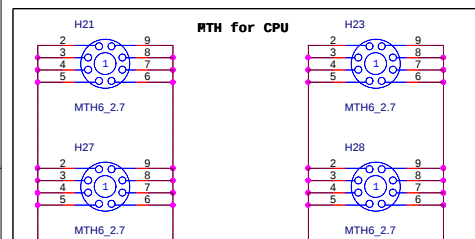


2nd BATTERY CONN

MODIFY FOR EMI 10/28

Hole (6.0X2.7) X5 for SYSTEM

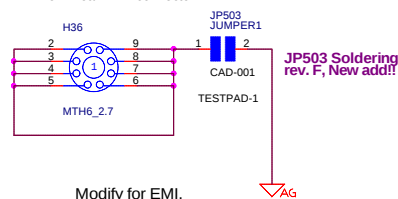
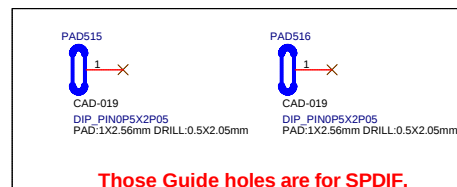
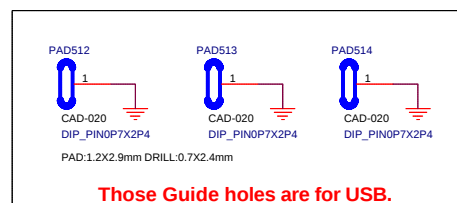
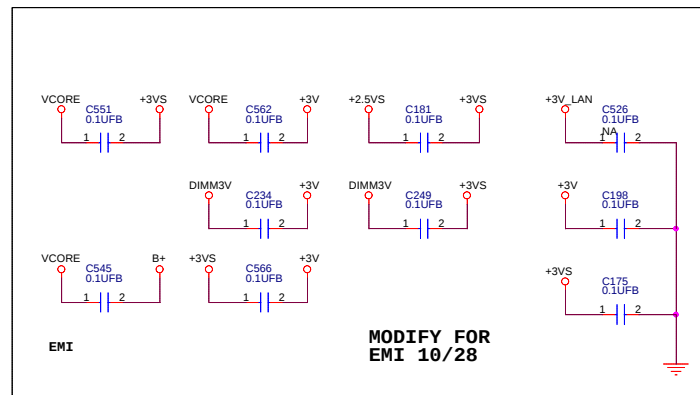
Near CPU's hole, Add one Guide hole!!!!



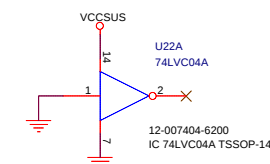
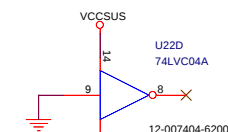
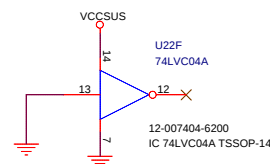
New! under MDC

ONE MTH_6/2.7 ON SCH29
ONE MTH_6/2.7 ON SCH30

MOUNT HOLE



Modify for EMI.



FID2
FIDUCIAL
 本PIN不可接任何信號或電源
CAD-016
FIDUCIAL MARK 光學定位用

FID3
FIDUCIAL
 本PIN不可接任何信號或電源
CAD-016
FIDUCIAL MARK 光學定位用

FID6
FIDUCIAL
 本PIN不可接任何信號或電源
CAD-016
FIDUCIAL MARK 光學定位用

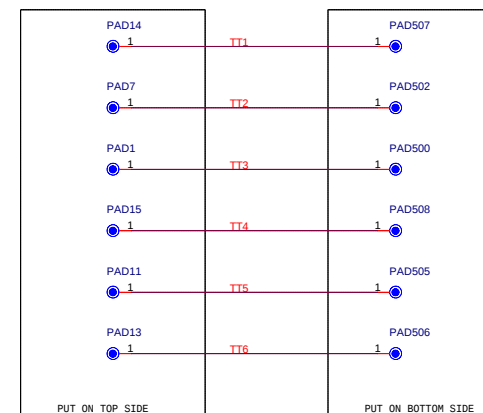
FID7
FIDUCIAL
 本PIN不可接任何信號或電源
CAD-016
FIDUCIAL MARK 光學定位用

FID1
FIDUCIAL
 本PIN不可接任何信號或電源
CAD-016
FIDUCIAL MARK 光學定位用

FID4
FIDUCIAL
 本PIN不可接任何信號或電源
CAD-016
FIDUCIAL MARK 光學定位用

FID5
FIDUCIAL
 本PIN不可接任何信號或電源
CAD-016
FIDUCIAL MARK 光學定位用

FID8
FIDUCIAL
 本PIN不可接任何信號或電源
CAD-016
FIDUCIAL MARK 光學定位用



EVENLY SPREAD AROUND THE PCB

Arima

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A00: INITIAL DESIGN ON MAY 7, 2002

MODIFY LIST: 1. Lead free PCB gerber files must send to Ger Chen (陳德吉) before making stencil.

2. Lead free PCB is required to plate with gold. (PCB要鍍金處理)

3. "Clock Generator" to CPU clock signal (HCLK_C0) changes from pin-44 (clock gen.) to pin-47. (BIOS modified the function already. 2002/5/23)

4. "VCOREOK" signal level is raising two steps for "VIAC3_PWRGD". First step is 0V to 0.7V, and the second step is 0.7V to 2.5V. The solution to the bug is as following:

- (a) Page 7 some components need to be changed.
- (b) Remove D14 (diode), and R759 (330 Ohm)
- (c) Add an BJT 3904 (P-channel)
- (d) B -> "SYS_PWR_GD" signal, C -> connecting 1K Ohm and pulling to 2.5VS, E -> connecting "VIAC3_PWRGD" signal and pulling 10K Ohm to ground.
- (e) Remove R730 (0 Ohm)
- (f) Add U523 (7417 single gate buffer)
- (g) Short U30 pin 9 and 10 (short "7417_VCOREOK" and "VRPWRGD") for AND gate output to high
- (h) Remove R238 (0 Ohm)
- (i) Add R240 (0 Ohm)

5. Intel CPU and VIA CPU have different dimension; therefore, their heat sinks have different types. 2002/5/28

6. BT1 and BT1+ have three USB ports (mechanical design), but BT1V has two USB ports (mechanical design). 2002/7/9

6.a.Pg.5 Add another 0 ohm resistor between GNDVGA and GND-----1pcs.

b.Pg.13 Add a 0.1uF bypass cap to CN5 Pin1.

c.Pg.37 CN502 Pin1 change to N.A from Net GND

d.Pg.37 Add a 0.1uF(BOM list N.A) bypass cap between CN502 Pin1 and GND

e.Pg.38 C175,C198,C181,C249,C234,C545,C551,C562,C566 change to 0.1uF from N.A

2002/10/28 EMI

HISTORY

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