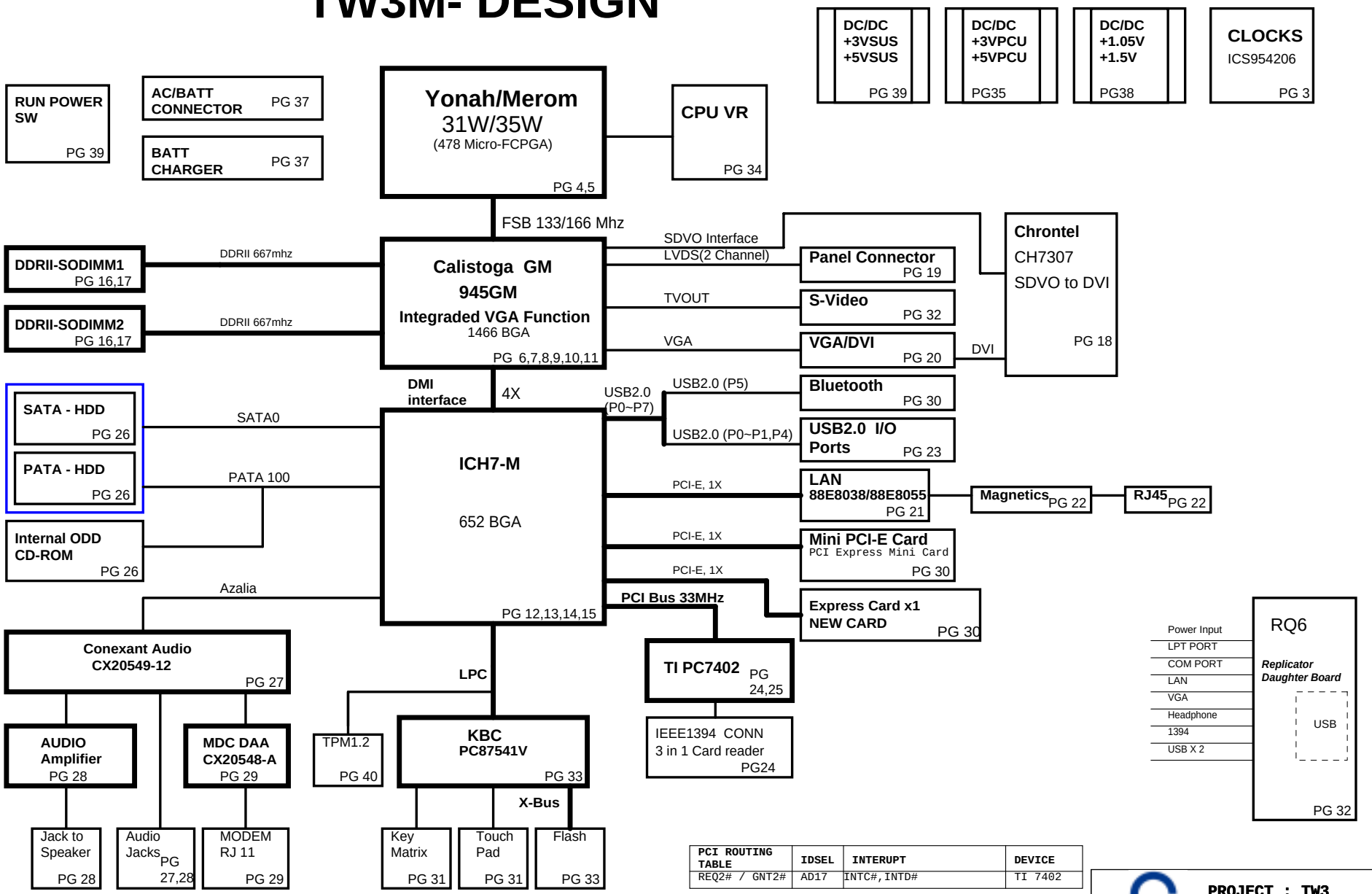
TW3M- DESIGN

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND1
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : IN3
- LAYER 7 : SGND2
- LAYER 8 : BOT



PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ2# / GNT2#	AD17	INTC#,INTD#	TI 7402

PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	Block Diagram	B2A

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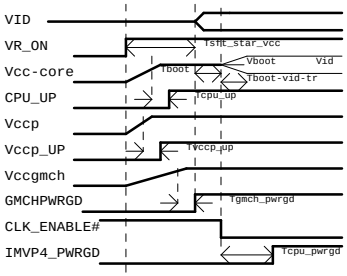
Board Stack up Description

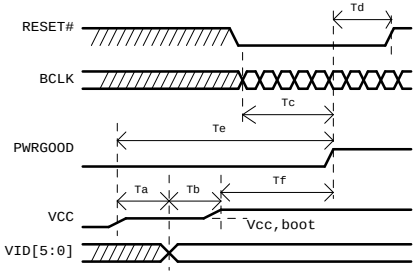
PCB Layers

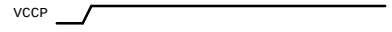
Layer 1		TOP(Component,Other)
Layer 2		Ground Plane
Layer 3		IN1
Layer 4		IN2
Layer 5		Power Plane
Layer 6		IN3
Layer 7		Ground Plane
Layer 8		BOTTOM

Power On Sequencing Timing Diagram



Dothan Power-up Timing Specifications



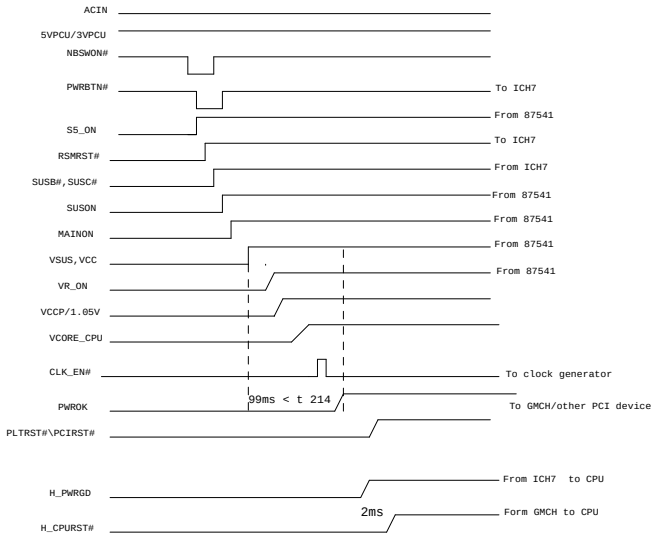


Ta=VCC and VCCP asseration to VID[5:0] vaild
Tb=VID[5:0] stable to VCC vaild
Tc=BCLK stable to PWRGOOD assertion
Td=PWRGOOD to RESET# de-assertion time
Te=Vcc,boot vaild to PWRGOOD assertion time

Voltage Rails

Voltage Rails		ON S0~S2	ON S3	ON S4	ON S5	Control signal
VCC_CORE	Core voltage for Processor	X				VR_ON 0.726V~0.94V
VCCP	Core voltage for CPU / NB	X				VR_ON
SMDDR_VTERM	0.9V for DDR2 Termination voltage	X				MAINON
RVCC1.5		X	X	X		RVCC_ON
RVCC3		X	X	X		RVCCD
VCC1.5		X				MAIND
VCC2.5		X				MAINON
VCC3		X				MAIND
VCC5		X				MAIND
1.8VSUS		X	X			SUSON
3VSUS		X	X			SUSD
5VSUS		X	X			SUSD
3VPCU		X	X	X	X	VL
5VPCU		X	X	X	X	VL
9VPCU		X	X	X	X	5VPCU

ACIN POWER ON TIMING



Voltage Rails		ON S0~S1	ON S3	ON S4	ON S5	Control signal
VCC_CORE	Core voltage for Processor	X				VRON
GMCH_VTT	Core voltage for GMCH 1.05V	X				MAINON
SMDDR_VTERM	0.9V for DDR II Termination voltage	X				MAINON
SMDDR_VREF	0.9V for DDR II Reference Voltage	X				MAINON
GMCH_1.5V		X				MAINON
1.8VSUS	1.8V for DDR II voltage	X	X			SUSON
+2.5V		X				MAINON
3VPCU		X	X	X	X	VL
3VSUS		X	X			SUSON
+3V		X				MAINON
5VPCU		X	X	X	X	VL
5VSUS		X	X			SUSON
+5V		X				MAINON
VIN	POWER SOURCE	X	X	X	X	

PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
PCI7402	AD17	REQ2# / GNT2#	PIRQ C/D

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Quanta Computer Inc.

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	System Information	82A

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FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

Place these termination to close CK410M. Cause those Pin-out is for Current-Mode.

R135 1 2 49.9/F
R131 1 2 49.9/F
R133 1 2 49.9/F
R134 1 2 49.9/F

C419 33p/50V XIN <500mil
Y1 14.318MHZ
C434 33p/50V XOUT

U13 CK-410M

XTAL_IN XTAL_OUT VDDA VSSA REF CPU0 CPU0# CPU1 CPU1# CPU2_ITP/SRC7 CPU2#_ITP/SRC7# SRC6 SRC6# SRC5 SRC5# SRC4 SRC4# SRC3 SRC3# SRC2 SRC2# SRC1 SRC1# SRC0 SRC0# PCI5 PCI4 PCI3 PCI2 PCIF1 PCIF0/ITP_EN

VTT_PWRGD#/PD# PCI_STOP# CPU_STOP# SCLK SDATA FSA/USB_48 FSB/TEST_MODE FSC/TEST_SEL VDD_REF VDD_CPU VDD_PCI_1 VDD_PCI_2 VDD_SRC0 VDD_SRC1 VDD_SRC2 VDD_48 IREF DOT96 DOT96# GND_48 GND_REF GND_PCI_1 GND_PCI_2 GND_SRC GND_CPU

14,37 CLK_EN# CLK_EN#
14 PM_STPPCI# PM_STPPCI#
14 PM_STPCPU# PM_STPCPU#
28 TI_CLK48M TI_CLK48M R181 10
14 CLKUSB_48 CLKUSB_48 R180 10

SMbus address D2
CGCLK_SMB CGDAT_SMB

4,7 CPU_MCH_BSEL0
4,7 CPU_MCH_BSEL1
4,7 CPU_MCH_BSEL2
R426 8.2K/F FSA
R408 8.2K/F FSC

+3VRUN
R172 10K
FSA
R171 *10K_NC

VDDREF_CR CLKVDD
CLKVDD1
CLKVDD
VDD48_CR

R132 475/F IREF
Iref=5mA, Ioh=4*Iref

7 DOT96 7 DOT96# 33x2 RP35 R_DOT96 R_DOT96#

14M_REF R145 33/F 14M_ICH 14
C405 *10p

RP33 R_HCLK_CPU R_HCLK_CPU# 33x2 CLK_CPU_BCLK 4 CLK_CPU_BCLK# 4
RP34 R_HCLK_MCH R_HCLK_MCH# 33x2 CLK_MCH_BCLK 6 CLK_MCH_BCLK# 6
RP31 R_PCIE_LAN R_PCIE_LAN# 33x2 CLK_PCIE_LAN 24 CLK_PCIE_LAN# 24
RP32 R_MCH_3GPLL R_MCH_3GPLL# 33x2 CLK_PCIE_3GPLL 7 CLK_PCIE_3GPLL# 7
RP40 R_PCIE_SATA R_PCIE_SATA# 33x2 CLK_PCIE_SATA 12 CLK_PCIE_SATA# 12
RP39 R_PCIE_ICH R_PCIE_ICH# 33x2 CLK_PCIE_ICH 13 CLK_PCIE_ICH# 13
RP38 R_PCIE_MINI R_PCIE_MINI# 33x2 CLK_PCIE_MINI 33 CLK_PCIE_MINI# 33
RP37 R_PCIE_NEW R_PCIE_NEW# 33x2 CLK_PCIE_NEW_C 33 CLK_PCIE_NEW_C# 33
RP50 R_DREFSSCLK R_DREFSSCLK# 33x2 DREFSSCLK 7 DREFSSCLK# 7

R_PCLK_SIO R169 33/F PCLK_541 36
R_PCLK_PCM R176 33/F PCLK_PCM 27
R_PCLK_LPC_DEBUG R173 33/F PCLK_LPC_DEBUG 33
R_PCLK_TPM R144 *33_4 PCLK_TPM 44
R_PCLK_ICH R179 33/F PCLK_ICH 13

R177 10K
R170 *10K +3VRUN
R178 10K

PCIF1
1:100 Mhz
0:96 Mhz

0816a

CT_0505: Change footprint to TSSOP56-8_1-5 from TSSOP56-240

ICS954206AGLFT
250mA (MAX.)

Bypass CAPs need to follow Bypass CAP. Routing Rule, no vias between CAP to CHIPSET VCC Pin or GND.

Tie to VCC (Logic 1) is for ITP using.
Tie to GND (Logic 0) is for PCIE using.

120 ohms@100Mhz L21 HB-1T2012-121JT
+3VRUN
C438 0.047u/10V C408 0.047u/10V C445 0.047u/10V C406 0.047u/10V C432 4.7u/10V_8
CLKVDD
R149 2.2_6 VDDA_CR
C409 0.047u/10V C388 4.7u/10V_8

120 ohms@100Mhz L22 HB-1T2012-121JT
+3VRUN
C446 0.047u/10V C443 0.047u/10V C441 4.7u/10V_8
CLKVDD1
R175 2.2_6 VDD48_CR
C444 0.047u/10V C454 4.7u/10V_8
R146 1/F_6 VDDREF_CR
C407 0.047u/10V

Connect ICH6 SMB
14,33 PDAT_SMB PDAT_SMB Q22 RHU002N06
RP27 2.2Kx2
CGDAT_SMB CGDAT_SMB 16
Connect DDR Module's SMB

These are for backdrive issue

CT_0229: Change MOS to RHU002N06 due to layout concern.

+3VRUN Q23 RHU002N06
14,33 PCLK_SMB PCLK_SMB
CGCLK_SMB CGCLK_SMB 16

CLK_PCIE_LAN CLK_PCIE_LAN# RP29 49.9x2
CLK_PCIE_MINI CLK_PCIE_MINI# RP42 49.9x2
CLK_PCIE_NEW_C CLK_PCIE_NEW_C# RP41 49.9x2
CLK_MCH_3GPLL CLK_MCH_3GPLL# RP30 49.9x2
CLK_PCIE_SATA CLK_PCIE_SATA# RP44 49.9x2
CLK_PCIE_ICH CLK_PCIE_ICH# RP43 49.9x2
DREFSSCLK DREFSSCLK# RP55 49.9x2
DOT96 DOT96# RP51 49.9x2

Place these termination to close CK410M. Cause those Pin-out is for Current-Mode.

PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	CLOCK GENERATOR	B2A
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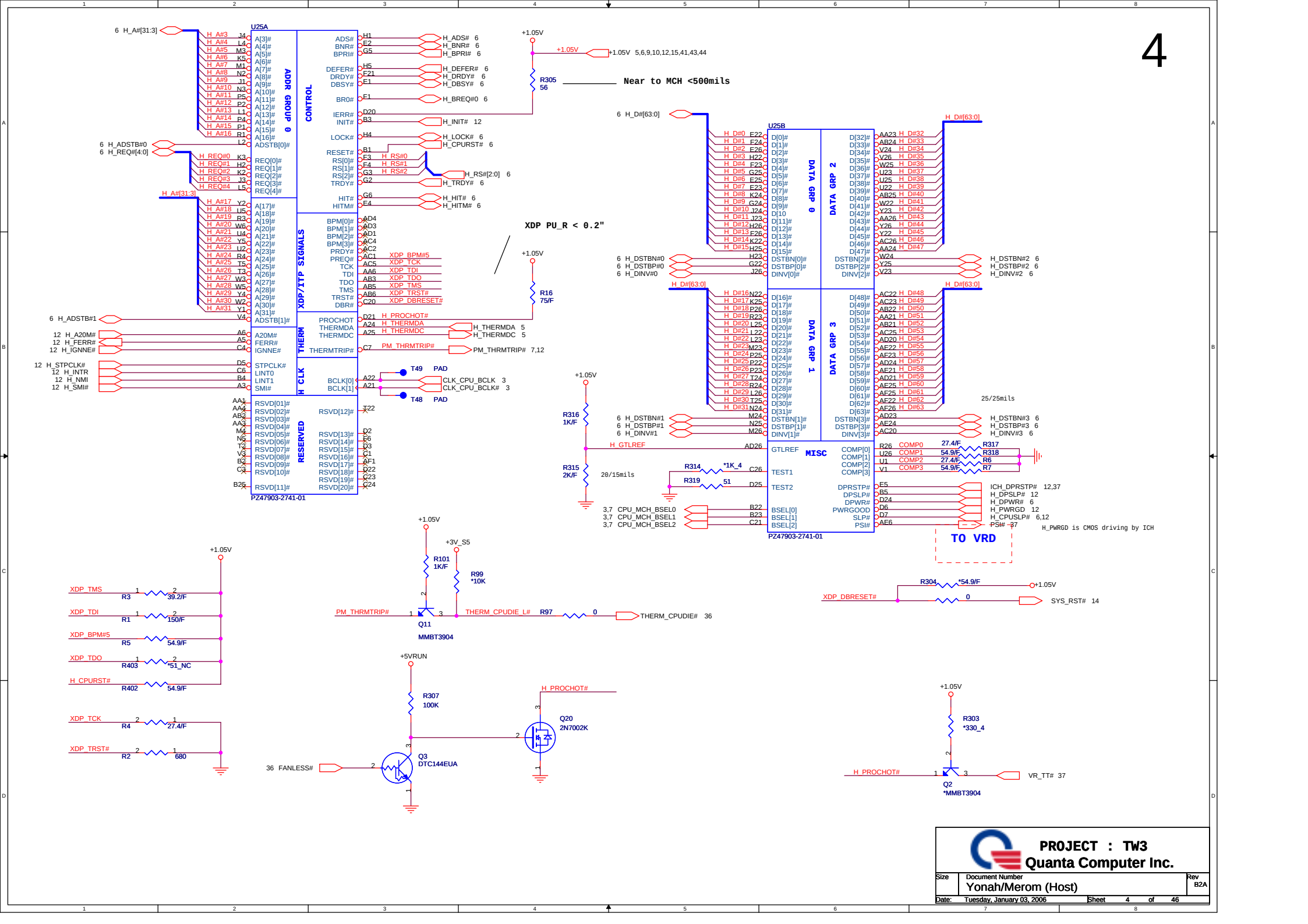
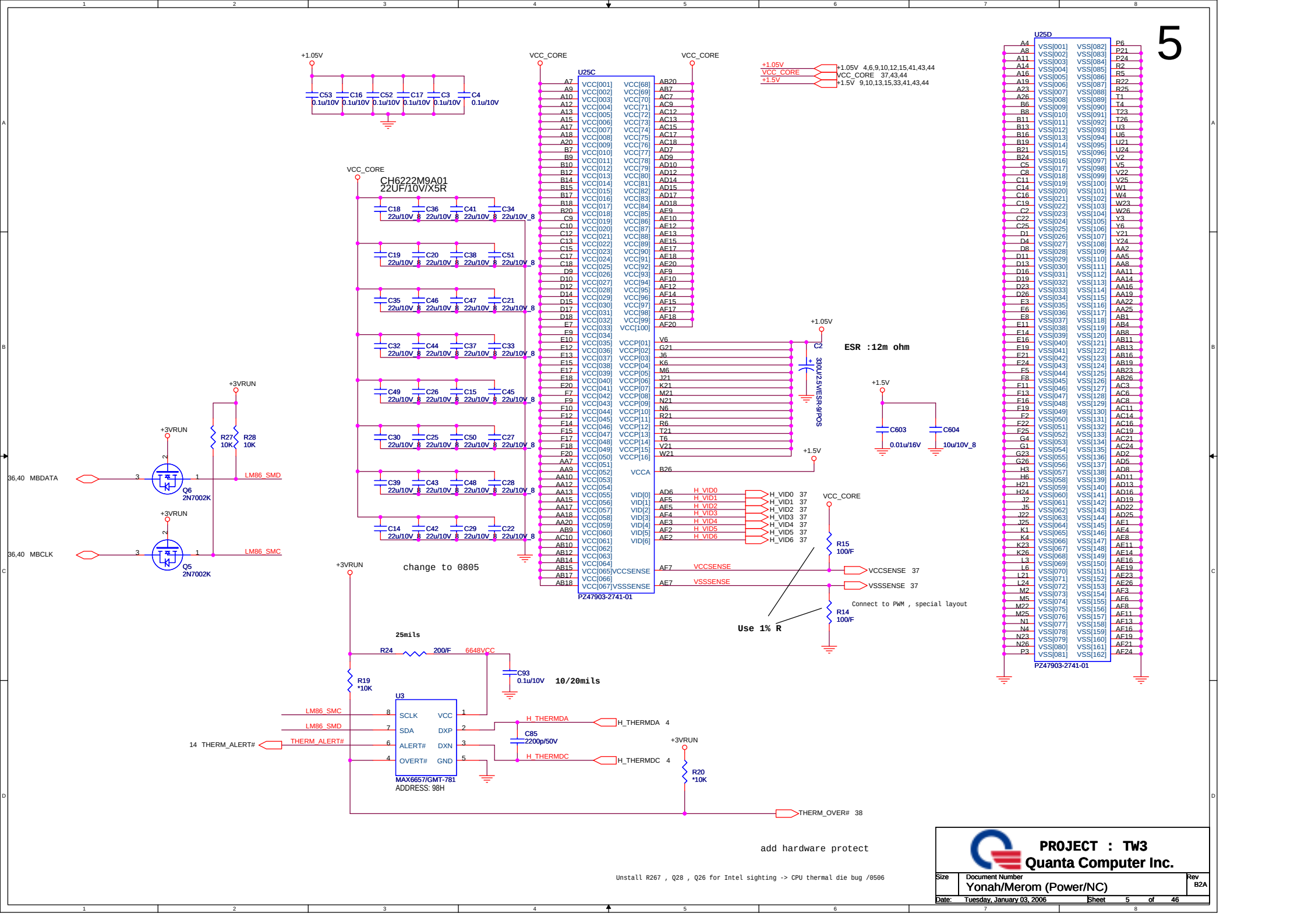

U25A
ADDR GROUP 0
CONTROL
XDP/ITP SIGNALS
THERM
H CLK
RESERVED
PZ47903-2741-01
U25B
DATA GRP 0
DATA GRP 2
DATA GRP 1
DATA GRP 3
MISC
PZ47903-2741-01
Near to MCH <500mils
XDP PU_R < 0.2"
25/25mils
TO VRD
H_PWRGD is CMOS driving by ICH
PROJECT : TW3
Quanta Computer Inc.
Yonah/Merom (Host)
Tuesday, January 03, 2006


5
+1.05V
VCC_CORE
C53 0.1u/10V
C16 0.1u/10V
C52 0.1u/10V
C17 0.1u/10V
C3 0.1u/10V
C4 0.1u/10V
U25C
PZ47903-2741-01
+1.05V 4,6,9,10,12,15,41,43,44
VCC_CORE 37,43,44
+1.5V 9,10,13,15,33,41,43,44
U25D
PZ47903-2741-01
CH6222M9A01
22UF/10V/X5R
C18 22u/10V_8
C36 22u/10V_8
C41 22u/10V_8
C34 22u/10V_8
C19 22u/10V_8
C20 22u/10V_8
C38 22u/10V_8
C51 22u/10V_8
C35 22u/10V_8
C46 22u/10V_8
C47 22u/10V_8
C21 22u/10V_8
C32 22u/10V_8
C44 22u/10V_8
C37 22u/10V_8
C33 22u/10V_8
C49 22u/10V_8
C26 22u/10V_8
C15 22u/10V_8
C45 22u/10V_8
C30 22u/10V_8
C25 22u/10V_8
C50 22u/10V_8
C27 22u/10V_8
C39 22u/10V_8
C43 22u/10V_8
C48 22u/10V_8
C28 22u/10V_8
C14 22u/10V_8
C42 22u/10V_8
C29 22u/10V_8
C22 22u/10V_8
change to 0805
C2
330U/2.5V/ESR-9/POS
ESR :12m ohm
C603 0.01u/16V
C604 10u/10V_8
+3VRUN
R27 10K
R28 10K
Q6 2N7002K
Q5 2N7002K
36,40 MBDATA
36,40 MBCLK
LM86_SMD
LM86_SMC
H_VID0 37
H_VID1 37
H_VID2 37
H_VID3 37
H_VID4 37
H_VID5 37
H_VID6 37
VCCSENSE 37
VSSSENSE 37
R15 100/F
R14 100/F
Use 1% R
Connect to PWM , special layout
25mils
R24 200/F 6648VCC
C93 0.1u/10V
10/20mils
R19 *10K
U3
MAX6657/GMT-781
ADDRESS: 98H
SCLK
SDA
ALERT#
OVERT#
VCC
DXP
DXN
GND
H_THERMDA
H_THERMDC
C85 2200p/50V
H_THERMDA 4
H_THERMDC 4
14 THERM_ALERT#
R20 *10K
THERM_OVER# 38
add hardware protect
Unstall R267 , Q28 , Q26 for Intel sighting -> CPU thermal die bug /0506
PROJECT : TW3
Quanta Computer Inc.
Size
Document Number
Yonah/Merom (Power/NC)
Rev
B2A
Date: Tuesday, January 03, 2006
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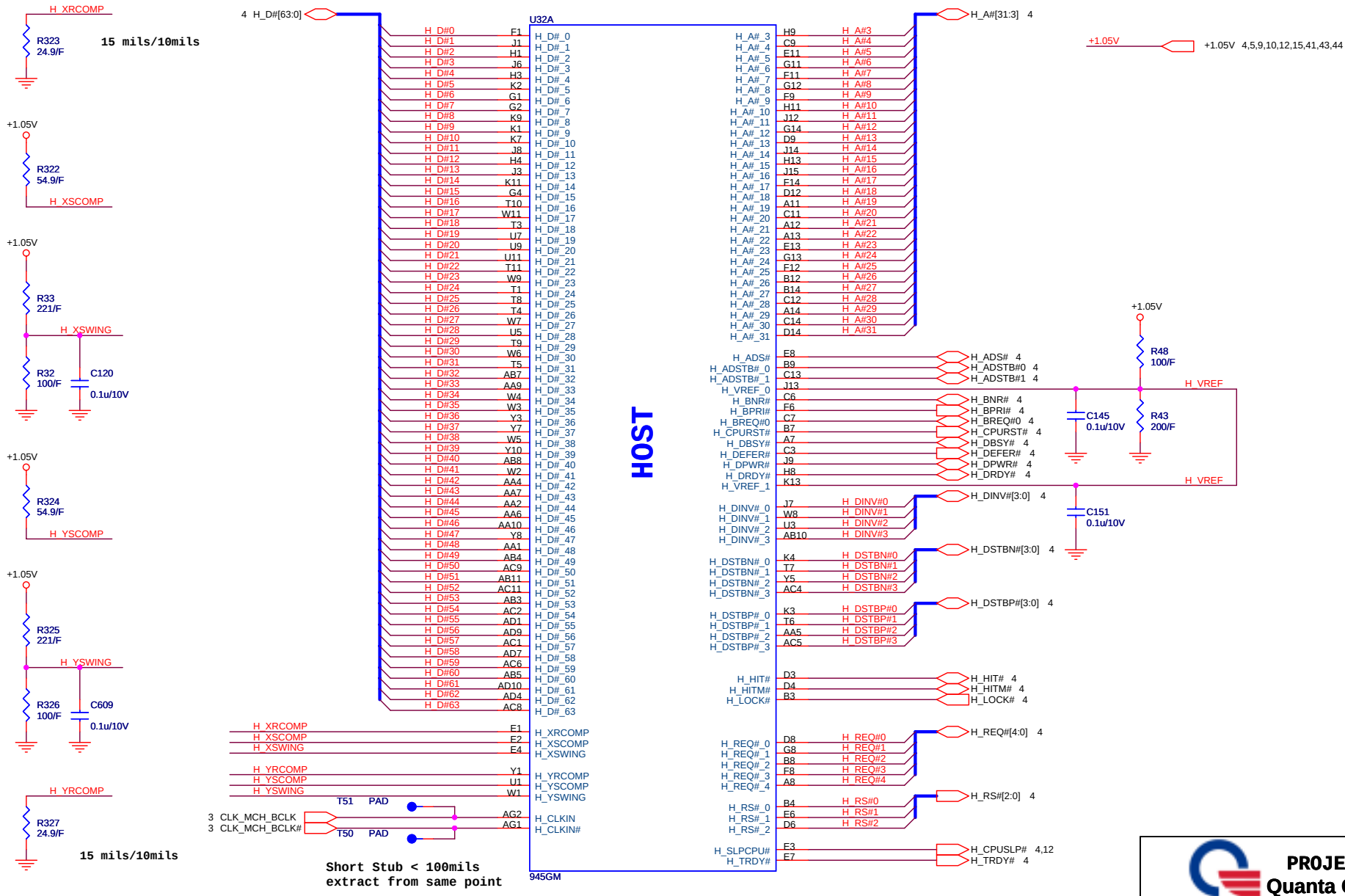
H_XRCOMP
R323 24.9/F
15 mils/10mils
+1.05V
R322 54.9/F
H_XSCOMP
+1.05V
R33 221/F
H_XSWING
R32 100/F
C120 0.1u/10V
+1.05V
R324 54.9/F
H_YSCOMP
+1.05V
R325 221/F
H_YSWING
R326 100/F
C609 0.1u/10V
H_YRCOMP
R327 24.9/F
15 mils/10mils
4 H_D#[63:0]
U32A
HOST
945GM
H_D#0 F1 H_D#_0
H_D#1 J1 H_D#_1
H_D#2 H1 H_D#_2
H_D#3 J6 H_D#_3
H_D#4 H3 H_D#_4
H_D#5 K2 H_D#_5
H_D#6 G1 H_D#_6
H_D#7 G2 H_D#_7
H_D#8 K9 H_D#_8
H_D#9 K1 H_D#_9
H_D#10 K7 H_D#_10
H_D#11 J8 H_D#_11
H_D#12 H4 H_D#_12
H_D#13 J3 H_D#_13
H_D#14 K11 H_D#_14
H_D#15 G4 H_D#_15
H_D#16 T10 H_D#_16
H_D#17 W11 H_D#_17
H_D#18 T3 H_D#_18
H_D#19 U7 H_D#_19
H_D#20 U9 H_D#_20
H_D#21 U11 H_D#_21
H_D#22 T11 H_D#_22
H_D#23 W9 H_D#_23
H_D#24 T1 H_D#_24
H_D#25 T8 H_D#_25
H_D#26 T4 H_D#_26
H_D#27 W7 H_D#_27
H_D#28 U5 H_D#_28
H_D#29 T9 H_D#_29
H_D#30 W6 H_D#_30
H_D#31 T5 H_D#_31
H_D#32 AB7 H_D#_32
H_D#33 AA9 H_D#_33
H_D#34 W4 H_D#_34
H_D#35 W3 H_D#_35
H_D#36 Y3 H_D#_36
H_D#37 Y7 H_D#_37
H_D#38 W5 H_D#_38
H_D#39 Y10 H_D#_39
H_D#40 AB8 H_D#_40
H_D#41 W2 H_D#_41
H_D#42 AA4 H_D#_42
H_D#43 AA7 H_D#_43
H_D#44 AA2 H_D#_44
H_D#45 AA6 H_D#_45
H_D#46 AA10 H_D#_46
H_D#47 Y8 H_D#_47
H_D#48 AA1 H_D#_48
H_D#49 AB4 H_D#_49
H_D#50 AC9 H_D#_50
H_D#51 AB11 H_D#_51
H_D#52 AC11 H_D#_52
H_D#53 AB3 H_D#_53
H_D#54 AC2 H_D#_54
H_D#55 AD1 H_D#_55
H_D#56 AD9 H_D#_56
H_D#57 AC1 H_D#_57
H_D#58 AD7 H_D#_58
H_D#59 AC6 H_D#_59
H_D#60 AB5 H_D#_60
H_D#61 AD10 H_D#_61
H_D#62 AD4 H_D#_62
H_D#63 AC8 H_D#_63
H_XRCOMP F1 H_XRCOMP
H_XSCOMP F2 H_XSCOMP
H_XSWING E4 H_XSWING
H_YRCOMP Y1 H_YRCOMP
H_YSCOMP U1 H_YSCOMP
H_YSWING W1 H_YSWING
T51 PAD
3 CLK_MCH_BCLK AG2 H_CLKIN
3 CLK_MCH_BCLK# AG1 H_CLKIN#
T50 PAD
Short Stub < 100mils
extract from same point
H_A#_3 H9 H_A#3
H_A#_4 C9 H_A#4
H_A#_5 E11 H_A#5
H_A#_6 G11 H_A#6
H_A#_7 F11 H_A#7
H_A#_8 G12 H_A#8
H_A#_9 F9 H_A#9
H_A#_10 H11 H_A#10
H_A#_11 J12 H_A#11
H_A#_12 G14 H_A#12
H_A#_13 D9 H_A#13
H_A#_14 J14 H_A#14
H_A#_15 H13 H_A#15
H_A#_16 J15 H_A#16
H_A#_17 F14 H_A#17
H_A#_18 D12 H_A#18
H_A#_19 A11 H_A#19
H_A#_20 C11 H_A#20
H_A#_21 A12 H_A#21
H_A#_22 A13 H_A#22
H_A#_23 E13 H_A#23
H_A#_24 G13 H_A#24
H_A#_25 F12 H_A#25
H_A#_26 B12 H_A#26
H_A#_27 B14 H_A#27
H_A#_28 C12 H_A#28
H_A#_29 A14 H_A#29
H_A#_30 C14 H_A#30
H_A#_31 D14 H_A#31
H_A#[31:3] 4
+1.05V
+1.05V 4,5,9,10,12,15,41,43,44
H_ADS# E8 H_ADS# 4
H_ADSTB#_0 B9 H_ADSTB#0 4
H_ADSTB#_1 C13 H_ADSTB#1 4
H_VREF_0 J13
H_BNR# C6 H_BNR# 4
H_BPRI# F6 H_BPRI# 4
H_BREQ#0 C7 H_BREQ#0 4
H_CPURST# B7 H_CPURST# 4
H_DBSY# A7 H_DBSY# 4
H_DEFER# C3 H_DEFER# 4
H_DPWR# J9 H_DPWR# 4
H_DRDY# H8 H_DRDY# 4
H_VREF_1 K13
+1.05V
R48 100/F
H_VREF
C145 0.1u/10V
R43 200/F
H_VREF
C151 0.1u/10V
H_DINV#_0 J7 H_DINV#0
H_DINV#_1 W8 H_DINV#1
H_DINV#_2 U3 H_DINV#2
H_DINV#_3 AB10 H_DINV#3
H_DINV#[3:0] 4
H_DSTBN#_0 K4 H_DSTBN#0
H_DSTBN#_1 T7 H_DSTBN#1
H_DSTBN#_2 Y5 H_DSTBN#2
H_DSTBN#_3 AC4 H_DSTBN#3
H_DSTBN#[3:0] 4
H_DSTBP#_0 K3 H_DSTBP#0
H_DSTBP#_1 T6 H_DSTBP#1
H_DSTBP#_2 AA5 H_DSTBP#2
H_DSTBP#_3 AC5 H_DSTBP#3
H_DSTBP#[3:0] 4
H_HIT# D3 H_HIT# 4
H_HITM# D4 H_HITM# 4
H_LOCK# B3 H_LOCK# 4
H_REQ#_0 D8 H_REQ#0
H_REQ#_1 G8 H_REQ#1
H_REQ#_2 B8 H_REQ#2
H_REQ#_3 F8 H_REQ#3
H_REQ#_4 A8 H_REQ#4
H_REQ#[4:0] 4
H_RS#_0 B4 H_RS#0
H_RS#_1 E6 H_RS#1
H_RS#_2 D6 H_RS#2
H_RS#[2:0] 4
H_SLPCPU# E3 H_CPUSLP# 4,12
H_TRDY# E7 H_TRDY# 4
PROJECT : TW3
Quanta Computer Inc.
Size
Document Number
Calistoga_A(Host)
Rev
B2A
Date: Tuesday, January 03, 2006
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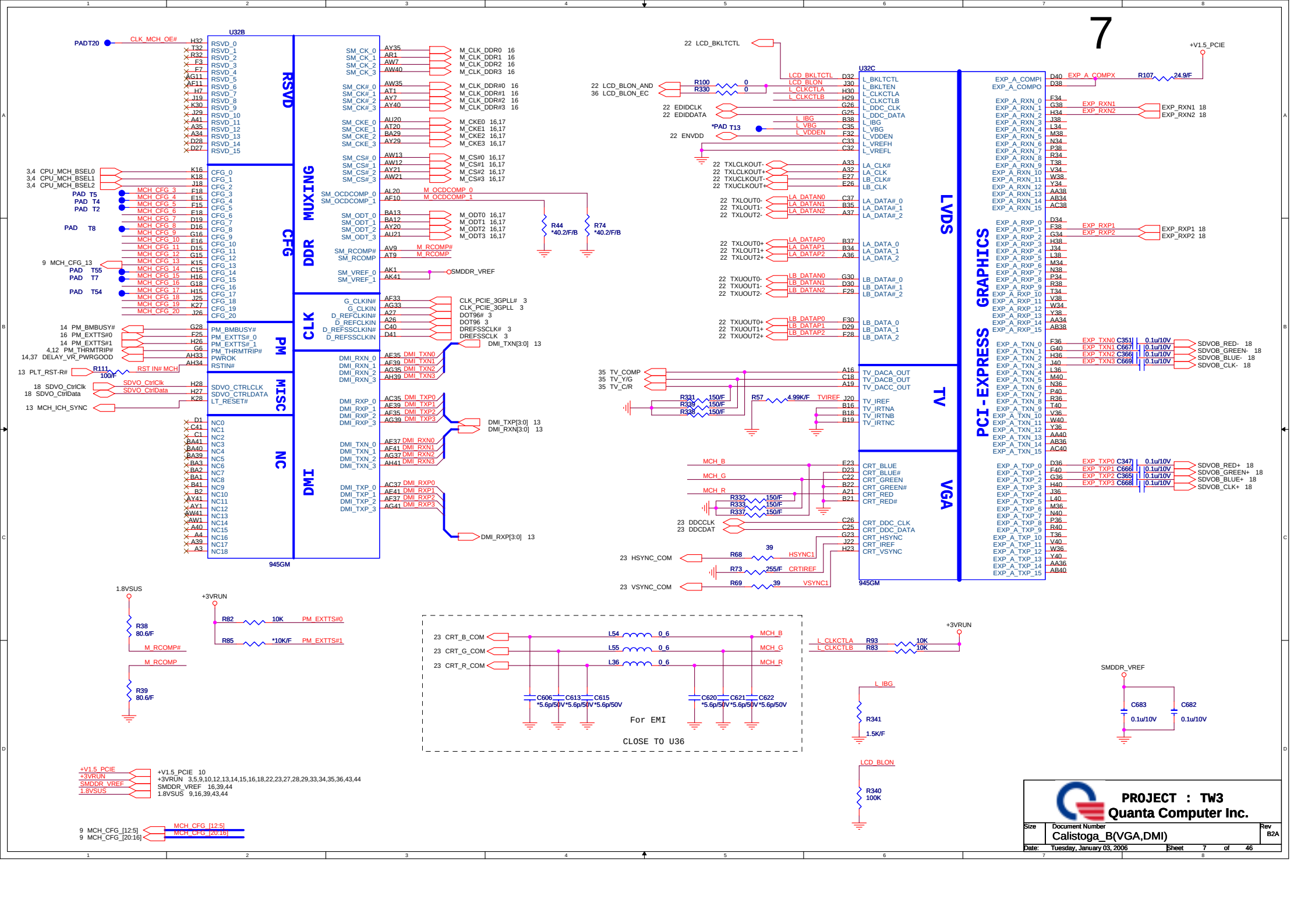
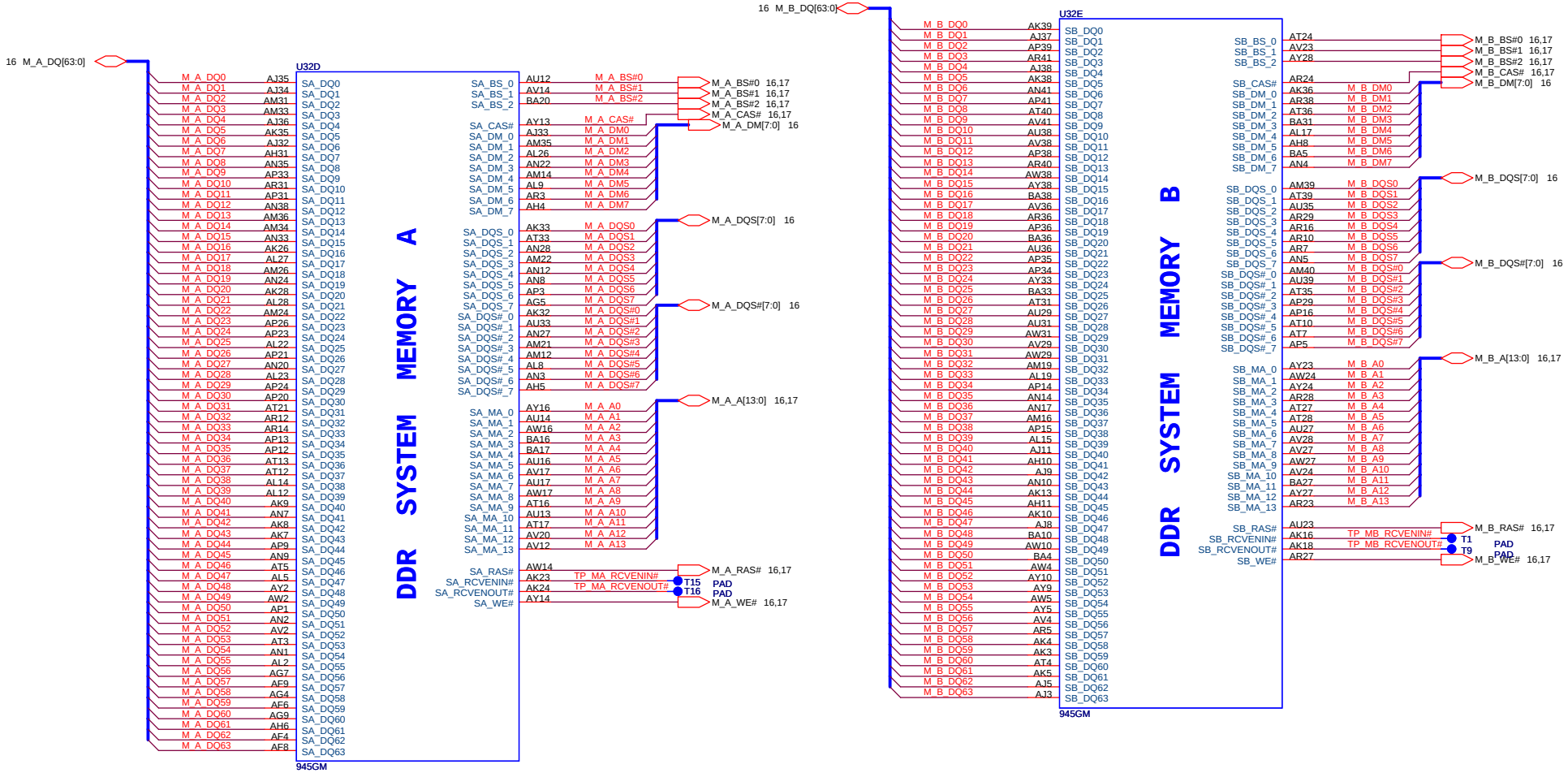
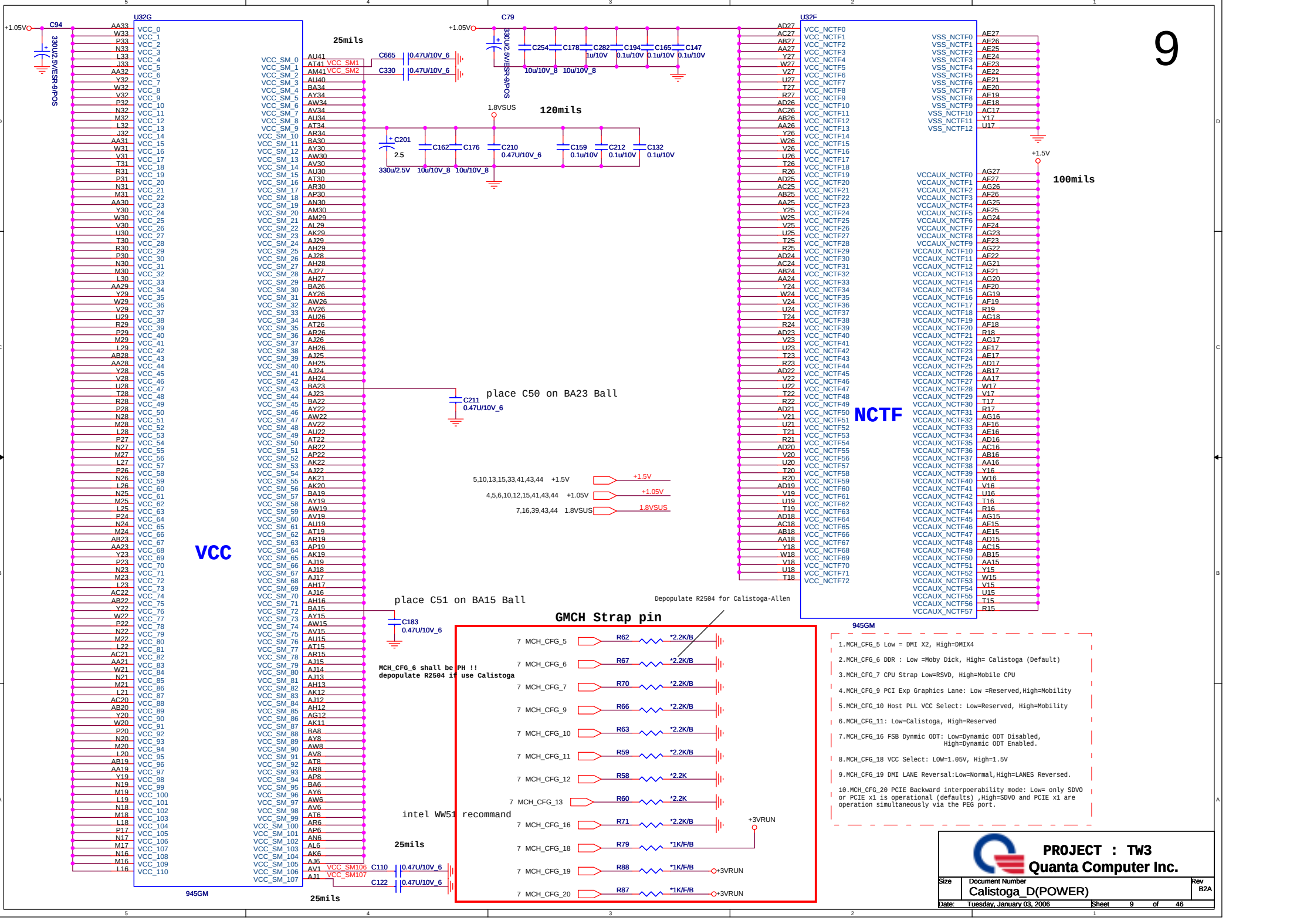

7
U32B
RSVD
CFG
PM
MISC
NC
945GM
DDR MUXING
CLK
DMI
U32C
LVDS
TV
VGA
945GM
PCI-EXPRESS GRAPHICS
PADT20
CLK_MCH_OE#
RSVD_0
RSVD_1
RSVD_2
RSVD_3
RSVD_4
RSVD_5
RSVD_6
RSVD_7
RSVD_8
RSVD_9
RSVD_10
RSVD_11
RSVD_12
RSVD_13
RSVD_14
RSVD_15
CFG_0
CFG_1
CFG_2
CFG_3
CFG_4
CFG_5
CFG_6
CFG_7
CFG_8
CFG_9
CFG_10
CFG_11
CFG_12
CFG_13
CFG_14
CFG_15
CFG_16
CFG_17
CFG_18
CFG_19
CFG_20
3,4 CPU_MCH_BSEL0
3,4 CPU_MCH_BSEL1
3,4 CPU_MCH_BSEL2
PAD T5
PAD T4
PAD T2
PAD T8
MCH_CFG_3
MCH_CFG_4
MCH_CFG_5
MCH_CFG_6
MCH_CFG_7
MCH_CFG_8
MCH_CFG_9
MCH_CFG_10
MCH_CFG_11
MCH_CFG_12
MCH_CFG_13
MCH_CFG_14
MCH_CFG_15
MCH_CFG_16
MCH_CFG_17
MCH_CFG_18
MCH_CFG_19
MCH_CFG_20
9 MCH_CFG_13
PAD T55
PAD T7
PAD T54
PM_BMBUSY#
PM_EXTTS#_0
PM_EXTTS#_1
PM_THRMTRIP#
PWROK
RSTIN#
14 PM_BMBUSY#
16 PM_EXTTS#0
14 PM_EXTTS#1
4,12 PM_THRMTRIP#
14,37 DELAY_VR_PWRGOOD
13 PLT_RST-R#
R111
100/F
RST IN# MCH
SDVO_CTRLCLK
SDVO_CTRLDATA
LT_RESET#
18 SDVO_CtrlClk
18 SDVO_CtrlData
13 MCH_ICH_SYNC
SDVO_CtrlClk
SDVO_CtrlData
NC0
NC1
NC2
NC3
NC4
NC5
NC6
NC7
NC8
NC9
NC10
NC11
NC12
NC13
NC14
NC15
NC16
NC17
NC18
SM_CK_0
SM_CK_1
SM_CK_2
SM_CK_3
SM_CK#_0
SM_CK#_1
SM_CK#_2
SM_CK#_3
SM_CKE_0
SM_CKE_1
SM_CKE_2
SM_CKE_3
SM_CS#_0
SM_CS#_1
SM_CS#_2
SM_CS#_3
SM_OCDCOMP_0
SM_OCDCOMP_1
SM_ODT_0
SM_ODT_1
SM_ODT_2
SM_ODT_3
SM_RCOMP#
SM_RCOMP
SM_VREF_0
SM_VREF_1
M_CLK_DDR0 16
M_CLK_DDR1 16
M_CLK_DDR2 16
M_CLK_DDR3 16
M_CLK_DDR#0 16
M_CLK_DDR#1 16
M_CLK_DDR#2 16
M_CLK_DDR#3 16
M_CKE0 16,17
M_CKE1 16,17
M_CKE2 16,17
M_CKE3 16,17
M_CS#0 16,17
M_CS#1 16,17
M_CS#2 16,17
M_CS#3 16,17
M_OCDCOMP_0
M_OCDCOMP_1
M_ODT0 16,17
M_ODT1 16,17
M_ODT2 16,17
M_ODT3 16,17
M_RCOMP#
M_RCOMP
SMDDR_VREF
R44 *40.2/F/B
R74 *40.2/F/B
G_CLKIN#
G_CLKIN
D_REFCLKIN#
D_REFCLKIN
D_REFSSCLKIN#
D_REFSSCLKIN
CLK_PCIE_3GPLL# 3
CLK_PCIE_3GPLL 3
DOT96# 3
DOT96 3
DREFSSCLK# 3
DREFSSCLK 3
DMI_TXN[3:0] 13
DMI_RXN_0
DMI_RXN_1
DMI_RXN_2
DMI_RXN_3
DMI_TXN0
DMI_TXN1
DMI_TXN2
DMI_TXN3
DMI_RXP_0
DMI_RXP_1
DMI_RXP_2
DMI_RXP_3
DMI_TXP0
DMI_TXP1
DMI_TXP2
DMI_TXP3
DMI_TXP[3:0] 13
DMI_RXN[3:0] 13
DMI_TXN_0
DMI_TXN_1
DMI_TXN_2
DMI_TXN_3
DMI_RXN0
DMI_RXN1
DMI_RXN2
DMI_RXN3
DMI_TXP_0
DMI_TXP_1
DMI_TXP_2
DMI_TXP_3
DMI_RXP0
DMI_RXP1
DMI_RXP2
DMI_RXP3
DMI_RXP[3:0] 13
22 LCD_BKLTCTL
22 LCD_BLON_AND
36 LCD_BLON_EC
R100
R330
0
0
22 EDIDCLK
22 EDIDDATA
*PAD T13
22 ENVDD
22 TXLCLKOUT-
22 TXLCLKOUT+
22 TXUCLKOUT-
22 TXUCLKOUT+
22 TXLOUT0-
22 TXLOUT1-
22 TXLOUT2-
22 TXLOUT0+
22 TXLOUT1+
22 TXLOUT2+
22 TXUOUT0-
22 TXUOUT1-
22 TXUOUT2-
22 TXUOUT0+
22 TXUOUT1+
22 TXUOUT2+
35 TV_COMP
35 TV_Y/G
35 TV_C/R
R331 150/F
R335 150/F
R338 150/F
R57 4.99K/F
TVIREF
MCH_B
MCH_G
MCH_R
R332 150/F
R333 150/F
R337 150/F
23 DDCCLK
23 DDCDAT
23 HSYNC_COM
23 VSYNC_COM
R68 39
HSYNC1
R73 255/F
CRTIREF
R69 39
VSYNC1
+V1.5_PCIE
EXP_A_COMPI
EXP_A_COMPO
EXP_A_COMPX
R107 24.9/F
EXP_A_RXN_0
EXP_A_RXN_1
EXP_A_RXN_2
EXP_A_RXN_3
EXP_A_RXN_4
EXP_A_RXN_5
EXP_A_RXN_6
EXP_A_RXN_7
EXP_A_RXN_8
EXP_A_RXN_9
EXP_A_RXN_10
EXP_A_RXN_11
EXP_A_RXN_12
EXP_A_RXN_13
EXP_A_RXN_14
EXP_A_RXN_15
EXP_RXN1
EXP_RXN2
EXP_RXN1 18
EXP_RXN2 18
EXP_A_RXP_0
EXP_A_RXP_1
EXP_A_RXP_2
EXP_A_RXP_3
EXP_A_RXP_4
EXP_A_RXP_5
EXP_A_RXP_6
EXP_A_RXP_7
EXP_A_RXP_8
EXP_A_RXP_9
EXP_A_RXP_10
EXP_A_RXP_11
EXP_A_RXP_12
EXP_A_RXP_13
EXP_A_RXP_14
EXP_A_RXP_15
EXP_RXP1
EXP_RXP2
EXP_RXP1 18
EXP_RXP2 18
EXP_A_TXN_0
EXP_A_TXN_1
EXP_A_TXN_2
EXP_A_TXN_3
EXP_A_TXN_4
EXP_A_TXN_5
EXP_A_TXN_6
EXP_A_TXN_7
EXP_A_TXN_8
EXP_A_TXN_9
EXP_A_TXN_10
EXP_A_TXN_11
EXP_A_TXN_12
EXP_A_TXN_13
EXP_A_TXN_14
EXP_A_TXN_15
EXP_TXN0 C351
EXP_TXN1 C667
EXP_TXN2 C366
EXP_TXN3 C669
0.1u/10V
SDVOB_RED- 18
SDVOB_GREEN- 18
SDVOB_BLUE- 18
SDVOB_CLK- 18
EXP_A_TXP_0
EXP_A_TXP_1
EXP_A_TXP_2
EXP_A_TXP_3
EXP_A_TXP_4
EXP_A_TXP_5
EXP_A_TXP_6
EXP_A_TXP_7
EXP_A_TXP_8
EXP_A_TXP_9
EXP_A_TXP_10
EXP_A_TXP_11
EXP_A_TXP_12
EXP_A_TXP_13
EXP_A_TXP_14
EXP_A_TXP_15
EXP_TXP0 C347
EXP_TXP1 C666
EXP_TXP2 C365
EXP_TXP3 C668
SDVOB_RED+ 18
SDVOB_GREEN+ 18
SDVOB_BLUE+ 18
SDVOB_CLK+ 18
LA_CLK#
LA_CLK
LB_CLK#
LB_CLK
LA_DATA#_0
LA_DATA#_1
LA_DATA#_2
LA_DATA_0
LA_DATA_1
LA_DATA_2
LB_DATA#_0
LB_DATA#_1
LB_DATA#_2
LB_DATA_0
LB_DATA_1
LB_DATA_2
TV_DACA_OUT
TV_DACB_OUT
TV_DACC_OUT
TV_IREF
TV_IRTNA
TV_IRTNB
TV_IRTNC
CRT_BLUE
CRT_BLUE#
CRT_GREEN
CRT_GREEN#
CRT_RED
CRT_RED#
CRT_DDC_CLK
CRT_DDC_DATA
CRT_HSYNC
CRT_IREF
CRT_VSYNC
L_BKLTCTL
L_BKLTEN
L_CLKCTLA
L_CLKCTLB
L_DDC_CLK
L_DDC_DATA
L_IBG
L_VBG
L_VDDEN
L_VREFH
L_VREFL
L_BLON
1.8VSUS
+3VRUN
R38 80.6/F
R39 80.6/F
M_RCOMP#
M_RCOMP
R82 10K
R85 *10K/F
PM_EXTTS#0
PM_EXTTS#1
23 CRT_B_COM
23 CRT_G_COM
23 CRT_R_COM
L54 0_6
L55 0_6
L36 0_6
C606 *5.6p/50V
C613 *5.6p/50V
C615 *5.6p/50V
C620 *5.6p/50V
C621 *5.6p/50V
C622 *5.6p/50V
For EMI
CLOSE TO U36
L_CLKCTLA
L_CLKCTLB
R93 10K
R83 10K
L_IBG
R341 1.5K/F
LCD_BLON
R340 100K
SMDDR_VREF
C683 0.1u/10V
C682 0.1u/10V
+V1.5_PCIE 10
+3VRUN 3,5,9,10,12,13,14,15,16,18,22,23,27,28,29,33,34,35,36,43,44
SMDDR_VREF 16,39,44
1.8VSUS 9,16,39,43,44
9 MCH_CFG_[12:5]
9 MCH_CFG_[20:16]
MCH_CFG_[12:5]
MCH_CFG_[20:16]
PROJECT : TW3
Quanta Computer Inc.
Size
Document Number
Calistoga_B(VGA,DMI)
Rev
B2A
Date: Tuesday, January 03, 2006
Sheet 7 of 46

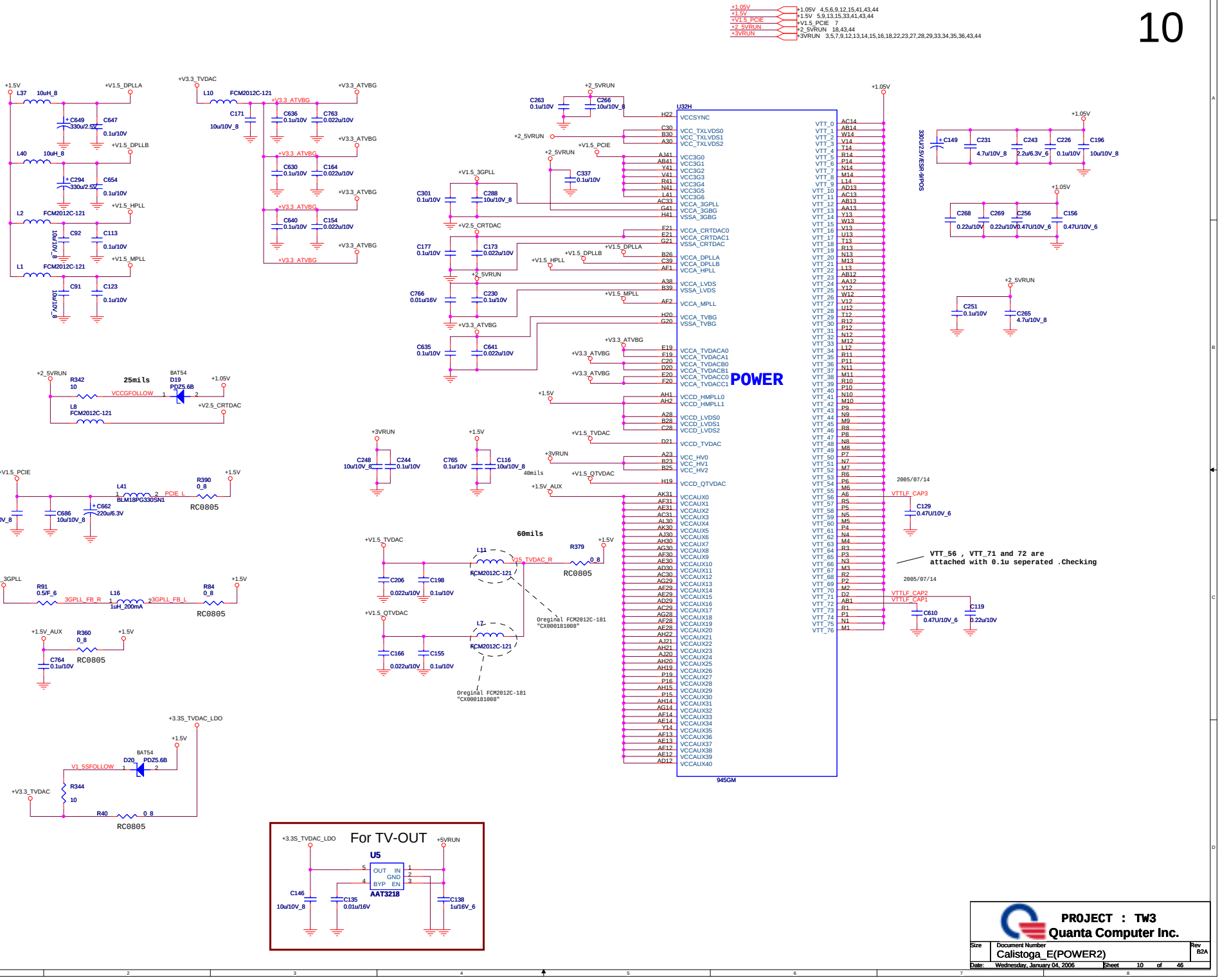


PROJECT : TW3
Quanta Computer Inc.

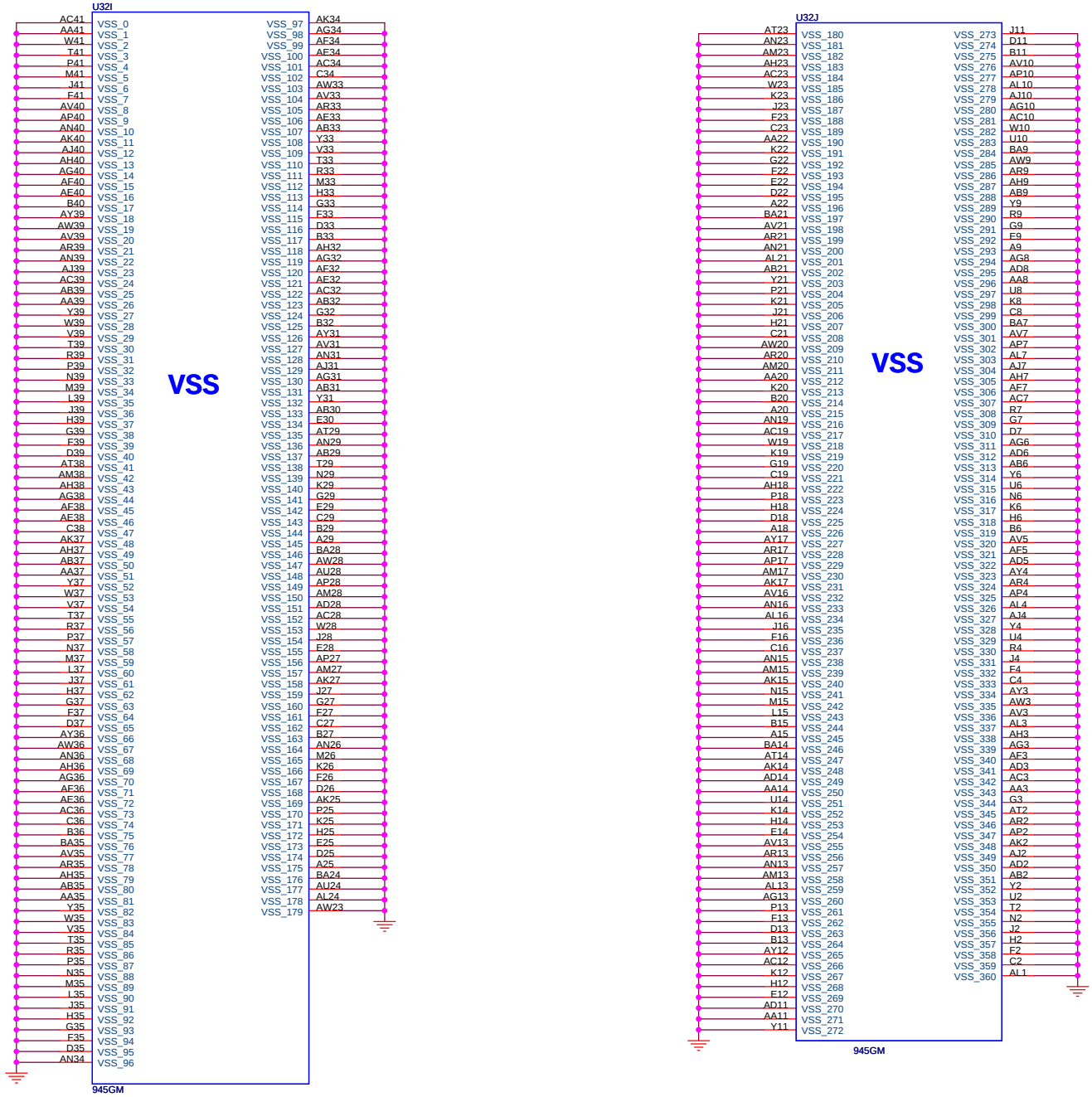
Size	Document Number	Rev
	Calistoga_C(DDR)	B2A

Date: Tuesday, January 03, 2006 Sheet 8 of 46


9
U32G
U32F
VCC
NCTF
945GM
25mils
120mils
100mils
place C50 on BA23 Ball
place C51 on BA15 Ball
GMCH Strap pin
Depopulate R2504 for Calistoga-Allen
MCH_CFG_6 shall be PH !!
depopulate R2504 if use Calistoga
intel WW51 recommand
1.MCH_CFG_5 Low = DMI X2, High=DMIX4
2.MCH_CFG_6 DDR : Low =Moby Dick, High= Calistoga (Default)
3.MCH_CFG_7 CPU Strap Low=RSVD, High=Mobile CPU
4.MCH_CFG_9 PCI Exp Graphics Lane: Low =Reserved,High=Mobility
5.MCH_CFG_10 Host PLL VCC Select: Low=Reserved, High=Mobility
6.MCH_CFG_11: Low=Calistoga, High=Reserved
7.MCH_CFG_16 FSB Dynmic ODT: Low=Dynamic ODT Disabled, High=Dynamic ODT Enabled.
8.MCH_CFG_18 VCC Select: LOW=1.05V, High=1.5V
9.MCH_CFG_19 DMI LANE Reversal:Low=Normal,High=LANES Reversed.
10.MCH_CFG_20 PCIE Backward interpoerability mode: Low= only SDVO or PCIE x1 is operational (defaults) ,High=SDVO and PCIE x1 are operation simultaneously via the PEG port.
PROJECT : TW3
Quanta Computer Inc.
Calistoga_D(POWER)
Tuesday, January 03, 2006



PROJECT : TW3			
Quanta Computer Inc.			
Size	Document Number		Rev
	Calistoga_E(POWER2)		B2A
Date: Wednesday, January 04, 2006		Sheet 10 of 46	



PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	Calistoga_F(VSS, NCTF)	B2A
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RTC

Place near to Mini-door

CKL:C1/C2: 18pF -> CL:12.5pF
C1/C: 10pF -> CL Value = 8.5pF

VCCRTC
3VPCU
D5 CH500H-40
D4 CH500H-40
VCCRTC_2
R201 1K/F
R198 1M
CN8 DFHD02MS784
R195 20K/F
C457 1u/10V
G1 *SHORT_ PAD1
C452 18p/50V
C453 18p/50V
Y2 32.768KHZ
R189 10M_6
CLK_32KX1
CLK_32KX2
C463 1u/16V_6
Internal PU

5VPCU
20MIL
20MIL
R197 1.2K/F
VCCRTC_1
R200 1K/F
VCCRTC_3
Q14 MMBT3904
R196 4.7K
R199 15K/F

+3VRUN
R148 10K
Internal PU
26 SATA_LED#
Review current rating

29 SATA_RXN0_C
29 SATA_RXP0_C
29 SATA_TXN0
29 SATA_TXP0
C709 3900p/25V
C708 3900p/25V
CKL:1n ~ 20nF
PAD T35
PAD T34
PAD T37
PAD T36
3 CLK_PCIE_SATA#
3 CLK_PCIE_SATA
25mils/15mils
R422 24.9/F
Place within 500 mils of ICH7
SATA_BIAS

29 PDIOR#
29 PDIOW#
29 PDDACK#
29 IRQ14
29 PIORDY
29 PDDREQ

T38
T72

U36A

RTXC1	AB1		
RTXC2	AB2		
RTCRST#	AA3	RTC	LPC
INTRUDER#	Y5		
INTVRMEN	W4		
EE_CS	W1		
EE_SHCLK	Y1		
EE_DOUT	Y2		
EE_DIN	W3		
LAN_CLK	V3		
LAN_RSTSYNC	U3		
LAN_RXD0	U5	LAN	CPU
LAN_RXD1	V4		
LAN_RXD2	T5		
LAN_TXD0	U7		
LAN_TXD1	V6		
LAN_TXD2	V7		
ACZ_BIT_CLK	U1		
ACZ_SYNC	R6		
ACZ_RST#	R5		
ACZ_SDIN0	T2	AC-97/AZALIA	
ACZ_SDIN1	T3		
ACZ_SDIN2	T1		
ACZ_SDOUT	T4		
SATALED#	AF18		
SATA0RXN	AF3		
SATA0RXP	AE3		
SATA0TXN	AG2		
SATA0TXP	AH2		
SATA2RXN	AF7		
SATA2RXP	AE7		
SATA2TXN	AG6		
SATA2TXP	AH6		
SATA_CLKN	AF1	SATA	
SATA_CLKP	AE1		
SATARBIASN	AH10		
SATARBIASP	AG10		
DIOR#	AF15	IDE	
DIOW#	AH15		
DDACK#	AF16		
IDEIRQ	AH16		
IORDY	AG16		
DDREQ	AE15		

ICH7-M

LAD0 AA6
LAD1 AB5
LAD2 AC4
LAD3 Y6
LDRQ0# AC3
LDRQ1#/GPIO23 AA5
LFRAME# AB3
A20GATE AE22
A20M# AH28
CPUSLP# AG27
TP1/DPRSTP# AF24
TP2/DPSLP# AH25
FERR# AG26
GPIO49/CPUPWRGD AG24
IGNNE# AG22
INIT3_3V# AG21
INIT# AE22
INTR AE25
RCIN# AG23
NMI AH24
SMI# AF23
STPCLK# AH22
THERMTRIP# AF26

LAD0 33,36,44
LAD1 33,36,44
LAD2 33,36,44
LAD3 33,36,44
LDRQ#0 36,44
LDRQ#1 T39
LFRAME# 33,36,44
GATEA20 36
H_A20M# 4
TP_H_CPUSLP# R104 *0 H_CPUSLP# 4,6
H_DPRSTP# R121 0 ICH_DPRSTP# 4,37
H_DPSLP# R109 0 H_DPSLP# 4
H_PWRGD 4
T65
H_IGNNE# 4
H_INIT# 4
H_INTR 4
RCIN# 36
H_SMI# R123 0 H_NMI 4 H_SMI# 4
H_STPCLK# 4
H_THERMTRIP_R R103 24.9/F PM_THRMTRIP# 4,7

DD0 AB15
DD1 AE14
DD2 AG13
DD3 AF13
DD4 AD14
DD5 AC13
DD6 AD12
DD7 AC12
DD8 AE12
DD9 AE12
DD10 AB13
DD11 AC14
DD12 AE14
DD13 AH13
DD14 AH14
DD15 AC15
DA0 AH17
DA1 AE17
DA2 AF17
DCS1# AE16
DCS3# AD16

PDD[15:0] 29
PDA[2:0] 29
PDCS1# 29
PDCS3# 29

R5506 close to MCH

+3VRUN
R404 10K
R415 10K
RCIN#
GATEA20

+1.05V
R108 *56_4
R120 *56_4
R110 56
R105 56
C784 *0.1u/10V
Should be 2" close ICH7
Should be 2" close ICH7

ACZ_SDIN0 ACZ_SDIN0 30
ACZ_SDOUT R187 39 ACZ_SDOUT_AUDIO 30
C460 *10p
Near To ICH7-M
ACZ_SYNC R184 39 ACZ_SYNC_AUDIO 30
C461 *10p
ACZ_BCLK R186 39 BIT_CLK_AUDIO 30
C459 22p/50V
ACZ_RST# R174 39 ACZ_RST#_AUDIO 30

ICH7 internal VR enable strap

	INTVRMEN
Enable (default)	1
Disable	0

VCCRTC
R188 332K/F_6
ICH_INTVRMEN
R185 *0

PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	ICH7-M HOST(1 of 4)	B2A

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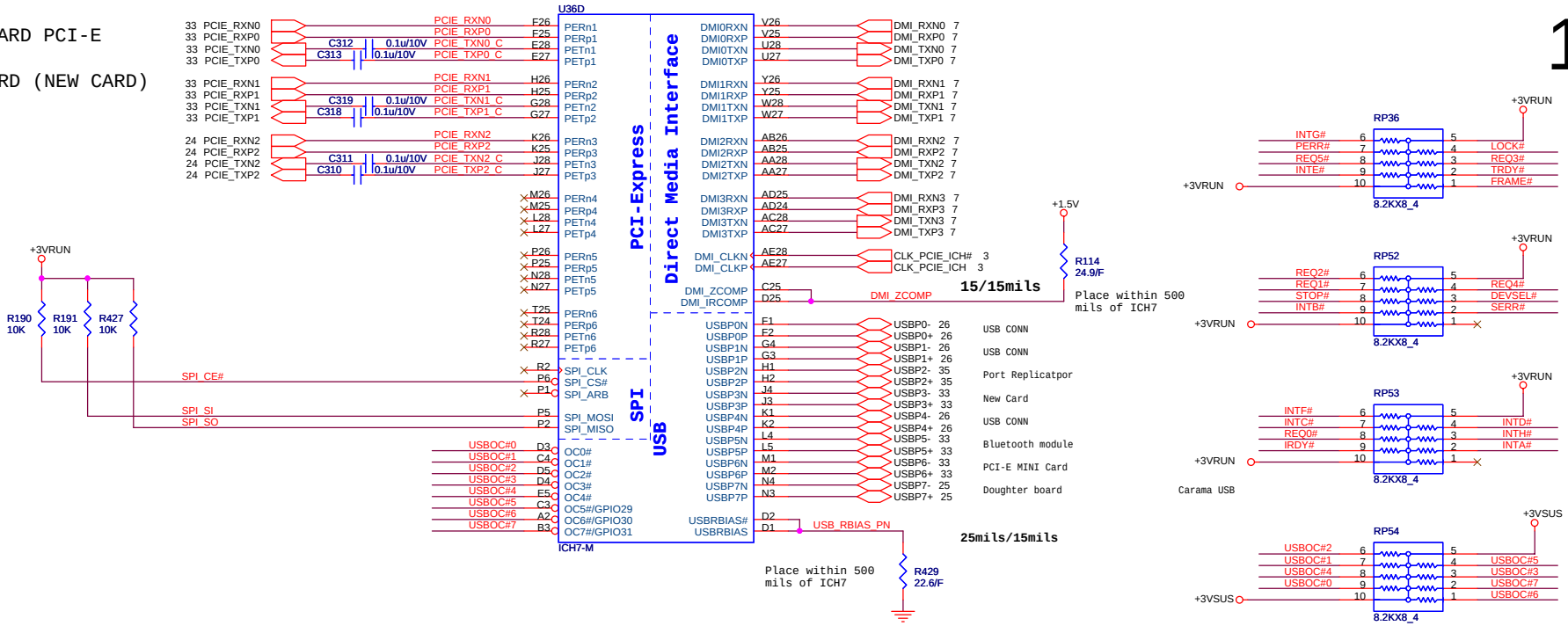
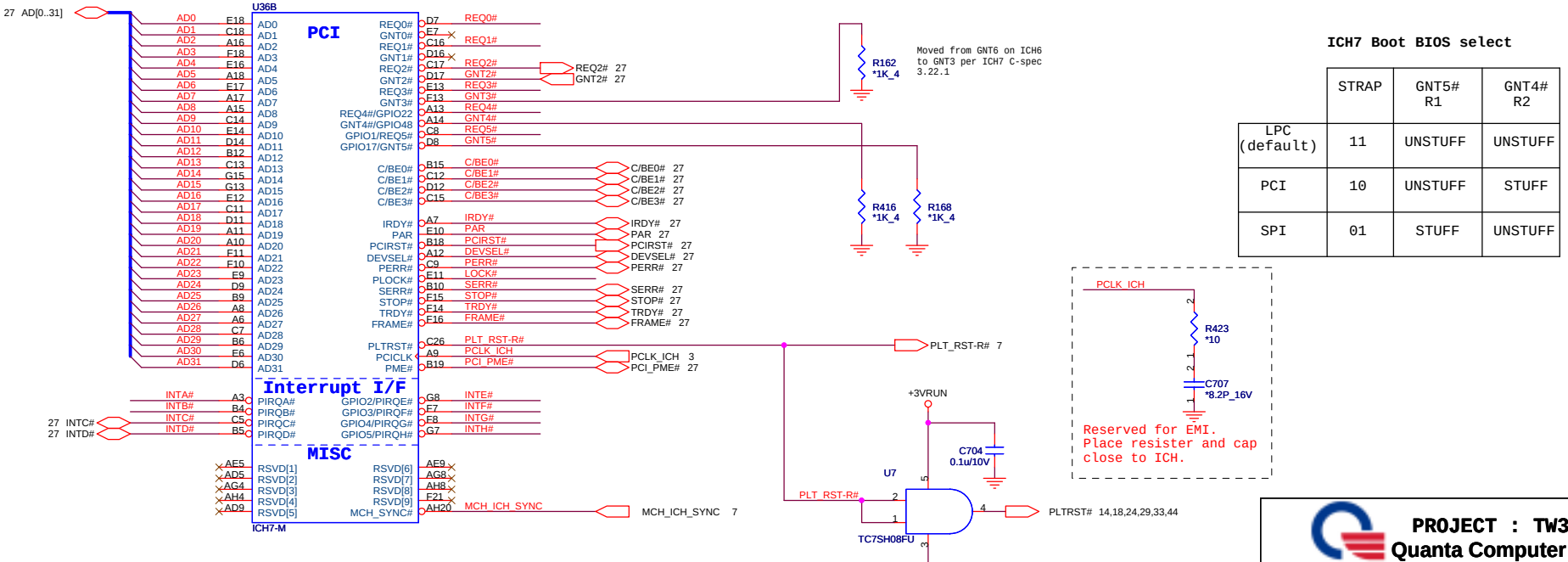
MINI CARD PCI-E

EXPRESS CARD (NEW CARD)





ICH7 Boot BIOS select

	STRAP	GNT5# R1	GNT4# R2
LPC (default)	11	UNSTUFF	UNSTUFF
PCI	10	UNSTUFF	STUFF
SPI	01	STUFF	UNSTUFF

PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	ICH7-M PCI E(2 of 4)	B2A

Date: Tuesday, January 03, 2006 Sheet 13 of 46

R376

No stuff-->boot
Stuff-->No boot

+3V_S5
PCLK_SMB R124 2.2K
PDAT_SMB R128 2.2K
PCIE_WAKE# R156 680

+3V_S5
RI# R389 10K
SMB_LINK_ALERT# R391 10K
SMLINK0 R392 10K
SMLINK1 R394 10K
EXTSMI# R R153 *10K
WAKE_SCI# R R95 10K
SMBALERT# R395 10K

+3V_S5
SWI# R409 10K
DNBSWON# R117 10K
SYS_RST# R396 10K
PM_BATLOW# R401 8.2K/F

+3VRUN
SYS_RST# R399 *10K
CLKRUN# R420 8.2K/F
SERIRQ R412 8.2K/F
RUNTIME_SCI# R R140 10K

SYS_RST is suspend rail

RSMRST# R424 10K

+3VRUN
R411 *1K_4

U36C

30 ACZ_SPKR
3,33 PCLK_SMB
3,33 PDAT_SMB
SMBCLK C22
SMBDATA B22
LINKALERT# A26
SMLINK0 B25
SMLINK1 A25
27 RI# RI# A28
SPKR A19
27,44 SUS_STAT# SUS_STAT# A27
4 SYS_RST# SYS_RST# A22
7 PM_BMBUSY# R166 0 GPIO0/BM_BUSY# AB18
T24 SMBALERT# GPIO11/SMBALERT# B23
No ASF support
3 PM_STPPCI# R130 0 PM_STPPCI_ICH# GPIO18/STPPCI# AC20
3 PM_STPCPU# R127 0 PM_STPCPU_ICH# GPIO20/STPCPU# AE21
T64 GPIO26 A21
T66 GPIO27 B21
T22 GPIO28 F23
27,36,44 CLKRUN# CLKRUN# GPIO32/CLKRUN# AG18
29 ICH_GPO33 ICH_GPO33 GPIO33/AZ_DOCK_EN# AC19
BOARD_ID2 GPIO34/AZ_DOCK_RST# U2
24,33 PCIE_WAKE# PCIE_WAKE# WAKE# F20
27,36,44 SERIRQ SERIRQ SERIRQ AH21
THRM# AE20
VR_PWRGD_CK410 VRMPWRGD AD22
T28 GPIO6 AC21
36 SCI# R141 0 RUNTIME_SCI# R GPIO7 AC18
36 KBSMI# R143 0 EXTSMI# R GPIO8 F21
ICH7-M

SMB
SATA GPIO
Clocks
SYS GPIO
Power MGT
GPIO

GPIO21/SATA0GP AF19 BOARD_ID1
GPIO19/SATA1GP AH18 BOARD_ID0
GPIO36/SATA2GP AH19 BOARD_ID3
GPIO37/SATA3GP AF19 BOARD_ID4
CLK14 AC1 14M_ICH 14M_ICH 3
CLK48 B2 CLKUSB_48 CLKUSB_48 3
SUSCLK C20 ICH_SUSCLK T31
SLP_S3# B24 R115 100/F SUSB# 36
SLP_S4# D23 R122 100/F SUSC# 36
SLP_S5# F22 T21
PWROK AA4 ICH_PWROK
GPIO16/DPRSLPVR AC22 PM_DPRSLPVR_R R113 100/F
R116 0 PM_EXTTS#1 7
R112 *100K PM_DPRSLPVR 37
TP0/BATLOW# C21 PM_BATLOW# R R400 100/F PM_BATLOW# 36
PWRBTN# C23 DNBSWON# R158 100K DNBSWON# 36
LAN_RST# C19 R98 0 PLTRST# 13,18,24,29,33,44
RSMRST# Y4 PM_RSMRST# R R425 100/F RSMRST# RSMRST# 36
GPIO9 E20 SWI# SWI# 36
GPIO10 A20 T67
GPIO12 E19 WAKE_SCI# R T27
GPIO13 R4 T19
GPIO14 E22 T40
GPIO15 R3 T25
GPIO24 D20 T29
GPIO25 AD21
GPIO35 AD20 GPIO38
GPIO38 AE20 T30

+3VRUN
U14
3,37 CLK_EN# VR_PWRGD_CK410
NL17SZ14DFT2G

Note: External pull-up 3V
CKL :100Kohm PD

GPIO25 /Suspend rail is a HW strap , don't pull down .

+3VRUN
R126 *10K
R129 *10K
+3VRUN
R418 8.2K/F
5 THERM_ALERT#

PWM require 6.9K
Change to 6.8K
+3VSUS
C451 0.047u/10V
R193 6.8K
+3VRUN
7,37 DELAY_VR_PWRGOOD
36 PWROK
U15
TC7SH08FU
ICH_PWROK
R182 100K
R183 10K

Level is incorrect !!

Place these close to ICH7.
CLKUSB_48
R428 *10
C712 *4.7P_50V
14M_ICH
R372 *10_NC
C637 *4.7P_50V_NC

+3VRUN
R421 *10K_4
BOARD_ID0
R167 10K
+3VRUN
R147 *10K
BOARD_ID1
R139 10K
+3VRUN
R371 *10K_NC
BOARD_ID2
R367 10K
+3VRUN
R136 *10K
BOARD_ID3
R137 10K
+3VRUN
R368 *10K
BOARD_ID4
R366 10K

+3VRUN
R482 10K
GPIO38
R483 *10K

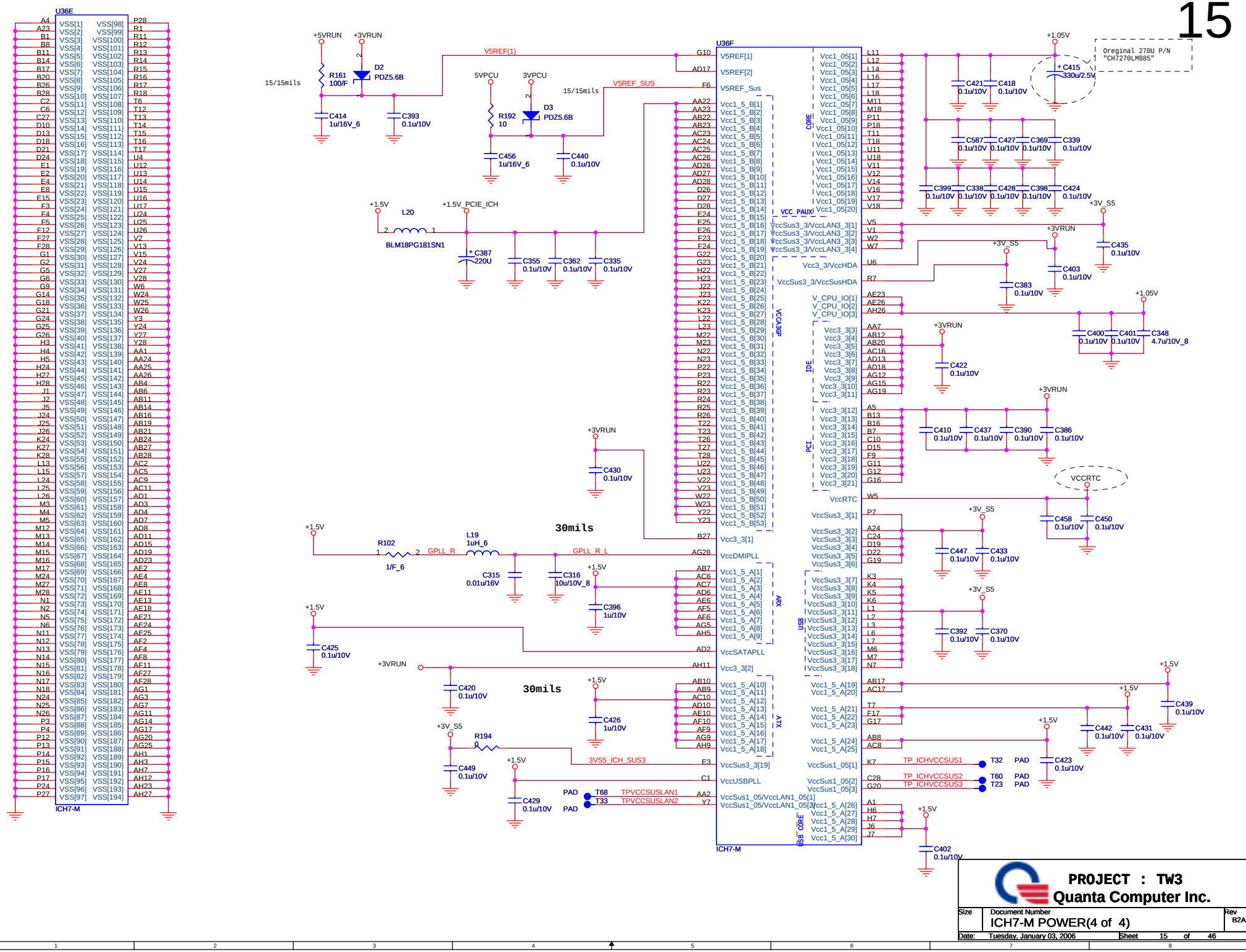
GPIO38	Function
High	CRT
Low	DVI

Board ID	Function
ID [1:0]	00: TW3 01: DW1
ID2	0: SATA HDD 1: PATA HDD
ID [4:3]	Reserve

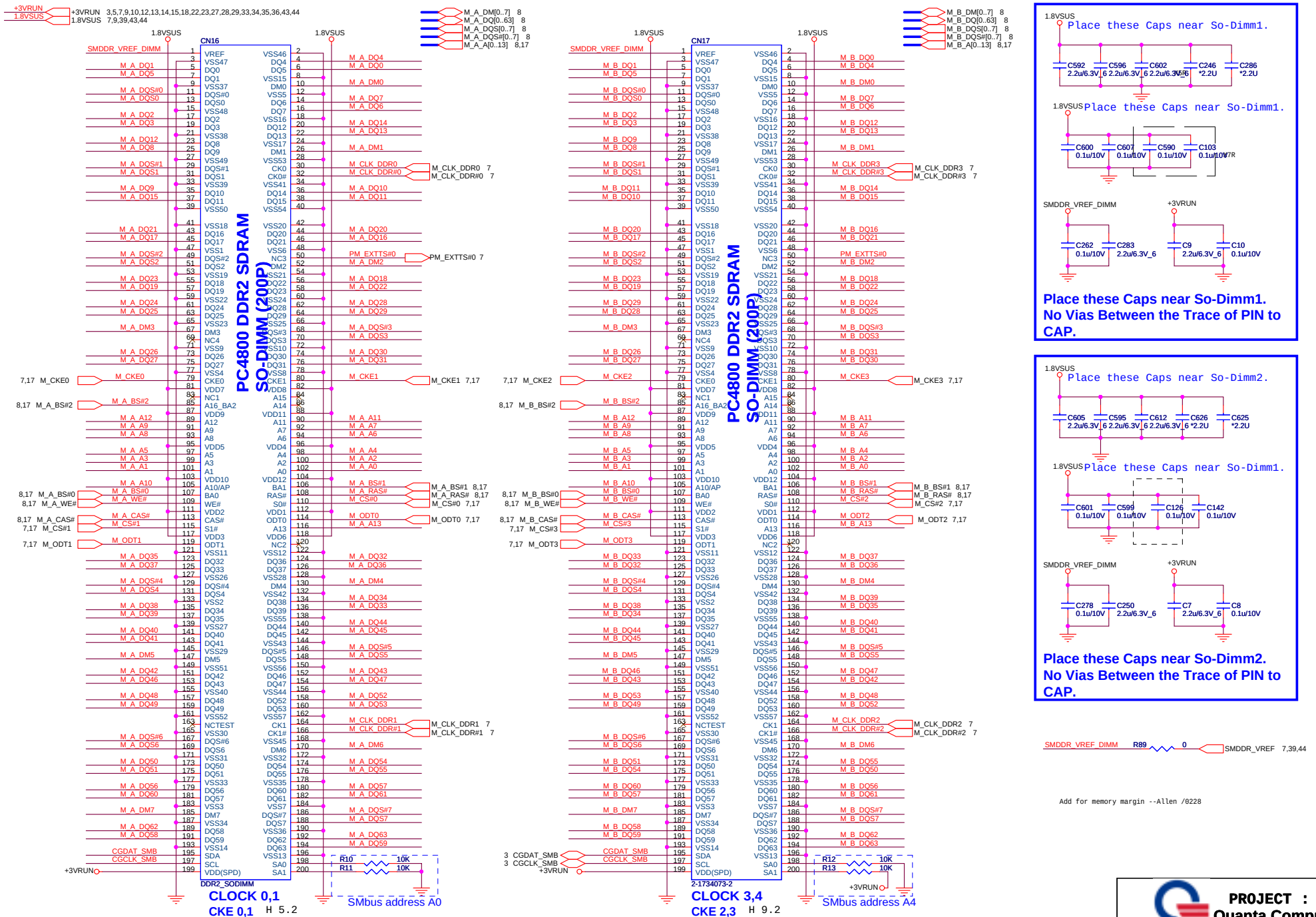
PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	ICH7-M GPIO(3 of 4)	B2A

Date: Tuesday, January 03, 2006 Sheet 14 of 46



Project	PROJECT : TW3
Company	Quanta Computer Inc.
Size	
Document Number	ICH7-M POWER(4 of 4)
Rev	B2A
Date	Tuesday, January 03, 2006
Sheet	15 of 46



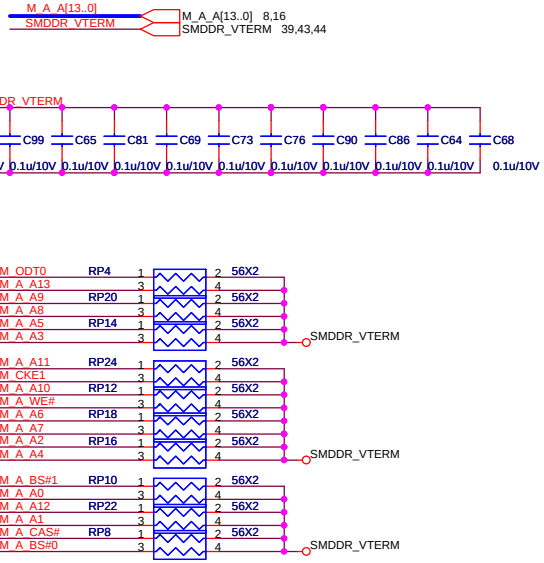
Add for memory margin --Allen /0228

PROJECT : TW3
Quanta Computer Inc.

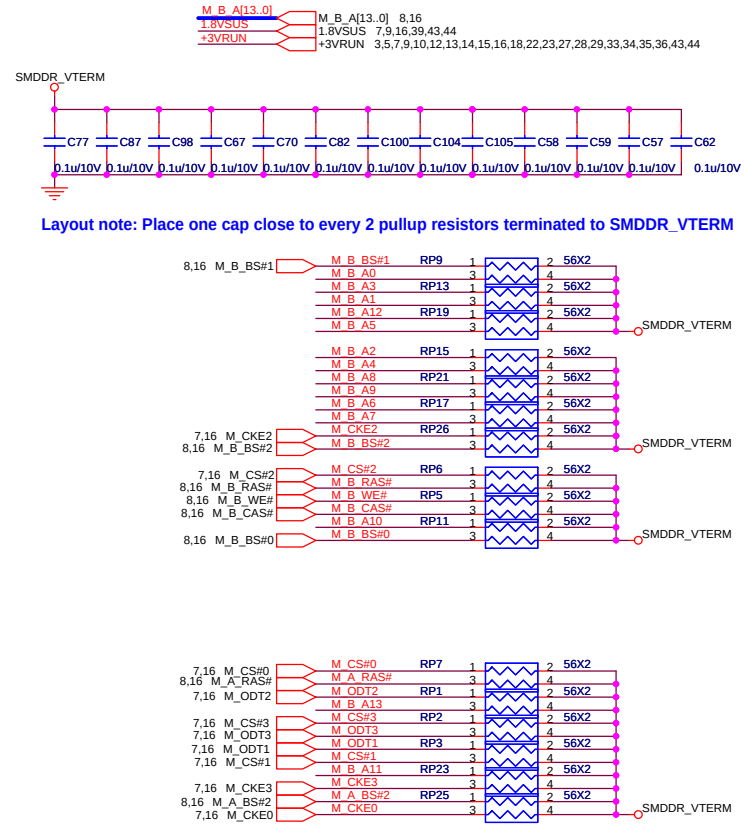
Size	Document Number	Rev
	DDRII SO-DIMM(200P)	B2A
Date: Tuesday, January 03, 2006	Sheet 16 of 46	

DDRII DUAL CHANNEL A,B.

DDRII A CHANNEL

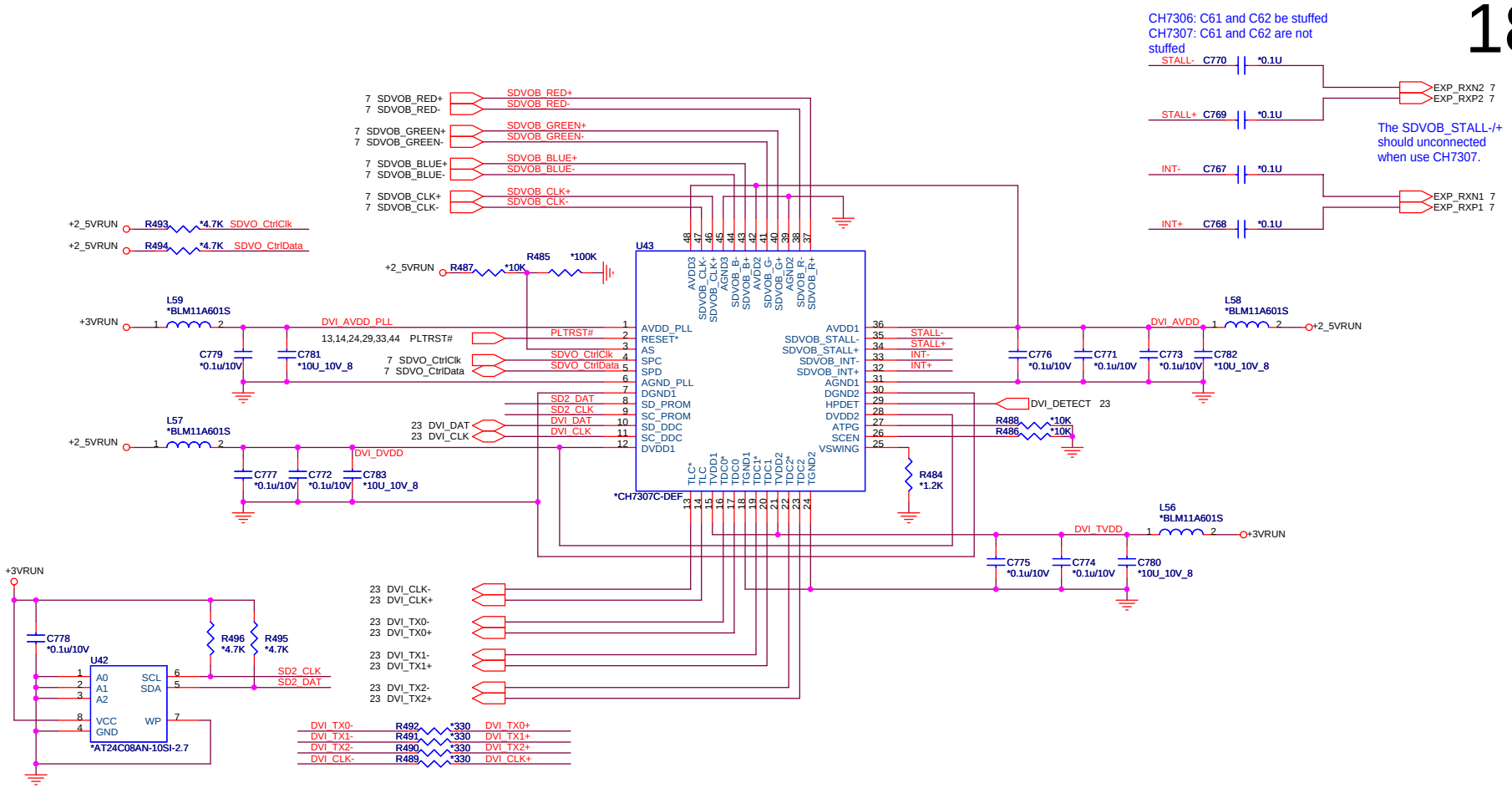


DDRII B CHANNEL



PROJECT : TW3		
Quanta Computer Inc.		
Size	Document Number: DDRII TERMINATION	Rev: B2A
Date: Tuesday, January 03, 2006	Sheet 17 of 46	

GMCH SDVO Signal to DVI Signal Bridge



PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	SDO to DVI (CH7307)	B2A

Date: Tuesday, January 03, 2006 Sheet 18 of 46

PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	Empty	B2A

Date: Tuesday, January 03, 2006 Sheet 19 of 46

PROJECT : TW3
Quanta Computer Inc.

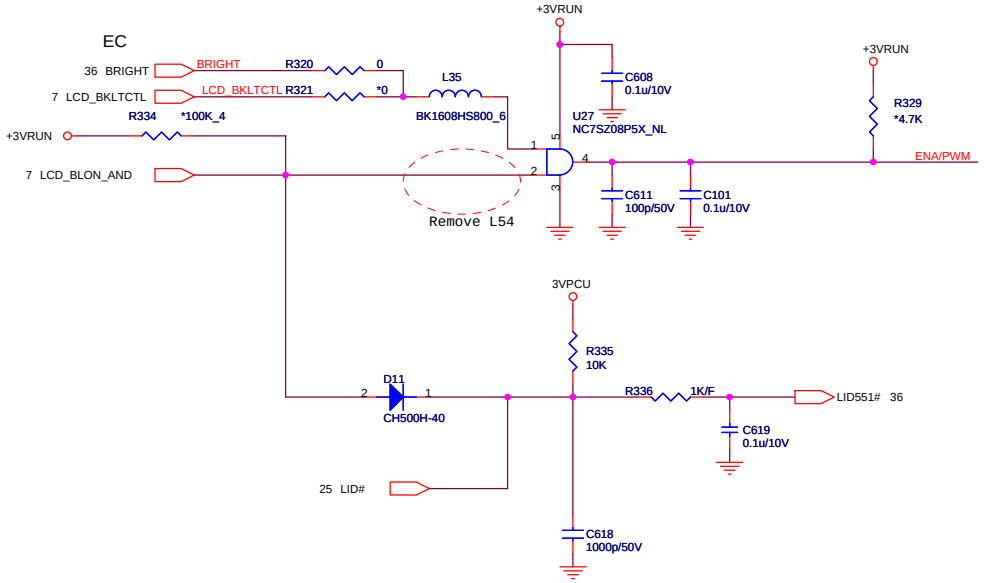
Size	Document Number	Rev
	Empty	B2A

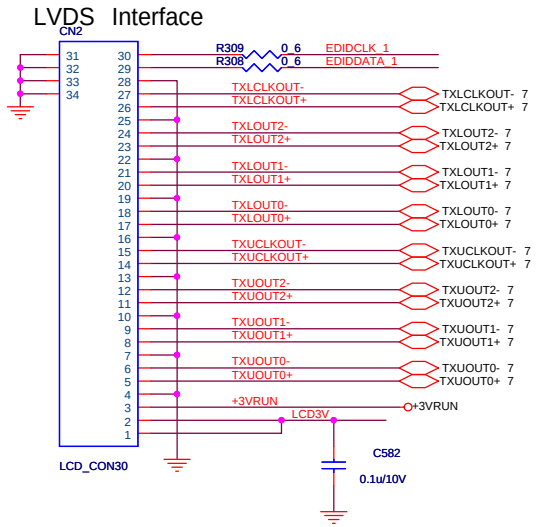
Date: Tuesday, January 03, 2006 Sheet 20 of 46

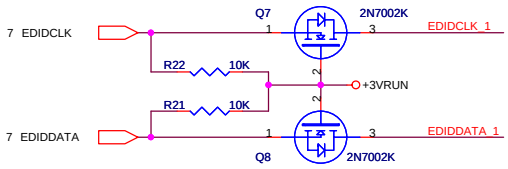
PROJECT : TW3
Quanta Computer Inc.

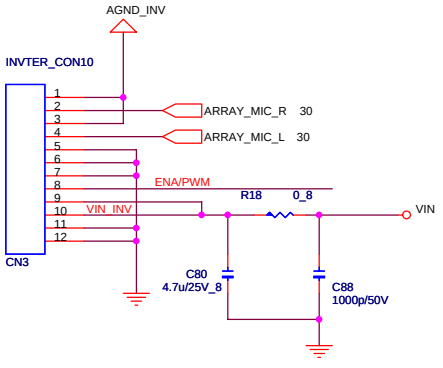
Size	Document Number	Rev
	Empty	B2A

Date: Tuesday, January 03, 2006 Sheet 21 of 46

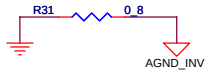


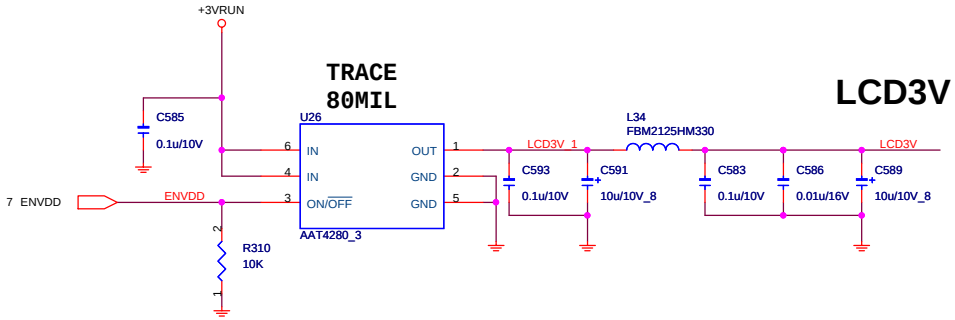






Inverter Interface

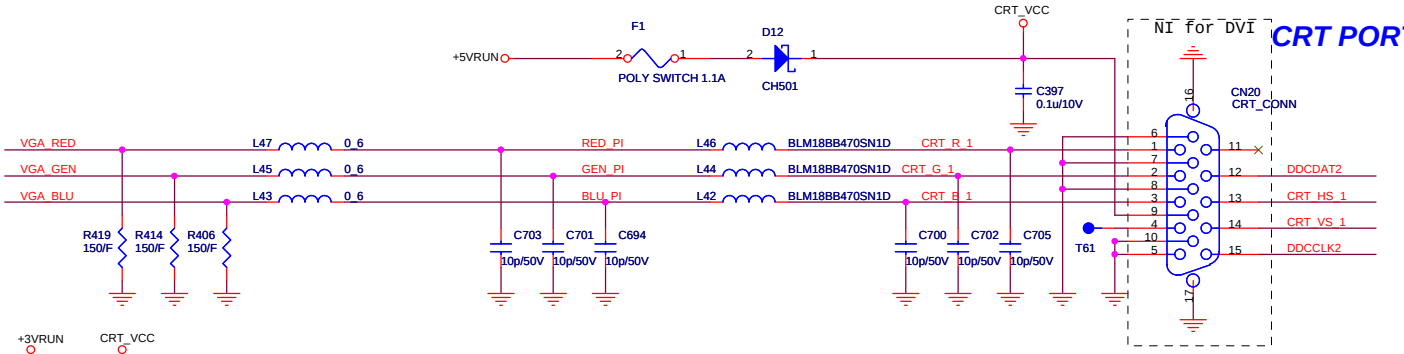




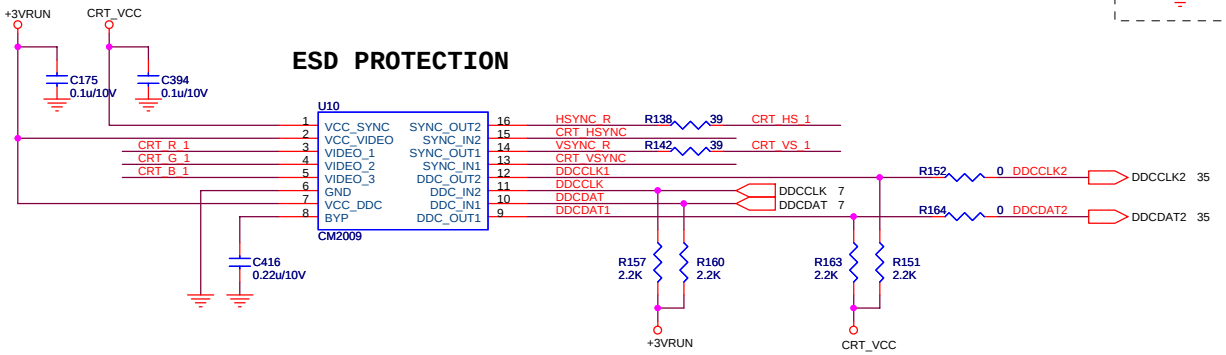
PROJECT : TW3
Quanta Computer Inc.

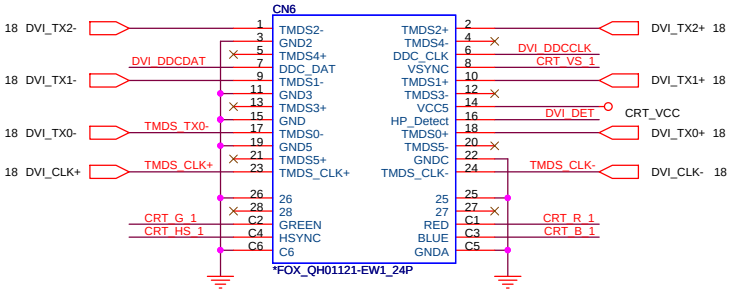
Size	Document Number	Rev
	LCD,INVERTER CONN	B2A
Date: Tuesday, January 03, 2006	Sheet 22 of 46	

CRT PORT

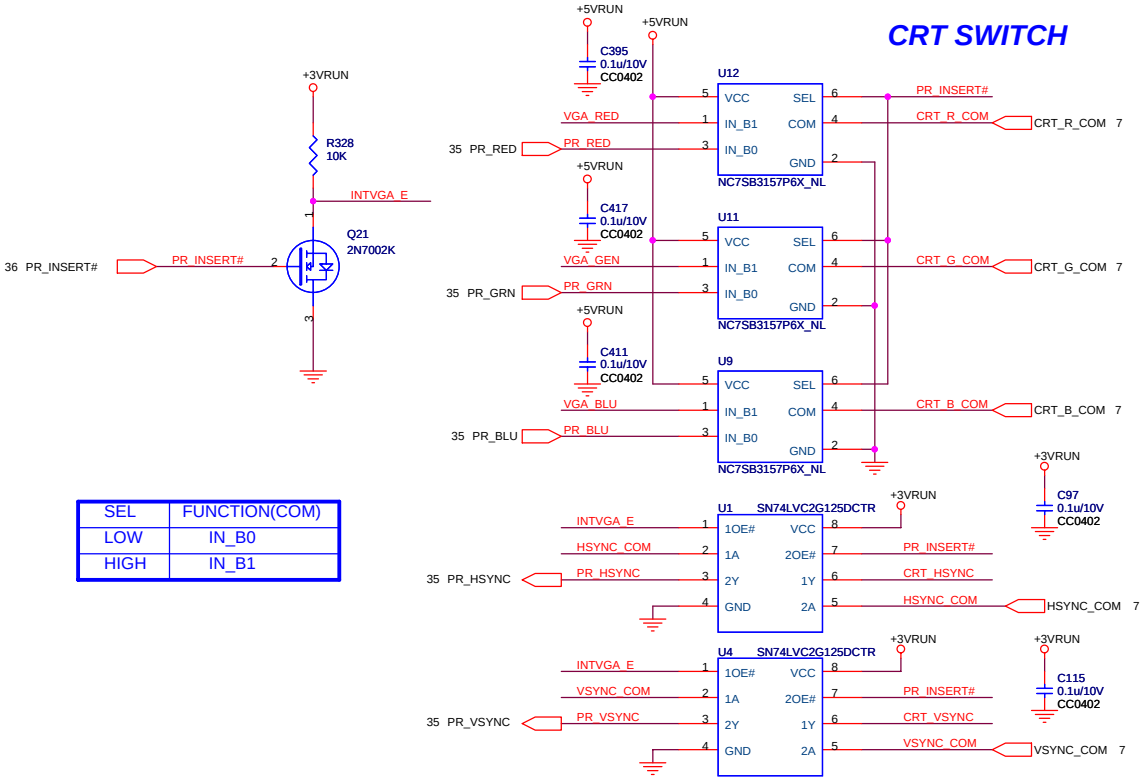


ESD PROTECTION

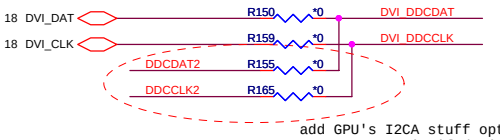




CRT SWITCH

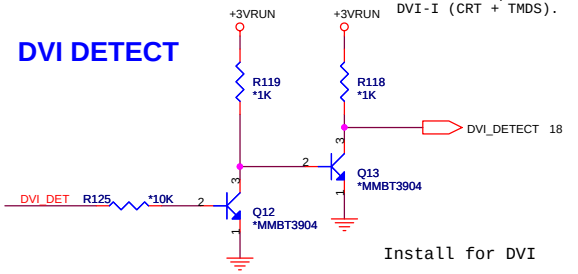


SEL	FUNCTION(COM)
LOW	IN_B0
HIGH	IN_B1



add GPU's I2CA stuff option to TMDS I2C pin if design DVI-I (CRT + TMDS).

DVI DETECT



Install for DVI

PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	CRT,TV-OUT,DVI CONN.	B2A

Date: Tuesday, January 03, 2006 Sheet 23 of 46

C: 88E8053 LF PN: AJ080530010 (20050414)

1Mbits

C: Add 9 X GND Pad for LAN controller. (20050411)

C: Add these GND pin for via hole to GND Plane.

C: Add RC (R37 change to 200K, Add C101) delay to control LOM_DISABLE#. (20050411)

C: Reserve R36. Change LANRST# to PCIRST# source from MB option modify.(2005/04/11)

CLOSE CHIP

DELAY PIN10 AT LEAST 150ms

88E8038/88E8055

FOR 8038	
R389	2K
R9	NC

Install for 8038

NI for 8038

LANVCC

PLACEMENT CLOSE TO EACH OTHER

C: Widen to 20 mils. AVDD25 to 20 mils.(20050411)

C: Widen to 20 mils. VDD to 20 mils.(20050411)

0804 REDUCING THE LANVCC NOISE

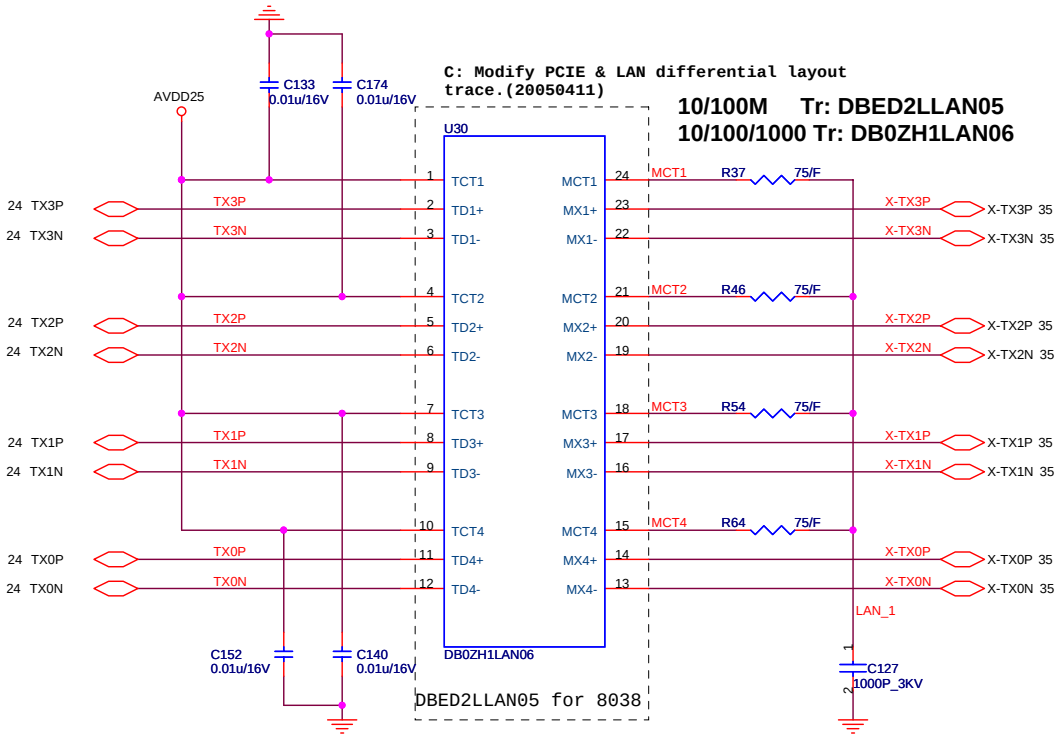
PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	Marvell 88E8038,88E8055	B2A

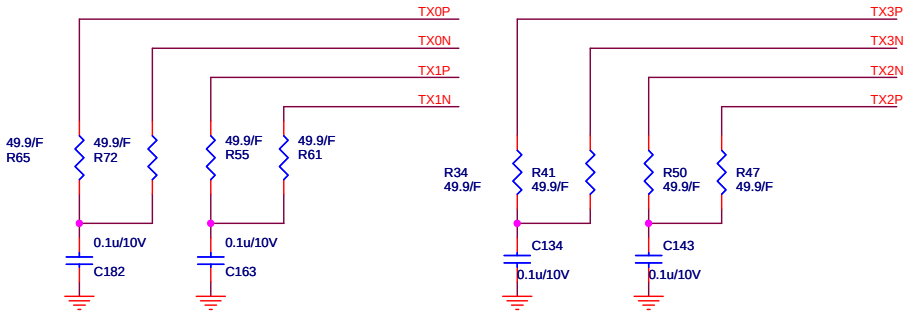
Date: Tuesday, January 03, 2006 Sheet 24 of 46

C: Modify PCIE & LAN differential layout trace.(20050411)

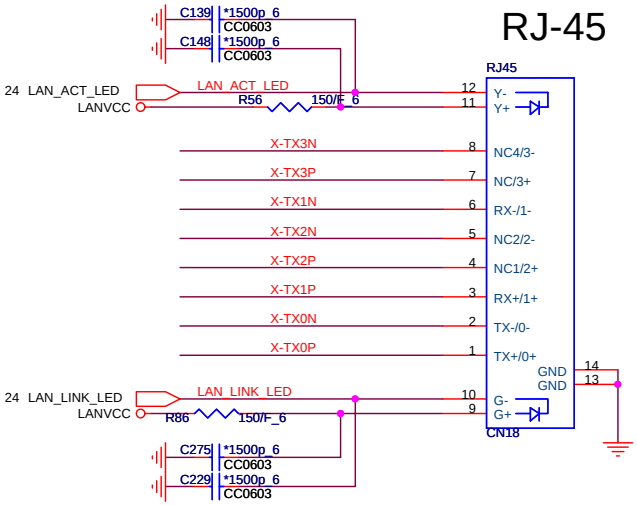
10/100M Tr: DBED2LLAN05
10/100/1000 Tr: DB0ZH1LAN06

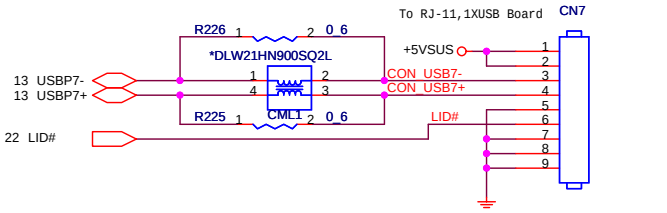


GigaLAN transformer



RJ-45



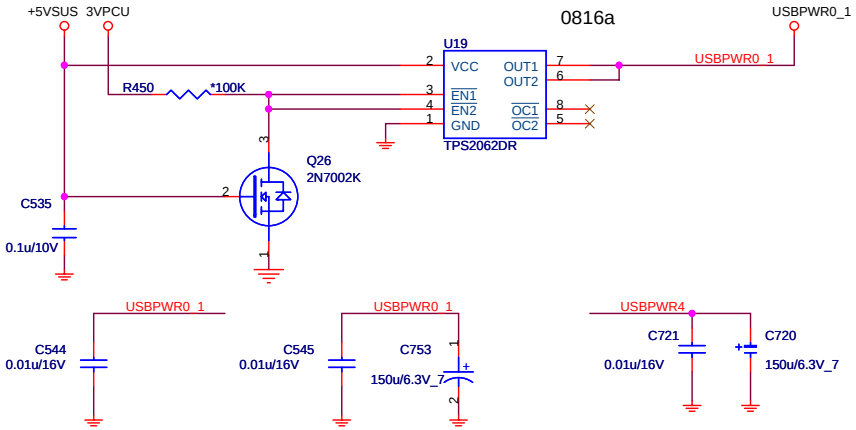


RJ-11,USB Board

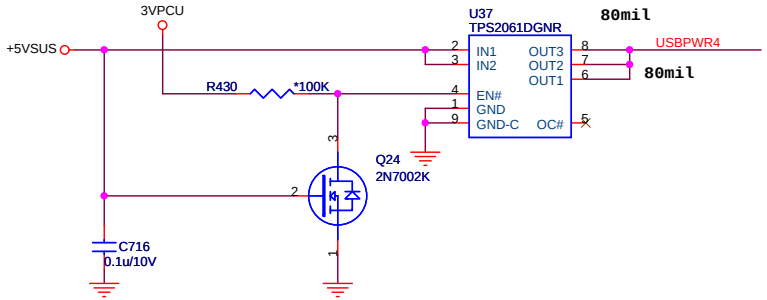
PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	LAN SW CONN& MDC CONN	B2A

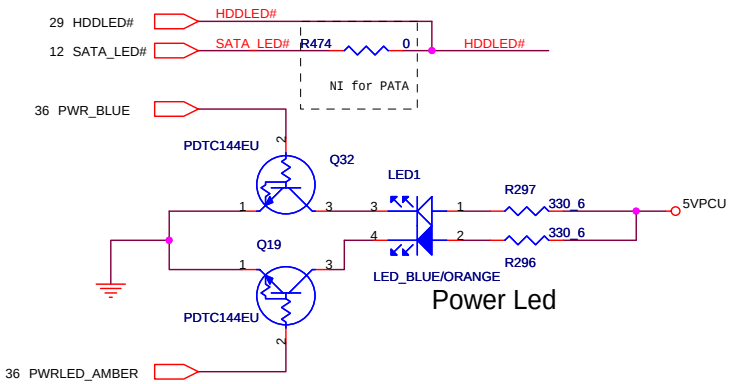
Date: Tuesday, January 03, 2006 Sheet 25 of 46



C:Change U1 from G528 to TPS2061

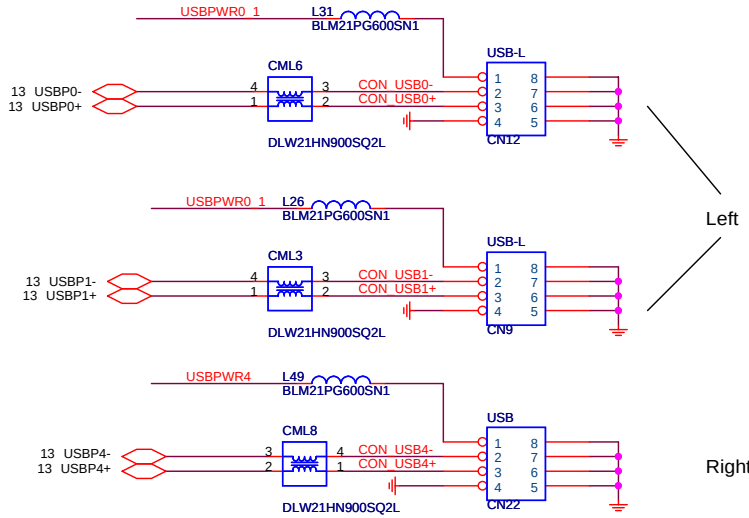


HDD,SATA Led



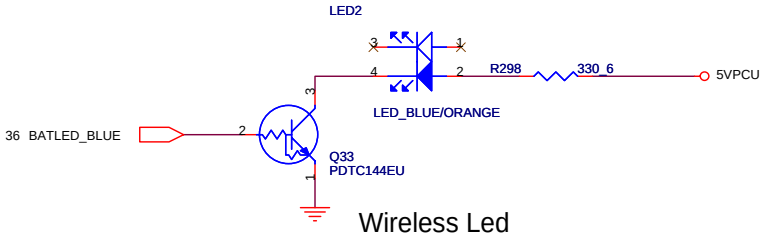
Power Led

USB Port

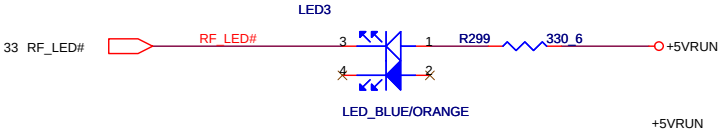


For Botton Board

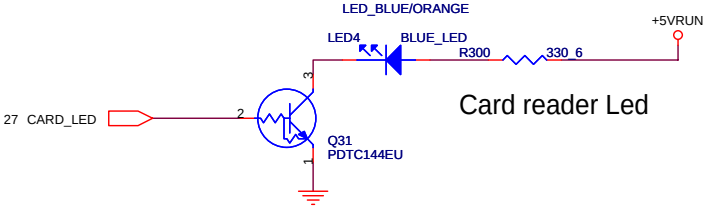
Battery Led

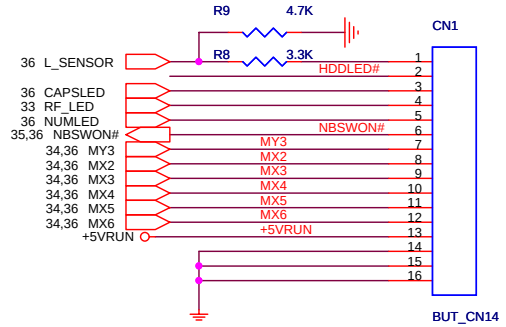


Wireless Led



Card reader Led

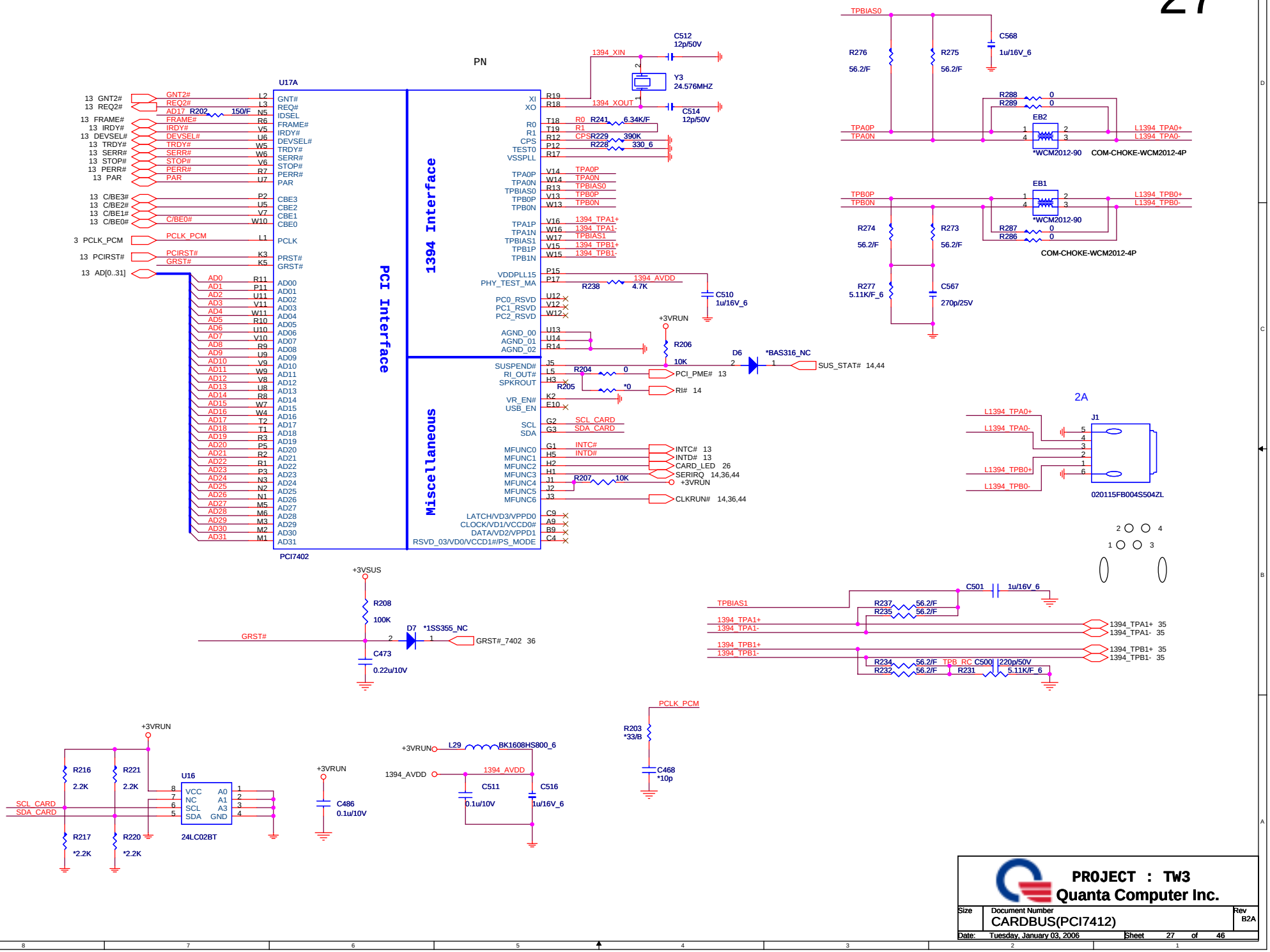




PROJECT : TW3
Quanta Computer Inc.

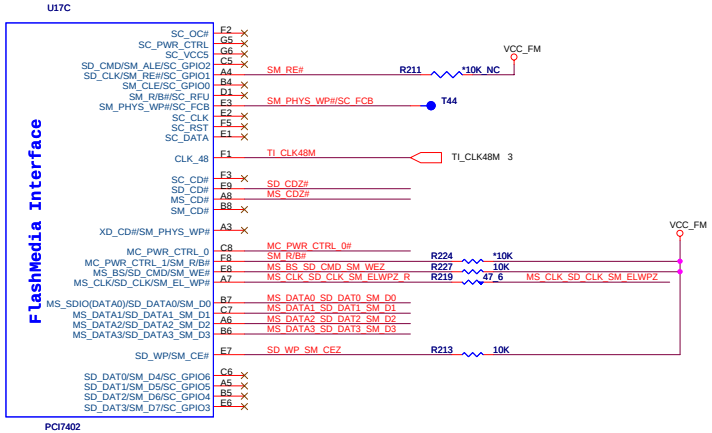
Size	Document Number	Rev
	USB,LED,Buttom/B	B2A

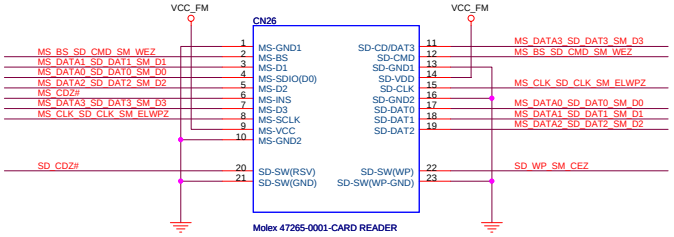
Date: Wednesday, January 04, 2006 Sheet 26 of 46


U17A
PCI7402
PCI Interface
1394 Interface
Miscellaneous
PN
GNT2#
REQ2#
AD17 R202 150/F
FRAME#
IRDY#
DEVSEL#
TRDY#
SERR#
STOP#
PERR#
PAR
C/BE3#
C/BE2#
C/BE1#
C/BE0#
PCLK_PCM
PCIRST#
GRST#
AD[0..31]
1394_XIN
1394_XOUT
Y3
24.576MHZ
C512
12p/50V
C514
12p/50V
R0 R241 6.34K/F
R1
CPS R229 390K
R228 330_6
1394_TPA1+
1394_TPA1-
1394_TPB1+
1394_TPB1-
1394_AVDD
R238 4.7K
C510
1u/16V_6
+3VRUN
R206
10K
D6
*BAS316_NC
SUS_STAT# 14,44
SUSPEND#
RI_OUT#
SPKROUT
R204 0
R205 *0
PCI_PME# 13
RI# 14
VR_EN#
USB_EN
SCL_CARD
SDA_CARD
INTC#
INTD#
CARD_LED 26
SERIRQ 14,36,44
CLKRUN# 14,36,44
LATCH/VD3/VPPD0
CLOCK/VD1/VCCD0#
DATA/VD2/VPPD1
RSVD_03/VD0/VCCD1#/PS_MODE
TPBIAS0
R276 56.2/F
R275 56.2/F
C568
1u/16V_6
R288 0
R289 0
EB2
*WCM2012-90
COM-CHOKE-WCM2012-4P
R274 56.2/F
R273 56.2/F
R287 0
R286 0
EB1
R277 5.11K/F_6
C567
270p/25V
2A
J1
020115FB004S504ZL
+3VSUS
R208
100K
D7 *1SS355_NC
GRST#_7402 36
C473
0.22u/10V
TPBIAS1
R237 56.2/F
R235 56.2/F
C501 1u/16V_6
R234 56.2/F
R232 56.2/F
TPB_RC C500 220p/50V
R231 5.11K/F_6
U16
24LC02BT
R216 2.2K
R221 2.2K
R217 *2.2K
R220 *2.2K
C486
0.1u/10V
L29 BK1608HS800_6
C511 0.1u/10V
C516 1u/16V_6
R203 *33/B
C468 *10p
PROJECT : TW3
Quanta Computer Inc.
CARDBUS(PCI7412)
Rev B2A
Tuesday, January 03, 2006
Sheet 27 of 46

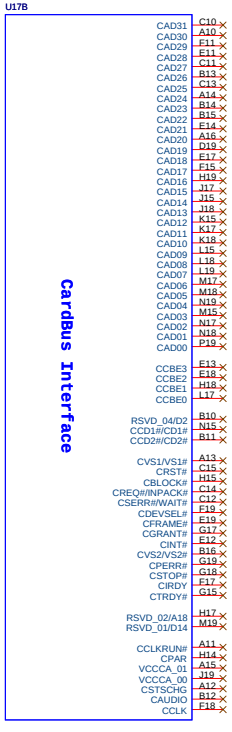
DO NOT INSERT SD/MMC, MEMORYSTICK AND XD SIMULTANEOUSLY.

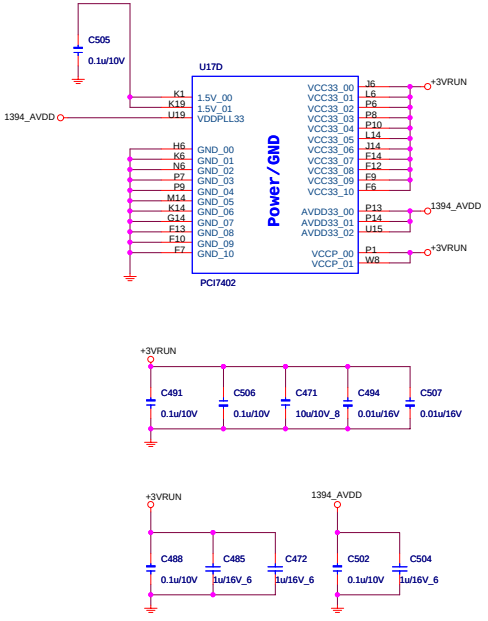
3 IN1 CARD READER (push-push)

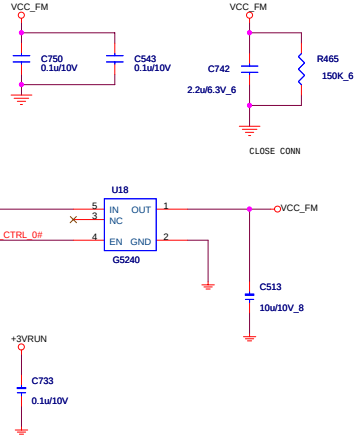




Supporting MMC/SD/MS Cards
Molex P/N:DFHD23MSBB6

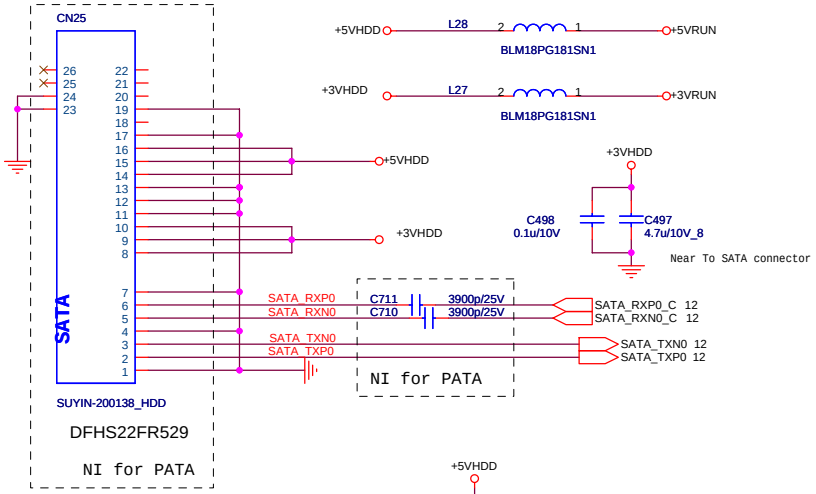


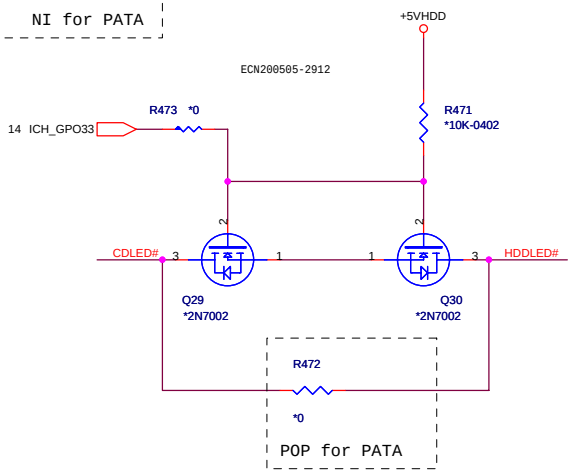




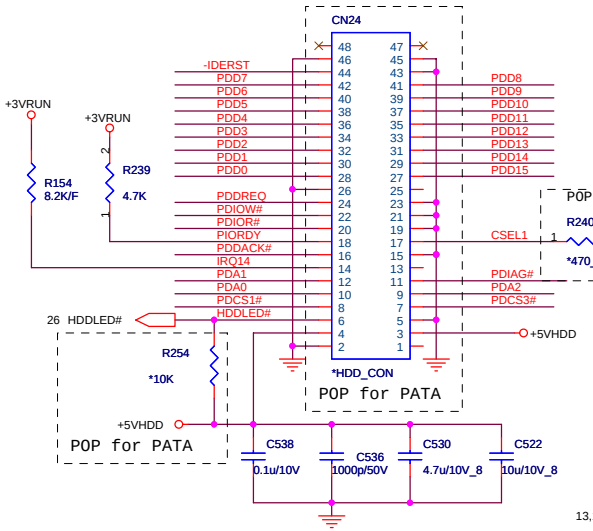
PROJECT : TW3		
Quanta Computer Inc.		
Size	Document Number: 1394 CONTROLLER	Rev: B2A
Date: Tuesday, January 03, 2006	Sheet 28 of 46	

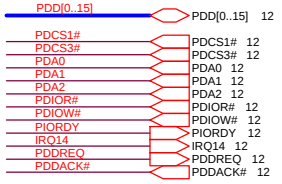
SATA HDD

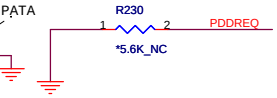


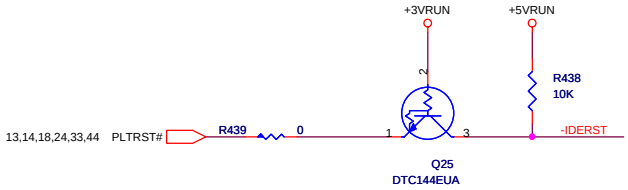


PATA HDD

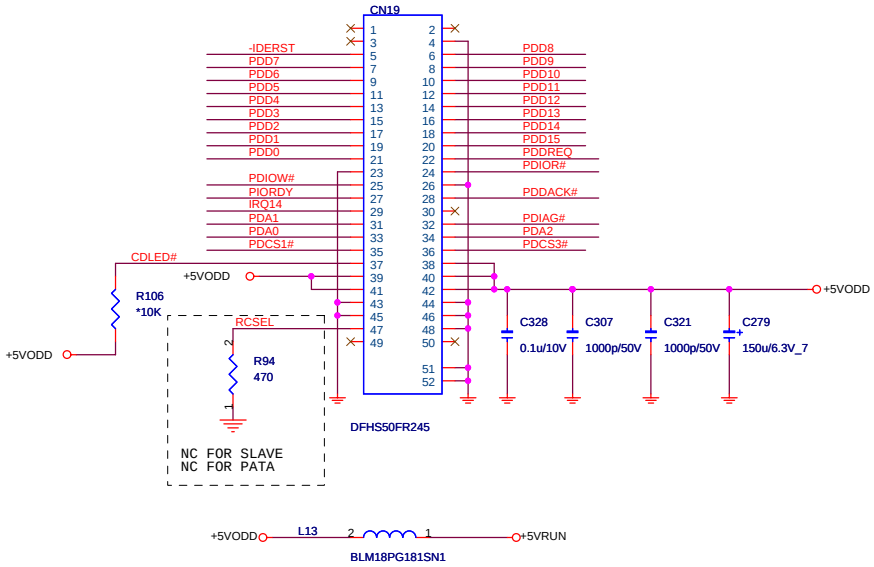








ODD



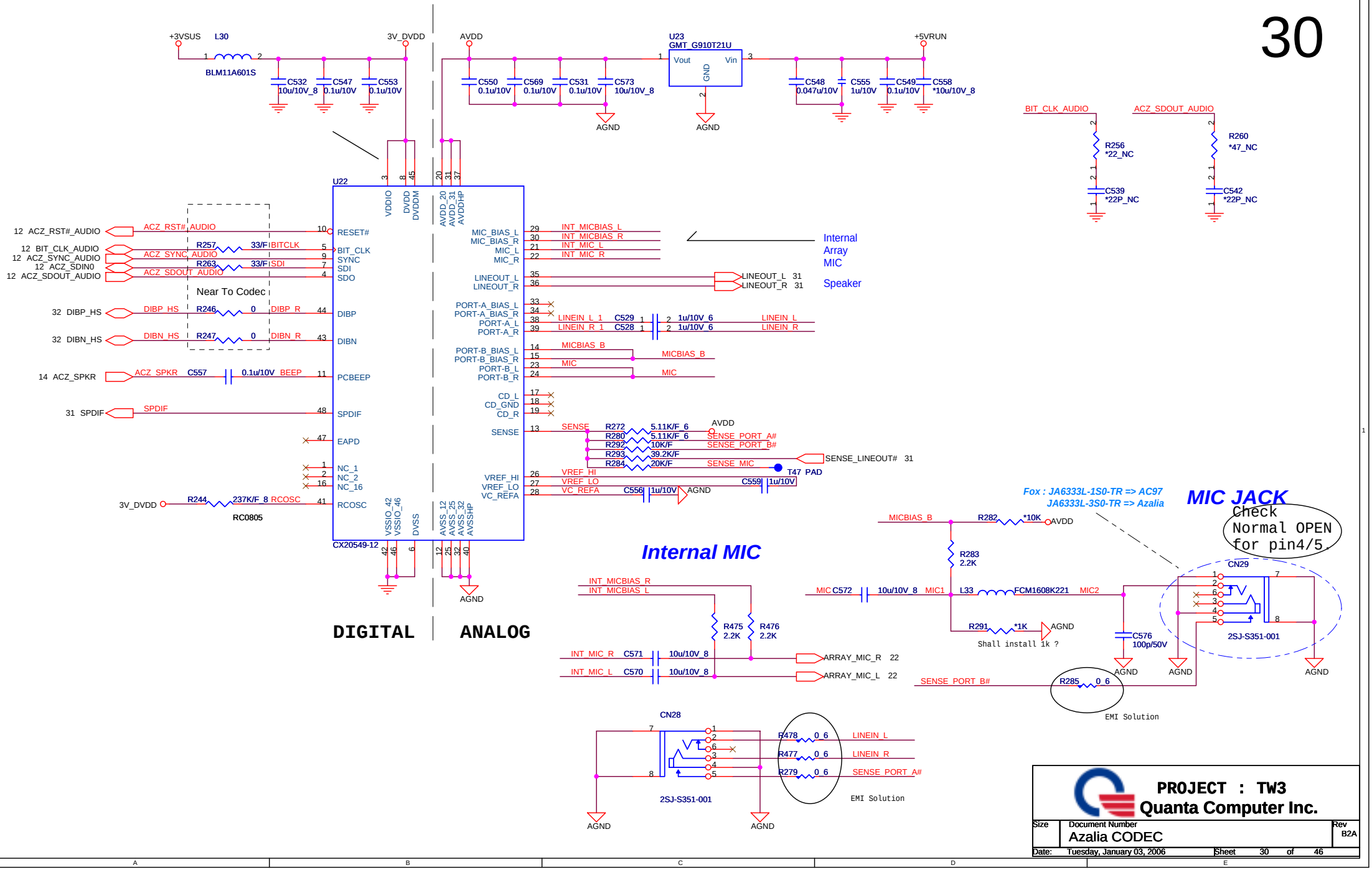
FOR PATA HDD

CN19	NI
C730	NI
C729	NI
CN18	HDD CON
R517	NI
Q25	2N7002
Q26	2N7002
R513	10K
R512	0
R168	470

PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	SATA,PATA(HDD,ODD)	B2A

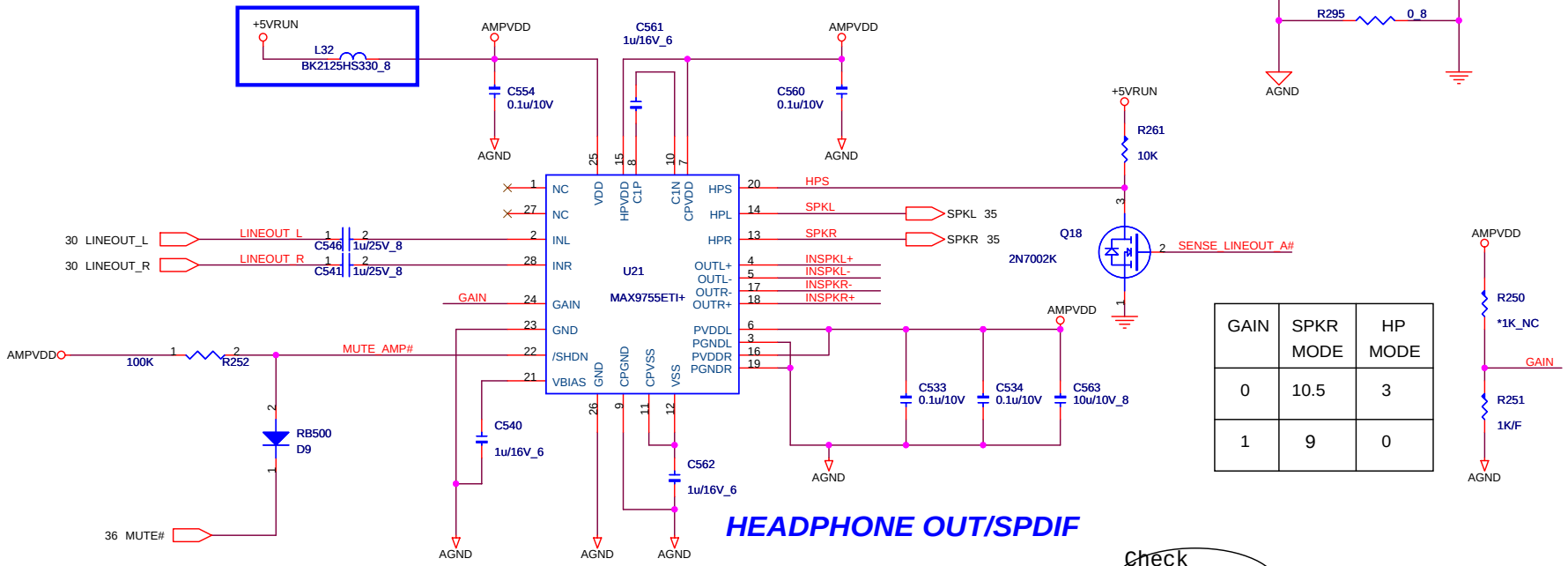
Date: Tuesday, January 03, 2006 Sheet 29 of 46



PROJECT : TW3			
Quanta Computer Inc.			
Size	Document Number		Rev
	Azalia CODEC		B2A
Date: Tuesday, January 03, 2006	Sheet 30 of 46		

0816a

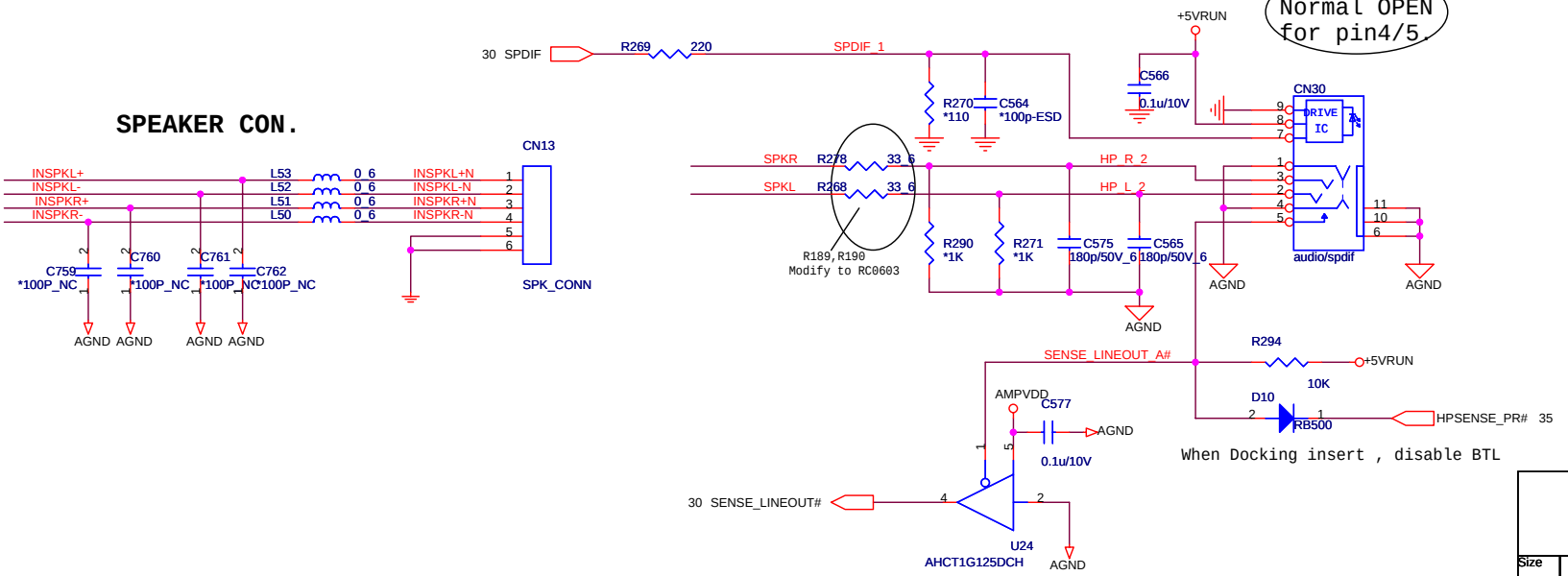
EAPD
low:mute



GAIN	SPKR MODE	HP MODE
0	10.5	3
1	9	0

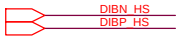
HEADPHONE OUT/SPDIF

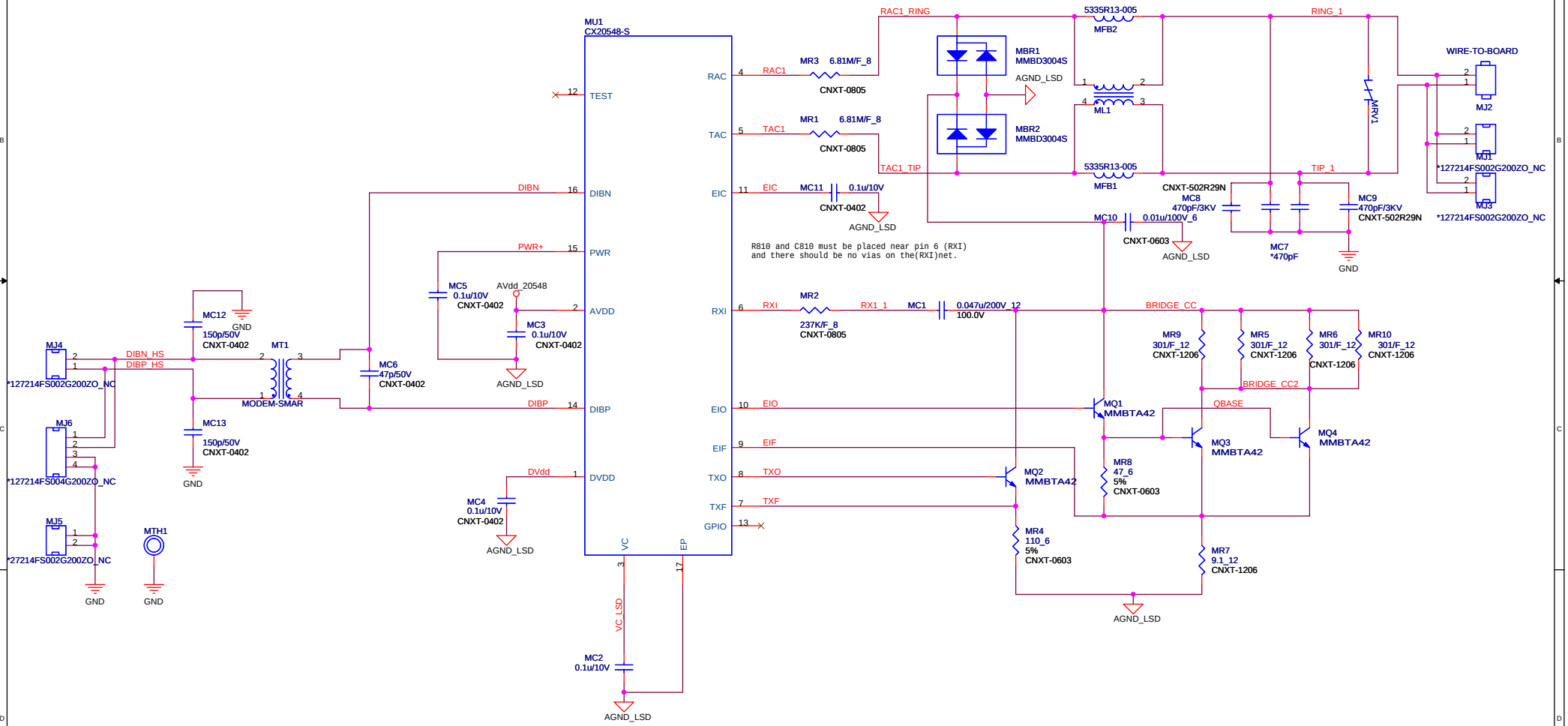
Check
Normal OPEN
for pin4/5.



Revision History		
REV	Description	Date
0	Initial Release	April 26, 2005

30 DIBN_HS
30 DIBP_HS



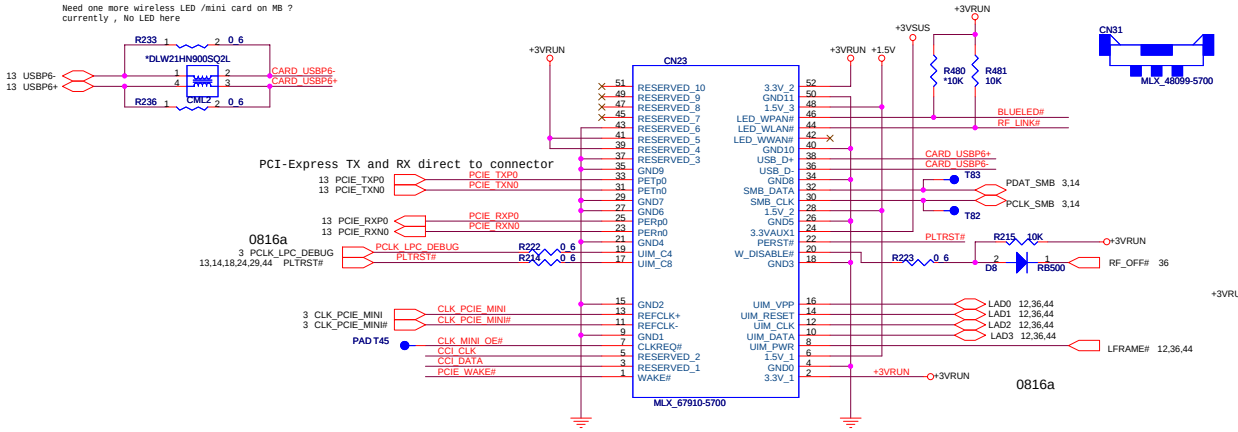


PROJECT : TW3
Quanta Computer Inc.

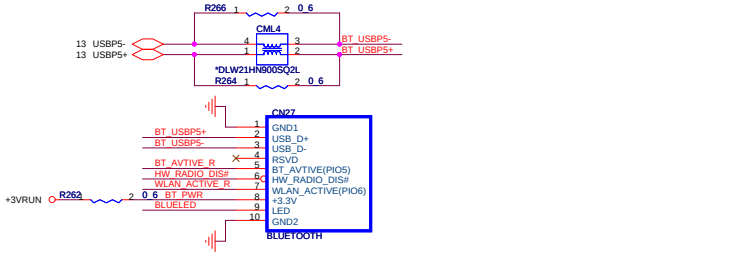
Size	Document Number	Rev
	Conexant Modem	B2A

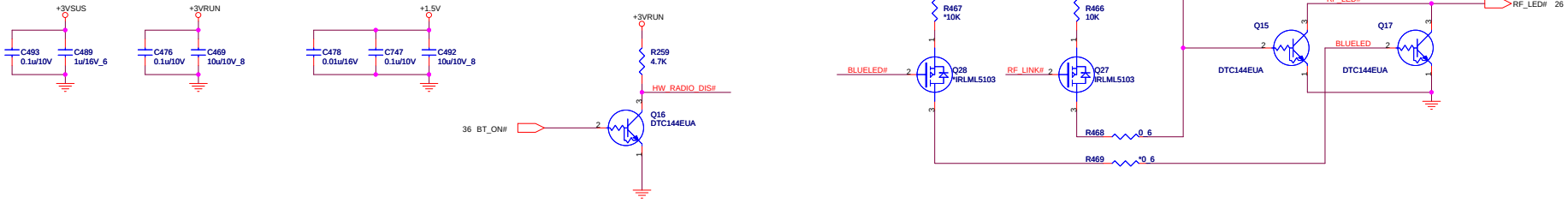
Date: Tuesday, January 03, 2006 Sheet 32 of 46

PCI-E Mini Card

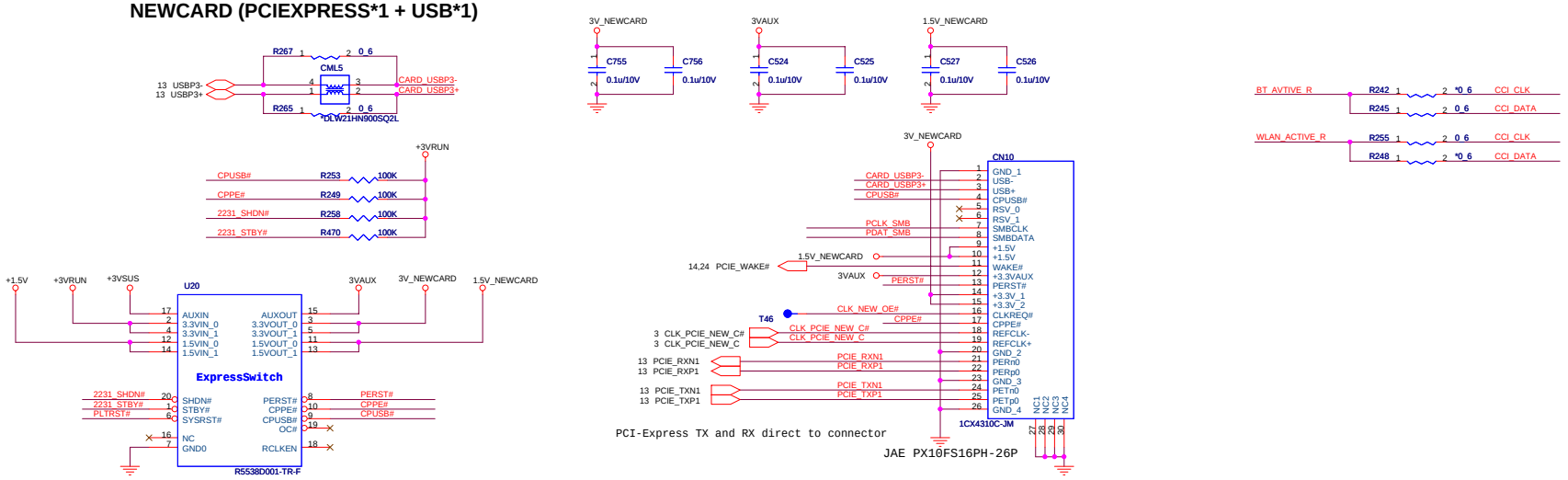


BLUETOOTH CONNECTOR

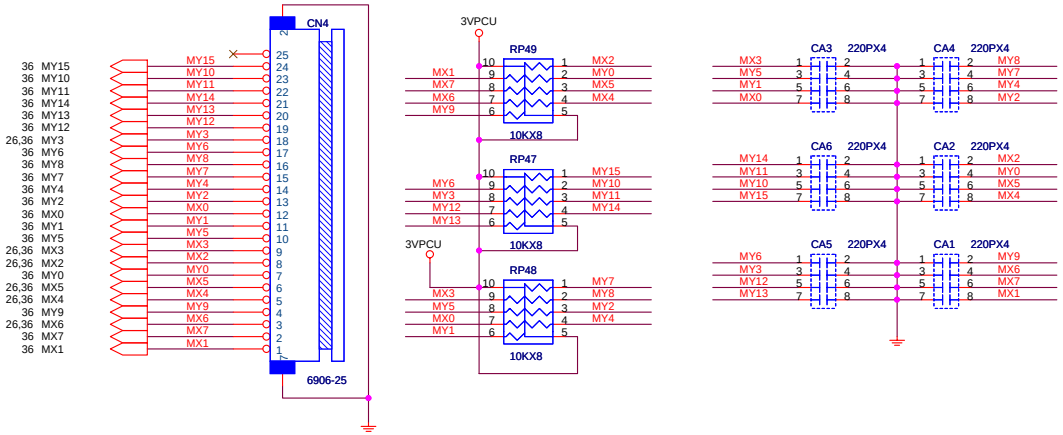


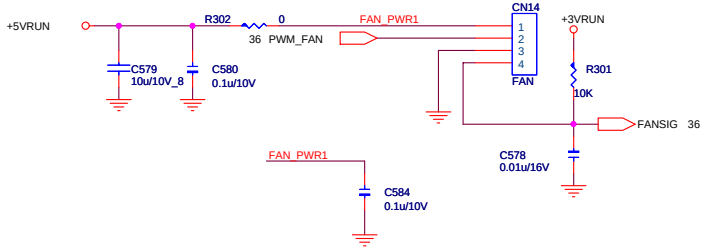


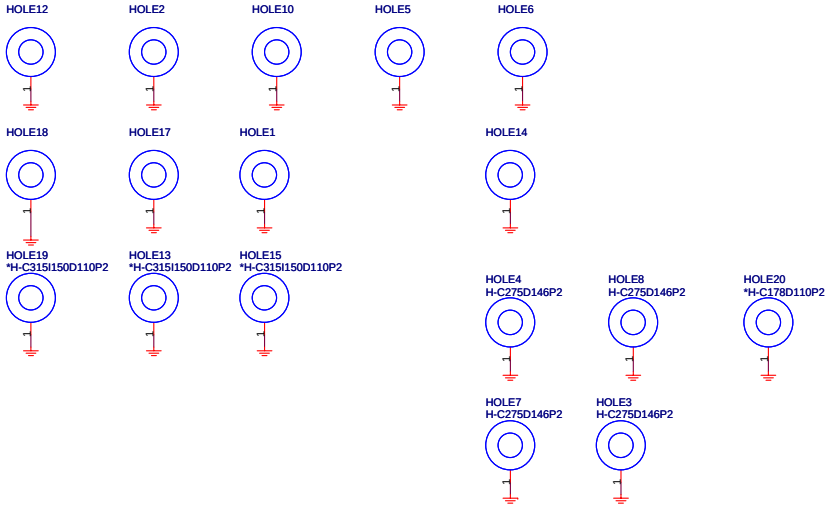
NEWCARD (PCIEXPRESS*1 + USB*1)



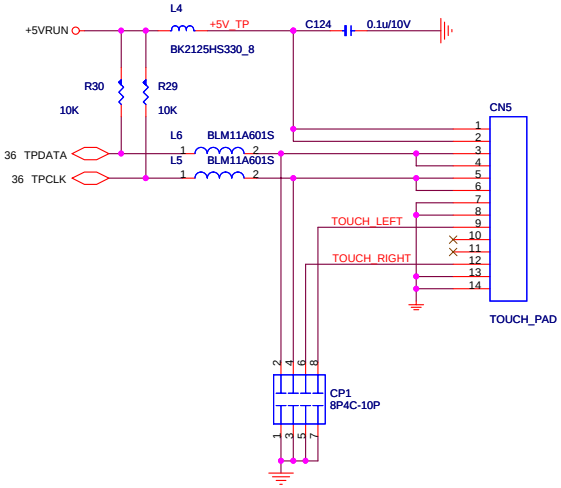
KeyBoard Interface

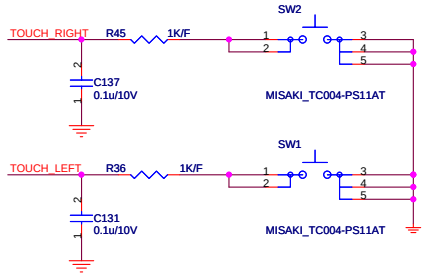






TOUCH PAD





PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	T/P,FAN,KB	B2A

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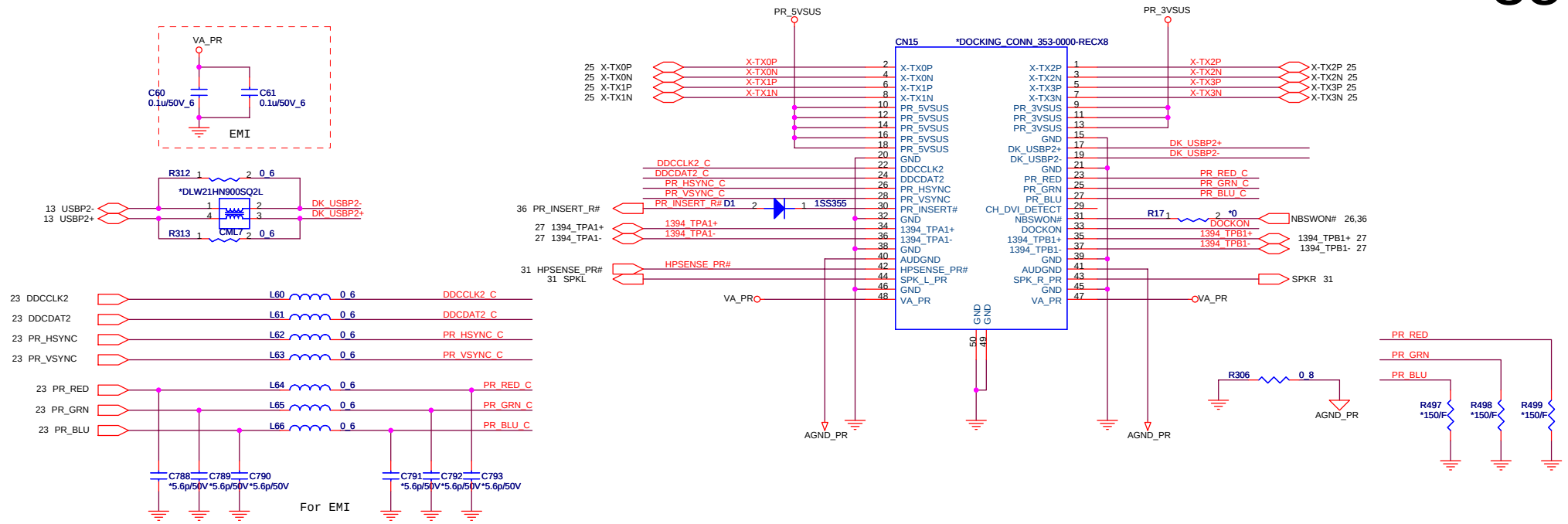
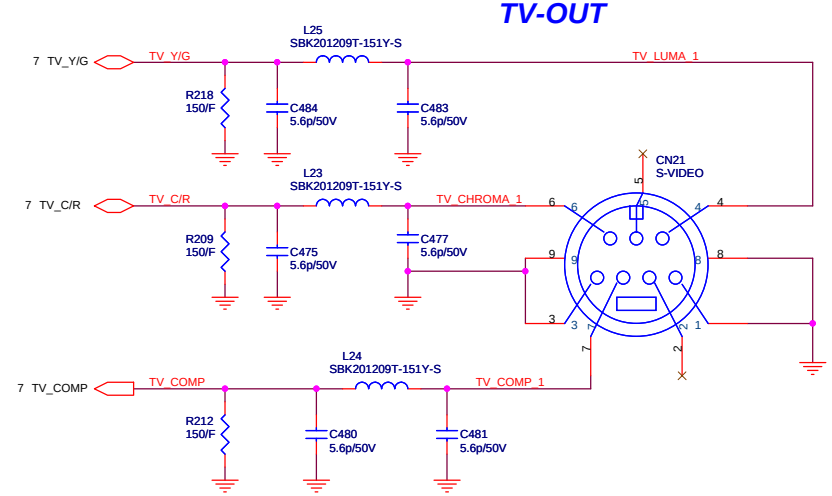
CABLE DOCKING CONNECTOR



TV-OUT



CX8PG181001 (180 ohm ,1.5A)

CH00606TB04 CH00606TB04

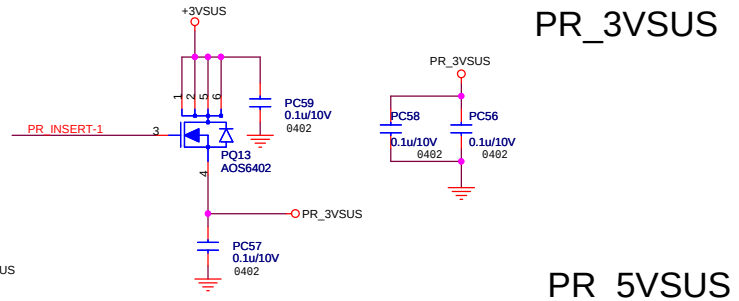
Intel CRB

150 ohm@ 100MHZ

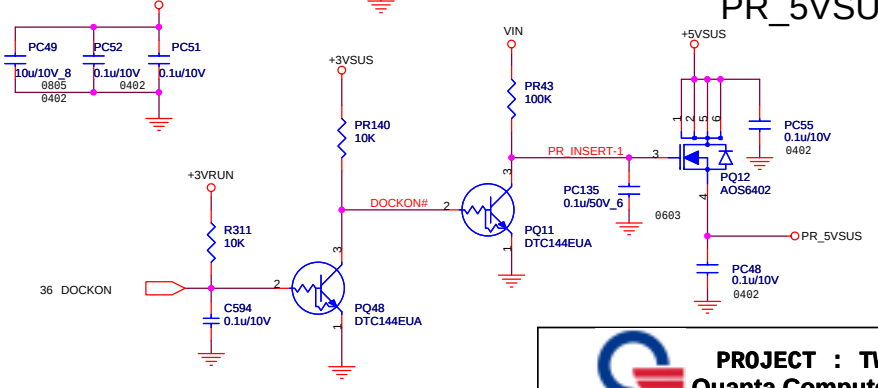
(100mA)

6pf 16V 6pf 16V

PR_3VSUS



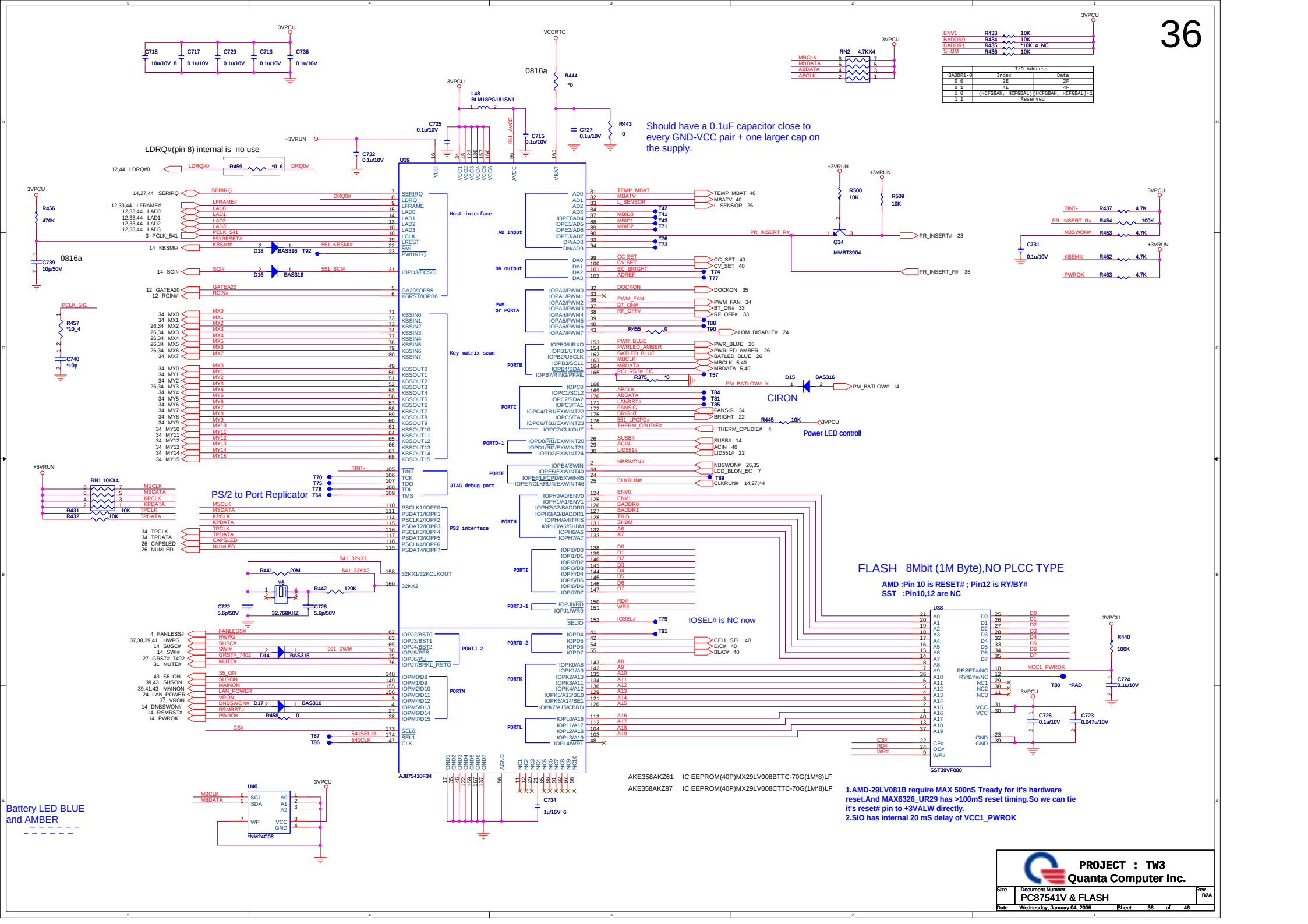
PR_5VSUS



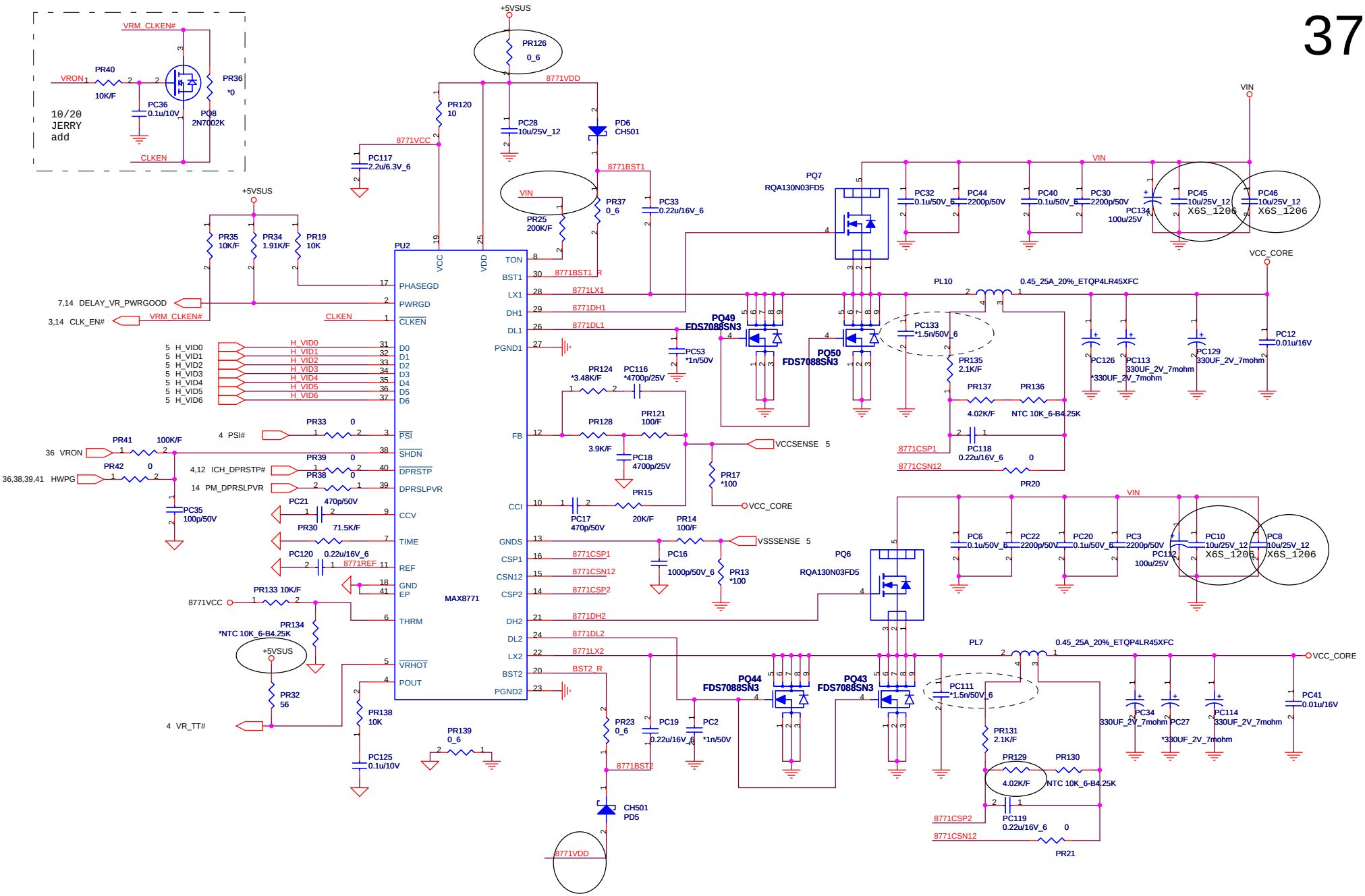
PROJECT : TW3

Quanta Computer Inc.

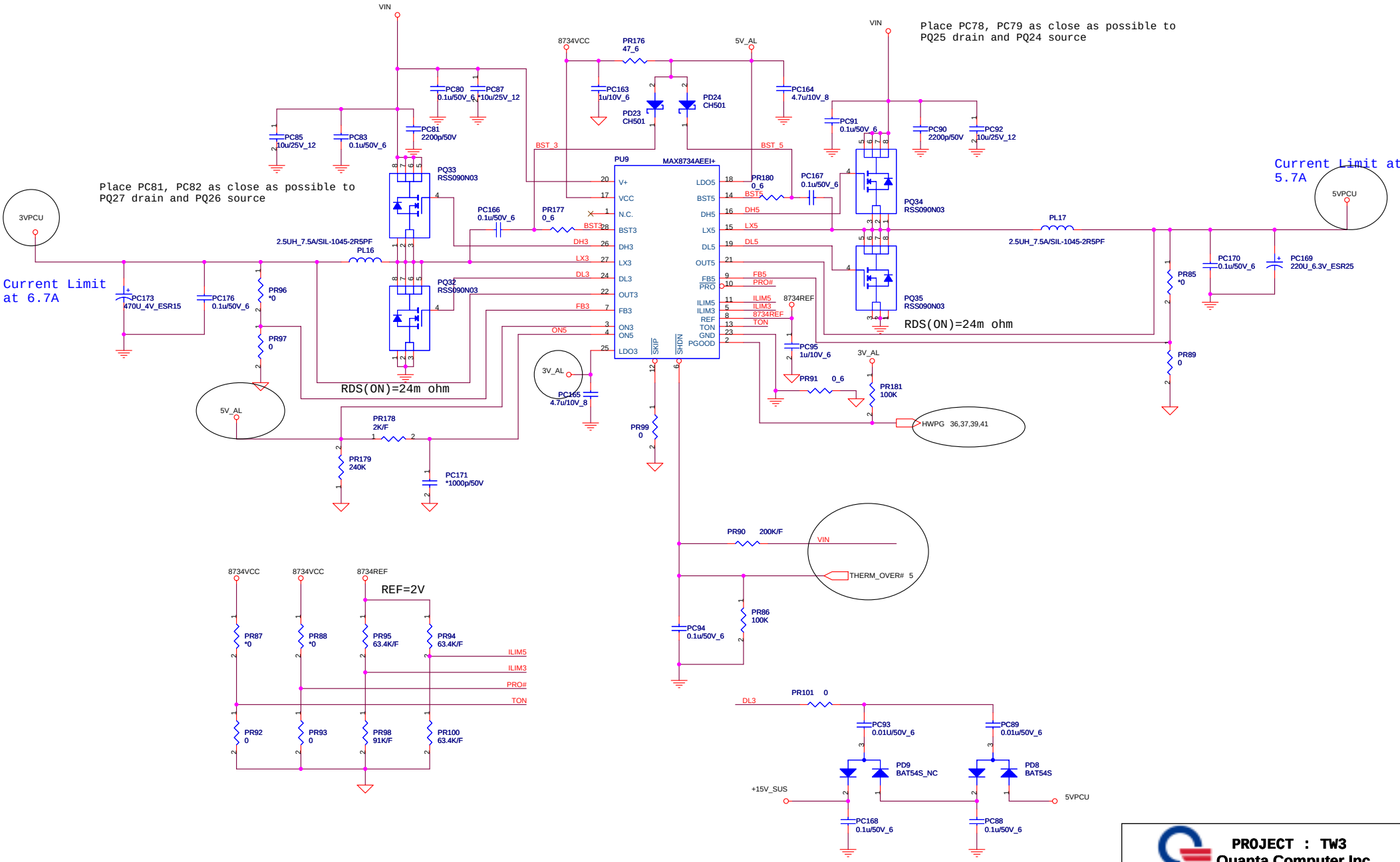
Size	Document Number	Rev
	PORT REPLICATOR	B2A
Date: Tuesday, January 03, 2006	Sheet 35 of 46	



PROJECT : TW3		
Quanta Computer Inc.		
Size	Document Number: PC87541V & FLASH	Rev: B2A
Date: Wednesday, January 04, 2006	Sheet 36 of 46	



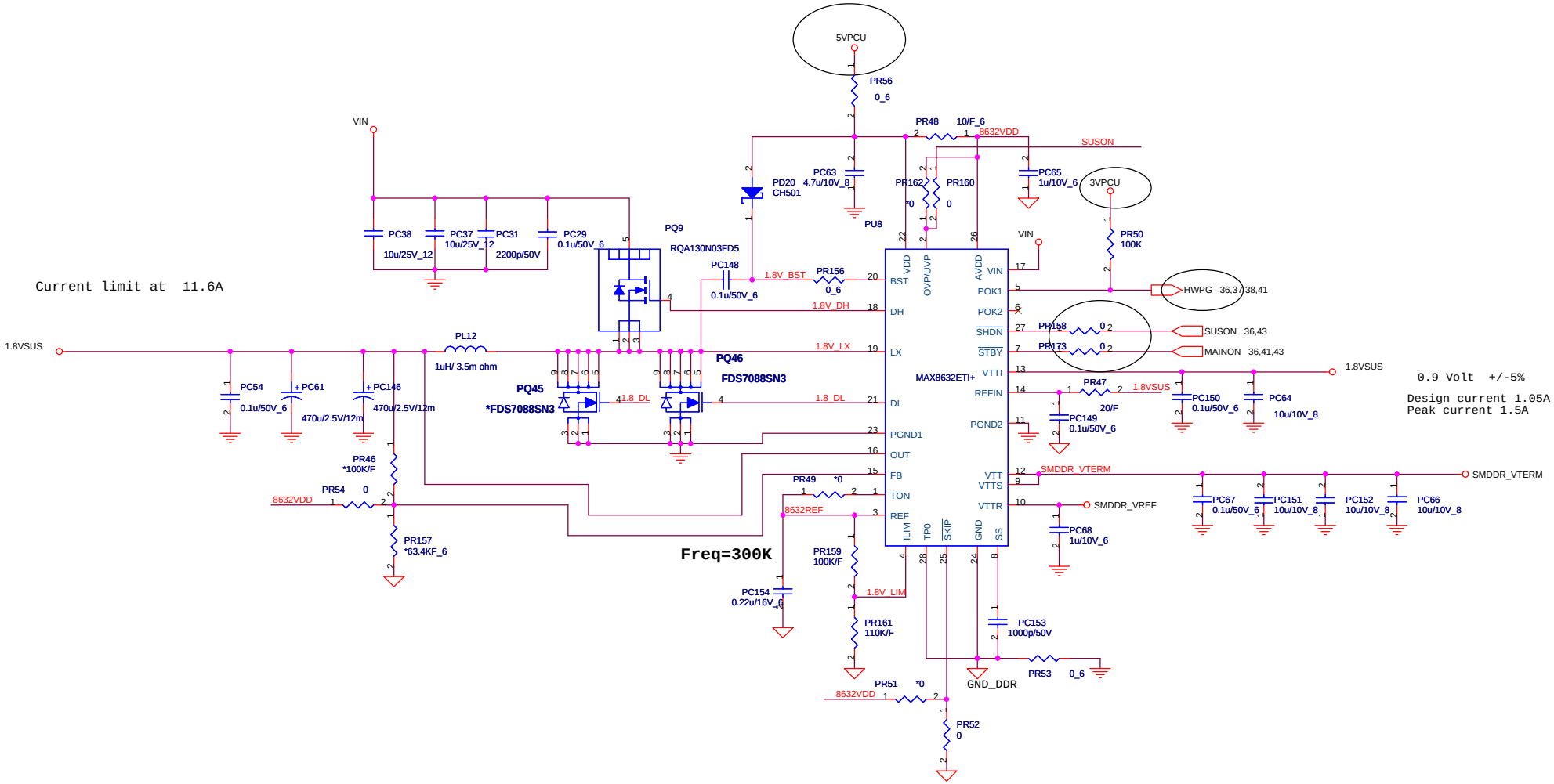
PROJECT : TW3		
Quanta Computer Inc.		
Size	Document Number: CPU CORE(ISL6262)	Rev: B2A
Date: Wednesday, January 04, 2006	Sheet 37 of 46	



PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	5V/3.3V(TPS51120)	B2A

Date: Tuesday, January 03, 2006 Sheet 38 of 46



PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	1.8VSUS/+0.9TERM/+2.5VSUS	B2A

Date: Tuesday, January 03, 2006 Sheet 39 of 46

Iinput =(V CLS / V REF)*(0.075/ RS1)

ICHG =(V ICTL / V REFIN)*(0.075/ RS2)

CELL-SET
0 = 4 CELL
1 = 3 CELL

300mil

PU1 MAX8724

PROJECT : DW1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CHARGER	B2A

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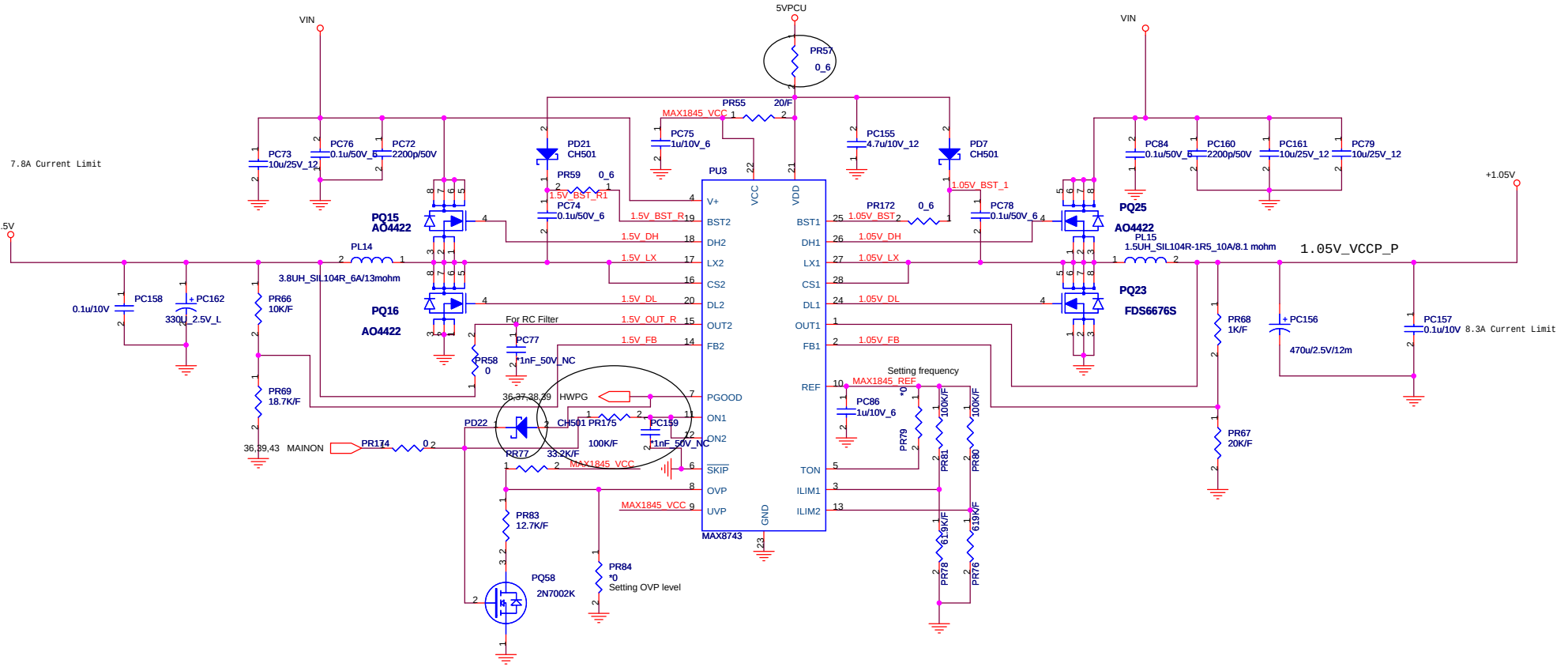
AO4422: Id= 11A, Rdson= 24m ohm, Qg= 19.8nC
FDS6676S: Id= 14.5A, Rdson= 7.25m ohm, Qg= 43 nC



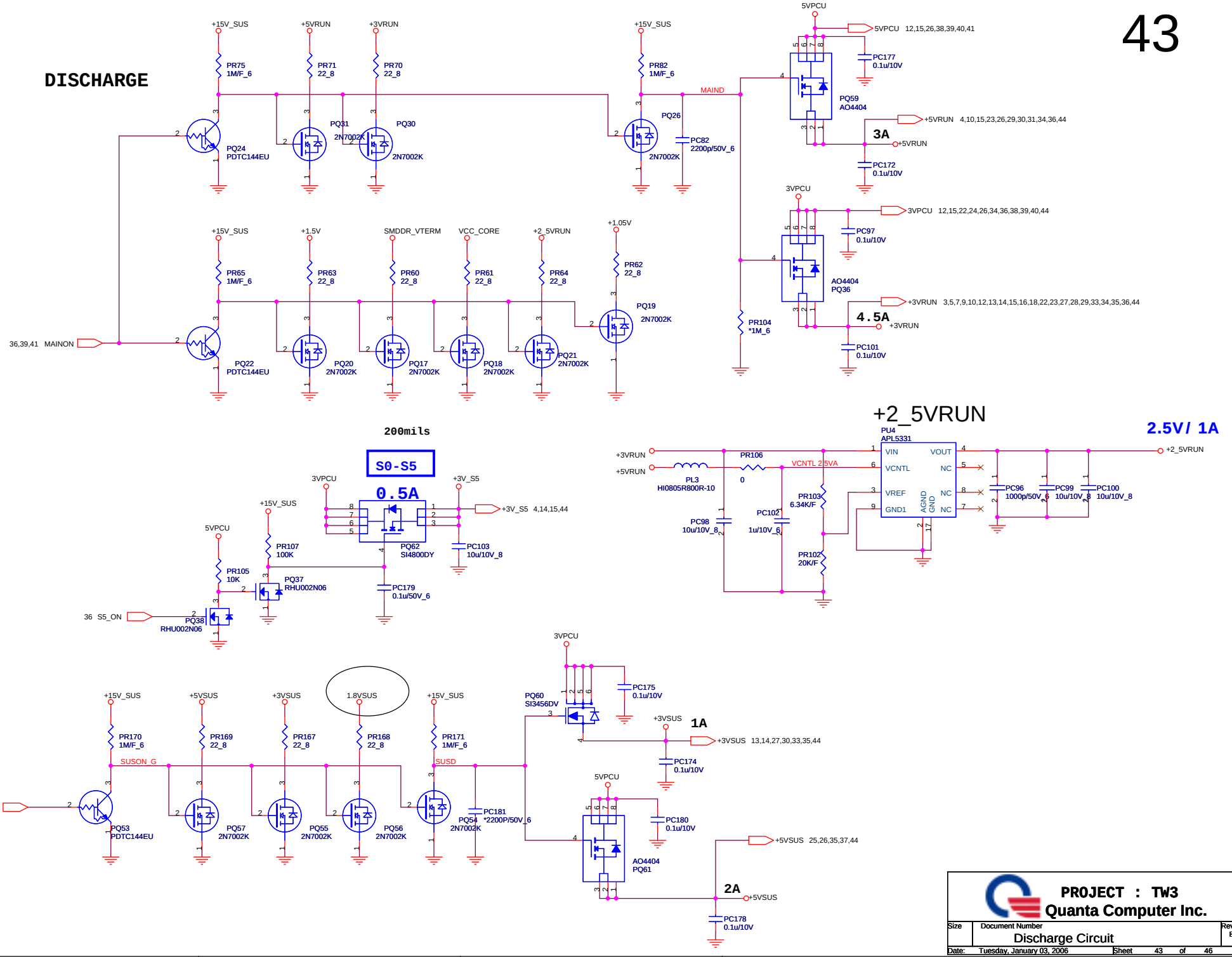
PROJECT : TW3		
Quanta Computer Inc.		
Size	Document Number: 1.05V&1.5V	Rev: B2A
Date: Tuesday, January 03, 2006	Sheet 41 of 46	

PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	Empty	B2A

Date: Tuesday, January 03, 2006 Sheet 42 of 46

DISCHARGE



+2_5VRUN

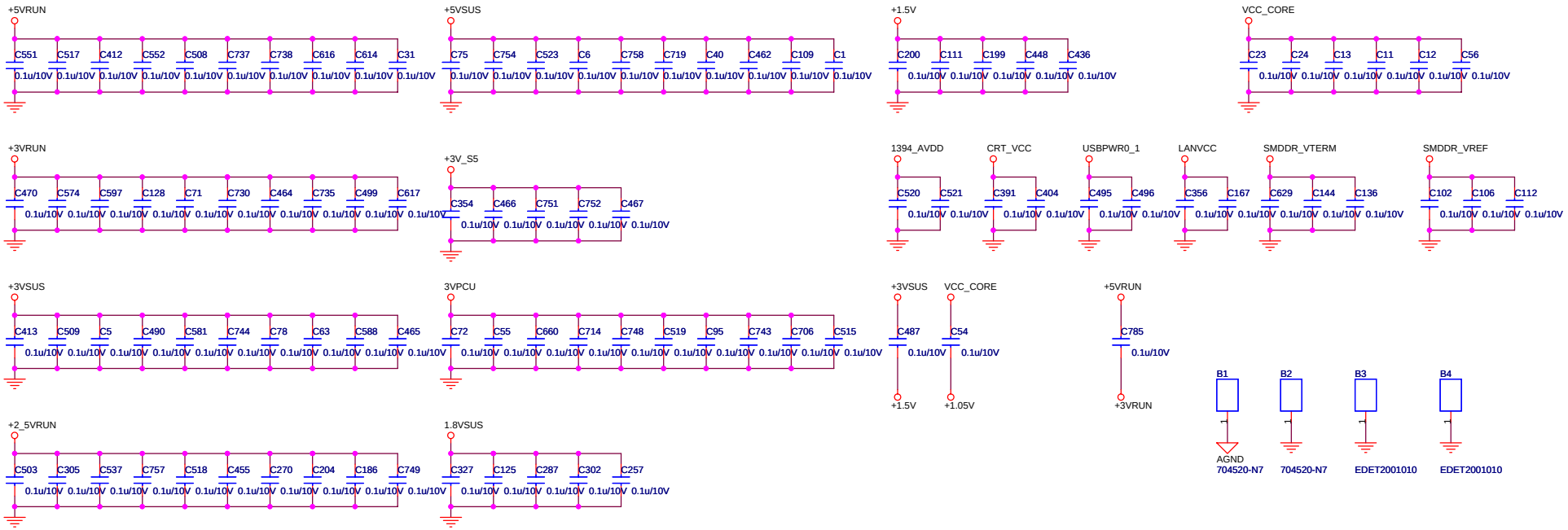
2.5V/ 1A

200mils

S0-S5

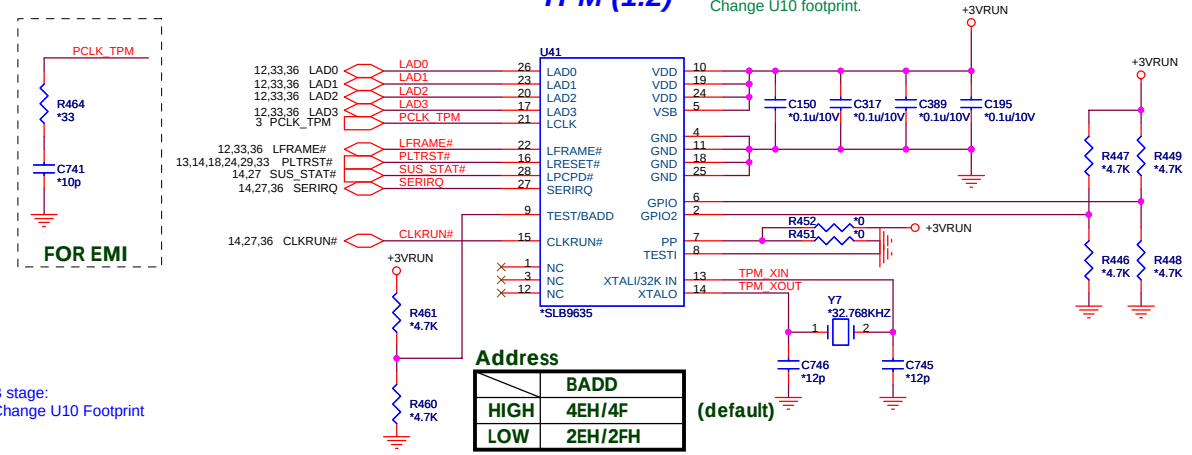
0.5A

PROJECT : TW3		
Quanta Computer Inc.		
Size	Document Number	Rev
	Discharge Circuit	B2A
Date: Tuesday, January 03, 2006	Sheet 43 of 46	



TPM (1.2)

B stage:
Change U10 footprint.



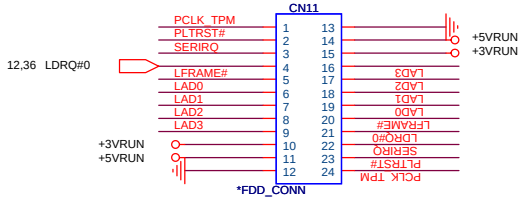
Address

	BADD
HIGH	4EH/4F
LOW	2EH/2FH

(default)

B stage:
Change U10 Footprint

Debug Conn.



PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	EMI & TPM & Debug Conn	B2A

Date: Wednesday, January 04, 2006 Sheet 44 of 46

MODEL	REV	CHANGE LIST		
TW3M M/B		Page	Description	
	B to 1223	Page 29	Change R472 to NI for SATA,install for PATA to solve sometimes ODD can't be detected and slow boot..	
		Page 33	Add R481,R480 to solve WLAN LED light leakage.	
		Page 3	Change R177 to install and pull low to set VGA clock to 100MHz.	
		Page 19	Change R345 to install to solve back light can't enable.	
		Page 29	Change R106 to NI for SATA,install for PATA.	
		Page 14	Add R482,R483 for CRT/DVI option.	
		Page 24	Change C645 to 10uF for LAN 1.2V per Marvell recommendation.	
		Page 19	R377 to install,R362,R365 to NI. (Set default to G72M)	
		Page 30	3V_DVDD connect to +3VSUS to solve WOR.	
	1223 to 1224	Page 32	Change MQ1,MQ2,MQ3,MQ4 to BA000420Z07 to solve MODEM low performance.	
		Page 37	Delete short pad.	
		Page 38	Delete short pad.PC92 change to install.	
		Page 39	Delete short pad.	
		Page 41	Delete short pad.	
		Page 43	Delete short pad.	
		Page 5	R19 change to NI for solving power-on shutdown.	
		Page 40	PR132 change to 13.3K.PR110 change to CS+0158JL11.	
		Page 34	HOLE3,HOLE4,HOLE7,HOLE8 change to MBRW1003011.	
		Page 37	PC34,PC113,PC114,PC129 change to CH733RM8831.	
		Page 23	F1 change to DK100TPU028.	
		Page 33	Q17 change to install for BT LED control.	
		Page 32	MC8,MC9 change to NI.	
		Page 34	Change CN4 footprint to "afn250-a2g1t-25p-l" for SMT issue.	
		Page 26	Change CN1.4 connection to RF_LED.	
		Page 33	Add NET RF_LED.	
		Page 36	Delete NET TUCHLED.	
		Page 31	Change C541,C546 to X7R for audio precision.	
	1223 to 1226	Page 38	Change PC93,PD9,PC168 to install. Delete NET 10V.	
		Page 41	Change NET 10V to +15V_SUS.	
		Page 26	LED2,LED3 change to dual color type(cost down and unify brightness and color).	
		Page 12	Reserve C784 on THERMTRIP for ESD.	
		Page 35	Reserve R497,R498,R499 for TW2 PR.	
		Page 33	Delete RP45,RP46,R210 for layout problem.	
	1226 to 1227	Page 33	Change CN23 to Molex (same as SW1). Add CN31 PCIE latch.	
		Page 44	Add EMI spring B1,B2,B3.	
		Page 32	Install MC8,MC9 for EMI.	
		Page 12	Change C459 TO 22pF for EMI.	
		Page 31	R479,R281,R295 change to install for EMI.	
	1227 to 1228	Page 3	Change Y1 P/N to BG614318081(CL=20pF) for solving system time delay issue.	
		Page 44	Add B4 for EMI.	
		Page 23	Change C694,C701,C703 to 10pF for signal quality.	
		Page 36	RN2 change to 4.7K for IIC signal quality.	
		Page 30	C528,C529 change to 1uF/10V X5R for audio precision.	
		Page 35	Add L60~L66,C788~C793 for EMI.	
	1227 to 1230	Page 26	Change CN9,CN12 P/N to DFHS04FRE80.	
		Page 36	Delete D13, add R508,R509,Q34 for PR leakage current.	

Model	TW3 M/B	
Page	From	To
1	1A	
2	1A	
3	1A	
4	1A	
5	1A	
6	1A	
7	1A	
8	1A	
9	1A	
10	1A	
11	1A	
12	1A	
13	1A	
14	1A	
15	1A	
16	1A	
17	1A	
18	1A	
19	1A	
20	1A	
21	1A	
22	1A	
23	1A	
24	1A	
25	1A	
26	1A	
27	1A	
28	1A	
29	1A	
30	1A	
31	1A	
32	1A	
33	1A	
34	1A	
35	1A	
36	1A	
37	1A	
38	1A	
39	1A	
40	1A	
41	1A	
42	1A	
43	1A	
44	1A	
45	1A	

PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	Change List (B2A)	B2A
Date: Wednesday, January 04, 2006	Sheet 45 of 46	

PROJECT: TW3	PCBA NO.	REV: 2B	DOC. NO :
APPROVED BY : Johnson Hsu	CHECK BY : Titan Chiang	DRAWING BY : Tony Huang	DATE :05/05/2005 SHEET 1

A. G72M to G72MV

1. change P/N to G72MV (AJ073000T14)
2. Set VGA core to 1.0V fix.
3. Change PCI_DEVID.

B. VRAM 128MB to 64MB

1.follow config table to set RAM_CFG.
2.Change VRAM P/N to HYNIX.
3.VRAMx2

C. LAN GIGA to 10/100.

1.Change LAN chip to 8038(AJ080380000).
2.Change Rset resistor.
3.Change transformer.

D. SATA to PATA

1.Set ODD to slave.
2.Set HDD to master.
3. Remove SATA conn.
4. Add PATA conn.
5. Change board ID to PATA.
6. Install resistor to connect ODD and HDD LED.
7. NI resistor of SATA LED.

MODEL	REV	CHANGE LIST		
TW3M		Page	Description	
	1230 to 0102	Page 38	PC173 change to 470uF.	
		Page 39	PC66 change to install.	
		Page 41	PD7,PD21,PD22 change to CH501.	
		Page 37	PD6,PD5 change to CH501.	
		Page 26	CN12,CN9 USB connector change to DIP type.	
		Page 29	CN25 pin25,26 and CN24 pin47,48 disconnect to GND.	
		Page 23	CN6 pin27,28 disconnect to GND.	
		Page 32	SW1,SW2 P/N change to DHP00FC1G16.	
		Page 36	Change R454 to 100K,R508,R509 to 10K.	
	0102 to 0103	Page 4	R101,R97,Q11 change to install.	
		Page 6,7,8,9,10,11	Change U32 P/N to AJSL8Z20T17.(945GM)	
		Page 12,13,14,15	Change U36 P/N to AJSL8YB0T12.(ICH7M)	
		Page 44	Add C785 for EMI.	
		Page 37	PR128 change to 3.9K.	

Model / Page	TW3 M/B From	To
1	1A	
2	1A	
3	1A	
4	1A	
5	1A	
6	1A	
7	1A	
8	1A	
9	1A	
10	1A	
11	1A	
12	1A	
13	1A	
14	1A	
15	1A	
16	1A	
17	1A	
18	1A	
19	1A	
20	1A	
21	1A	
22	1A	
23	1A	
24	1A	
25	1A	
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31	1A	
32	1A	
33	1A	
34	1A	
35	1A	
36	1A	
37	1A	
38	1A	
39	1A	
40	1A	
41	1A	
42	1A	
43	1A	
44	1A	
45	1A	

PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	Change List (B2A)	B1A

Date: Wednesday, January 04, 2006 Sheet 46 of 46

PROJECT: TW3	PCBA NO.	REV: 2B	DOC. NO :	
APPROVED BY : Johnson Hsu	CHECK BY : Titan Chiang	DRAWING BY : Tony Huang	DATE :05/05/2005	SHEET 1