AMD Geode™ LX EPIC RDK Reference Schematic

NOTES:
1) UNLESS OTHERWISE SPECIFIED RESISTORS HAVE 5% TOLERANCE.

2) UNLESS OTHERWISE SPECIFIED CAPACITORS HAVE 20% TOLERANCE.

IMPORTANT NOTICE:

1. THIS DOCUMENT MAY NOT REFLECT THE MOST RECENT CHANGES IN BOARD DEVELOPMENT AND DEBUG. ANY DEVELOPER INTENDING TO USE THIS SCHEMATIC AS A REFERNCE SHOULD CONTACT THEIR LOCAL FIELD APPLICATIONS ENGINEER, REGIONAL SALES OFFICE, OR PROGRAM MANAGER FOR SCHEMATIC UPDATES, DESIGN RECOMMENDATIONS AND PCB LAYOUT GUIDELINES. AMD ALSO RECOMMENDS A DESIGN REVIEW OF BOTH THE SCHEMATIC DIAGRAM AND PCB LAYOUT BEFORE CONSIDERING PRODUCTION.

2. AMD RESERVES THE RIGHT TO CHANGE DESIGNS OR SPECIFICATIONS WITHOUT NOTICE. CUSTOMERS ARE ADVISED TO OBTAIN THE LATEST VERSIONS OF PRODUCT SPECIFICATIONS, WHICH SHOULD BE CONSIDERED IN EVALUATING A PRODUCT'S APPROPRIATENESS FOR A PARTICULAR USE.

3. AMD MAKES NO WARRANTIES, EXPRESSED OR IMPLIED, FOR MERCHANTABILITY OR FITNESS FOR A PARTICULAR APPLICATION. IN NO EVENT SHALL AMD BE LIABLE FOR ANY INDIRECT, SPECIAL, INCIDENTAL OR CONSEQUENTIAL DAMAGES AS A RESULT OF THE PERFORMANCE, OR FAILURE TO PEFORM, OF ANY AMD PRODUCT OR DOCUMENTATION.

IMPORTANT NOTES ABOUT THIS SCHEMATIC

DESIGN NOTE: Example text for the design note to show the note inside the colored box.

1) DESIGN NOTES in grey are information notes.

DESIGN NOTE: Example text for the design note to show the note inside the colored box.

2) DESIGN NOTES in yellow are notes of caution.

DESIGN NOTE: Example text for the design note to show the note inside the colored box.

3) DESIGN NOTES in red are critical, and must be understood and followed.

AMD CONFIDENTIAL

Advanced Micro Devices
1351 South Sunset St.
Longmont CO 80501

Title	AMD GEODE™ LX EPIC RDK Reference Schematic		
Document Number	40744	Rev	D
Size B	Date: Wednesday, April 11, 2007	Sheet	1 of 26

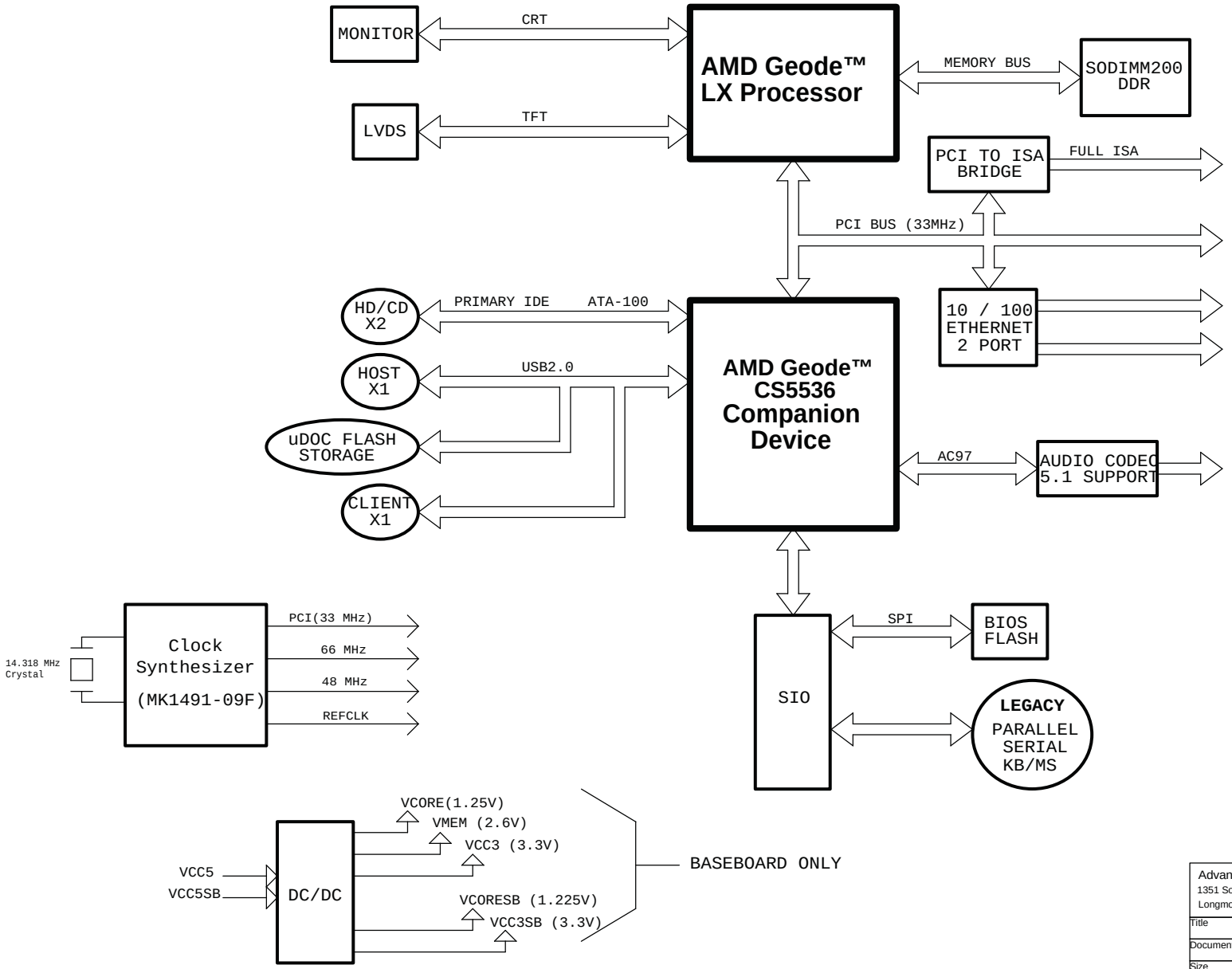
REVISION HISTORY:

REV	DATE	NOTES
A	07-09-2006	* Initial Release
B	12-04-2006	* Page 8 - Changed LX symbol - DRGB6 pin from Y32 to AH8
C	01-19-2007	* Page 10 - Connected C102-C108 to Ground
		* Page 13 - Connected C133-C137 and C149-C152 to Ground
D	04-10-2007	* Page 13 - Added design note regarding USB VCORE supply.

AMD CONFIDENTIAL

Advanced Micro Devices
1351 South Sunset St.
Longmont CO 80501

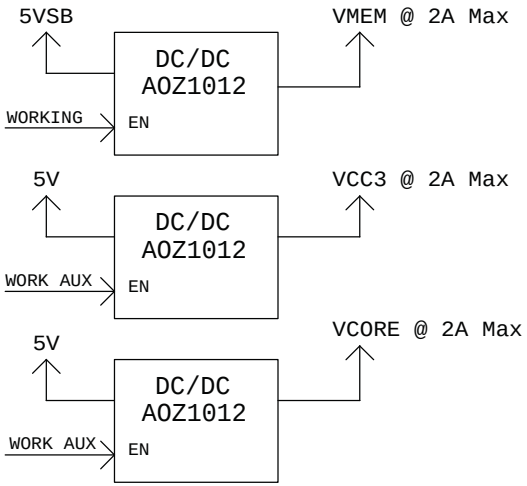
Title: AMD GEODE™ LX EPIC RDK Reference Schematic			
Document Number: 40744		Rev: D	
Size: B	Date: Wednesday, April 11, 2007	Sheet 2 of 26	

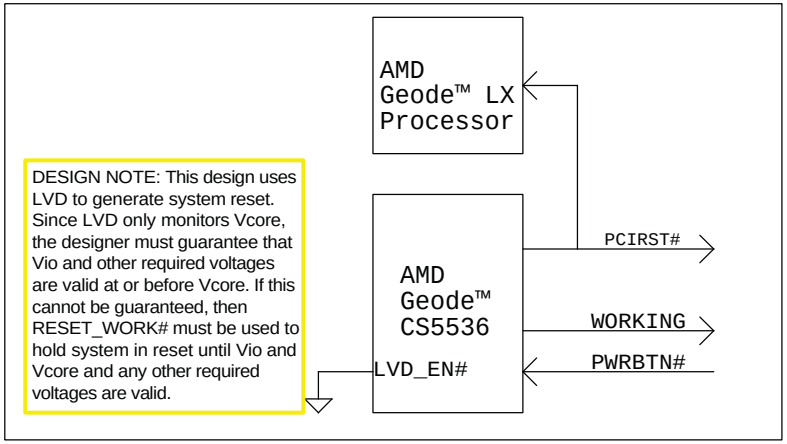


AMD CONFIDENTIAL

Advanced Micro Devices
1351 South Sunset St.
Longmont CO 80501

Title	AMD GEODE™ LX EPIC RDK Reference Schematic		
Document Number	40744	Rev	D
Size B	Date: Wednesday, April 11, 2007	Sheet	3 of 26





SYSTEM POWER

VCC=+5.0V
VCC3=+3.30V - BASEBOARD
VCC3_EXT=+3.30V - PC104 SLOTS

AMD Geode™ LX Processor

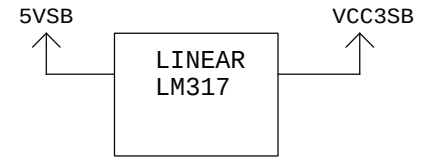
VCORE=+1.25V
VCCMEM=+2.60V
MVREF=+1.3V
VIO=+3.30V

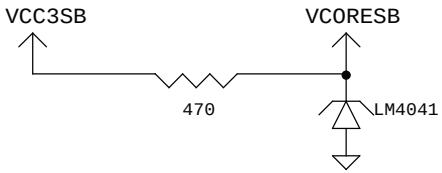
AMD Geode™ CS5536

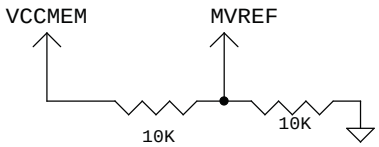
VCORE=+1.25V
VCORESB=+1.225V
VIO=+3.30V

MEMORY

VMEM=+2.60V
MVREF=+1.3V







Power On and Reset Sequence - Cold start

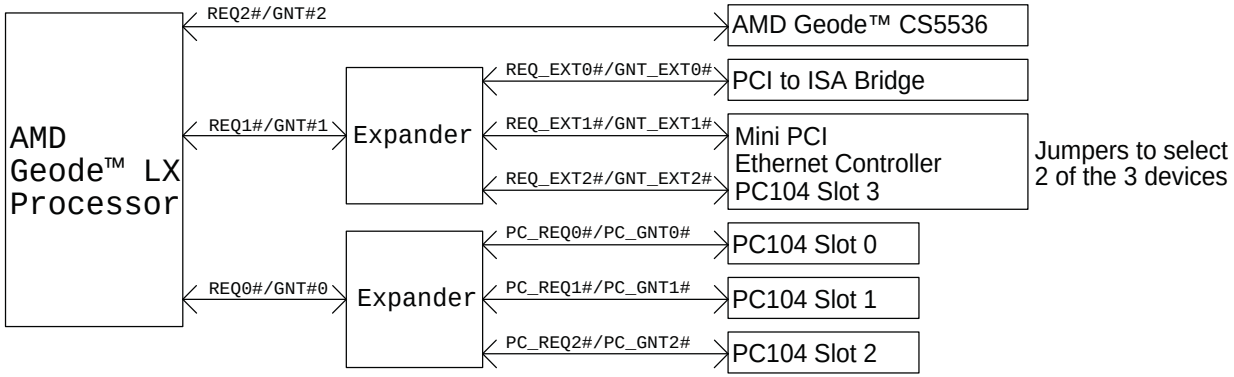
5VSB → 3.3VSB / 1.225VSB → PWRBTN# → 5V → WORKING → VCC3 / VCORE / VMEM → LVD → SYS_RST# → PCIRST#

AMD CONFIDENTIAL

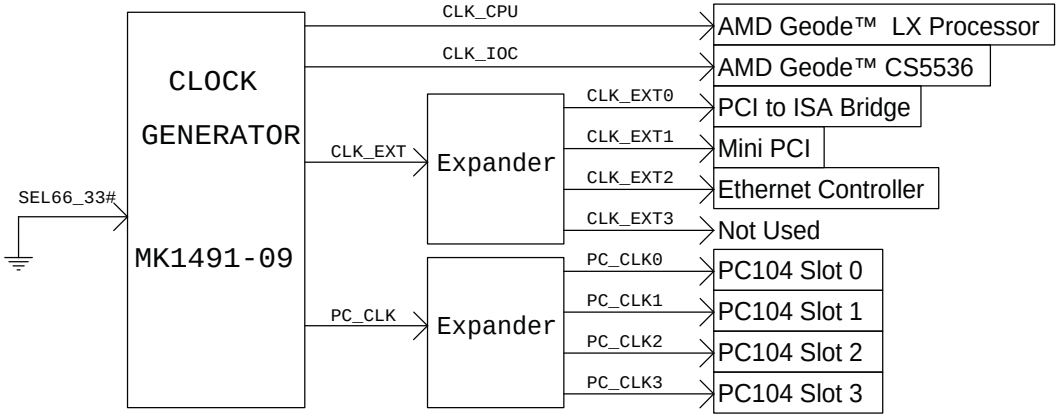
Advanced Micro Devices
1351 South Sunset St.
Longmont CO 80501

Title	AMD GEODE™ LX EPIC RDK Reference Schematic	
Document Number	40744	Rev D
Size B	Date: Wednesday, April 11, 2007	Sheet 4 of 26

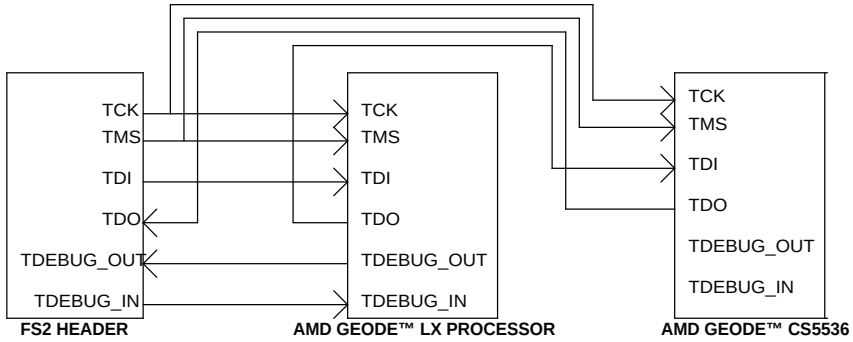
PCI MASTER SETTING



PCI CLOCK SETTING



JTAG DAISY CHAIN MODE WITH AMD GEODE™ CS5536 COMPANION DEVICE



SEL66_33#	Function
1	PCI 66 MHz
0	PCI 33 MHz

AMD CONFIDENTIAL

Advanced Micro Devices
1351 South Sunset St.
Longmont CO 80501

Title	AMD GEODE™ LX EPIC RDK Reference Schematic
Document Number	40744
Rev	D
Size	B
Date:	Wednesday, April 11, 2007
Sheet	5 of 26

DESIGN NOTE: See LX layout guidelines for latest recommendations on memory routing.

DESIGN NOTE: BA0,BA1 must be trace length matched to within 50 mils.

DESIGN NOTE: Use SDCLK pairs that are most convient for clean routing.

DESIGN NOTE: Swap series resistors on the DQS lines in order minimize the number of vias.

DESIGN NOTE: Swap series resistors on the address lines in order minimize the number of vias.

DESIGN NOTE: Do not swap series resistors on the DQS, DQM or Data lines with the Address or control lines.

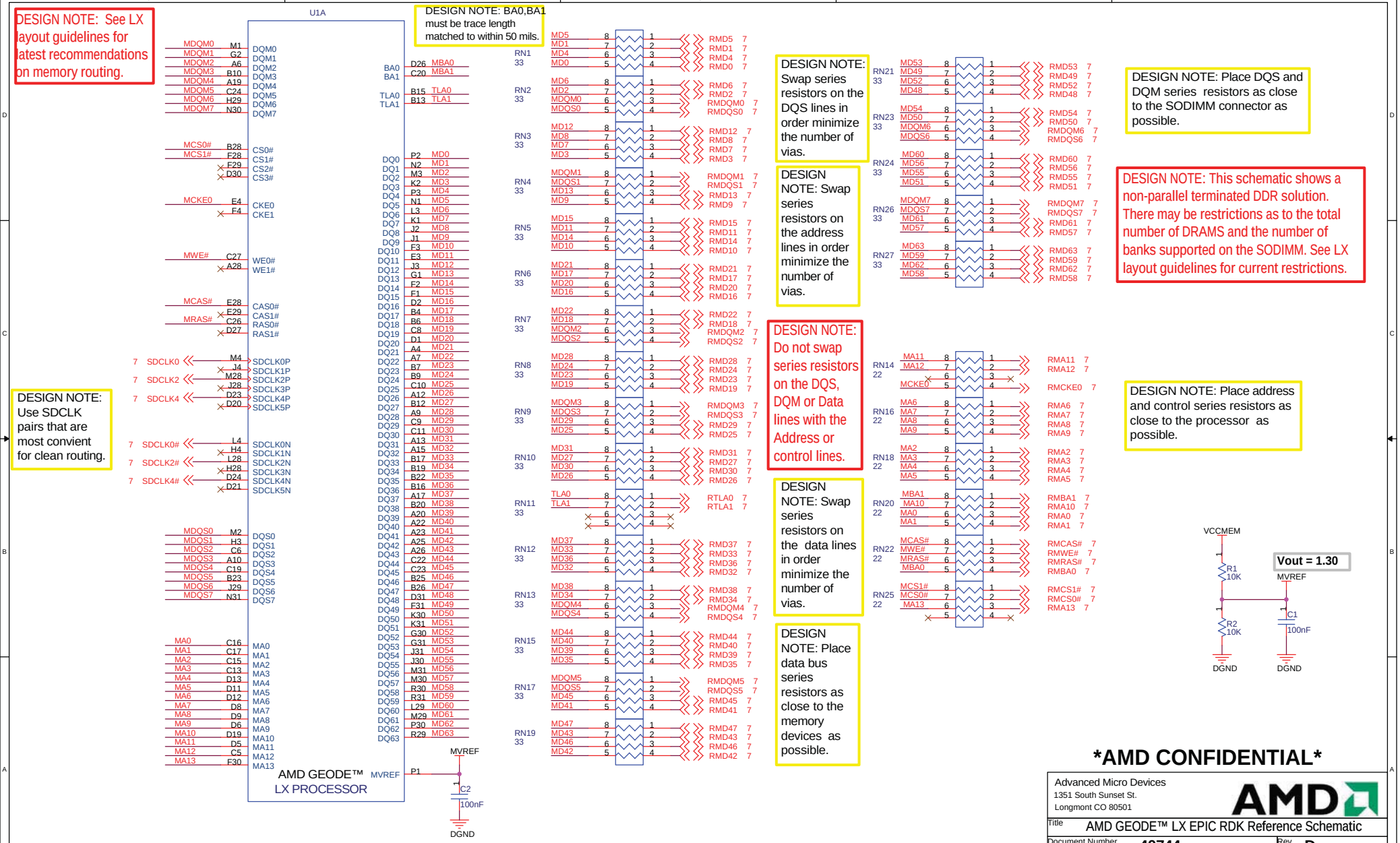
DESIGN NOTE: Swap series resistors on the data lines in order minimize the number of vias.

DESIGN NOTE: Place data bus series resistors as close to the memory devices as possible.

DESIGN NOTE: Place DQS and DQM series resistors as close to the SODIMM connector as possible.

DESIGN NOTE: This schematic shows a non-parallel terminated DDR solution. There may be restrictions as to the total number of DRAMS and the number of banks supported on the SODIMM. See LX layout guidelines for current restrictions.

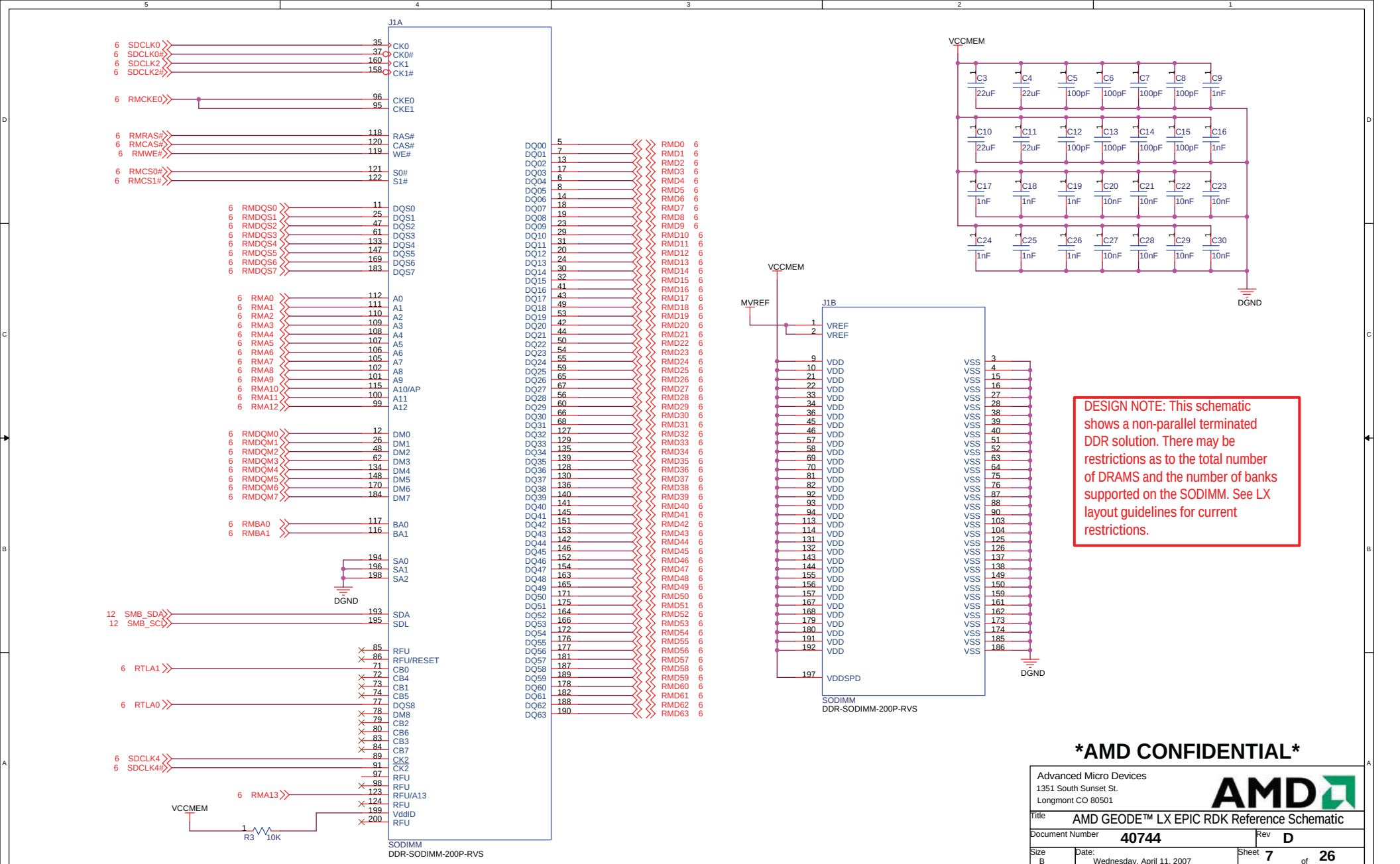
DESIGN NOTE: Place address and control series resistors as close to the processor as possible.



AMD CONFIDENTIAL

Advanced Micro Devices
1351 South Sunset St.
Longmont CO 80501

Title	AMD GEODE™ LX EPIC RDK Reference Schematic
Document Number	40744
Rev	D
Size	B
Date:	Wednesday, April 11, 2007
Sheet	6 of 26



AMD CONFIDENTIAL

Advanced Micro Devices 1351 South Sunset St. Longmont CO 80501	AMD
Title	AMD GEODE™ LX EPIC RDK Reference Schematic
Document Number 40744	Rev D
Size B	Date: Wednesday, April 11, 2007
Sheet 7 of 26	

High Speed Input Port

DESIGN NOTE: 8-bit Data Streaming Mode is the simplest data input mode, but is limited to 8-bits.

DESIGN NOTE: When using 16 data capture mode (Mode 4 - BT.601), the TFT interface cannot be used due to pin sharing conflicts.

DESIGN NOTE: There are two conventions for connecting 24 bit panels. One is backward compatible with 18 bit panels. The connections defined here are backwards compatible.

DESIGN NOTE: The LSB's for each color (R0,R1,G0,G1,B0,B1) are not used in by 18-bit panels.

DESIGN NOTE: For 18-bit panels use OUT0, OUT1, and OUT2. For 24-bit panels use OUT0, OUT1, OUT2, and OUT3.

DESIGN NOTE: AGND_VGA should be an island with single point connection to the full ground plane to reduce noise content. Zero ohm resistor can be removed as long as above condition is met.

J3 — PFL-2x20-2M0-SMD-S

U26C — AMD GEODE™ LX PROCESSOR

U2 — DS90C385 — TSSOP56 Package

U22, U23 — NC7SZ125/SC70

D1 — LM4041AIM3-1.2

FB1, FB2 — BLM18PG600SN1

24-bit LVDS Transmitter

AMD CONFIDENTIAL

Advanced Micro Devices
1351 South Sunset St.
Longmont CO 80501

Title	AMD GEODE™ LX EPIC RDK Reference Schematic
Document Number	40744
Rev	D
Size	B
Date:	Wednesday, April 11, 2007
Sheet	8 of 26

DESIGN NOTE: There are 8 PCI devices in this design requireing REQ / GNT pairs. Two 1 to 3 expanders are provided, giving a total of 7 pairs. Two pairs are mapped to the following three devices: Ethernet, MiniPCI and PC104 slot 3. Jumpers are provided to select.

U1B

AMD GEODE™ LX PROCESSOR

PCI_PAR 11,15,19,20,24

PCI_AD[31:0] 11,15,19,20,24

5	4	3	2	1	CORE	MEM
Off	On	Off	Off	Off	500	400
Off	On	Off	Off	On	500	333
Off	On	On	On	On	433	333
On	On	On	On	On	Bypass	Bypass

Debug Stall

Normal Setting

DESIGN NOTE: Two REQ/GNT pairs are mapped to the following three devices: Ethernet, MiniPCI and PC104 slot 3. Jumpers are provided to select.

DESIGN NOTE: CLKFB output is used internally by the 8209 to produce the zero delay.

U1D

AMD GEODE™ LX PROCESSOR

DESIGN NOTE: COREPLLGND, DOTPLLGND and GLPLLGND should each be an island with single point connection to the full ground plane to reduce noise content. Zero ohm resistor can be removed as long as above condition is met.

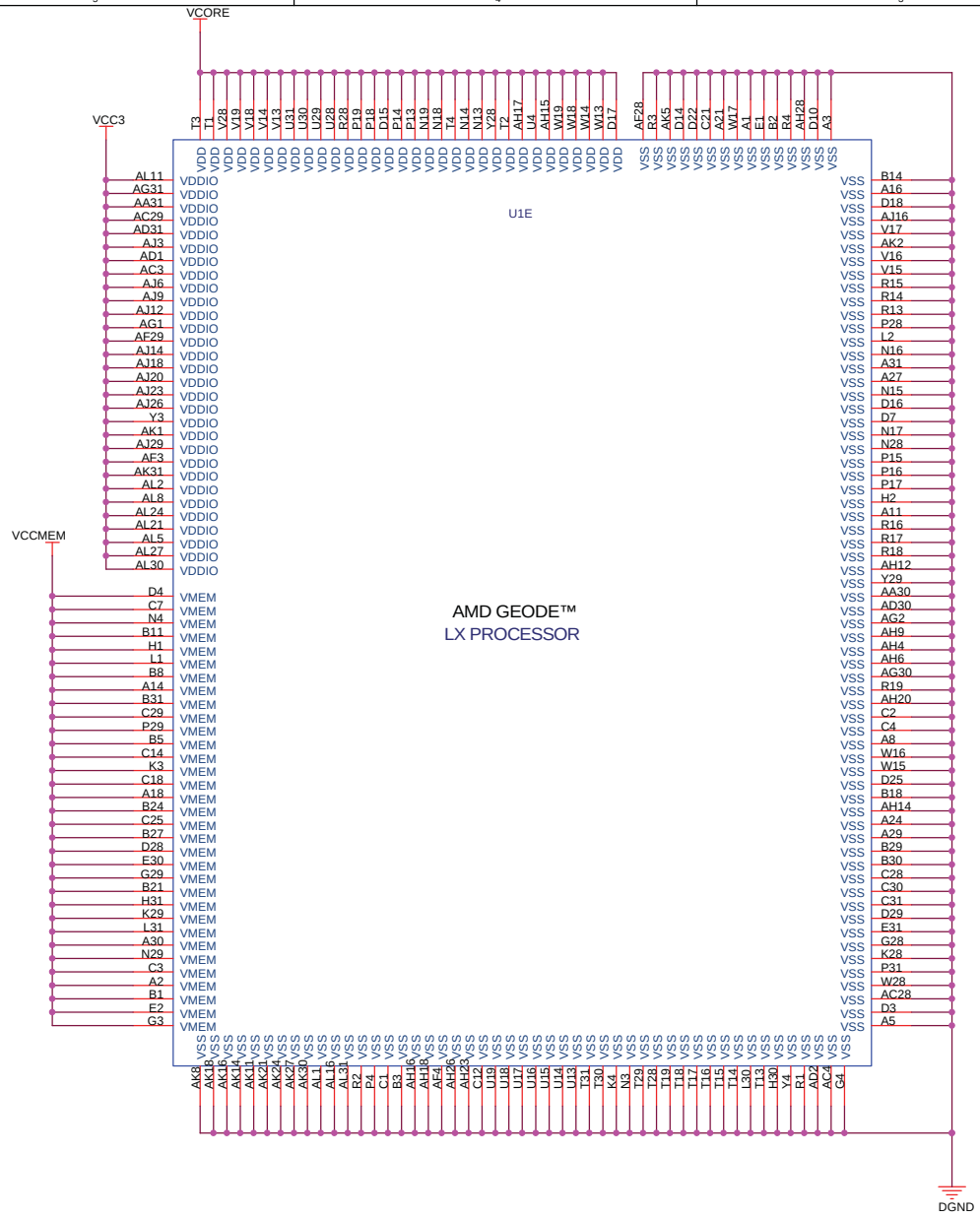
JTAG HEADER

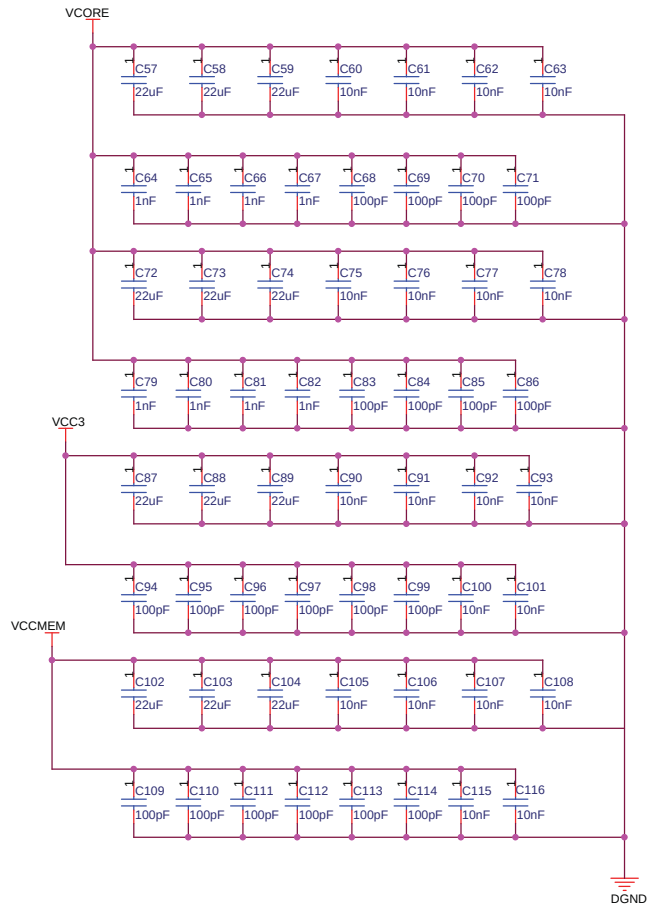
DESIGN NOTE: Add "JTAG HEADER" to the silkscreen

AMD CONFIDENTIAL

Advanced Micro Devices
1351 South Sunset St.
Longmont CO 80501

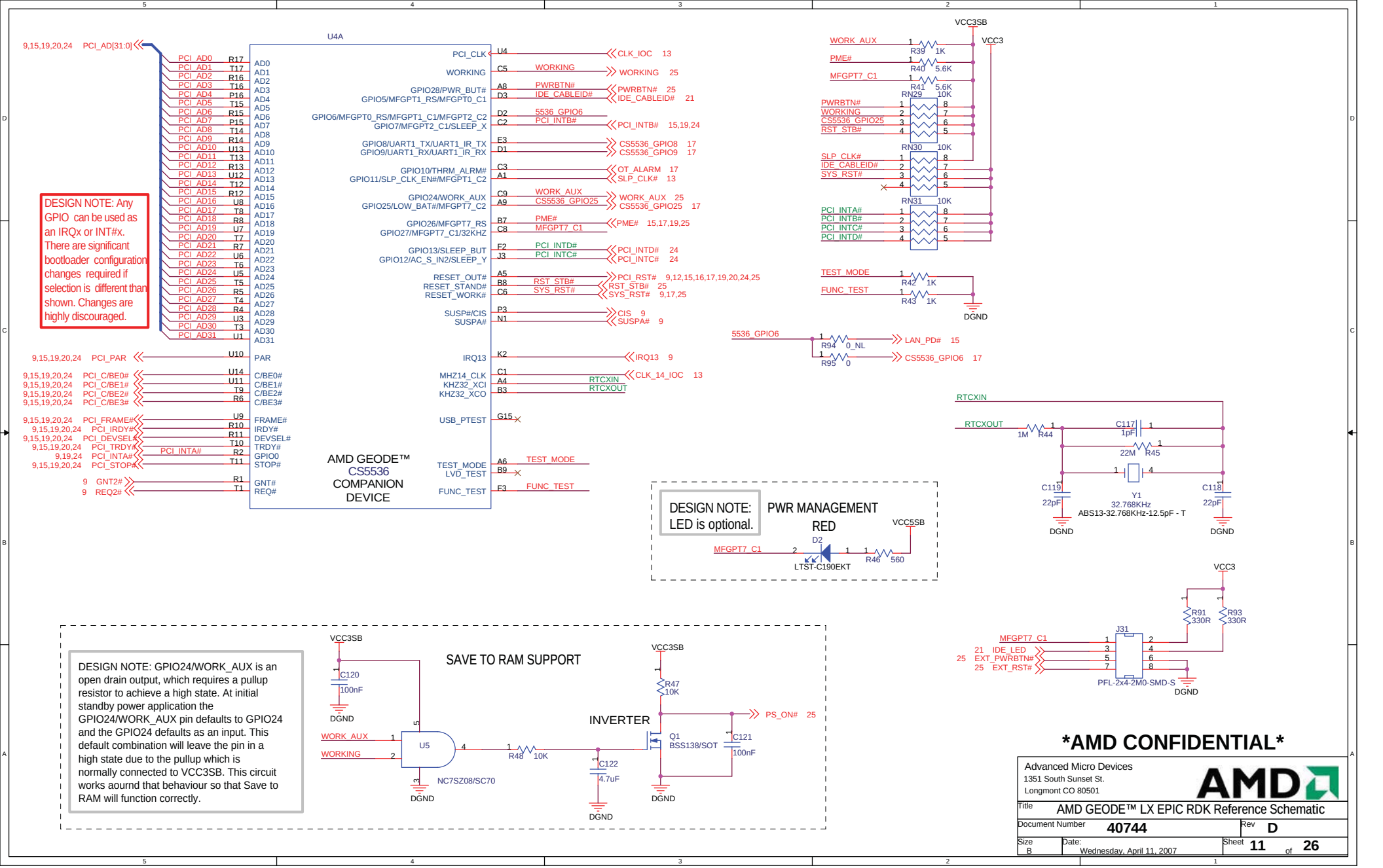
Title	AMD GEODE™ LX EPIC RDK Reference Schematic
Document Number	40744
Rev	D
Size	B
Date:	Wednesday, April 11, 2007
Sheet	9 of 26



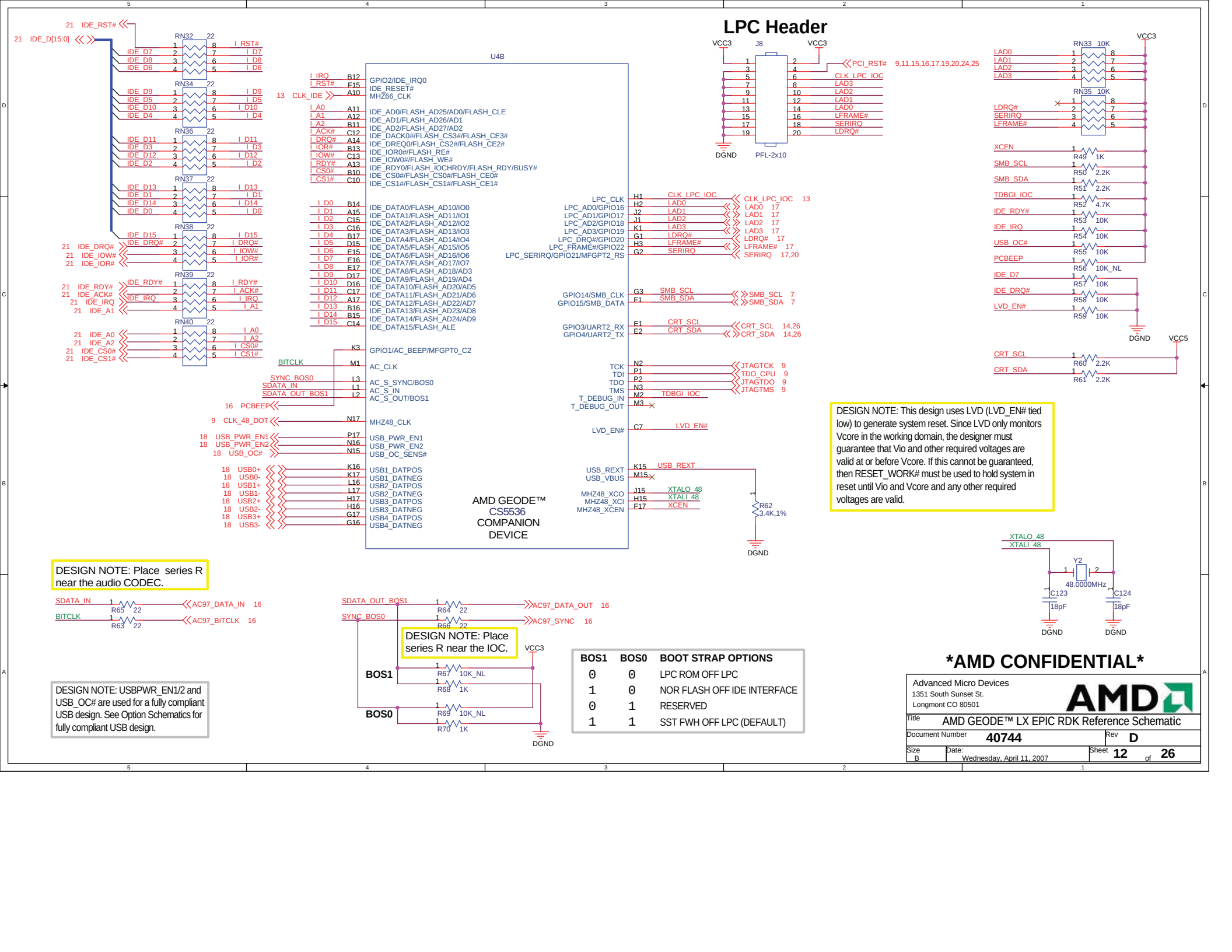


AMD CONFIDENTIAL

Advanced Micro Devices 1351 South Sunset St. Longmont CO 80501	AMD
Title	AMD GEODE™ LX EPIC RDK Reference Schematic
Document Number 40744	Rev D
Size B	Date: Wednesday, April 11, 2007
Sheet 10 of 26	


U4A
AMD GEODE™ CS5536 COMPANION DEVICE
DESIGN NOTE: Any GPIO can be used as an IRQx or INT#x. There are significant bootloader configuration changes required if selection is different than shown. Changes are highly discouraged.
DESIGN NOTE: LED is optional.
PWR MANAGEMENT
RED
DESIGN NOTE: GPIO24/WORK_AUX is an open drain output, which requires a pullup resistor to achieve a high state. At initial standby power application the GPIO24/WORK_AUX pin defaults to GPIO24 and the GPIO24 defaults as an input. This default combination will leave the pin in a high state due to the pullup which is normally connected to VCC3SB. This circuit works aourn that behaviour so that Save to RAM will function correctly.
SAVE TO RAM SUPPORT
INVERTER
NC7SZ08/SC70
LTST-C190EKT
PFL-2x4-2M0-SMD-S
ABS13-32.768KHz-12.5pF - T
32.768KHz
BSS138/SOT
AMD CONFIDENTIAL
Advanced Micro Devices
1351 South Sunset St.
Longmont CO 80501
AMD GEODE™ LX EPIC RDK Reference Schematic
Document Number 40744
Rev D
Size B
Date: Wednesday, April 11, 2007
Sheet 11 of 26

LPC Header


U4B
AMD GEODE™ CS5536 COMPANION DEVICE
J8
PFL-2x10
RN32
RN33 10K
RN34
RN35 10K
RN36
RN37
RN38
RN39
RN40
DESIGN NOTE: This design uses LVD (LVD_EN# tied low) to generate system reset. Since LVD only monitors Vcore in the working domain, the designer must guarantee that Vio and other required voltages are valid at or before Vcore. If this cannot be guaranteed, then RESET_WORK# must be used to hold system in reset until Vio and Vcore and any other required voltages are valid.
DESIGN NOTE: Place series R near the audio CODEC.
DESIGN NOTE: Place series R near the IOC.
DESIGN NOTE: USBPWR_EN1/2 and USB_OC# are used for a fully compliant USB design. See Option Schematics for fully compliant USB design.
BOS1 BOS0 BOOT STRAP OPTIONS
0 0 LPC ROM OFF LPC
1 0 NOR FLASH OFF IDE INTERFACE
0 1 RESERVED
1 1 SST FWH OFF LPC (DEFAULT)
AMD CONFIDENTIAL
Advanced Micro Devices
1351 South Sunset St.
Longmont CO 80501
Title AMD GEODE™ LX EPIC RDK Reference Schematic
Document Number 40744
Rev D
Size B
Date: Wednesday, April 11, 2007
Sheet 12 of 26

DESIGN NOTE: Without UL approval of the internal VBAT circuity, a 47 ohm resistor (R1) is required. UL approval is in process and is expected. With UL approval R1 can be removed.

DESIGN NOTE: If this schematic is used for future designs, R72 should be replaced with a 220_2A ferrite bead.

J1	
1-2	Normal
2-3	Clear CMOS

R1 R71 47 J9 J1 PFL-1x3 BT1 VBH2032-1 R73 1K C127 100nF DGND

VBAT VCORE R72 4.7R VCORESB VCC3SB C128 22uF C129 10nF C130 10nF C131 1uF C132 100nF DGND

U4C

AMD GEODE™ CS5536 COMPANION DEVICE

VBAT VCORE_VSB VIO_VSB VDDC_USB1 VDDC_USB0 VCORE VDDIO_USB0 VDDIO_USB1 VDDIO_USB2 VDDIO_USB3 VIO VSSIO_USB0 VSSIO_USB1 VSSIO_USB2 VSS NC

VCC3USB VCC3 FB4 HI1206N101R-00 C143 22uF C144 10nF C145 10nF C146 100pF DGND

VCC3 C125 22uF C126 22uF C133 10nF C134 10nF C135 10nF C136 10nF C137 10nF C138 100pF C139 100pF C140 100pF C141 100pF C142 100pF

VCORE C147 22uF C148 22uF C149 10nF C150 10nF C151 10nF C152 10nF C154 100pF C155 100pF C156 100pF DGND

VCC3SB VBAT 330_NL R213 D17 BAS40_NL VCC5 330_NL R214 D19 BAS40_NL D18 BAS40_NL R215 1K_NL C222 220M_NL DGND

VCC3 C157 22uF C158 100nF C159 100nF C160 100nF C161 100nF DGND

U6 MK1491-09F

VDD VDD VDD VDD VDD VDD VDD

11 SLP_CLK# PD# SEL66/33# XTALIN XTALOUT CLKX1 CLKX2 Y3 14.31818MHz R75 10M_NL C162 18pF C163 18pF

REFCLK1 REFCLK0/SP# 48MHz 48MHz/TS# 66MHz LCLK2 LCLK1 LCLK0 PCICLK0 PCICLK1 PCICLK2 PCICLK3

14_318MHZ0 14_318MHZ1 48MHZ IDE_CLK LCLK0 LCLK1 PCI_CLK0 PCI_CLK1 PCI_CLK2 PCI_CLK3

DESIGN NOTE: Enables spread spectrum. EMI mitigation technique

R74 10K DGND

RN41 14_318MHZ0 14_318MHZ1 CLK_14_CODEC 16 CLK_14_ISA 24 CLK_14_IOC 11

IDE_CLK R23 22 CLK_IDE 12

RN42 PCI_CLK3 PCI_CLK2 PCI_CLK1 PCI_CLK0 PC_CLK 24 CLK_EXT 9 CLK_IOC 11 CLK_CPU 9

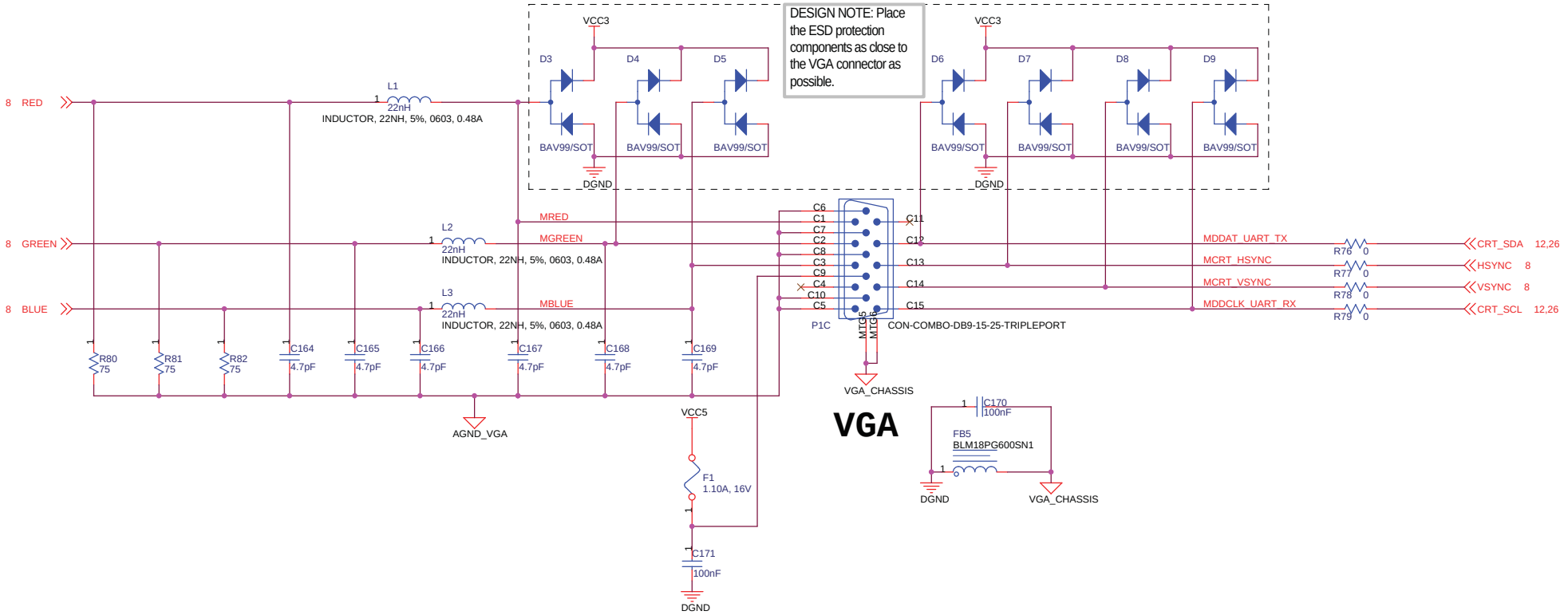
RN43 48MHZ LCLK0 LCLK1 SIO_CLK_48 17 CLK_LPC_SIO_EXT 17 CLK_LPC_IOC 12

DESIGN NOTE: Swap series resistors on the clock lines in order minimize the number of vias.

AMD CONFIDENTIAL

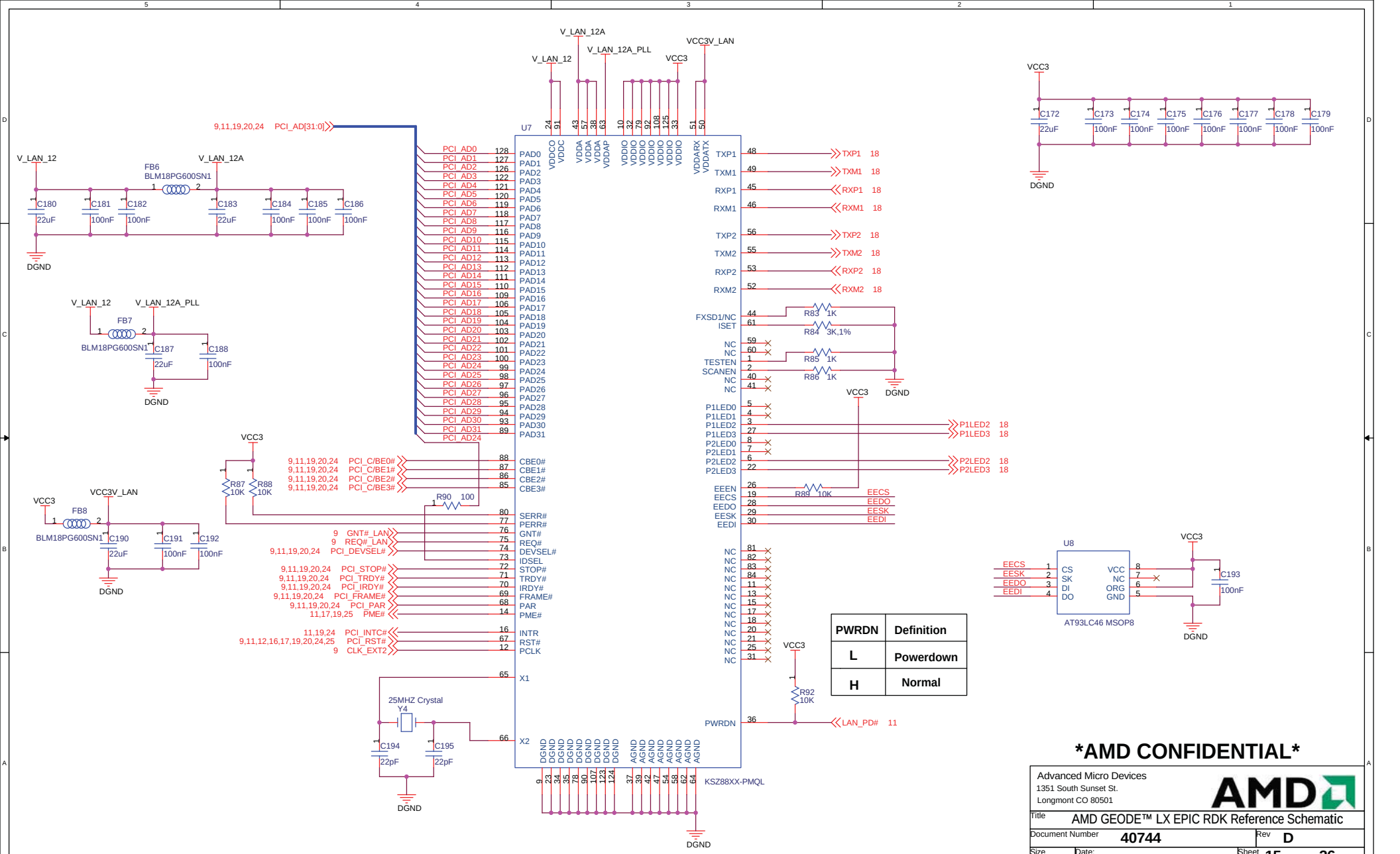
Advanced Micro Devices
1351 South Sunset St.
Longmont CO 80501

Title	AMD GEODE™ LX EPIC RDK Reference Schematic
Document Number	40744
Rev	D
Size	B
Date:	Wednesday, April 11, 2007
Sheet	13 of 26



AMD CONFIDENTIAL

Advanced Micro Devices 1351 South Sunset St. Longmont CO 80501		AMD
Title	AMD GEODE™ LX EPIC RDK Reference Schematic	
Document Number 40744		Rev D
Size B	Date: Wednesday, April 11, 2007	Sheet 14 of 26

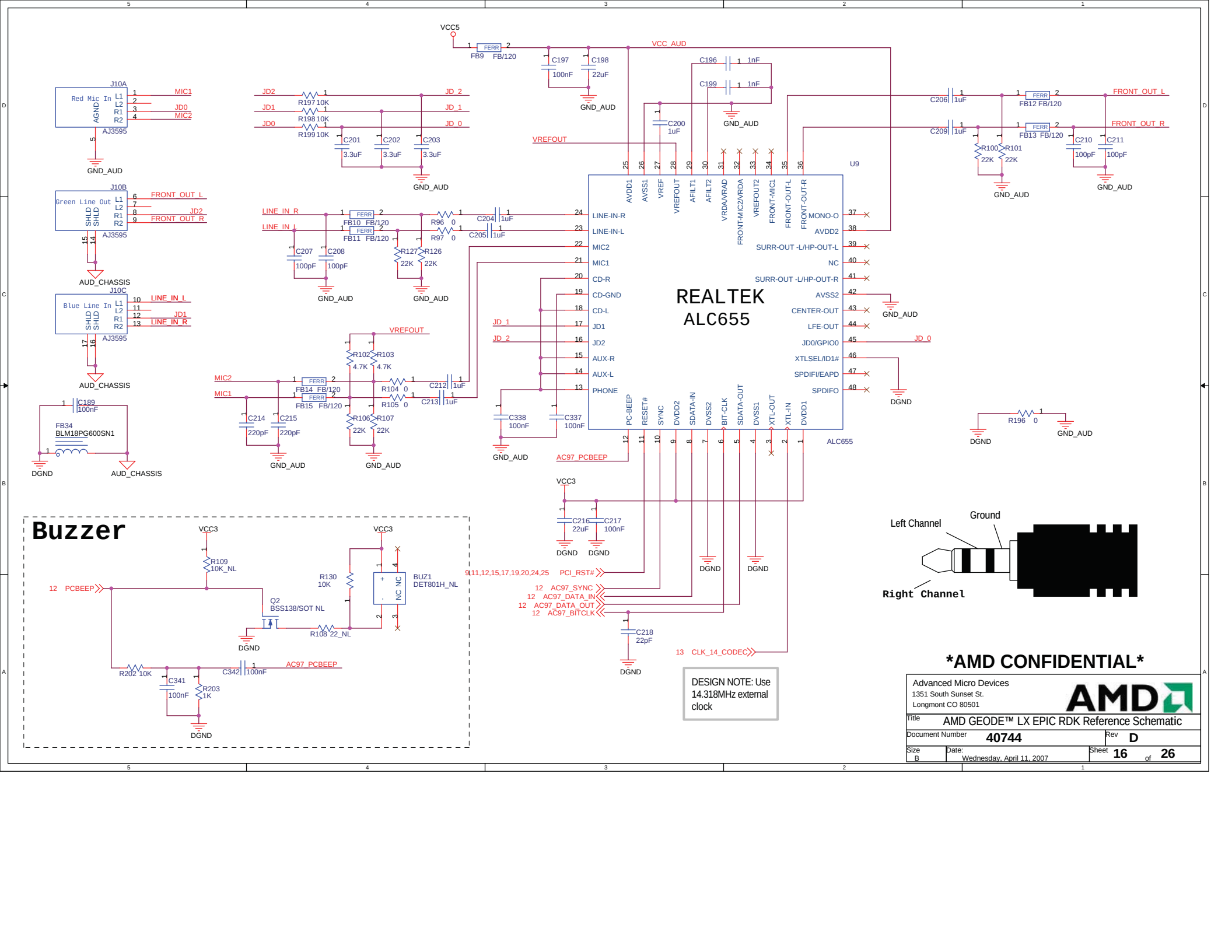


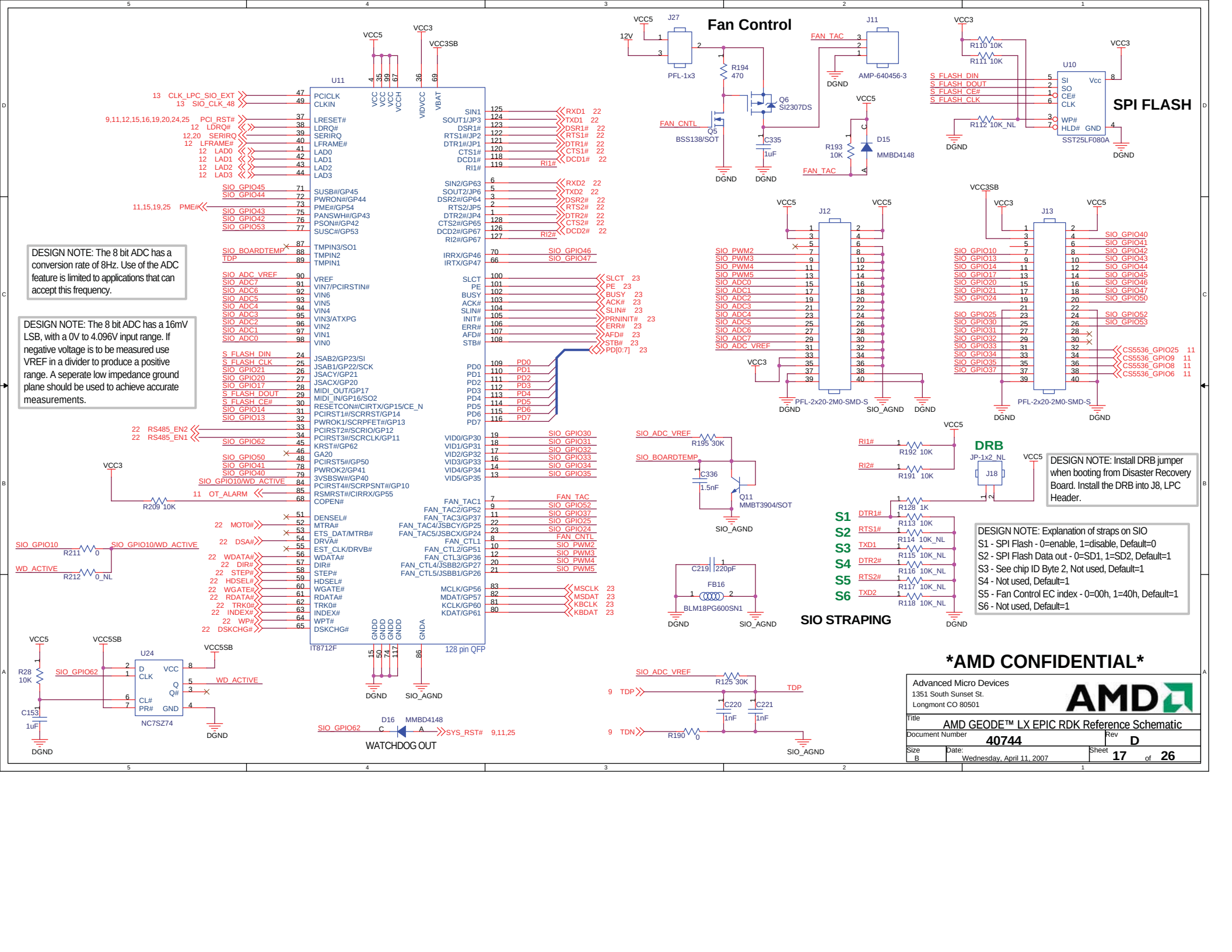
PWRDN	Definition
L	Powerdown
H	Normal

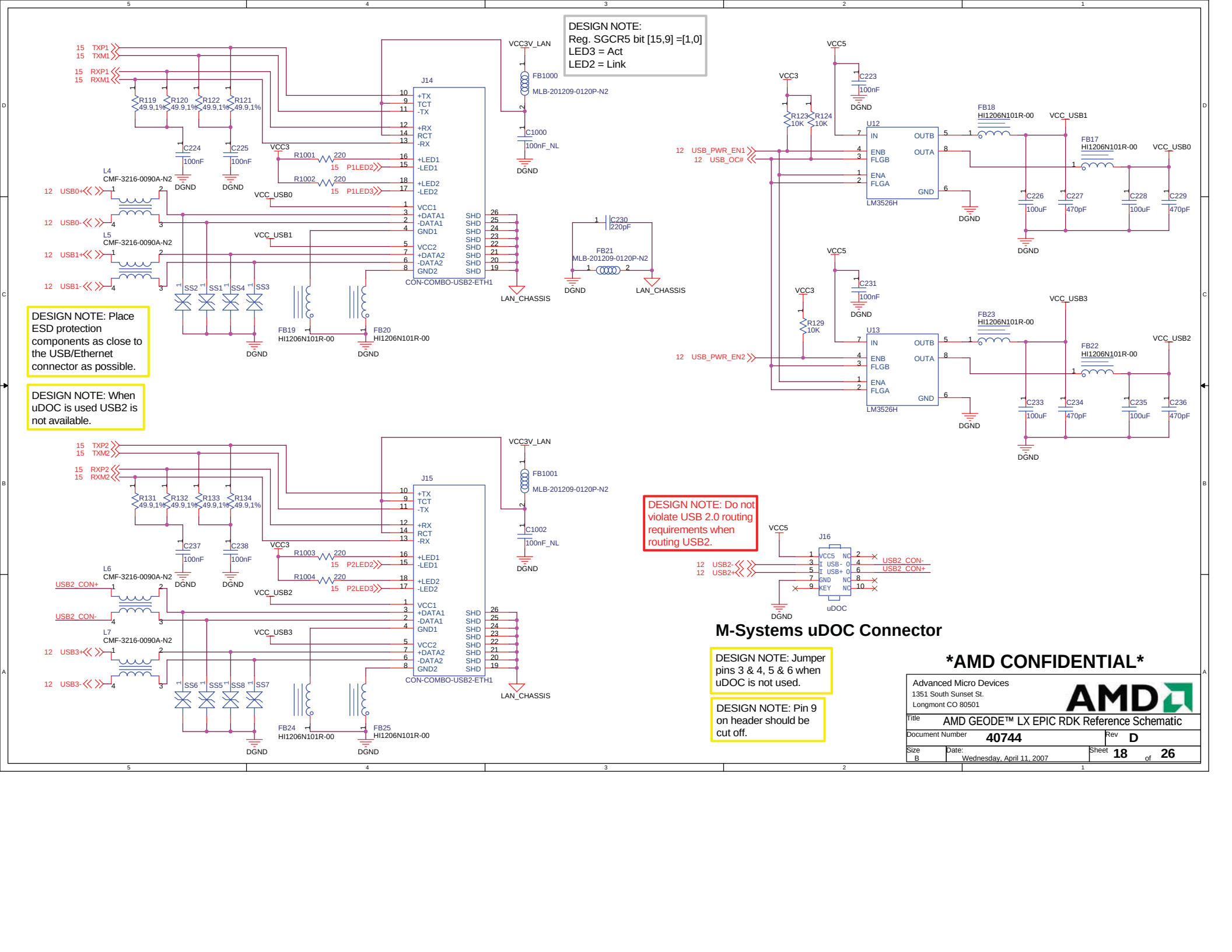
AMD CONFIDENTIAL

Advanced Micro Devices
1351 South Sunset St.
Longmont CO 80501

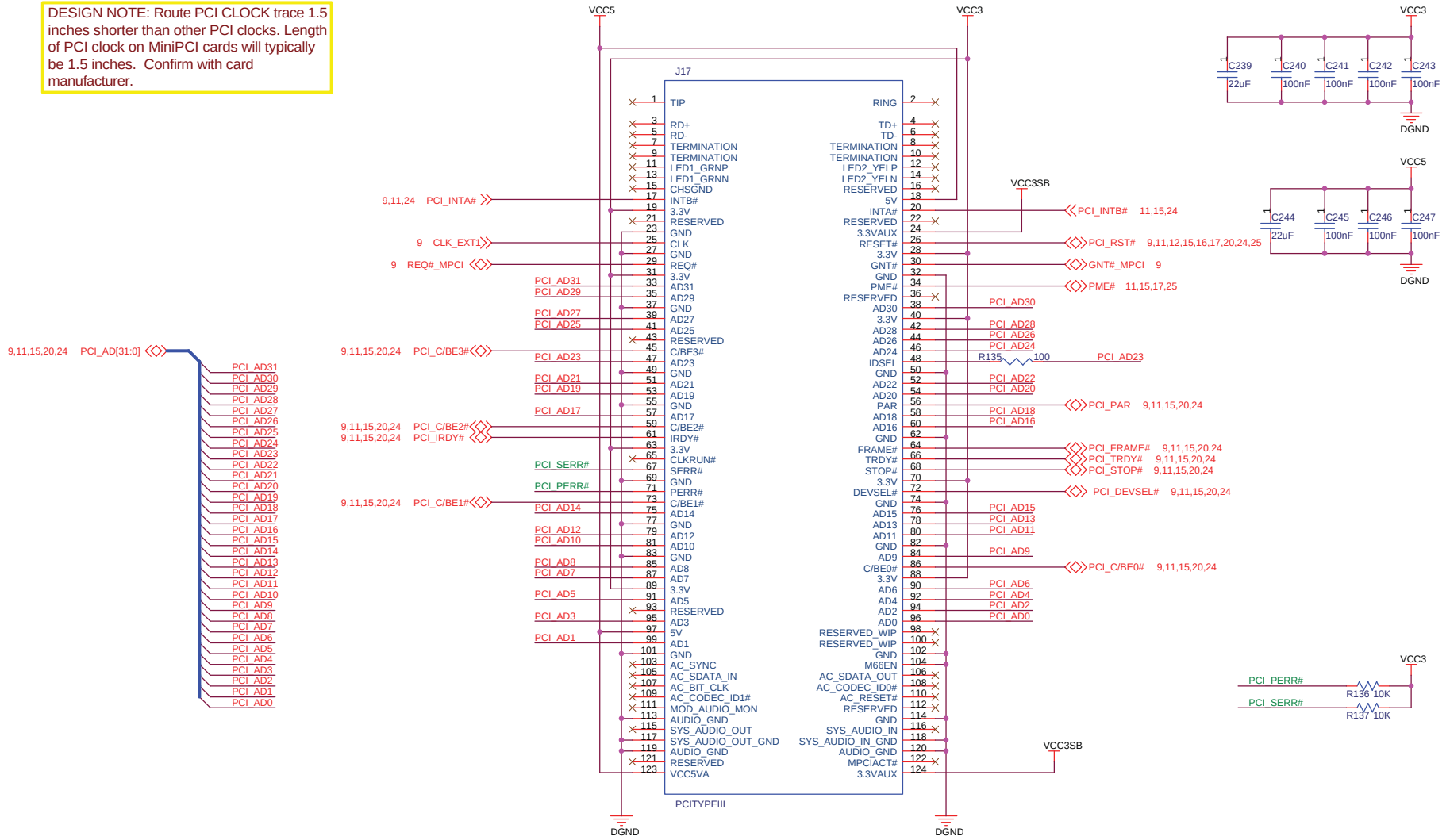
Title	AMD GEODE™ LX EPIC RDK Reference Schematic
Document Number	40744
Rev	D
Size	B
Date:	Wednesday, April 11, 2007
Sheet	15 of 26


REALTEK
ALC655
ALC655
U9
Buzzer
Left Channel
Ground
Right Channel
DESIGN NOTE: Use 14.318MHz external clock
AMD CONFIDENTIAL
Advanced Micro Devices
1351 South Sunset St.
Longmont CO 80501
AMD
Title
AMD GEODE™ LX EPIC RDK Reference Schematic
Document Number
40744
Rev
D
Size
B
Date:
Wednesday, April 11, 2007
Sheet
16
of
26


Fan Control
SPI FLASH
SST25LF080A
PFL-1x3
AMP-640456-3
BSS138/SOT
SI2307DS
MMBD4148
PFL-2x20-2M0-SMD-S
DRB
JP-1x2_NL
SIO STRAPING
S1 DTR1# 1
S2 RTS1# 1
S3 TXD1 1
S4 DTR2# 1
S5 RTS2# 1
S6 TXD2 1
DESIGN NOTE: Explanation of straps on SIO
S1 - SPI Flash - 0=enable, 1=disable, Default=0
S2 - SPI Flash Data out - 0=SD1, 1=SD2, Default=1
S3 - See chip ID Byte 2, Not used, Default=1
S4 - Not used, Default=1
S5 - Fan Control EC index - 0=00h, 1=40h, Default=1
S6 - Not used, Default=1
DESIGN NOTE: The 8 bit ADC has a conversion rate of 8Hz. Use of the ADC feature is limited to applications that can accept this frequency.
DESIGN NOTE: The 8 bit ADC has a 16mV LSB, with a 0V to 4.096V input range. If negative voltage is to be measured use VREF in a divider to produce a positive range. A seperate low impedance ground plane should be used to achieve accurate measurements.
DESIGN NOTE: Install DRB jumper when booting from Disaster Recovery Board. Install the DRB into J8, LPC Header.
U11
IT8712F
128 pin QFP
U24
NC7SZ74
WATCHDOG OUT
AMD CONFIDENTIAL
Advanced Micro Devices
1351 South Sunset St.
Longmont CO 80501
AMD GEODE™ LX EPIC RDK Reference Schematic
Document Number 40744
Rev D
Size B
Date: Wednesday, April 11, 2007
Sheet 17 of 26


DESIGN NOTE:
Reg. SGCR5 bit [15,9] =[1,0]
LED3 = Act
LED2 = Link
DESIGN NOTE: Place ESD protection components as close to the USB/Ethernet connector as possible.
DESIGN NOTE: When uDOC is used USB2 is not available.
DESIGN NOTE: Do not violate USB 2.0 routing requirements when routing USB2.
DESIGN NOTE: Jumper pins 3 & 4, 5 & 6 when uDOC is not used.
DESIGN NOTE: Pin 9 on header should be cut off.
M-Systems uDOC Connector
AMD CONFIDENTIAL
Advanced Micro Devices
1351 South Sunset St.
Longmont CO 80501
AMD
Title
AMD GEODE™ LX EPIC RDK Reference Schematic
Document Number
40744
Rev
D
Size
B
Date:
Wednesday, April 11, 2007
Sheet
18
of
26

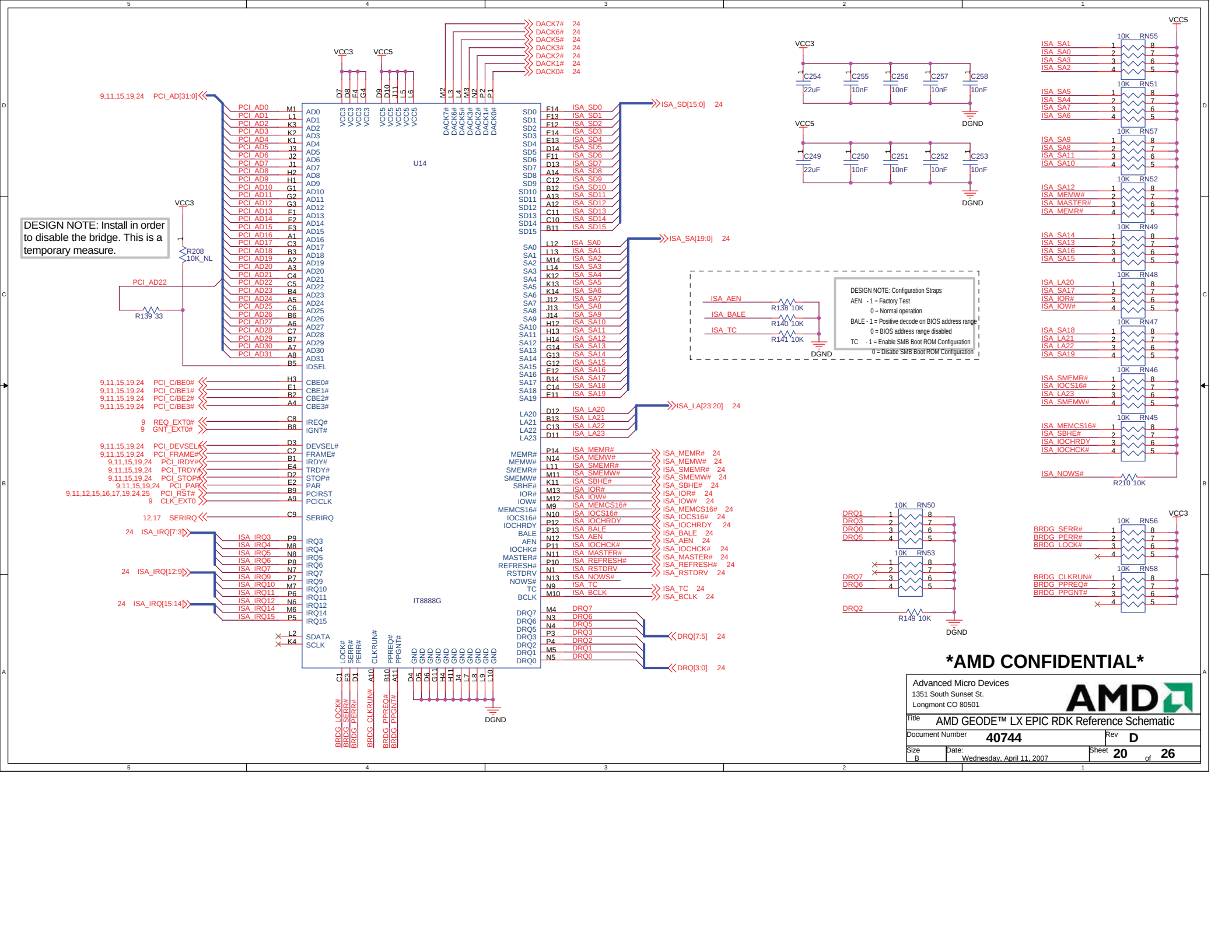
DESIGN NOTE: Route PCI CLOCK trace 1.5 inches shorter than other PCI clocks. Length of PCI clock on MiniPCI cards will typically be 1.5 inches. Confirm with card manufacturer.



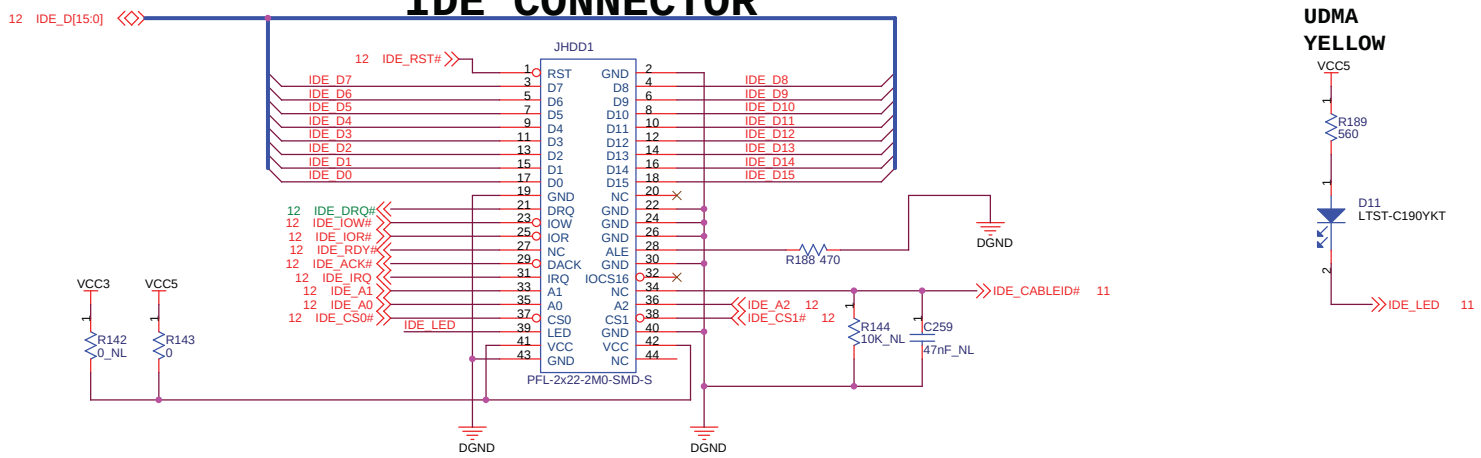
DESIGN NOTE: Consult MiniPCI card manufacturer for any special design or layout considerations of MiniPCI slot to accomidate a particular MiniPCI card.

AMD CONFIDENTIAL

Advanced Micro Devices 1351 South Sunset St. Longmont CO 80501	AMD
Title: AMD GEODE™ LX EPIC RDK Reference Schematic	
Document Number: 40744	Rev: D
Size: B	Date: Wednesday, April 11, 2007
Sheet 19 of 26	


DESIGN NOTE: Install in order to disable the bridge. This is a temporary measure.
DESIGN NOTE: Configuration Straps
AEN - 1 = Factory Test
0 = Normal operation
BALE - 1 = Positive decode on BIOS address range
0 = BIOS address range disabled
TC - 1 = Enable SMB Boot ROM Configuration
0 = Disabe SMB Boot ROM Configuration
U14
IT8888G
AMD CONFIDENTIAL
Advanced Micro Devices
1351 South Sunset St.
Longmont CO 80501
AMD GEODE™ LX EPIC RDK Reference Schematic
Document Number 40744
Rev D
Size B
Date: Wednesday, April 11, 2007
Sheet 20 of 26

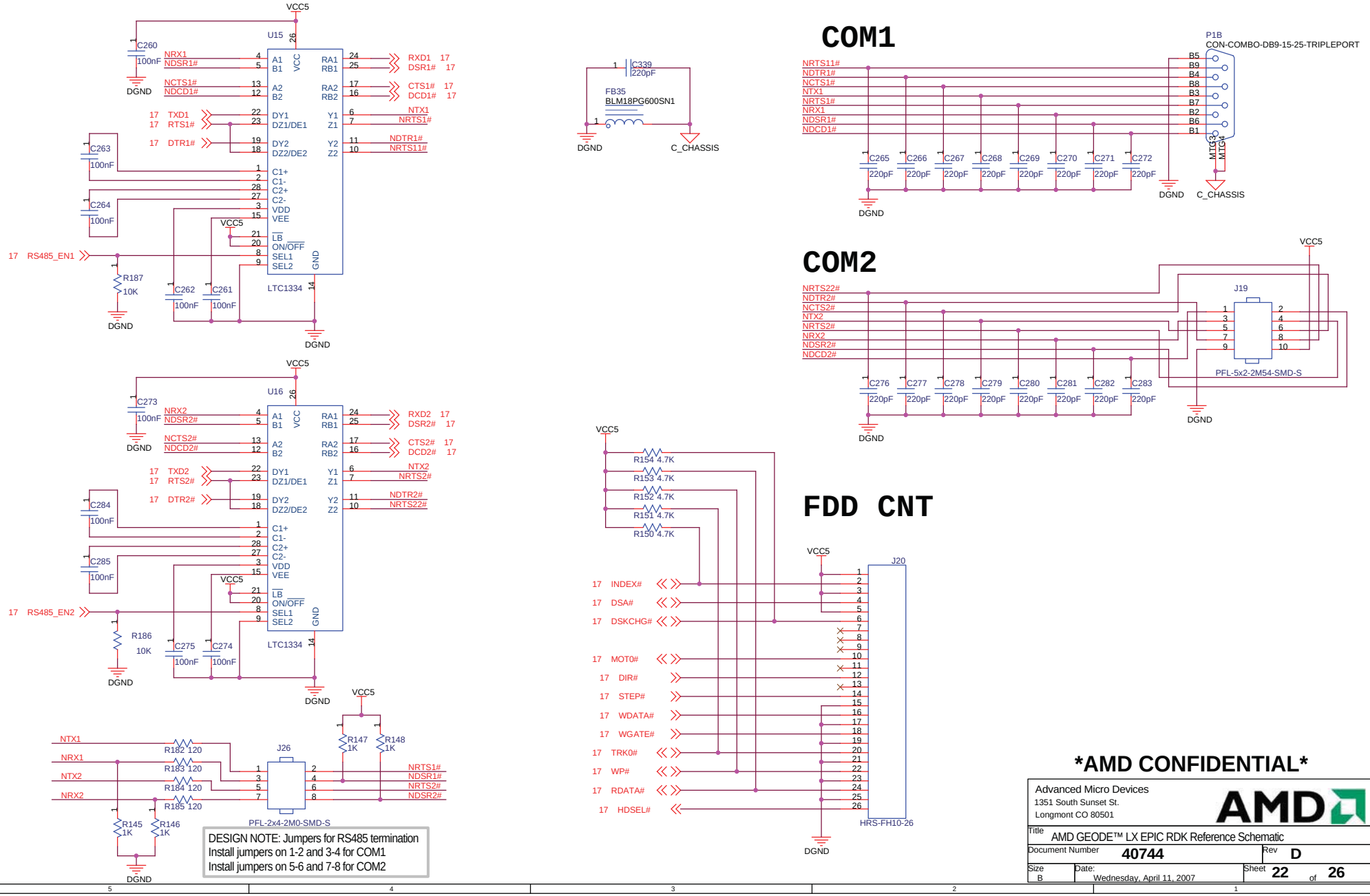
IDE CONNECTOR



UDMA YELLOW

AMD CONFIDENTIAL

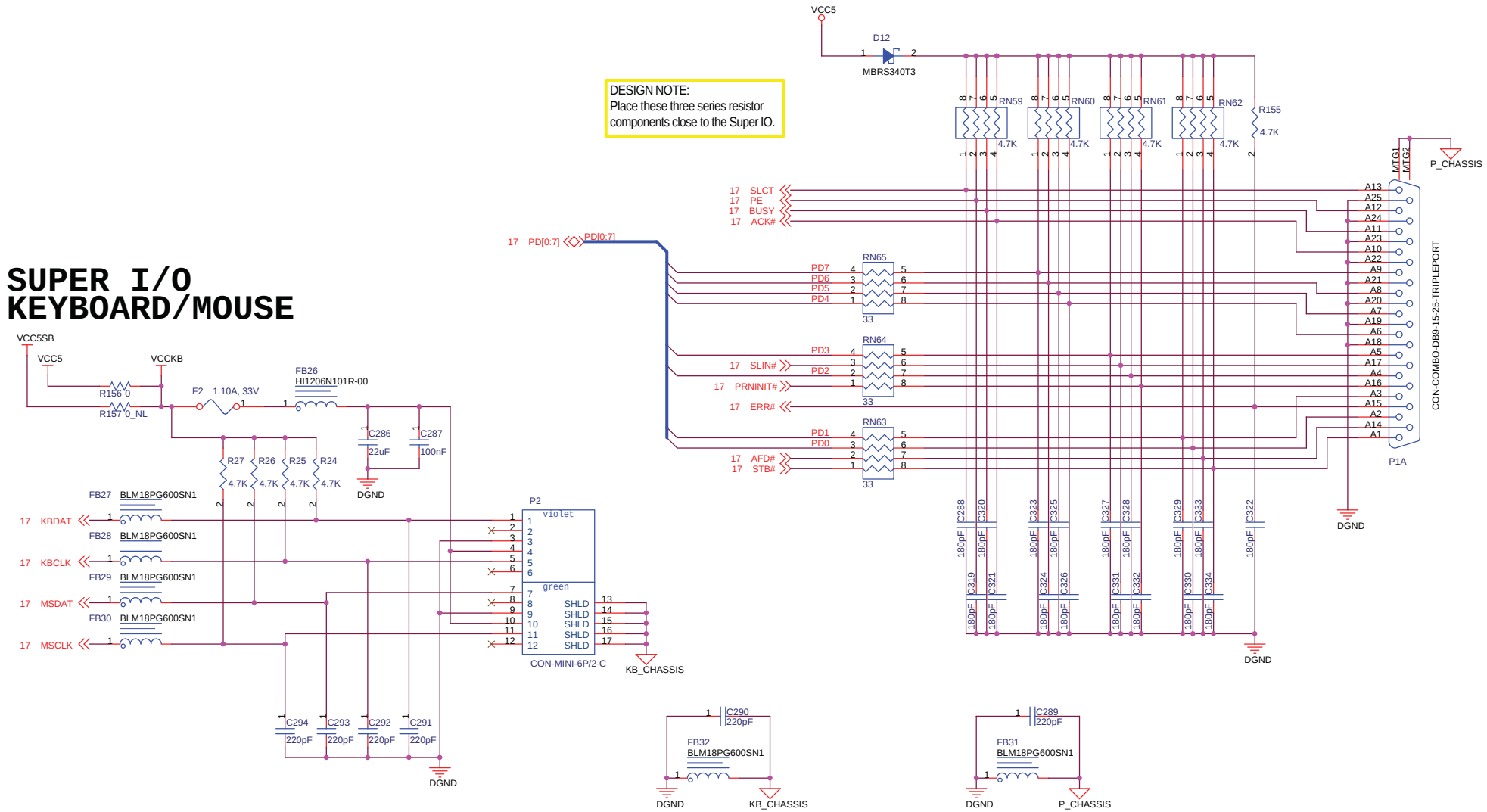
Advanced Micro Devices 1351 South Sunset St. Longmont CO 80501			
Title	AMD GEODE™ LX EPIC RDK Reference Schematic		
Document Number	40744	Rev	D
Size B	Date: Wednesday, April 11, 2007	Sheet	21 of 26



AMD CONFIDENTIAL

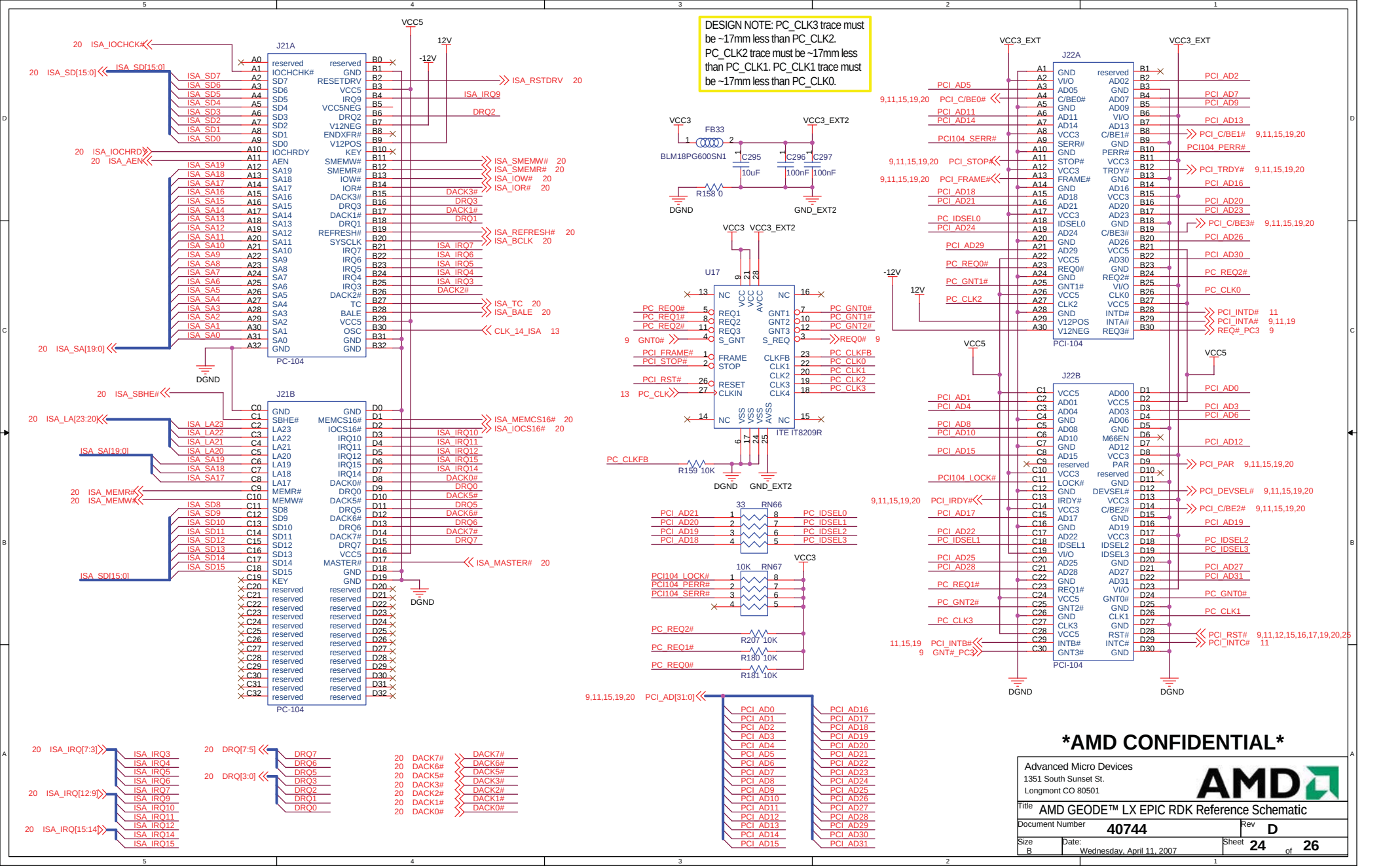
Advanced Micro Devices 1351 South Sunset St. Longmont CO 80501	AMD
Title: AMD GEODE™ LX EPIC RDK Reference Schematic	
Document Number: 40744	Rev: D
Size: B	Date: Wednesday, April 11, 2007
Sheet: 22 of 26	

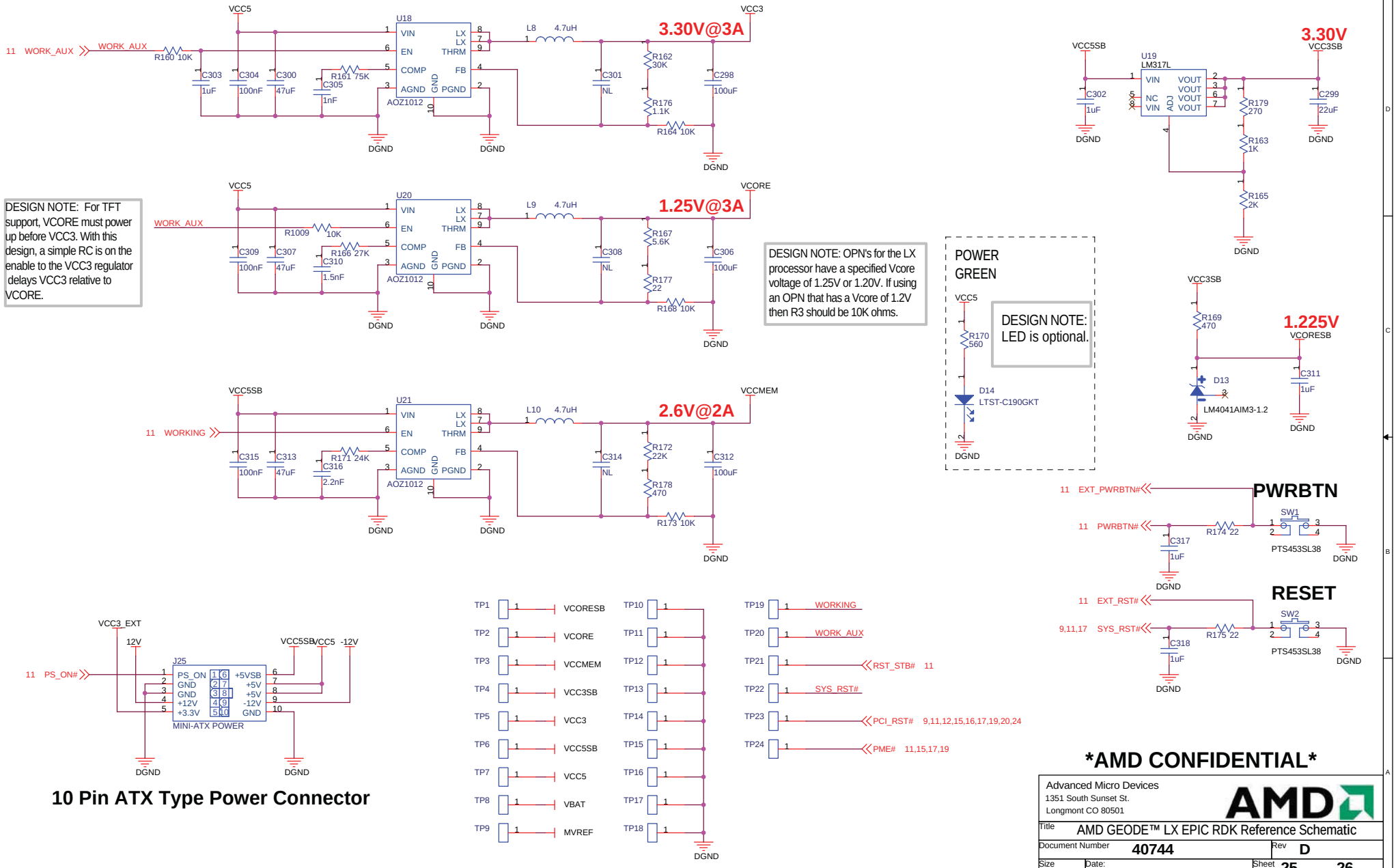
SUPER I/O KEYBOARD/MOUSE



AMD CONFIDENTIAL

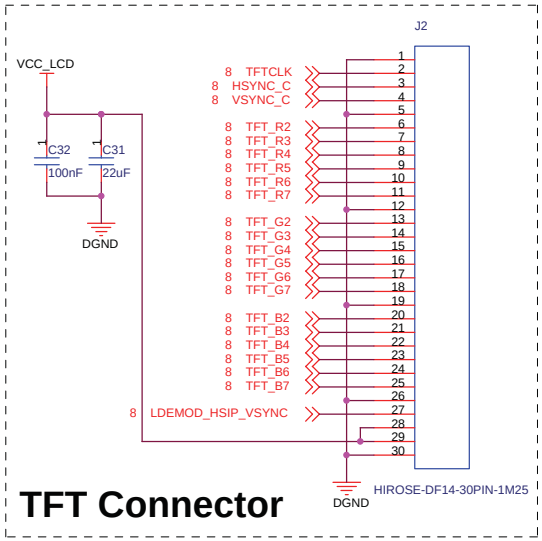
Advanced Micro Devices 1351 South Sunset St. Longmont CO 80501		AMD
Title: AMD GEODE™ LX EPIC RDK Reference Schematic		
Document Number: 40744		Rev: D
Size: B	Date: Wednesday, April 11, 2007	Sheet 23 of 26

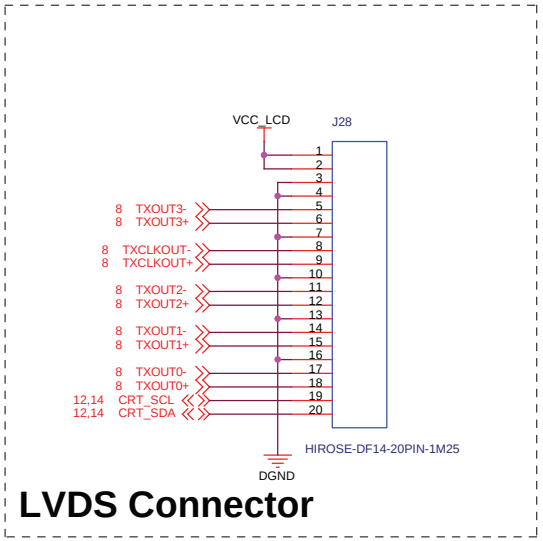

DESIGN NOTE: PC_CLK3 trace must be ~17mm less than PC_CLK2. PC_CLK2 trace must be ~17mm less than PC_CLK1. PC_CLK1 trace must be ~17mm less than PC_CLK0.
J21A
J21B
PC-104
U17
ITE IT8209R
FB33
BLM18PG600SN1
J22A
J22B
PCI-104
RN66
RN67
AMD CONFIDENTIAL
Advanced Micro Devices
1351 South Sunset St.
Longmont CO 80501
AMD GEODE™ LX EPIC RDK Reference Schematic
Document Number 40744
Rev D
Size B
Date: Wednesday, April 11, 2007
Sheet 24 of 26

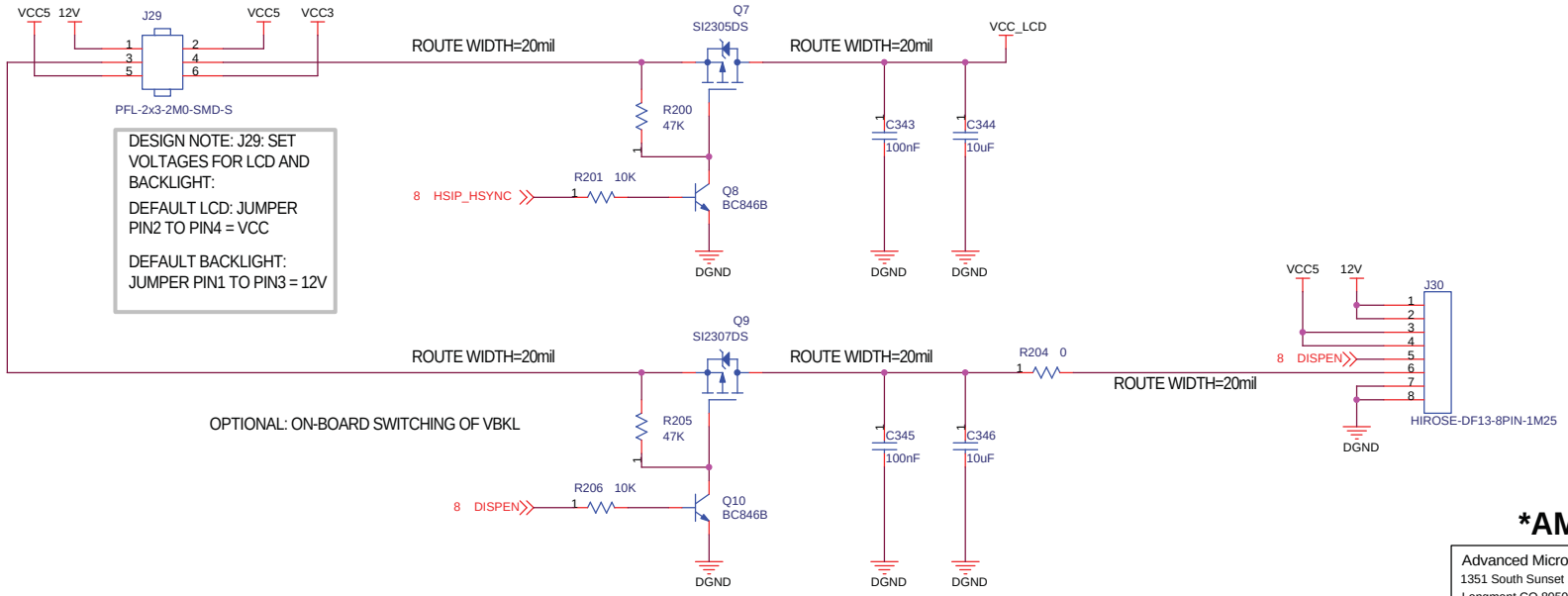


AMD CONFIDENTIAL

Advanced Micro Devices 1351 South Sunset St. Longmont CO 80501	AMD
Title	AMD GEODE™ LX EPIC RDK Reference Schematic
Document Number 40744	Rev D
Size B	Date: Wednesday, April 11, 2007
Sheet 25 of 26	







AMD CONFIDENTIAL

Advanced Micro Devices 1351 South Sunset St. Longmont CO 80501		AMD
Title	AMD GEODE™ LX EPIC RDK Reference Schematic	
Document Number	40744	Rev D
Size B	Date: Wednesday, April 11, 2007	Sheet 26 of 26