

Desert Eagle
LA-3161P

Compal confidential

HEL80/HEL81 Schematics Document

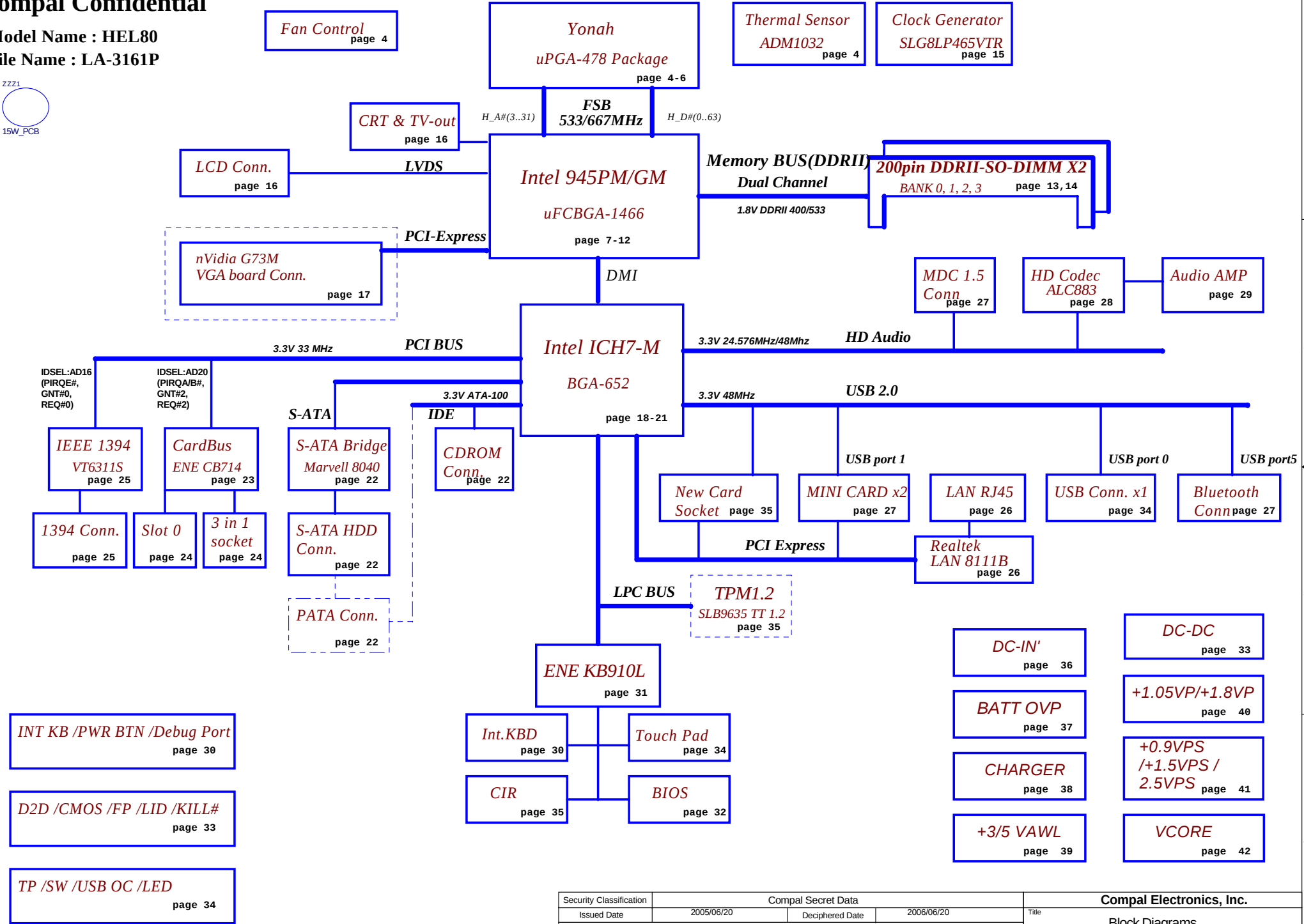
Mobile Yonah uFCPGA with Intel
Calistoga_GM/PM+ICH7-M

Thursday, February 23, 2006
REV: 0.3

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Compal Confidential

Model Name : HEL80
File Name : LA-3161P



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Voltage Rails

power plane State	+B LD03 LD05	+5VALW +3VALW	+1.8V +5V	+5VS +3VS +2.5VS +1.8VS +1.5VS +1.2VS +VGA_CORE +0.9VS +CPU_CORE +VCCP
S0	0	0	0	0
S1	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

0 MEANS ON
X MEANS OFF

S3 : STR
S4 : STD
S5 : SOFT OFF

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD20	2	PIRQA/B
1394	AD16	0	PIRQE

EC SM Bus1 address

EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 100X b
EEPROM(24C16/02)	1010 000X b		

ICH7 SM Bus address

Device	Address
Clock Generator (SLG8LP465VTR)	1101 001Xb
DDRII DIMM0	1010 000Xb
DDRII DIMM1	1010 010Xb

SKU ID Table

Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

SKU ID	HEL80/81 SKU
* 0	HEL80 SKU
1	HEL81 SKU
2	TEST MODE
3	
4	
5	
6	
7	

BOM Structure

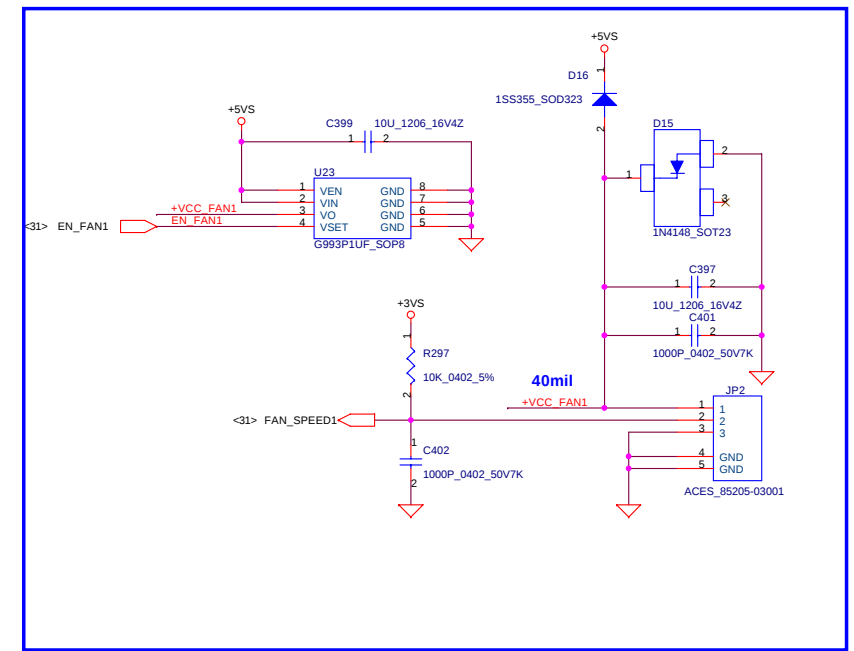
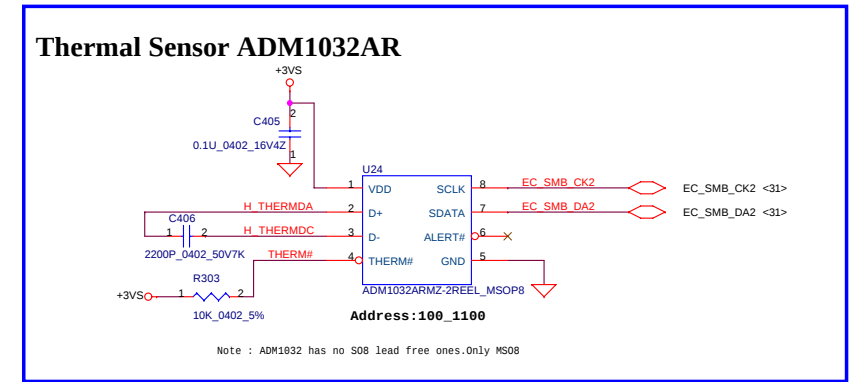
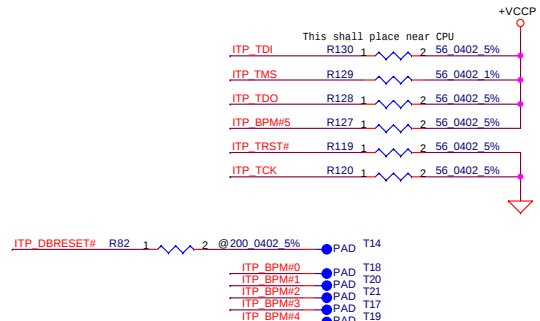
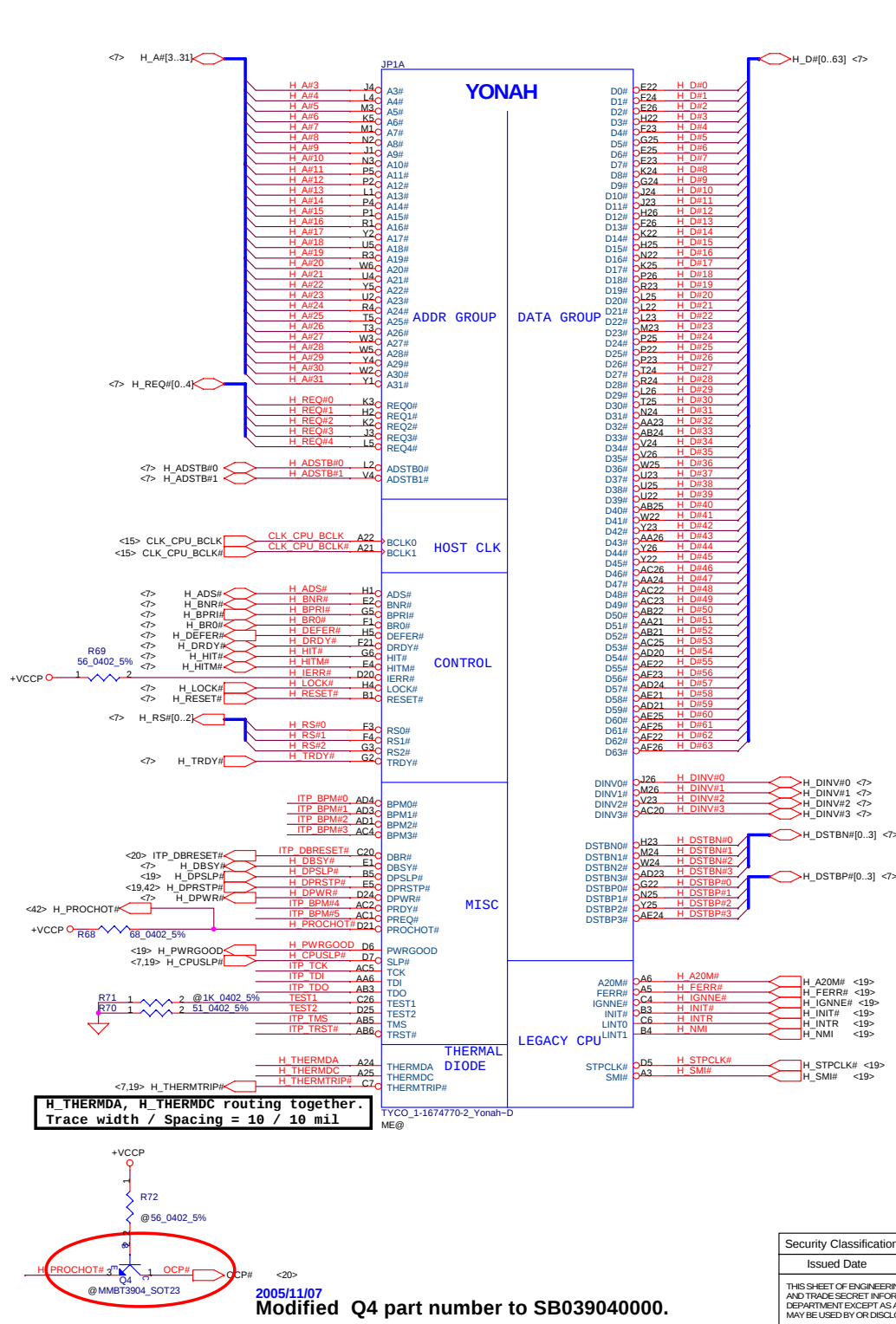
MARK	FUNCTION
@	NC FOR ALL
UMA@	Internal 945GM
VGA@	External G7xM
TPM@	TPM1.2
CIR@	CIR
1394@	1394
SATA@	SATA HDD
8040@	PATA HDD
IOMP@	IOMP
15W@	15W PANEL
APA@	HP out from AMP
HPA@	HP out from HP AMP
HP@	HP out from CODEC

USB PORT LIST

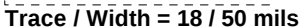
PORT	DEVICE
0	LEFT SIDE
1	BLUE TOOTH
2	RIGHT SIDE
3	CMOS
4	RIGHT SIDE
5	FINGER PRINTER
6	NEW CARD
7	TV

+3VALW	KB910L SB RTL8110SBL/CL	mA 160mA
+CPU_CORE	CPU	36A
+VCCP	CPU NB	2.5A 9.8A (14.7A)
+5VS	EXPRESS CARD HDD ODD MDC APA2066 TPA0211 AD1986 USB PORT * 6	1A 1.5A 1.8A 300mA 1A mA 70mA 3A
+3VS	NB EXPRESS CARD CLK_GEN LCDVCC VGA CARD (G7XM) SB R5C832 BIOS ROM KB910L CB1410	480mA 1A 200mA 1A 655mA 680mA mA 15mA 200mA mA
+2.5VS	VGA CARD (G7XM) NB	130mA (143mA)
+1.8V	DDR2_DIMM NB (667Mhz)	8A 3.1A
+1.8VS	GDDR2 VGA CARD (G7XM)	6A 4.06A
+0.9VREF	DDR2_DIMM	10mA
+0.9VS	GDDR2 DDR2_DIMM	1A 2A
+1.5V	SB	40mA
+1.5VS	NB SB MiniCard EXPRESS CARD VGA CARD (G7XM)	8.9A(13.8A) 3.8A 1A 0.65A 2A

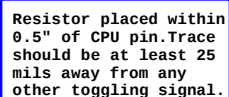
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Issued Date	2005/10/06		Deciphered Date	2006/10/06		Title Notes List
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Date:		Thursday, February 23, 2006		Sheet	3	of 43



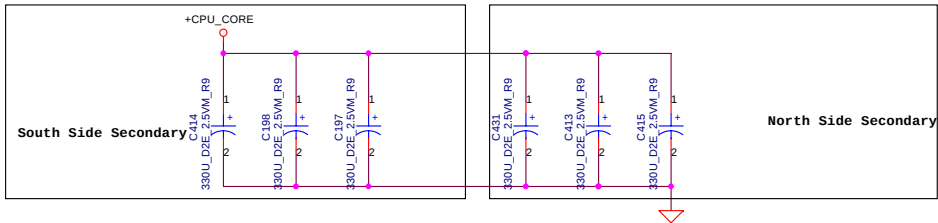
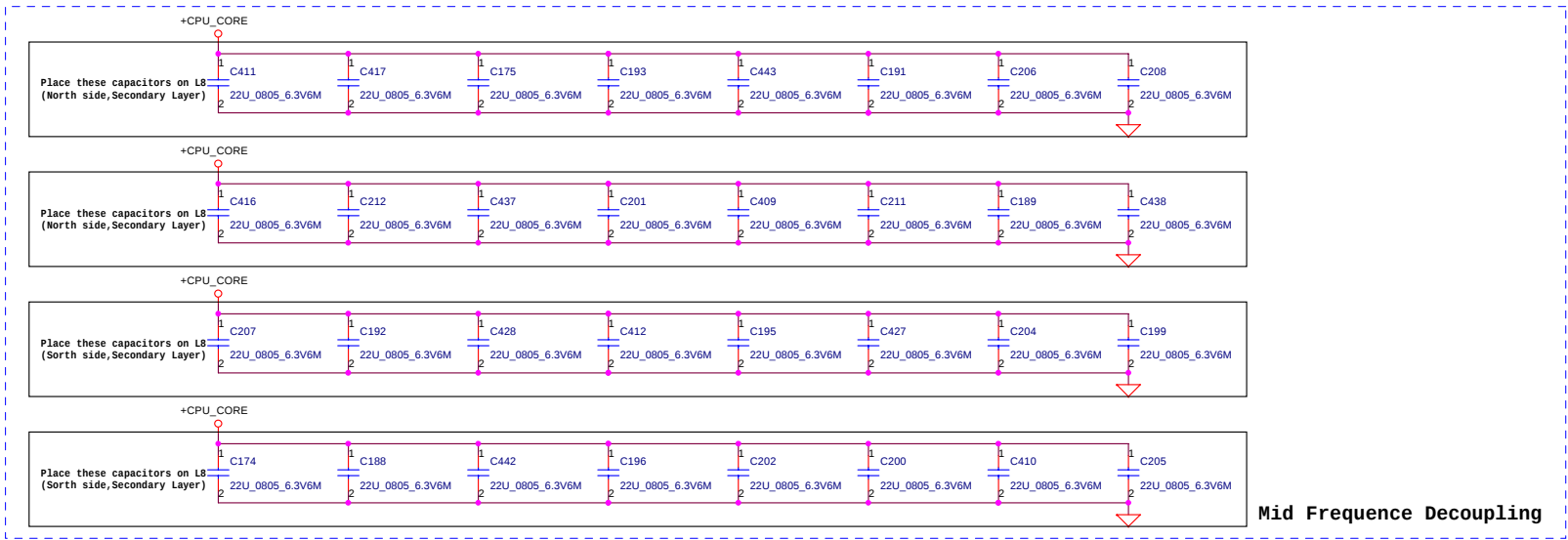
Security Classification		Compal Secret Data		Title	
Issued Date	2005/10/06	Deciphered Date	2006/10/06	Yonah CPU in mFCPGA479	
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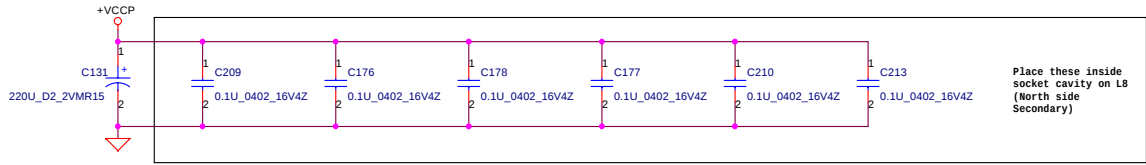
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1



COMP 0/2Trace / Width = 18 / 25 mils
COMP 1/3Trace / Width = 5 / 25 mils



ESR <= 1.5m ohm
Capacitor > 1980uF



U22

FM

VCA

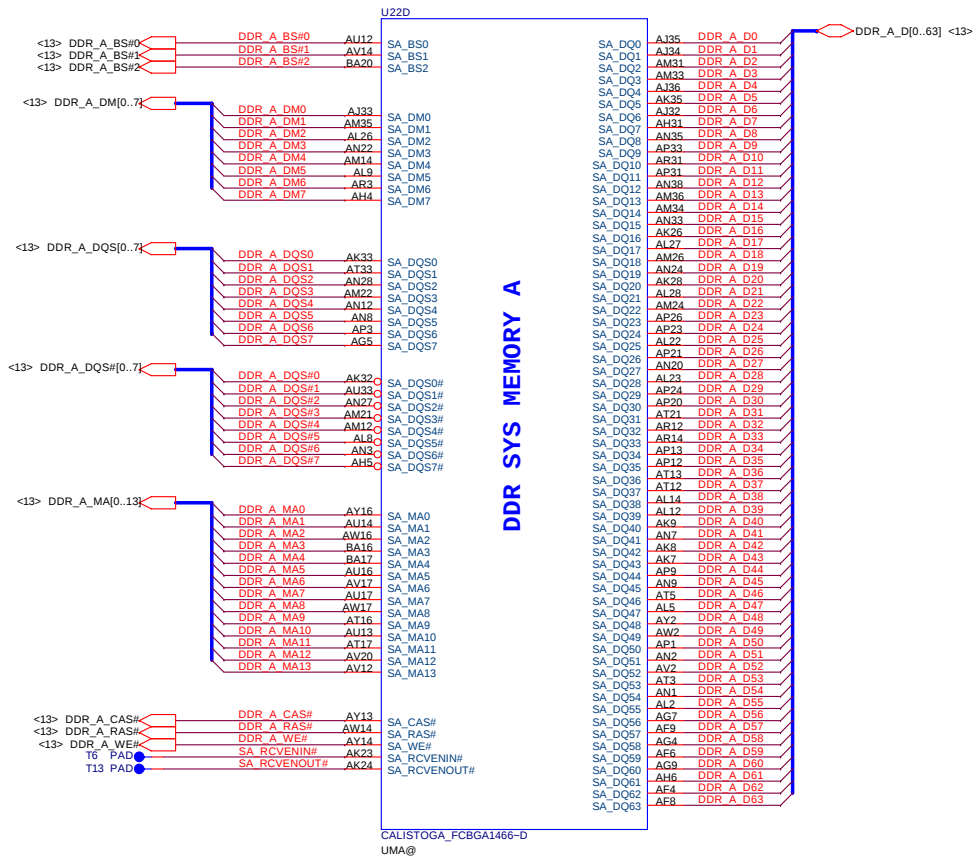
CEG

NC

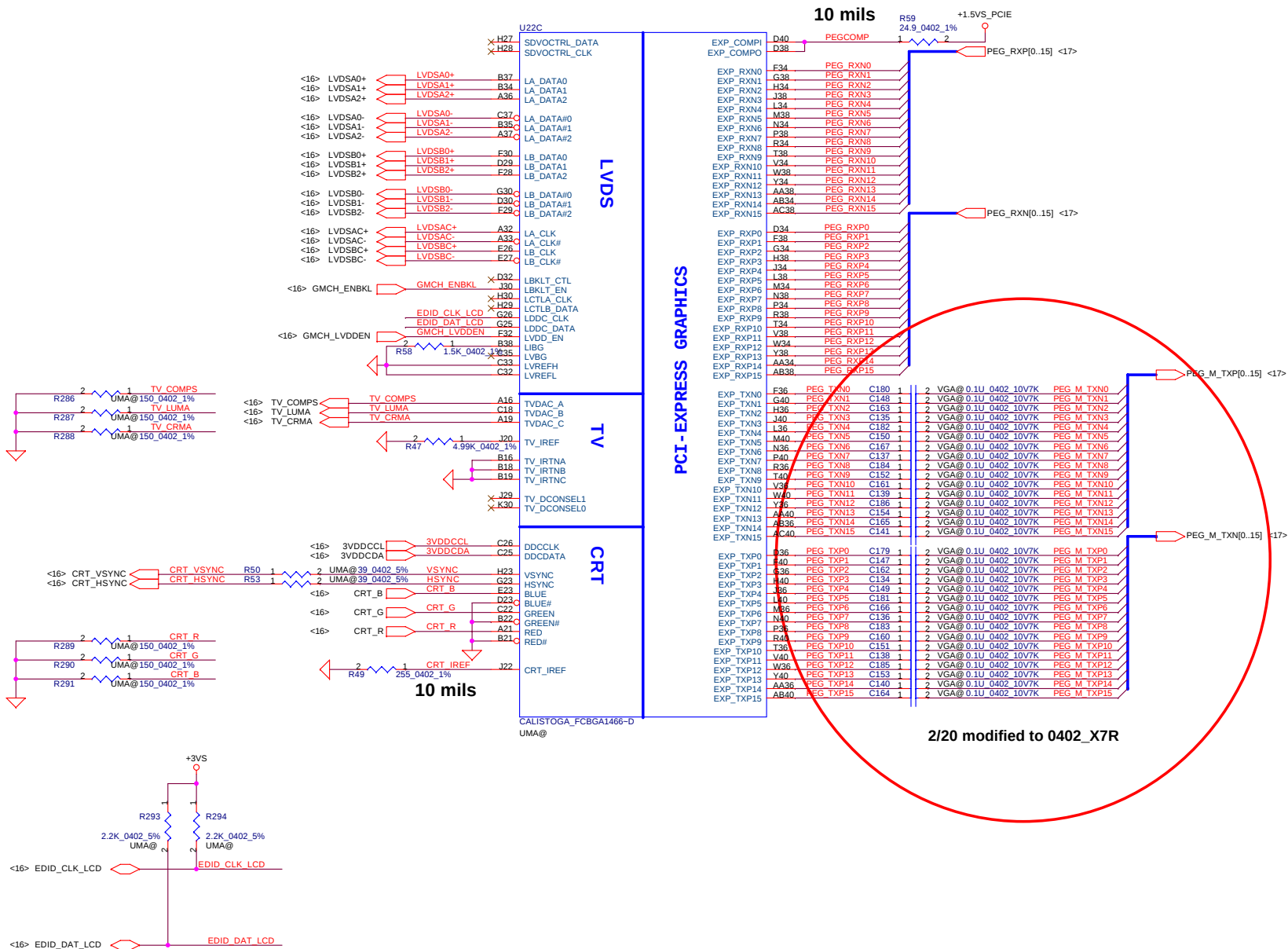
RESERVED

Layout Note:
+DDR_MCH_REF
trace width and
spacing is 20/20.

nexainf@hotmail.com

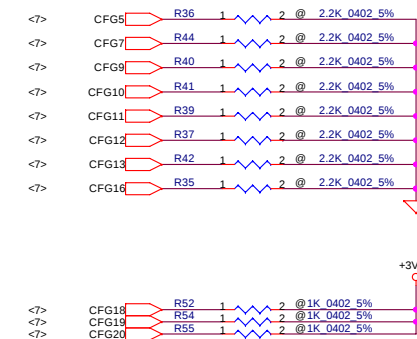
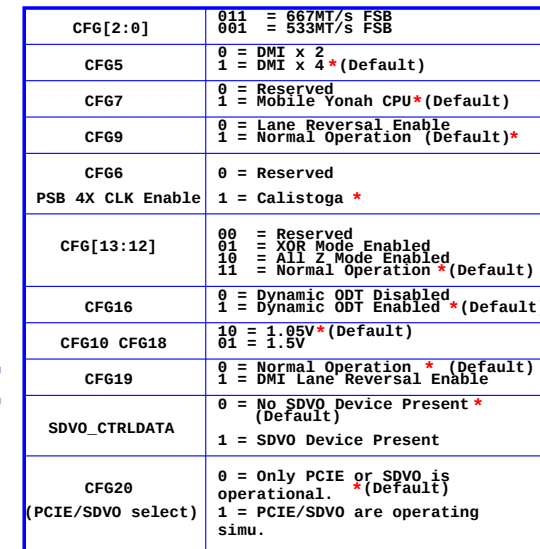


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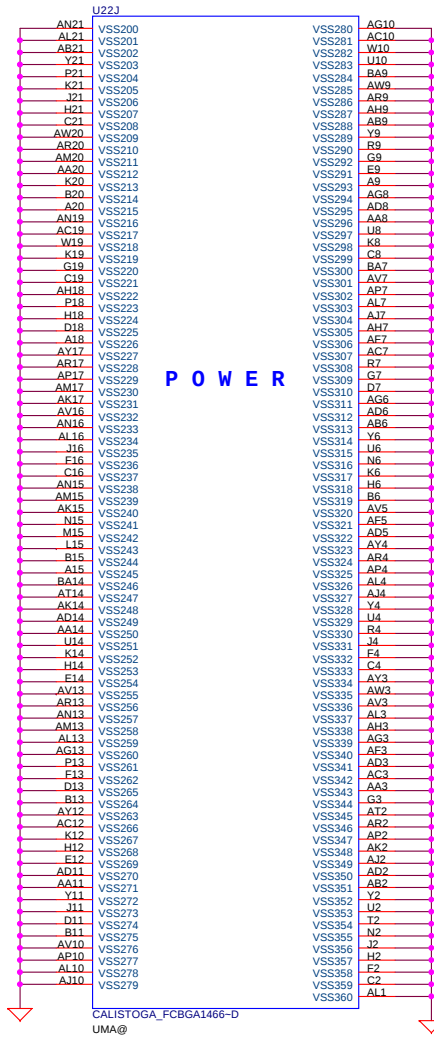
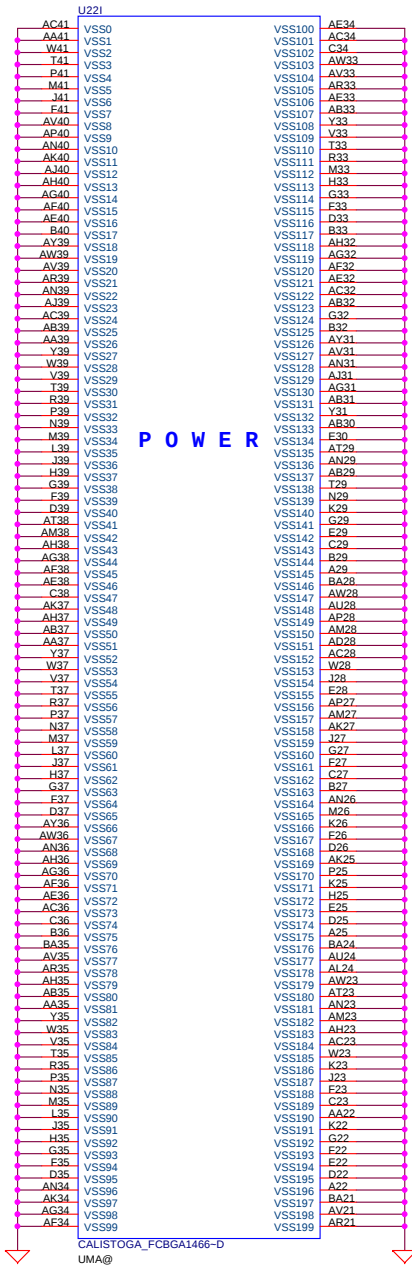


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CFG[3:17] have internal pull up
CFG[19:18] have internal pull down



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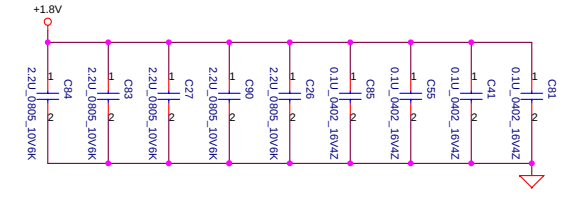


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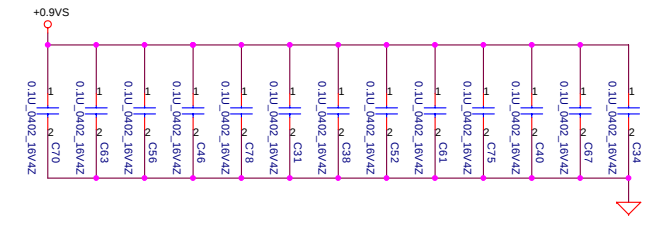
 DDR_A_DQS#[0..7]
 DDR_A_D[0..63]
 DDR_A_DM[0..7]
 DDR_A_DQS[0..7]
 DDR_A_MA[0..13]

Layout Note:
Place near JP41

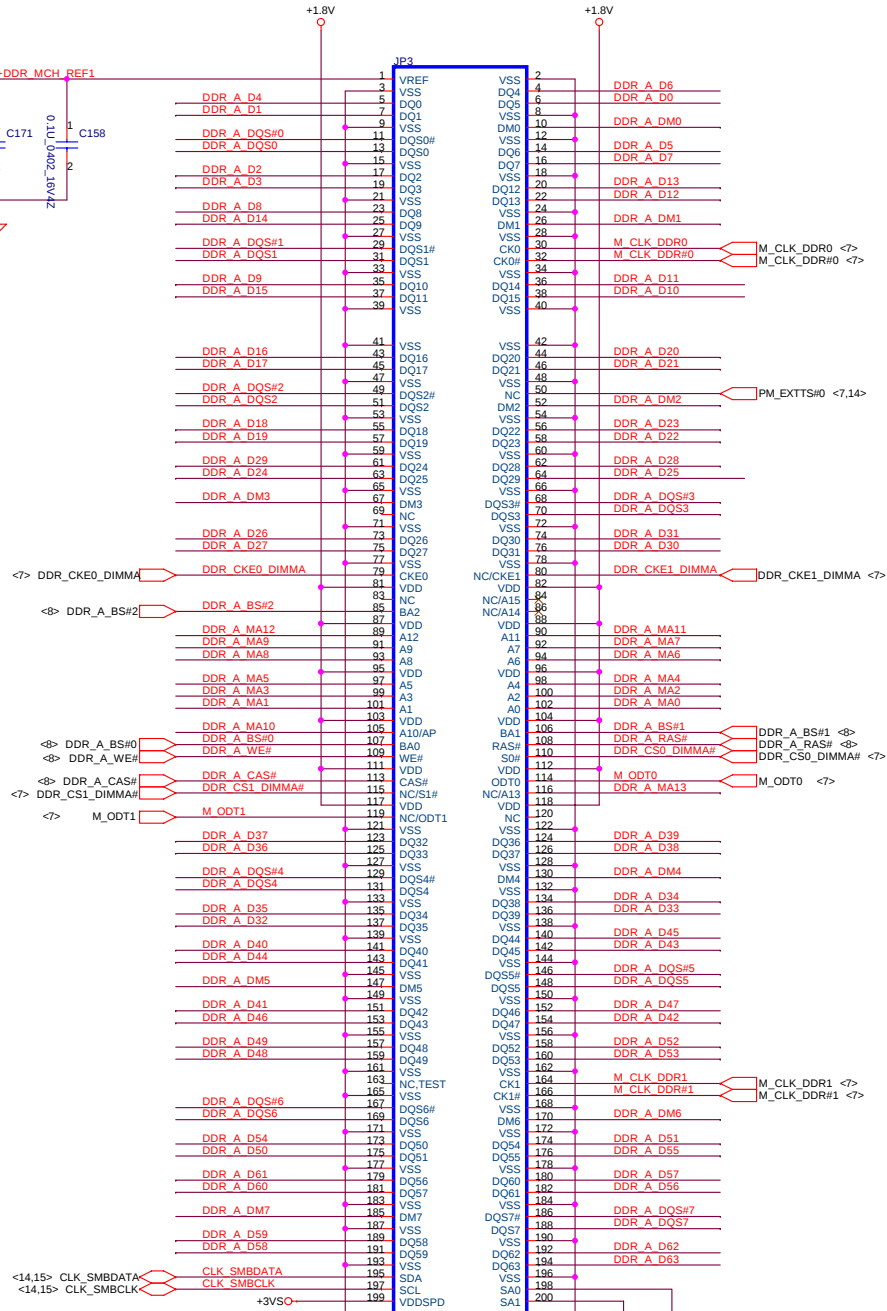
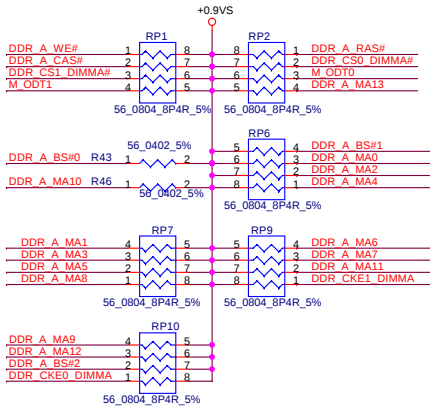
Layout Note:
+DDR_MCH_REF
trace width and
spacing is 20/20.



Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS



Layout Note:
Place these resistor
closely JP41,all
trace length Max=1.5"

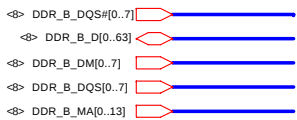


11/9 Modify pn to SP070006V00

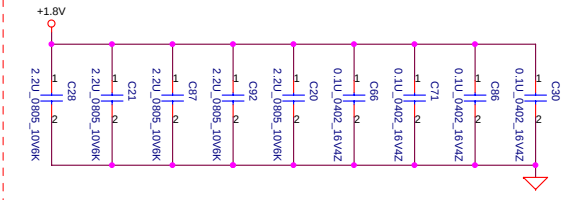
SO-DIMM A

Top side

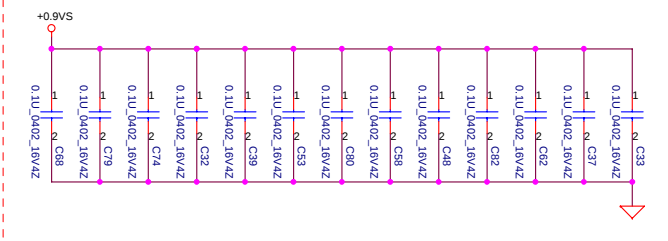
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Issued Date				2005/10/06				Deciphered Date			
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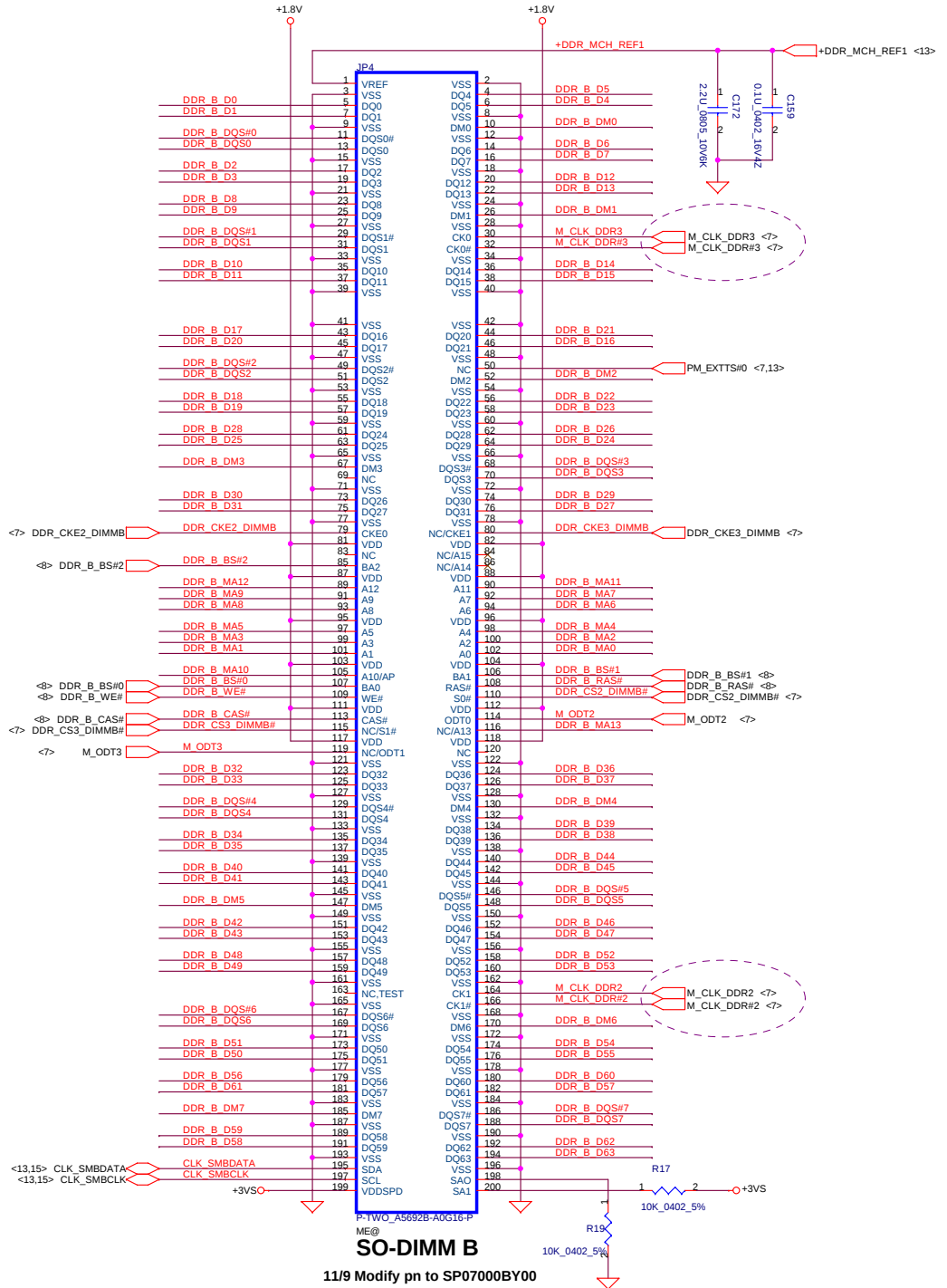
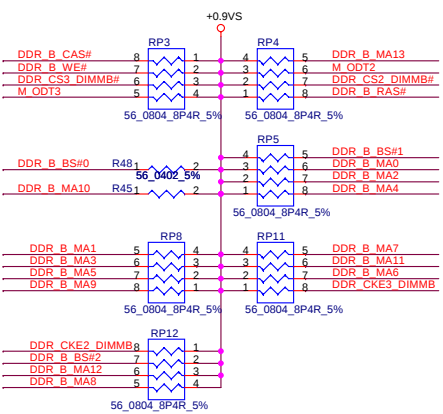
Layout Note:
Place near JP42



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



Layout Note:
Place these resistor closely JP42, all trace length Max=1.5"



SO-DIMM B

11/9 Modify pn to SP07000BY00

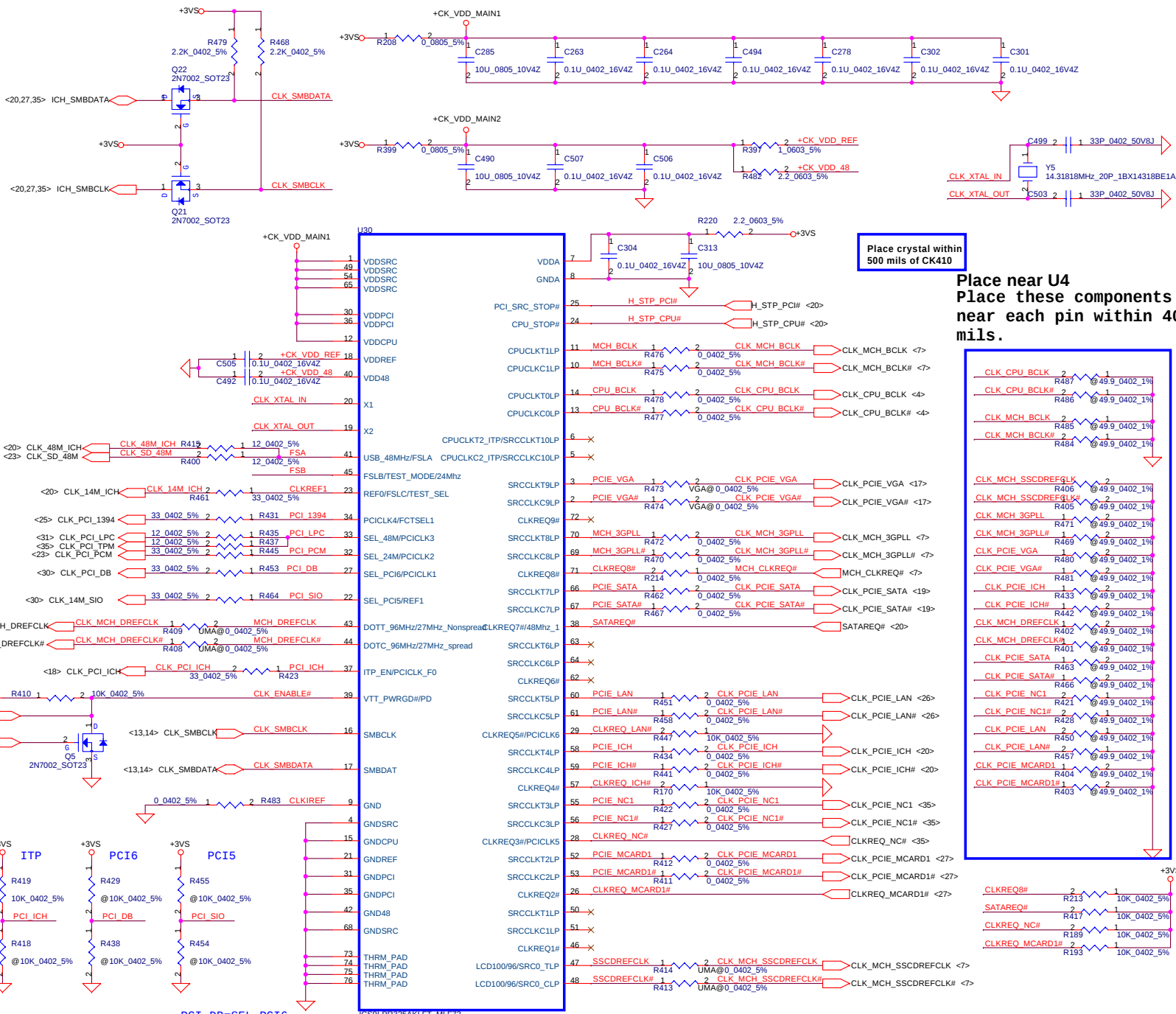
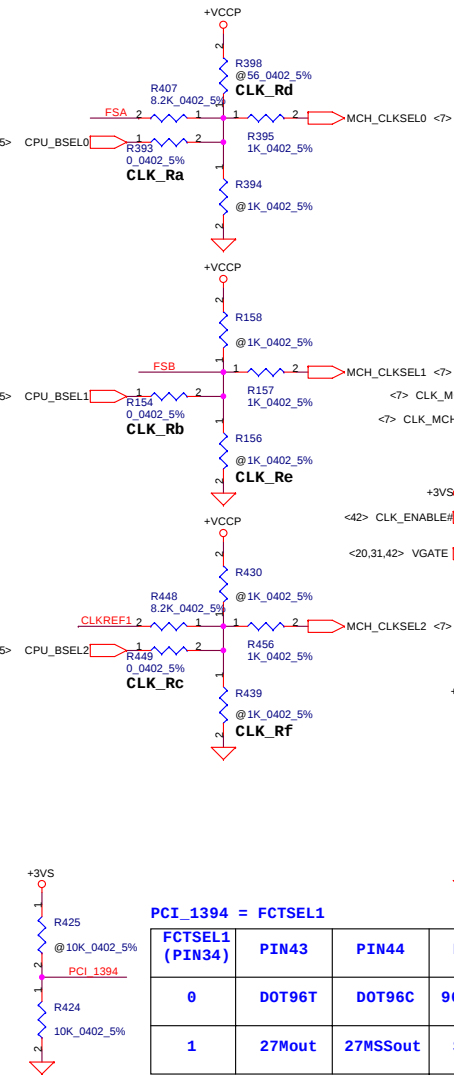
Security Classification		Compal Secret Data		Compal Electronics, Inc.			
Issued Date	2005/10/06	Deciphered Date	2006/10/06	DDRII-SODIMM SLOT2			
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FSLC	FSLB	FSLA	CPU	SRC	PCI
CLKSEL2	CLKSEL1	CLKSEL0	MHZ	MHZ	MHZ
0	0	1	133	100	33.3
0	1	1	166	100	33.3

Table : ICS954306

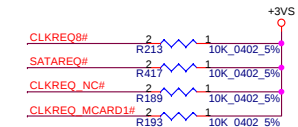
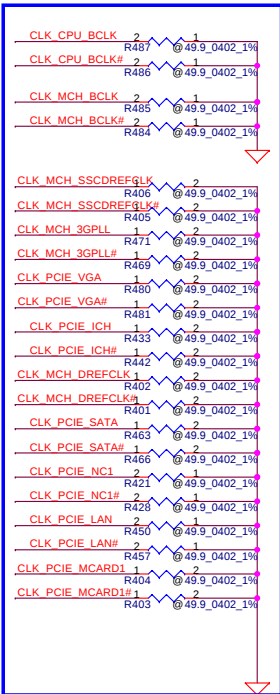
FSB Frequency Selet:

CPU Driven	Stuff	CLK_Ra	CLK_Rb	CLK_Rc
* (Default)	No Stuff	CLK_Rd	CLK_Re	CLK_Rf
533MHz	Stuff	CLK_Rd	CLK_Re	CLK_Rf
	No Stuff	CLK_Ra	CLK_Rb	CLK_Rc
667MHz	Stuff	CLK_Rd	CLK_Rf	
	No Stuff	CLK_Ra	CLK_Rb	CLK_Rc
		CLK_Re		



Place crystal within 500 mils of CK410

Place near U4
Place these components near each pin within 40 mils.



PCI_1394 = FCTSEL1				
FCTSEL1 (PIN34)	PIN43	PIN44	PIN47	PIN48
0	D0T96T	D0T96C	96/100M_T	96/100M_C
1	27Mout	27MSSout	SRCT0	SRCC0

PCI_DB=SEL_PCI6	
PCI_DB	PIN27
0	CLKREQ5
1	PCICLK6

ICS9LPR325CKLET_MLF72

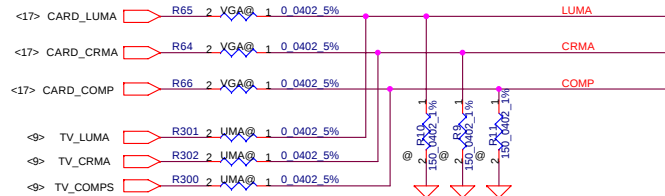
ICS9LPR325CKLET_MLF72: SA00000RE20

SLG8LP465VTR: SA00000TS00

2005/11/8 modify footprint to ICS954305DKLFT_MLF72 for Thermal Pad use

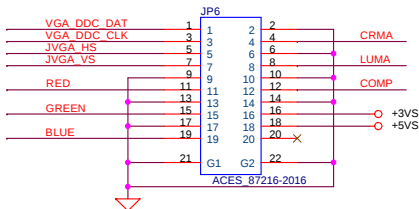
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TV-OUT Conn.

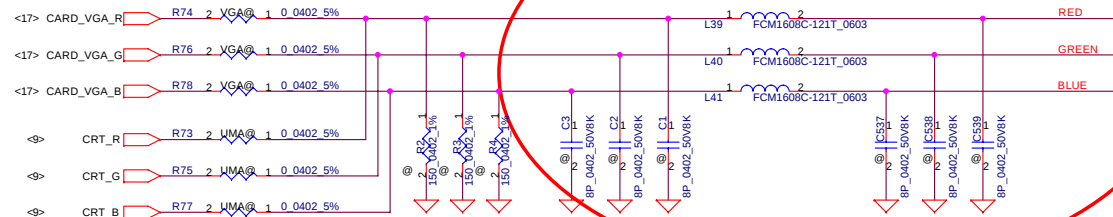


Pop when with internal graphics

VGA I/O PORT Conn.



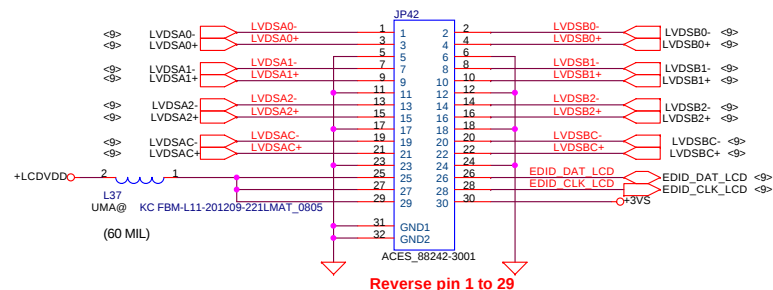
CRT Conn.



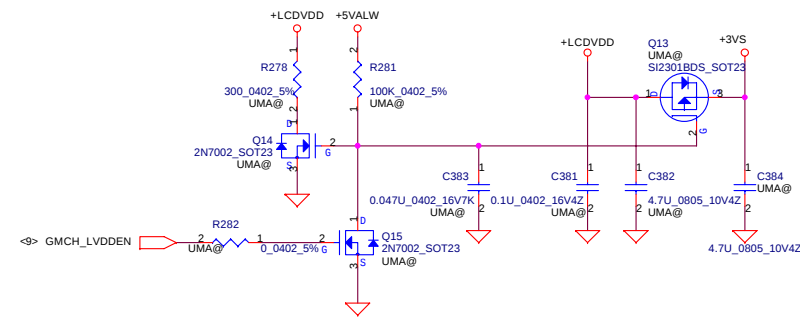
Pop when with internal graphics

2/09 Add for Compliance Engineering request

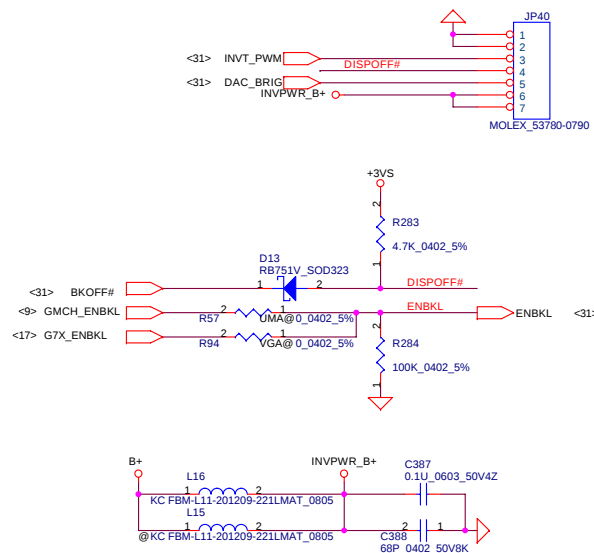
UMA LCD / PANEL Conn.



Reverse pin 1 to 29

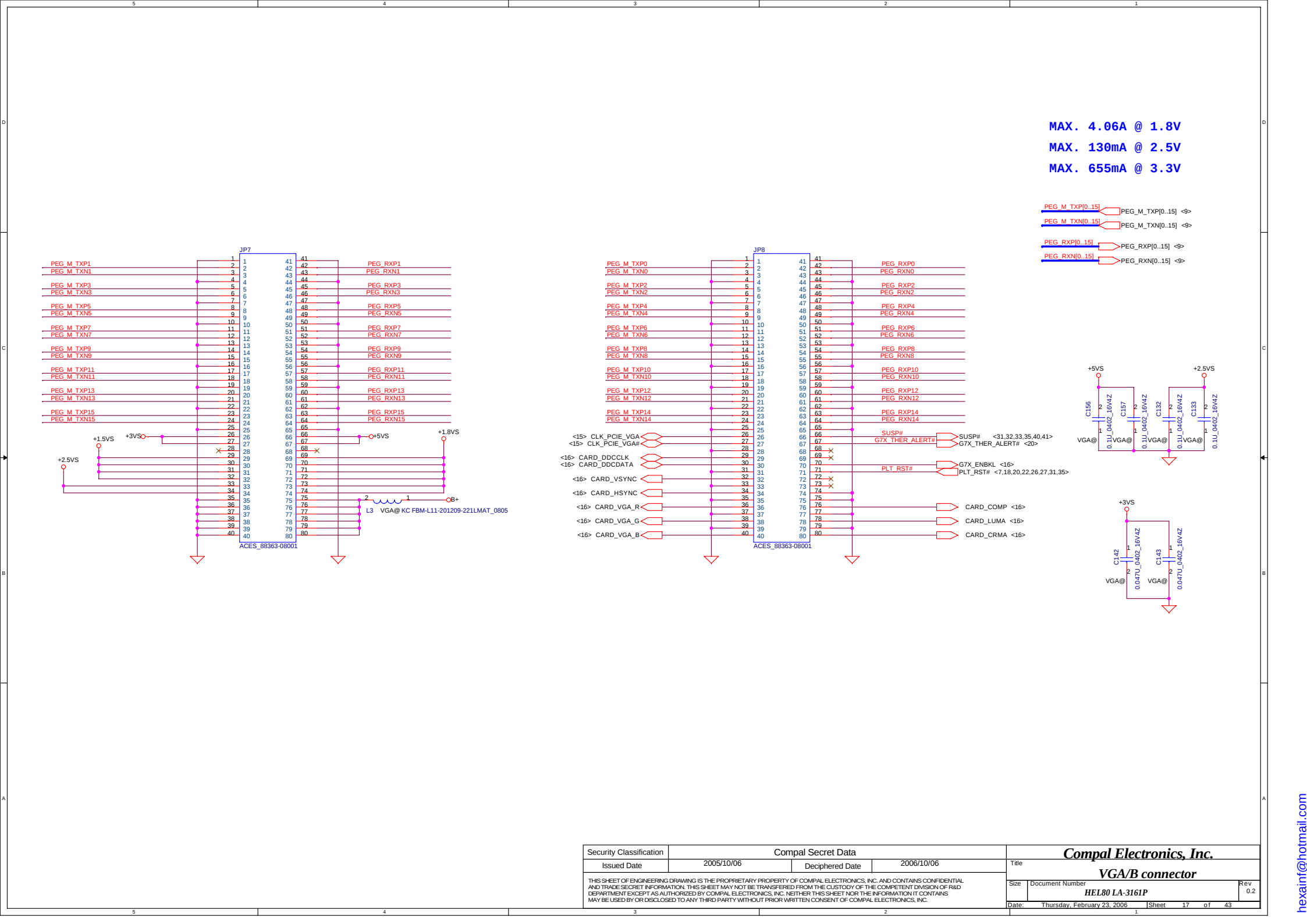


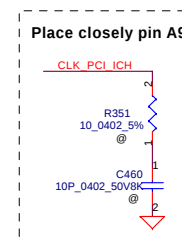
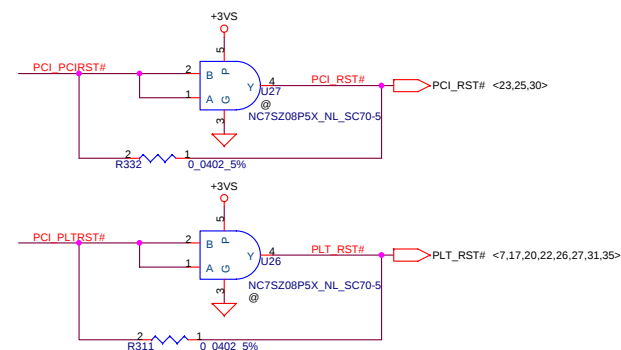
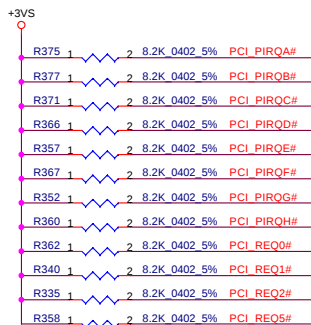
INVERTER Conn.



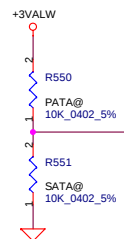
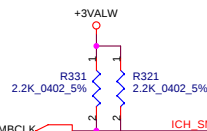
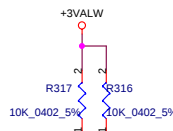
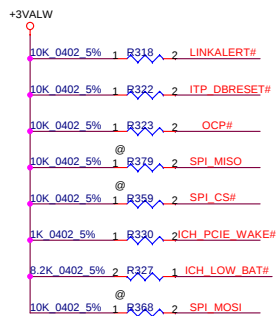
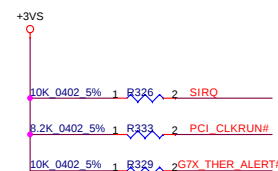
Pop when with internal graphics

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Size	Document Number	Rev		0.2	
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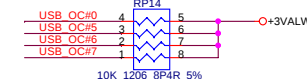
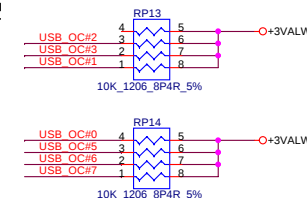
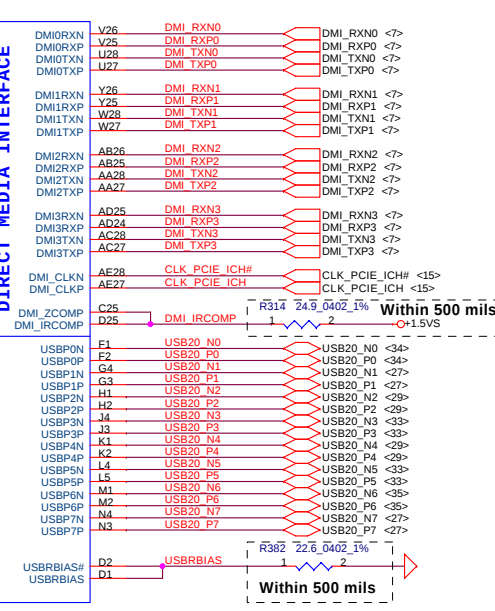
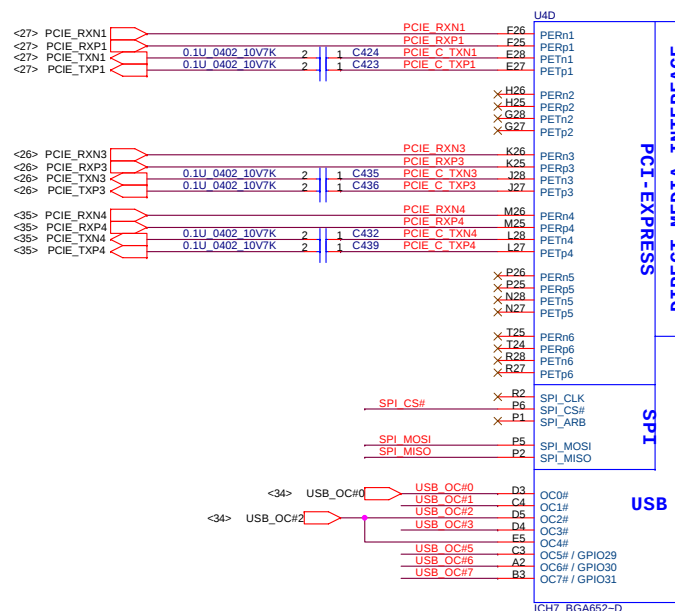
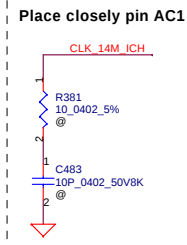
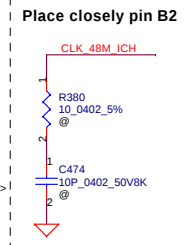
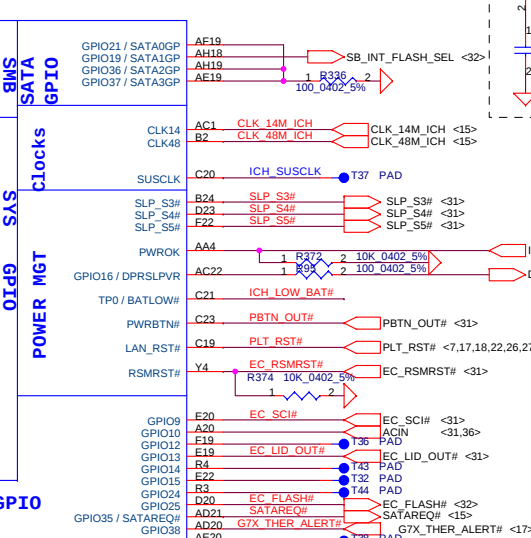
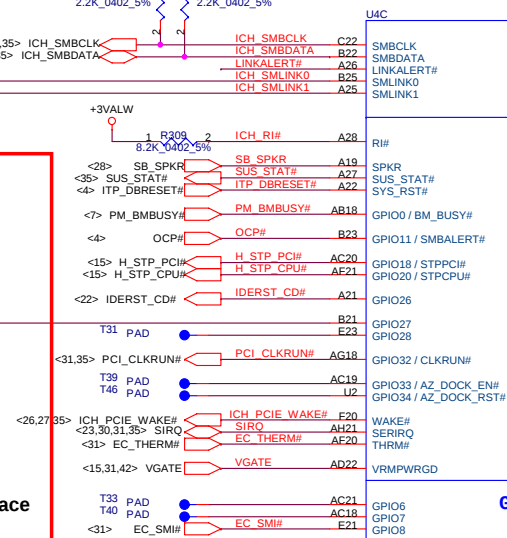




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				ICH7-M(1/4)		
				Size	Document Number	Rev
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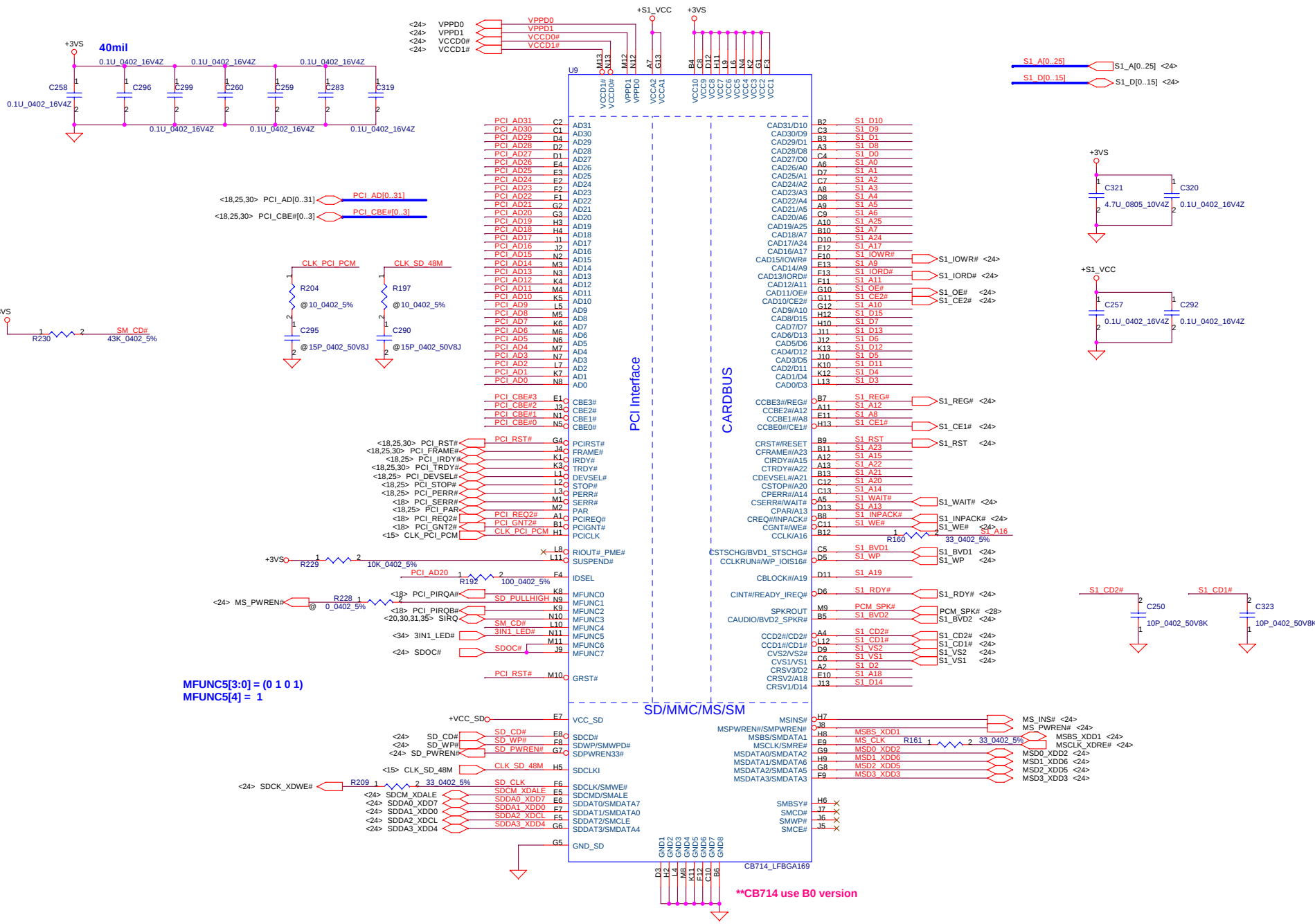


2/13 Add feature:
Pull high for pure IDE interface
Pull low for SATA interface



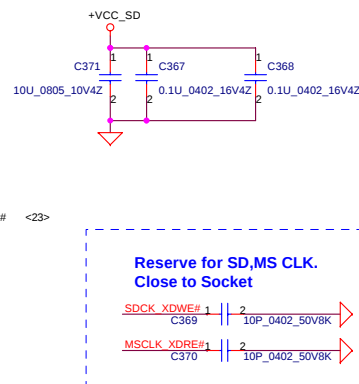
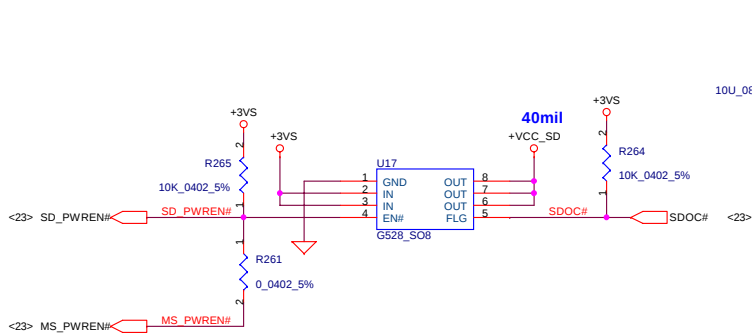
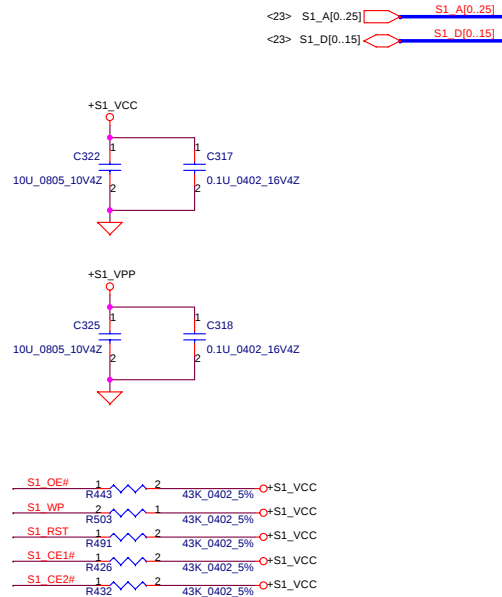
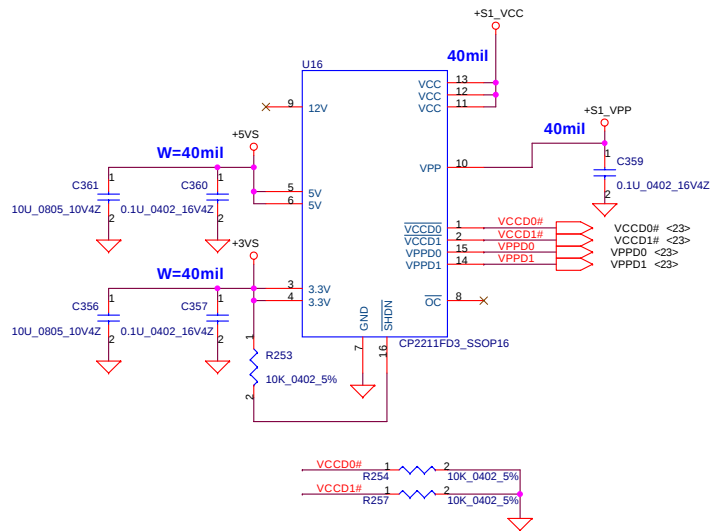
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				Size	Document Number
				Custom	HE180 LA-3161P
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PCMCIA Power Control

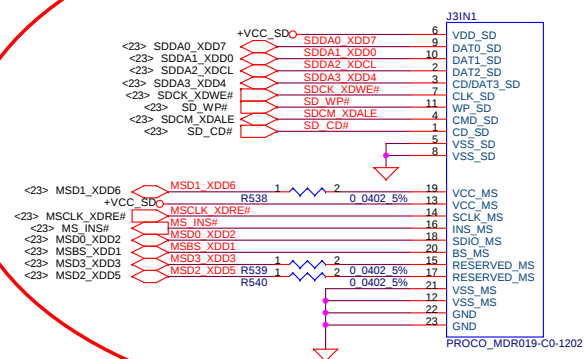
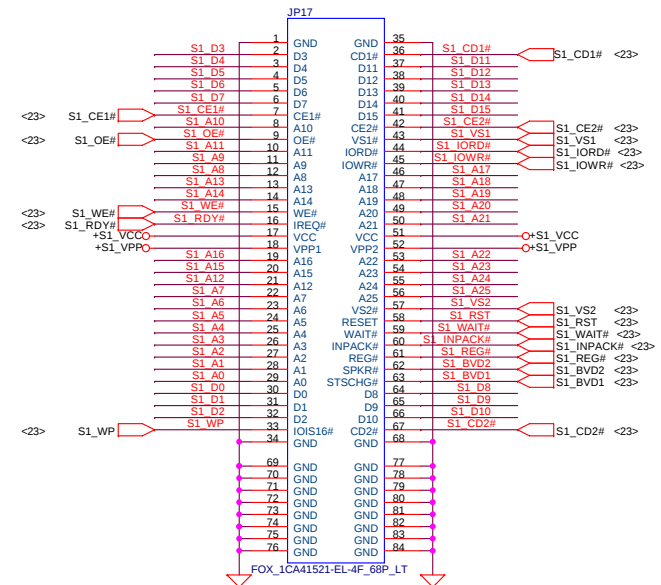


PCMCIA Socket

Note : 11/10 modify library to meet spec

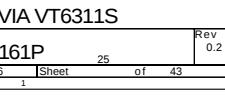
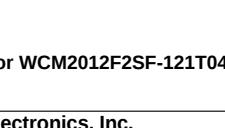
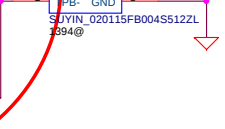
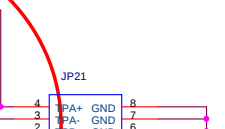
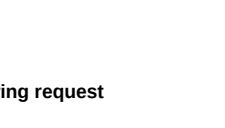
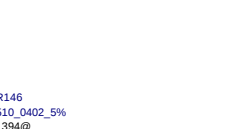
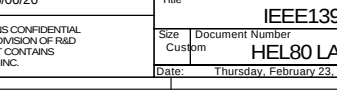
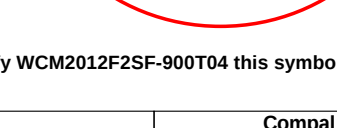
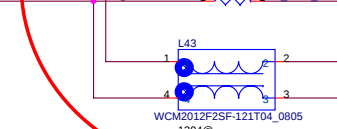
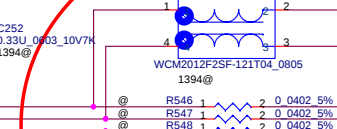
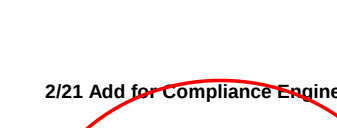
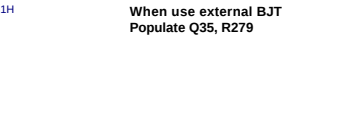
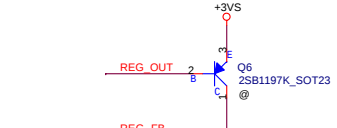
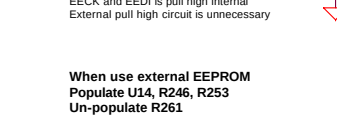
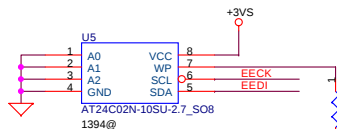
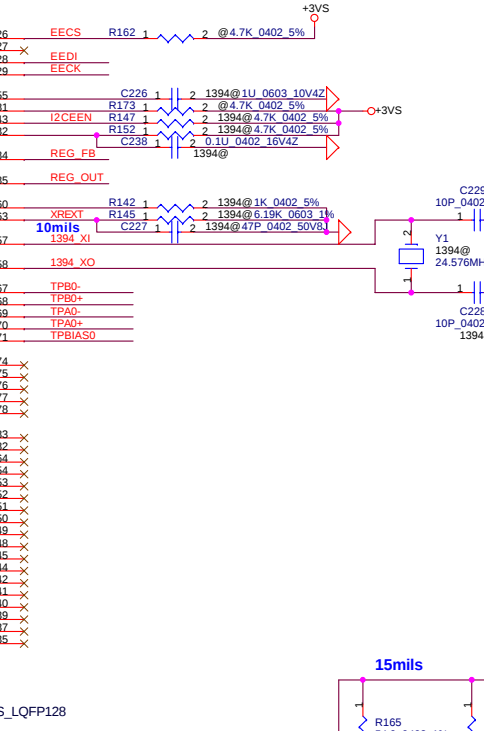
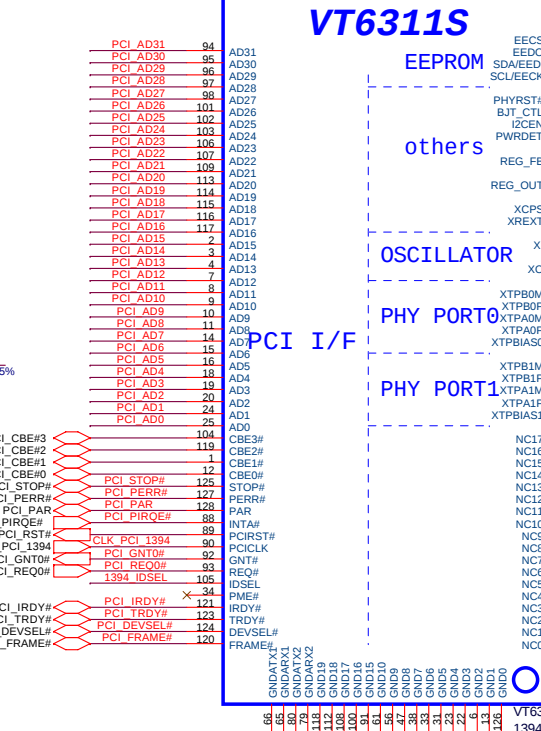
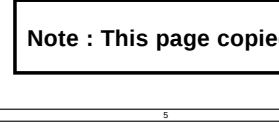
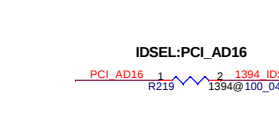
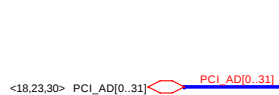
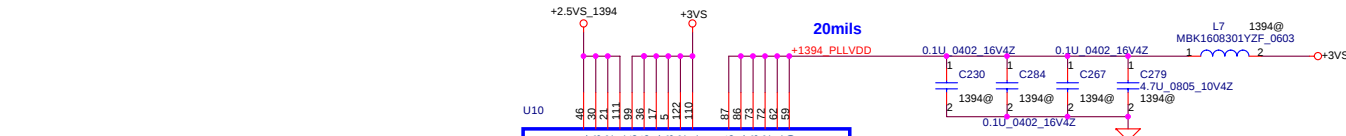
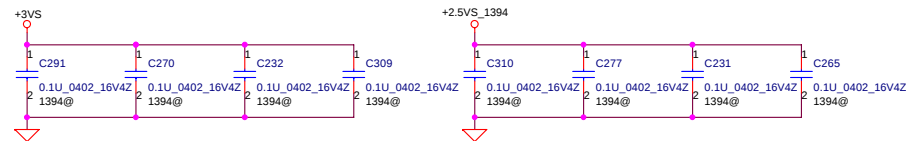
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02/17 modify footprint to FOX_1CA41521-EL-4F_68P_LT



12/20 modified

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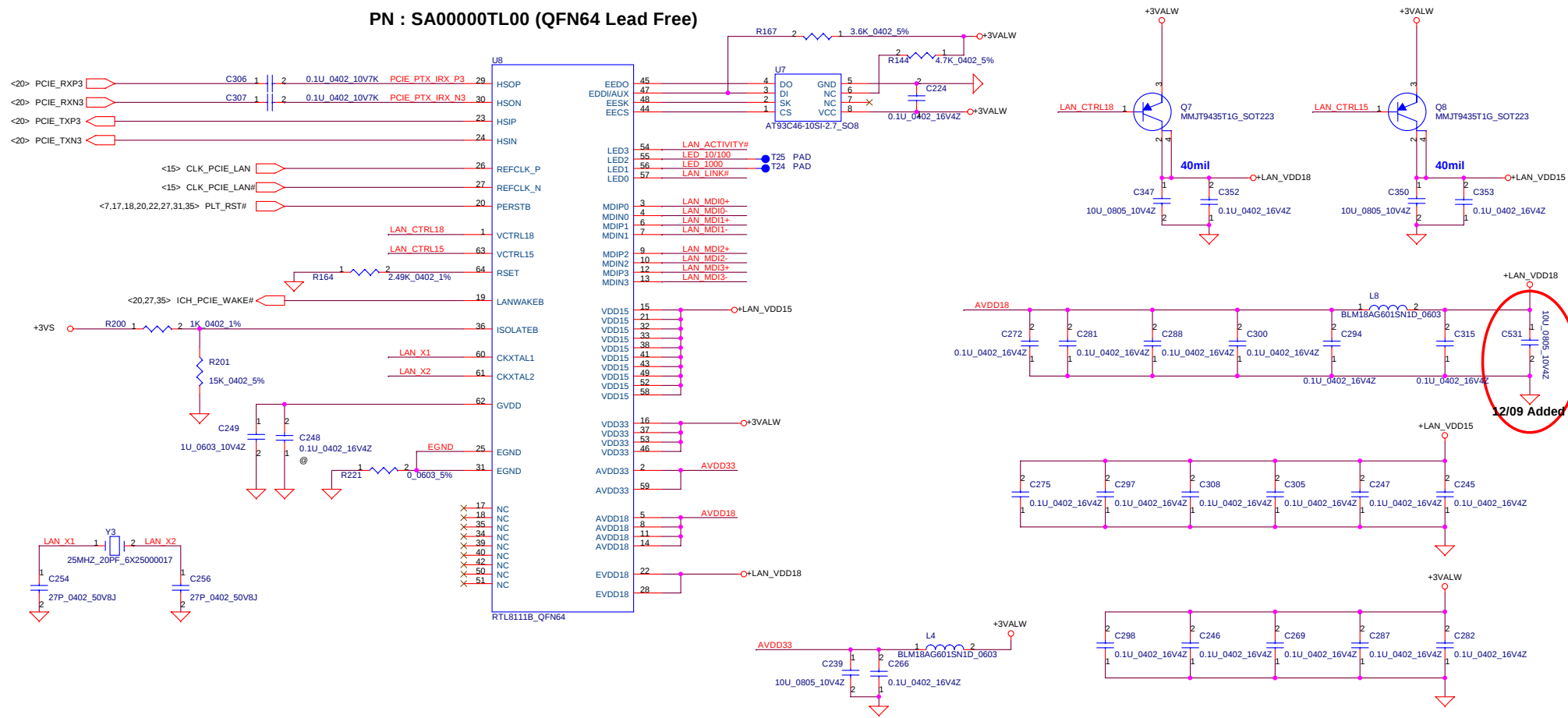
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Size		Document Number		Rev	
Custom		HEL80 LA-3161P		25	
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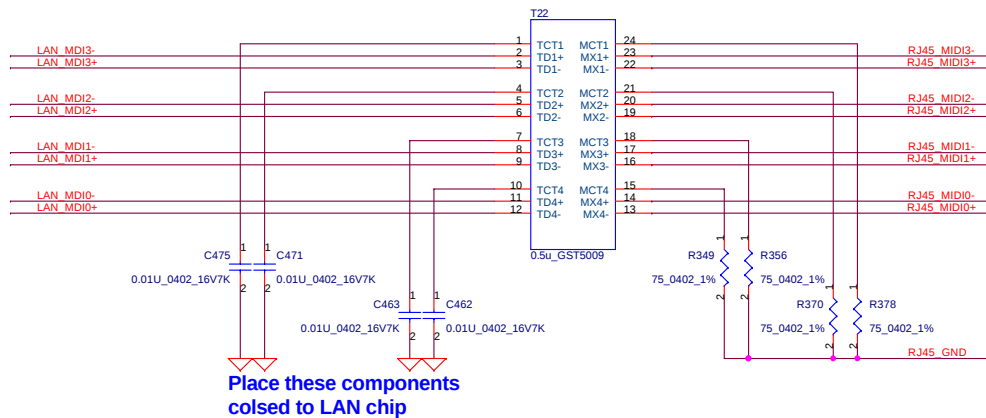
Modify WCM2012F2SF-900T04 this symbol for WCM2012F2SF-121T04

2/21 Add for Compliance Engineering request

PN : SA00000TL00 (QFN64 Lead Free)

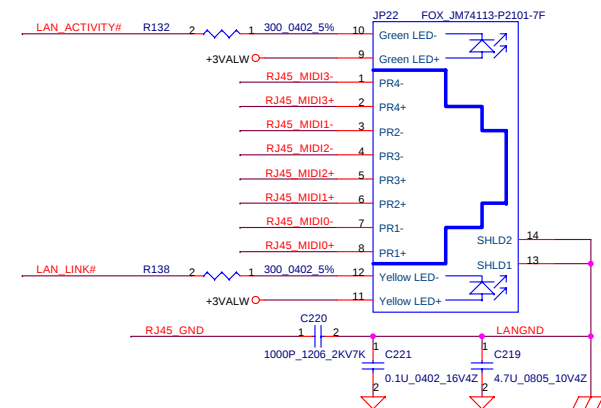


GbE Transformer: GST5009 (SP050005610) MY



Place these components
colsed to LAN chip

LAN Conn.

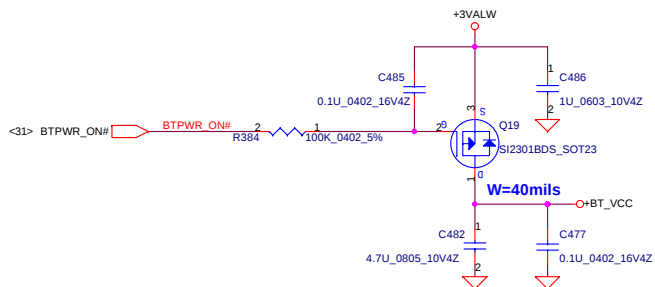
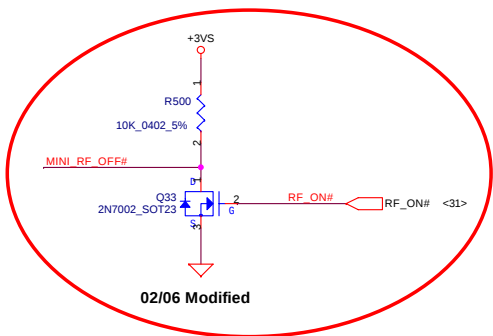
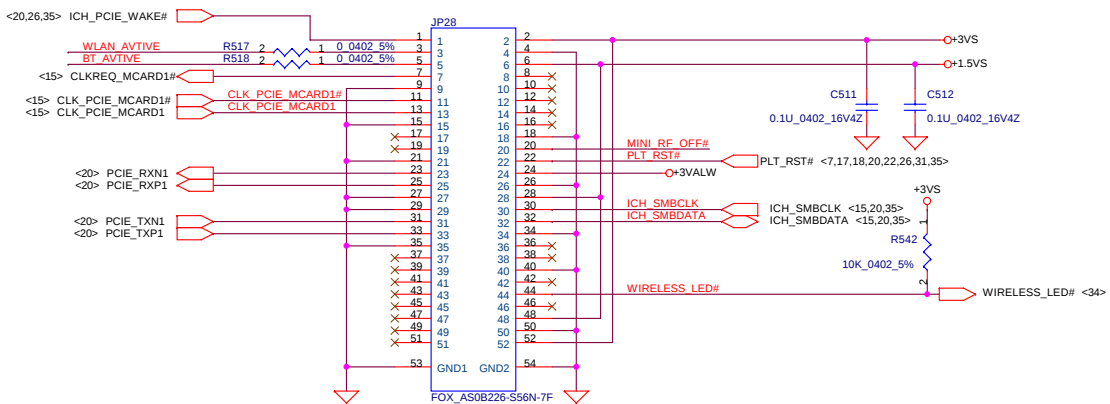


Compal Electronics, Inc.

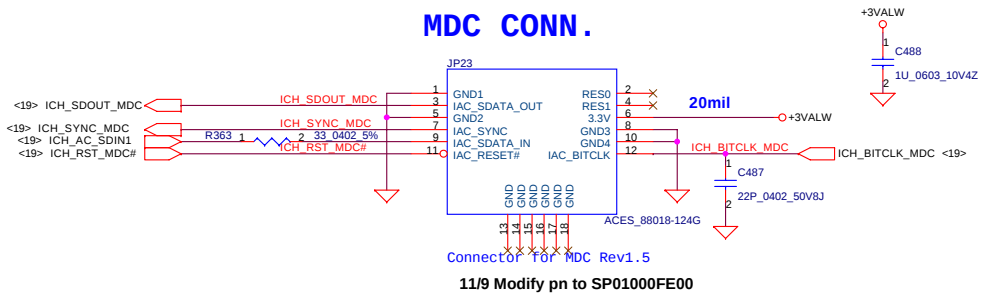
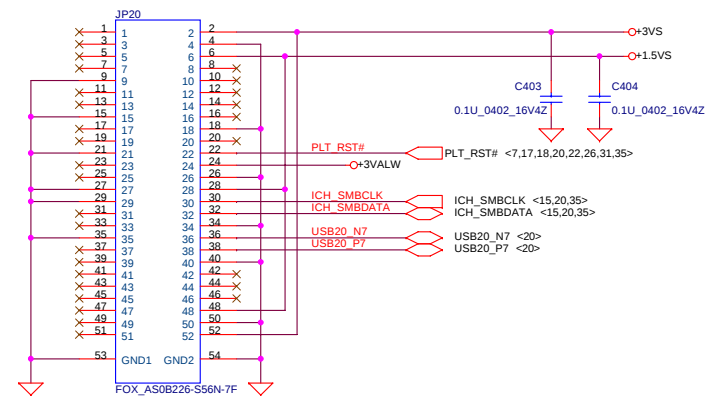
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Size	Document Number	HEL80 LA-3161P		Rev 0.2
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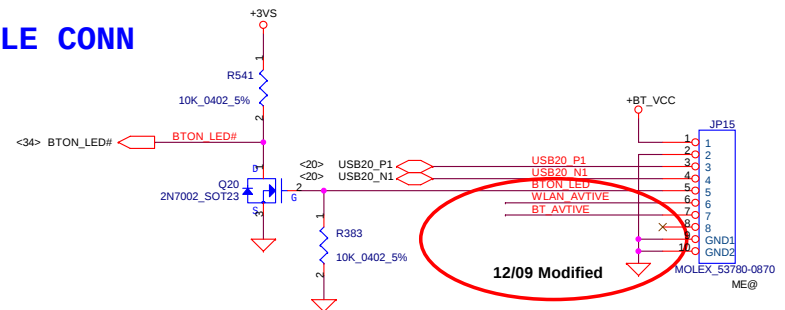
Mini-Express Card(Slot 1-WLAN)



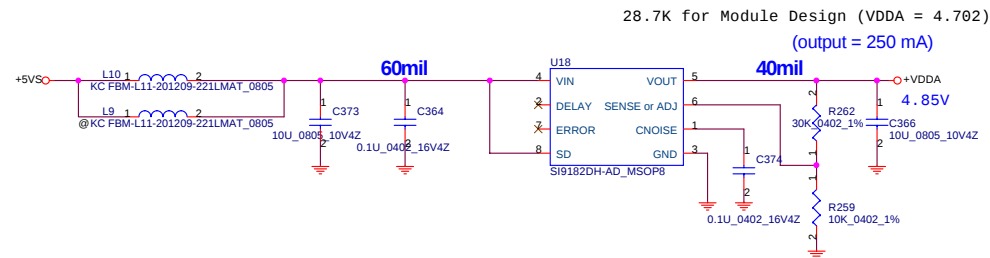
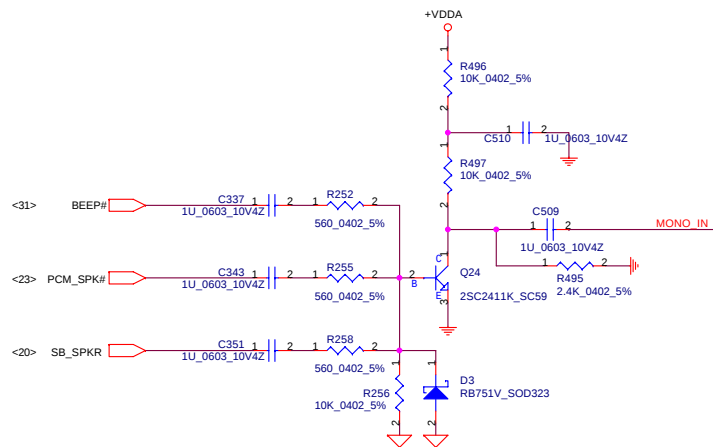
Mini-Express Card(Slot 2-TV)



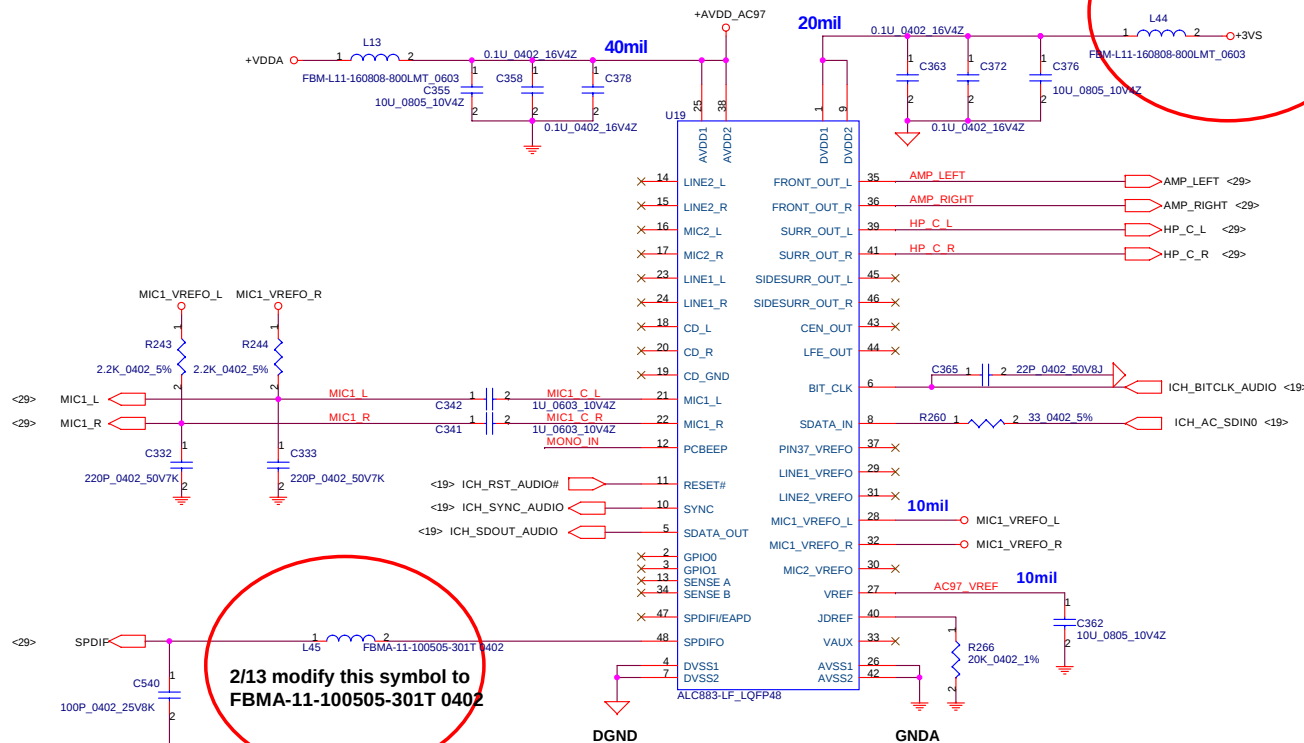
BT MODULE CONN



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				Custody	HEL80/81 LA-3161P	0.1
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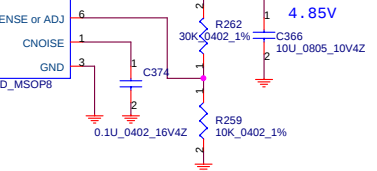


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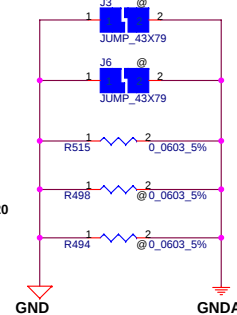


28.7K for Module Design (VDDA = 4.702)

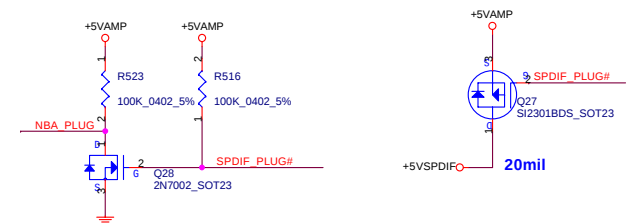
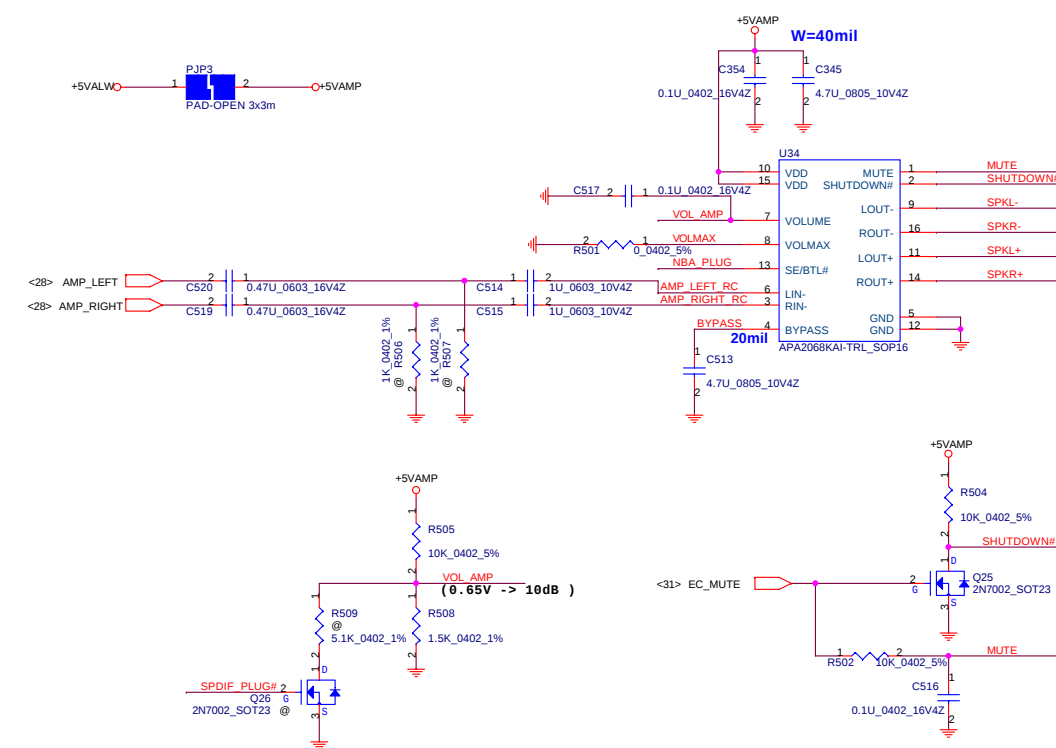
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2005/09/20

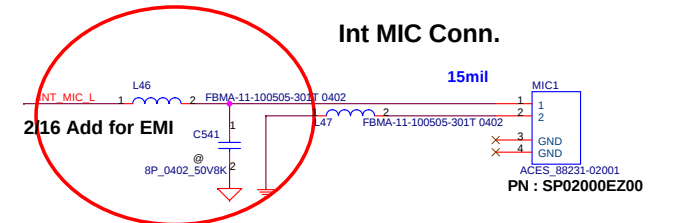
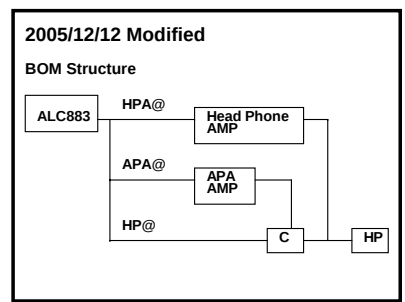
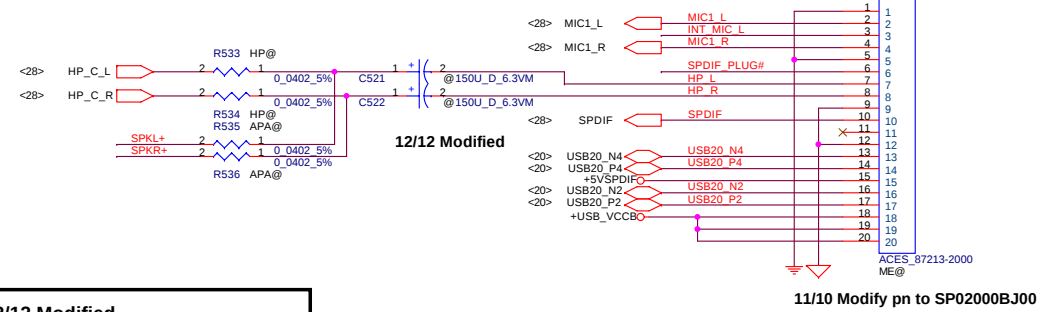


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				Size	Document Number
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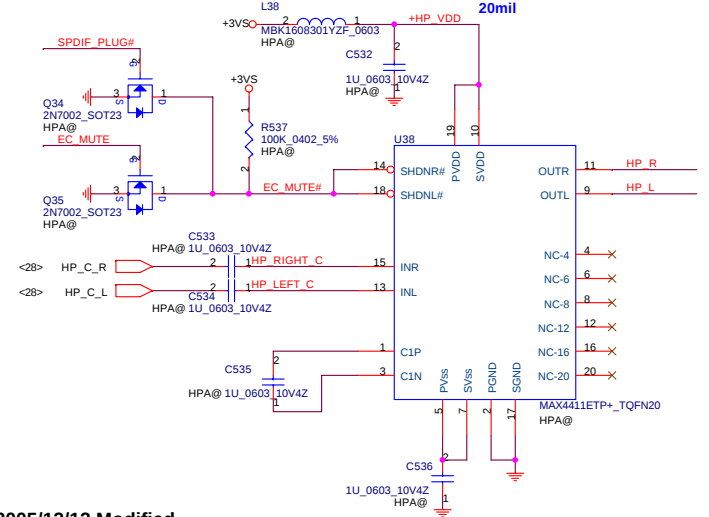
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Un-Plug	H	L
HP_Plug_In	L	H
SPDIF_Plug_In	L	H

Audio Jack/USB Conn.



HEAD PHONE AMP

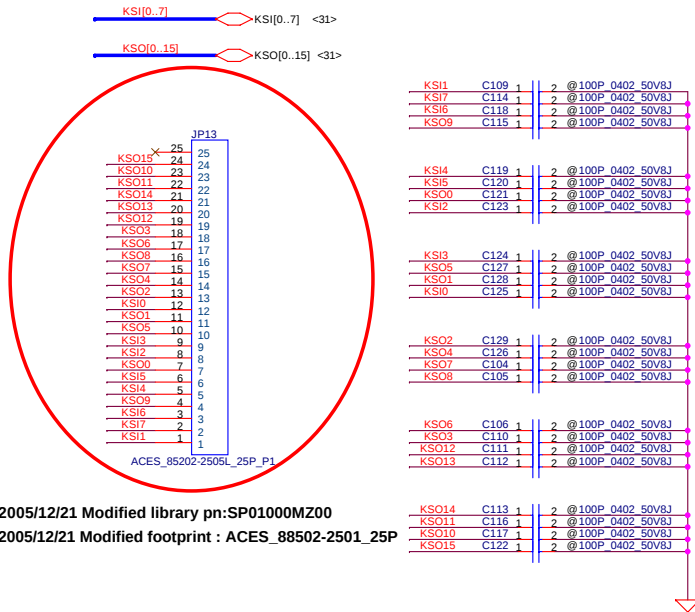
HPF Fc = 338Hz
R=1K, C=0.22U for HBQ60



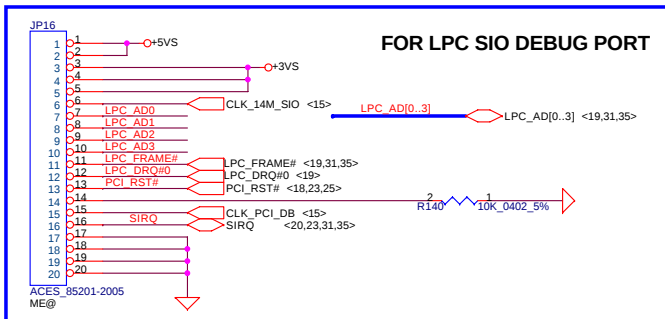
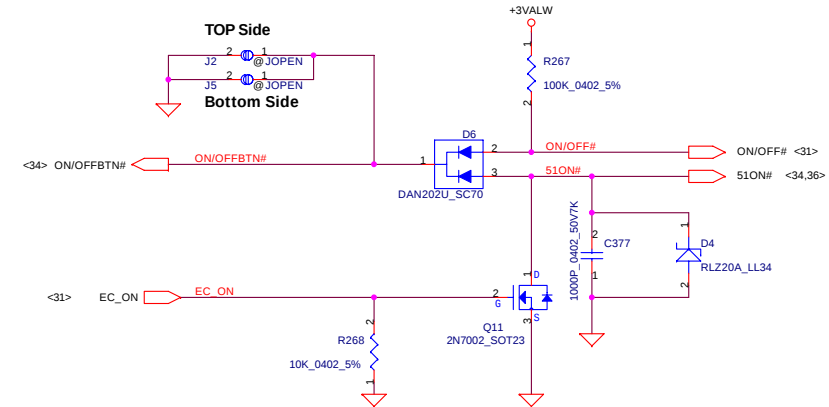
2005/12/12 Modified

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Issued Date	2005/10/06	Deciphered Date	2006/10/06	AMP & Audio Jack	
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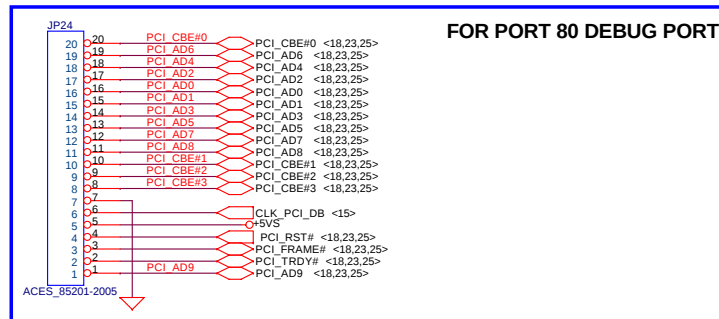
INT_KBD CONN.(TYPE "D" KB)



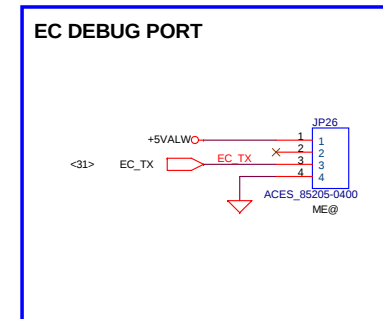
Power BTN



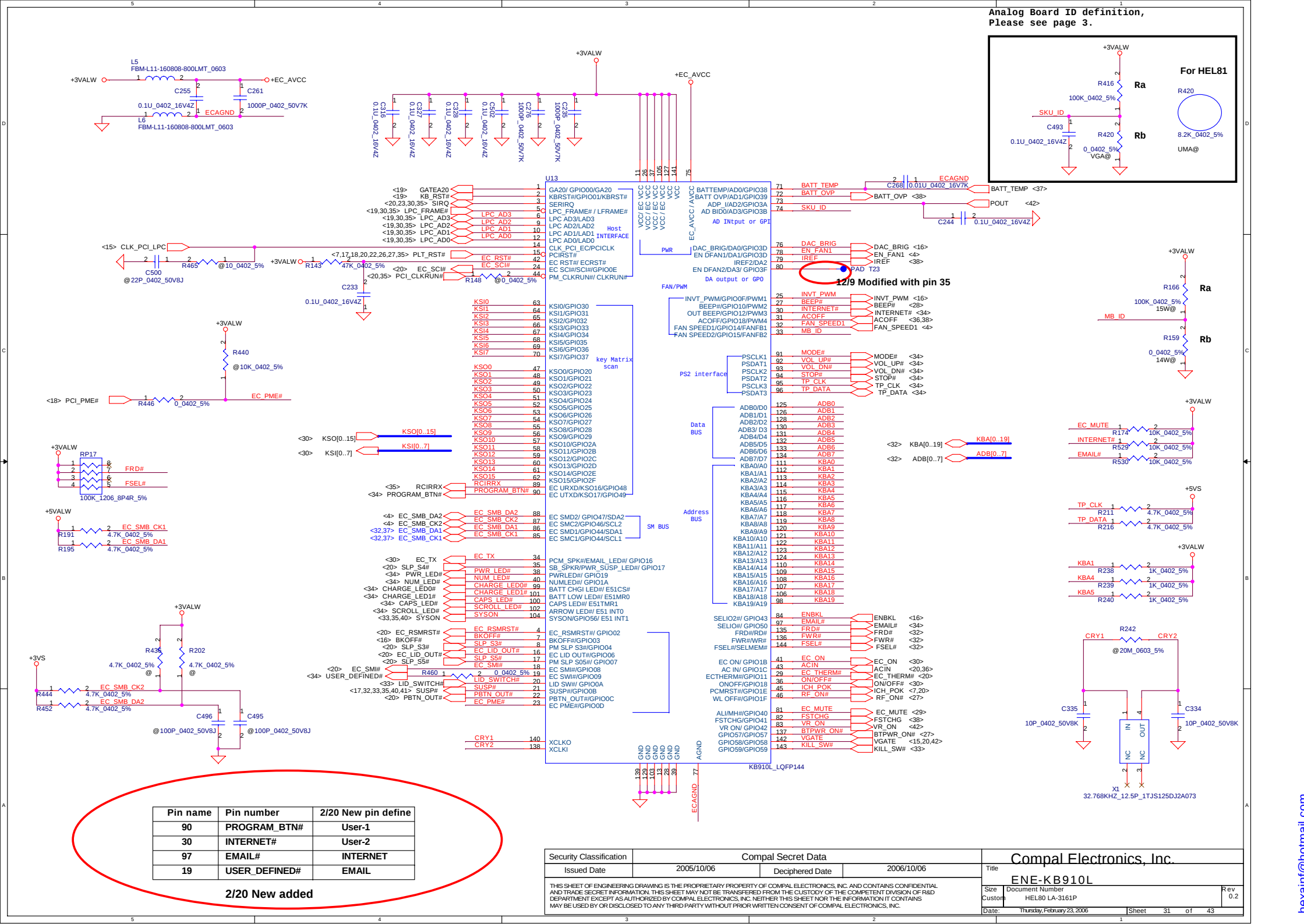
Not lead free



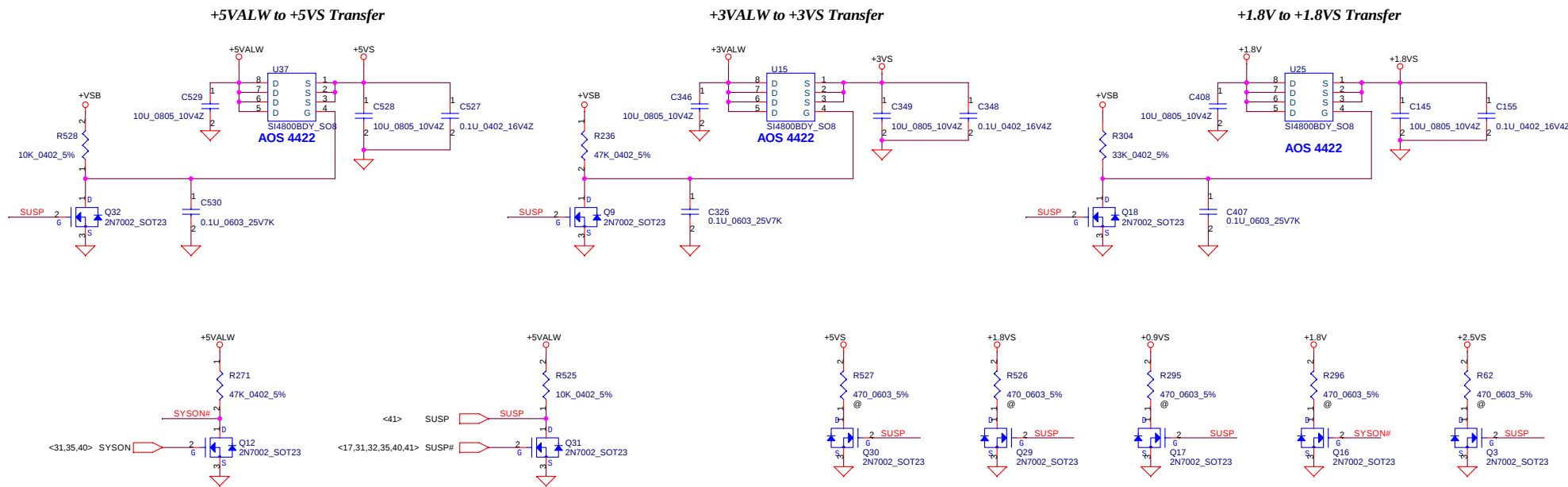
Not lead free



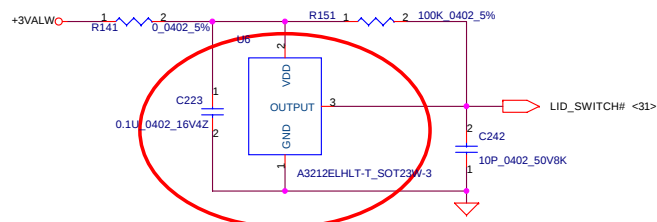
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Issued Date	2005/10/06	Deciphered Date	2006/10/06	KBD,ON/OFF,T/P,LED/B,DEBUG	
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				Size	Document Number	Rev
				Custome	HEL80 LA-3161P	0.2
				Date:	Thursday, February 23, 2006	ISheet 32 of 43

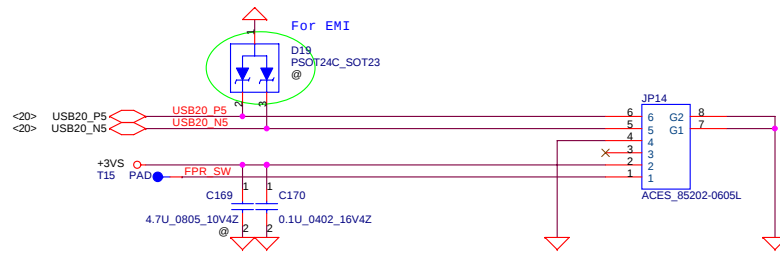


LID Switch



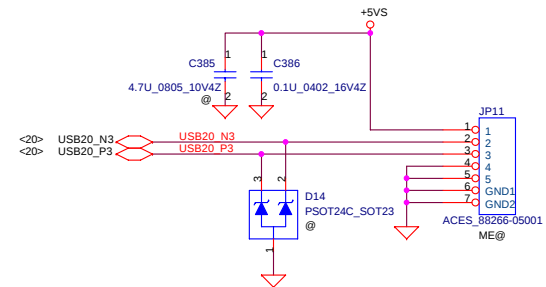
12/9 Change to SA032120010

Finger Print board + MP3 Module CONN.

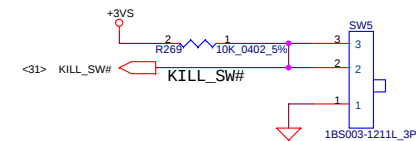


ACES

CMOS Camera Conn

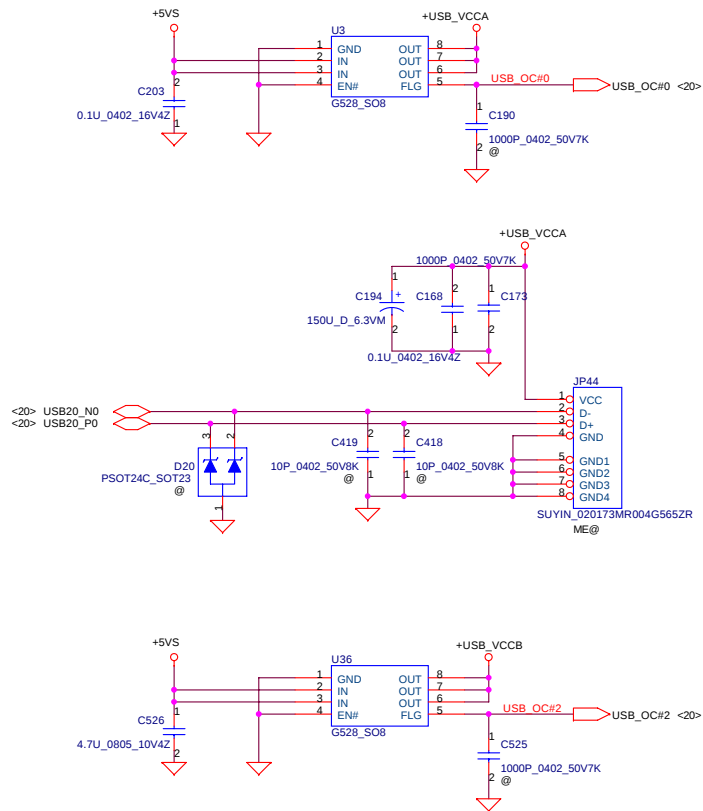


Kill Switch

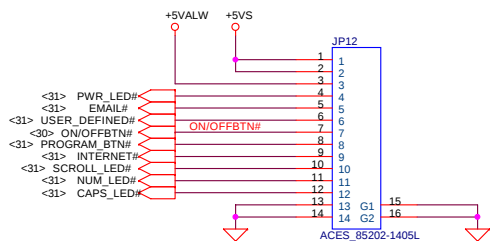


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				Date	Thursday, February 23, 2006
				Sheet	33 of 43
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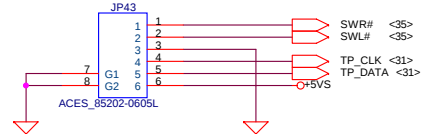
USB Port



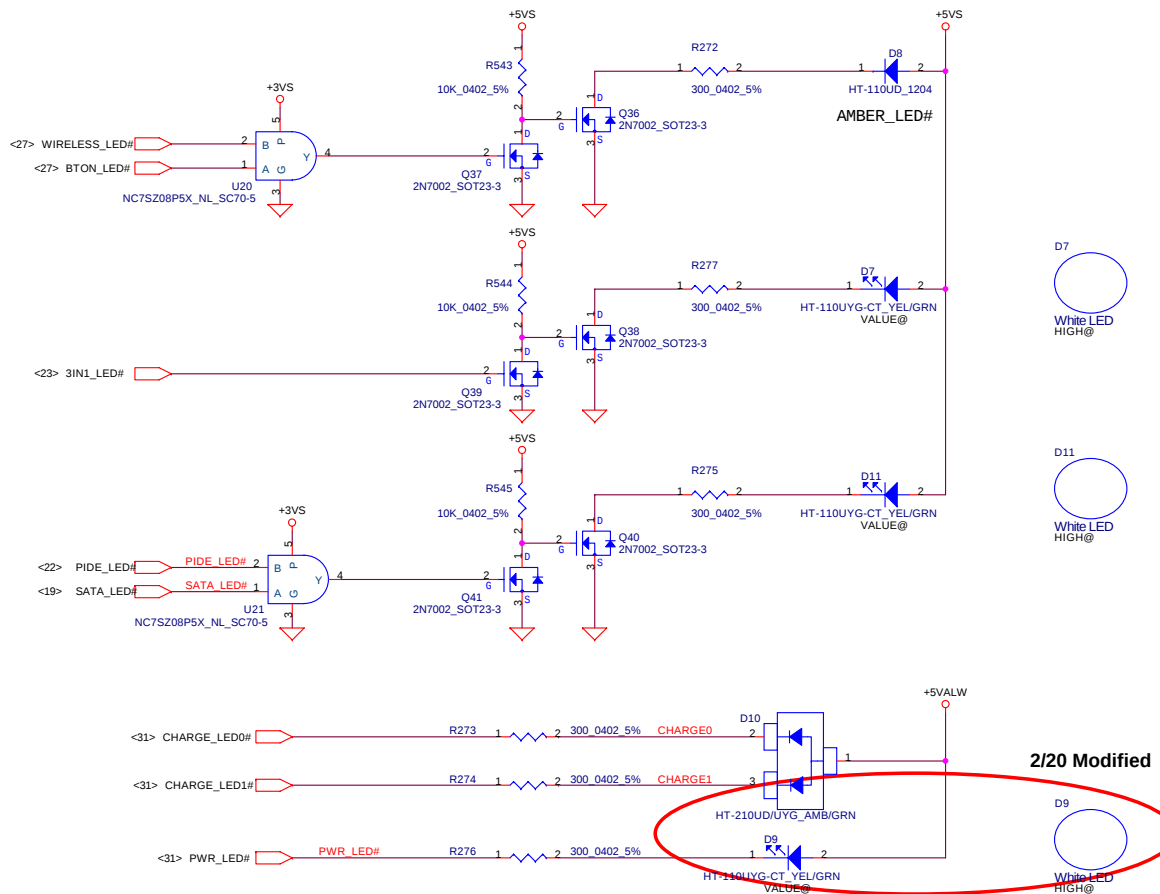
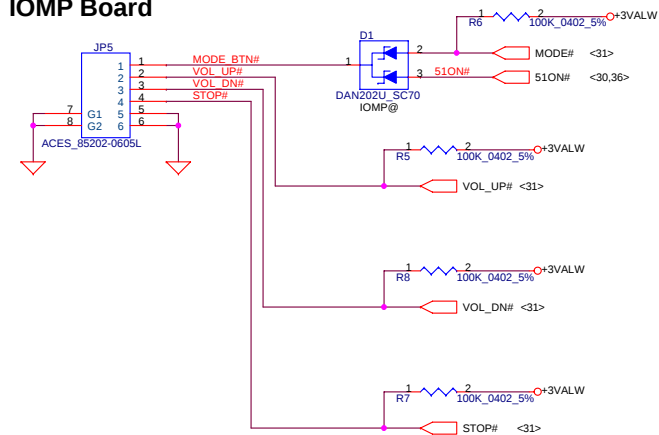
Switch Board CONN.



T/P Board

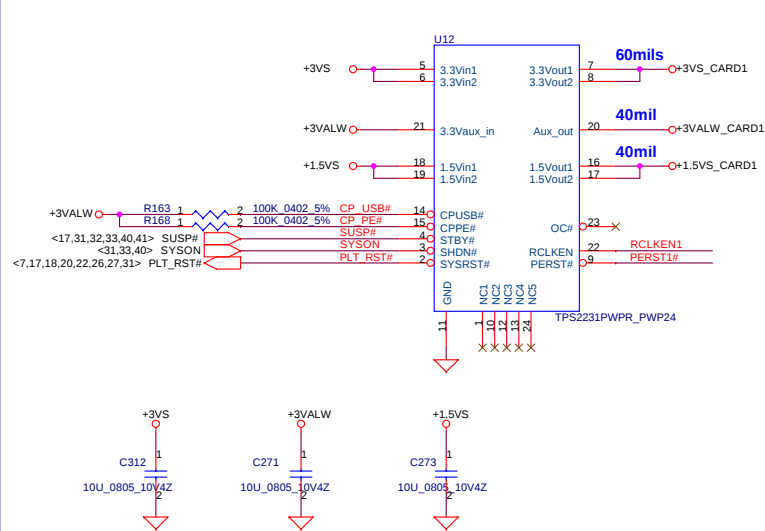


IOMP Board

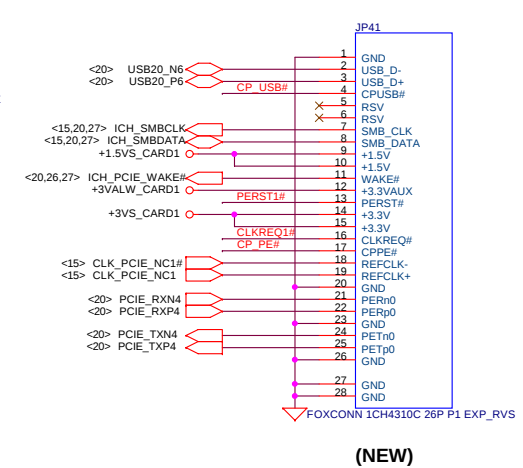


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				INDICATE LED	
				Size	
				Document Number	
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New Card Power Switch

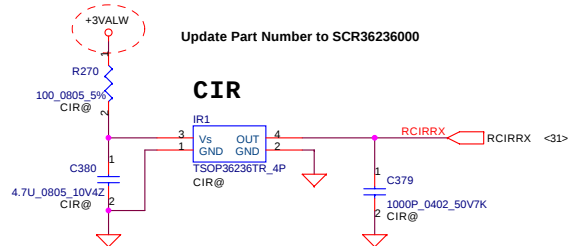


New Card Socket (Left)

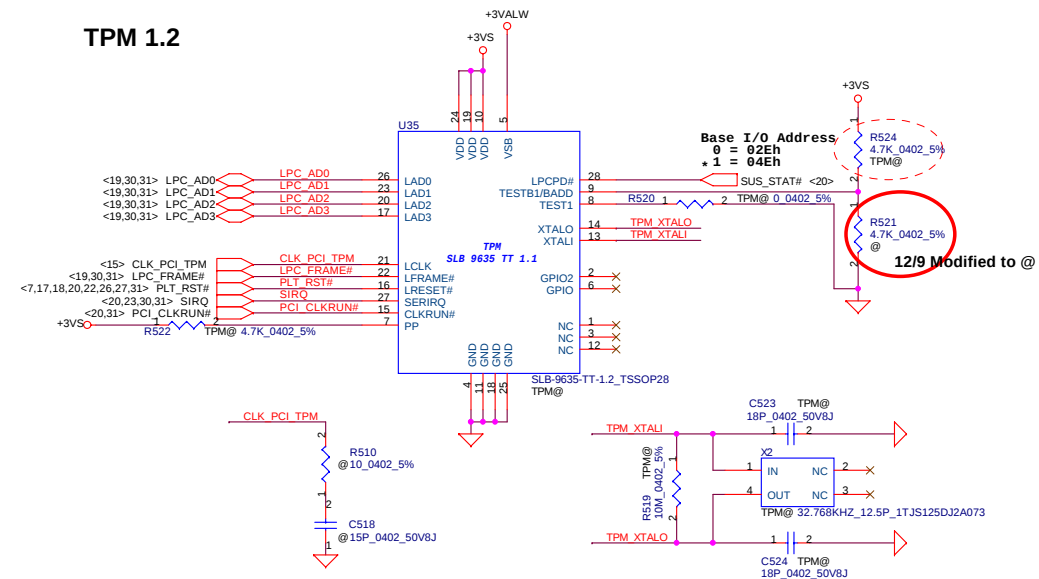


2005/11/4 Modified library pn:SP02000JC00
2005/12/9 Modified footprint to FOX_1CX43201_26P_LB

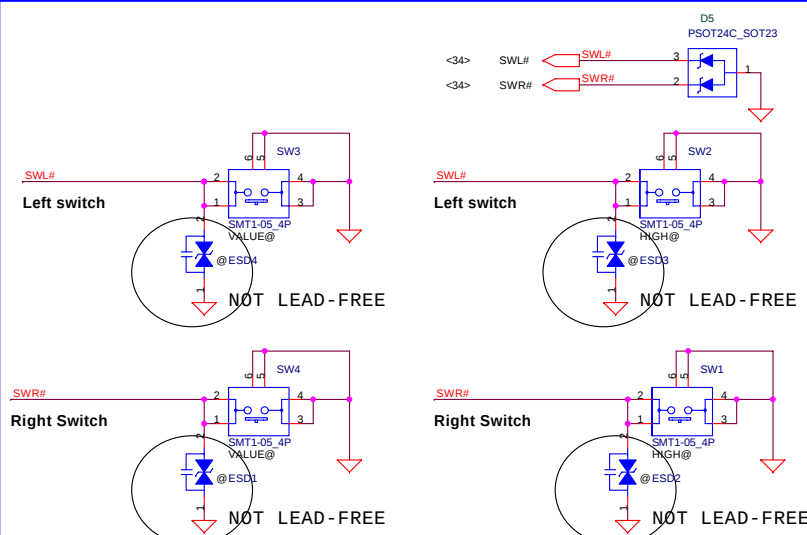
CIR



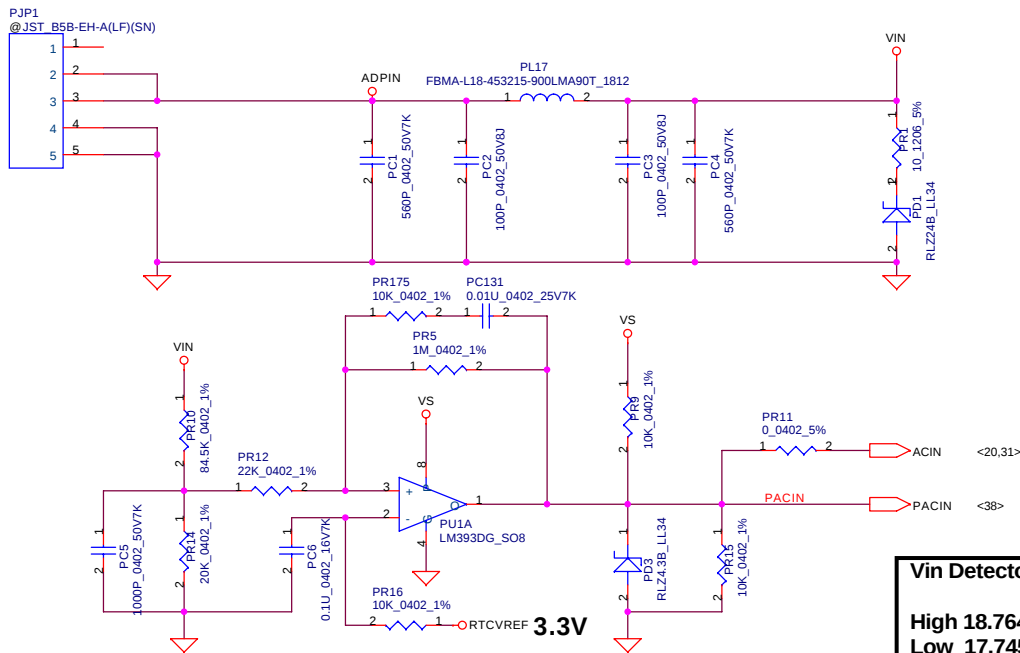
TPM 1.2



Note : TPM IC Lead free status is MN



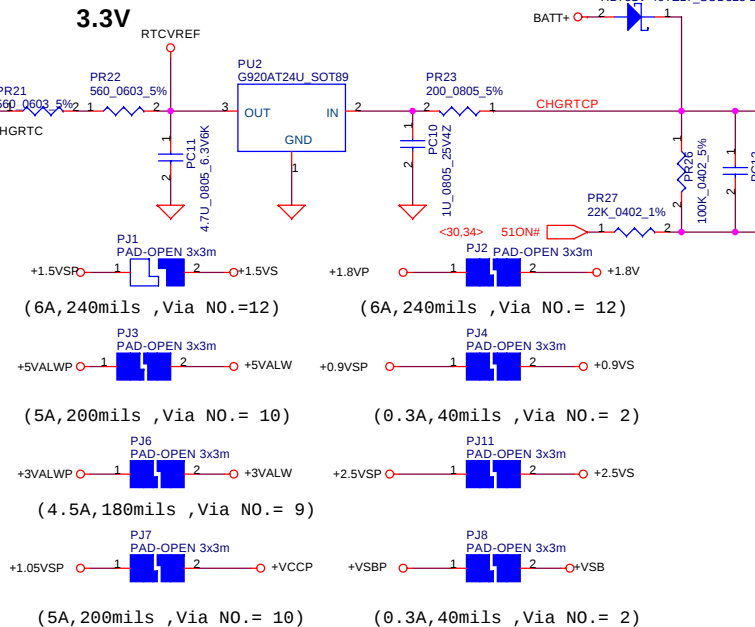
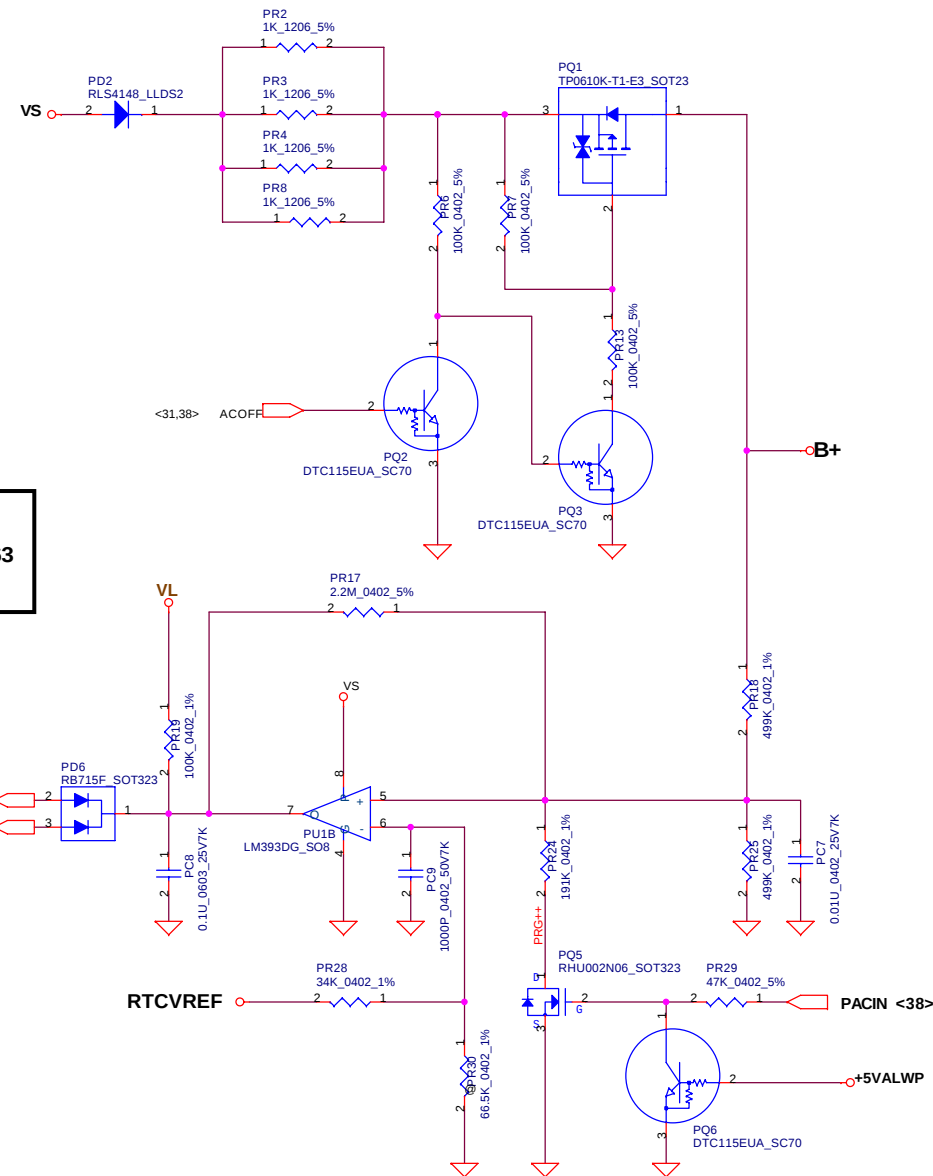
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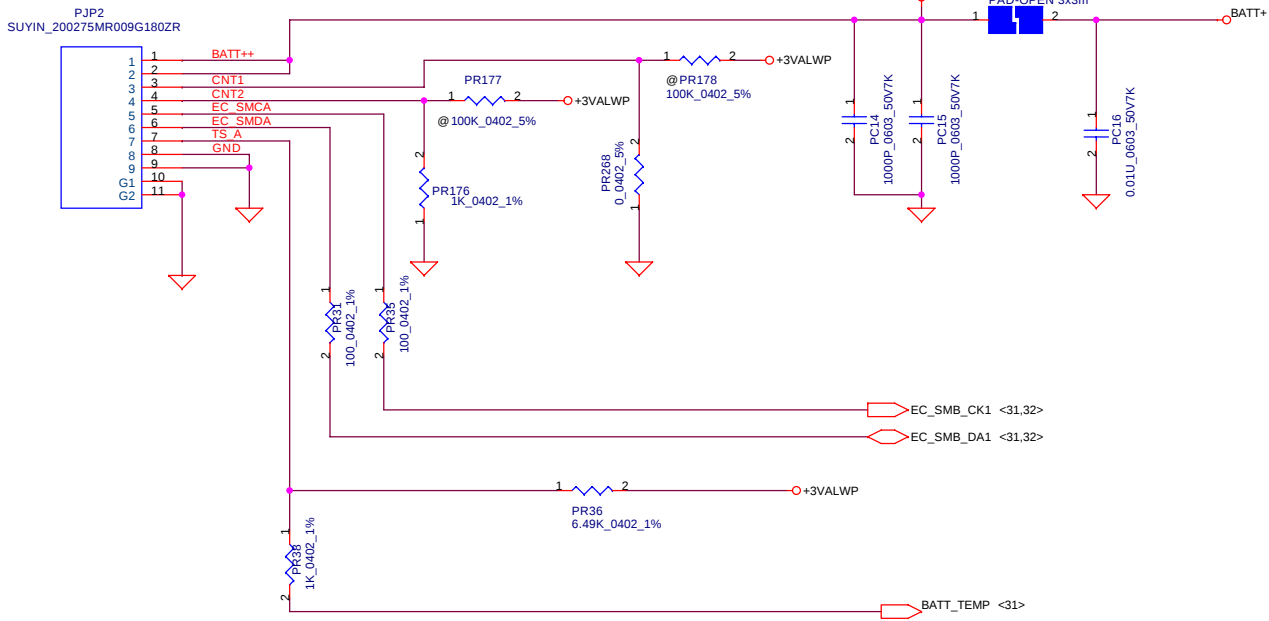
Vin Detector			
High	18.764	17.901	17.063
Low	17.745	16.9	16.03

ACIN			
	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

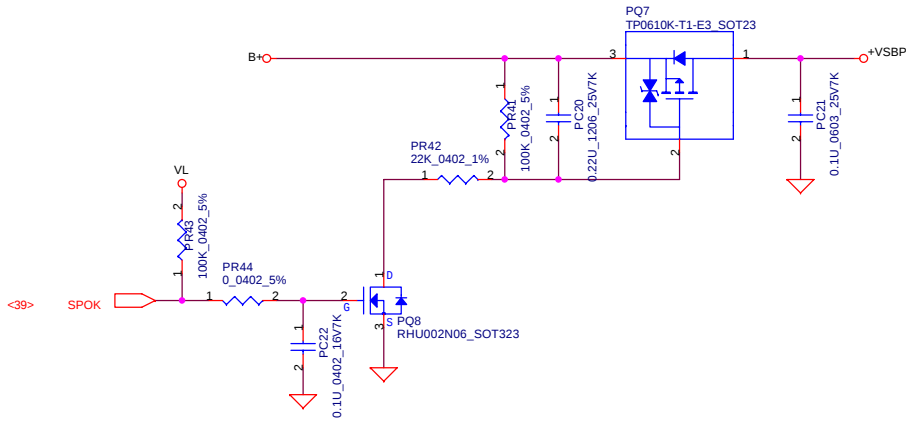
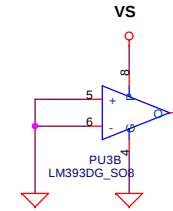
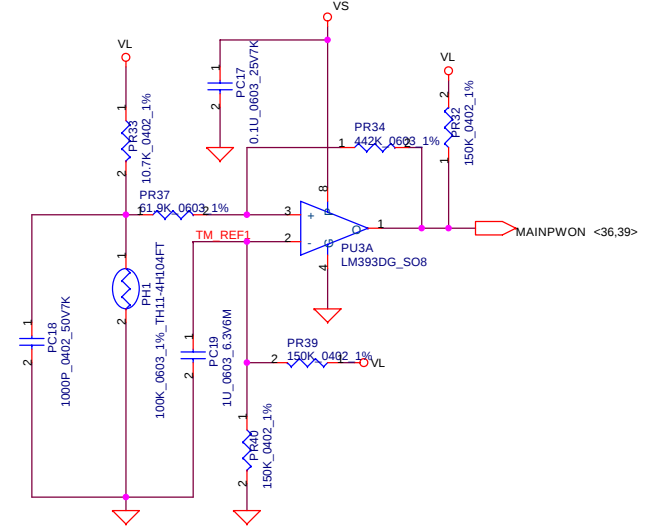
BATT ONLY			
	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V



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PH1 under CPU bottom side :
 CPU thermal protection at 85 degree C
 Recovery at 70 degree C



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$$F_{osc} = 14100 / R_t = 14100 / 47 = 300 \text{ KHz}$$

IREF=0.932*Icharge
IREF=0.466~2.8V

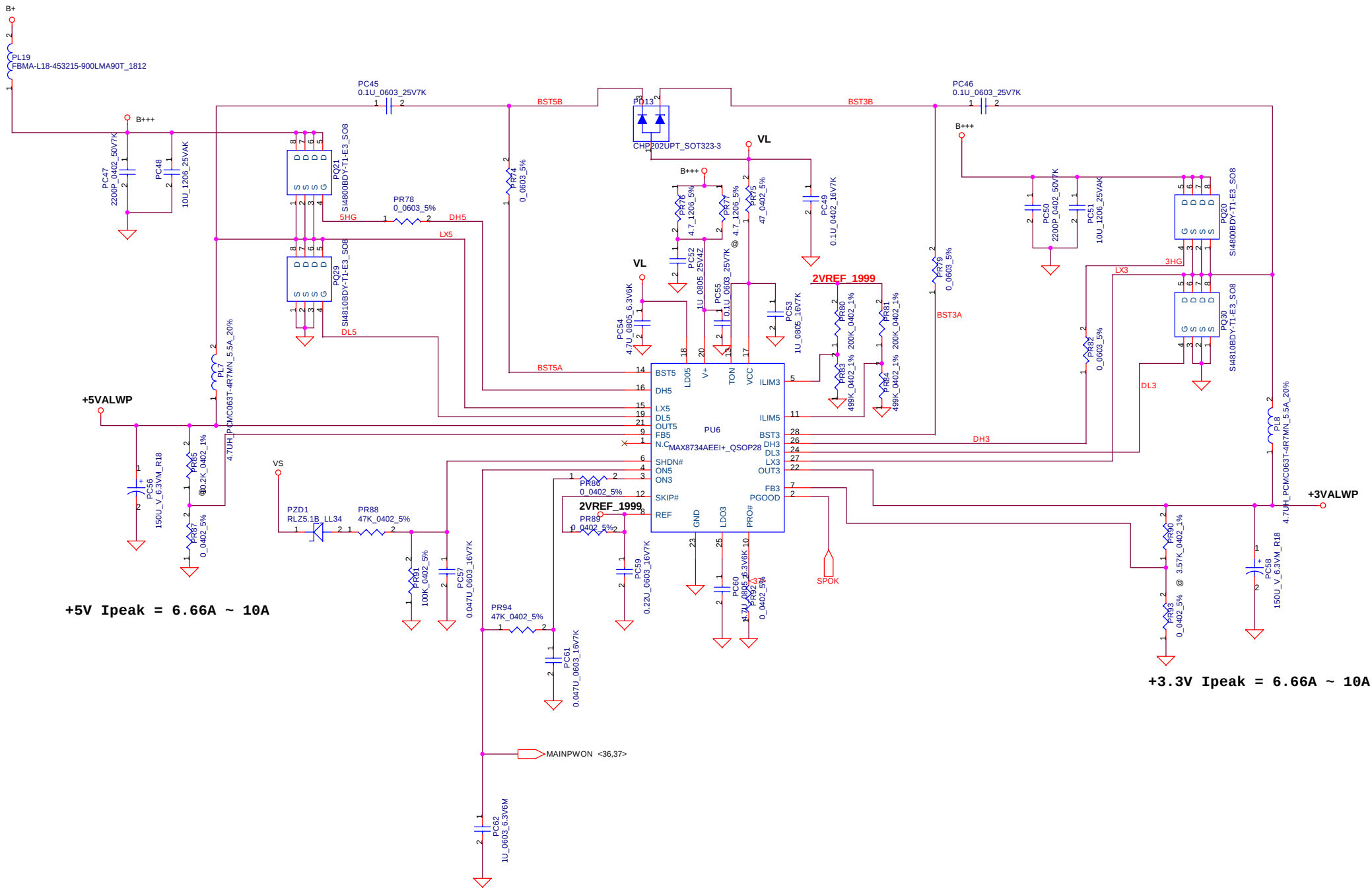
LI-3S :13.5V---BATT-OVP=1.5V
BATT-OVP=0.111*BATT+

$$\begin{aligned} CC &= 3A \\ (100K / (100K + 133K)) * 2.8V &= 1.2V \\ 1.2 / (20 * 10^{-2}) &= 3A \end{aligned}$$

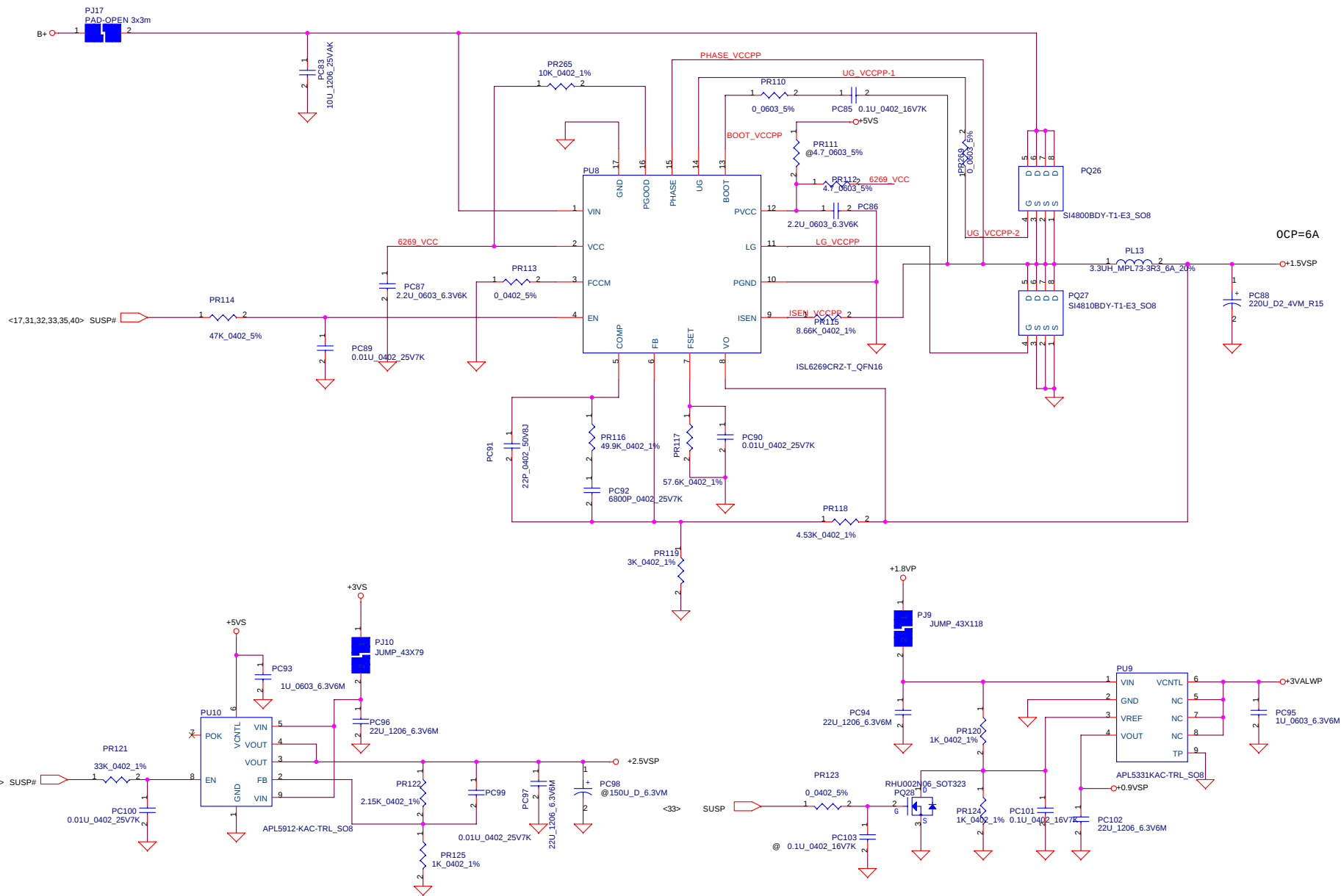
CP Point=4.3A
 $5V \cdot (10K / (28.7k + 10k)) = 1.292V$
 $1.292V / (15 \cdot 0.02) = 4.3A$

```
Charge voltage
3S CC-CV MODE : 12.6V
SEL is L
```

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				Size	Document Number	Rev
				B		0.1
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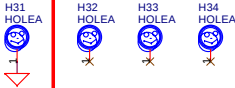
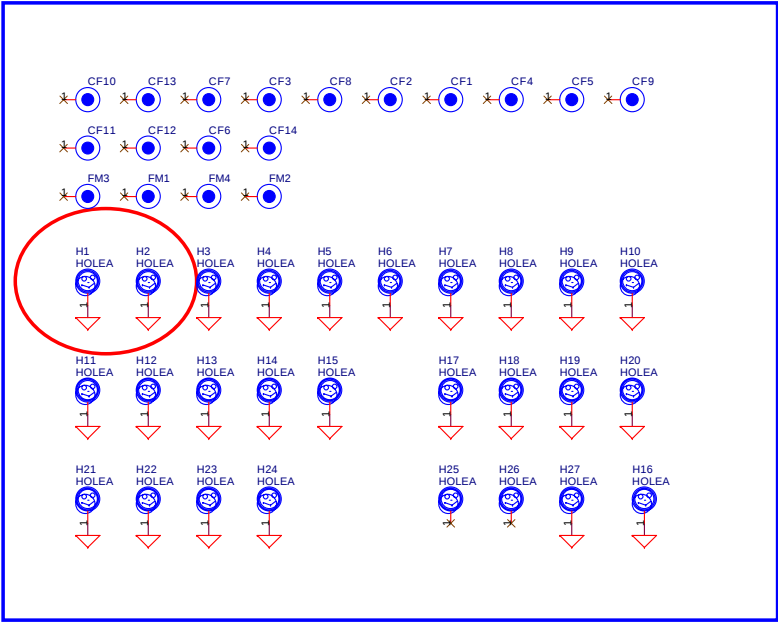


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				+5VALWP/+3VALWP	
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		Custom						0.1	
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2/13 Modified



2/13 New added

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				Date: Thursday, February 23, 2006	Sheet 43 of 43