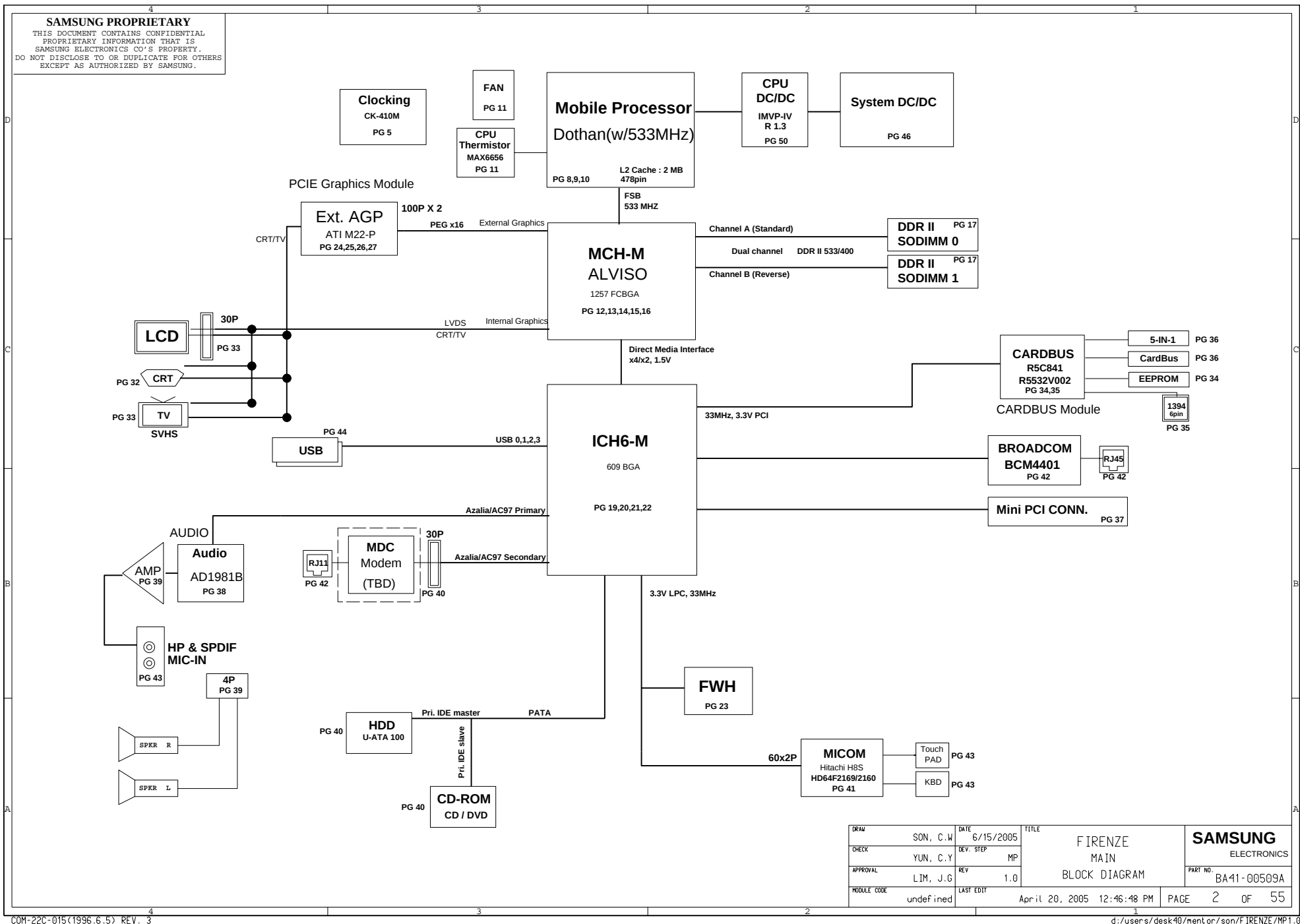


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FIRENZE																																																																																																	
CPU : Dothan533 Chip Set : ALVISO & ICH6-M Remarks : EXTERNAL GFX																																																																																																	
Model Name : FIRENZE PBA Name : MAIN PCB Code : BA41-00509A Dev. Step : MP Revision : 1.0 T.R. Date : 2005.06.07																																																																																																	
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SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

DEVICES	IDSEL#	REQ/GNT#	INTERRUPTS
CARDBUS CONTROLLER	AD25	0	A,B,C
MINIPCI	AD23	1	E,F
LAN CONTROLLER	AD21	2	G

CPU Core Voltage Table

VID5	VID4	VID3	VID2	VID1	VID0	Voltage	VID5	VID4	VID3	VID2	VID1	VID0	Voltage	
0	0	0	0	0	0	1.708 V	1	0	0	0	0	0	1.196 V	Northwood-B
0	0	0	0	0	1	1.692 V	1	0	0	0	0	1	1.180 V	(Interposer B'd)
0	0	0	0	1	0	1.676 V	1	0	0	0	1	0	1.164 V	
0	0	0	0	1	1	1.660 V	1	0	0	0	1	1	1.148 V	
0	0	0	1	0	0	1.644 V	1	0	0	1	0	0	1.132 V	
0	0	0	1	0	1	1.628 V	1	0	0	1	0	1	1.116 V	
0	0	0	1	1	0	1.612 V	1	0	0	1	1	0	1.100 V	
0	0	0	1	1	1	1.596 V	1	0	0	1	1	1	1.084 V	
0	0	1	0	0	0	1.580 V	1	0	1	0	0	0	1.068 V	
0	0	1	0	0	1	1.564 V	1	0	1	0	0	1	1.052 V	
0	0	1	0	1	0	1.548 V	1	0	1	0	1	0	1.036 V	
0	0	1	0	1	1	1.532 V	1	0	1	0	1	1	1.020 V	
0	0	1	1	0	0	1.516 V	1	0	1	0	1	0	1.004 V	
0	0	1	1	0	1	1.500 V	1	0	1	1	0	1	0.988 V	
0	0	1	1	1	0	1.484 V	1	0	1	1	1	0	0.972 V	
0	0	1	1	1	1	1.468 V	1	0	1	1	1	1	0.956 V	
0	1	0	0	0	0	1.452 V	1	1	0	0	0	0	0.940 V	
0	1	0	0	0	1	1.436 V	1	1	0	0	0	1	0.924 V	
0	1	0	0	1	0	1.420 V	1	1	0	0	1	0	0.908 V	
0	1	0	0	1	1	1.404 V	1	1	0	0	1	1	0.892 V	
0	1	0	1	0	0	1.388 V	1	1	0	1	0	0	0.876 V	
0	1	0	1	0	1	1.372 V	1	1	0	1	0	1	0.860 V	
Highest Freq.	0	1	0	1	1	1.356 V	1	1	0	1	1	0	0.844 V	Lowest Freq.
	0	1	0	1	1	1.340 V	1	1	0	1	1	0	0.828 V	
0	1	1	0	0	0	1.324 V	1	1	1	0	0	0	0.812 V	
0	1	1	0	0	1	1.308 V	1	1	1	0	0	1	0.796 V	
0	1	1	0	1	0	1.292 V	1	1	1	0	1	0	0.780 V	
0	1	1	0	1	1	1.276 V	1	1	1	0	1	1	0.764 V	
0	1	1	1	0	0	1.260 V	1	1	1	1	0	0	0.748 V	Deeper Sleep
0	1	1	1	0	1	1.244 V	1	1	1	1	0	1	0.732 V	
0	1	1	1	1	0	1.228 V	1	1	1	1	1	0	0.716 V	
0	1	1	1	1	1	1.212 V	1	1	1	1	1	1	0.700 V	

Voltage Rails

VDC	Primary DC system power supply (9 to 20V)
VCC_CORE	Core voltage for DOTHAN (0.7~1.708V)
VTT	DOTHAN/ALVISO Processor System Bus(PSB) Termination (1.05V)
GFX_CORE	MCH-M Core Voltage (off in S3-S5) ATI M24-P Core Voltage (1.0~1.2V) (off in S3-S5)
P0.9V	0.9V power rail (off in S3-S5)
P1.2V	1.2V power rail (off in S3-S5)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.5V_AUX	1.5V power rail (off in S4-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail(off in S4-S5)
P2.5V	2.5V power rail (off in S3-S5)
MICOM_P3V	3.3V always on power rail for MICOM
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V power rail (off in S4-S5)
P5V	5.0V switched power rail (off in S3-S5)
P5V_AUX	5.0V power rail (off in S4-S5)

IC / SMB Address

Devices	Address	Hex	Bus
SOUTH BRIDGE	Master	-	SMBUS Master
ADM1032(CPU Thermal Sensor)	1001 110X	9Ch	Thermal Sensor
SODIMM0	1010 0000	A0h	-
SODIMM1	1010 001X	A2h	-
CK-408 (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable

USB PORT Assign

PORT NUMBER	ASSIGNED TO
1,3	SYSTEM PORT A
0,2	SYSTEM PORT B

System Power States

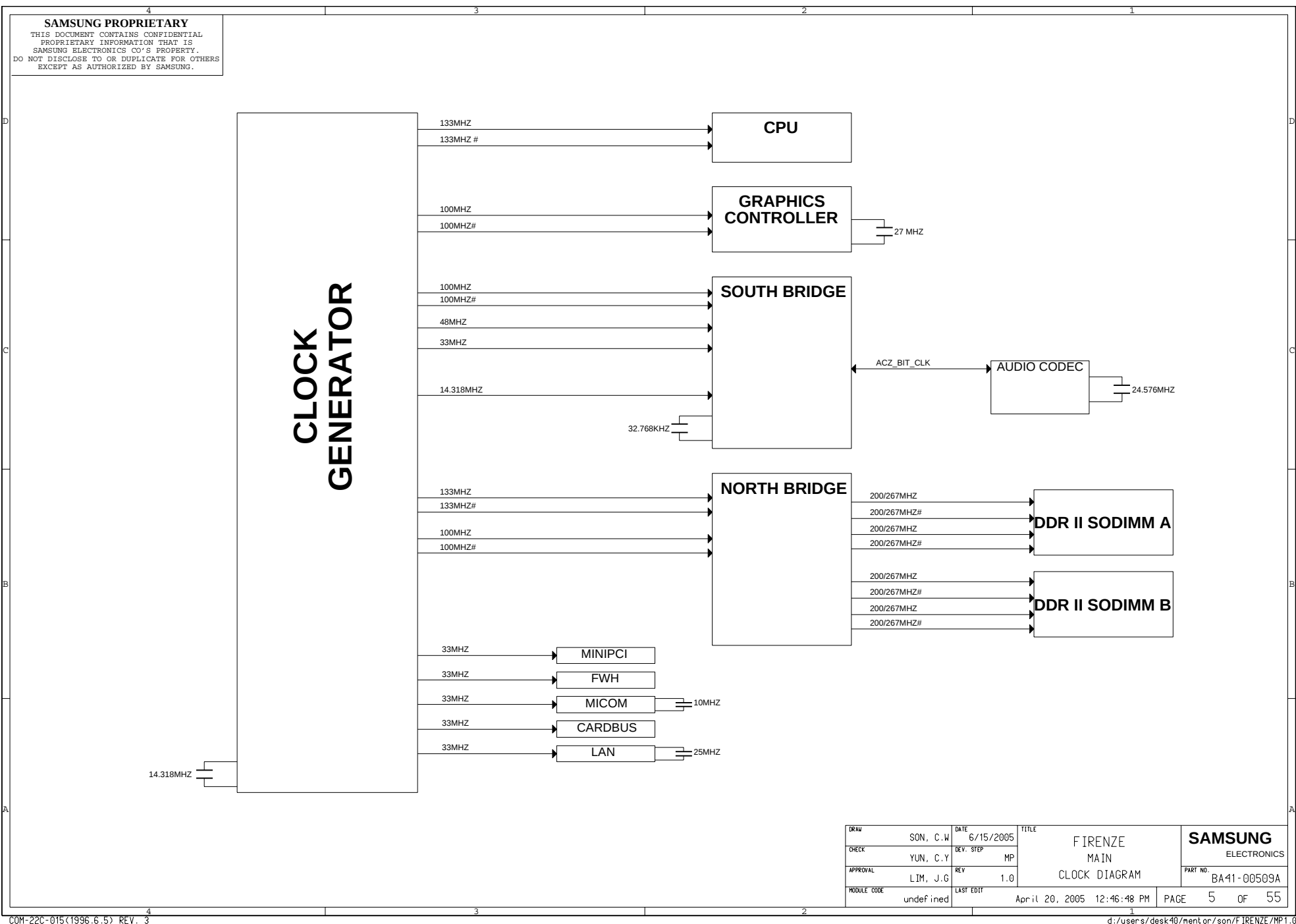
- CHP3_SLPS1* S1, Powered-On-Suspend(POS) : In this state, all clocks(except the 32.768KHz clock) are stopped. The system context is maintained in system DRAM. Power is maintained to PCI, the CPU, memory controller, memory, and all other critical subsystems. Note that this state does not preclude power being removed from non-essential devices, such as disk drives. During this state, CPU can be selected for either Deep Sleep or Deeper Sleep.
- In Deeper Sleep, CPU voltage reduced in this state to reduce the leakage power.
- CHP3_SLPS3* S3, Suspend-To-RAM(STR) : The system context is maintained in system DRAM, but power is shut off to non-critical circuits. Memory is retained, and refreshes continue. All clocks stop except RTC clock.
- CHP3_SLPS4* S4, Suspend-To-Disk(STD) : The Context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume. Externally appears same as S5, but may have different wake events.
- CHP3_SLPS5* S5, Soft Off(SOFF) : System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.

REVISION HISTORY

See rev notes in the changes file for more information.

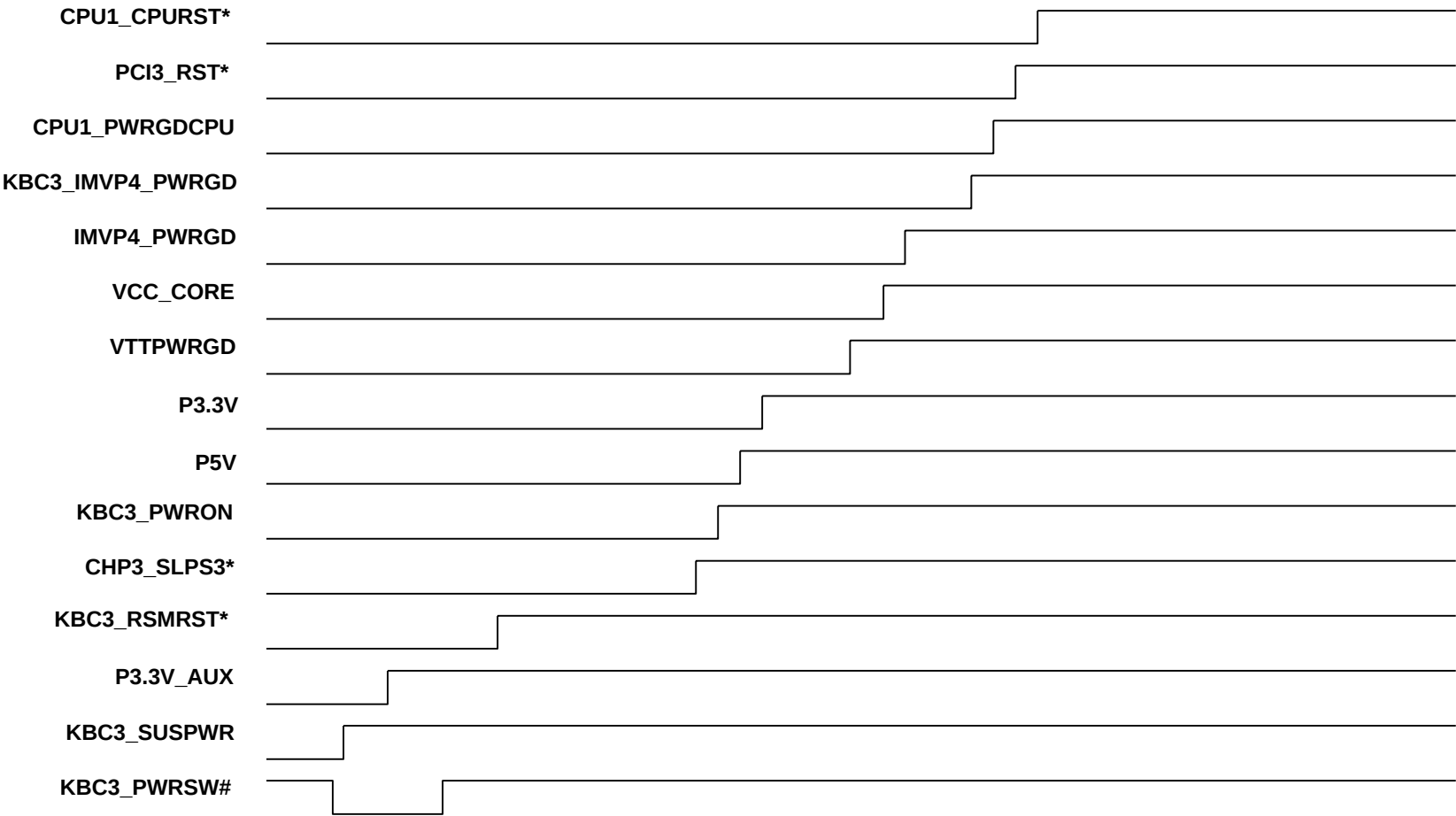
MiniPCI SLOT1

DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE MAIN BOARD INFORMATION	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	MP			PART NO. BA41-00509A
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	4	OF 55



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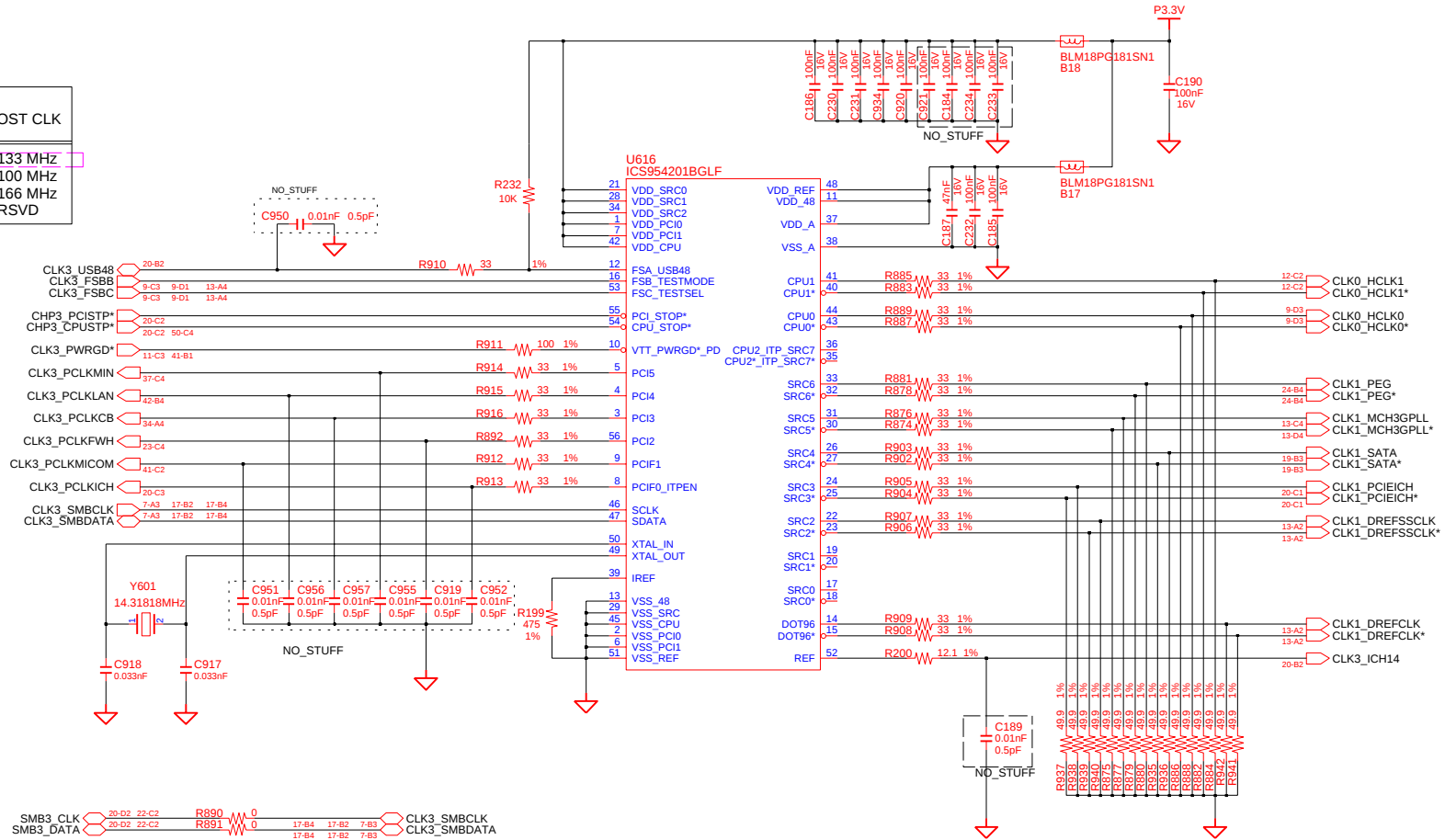
RESET DIAGRAM



DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE MAIN RESET DIAGRAM	SAMSUNG ELECTRONICS
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APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	6	OF 55

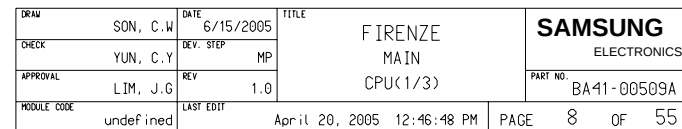
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FSA	FSB	FSC	HOST CLK
BSEL2	BSEL1	BSEL0	
1	0	0	133 MHz
1	0	1	100 MHz
1	1	0	166 MHz
1	1	1	RSVD

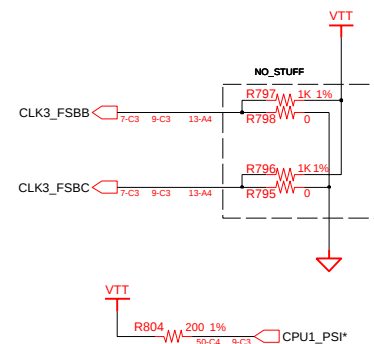


DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE MAIN CLOCK GENERATOR	SAMSUNG ELECTRONICS
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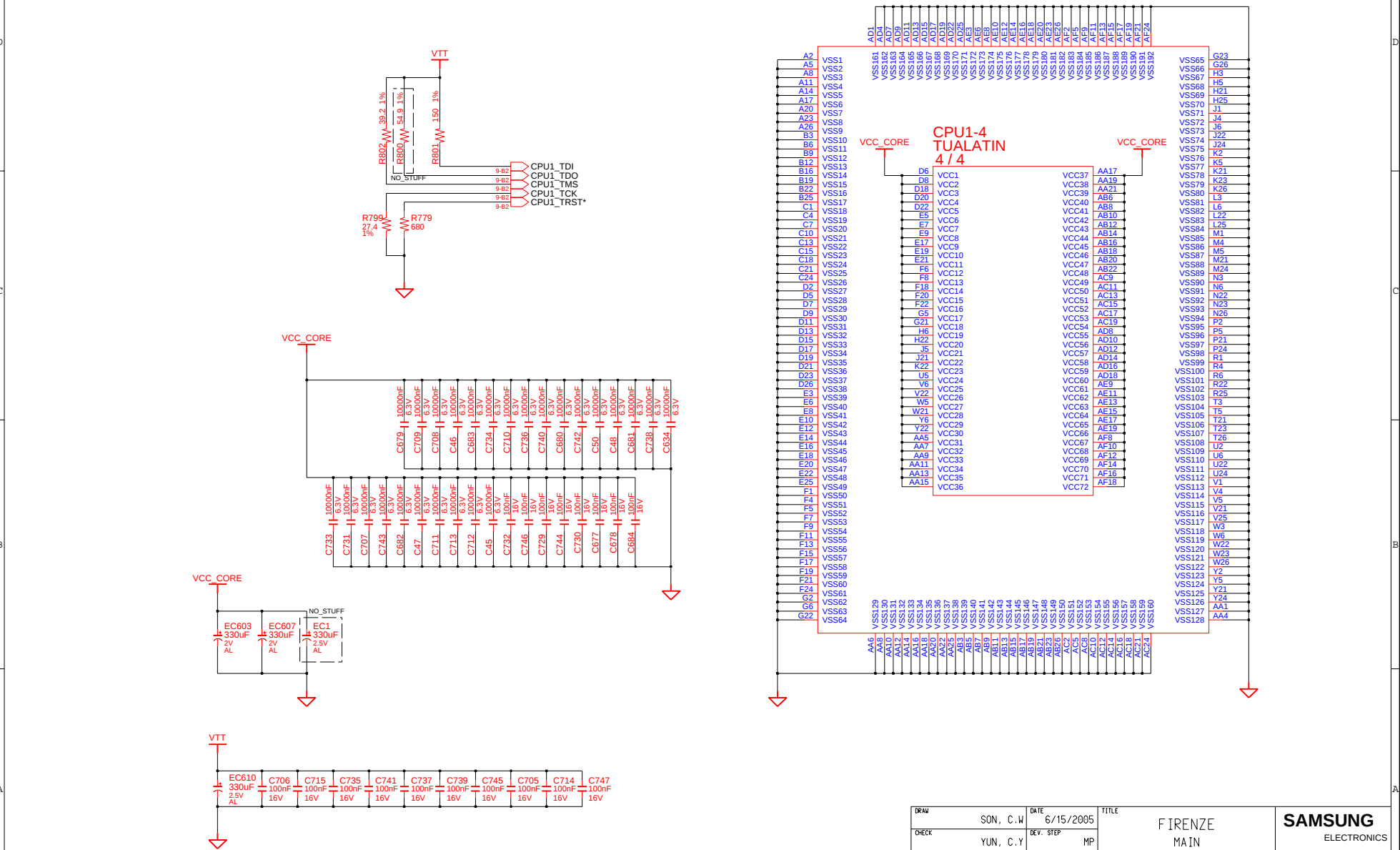


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VID(5:0)						Voltage	VID(5:0)						Voltage
0	0	0	0	0	0	1.708 V	1	0	0	0	0	1.196 V	
0	0	0	0	0	1	1.692 V	1	0	0	0	1	1.180 V	
0	0	0	0	1	0	1.676 V	1	0	0	0	0	1.164 V	
0	0	0	0	1	1	1.660 V	1	0	0	0	1	1.148 V	
0	0	0	1	0	0	1.644 V	1	0	0	1	0	1.132 V	
0	0	0	1	0	1	1.628 V	1	0	0	1	0	1.116 V	
0	0	0	1	1	0	1.612 V	1	0	0	1	1	1.100 V	
0	0	1	0	0	1	1.596 V	1	0	0	1	1	1.084 V	
0	0	1	0	0	0	1.580 V	1	0	1	0	0	1.068 V	
0	0	1	0	0	1	1.564 V	1	0	1	0	1	1.052 V	
0	0	1	0	1	0	1.548 V	1	0	1	0	1	1.036 V	
0	0	1	0	1	1	1.532 V	1	0	1	0	1	1.020 V	
0	0	1	1	0	0	1.516 V	1	0	1	1	0	1.004 V	
0	0	1	1	0	1	1.500 V	1	0	1	1	0	0.988 V	
0	0	1	1	1	0	1.484 V	1	0	1	1	1	0.972 V	
0	0	1	1	1	1	1.468 V	1	0	1	1	1	0.956 V	
0	1	0	0	0	0	1.452 V	1	1	0	0	0	0.940 V	
0	1	0	0	0	1	1.436 V	1	1	0	0	1	0.924 V	
0	1	0	0	1	0	1.420 V	1	1	0	0	0	0.908 V	
0	1	0	0	1	1	1.404 V	1	1	0	0	1	0.892 V	
0	1	0	1	0	0	1.388 V	1	1	0	1	0	0.876 V	
0	1	0	1	0	1	1.372 V	1	1	0	1	0	0.860 V	
0	1	0	1	1	0	1.356 V	1	1	0	1	1	0.844 V	
0	1	0	1	1	1	1.340 V	1	1	0	1	1	0.828 V	
0	1	1	0	0	0	1.324 V	1	1	1	0	0	0.812 V	
0	1	1	0	0	1	1.308 V	1	1	1	0	1	0.796 V	
0	1	1	0	1	0	1.292 V	1	1	1	0	1	0.780 V	
0	1	1	0	1	1	1.276 V	1	1	1	0	1	0.764 V	
0	1	1	1	0	0	1.260 V	1	1	1	1	0	0.748 V	
0	1	1	1	0	1	1.244 V	1	1	1	1	0	0.732 V	
0	1	1	1	1	0	1.228 V	1	1	1	1	1	0.716 V	
0	1	1	1	1	1	1.212 V	1	1	1	1	1	0.700 V	

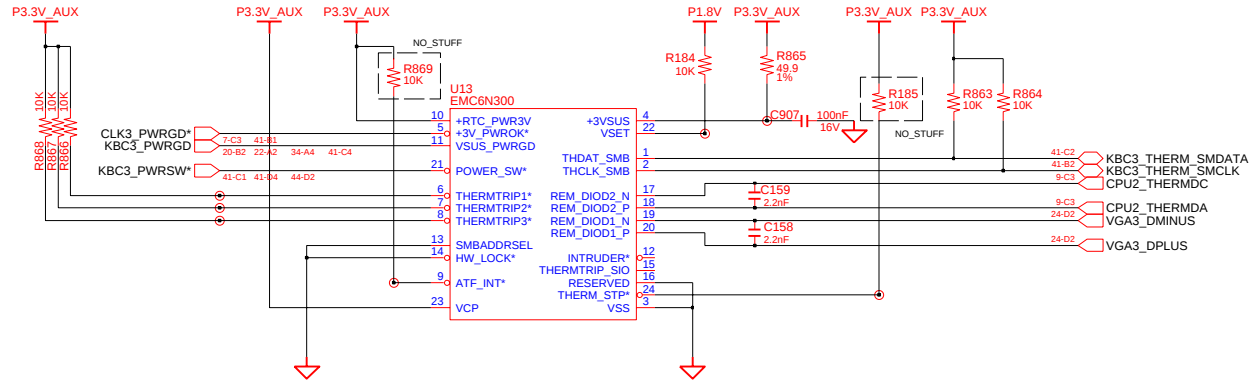
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CHECK	YUN, C.O.Y	DEV. STEP	MP				
APPROVAL	LIM, J.G	REV	1.0				
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM				PAGE



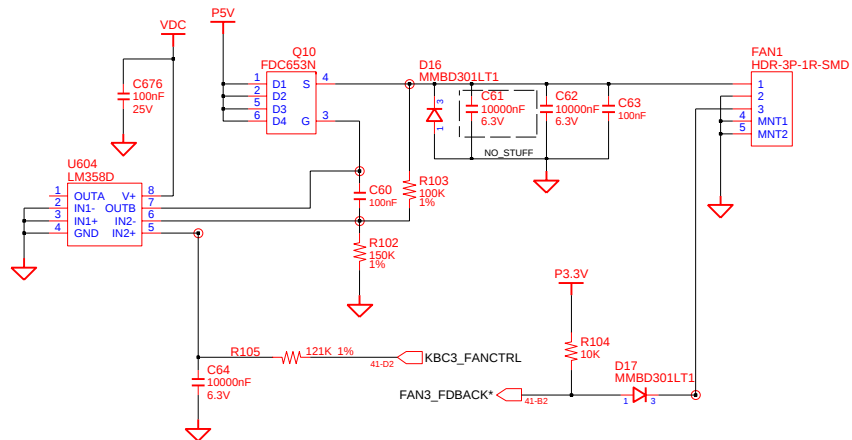
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CHECK	YUN, C.Y	DEV. STEP	MP			PART NO. BA41-00509A
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	10 OF 55	

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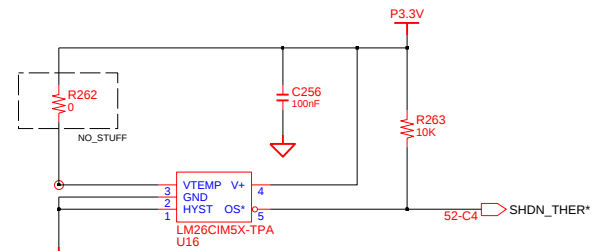
CPU/GFX Thermal Sensor



FAN CONTROL

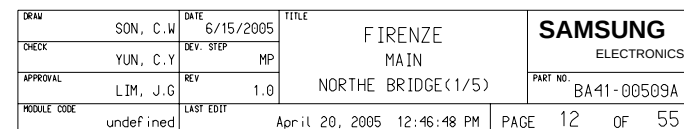


OPT CIRCUIT

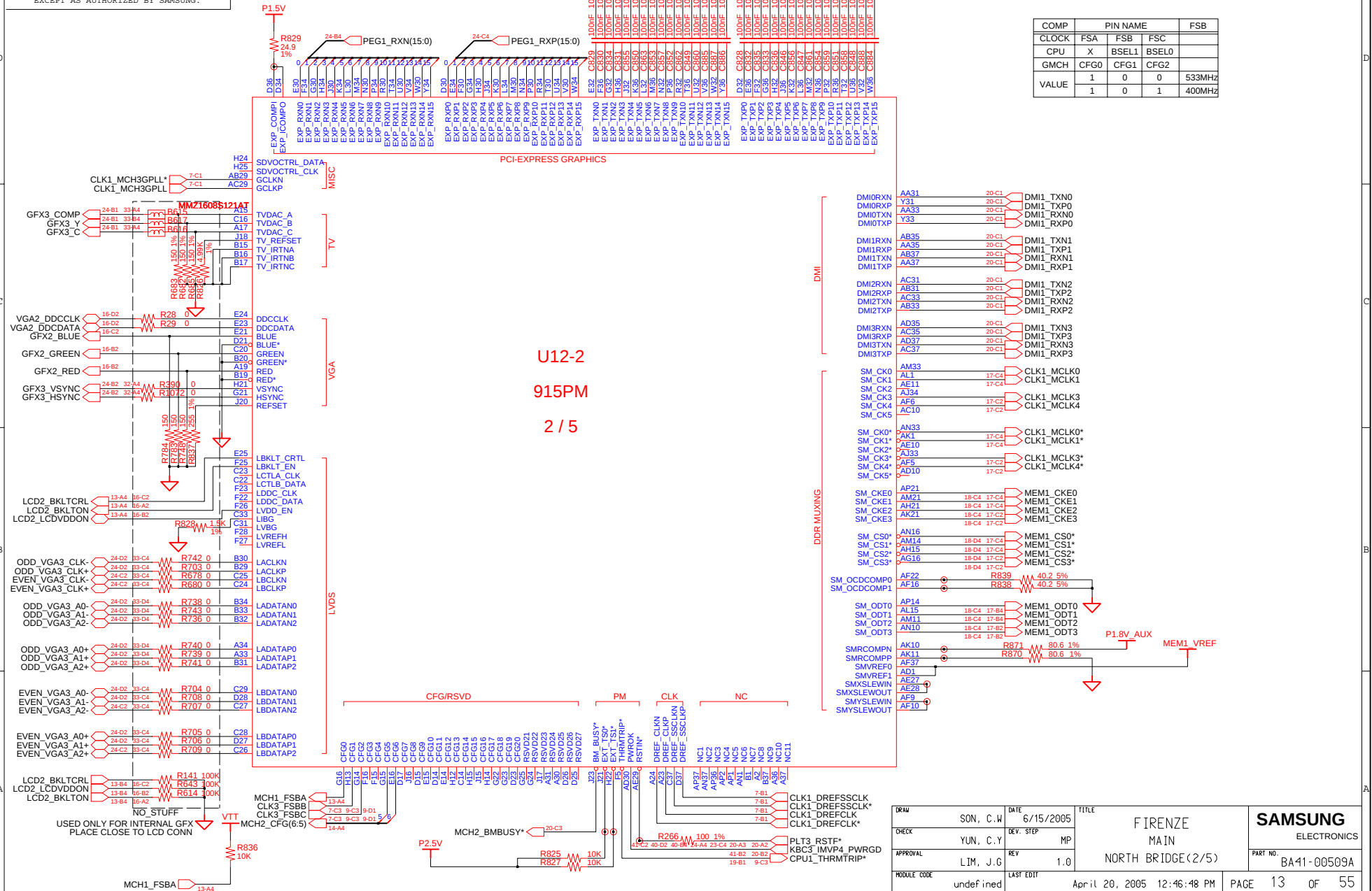


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CHECK	YUN, C.Y	DEV. STEP	MP			
APPROVAL	LIM, J.G	REV	1.0		THERMAL SENSOR/FAN CTRL	PART NO. BA41-00509A
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	11	OF 55

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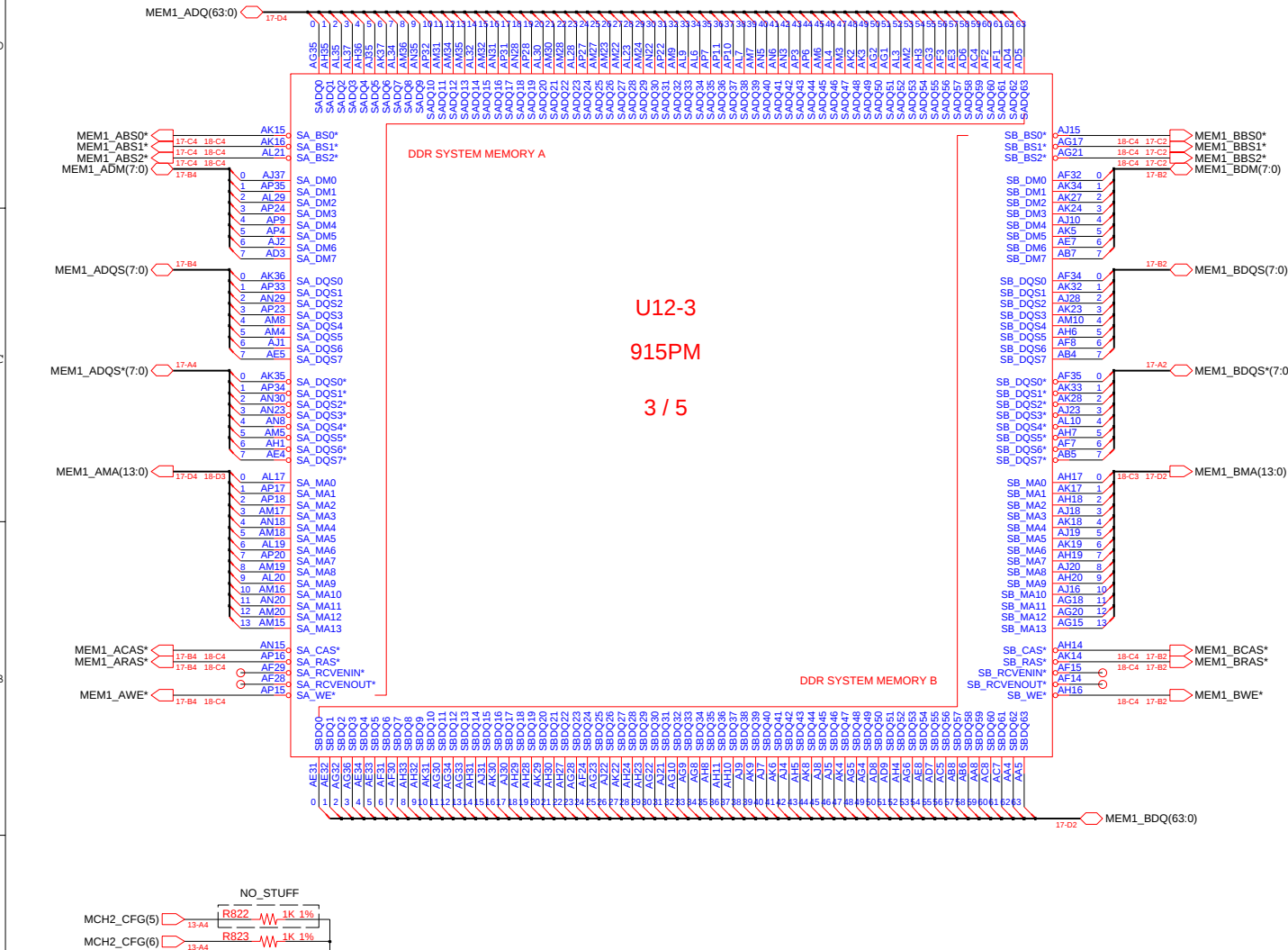
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COMP	FSA	FSB	FSC	FSB
CLOCK	X	BSEL1	BSEL0	
CPU	CFG0	CFG1	CFG2	
GMCH	CFG0	CFG1	CFG2	
VALUE	1	0	0	533MHz
	1	0	1	400MHz

DATE	6/15/2005	TITLE	FIRENZE MAIN NORTH BRIDGE(2/5)	SAMSUNG ELECTRONICS
CHECK	YUN, C. Y.	DEV. STEP	MP	PART NO. BA41-00509A
APPROVAL	LIM, J. G.	REV	1.0	
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE 13 OF 55

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DDR-II ONLY	DDR-I
SA_DQS(7:0)*	NC
SB_DQS(7:0)*	NC
SM_ODT(3:0)	NC

Dual Channel	Ch. A (So-DIMM A)	Ch. B (So-DIMM B)
SM_CK(2:0)	SA_CK(2:0)	N/A
SM_CK(2:0)*	SA_CK(2:0)*	N/A
SM_CK(5:3)	N/A	SB_CK(2:0)
SM_CK(5:3)*	N/A	SB_CK(2:0)*
SM_CS(1:0)*	SA_CS(1:0)*	N/A
SM_CKE(1:0)	SA_CKE(1:0)	N/A
SM_ODT(1:0)	SA_ODT(1:0)	N/A
SM_CS(3:2)*	N/A	SB_CS(3:2)*
SM_SKE(3:2)	N/A	SB_CKE(3:2)
SM_ODT(3:2)	N/A	SB_ODT(3:2)

SDVO Mode	PEG (SAGP) Mode
SDVOB_RED*	EXP_TXN_0
SDVO_RED	EXP_TXP_0
SDVOB_GREEN*	EXP_TXN_1
SDVOB_GREEN	EXP_TXP_1
SDVOB_BLUE*	EXP_TXN_2
SDVOB_BLUE	EXP_TXP_2
SDVOB_CLK*	EXP_TXN_3
SDVOB_CLK	EXP_TXP_3
SDVOC_RED*	EXP_TXN_4
SDVOB_ALPHA*	
SDVOC_RED	EXP_TXP_4
SDVOB_ALPHA	
SDVOC_GREEN*	EXP_TXN_5
SDVOC_GREEN	EXP_TXP_5
SDVOC_BLUE*	EXP_TXN_6
SDVOC_BLUE	EXP_TXP_6
SDVOC_CLK*	EXP_TXN_7
SDVOC_CLK	EXP_TXP_7
SDVO_TVCLKIN*	EXP_RXN_0
SDVO_TVCLKIN	EXP_RXP_0
SDVOB_INT*	EXP_RXN_1
SDVOB_INT	EXP_RXP_1
SDVO_STALLB	EXP_RXN_2
SDVO_STALL	EXP_RXP_2
SDVOC_INTB	EXP_RXN_5
SDVOC_INT	EXP_RXP_5

def. : default Option

CFG#	Low	High
CFG(5)	DMix2	DMix4 (def.)
CFG(6)	DDR-1	DDR-1
CFG(7)	DT/Transportable	Mobile CPU (def.)
CFG(9)	PEG Reversal	Normal
CFG(10)	TBD	TBD
CFG(11)	TBD	TBD
CFG(16)	Dynamic ODT Disabled	Enabled (def.)
CFG(18)	VCC 1.05V (def.)	VCC 1.5V
CFG(19)	VTT 1.05V (def.)	VTT 1.2V
SDVODTA	No (def.)	SDVO Present

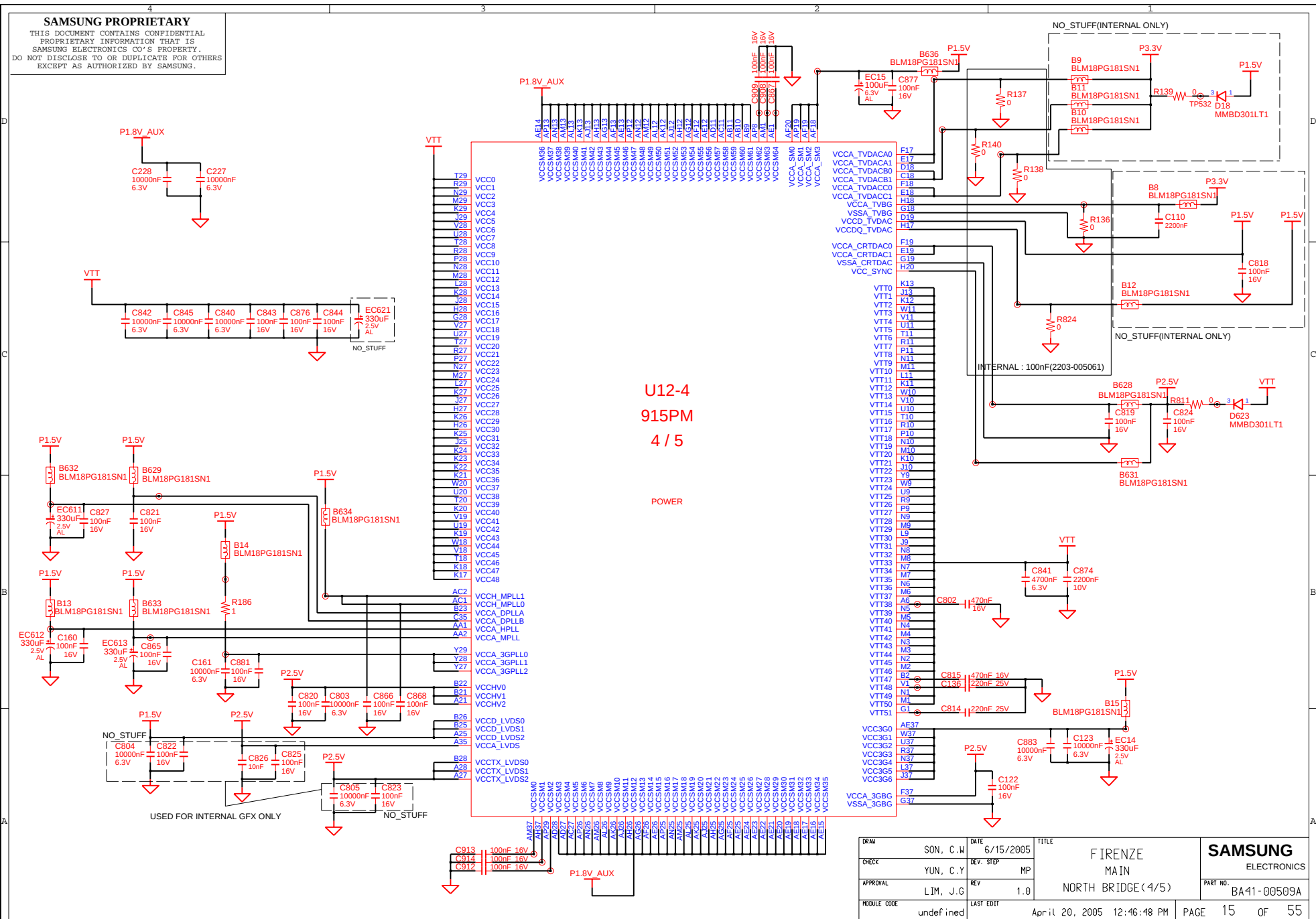
DIM x2 / x4 x4 only

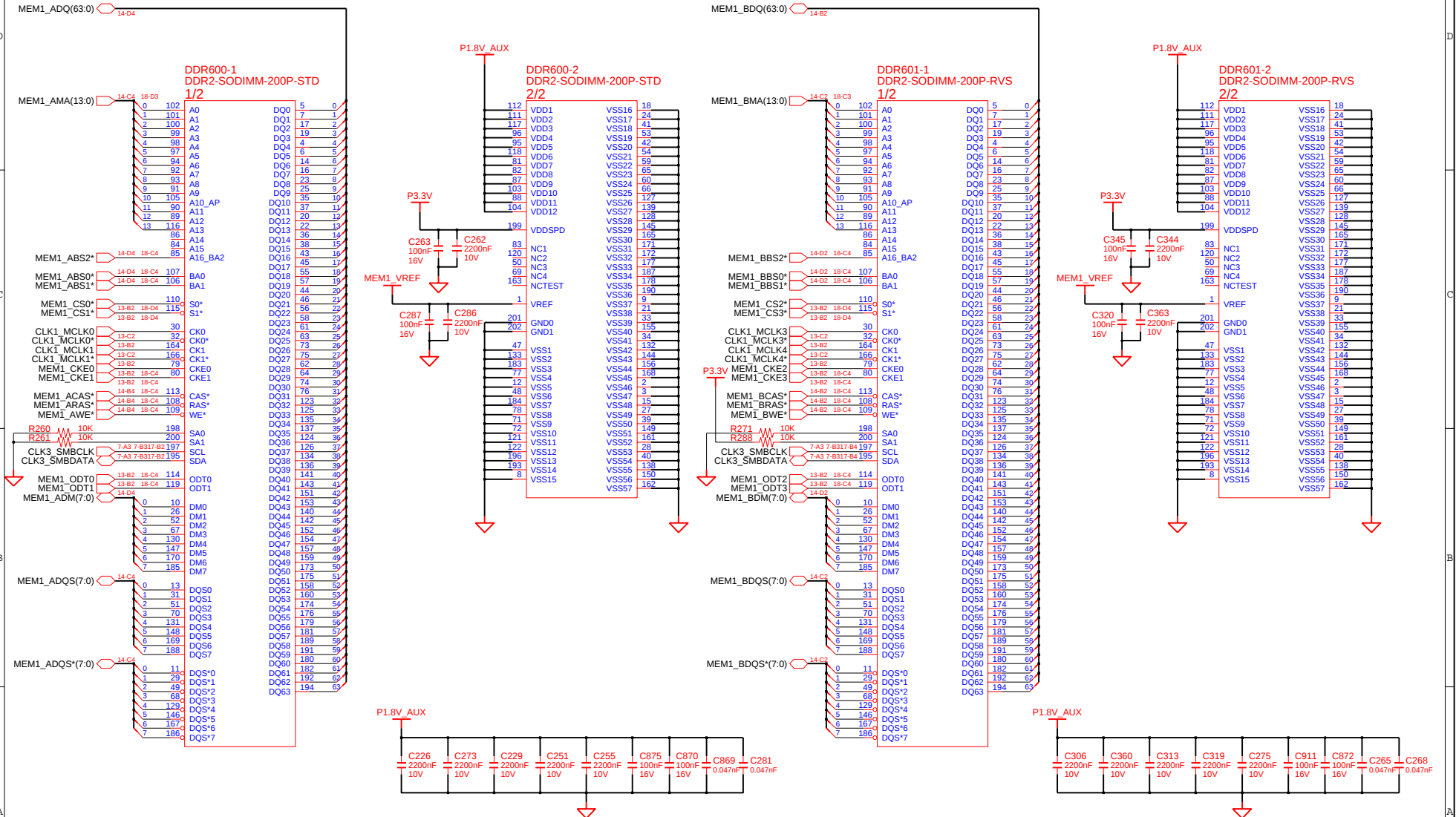
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CHECK	YUN, C.Y	DEV. STEP	MP			PART NO. BA41-00509A
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	14	OF 55

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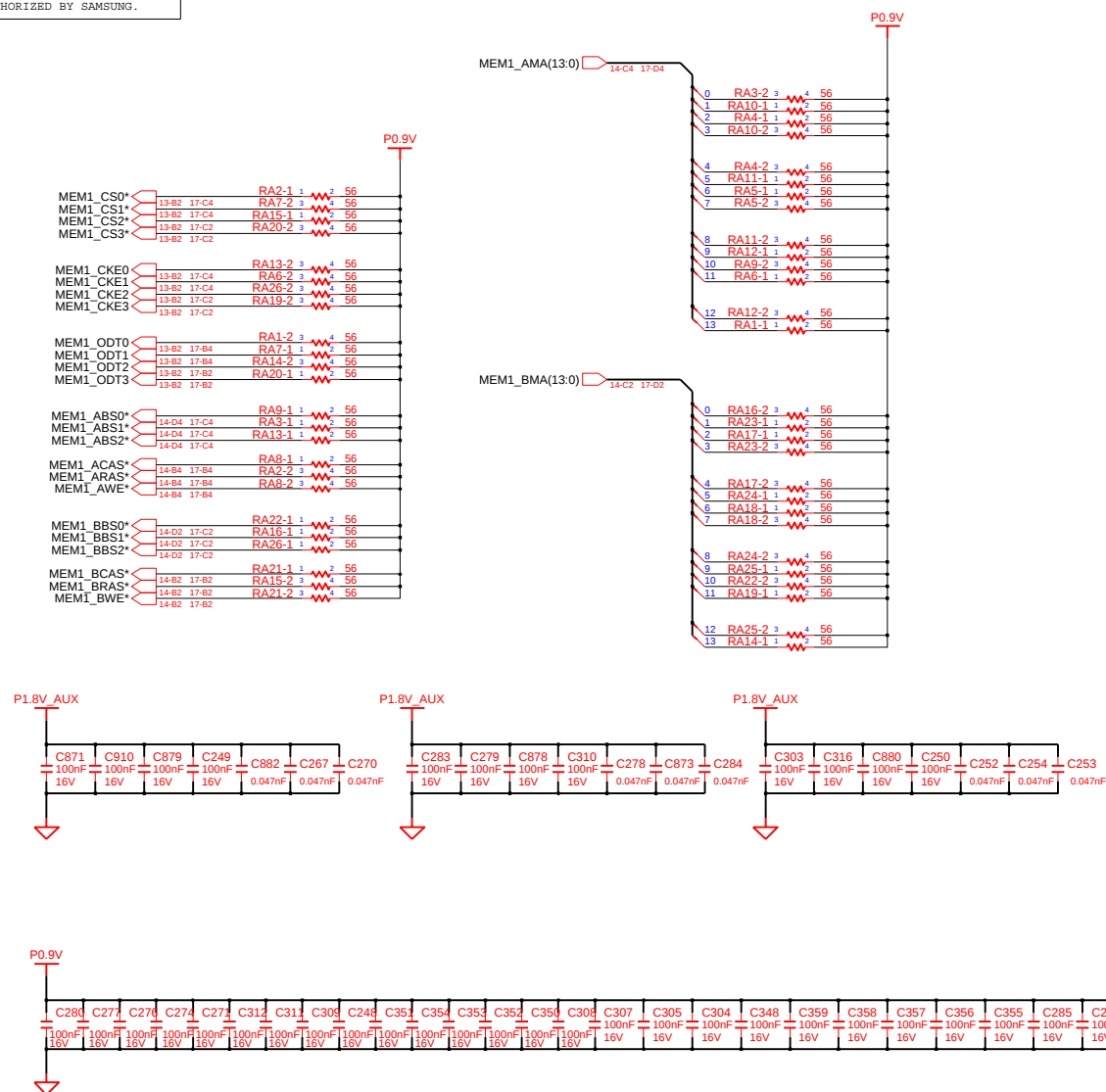
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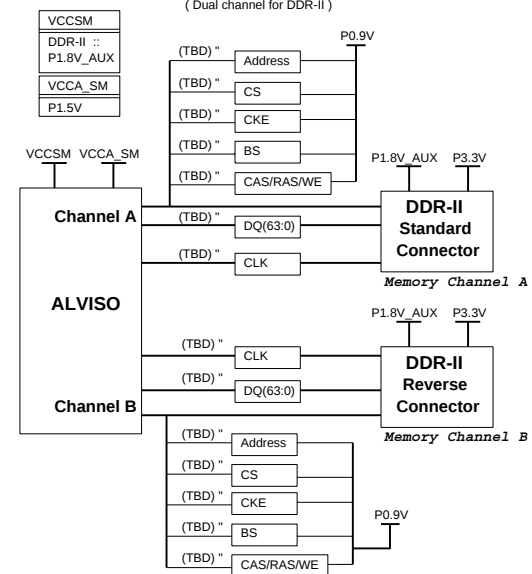
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CHECK	YUN, C.Y.	DEV. STEP	MP	MAIN	MAIN	
APPROVAL	LIM, J.G.	REV	1.0	DDR2-SODIMM		
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	17 OF 55	

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Memory Topology

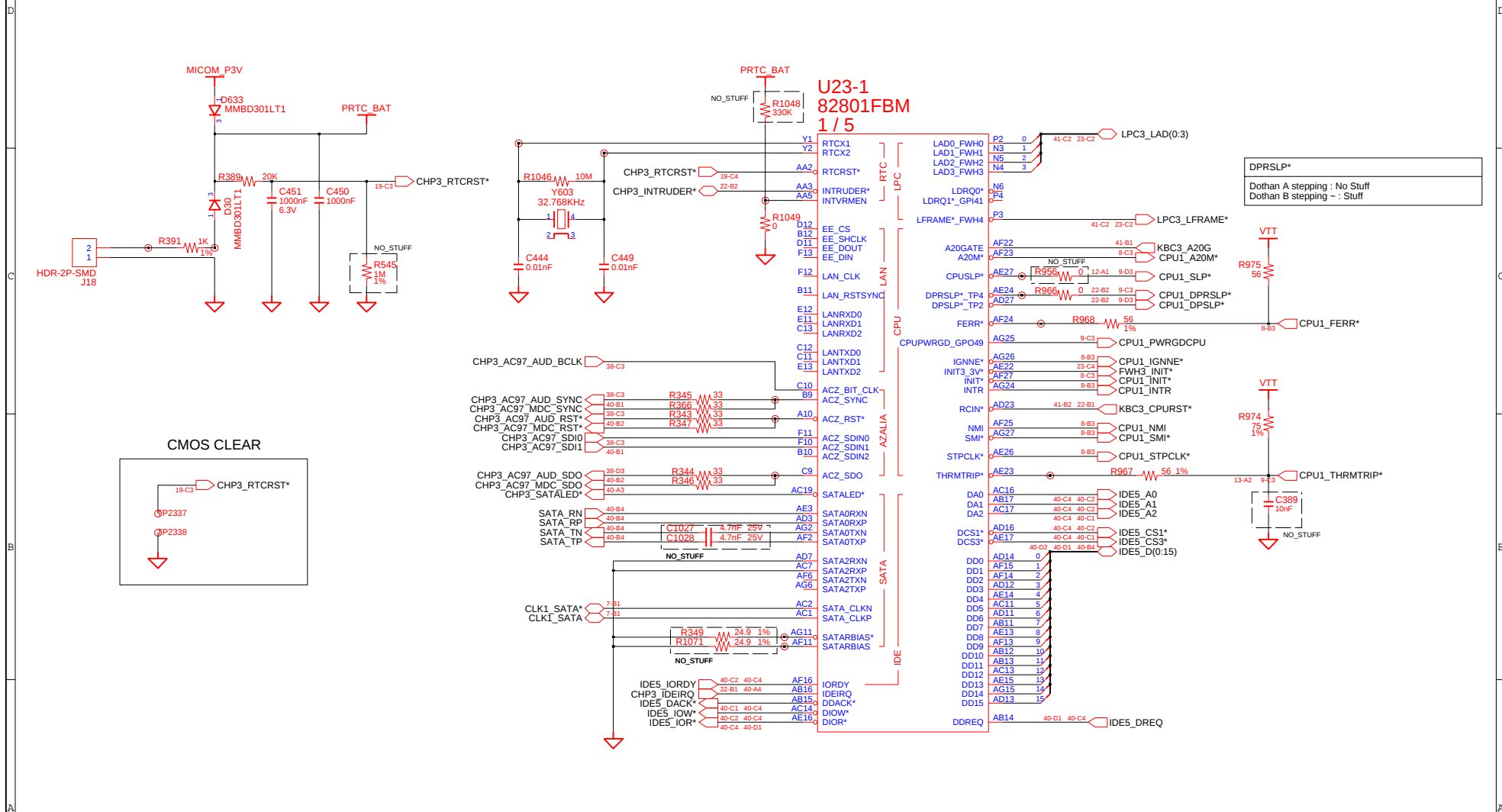
(Dual channel for DDR-II)



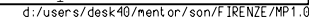
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CHECK	YUN, C. Y.					DEV. STEP	MP
APPROVAL	LIM, J. G.					REV	1.0
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	18 OF 55		

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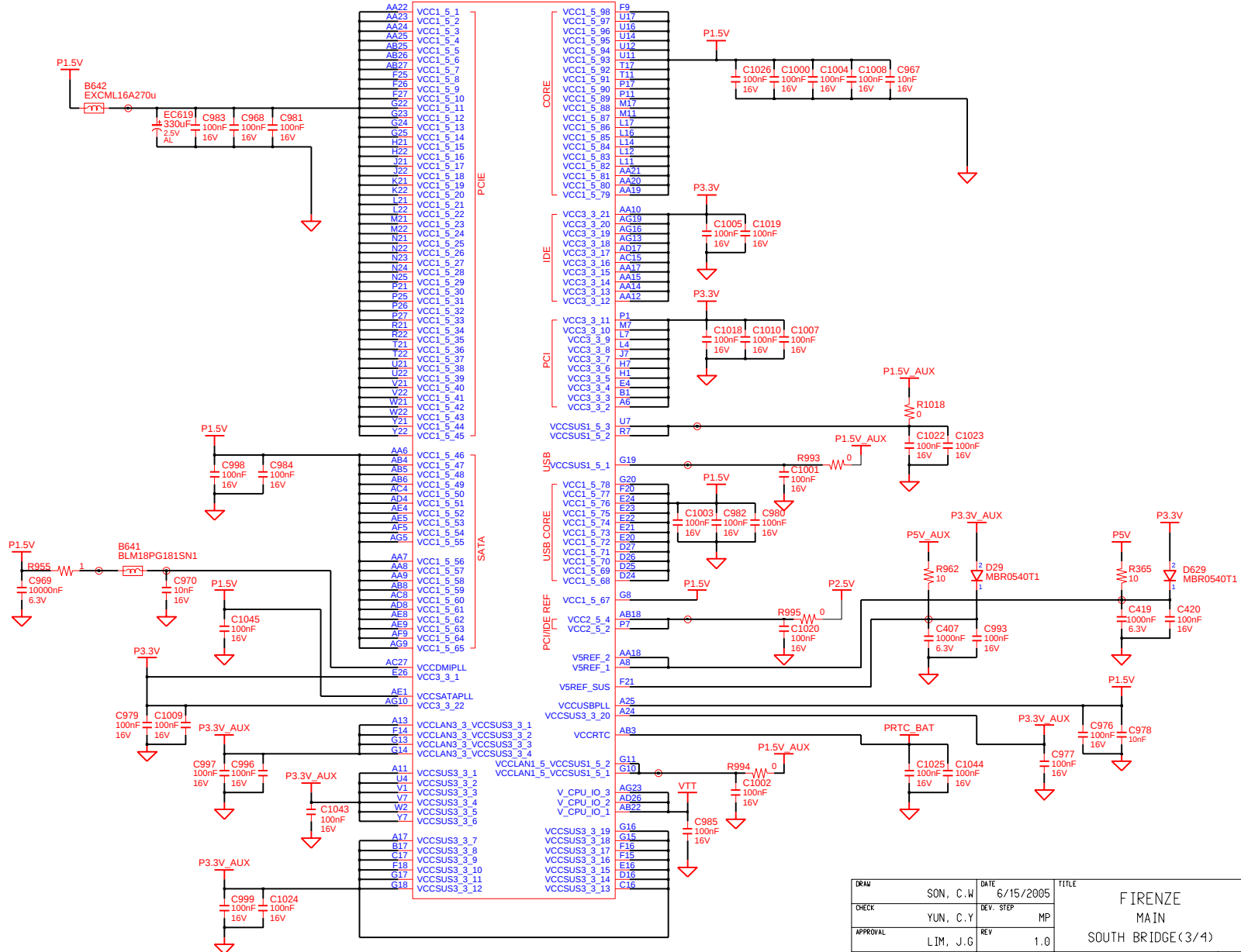
DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE	SAMSUNG
CHECK	YUN, C.Y	DEV. STEP	MP		MAIN	ELECTRONICS
APPROVAL	LIM, J.G	REV	1.0		SOUTH BRIDGE(1/4)	PART NO.
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM			BA41-00509A
				PAGE	19	OF 55



d:/users/desk40/mentor/son/FIRENZE/MP1.0

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**U23-4
82801FBM
4 / 5**

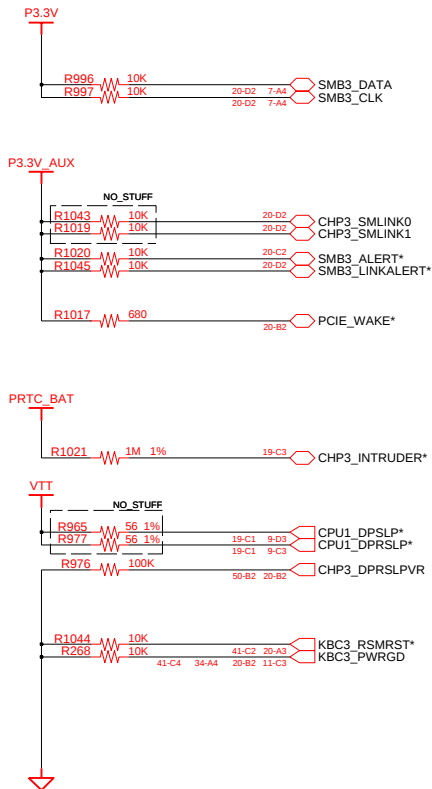


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CHECK	YUN, C.Y	DEV. STEP	MP			PART NO. BA41-00509A
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	21	OF 55

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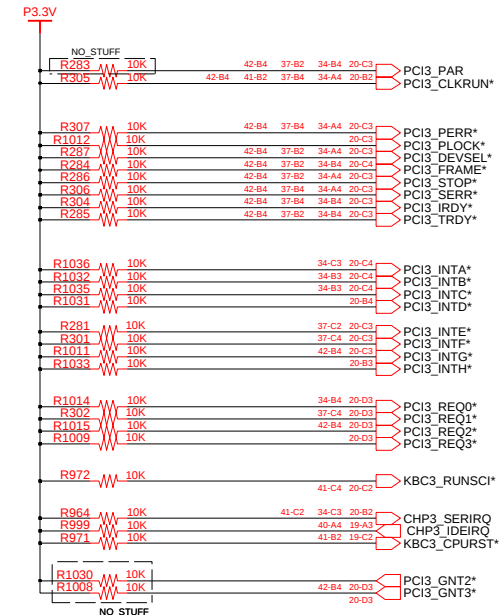
U23-5
82801FBM
5 / 5

AG22	VSS_172	VSS_86	P22
AG20	VSS_171	VSS_85	P16
AG17	VSS_170	VSS_84	P15
AG14	VSS_169	VSS_83	P14
AG12	VSS_168	VSS_82	P13
AG7	VSS_167	VSS_81	P12
AG3	VSS_166	VSS_80	N17
AG1	VSS_165	VSS_79	N16
AF26	VSS_164	VSS_78	N15
AF12	VSS_163	VSS_77	N14
AF10	VSS_162	VSS_76	N13
AF7	VSS_161	VSS_75	N12
AF3	VSS_160	VSS_74	N11
AF1	VSS_159	VSS_73	N7
AE25	VSS_158	VSS_72	N1
AE21	VSS_157	VSS_71	M27
AE12	VSS_156	VSS_70	M26
AE11	VSS_155	VSS_69	M23
AE10	VSS_154	VSS_68	M18
AE7	VSS_153	VSS_67	M16
AE6	VSS_152	VSS_66	M14
AE2	VSS_151	VSS_65	M13
AD24	VSS_150	VSS_64	M12
AD18	VSS_149	VSS_63	M4
AD15	VSS_148	VSS_62	L25
AD10	VSS_147	VSS_61	L24
AD6	VSS_146	VSS_60	L23
AD2	VSS_145	VSS_59	L22
AD1	VSS_144	VSS_58	L13
AC26	VSS_143	VSS_57	K27
AC24	VSS_142	VSS_56	K26
AC23	VSS_141	VSS_55	K23
AC22	VSS_140	VSS_54	K7
AC12	VSS_139	VSS_53	K1
AC10	VSS_138	VSS_52	J25
AC6	VSS_137	VSS_51	J24
AC3	VSS_136	VSS_50	J23
AB19	VSS_135	VSS_49	J4
AB10	VSS_134	VSS_48	H27
AB9	VSS_133	VSS_47	H26
AB7	VSS_132	VSS_46	H23
AB2	VSS_131	VSS_45	G27
AB1	VSS_130	VSS_44	G12
AA16	VSS_129	VSS_43	G9
AA13	VSS_128	VSS_42	G7
AA11	VSS_127	VSS_41	G1
AA4	VSS_126	VSS_40	F22
Y27	VSS_125	VSS_39	F19
Y26	VSS_124	VSS_38	F17
Y23	VSS_123	VSS_37	F4
Y6	VSS_122	VSS_36	E27
W25	VSS_121	VSS_35	E26
W24	VSS_120	VSS_34	E19
W23	VSS_119	VSS_33	E18
W7	VSS_118	VSS_32	E15
W1	VSS_117	VSS_31	D22
V27	VSS_116	VSS_30	D20
V26	VSS_115	VSS_29	D18
V23	VSS_114	VSS_28	D14
V4	VSS_113	VSS_27	D13
U25	VSS_112	VSS_26	D10
U24	VSS_111	VSS_25	D7
U23	VSS_110	VSS_24	D1
U15	VSS_109	VSS_23	C22
U13	VSS_108	VSS_22	C20
T27	VSS_107	VSS_21	C18
T26	VSS_106	VSS_20	C14
T23	VSS_105	VSS_19	C4
T16	VSS_104	VSS_18	B25
T15	VSS_103	VSS_17	B24
T14	VSS_102	VSS_16	B23
T13	VSS_101	VSS_15	B21
T12	VSS_100	VSS_14	B19
T7	VSS_99	VSS_13	B15
T1	VSS_98	VSS_12	B13
R25	VSS_97	VSS_11	A26
R24	VSS_96	VSS_10	A23
R23	VSS_95	VSS_9	A21
R17	VSS_94	VSS_8	A19
R16	VSS_93	VSS_7	A18
R15	VSS_92	VSS_6	A15
R14	VSS_91	VSS_5	A12
R13	VSS_90	VSS_4	A9
R12	VSS_89	VSS_3	A7
R11	VSS_88	VSS_2	A4
R4	VSS_87	VSS_1	A1



ICH6-m Strapping Options

	Function	Default
CHP3_SPKR	No Reboot	No Stuff
CHP3_BIOSWP*	Boot BIOS	No Stuff
PC/PCI_GNTA*	A16 swap override	No Stuff
AC97_SDOUT	Safe Mode	TBD
EEP_DOUT		TBD



DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	MP	MAIN	MAIN	
APPROVAL	LIM, J.G	REV	1.0	SOUTH BRIDGE(4/4)	PART NO.	
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	22 OF 55	

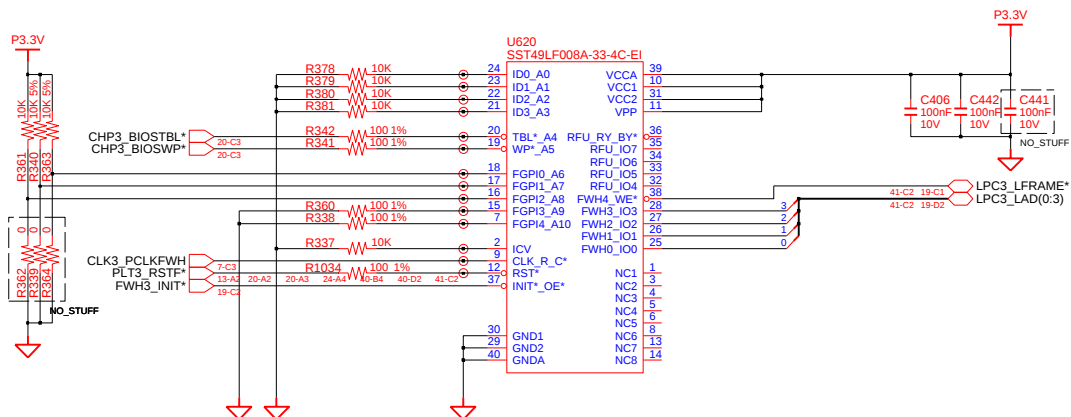
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D

C

B

A



- 02 VERIFY REAL MODE
- 03 DISABLE NMI
- 04 GET CPU TYPE
- 06 INIT. SYSTEM H/W
- 08 INIT. CHIPSET REG.
- 09 SET IN POST FLAG
- 0A INIT CPU.REG
- 0B CPU CACHE ON
- 0C INIT.CACHE TO POST
- 0E INIT. I/O VALUE
- 0F ENABLE THE L-BUS IDE
- 10 INIT. POWER MANAGER
- 11 LOAD ALTERNATE REG.
- 13 PCI BUS MASTER RESET
WITH INITIAL POST VALUE
- 14 INIT. KEYBOARD CONTROLLER
- 16 CHECK CHECKSUM
- 18 8254 TIMER INIT.
- 1A 8237 DMA CONTROLLER INIT.
- 1C RESET INTERRUPT CONTROLLER
- 20 TEST DRAM REFRESH
- 22 TEST 8742 KEYBOARD CONTROLLER
- 24 SET ES SEGMENT REG. TO 4GB
- 26 ENABLE A20
- 28 AUTO SIZING DRAM
- 32 COMPUTE THE CPU SPEED
- 34 TESET CMOS RAM
- 38 SHADOW SYSTEM BIOS ROM
- 3A AUTO SIZING CACHE
- 3C CONFIGURE ADVANCED CHIPSET REG.
- 3D LOAD ALTER REG. WITH CMOS VALUE
- 42 INIT. INTERRUPT VECTOR
- 44 INIT. BIOS INTERRUPT
- 46 CHECK ROM COPYRIGHT NOTICE
- 47 INIT. I20 SUPPORT IF INSTALLED
- 48 CHECK VIDEO CONFIGURE AGAINST CMOS
- 49 INIT. PCI BUS AND DEVICE
- 4A INIT. ALL VIDEO BIOS ROM
- 4C SHADOW VIDEO BIOS ROM
- 50 DISPLAY CPU TYPE AND SPEED
- 52 TEST KEYBOARD
- 54 SET KEYCLICK IF ENABLED
- 56 ENABLE KEYBOARD
- 58 TEST FOR UNEXPECTED INTERRUPTS
- 5A DISPLAY " PRESS SETUP"
- 5C TEST RAM BETWEEN 512K AND 640K
- 60 TEST EXTENDED MEMORY
- 62 TEST EXTENDED MEMORY ADDRESS LINE
- 64 JUMP TO USER PATCH 1

- 66 CONFIGURE ADVANCE CACHE REG.
- 6A DISPLAY EXTERNAL CACHE SIZE
- 6C DISPLAY SHADOW MESSAGE
- 6E DISPLAY NON-DISPOSABLE SEGMENT
- 70 DISPLAY ERROR MESSAGE
- 72 CHECK FOR CONFIGURATION ERROR
- 74 TEST REAL-TIME CLOCK
- 76 CHECK FOR KEYBOARD ERROR
- 7C SETUP HARDWARE INTERRUPT VECTOR
- 7E TEST COPROCESSER IF PRESENT
- 80 DISABLE ON-BOARD I/O PORT
- 82 DETECT AND INSTALL EXT.RS232C
- 84 DETECT AND INSTALL EXT.PARALLEL
- 86 RE-INIT. ON-BOARD I/O PORT
- 88 INIT. BIOS DATA ROM
- 8A INIT.EXTENDED BIOS DATA AREA
- 8C INIT. FDD CONTROLLER
- 9A SHADOW OPTION ROMS
- 9C SETUP POWER MANAGEMENT
- 9E ENABLE H/W INTERRUPT
- A0 SET TIME OF DAY
- A4 INIT. TYPEMATIC RATE
- A8 ERASE F2 PROMPT
- AA SCAN FOR F2 KEY STROKE
- AC ENTER SETUP
- AE CLEAR IN POST FLAG
- B0 CHECK FOR ERRORS
- B2 POST DONE-PREPARE TO BOOT O/S
- B4 ONE BEEP
- B6 CHECK PASSWORD (OPTION)
- B7 ACPI INIT
- BA DMI INIT
- BE CLEAR SCREEN
- C0 TRY BOOT WITH INT19
- D0 INTERRUPT HANDLER ERROR
- D2 UNKNOWN INTERRUPT ERROR
- D4 PENDING INTERRUPT ERROR
- D6 SHUTDOWN 5
- D8 SHUTDOWN ERROR
- DA EXTENDED BLOCK MOVE
- DC SHUTDOWN 10
- 89 ENABLE NMI
- 90 INIT. HDD CONTROLLER
- 91 INIT. LOCAL BUS HDD CONTROLLER
- 92 JUMP TO USER PATCH 2
- 94 DISABLE A20 ADDRESS LINE
- 96 CLEAR HUGE ES SEGMENT REG.
- 98 SEARCH FOR OPTION ROMS

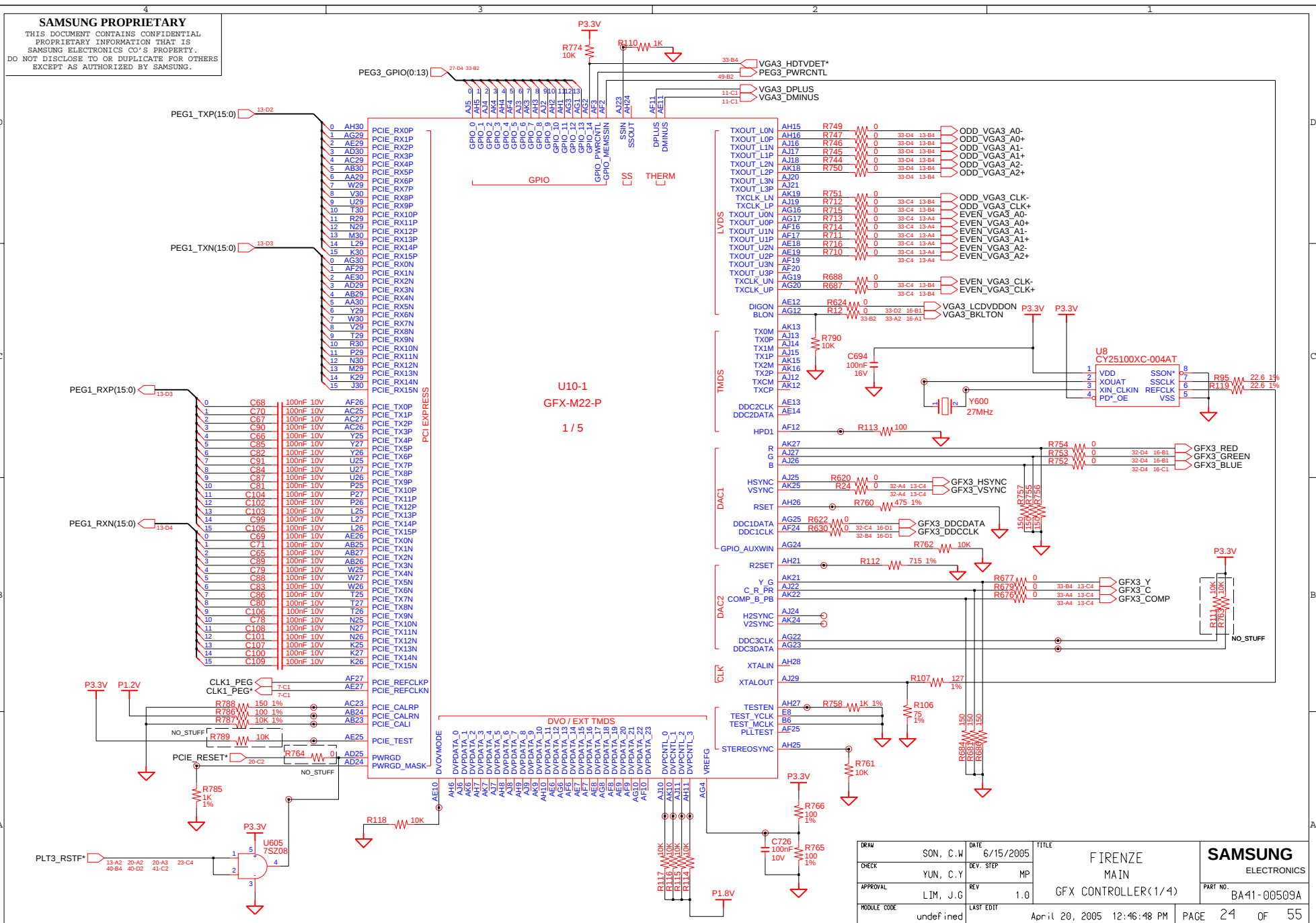
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C

B

A

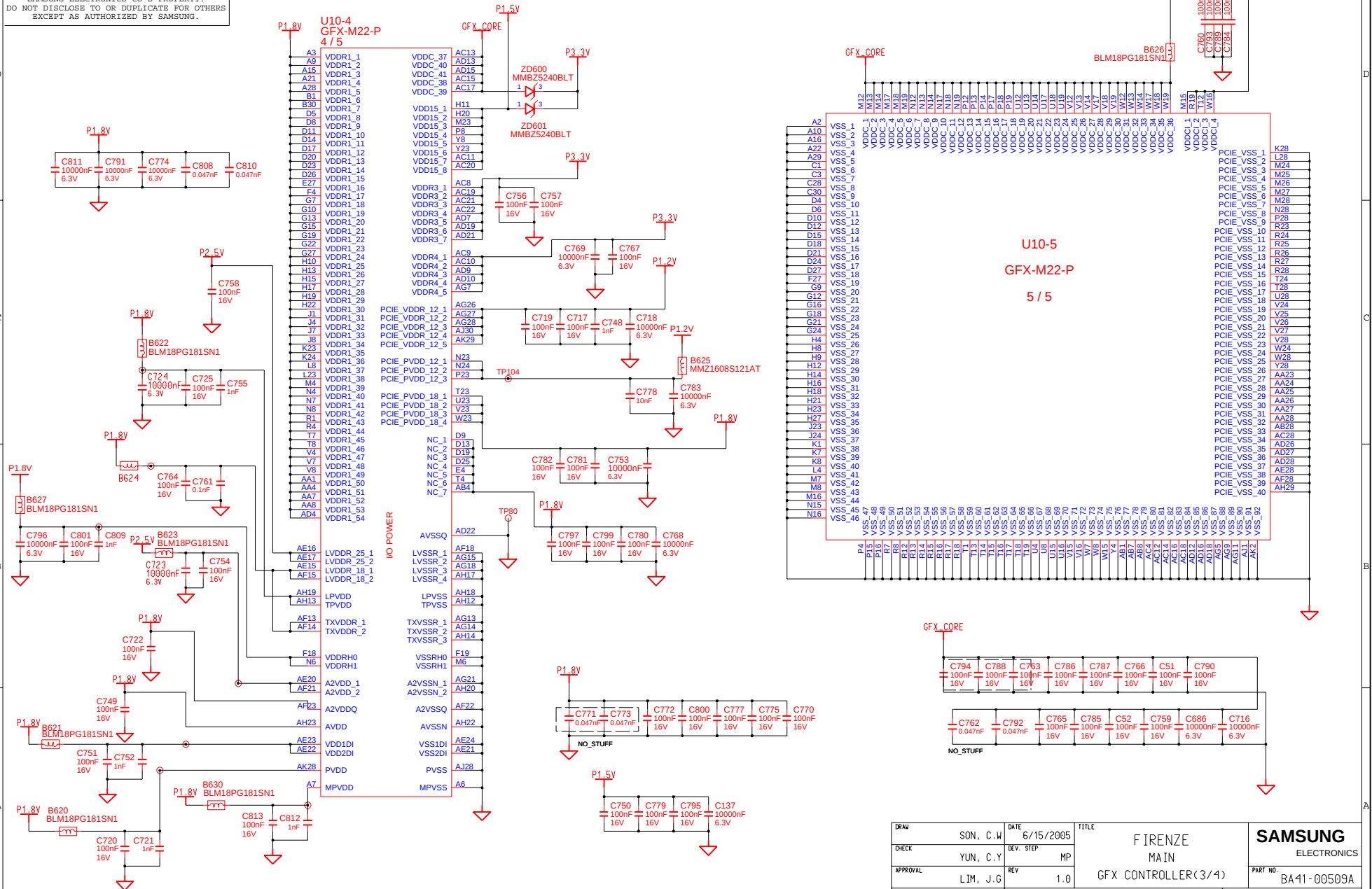
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CHECK	YUN, C.Y	DEV. STEP	MP		MAIN	ELECTRONICS
APPROVAL	LIM, J.G	REV	1.0		FWH	PART NO.
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	23	BA41-00509A
				OF	55	



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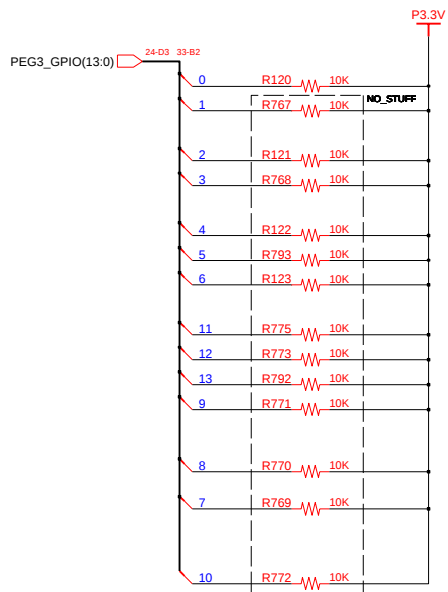


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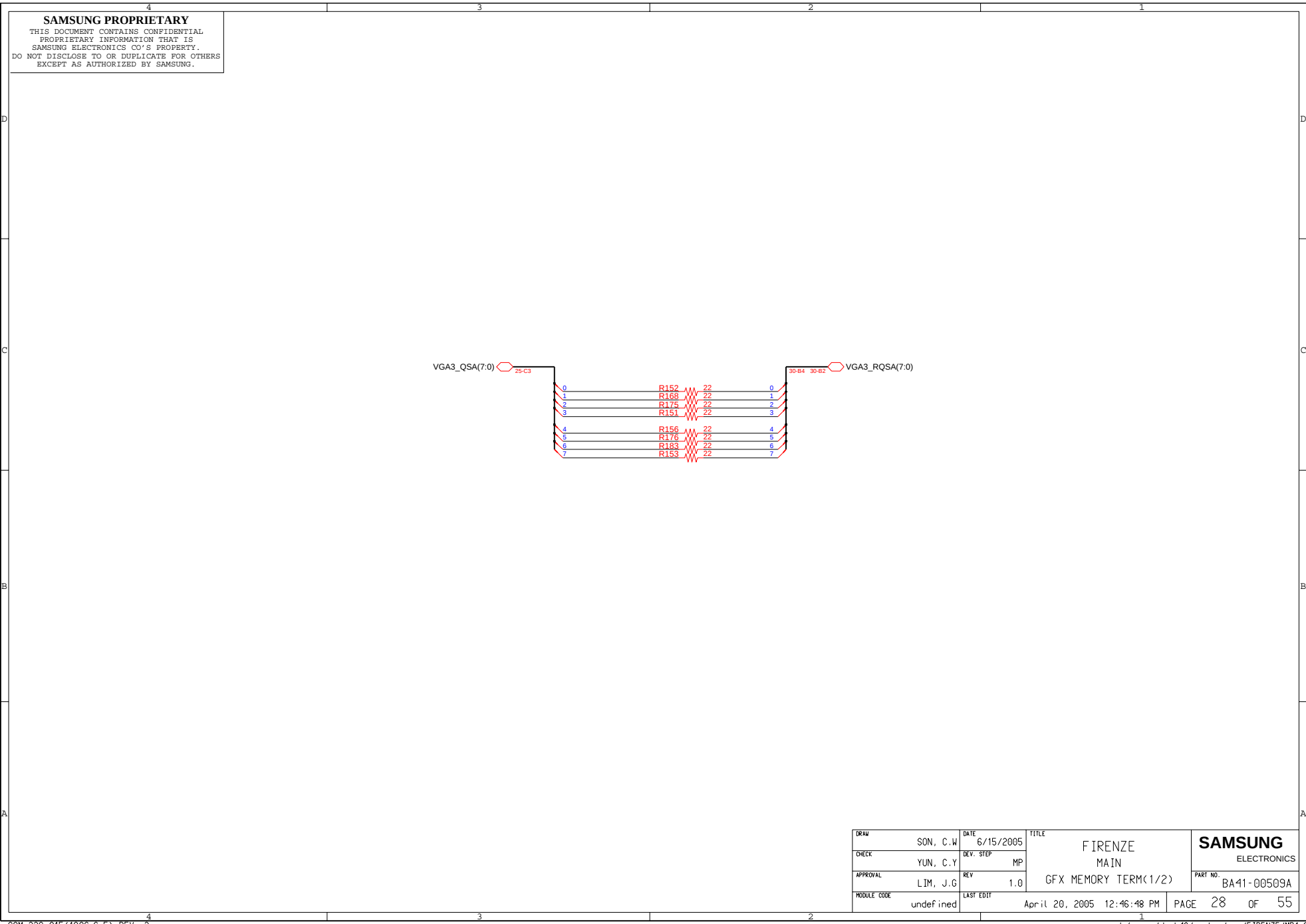
DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE MAIN GFX CONTROLLER(3/4)	SAMSUNG ELECTRONICS PART NO. BA41-00509A
CHECK	YUN, C.Y	DEV. STEP	MP			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	26 OF 55	

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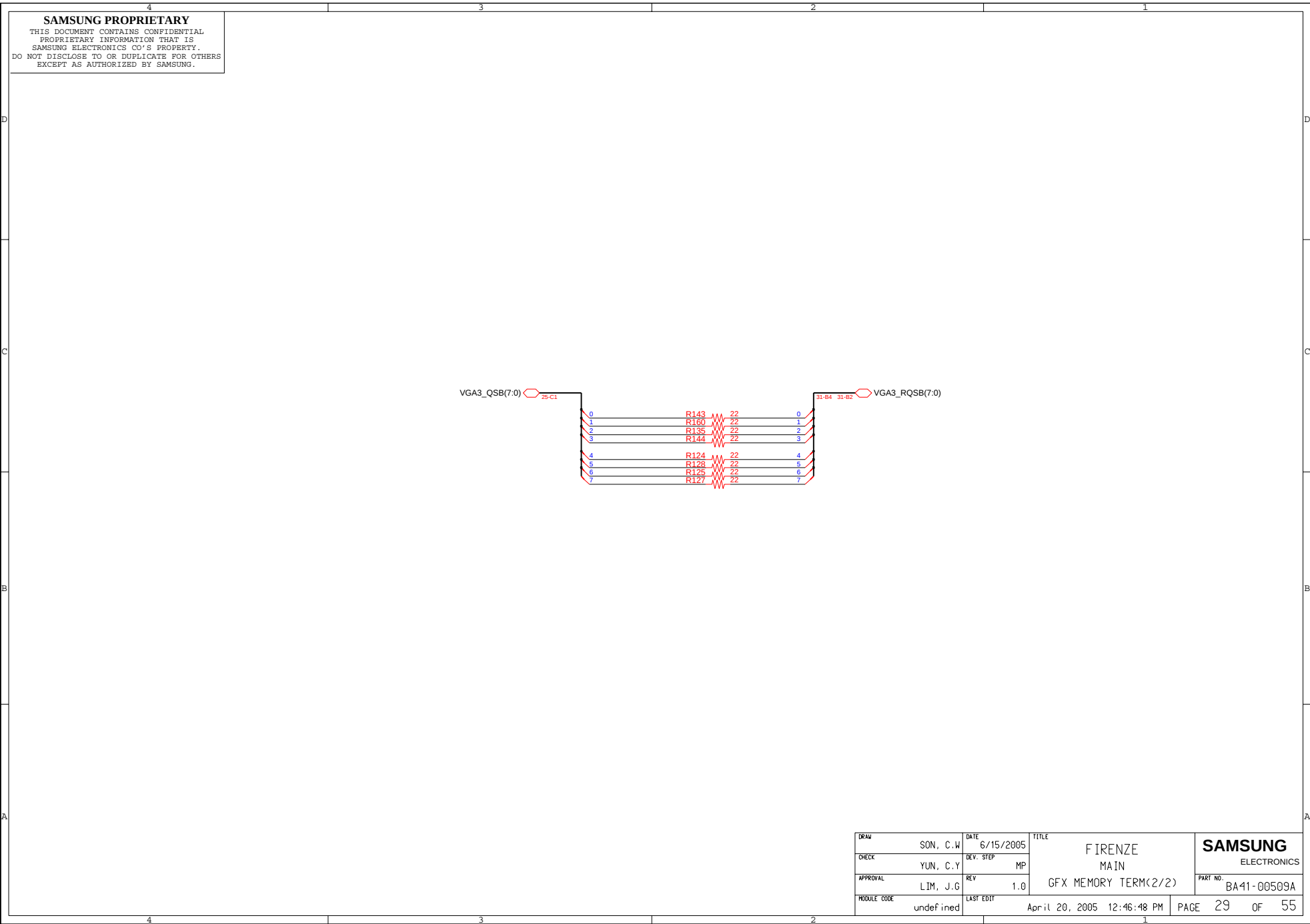


Straps	Pin Number	Descriptions
CAL_BG_BACKUP	GPIO0	PCI-Express Current Calibration Bandgap Backup 0 : use reference voltage from bandgap (Default) 1: use reference voltage from resistor divider
PLL_CAL_FORCE_EN	GPIO1	PCI-Express PLL Calibration Force Enable 0: Disable PLL force calibration (Default) 1 : Enable PLL force calibration
PCIE Mode(1:0)	GPIO(3:2)	PCI-Express Mode 00 : PCI Express 1.0A mode (Default) 01 : Reserved 10 : PCI Express 1.0 mode 11 : Reserved
CAL_OFF	GPIO4	Turn-Off PCI-Express Impedance / Strength Calibration 0 : Enable (Default) 1 : Disable Also, used to demux VCOREF / CALREF
BYPASS_PLL	GPIO5	Bypass PCI-Express PLL 0 : - (Default) 1 : -
ICOMP	GPIO6	PCI-Express Transmitter Current Compensation 0 : Normal (Default) 1: Inject extra current for output buffer switching
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, controls chip IDs. 0000 : No ROM, CHG_ID = 0 0001 : No ROM, CHG_ID = 1 0100 : Reserved 0110 : Reserved Others : ROM (Third party vendors)
DEBUG_ACCESS	GPIO8	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible.

DRAW	SON, C.W	DATE	6/15/2005	TITLE FIRENZE MAIN GFX CONTROLLER(4/4)		SAMSUNG ELECTRONICS	
CHECK	YUN, C.Y	DEV. STEP	MP				
APPROVAL	LIM, J.G	REV	1.0				
MODULE CODE		LAST EDIT		April 20, 2005 12:46:48 PM	PAGE	27	OF 55

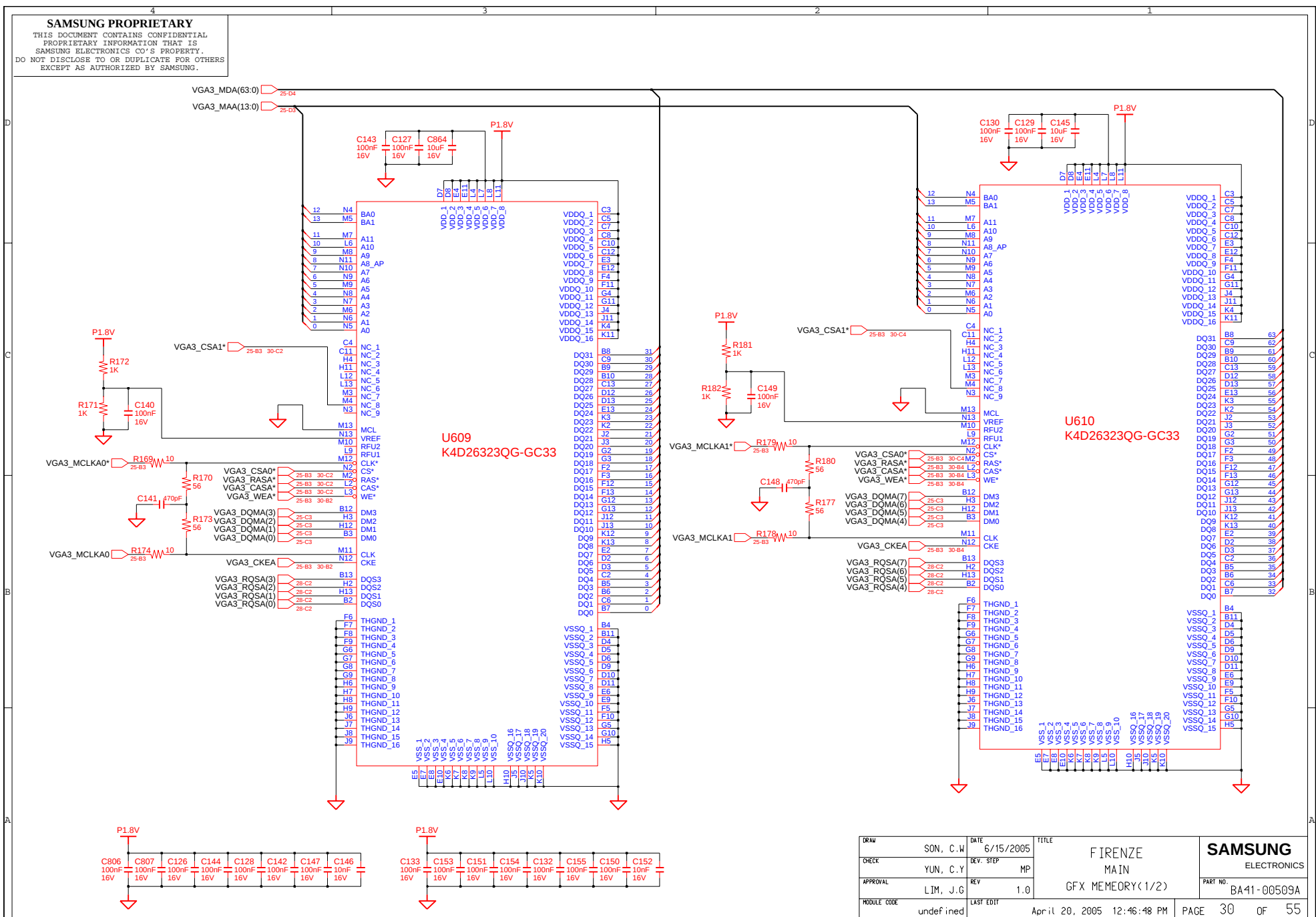


DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	MP	MAIN		
APPROVAL	LIM, J.G	REV	1.0	GFX MEMORY TERM(1/2)	PART NO. BA41-00509A	
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE 28 OF 55		

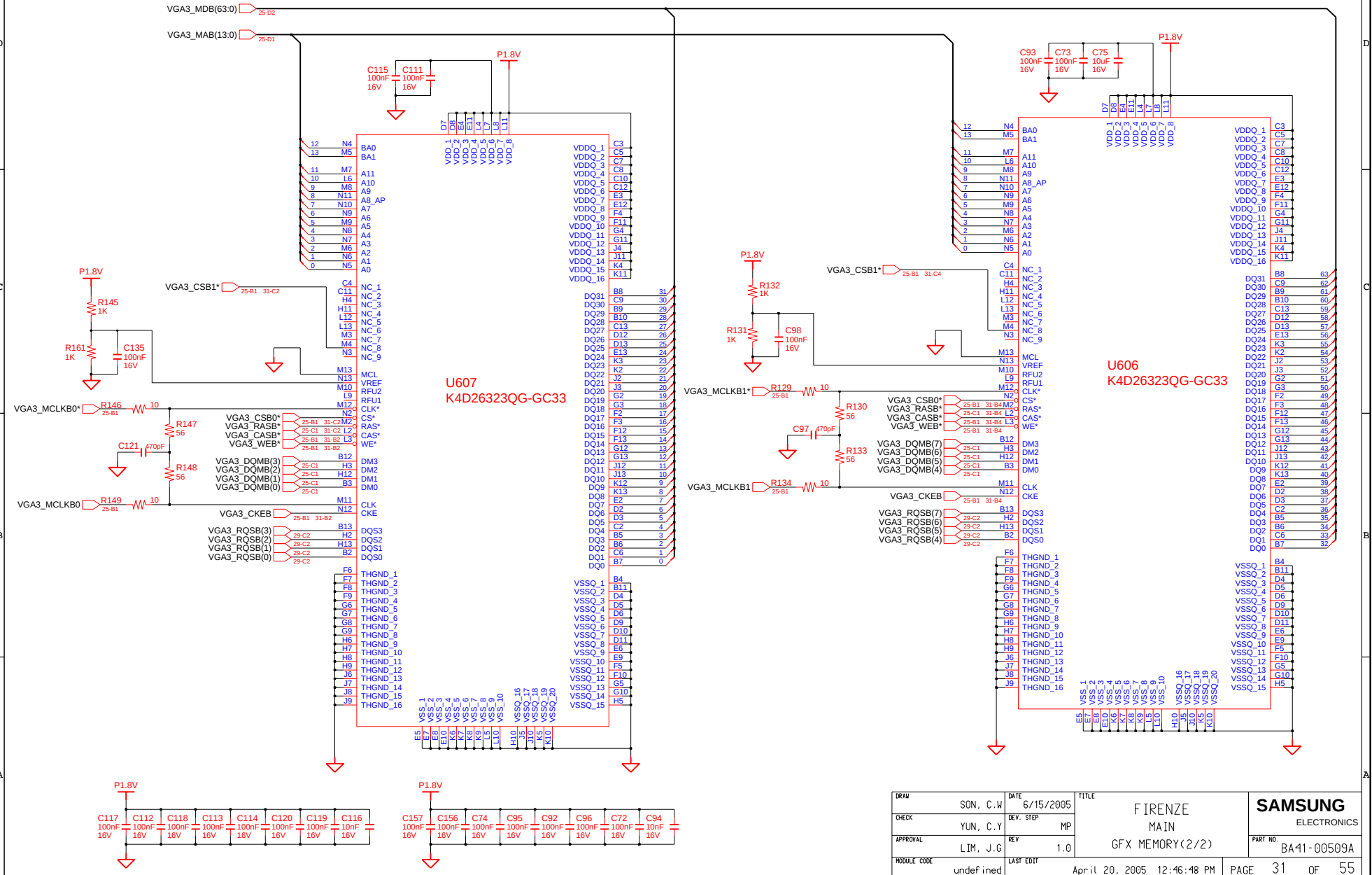


DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	MP	MAIN		
APPROVAL	LIM, J.G	REV	1.0	GFX MEMORY TERM(2/2)	PART NO. BA41-00509A	
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	29 OF 55	

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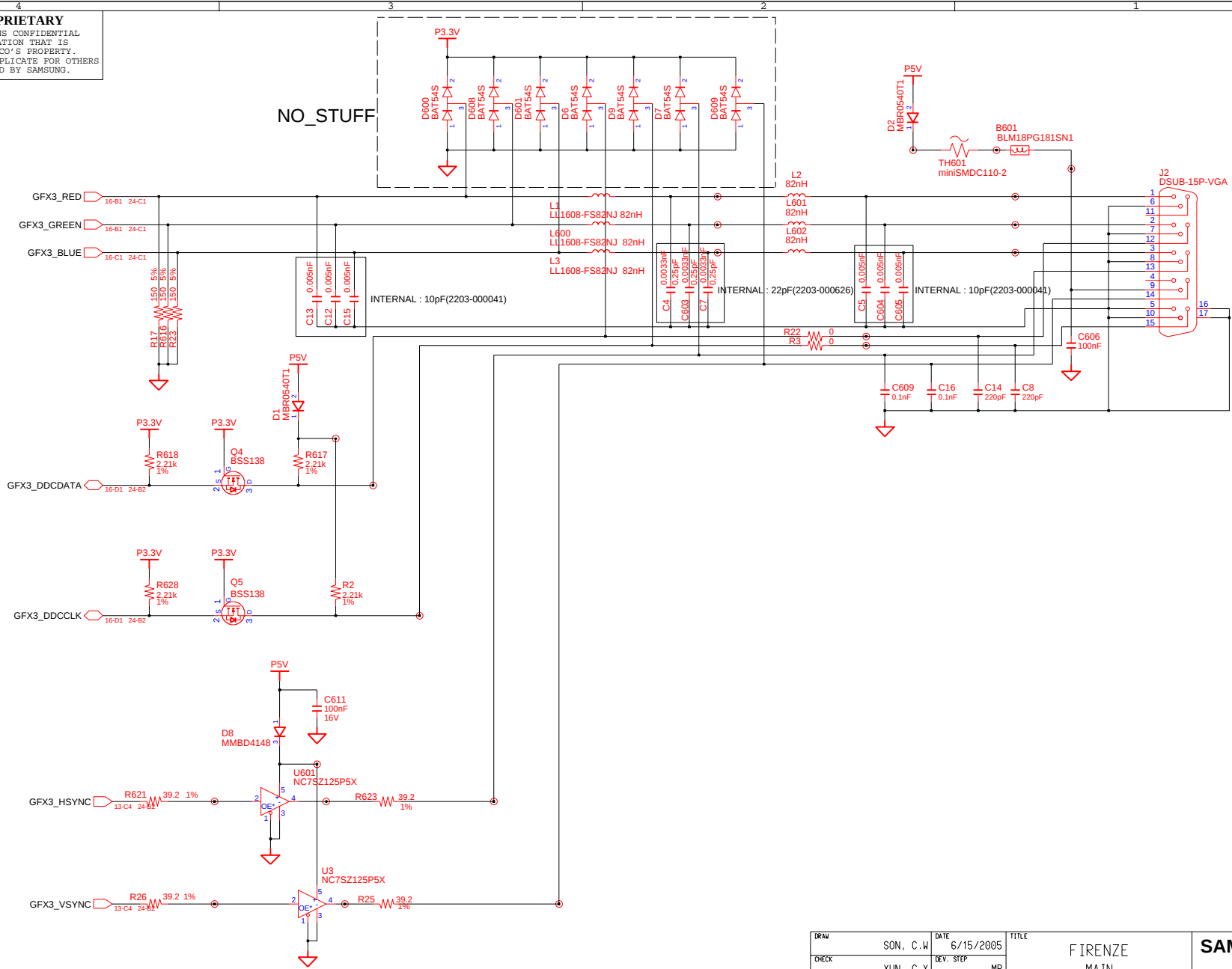


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DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	MP	MAIN	MAIN	
APPROVAL	LIM, J.G	REV	1.0	GFX MEMORY(2/2)		PART NO. BA41-00509A
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	31	OF 55

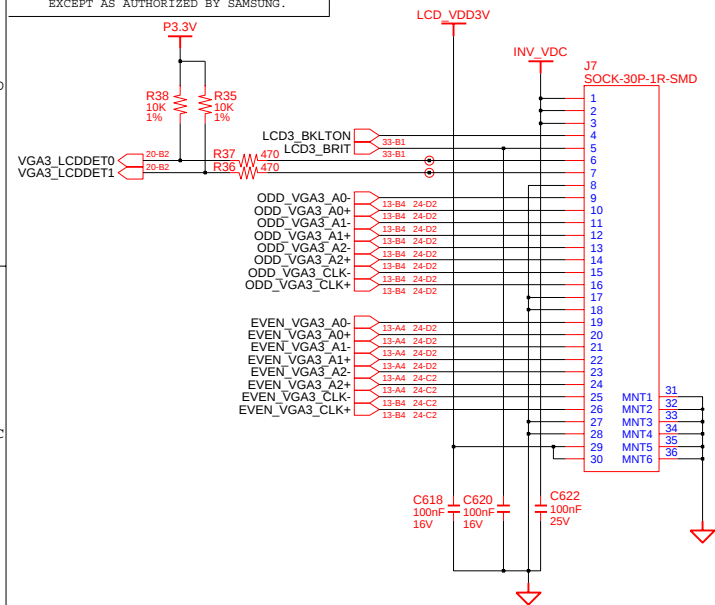
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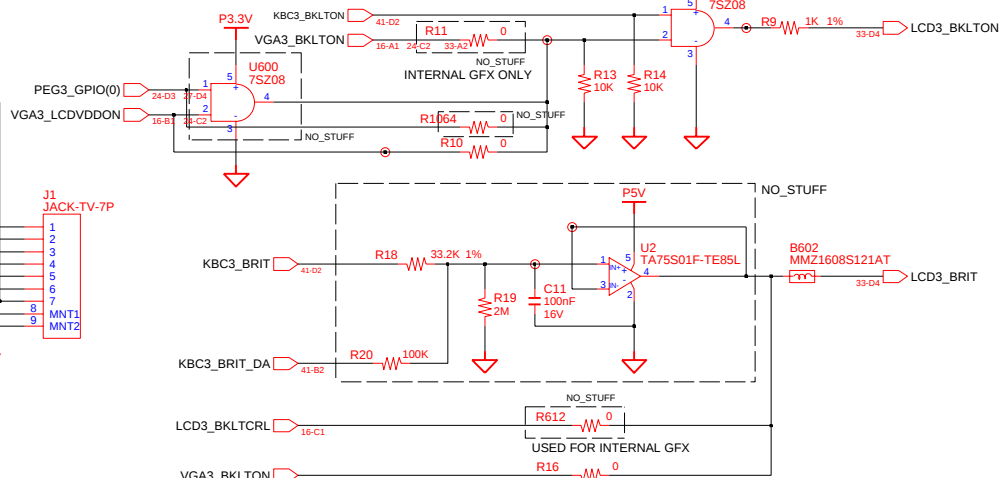
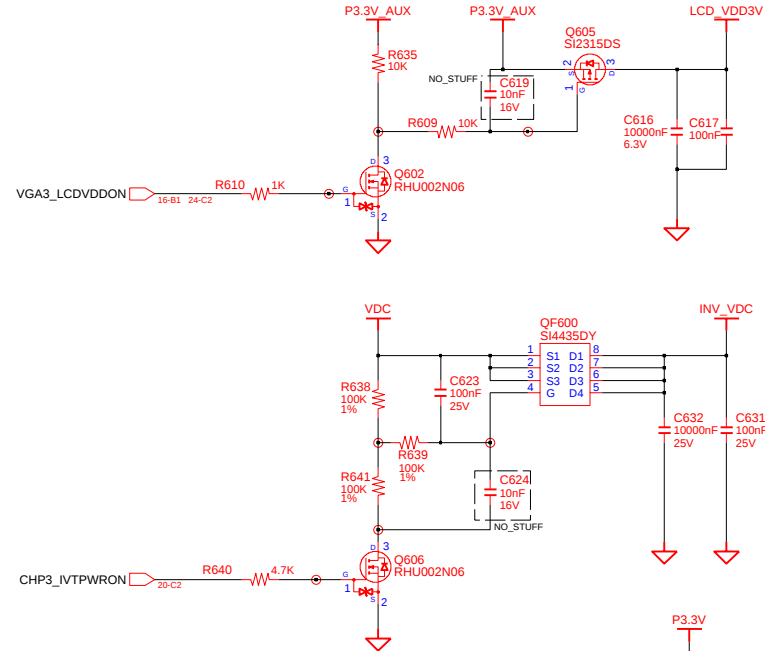
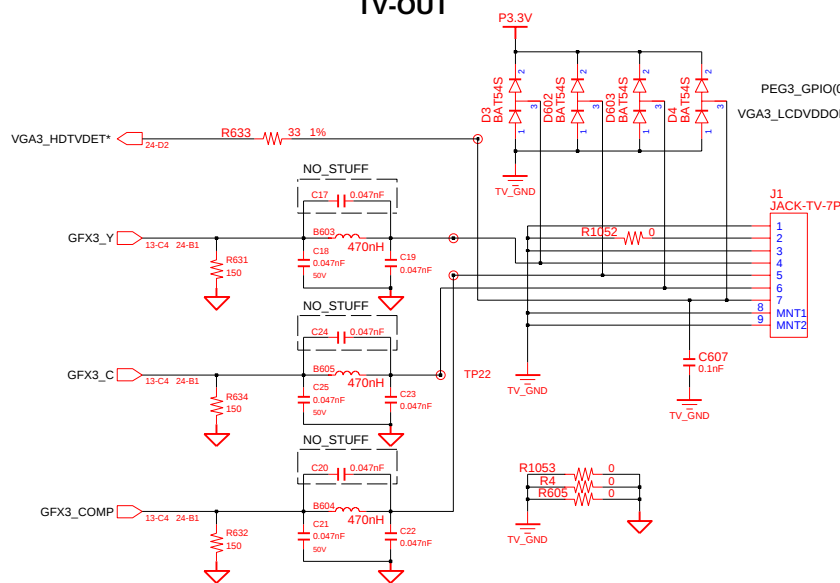
DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZA MAIN CRT PORT	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	MP			PART NO. BA41-00509A
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	32	OF 55

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LCD CONNECTOR

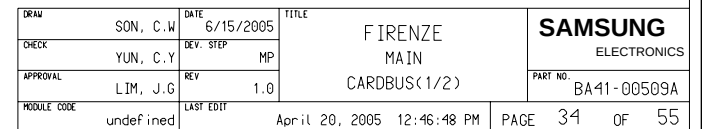


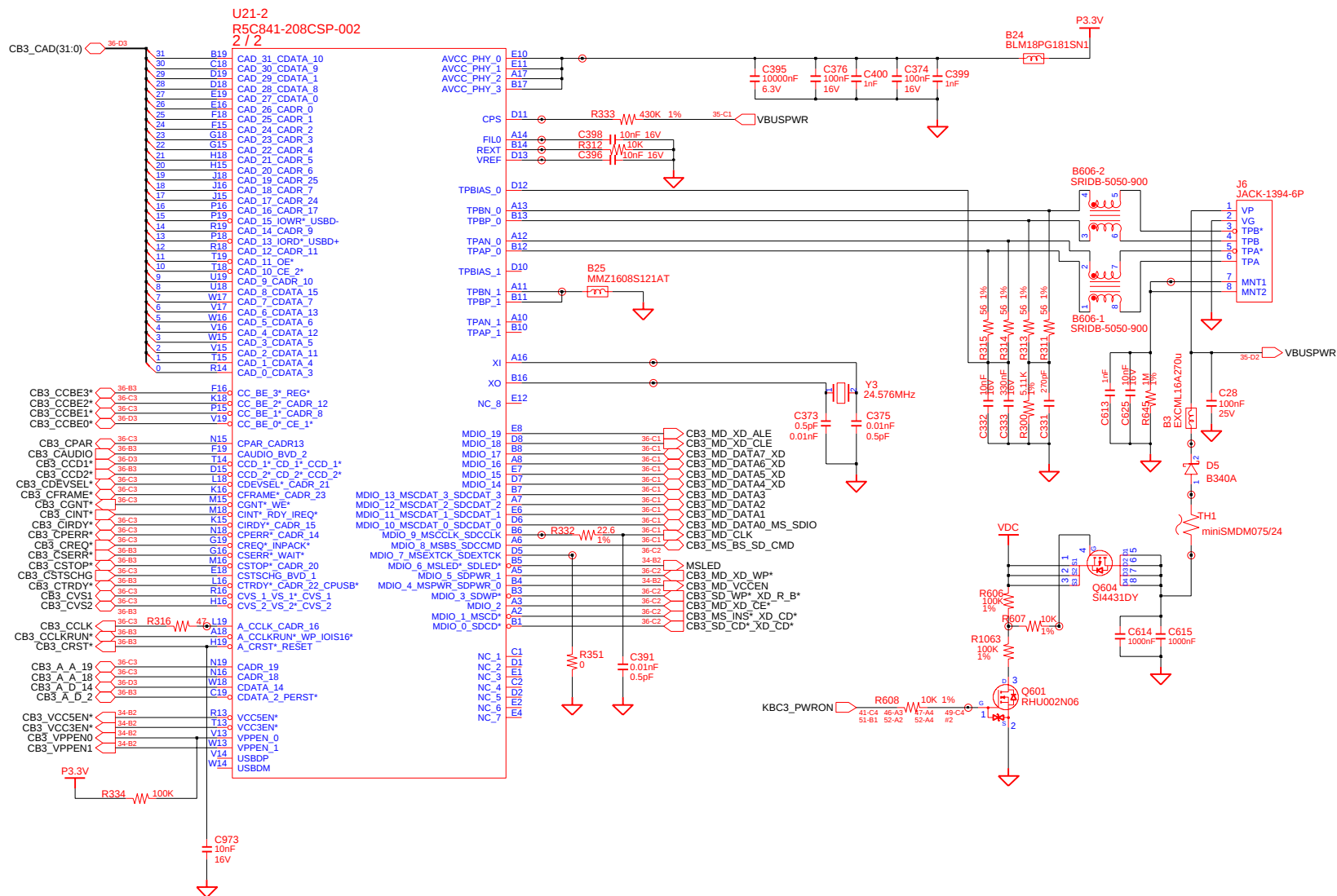
TV-OUT



DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE MAIN LCD/TV-OUT	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	MP			PART NO. BA41-00509A
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	33	OF 55

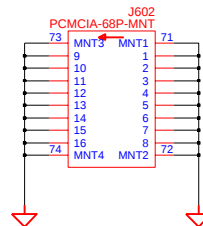
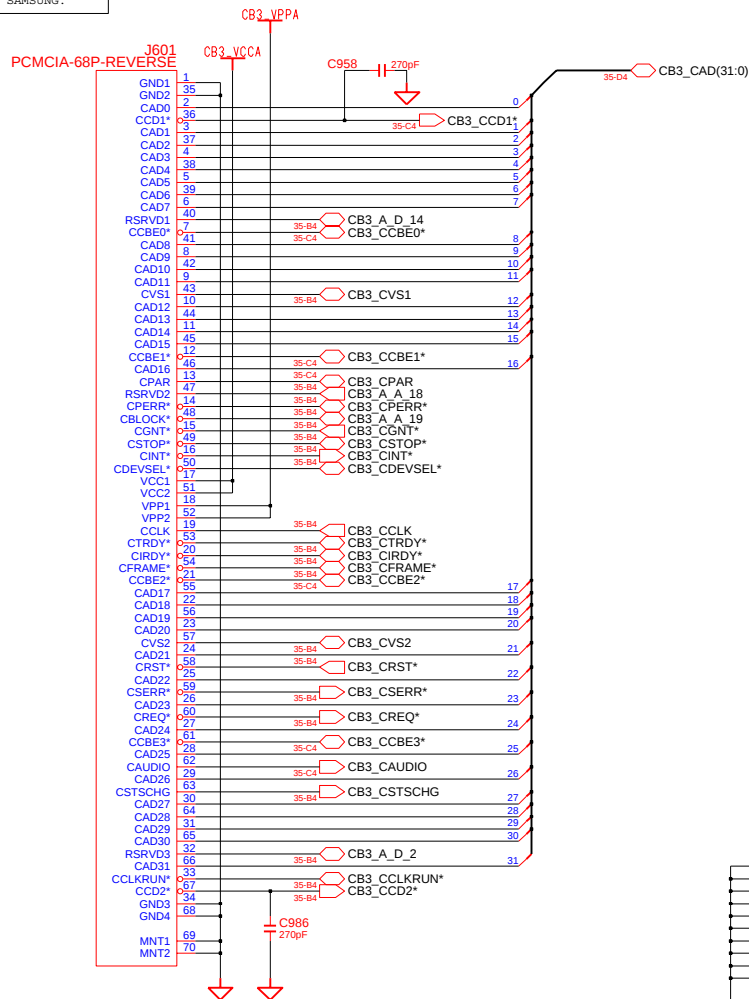
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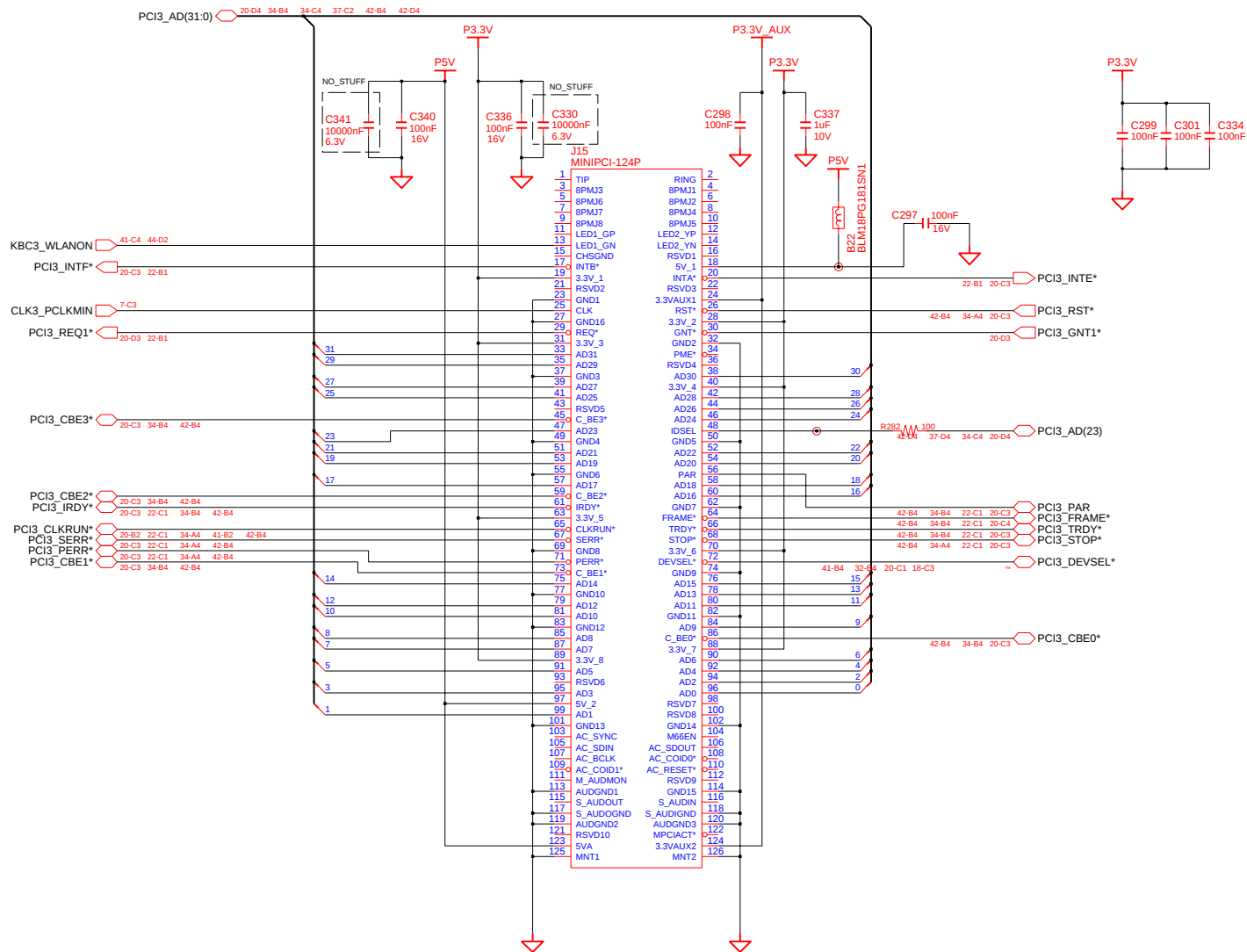
DATE	6/15/2005	TITLE FIRENZE MAIN CARBUS(2/2)		SAMSUNG ELECTRONICS			
CHECK	YUN, C.Y.					DEV. STEP	MP
APPROVAL	LIM, J.G.					REV	1.0
MODULE CODE		LAST EDIT		April 20, 2005 12:46:48 PM	PAGE 35 OF 55		

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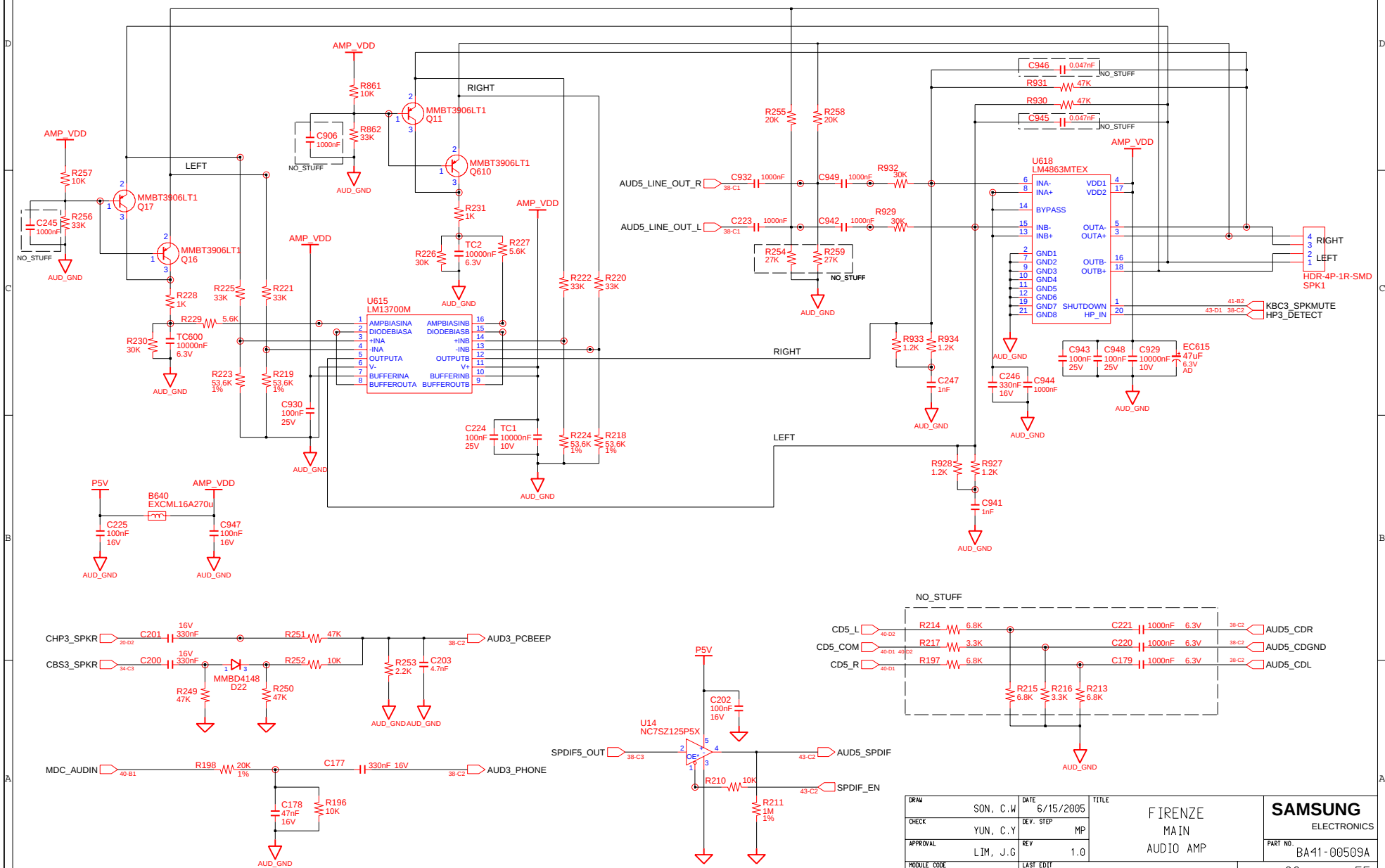
DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE MAIN	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	MP	REV	1.0	PART NO. BA41-00509A
APPROVAL	LIM, J.G	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	36	OF 55
MODULE CODE	undefined					

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DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE MAIN MINI PCI	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	MP			PART NO. BA41-00509A
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	37	OF 55

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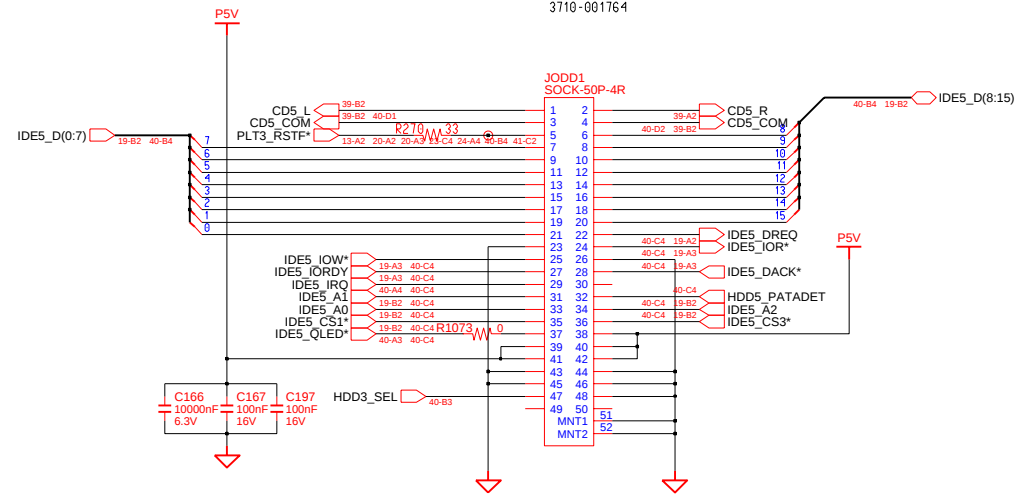


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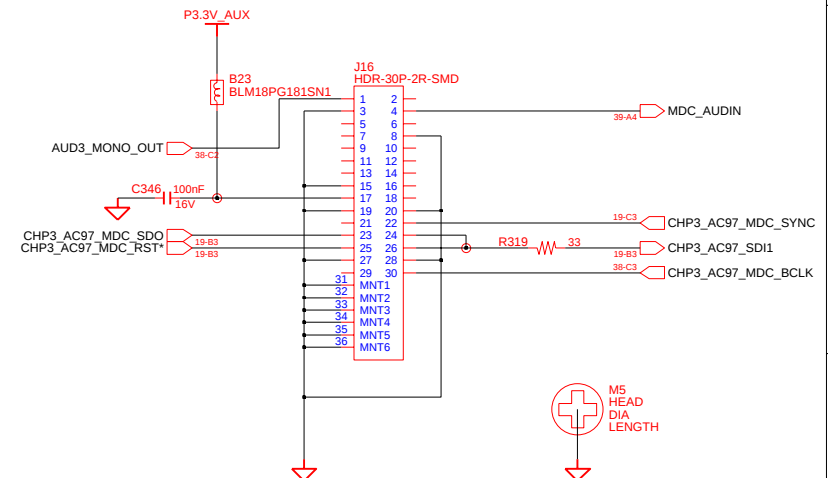
MAIN TO HDD

MAIN TO ODD

3710-001764

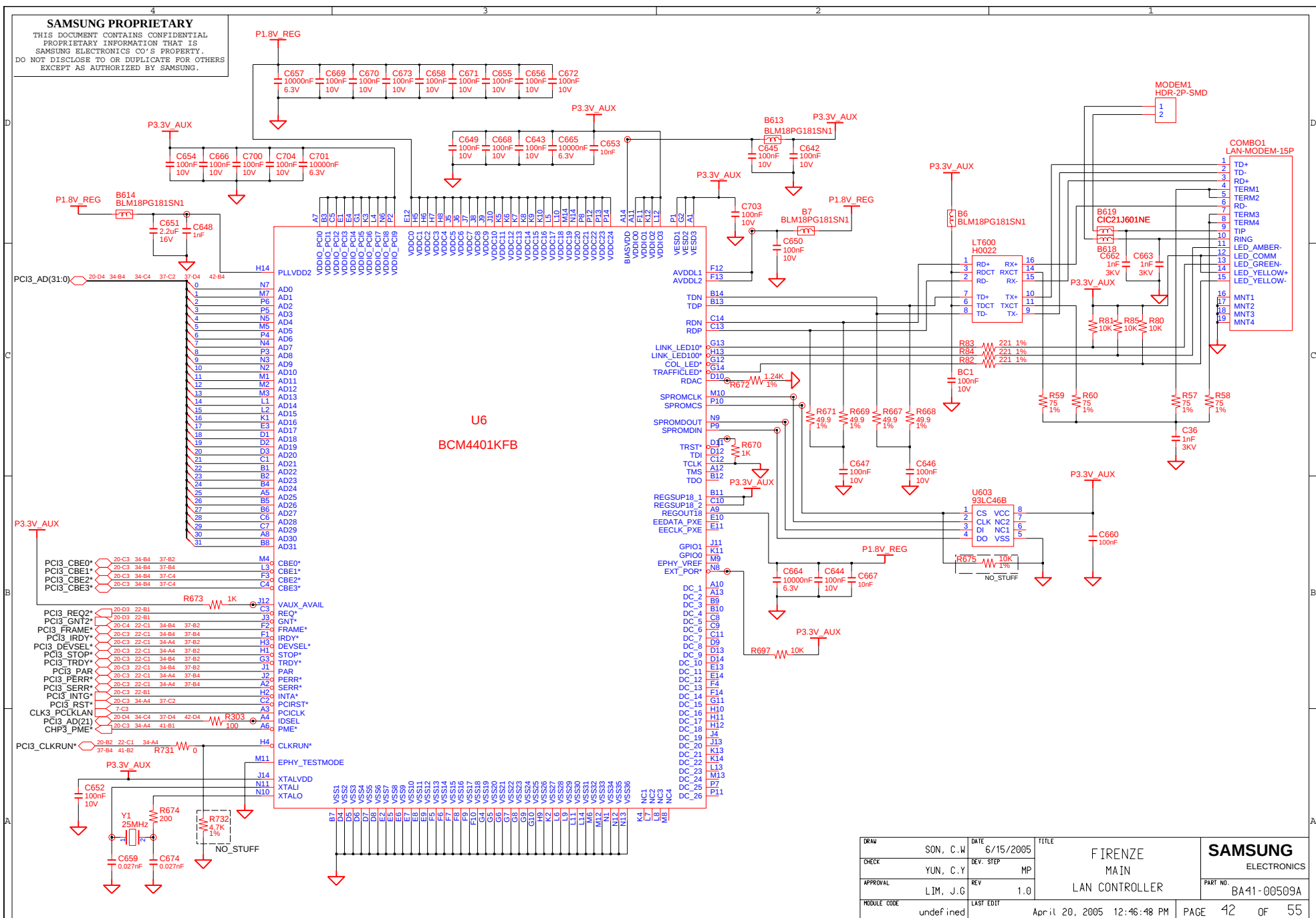


MDC Connector



DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE MAIN HDD/ODD/MDC CONN	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	MP			PART NO. BA41-00509A
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	40	OF 55

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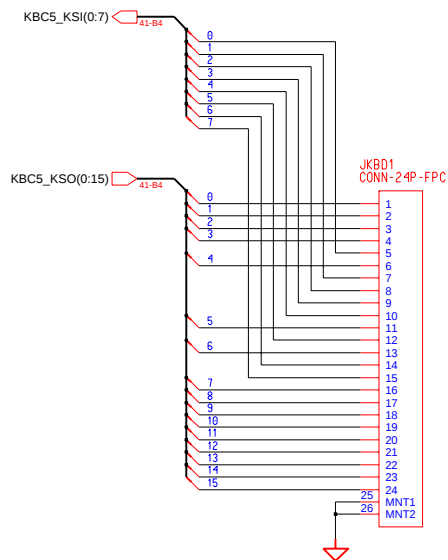


DRAM	SON, C. W.	DATE	6/15/2005	FIRENZE MAIN LAN CONTROLLER	SAMSUNG ELECTRONICS PART NO. BA41-00509A	
CHECK	YUN, C. Y.	DEV. STEP	MP			
APPROVAL	LIM, J. G.	REV	1.0			
MODULE CODE	undef ined		LAST EDIT			

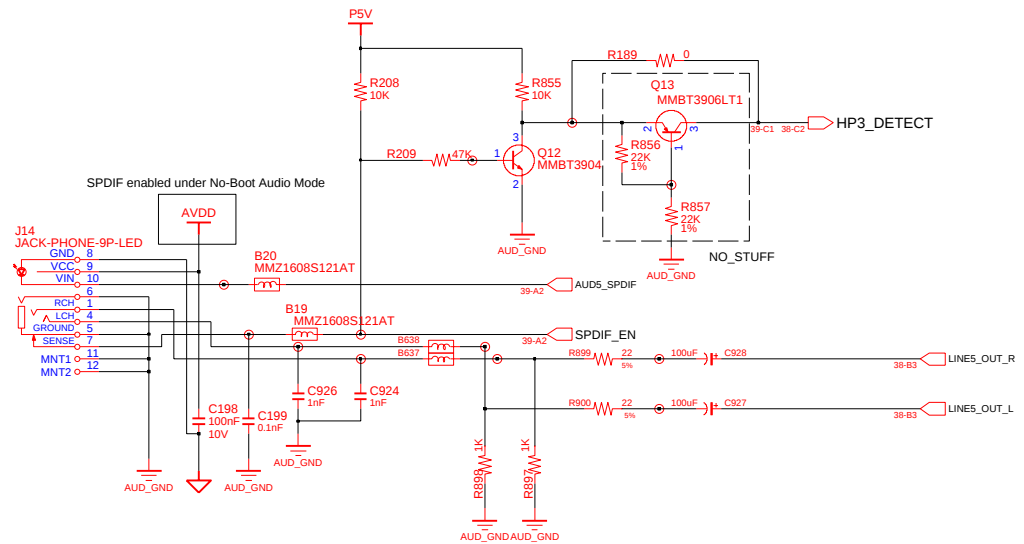
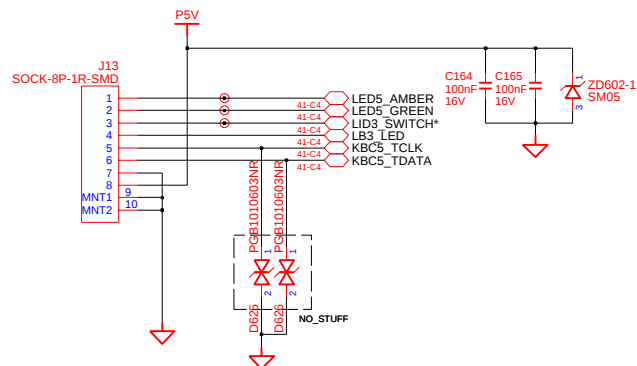
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OPTICAL SPDIF OUTPUT & HEADPHONE

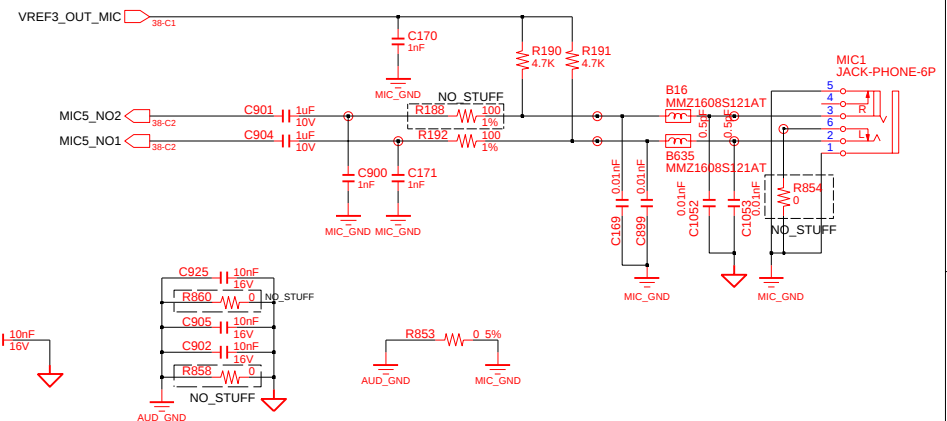
KEYBOARD



TOUCH PAD



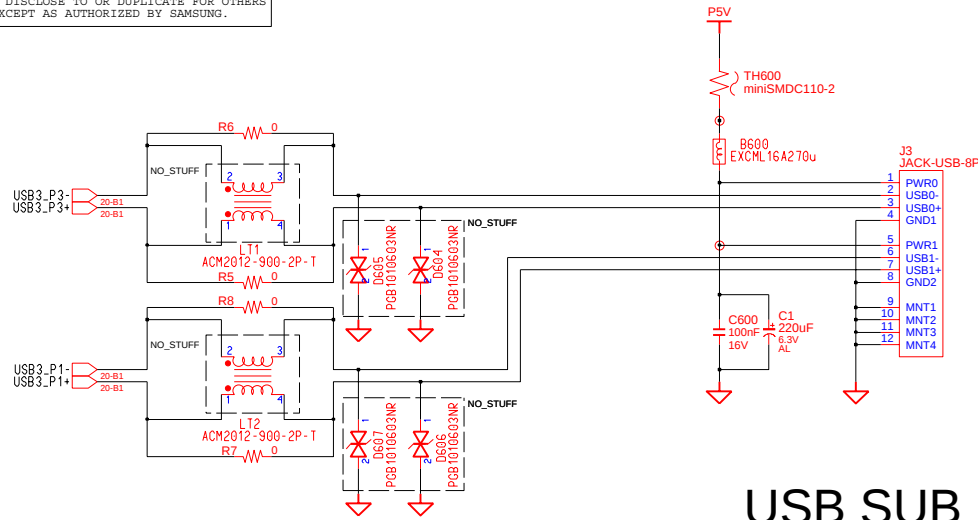
MICROPHONE



DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE	SAMSUNG
CHECK	YUN, C.Y	DEV. STEP	MP	MAIN		ELECTRONICS
APPROVAL	LIM, J.G	REV	1.0	KBD/TPAD/HP/MIC		PART NO. BA41-00509A
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	43	OF 55

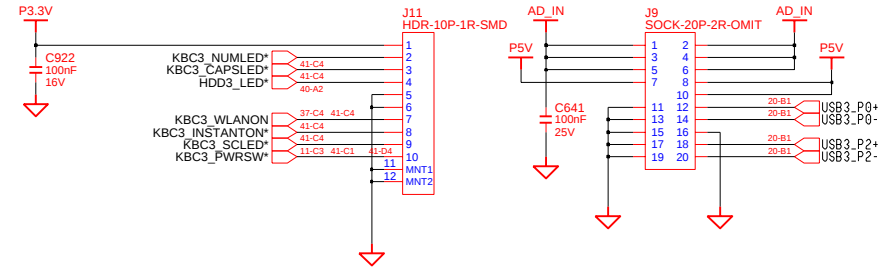
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USB PORT

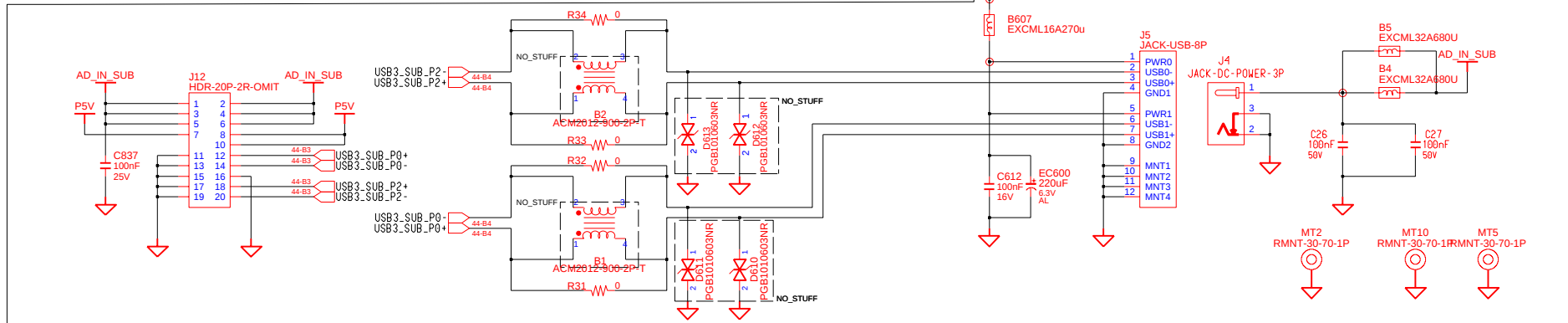


MAIN TO ON-TOP

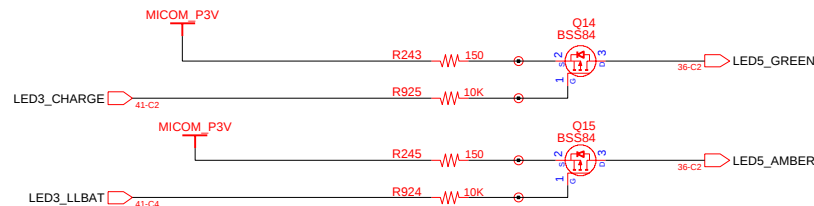
MAIN TO USB



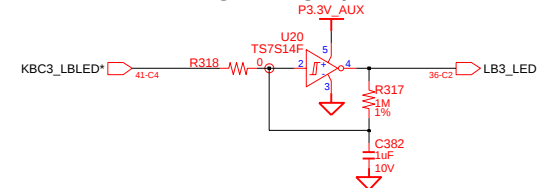
USB SUB B'D



ADAPTER IN / CHARGER LED

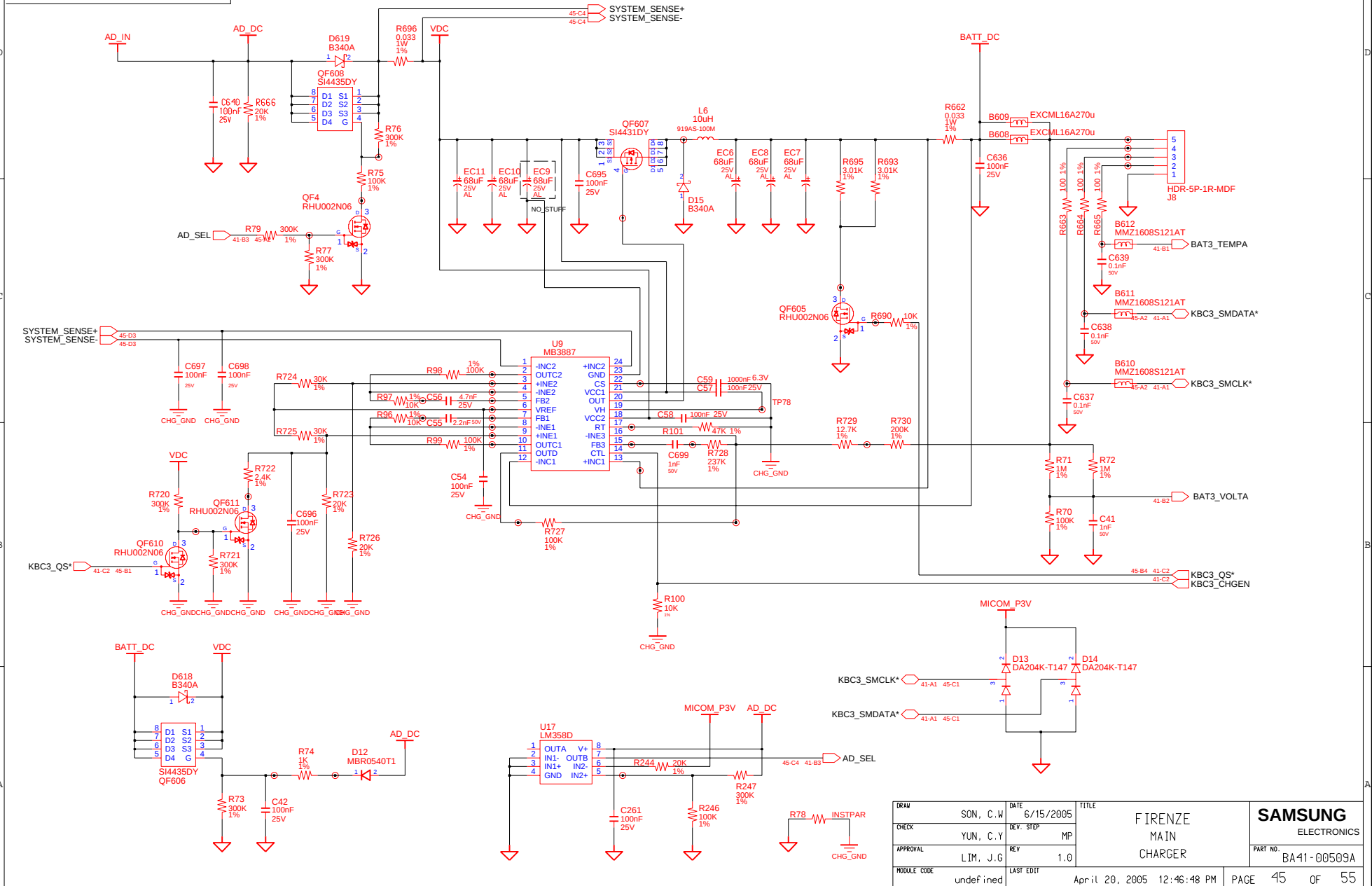


POWER ON / LB LED



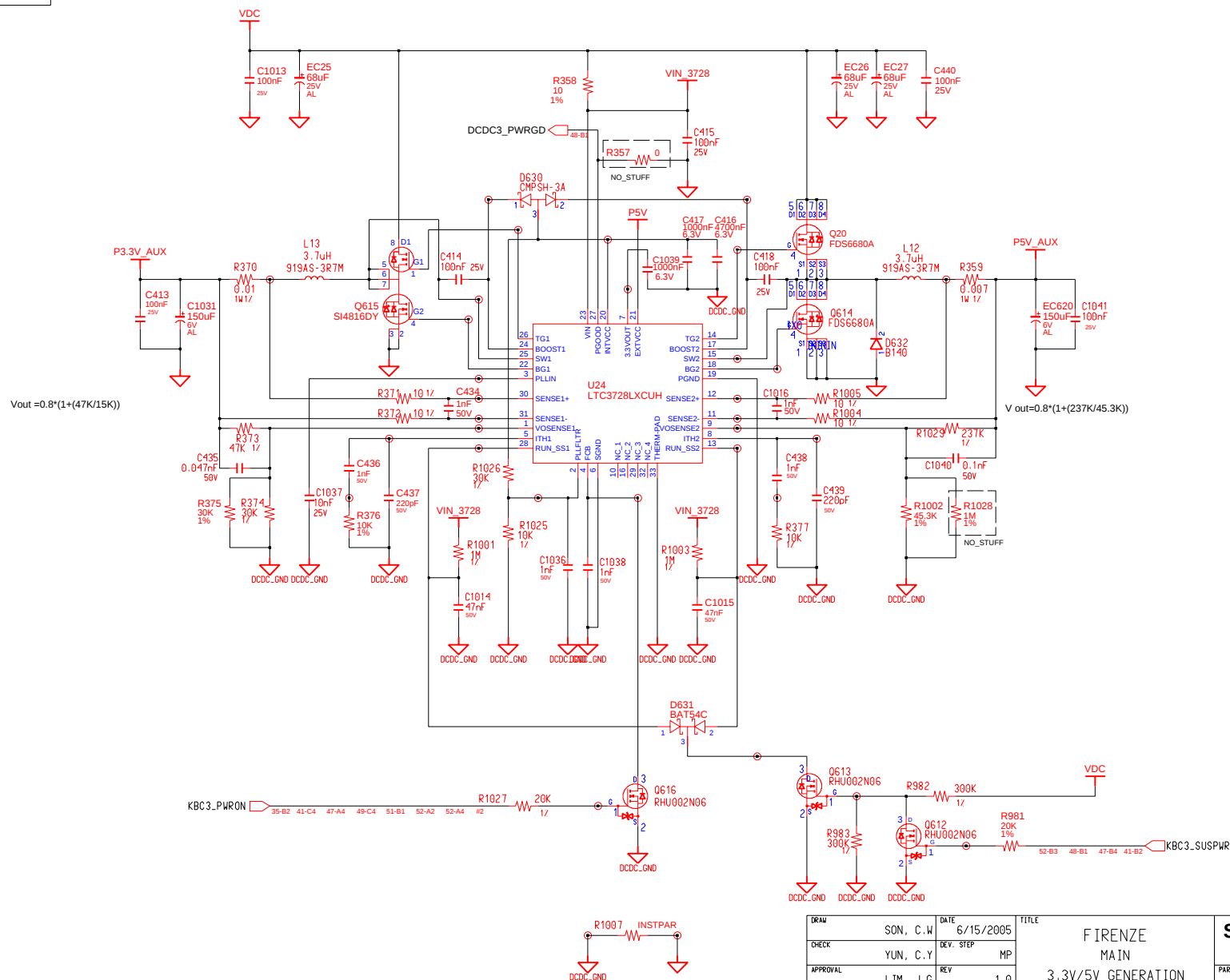
DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE	SAMSUNG
CHECK	YUN, C.Y	DEV. STEP	MP	MAIN	MAIN	ELECTRONICS
APPROVAL	LIM, J.G	REV	1.0	USB PORT/LED/ON-TOP	PART NO.	BA41-00509A
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	44	OF 55

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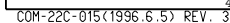
DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZA MAIN CHARGER	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	MP			PART NO. BA41-00509A
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	45	OF 55

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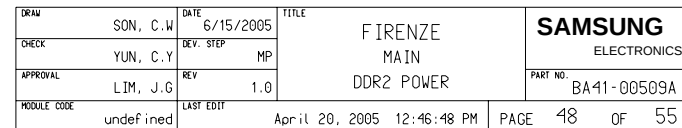


DRAM	SON, C.W.	DATE	6/15/2005	TITLE	FIRENZE MAIN 3.3V/5V GENERATION	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y.	DEV. STEP	MP			
APPROVAL	LIM, J.G.	REV	1.0			
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM			
				PAGE	46	OF 55

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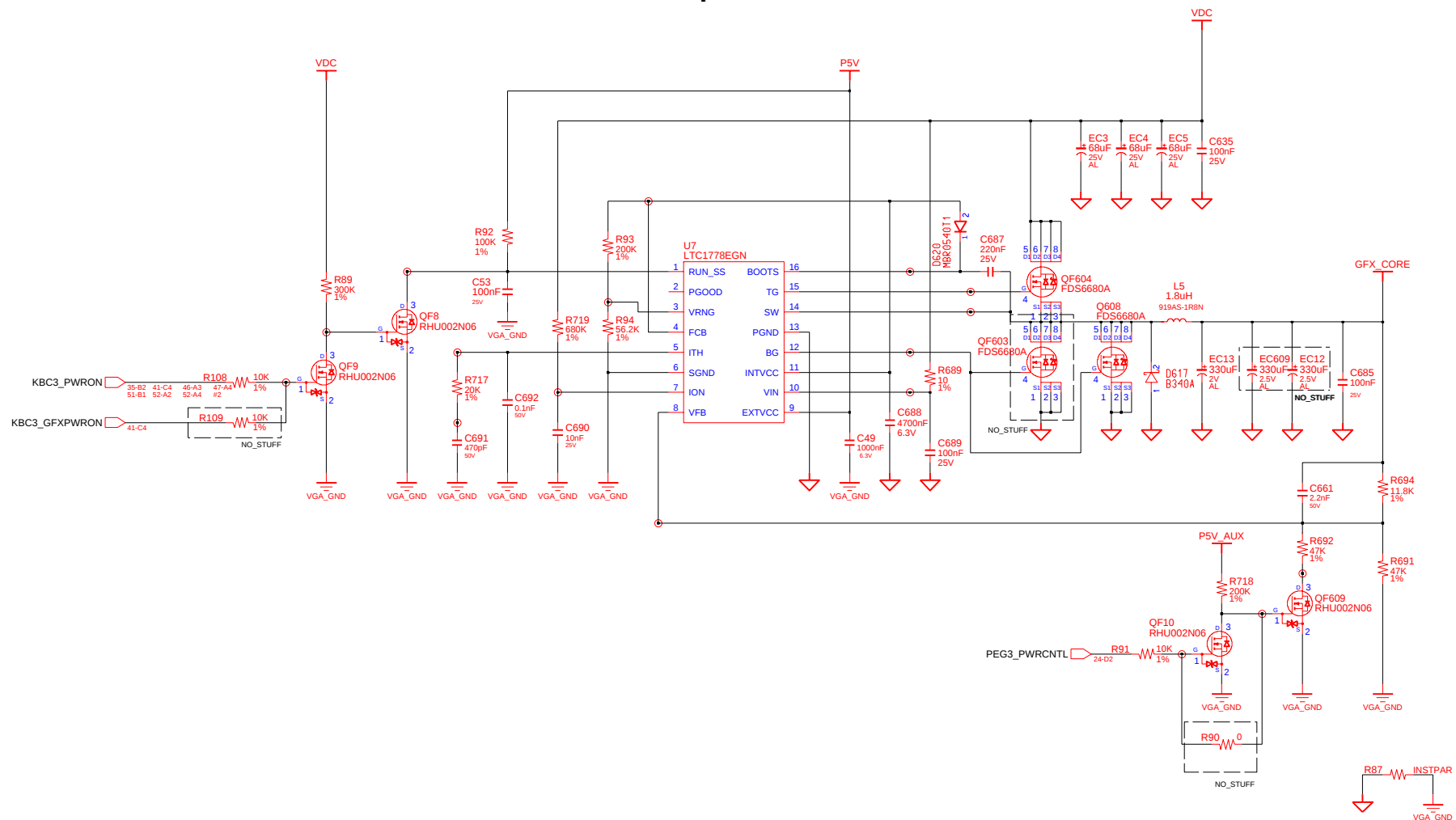


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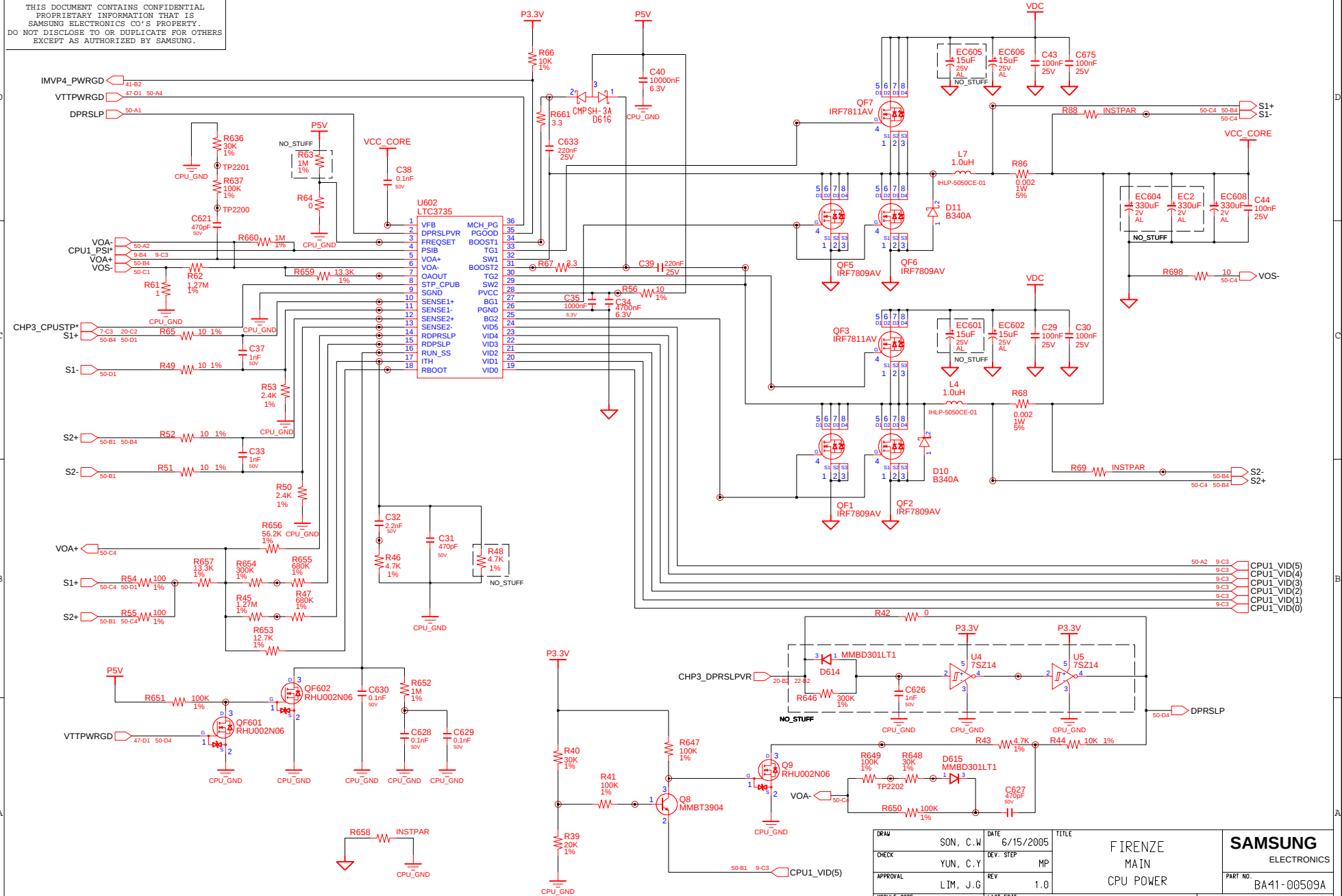
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Graphic Core Power



DRAW	SON, C.W.	DATE	6/15/2005	TITLE FIRENZE MAIN GRAPHIC CORE POWER		SAMSUNG ELECTRONICS	
CHECK	YUN, C.Y.	DEV. STEP	MP				
APPROVAL	LIM, J.G.	REV	1.0				
MODULE CODE		LAST EDIT		April 20, 2005 12:46:48 PM	PAGE	49	OF 55

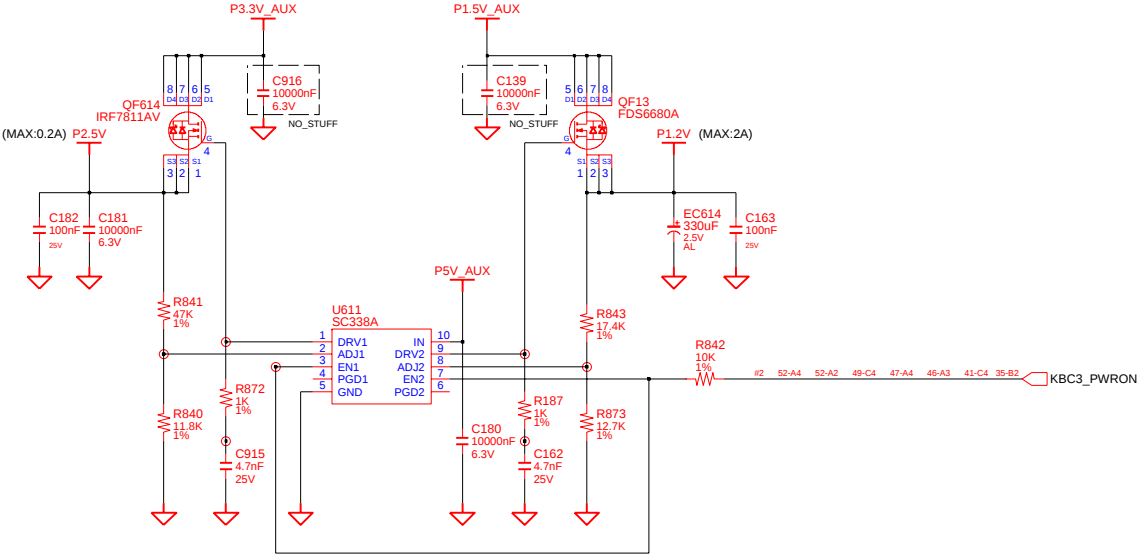
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DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE MAIN CPU POWER	SAMSUNG ELECTRONICS PART NO. BA41-00509A
CHECK	YUN, C.Y	DEV. STEP	MP			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	50 OF 55	

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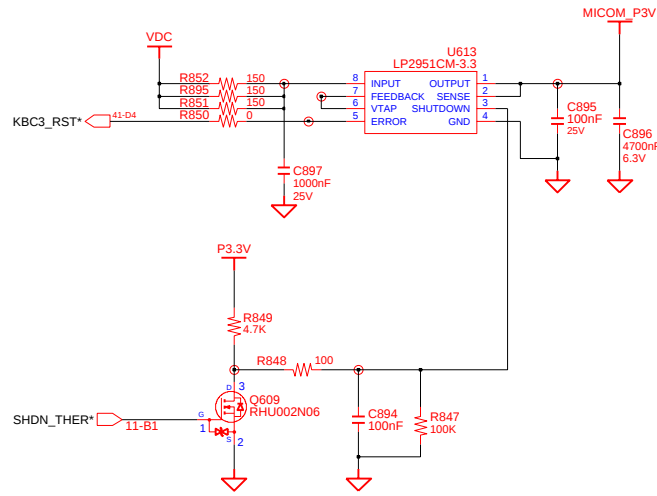
P1.2V / P2.5V POWER



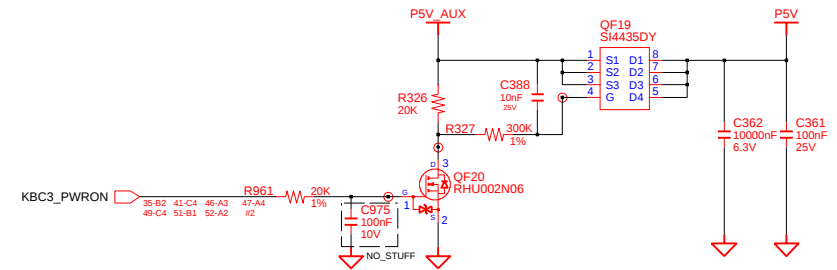
DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE MAIN 1.2V/2.5V POWER	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	MP	REV	1.0	PART NO. BA41-00509A
APPROVAL	LIM, J.G	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	51	OF 55
MODULE CODE	undefined					

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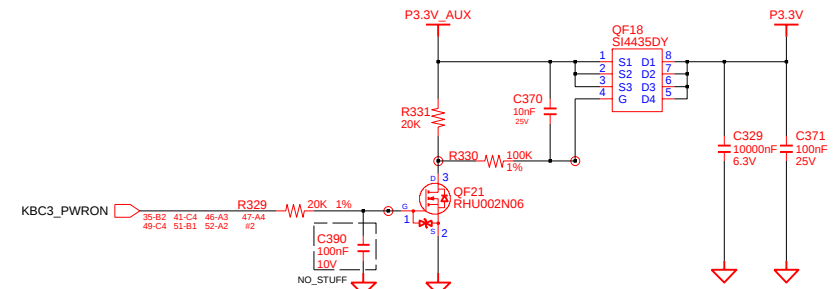
MICOM_P3V Power



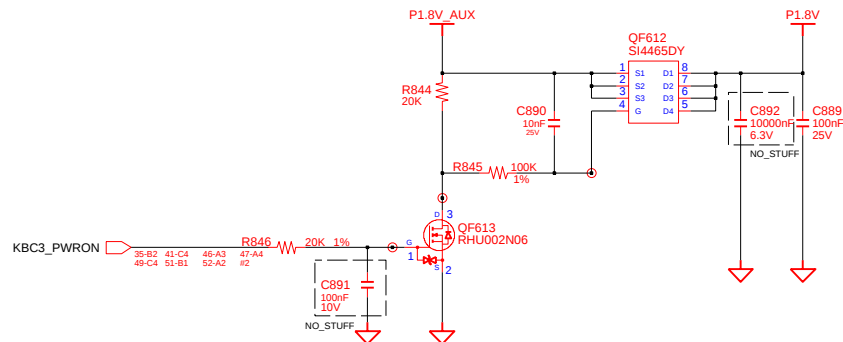
Switched Power On (P5V)



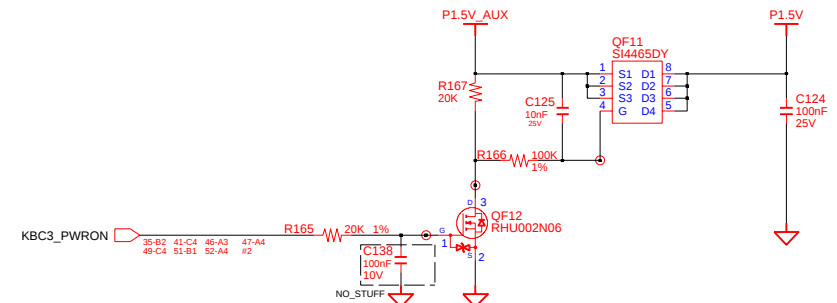
Switched Power On (P3.3V)



Switched Power On (P1.8V)

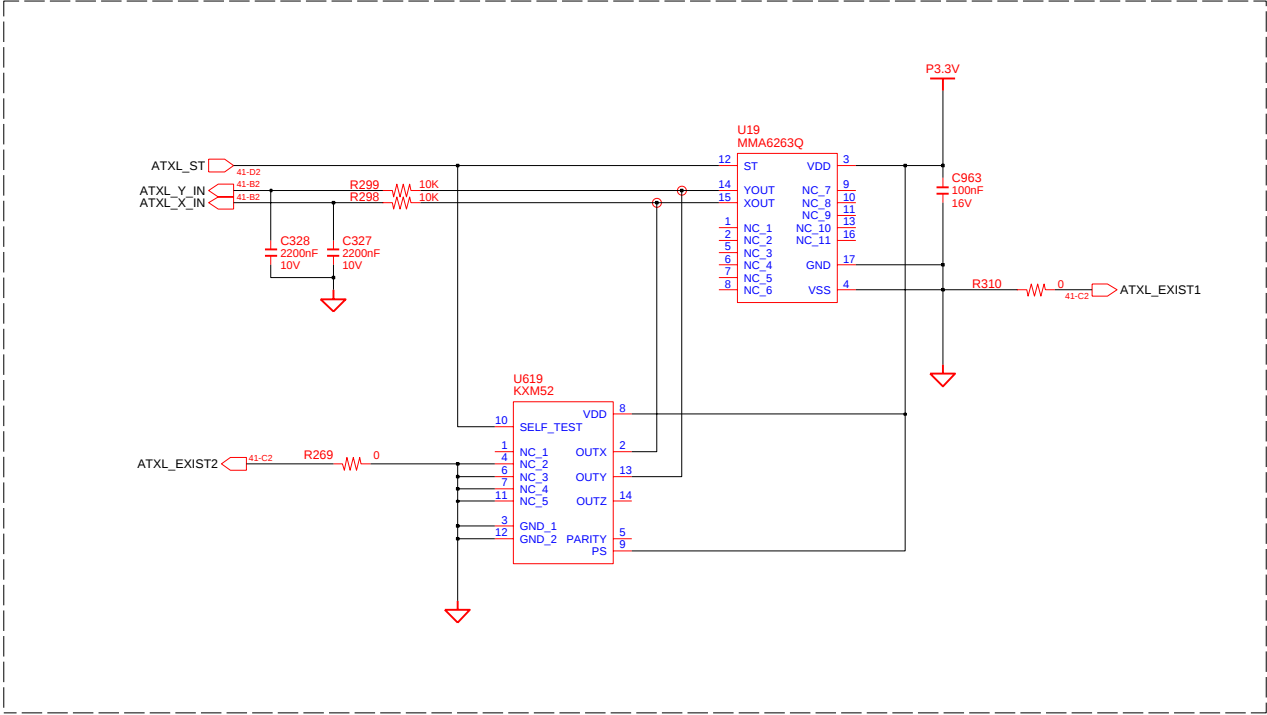


Switched Power On (P1.5V)

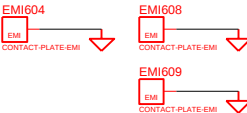


DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE MAIN	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	MP			
APPROVAL	LIM, J.G	REV	1.0		MICOM&SWITCHED POWER	PART NO. BA41-00509A
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	52	OF 55

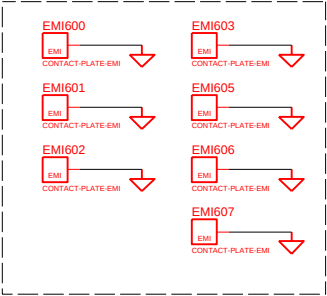
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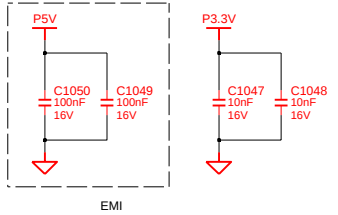
NO_STUFF



NO_STUFF



NO_STUFF



DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE MAIN AIR BAG	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	MP			PART NO. BA41-00509A
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	54 OF 55	

