SERVICE MANUAL FOR

8965

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MiTAC

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1. Hardware Engineering Specification

1.1 Introduction

1.1.1 General Description

This document describes the brief introduction for MITAC 8965 portable notebook computer system.

1.1.2 System Overview

The MITAC 8965 model is designed for Intel Banias processor with 400MHz FSB with Micro-FCPGA package. It can support Banias 1.5G ~ 1.9GHz.

This system is based on PCI architecture and is fully compatible with IBM PC/AT specification, which has standard hardware peripheral interface. The power management complies with Advanced Configuration and Power Interface (ACPI) 2.0. It also provides easy configuration through CMOS setup, which is built in system BIOS software and can be pop-up by pressing F2 key at system start up or warm reset. System also provides icon LEDs to display system status, such as Wireless Lan indicator, Power indicator, Battery status indicator, HDD, Num Lock, Caps Lock, Scroll Lock. It also equipped with LAN, 4 USB ports, and audio line out, external microphone function.

The memory subsystem supports two expansion DDR SDRAM slot with unbuffered PC3200 DDR400 SDRAM.

The VIA PN800 Mobile North Bridge integrates a high performance CPU interface for Intel Pentium 4 / Pentium-M processor, a full featured AGP port controller, integrated Graphics with 2D/ 3D/ Video Controllers, a advanced high-performance DDR400 SDRAM controller, and high bandwidth Ultra V-Link host controller connecting with VIA

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VT8235CE South Bridge.

The VIA VT8235CE integrates Universal Serial Bus 2.0 Host Controllers Interface (UHCI), the Audio Controller with AC97 interface, the Ethernet includes a 32-bit PCI controller, the IDE Master/Slave controllers, and Inter-operable with VIA Host-to-V-Link Host Controller.

The VIA VT6103L is a Fast Ethernet 10 / 100 1-port PHY / Transceiver with MII interface, and meet all applicable IEEE 802.3, 10Base-T and 100Base-Tx standards.

The W83L950D is a high performance microcontroller on-chip supporting functions optimized for embedded control. These include ROM, RAM, four types of timers, a serial communication interface, optional I²C bus interface, host interface, A/D converter, D/A converter, I/O ports, and other functions needed in control system configurations, so that compact, high performance systems can be implemented easily.

A full set of software drivers and utilities are available to allow advanced operating systems such as Windows ME, Windows 2000 and Windows XP to take full advantage of the hardware capabilities. Features such as bus mastering IDE, Plug and Play, Advanced Power Management (APM) with application restart, software-controlled power shutdown.

Following chapters will have more detail description for each individual sub-systems and functions.

1.2 System Hardware Parts

CPU	Mobile Pentium-M Processor 1.3G ~ 1.9GHz Thermal spec 35W TDP
Core logic	VIA PN800 + VIA VT8235CE chipset
VGA Control	North Bridge Integrated
System BIOS	SST49LF040
Memory	DDR RAM : DDR333 Nanya NT512D64S8HBAFM-6K DDR400 Micron, MT8VDDT3264HD
Video Memory	Share memory
Clock Generator	ICS 950902
LVDS	VIA VT1634AL
LAN PHY	VIA VT6103L
Audio System	AC97 CODEC: Advance Logic, Inc, ALC655 Power Amplifier: TI TPA0212

1.2.1 Intel Banias Processors in Micro-FCPGA Package

Intel Banias Processors with 593 pins Micro-FCBGA package.

It has the Intel NetBurst micro-architecture which features include hyper-pipelined technology, a rapid execution engine, a 400MHz system, an execution trace cache, advanced dynamic execution, advanced transfer cache, enhanced floating point and multi-media unit, and Streaming SIMD Extensions 2 (SSE2).

The Streaming SIMD Extensions 2 (SSE2) enable break-through levels of performance in multimedia applications including 3-D graphics, video decoding/encoding, and speech recognition.

Use Source-Synchronous Transfer (SST) of address and data to improve performance by transferring data four times per bus clock.

Support Enhanced Intel SpeedStep technology, which enables real-time dynamic switching of the voltage and frequency between two performance modes.

1.2.2 Clock Generator

The ICS950902 is a single chip clock solution for desktop designs using the VIA P4X/P4M/KT/KN266/333 style chipsets with PC133 or DDR memory. The ICS950902 is part of a whole new line of ICS clock generators and buffers called TCH™ (Timing Control Hub). This part incorporates ICS's newest clock technology which offers more robust features and functionality. Employing the use of a serially programmable I2C interface, this device can adjust the output clocks by configuring the frequency setting, the output divider ratios, selecting the ideal spread percentage, the output skew, the output strength, and enabling/disabling each individual output clock. M/N control can configure output frequency with resolution up to 0.1MHz increment.

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Recommended Application

- VIA P4X/P4M/KT/KN266/333 style chipsets

Output Features

- 1 - Pair of differential CPU clocks @ 3.3V (CK408)/ 1 - Pair of differential open drain CPU clocks (K7)
- 1 - Pair of differential push pull CPU_CS clocks @ 2.5V
- 3 - AGP @ 3.3V
- 7 - PCI @ 3.3V (1 - Free running)
- 1 - 48MHz @ 3.3V fixed
- 1 - 24_48MHz @ 3.3V (Default 48MHz I2C select only)
- 2 - REF @ 3.3V, 14.318MHz
- 12 - SDRAM (6 pair - DDR) selectable

Features/Benefits

- Programmable output frequency
- Programmable output divider ratios
- Programmable output rise/fall time
- Programmable output skew
- Programmable spread percentage for EMI control
- DDR output buffer supports up to 200MHz
- Watchdog timer technology to reset system if system malfunctions

- Programmable watch dog safe frequency
- Support I2C Index read/write and block read/write operations
- Uses external 14.318MHz crystal

1.2.3 PN800 Mobile North Bridge

The PN800 is a high performance, cost-effective and energy efficient UMA North Bridge with integrated UniChrome Pro graphics / video controllers used for the implementation of mobile personal computer systems based on 800 / 533 / 400 MHz FSB Intel Pentium 4 and Pentium M super-scalar processors. The complete mobile chipset consists of the PN800 North Bridge (829 pin HSBGA) and the VT8235-CE V-Link South Bridge (539-pin BGA). The PN800 integrates VIA's PT800 system controller with high-performance UniChrome Pro 3D/2D graphics accelerator plus flat panel, DVI monitor and TV out interfaces. The PN800 provides superior performance between the CPU, DRAM, V-Link bus and internal AGP 8x graphics controller bus with pipelined, burst, and concurrent operation. The VT8235-CE is a highly integrated peripheral controller which includes V-Link-to-PCI / V-Link-to-LPC controllers, Ultra DMA IDE controller,USB2.0 host controller, 10/100Mb networking MAC, AC97, and system power management controllers.

Host CPU Interface

The PN800 supports 800 / 533 / 400 MHz FSB Intel Pentium 4 and Pentium M super-scalar processors. It implements a twelve level In-Order-Queue and supports Intel Hyper-Threading Technology to maximize system performance for multi-threaded software applications. DBI and Pentium M bus protocol, as well as Intel SpeedStep Technology, are supported which effectively reduce overall system power consumption.

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AGP Interface

The PN800 AGP controller is AGP 3.0 compliant with up to 2.1 GB / second data transfer rate capability. It supports asynchronous AGP and CPU interfaces for flexible system configuration. Deep read (1024 byte) and write (512 byte) FIFOs are integrated for optimal bus utilization and minimum data transfer latency.

Memory Controller

The PN800 SDRAM Controller supports two sets of 64-bit memory data, address and control signals to minimize signal loading and up to 4 double-sided DDR400 / 333 / 266 DIMMs for 8 GB maximum physical memory. The DDR DRAM interface allows zero wait-state data transfer bursting between the DRAM and the memory controller's data buffers. The different banks of DRAM can be composed of an arbitrary mixture of 64 / 128 / 256 / 512 / 1024Mb DRAMs in x8 and x16 configurations. The DRAM controller can run either synchronous or pseudo-synchronous with the host CPU bus. The PN800 North Bridge is pin compatible with the PN880 North Bridge which connects to the memory modules in exactly the same manner while supporting true 128-bit operation (simultaneous memory access on both sets of 64-bit memory data / address / control signals).

Ultra V-Link

The PN800 North Bridge interfaces to the South Bridge through a high speed (up to 1 GB/sec) 8x, 66 MHz Data Transfer interconnect bus called "Ultra V-Link". Deep pre-fetch and post-write buffers are included to allow for concurrent CPU and Vlink operation. The combined PN800 North Bridge and VT8235-CE South Bridge system supports enhanced PCI bus commands such as "Memory-Read-Line", "Memory-Read-Multiple" and "Memory-Write-Invalid" commands to minimize snoop overhead. In addition, advanced features are supported such as CPU write-back forward to PCI master, and CPU write-back merged with PCI post write buffers to minimize PCI master read latency and DRAM utilization. Delay transaction and read caching mechanisms are also implemented for

further improvement of overall system performance.

System Power Management

For sophisticated power management, the PN800 supports dynamic CKE control to minimize DDR SDRAM power consumption during normal system state (S0). A separate suspend power plane is implemented for the memory control logic for Suspend-to-DRAM state. Enhanced Intel SpeedStep™ Technology enables minimization of CPU power consumption while sustaining processing power. The PN800 graphics accelerator implements dynamic clock gating for inactive functions to achieve maximum power savings. The system can also be switched to standby or suspend states to further reduce power consumption when idle.Automatic panel power sequencing and VESA DPMS (Display Power Management Signaling) CRT power-down are supported.Coupled with the VT8235-CE South Bridge chip, a complete power conscious PC main board can be implemented with no external glue logic.

3D Graphics Engine

Featuring an integrated 128-bit 3D graphics engine, the PN800 North Bridge utilizes a highly pipelined architecture that provides high performance along with superior image quality. Several new features enhance the 3D architecture, including two pixel rendering pipes, single-pass multitexturing, bump and cubic mapping, texture compression, edge anti-aliasing, vertex fog and fog table, hardware back-face culling, specular lighting, anisotropic filtering and an 8-bit stencil buffer. The chip also offers the industry's only simultaneous usage of single-pass multitexturing and single-cycle trilinear filtering – enabling stunning image quality without performance loss. Image quality is further enhanced with true 32-bit color rendering throughout the 3D pipeline to produce more vivid and realistic images. The advanced triangle setup engine provides industry leading 3D performance for a realistic user experience in games and other interactive 3D applications. The 3D engine is optimized for AGP texturing from system memory.

128-bit 2D Graphics Engine

The PN800 North Bridge's advanced 128-bit 2D graphics engine delivers high-speed 2D acceleration for productivity applications. The enhanced 2D architecture with direct access frame buffer capability optimizes UMA performance and provides acceleration of all color depths.

MPEG Playback

The PN800 North Bridge provides the ideal architecture for high quality MPEG-2 based video applications. For MPEG video playback, the integrated video engine offloads the CPU by performing planar-to-packed format conversion and motion video compensation tasks, while its enhanced scaling algorithm delivers incredible full-screen video playback.

Video Capture

The PN800 North Bridge implements an optional Video Capture Port which supports various video capture standards, including ITU-R BT656, VIP 1.1 and VIP 2.0 and is compliant with the most common video capture formats: 16 / 32-bit RGB and YUV422. With the integrated video capture feature, the PN800 can provide high performance video effects for video capturing and playback.

LCD, DVI Monitor and TV Output Display Support

The PN800 provides three “Digital Video Port” interfaces: FPDP, GDVP1 and DVP0. The Flat Panel Display Port (FPDP) implements a 24-bit / dual 12-bit interface which is designed to drive a Flat Panel Display via an external LVDS transmitter chip (such as the VIA VT1631, NSC DS90C387R or Chrontel CH7017). The PN800 can be connected to the external LVDS transmitter chip in either 24-bit or dual-12-bit modes. A wide variety of LCD panels are supported including VGA, SVGA, XGA, SXGA+ and up to UXGA-resolution TFT color panels, in either SDR (1

pixel / clock) or DDR (2 pixels / clock) modes. UXGA and higher resolutions require dual-edge data transfer (DDR) mode which is supported by the VIA VT1631 LVDS transmitter chip Digital Video Port 0 (DVP0) is normally used for interfacing to a TV encoder (such as the VIA VT1622A or VT1622AM using 3.3V signal levels), however if DVP0 is used for video capture, Digital Video Port 1 (GDVP1) may be configured for support of an external TV encoder (VIA VT1623 or VT1623M using low-voltage 1.5V signal levels). If GDVP1 is not being used for TV out, it can optionally be used to drive a DVI monitor via an external TMDS transmitter chip (such as the VIA VT1632) The flexible display configurations of the PN800 allow support of a flat panel (LVDS interface) or flat panel monitor (TMDS / DVI interface), TV display and CRT display at the same time. Internally the PN800 North Bridge provides two separate display engines, so if two display devices are connected, each can display completely different information at different resolutions, pixel depths and refresh rates. If more than two display devices are connected, the additional displays must have the same resolution, pixel depth and refresh rate as one of the first two. The maximum display resolutions supported for one display device are listed in the table below. If more than one display is implemented (i.e., if both display engines are functioning at the same time), then available memory bandwidth may limit the display resolutions supported on one or both displays. This will be dependent on many factors including primarily clock rates and memory speeds (contact VIA for additional information).

1.2.4 VT8235CE Highly Integrated South Bridge

The VT8235 Version CE South Bridge is a high integration, high performance, power-efficient and high compatibility device that supports Intel and non-Intel based processor to V-Link bus bridge functionality to make a complete Microsoft PC2001-compliant PCI/LPC system. The VT8235 Version CE includes standard intelligent peripheral controllers.

a) IEEE 802.3 compliant 10 / 100 Mbps PCI bus master Ethernet MAC with standard MII interface to external PHY ceiver.

b) Master mode enhanced IDE controller with dual channel DMA engine and interlaced dual channel commands. Dedicated FIFO coupled with scatter and gather master mode operation allows high performance transfers between PCI and IDE devices. In addition to standard PIO and DMA mode operation, the VT8235 Version CE also supports the Ultra DMA-133, 100, 66 and 33 standards to allow reliable data transfer at rates up to 133 MB/sec. The IDE controller is SFF-8038i v1.0 and Microsoft Windows-family compliant.

c) Universal Serial Bus controller that is USB v2.0 / 1.1 and Universal HCI v2.0 / 1.1 compliant. The VT8235 Version CE includes three root hubs with six function ports with integrated physical layer transceivers. The USB controller allows hot plug and play and isochronous peripherals to be inserted into the system with universal driver support. The controller also implements legacy keyboard and mouse support so that legacy software can run transparently in a non-USB-aware operating system environment.

d) Keyboard controller with PS2 mouse support.

e) Real Time Clock with 256 byte extended CMOS. In addition to the standard ISA RTC functionality, the integrated RTC also includes the date alarm, century field and other enhancements for compatibility with the ACPI standard.

f) Notebook-class power management functionality compliant with ACPI and legacy APM requirements. Multiple sleep states (power-on suspend, suspend-to-DRAM and suspend-to-Disk) are supported with hardware automatic wake-up. Additional functionality includes event monitoring, CPU clock throttling and stop (Intel processor protocol), PCI bus clock stop control, modular power, clock and leakage control, hardware-based and software-based event handling, general purpose I/O, chip select and external SMI.

g) Full System Management Bus (SMBus) interface.

h) Integrated bus-mastering dual full-duplex direct-sound AC97-link-compatible sound system.

I) Plug and Play controller that allows complete steerability of all PCI interrupts and internal interrupts / DMA channels to any interrupt channel. One additional steerable interrupt channel is provided to allow plug and play and reconfigurability of onboard peripherals for Windows family compliance.

The VT8235 Version CE also enhances the functionality of the standard ISA peripherals. The integrated interrupt controller supports both edge and level triggered interrupts channel by channel. The integrated DMA controller supports type F DMA in addition to standard ISA DMA modes. Compliant with the PCI-2.2 specification, the VT8235 Version CE supports delayed transactions and remote power management so that slower ISA peripherals do not block the traffic of the PCI bus. Special circuitry is built in to allow concurrent operation without causing dead lock even in a PCI-to-PCI bridge environment. The chip also includes eight levels (double words) of line buffers from the PCI bus to the ISA bus to further enhance overall system performance.

1.2.5 AC'97 Audio System: Advance Logic, Inc, ALC655

The ALC655 is a 16-bit, full duplex AC'97 2.3 compatible six channels audio CODEC designed for PC multimedia systems, including host/soft audio and AMR/CNR based designs. The ALC655 incorporates proprietary converter technology to meetperformance requirements on PC99/2001 systems. The ALC655 CODEC provides three pairs of stereo outputs with 5-Bitvolume controls, a mono output and multiple stereo and mono inputs, along with flexible mixing, gain and mute functions toprovide a complete integrated audio solution for PCs. The digital interface circuitry of the ALC655 CODEC operates from a 3.3V power supply for use in notebook and PC applications. The ALC655 integrates 50mW/20ohm headset audio amplifiers at Front-Out and Surr-Out, built-in 14.318M 24.576MHz PLL and PCBEEP generator, those can save BOM costs. The ALC655 also supports the S/PDIF input and output function, which can offer easy connection of PCs to consumer electronic products, such as AC3 decoder/speaker and mini disk

devices. ALC655 supports host/soft audio from Intel ICHx chipsets as well as audio controller based VIA/SIS/ALI/AMD/nVIDIA/ATI chipset. Bundled Windows series drivers (WinXP/ME/2000/98/NT), EAX/Direct Sound 3D/ I3DL2/ A3D compatible sound effect utilities (supporting Karaoke, 26-kind of environment sound emulation,10-band equalizer), HRTF 3D positional audio and Sensaura™ 3D (optional) provide an excellent entertainment package and game experience for PC users. Besides, ALC655 includes Realtek's impedance sensing techniques that makes device load on outputs and inputs can be detected.

- Meets performance requirements for audio on PC99/2001 systems
- Meets Microsoft WHQL/WLP 2.0 audio requirements
- 16-bit Stereo full-duplex CODEC with 48KHz sampling rate
- Compliant with AC'97 2.3 specifications
  - 14.318MHz- 24.576MHz PLL to save crystal
  - 12.288MHz BITCLK input can be consumed
  - Integrated PCBEEP generator to save buzzer
  - Interrupt capability
- Three analog line-level stereo inputs with 5-bit volume control: LINE_IN**,** CD, AUX
- High quality differential CD input
- Two analog line-level mono input: PCBEEP, PHONE-IN
- Two software selectable MIC inputs applications (software selectable)
- Boost preamplifier for MIC input
- 50mW/20 amplifier

- External Amplifier Power Down (EAPD) capability
- Power management and enhanced power saving features
- Stereo MIC record for AEC/BF application
- Supports Power Off CD function
- Adjustable VREFOUT control Supports double sampling rate (96KHz) of DVD audio playback
- Support 48KHz of S/PDIF output is compliant with AC'97 rev2.3 specification
- Power support: Digital: 3.3V; Analog: 3.3V/5V

1.2.6 System Flash Memory (BIOS)

- Firmware Hub for Intel® 810, 810E, 815, 815E,815EP, 820, 840, 850 Chipsets
- Flexible Erase Capability
  - Uniform 4 KByte Sectors
  - Uniform 16 KByte overlay blocks for SST49LF002A
  - Uniform 64 KByte overlay blocks for SST49LF004A
  - Top boot block protection
  - 16 KByte for SST49LF002A
  - 64 KByte for SST49LF004A
  - Chip-Erase for PP Mode
- Single 3.0-3.6V Read and Write Operations
- Superior Reliability

- Firmware Hub Hardware Interface Mode
  - 5-signal communication interface supporting byte Read and Write
  - 33 MHz clock frequency operation
  - WP# and TBL# pins provide hardware write protect for entire chip and/or top Boot Block
  - Block Locking Register for all blocks
  - Standard SDP Command Set
  - Data# Polling and Toggle Bit for End-of-Write detection
  - 5 GPI pins for system design flexibility
  - 4 ID pins for multi-chip selection

1.2.7 Memory System

1.2.7.1 64MB, 128MB, 256MB, 512MB (x64) 200-Pin DDR SDRAM SODIMMs

- JEDEC-standard 200-pin, small-outline, dual in-line memory module (SODIMM)
- Utilizes 200 Mb/s and 266 Mb/s DDR SDRAM components
- 64MB (8 Meg x 64 [H]); 128MB (16 Meg x 64, [H] and [HD]); 256MB (32 Meg x 64 [HD]); 512MB (64 Meg x 64 [HD])
- VDD= VDDQ= +2.5V ±0.2V
- VDDSPD = +2.2V to +5.5V
- 2.5V I/O (SSTL_2 compatible)
- Commands entered on each positive CK edge

- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Bidirectional data strobe (DQS) transmitted/received with data—i.e.,source-synchronous data capture
- Differential clock inputs (CK and CK# can be multiple clocks, CK0/CK0#, CK1/CK1#, etc.)
- Four internal device banks for concurrent operation
- Selectable burst lengths: 2, 4 or 8
- Auto precharge option
- Auto Refresh and Self Refresh Modes
- 15.6µs (MT4VDDT864H, MT8VDDT1664HD), 7.8125µs (MT4VDDT1664H, MT8VDDT3264HD, MT8VDDT6464HD) maximum average periodic refresh interval
- Serial Presence Detect (SPD) with EEPROM
- Fast data transfer rates PC2100 or PC1600
- Selectable READ CAS latency for maximum compatibility
- Gold-plated edge contacts

1.2.8 PHY: 3.3-V 10Base-T/100Base-TX Integrated PHY Receiver is a Low-power, Physical-layer Device (PHY)

The VT6103L is a Physical Layer device for Ethernet 10Base-T and 100Base-TX using category 5 Unshielded and Type 1 Shielded cables. This VLSI device is designed for easy implementation of 10 / 100 Mb/s Fast Ethernet LANs. It interfaces to a MAC through an MII interface ensuring interoperability between products from different vendors.

Product Features

- Single Chip 100Base-TX / 10Base-T Physical Layer Solution
- Dual Speed – 100 / 10 Mbps
- Half and Full Duplex
- MII Interface to Ethernet Controller
- MII Interface to Configuration & Status
- Auto Power Saving Mode
- Auto Negotiation: 10 / 100, Full / Half Duplex
- Meet All Applicable IEEE 802.3, 10Base-T and 100Base-Tx Standards
- On Chip Wave Shaping – No External Filters Required
- Adaptive Equalizer
- Baseline Wander Correction
- LED Outputs
  - Link Status
  - Duplex status
  - Speed Status
  - Collision
- 48 Pin LQFP Package

1.2.9 Keyboard System: Winbond W83L950D

The Winbond Keyboard controller architecture consists of a Turbo 51 core controller surrounded by various registers, nine general purpose I/O port, 2k+256 bytes of RAM, four timer/counters, dual serial ports, 40K MTP-ROM that is divided into four banks, two SMBus interface for master and slave, support 4 PWM channels, 2 D-A and 8 A-D converters.

- 8051 uC based
- Keyboard Controller Embedded Controller
- Supply embedded programmable flash memory (internal ROM size: 40KB) and RAM size is 2 KB
- Support 4 Timer (8 bit) signal with 3 prescalers
- Support 2 PWM channels, 2 D-A and 8 A-D converters
- Reduce Firmware burden by Hardware PS/2 decoding
- Support 72 useful GPIOs totally
- Support Flash utility for on board re-flash
- Support ACPI
- Hardware fast Gate A20 with software programmable

1.3 Other Functions

1.3.1 Hot Key Function (TBD)

Keys Combination	Meaning
Fn + F3	Volume Decrease
Fn + F4	Volume Increase
Fn + E5	Toggle Among LCD, External CRT
Fn + F6	LCD Brightness Decrease
Fn + F7	LCD Brightness Increase
Fn + F8	Disable Touchpad
Fn + F10	Mute
Fn + F11	Toggle Between LCD ON and OFF
Fn + F12	Activate Suspend-to-Disk or Suspend-to-RAM
Fn + F1	Enable/Disable WLAN

1.3.2 Power on/off/Suspend/Resume Button

APM mode

At APM mode, Power button is on/off system power.

ACPI mode

At ACPI mode. Windows power management control panel set power button behavior.
You could set “standby”, “power off” or “hibernate”(must enable hibernate function in power Management) to power button function.

Continue pushing power button over 4 seconds will force system off at ACPI mode.

1.3.3 Cover Switch

System automatically provides power saving by monitoring Cover Switch. It will save battery power and prolong the usage time when user closes the notebook cover.

At ACPI mode there are four functions to be chosen at windows power management control panel.

1. None
2. Standby
3. Off
4. Hibernate (must enable hibernate function in power management)

1.3.4 LED Indicators

1.3.4.1 Three LED Indicators

There are 2 sets of 3 LED indicators on panel housing and above keyboard separately.

From left to right that indicate WIRELESS LAN, POWER, BATTERY STATUS

Wireless LAN

This LED lights green when operated in wireless LAN mode, otherwise it turns off.

Power

This LED lights green when the notebook was powered by AC power line or Battery, Flashes (on 1 second, off 1 second) when entered suspend to RAM state. The LED is off when the notebook is in power off state.

Battery Status

During normal operation, this LED stays off as long as the battery is charged. When the battery charge drops to 10% of capacity, the LED lights red, flashes per 1 second and beeps per 2 second. When AC is connected, this indicator glows green if the battery pack is fully charged or orange (amber) if the battery is being charged.

1.3.4.2 Five LED Indicators

System has 4 status LED indicators at front side which to display system activity. From left to right that indicate HARD DISK, NUM LOCK, CAPS LOCK, SCROLL LOCK.

1.3.5 Battery Status

1.3.5.1 Battery Warning

System also provides Battery capacity monitoring and gives users a warning signal to alarm they to store data before battery dead. This function also protects system from mal-function while battery capacity is low.

Battery Warning: Capacity below 10%, Battery Capacity LED flashes per second, system beeps per 2 seconds.

System will Suspend to HDD after 2 Minutes to protect users data.

1.3.5.2 Battery Low State

After Battery Warning State and battery capacity is below 5%, system will generate beep sound for twice per second.

1.3.5.3 Battery Dead State

When the battery voltage level reaches 11.5 volts, system will shut down automatically in order to extend the battery packs' life.

1.3.6 Fan Power on/off Management

FAN is controlled by W83L950D embedded controller-using ADT7460 to sense CPU temperature and PWM control fan speed. Fan speed is depended on CPU temperature. Higher CPU temperature faster Fan Speed.

1.3.7 CMOS Battery

CR2032 3V 220mAh lithium battery

When AC in or system main battery inside, CMOS battery will consume no power

AC or main battery not exists, CMOS battery life at less (220mAh/5.8uA) 4 years

1.3.8 I/O Port

One Power Supply Jack.

One External CRT Connector For CRT Display

Supports four USB port for all USB devices

One RJ-45 for LAN

Headphone Out Jack

Microphone Input Jack

1.3.9 Battery Current Limit and Learning

Implanted H/W current limit and battery learning circuit to enhance protection of battery

1.4 Power Management

The 8965 system has built in several power saving modes to prolong the battery usage for mobile purpose. User can enable and configure different degrees of power management modes via ROM CMOS setup (booting by pressing F2 key). Following are the descriptions of the power management modes supported.

1.4.1 System Management Mode

Full on Mode

In this mode, each device is running with the maximal speed. CPU clock is up to its maximum.

Doze Mode

In this mode, CPU will be toggling between on & stop grant mode either. The technology is clock throttling. This can save battery power without loosing much computing capability.

The CPU power consumption and temperature is lower in this mode.

Standby Mode

For more power saving, it turns off the peripheral components. In this mode, the following is the status of each device:

- CPU: stop grant
- LCD: backlight off
- HDD: spin down

Suspend to DRAM and HDD

The most chipset of the system is entering power down mode for more power saving. In this mode, the following is the status of each device

- Suspend to DRAM
  - CPU: off
  - Intel 855GME: partial off
  - VGA: suspend
  - PCMCIA: suspend
  - Audio: off
  - SDRAM: self refresh
- Suspend to HDD
  - All devices are stopped clock and power-down
  - System status is saved in HDD
  - All system status will be restored when powered on again

1.4.2 Other Power Management Functions

HDD & Video Access

System has the ability to monitor video and hard disk activity. User can enable monitoring function for video and/or hard disk individually. When there is no video and/or hard disk activity, system will enter next PMU state depending

on the application. When the VGA activity monitoring is enabled, the performance of the system will have some impact.

1.5 Appendix 1: VIA VT8235CE GPI/O Pin Definitions (1)

Pin name	MUX Function	GPIO Function	Power plane
GPI0	B/CB#	GPI	
GPO0	WIRELESS_PD#	GPO	
GPI1	SCI#	GPI	
GPO1	SUSA#	GPO	
GPI2	EXTSMI#	GPI	
GPO2	SUSB#	GPO	
GPI3	WAKE_UP#	GPI	
GPO3	SUSST#	GPO	
GPI4	LIDSW#	GPI4	
GPO4	SPK_OFF	GPO	
GPI5	CARD_RI#	GPI	
GPO5	CPU_STP#	GPO	
GPI6	AGPBUSY#	GPI	
GPO6	PCI_STP#	GPO	
GPI7	PCI_REQ5#	GPI	
GPO7	PCI_GNT5#	GPO	
GPIO12	PCI_INTE#	GPIO	

1.5 Appendix 1: VIA VT8235CE GPI/O Pin Define (2)

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Pin name	MUX Function	GPIO Function	Power plane
GPIO13	KBD_US/JP#	GPIO	
GPIO14	CRT_IN#	GPIO	
GPIO15	ENABKL_SB	GPIO	
GPI16	X	GPI	
GPI17	X	GPI	
GPI18	SB_THRM#	GPI	
GPIO20	X	GPIO	
GPIO21	X	GPIO	
GPIO22	MINIPCI_ACT#	GPIO	
GPIO23	HDPSLP#	GPIO	
GPIO26	SMBDATA2	GPIO	
GPIO27	SMBCLK2	GPIO	
GPIO28	X	GPIO	
GPIO29	DPRSLPVR	GPIO	

1.6 Appendix 2: W83L950D KBC Pins Definitions (1)

Port	pin	Function	Implement
P0	0-7	Scan matrix	KO[0..7]
P1	0-7		KO[8..15]
P3	0-7		KI[0..7]
P2	0	LPC enable	H8_THRM#
	1	GPIO x1	H8_WAKE_UP#
	2	SMBUS1 or UART	BATT_G#
	3		BATT_R#
	4	GPIO x4	EXTSMI#
	5		CAP#
	6		NUM#
	7		SCROLL#
P4	0	Xcin/cout or PWM 2,3	H8_ENABKL
	1		CHARGING
	2	GPIO x2 (INT1)	LEARING
	3		H8_SUSB
	4	KBRST	H8_HRCIN#
	5	GPIO x2	H8_SCI
	6		H8_PWRON
P5	0	GPIO x1	SW_VDD3
	1	GPIO x3 (INT20,30,40)	H8_LIDSW#
	2		BATT_DEAD#
	3		H8_ADEN#
	4	GPIO x2	BATT_LED#
	5		KBC_PWRON_VDD3S
	6	D/A, PWM 2,3	BLADJ
	7		H8_I_CTR

1.6 Appendix 2: W83L950D KBC Pins Definitions (2)

Continue to the previous page

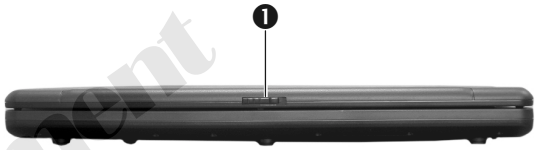
Port	pin	Function	Implement
P6	0	A/D (INT5-12)	PWRBTN#
	1		KBC_RI#
	2		AC_POWER#
	3		BATT_V
	4		BATT_T
	5		H8_I_LIMIT
	6		H8_PROCHOT#
	7		+BC_CPUCORE
P7	0	PS/2 port x3	T_DATA
	1		H8_RSMRST
	2		ICH_PWRBTN
	3		T_CLK
	4		H8_PWRON_SUSB#
	5		SUSC#
	6	SMBUS	BAT_DATA
	7		BAT_CLK
P8	0	LPC interface	PCICLK_KBC
	1		SERIRQ
	2		LAD3
	3		LAD2
	4		LAD1
	5		LAD0
	6		KBC_PCIRST#
	7		LFRAME#

2. System View and Disassembly

2.1 System View

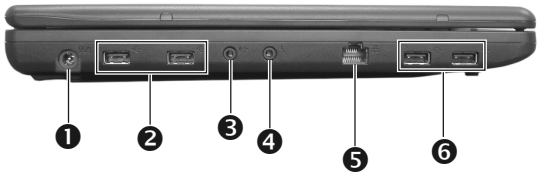
2.1.1 Front View

❶ Top Cover Latch



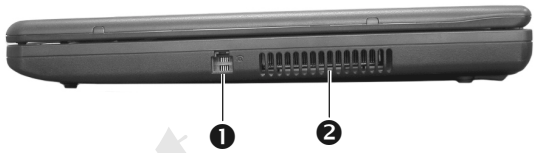
2.1.2 Left-side View

❶ AC Power Connector
❷ USB Ports *2
❸ Line Out Connector
❹ MIC In Connector
❺ RJ-45 Connector
❻ USB Ports *2



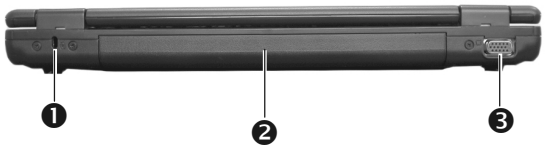
2.1.3 Right-side View

❶ RJ-11 Connector
❷ Ventilation Openings



2.1.4 Rear View

❶ Lock
❷ Battery Pack
❸ VGA Port



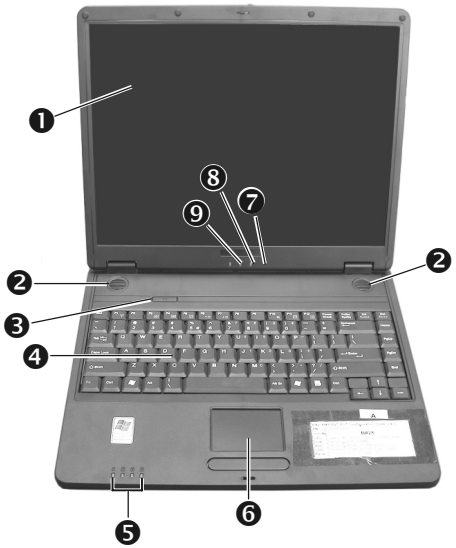
8965 N/B Maintenance

2.1.5 Bottom View

❶ Hard Disk Drive
❷ DDR-SDRAM
❸ CPU
❹ Battery Park

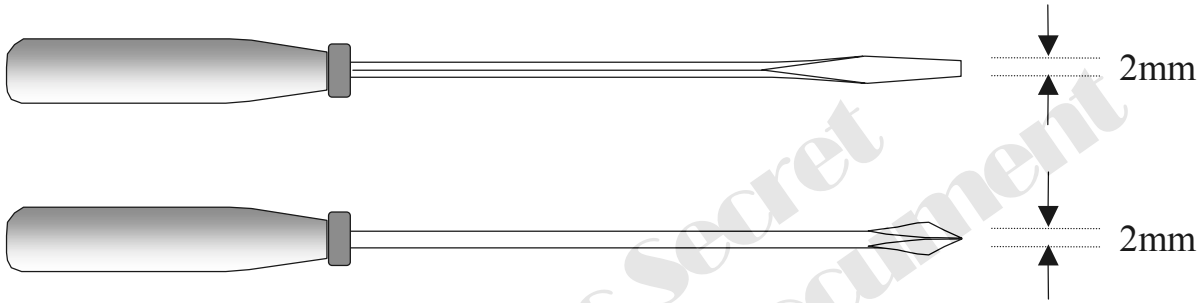
2.1.6 Top-open View

❶ LCD Screen
❷ Stereo Speaker Set
❸ Power Button
❹ Keyboard
❺ Device LED Indicators
❻ Touch Pad
❼ Battery Charge Indicator
❽ AC Power Indicator
❾ Wireless Indicator

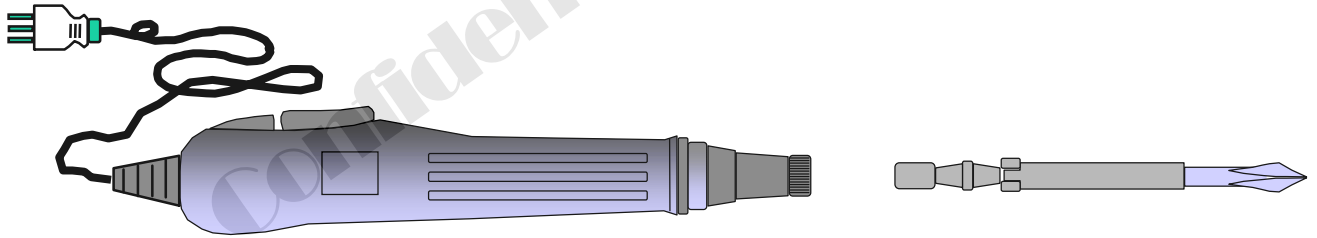


2.2 Tools Introduction

1. Minus screw driver with bit size 2mm for notebook assembly & disassembly.



2. Auto screw driver for notebook assembly & disassembly.



Bit Size

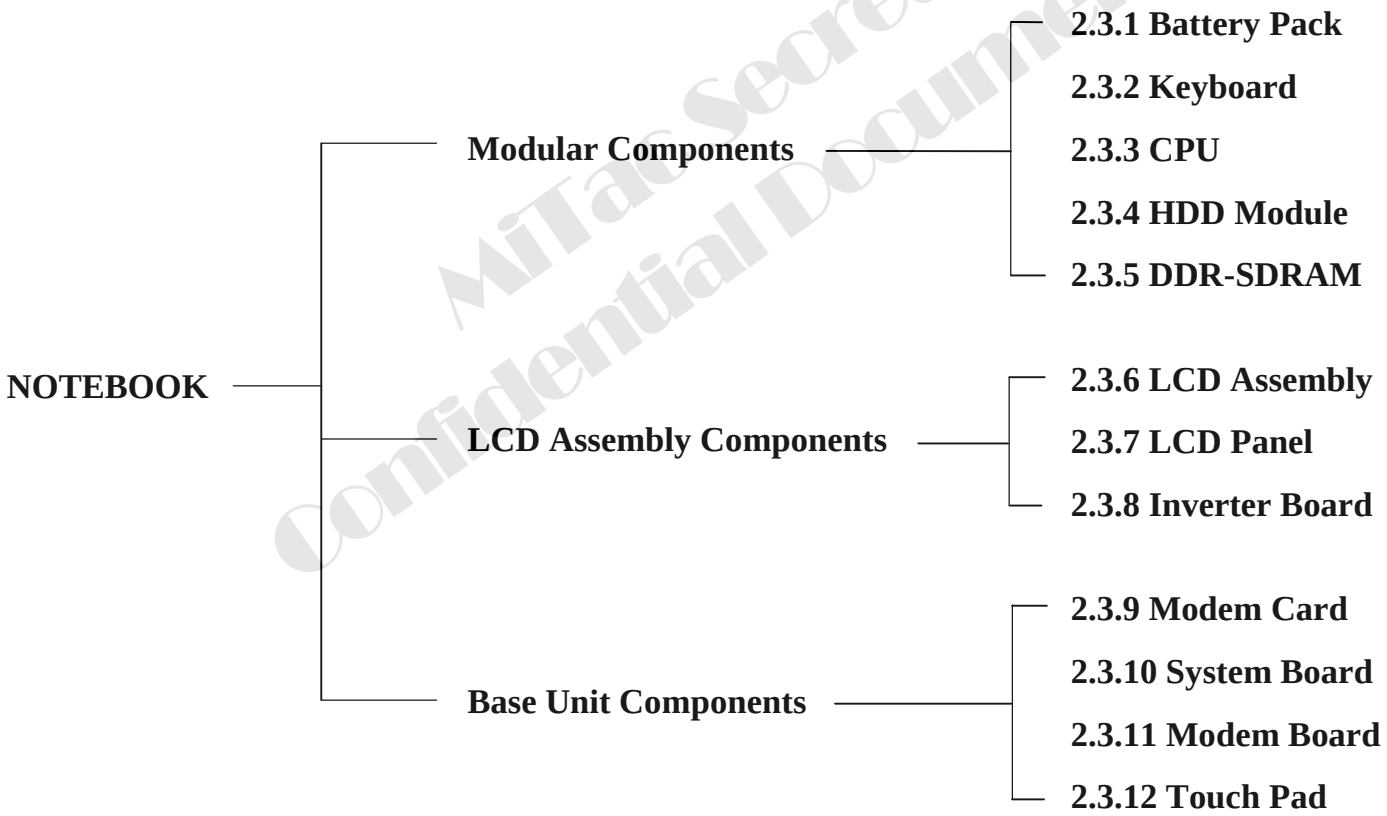
#0

Screw Size	Tooling	Tor.	Bit Size
1. M2.0	Auto-Screw driver	2.0-2.5 kg/cm2	#0

2.3 System Disassembly

The section discusses at length each major component for disassembly/reassembly and show corresponding illustrations.Use the chart below to determine the disassembly sequence for removing components from the notebook.

NOTE: *Before you start to install/replace these modules, disconnect all peripheral devices and make sure the notebook is not turned on or connected to AC power.*



2.3.1 Battery Pack

Disassembly

1. Carefully put the notebook upside down.
2. Slide the two release lever outwards to the "unlock" ( ) position (❶), while take the battery pack out of the compartment (❷). (Figure 2-1)

Figure 2-1 Remove the battery pack

Reassembly

1. Replace the battery pack into the compartment. The battery pack should be correctly connected when you hear a clicking sound.
2. Slide the release lever to the "lock" ( ) position.

2.3.2 Keyboard

Disassembly

1. Remove the battery pack. (Refer to section 2.3.1 Disassembly)
2. Push the keyboard cover to loose the locks from the battery compartment. (Figure 2-2)
3. Lift the keyboard cover up. (Figure 2-3)

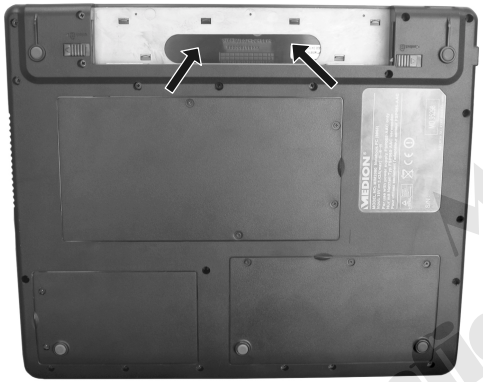


Figure 2-2 Push the keyboard cover

Figure 2-3 Lift the keyboard cover

4. Slightly lift up the keyboard. (Figure 2-4)
5. Disconnect the cable from the system board, then separate the keyboard. (Figure 2-5)

Figure 2-4 Lift the keyboard

Figure 2-5 Disconnect the cable

Reassembly

1. Reconnect the keyboard cable and fit the keyboard back into place.
2. Replace the keyboard cover.
3. Replace the battery pack. (Refer to section 2.3.1 Reassembly)

2.3.3 CPU

Disassembly

1. Remove the battery pack. (Refer to section 2.3.1 Disassembly)
2. Remove the four screws fastening the CPU cover. (Figure 2-6)
3. Remove the four spring screws and two screws that secure the heatsink upon the CPU and disconnect the fan's power cord from the system board. (Figure 2-7)

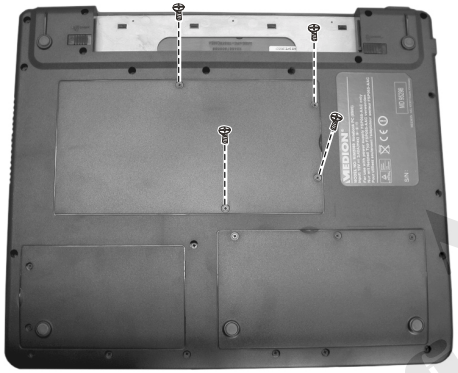


Figure 2-6 Remove the four screws

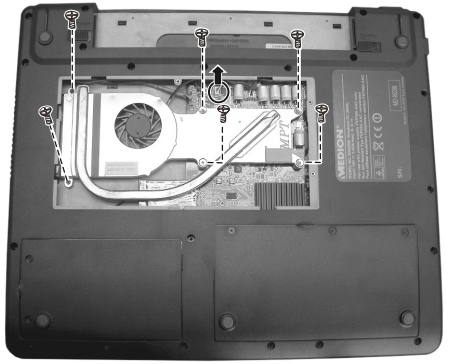


Figure 2-7 Free the heatsink

4. To remove the existing CPU, loosen the screw by a flat screw driver, upraise the CPU socket to unlock the CPU. (Figure 2-8)

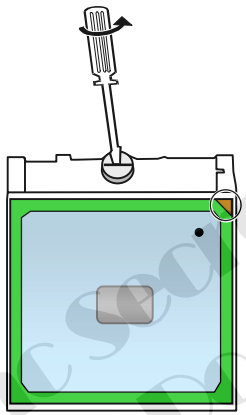


Figure 2-8 Remove the CPU

Reassembly

1. Carefully, align the arrowhead corner of the CPU with the beveled corner of the socket, then insert CPU pins into the holes. Tighten the screw by a flat screwdriver to locking the CPU.
2. Connect the fan's power cord to the system board, fit the heatsink upon the CPU, then secure with four spring screws and two screws.
3. Replace the CPU cover and secure with four screws.
4. Replace the battery pack. (Refer to section 2.3.1 Reassembly)

2.3.4 HDD Module

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (Refer to section 2.3.1 Disassembly)
2. Remove the two screws fastening the HDD compartment cover. (Figure 2-9)
3. Remove the one screw and slide the HDD module out of the compartment. (Figure 2-10)

Figure 2-9 Remove the HDD compartment cover

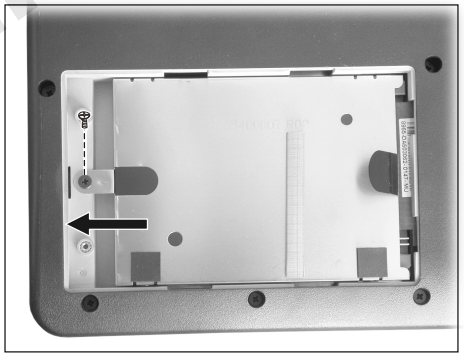


Figure 2-10 Remove HDD module

4. Remove the four screws to separate the hard disk drive from the bracket, remove the hard disk drive. (Figure 2-11)

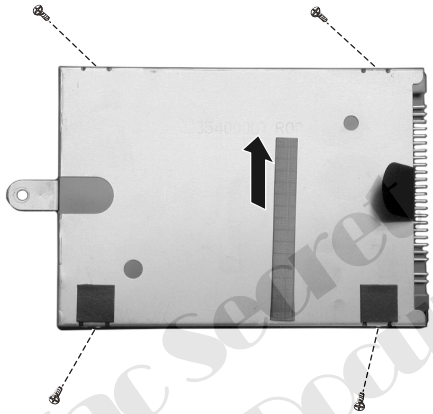


Figure 2-11 Remove hard disk drive

Reassembly

1. Attach the bracket to hard disk drive and secure with four screws.
2. Slide the HDD module into the compartment and secure with one screw.
3. Place the HDD compartment cover and secure with two screws.
4. Replace the battery pack. (Refer to section 2.3.1 Reassembly)

2.3.5 DDR-SDRAM

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (See section 2.3.1 Disassembly)
2. Remove the three screws fastening the DDR cover. (Figure 2-12)

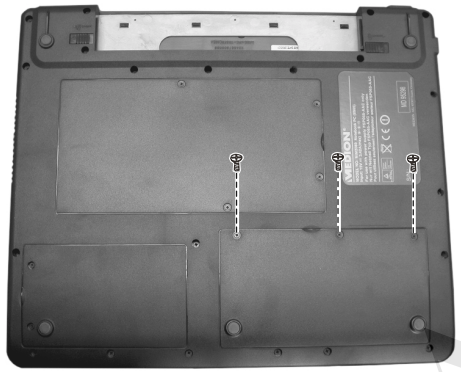


Figure 2-12 Remove the three screws

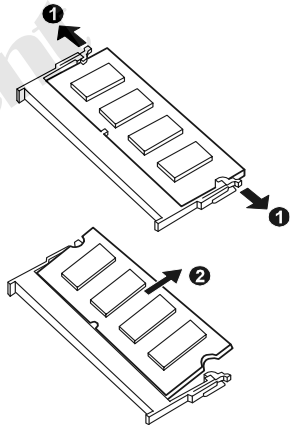


Figure 2-13 Remove the SO-DIMM

3. Pull the retaining clips outwards (❶) and remove the SO-DIMM (❷). (Figure 2-13)

Reassembly

1. To install the DDR, match the DDR's notched part with the socket's projected part and firmly insert the SO-DIMM into the socket at 20-degree angle. Then push down until the retaining clips lock the DDR into position.
2. Replace the DDR cover and secure with three screws.
3. Replace the battery pack. (See section 2.3.1 Reassembly)

2.3.6 LCD ASSY

Disassembly

1. Remove the battery pack and keyboard. (See sections 2.3.1 and 2.3.2 Disassembly)
2. Remove the CPU cover. (Refer to the step 2 of section 2.3.3 Disassembly)
3. Remove the DDR cover. (Refer to the step 2 of section 2.3.5 Disassembly)
4. Separate the antenna from the system board. And disconnect the inverter board's cable from the system board. (Figure 2-14)
5. Remove the two hinge covers. (Figure 2-15)

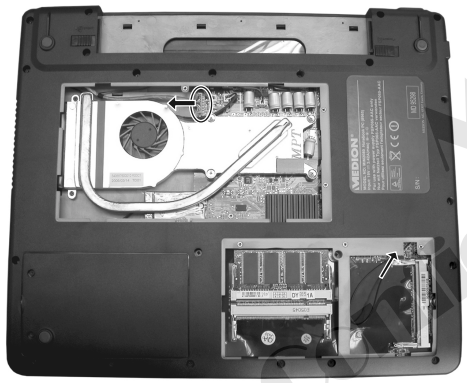


Figure 2-14 Separate the antenna and disconnect the cable

Figure 2-15 Remove the two hinge covers

6. Disconnect the cable from the system board, then separate the inverter board's cable and the antenna from the housing. (Figure 2-16)
7. Remove the four screws, then free the LCD assembly. (Figure 2-17)

Figure 2-16 Free the cables

Figure 2-17 Free the LCD assembly

Reassembly

1. Attach the LCD assembly to the base unit and secure with four screws.
2. Replace the antenna back into Mini PCI compartment.
3. Reconnect the two cables to the system board.
4. Replace the two hinge covers.
5. Replace the DDR cover. (Refer to the step 2 of section 2.3.5 Reassembly)
6. Replace the CPU cover. (Refer to the step 3 of section 2.3.3 Reassembly)
7. Replace the keyboard and battery pack. (Refer to sections 2.3.2 and 2.3.1 Reassembly)

2.3.7 LCD Panel

Disassembly

1. Remove the battery, keyboard and LCD assembly. (Refer to section 2.3.1, 2.3.2 and 2.3.6 Disassembly)
2. Remove the two rubber pads and two screws on the corners of the panel. (Figure 2-18)
3. Insert a flat screwdriver to the lower part of the LCD cover and gently pry the frame out. Repeat the process until the cover is completely separated from the housing.
4. Remove the eight screws and disconnect the cable. (Figure 2-19)

Figure 2-18 Remove LCD cover

Figure 2-19 Remove the eight screws and disconnect the cable

5. Remove the four screws that secure the LCD brackets. (Figure 2-20)
6. Disconnect the cable to free the LCD panel. (Figure 2-21)

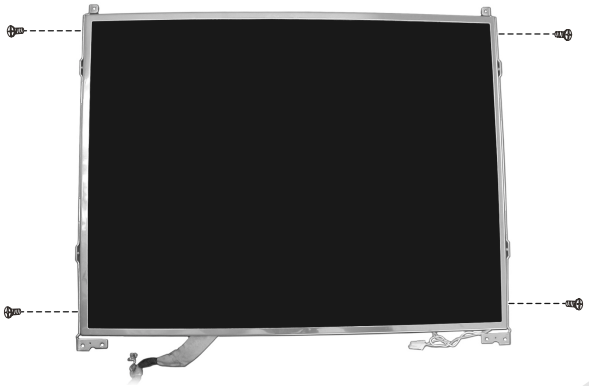


Figure 2-20 Remove the four screws

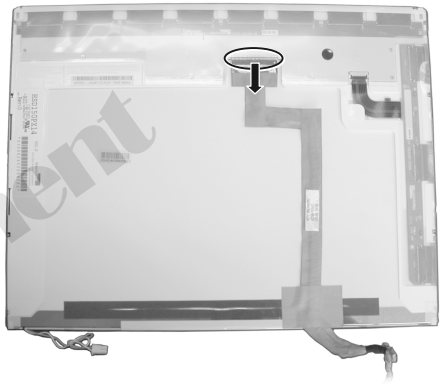


Figure 2-21 Free the LCD panel

Reassembly

1. Replace the cable to the LCD panel.
2. Attach the LCD panel's brackets back to LCD panel and secure with four screws.
3. Replace the LCD panel into LCD housing and secure with eight screws.
4. Reconnect one cable to inverter board.
5. Fit the LCD cover and secure with two screws and rubber pads.
6. Replace the LCD assembly, keyboard and battery pack. (See sections 2.3.6, 2.3.2 and 2.3.1 Reassembly)

2.3.8 Inverter Board

Disassembly

1. Remove the battery, keyboard and LCD assembly. (Refer to section 2.3.1, 2.3.2 and 2.3.6 Disassembly)
2. Remove the LCD cover. (Refer to the steps 1-3 of section 2.3.7 Disassembly)
3. Remove the two screws fastening the inverter board and disconnect the cable, then free the inverter board. (Figure 2-22)

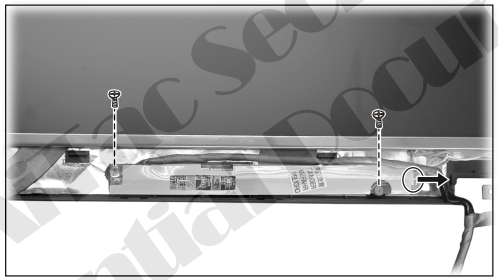


Figure 2-22 Free the inverter board

Reassembly

1. Reconnect the cable. Fit the inverter board back into place and secure with two screws.
2. Replace the LCD cover. (Refer to section 2.3.7 Reassembly)
3. Replace the LCD assembly. (Refer to section 2.3.6 Reassembly)
4. Replace the keyboard and battery pack. (Refer to sections 2.3.2 and 2.3.1 Reassembly)

2.3.9 Modem Card

Disassembly

1. Remove the battery, keyboard, CPU, hard disk drive, DDR and LCD assembly. (Refer to sections 2.3.1, 2.3.2, 2.3.3, 2.3.4, 2.3.5 and 2.3.6 Disassembly)
2. Remove the three screws fastening the housing. (Figure 2-23)
3. Disconnect the (L&R) speakers' cables from the system board and remove the twenty-two screws fastening the housing, then free the housing. (Figure 2-24)

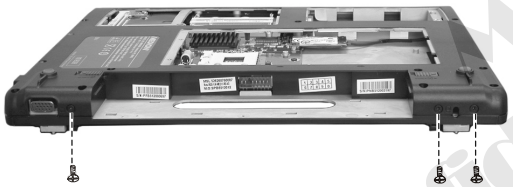


Figure 2-23 Remove the three screws

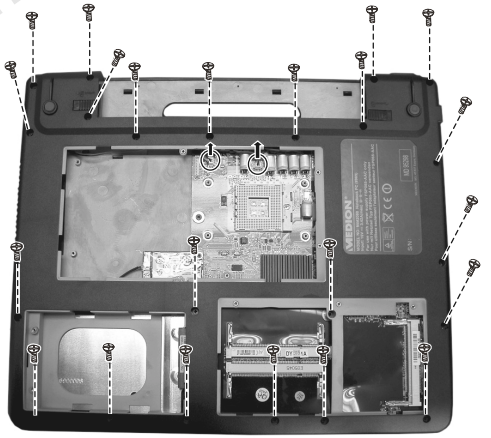


Figure 2-24 Free the housing

4. Disconnect the modem card's cable, then remove the two screws and free the modem card. (Figure 2-25)

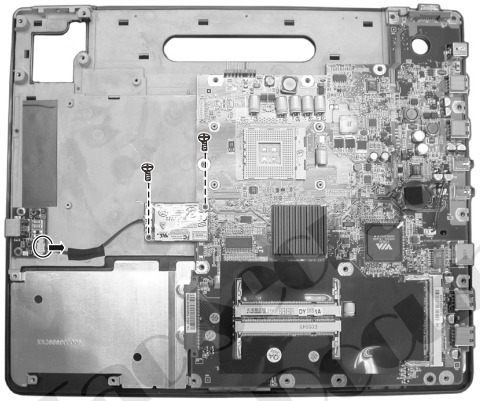


Figure 2-25 Free the modem card

Reassembly

1. Replace the modem card into the system board and secure with two screws.
2. Reconnect the modem card's cable into the modem board.
3. Replace the housing and secure with twenty-five screws.
4. Reconnect the (L&R) speakers' cables into the system board.
5. Replace the LCD assembly, DDR, hard disk drive, CPU, keyboard and battery pack. (Refer to previous section reassembly)

2.3.10 System Board

Disassembly

1. Remove the battery, keyboard, CPU, hard disk drive, DDR, LCD assembly and modem card. (Refer to sections 2.3.1, 2.3.2, 2.3.3, 2.3.4, 2.3.5, 2.3.6 and 2.3.9 Disassembly)
2. Disconnect the touch pad's cable from the system board. (Figure 2-26)
3. Remove the four screws fastening the system board and free the system board. (Figure 2-27)

Figure 2-26 Disconnect the cable

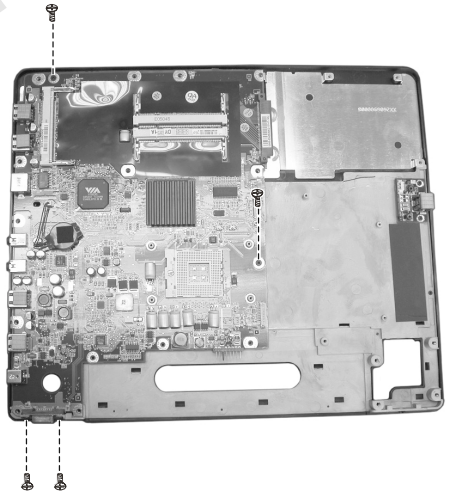


Figure 2-27 Free the system board

Reassembly

1. Replace the system board into the top cover and secure with four screws.
2. Turn over the base unit, then reconnect the touch pad's cable.
3. Replace modem card, LCD assembly, DDR, DDR, hard disk drive, CPU, keyboard and battery pack. (Refer to previous section reassembly)

2.3.11 Modem Board

Disassembly

1. Remove the battery, keyboard, CPU, hard disk drive, DDR, LCD assembly and modem card. (Refer to sections 2.3.1, 2.3.2, 2.3.3, 2.3.4, 2.3.5, 2.3.6 and 2.3.9 Disassembly)
2. Remove the two screws fastening the modem board and free the modem board. (Figure 2-28)

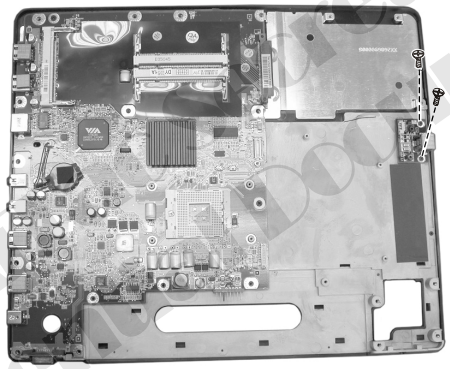


Figure 2-28 Free the modem board

Reassembly

1. Replace the modem board into the top cover and secure with two screws.
2. Replace the modem card, LCD assembly, DDR, DDR, hard disk drive, CPU, keyboard and battery pack. (Refer to previous section reassembly)

2.3.12 Touch Pad

Disassembly

1. Remove the battery pack, keyboard, CPU, hard disk drive, DDR, LCD assembly, modem card and the system board. (See sections 2.3.1, 2.3.2, 2.3.3, 2.3.4, 2.3.5, 2.3.6, 2.3.9 and 2.3.10 Disassembly)
2. Remove the four screws and lift the shielding, then free the touch pad. (Figure 2-29)

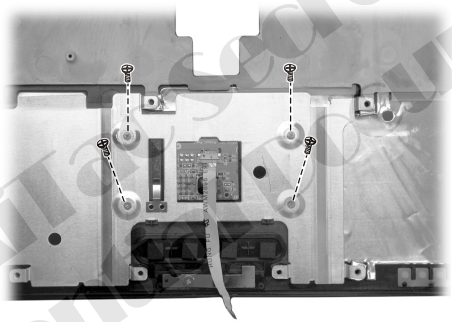


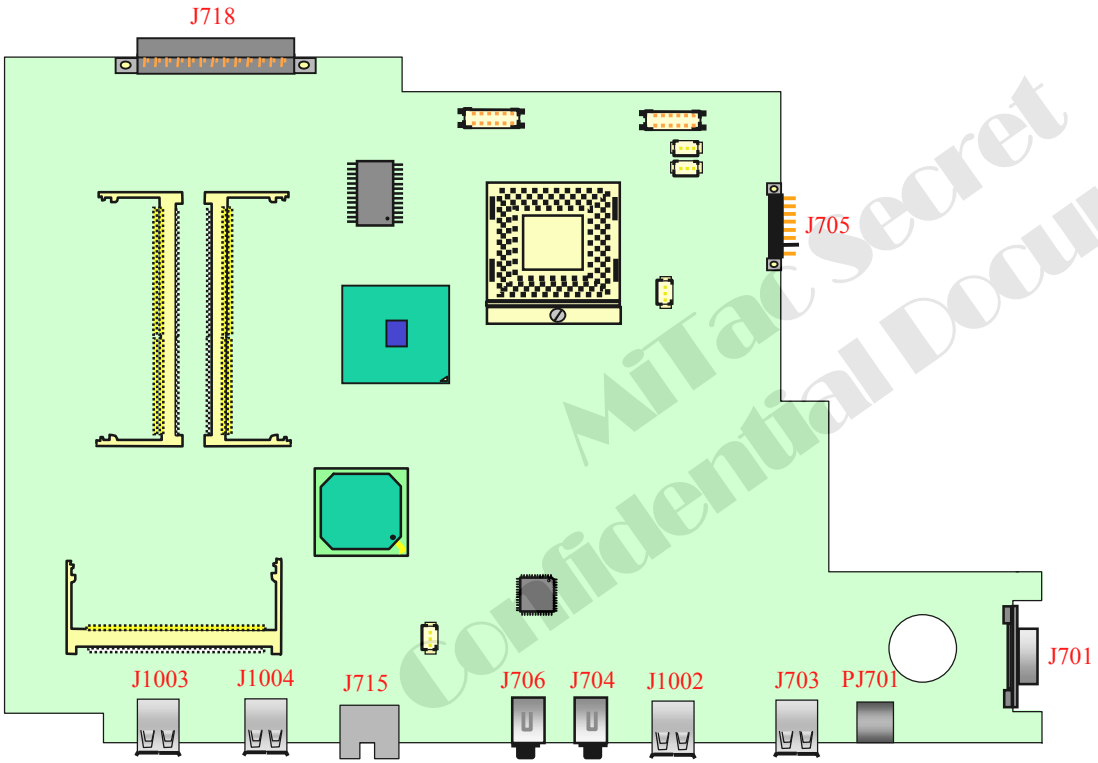
Figure 2-29 Free the touch pad

Reassembly

1. Replace the touch pad, then fit the shielding and secure with four screws.
2. Replace the battery pack, keyboard, CPU, hard disk drive, DDR, LCD assembly, modem card and the system board. (See sections previous section reassembly)

3. Definition & Location of Connectors / Switches

3.1 Mother Board (Side A) - 1

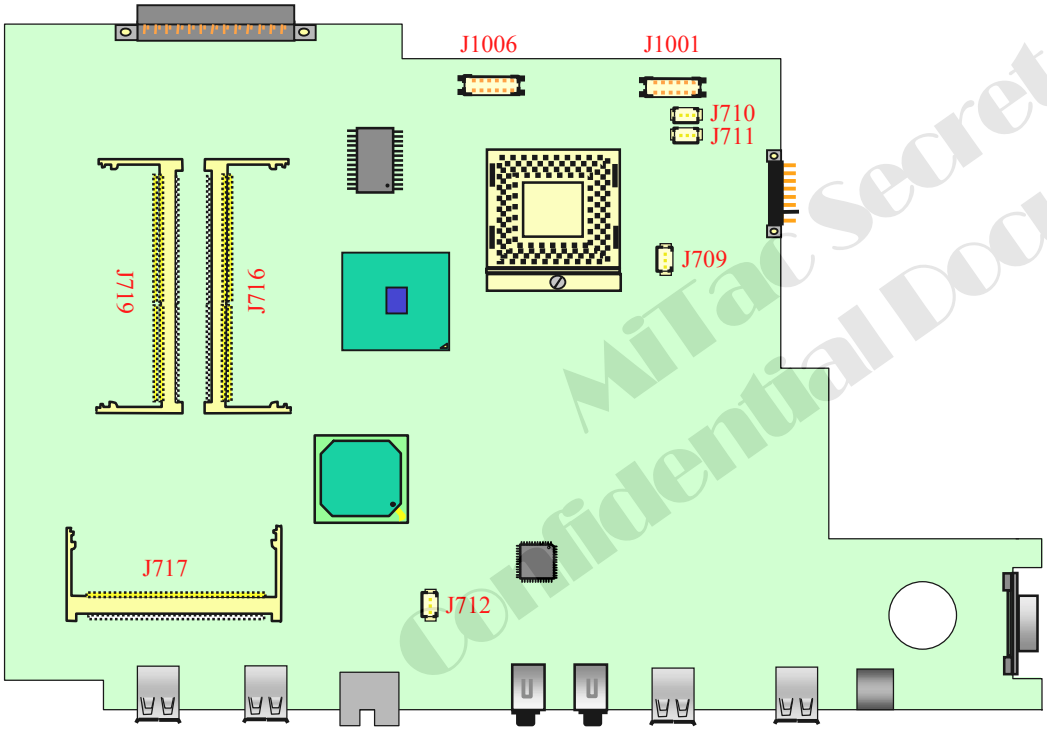


- PJ701 : Power Jack
- J701 : External VGA Connector
- J703,J1002 : USB Port
- J704 : Line Out Jack
- J705 : Battery Connector
- J706 : MIC In Jack
- J715 : RJ45 Connector
- J718 : HDD Connector
- J1003,J1004 : USB Port

------ To next page ------

3. Definition & Location of Connectors / Switches

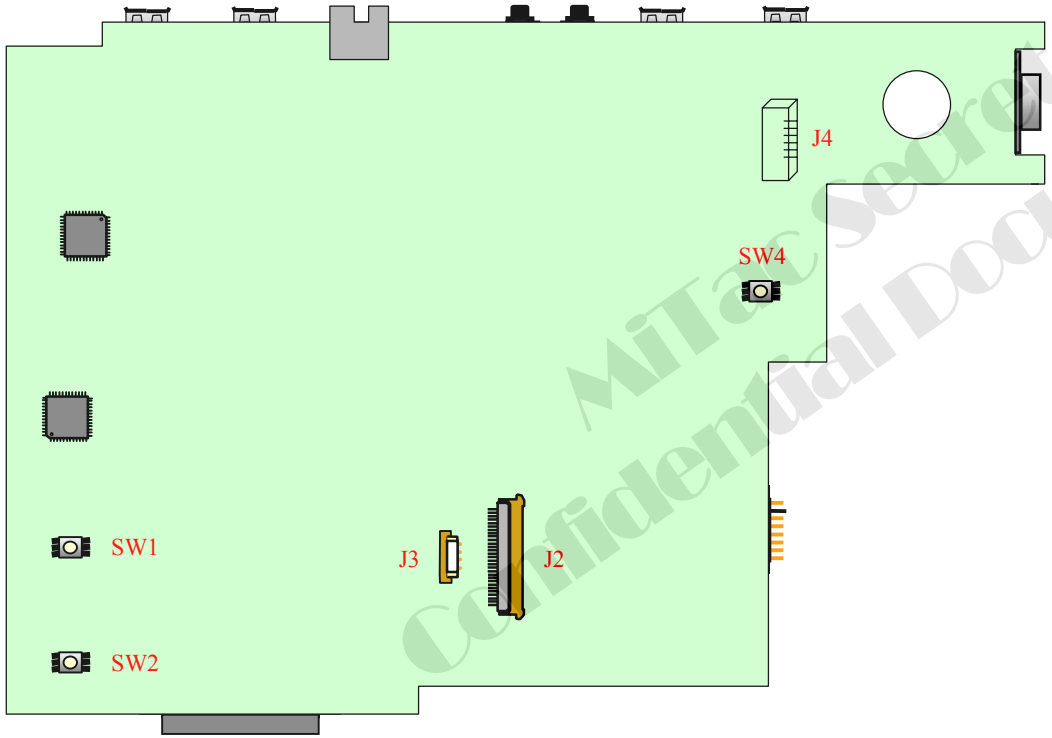
3.1 Mother Board (Side A) - 2



- J1001 : Inverter Board Connector
- J1006 : MDC Jump Wire Connector
- J709 : Internal Left Speaker Connector
- J710 : Internal Right Speaker Connector
- J711 : CPU Fan Connector
- J712 : RTC Battery Connector
- J716,J719 : DDR_SODIMM Socket
- J717 : Mini PCI Socket

3. Definition & Location of Connectors / Switches

3.1 Mother Board (Side B)

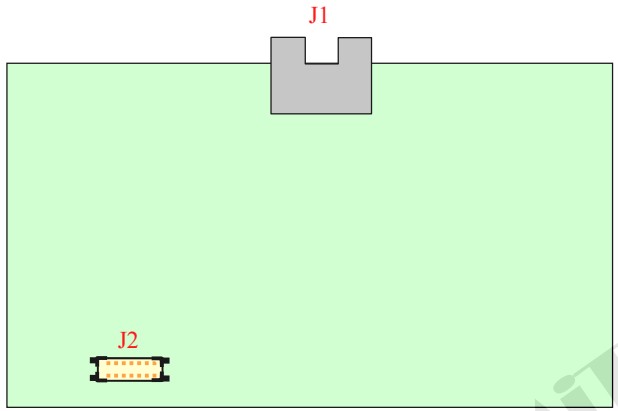


- J2 : Internal Keyboard Connector
- J3 : Touch-Pad Connector
- J4 : LCD Connector

- SW1 : Touch-Pad Left Button
- SW2 : Touch-Pad Right Button
- SW4 : Power Button

3. Definition & Location of Connectors / Switches

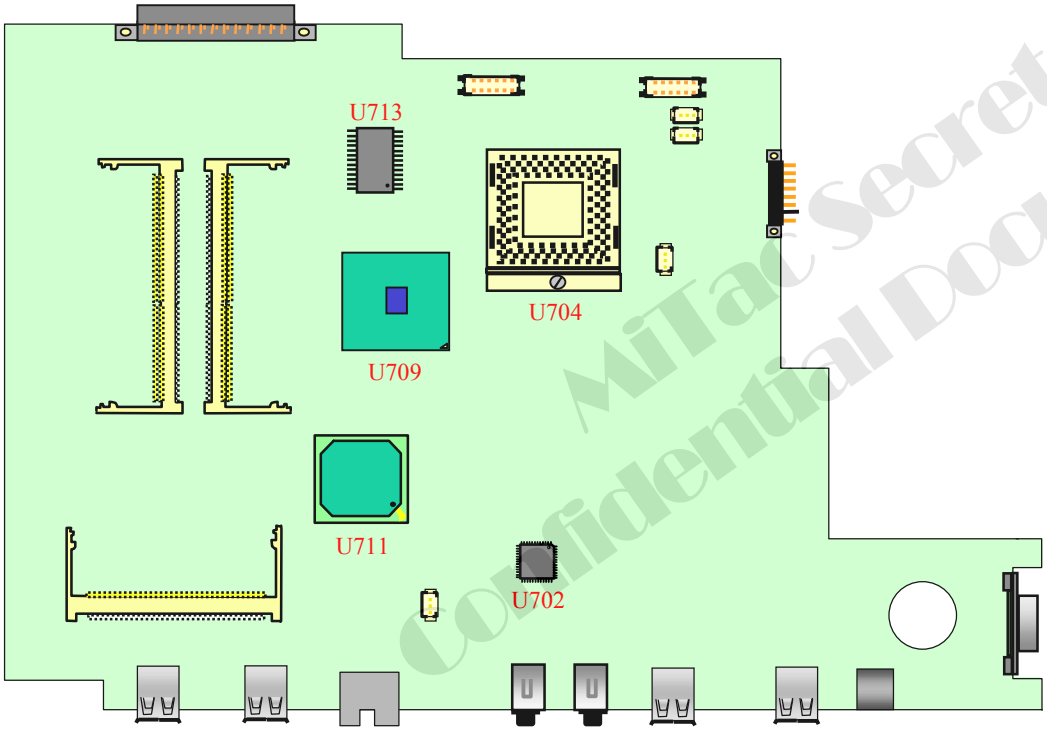
3.2 Modem Board (Side A)



- J1 : RJ11 Connector
- J2 : MDC Board Connector

4. Definition & Location of Major Components

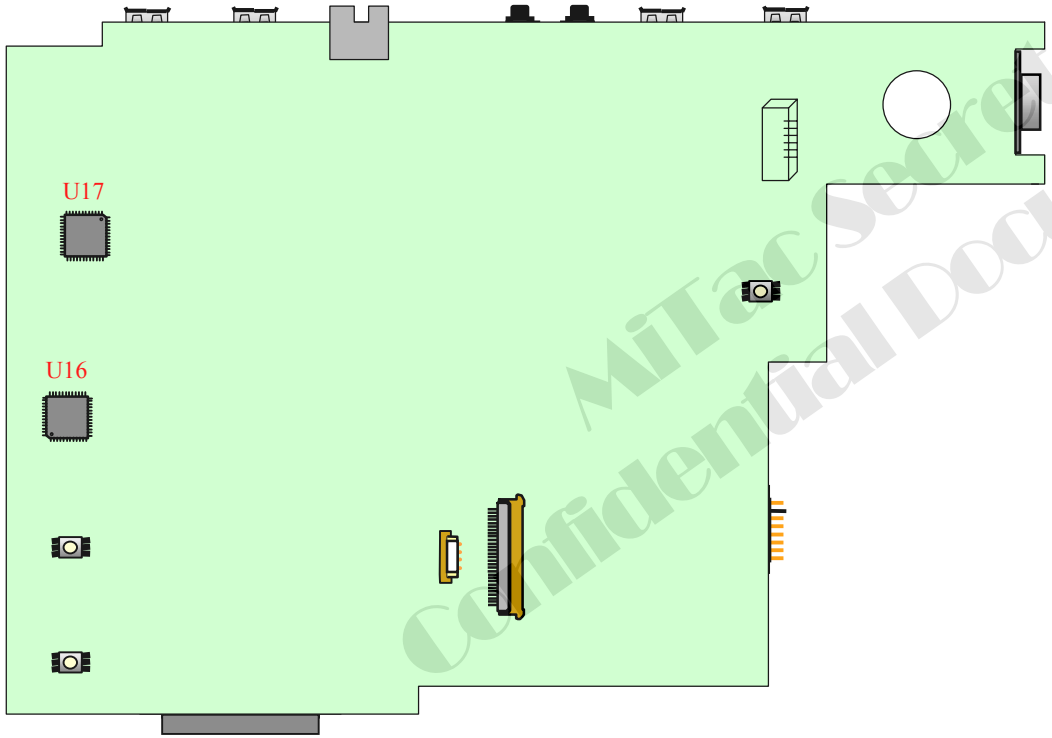
4.1 Mother Board (Side A)



- U702 : ALC655 Audio Codec
- U704 : CPU (Pentium-M/Celeron-M) Socket
- U709 : NB VIA PN800
- U711 : SB VIA VT8235CE
- U713 : ICS950902 Clock Generator

4. Definition & Location of Major Components

4.1 Mother Board (Side B)



U16 : System BIOS

U17 : KBC (W83L950D)

5. Pin Descriptions of Major Components

5.1 Intel Pentium M Processor CPU - 1

CPU Pin Description

`Signal Name	Type	Description
A[31:3]#	I/O	A[31:3]# (Address) define a 2 32 -byte physical memory address space. In sub-phase 1 of the address phase, these pins transmit the address of a transaction. In sub-phase 2, these pins transmit transaction type information. These signals must connect the appropriate pins of both agents on the Intel Pentium M processor system bus. A[31:3]# are source synchronous signals and are latched into the receiving buffers by ADSTB[1:0]#. Address signals are used as straps which are sampled before RESET# is deasserted.
A20M#	I	If A20M# (Address-20 Mask) is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-Mbyte boundary. Assertion of A20M# is only supported in real mode. A20M# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.
ADS#	I/O	ADS# (Address Strobe) is asserted to indicate the validity of the transaction address on the A[31:3]# and REQ[4:0]# pins. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction.
ADSTB[1:0]#	I/O	Address strobes are used to latch A[31:3]# and REQ[4:0]# on their rising and falling edges. Strobes are associated with signals as shown below. Signals / Associated Strobe REQ[4:0]#, A[16:3]# / ADSTB[0]# A[31:17]# / ADSTB[1]#
BCLK[1:0]	I	The differential pair BCLK (Bus Clock) determines the system bus frequency. All processor system bus agents must receive these signals to drive their outputs and latch their inputs.
BNR#	I/O	BNR# (Block Next Request) is used to assert a bus stall by any bus agent that is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions.
BPM[2:0]# **BPM[3]**	O I/O	BPM[3:0]# (Breakpoint Monitor) are breakpoint and performance monitor signals. They are outputs from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance. BPM[3:0]# should connect the appropriate pins of all Intel Pentium M processor system bus agents. This includes debug or performance monitoring tools.

CPU Pin Description (Continued)

Signal Name	Type	Description
BPRI#	I	BPRI# (Bus Priority Request) is used to arbitrate for ownership of the processor system bus. It must connect the appropriate pins of both processor system bus agents. Observing BPRI# active (as asserted by the priority agent) causes the other agent to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed, then releases the bus by deasserting BPRI#.
BR0#	I/O	BR0# is used by the processor to request the bus. The arbitration is done between the Intel Pentium M processor (Symmetric Agent) and the MCH-M (High Priority Agent) of the Intel 855PM or Intel 855GM chipset.
COMPP3:0]	Analog	COMP[3:0] must be terminated on the system board using precision (1% tolerance) resistors. Refer to the platform design guides for more implementation details.
D[63:0]#	I/O	D[63:0]# (Data) are the data signals. These signals provide a 64-bit data path between the processor system bus agents, and must connect the appropriate pins on both agents. The data driver asserts DRDY# to indicate a valid data transfer. D[63:0]# are quad-pumped signals and will thus be driven four times in a common clock period. D[63:0]# are latched off the falling edge of both DSTBP[3:0]# and DSTBN[3:0]#. Each group of 16 data signals correspond to a pair of one DSTBP# and one DSTBN#. The following table shows the grouping of data signals to data strobes and DINV#. **Quad-Pumped Signal Groups** Data Group / DSTBN#/DSTBP# / DINV# D[15:0]# / 0 / 0 D[31:16]# / 1 / 1 D[47:32]# / 2 / 2 D[63:48]# / 3 / 3 Furthermore, the DINV# pins determine the polarity of the data signals. Each group of 16 data signals corresponds to one DINV# signal. When the DINV# signal is active, the corresponding data group is inverted and therefore sampled active high.
DBR#	O	DBR# (Data Bus Reset) is used only in processor systems where no debug port is implemented on the system board. DBR# is used by a debug port interposer so that an in-target probe can drive system reset. If a debug port is implemented in the system, DBR# is a no connect. DBR# is not a processor signal.

5.1 Intel Pentium M Processor CPU - 2

CPU Pin Description (Continued)

Signal Name	Type	Description
DBSY#	I/O	DBSY# (Data Bus Busy) is asserted by the agent responsible for driving data on the processor system bus to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted. This signal must connect the appropriate pins on both processor system bus agents.
DEFER#	I	DEFER# is asserted by an agent to indicate that a transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or Input/Output agent. This signal must connect the appropriate pins of both processor system bus agents.
DINV[3:0]#	I/O	DINV[3:0]# (Data Bus Inversion) are source synchronous and indicate the polarity of the D[63:0]# signals. The DINV[3:0]# signals are activated when the data on the data bus is inverted. The bus agent will invert the data bus signals if more than half the bits, within the covered group, would change level in the next cycle. **DINV[3:0]# Assignment To Data Bus** Bus Signal / Data Bus Signals: DINV[3]# — D[63:48]# DINV[2]# — D[47:32]# DINV[1]# — D[31:16]# DINV[0]# — D[15:0]#
DPSLP#	I	DPSLP# when asserted on the platform causes the processor to transition from the Sleep state to the Deep Sleep state. In order to return to the Sleep state, DPSLP# must be deasserted. DPSLP# is driven by the ICH4-M component and also connects to the MCH-M component of the Intel 855PM or Intel 855GM chipset.
DRDY#	I/O	DRDY# (Data Ready) is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-common clock data transfer, DRDY# may be deasserted to insert idle clocks. This signal must connect the appropriate pins of both processor system bus agents.
DSTBN[3:0]#	I/O	Data strobe used to latch in D[63:0]#. Signals / Associated Strobe: D[15:0]#, DINV[0]# — DSTBN[0]# D[31:16]#, DINV[1]# — DSTBN[1]# D[47:32]#, DINV[2]# — DSTBN[2]# D[63:48]#, DINV[3]# — DSTBN[3]#
DSTBP[3:0]#	I/O	Data strobe used to latch in D[63:0]#. Signals / Associated Strobe: D[15:0]#, DINV[0]# — DSTBP[0]# D[31:16]#, DINV[1]# — DSTBP[1]# D[47:32]#, DINV[2]# — DSTBP[2]# D[63:48]#, DINV[3]# — DSTBP[3]#

CPU Pin Description (Continued)

Signal Name	Type	Description
DPWR#	I	DPWR# is a control signal from the Intel 855PM and Intel 855GM chipsets used to reduce power on the Intel Pentium M data bus input buffers.
FERR#/PBE#	O	FERR# (Floating-point Error)/PBE#(Pending Break Event) is a multiplexed signal and its meaning is qualified by STPCLK#. When STPCLK# is not asserted, FERR#/PBE# indicates a floating point when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel 80387 coprocessor, and is included for compatibility with systems using MS-DOS* type floating-point error reporting. When STPCLK# is asserted, an assertion of FERR#/PBE# indicates that the processor has a pending break event waiting for service. The assertion of FERR#/PBE# indicates that the processor should be returned to the Normal state. When FERR#/PBE# is asserted, indicating a break event, it will remain asserted until STPCLK# is deasserted. Assertion of PREQ# when STPCLK# is active will also cause an FERR# break event.
GTLREF	I	GTLREF determines the signal reference level for AGTL+ input pins. GTLREF should be set at 2/3 V_{CCP}. GTLREF is used by the AGTL+ receivers to determine if a signal is a logical 0 or logical 1.
HIT# **HITM#**	I/O I/O	HIT# (Snoop Hit) and HITM# (Hit Modified) convey transaction snoop operation results. Either system bus agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.
IERR#	O	IERR# (Internal Error) is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the processor system bus. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#, BINIT#, or INIT#.
IGNNE#	I	IGNNE# (Ignore Numeric Error) is asserted to force the processor to ignore a numeric error and continue to execute noncontrol floating-point instructions. If IGNNE# is deasserted, the processor generates an exception on a noncontrol floating-point instruction if a previous floating-point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 (CR0) is set. IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.
REQ[4:0]#	I/O	REQ[4:0]# (Request Command) must connect the appropriate pins of both processor system bus agents. They are asserted by the current bus owner to define the currently active transaction type. These signals are source synchronous to ADSTB[0]#.

5.1 Intel Pentium M Processor CPU - 3

CPU Pin Description (Continued)

Signal Name	Type	Description
INIT#	I	INIT# (Initialization), when asserted, resets integer registers inside the processor without affecting its internal caches or floating-point registers. The processor then begins execution at the power on Reset vector configured during power on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output Write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction. INIT# must connect the appropriate pins of both processor system bus agents. If INIT# is sampled active on the active to inactive transition of RESET#, then the processor executes its Built-in Self-Test (BIST)
LINT[1:0]	I	LINT[1:0] (Local APIC Interrupt) must connect the appropriate pins of all APIC Bus agents. When the APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a nonmaskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium processor. Both signals are asynchronous. Both of these signals must be software configured using BIOS programming of the APIC register space and used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration.
LOCK#	I/O	LOCK# indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins of both processor system bus agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction to the end of the last transaction. When the priority agent asserts BPRI# to arbitrate for ownership of the processor system bus, it will wait until it observes LOCK# deasserted. This enables symmetric agents to retain ownership of the processor system bus throughout the bus locked operation and ensure the atomicity of lock.
PRDY#	O	Probe Ready signal used by debug tools to determine processor debug readiness.
PREQ#	I	Probe Request signal used by debug tools to request debug operation of the processor.
PROCHOT#	O	PROCHOT# (Processor Hot) will go active when the processor temperature monitoring sensor detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit has been activated, if enabled. This signal may require voltage translation on the motherboard.
PSI#	O	Processor Power Status Indicator signal. This signal is asserted when the processor is in a lower state (Deep Sleep and Deeper Sleep).

CPU Pin Description (Continued)

Signal Name	Type	Description
PWRGOOD	I	PWRGOOD (Power Good) is a processor input. The processor requires this signal as a clean indication that the clocks and power supplies are stable and within their specifications. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD. The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout the boundary scan operation.
ITP_CLK[1:0]	I	ITP_CLK[1:0] are copies of BCLK that are used only in processor systems where no debug port is implemented on the system board. ITP_CLK[1:0] are used as BCLK[1:0] references for a debug port implemented on an interposer. If a debug port is implemented in the system, ITP_CLK[1:0] are no connects. These are not processor signals.
RESET#	I	Asserting the RESET# signal resets the processor to a known state and invalidates its internal caches without writing back any of their contents. For a power-on Reset, RESET# must stay active for at least two milliseconds after VCC and BCLK have reached their proper specifications. On observing active RESET#, both system bus agents will deassert their outputs within two clocks. All processor straps must be valid within the specified setup time before RESET# is deasserted.
RS[2:0]#	I	RS[2:0]# (Response Status) are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of both processor system bus agents.
RSVD	-	These pins are RESERVED and must be left unconnected on the board. However, it is recommended that routing channels to these pins on the board be kept open for possible future use. Please refer to the platform design guides for more details.
SLP#	I	SLP# (Sleep), when asserted in Stop-Grant state, causes the processor to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts. The processor will recognize only assertion of the RESET# signal, deassertion of SLP#, and removal of the BCLK input while in Sleep state. If SLP# is deasserted, the processor exits Sleep state and returns to Stop-Grant state, restarting its internal clock signals to the bus and processor core units. If DPSLP# is asserted while in the Sleep state, the processor will exit the Sleep state and transition to the Deep Sleep state.

5.1 Intel Pentium M Processor CPU - 4

CPU Pin Description (Continued)

Signal Name	Type	Description
SMI#	I	SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, the processor saves the current state and enter System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler. If SMI# is asserted during the deassertion of RESET# the processor will tristate its outputs.
STPCLK#	I	STPCLK# (Stop Clock), when asserted, causes the processor to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the system bus and APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.
TCK	I	TCK (Test Clock) provides the clock input for the processor Test Bus (also known as the Test Access Port).
TDI	I	TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.
TDO	O	TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.
TEST1, TEST2, TEST3	I	TEST1, TEST2, and TEST3 must be left unconnected but should have a stuffing option connection to V SS separately using 1-k, pull-down resisitors.
THERMDA	Other	Thermal Diode Anode.
THERMDC	Other	Thermal Diode Cathode.
THERMTRIP#	O	The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all execution when the junction temperature exceeds approximately 125°C. This is signalled to the system by the THERMTRIP# (Thermal Trip) pin.
TMS	I	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools.
TRDY#	I	TRDY# (Target Ready) is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of both system bus agents.
TRST#	I	TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset.

CPU Pin Description (Continued)

Signal Name	Type	Description
VCC	I	Processor core power supply.
VCCA[3:0]	I	VCCA provides isolated power for the internal processor core PLL's.
VCCP	I	Processor I/O Power Supply.
VCCQ[1:0]	I	Quiet power supply for on die COMP circuitry. These pins should be connected to VCCP on the motherboard. However, these connections should enable addition of decoupling on the VCCQ lines if necessary.
VCCSENSE	O	VCCSENSE is an isolated low impedance connection to processor core power (VCC). It can be used to sense or measure power near the silicon with little noise.
VID[5:0]	O	VID[5:0] (Voltage ID) pins are used to support automatic selection of power supply voltages (Vcc). Unlike some previous generations of processors, these are CMOS signals that are driven by the Intel Pentium M processor. The voltage supply for these pins must be valid before the VR can supply Vcc to the processor. Conversely, the VR output must be disabled until the voltage supply for the VID pins becomes valid. The VID pins are needed to support the processor voltage specification variations.
VSSSENSE	O	VSSSENSE is an isolated low impedance connection to processor core VSS. It can be used to sense or measure ground near the silicon with little noise.

5.2 PN800 North Bridge - 1

CPU Interface

Signal Name	Pin #	I/O	Signal Description
HA[35:3]#	(see pin lists)	IO	**Host CPU Address Bus.** Connect to the address bus of the host CPU. Inputs during CPU cycles and driven by the North Bridge during cache snooping operations. Address signals up through HA[35]# allow future support of a 64 Gbyte memory space (the current design supports up to HA[33]# for support of 16 GB)..
HADSTB [1:0]#	C26, A22	IO	**Host CPU Address Strobe.** Source synchronous strobes used to transfer HA[31:3]# and HREQ[4:0]# at a 2x transfer rate. HASTB1# is the strobe for HA[31:17]# and HASTB0# is the strobe for HA[16:3] and HREQ[4:0]#.
HD[63:0]#	(see pin lists)	IO	**Host CPU Data.** These signals are connected to the CPU data bus.
HDBI[3:0]#	A5, J3, B13, A6	IO	**Host CPU Dynamic Bus Inversion.** Driven along with HD[63:0]# to indicate if the associated signals are inverted or not. Used to limit the number of simultaneously switching signals to 8 for the associated 16-bit data pin group (HDBI3# for HD[63:48]#, HDBI2# for HD[47:32]#, HDBI1# for HD[31:16]#, and HDBI0# for HD[15:0]#). HDBIn# is asserted such that the number of data bits driven low for the corresponding group does not exceed 8.
HDSTBP [3:0]# HDSTBN [3:0]#	D1, H3, E13, F8 E1, H2, D13, D8	IO	**Host CPU Differential Data Strobes.** Source synchronous strobes used to transfer HD[63:0]# and HDBI[3:0]# at a 4x transfer rate. HDSTBP3# / HDSTBN3# are the strobes for HD[63:48]# & HDBI3#; HDSTBP2# / HDSTBN2# are the strobes for HD[47:32]# & HDBI2#; HDSTBP1# / HDSTBN1# are the strobes for HD[31:16]# & HDBI1#; and HDSTBP0# / HDSTBN0# are the strobes for HD[15:0]# & HDBI0#.
ADS#	A19	IO	**Address Strob**e. The CPU asserts ADS# in T1 of the CPU bus cycle.
DBSY#	B19	IO	**Data Bus Busy**. Used by the data bus owner to hold the data bus for transfers requiring more than one cycle.
DRDY#	C19	IO	**Data Read**y. Asserted for each cycle that data is transferred.
HIT#	C17	IO	**Hi**t. Indicates that a caching agent holds an unmodified version of the requested line. Also driven in conjunction with HITM# by the target to extend the snoop window.
HITM#	F16	I	**Hit Modifie**d. Asserted by the CPU to indicate that the address is modified in the L1 cache and needs to be written back.

CPU Interface (Continued)

Signal Name	Pin #	I/O	Signal Description
HLOCK#	F18	I	**Host Loc**k. All CPU cycles sampled with the assertion of HLOCK# and ADS# until the negation of HLOCK# must be atomic.
HREQ[4:0]#	F19, E19, D20, C20, D19	IO	**Request Comman**d. Asserted during both clocks of the request phase. In the first clock, the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second clock, the signals carry additional information to define the complete transaction type.
HTRDY#	G18	IO	**Host Target Read**y. Indicates that the target of the processor transaction is able to enter the data transfer phase.
RS[2:0]#	B17, D18, B18	IO	**Response Signal**s. Indicates the type of response per the table below: **RS[2:0]# Response type RS[2:0]# Response type** 000 Idle State 100 Hard Failure 001 Retry Response 101 Normal Without Data 010 Defer Response 110 Implicit Writeback 011 Reserved 111 Normal With Data
DPWR#	G15	O	**Data Bus Power Reduction.** Request to reduce power on the mobile CPU data bus input buffer. Connect to mobile CPU if used.
BREQ0#	E18	O	**Bus Request 0.** Bus request output to CPU.
BPRI#	C16	IO	**Priority Agent Bus Reques**t. The owner of this signal will always be the next bus owner. This signal has priority over symmetric bus requests and causes the current symmetric owner to stop issuing new transactions unless the HLOCK# signal is asserted. The PN800 drives this signal to gain control of the processor bus.
BNR#	C18	IO	**Block Next Reques**t. Used to block the current request bus owner from issuing new requests. This signal is used to dynamically control the processor bus pipeline depth.
DEFER#	E17	IO	**Defe**r. The PN800 uses a dynamic deferring policy to optimize system performance. The PN800 also uses the DEFER# signal to indicate a processor retry response.
CPURST#	K6	O	**CPU Reset.** Reset output to CPU. External pullup and filter capacitor to ground should be provided per CPU manufacturer's recommendations.

Note: Clocking of the CPU interface is performed with HCLK+ and HCLK– (see clock pin description group).

5.2 PN800 North Bridge - 2

DDR SDRAM Interface – "A" Data

Signal Name	Pin #	I/O	Signal Description
MDA[63:0]	(see pin lists)	IO	**Memory Data.** These signals are connected to the DRAM data bus. Output drive strength may be set by Device 0 Function 3 RxE2.
DQMA[7:0]	AT16, AP20, AP24, AN32, AD35, V34, L33, D36	O	**Data Mask.** Data mask of each byte lane. Output drive strength may be set by Device 0 Function 3 RxE2.
DQSA[7:0]#	AR16, AN20, AT24, AT33, AD34, U34, L31, D35	IO	**DDR Data Strobe.** Data strobe of each byte lane. Output drive strength may be set by Device 0 Function 3 RxE0.
CSA[3:0]#	AP25, AP29, AR25, AT25	O	**Chip Select.** Chip select of each bank. Output drive strength may be set by Device 0 Function 3 RxE4.
CKEA[3:0]	L34, R35, M35, T33	O	**Clock Enables.** Clock enables for each DRAM bank for powering down the SDRAM or clock control for reducing power usage and for reducing heat / temperature in high-speed memory systems.

DDR SDRAM Interface – "B" Data

Signal Name	Pin #	I/O	Signal Description
MDB[63:0]	(see pin lists)	IO	**Memory Data.** These signals are connected to the DRAM data bus. Output drive strength may be set by Device 0 Function 3 RxE2.
DQMB[7:0]	AN18, AP22, AR28, AG32, Y33, N35, H36, A34	O	**Data Mask.** Data mask of each byte lane. Output drive strength may be set by Device 0 Function 3 RxE2.
DQSB[7:0]#	AP18, AR22, AT28, AG33, Y34, N34, H34, A33	IO	**DDR Data Strobe.** Data strobe of each byte lane. Output drive strength may be set by Device 0 Function 3 RxE0.
CSB[3:0]#	AP28, AR29, AT29, AT30	O	**Chip Select.** Chip select of each bank. Output drive strength may be set by Device 0 Function 3 RxE4.
CKEB[3:0]	J35, K31, J33, K32	O	**Clock Enables.** Clock enables for each DRAM bank for powering down the SDRAM or clock control for reducing power usage and for reducing heat / temperature in high-speed memory systems.

5.2 PN800 North Bridge - 3

AGP 8x / 4x Bus Interface

Signal Name	Pin #	I/O	Signal Description
GADSTB1F (GADSTB1 for 4x), **GADSTB1S** (GADSTB1# for 4x)	AG3 AG1	IO	**Bus Strobe 1.** Source synchronous strobes for GD[31:16] (i.e., the agent that is providing the data drives these signals). For 8x transfer mode, GADSTB1 is interpreted as GADSTB1F ("First" strobe) and GADSTB1# as GADSTB1S ("Second" strobe). GADSTB1 and GADSTB1# provide timing for 4x transfer mode.
GFRAME (GFRAME# for 4x)	AL4	IO	**Frame.** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator. Interpreted as active high for 8x.
GDEVSEL (GDEVSEL# for 4x)	AK1	IO	**Device Select (PCI transactions only).** Driven by the North Bridge when a PCI initiator is attempting to access main memory. Input when the chip is acting as PCI initiator. Not used for AGP cycles. Interpreted as active high for AGP 8x.
GIRDY (GIRDY# for 4x)	AL5	IO	**Initiator Ready.** (Interpreted as active low for PCI/AGP4x and high for AGP 8x). For AGP write cycles, the assertion of this pin indicates that the master is ready to provide all write data for the current transaction. Once this pin is asserted, the master is not allowed to insert wait states. For AGP read cycles, the assertion of this pin indicates that the master is ready to transfer a subsequent block of read data. The master is *never* allowed to insert a wait state during the initial block of a read transaction. However, it may insert wait states after each block transfers. For PCI cycles, asserted when initiator is ready for data transfer.
GTRDY (GTRDY# for 4x)	AK3	IO	**Target Ready.** (Interpreted as active low for PCI/AGP4x and high for AGP 8x). For AGP cycles, indicates that the target is ready to provide read data for the entire transaction (when the transaction can complete within four clocks) or is ready to transfer a (initial or subsequent) block of data when the transfer requires more than four clocks to complete. The target is allowed to insert wait states after each block transfer for both read and write transactions. For PCI cycles, asserted when target is ready for data transfer.
AGP8XDET#	AB1	I	**AGP 8x Transfer Mode Detect.** Low indicates that the external graphics card can support 8x transfer mode. Readable in Device 0 Function 0 Rx84[3].

AGP 8x / 4x Bus Interface (Continued)

Signal Name	Pin #	I/O	Signal Description
GD[31:0]	(see pin list)	IO	**Address / Data Bus.** Address is driven with GADSTB assertion for AGP-style transfers and with GFRAME# assertion for PCI-style transfers.
GC#BE[3:0] (GCBE#[3:0] for 4x mode)	AK5, AK2, AL3, AN4	IO	**Command / Byte Enable.** (Interpreted as C/BE# for AGP 4x and C#/BE for 8x). For AGP cycles these pins provide command information (different commands than for PCI) driven by the master (graphics controller) when requests are being enqueued using GPIPE# (4x only as GPIPE# isn't used in 8x mode). These pins provide valid byte information during AGP write transactions and are driven by the master. The target (this chip) drives these lines to "0000" during the return of AGP read data. For PCI cycles, commands are driven with GFRAME# assertion. Byte enables corresponding to supplied or requested data are driven on following clocks.
GPAR	AN3	IO	**AGP Parity.** A single parity bit is provided over GD[31:0] and GC#BE[3:0].
GDBIH / GPIPE# **GDBIL**	AF4 AG4	IO	**Dynamic Bus Inversion High / Low.** AGP 8x transfer mode only. Driven by the source to indicate whether the corresponding data bit group (GDBIH for GD[31:16] and GDBIL for GD[15:0]) needs to be inverted on the receiving end (1 on GDBIx indicates that the corresponding data bit group should be inverted). Used to limit the number of simultaneously switching outputs to 8 for each 16-pin group. **Pipelined Request.** Not used by AGP 8x. Asserted by the master (external graphics controller) to indicate that a full-width request is to be enqueued by the target (North Bridge). The master enqueues one request each rising edge of GCLK while GPIPE# is asserted. When GPIPE# is deasserted no new requests are enqueued across the AD bus. **Not**e: See RxAE[1] for GPIPE# / GDBIH pin function selection.
GADSTB0F (GADSTB0 for 4x), **GADSTB0S** (GADSTB0# for 4x)	AT3 AR3	IO	**Bus Strobe 0.** Source synchronous strobes for GD[15:0] (the agent that is providing the data drives these signals). For 8x transfer mode, GADSTB0 is interpreted as GADSTB0F ("First" strobe) and GADSTB0# as GADSTB0S ("Second" strobe). GADSTB0 and GADSTB0# provide timing for 4x mode.

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AGP 8x / 4x Bus Interface (Continued)

Signal Name	Pin #	I/O	Signal Description
GSBA[7:0]# (GSBA[7:0] for 4x)	AE1, AE4, AE3, AE2, AD2, AC3, AC4, AC1	I	**Side Band Address.** Provides an additional bus to pass address and command information from the master (graphics controller) to the target (North Bridge). These pins are ignored until enabled.
GSBSTBF (GSBSTB for 4x), **GSBSTBS** (GSBSTB# for 4x)	AD3 AD1	I	**Side Band Strobe.** Driven by the master to provide timing for GSBA[7:0]. 8x mode uses GSBSTBF ("First" strobe) and GSBSTBS ("Second" strobe). These signals are interpreted as GSBSTB & GSBSTB# for AGP4x.
GST[2:0]	AE6, AE5, AD6	O	**Status (AGP only).** Provides information from the arbiter to a master to indicate what it may do. Only valid while GGNT# is asserted. 000 Indicates that previously requested low priority read or flush data is being returned to the master (graphics controller). 001 Indicates that previously requested high priority read data is being returned to the master. 010 Indicates that the master is to provide low priority write data for a previously enqueued write command. 011 Indicates that the master is to provide high priority write data for a previously enqueued write command. 100 Reserved. (arbiter must not issue, may be defined in the future). 101 Reserved. (arbiter must not issue, may be defined in the future). 110 Reserved. (arbiter must not issue, may be defined in the future). 111 Indicates that the master (graphics controller) has been given permission to start a bus transaction. The master may enqueue AGP requests by asserting GPIPE# or start a PCI transaction by asserting GFRAME#. GST[2:0] are always outputs from the target (North Bridge) and inputs to the master (graphics controller).

AGP 8x / 4x Bus Interface (Continued)

Signal Name	Pin #	I/O	Signal Description
GWBF (GWBF# for 4x)	AB2	I	**Write Buffer Full.**
GRBF (GRBF# for 4x)	AE7	I	**Read Buffer Full.** Indicates if the master (graphics controller) is ready to accept previously requested low priority read data. When GRBF# is asserted, the North Bridge will not return low priority read data to the graphics controller.
GREQ (GREQ# for 4x)	AD4	I	**Request.** Master (graphics controller) request for use of the AGP bus.
GGNT (GGNT# for 4x)	AD5	O	**Grant.** Permission is given to the master (graphics controller) to use the AGP bus.
GSERR (GSERR# for 4x)	AN1	IO	**System Error.**
GSTOP (GSTOP# for 4x)	AM3	IO	**Stop.** Asserted by the target to request the master to stop the current transaction. Interpreted as active high for AGP 8x.

Note: I/O pads for all pins on this page are powered by VCC15AGP. Input voltage levels are referenced to AGPVREF.
Note: The AGP interface pins can be optionally configured as additional interfaces for connecting to external display devices. For simplification of the AGP pin description tables above and on the next page, that multiplexing is not shown here (see "Additional I2C Interfaces" and "Digital Display" pin description tables later in this document for more information).
Note: I/O pads for all pins on this page are powered by VCC15AGP. Input voltage levels are referenced to AGPVREF.
Note: The AGP interface pins can be optionally configured as additional interfaces for connecting to external display devices. For simplification of the AGP pin description tables above and on the next page, that multiplexing is not shown here (see "Additional I2C Interfaces" and "Digital Display" pin description tables later in this document for more information).
Note: Separate system interrupts are not provided for AGP. The AGP connector provides interrupts via PCI bus INTA-B#.
Note: A separate reset is not required for the AGP bus (RESET# resets both PCI and AGP buses)
Note: Two mechanisms are provided by the AGP bus to enqueue master requests: GPIPE# (to send addresses multiplexed on the AD lines) and the GSBA port (to send addresses unmultiplexed). AGP masters implement one or the other or select one at initialization time (they are not allowed to change during runtime). Only one of the two will be used; the signals associated with the other will not be used. GRBF# has an internal pullup to maintain it in the de-asserted state in case it is not implemented on the master device. AGP 8x mode allows only GSBA (GPIPE# isn't used in 8x mode).
Note: AGP 8x signal levels are 0V and 0.8V. AGP 8x mode maintains most signals at a low level when inactive resulting in no current flow.

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CRT Interface

Signal Name	Pin #	I/O	Signal Description
AR	R1	AO	**Analog Red.** Analog red output to the CRT monitor.
AG	R2	AO	**Analog Green.** Analog green output to the CRT monitor.
AB	R3	AO	**Analog Blue.** Analog blue output to the CRT monitor.
HSYNC	U4	O	**Horizontal Sync.** Output to CRT.
VSYNC	U3	O	**Vertical Sync.** Output to CRT.
RSET	V7	AI	**Reference Resistor.** Tie to GNDDAC through an external 82 Ω 1%%resistor to control the RAMDAC full-scale current value. See Design Guide for details.

I/O pads for the pins in the above table are powered by VCC33GFX (i.e., 3.3V I/O).

Digital Power / Ground

Signal Name	Pin #	I/O	Signal Description
VTT	(see pin lists	P	**Power** for **CPU I/O Interface Logic (15 Pins).** Typical 1.65V (CPU dependent)
VCC25MEM	(see pin lists	P	**Power** for **Memory I/O Interface Logic (25 Pins).** 2.5V ±5%.
VCC15VL	AD16-17	P	**Power** for **V-Link I/O Interface Logic (2 Pins).** 1.5V ±5%
VCC15AGP	(see pin lists	P	**Power** for **AGP Bus I/O Interface Logic (6 Pins).** 1.5V ±5%
VCC33GFX	V13, W13, Y13	P	**Power for Graphics Display I/O Logic (3 Pins).** 3.3V ±5%
VCC15	(see pin lists	P	**Power** for **Internal Logic (51 Pins).** 1.5V ±5%
VSUS15	AT14	P	**Suspend Power (1 Pin).** 1.5V ±5%
GND	(see pin lists	P	**Digital Ground (161 Pins).** Connect to main ground plane.

Ultra V-Link Interface

Signal Name	Pin #	I/O	Signal Description
VD15,	AP13	IO	**V-Link Data Bus.** During system initialization, VD[7:0] are used to transmit strap information from the South Bridge (the straps are not on the VD pins but are on the indicated pins of the South Bridge chip). Check the strap pin table for details.
VD14,	AN13	IO	
VD13,	AR6	IO	
VD12,	AT6	IO	
VD11,	AM12	IO	
VD10,	AP12	IO	
VD9,	AN6	IO	
VD8,	AM7	IO	
VD7,	AP11	IO	
VD6,	AM11	IO	
VD5,	AP7	IO	
VD4,	AR7	IO	
VD3,	AR11	IO	
VD2,	AN10	IO	
VD1,	AR8	IO	
VD0	AP8	IO	
VPAR	AT7	IO	**V-Link Parity.**
VBE#	AN7	IO	**V-Link Byte Enable.**
UPCMD	AN12	I	**V-Link Command from Client (South Bridge) to Host (North Bridge).**
UPSTB+	AM10	I	**V-Link Strobe from Client to Host.**
UPSTB–	AM9	I	**V-Link Complement Strobe from Client to Host.**
DNCMD	AP10	O	**V-Link Command from Host (North Bridge) to Client (South Bridge).**
DNSTB+	AN9	O	**V-Link Strobe from Host to Client.**
DNSTB–	AP9	O	**V-Link Complement Strobe from Host to Client.**

Note: I/O pads for the pins in the above table are powered by VCC15VL. Input voltage levels are referenced to VLVREF.

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Dedicated Digital Video Port 0 (DVP0)

Signal Name	Pin #	I/O	Signal Description
TVD11 / DVP0D11 / CAPD11,	AA6	O	**TV Encoder 0 Data.**
TVD10 / DVP0D10 / CAPD10 / strap,	AB6		To configure DVP0 as a TV Out interface port, pins DVP0D[6:5] must be strapped high.
TVD9 / DVP0D9 / CAPD9 / strap,	AB5		Note: One TV Encoder interface is supported through either DVP0 or GDVP1.
TVD8 / DVP0D8 / CAPD8 / strap,	Y7		
TVD7 / DVP0D7 / CAPD7 / strap,	Y6		
TVD6 / DVP0D6 / CAPD6 / strap,	Y5		
TVD5 / DVP0D5 / CAPD5 / strap,	AA4		
TVD4 / DVP0D4 / CAPD4 / strap,	Y2		
TVD3 / DVP0D3 / CAPD3 / strap,	Y3		
TVD2 / DVP0D2 / CAPD2 / strap,	AA5		
TVD1 / DVP0D1 / CAPD1 / strap,	W2		
TVD0 / DVP0D0 / CAPD0 / strap	W1		
TVHS / DVP0HS / CAPHS	W4	O	**TV Encoder 0 Horizontal Sync.** Internally pulled down.
TVVS / DVP0VS / CAPVS	V1	O	**TV Encoder 0 Vertical Sync.** Internally pulled down.
TVDE / DVP0DE	W3	O	**TV Encoder 0 Display Enable.** Internally pulled down.
TVCLKIN / DVP0DET / CAPBCLK	V2	I	**TV Encoder 0 Clock In.** Feedback from TV encoder. Internally pulled down.
TVCLK / DVP0CLK / CAPACLK	Y4	O	**TV Encoder 0 Clock Out.** Output to TV encoder. Internally pulled down.

The above pins may be connected to an external TV Encoder chip such as a VIA VT1622A or VT1622AM for driving a TV set.
I/O pads for the pins on this page are powered by VCC33GFX (3.3V I/O).

SMB / I2C Interface

Signal Name	AGP Name	Pin #	I/O	Signal Description
SBPLCLK	GIRDY	AL5	IO	**I2C Serial Bus Clock for Panel (Muxed on AGP Bus Pins).**
SBPLDAT	GC#BE1	AL3	IO	**I2C Serial Bus Data for Panel (Muxed on AGP Bus Pins).**
SBDDCCLK	GREQ	AD4	IO	**I2C Serial Bus Clock for CRT DDC (Muxed on AGP Bus Pins).**
SBDDCDAT	GGNT	AD5	IO	**I2C Serial Bus Data for CRT DDC (Muxed on AGP Bus Pins).**
SPCLK2	n/a	T3	IO	**Serial Port (SMB/I2C) Clock and Data.** The SPCLKn pins are the clocks for serial data transfer. The SPDATn pins are the data signals used for serial data transfer. SPxxx1 is typically used for DVI monitor communications and SPxxx2 is typically used for DDC for CRT monitor communications. These pins are programmed via "Sequencer" graphics registers (port 3C5) in the "Extended" VGA register space (see the UniChrome-II Graphics Registers document for additional details). The SPxxx1 registers are programmed via 3C5.31 ("IIC Serial Port Control 1") and the SPxxx2 registers are programmed via 3C5.26 ("IIC Serial Port Control 0"). In both registers, the clock out state is programmed via bit-5 and the data out state via bit-4, clock in status may be read in bit-3 and data in status in bit-2, and the port may be enabled via bit-0.
SPCLK1 / CAPD12	n/a	V3		
SPDAT2,	n/a	T4		
SPDAT1 / CAPD13	n/a	V4		

I/O pads for SPCLK[2:1] / SPDAT[2:1] above are powered by VCC33GFX (i.e., 3.3V I/O).
All other pins in the above table are powered by VCC15AGP (i.e., 1.5V I/O)

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CCIR601 / CCIR656 / VIP1.1 / VIP2.0 Video Capture Port (VCP)

Signal Name	Pin #	I/O	Signal Description
		I	**Video Capture Data.** To configure DVP0 as a video capture port, pin DVP0D6 must be strapped low. Pin Function: 8-Bit Mode 16-Bit Mode
CAPD15 / GPO0	V5		CAPBD7 CAPAD15
CAPD14 / GPOUT	W5		CAPBD6 CAPAD14
CAPD13 / SPDAT1	V4		CAPBD5 CAPAD13
CAPD12 / SPCLK1,	V3		CAPBD4 CAPAD12
CAPD11 / DVP0D11 / TVD11,	AA6		CAPBD3 CAPAD11
CAPD10 / DVP0D10 / TVD10 / strap,	AB6		CAPBD2 CAPAD10
CAPD9 / DVP0D9 / TVD9 / strap,	AB5		CAPBD1 CAPAD9
CAPD8 / DVP0D8 / TVD8 / strap,	Y7		CAPBD0 CAPAD8
CAPD7 / DVP0D7 / TVD7 / strap,	Y6		CAPAD7 CAPAD7
CAPD6 / DVP0D6 / TVD6 / strap,	Y5		CAPAD6 CAPAD6
CAPD5 / DVP0D5 / TVD5 / strap,	AA4		CAPAD5 CAPAD5
CAPD4 / DVP0D4 / TVD4 / strap,	Y2		CAPAD4 CAPAD4
CAPD3 / DVP0D3 / TVD3 / strap,	Y3		CAPAD3 CAPAD3
CAPD2 / DVP0D2 / TVD2 / strap,	AA5		CAPAD2 CAPAD2
CAPD1 / DVP0D1 / TVD1 / strap,	W2		CAPAD1 CAPAD1
CAPD0 / DVP0D0 / TVD0 / strap	W1		CAPAD0 CAPAD0
CAPHS / DVP0HS / TVHS	W4	I	**Video Capture Horizontal Sync.** For capture port "A" (16-bit and 8-bit mode). Internally pulled down.
CAPVS / DVP0VS / TVVS	V1	I	**Video Capture Vertical Sync.** For capture port "A" (16-bit and 8-bit mode). Internally pulled down.

CCIR601 / CCIR656 / VIP1.1 / VIP2.0 Video Capture Port (VCP) (Continued)

Signal Name	Pin #	I/O	Signal Description
CAPAFLD / BISTIN	V6	I	**Video Capture "A"-Channel TV Field Indicator.** For capture port "A" (16-bit and 8-bit mode).
CAPBCLK / DVP0DET / TVCLKIN	V2	I	**Video Capture Clock B.** Port "B" (8-bit mode) input clock from external video decoder. Internally pulled down. Not used in 16-bit mode.
CAPACLK / DVP0CLK / TVCLK	Y4	I	**Video Capture Clock A.** Port "A" (16-bit and 8-bit mode) input clock from external video decoder. Internally pulled down.

Note: I/O pads for the pins on this page are powered by VCC33GFX (3.3V I/O)

DDR SDRAM Interface – Address

Signal Name	Pin #	I/O	Signal Description
MAA[13:0], MAB[13:0]	(see pin lists)	O	**Memory Address A and B.** Two sets for additional drive. Output drive strength may be set by Device 0 Function 3 RxE8 (MAA) and EA (MAB).
BAA[1:0], BAB[1:0]	AT35, AT31, AF36, AJ36	O	**Bank Address A and B.** Two sets for additional drive. Output drive strength may be set by Device 0 Function 3 RxE8 (BA) and EA (BB).
SRASA#, SCASA#, SWEA#, SRASB#, SCASB#, SWEB#	AP26, AN25, AR26, AL29, AN28, AN31	O	**Row Address, Column Address and Write Enable Command Indicators A and B.** Two sets for additional drive. Output drive strength may be set by Device 0 Function 3 Rx E8 (ScmdA) and EA (ScmdB).

Note: I/O pads for all SDRAM pins are powered by VCC25MEM. MD / DQS input voltage levels are referenced to MEMVREF.

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AGP-Multiplexed Digital Video Port 1 (GDVP1) – TV Encoder

Signal Name	AGP Name	Pin #	I/O	Signal Description
GTVD11 / GDVP1D11,	GC#BE3	AK5	O	**Data.**
GTVD10 / GDVP1D10,	GD26	AH5		
GTVD9 / GDVP1D9,	GD24	AG5		
GTVD8 / GDVP1D8,	GD30	AG6		
GTVD7 / GDVP1D7,	GD28	AH4		
GTVD6 / GDVP1D6,	GD29	AF3		
GTVD5 / GDVP1D5,	GSBA4#	AE2		
GTVD4 / GDVP1D4,	GD27	AG2		
GTVD3 / GDVP1D3,	GSBA5#	AE3		
GTVD2 / GDVP1D2,	GSBSTBS	AD1		
GTVD1 / GDVP1D1,	GSBSTBF	AD3		
GTVD0 / GDVP1D0	GSBA2#	AC3		
GTVHS / GDVP1HS	GSBA3#	AD2	O	**Horizontal Sync.** Internally pulled down.
GTVVS / GDVP1VS	GSBA0#	AC1	O	**Vertical Sync.** Internally pulled down.
GTVDE / GDVP1DE	GSBA1#	AC4	O	**Display Enable.** Internally pulled down.
GTVCLKIN / FPDET	GADSTB1S	AG1	I	**Clock In.** Input from TV encoder. Internally pulled down.
GTVCLK / GDVP1CLK	GSBA6#	AE4	O	**Clock Out.** Output to TV encoder. Internally pulled down.
GTVCLK# / GDVP1CLK#	GSBA7#	AE1	O	**Clock Out Complement.** Output to TV encoder. Internally pulled down.

The above pins may be connected to an external TV Encoder chip such as a VIA VT1623 or VT1623M for driving a TV set.
I/O pads for the pins on this page are powered by VCC15AGP (1.5V I/O).
Note: If the FPD port is enabled and TV-out capability is required at the same time, the dedicated TV-out port (DVP0) must be used because pin AG1 will be dedicated to the FPDET function.

AGP-Multiplexed Digital Video Port 1 (GDVP1) – DVI Interface

Signal Name	AGP Name	Pin #	I/O	Signal Description
GDVP1D11 / GTVD11,	GC#BE3	AK5	O	**Data.**
GDVP1D10 / GTVD10,	GD26	AH5		
GDVP1D9 / GTVD9,	GD24	AG5		
GDVP1D8 / GTVD8,	GD30	AG6		
GDVP1D7 / GTVD7,	GD28	AH4		
GDVP1D6 / GTVD6,	GD29	AF3		
GDVP1D5 / GTVD5,	GSBA4#	AE2		
GDVP1D4 / GTVD4,	GD27	AG2		
GDVP1D3 / GTVD3,	GSBA5#	AE3		
GDVP1D2 / GTVD2,	GSBSTBS	AD1		
GDVP1D1 / GTVD1,	GSBSTBF	AD3		
GDVP1D0 / GTVD0,	GSBA2#	AC3		
GDVP1HS / GTVHS	GSBA3#	AD2	O	**Horizontal Sync.**
GDVP1VS / GTVVS	GSBA0#	AC1	O	**Vertical Sync.**
GDVP1DE / GTVDE	GSBA1#	AC4	O	**Data Enable.**
GDVP1DET	GD31	AF1	I	**Display Detect.** If VGA register 3C5.3E[0] = 1, 3C5.1A[4] will read 1 if a display is connected. Tie to GND if not used.
GDVP1CLK / GTVCLK	GSBA6#	AE4	O	**Clock.**
GDVP1CLK# / GTVCLK#	GSBA7#	AE1	O	**Clock Complement.**

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24-Bit / Dual 12-Bit Flat Panel Display Interface

Signal Name	AGP Name	Pin #	I/O	Signal Description
FPD23 / **FPD0D11,**	GD11	AM4	O	**Flat Panel Data.** For 24-bit or dual 12-bit flat panel display modes.
FPD22 / **FPD0D10,**	GD13	AN2		Two FPD interface modes, 24-bit and dual 12-bit, are supported.
FPD21 / **FPD0D09,**	GD14	AL1		Strapping pin DVP0D4 is used to select the interface mode to theLVDS transmitter chip:
FPD20 / **FPD0D08,**	GD15	AP1		Strap High (3C5.12[4]=1): 24-bit Strap Low (3C5.12[4]=0): Dual 12-bit
FPD19 / **FPD0D07,**	GC#BE2	AK2		In “24-bit” mode, only one set of control pins is required. However, in dual 12-bit mode, the
FPD18 / **FPD0D06,**	GD16	AJ3		PN800 provides two sets of control signals that are required for certain LVDS transmitter chips.
FPD17 / **FPD0D05,**	GD17	AJ1		In 24-bit mode, two operating modes are supported:
FPD16 / **FPD0D04,**	GD18	AJ4		3C5.12[4]=1 & 3x5.88[2]=0 & 3x5.88[4]=0 Double data rate: each rising & falling clock edge
FPD15 / **FPD0D03,**	GD23	AH3		transmits a complete 24-bit pixel 3C5.12[4]=1 & 3x5.88[2]=0 & 3x5.88[4]=1
FPD14 / **FPD0D02,**	GD20	AH1		Single data rate: each clock rising edge transmits a complete 24-bit pixel
FPD13 / **FPD0D01,**	GD22	AK4		In dual 12-bit mode, 3C5.12[4]=0 & 3x5.88[2] = 1
FPD12 / **FPD0D00,**	GADSTB1F	AG3		Double data rate: each rising and falling clock edge transmits half (12 bits) of two 24-bit pixels
FPD11 / **FPD1D1**1,	GD1	AP2		
FPD10 / **FPD1D1**0,	GD0	AT2		
FPD09 / **FPD1D0**9,	GD3	AT5		
FPD08 / **FPD1D0**8,	GD4	AR4		
FPD07 / **FPD1D0**7,	GD5	AT1		
FPD06 / **FPD1D0**6,	GD6	AN5		
FPD05 / **FPD1D0**5,	GD7	AT4		

24-Bit / Dual 12-Bit Flat Panel Display Interface (Continued)

Signal Name	AGP Name	Pin #	I/O	Signal Description
FPD04 / **FPD1D0**4,	GADSTB0F	AT3	O	
FPD03 / **FPD1D0**3,	GC#BE0	AN4		
FPD02 / **FPD1D0**2,	GADSTB0S	AR3		
FPD01 / **FPD1D0**1,	GD10	AR1		
FPD00 / **FPD1D00**	GD12	AL2		
FPHS	GFRAME	AL4	O	**Flat Panel Horizontal Sync.** 24-bit mode or port 0 in dual 12-bit mode.
FPVS	GDEVSEL	AK1	O	**Flat Panel Vertical Sync.** 24-bit mode or port 0 in dual 12-bit mode.
FPDE	GD19	AK6	O	**Flat Panel Data Enable.** 24-bit mode or port 0 in dual 12-bit mode
FPDET	GADSTB1S	AG1	I	**Flat Panel Detect.** 24-bit mode or port 0 in dual 12-bit mode
FPCLK	GD21	AH2	O	**Flat Panel Clock.** 24-bit mode or port 0 in dual 12-bit mode
FPCLK#	GWBF	AB2	O	**Flat Panel Clock Complement.** 24-bit mode or port 0 in dual 12-bit mode. For double-data-rate data transfers.
FP1HS	GD9	AP3	O	**Flat Panel Horizontal Sync.** For port 1 in dual 12-bit mode.
FP1VS	GPAR	AN3	O	**Flat Panel Vertical Sync.** For port 1 in dual 12-bit mode.
FP1DE	GSERR	AN1	O	**Flat Panel Data Enable.** For port 1 in dual 12-bit mode.
FP1DET / GTVCLKIN	GD8	AM1	I	**Flat Panel Detect.** For port 1 in dual 12-bit mode.
FP1CLK	GD2	AP4	O	**Flat Panel Clock.** For port 1 in dual 12-bit mode.
FP1CLK#	GSTOP	AM3	O	**Flat Panel Clock Complement.** For port 1 in dual 12-bit mode. For double-data-rate data transfers.

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Clocks, Resets, Power Control, General Purpose I/O, Interrupts and Test

Signal Name	Pin #	I/O	Signal Description	Power Plane
HCLK+	M5	I	**Host Clock.** This pin receives the host CPU clock (100 / 133 / 166 / 200 / 266 MHz). This clock is used by all PN800 logic that is in the host CPU domain.	**VTT**
HCLK–	M6	I	**Host Clock Complement.** Used for Quad Data Transfer on host CPU bus.	**VTT**
MCLKOA	B31	O	**Memory (SDRAM) Clock A.** Output from internal clock generator to external memory interface clock buffer (if required for fanout)	**VCC25MEM**
MCLKIA	A32	I	**Memory (SDRAM) Clock Feedback.** Input from MCLKOA.	**VCC25MEM**
MCLKOB	A31	O	**Memory (SDRAM) Clock B.** Output from internal clock generator to external memory interface clock buffer (if required for fanout)	**VCC25MEM**
DISPCLKI	N3	I	**Dot Clock (Pixel Clock) In.** Used for external EMI reduction circuit if used. Connect to GND if external EMI reduction circuit not implemented.	**VCC33GFX**
DISPCLKO	N4	O	**Dot Clock (Pixel Clock) Out.** Used for external EMI reduction circuit if used. NC if external EMI reduction circuit not implemented.	**VCC33GFX**
GCLK	N7	I	**AGP Clock.** Clock for AGP logic.	**VCC15AGP**
XIN	N5	I	**Reference Frequency Input.** External 14.31818 MHz clock source. All internal graphics controller clocks are synthesized on chip using this frequency as a reference.	**VCC33GFX**
RESET#	AM13	I	**Reset.** Input from the South Bridge chip. When asserted, this signal resets the PN800 and sets all register bits to the default value. The rising edge of this signal is used to sample all power-up strap options	**VSUS15**
PWROK	AP14	I	**Power OK.** Connect to South Bridge and Power Good circuitry.	**VSUS15**
SUSST#	AN14	I	**Suspend Status.** For implementation of the Suspend-to-DRAM feature. Connect to an external pull-up to disable.	**VSUS15**

Clocks, Resets, Power Control, General Purpose I/O, Interrupts and Test (Continued)

Signal Name	Pin #	I/O	Signal Description	Power Plane
AGPBUSY# / NMI	AL14	O	**AGP Interface Busy.** Connect to a South Bridge GPIO pin for monitoring the status of the internal AGP bus. See Design Guide for details. Pin function selectable with Device 0 Function 0 RxBE[7] (default = NMI).	**VCC25MEM**
GPOUT / CAPD14	W5	O	**General Purpose Output.** This pin reflects the state of SRD[0].	**VCC33GFX**
GPO0 / CAPD15	V5	O	**General Output Port.** When SR1A[4] is cleared, this pin reflects the state of CR5C[0].	**VCC33GFX**
INTA#	U2	O	**Interrupt.** PCI interrupt output (handled by the interrupt controller in the South Bridge)	**VCC33GFX**
TCLK	W6	I	**Test Clock.** This pin is used for testing and must be connected to GND through a 1K-4.7K ohm resistor for all board designs.	**VCC33GFX**
TESTIN#	C31	I	**Test In.** This pin is used for testing and must be connected to VTT through a 1K-4.7K ohm resistor for all board designs.	**VCC25MEM**
DFTIN#	D32	I	**DFT In.** This pin is used for testing and must be connected to VTT through a 1K-4.7K ohm resistor for all board designs.	**VCC25MEM**
BISTIN / CAPAFLD	V6	I	**BIST In.** This pin is used for testing and must be tied to GND with a 1K-4.7K ohm resistor on all board designs.	**VCC33GFX**

Flat Panel Power Control (Muxed with AGP)

Signal Name	AGP Name	Pin #	I/O	Signal Description
ENAVDD	ST1	AE5	IO	**Enable Panel VDD Power.**
ENAVEE	ST0	AD6	IO	**Enable Panel VEE Power.**
ENABLT	ST2	AE6	IO	**Enable Panel Back Light.**

Note: I/O pads for all pins on this page are powered by VCC15AGP (i.e., 1.5V I/O).

5.2 PN800 North Bridge - 11

Compensation

Signal Name	Pin #	I/O	Signal Description	Power Plane
HRCOMP	F15	AI	**Host CPU Compensation.** Connect 20.5 §Ù 1% resistor to ground. Used for Host CPU interface I/O buffer calibration.	**VTT**
VLCOMPP	AM6	AI	**V-Link Compensation.** Connect a 360Ω 1% resistor to ground.	**VCC15VL**
AGPCOMPN	AB3	AI	**AGP N Compensation.** Connect a 60.4Ω1% resistor to VCC15AGP.	**VCC15AGP**
AGPCOMPP	AC6	AI	**AGP P Compensation.** Connect a 60.4Ω1% resistor to ground.	**VCC15AGP**

Reference Voltages

Signal Name	Pin #	I/O	Signal Description	Power Plane
GTLVREF	H17	P	**Host CPU Interface AGTL+ Voltage Reference.** 2/3 VTT ±2% typically derived using a resistive voltage divider. See Design Guide.	**VTT**
HDVREF[0:3]	H11, H14, K7, J7	P	**Host CPU Data Voltage Reference.** 2/3 VTT ±2% typically using a resistive voltage divider. See Design Guide.	**VTT**
HAVREF[0:1]	H19, G22	P	**Host CPU Address Voltage Reference.** 2/3 VTT ±2% typically derived using a resistive voltage divider. See Design Guide.	**VTT**
HCOMPVREF	G14	P	**Host CPU Compensation Voltage Reference.** 1/3 VTT ±2% typically derived using a resistive voltage divider. See Design Guide.	**VTT**
MEMVREF [0:5]	J29, R29, W29, AE29, AK22, AK17	P	**Memory Voltage Reference.** 0.5 VCC25MEM ±2% typically derived using a resistive voltage divider. See Design Guide.	**VCC25MEM**
VLVREF	AL7	P	**V-Link Voltage Reference.** 0.625V ±2% derived using a resistive voltage divider. See Design Guide.	**VCC15VL**
AGPVREF[0:1]	AF7, AD7	P	**AGP Voltage Reference.** ½ VCC15AGP (0.75V) for AGP 2.0 (4x transfer mode) and 0.23 VCC15AGP (0.35V) for AGP 3.0 (8x transfer mode). See the Design Guide for additional information and circuit implementation details.	**VCC15AGP**

Analog Power / Ground

Signal Name	Pin #	I/O	Signal Description
VCCA33HCK1	M4	P	**Power for Host CPU Clock PLL 1** (3.3V ±5%). Host CPU Clock PLL 1 generates 400 MHz for CPU / DRAM frequencies of multiples of 100, 133, and 200 MHz.
GNDAHCK1	M3	P	**Ground for Host CPU Clock PLL 1.** Connect to main ground plane through a ferrite bead.
VCCA33HCK2	L1	P	**Power for Host CPU Clock PLL 2** (3.3V ±5%). Host CPU Clock PLL 2 generates 500 MHz for CPU / DRAM frequencies of multiples of 166 MHz.
GNDAHCK2	L2	P	**Ground for Host CPU Clock PLL 2.** Connect to main ground plane through a ferrite bead.
VCCA33MCK	D31	P	**Power for Memory Clock PLL** (3.3V ±5%)
GNDAMCK	E31	P	**Ground for Memory Clock PLL.** Connect to main ground plane through a ferrite bead.
VCCA33GCK	M1	P	**Power for AGP Clock PLL** (3.3V ±5%)
GNDAGCK	M2	P	**Ground for AGP Clock PLL.** Connect to main ground plane through a ferrite bead.
VCCA15PLL1	P3	P	**Power for Graphics Controller PLL 1** (1.5V ±5%).
GNDAPLL1	P2	P	**Ground for Graphics Controller PLL 1.** Connect to main ground plane through a ferrite bead.
VCCA15PLL2	P6	P	**Power for Graphics Controller PLL 2** (1.5V ±5%).
GNDAPLL2	N6	P	**Ground for Graphics Controller PLL 2.** Connect to main ground plane through a ferrite bead.
VCCA15PLL3	N1	P	**Power for Graphics Controller PLL 3** (1.5V ±5%).
GNDAPLL3	N2	P	**Ground for Graphics Controller PLL 3.** Connect to main ground plane through a ferrite bead.
VCCA33DAC[1:2]	T5, P4	P	**Power for DAC.** (3.3V ±5%)
GNDADAC[1:3]	T6, P5, R4	P	**Ground for DAC.** Connect to main ground plane through a ferrite bead.

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V-Link Interface

Signal Name	Pin #	I/O	Signal Description
VD[7:0]	(see pin list)	IO	**Data Bus.** These pins are also used to send strap information to the chipset north bridge. At power up, VD7 reflects the state of a strap on SDCS3#, VD[6:4] reflect the state of straps on pins SDA[2:0], and VD[3:0] reflect the state of straps on pins Strap_VD3-0. The specific interpretation of these straps is north bridge chip design dependent.
VPAR	F24	IO	**Parity.** If the VPAR function is implemented in a compatible manner on the north bridge, this pin should be connected to the north bridge VPAR pin (P4X333, P4X400, P4X800, KT400). If VPAR is not implemented in the north bridge chip or is incompatible with the 8235CE (4x V-Link north bridges) connect this pin to an 8.2K pullup to 2.5V (Pro266, Pro266T, KT266, KT266A, KT333, P4X266, PN266, KN266, KM266, P4M266, P4N266). See app note AN222 for details.
VBE#	G24	IO	**Byte Enable.**
VCLK	L22	I	**V-Link Clock.**
UPCMD	K23	O	**Command from Client-to-Host.**
DNCMD	K25	I	**Command from Host-to-Client.**
UPSTB	J26	O	**Strobe from Client-to-Host.**
UPSTB#	J24	O	**Complement Strobe from Client-to-Host.**
DNSTB	K26	I	**Strobe from Host-to-Client.**
DNSTB#	H24	I	**Complement Strobe from Host-to-Client.**

CPU Interface

Signal Name	Pin #	I/O	Signal Description
A20M#	U26	OD	**A20 Mask.** Connect to A20 mask input of the CPU to control address bit-20 generation. Logical combination of the A20GATE input (from internal or external keyboard controller) and Port 92 bit-1 (Fast_A20).
FERR#	U24	I	**Numerical Coprocessor Error.** This signal is tied to the coprocessor error signal on the CPU. Internally generates interrupt 13 if active. Output voltage swing is programmable tot 1.5V or 2.5V by Device 17 Function 0 Rx67[2].
IGNNE#	T24	OD	**Ignore Numeric Error.** This pin is connected to the CPU iPignore errorlr pin.
INIT#	R26	OD	**Initialization.** The VT8235 Version CE asserts INIT# if it detects a shut-down special cycle on the PCI bus or if a soft reset is initiated by the register
INTR	T25	OD	**CPU Interrupt.** INTR is driven by the VT8235 Version CE to signal the CPU that an interrupt request is pending and needs service.
NMI	T26	OD	**Non-Maskable Interrupt.** NMI is used to force a non-maskable interrupt to the CPU. The VT8235 Version CE generates an NMI when PCI bus SERR# is asserted.
SLP#	V26	OD	**Sleep.** Used to put the CPU to sleep.
SMI#	U25	OD	**System Management Interrupt.** SMI# is asserted by the VT8235 Version CE to the CPU in response to different Power-Management events.
STPCLK#	R24	OD	**Stop Clock.** STPCLK# is asserted by the VT8235 Version CE to the CPU to throttle the processor clock.

Note: Connect each of the above signals to 150 §Ù pullup resistors to VCC_CMOS (see Design Guide).

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Advanced Programmable Interrupt Controller (APIC) Interface

Signal Name	Pin #	I/O	Signal Description
APICD1	T23	O	**Internal APIC Data 1.** Function 0 Rx58[6] = 1
APICD0	R25	O	**Internal APIC Data 0.** Function 0 Rx58[6] = 1
APICCLK	U23	I	**APIC Clock.**

CPU Speed Control Interface

Signal Name	Pin #	I/O	Signal Description
VRDSLP / GPI29/ GPO29	AB9	OD	**Voltage Regulator Deep Sleep.** Connected to the CPU voltage regulator. High selectsthe proper voltage for deep sleep mode. This pin performs the VRDPSLP function if Function 0 RxE5[3] = 0.
GHI# / **GPI22/ GPO22**	R22	OD	**CPU Speed Select.** Connected to the CPU voltage regulator, used to select high speed (L) or low speed (H). This pin performs the GHI# function if Function 0 RxE5[3] = 0.
DPSLP# / GPI23/ GPO23	P21	OD	**CPU Deep Sleep.** This pin performs the DPSLP# function if Device 17 Function 0RxE5[3]=0.
CPUMISS / GPI17	Y1	I	**CPU Missing.** Used to detect the physical presence of the CPU chip in its socket. High indicates no CPU present. Connect to the CPUMISS pin of the CPU socket. The state of this pin may be read in the SMBus 2 registers. This pin may be used as CPUMISS and GPI17 at the same time.
AGPBZ# / GPI6	AD10	I	**AGP Busy.** Low indicates that an AGP master cycle is in progress (CPU speed transitions will be postponed if this input is asserted low). Connected to the AGP Bus AGPBZ# pin.

PCI Bus Interface

Signal Name	Pin #	I/O	Signal Description
AD[31:0]	(see pinlist)	IO	**Address / Data Bus.** Multiplexed address and data. The address is driven with FRAME#assertion and data is driven or received in following cycles.
CBE[3:0]#	M3, L4, C1, E2	IO	**Command / Byte Enable.** The command is driven with FRAME# assertion. Byteenables corresponding to supplied or requested data are driven on following clocks.
DEVSEL#	H2	IO	**Device Select.** The VT8235 Version CE asserts this signal to claim PCI transactions through positive or subtractive decoding. As an input, DEVSEL# indicates the response to a VT8235 Version CE-initiated transaction and is also sampled when decoding whether to subtractively decode the cycle.
FRAME#	J1	IO	**Frame.** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator.
IRDY#	J2	IO	**Initiator Ready.** Asserted when the initiator is ready for data transfer.
TRDY#	H1	IO	**Target Ready.** Asserted when the target is ready for data transfer.
STOP#	K4	IO	**Stop.** Asserted by the target to request the master to stop the current transaction.
SERR#	C2	I	**System Error.** SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, the VT8235 Version CE can be programmed to generate an NMI to the CPU.
PERR#	C3	_	**Parity Error.** PERR#, sustained tri-state, is only for the reporting of data parity errors during all PCI transactions except for a Special Cycle.
PAR	F4	IO	**Parity.** A single parity bit is provided over AD[31:0] and C/BE[3:0]#.

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PCI Bus Interface (Continued)

Signal Name	Pin #	I/O	Signal Description
INTA# **INTB#** **INTC#** **INTD#** **INTE#** / GPI12, / GPO12, **INTF#** / GPI13, / GPO13, **INTG#** / GPI14, / GPO14, **INTH#** / GPI15, / GPO15	A4 B4 B5 C4 D4 E4 A3 B3	I	**PCI Interrupt Reques**t. The INTA# through INTD# pins are typically connected to thePCI bus INTA#-INTD# pins per the table below. INTE-H# are enabled by setting Device17, Function 0 Rx5B[1] = 1. BIOS settings must match the physical connection method. INTA# INTB# INTC# INTD# PCI Slot 1 INTA# NTB# INTC# INTD# PCI Slot 2 INTB# INTC# INTD# INTE# PCI Slot 3 INTC# INTD# INTE# INTF# PCI Slot 4 INTD# INTE# INTF# INTG# PCI Slot 5 INTE# INTF# INTG# INTH# PCI Slot 6 INTF# INTG# INTH# INTA#
REQ5# / GPI7, **REQ4#,** **REQ3#,** **REQ2#,** **REQ1#,** **REQ0#**	R3 P3 D5 C5 B6 A5	I	**PCI Request.** These signals connect to the VT8235 Version CE from each PCI slot (oreach PCI master) to request the PCI bus. To use pin R3 as REQ5#, Function 0 RxE4 mustbe set to 1 otherwise this pin will function as General Purpose Input 7.
GNT5# / GPO7, **GNT4#,** **GNT3#,** **GNT2#,** **GNT1#,** **GNT0#**	R2 R4 E5 C6 D6 A6	O	**PCI Grant.** These signals are driven by the VT8235 Version CE to grant PCI access to aspecific PCI master. To use pin R2 as GNT5#, Function 0 RxE4 must be set to 1otherwise this pin will function as General Purpose Output 7.
PCIRST#	R1	O	**PCI Reset.** This signal is used to reset devices attached to the PCI bus.
PCICLK	R23	I	**PCI Clock.** This signal provides timing for all transactions on the PCI Bus.
PCKRUN#	AB7	IO	**PCI Bus Clock Run.** This signal indicates whether the PCI clock is or will be stopped (high) or running (low). The VT8235 Version CE drives this signal low when the PCI clock is running (default on reset) and releases it when it stops the PCI clock. External devices may assert this signal low to request that the PCI clock be restarted or prevent it from stopping. Connect this pin to ground using a 100 §Ù resistor if the function is not used. Refer to the ihPCI Mobile Design Guidelo and applicable VIA North Bridge Design Guide (KT400A, CLE266, or P4X400) for more details.

LAN Controller - Media Independent Interface (MII)

Signal Name	Pin #	I/O	PU	Signal Description
MCOL	B11	I	***PD***	**MII Collision Detect.** From the external PHY.
MCRS	A11	I	***PD***	**MII Carrier Sense.** Asserted by the external PHY when the media is active.
MDCK	A7	O	***PD***	**MII Management Data Clock.** Sent to the external PHY as a timing reference for MDIO
MDIO	B7	IO	***PD***	**MII Management Data I/O.** Read from the MDI bit or written to the MDO bit.
MRXCLK	C9	I	***PD***	**MII Receive Clock.** 2.5 or 25 MHz clock recovered by the PHY.
MRXD[3-0]	C7, A8, B8, C8	I	***PD***	**MII Receive Data.** Parallel receive data lines driven by the external PHY synchronous with MRXCLK.
MRXDV	D8	I	***PD***	**MII Receive Data Valid.**
MRXERR	D10	I	***PD***	**MII Receive Error.** Asserted by the PHY when it detects a data decoding error.
MTXCLK	C10	I	***PD***	**MII Transmit Clock.** Always active 2.5 or 25 MHz clock supplied by the PHY.
MTXD[3-0]	A9, B9, B10, A10	O	***PD***	**MII Transmit Data.** Parallel transmit data lines synchronized to MTXCLK.
MTXENA	C11	O	***PD***	**MII Transmit Enable.** Signals that transmit is active from the MII port to the PHY.
MIIVCC	D9, E9, E10, E11	**Power**		**MII Interface Power.** 3.3V ±5%.
MIIVCC25	D12, E12	**Power**		**MII Suspend Power.** 2.5V ±5%.
RAMVCC	E7	**Power**		**Power For Internal LAN RAM.** 2.5V ±5%.
RAMGND	E6	**Power**		**Ground For Internal LAN RAM.**

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Serial EEPROM Interface

Signal Name	Pin #	I/O	PU	Signal Description
EECS#	**D11**	**O**		Serial EEPROM Chip Select.
EECK	**C12**	**O**		Serial EEPROM Clock.
EEDO	**B12**	**I**		Serial EEPROM Data Output. **Connect to EEPROM Data Out pin.**
EEDI	**A12**	**O**		Serial EEPROM Data Input. **Connect to EEPROM Data In pin.**

Low Pin Count (LPC) Interface

Signal Name	Pin #	I/O	PU	Signal Description
LFRM#	**AF6**	**IO**		LPC Frame.
LREQ#	**AE6**	**IO**		LPC DMA / Bus Master Request.
LAD[3-0]	**AD7, AE7, AF7, AD8**	**IO**	**PU**	LPC Address / Data.

Note: Connect the LPC interface LPCRST# (LPC Reset) signal to PCIRST#

System Management Bus (SMB) Interface (I 2 C Bus)

Signal Name	Pin #	I/O	Signal Description
SMBCK1	AC4	IO	**SMB / I 2 C Channel 1 Clock.**
SMBCK2 / GPI27 / GPO27	AC3	IO	**SMB / I 2 C Channel 2 Clock.** Rx95[2] = 0
SMBDT1	AB2	IO	**SMB / I 2 C Channel 1 Data.**
SMBDT2 / GPI26 / GPO26	AD1	IO	**SMB / I 2 C Channel 2 Data.** Rx95[2] = 0
SMBALRT#	AB1	I	**SMB Alert.** (enabled by System Management Bus I/O space Rx08[3] = 1) When the chip is enabled to allow it, assertion generates an IRQ or SMI interrupt or a power management resume event. Connect to a 10K ohm pullup to VSUS33 if not used.

Universal Serial Bus 2.0 Interface

Signal Name	Pin #	I/O	Signal Description
USBP0+	E20	IO	**USB 2.0 Port 0 Data +**
USBP0Œ	D20	IO	**USB 2.0 Port 0 Data Œ**
USBP1+	A20	IO	**USB 2.0 Port 1 Data +**
USBP1Œ	B20	IO	**USB 2.0 Port 1 Data Œ**
USBP2+	E18	IO	**USB 2.0 Port 2 Data +**
USBP2Œ	D18	IO	**USB 2.0 Port 2 Data Œ**
USBP3+	A18	IO	**USB 2.0 Port 3 Data +**
USBP3Œ	B18	IO	**USB 2.0 Port 3 Data Œ**
USBP4+	D16	IO	**USB 2.0 Port 4 Data +**
USBP4Œ	E16	IO	**USB 2.0 Port 4 Data Œ**
USBP5+	A16	IO	**USB 2.0 Port 5 Data +**
USBP5Œ	B16	IO	**USB 2.0 Port 5 Data Œ**
USBCLK	E23	I	**USB 2.0 Clock.** 48MHz clock input for the USB interface
USBOC0#	C26	I	**USB 2.0 Port 0 Over Current Detect.** Port 0 is disabled if low.
USBOC1#	D24	I	**USB 2.0 Port 1 Over Current Detect.** Port 1 is disabled if low.
USBOC2#	B26	I	**USB 2.0 Port 2 Over Current Detect.** Port 2 is disabled if low.
USBOC3#	C25	I	**USB 2.0 Port 3 Over Current Detect.** Port 3 is disabled if low.
USBOC4#	B24	I	**USB 2.0 Port 4 Over Current Detect.** Port 4 is disabled if low.
USBOC5#	A24	I	**USB 2.0 Port 5 Over Current Detect.** Port 5 is disabled if low.
USBVCC	(see pin list)	**Power**	**USB 2.0 Port Differential Output Interface Logic Voltage.** 3.3V
USBGND	(see pin list)	**Power**	**USB 2.0 Port Differential Output Interface Logic Ground.**
VSUSUSB	C24	**Power**	**USB 2.0 Suspend Power.** 2.5V ±5%.
VCCUPLL	A23, B23	**Power**	**USB 2.0 PLL Analog Voltage.** 2.5V ±5%.
GNDUPLL	C23, D23	**Power**	**USB 2.0 PLL Analog Ground.**

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UltraDMA-133 / 100 / 66 / 33 Enhanced IDE Interface

Signal Name	Pin #	I/O	Signal Description
PDRDY /PDDMARDY /PDSTROBE	Y22	I	EIDE Mode: **Primary I/O Channel Ready.** Device ready indicator UltraDMA Mode: **Primary Device DMA Read**y. Output flow control. The device mayassert DDMARDY to pause output transfers **Primary Device Strob**e. Input data strobe (both edges). The device may stop DSTROBE to pause input data transfers
SDRDY /SDDMARDY /SDSTROBE	AF17	I	EIDE Mode: **Secondary I/O Channel Ready.** Device ready indicator UltraDMA Mode: **Secondary Device DMA Read**y. Output flow control. The devicemay assert DDMARDY to pause output transfers **Secondary Device Strob**e. Input data strobe (both edges). The device may stop DSTROBE to pause input data transfers
PDIOR# /PHDMARDY /PHSTROBE	W26	O	EIDE Mode: **Primary Device I/O Read.** Device read strobe UltraDMA Mode: **Primary Host DMA Read**y. Primary channel input flow contro**l.** Thehost may assert HDMARDY to pause input transfers **Primary Host Strob**e. Output data strobe (both edges). The host may stop HSTROBE to pause output data transfers
SDIOR# /SHDMARDY /SHSTROBE	AF23	O	EIDE Mode: **Secondary Device I/O Read.** Device read strobe UltraDMA Mode: **Secondary Host DMA Read**y. Input flow control. The host mayassert HDMARDY to pause input transfers **Host Strobe** B. Output strobe (both edges). The host may stop HSTROBE to pause output data transfers
PDIOW# /PSTOP	Y25	O	EIDE Mode: **Primary Device I/O Write.** Device write strobe UltraDMA Mode: **Primary Sto**p. Stop transfer: Asserted by the host prior to initiation of an UltraDMA burst; negated by the host before data is transferred in an UltraDMA burst. Assertion of STOP by the host during or after data transfer in UltraDMA mode signals the termination of the burst.
SDIOW# /SSTOP	AE23	O	EIDE Mode: **Secondary Device I/O Write.** Device write strobe UltraDMA Mode: **Secondary Sto**p. Stop transfer: Asserted by the host prior to initiation of an UltraDMA burst; negated by the host before data is transferred in an UltraDMA burst. Assertion of STOP by the host during or after data transfer in UltraDMA mode signals the termination of the burst.
PDDRQ	Y23	I	**Primary Device DMA Request.** Primary channel DMA request
SDDRQ	AD17	I	**Secondary Device DMA Request.** Secondary channel DMA request

UltraDMA-133 / 100 / 66 / 33 Enhanced IDE Interface (Continued)

Signal Name	Pin #	I/O	Signal Description
PDDACK#	Y24	O	**Primary Device DMA Acknowledge.** Primary channel DMA acknowledge
SDDACK#	AD23	O	**Secondary Device DMA Acknowledge.** Secondary channel DMA acknowledge
IRQ14	AD24	I	**Primary Channel Interrupt Request.**
IRQ15	AE26	I	**Secondary Channel Interrupt Request.**
PDCS1#	V22	O	**Primary Master Chip Select.** This signal corresponds to CS1FX# on the primary IDE connector.
PDCS3#	V23	O	**Primary Slave Chip Select.** This signal corresponds to CS3FX# on the primary IDE connector.
SDCS1# / strap	AF25	O	**Secondary Master Chip Select.** This signal corresponds to CS17X# on the secondary IDE connector. Strap low (resistor to ground) to enable serial EEPROM interface via the MII bus (this disables the EExx pins). This pin has an internal pullup to default to serial EEPROM interface via the EExx pins.
SDCS3# / strap	AF26	O	**Secondary Slave Chip Select.** This signal corresponds to CS37X# on the secondary IDE connector. Strap information is communicated to the north bridge via VD[7].
PDA[2-0]	W24, V25, W23	O	**Primary Disk Address.** PDA[2:0] are used to indicate which byte in either the ATA command block or control block is being accessed.
SDA[2-0] / strap	AE24, AC22, AF24	O	**Secondary Disk Address.** SDA[2:0] are used to indicate which byte in either the ATA command block or control block is being accessed. Strap information is communicated to the north bridge via VD[6:4].
PDD[15-0]	(see pin list)	IO	**Primary Disk Data.**
SDD[15-0]	(see pin list)	IO	**Secondary Disk Data.**

Serial IRQ

Signal Name	Pin #	I/O	Signal Description
SERIRQ	AD9	I	**Serial IRQ.** This pin has an internal pull-up resistor.

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AC97 Audio / Modem Interface

Signal Name	Pin #	I/O	Signal Description
ACRST#	T3	O	**AC97 Reset.**
ACBTCK	T1	I	**AC97 Bit Clock.**
ACSYNC	T2	O	**AC97 Sync.**
ACSDO	U2	O	**AC97 Serial Data Out.**
ACSDIN0 (VSUS33)*f*	U3	I	**AC97 Serial Data In 0.**
ACSDIN1 (VSUS33)*f*	V2	I	**AC97 Serial Data In 1.**
ACSDIN2 / GPIO20 / PCS0#	U1	I	**AC97 Serial Data In 2.** RxE4[6]=0,E5[1]=0, PMIO Rx4C[20]=1
ACSDIN3 / GPIO21 / PCS1# / SLPBTN#	V3	I	**AC97 Serial Data In 3.** RxE4[6]=0,E5[2]=0, PMIO Rx4C[21]=1

Resets, Clocks, and Power Status

Signal Name	Pin #	I/O	Signal Description
PWRGD	**AC5**	**I**	**Power Good.** Connected to the Power Good signal on the Power Supply. Internal logic **powered by VBAT.**
PWROK#	**AF1**	**O**	**Power OK.** Internal logic powered by VSUS33.
PCIRST#	**R1**	**O**	**PCI Reset.** Active low reset signal for the PCI bus. The VT8235 Version CE will assert this pin during power-up or from the control register.
OSC	**AB8**	**I**	**Oscillator.** 14.31818 MHz clock signal used by the internal Timer.
RTCX1	**AE4**	**I**	**RTC Crystal Input**: 32.768 KHz crystal or oscillator input. This input is used for the internal RTC and power-well power management logic and is powered by VBAT.
RTCX2	**AF3**	**O**	**RTC Crystal Output**: 32.768 KHz crystal output. Internal logic powered by VBAT.
TEST	**AE9**	**I**	**Test.**
TPO	**AF9**	**O**	**Test Pin Output.** Output pin for test mode.
NC	**(see pin list)**	**–**	**No Connect.** Do not connect.

Internal Keyboard Controller

Signal Name	Pin #	I/O	PU	Signal Description
MSCK / IRQ1	**W1**	**IO / I**	**PU**	**MultiFunction Pin** (Internal mouse controller enabled by Rx51[1]) Rx51[2]=1 **Mouse Clock.** From internal mouse controller. **Rx51[2]=0** Interrupt Request **1. Interrupt input 1.**
MSDT / IRQ12	**W2**	**IO / I**	**PU**	**MultiFunction Pin** (Internal mouse controller enabled by Rx51[1]) Rx51[2]=1 **Mouse Data.** From internal mouse controller. Rx51[2]=0 **Interrupt Request 1**2. Interrupt input 12.
KBCK / KA20G	**W3**	**IO / I**	**PU**	**MultiFunction Pin** (Internal keyboard controller enabled by Rx51[0]) Rx51[0]=1 **Keyboard Clock.** From internal keyboard controller Rx51[0]=0 **Gate A20.** Input from external keyboard controller.
KBDT / KBRC	**V1**	**IO / I**	**PU**	**MultiFunction Pin** (Internal keyboard controller enabled by Rx51[0]) Rx51[0]=1 **Keyboard Data.** From internal keyboard controller. Rx51[0]=0 **Keyboard Reset.** From external keyboard controller (KBC) for CPURST# generation
KBCS# / strap	**AF10**	**O**		**Keyboard Chip Select** (Rx51[0]=0). To external keyboard controller chip. Strap high to enable LPC BIOS ROM.

Note: KBCK, KBDT, MSCK, and MSDT are powered by the VSUS33 suspend voltage plane.

Speaker

Signal Name	Pin #	I/O	PU	Signal Description
SPKR / strap	**AF8**	**O**		**Speaker.** Strap low to enable (high to disable) CPU frequency **strapping.**

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General Purpose Inputs

Signal Name	Pin #	I/O	Signal Description
GPI0 ***(VBAT)***	**AE2**	**I**	General Purpose Input 0. **Status on PMIO Rx20[0]**
GPI1 ***(VSUS33)***	**AC2**	**I**	General Purpose Input 1. **Status on PMIO Rx20[1]**
GPI2 / EXTSMI# ***(VSUS33)***	**AA1**	**I**	General Purpose Input 2. **Status on PMIO Rx20[4]**
GPI3 / RING# ***(VSUS33)***	**Y2**	**I**	General Purpose Input 3. **Status on PMIO Rx20[8]**
GPI4 / LID# ***(VSUS33)***	**AC1**	**I**	General Purpose Input 4. **Status on PMIO Rx20[11]**
GPI5 / BATLOW# ***(VSUS33)***	**V4**	**I**	General Purpose Input 5. **Status on PMIO Rx20[12]**
GPI6 / AGPBZ#	**AD10**	**I**	General Purpose Input 6. **Status on PMIO Rx20[5]**
GPI7 / REQ5#	**R3**	**I**	General Purpose Input 7. **RxE4[2] = 0**
GPI12 / GPO12 / INTE#	**D4**	**I**	General Purpose Input 12. **RxE4[4] = 0, 5B[1]=0**
GPI13 / GPO13 / INTF#	**E4**	**I**	General Purpose Input 13. **RxE4[4] = 0, 5B[1]=0**
GPI14 / GPO14 / INTG#	**A3**	**I**	General Purpose Input 14. **RxE4[4] = 0, 5B[1]=0**
GPI15 / GPO15 / INTH#	**B3**	**I**	General Purpose Input 15. **RxE4[4] = 0, 5B[1]=0**
GPI16 / INTRUDER# ***(VBAT)***	**AE1**	**I**	General Purpose Input 16. **Status on PMIO Rx20[6]**
GPI17 / CPUMISS	**Y1**	**I**	General Purpose Input 17. **Status on PMIO Rx20[5]**
GPI18 / THRM# / AOLGPI	**Y4**	**I**	General Purpose Input 18. **Rx8C[3] = 0**
GPI20 / GPO20 / ACSDIN2 / PCS0#	**U1**	**I**	**General Purpose Input 20.** RxE4[6]=1, E5[1]=0, **PMIO 4C[20] = 1**
GPI21 / GPO21 / ACSDIN3 / PCS1# / SLPBTN#	**V3**	**I**	**General Purpose Input 21.** RxE4[6]=1, E5[2]=0 PMIO 4C[21] = 1
GPI22 / GPO22 / GHI#	**R22**	**I**	**General Purpose Input 22.** RxE5[3] = 1, PMIO 4C[22] = 1
GPI23 / GPO23 / DPSLP#	**P21**	**I**	**General Purpose Input 23.** RxE5[3] = 1, PMIO 4C[23] = 1

General Purpose Inputs (Continued)

Signal Name	Pin #	I/O	Signal Description
GPI26 / GPO26 / SMBDT2 ***(VSUS33)***	**AD1**	**I**	**General Purpose Input 26.** Rx95[2] = 1, 95[3] = 0
GPI27 / GPO27 / SMBCK2 ***(VSUS33)***	**AC3**	**I**	**General Purpose Input 27.** Rx95[2] = 1, 95[3] = 0
GPI28 / GPO28	**AC8**	**I**	**General Purpose Input 28.** RxE5[3] = 1, PMIO 4C[28] = 1
GPI29 / GPO29 / VRDSLP	**AB9**	**I**	**General Purpose Input 29.** RxE5[3] = 1, PMIO 4C[29] = 1

Note: Register references above are Device 17 Function 0 unless indicated otherwise.
Note: Default pin function is underlined in the signal name column above.
Note: Input pin status for the above GPI pins 31-0 is also available on PMIO Rx4B-48[31-0]
Note: See also Power Management I/O register Rx50 for input pin change status for GPI16-19 and 24-27
Note: See also Power Management I/O register Rx52 for SCI/SMI select for GPI16-19 and 24-27
Note: See also Power Management I/O register Rx4C. General purpose input pins 20-31 are shared with OD (open drain) general

Programmable Chip Selects

Signal Name	Pin #	I/O	Signal Description
PCS0# / GPIO20 / ACSDIN2	**U1**	**O**	Programmable Chip Select 0. **RxE4[6]=1, E5[1]=1**
PCS1# / GPIO21 / ACSDIN3 / SLPBTN#	**V3**	**O**	Programmable Chip Select 1. **RxE4[6]=1, E5[2]=1**

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General Purpose Outputs

Signal Name	Pin #	I/O	Signal Description
GPO0 ***(VSUS33)***	**AA3**	**O**	General Purpose Output 0.
GPO1 / SUSA# ***(VSUS33)***	**AA2**	**O**	General Purpose Output 1. **Rx94[2] = 1**
GPO2 / SUSB# ***(VSUS33)***	**AD3**	**O**	General Purpose Output 2. **Rx94[3] = 1**
GPO3 / SUSST1# ***(VSUS33)***	**Y3**	**O**	General Purpose Output 3. **Rx94[4] = 1**
GPO4 / SUSCLK ***(VSUS33)***	**AB3**	**O**	General Purpose Output 4. **Rx95[1] = 1**
GPO5 / CPUSTP#	**AC7**	**O**	General Purpose Output 5. **RxE4[0] = 1**
GPO6 / PCISTP#	**AD6**	**O**	General Purpose Output 6. **RxE4[1] = 1**
GPO7 / GNT5#	**R2**	**O**	General Purpose Output 7. **RxE4[2] = 0**
GPO12 / GPI12 / INTE#	**D4**	**O**	General Purpose Output 12. **RxE4[4]=1, 5B[1]=0**
GPO13 / GPI13 / INTF#	**E4**	**O**	General Purpose Output 13. **RxE4[4]=1, 5B[1]=0**
GPO14 / GPI14 / INTG#	**A3**	**O**	General Purpose Output 14. **RxE4[4]=1, 5B[1]=0**
GPO15 / GPI15 / INTH#	**B3**	**O**	General Purpose Output 15. **RxE4[4]=1, 5B[1]=0**
GPO20 / GPI20 / ACSDIN2 / PCS0#	**U1**	**OD**	General Purpose Output 20. **RxE4[6]=1, E5[1]=0**
GPO21 / GPI21 / ACSDIN3 / PCS1# /SLPBTN#	**V3**	**OD**	General Purpose Output 21. **RxE4[6]=1, E5[2]=0**
GPO22 / GPI22 / GHI#	**R22**	**OD**	General Purpose Output 22. **RxE5[3]=1, PMIO 4C[22]=1**
GPO23 / GPI23 / DPSLP#	**P21**	**OD**	General Purpose Output 23. **RxE5[3]=1, PMIO 4C[23]=1**
GPO26 / GPI26 / SMBDT2 ***(VSUS33f)***	**AD1**	**OD**	General Purpose Output 26. **Rx95[2] = 1, 95[3] = 1**
GPO27 / GPI27 / SMBCK2 ***(VSUS33f)***	**AC3**	**OD**	General Purpose Output 27. **Rx95[2] = 1, 95[3] = 1**

General Purpose Outputs (Continued)

Signal Name	Pin #	I/O	Signal Description
GPO28 / GPI28	**AC8**	**OD**	General Purpose Output 28. **RxE5[3] = 1, PMIO 4C[28]=1**
GPO29 / GPI29 / VRDSLP	**AB9**	**OD**	General Purpose Output 29. **RxE5[3] = 1, PMIO 4C[29]=1**

Note: The output state for each of the above general purpose outputs is selectable via Power Management I/O registers Rx4C-48
Note: Default pin functions are underlined in the table above.

Power Management and Event Detection

Signal Name	Pin #	I/O	Signal Description
PWRBTN#	**AD2**	**I**	**Power Button.** Used by the Power Management subsystem to monitor an external **system on/off button or switch. Internal logic powered by VSUS33.**
SLPBTN# / GPIO21/ ACSDIN3 / PCS1#	**V3**	**I**	**Sleep Button.** Used by the Power Management subsystem to monitor an external sleepbutton or switch. RxE4[6] = 1, 80[6] = 1, E5[2] = 0 and PMIO Rx4C[21] = 1
RSMRST#	**AD4**	**I**	**Resume Reset.** Resets the internal logic connected to the VSUS33 power plane and also resets portions of the internal RTC logic. Internal logic powered by VBAT.
EXTSMI# / GPI2	**AA1**	**IOD**	**External System Management Interrupt.** When enabled to allow it, a falling edge on this input causes an SMI# to be generated to the CPU to enter SMI mode. (10K PU to VSUS33 if not used) (3.3V only)
PME#	**W4**	**I**	**Power Management Event.** (10K PU to VSUS33 if not used)
SMBALRT#	**AB1**	**I**	**SMB Aler**t. When programmed to allow it (SMB I/O Rx8[3]=1), assertion generates an IRQ, SMI, or power management event. (10K PU to VSUS33 if not used)

5.3 VT8235CE South Bridge - 9

Power Management and Event Detection (Continued)

Signal Name	Pin #	I/O	Signal Description
LID# / GPI4	**AC1**	**I**	**Notebook Computer Display Lid Open / Closed Monitor.** Used by the Power Management subsystem to monitor the opening and closing of the display lid of notebook computers. Can be used to detect either low-to-high or high-to-low transitions to generate an SMI#. (10K PU to VSUS33 if not used)
INTRUDER# / GPI16	**AE1**	**I**	**Intrusion Indicator.** The value of this bit may be read at PMIO Rx20[6]
THRM# / GPI18/ AOLGPI	**Y4**	**I**	**Thermal Alarm Monitor.** Rx8C[3] = 1. Rising or falling edges (selectable by PMIORx2C[6]) may be detected to set status at PMIO Rx20[10]. Setting of this status bit may then be used to generate an SCI or SMI. THRM# may also be used to enable duty cycle control of stop-clock (STPCLK#) to automatically limit maximum temperature (see Device 17 Function 0 Rx8C[7-4]).
RING# / GPI3	**Y2**	**I**	**Ring Indicator.** May be connected to external modem circuitry to allow the system to be re-activated by a received phone call. (10K PU to VSUS33 if not used)
BATLOW# / GPI5	**V4**	**I**	**Battery Low Indicator.** (10K PU to VSUS33 if not used) (3.3V only)
CPUSTP# / GPO5	**AC7**	**O**	**CPU Clock Stop** (RxE4[0] = 0). Signals the system clock generator to disable the CPU clock outputs. Not connected if not used.
PCISTP# / GPO6	**AD6**	**O**	**PCI Clock Stop** (RxE4[1] = 0). Signals the system clock generator to disable the PCI clock outputs. Not connected if not used.
SUSA# / GPO1	**AA2**	**O**	**Suspend Plane A Control** (Rx94[2]=0). Asserted during power management POS, STR, and STD suspend states. Used to control the primary power plane. (10K PU to VSUS33 if not used)
SUSB# / GPO2	**AD3**	**O**	**Suspend Plane B Control** (Rx94[3]=0). Asserted during power management STR and STD suspend states. Used to control the secondary power plane. (10K PU to VSUS33 if not used)
SUSC#	**AF2**	**O**	**Suspend Plane C Control.** Asserted during power management STD suspend state. Used to control the tertiary power plane. Also connected to ATX power-on circuitry. (10K PU to VSUS33 if not used)

Power Management and Event Detection (Continued)

Signal Name	Pin #	I/O	Signal Description
SUSST1# / GPO3	**Y3**	**O**	**Suspend Status 1** (Rx94[4] = 0). Typically connected to the North Bridge to provide information on host clock status. Asserted when the system may stop the host clock, such as Stop Clock or during POS, STR, or STD suspend states. Connect 10K PU to VSUS33.
SUSCLK	**AB3**	**O**	**Suspend Clock.** 32.768 KHz output clock for use by the North Bridge (e.g., KT400A, CLE266, or P4X400) for DRAM refresh purposes. Stopped during Suspend-to-Disk and Soft-Off modes. Connect 10K PU to VSUS33.
CPUMISS / GPI17	**Y1**	**I**	**CPU Missing.** Used to detect the physical presence of the CPU chip in its socket. High indicates no CPU present. Connect to the CPUMISS pin of the CPU socket. The state of this pin may be read in the SMBus 2 registers. This pin may be used as CPUMISS and GPI17 at the same time.
AOLGPI / GPI18/ THRM#	**Y4**	**I**	**Alert On LAN.** The state of this pin may be read in the SMBus 2 registers. This pinmay be used as AOLGPI, GPI18 and THRM# all at the same time.

Strap Pins for VT8235 Version CE Configuration

Signal Name	Pin #	Function	Description	Note
Strap_AUTO	**AE10**	**Auto Reboot**	L: Enable Auto Reboot **H: Disable Auto Reboot (Default)**	
SPKR	**AF8**	**CPU Frequency Strapping**	L: Enable CPU Frequency Strapping H: Disable CPU Frequency Strapping (Default)	
KBCS#	**AF10**	**Internal Keyboard** Controller	L: Disable internal KBC H: Enable internal KBC (Default)	
SDCS1#	**AF25**	Eliminate External LAN EEPROM	L: Enable. Use external EEPROM (Default) H: Disable. Do not use external EEPROM	

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Power and Ground

Signal Name	Pin #	I/O	Signal Description
VSUS33	AA4, AB4-6	P	**Suspend Power.** 3.3V ±5%. Always available unless the mechanical switch of the power supply is turned off. If the ihsoft-offlÉD state is not implemented, then this pin can be connected to VCC33. Signals powered by or referenced to this plane are: PWRGD, RSMRST#, PWRBTN#, SMBCK1/2, SMBDT1/2, GPO0, SUSA# / GPO1, SUSB# / GPO2, SUSC#, SUSST1# / GPO3, SUSCLK / GPO4, GPI1, GPI2 / EXTSMI#, GPI3 / RING#, GPI4 / LID, GPI5 / BATLOW#, GPI6 / PME#, SMBALRT#
VSUS25	T4, U4	P	**Suspend Power.** 2.5V ±5%.
VSUSUSB	C24	P	**USB Suspend Power.** 2.5V ±5%.
VBAT	AF4	P	**RTC Battery.** Battery input for internal RTC (RTCX1, RTCX2)
VLVREF	H22	P	**V-Link Voltage Reference.** 0.9V ±5% for 4x transfers and 0.625V ±5% for 8x transfers.
VLCOMP	J22	AI	**V-Link Compensation.**
VCCVK	(see pin list)	P	**V-Link Compensation Circuit Voltage.** 2.5V ±5%
MIIVCC	D9, E9-11	P	**LAN MII Power.** 3.3V ±5%.Power for LAN Media Independent Interface (interface to external PHY). Connect to VCC33 through a ferrite bead.
MIIVCC25	D12. E12	P	**LAN MII Suspend Power.** 2.5V ±5%.
LANVCC	E7	P	**LAN Power.** 2.5V ±5%. Power for LAN. Connect to VCC through a ferrite bead.
LANGND	E6	P	**LAN Ground.** Connect to GND through a ferrite bead.
USBVCC	(see pin list)	P	**USB 2.0 Differential Output Power.** 3.3V ±5%. Power for USB differential outputs (USBP0+, P0Œ, P1+, P1Œ, P2+, P2Œ, P3+, P3Œ, P4+, P4Œ, P5+, P5Œ). Connect to VSUS33 through a ferrite bead.
USBGND	(see pin list)	P	**USB 2.0 Differential Output Ground.** Connect to GND through a ferrite bead.
VCCUPLL	A23, B23	P	**USB 2.0 PLL Analog Voltage.** 2.5V ±5%. Connect to VCC through a ferrite bead.
GNDUPLL	C23, D23	P	**USB 2.0 PLL Analog Ground.** Connect to GND through a ferrite bead.
PLLVCC	T22	P	**PLL Analog Power.** 2.5V ±5%. Connect to VCC through a ferrite bead.
PLLGND	U22	P	**PLL Analog Ground.** Connect to GND through a ferrite bead.

Power and Ground (Continued)

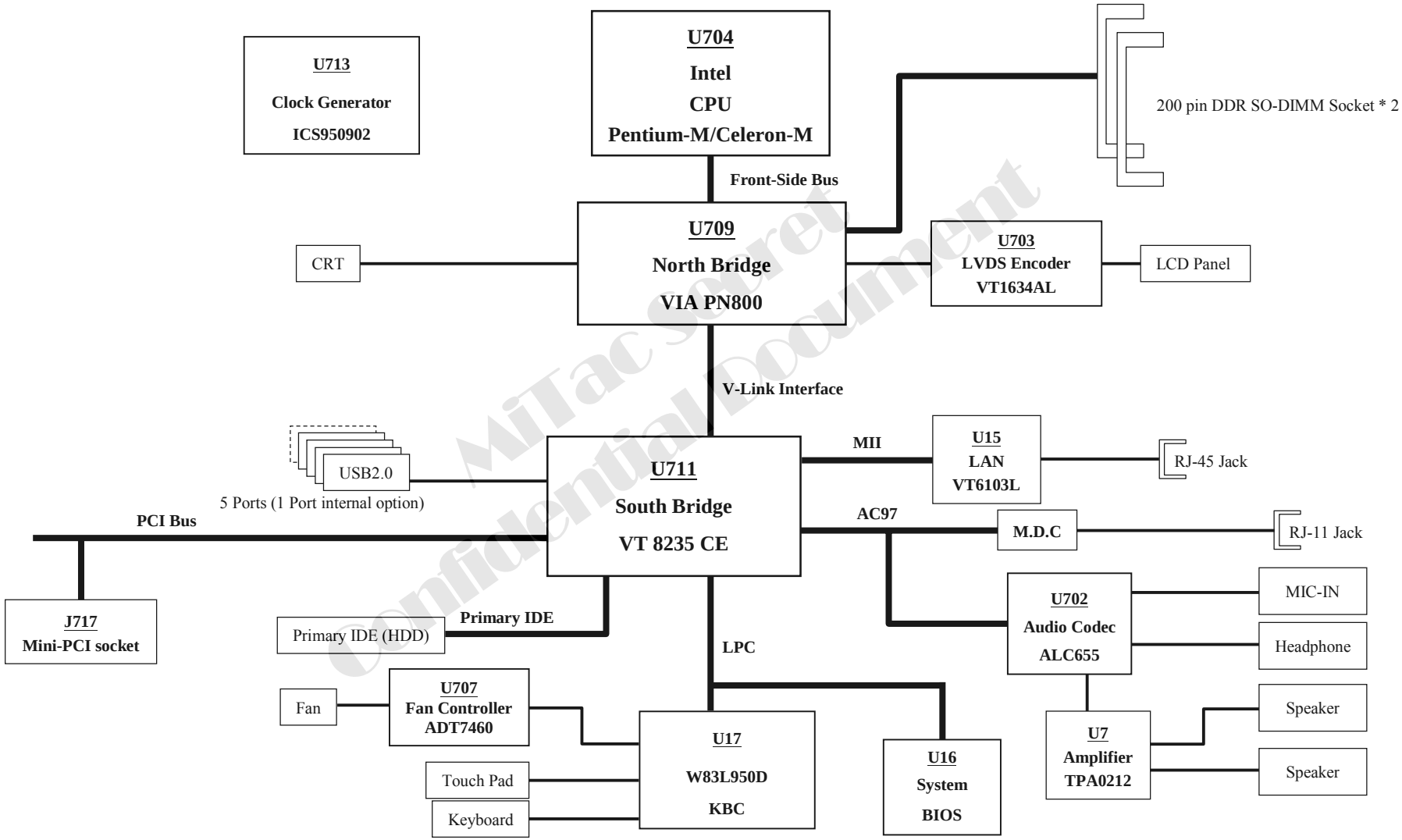
Signal Name	Pin #	I/O	Signal Description
VCC33	(see pin list)	P	I/O Power. **3.3V ±5%**
VCC	(see pin list)	P	Core Power. **2.5V ±5%. This supply is turned on only when the mechanical switch on the power supply is turned on and the PWRON signal is conditioned high.**
GND	(see pin list)	P	**Ground.** Connect to primary motherboard ground plane.

Strap Pins for North Bridge Configuration

Signal Name	Pin #	Function	Description	Note
SDCS3#	AF26	NB Configuration	SDCS3# signal state is reflected on signal pinVD[7] during power up for North Bridgeconfiguration.	**Check the NorthBridge DS fordetails**
SDA2	AE24	NB Configuration	SDA2 signal state is reflected on signal pinVD[6] during power up for North Bridgeconfiguration.	**Check the NorthBridge DS fordetails**
SDA1	AC22	NB Configuration	SDA1 signal state is reflected on signal pinVD[5] during power up for North Bridgeconfiguration.	**Check the NorthBridge DS fordetails**
SDA0	AF24	NB Configuration	SDA0 signal states is reflected on signal pinsVD[4] during power up for North Bridgeconfiguration.	**Check the NorthBridge DS fordetails**
Strap_VD3	AC6	NB Configuration	Strap_VD3 signal state is reflected on signal pinVD[3] during power up for North Bridgeconfiguration.	**Check the NorthBridge DS fordetails**
Strap_VD2	AD5	NB Configuration	Strap_VD2 signal state is reflected on signal pinVD[2] during power up for North Bridgeconfiguration.	**Check the NorthBridge DS fordetails**
Strap_VD1	AE5	NB Configuration	Strap_VD1 signal state is reflected on signal pin, VD[1] during power up for North Bridge configuration.	**Check the North Bridge DS for details**
Strap_VD0	AF5	NB Configuration	Strap_VD0 signal state is reflected on signalpin, VD[0] during power up for North Bridgeconfiguration.	**Check the NorthBridge DS fordetails**

Note: Internal Pullups are present on pins KBCK, KBDT, MSCK, MSDT, SERIRQ, LAD[3:0]
Internal Pulldowns are present on all LAN pins

6. System Block Diagram



7. Maintenance Diagnostics

7.1 Introduction

Each time the computer is turned on, the system bios runs a series of internal checks on the hardware. This power-on self test (post) allows the computer to detect problems as early as the power-on stage. Error messages of post can alert you to the problems of your computer.

If an error is detected during these tests, you will see an error message displayed on the screen. If the error occurs before the display is initialized, then the screen cannot display the error message. Error codes or system beeps are used to identify a post error that occurs when the screen is not available.

The value for the diagnostic port (378H) is written at the beginning of the test. Therefore, if the test failed, the user can determine where the problem occurred by reading the last value written to port 378H by the Mini PCI debug board.

7.2 Error Codes (1)

Following is a list of error codes in sequent display on the MINI PCI debug board.

Code	POST Routine Description
10h	Signals that Reset occurred
11h	Turn off FAST A20 for POST
12h	Signal power on reset
13h	Initialize the chipset
14h	Search for ISA Bus VGA adapter
15h	Reset counter / Timer 1
16h	User register config through CMOS
17h	Size memory
18h	Dispatch to RAM test
19h	Check sum the ROM
1Ah	Reset PIC's
1Bh	Initialize video adapter
1Ch	Initialize video
1Dh	Initialize color adapter
1Eh	Initialize monochrome adapter
1Fh	Test 8237A page registers

Code	POST Routine Description
20h	Test keyboard
21h	Test keyboard controller
22h	Check if CMOS RAM valid
23h	Test battery fail & CMOS X-SUM
24h	Test DMA controller
25h	Initialize 8237A controller
26h	Initialize int vectors
27h	RAM quick sizing
28h	Protected mode entered safely
29h	RAM test completed
2Ah	Protected mode exit successful
2Bh	Setup shadow
2Ch	Going to initialize video
2Dh	Search for monochrome adapter
2Eh	Search for color adapter
2Fh	Sign-on messages displayed

7.2 Error Codes (2)

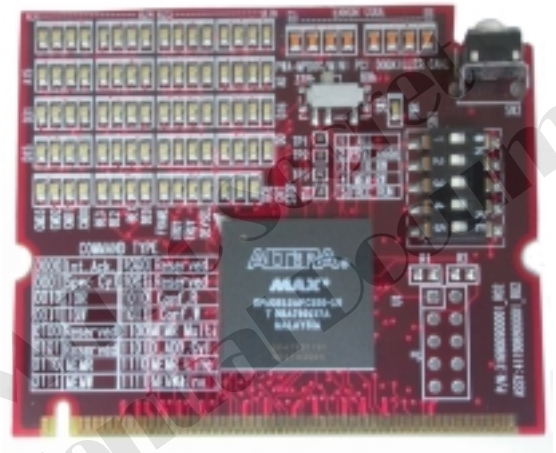
Following is a list of error codes in sequent display on the MINI PCI debug board.

Code	POST Routine Description
30h	OEM initialization of keyboard controller
31h	Test if keyboard Present
32h	Test keyboard Interrupt
33h	Test keyboard command byte
34h	Test, blank and count all RAM
35h	Protected mode entered safely(2)
36h	RAM test complete
37h	Protected mode exit successful
38h	Update keyboard controller output port
39h	Setup cache controller
3Ah	Test if 18.2Hz periodic working
3Bh	Test for RTC ticking
3Ch	Initialize the hardware vectors
3Dh	Search for and initialize the mouse
3Eh	Update NUMLOCK status
3Fh	OEM initialization of COM and LPT ports

Code	POST Routine Description
40h	Configure the COMM and LPT ports
41h	Initialize the floppies
42h	Initialize the hard disk
43h	Initialize option ROMs
44h	OEM's initialization of power management
45h	Update NUMLOCK status
46h	Test for coprocessor installed
47h	OEM functions before boot
48h	Dispatch to operate system boot
49h	Jump into bootstrap code

7.3 Debug Tool

7.3.1 Diagnostic Tool for Mini PCI Slot :



P/N:411906900001
Description: PWA-MPDOG;MINI PCI DOGKELLER CARD
Note: Order it from MIC/TSSC

8. Trouble Shooting

- 8.1 No Power (*1)
- 8.2 Battery Can not Be Charged
- 8.3 No Display (*2)
- 8.4 LCD No Display or Picture Abnormal
- 8.5 External Monitor No Display or Color Abnormal
- 8.6 Memory Test Error
- 8.7 Keyboard (K/B) Touch-Pad (T/P) Test Error
- 8.8 Hard Disk Drive Test Error
- 8.9 USB Port Test Error
- 8.10 Mini-PCI Socket Test Error
- 8.11 Audio Test Error
- 8.12 LAN Test Error

8965 N/B Maintenance

*1: No Power Definition

Base on ACPI Spec. We define the no power as while we press the power button, the system can't leave S5 status or none the PG signal send out from power supply.

Judge condition:

- Check whether there are any voltage feedback control to turn off the power.
- Check whether no CPU power will cause system can't leave S5 status.

If there are not any diagram match these condition, we should stop analyzing the schematic in power supply sending out the PG signal. If yes, we should add the effected analysis into no power chapter.

*2: No Display Definition

Base on the digital IC three basic working conditions: working power, reset, Clock. We define the no display as while system leave S5 status but can't get into S0 status.

Judge condition:

- Check which power will cause no display
- Check which reset signal will cause no display
- Check which Clock signal will cause no display

Base on these three conditions to analyze the schematic and edit the no display chapter.

Keyword:

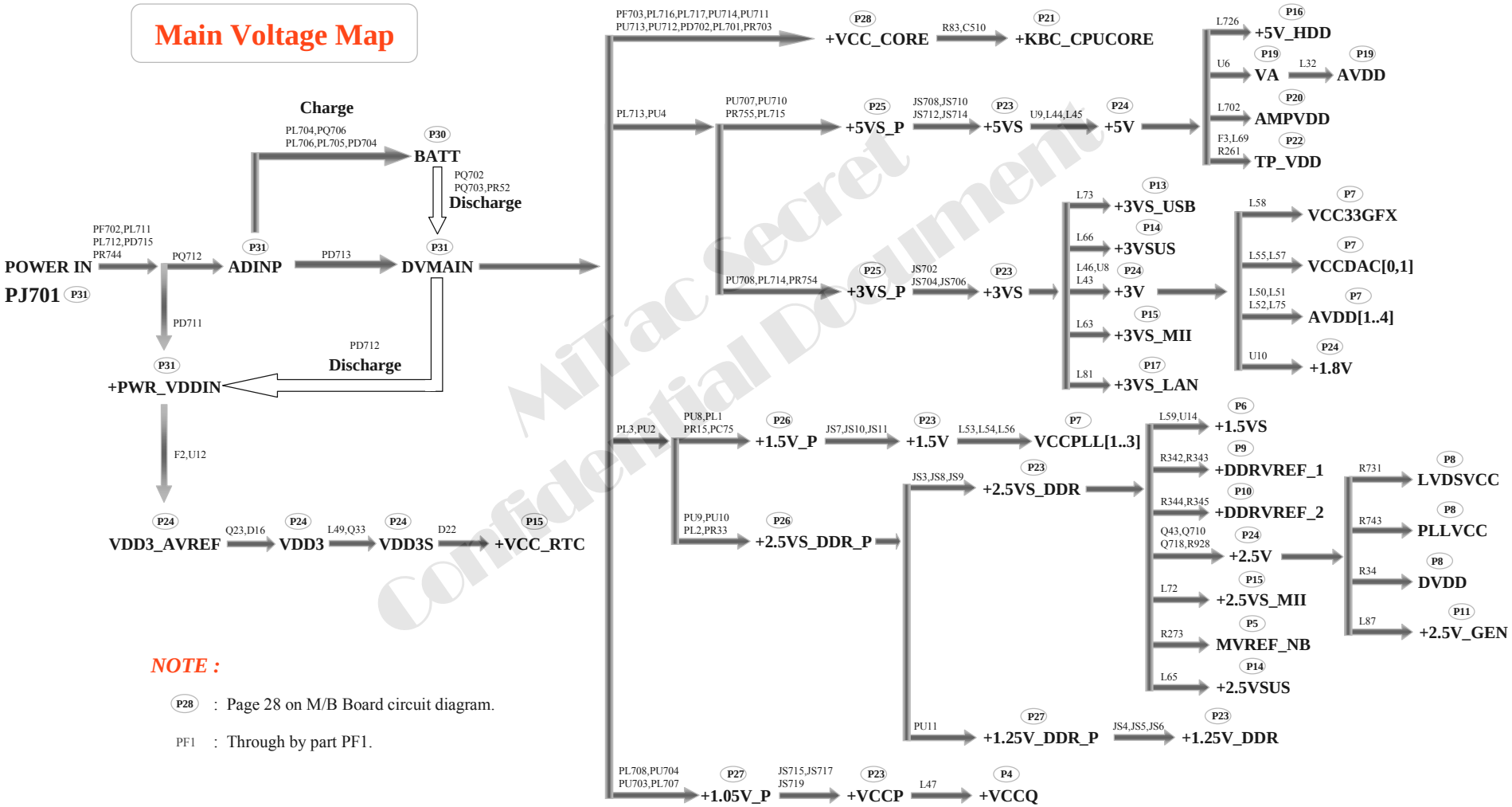
- S5: *Soft Off*
- S0: *Working*

For detail please refer the ACPI specification

8965 N/B Maintenance

8.1 No Power (1)

When power button is pressed, nothing happens, power indicator does not light up.



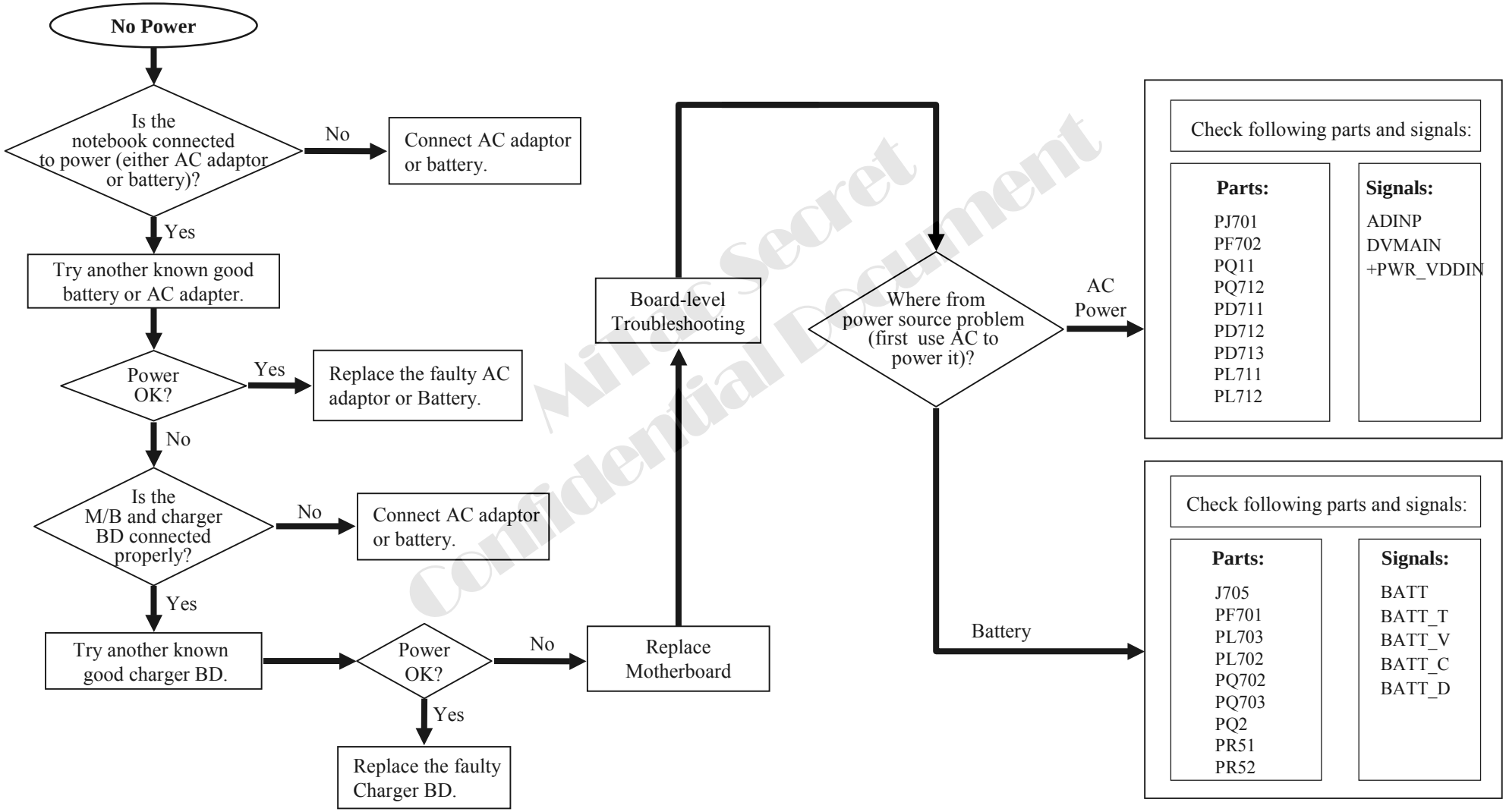
NOTE :

P28 : Page 28 on M/B Board circuit diagram.

PF1 : Through by part PF1.

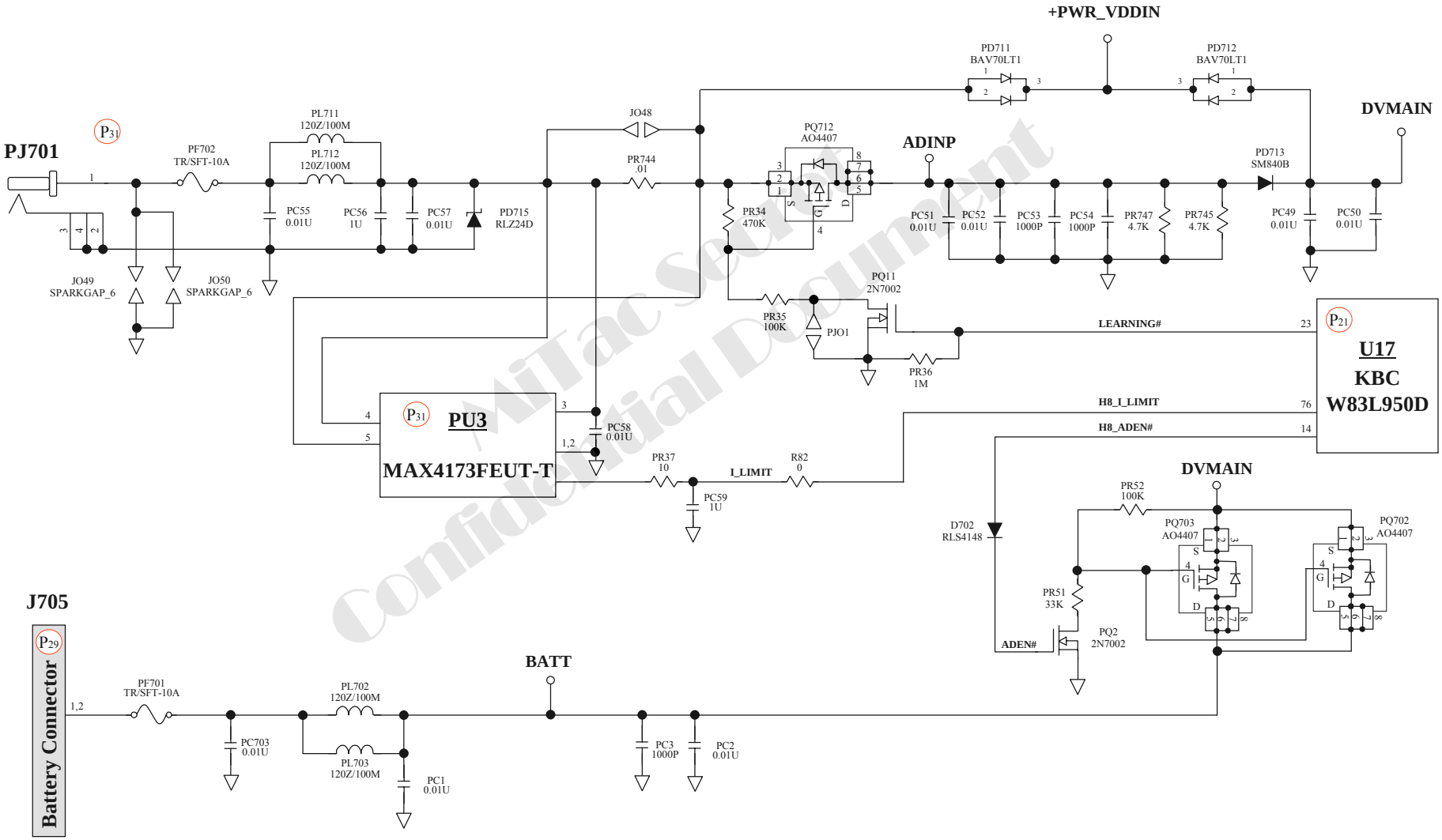
8.1 No Power (2)

When power button is pressed, nothing happens, power indicator does not light up.



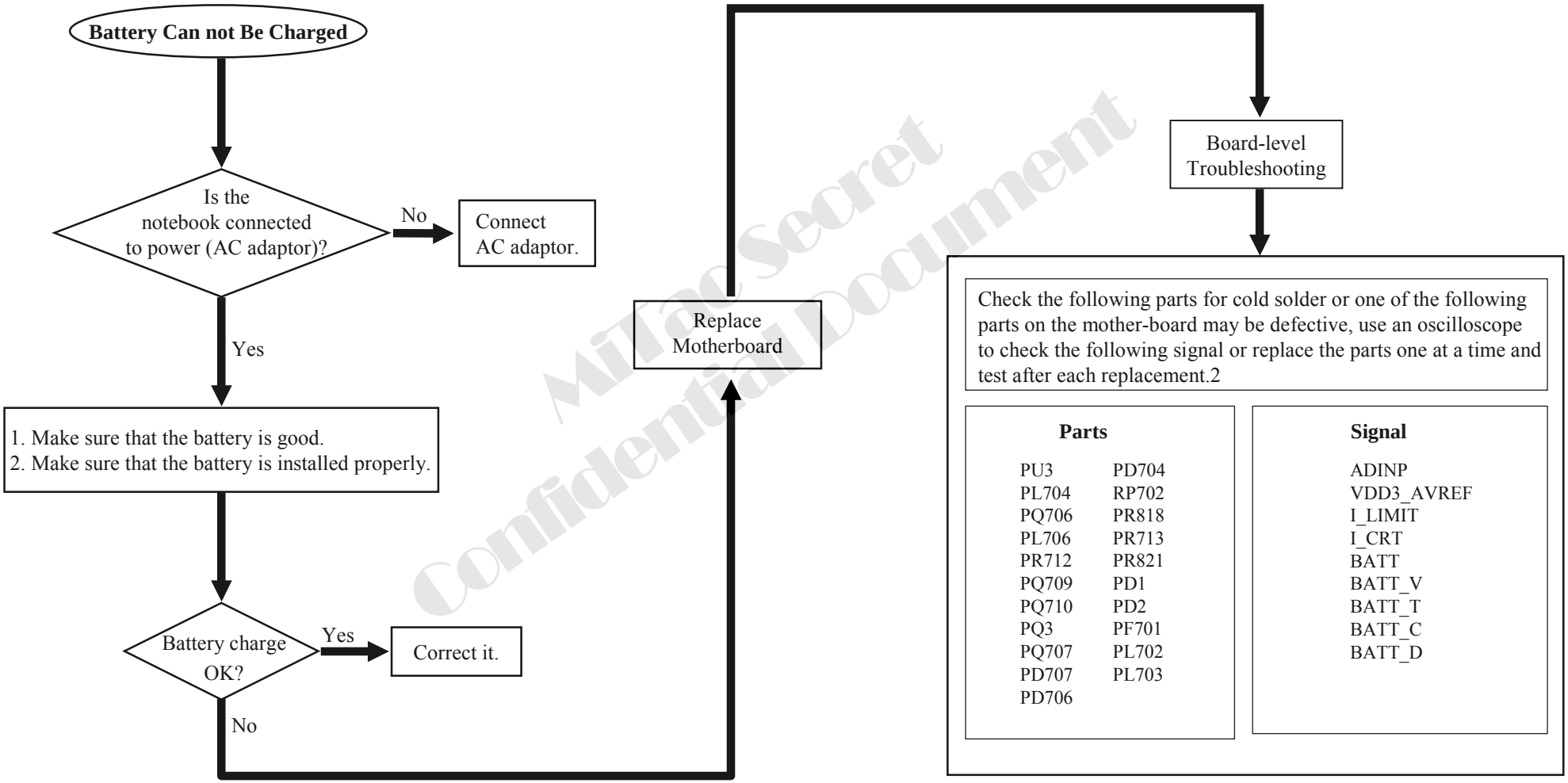
8.1 No Power (3)

When power button is pressed, nothing happens, power indicator does not light up.



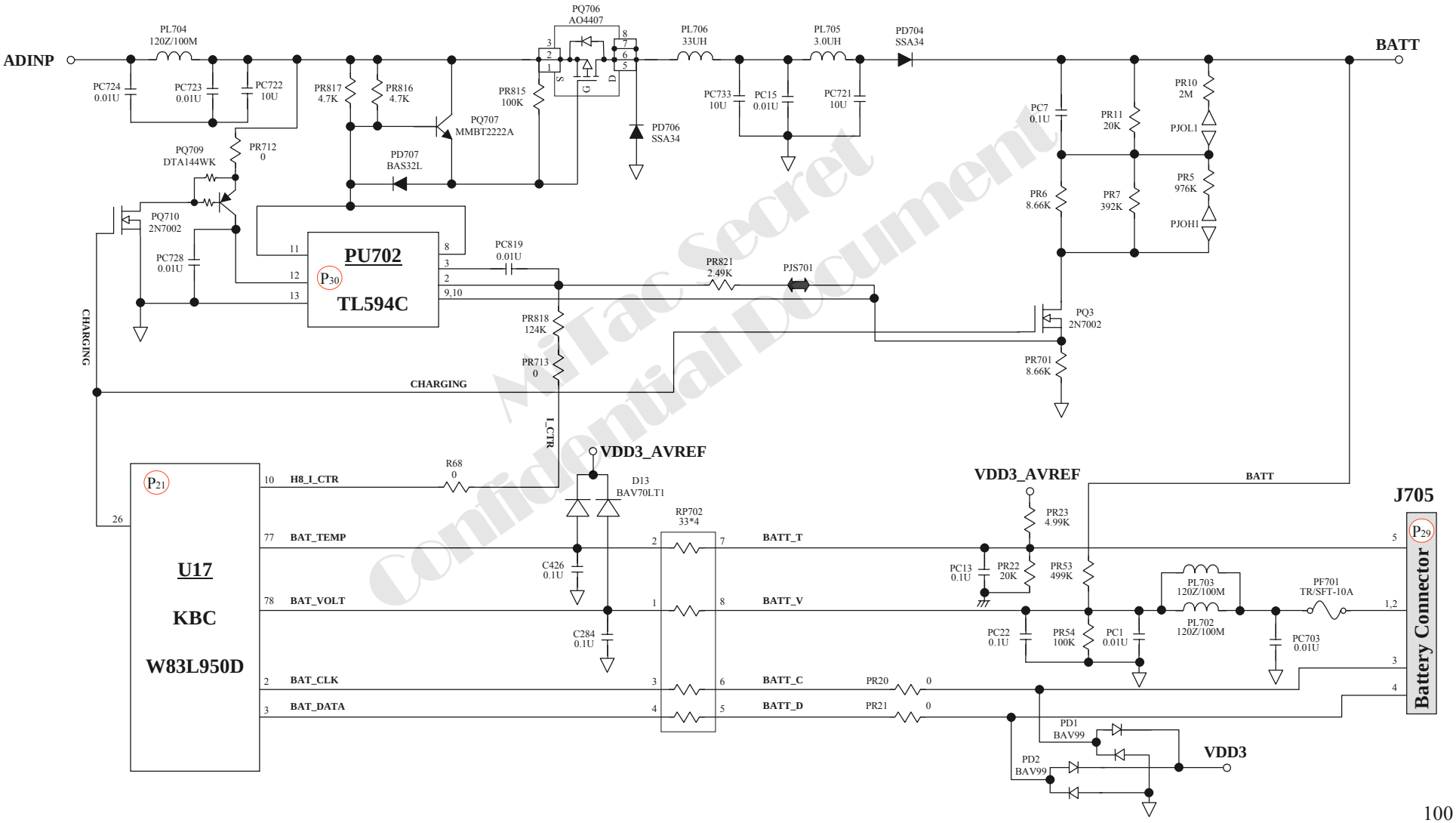
8.2 Battery Can not Be Charged (1)

When the battery is installed but the battery status indicate LED display abnormal.



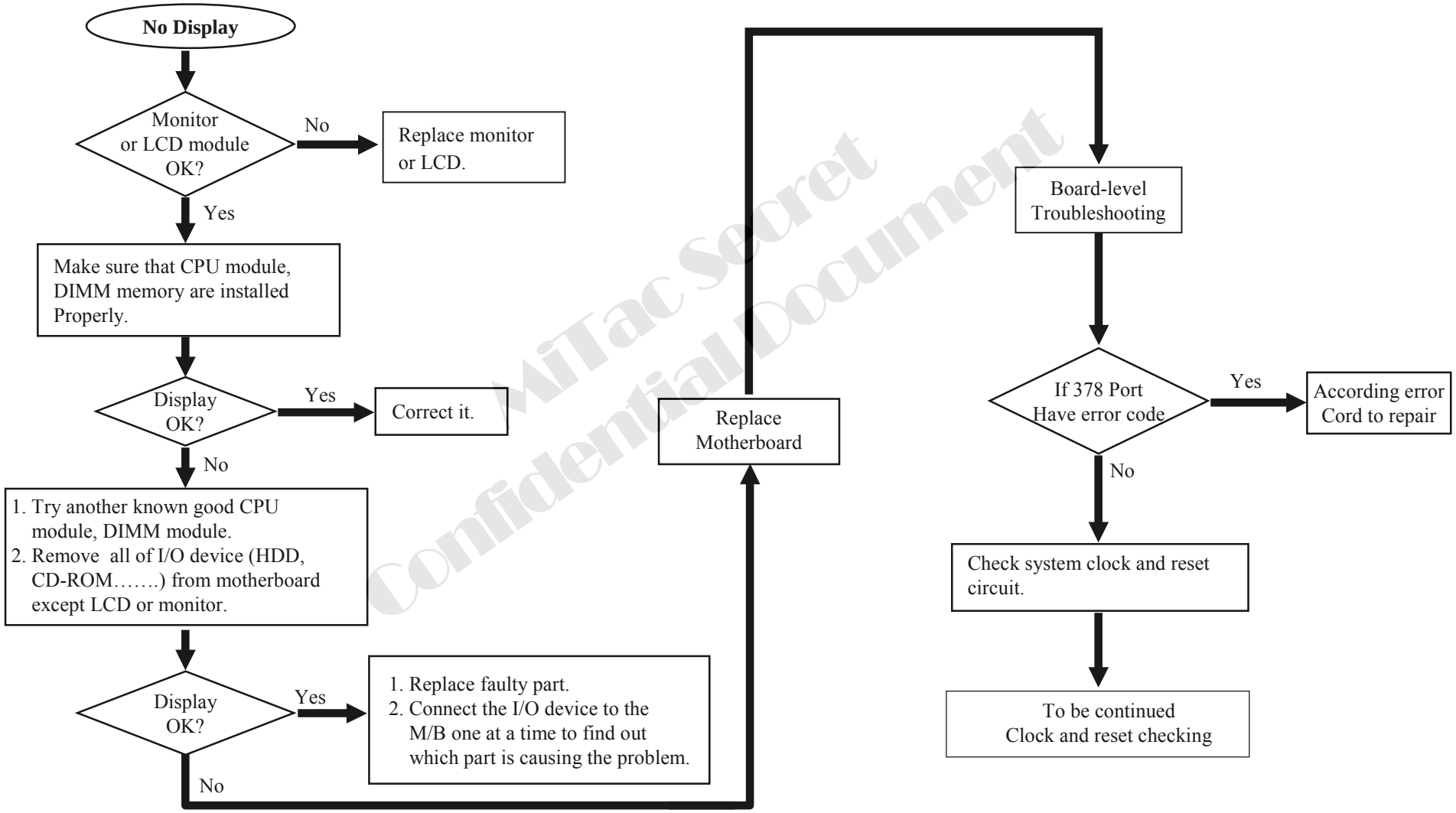
8.2 Battery Can not Be Charged (2)

When the battery is installed but the battery status indicate LED display abnormal.



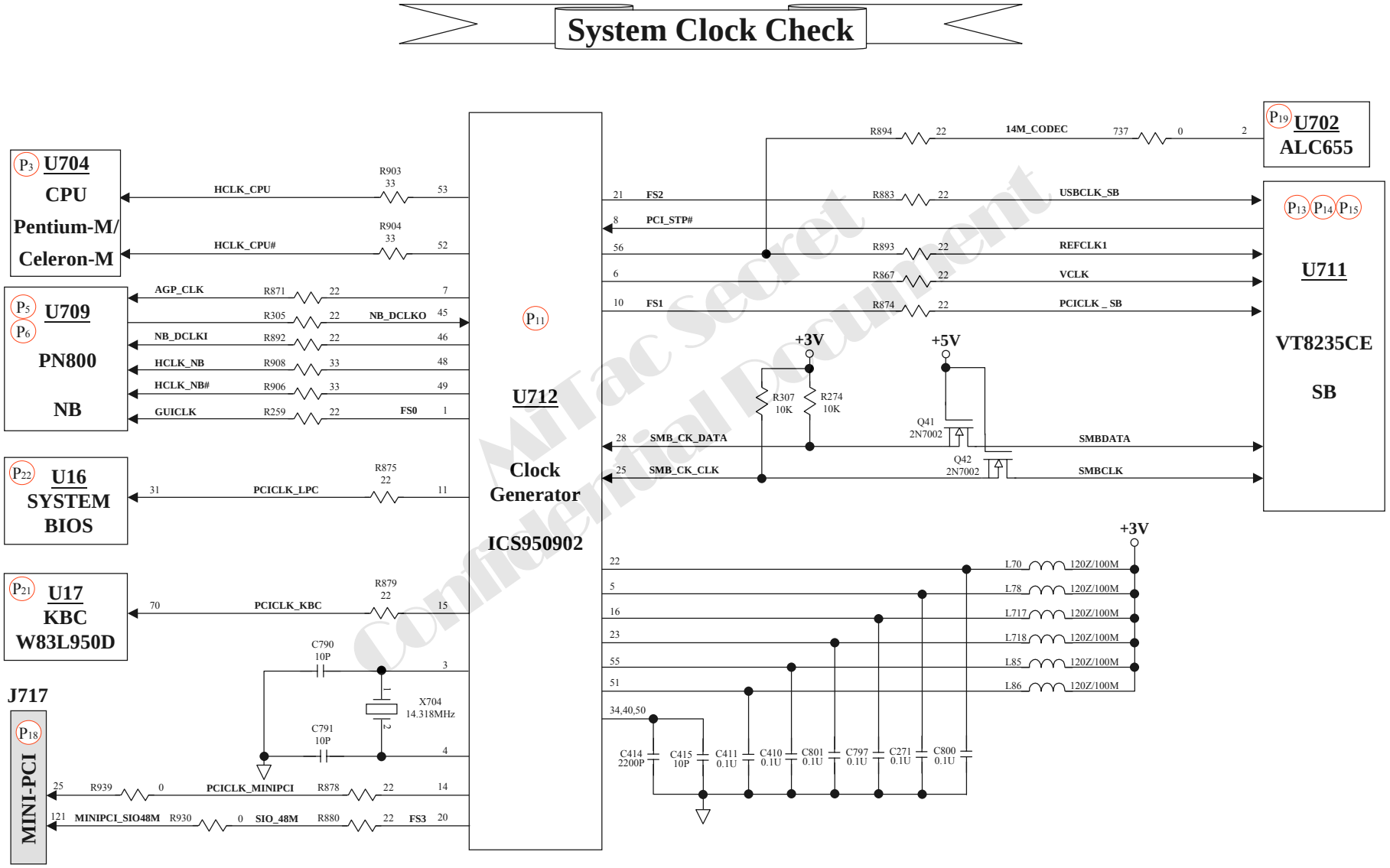
8.3 No Display (1)

There is no display on both LCD and VGA monitor after power on although the LCD and monitor is known-good.



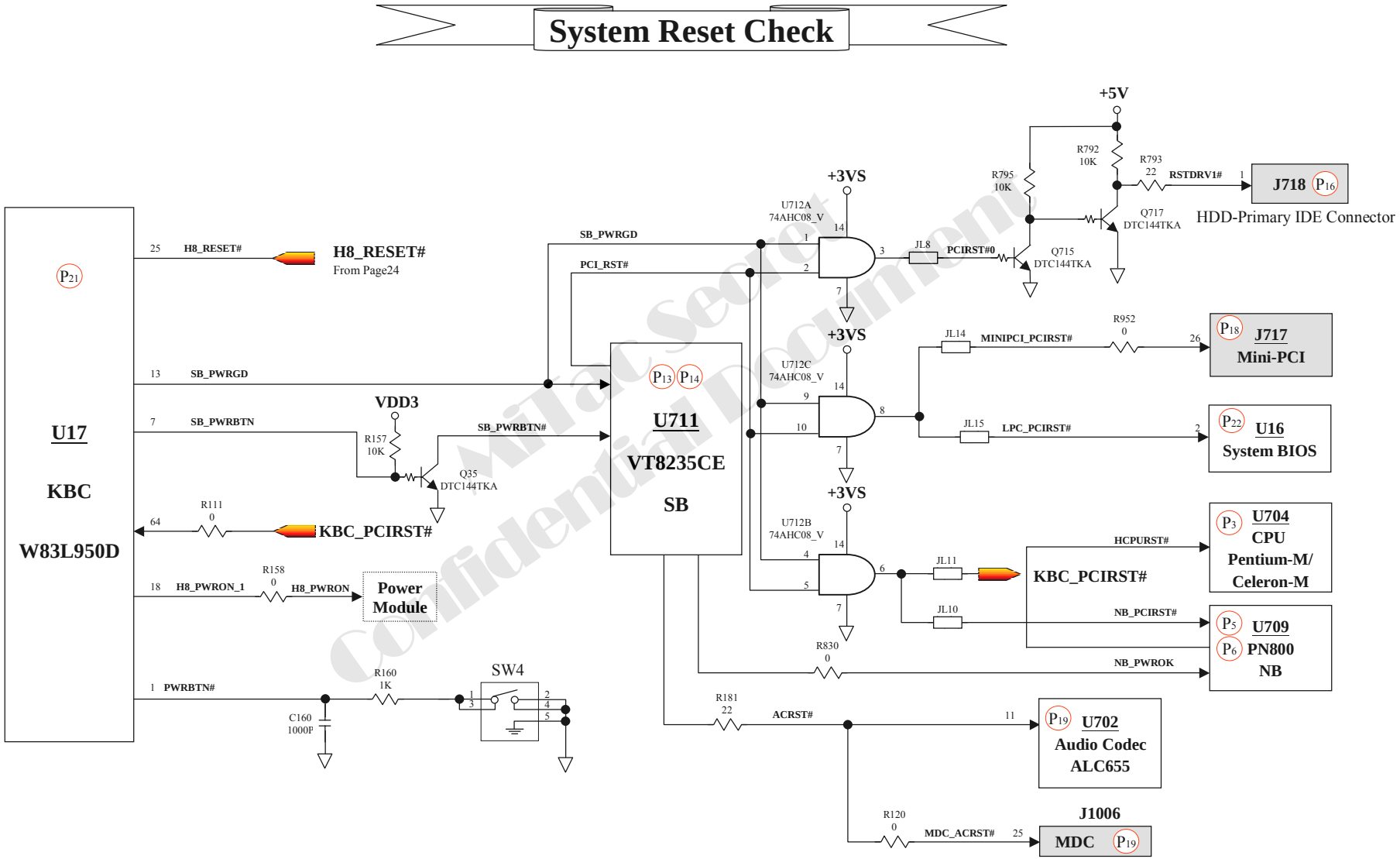
8965 N/B Maintenance

8.3 No Display (2)



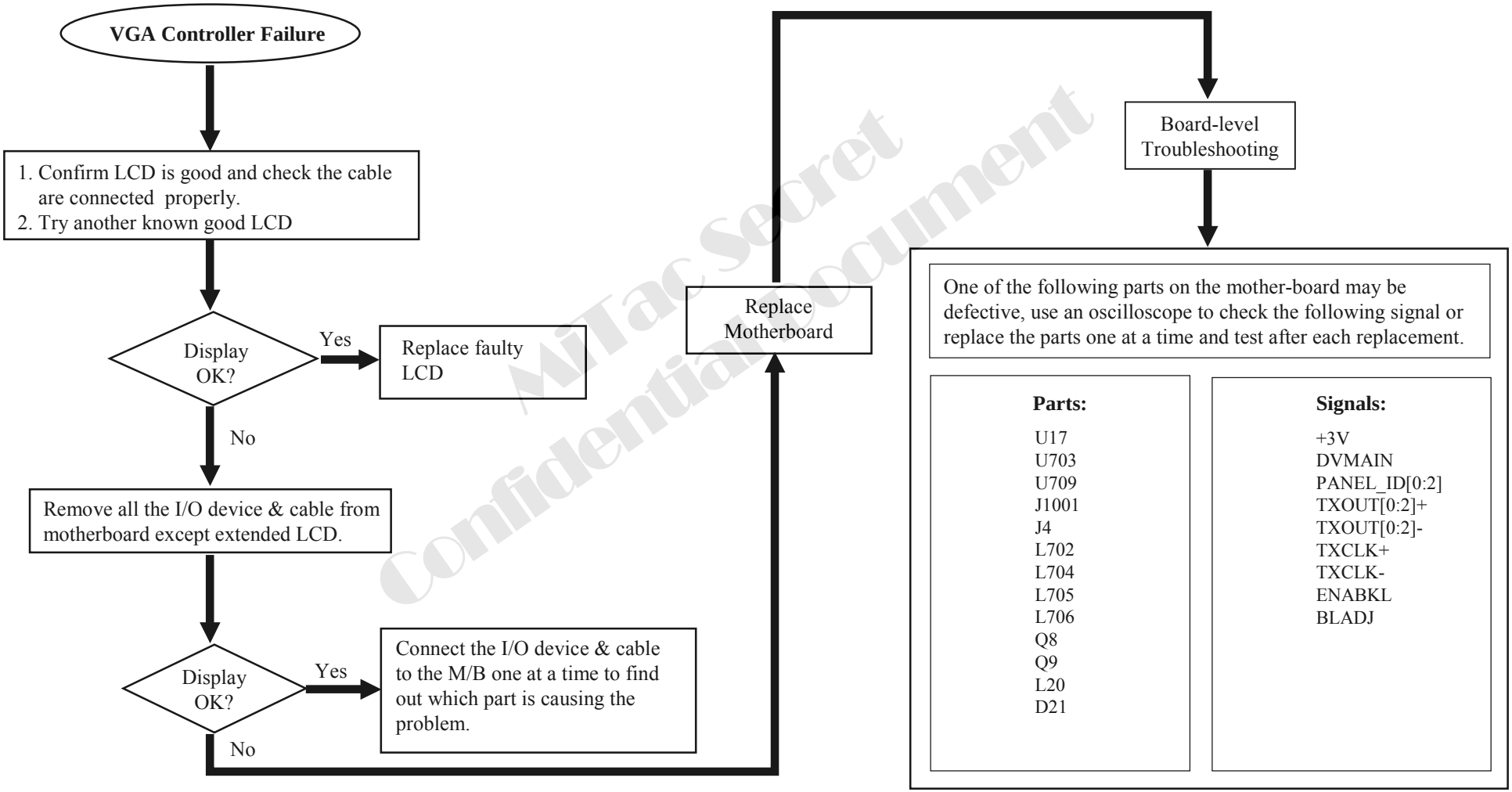
8965 N/B Maintenance

8.3 No Display (3)



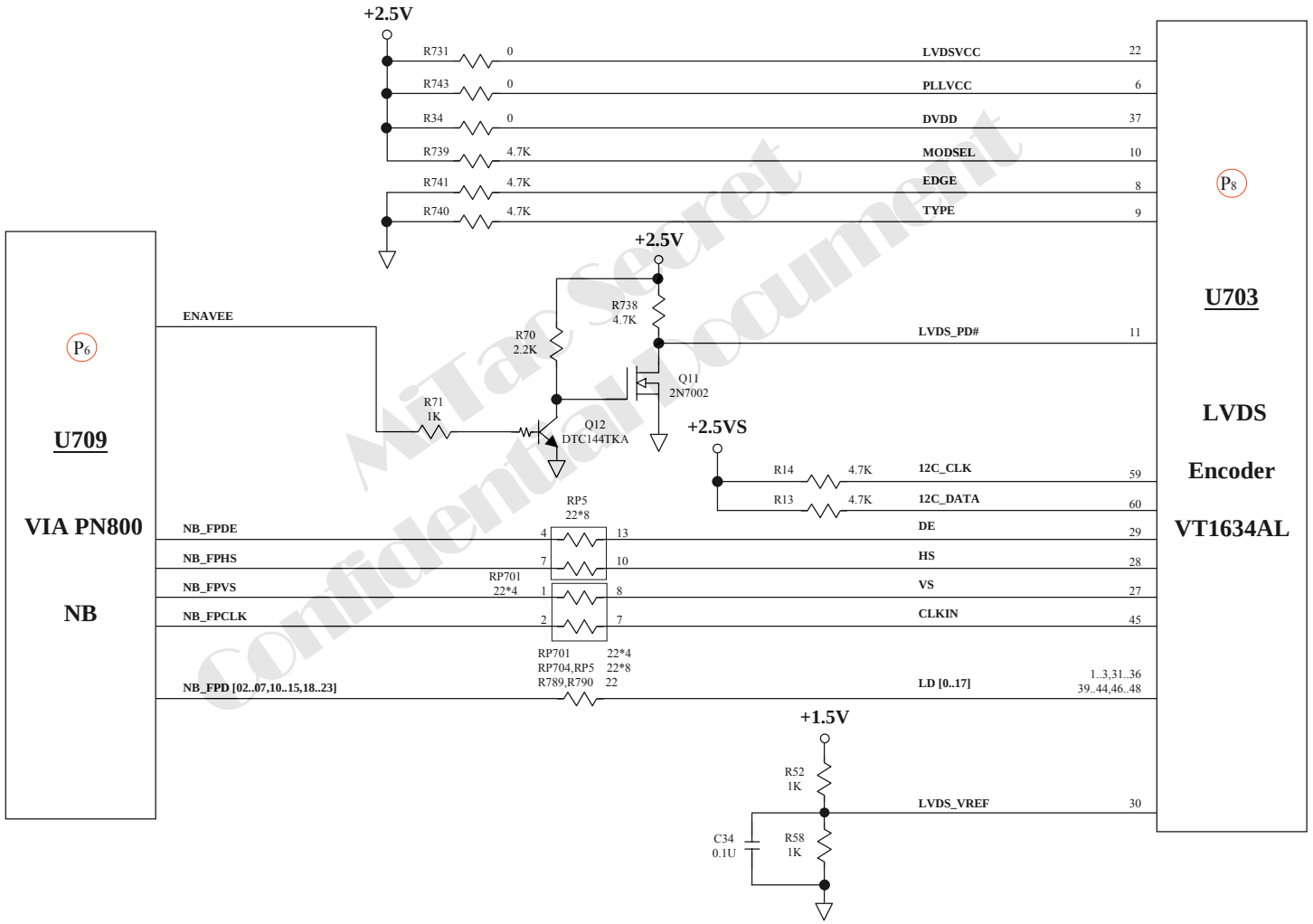
8.4 LCD No Display or Picture Abnormal (1)

There is no display or picture abnormal on LCD or monitor.



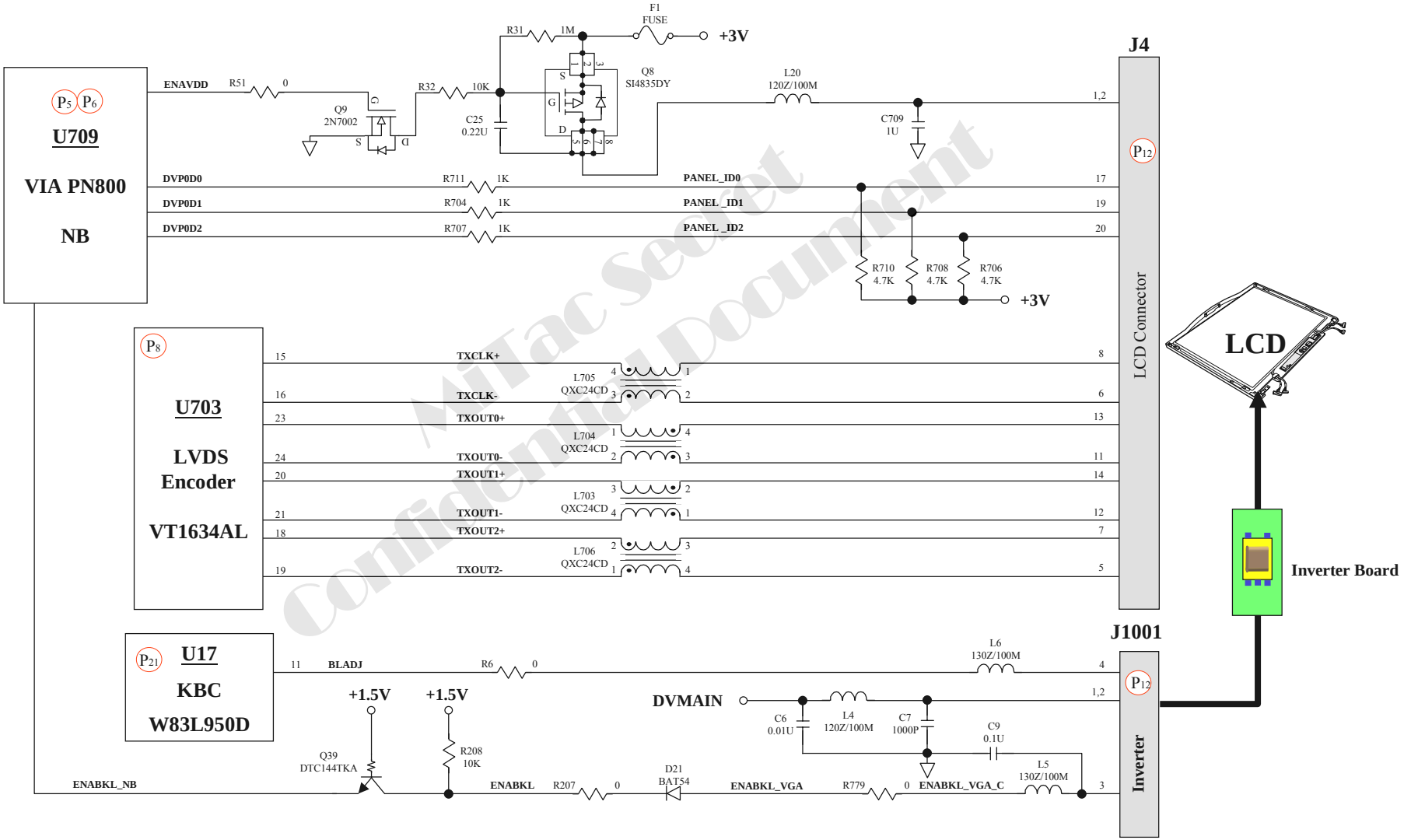
8.4 LCD No Display or Picture Abnormal (2)

There is no display or picture abnormal on LCD or monitor.



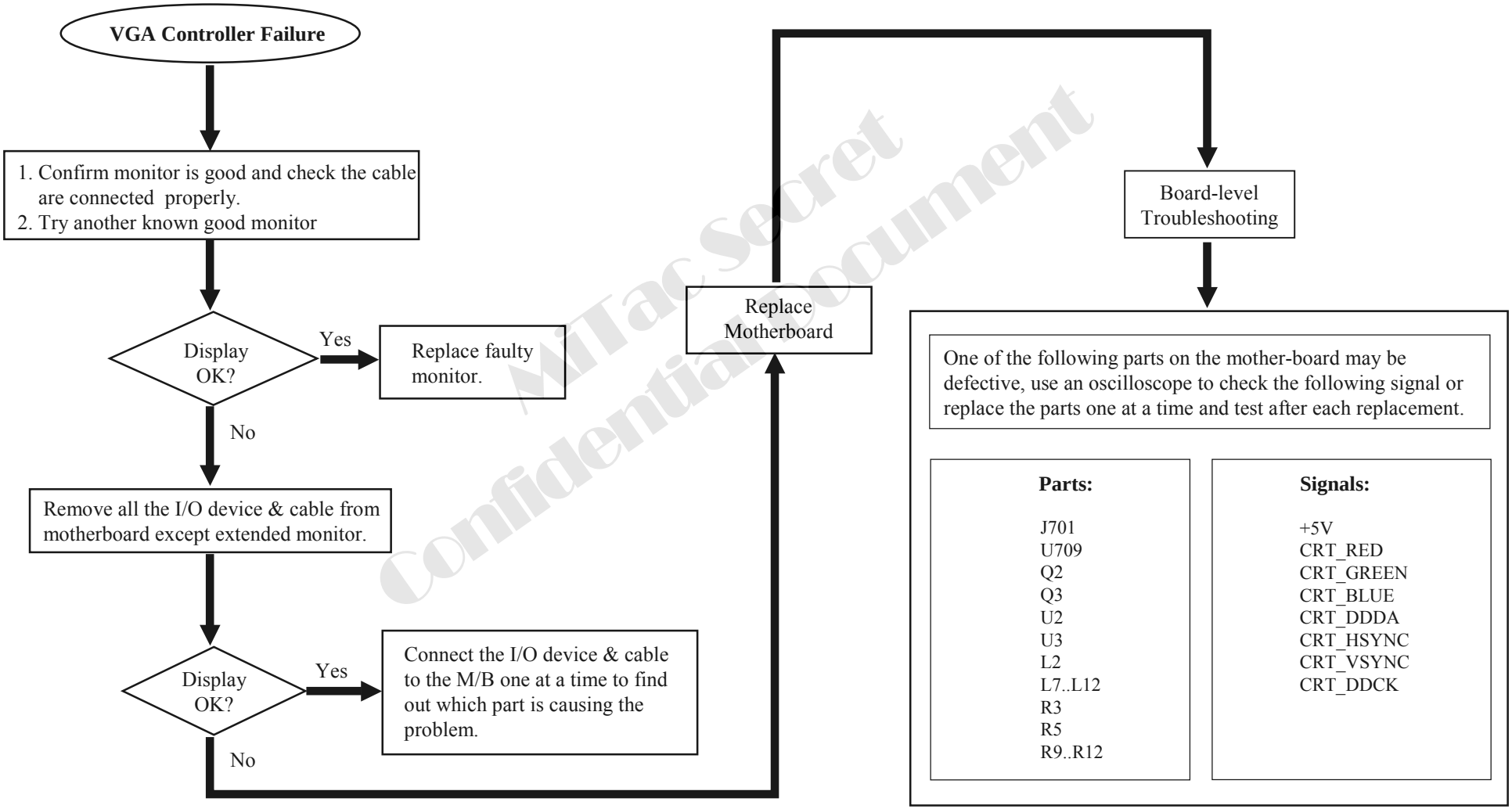
8.4 LCD No Display or Picture Abnormal (3)

There is no display or picture abnormal on LCD or monitor.



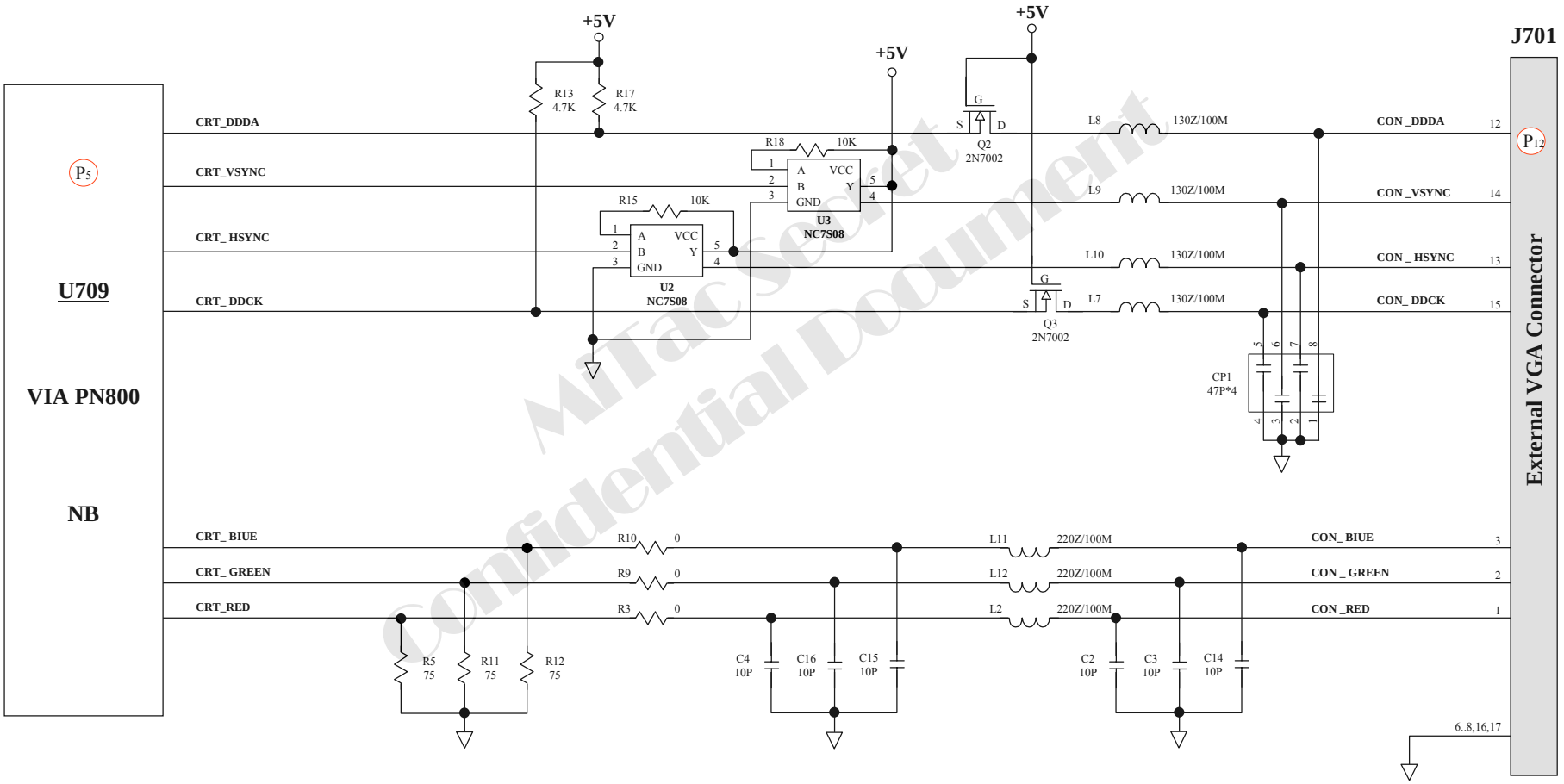
8.5 External Monitor No Display or Color Abnormal (1)

There is no display or picture abnormal on monitor.



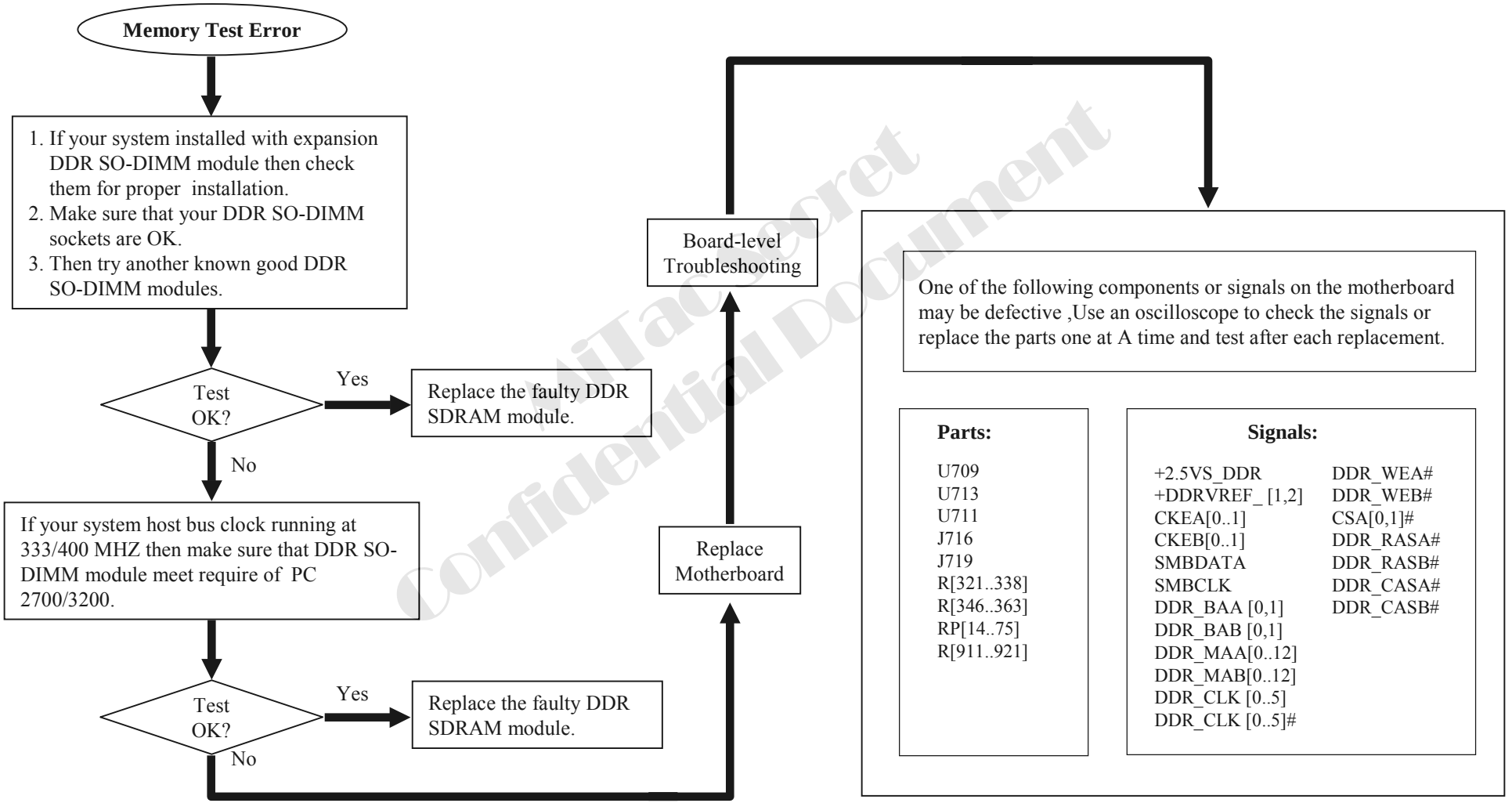
8.5 External Monitor No Display or Color Abnormal (2)

There is no display or picture abnormal on monitor.



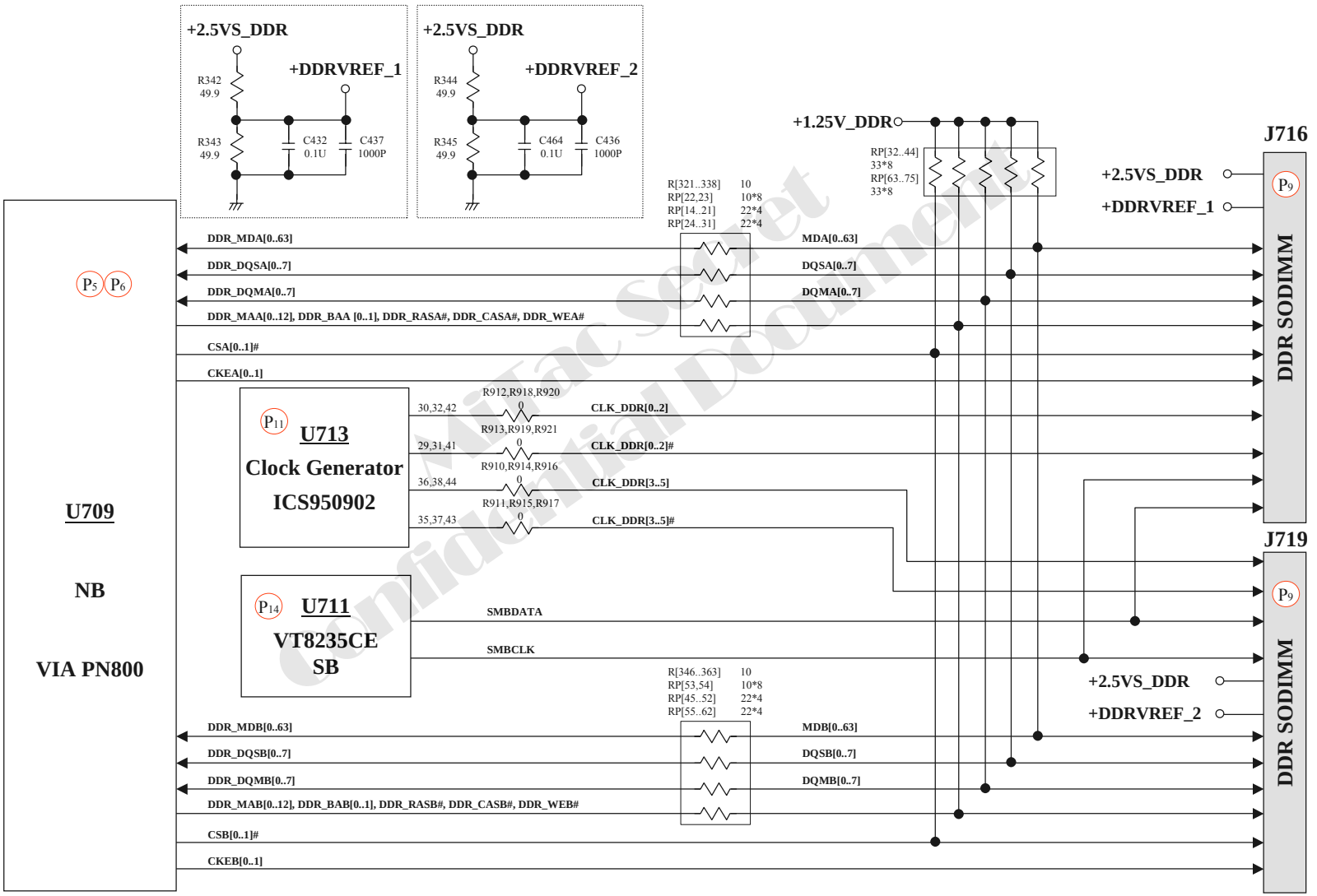
8.6 Memory Test Error (1)

Extend DDRAM is test error or system hangs up.



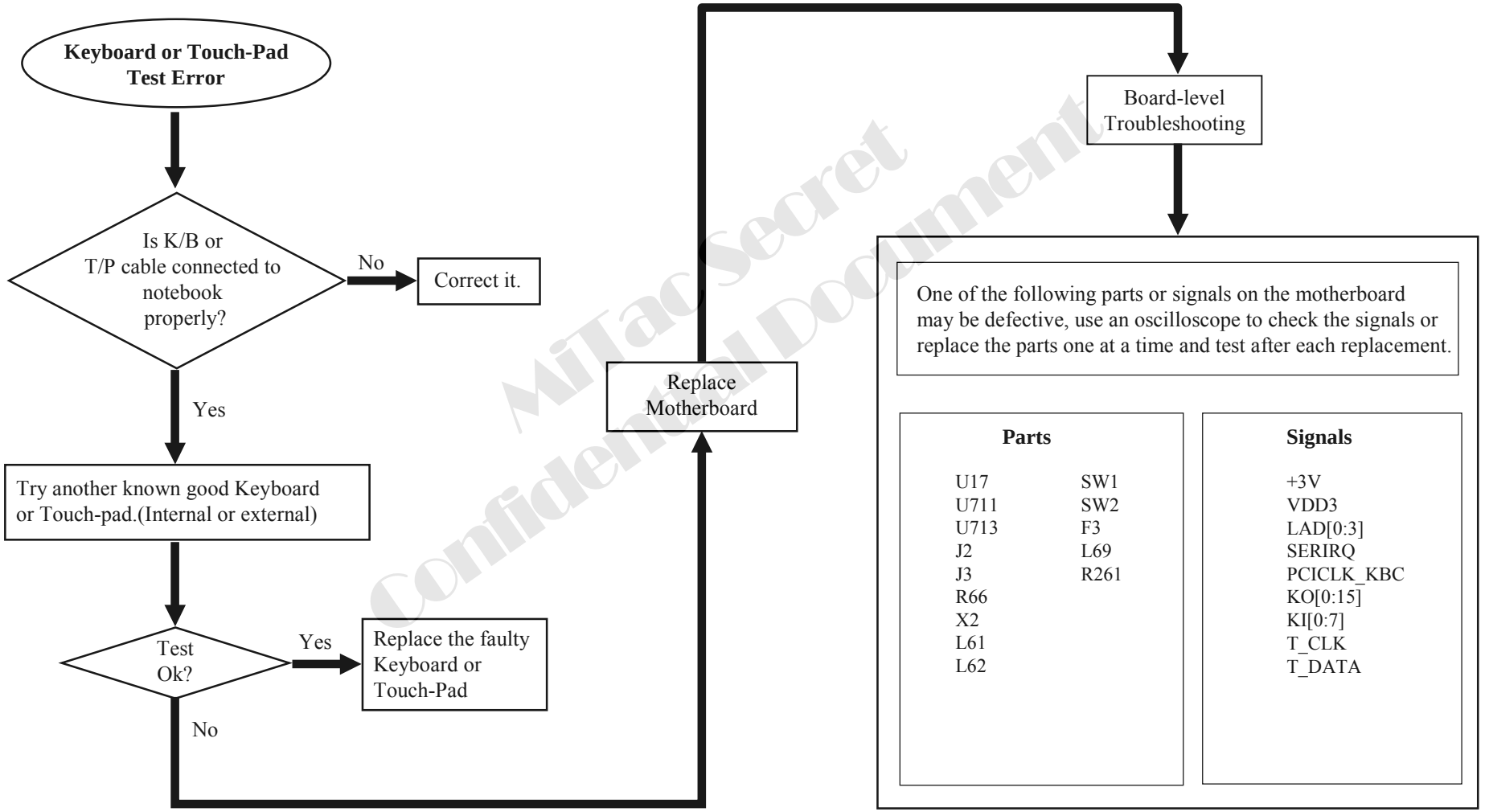
8.6 Memory Test Error (2)

Extend DDRAM is test error or system hangs up.



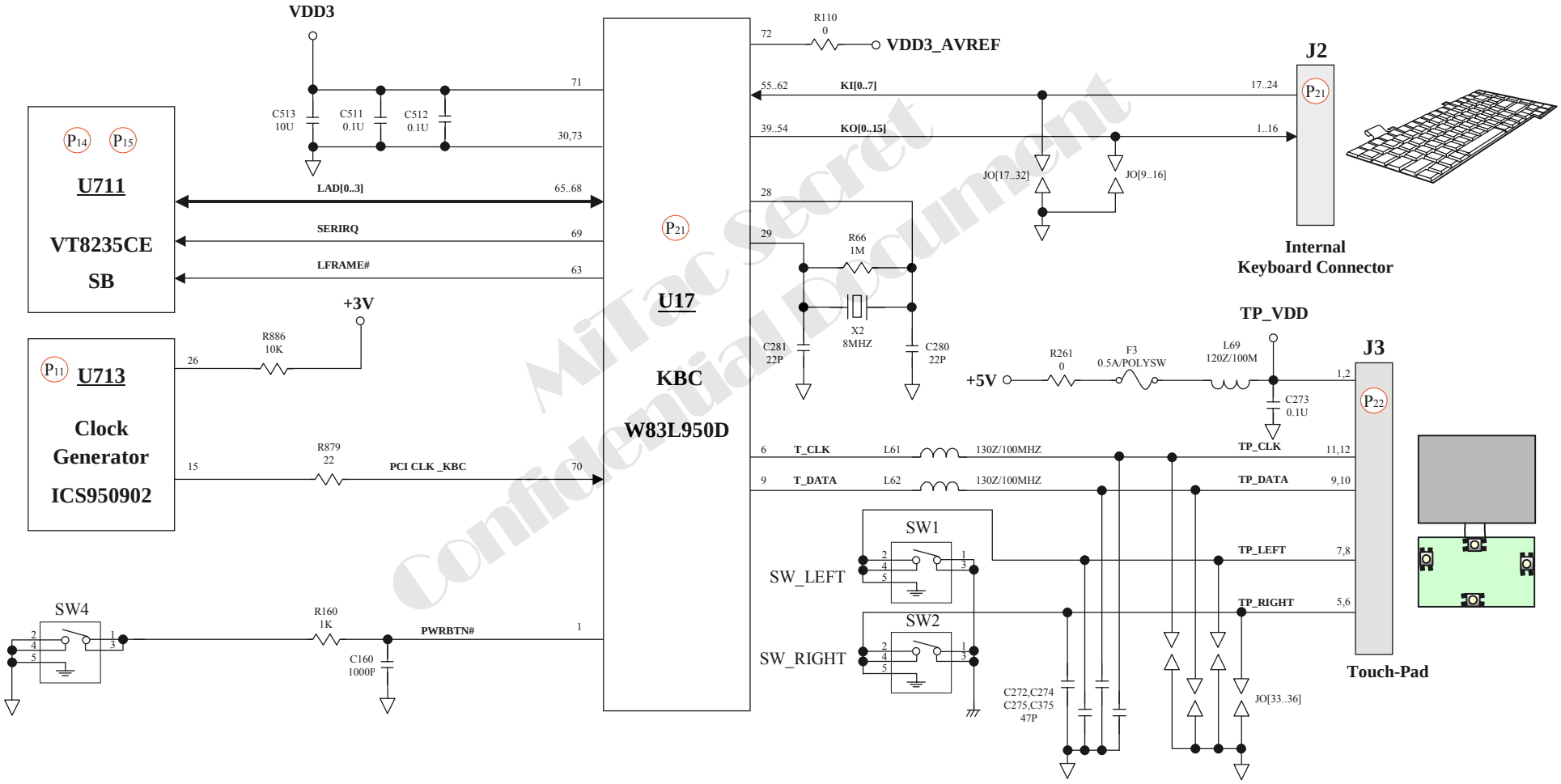
8.7 Keyboard (K/B) Touch-Pad (T/P) Test Error (1)

Error message of keyboard or touch-pad test error is shown or any key does not work.



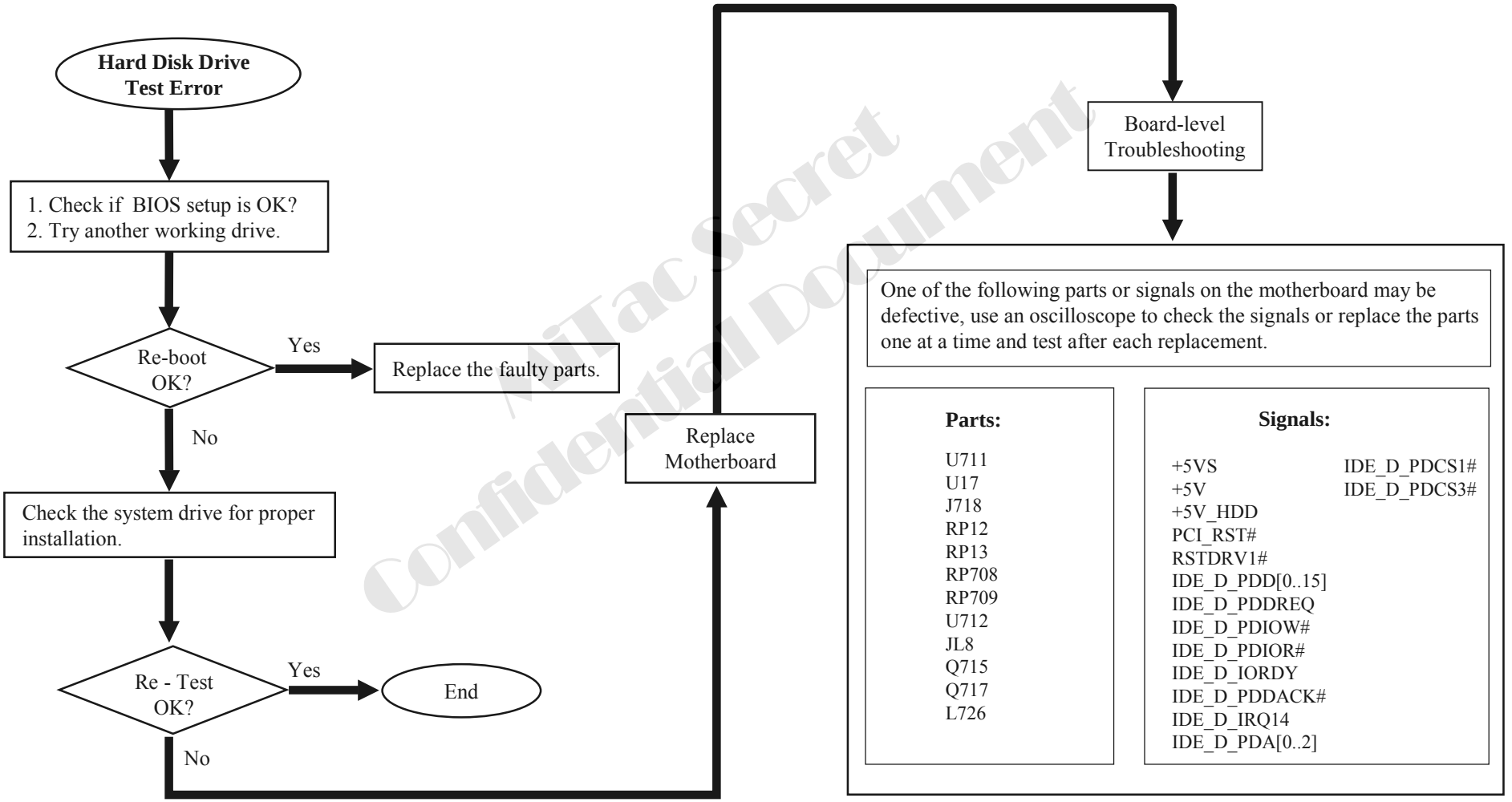
8.7 Keyboard (K/B) Touch-Pad (T/P) Test Error (2)

Error message of keyboard or touch-pad test error is shown or any key does not work.



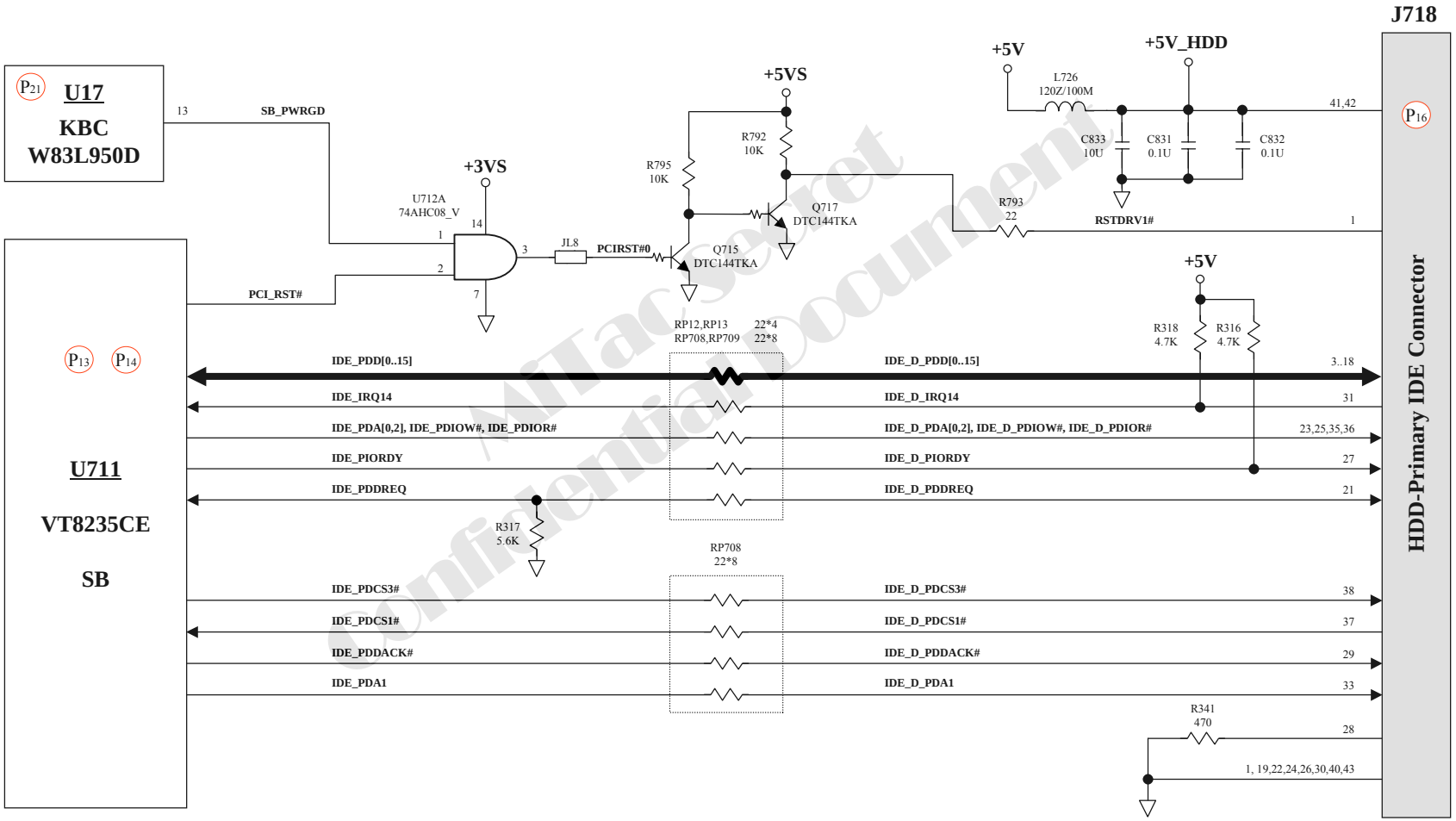
8.8 Hard Disk Drive Test Error (1)

Either an error message is shown, or the driver motor continues spinning, while reading data is from or writing data is to hard drive.



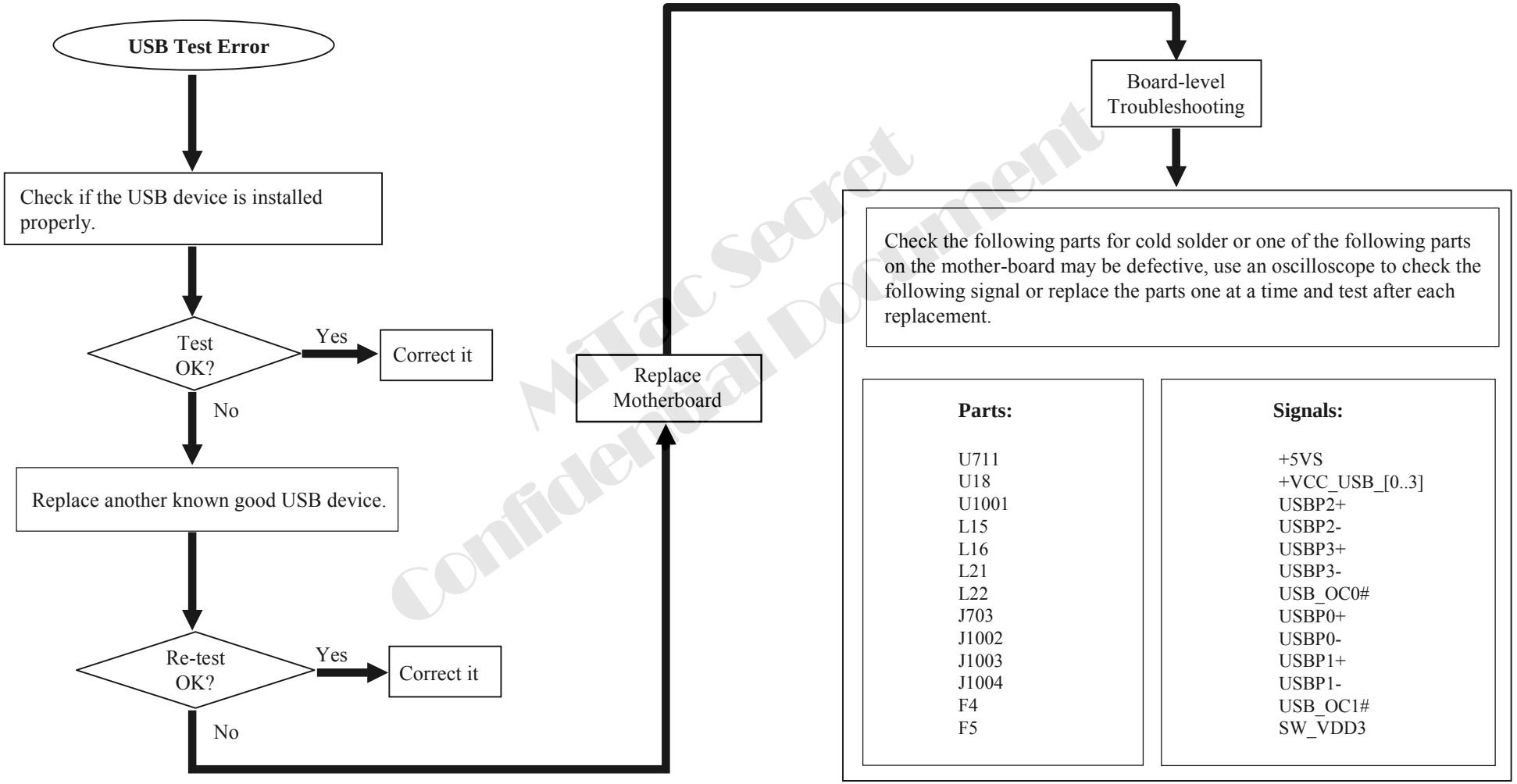
8.8 Hard Disk Drive Test Error (2)

Either an error message is shown, or the driver motor continues spinning, while reading data is from or writing data is to hard drive.



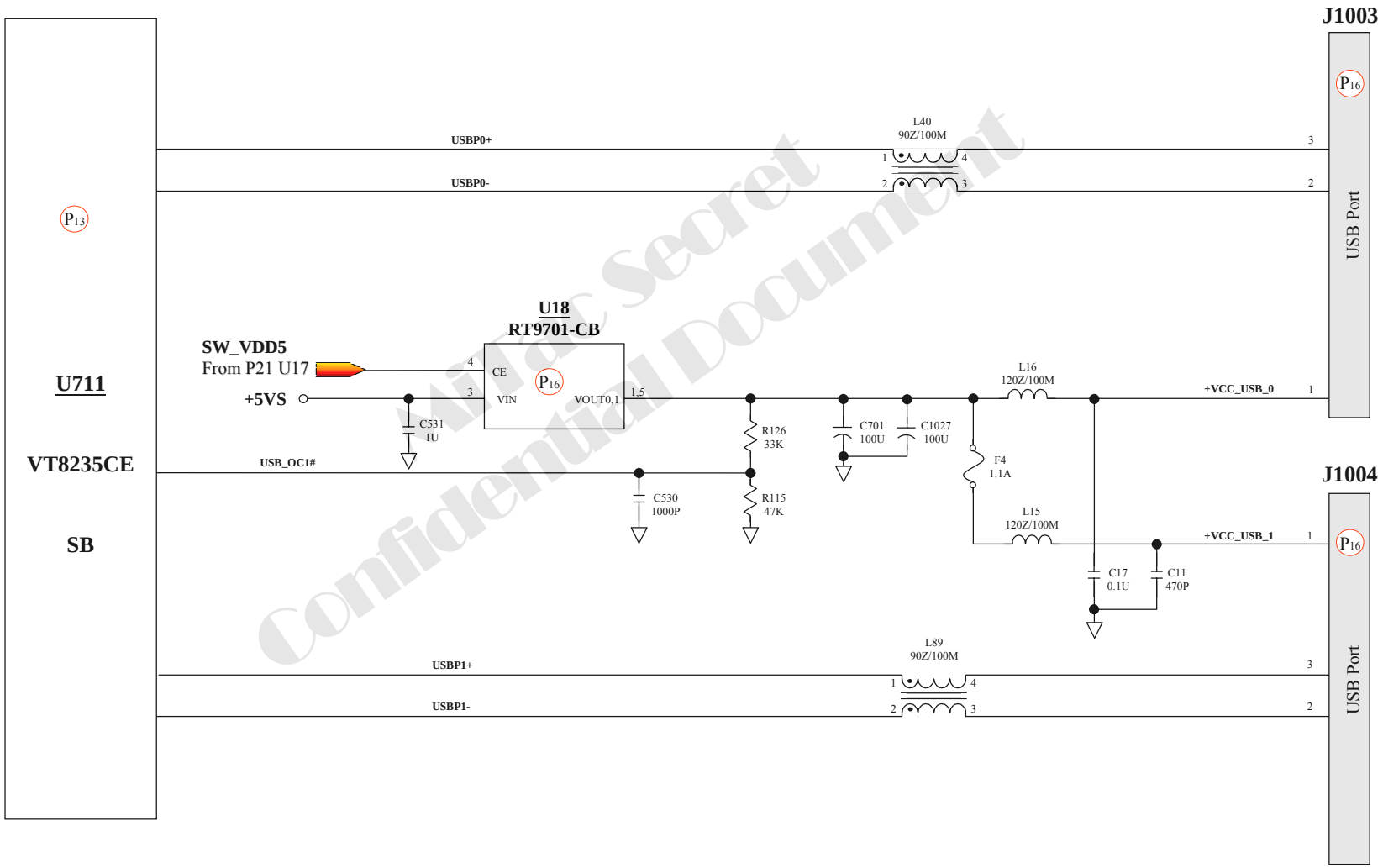
8.9 USB Port Test Error (1)

An error occurs when a USB I/O device is installed.



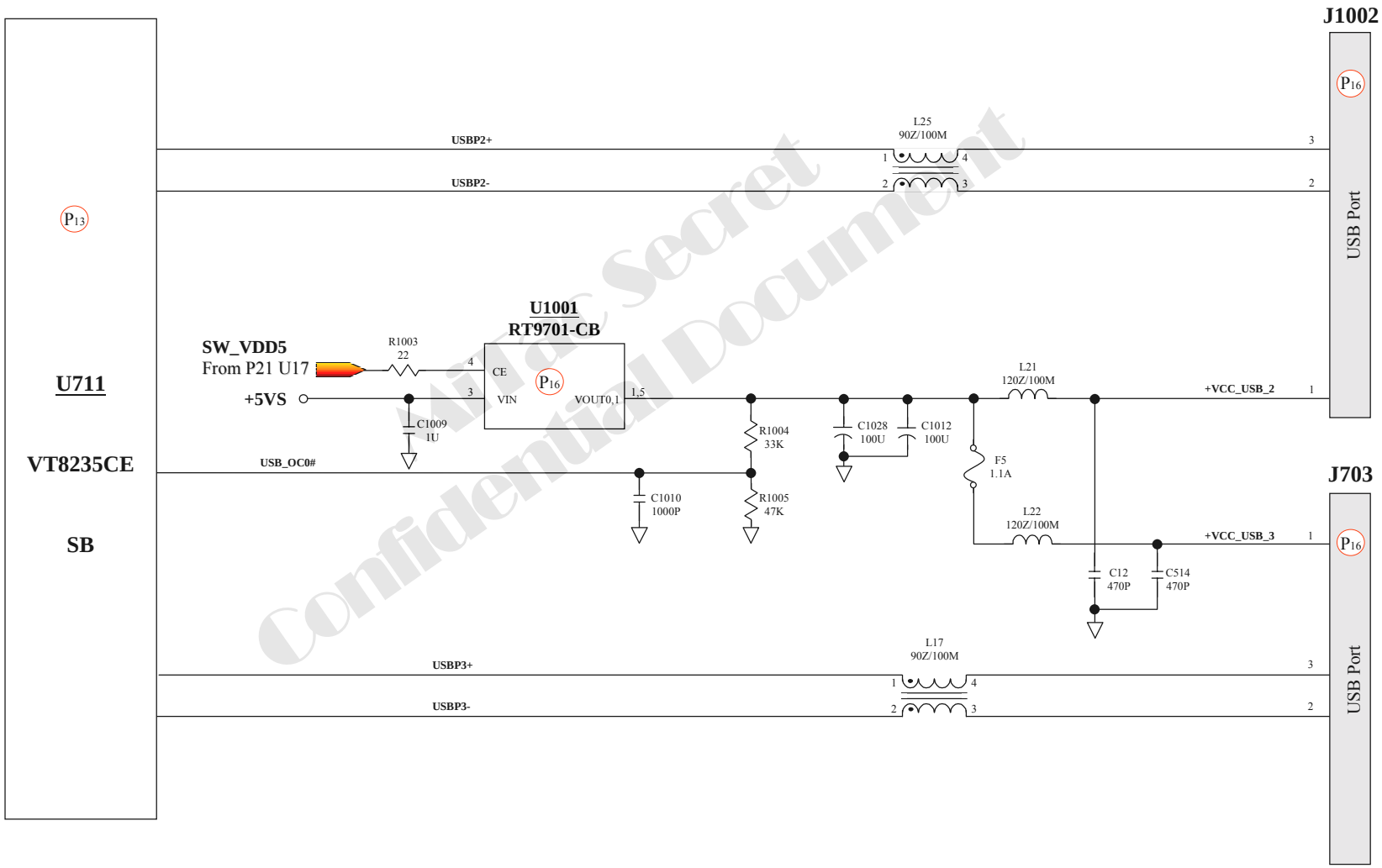
8.9 USB Port Test Error (2)

An error occurs when a USB I/O device is installed.



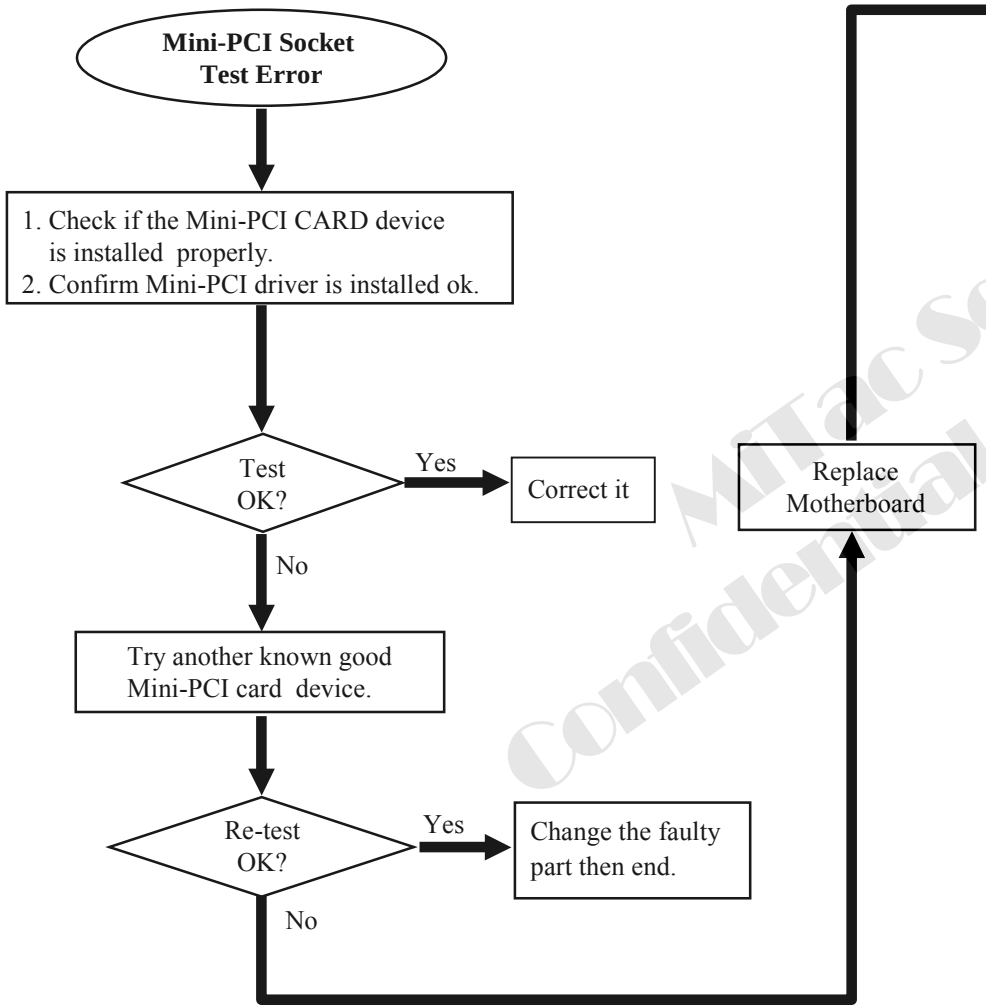
8.9 USB Port Test Error (3)

An error occurs when a USB I/O device is installed.



8.10 Mini-PCI Socket Test Error (1)

An error occurs when a PC card device is installed.



Board-level Troubleshooting

Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:

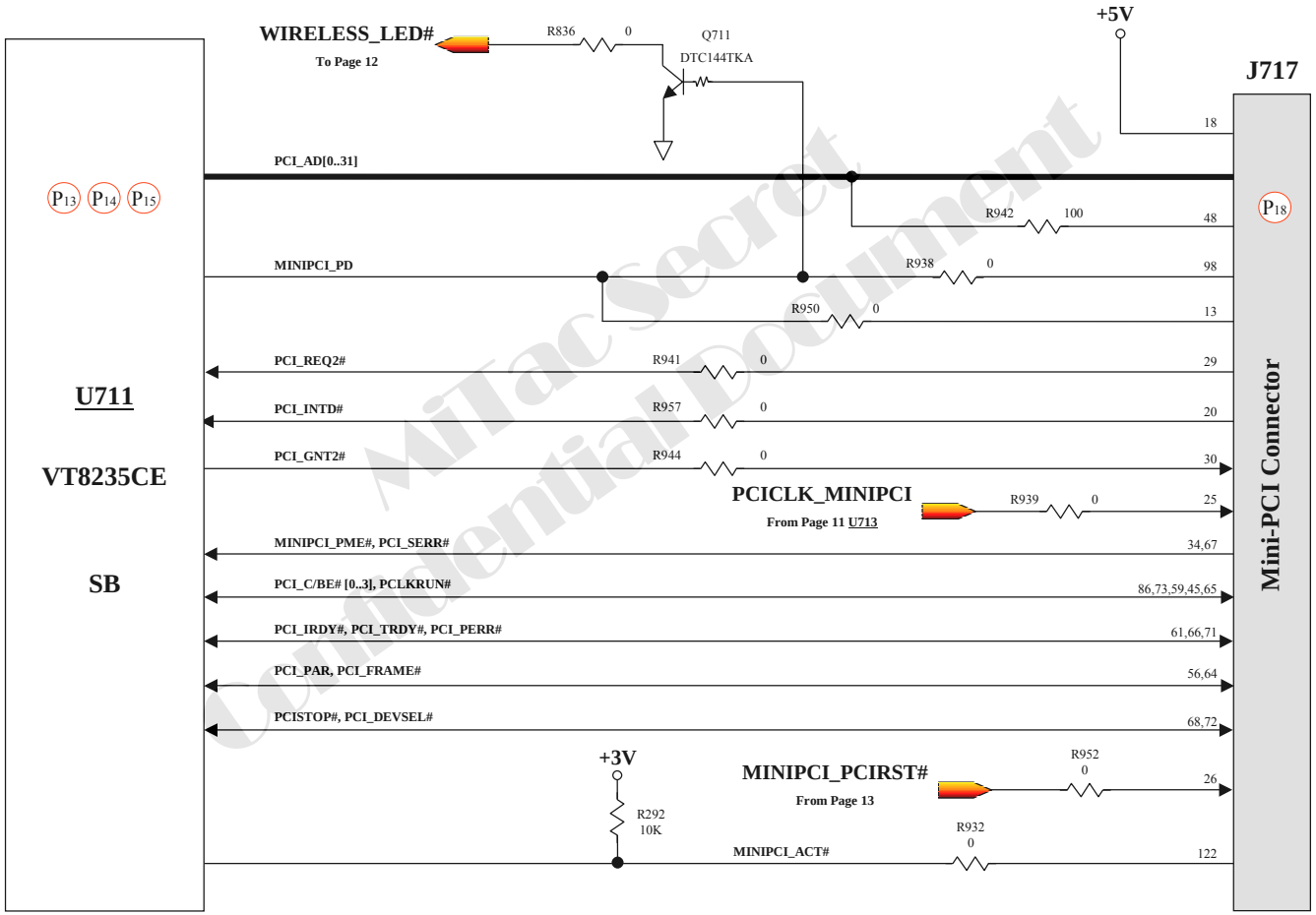
U711
J717
Q711
R944
R952
R957
R942
R938
R932
R941
R939

Signals

+5V	PCI_SERR#
+3V	PCI_PERR#
PCI_AD[0..31]	PCI_INTD#
PCI_C/BE#[0..3]	MINIPCI_PCIRST#
MINIPCI_PD	PCI_PAR
PCI_GNT2#	PCI_FRAME#
PCICLK_MINIPCI	PCI_TRDY#
PCI_REQ2#	PCI_STOP#
PCI_IRDY#	PCI_DEVSEL#
PCLKRUN#	

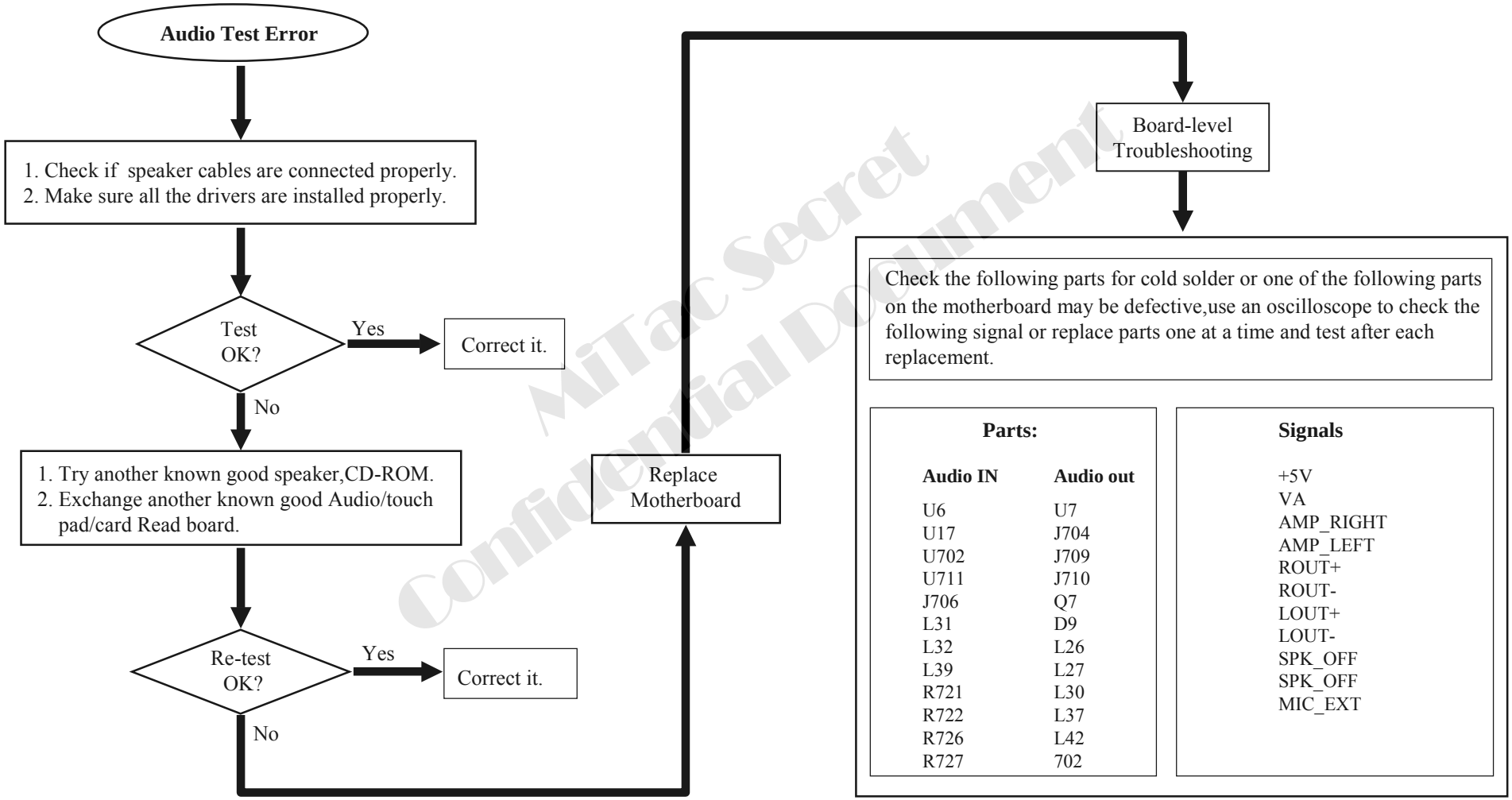
8.10 Mini-PCI Socket Test Error (2)

An error occurs when a PC card device is installed.



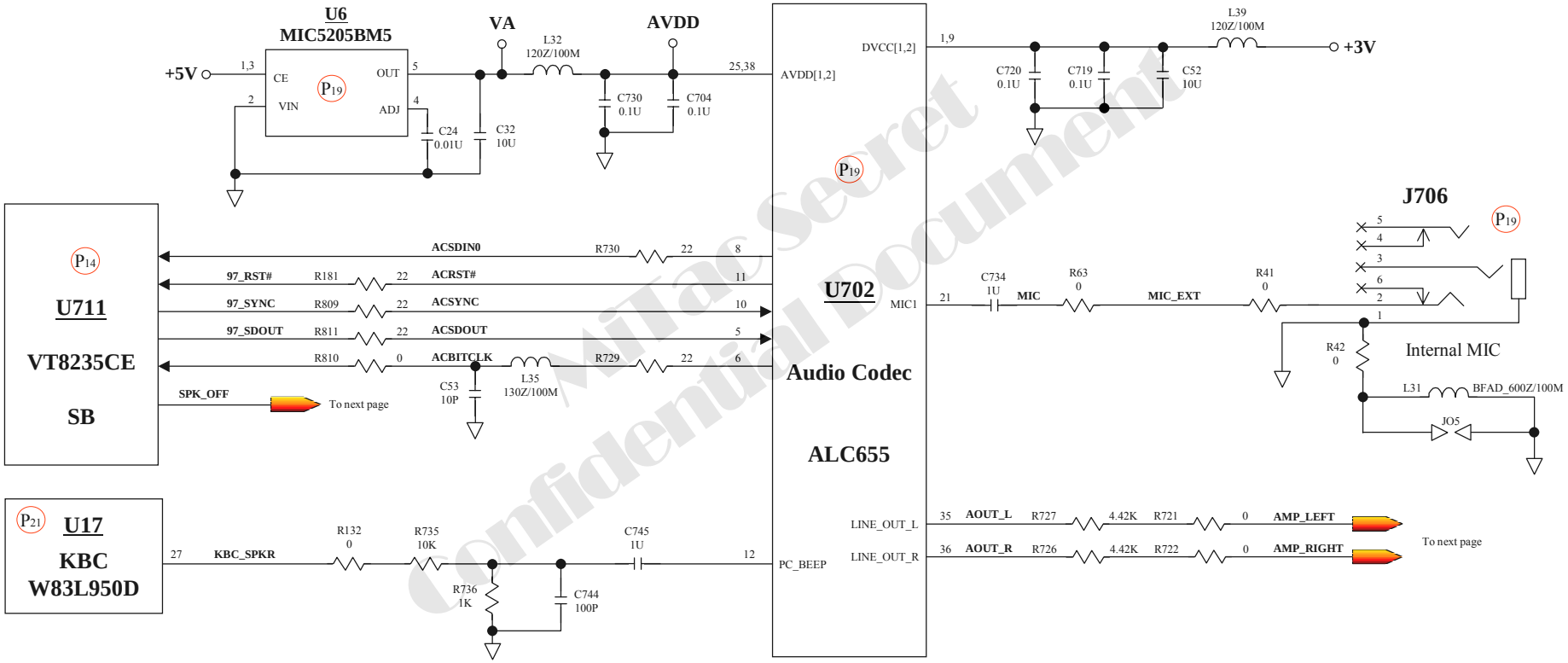
8.11 Audio Test Error (1)

No sound from speaker after audio driver is installed.



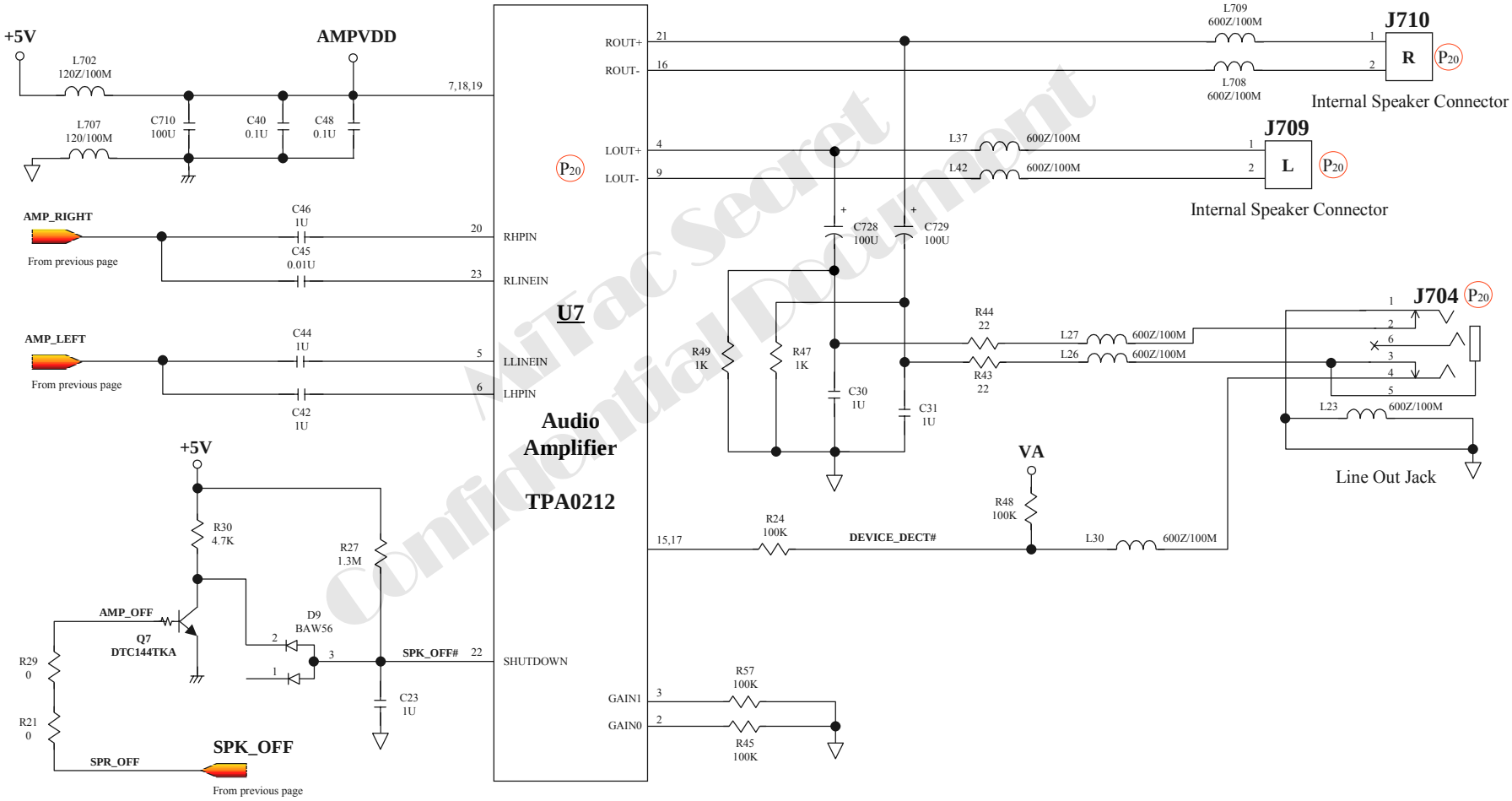
8.11 Audio Test Error (2) – Audio IN

No sound from speaker after audio driver is installed.



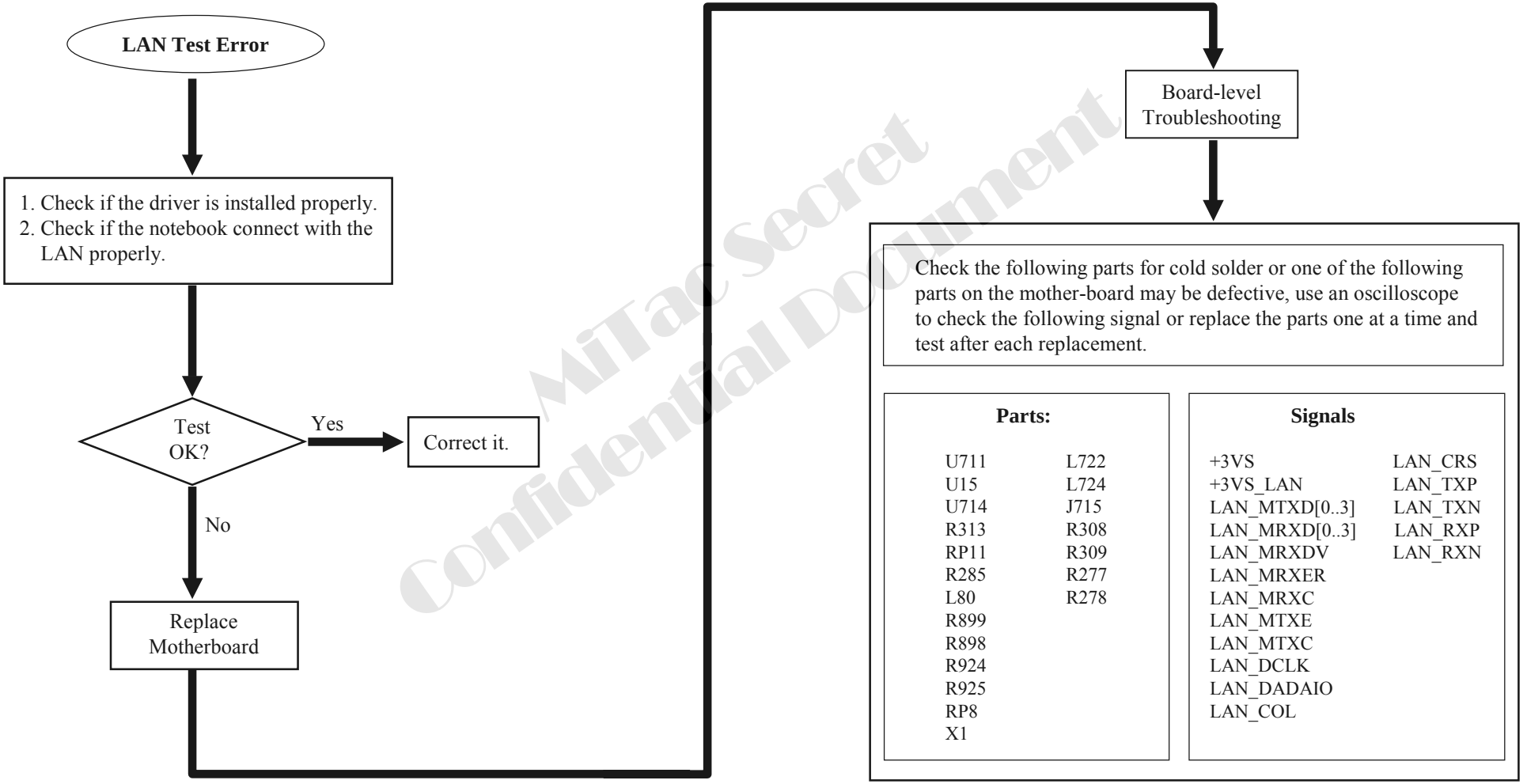
8.11 Audio Test Error (3) – Audio OUT

No sound from speaker after audio driver is installed.



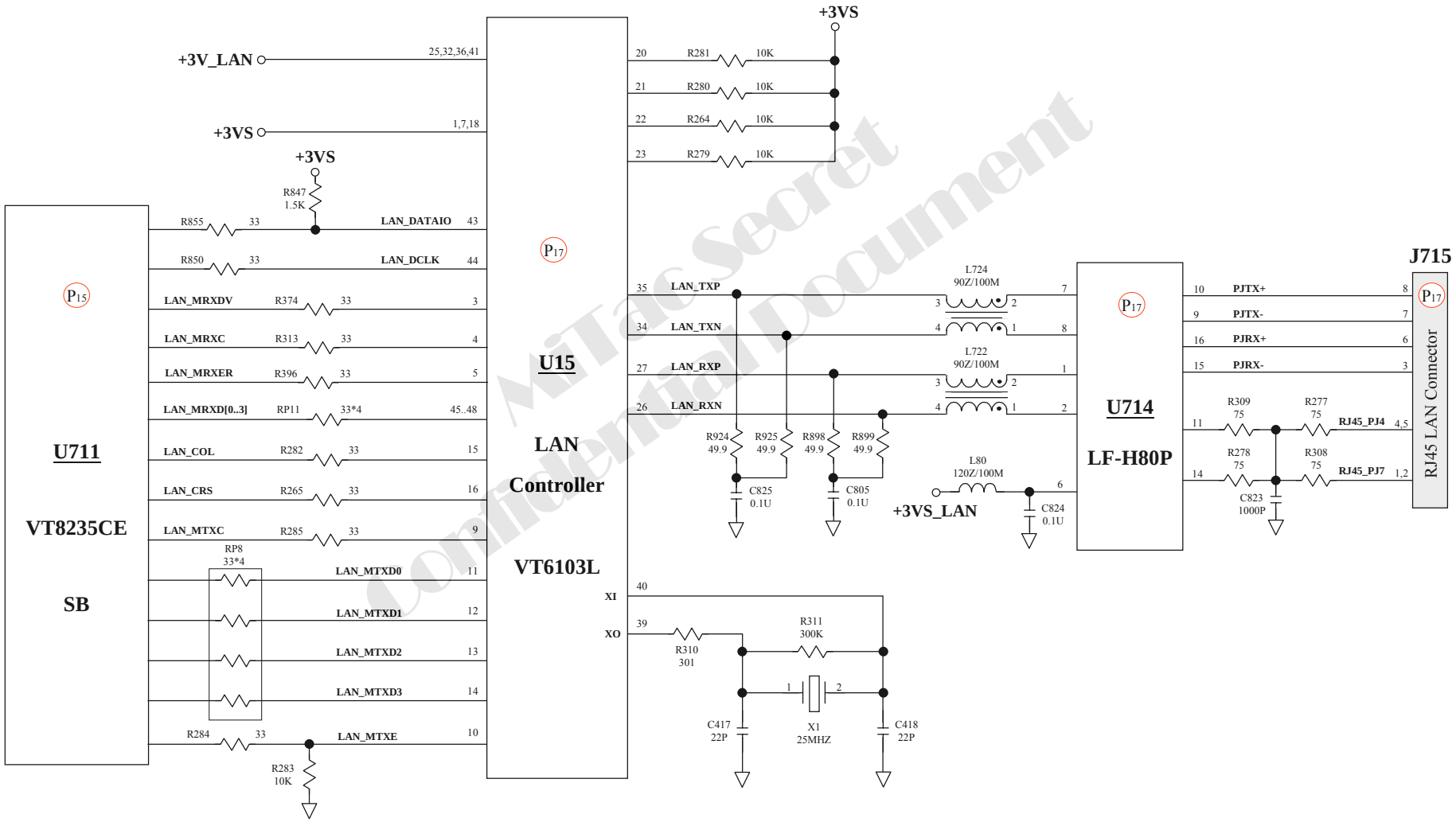
8.12 LAN Test Error (1)

An error occurs when a LAN device is installed.



8.12 LAN Test Error (2)

An error occurs when a LAN device is installed.



9. Spare Parts List (1)

Part Number	Description	Location(S)
361400003030	ADHESIVE;ABS+PC PACK,G485,CEMIDAIN	
361400003005	ADHESIVE;HEAT,TRANSFER,HTA-48(W)	
221682840001	AK BOX;BEN Q,8089P	
541668760001	AK KIT;MD95298,8965	
441687600001	BATT ASSY;14.8V,2.2Ah,CGR18650C/P,8965	
441687600004	BATT ASSY;14.8V/2.2AH,LI,PANASONIC,4CELLS,8	
242670800113	BFM-WORLD MARK;WINXP,7521N	
342686900002	BRACKET;LCD,HOUSING,L,8066	
342686900003	BRACKET;LCD,HOUSING,R,8066	
421311310001	CABLE ASSY;PHONE LINE,6P2C,W/Z CORE,BLACK	
422687600005	CABLE FFC;TP,8965	
272991477501	CAP ; 470U , 6.3V , 20% , φ8*7.7 , H80 SMT , PXE6.3	PC793
272991687501	CAP ; 680U , 4V , 20% , φ8*7.7 , H80 SMT , PXE4VC	PC794
272075103408	CAP ;0.1U CR 50V 10% 0603 X7R SMT only TDK	C10,C11,C12,C15,C16,C3,C5
272005104705	CAP ;1U CR 50V +80-20% 0805 Y5V SMT only TDK	C14A,C14B,C4A,C4B
272075101404	CAP; 0.001U CR 50V 10% 0603 X7R SMT only TDK	C13
272075471409	CAP; 0.0047U CR 50V 10% 0603 X7R SMT only TDK	C4
272075223702	CAP; 0.22U CR 50V +80-20% 0603 Y5V SMT only TI	C1,C2,C20A,C24,C25
272105103702	CAP;.01U ,50V,+80-20%,0402,SMT	C155,C24,C244,C25,C6,PC28
272105103402	CAP;.01U ,CR,25V ,10%,0402,X7R,SMT	C174,C175,C176,C206,C208
272075103401	CAP;.01U ,CR,50V ,10%,0603,X7R,SMT	PC1,PC15,PC2,PC48,PC49,PC5
272075103401	CAP;.01U ,CR,50V ,10%,0603,X7R,SMT	C11,C13,C3,C8
272073223401	CAP;.022U,CR,25V ,10%,0603,X7R,SMT	C9
272105104701	CAP;.1U ,16V,+80-20%,0402,SMT	C1006,C101,C1026,C103,C1032
272075104701	CAP;.1U ,50V,+80-20%,0603,Y5V,SMT	PC10,PC12,PC13,PC22,PC4,PC7

Part Number	Description	Location(S)
272102104401	CAP;.1U ,CR,10V,10%,0402,X5R,SMT	C34,C35,C377,C424,C440,C443,C
272072104402	CAP;.1U ,CR,16V,10%,0603,X7R,SMT	PC62,PC65,PC66,PC818
272072104402	CAP;.1U ,CR,16V,10%,0603,X7R,SMT	C12,C16,C6
272073104401	CAP;.1U ,CR,25V,10%,0603,X7R,PRC	C22,C7
272005104404	CAP;.1U,CR,50V,10%,0805,SMT	PC25,PC44,PC63,PC64,PC826
272071332401	CAP;.33U ,10V ,10%,0603,X7R,SMT	C2
272030102401	CAP;1000P,2KV,10%,1808,X7R,SMT	C823
272030102401	CAP;1000P,2KV,10%,1808,X7R,SMT	C1,C2
272105102501	CAP;1000P,50V ,+/-20%,0402,X7R,SMT	C160,C171,C183,C184,C185,C188
272105102408	CAP;1000P,CR,50V,10%,0402,X7R,SMT	C163,C165,C167,C179,C180,C186
272075102403	CAP;1000P,CR,50V,10%,0603,X7R,SMT	PC3,PC53,PC54,PC68,PC69,PC73
272105101402	CAP;100P ,50V ,+ -10%,0402,NPO,SMT	C744,PC18,PC20,PC737,PC813
272075101401	CAP;100P ,50V ,10%,0603,COG,SMT	C20,C21
272105101401	CAP;100P ,50V ,5%,0402,COG,SMT	C164
272105100303	CAP;10P ,CR,50V ,5%,0402,NPO,SMT	C14,C15,C16,C2,C3,C4,C415
272011106407	CAP;10U,10V,+/-10%,1206,X5R,SMT,AVX	
272011106419	CAP;10U,10V,+-10%,X5R,1206,SMT	PC17,PC40,PC41,PC45,PC47,PC7
272001106703	CAP;10U,10V,+80-20%,0805,Y5V,SMT,YAGEO	C200,C203,C204,C207,C211,C218
272013106503	CAP;10U,25V,+-20%,X5R,1206,Mitsubishi	PC32,PC34,PC35,PC701,PC702
272001106702	CAP;10U,6.3V,+- 20%,0805,X5R,SMT	C109,C114,C115,C116,C117,C118
272011106404	CAP;10U,6.3V,10%,1206,X7R,SMT	C430,C431,C435,C461,C462,C463
272075120301	CAP;12P ,CR,50V ,5% ,0603,NPO,SMT	C787,C789
272431157507	CAP;150U ,TPC,6.3V,20%,H1.9,7343	C758
272075181301	CAP;180P ,50V ,5% ,0603,NPO,SMT	PC70,PC8
272105181403	CAP;180P,50V,10%,0402,SMT	PC19

9. Spare Parts List (2)

Part Number	Description	Location(S)
272001105403	CAP;1U ,10%,10V ,0805,X7R,SMT	PC11,PC59
272012105401	CAP;1U ,CR,16V ,10%,1206,X7R,SMT	C14A,C14B
272072105702	CAP;1U ,CR,16V,+80-20%,0603,Y5V,SMT	PC743
272003105701	CAP;1U ,CR,25V ,+80%-20%,0805,Y5V	PC56
272102105701	CAP;1U ,CR,6.3V ,80-20%,0402,Y5V	C1009,C1049,C170,C182,C205
272071105403	CAP;1U ,10V ,10%,0603,X5R,SMT	C10,C4
272101015401	CAP;1U,6.3V,+-10%,0402,X5R,SMT	C110,C111,C162,C166,C168,C169
272002225701	CAP;2.2U ,CR,16V ,+80-20%,0805,Y5V	C384,C63,C82,C851
272071225401	CAP;2.2U ,CR,6.3V ,10%,0603,X5R,SMT	C106,C112,C154,C158,C159
272105222501	CAP;2200P,50V ,+/-20%,0402,X7R,SMT	C28,C414,C762
272075222401	CAP;2200P,50V ,10%,0603,X7R,SMT	C15A
272105221403	CAP;220P ,CR,50V ,10%,0402,X7R,SMT	C102,C104,PC21,PC825
272431227504	CAP;220U ,4V ,20%,7343,POSCAP,SMT	C1038
272431227528	CAP;220U,2.5V,TPE-MC,20%,POSCAP,H1.8,7343,SM	
272431227516	CAP;220U,2V,20%,7343,SDK-CAP	PC75,PC76
272105220402	CAP;22P ,50V ,+ -10%,0402,NPO,SMT	C100,C280,C281,C417,C418,C468
272105332402	CAP;3300P,50V,10%,0402,SMT	PC812
272103331401	CAP;33P ,25V ,+/-10%,0402,NPO,SMT	C329,C330,C331,C337,C342,C344
272013475402	CAP;4.7U ,25V ,10%,1206,X5R,SMT,PANASONIC	PC708
272023475401	CAP;4.7U ,25V ,10%,1210,X5R,SMT	C1
272001475701	CAP;4.7U ,CR,10V ,+80-20%,0805,Y5V,SMT	C133,C763,C890
272070475701	CAP;4.7U,CR,6.3V,+80-20%,0603,Y5V,SMT	C214,C239,C256,C268,C269,C285
272075472701	CAP;4700P,50V ,+ -20%,0603,X7R,SMT	PC72
272073472301	CAP;4700P,CR,50V ,5% ,0603,X7R,SMT	C5
272105471403	CAP;470P ,50V,10%,0402,X7R,SMT	C11,C12,C17,C543

Part Number	Description	Location(S)
272075471401	CAP;470P ,50V,10%,0603,X7R,SMT	C17
272105470402	CAP;47P ,50V ,+ -10%,0402,NPO,SMT	C272,C274,C275,C375
272075470302	CAP;47P ,CR,50V ,5%,0603,NPO,SMT	PC71,PC73
272075562401	CAP;5600P,CR,50V ,10%,0603,X7R	PC43,PC67
272030050302	CAP;5P,3KV,5%,1808,NPO,SMT,only HolyStone	C19
272010680401	CAP;68P ,CR,2KV,10%,1206,NPO,SMT,PRC	
272010680301	CAP;68P,2KV,5%,1206,NPO,SMT,only HolyStone	C18
221682850007	CARD BOARD;FRAME,PALLET,BEN Q,8089P	
221686950001	CARD BOARD;PARTITION,PALLET,8066	
221682850003	CARD BOARD;TOP/BTM,PALLET,BEN Q,8089P	
221687620001	CARTON,DOUBLE PACKING,OUT,8965	
221687620002	CARTON;MD95298,8965	
431687600001	CASE KIT;8965	
442685400008	CFM Medion AC ADPT ASSY;19V,3.42A,FSP065-AA(	
413000020475	CFM_MEDION;LCD,LTN150XB-L03,TFT,15",XGA,S	
242682800003	CFM-INTEL;Celeron M,NOTBOOK,8089P	
242682800079	CFM-MEDION COA LABEL,WINXP SP2 VERSION,8	
523410484031	CFM-Medion Panasonic USB external ODD(COMBO) -	
561867993008	CFM-MEDION SINGLE PAGE;CYBERLINK DVD SOL	
412687600001	CFM-Medion Zcom;mini-PCI,802.11bg, XG630	
523402259050	CFM-Medion,HDD DRIVE,40GB,2.5",SAMSUNG MP0	
323768560002	CFM-Medion;DDR SODIMM MODULE,256MB(32M*	
324180786914	CFM-Medion;IC,CPU,Celeron-M 320,1.3GHZ(Banias),	
565168760001	CFM-MEDION;S/W,CD ROM SYSTEM DRIVER,FR,S2	
565167880005	CFM-Medion;SW CD ROM,NERO	

9. Spare Parts List (3)

Part Number	Description	Location(S)
421687600001	CFM-Medion;USB Y-Cable for External ODD ,8965	
565168292006	CFM-MEDION;WINXP WITH SP2, FRANCE VERSIO	
273000500237	CHOCK COIL; 3.0UH,35mOHM,3.5A,6.7X6.7X4.0,KI	PL705
273000500236	CHOCK COIL; 4.7UH,45mOHM,2.5A,5.8X5.2X4.5,KI	PL1,PL707
273000500244	CHOCK COIL;10UH,40mOHM,25%,4.5A,KRH105R-1	PL714,PL715
273000500241	CHOCK COIL;2.8UH,15mOHM,25%,8.0A,KRH105R-1	PL2
273000500239	CHOCK COIL;33UH,97mOHM,20%,2.7A,KRH124-33	PL706
273000500111	CHOCK COIL;3UH,14mOHM,7.5A,10039P	
273000500100	CHOKE COIL;0.47µH,20%,55A,3.5M	PL701
273000500084	CHOKE COIL;400UH(REF),D.2*1,10.5T,SMT,WLT0	L1,L2
273000150313	CHOKE COIL;90OHM/100MHZ,20%,2012,TDK	L17,L25,L40,L722,L724,L89
273000150352	CHOKE COIL;QXC24CD121U,120OHM/100MHZ,201	L703,L704,L705,L706
361200001018	CLEANNER;YC-336,LIQUID,STENCIL/PCB SMT,PR	
331000007056	CON;BATT,C10367-10701,7 PIN,ALLTOP	J705
331720015084	CON;D,FM,15P/3R,R/A,070915FR015S201ZU,SUYIN,	J701
291000002601	CON;FPC,26P*1,1MM,R/A,SMT	J2
291000141204	CON;FPC/FFC,12P,0.5MM,H=2,ACES,SMT	J3
291000143007	CON;FPC/FFC,88018-3000,15P*2,.8MM,BD/BD,SMT	J1006
291000024426	CON;HDR,FM,22P*2,2MM,R/A,SMT,SUYIN,200062F	J718
291000012031	CON;HDR,MA,10P*2,1MM,H5.4,R/A,SMT,ACES-881	J4
291000021104	CON;HDR,MA,11P*1,1.25,R/A,3811Y-T011-NNNA,S	CN1
291000021108	CON;HDR,MA,11P*1,1.25,ST,SMT,ACECON	J1001
291000020221	CON;HDR,MA,11P*1,1.25MM,R/A,ACES,85204-1100	
291000010209	CON;HDR,MA,2P*1,1.25MM,H4.2,ST,SMT,ACES	J709,J710,J712
291000000203	CON;HDR,MA,2P*1,3.5MM,R/A,SMT,SM02B,only AC	J2

Part Number	Description	Location(S)
291000020204	CON;HDR,MA,2P*1,3.5MM,R/A,SMT,SMO2B	
291000010303	CON;HDR,MA,3P*1,1.25MM,H4.2,ST,SMT,ACES	J711
291000020408	CON;HDR,MA,4P,1.25MM,H3.5MM,R/A,SMT,ACES	J2
291000610075	CON;MINI PIC FOR FAX MODEM SOCKET,0.8MM,I	J717
331810006008	CON;MODULAR JACK,FM,6P4C,R/A,FR	
291000810408	CON;PHONE JACK,4P,1.016MM,ALLTOP,C10138	J1
291000810802	CON;PHONE JACK,8P,H=12.59,R/A,RJ45	J715
331910002006	CON;POWER JACK,2P,20VDC,5A,DIP	PJ701
291000920607	CON;STEREO JACK,6P,W9.5,933100000180,SMT,AC	J704,J706
331040004031	CON;USB,FM,H7.85,R/A,4P*1,020173MR004SXXXZ	J1002,J1003,J1004,J703
346686900013	CONDUCTIVE TAPE;HOUSING,LCD,I-CABLE,8066	
345677000018	CONDUCTIVE TAPE;LCD,LYNX	
331000007025	CONNECTOR;7 PIN,DIP,ALLTOP,C10345-10701	CON1
342686900014	CONTACT PLATE;3CELL,L=45mm,W=5mm,PWR	
342503200003	CONTACT PLATE;W4L18T0.15,7521/GRAMPUS	
342503200005	CONTACT PLATE;W4L30T0.15,GRAMPUS	
342503400002	CONTACT PLATE;W5L9T0.13,7170LI,PRC	
342503400003	CONTACT PLATE;W7L7T0.13,7170LI,PRC	
340687600001	COVER ASSY;8965	
340687600002	COVER ASSY;DDR,8965	
340687600003	COVER ASSY;HDD,8965	
340687600004	COVER ASSY;KB,8965	
340687600005	COVER ASSY;LCD,8965	
344687600018	COVER;BATTERY,8965	
344687600004	COVER;CPU,8965	

9. Spare Parts List (4)

Part Number	Description	Location(S)
344687600007	COVER;HINGE,8965	
272625470401	CP;47P*4 ,8P,50V ,10%,1206,NPO,SMT	CP1
361300000011	DESICCANT PACK;60g,COMMON,PRC	
331660020004	DIMM SOCKET;DDR SODIMM 200P, CA0075 STD	J719
331660020005	DIMM SOCKET;DDR SODIMM 200P, CA0115 RVS	J716
288111544001	DIODE; 1SR-154-400 400V 1.0A SMT	
288100280001	DIODE; DII S1G ,280V1A,SMA, SMT,PWR	D1
288114148004	DIODE;1N4148WS,75V,200mW,SOD-323,SMT	D1
288110355001	DIODE;1SS355,80V,100mA,SOD-23,SMT	D2
288100340008	DIODE;B340LA,40V,3A,SMA,DIODES,SMT	
288100032013	DIODE;BAS32L,VRRM75V,MELF,SOD-80	D19,PD707
288100054001	DIODE;BAT54,30V,200mA,SOT-23	D20,D21
288100541002	DIODE;BAT54ALT1,COM. ANODE,SOT-23	PD709
288100054002	DIODE;BAT54C,SCHOTTKY DIODE,SOT23	PD717
288100701002	DIODE;BAV70LT1,70V,225MW,SOT-23	D13
288100070006	DIODE;BAV70LT1,70V,225MW,SOT-23,ON	D22,PD711,PD712
288100099001	DIODE;BAV99,70V,450MA,SOT-23	D3,D7,D8,PD1,PD2
288100099012	DIODE;BAV99LT1,70V,450MA,SOT-23,ON	
288100056003	DIODE;BAW56,70V,215mA,SOT-23	D9,PD4,PD5
288100056017	DIODE;BAW56LT1,70V,215MA,SOT-23,ON	
288105256001	DIODE;BZT52C5V6S,ZENER,5.2-6.0V,200mW,SOD-3	ZD3,ZD4
288104148024	DIODE;DII 1N4448HWS,57V250mA,SOD-323,SMT,P	
288101004024	DIODE;EC10QS04,RECT,40V,1A,CHIP,SMT	PD701
288200717001	DIODE;RB717F,SCHOTTKY,40V,SOT323,SMT	D3
288104148001	DIODE;RLS4148,200MA,500MW,MELF,SMT	D12,D702

Part Number	Description	Location(S)
288100024002	DIODE;RLZ24D,ZENER,23.63V,5%,SMT	PD715
288100840001	DIODE;SM840B,40V,8A,STD-202	PD713
288100034004	DIODE;SSA34,40V,3A,SMA	PD702,PD704,PD706
288100056005	DIODE;UDZ5.6B,ZENER,5.6V,UMD2,SMT	D16
288100056005	DIODE;UDZ5.6B,ZENER,5.6V,UMD2,SMT	
297120200002	DIP SW,4P,24VDC,25mA,SMT,FHDS-02F-T/R	SW701,SW702
344681700001	DUMMY;PVC-1088,D18L31.5,BATTERY,PWR	
272602107501	EC;100U,16V,M,6.3*5.5,-55+85'C,SMT	C1012,C1027,C1028,C1046,C105
312271006358	EC;100U,25V,RA,M,D6.3*7,SGX,SANYO	PC705,PC706
312075606131	EC;560U,4V,20%,8.0XL9.0,7mohm,4SEPC560MX,SA	PC46
312278206161	EC;820U ,2.5V,+-20%,8X12.5,OS-CON	PC710,PC711,PC712,PC714,PC71
343685200005	EMI FINGER;2X2MM,H5.5,MSML-0055A-H,MAGIC	TP40
343685200001	EMI FINGER;3X2MM,H2.5,SME-0025RA,U-TEK	TP10,TP38
343685200006	EMI FINGER;4.5X2MM,H7,SME-0070RA,MAGIC	TP41
227687600002	END CAP;L/R,NORMAL,8965	
481687600002	F/W ASSY;KBC,8965	U17
481687600001	F/W ASSY;SYS BIOS,8965	U16
273000150332	FERRIET CHIP;120OHM/100MHZ,2012,5A,MAGIC	L1004,L1021,L20,L32,L4,L43,L4
273000150156	FERRIET CHIP;120OHM/100MHZ,2012,6A,MAGIC	PL3,PL702,PL703,PL704,PL708,
273000610025	FERRITE ARRAY;120OHM/100MHZ,ONLY TDK.	FA1001
273000130001	FERRITE CHIP;120OHM/100MHZ,1608,200mA,SMT	L39,L47,L50,L51,L52,L53,L54,L5
273000130039	FERRITE CHIP;130OHM/100MHZ,1608,SMT	L10,L35,L5,L6,L61,L62,L63,L7,L
273000130015	FERRITE CHIP;220OHM/100MHZ,1608,200mA,SMT	L11,L12,L2
273000130006	FERRITE CHIP;600OHM/100MHZ,.2A,1608	L23,L26,L27,L30,L31,L37,L42,L7
273000150357	FERRITE CHIP;60OHM/100M,QT2012RL060HC3A,N	L15,L16,L21,L22

9. Spare Parts List (5)

Part Number	Description	Location(S)
245600010007	FLOW CARD;M/B,WHITE	
335152000085	FUSE; 128 DC-7A/50V 139℃only UCHIHASHI（內橋	F2
295000010048	FUSE;0.5A/15V,POLY SWITCH,SMD	F3
295000010008	FUSE;1.1A,POLY SWITCH,1812,SMT	F4,F5,F6,F7
295000010116	FUSE;FAST, 10A, 86VDC, 6125,SMT	PF701,PF702
295000010120	FUSE;FAST,1.5A,63V,1206,SMT,PRC	F1
295000010149	FUSE;FAST,1.5A,63VDC,1206,SMT,043301.5	
295000100004	FUSE;FAST,1A,63V,1206,THIN FILM	F2
295000100006	FUSE;FAST,2A/63V,R433002,1206,SMT	F1
335152000097	FUSE;LR4-73X,POLY SWITCH,PWR	
295000010163	FUSE;NORMAL,7A/24VDC,0433007,1206,LITTELFU	PF703
335152000060	FUSE;THERMAL FUSE,G7F510,93'C,PRC	
347107005010	GASKET;1,07,005,010	
347107010010	GASKET;1,07,010,010	
347210003015	GASKET;2,10,003,015	
347210020012	GASKET;2,10,020,012	
347210020012	GASKET;2,10,020,012	
347210030010	GASKET;2,10,030,010	
523468760004	HDD ASSY;40GB,2.5",SAMSUNG MP0402H,8965	
451687600004	HDD ME KIT;8965	
340687600009	HEATSINK ASSY;ALRO,CPU,8965	
340687600010	HEATSINK ASSY;MPT,CPU,8965	
451687600003	HEATSINK ME KIT;8965	
343674300005	HEATSINK;NORTH BRIDGE,E-NOTE	
342686900005	HINGE;HOUSING,LCD,L,8066	

Part Number	Description	Location(S)
342686900004	HINGE;HOUSING,LCD,R,8066	
342686900012	HINGE;L,SZS,8066	
342686900013	HINGE;R,SZS,8066	
340687600006	HOUSING ASSY;8965	
340687600007	HOUSING ASSY;LCD,8965	
451687600001	HOUSING KIT;8965	
344687600015	HOUSING;BATTERY,8965	
291000614793	IC SOCKET;UPGA479M,479P,MOLEX	U704
282574008005	IC;74AHC08,QUAD 2-I/P AND,TSSOP,14P	U712
282574014004	IC;74AHC14,HEX INVERTER,TSSOP,14P	U716
284507460002	IC;ADT7460,TEMPERATURE MTR,QSOP,16P,SMT	U707
284500655003	IC;ALC655,AUDIO CODEC,LQFP,48P,SMT	U702
286308800014	IC;AME8800,0.3A,1.5V,REG,SOT89	U14
286308800022	IC;AME8800MEFT,0.3A,1.8V,REG,SOT89N,SMT	U10
286303107001	IC;AMS3107C,3.3V,1%,VOL REGULATOR,SOT-223	U12
286002040001	IC;BQ2040,GAS GAUGE,SO,16P,SMT	IC1
283467540001	IC;EEPROM,M24C02-WMN6T,2K,SO8,SMT	IC2
283467540002	IC;EEPROM,M93C46-WMN6T,64*16 BITS,SO8,SMT	U710
283467530001	IC;EEPROM,S24CC02A,2K,SO8,SMT,ONLY SEIKO;P	
286305234001	IC;FAN5234MTCX,PWM,TSSOP,16P,FAIRCHILD	PU704
283468180001	IC;FLASH,512K*8,LPC & FWH,SST49LF004B,PLCC	
286302996001	IC;G2996,DDR,GMT,SOP8FD,SMT	PU11
286369229301	IC;G692L293T,RESET CIRCUIT,2.93V,SOT143,SMT	U13
284595090202	IC;ICS950902,CLOCK GEN,SSOP56,56P,SMT	U713
286100393004	IC;LMV393,DUAL COMPARTOR,SSOP,8P	PU1

9. Spare Parts List (6)

Part Number	Description	Location(S)
286303728002	IC;LTC3728LX,PWM CTRL,LTC,5X5 QFN,SMT	PU2,PU4
286303734001	IC;LTC3734,PWM CONTROLLER,32-QFN,SMT	PU711
286104173001	IC;MAX4173F,I-SENSE AMP,SOT23,6P	PU3
286301414001	IC;MM1414,PROTECTION,TSOP-20A,PRC	IC4
281101015001	IC;MP1015EM-Z,CCFL CTRL,TSSOP20,MPS	U1
281307085001	IC;NC7SZ08P5,2-INPUT & GATE,SC70-5P	U2,U3
284500800003	IC;PN800CD,NORTH BRIDGE,HSBGA,829P	U709
286309167001	IC;RT9167-47CB,200MA LDO REGULATOR,SOT-25	U6
286309702001	IC;RT9702A,POWER DISTRI SW,1.1A,SOT23-5,5P	U1001,U1004,U18,U19
286300812002	IC;S-812C,DECECTOR,SOT-89,PRC	IC3
286300431014	IC;SC431LCSK-.5,.5%,ADJ REG,SOT23	PQ4
286300594001	IC;TL594C,PWM CONTROL,SO,16P	PU702
286100212001	IC;TPA0212,AMPLIFIER,TSSOP,24P,SMT	U7
284501634002	IC;VT1634AL,LVDS TRANSMITTER,LQFP,48P,SMT	U703
284506103008	IC;VT6103L,LAN-PHY,LQFP48,SMT	U15
284508235008	IC;VT8235CE,SOUTH BRIDGE,BGA,487P,SMT	U711
284583950002	IC;W83L950D-Ver.C,LPC_KBC,LQFP,80P,SMT	
273000990180	INDUCTOR;3.0UH,30%,SPC06703,H2.85,TMP,SMT	
273000990021	INDUCTOR;33uH,CDRH124,SUMIDA,SMT	
346503100005	INSULATOR;5,BATTERY ASSY,7521Li	
346503200202	INSULATOR;BATT ASSY,ONE ROUND,BLAC,WEAS	
346503100001	INSULATOR;BATT ASSY,THERMAL FUSE,7521	
346503400503	INSULATOR;BATT ASSY,W7L13,8175	
346687600001	INSULATOR;DDR,8965	
346686900015	INSULATOR;FIBER,T=0.25mm,107*12,PCB,PWR	

Part Number	Description	Location(S)
346677300001	INSULATOR;FIBER,UL94V-0,D=17.5mm,T=0.25mm,	
346686900012	INSULATOR;FIBRE,T=1.2mm,L=25mm,W=7.5mm,P	
346669900004	INSULATOR;INVERTER,7170	
346687600002	INSULATOR;MB,8965	
346687600009	INSULATOR;RJ11 BD,8965	
361400003003	JET-MELT ADHESIVES;3478-Q,5/8in*8in,PRC	
531068760904	KBD OPTION;FR,BK,8965	
531068690004	KBD;FRANCE,JME,BLACK,8066	
451687600012	LABEL KIT;MD95298,8965	
242600000145	LABEL;10*10,BLANK,COMMON	
242600000145	LABEL;10*10,BLANK,COMMON	
242600000385	LABEL;27*10,LAN ID BAR CODE	
242600000378	LABEL;27*7MM,HI-TEMP 260'C	
242668300028	LABEL;32*7MM,POLYESTER FILM,HOPE	
242668300017	LABEL;4*3MM,HI-TEMP,260'C,HOPE	
242683700006	LABEL;48*6mm,EMPTY,WHITE,MIO 136 BATT,PV	
624200010140	LABEL;5*20,BLANK,COMMON	
624200010140	LABEL;5*20,BLANK,COMMON	
242600000232	LABEL;6*6MM,GAL,BLANK,COMMON	
242679900005	LABEL;BAR CODE,(25*10MM)*12pcs,8640C	
242600000157	LABEL;BAR CODE,125*65,COMMON	
242687600001	LABEL;BATT,14.8V/2.2AH,LI,PANASONIC,8965	
242600000433	LABEL;BLANK,11*5MM,COMMON	
242669900009	LABEL;BLANK,60*80MM,7170	
242600000452	LABEL;BLANK,7MM*7MM,PRC	

9. Spare Parts List (7)

Part Number	Description	Location(S)
242600000452	LABEL;BLANK,7MM*7MM,PRC	
242664800013	LABEL;CAUTION,INVERT BD,PITCHING	
242673800010	LABEL;CLASS LASER,MICRO MAXX,8375	
242687600013	LABEL;LCD HOUSING,LEFT,RED,8965	
242687600015	LABEL;LCD HOUSING,LEFT,SILVER,8965	
242687600011	LABEL;LCD HOUSING,LEFT,WHITE,8965	
242687600017	LABEL;LCD HOUSING,LEFT,YELLOW8965	
242687600014	LABEL;LCD HOUSING,RIGHT,RED,8965	
242687600016	LABEL;LCD HOUSING,RIGHT,SILVER,8965	
242687600012	LABEL;LCD HOUSING,RIGHT,WHITE,8965	
242687600018	LABEL;LCD HOUSING,RIGHT,YELLOW,8965	
242669600005	LABEL;LOT NUMBER,RACE	
242687600020	LABEL;MD95298,BAR CODE,EXTERNAL CARTON	
242687600019	LABEL;MD95298,SHIPPING MARK,EXTERNAL CA	
242600000001	LABEL;PAL,20*5MM,COMMON	
242687600003	LABEL;RATING,MD95298,MEDION,8965	
242678800019	LABEL;TRANSPARENT, § 50, 8381-Medion	
441687600015	LCD ASSY;15",CFM-MEDION,SAMSUNG-ID1,LTN15	
451687600014	LCD ME KIT;15",CFM-MEDION,SAMSUNG-ID1,LTN	
294011200043	LED;RE/GR,H0.8,L1.9,W1.6,19-22SRVGC	LED1,LED2
416268760008	LT PF;15",CFM-MEDION,ID1,SAMSUNG,LTN150XB	
526268760009	LTO;8965ID1/T5PB/40E/3FR9/A5S4A/	
561568760002	MANUAL;USER'S,FR,8965,MD95298,MEDION	
346687600004	MYLAR;LCD,8965	
242687600010	NAMEPLATE;MEDION,8965	

Part Number	Description	Location(S)
461687600003	PACKING KIT;MD95298,8965	
224682800001	PALLET;COMPLEX,1200*1000*126,8089P	
221682850006	PARTITION;BEN Q,AK BOX,8089P	
412678800001	PCB ASSY;FAX MODEM 56K,1456VQL4A,8381B	
316687600001	PCB;PWA-8965/M BD	R01
316687600003	PCB;PWA-8965-8066/BATTERY BD,PWR	R0A
316682200003	PCB;PWA-INVERTER BD(DA-1A08-D03);PWR	R0A
316687600004	PCB;PWA-RJ11 card	R01
222670820003	PE BAG;L560*W345,7521N	
222671330003	PE BAG;LCD BRACKET,STINGRAY	
222672730001	PE BUBBLE BAG;200*240mm,AMM-9019	
222503220001	PE BUBBLE BAG;BATTERY,GRAMPUS	
273000150033	PHASEOUT;FERRITE CHIP,120OHM/100MHZ,25%,	L87
346687600011	PROTECT FILM;LCD HOUSING,15",8965	
222677800001	PROTECTING COLTH;LCD/KB/8375P	
411687600001	PWA;PWA-8965,MOTHER BD	
411687600003	PWA;PWA-8965,MOTHER BD,SMT	
411687600002	PWA;PWA-8965,MOTHER BD,T/U	
411687600012	PWA;PWA-8965,RJ-11,MODEM BD	
411687600013	PWA;PWA-8965,RJ-11,MODEM BD,SMT	
411687600006	PWA;PWA-8965/BATT PANASONIC,4CELLS,BOAR	
411687600007	PWA;PWA-8965/BATT PANASONIC,4CELLS,GAUG	
411682200006	PWA;PWA-INVERTER BD,DA-1A08-D03/8965,PWR	
411682200007	PWA;PWA-INVERTER BD,SMT,DA-1A08-D03/8965	
332810000213	PWR CORD;250V/2.5A,2P,BLK,EU,175CM,I-SHENG	

9. Spare Parts List (8)

Part Number	Description	Location(S)
271046017301	RES;.001,2W,5%,2512,CYNTEC,SMT	PR703
271046068101	RES;.006 ,1.5W ,1% ,2512,SMT;PWR	PR33
271046067102	RES;.006 ,1.5W ,1% ,2512,SMT;PWR,only Cyntec	
271045087101	RES;.008 ,1W ,1% ,2512,SMT	PR755
271045107101	RES;.01 ,1W ,1% ,2512,SMT	PR744
271045127102	RES;.012,1W,1%,2512,SMT	PR754
271045157101	RES;.015 ,1W ,1% ,2512,SMT	PR15
271584029101	RES;.02 ,2W ,1% ,2512 ,SMT,Cyntec	PR701
271586026101	RES;.02 ,2W,1%,2512,SMT	
271046257101	RES;.025 ,2W ,1% ,2512,SMT,PRC	R6
271002000301	RES;0 ,1/10W,5% ,0805,SMT	L34,L38,L49,L710,L92,R261,R34
271061000002	RES;0 ,1/16W,0402,SMT	PR25,PR29,PR704,PR725,PR779,
271071000002	RES;0 ,1/16W,5% ,0603,SMT	L723,L727,L79,L88,PR20,PR21,P
271071000002	RES;0 ,1/16W,5% ,0603,SMT	R41
271012000301	RES;0 ,1/8W,5% ,1206,SMT	PR712
271045507103	RES;0.050,1W, 1%,2512,SMT, only KOA;PWR	R24,R24A,R24C
271061010101	RES;1,1/16W,1%,0402,SMT	PR813
271061135101	RES;1.3M,1/16W,1%,0402,SMT	PR793,R27
271061152501	RES;1.5K ,1/16W,5% ,0402,SMT	R172,R847
271071152302	RES;1.5K ,1/16W,5% ,0603,SMT	R17,R19
271071161102	RES;1.6K,1/16W,1% ,0603,SMT	PR62
271071182101	RES;1.8K ,1/16W,1% ,0603,SMT	PR719
271061196212	RES;1.96K,1/16W,1%,0402,SMT	PR791
271071100101	RES;10 ,1/16W,1% ,0603,SMT	PR37
271061100501	RES;10 ,1/16W,5% ,0402,SMT	PR721,R321,R322,R323,R324,R32

Part Number	Description	Location(S)
271071100302	RES;10 ,1/16W,5% ,0603,SMT	PR726
271061100102	RES;10,1/16W,1%,0402,SMT	PR777,PR778,PR784
271061101103	RES;100 ,1/16W,1% ,0402,SMT	R209,R210,R225,R226,R256,R86,I
271071101301	RES;100 ,1/16W,5% ,0603,SMT	R11,R12,R14,R15,R16,R20,R21,R2
271061104102	RES;100K ,1/16W,1% ,0402,SMT	PR30,PR31,PR67,PR702,PR812,P
271071104101	RES;100K ,1/16W,1% ,0603,SMT	PR35,PR4,PR52,PR54,PR55,PR56
271071104101	RES;100K ,1/16W,1% ,0603,SMT	R18,R22,R23,R9
271061104501	RES;100K ,1/16W,5% ,0402,SMT	R109,R154,R24,R45,R48,R57,R75
271071104302	RES;100K ,1/16W,5% ,0603,SMT	R7
271071107311	RES;107K ,1/16W,1% ,0603,SMT	PR41
271061103102	RES;10K ,1/16W,1% ,0402,SMT	PR775
271071103101	RES;10K ,1/16W,1% ,0603,SMT	PR716
271061103501	RES;10K ,1/16W,5% ,0402,SMT	PR723,PR727,R1007,R1015,R101
271071103302	RES;10K ,1/16W,5% ,0603,SMT	R5,R7,R8
271061106501	RES;10M ,1/16W,5% ,0402,SMT	R857
271061127212	RES;12.7K,1/16W,1%,0402,SMT	PR797
271071124311	RES;124K ,1/16W,1% ,0603,SMT	PR818
271061133311	RES;13.3K,1/16W,1%,0402,SMT	PR794
271071137211	RES;13.7K,1/16W,1% ,0603,SMT	PR6
271071137011	RES;137 ,1/16W,1% ,0603,SMT	R14A
271071151101	RES;150 ,1/16W,1% ,0603,SMT	R272,R273
271071151302	RES;150 ,1/16W,5% ,0603,SMT	R133,R134,R135,R137,R138,R139
271061151102	RES;150 ,1/16W, 1%,0402,SMT	R119
271061153102	RES;15K ,1/16W,1% ,0402,SMT	PR17,PR18
271061152302	RES;15K ,1/16W,5% ,0402,SMT	R73

9. Spare Parts List (9)

Part Number	Description	Location(S)
271071164101	RES;160K ,1/16W,1% ,0603,SMT	R13
271061184302	RES;180K ,1/16W, 5%,0402,SMT	R972
271071184101	RES;180K ,1/16W,1% ,0603,SMT	PR61
271071183101	RES;18K ,1/16W,1% ,0603,SMT	PR19
271071196211	RES;19.6K,1/16W,1% ,0603,SMT	PR47
271002102301	RES;1K ,1/10W,5% ,0805,SMT	R84,R85
271061102105	RES;1K ,1/16W,1% ,0402,SMT	PR16,PR26,PR798,R1043,R229,R4
271071102102	RES;1K ,1/16W,1% ,0603,SMT	PR12,PR43,PR44,PR722
271061102303	RES;1K ,1/16W,5% ,0402,SMT	R1028,R160,R216,R253,R296,R29
271071102302	RES;1K ,1/16W,5% ,0603,SMT	R11
271013102301	RES;1K ,1/4W ,5% ,1206,SMT	PR75
271061105501	RES;1M ,1/16W,5% ,0402,SMT	PR71,PR72,PR796,PR811,PR814,
271071105301	RES;1M ,1/16W,5% ,0603,SMT	PR36,PR58,PR59
271071105301	RES;1M ,1/16W,5% ,0603,SMT	R10,R3
271061222501	RES;2.2K ,1/16W,5% ,0402,SMT	R300,R301,R302,R70
271061232111	RES;2.32K,1/16W,1%,0402,SMT	PR776
271071249111	RES;2.49K,1/16W,1% ,0603,SMT	PR821
271061272102	RES;2.7K ,1/16W,1% ,0402,SMT	R72,R80
271071201301	RES;200 ,1/16W,5% ,0603,SMT	R1A,R1B
271061201101	RES;200 ,1/16W, 1%,0402,SMT	R116,R122,R146,R148,R152
271071204101	RES;200K ,1/16W,1% ,0603,SMT	PR45,PR46
271071204101	RES;200K ,1/16W,1% ,0603,SMT	R17B
271071203701	RES;20K ,1/16W,.1%,0603,SMT	PR11
271071203101	RES;20K ,1/16W,1% ,0603,SMT	PR22,PR24,PR27,PR48
271061220501	RES;22 ,1/16W,5% ,0402,SMT	R1024,R1026,R181,R259,R305,R4

Part Number	Description	Location(S)
271012221301	RES;220 ,1/8W,5% ,1206,SMT	PR14,PR73,PR74,PR771,PR772,P
271061221313	RES;220 ,1/16W, 5%,0402,SMT	R106,R386,R389,R392
271071224301	RES;220K ,1/16W,5% ,0603,SMT	R1
271071226311	RES;226K ,1/16W,1% ,0603,SMT	PR1
271071237211	RES;23.7K,1/16W,1% ,0603,SMT	PR9
271061249312	RES;249K,1/16W,1%,0402,SMT	PR803
271061270102	RES;27.4 ,1/16W, 1%,0402,SMT	R107,R151,R96
271071274911	RES;27.4 ,1/16W,1% ,0603,SMT	R255
271071202301	RES;2K ,1/16W,5% ,0603,SMT	R12
271071205101	RES;2M ,1/16W,1% ,0603,SMT	PR10
271071304301	RES;300K ,1/16W,5% ,0603,SMT	R311
271061301112	RES;301 ,1/16W,1% ,0402,SMT	R310
271071301011	RES;301 ,1/16W,1% ,0603,SMT	PR720
271071301311	RES;301K ,1/16W,1% ,0603,SMT	R3
271061330501	RES;33 ,1/16W,5% ,0402,SMT	R265,R282,R284,R285,R313,R37,
271061331304	RES;330 ,1/16W,5% ,0402,SMT	R291,R929
271071331301	RES;330 ,1/16W,5% ,0603,SMT	R16,R18,R20,R21,R22,R23
271071331301	RES;330 ,1/16W,5% ,0603,SMT	C14
271071333101	RES;33K ,1/16W,1% ,0603,SMT	PR51
271061361101	RES;360 ,1/16W,1% ,0402,SMT	R228,R289
271061390501	RES;39, 1/16W, 5%,0402,SMT	R118
271071392311	RES;392K ,1/16W,1% ,0603,SMT	PR7
271061302101	RES;3K ,1/16W,1% ,0402,SMT	R230
271071432111	RES;4.32K,1/16W,1% ,0603,SMT	R10
271071478101	RES;4.7 ,1/16W,1% ,0603,SMT	PR32,PR38,PR39,PR70,PR802

9. Spare Parts List (10)

Part Number	Description	Location(S)
271002472301	RES;4.7K ,1/10W,5% ,0805,SMT	PR745,PR747
271061472102	RES;4.7K ,1/16W,1% ,0402,SMT	R288
271061472501	RES;4.7K ,1/16W,5% ,0402,SMT	R1023,R13,R167,R168
271071472302	RES;4.7K ,1/16W,5% ,0603,SMT	PR816,PR817
271071499111	RES;4.99K,1/16W,1% ,0603,SMT	PR23
271071432211	RES;43.2K,1/16W,1% ,0603,SMT	R1
271071442311	RES;442K,1/16W,1% ,0603,SMT	PR3
271071453211	RES;45.3K,1/16W,1% ,0603,SMT	PR28
271061471501	RES;470 ,1/16W,5% ,0402,SMT	R341,R382
271072474101	RES;470K ,1/10W,1% ,0603,SMT	PR34
271072474101	RES;470K ,1/10W,1% ,0603,SMT	R4,R5
271061474501	RES;470K ,1/16W,5% ,0402,SMT	PR77,R164
271061475111	RES;475 ,1/16W,1% ,0402,SMT	R895
271061499012	RES;49.9 ,1/16W,1% ,0402,SMT	R211,R212,R254,R342,R343,
271071499211	RES;49.9K,1/16W,1% ,0603,SMT	PR724
271071499311	RES;499K ,1/16W,1% ,0603,SMT	PR53
271071499311	RES;499K ,1/16W,1% ,0603,SMT	R17A
271061562102	RES;5.6K ,1/16W, 1%,0402,SMT	R275,R317,R720
271061510303	RES;51, 1/16W, 5%,0402,SMT	R136,R149,R760,R763
271061549011	RES;54.9 ,1/16W,1% ,0402,SMT	R108,R147,R95,R97,R98
271061562212	RES;56.2K,1/16W,1%,0402,SMT	PR790
271071563101	RES;56K ,1/16W,1% ,0603,SMT	R6
271061576411	RES;576K ,1/16W,1% ,0402,SMT	PR774
271071604111	RES;6.04K,1/16W,1% ,0603,SMT	R926
271071619111	RES;6.19K,1/16W,1% ,0603,SMT	PR819

Part Number	Description	Location(S)
271061649212	RES;6.49K,1/16W,1% ,0402,SMT	R901
271061604011	RES;60.4 ,1/16W,1% ,0402,SMT	R169,R223
271071634211	RES;63.4K,1/16W,1% ,0603,SMT	PR2,PR42
271071665011	RES;665 ,1/16W,1% ,0603,SMT	R314
271061681501	RES;680 ,1/16W,5% ,0402,SMT	R120,R247
271071684101	RES;680K ,1/16W,1% ,0603,SMT	PR795
271071752101	RES;7.5K ,1/16W,1% ,0603,SMT	PR718
271061753101	RES;75,1/16W,1%,0402,SMT	R11,R12,R277,R278,R308,R309,R
271071753301	RES;75K ,1/16W,5% ,0603,SMT	R8
271071822102	RES;8.2K ,1/16W,1% ,0603,SMT	R14B
271061806311	RES;80.6K,1/16W,1% ,0402,SMT	PR800
271061820501	RES;82 ,1/16W,5% ,0402,SMT	R214
271071976311	RES;976K ,1/16W,1% ,0603,SMT	PR5
271571100301	RP;10*8 ,16P ,1/16W,5% ,1606,SMT	RP22,RP23,RP53,RP54
271611103301	RP;10K*4 ,8P ,1/16W,5% ,0612,SMT	RP707
271621103302	RP;10K*8 ,10P,1/32W,5% ,1206,SMT	RP705
271611153301	RP;15K*4 ,8P ,1/16W,5% ,0612,SMT	RP6,RP706,RP9
271611220301	RP;22*4 ,8P ,1/16W,5% ,0612,SMT	RP701
271591220301	RP;22*4,8P,1/16W,5%,0804,SMT	RP12,RP14,RP15,RP16,RP17,RP1
271571220301	RP;22*8 ,16P ,1/16W,5% ,1606,SMT	RP13,RP5,RP704,RP708,RP709
271611330301	RP;33*4 ,8P ,1/16W,5% ,0612,SMT	RP11,RP702,RP8
271591330302	RP;33*4,8P,1/16W,5%,0804,SMT	RP39
271571330301	RP;33*8 ,16P ,1/16W,5% ,1606,SMT	RP32,RP33,RP34,RP35,RP36,RP3
271621472302	RP;4.7K*8,10P,1/32W,5% ,1206,SMT	RP3,RP703
371102610603	SCREW;M2.6L6,FLNG/PAN(+),NIW/NLK	

9. Spare Parts List (11)

Part Number	Description	Location(S)
371102010252	SCREW;M2L2.5,K-HEAD(+),NIB/NLK	
371102010252	SCREW;M2L2.5,K-HEAD(+),NIB/NLK	
340686900009	SHIELDING ASSY;COVER,8066	
340686900016	SHIELDING ASSY;HDD,8066	
333025000005	SHRINK TUBE;300V,125,I.D=2.5,T=0.15,L=13,BLAC	
333025000004	SHRINK TUBE;300V,125,I.D=2.5,T=0.15,L=7,BLACK	
333025000011	SHRINK TUBE;600V,125'C,ID3.5L15,PWR	
333050000117	SHRINK TUBE;UL,600V,105'C,ID2.5*7MM,8175	
561868290002	SINGLE PAGE;BAG ORDER CARD,FR,8599,MD4263	
561867880001	SINGLE PAGE;DISPLAY ATTENTION,GN,8381,ME	
561867780003	SINGLE PAGE;ETRUST FLYER,FR,8375P,MEDION	
561868760001	SINGLE PAGE;RECOVERY FLYER,FR/GR/EN,8965,M	
561868560007	SINGLE PAGE;WARRANTY,GN,8089C,MD95196,12-	
361400003021	SOLDER CREAM;NOCLEAN,P4020870980	
361400003021	SOLDER CREAM;NOCLEAN,P4020870980	
361200003047	SOLDER PASTE;NO CLEAN,RMA,CK3000-2	
365350000003	SOLDER WIRE;0.8MM,SN43/PB43/BI14,N/C,TELEC	MTG701
600100010009	SOLDER WIRE;63/37,0.8,CM,N/C,PRC	
600100010009	SOLDER WIRE;63/37,0.8,CM,N/C,PRC	
600100010009	SOLDER WIRE;63/37,0.8,CM,N/C,PRC	
600100010009	SOLDER WIRE;63/37,0.8,CM,N/C,PRC	
341680900001	SPC SCREW;#4-1/4,8050	
370102010502	SPC-SCREW;M2 L5,NIB,K-HD,t0.8,NLK	
370102610401	SPC-SCREW;M2.6L4,K-HD,t0.8,NIB/NLK	
370102610401	SPC-SCREW;M2.6L4,K-HD,t0.8,NIB/NLK	

Part Number	Description	Location(S)
370102610603	SPC-SCREW;M2.6L6,K-HD,NIB/NLK	
370102610603	SPC-SCREW;M2.6L6,K-HD,NIB/NLK	
370102030301	SPC-SCREW;M2L3,K-HD,1,NIB/NLK	
370102010407	SPC-SCREW;M2L4,K-HD,NIB/NLK	
370103010405	SPC-SCREW;M3L4,NIW,K-HD,T0.3	
340687600008	SPEAKER ASSY;L,8965	
340686900010	SPEAKER ASSY;R,8066	
340687600011	SPEAKER ASSY;VECO,L,8965	
340686900013	SPEAKER ASSY;VECO,R,8066	
226600030332	SPONGE;320*290*10,CAIMAN,PWR	
346677000016	SPONGE;RTC,LYNX	
345686900004	SPONGE;SPEAKER,LEFT,MB,8066	
341677000002	SPRING;SCREW,HEATSINK,LYNX	
342674500002	STAND OFF;AM20-30,GP3	MTG701
225678800001	TAPE; adhesive tape , kraft paper,W=48MM,8381-MI	
225600000061	TAPE;ADHENSIVE,DOUBLE-FACE,W20,UL,PRC	
225600000054	TAPE;INSULATING,POLYESTER FILM,17.5MM,13	
338536010053	TF041-BATTERY;LI,3.6V/2.2AH,CGR18650C,PAN,P	
294011200534	TF041-TH-LED;RED,H0.8,0603,C190KRKT,SMT	D29,D31,D32,D33
294011200534	TF041-TH-LED;RED,H0.8,0603,C190KRKT,SMT	LED3,LED4,LED5,LED6
297040100033	TF041-TH-SW;PUSH BUTTOM,5P,SPST,12VDC,50m	SW1,SW2,SW4
297030100019	TF041-TH-SW;TOGGLE,SPST,5V/1mA,DT016-Pt11A	SW3
310111103027	THERMISTOR;10K,1%,RA,DISK,103AT-4,only 爲勤	RT1
442687600002	Touch Pad;Single-Chip Atp-Ultra Thin Module Model T	
288227002006	TRANS;2N7002LT1,N-CHANNEL FET,ESD	PQ11,PQ12,PQ13,PQ14,PQ15,PQ

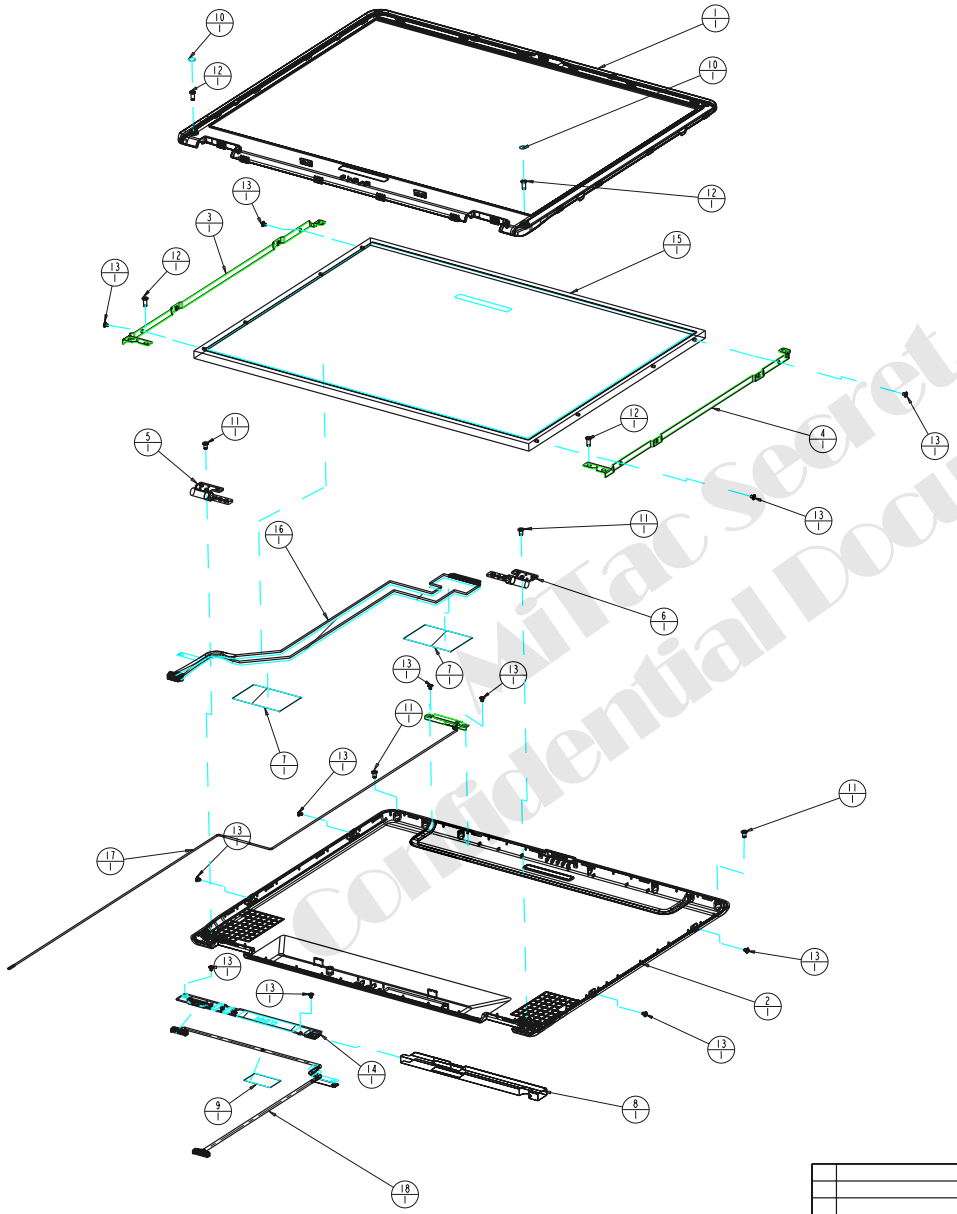
9. Spare Parts List (12)

Part Number	Description	Location(S)
288227002001	TRANS;2N7002LT1,N-CHANNEL FET,SOT-23	Q11,Q41,Q42
288227002001	TRANS;2N7002LT1,N-CHANNEL FET,SOT-23	
288203414001	TRANS;AO3414,N-CHANNEL FET,SOT-23	Q14,Q16
288204407001	TRANS;AO4407,P-MOS,.01OHM,SO8,SMT	PQ702,PQ703,PQ706,PQ712
288204409001	TRANS;AO4409,P-MOSFET,SO-8P,MSL,PWR	Q3,Q5
288204410010	TRANS;AO4410,N-MOSFET,ID=18A,0.0065OHM,SO	PU10
288204419001	TRANS;AO4419,P-MOSFET,20mOHM(VGS = -10V),S	Q8,U8,U9
288204422001	TRANS;AO4422,24mOHM,N-MOSFET,SOIC-8	PU707,PU9
288204912001	TRANS;AO4912,24mOHM ,SMT	PU703,PU708,PU8
288200404001	TRANS;AOD404,N-MOSFET,8mOHM,TO-252,SMT	
288200414001	TRANS;AOD414,N-MOSFET,7mOHM,TO-252,SMT	
288200436002	TRANS;AOD436,N-MOS,85A,30V,13mOHM,TO-252,	PU714
288200438002	TRANS;AOD438,N-MOS,85A,30V,5.5mOHM,TO-252	PU712,PU713
288200114009	TRANS;DDTC114TCA,N-MOSFET,SOT-23,DII	Q713,Q714
288200144011	TRANS;DDTC144TCA,NPN,SOT-23,SMT	Q29,Q31,Q34,Q36,Q37,Q38,Q39,(
288200144009	TRANS;DDTC144WCA,NPN,SOT-23,SMT	Q22
288200144037	TRANS;DII DDTA144EKA,40V100mA ,PNP,SMT,PW	Q1
288200144008	TRANS;DTA144EKA,PNP,SMT	
288200144002	TRANS;DTA144WK,PNP,SMT	PQ709
288200114001	TRANS;DTC114TKA,10K,N-MOSFET,SOT23	Q12
288200114006	TRANS;DTC114TKA,NPN,SOT23,SMT,PANASONIC	
288200144003	TRANS;DTC144TKA,N-MOSFET,SOT-23	Q28,Q35,Q703,Q705
288200144020	TRANS;DTC144TKA,NPN,SOT-23,SMT,PANASONIC	
288200144001	TRANS;DTC144WK,NPN,SOT-23,SMT	PQ1
288200144019	TRANS;DTC144WK,NPN,SOT-23,SMT,PANASONIC	

Part Number	Description	Location(S)
288204435003	TRANS;FDS4435,P-MOSFET,35mOHM,SO,8P,MRS	
288200301001	TRANS;FDV301N,N-CHANNEL,SOT23	Q40,Q9
288202222001	TRANS;MMBT2222AL,NPN,TO236AB	PQ707
288202222019	TRANS;MMBT2222ALT1,NPN,TO236AB,ON	
288203904010	TRANS;MMBT3904L,NPN,Tr35NS,TO236AB	PQ720
288203904022	TRANS;MMBT3904L,NPN,Tr35NS,TO236AB,ON	
288202301001	TRANS;SI2301DS,P-MOSFET,SOT-23	Q21,Q23,Q33,Q5,Q710,Q718
288204800001	TRANS;SI4800DY,N-MOS,.0185OHM,SO8	
288204814001	TRANS;SI4814,26.5mOHM,N_MOS ,SMT	
288204832001	TRANS;SI4832DY,N-MOSFET,.028OHM,SO8	PU710
422677000008	WIRE ASSY;BATT TO MB,FOR LYNX,MOLEX	J712
422687600006	WIRE ASSY;INVERTER,MPT,8965	
422686900002	WIRE ASSY;LCD,HSD150PX14,8066	
422686900005	WIRE ASSY;LCD,HSD150PX14,MPT,8066	
422687600007	WIRE ASSY;MDC,4P TO 2P,8965	
332110020177	WIRE;#20,UL1007,140MM,BLK,PWR	CN5
332110020094	WIRE;#20,UL1007,65MM,RED,YIYI;PWR	CN1
332110026135	WIRE;#26,UL1007,40MM,ORANGE,PRC,PWR	CN4
332110026172	WIRE;#26,UL1007,60MM,BLUE,YIYI;PWR	CN3
332110026124	WIRE;#26,UL1007,80MM,YELLOW,YIYI;PWR	CN2
422686900003	WLEN ASSY;CABLE,8066	
273001050160	XFMR;CI8.5,25T/2150T,300mH,ONLY TMP,PWR	T1
273001050039	XSFORMER;10/100 BASE,LF-H80P,SMT	U714
274011431449	XTAL;14.318MHZ,32PF,50PPM,8*4.5,2P	X704
274011431414	XTAL;14.318MHZ,32PF,50PPM,8*4.5,2P	

9. Spare Parts List (13)

Part Number	Description	Location(S)
274012500436	XTAL;25Mhz,GF DIP 49SS SMD 30PPM,16PF,10.0*3	X1
274013276103	XTAL;32.768KHZ,20PPM,12.5PF,CM200	X705
274010800410	XTAL;8Mhz,GF DIP 49SS SMD 30PPM,20PF,10.0*3.(	X2
		P/N:526268760009



ITEM	PART NO	DESCRIPTION	Q'TY	TYPE	REMARK
1	340687600005	COVER ASSY;LCD,8965	1	ASSEMBLY	
2	340687600007	HOUSING ASSY;LCD,8965	1	ASSEMBLY	
3	342686900002	BREAKET-LCD-HOUSING-L-8066	1	PART	
4	342686900003	BREAKET-LCD-HOUSING-R-8066	1	PART	
5	342686900012	HINGE;L,SZS,8066	1	PART	
6	342686900013	HINGE;R,SZS,8066	1	PART	
7	345677000018	CONDUCTIVE TAPE;LCD,LYNX	2	PART	
8	346669900004	INSURLATOR;INVERTER,7170	1	PART	
9	346686900013	CONDUCTIVE TAPE;LCD-I_CABLE,8066	1	PART	
10	346687600004	MYLAR;COVER,LCD,8965	2	PART	
11	370102610401	SPC-SCREW;M2.6L4,K-HD,t0.8,NIB/N	4	PART	
12	370102610603	SPC-SCREW; M2.6L6 K-HEAD,NIB/NLK	4	PART	
13	371102010252	SCREW;M2L2.5,K-HEAD(+),NIB/NLK	12	PART	
14	411682200006	PWA;PWA-INVERTER BD,DA-1A08-D03/	1	ASSEMBLY	
15	413000020433	LCD;LTM150XB-L03,15",XGA,SAMSUNG	1	PART	
16	422686900002	WIRE ASSY;LCD ,HSD150PX14,8066	1	ASSEMBLY	
17	422686900003	WLEN CABLE;CABLE,8066	1	ASSEMBLY	
18	422687600001	WIRE ASSY;INVERTER,8965	1	ASSEMBLY	

ITEM	CONTENTS OF CHANGE	RVS	CHK	APV	M/D/Y
					/ /
					/ /
					/ /
					/ /
					/ /

TOL ± RANGE	Pla	Met	Ins	Por	Cab	Pac	Gas	PCB
0-6	0.1	0.1	0.1	0.2	0.5	1	0.5	0.1
6-30	0.1	0.1	.15	.25	1	1	0.5	0.1
30-80	0.1	.15	0.2	0.3	2	1.5	1	0.1
80-180	.15	.15	.25	0.3	2	2	1	.15
180-315	.15	0.2	0.3	0.4	2.5	2	1	.15
315-800	0.2	0.3	0.4	0.5	3	3	2	.15

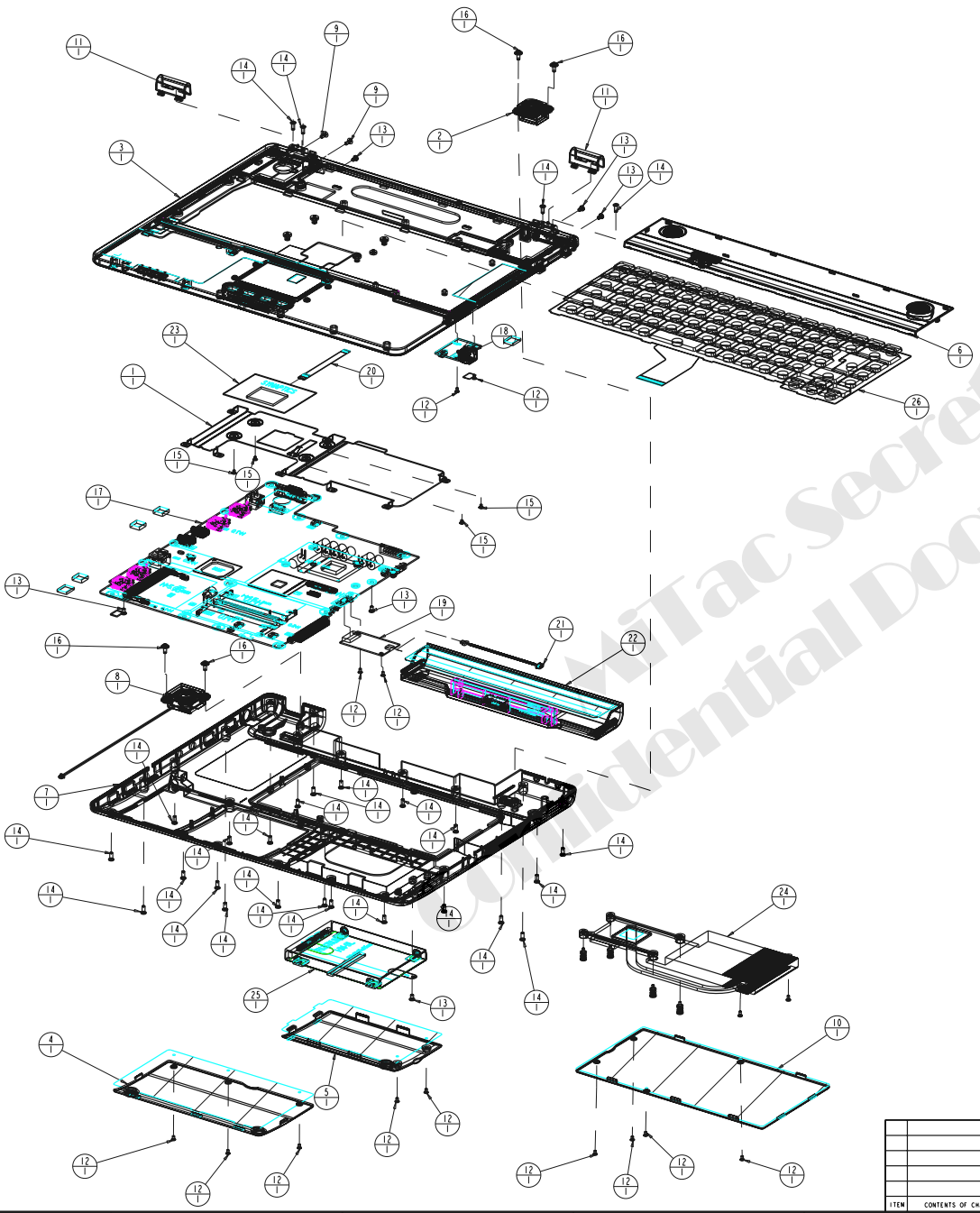
DATE	12-Nov-04	MATERIAL	SEE NOTES	TREATMENT	REMARK
UNIT	MM	SCALE	0.50	DRAWING NAME	LCD ME KIT;15",SAMSUNG,8965
DRAWN	DESIGNED	CHECKED	APPROVED	MATERIAL NO.	AD 451 6876 00007 R 00

MiTAC Technology Corp.

model name:LCD-ASSY-8965

file name:LCD_ME-KIT-SAMSUNG-8965

SHEET NO. 1 of 1



ITEM	PART NO	DESCRIPTION	Q'TY	TYPE	REMARK
1	340686900009	SHIELDING ASSY;COVER,8066	1	ASSEMBLY	
2	340686900010	SPEAKER ASSY;R,8066	1	ASSEMBLY	
3	340687600001	COVER ASSY;8965	1	ASSEMBLY	
4	340687600002	COVER ASSY;DDR,8965	1	ASSEMBLY	
5	340687600003	COVER ASSY;HDD,8965	1	ASSEMBLY	
6	340687600004	COVER ASSY;KB,8965	1	ASSEMBLY	
7	340687600006	HOUSING ASSY;8965	1	ASSEMBLY	
8	340687600008	SPEAKER ASSY;L,8965	1	ASSEMBLY	
9	341680900001	SPC SCREW;#4-1/4,8050	2	PART	
10	344687600004	COVER;CPU,8965	1	PART	
11	344687600007	COVER;HINGE,8965	2	PART	
12	370102030301	SPC-SCREW; M2L3,K-HEAD,I,NIB,NLK	13	PART	
13	370102610401	SPC-SCREW;M2.6L4,K-HD,t0.8,NIB/N	6	PART	
14	370102610603	SPC-SCREW; M2.6L6 K-HEAD,NIB/NLK	26	PART	
15	371102010252	SCREW;M2L2.5,K-HEAD(+),NIB/NLK	4	PART	
16	371102610603	SCREW;M2.6L6,FLNG/PAN(+),NIW/NLK	4	PART	
17	411687600001	PWA;PWA-8965,MOTHER BD	1	ASSEMBLY	
18	411687600012	PWA;PWA-8965,RJ-11,MODEM BD	1	ASSEMBLY	
19	412671800001	PCB ASSY;FAXMODEM,56K,MDC,GP2	1	PART	
20	422687600005	CABLE FFC;TP,8965	1	PART	
21	422687600007	WIRE ASSY;MDC,4P TO 2P,8965	1	ASSEMBLY	
22	441687600001	BATT ASSY;8965	1	ASSEMBLY	
23	442687600002	TOUCHPAD;SINGLE-CHIP ATP-ULTRA-T	1	PART	
24	451687600003	HEATSINK ME KI;8965	1	ASSEMBLY	
25	451687600004	HDD ME KIT;8965	1	ASSEMBLY	
26	531020237661	KBD;89,US,K011718MI,LYNX	1	PART	

ITEM	CONTENTS OF CHANGE	RVS	CHK	APV	M/D/Y

TOL ± RANGE	Pla	Met	Ins	Por	Cab	Pac	Gas	PCB
0-6	0.1	0.1	0.1	0.2	0.5	1	0.5	0.1
6-30	0.1	0.1	.15	.25	1	1	0.5	0.1
30-80	0.1	.15	0.2	0.3	2	1.5	1	0.1
80-180	.15	.15	.25	0.3	2	2	1	.15
180-315	.15	0.2	0.3	0.4	2.5	2	1	.15
315-800	0.2	0.3	0.4	0.5	3	3	2	.15

DATE	12-Nov-04	MATERIAL	SEE NOTES	TREATMENT	REMARK
UNIT	MM	SCALE	0.50	DRAWING NAME	HOUSING KIT;8965
DRAWN	DESIGNED	CHECKED	APPROVED	MATERIAL NO.	AD 451 6876 00001 R 00

MiTAC Technology Corp.

model name:8965-STRU

file name:HOUSING_KIT-8965

Reference Material

❖ Intel Pentium-M Processor Data Sheet	Intel, INC
❖ VIA PN800 North Bridge	VIA, INC
❖ VIA VT8235CE South Bridge	VIA, INC
❖ Keyboard controller W83L950D Data Sheet	WIN, INC
❖ 8965 Hardware Engineering Specification	*Technology Corp*/MITAC

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