SERVICE MANUAL FOR

8050D

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Mar.2004

MiTAC

8050D N/B Maintenance

Contents

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Contents

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1. Engineer Hardware Specification

1.1 Introduce

The MiTAC 8050D model is designed for Intel Banias processor with 400MHz FSB with Micro-FCPGA package. It can support Banias 1.5G ~ 1.9GHz/Dothan 2.0GHz and above.

This system is based on PCI architecture and is fully compatible with IBM PC/AT specification, which has standard hardware peripheral interface. The power management complies with Advanced Configuration and Power Interface (ACPI) 2.0. It also provides easy configuration through CMOS setup, which is built in system BIOS software and can be pop-up by pressing F2 key at system start up or warm reset. System also provides icon LEDs to display system status, such as AC Power indicator, Battery Power indicator, Battery status indicator, HDD,CD-ROM, NUM LOCK, CAP LOCK, SCROLL LOCK, RF on/off Card Reader indicator. It also equipped with LAN, 56K Fax MODEM, 3 USB port, S-Video and audio line in/out , external microphone function.

The memory subsystem supports two expansion DDR SDRAM slot with unbuffered PC1600/PC2100 DDR-SDRAM.

The Montara-GME GMCH Host Memory Controller integrates a high performance host interface for Intel Banias processor, a high performance 2D/3D Graphic Engine, a high performance memory controller, Digital Video port (DVOB & DVOC) interface, and Intel Hub interface Technology connecting with Intel 82801DBM ICH4-M.

The Intel ICH4-M integrates three Universal Serial Bus 2.0 Host Controllers Interface (UHCI), the Audio Controller with AC97 interface, the Ethernet includes a 32-bit PCI controller, the IDE Master/Slave controllers, and Intel Hub interface technology.

The MOBILITY M10 provides one of the fastest and most advanced 2D, 3D, and multimedia graphics performance for notebooks. It's architecture introduces the latest achievements in the graphics industry, which enable the use of the progressive new features in upcoming applications, but without compromising performance. ATIs support of support of DirectX® 9 features, highly optimized Open GL® support, and flexible memory configurations allow implementations targeted at the gaming enthusiast, consumer, business and workstation platforms.

The Realtek RTL8100C(L) is a highly integrated, cost-effective single-chip Fast Ethernet controller that provides 32-bit performance, PCI bus master capability, and full compliance with IEEE 802.3u 100Base-T specifications and IEEE 802.3x Full Duplex Flow Control. It also supports the Advanced Configuration Power management Interface (ACPI).

The VT6307L is a single chip PCI Host Controller for IEEE 1394-1995 Release 1.0 and IEEE 1394a P2000. It implements the Link and PHY layers for IEEE 1394-1995 High Performance Serial Bus specification release 1.0 and 1394a P2000. It is compliant with 1394 Open HCI 1.0 and 1.1 with DMA engine support for high performance data transfer via a 32-bit bus master PCEI host bus interface. The VT6307L supports 100, 200 and 400 Mbit/sec transmission via an integrated 2-port PHY. The VT6307L services two types of data packets: asynchronous and isochronous(real time). The 1394 link core performs arbitration requesting, packet generation and checking, and bus cycle master operations. It also has root node capability and performs retry operations.

The RICOH R5C592 CardBus/Media Reader controller functions as a single slot PCI to Cardbus bridge and also PCI interface smart card and MS/SD/MMC flash card reader. The R5C592 provide one Cardbus slot and all reader interface may operate simultaneously.

The CH7011A is a display controller device which accepts a digital graphics input signal, and encodes and

transmits data to a TV output (analog composite, s-video or RGB). The device accepts data over one 12-bit wide variable voltage data port which supports five different data format including RGB and YcrCb. The TV-Out processor will perform non-interlace to interlace conversion with scaling and flicker filters, and encode the data into any of the NTSC or PAL video standards. The scaling and flicker filter is adaptive and programmable to enable superior text display. Eight graphics resolutions are supported up to 1024 X 768 with full vertical and horizontal underscan capability in all modes. A high accuracy low jitter phase locked loop is integrated to create outstanding video quality. Support is provided for Macrovision and RGB bypass mode which enable driving a VGA CRT with the input data.

The W83L950D is a high performance micro-controller on-chip supporting functions optimized for embedded control. These include ROM, RAM, four types of timers, a serial communication interface, optional I²C bus interface, host interface, A/D converter, D/A converter, I/O ports, and other functions needed in control system configurations, so that compact, high performance systems can be implemented easily.

A full set of software drivers and utilities are available to allow advanced operating systems such as Windows ME, Windows 2000 and Windows XP to take full advantage of the hardware capabilities. Features such as bus mastering IDE, Plug and Play, Advanced Power Management (APM) with application restart, software-controlled power shutdown.

Following chapters will have more detail description for each individual sub-systems and functions.

1.2 System Overview

CPU	Mobile Pentium-M Processor 1.5G ~ 1.9GHz/Dothan 2.0GHz and above Thermal spec 35W TDP
Core logic	Intel 855GME + ICH4-M chipset
VGA Control	ATi M10
System BIOS	ST39SF040
Memory	DDR RAM : Apacer : 77.11021.460 Samsung 16*16 256MB 1st Apacer : 77.11021.580 Winbond 16*16 256MB 2nd A-DATA : 256MB
Video Memory	Share memory 32Mb
Clock Generator	ICS 950812
TV	ATi M10
IEEE1394	VT6307L
LAN	RTL8100C
PCMCIA + 4 IN 1 CARD	ENE CB710
Audio System	AC97 CODEC: Advance Logic, Inc, ALC655 Power Amplifier: TI TPA0212
Modem	AC97 Link: MDC (Mobile Daughter Card) Askey: V1456VQL-P1(INT)

1.3 System Hardware Parts

1.3.1 Intel Banias Processors in Micro-FCPGA Package

Intel Banias Processors with 478 pins Micro-FCPGA package.

The first Intel mobile processor with the Intel Net Burst micro-architecture which features include hyper-pipelined technology, a rapid execution engine, a 400MHz system, an execution trace cache, advanced dynamic execution, advanced transfer cache, enhanced floating point and multi-media unit, and Streaming SIMD Extensions 2 (SSE2).

The Streaming SIMD Extensions 2 (SSE2) enable break-through levels of performance in multimedia applications including 3-D graphics, video decoding/encoding, and speech recognition.

Use Source-Synchronous Transfer (SST) of address and data to improve performance by transferring data four times per bus clock.

Support Enhanced Intel Speed Step technology, which enables real-time dynamic switching of the voltage and frequency between two performance modes.

1.3.2 Clock Generator

System frequency synthesizer: ICS950812 Programmable output frequency, divider ratios, output rise/fall time, output skew. Programmable spread percentage for EMI control. Watchdog timer technology to reset system if

system malfunctions. Programmable watchdog safe frequency. Support I2C Index read/write and block read/write operations. Use external 14.318MHz crystal.

- Provides standard frequencies and additional 5% and 10% over-clocked frequencies
- Supports spread spectrum modulation: No spread, Center Spread (±0.35%, ±0.5%,or ±0.75%), or Down Spread (- 0.5%, -1.0%, or -1.5%)
- Offers adjustable PCI early clock via latch inputs
- Selectable 1X or 2X strength for REF via I2C interface
- Efficient power management scheme through PD#,CPU_STOP# and PCI_STOP#.
- Uses external 14.318MHz crystal
- Stop clocks and functional control available through

1.3.3 Montara-GME GMCH IGUI 3D Graphic DDR/SDR Chipset

Montara-GME GMCH IGUI Host Memory Controller integrates a high performance host interface for Intel Banias processor, a high performance 2D/3D Graphic Engine, a high performance memory controller, an AGP 4Xinterface, and Intel®' I/O Hub architecture INTEL 82801DBM ICH4-M

Montara-GME GMCH Host Interface features the AGTL & AGTL+ compliant bus driver technology with integrated on-die termination to support Intel Banias processors. Montara-GME GMCH provides a 12-deep In

-Order-Queue to support maximum outstanding transactions up to 12. It integrated a high performance 2D/3D Graphic Engine, Video Accelerator and Advanced Hardware Acceleration MPEGI/MPEGII Video Decoder for the Intel Banias series based PC systems. It also integrates a high performance 2.1GB/s DDR266 Memory controller to sustain the bandwidth demand from the integrated GUI or external AGP master, host processor, as well as the multi I/O masters. In addition to integrated GUI, Montara-GME GMCH also can support external AGP slot with AGP 1X/2X/4X capability and Fast Write Transactions. A high bandwidth and mature Intel®' I/O Hub architecture is incorporated to connect Montara-GME GMCH and INTEL 82801DBM ICH4-M together. Intel®' I/O Hub architecture is developed into three layers, the Multi-threaded I/O Link Layer delivering 1.2GB bandwidth to connect embedded DMA Master devices and external PCI masters to interface to Multi-threaded I/O Link layer, the Multi-threaded I/O Link Encoder/Decoder in INTEL 82801DBM ICH4-M to transfer data w/ 533 MB/s bandwidth from/to Multi-threaded I/O Link layer to/from Montara-GME GMCH, and the Multi-threaded I/O Link Encoder/Decoder in Montara-GME GMCH to transfer data w/ 533 MB/s from/to Multi-threaded I/O Link layer to/from INTEL 82801DBM ICH4-M.

An Unified Memory Controller supporting DDR266 DRAM is incorporated, delivering a high performance data transfer to/from memory subsystem from/to the Host processor, the integrated graphic engine or external AGP master, or the I/O bus masters. The memory controller also supports the Suspend to RAM function by retaining the CKE# pins asserted in ACPI S3 state in which only AUX source deliver power. The Montara-GME GMCH adopts the Shared Memory Architecture, eliminating the need and thus the cost of the frame buffer memory by organizing the frame buffer in the system memory. The frame buffer size can be allocated from 8MB to 64MB.

Features

❑ Processor/Host Bus Support

- Intel® Banias processor
- 2X Address, 4X data
- Support host bus Dynamic Bus Inversion (DBI)
- Supports system bus at 400MT/s (100 MHz)
- Supports 64-bit host bus addressing
- 8-deep In-Order-Queue
- AGTL+ bus driver technology with integrated GTL termination resistors and low voltage operation (1.05V)
- Supports Enhanced Intel® Speed Step TM Technology (EIST) and Geyserville III
- Support for DPWR# signal to Banias processor for PSB power management

❑ Memory System

- Directly supports one DDR channel, 64-bits wide (72-b with ECC).
- Supports 200-MHz and 266-MHz DDR devices with max of 2 Double-Sided SO-DIMMs(4 rows populated) with unbuffered PC1600/PC2100 DDR(with ECC).
- Supports 128-Mb, 256-Mb and 512-Mbit technologies providing maximum capacity of 1-GB with only x

16 devices.

- All supported devices have 4 banks.
- Supports up to 16 simultaneous open pages.
- Supports page sizes of 2KB, 4KB, 8KB, and 16KB. Page size is individually selected for every row.
- UMA support only.

System Interrupt

- Supports 8259 and Processor System Bus interrupt delivery mechanism
- Supports interrupts signaled as upstream Memory Writes from PCI and Hub interface
- MSI sent to the CPU through the system Bus
- From IOxAPIC in ICH4-M
- Provides redirection for upstream interrupts to the System Bus
- Video Stream Decoder
- Improved HW Motion Compensation for MPEG2All format decoder (18 ATSC formats) supported
- Dynamic Bob and Weave support for Video Streams
- Software DVD at 60 fields/second and 30 frames/second full screen
- Support for 720x480 pixel resolution DVD quality encoding at low CPU utilization

- Video Overlay
- Single high quality scalable overlay and second Sprite to support second overlay
- Multiple overay functionality provided via Arithmetic Stretch Blt
- Direct YUV from Overlay to TV-out
- Independent Gamma Correction
- Independent Brightness / Contrast / Saturation
- Independent Tint / Hue support
- Destination Color keying
- Source Chromakeying
- Maximum source resolution of 1920x1080 pixels
- Maximum overlay clock of 133 MHz/200 MHz provides a pixel resolution up to 1600x1200@ 60Hz or 1280x1024@ 85 Hz

❑ Display

- Analog Display Support 350 MHz integrated 24-bit RAMDAC that can drive a standard progressive scan analog monitor up to 1800x1350 @ 85 Hz accompanying I2C and DDC channels provided through multiplexed interface hot plug and display support
- Dual independent pipe with single display support Simultaneous: Same images and native display timings on

each display device

- DVO (DVOB) support
- Digital video out port DVOB with 165-MHz dot clock on 12-bit interface
  - ✓ Variety of DVO devices channel
  - ✓ Compliant with DVI Specification 1.0, thereby providing support for a flat panel up to 2048x1536 pixel resolution, or digital CRT up to 1920x1080 pixel resolution

1.3.4 I/O Controller Hub : INTEL 82801DBM

The INTEL 82801DBM ICH4-M integrates three Universal Serial Bus 2.0 Host Controllers, the Audio Controller with AC 97 Interface, the IDE Master/Slave controllers, and Intel®' I/O Hub architecture. The PCI to LPC Bridge, I/O Advanced Programmable Interrupt Controller, legacy system I/O and legacy power management functionalities are integrated as well.

The integrated Universal Serial Bus Host Controllers features Dual Independent UHCI Compliant Host controllers with six USB ports delivering 480 Mb/s bandwidth and rich connectivity. Besides, Legacy USB devices as well as over current detection are also implemented.

The Integrated AC97 v2.3 compliance Audio Controller that features a 7-channels of audio speaker out and HSP v.90 modem support. Additionally, the AC97 interface supports 4 separate SDATAIN pins that is capable of supporting multiple audio codecs with one separate modem codec.

The integrated IDE Master/Slave controllers features Dual Independent IDE channels supporting PIO mode transfers up to 16 Mbytes/sec and Ultra DMA 33/66/100. It provides two separate data paths for the dual IDE channels that sustain the high data transfer rate in the multitasking environment.

INTEL 82801DBM ICH4-M supports 6 PCI masters and complies with PCI 2.2 specification. It also incorporates the legacy system I/O like: two 82C37 compatible DMA controllers, Channels 0-3 are hardwired to 8 bit, three 8254 compatible programmable 16-bit counters channels 5-7, hardwired keyboard controller and PS2 mouse interface(not use in MiTAC 8050 model), Real Time clock with 512Bytes CMOS SRAM and two 82C59 compatible Interrupt controllers. Besides, the I/O APIC managing up to 14 interrupts with both Serial and FSB interrupt delivery modes is supported.

The integrated power management module incorporates the ACPI 1.0b compliance functions, the APM 1.2 compliance functions, and the PCI bus power management interface spec. v1.1. Numerous power-up events and power down events are also supported. 21 general purposed I/O pins are provided to give an easy to use logic for specific application. In addition, the INTEL 82801DBM ICH4-M supports Deeper Sleep power state for Intel Mobile processor.

A high bandwidth and mature Intel®' I/O Hub architecture is incorporated to connect Montara and Intel 82801DBM ICH4-M Hub interface together. Intel®' I/O Hub architecture is developed

1.3.5 VGA Control

- **Introducing MOBILITY M10**

The MOBILITY M10 provides one of the fastest and most advanced 2D, 3D, and multimedia graphics performance for notebooks. Its architecture introduces the latest achievements in the graphics industry, which enable the use of the progressive new features in upcoming applications, but without compromising performance. ATI's support of DirectX® 9 features, highly optimized OpenGL® support, and flexible memory configurations allow implementations targeted at the gaming enthusiast, consumer, business and workstation platforms.

❑ SMARTSHADER™ 2.0 — Advanced Shader Technology

- Provides complete hardware-accelerated support for the new DirectX® 9 programmable shader model, enabling more complex and realistic texture and lighting effects than ever before.
- Significant improvement over first-generation shaders introduced in DirectX® 8, with a much more powerful and intuitive instruction set.
- Offers full support for this feature in OpenGL® applications.

❑ MOOTHVISION™ 2.0 — Flexible Anti-Aliasing and Anisotropic Filtering

- 2x/4x/6x full-scene anti-aliasing modes
- Adaptive algorithm with programmable sample patterns
- 2x/4x/8x/16x anisotropic filtering modes
- Adaptive algorithm with bi-linear (performance) and tri-linear (quality) options

❑ High Performance Memory Support

- ➢ Incorporates support for DDR SDRAM/SGRAM.
- ➢ Features key items from ATI's third generation HYPER Z™ III technology that conserves memory bandwidth for improved performance in demanding applications.

❑ Dual Display Support

- ➢ Leading-edge technology, fully optimized with HYDRA VISION™, flexibly supports multiple combinations of notebook LCD, traditional CRT monitors, flat panel displays and TV.
- ➢ Features Dual Channel DVI support.
- ➢ 230MHz LVDS transmitter supports LCD panels up to QXGA (2048x1536) resolution.
- ➢ Integrated 165MHz TMDS transmitter supports external flat panels up to UXGA (1600x1200) resolution.
- ➢ High performance DAC speeds of 400MHz.

Features in Detail

❑ VIDEO Acceleration

- ➢ M10 allows the integration of industry leading digital video features, including advanced de-interlacing algorithms for unprecedented video quality and integrated digital TV decode capability. Includes programmable,independent gamma control for the video overlay.
- ➢ New FULLSTREAM™ technology removes blocky artifacts from streaming and Internet video and

provides sharper image quality.

- Integrated general purpose xDCT engine (capable of performing both forward and inverse discrete cosine transform) and motion compensation (MC) support for the acceleration of MPEG encoding and decoding as well as DV (digital video) encoding and decoding.

1.3.6 CardBus: CB710

Features

- 3.3V operation with 5V tolerant
- 208-pin LQFP / 209-ball LFBGA package for CB710
- 328-ball LFBGA package for CB720
- PCI Interface compliant with
  - ✓ PCI Local Bus Specification, Revision 2.2
  - ✓ PCI Bus Power Management Interface Specification, Revision 1.1
  - ✓ PCI Mobile Design Guide, Version 1.1
  - ✓ Advanced Configuration and Power Interface Specification, Revision 1.0
  - ✓ CardBus Interface
  - ✓ Compliant with PC Card Standard 8.0Support Standardized Zoomed Video Register Model

- ✓ Support CardBay PC card interface
- ✓ Smart Card Interface
- ✓ Compliant with PC/SC Specification 1.0
- ✓ Support ISO7816 T=0 and T=1 asynchronous communication protocols
- ✓ Two power enable pins to support 5V and 3V smart cards
- ✓ Support programmable card clock frequencies
- ✓ Programmable F and D parameters to support different data rates
- ✓ One traffic LED pin.
- ✓ Secure Digital Interface
- ✓ Compliant with SD Memory Card Specification Version 1.0
- ✓ Support 4 parallel data lines
- ✓ Has an optional reference clock source to control the operating clock frequency of SD card
- ✓ Up to 10MByte/sec Read/Write rate when the optional reference clock source is used
- ✓ Contains 16 Bytes of data buffer to regulate the data flow between PCI interface and the SD card interface
- ✓ Support Write Protect Switch
- ✓ Support Card Detect either by DAT3 or by dedicated Card Detect Switch
- ✓ One Traffic LED pin

- ✓ One power enable pin.
- ✓ Memory Stick Interface
- ✓ Compliant with Memory Stick Standard Format Specification Version 1.3
- ✓ Has an optional reference clock source to control the operating clock frequency of Memory Stick
- ✓ Up to 2.5MByte/sec Read/Write rate when the optional reference clock source is used
- ✓ Stick interface
- ✓ One Traffic LED pin
- ✓ One power enable pin
  - ❖ Smart Media Interface
- ✓ One traffic LED pin
  - ❖ Interrupt configuration
- ✓ Supports CLKRUN# protocol
- ✓ Supports SUSPEND#
- ✓ Supports D3STATE#
  - ❖ Supports Zoomed Video port.
  - ❖ Power Switch Interface
  - ❖ Misc Control Logic

- ✓ Supports socket activity LED
- ✓ Supports 12 GPIOs and GPE#
- ✓ Supports PCI LOCK

1.3.7 AC'97 AUDIO SYSTEM: Advance Logic, Inc, ALC655

The ALC655 is a 16-bit, full duplex AC'97 2.3 compatible six channels audio CODEC designed for PC multimedia systems,including host/soft audio and AMR/CNR based designs. The ALC655 incorporates proprietary converter technology to meet performance requirements on PC99/2001 systems. The ALC655 CODEC provides three pairs of stereo outputs with 5-Bitvolume controls, a mono output, and multiple stereo and mono inputs, along with flexible mixing, gain and mute functions to provide a complete integrated audio solution for PCs. The digital interface circuitry of the ALC655 CODEC operates from a 3.3V power supply for use in notebook and PC applications. The ALC655 integrates 50mW/20ohm headset audio amplifiers at Front-Out and Surr-Out, built-in 14.318M 24.576MHz PLL and PCBEEP generator, those can save BOM costs. The ALC655also supports the S/PDIF input and output function, which can offer easy connection of PCs to consumer electronic products, such as AC3 decoder/speaker and mini disk devices. ALC655 supports host/soft audio from Intel ICHx chipsets as well as audio controller based VIA/SIS/ALI/AMD/nVIDIA/ATI chipset. Bundled Windows series drivers (Win XP/ME/2000/98/NT), EAX/Direct Sound 3D/ I3DL2/ A3D compatible sound effect utilities (supporting Karaoke, 26-kind of environment sound emulation,10-band equalizer), HRTF 3D positional audio and Sensaura™ 3D (optional) provide an excellent entertainment package and game experience for PC users. Besides, ALC655 includes Realtek's impedance sensing techniques that makes device load on outputs and inputs can be detected.

8050D N/B Maintenance

- Meets performance requirements for audio on PC99/2001 systems
- Meets Microsoft WHQL/WLP 2.0 audio requirements
- 16-bit Stereo full-duplex CODEC with 48KHz sampling rate
- Compliant with AC'97 2.3 specifications
  - ✓ 14.318MHz- 24.576MHz PLL to save crystal
  - ✓ 12.288MHz BITCLK input can be consumed
  - ✓ Integrated PCBEEP generator to save buzzer
  - ✓ Interrupt capability
- Three analog line-level stereo inputs with 5-bit volume control: LINE_IN, CD, AUX
- High quality differential CD input
- Two analog line-level mono input: PCBEEP,PHONE-IN
- Two software selectable MIC inputs applications (software selectable)
- Boost preamplifier for MIC input
- 50mW/20 amplifier
- External Amplifier Power Down (EAPD) capability
- Power management and enhanced power saving features.
- Stereo MIC record for AEC/BF application

- Supports Power Off CD function
- Adjustable VREFOUT control Supports double sampling rate (96KHz) of DVD audio playback
- Support 48KHz of S/PDIF output is compliant with AC'97 rev2.3 specification
- Power support: Digital: 3.3V; Analog: 3.3V/5V

1.3.8 MDC:PCTEL MODEM DAUGHTER CARD PCT2303W (ASKEY V1456VQL-P1)

The PCT2303W chipset is designed to meet the demand of this emerging worldwide AMR/MDC market. The combination of PC-TEL's well proven PCT2303W chipset and the HSP56TM MR software modem driver allows systems manufactures to implement modem functions in PCs at a lower bill of materials (BOM) while maintaining higher system performance.

PC-TEL has streamlined the traditional modem into the Host Signal Processing (HSP) solution. Operating with the Pentium class processors, HSP becomes part of the host computer's system software. It requires less power to operate and less physical space than standard modem solutions. PC-TEL's HSP modem is an easily integrated, cost-effective communications solution that is flexible enough to carry you into the future.

The PCT2303W chip set is an integrated direct access arrangement (DAA) and Codec that provides a programmable line interface to meet international telephone line requirements. The PCT2303W chip set is available in two 16-pin small outline packages (AC'97 interface on PCT303A and phone-line interface on PCT303W). The chip set eliminates the need for an AFE, an isolation transformer, relays, opto-isolators, and 2-to

4-wire hybrid. The PCT2303W chip set dramatically reduces the number of discrete components and cost required to achieve compliance with international regulatory requirements. The PCT2303W complies with AC'97 Interface specification Rev. 2.1.

The chip set is fully programmable to meet world-wide telephone line interface requirements including those described by CTR21, NET4, JATE, FCC, and various country-specific PTT specifications. The programmable parameters of the PCT2303W chip set include AC termination, DC termination, ringer impedance, and ringer threshold. The PCT2303W chip set has been designed to meet stringent world-wide requirements for out-of-band energy, billing-tone immunity, lightning surges, and safety requirements.

❑ Features

- Virtual com port with a DTE throughout up to 460.8Kbps.
- G3 Fax compatible
- Auto dial and auto answer
- Ring detection
- Codec/DAA Features
- AC97 2.1 compliant
- 86dB dynamic range TX/RX paths
- 2-4-wire hybrid
- Integrated ring detector

- High voltage isolation of 4000V
- Support for “Caller ID”
- Compliant with FCC Part68, CTR21, Net4 and JATE
- Low power standby
- Low profile SOIC package 16 pins 10x3x1.55mm
- Low power consumption
- 10mA @ 3.3V operation
- 1mA @ 3.3V power down
- Integrated modem codec

❑ Standard Features

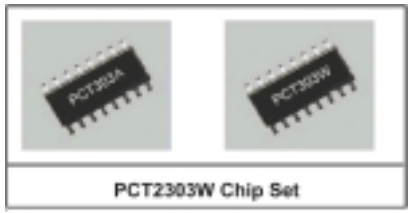
➢ Data

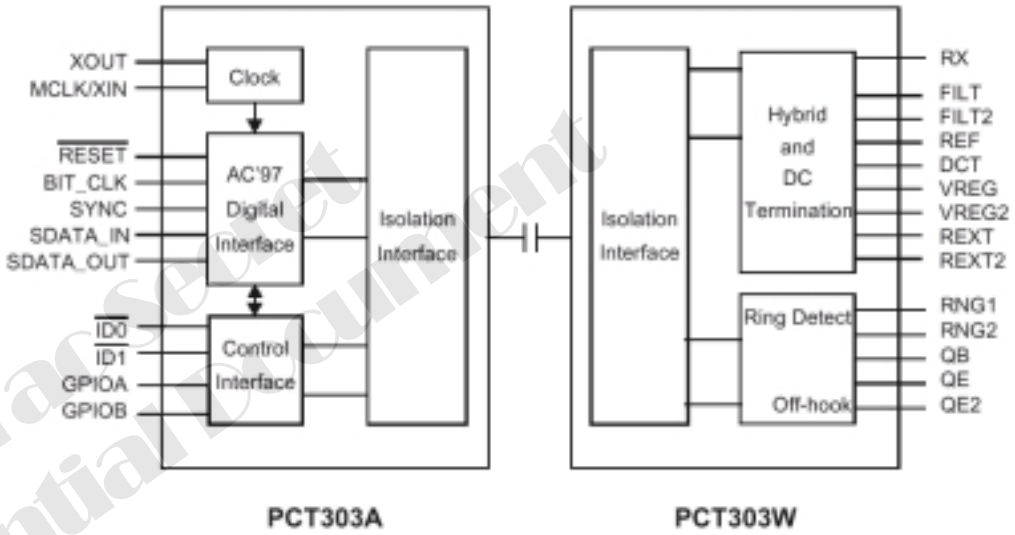
ITU-T V.90 (56Kbps), V.34 (4.8Kbps TO 33.6 Kbps), V.32 bits (4.8Kbps to 14.4Kbps), V.22 bits (1.2 bps to 2.4 Kbps), V.21 and Bell 103 and 212A(300 to 1200 bps) modulation protocol.

- ✓ **Data Compression** ITU-T V.42bis MNP Class 5
- ✓ **Error Correction** ITU-T V.42 LAPM MNP 2-4

- **Fax**

ITU-T V. 17, V.29, V.27ter, V.21, Channel 2, Group 3, EIA Class I





1.3.9 IEEE1394 VT6307L (Option)

1.3.9.1 Overview

The VT6307 IEEE 1394 OHCI Host Controller provides high performance serial connectivity. It implements the Link and Phy layers for IEEE 1394-1995 High Performance Serial Bus specification release 1.0 and 1394a-2000. It is compliant with 1394 Open HCI 1.0 and 1.1 with DMA engine support for high performance data transfer via a 32-bit bus master PCI host bus interface. The VT6307 supports 100, 200 and 400 M bit/sec transmission via an

integrated 2-port PHY. The VT6307 services two types of data packets: asynchronous and isochronous (real time). The 1394 link core performs arbitration requesting, packet generation and checking, and bus cycle master operations. It also has root node capability and performs retry operations. The VT6307 is ready to provide industry-standard IEEE 1394 peripheral connections for desktop and mobile PC platforms. Support for the VT6307 is built into Microsoft Windows 98, Windows ME, Windows 2000, and Windows XP.

1.3.9.2 Features

- 32 bit CRC generator and checker for receive and transmit data
- On-chip isochronous and asynchronous receive and transmit FIFOs for packets (2K for general receive plus 2K for isochronous transmit plus 2K for asynchronous transmit)
- 8 isochronous transmit contexts
- 4 isochronous receive context
- 3-deep physical post-write queue
- 2-deep physical response queue
- Dual buffer mode enhancements
- Skip Processing enhancements
- Block Read Request handling
- Ack_tardy processing

1.3.10 System Flash Memory (BIOS)

- **Firmware Hub for Intel® 810, 810E, 815, 815E,815EP, 820, 840, 850 Chipsets**
- **Flexible Erase Capability**
  - Uniform 4 K Byte Sectors
  - Uniform 16 K Byte overlay blocks for SST49LF002A
  - Uniform 64 K Byte overlay blocks for SST49LF004ATop boot block protection
  - 16 K Byte for SST49LF002A
  - 64 K Byte for SST49LF004A
  - Chip-Erase for PP Mode
- **Single 3.0-3.6V Read and Write Operations**
- **Superior Reliability**
- **Firmware Hub Hardware Interface Mode**
  - 5-signal communication interface supporting byte Read and Write
  - 33 MHz clock frequency operation
  - WP# and TBL# pins provide hardware write protect for entire chip and/or top Boot Block

- Block Locking Register for all blocks
- Standard SDP Command Set
- Data# Polling and Toggle Bit for End-of-Write detection
- 5 GPI pins for system design flexibility
- 4 ID pins for multi-chip selection

1.3.11 Memory System

1.3.11.1 64MB, 128MB, 256MB, 512MB (x64) 200-Pin DDR SDRAM SODIMM

- JEDEC-standard 200-pin, small-outline, dual in-line memory module (SODIMM)
- Utilizes 200 Mb/s and 266 Mb/s DDR SDRAM components
- 64MB (8 Meg x 64 [H]); 128MB (16 Meg x 64, [H] and [HD]); 256MB (32 Meg x 64 [HD]); 512MB (64 Meg x 64 [HD])
- VDD= VDDQ= +2.5V ±0.2V
- VDDSPD = +2.2V to +5.5V
- 2.5V I/O (SSTL_2 compatible)
- Commands entered on each positive CK edge

- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Bidirectional data strobe (DQS) transmitted/received with data—i.e.,source-synchronous data capture
- Differential clock inputs (CK and CK# - can be multiple clocks, CK0/CK0#, CK1/CK1#, etc.)
- Four internal device banks for concurrent operation
- Selectable burst lengths: 2, 4, or 8
- Auto precharge option
- Auto Refresh and Self Refresh Modes
- 15.6µs (MT4VDDT864H, MT8VDDT1664HD), 7.8125µs (MT4VDDT1664H, MT8VDDT3264HD, MT8VDDT6464HD) maximum average periodic refresh interval
- Serial Presence Detect (SPD) with EEPROM
- Fast data transfer rates PC2100 or PC1600
- Selectable READ CAS latency for maximum compatibility
- Gold-plated edge contacts

1.3.12 PHY: 3.3-V 10Base-T/100Base-TX Integrated PHY Ceiver ,The ICS1893 is a low-power, physical-layer device (PHY)

General

The Realtek RTL8100C(L) is a highly integrated, cost-effective single-chip Fast Ethernet controller that provides 32-bit performance, PCI bus master capability, and full compliance with IEEE 802.3u 100Base-T specifications and IEEE 802.3x Full Duplex Flow Control. It also supports the Advanced Configuration Power management Interface (ACPI), PCI power management for modern operating systems that are capable of Operating System Directed Power Management (OSPM) to achieve the most efficient power management possible. The RTL8100C(L) does not support CardBus mode as the RTL8139C does. In addition to the ACPI feature, the RTL8100C(L) also supports remote wake-up(including AMD Magic Packet, LinkChg, and Microsoft® wake-up frame) in both ACPI and APM environments. The RTL8100C(L) is capable of performing an internal reset through the application of auxiliary power. When auxiliary power is applied and the main power remains off, the RTL8100C(L) is ready and waiting for the Magic Packet or Link Change to wake the system up. Also, the LWAKE pin provides 4 different output signals including active high, active low, positive pulse, and negative pulse. The versatility of the RTL8100C(L) LWAKE pin provides motherboards with Wake-On-LAN (WOL) functionality. The RTL8100C(L) also supports Analog Auto-Power-down, that is, the analog part of the RTL8100C(L) can be shut down temporarily according to user requirements or when the RTL8100C(L) is in a power down state with the wakeup function disabled. In addition, when the analog part is shut down and the Isolate B pin is low (i.e. the main power is off), then both the analog and digital parts stop functioning and the power consumption of the RTL8100C(L) will be negligible. The RTL8100C(L) also supports an auxiliary power auto-detect function, and will auto-configure related bits of their own PCI power management registers in PCI configuration space.

- 128 pin QFP/LQFP
- Integrated Fast Ethernet MAC, Physical chip and transceiver in one chip
- 10 Mb/s and 100 Mb/s operation
- Supports 10 Mb/s and 100 Mb/s N-way Auto-negotiation operation
- PCI local bus single-chip Fast Ethernet controller
  - ✓ Compliant to PCI Revision 2.2
  - ✓ Supports PCI clock 16.75MHz-40MHz
  - ✓ Supports PCI target fast back-to-back transaction
  - ✓ Provides PCI bus master data transfers and PCI memory space or I/O space mapped data transfers of RTL8100C(L)'s operational registers
  - ✓ Supports PCI VPD (Vital Product Data)
  - ✓ Supports ACPI, PCI power management
- Supports 25MHz crystal or 25MHz OSC as the internal clock source.
- The frequency deviation of either crystal or OSC must be within 50 PPM.
- Compliant to PC99/PC2001 standard
- Supports Wake-On-LAN function and remote wake-up (Magic Packet*, LinkChg and Microsoft® wake-up frame)

- Supports 4 Wake-On-LAN (WOL) signals (active high, active low, positive pulse, and negative pulse)
- Supports auxiliary power-on internal reset, to be ready for remote wake-up when main power still remains off
- Supports auxiliary power auto-detect, and sets the related capability of power management registers in PCI configuration space.
- Includes a programmable, PCI burst size and early Tx/Rx threshold.
- Supports a 32-bit general-purpose timer with the external PCI clock as clock source, to generate timer-interrupt
- Contains two large (2Kbyte) independent receive and transmit FIFOs
- Advanced power saving mode when LAN function or wakeup function is not used
- Uses 93C46 (64*16-bit EEPROM) to store resource configuration, ID parameter, and VPD data.
- Supports LED pins for various network activity indications
- Supports loop back capability
- Half/Full duplex capability
- Supports Full Duplex Flow Control (IEEE 802.3x)

1.3.13 Keyboard System: Winbond W83L950D

The Winbond Keyboard controller architecture consists of a Turbo 51 core controller surrounded by various registers, nine general purpose I/O port, 2k+256 bytes of RAM, four timer/counters, dual serial ports, 40K MTP-ROM that is divided into four banks, two SMBus interface for master and slave, Support 4 PWM channels, 2 D-A and 8 A-D converters. 2

- 8051 uC based
- Keyboard Controller Embedded Controller
- Supply embedded programmable flash memory (internal ROM size: 40KB) and RAM size is 2 KB.
- Support 4 Timer (8 bit) signal with 3 prescalers.
- Support 2 PWM channels, 2 D-A and 8 A-D converters.
- Reduce Firmware burden by Hardware PS/2 decoding
- Support 72 useful GPIOs totally
- Support Flash utility for on board re-flash
- Support ACPI
- Hardware fast Gate A20 with software programmable

1.4 Other Functions

1.4.1 Hot Key Function

Keys Combination	Feature	Meaning
Fn + F1	Power down	Mini PCI power down
Fn + F2	Reserve	
Fn + F3	Volume Down	
Fn + F4	Volume Up	
Fn + F5	LCD/external CRT switching	Rotate display mode in LCD only, CRT only, and simultaneously display.
Fn + F6	Brightness down	Decreases the LCD brightness
Fn + F7	Brightness up	Increases the LCD brightness
Fn + F10	Battery Low Beep	On/Off Battery Low Beep
Fn + F11	Panel Off/On	Toggle Panel on/off
Fn + F12	Suspend to DRAM / HDD	Force the computer into either Suspend to HDD or Suspend to DRAM mode depending on BIOS Setup.

1.4.2 Power on/off/suspend/resume button

- **APM mode**

  At APM mode, Power button is on/off system power.

- **ACPI mode**

  At ACPI mode. Windows power management control panel set power button behavior.You could set "standby", "power off" or "hibernate"(must enable hibernate function in power Management) to power button function.

  Continue pushing power button over 4 seconds will force system off at ACPI mode.

1.4.3 Cover Switch

System automatically provides power saving by monitoring Cover Switch. It will save battery power and prolong the usage time when user closes the notebook cover.

At ACPI mode there are four functions to be chosen at windows power management control panel.

- None
- Standby

- Off
- Hibernate (must enable hibernate function in power management)

1.4.4 LED Indicators

- **Three LED indicators at front side:**

From left to right that indicate BATTERY POWER, BATTERY STATUS and AC POWER

- AC POWER:

This LED lights green when the notebook was powered by AC power line, Flashes (on 1 second, off 1 second) when entered suspend to RAM state with AC powered. The LED is off when the notebook is in power off state or powered by battery.

- BATTERY POWER:

This LED lights green when the notebook is being powered by Battery, and flashes (on 1 second, off 1 second) when entered suspend to RAM state with AC powered. The LED is off when the notebook is in power off state or powered by AC adapter.

- BATTERY STATUS:

During normal operation, this LED stays off as long as the battery is charged. When the battery charge drops to 10% of capacity, the LED lights red, flashes per 1 second and beeps per 2 second. When AC is connected, this indicator glows green if the battery pack is fully charged or orange (amber) if the battery is being charged.

- ✓ *AC POWER*:

This LED lights green when AC is powering the notebook, and flash (on 1 second, off 1 second) when Suspend to RAM no matter using AC power or Battery power. The LED is off when the notebook is off or powered by battery.

- ✓ *BATTERY POWER:*

This LED lights green when the notebook is being powered by Battery, and flash (on 1 second, off 1 second) when Battery is low. The LED is off when the notebook is off or powered by AC adaptor.

❑ Seven LED indicators:

System has seven status LED indicators at front side which to display system activity. From left to right that indicate HARD DISK, CD-ROM, NUM LOCK, CAPS LOCK, SCROLL LOCK, Mini PCI and Card Reader.

1.4.5 Battery status

❑ Battery Warning

- System also provides Battery capacity monitoring and gives users a warning signal to alarm they to store data before battery dead. This function also protects system from mal-function while battery capacity is low.
- Battery Warning: Capacity below 10%, Battery Capacity LED flashes per second, system beeps per 2 seconds.
- System will Suspend to HDD after 2 Minutes to protect users data.

❑ Battery Low State

- After Battery Warning State, and battery capacity is below 5%, system will generate beep sound for twice per second.

❑ Battery Dead State

- When the battery voltage level reaches 11.5 volts, system will shut down automatically in order to extend the battery packs' life.

1.4.6 Fan power on/off management

FAN is controlled by W83L950D embedded controller-using ADT7460 to sense CPU temperature and PWM control fan speed. Fan speed is depended on CPU temperature. Higher CPU temperature faster Fan Speed.

1.4.7 CMOS Battery

CR2032 3V 220mAh lithium battery When AC in or system main battery inside, CMOS battery will consume no power AC or main battery not exists, CMOS battery life at less (220mAh/5.8uA) 4 years.

1.4.8 I/O Port

- One Power Supply Jack.
- One External CRT Connector For CRT Display
- Supports three USB port for all USB devices.
- One MODEM RJ-11 phone jack for PSTN line
- One RJ-45 for LAN.
- One IEEE1394 port

- Headphone Out Jack.
- Microphone Input Jack.
- Line in Jack

1.4.9 Battery current limit and learning.

Implanted H/W current limit and battery learning circuit to enhance protection of battery.

1.5 Power management

The 8050D system has built in several power saving modes to prolong the battery usage for mobile purpose. User can enable and configure different degrees of power management modes via ROM CMOS setup (booting by pressing F2 key). Following are the descriptions of the power management modes supported.

1.5.1 System Management Mode

- **Full on mode**

In this mode, each device is running with the maximal speed. CPU clock is up to its maximum.

❑ Doze Mode

In this mode, CPU will be toggling between on & stop grant mode either. The technology is clock throttling. This can save battery power without loosing much computing capability.

The CPU power consumption and temperature is lower in this mode.

❑ Standby mode

For more power saving, it turns of the peripheral components. In this mode, the following is the status of each device:

-- CPU: Stop grant
-- LCD: backlight off
-- HDD: spin down

❑ Suspend to DRAM

The most chipset of the system is entering power down mode for more power saving. In this mode, the following is the status of each device:

- Suspend to DRAM
  - ✓ CPU: off
  - ✓ Intel 855GME: Partial off

- ✓ VGA: Suspend
- ✓ PCMCIA: Suspend
- ✓ Audio: off
- ✓ SDRAM: self refresh

➢ Suspend to HDD

- ✓ All devices are stopped clock and power-down
- ✓ System status is saved in HDD
- ✓ All system status will be restored when powered on again

1.5.2 Other power management functions

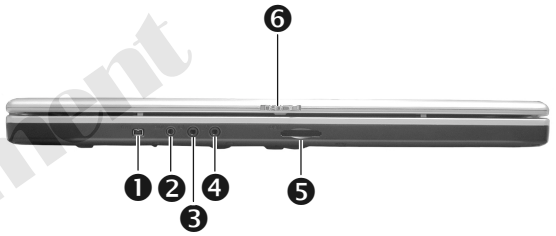
❑ HDD & Video access

System has the ability to monitor video and hard disk activity. User can enable monitoring function for video and/or hard disk individually. When there is no video and/or hard disk activity, system will enter next PMU state depending on the application. When the VGA activity monitoring is enabled, the performance of the system will have some impact.

2. System View and Disassembly

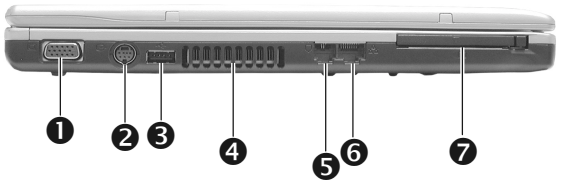
2.1 System View

2.1.1 Front View



❶ 1394 Jack
❷ Line Out Connector
❸ Line In Connector
❹ MIC In Connector
❺ SD Card Slot
❻ Top Cover Latch

2.1.2 Left-side View



❶ VGA Port
❷ S-Video Port
❸ USB Ports *1
❹ Ventilation Openings
❺ RJ-11 Connector
❻ RJ-45 Connector
❼ PCMCIA Card Socket

2.1.3 Right-side View

❶ CD-ROM/DVD-ROM Drive

❷ Kensington Lock

2.1.4 Rear View

❶ Kensington Lock

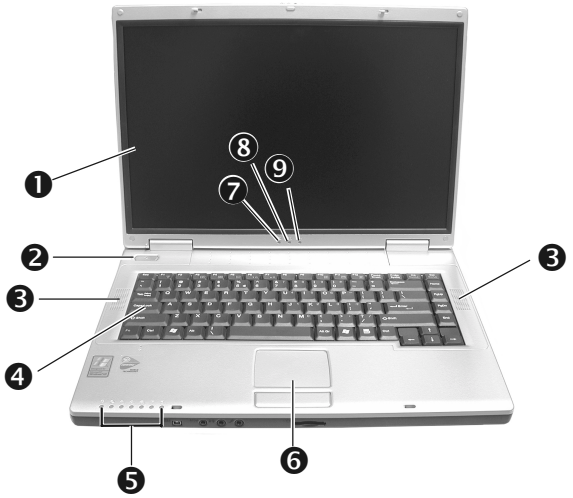
❷ Power Connector

❸ USB Port*2

2.1.5 Bottom View

❶ Hard Disk Drive
❷ DDR SDRAM Card
❸ Wireless Card
❹ CPU
❺ Battery Park
❻ Stereo Speaker Set

2.1.6 Top-open View

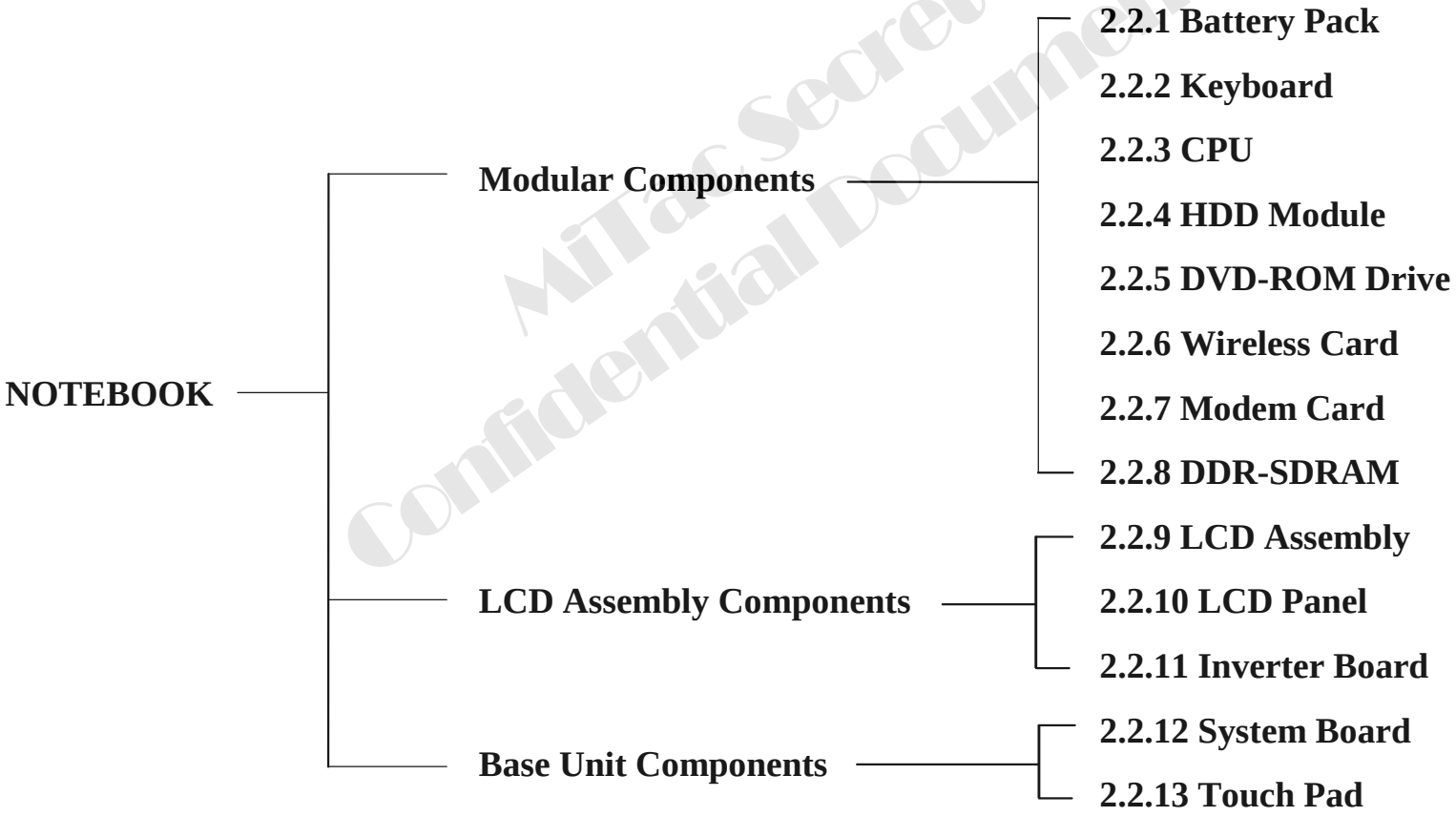


❶ LCD Screen
❷ Power Button
❸ Stereo Speaker Set
❹ Keyboard
❺ Device LED Indicators
❻ Touch Pad
❼ Hard Disk Drive Indicator
❽ Battery Power Charging Indicator
❾ Power Indicator

2.2 System Disassembly

The section discusses at length each major component for disassembly/reassembly and show corresponding illustrations.Use the chart below to determine the disassembly sequence for removing components from the notebook.

NOTE: *Before you start to install/replace these modules, disconnect all peripheral devices and make sure the notebook is not turned on or connected to AC power.*



2.2.1 Battery Pack

Disassembly

1. Carefully put the notebook upside down.
2. Slide the two release lever outwards to the "unlock" ( ) position (❶), while take the battery pack out of the compartment (❷). (Figure 2-1)

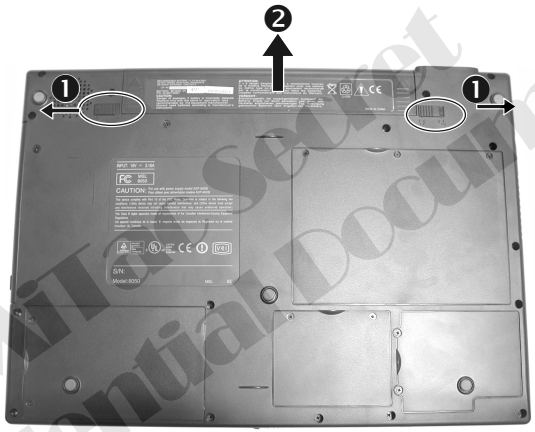


Figure 2-1 Remove the battery pack

Reassembly

1. Replace the battery pack into the compartment. The battery pack should be correctly connected when you hear a clicking sound.
2. Slide the release lever to the "lock" ( ) position.

2.2.2 Keyboard

Disassembly

1. Remove the battery pack. (Refer to section 2.2.1 Disassembly)
2. Open the top cover.
3. Loosen the four latches locking the keyboard. (Figure 2-2)
4. Slightly lift up the keyboard and disconnect the cable from the mother board, then separate the keyboard. (Figure 2-3)

Figure 2-2 Loosen the four latches

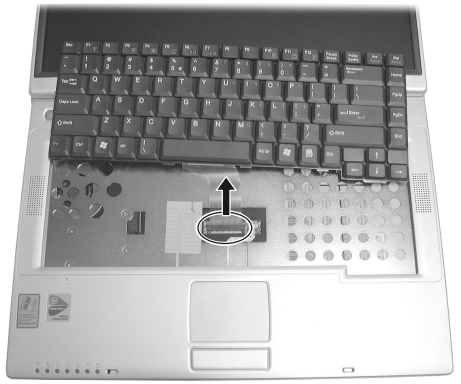


Figure 2-3 Disconnect the cable

Reassembly

1. Reconnect the keyboard cable and fit the keyboard back into place with four latches.
2. Replace the battery pack. (Refer to section 2.2.1 reassembly)

2.2.3 CPU

Disassembly

1. Remove the battery pack. (Refer to section 2.2.1 Disassembly)
2. Remove three screws fastening the heatsink cover. (Figure 2-4)
3. Remove three spring screws that secure the heatsink upon the CPU and disconnect the fan's power cord from system board. (Figure 2-5)

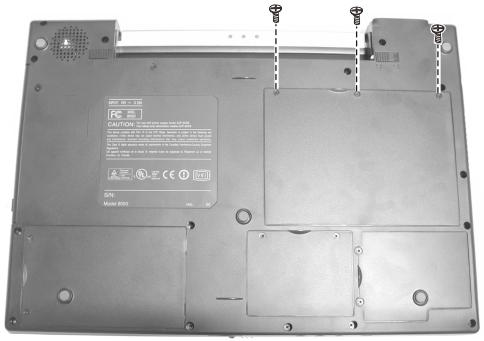


Figure 2-4 Remove three screws

Figure 2-5 Free the heatsink

4. To remove the existing CPU, Loosen the screw by a flat screwdriver,upraise the CPU socket to unlock the CPU. (Figure 2-6)

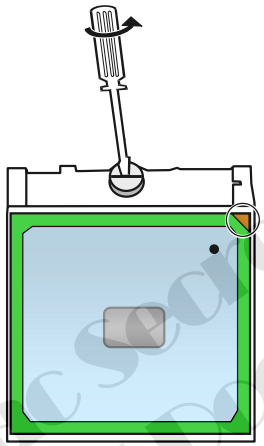


Figure 2-6 Remove the CPU

Reassembly

1. Carefully, align the arrowhead corner of the CPU with the beveled corner of the socket, then insert CPU pins into the holes. Tighten the screw by a flat screwdriver to locking the CPU.
2. Connect the fan's power cord to the system board, fit the heatsink upon the CPU and secure with three spring screws.
3. Replace the CPU cover and secure with three screws.
4. Replace the battery pack. (Refer to section 2.2.1 reassembly)

2.2.4 HDD Module

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (Refer to section 2.2.1 Disassembly)
2. Remove two screws fastening the HDD compartment cover. (Figure 2-7)
3. Remove the one screw and slide the HDD module out of the compartment. (Figure 2-8)

Figure 2-7 Remove the HDD compartment cover

Figure 2-8 Remove HDD module

4. Remove four screws to separate the hard disk drive from the bracket, remove four screws. (Figure 2-9)

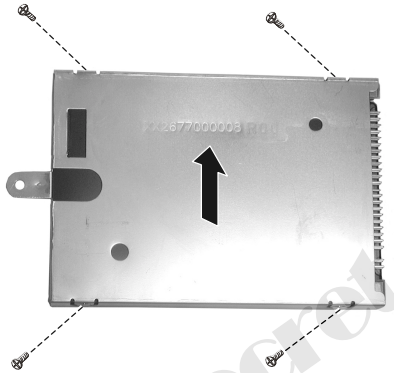


Figure 2-9 Remove hard disk drive

Reassembly

1. Attach the bracket to hard disk drive and secure with four screws.
2. Slide the HDD module into the compartment and secure with one screw.
3. Place the HDD compartment cover and secure with two screws.
4. Replace the battery pack. (Refer to section 2.2.1 reassembly)

2.2.5 CD/DVD-ROM Drive

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (Refer to section 2.2.1 Disassembly)
2. Remove one screw fastening the CD/DVD-ROM drive. (Figure 2-10)
3. Push firmly to release the tray. Then gently pull out the CD/DVD-ROM drive by holding the tray that pops out. (Figure 2-11)

Figure 2-10 Remove one screw

Figure 2-11 Remove the CD/DVD-ROM drive

Reassembly

1. Push the CD/DVD-ROM drive into the compartment and secure with one screw.
2. Replace the battery pack. (Refer to section 2.2.1 reassembly)

2.2.6 Wireless Card

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (Refer to sections 2.2.1 Disassembly)
2. Remove the two screws fastening the Mini PCI compartment cover. (Figure 2-12)
3. Disconnect the wireless card's antennae first (❶). Then pull the retaining clips outwards (❷) and remove the wireless card (❸). (Figure 2-13)

Figure 2-12 Remove two screws

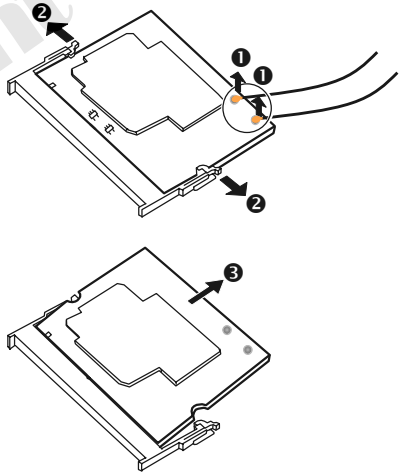


Figure 2-13 Remove the Wireless card

Reassembly

1. To install the wireless card, match the wireless card 's notched part with the socket's projected part and firmly insert it into the socket. Then push down until the retaining clips lock the wireless card into position. Then sure that the antennae fully populated.
2. Tighten the screws to secure the wireless card compartment cover to the housing.
3. Replace the battery pack. (Refer to section 2.2.1 reassembly)

2.2.7 Modem Card

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (Refer to section 2.2.1 Disassembly)
2. Remove two screws fastening modem card's compartment cover. (Refer to steps 1-2 of section 2.2.6 Disassembly)
3. Remove two screws fastening the modem card. (Figure 2-14)
4. Lift up the modem card and disconnect the cord. (Figure 2-15)

Figure 2-14 Remove two screws

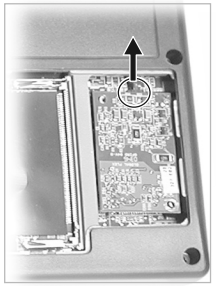


Figure 2-15 Disconnect the cord

Reassembly

1. Reconnect the cord and fit the modem card.
2. Fasten the modem card by two screws.
3. Replace the modem card's compartment cover by two screws. (Refer to step 2 of section 2.2.6 reassembly).
4. Replace the battery pack. (Refer to section 2.2.1 reassembly)

2.2.8 DDR-SDRAM

Disassembly

1. Carefully put the notebook upside down. And remove the battery pack. (See section 2.2.1 disassembly)
2. Remove two screws fastening the DDR compartment cover to access the SO-DIMM socket. (Figure 2-16)

Figure 2-16 Remove the cover

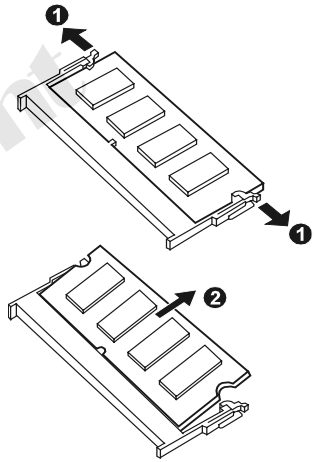


Figure 2-17 Remove the SO-DIMM

3. Pull the retaining clips outwards (❶) and remove the SO-DIMM (❷). (Figure 2-17)

Reassembly

1. To install the DDR, match the DDR's notched part with the socket's projected part and firmly insert the SO-DIMM into the socket at 20-degree angle. Then push down until the retaining clips lock the DDR into position.
2. Replace two screws to fasten the DDR compartment cover.
3. Replace the battery pack. (See section 2.2.1 reassembly)

2.2.9 LCD ASSY

Disassembly

1. Remove the battery pack, keyboard,CPU, hard disk drive, CD/DVD-drive and wireless card. (See sections 2.2.1,2.2.2, 2.2.3, 2.2.4, 2.2.5 and 2.2.6 Disassembly)
2. Remove the nineteen screws on the bottom of notebook. (Figure 2-18)
3. Remove the four screws that secure the hinge cover. (Figure 2-19)

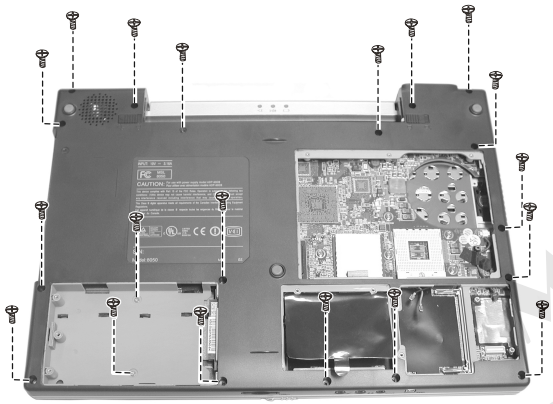


Figure 2-18 Remove nineteen screws

Figure 2-19 Remove four screws

4. Remove the two screws and disconnect the touch pad's cable, then free the top cover.(Figure 2-20)
5. Remove the two hinge covers. (Figure 2-21)

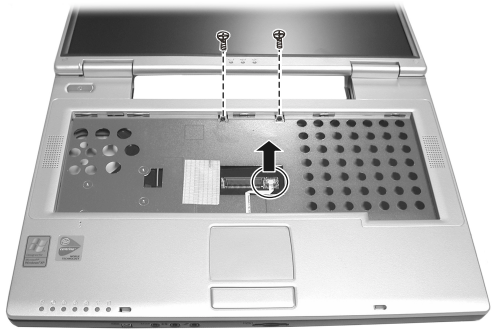


Figure 2-20 Free the Top cover

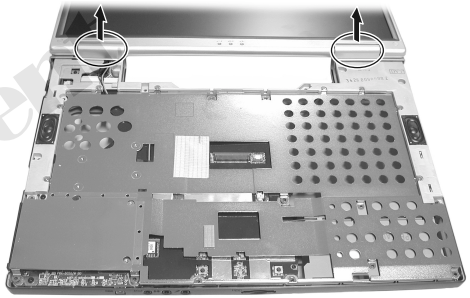


Figure 2-21 Remove the hinge covers

6. Disconnect the two cables and remove the four screws. (Figure 2-22)
7. Remove the eight screws. (Figure 2-23)

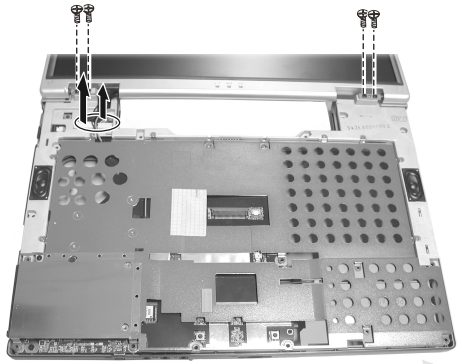


Figure 2-22 Remove the four screws and Disconnect the two cables

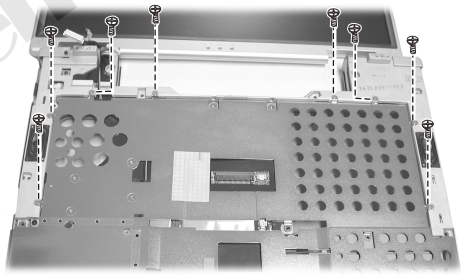


Figure 2-23 Remove the eight screws

8. Carefully pull the antenna wires out. Now you can lift up the LCD ASSY from base unit. (Figure 2-24)

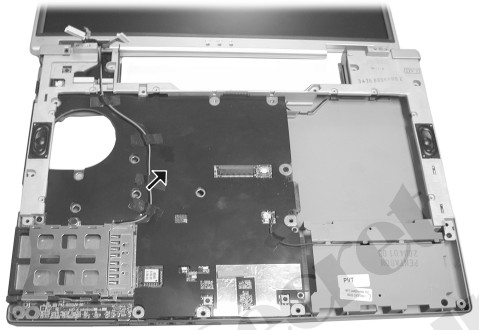


Figure 2-24 Free the LCD ASSY

Reassembly

1. Attach the LCD assembly to the base unit and secure with four screws.
2. Rip the antenna wires back into Min-PCI compartment.
3. Reconnect the two cables to the system board. Screw the hinge covers by two screws.
4. Replace the shield and secure with eight screws.
5. Replace the top cover and secure with two screws. And reconnect the touch pad's cable.
6. Upside down the notebook. secure the housing by nineteen screws and secure two screws in the rear.
7. Replace the Wireless card, CD/DVD-ROM, hard disk drive, CPU, keyboard and battery pack. (Refer to sections 2.2.6, 2.2.5, 2.2.4, 2.2.3, 2.2.2 and 2.2.1 reassembly)

2.2.10 LCD Panel

Disassembly

1. Remove the battery, keyboard, hard disk drive, CD/DVD-ROM drive and LCD assembly. (Refer to section 2.2.1, 2.2.2, 2.2.4, 2.2.5 and 2.2.9 Disassembly)
2. Remove the two rubber pads and two screws on the corners of the panel. (Figure 2-25)
3. Insert a flat screwdriver to the lower part of the LCD cover and gently pry the frame out. Repeat the process until the cover is completely separated from the housing.
4. Remove the twelve screws and disconnect the cable. (Figure 2-26)

Figure 2-25 Remove LCD cover

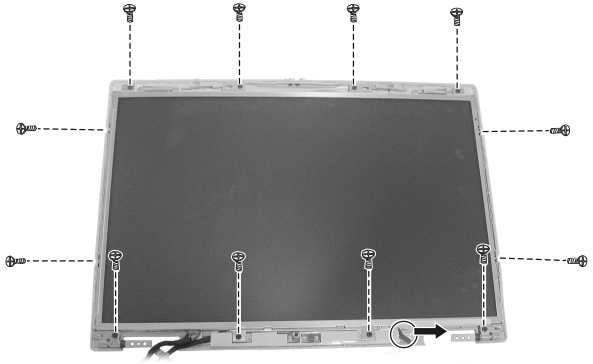


Figure 2-26 Remove twelve screws and disconnect the cable

5. Remove the six screws that secure the LCD bracket. (Figure 2-27)
6. Disconnect the cable to free the LCD panel. (Figure 2-28)

Figure 2-27 Remove the six screws

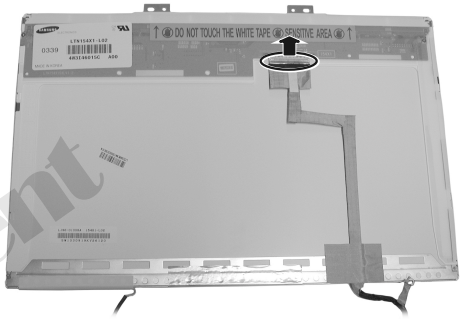


Figure 2-28 Free the LCD panel

Reassembly

1. Replace the cable to the LCD.
2. Attach the LCD panel's bracket back to LCD panel and secure with six screws.
3. Replace the LCD panel into LCD housing.and reconnect two cables to inverter board and secure with two screws.
4. Fasten the LCD panel by ten screws.
5. Fit the LCD cover and secure with two screws and rubber pads.
6. Replace the LCD assembly, CD/DVD-ROM drive, hard disk drive, keyboard, battery pack. (See sections 2.2.9, 2.2.5, 2.2.4, 2.2.2, and 2.2.1 reassembly)

2.2.11 Inverter Board

Disassembly

1. Remove the battery, keyboard, hard disk drive, CD/DVD-ROM drive and LCD assembly. (Refer to section 2.2.1, 2.2.2, 2.2.4, 2.2.5 and 2.2.9 Disassembly)
2. Remove the LCD cover and LCD panel. (Refer to the steps 1-4 of section 2.2.10 Disassembly)
3. Remove the one screw fastening the inverter board and disconnect the cable, Then free the inverter board. (Figure 2-29)

Figure 2-29 Free the inverter board

Reassembly

1. Reconnect the cable. Fit the inverter board back into place and secure with one screw.
2. Replace the LCD Panel and LCD cover. (Refer to section 2.2.10 reassembly)
3. Replace the LCD assembly. (Refer to section 2.2.9 reassembly)
4. Replace the CD/DVD-ROM drive, hard disk drive, keyboard and battery pack. (Refer to sections 2.2.5, 2.2.4, 2.2.2 and 2.2.1 reassembly)

2.2.12 System Board

Disassembly

1. Remove the battery, keyboard, hard disk drive, CD/DVD-ROM drive, Wireless card and LCD assembly. (Refer to sections 2.2.1, 2.2.2, 2.2.4, 2.2.5, 2.2.6 and 2.2.9 Disassembly)
2. Remove the four screws that secure the system board and disconnect the two speaker's cables. Then lift it up from the housing. (Figure 2-30)
3. Disconnect the one speaker's cables from the system board and remove the two screws, Then separate the bracket and free the system board. (Figure 2-31)

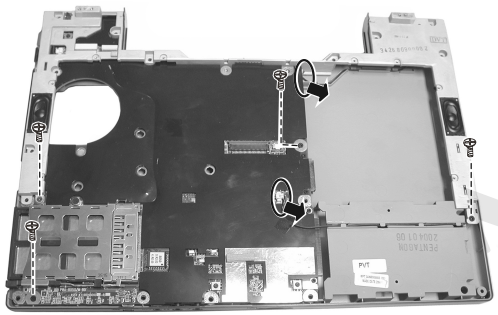


Figure 2-30 Remove four screws and disconnect the two cables

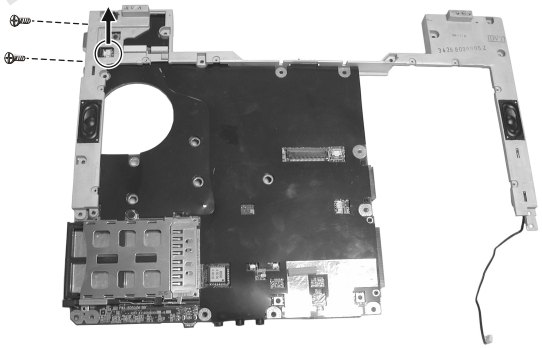


Figure 2-31 Free the system board

Reassembly

1. Fit the bracket and secure with two screws .
2. Turn over the system board. Reconnect the speaker's cords.
3. Replace the system board back into the housing and secure with four screws, then reconnect the cable.
4. Replace the LCD assembly, CD/DVD-ROM, HDD, keyboard and battery pack. (Refer to previous section reassembly)

2.2.13 Touch Pad

Disassembly

1. Remove the battery pack, keyboard, hard disk drive and CD/DVD-drive. (See sections 2.2.1,2.2.2 , 2.2.4 and 2.2.5 Disassembly)
2. Remove the top cover. (See steps 1-5 in section 2.2.9 Disassembly)
3. Remove the two screws and free the touch pad. (Figure 2-32).

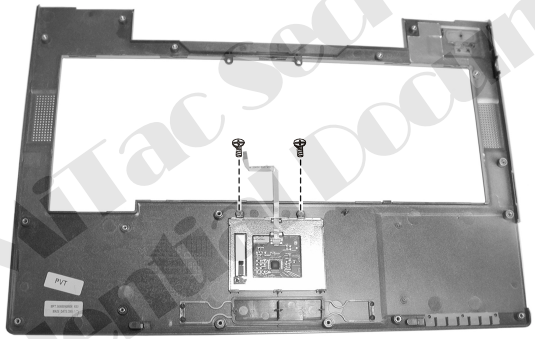


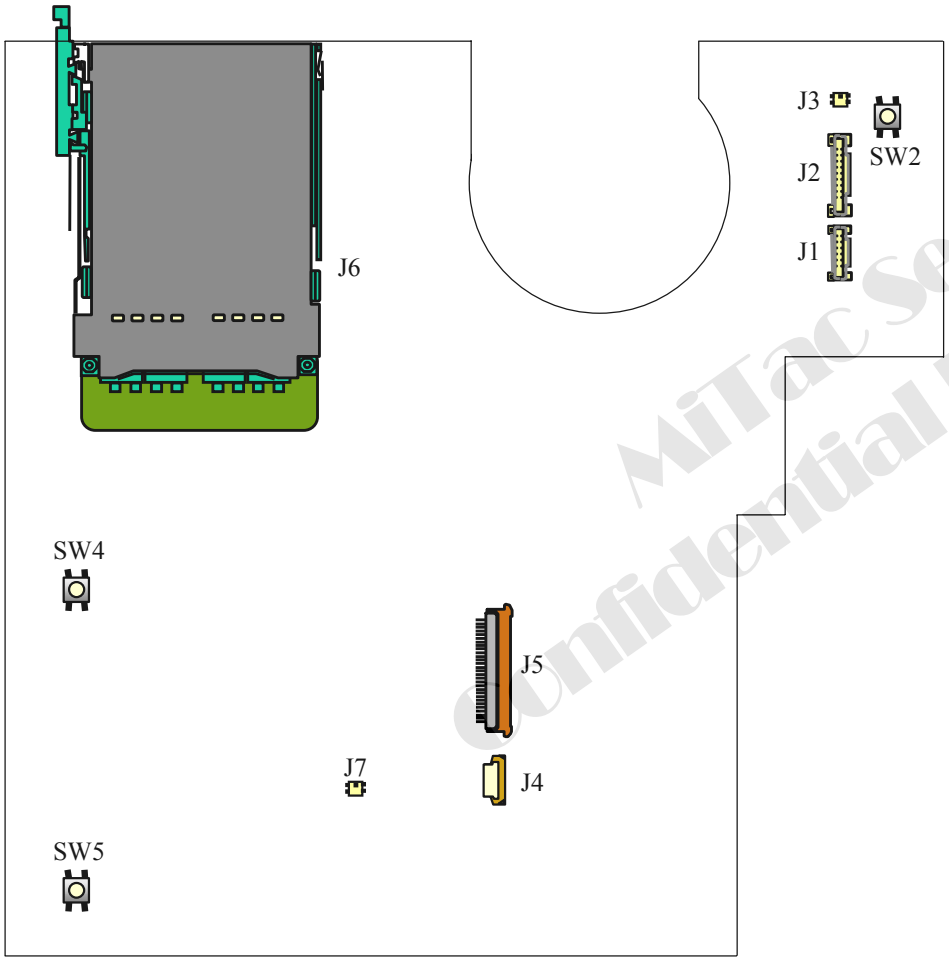
Figure 2-32 Remove the two screws

Reassembly

1. Replace the touch pad and secure the two screws.
2. Replace the top cover. (Refer to the section in 2.2.9 reassembly)
3. Replace the battery pack, keyboard, hard disk drive and CD/DVD-drive. (See sections 2.2.1,2.2.2 , 2.2.4 and 2.2.5 Disassembly).

3. Definition & Location of Connectors / Switches

3.1 Mother Board - A

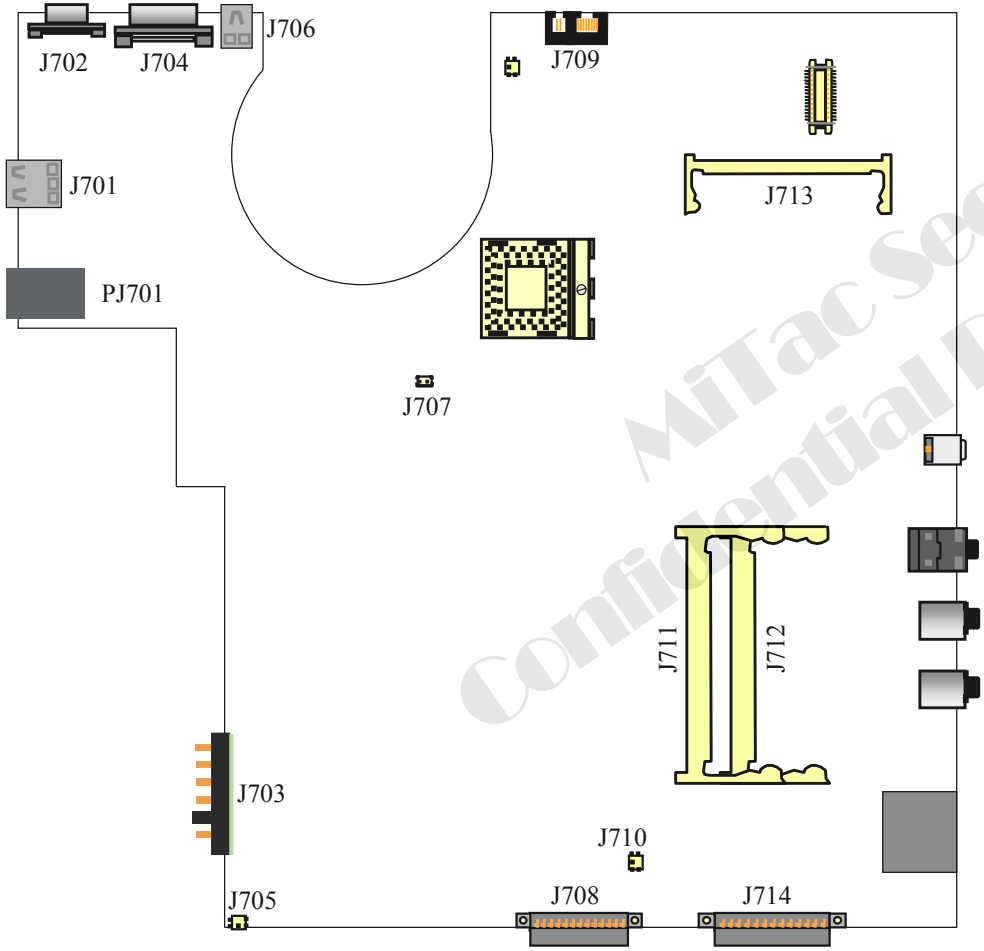


- J1 : Inverter Board Connector
- J2 : LCD panel connector
- J3 : Internal Left Speaker Connector
- J4 : Touch-pad Module Connector
- J5 : Internal Key-board Connector
- J6 : PCMCIA Card Connector
- J7 : Internal Right Speaker Connector

- SW2 : Power Button
- SW4 : Left Button Switch of Touch-pad
- SW5 : Right Button Switch of Touch-pad

3. Definition & Location of Connectors / Switches

3.2 Mother Board - B



- PJ701 : AC Adaptor Connector
- J701&J706 : USB Port Connector
- J702 : CRT Connector
- J703 : Battery Connector
- J704 : External VGA Connector
- J705 : Internal Subwoofer Speaker
- J707: FAN Connector
- J708 : CD-ROM IDE Connector
- J709: RJ45 & RJ11 Connector
- J710 : RTC Battery Connector
- J711&J712 : DDR SO-DIMM Module Socket
- J713 : Mini-PCI Connector
- J714 : Hard Disk Driver Connector

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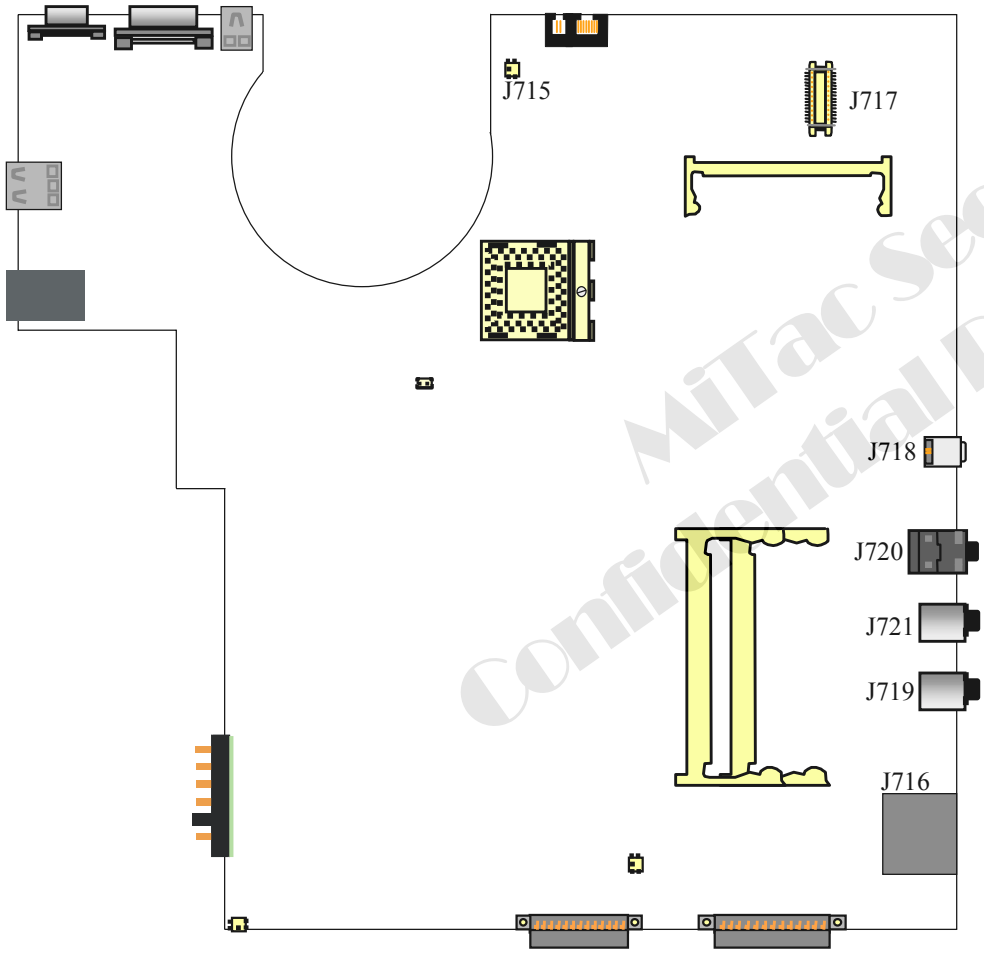
3. Definition & Location of Connectors / Switches

3.2 Mother Board - B



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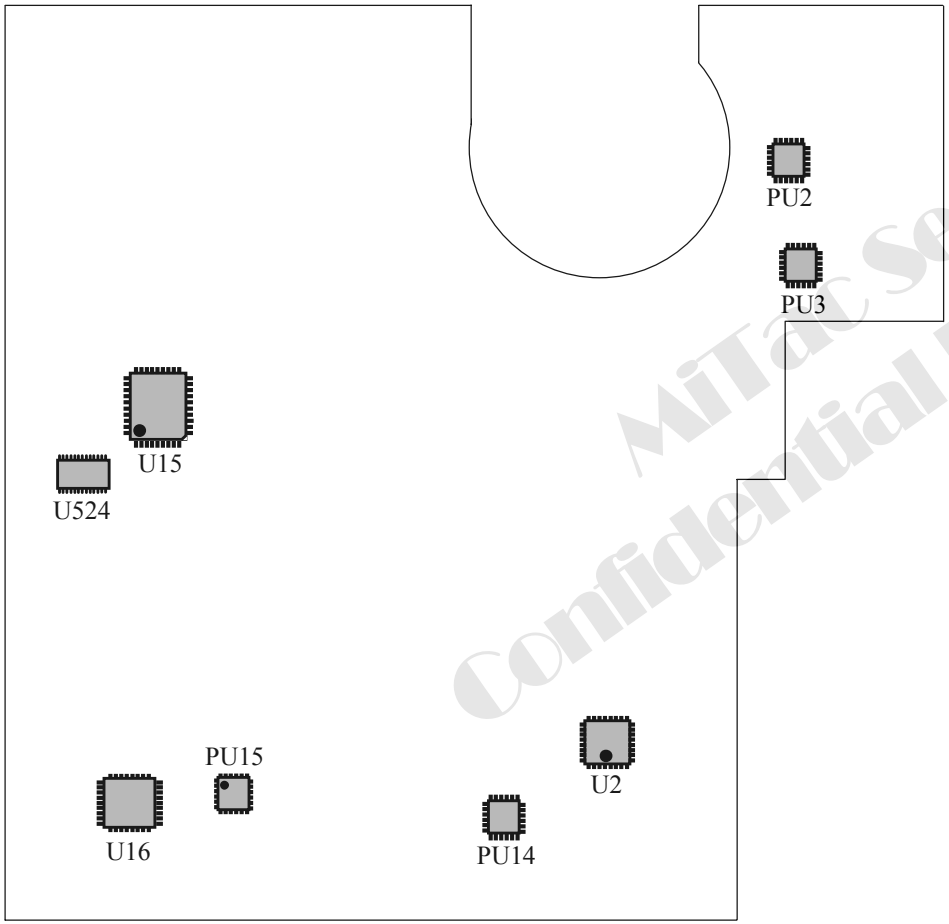
- J715&J717: Modem Daughter Board Connector
- J716 : SD&MS Card Socket
- J718 : IEEE 1394 Connector
- J719 : External Micro Phone Jack
- J720 : Line Out HP/OPT Jack
- J721 : External Line-in Jack

4. Definition & Location of Major Components

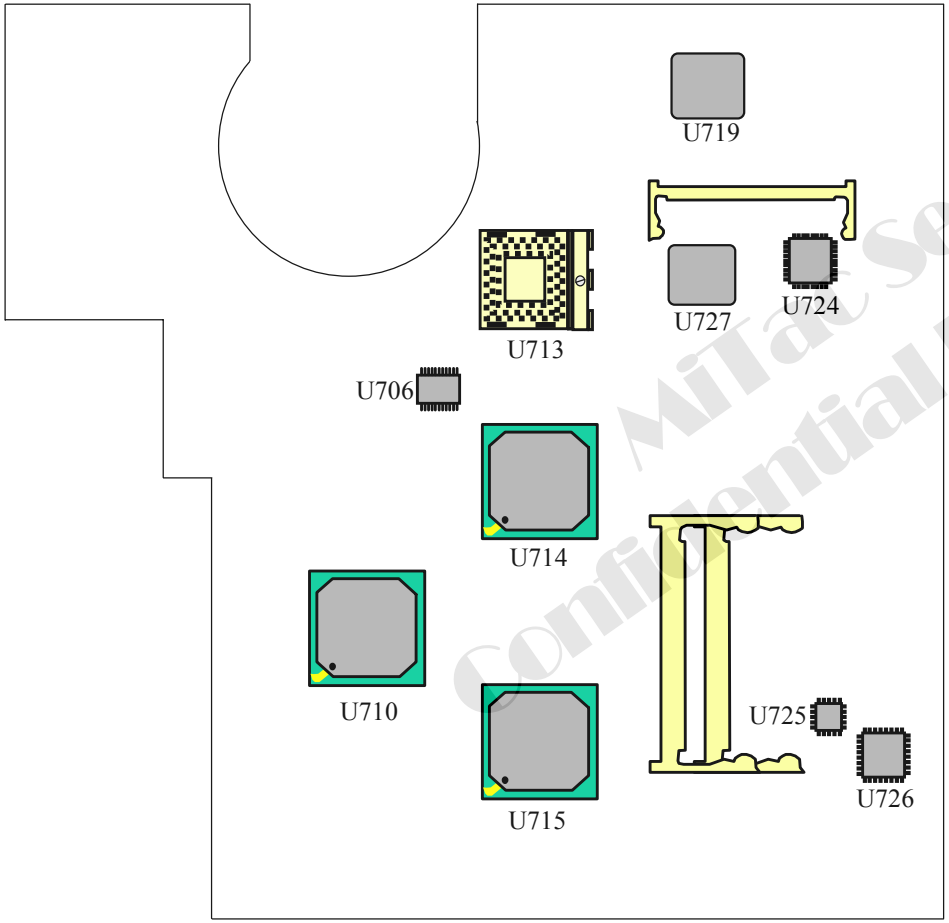
4.1 Mother Board - A



- **PU2 : +3VS/+5VS Voltage Generator**
- **PU3 : CPU Core Voltage Generator**
- **PU14: +1.8V/+1.35V Voltage Generator**
- **PU15 : +2.5VS/+1.25V Voltage Generator**
- **U2 : TV Encoder Controller**
- **U15: SYS BIOS Controller**
- **U16: WINBOND KBC Controller**
- **U524: TPA02012 Audio Amplifier**

4. Definition & Location of Major Components

4.2 Mother Board - B



- U706 : Thermal Sensor/Fan Controller
- U710 : ATI-M10-P
- U713 : Intel BANIAS CPU
- U714 : Intel 855GM/GME North Bridge
- U715 : Intel ICH4-M South Bridge
- U719 : LAN-RTL8100CL Controller
- U724 : IEEE1394 Controller
- U725 : SUBWOOFER AMP Controller
- U726 : Audio CODEC(ALC655)
- U727 : CB710 Card Bus Reader Controller

5. Pin Descriptions of Major Components

5.1 Intel Pentium M(Banias) Processor(1)

Signal Name	Type	Description
A[31:3]#	I/O	A[31:3]# (Address) define a 2 32 -byte physical memory address space. In sub-phase 1 of the address phase, these pins transmit the address of a transaction. In sub-phase 2, these pins transmit transaction type information. These signals must connect the appropriate pins of both agents on the Intel Pentium M processor system bus. A[31:3]# are source synchronous signals and are latched into the receiving buffers by ADSTB[1:0]#. Address signals are used as straps which are sampled before RESET# is deasserted.
A20M#	I	If A20M# (Address-20 Mask) is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-Mbyte boundary. Assertion of A20M# is only supported in real mode. A20M# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.
ADS#	I/O	ADS# (Address Strobe) is asserted to indicate the validity of the transaction address on the A[31:3]# and REQ[4:0]# pins. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction.
ADSTB[1:0]#	I/O	Address strobes are used to latch A[31:3]# and REQ[4:0]# on their rising and falling edges. Strobes are associated with signals as shown below. Signals / Associated Strobe REQ[4:0]#, A[16:3]# / ADSTB[0]# A[31:17]# / ADSTB[1]#
BCLK[1:0]	I	The differential pair BCLK (Bus Clock) determines the system bus frequency. All processor system bus agents must receive these signals to drive their outputs and latch their inputs.
BNR#	I/O	BNR# (Block Next Request) is used to assert a bus stall by any bus agent that is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions.
BPM[2:0]# **BPM[3]**	O I/O	BPM[3:0]# (Breakpoint Monitor) are breakpoint and performance monitor signals. They are outputs from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance. BPM[3:0]# should connect the appropriate pins of all Intel Pentium M processor system bus agents. This includes debug or performance monitoring tools.

Signal Name	Type	Description
BPRI#	I	BPRI# (Bus Priority Request) is used to arbitrate for ownership of the processor system bus. It must connect the appropriate pins of both processor system bus agents. Observing BPRI# active (as asserted by the priority agent) causes the other agent to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed, then releases the bus by deasserting BPRI#.
BR0#	I/O	BR0# is used by the processor to request the bus. The arbitration is done between the Intel Pentium M processor (Symmetric Agent) and the MCH-M (High Priority Agent) of the Intel 855PM or Intel 855GM chipset.
COMPP3:0]	Analog	COMP[3:0] must be terminated on the system board using precision (1% tolerance) resistors. Refer to the platform design guides for more implementation details.
D[63:0]#	I/O	D[63:0]# (Data) are the data signals. These signals provide a 64-bit data path between the processor system bus agents, and must connect the appropriate pins on both agents. The data driver asserts DRDY# to indicate a valid data transfer. D[63:0]# are quad-pumped signals and will thus be driven four times in a common clock period. D[63:0]# are latched off the falling edge of both DSTBP[3:0]# and DSTBN[3:0]#. Each group of 16 data signals correspond to a pair of one DSTBP# and one DSTBN#. The following table shows the grouping of data signals to data strobes and DINV#. **Quad-Pumped Signal Groups** Data Group / DSTBN#/DSTBP# / DINV# D[15:0]# / 0 / 0 D[31:16]# / 1 / 1 D[47:32]# / 2 / 2 D[63:48]# / 3 / 3 Furthermore, the DINV# pins determine the polarity of the data signals. Each group of 16 data signals corresponds to one DINV# signal. When the DINV# signal is active, the corresponding data group is inverted and therefore sampled active high.
DBR#	O	DBR# (Data Bus Reset) is used only in processor systems where no debug port is implemented on the system board. DBR# is used by a debug port interposer so that an in-target probe can drive system reset. If a debug port is implemented in the system, DBR# is a no connect. DBR# is not a processor signal.

5.1 Intel Pentium M(Banias) Processor(2)

Signal Name	Type	Description
DBSY#	I/O	DBSY# (Data Bus Busy) is asserted by the agent responsible for driving data on the processor system bus to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted. This signal must connect the appropriate pins on both processor system bus agents.
DEFER#	I	DEFER# is asserted by an agent to indicate that a transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or Input/Output agent. This signal must connect the appropriate pins of both processor system bus agents.
DINV[3:0]#	I/O	DINV[3:0]# (Data Bus Inversion) are source synchronous and indicate the polarity of the D[63:0]# signals. The DINV[3:0]# signals are activated when the data on the data bus is inverted. The bus agent will invert the data bus signals if more than half the bits, within the covered group, would change level in the next cycle. **DINV[3:0]# Assignment To Data Bus** Bus Signal / Data Bus Signals: DINV[3]# — D[63:48]# DINV[2]# — D[47:32]# DINV[1]# — D[31:16]# DINV[0]# — D[15:0]#
DPSLP#	I	DPSLP# when asserted on the platform causes the processor to transition from the Sleep state to the Deep Sleep state. In order to return to the Sleep state, DPSLP# must be deasserted. DPSLP# is driven by the ICH4-M component and also connects to the MCH-M component of the Intel 855PM or Intel 855GM chipset.
DRDY#	I/O	DRDY# (Data Ready) is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-common clock data transfer, DRDY# may be deasserted to insert idle clocks. This signal must connect the appropriate pins of both processor system bus agents.
DSTBN[3:0]#	I/O	Data strobe used to latch in D[63:0]#. Signals / Associated Strobe: D[15:0]#, DINV[0]# — DSTBN[0]# D[31:16]#, DINV[1]# — DSTBN[1]# D[47:32]#, DINV[2]# — DSTBN[2]# D[63:48]#, DINV[3]# — DSTBN[3]#
DSTBP[3:0]#	I/O	Data strobe used to latch in D[63:0]#. Signals / Associated Strobe: D[15:0]#, DINV[0]# — DSTBP[0]# D[31:16]#, DINV[1]# — DSTBP[1]# D[47:32]#, DINV[2]# — DSTBP[2]# D[63:48]#, DINV[3]# — DSTBP[3]#

Signal Name	Type	Description
DPWR#	I	DPWR# is a control signal from the Intel 855PM and Intel 855GM chipsets used to reduce power on the Intel Pentium M data bus input buffers.
FERR#/PBE#	O	FERR# (Floating-point Error)/PBE#(Pending Break Event) is a multiplexed signal and its meaning is qualified by STPCLK#. When STPCLK# is not asserted, FERR#/PBE# indicates a floating point when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel 80387 coprocessor, and is included for compatibility with systems using MS-DOS* type floating-point error reporting. When STPCLK# is asserted, an assertion of FERR#/PBE# indicates that the processor has a pending break event waiting for service. The assertion of FERR#/PBE# indicates that the processor should be returned to the Normal state. When FERR#/PBE# is asserted, indicating a break event, it will remain asserted until STPCLK# is deasserted. Assertion of PREQ# when STPCLK# is active will also cause an FERR# break event.
GTLREF	I	GTLREF determines the signal reference level for AGTL+ input pins. GTLREF should be set at 2/3 V_{CCP}. GTLREF is used by the AGTL+ receivers to determine if a signal is a logical 0 or logical 1.
HIT# **HITM#**	I/O I/O	HIT# (Snoop Hit) and HITM# (Hit Modified) convey transaction snoop operation results. Either system bus agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.
IERR#	O	IERR# (Internal Error) is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the processor system bus. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#, BINIT#, or INIT#.
IGNNE#	I	IGNNE# (Ignore Numeric Error) is asserted to force the processor to ignore a numeric error and continue to execute noncontrol floating-point instructions. If IGNNE# is deasserted, the processor generates an exception on a noncontrol floating-point instruction if a previous floating-point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 (CR0) is set. IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.
REQ[4:0]#	I/O	REQ[4:0]# (Request Command) must connect the appropriate pins of both processor system bus agents. They are asserted by the current bus owner to define the currently active transaction type. These signals are source synchronous to ADSTB[0]#.

5.1 Intel Pentium M(Banias) Processor(3)

Signal Name	Type	Description
INIT#	I	INIT# (Initialization), when asserted, resets integer registers inside the processor without affecting its internal caches or floating-point registers. The processor then begins execution at the power on Reset vector configured during power on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output Write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction. INIT# must connect the appropriate pins of both processor system bus agents. If INIT# is sampled active on the active to inactive transition of RESET#, then the processor executes its Built-in Self-Test (BIST)
LINT[1:0]	I	LINT[1:0] (Local APIC Interrupt) must connect the appropriate pins of all APIC Bus agents. When the APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a nonmaskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium processor. Both signals are asynchronous. Both of these signals must be software configured using BIOS programming of the APIC register space and used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration.
LOCK#	I/O	LOCK# indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins of both processor system bus agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction to the end of the last transaction. When the priority agent asserts BPRI# to arbitrate for ownership of the processor system bus, it will wait until it observes LOCK# deasserted. This enables symmetric agents to retain ownership of the processor system bus throughout the bus locked operation and ensure the atomicity of lock.
PRDY#	O	Probe Ready signal used by debug tools to determine processor debug readiness.
PREQ#	I	Probe Request signal used by debug tools to request debug operation of the processor.
PROCHOT#	O	PROCHOT# (Processor Hot) will go active when the processor temperature monitoring sensor detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit has been activated, if enabled. This signal may require voltage translation on the motherboard.
PSI#	O	Processor Power Status Indicator signal. This signal is asserted when the processor is in a lower state (Deep Sleep and Deeper Sleep).

Signal Name	Type	Description
PWRGOOD	I	PWRGOOD (Power Good) is a processor input. The processor requires this signal as a clean indication that the clocks and power supplies are stable and within their specifications. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD. The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout the boundary scan operation.
ITP_CLK[1:0]	I	ITP_CLK[1:0] are copies of BCLK that are used only in processor systems where no debug port is implemented on the system board. ITP_CLK[1:0] are used as BCLK[1:0] references for a debug port implemented on an interposer. If a debug port is implemented in the system, ITP_CLK[1:0] are no connects. These are not processor signals.
RESET#	I	Asserting the RESET# signal resets the processor to a known state and invalidates its internal caches without writing back any of their contents. For a power-on Reset, RESET# must stay active for at least two milliseconds after VCC and BCLK have reached their proper specifications. On observing active RESET#, both system bus agents will deassert their outputs within two clocks. All processor straps must be valid within the specified setup time before RESET# is deasserted.
RS[2:0]#	I	RS[2:0]# (Response Status) are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of both processor system bus agents.
RSVD	-	These pins are RESERVED and must be left unconnected on the board. However, it is recommended that routing channels to these pins on the board be kept open for possible future use. Please refer to the platform design guides for more details.
SLP#	I	SLP# (Sleep), when asserted in Stop-Grant state, causes the processor to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts. The processor will recognize only assertion of the RESET# signal, deassertion of SLP#, and removal of the BCLK input while in Sleep state. If SLP# is deasserted, the processor exits Sleep state and returns to Stop-Grant state, restarting its internal clock signals to the bus and processor core units. If DPSLP# is asserted while in the Sleep state, the processor will exit the Sleep state and transition to the Deep Sleep state.

5.1 Intel Pentium M(Banias) Processor(4)

Signal Name	Type	Description
SMI#	I	SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, the processor saves the current state and enter System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler. If SMI# is asserted during the deassertion of RESET# the processor will tristate its outputs.
STPCLK#	I	STPCLK# (Stop Clock), when asserted, causes the processor to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the system bus and APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.
TCK	I	TCK (Test Clock) provides the clock input for the processor Test Bus (also known as the Test Access Port).
TDI	I	TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.
TDO	O	TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.
TEST1, TEST2, TEST3	I	TEST1, TEST2, and TEST3 must be left unconnected but should have a stuffing option connection to V SS separately using 1-k, pull-down resisitors.
THERMDA	Other	Thermal Diode Anode.
THERMDC	Other	Thermal Diode Cathode.
THERMTRIP#	O	The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all execution when the junction temperature exceeds approximately 125°C. This is signalled to the system by the THERMTRIP# (Thermal Trip) pin.
TMS	I	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools.
TRDY#	I	TRDY# (Target Ready) is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of both system bus agents.
TRST#	I	TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset.

Signal Name	Type	Description
VCC	I	Processor core power supply.
VCCA[3:0]	I	VCCA provides isolated power for the internal processor core PLL's.
VCCP	I	Processor I/O Power Supply.
VCCQ[1:0]	I	Quiet power supply for on die COMP circuitry. These pins should be connected to VCCP on the motherboard. However, these connections should enable addition of decoupling on the VCCQ lines if necessary.
VCCSENSE	O	VCCSENSE is an isolated low impedance connection to processor core power (VCC). It can be used to sense or measure power near the silicon with little noise.
VID[5:0]	O	VID[5:0] (Voltage ID) pins are used to support automatic selection of power supply voltages (Vcc). Unlike some previous generations of processors, these are CMOS signals that are driven by the Intel Pentium M processor. The voltage supply for these pins must be valid before the VR can supply Vcc to the processor. Conversely, the VR output must be disabled until the voltage supply for the VID pins becomes valid. The VID pins are needed to support the processor voltage specification variations.
VSSSENSE	O	VSSSENSE is an isolated low impedance connection to processor core VSS. It can be used to sense or measure ground near the silicon with little noise.

5.2 Intel 855GM/GME North Bridge(1)

Host Interface Signal Descriptions

Signal Name	Type	Description
ADS#	I/O AGTL+	**Address Strobe:** The system bus owner asserts ADS# to indicate the first of two cycles of a request phase. The GMCH can assert this signal for snoop cycles and interrupt messages.
BNR#	I/O AGTL+	**Block Next Request:** Used to block the current request bus owner from issuing a new request. This signal is used to dynamically control the CPU bus pipeline depth.
BPRI#	O AGTL+	**Bus Priority Request:** The GMCH is the only Priority Agent on the system bus. It asserts this signal to obtain the ownership of the address bus. This signal has priority over symmetric bus requests and will cause the current symmetric owner to stop issuing new transactions unless the HLOCK# signal was asserted.
BREQ0#	I/O AGTL+	**Bus Request 0#:** The GMCH pulls the processor bus BREQ**0#** signal low during **CPURST#.** The signal is sampled by the processor on the active-to-inactive transition of CPURST#. The minimum setup time for this signal is 4 BCLKs. The minimum hold time is 2 clocks and the maximum hold time is 20 BCLKs. BREQ0# should be tristated after the hold time requirement has been satisfied. During regular operation, the GMCH will use BREQ0# as an early indication for FSB Address and Ctl input buffer and sense amp activation.
CPURST#	O AGTL+	**CPU Reset:** The CPURST# pin is an output from the GMCH. The GMCH asserts CPURST# while RESET# (PCIRST# from ICH4-M) is asserted and for approximately 1 ms after RESET# is deasserted. The CPURS**T#** allows the processor to begin execution in a known state. Note that the ICH4-M must provide CPU strap set-up and hold-times around CPURST#. This requires strict synchronization between GMCH, CPURST# deassertion and ICH4-M driving the straps.
DBSY#	I/O AGTL+	**Data Bus Busy:** Used by the data bus owner to hold the data bus for transfers requiring more than one cycle.
DEFER#	O AGTL+	**Defer:** GMCH will generate a deferred response as defined by the rules of the GMCH's Dynamic Defer policy. The GMCH will also use the DEFER# signal to indicate a CPU retry response.

Host Interface Signal Descriptions(Continued)

Signal Name	Type	Description
DINV[3:0]#	I/O AGTL+	**Dynamic Bus Inversion:** Driven along with the HD[63:0]# signals. Indicates if the associated signals are inverted or not. DINV[3:0]# are asserted such that the number of data bits driven electrically low (low voltage) within the corresponding 16-bit group never exceeds 8. **DINV# Data Bits** DINV[3]# HD[63:48]# DINV[2]# HD[47:32]# DINV[1]# HD[31:16]# DINV[0]# HD[16:0]#
DPSLP#	I CMOS	**Deep Sleep #:** This signal comes from the ICH4-M device, providing an indication of C3 and C4 state control to the CPU. Deassertion of this signal is used as an early indication for C3 and C4 wake up (to active HPLL). Note that this is a low-voltage CMOS buffer operating on the FSB VTT power plane.
DRDY#	I/O AGTL+	**Data Ready:** Asserted for each cycle that data is transferred.
HA[31:3]#	I/O AGTL+	**Host Address Bus:** HA[31:3]# connects to the CPU address bus. During processor cycles the HA[31:3]# are inputs. The GMCH drives HA[31:3]# during snoop cycles on behalf of Hub interface. HA[31:3]# are transferred at 2x rate. Note that the address is inverted on the CPU bus.
HADSTB[1:0]#	I/O AGTL+	**Host Address Strobe:** HA[31:3]# connects to the CPU address bus. During CPU cycles, the source synchronous strobes are used to transfer HA[31:3]# and HREQ[4:0]# at the 2x transfer rate. **Strobe Address Bits** HADSTB[0]# HA[16:3]#, HREQ[4:0]# HADSTB[1]# HA[31:17]#
HD[63:0]#	I/O AGTL+	**Host Data:** These signals are connected to the CPU data bus. HD[63:0]# are transferred at 4x rate. Note that the data signals are inverted on the CPU bus.

5.2 Intel 855GM/GME North Bridge(2)

Host Interface Signal Descriptions (Continued)

Signal Name	Type	Description
HDSTBP[3:0]# **HDSTBN[3:0]#**	I/O AGTL+	**Differential Host Data Strobes:** The differential source synchronous strobes are used to **transfer HD[63:0]# and DINV[3:0]# at** the 4x transfer rate. **Strobe Data Bits** HDSTBP[3]#, HDSTBN[3]# HD[63:48]#, DINV[3]# HDSTBP[2]#, HDSTBN[2]# HD[47:32]#, DINV[2]# HDSTBP[1]#, HDSTBN[1]# HD[31:16]#, DINV[1]# HDSTBP[0]#, HDSTBN[0]# HD[15:0]#, DINV[0]#
HIT#	I/O AGTL+	**Hit:** Indicates that a caching agent holds an unmodified version of the requested line. Also, driven in conjunction with HITM# by the target to extend the snoop window.
HITM#	I/O AGTL+	**Hit Modified:** Indicates that a caching agent holds a modified version of the requested line and that this agent assumes responsibility for providing the line. Also, driven in conjunction with HIT# to extend the snoop window.
HLOCK#	I/O AGTL+	**Host Lock:** All CPU bus cycles sampled with the assertion of HLOCK# and ADS#, until the negation of HLOCK# must be atomic, i.e. no Hub interface snoopable access to system memory is allowed when HLOCK# is asserted by the CPU.
HREQ[4:0]#	I/O AGTL+	**Host Request Command:** Defines the attributes of the request. HREQ[4:0]# are transferred at 2x rate. Asserted by the requesting agent during both halves of the Request Phase. In the first half the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second half the signals carry additional information to define the complete transaction type. The transactions supported by the GMCH Host Bridge are defined in the Host Interface section of this document.
HTRDY#	O AGTL+	**Host Target Ready:** Indicates that the target of the processor transaction is able to enter the data transfer phase.
RS[2:0]#	O AGTL+	**Response Status:** Indicates the type of response according to the following the table: **RS[2:0]# Response type** 000 Idle state 001 Retry response 010 Deferred response 011 Reserved (not driven by GMCH) 100 Hard Failure (not driven by GMCH) 101 No data response 110 Implicit Write back 111 Normal data response

DDR SDRAM Interface Descriptions

Signal Name	Type	Description
SCS[3:0]#	O SSTL_2	**Chip Select:** These pins select the particular DDR SDRAM components during the active state. **NOTE:** There is one SCS# per DDR-SDRAM Physical SO-DIMM device row. These signals can be toggled on every rising System Memory Clock edge (SCMDCLK).
SMA[12:0]	O SSTL_2	**Multiplexed Memory Address:** These signals are used to provide the multiplexed row and column address to the DDR SDRAM.
SBA[1:0]	O SSTL_2	**Bank Select (Memory Bank Address):** These signals define which banks are selected within each DDR SDRAM row. The SMA and SBA signals combine to address every possible location within a DDR SDRAM device.
SRAS#	O SSTL_2	**DDR Row Address Strobe: SRAS#** may be heavily loaded and requires tw0 DDR SDRAM clock cycles for setup time to the DDR SDRAMs. Used with SCAS# and SWE# (along with SCS#) to define the system memory commands.
SCAS#	O SSTL_2	**DDR Column Address Strobe:** SCAS# may be heavily loaded and requires two clock cycles for setup time to the DDR SDRAMs. Used with SRAS# and SWE# (along with SCS#) to define the system memory commands.
SWE#	O SSTL_2	**Write Enable:** Used with SCAS# and SRAS# (along with SCS#) to define the DDR SDRAM commands. SWE# is asserted during writes to DDR SDRAM. SWE# may be heavily loaded and requires two clock cycles for setup time to the DDR SDRAMs.
SDQ[71:0]	I/O SSTL_2	**Data Lines:** These signals are used to interface to the DDR SDRAM data bus. **NOTE:** ECC error detection is supported: by the SDQ[71:64] signals.

5.2 Intel 855GM/GME North Bridge(3)

DDR SDRAM Interface Descriptions (Continued)

Signal Name	Type	Description
SDQS[8:0]	I/O SSTL_2	**Data Strobes:** Data strobes are used for capturing data. During writes, SDQS is centered on data. During reads, SDQS is edge aligned with data. The following list matches the data strobe with the data bytes. There is an associated data strobe (DQS) for each data signal (DQ) and check bit (CB) group. SDQS[7] -> SDQ[63:56] SDQS[6] -> SDQ[55:48] SDQS[5] -> SDQ[47:40] SDQS[4] -> SDQ[39:32] SDQS[3] -> SDQ[31:24] SDQS[2] -> SDQ[23:16] SDQS[1] -> SDQ[15:8] SDQS[0] -> SDQ[7:0] **NOTE:** ECC error detection is supported by the SDQS[8] signal.
SCKE[3:0]	O SSTL_2	**Clock Enable:** These pins are used to signal a self-refresh or power down command to the DDR SDRAM array when entering system suspend. SCKE is also used to dynamically power down inactive DDR SDRAM rows. There is one SCKE per DDR SDRAM row. These signals can be toggled on every rising SCK edge.
SMAB[5,4,2,1]	O SSTL_2	**Memory Address Copies:** These signals are identical to SMA[5,4,2,1] and are used to reduce loading for selective CPC(clock-per-command). These copies are not inverted.
SDM[8:0]	O SSTL_2	**Data Mask:** When activated during writes, the corresponding data groups in the DDR SDRAM are masked. There is one SDM for every eight data lines. SDM can be sampled on both edges of the data strobes. **NOTE:** ECC error detection is supported by the SDM[8] signal.
RCVENOUT#	O SSTL_2	**Clock Output:** Reserved, NC.
RCVENIN#	O SSTL_2	**Clock Input:** Reserved, NC.

AGP Addressing Signal Descriptions

Signal Name	Type	Description
GPIPE#	I AGP	**Pipelined Read:** This signal is asserted by the AGP master to indicate a full width address is to be enqueued on by the target using the **AD** bus. One address is placed in the AGP request queue on each rising clock edge while **PIPE#** is asserted. When **PIP**E# is deasserted no new requests are queued across the AD bus. **During SBA Operation:** This signal is **not used** if SBA (Side Band Addressing) is selected. **During FRAME# Operation:** This signal is **not used** during AGP FRAME# operation. **PIPE#** is a sustained tri-state signal from masters (graphics controller), and is an input to the GMCH.
GSBA[7:0]	I AGP	**Side-band Address:** These signals are used by the AGP master (graphics controller) to pass address and command to the GMCH. The **SBA** bus and AD bus operate independently. That is, transactions can proceed on the **SBA** bus and the AD bus simultaneously. **During PIPE# Operation:** These signals are **not used** during PIPE# operation. **During FRAME# Operation:** These signals are **not used** during AGP FRAME# operation. **NOTE:** When sideband addressing is disabled, these signals are isolated (no external/internal pull-ups are required).

5 contains two mechanisms to queue requests by the AGP master. Note that the master can only use one mechanism. The master may not switch methods without a full reset of the system. When PIPE# is used to queue addresses the master isnot allowed to queue addresses using the SBA bus. For example, during configuration time, if the master indicates that it can use either mechanism, the configuration software will indicate which mechanism the master will use. Once this choice has been made, the master will continue to use the mechanism selected until the master is reset (and reprogrammed) to use the other mode. This change of modes is not a dynamic mechanism, but rather a static decision when the device is first being configured after reset

5.2 Intel 855GM/GME North Bridge(4)

AGP Status Signal Descriptions

Signal Name	Type	Description		
GST[2:0]	O AGP	**Status:** Provides information from the arbiter to an AGP Master on what it may do. **ST[2:0]** only have meaning to the master when its **GNT#** is asserted. When **GNT#** is deasserted these signals have no meaning and must be gnored.	**ST[2:0**	**Meaning**
			000	Previously requested low priority read data is being returned to the master arbiter to an AGP
			001	Previously requested high priority read data is being returned to the master
			010	The master is to provide low priority write data for a previously queued write command
			011	The master is to provide high priority write data for a previously queued write command.
			100	Reserved
			101	Reserved
			110	Reserved
			111	The master has been given permission to start a bus transaction. The master may queue AGP requests by asserting **PIPE#** or start a PCI transaction by asserting **FRAME#**

AGP Flow Control Signals

Signal Name	Type	Description
GRBF#	I AGP	**Read Buffer Full:** Read buffer full indicates if the master is ready to accept previously requested low priority read data. When **RBF#** is asserted the GMCH is not allowed to initiate the return low priority read data. That is, the GMCH can finish returning the data for the request currently being serviced. **RBF#** is only sampled at the beginning of a cycle. If the AGP master is always ready to accept return read data then it is not required to implement this signal. **During FRAME# Operation:** This signal is not used during AGP FRAME# operation.
GWBF#	I AGP	**Write-Buffer Full:** indicates if the master is ready to accept Fast Write data from the GMCH. When **WBF#** is asserted the GMCH is not allowed to drive Fast Write data to the AGP master. **WBF#** is only sampled at the beginning of a cycle. If the AGP master is always ready to accept fast write data then it is not required to implement this signal. **During FRAME# Operation:** This signal is not used during AGP FRAME# operation.

5.2 Intel 855GM/GME North Bridge(5)

AGP/PCI Signals-Semantics Descriptions

Signal Name	Type	Description
GFRAME#	I/O AGP	**G_FRAME:** Frame. **During PIPE# and SBA Operation:** Not used by AGP SBA and PIPE# operations. **During Fast Write Operation:** Used to frame transactions as an output during Fast Writes. **During FRAME# Operation:** G_FRAME# is an output when the GMCH acts as an initiator on the AGP Interface. G_FRAME# is asserted by the GMCH to indicate the beginning and duration of an access. G_FRAME# is an input when the GMCH acts as a FRAME#-based AGP target. As a FRAME#-based AGP target, the GMCH latches the C/BE[3:0]# and the AD[31:0] signals on the first clock edge on which GMCH samples FRAME# active.
GIRDY#	I/O AGP	**G_IRDY#: Initiator Ready.** **During PIPE# and SBA Operation:** Not used while enqueueing requests via AGP SBA and PIPE#, but used during the data phase of PIPE# and SBA transactions. **During FRAME# Operation:** G_IRDY# is an output when GMCH acts as a FRAME#-based AGP initiator and an input when the GMCH acts as a FRAME#-based AGP target. The assertion of G_IRDY# indicates the current FRAME#-based AGP bus initiator's ability to complete the current data phase of the transaction. **During Fast Write Operation:** In Fast Write mode, G_IRDY# indicates that the AGP-compliant master is ready to provide all write data for the current transaction. Once G_IRDY# is asserted for a write operation, the master is not allowed to insert wait states. The master is never allowed to insert a wait state during the initial data transfer (32 bytes) of a write transaction. However, it may insert wait states after each 32-byte block is transferred.

AGP Strobe Descriptions

Signal Name	Type	Description
GADSTB[0]	I/O AGP	**Address/Data Bus Strobe-0:** provides timing for 2x and 4x data on **AD[15:0]** and **C/BE[1:0]#** signals. The agent that is providing the data will drive this signal.
GADSTB#[0]	I/O AGP	**Address/Data Bus Strobe-0 Complement:** With AD STB0, forms a differential strobe pair that provides timing information for the **AD[15:0]** and **C/BE[1:0]#** signals. The agent that is providing the data will drive this signal.
GADSTB[1]	I/O AGP	**Address/Data Bus Strobe-1:** Provides timing for 2x and 4x data on **AD[31:16]** and **C/BE[3:2]#** signals. The agent that is providing the data will drive this signal.
GADSTB#[1]	I/O AGP	**Address/Data Bus Strobe-1 Complement:** With AD STB1, forms a differential strobe pair that provides timing information for the AD[15:0] and C/BE[1:0]# signals in 4X mode. The agent that is providing the data will drive this signal.
GSBSTB	I AGP	**Sideband Strobe:** Provides timing for 2x and 4x data on the **SBA[7:0]** bus. It is driven by the AGP master after the system has been configured for 2x or 4x sideband address mode.
GSBSTB#	I AGP	**Sideband Strobe Complement:** The differential complement to the **SB_STB** signal. It is used to provide timing 4x mode.

5.2 Intel 855GM/GME North Bridge(6)

AGP/PCI Signals-Semantics Descriptions (Continued)

Signal Name	Type	Description
GTRDY#	I/O AGP	**G_TRDY#:** Target Ready. **During PIPE# and SBA Operation:** Not used while enqueueing requests via AGP SBA and PIPE#, but used during the data phase of PIPE# and SBA transactions. **During FRAME# Operation:** G_TRDY# is an input when the GMCH acts as an AGP initiator and is an output when the GMCH acts as a FRAME#-based AGP target. The assertion of G_TRDY# indicates the target's ability to complete the current data phase of the transaction. **During Fast Write Operation:** In Fast Write mode, G_TRDY# indicates the AGP-compliant target is ready to receive write data for the entire transaction (when the transfer size is less than or equal to 32 bytes) or is ready to transfer the initial or subsequent block (32 bytes) of data when the transfer size is greater than 32 bytes. The target is allowed to insert wait states after each block (32 bytes) is transferred on write transactions.
GSTOP#	I/O AGP	**G_STOP#:** Stop. **During PIPE# and SBA Operation:** This signal is not used during PIPE# or SBA operation. **During FRAME# Operation:** G_STOP# is an input when the GMCH acts as a FRAME#-based AGP initiator and is an output when the GMCH acts as a FRAME#-based AGP target. G_STOP# is used for disconnect, retry, and abort sequences on the AGP interface.
GDEVSEL#	I/O AGP	**G_ DEVSEL#: Device Select.** **During PIPE# and SBA Operation:** This signal is not used during PIPE# or SBA operation. **During FRAME# Operation:** G_DEVSEL#, when asserted, indicates that a FRAME#-based AGP target device has decoded its address as the target of the current access. The GMCH asserts G_DEVSEL# based on the DDR SDRAM address range being accessed by a PCI initiator. As an input, G_DEVSEL# indicates whether the AGP master has recognized a PCI cycle to it.
GREQ#	I AGP	**G_REQ#:** Request. **During SBA Operation:** This signal is not used during SBA operation. **During PIPE# and FRAME# Operation:** G_REQ#, when asserted, indicates that the AGP master is requesting use of the AGP interface to run a FRAME#- or PIPE#-based operation.

ATP/PCI Signals-Semantics Descriptions(Continued)

Signal Name	Type	Description
GGNT#	O AGP	**G_GNT#: Grant.** **During SBA, PIPE# and FRAME# Operation:** G_GNT#, along with the information on the ST[2:0] signals (status bus), indicates how the AGP interface will be used next. Refer to the *AGP Interface Specification, Revision 2.0* for further explanation of the ST[2:0] values and their meanings.
GAD[31:0]	I/O AGP	**G_AD[31:0]: Address/Data Bus.** **During PIPE# and FRAME# Operation:** The G_AD[31:0] signals are used to transfer both address and data information on the AGP interface. **During SBA Operation:** The G_AD[31:0] signals are used to transfer data on the AGP interface.
GCBE#[3:0]	I/O AGP	**Command/Byte Enable.** **During FRAME# Operation:** During the address phase of a transaction, the G_CBE[3:0]# signals define the bus command. During the data phase, the G_CBE[3:0]# signals are used as byte enables. The byte enables determine which byte lanes carry meaningful data. The commands issued on the G_CBE# signals during FRAME#-based AGP transactions are the same G_CBE# command described in the PCI 2.2 specification. **During PIPE# Operation:** When an address is enqueued using PIPE#, the C/BE# signals carry command information. The command encoding used during PIPE#-based AGP is *different* than the command encoding used during FRAME#-based AGP cycles (or standard PCI cycles on a PCI bus). **During SBA Operation:** These signals are not used during SBA operation.
GPAR	I/O AGP	**Parity.** **During FRAME# Operation:** G_PAR is driven by the GMCH when it acts as a FRAME#-based AGP initiator during address and data phases for a write cycle, and during the address phase for a read cycle. G_PAR is driven by the GMCH when it acts as a FRAME#-based AGP target during each data phase of a FRAME#-based AGP memory read cycle. Even parity is generated across G_AD[31:0] and G_CBE[3:0]#. **During SBA and PIPE# Operation:** This signal is not used during SBA and PIPE# operation.

PCIRST# from the ICH4-M is assumed to be connected to RSTIN# and is used to reset AGP interface logic within the GMCH. The AGP agent will also typically use PCIRST# provided by the ICH4-M as an input to reset its internal logic.

5.2 Intel 855GM/GME North Bridge(7)

Hub Interface Signals

Signal Name	Type	Description
HL[10:0]	I/O Hub	**Packet Data:** Data signals used for HI read and write operations.
HLSTB	I/O Hub	**Packet Strobe:** One of two differential strobe signals used to transmit or receive packet data over HI.
HLSTB#	I/O Hub	**Packet Strobe Complement**: One of two differential strobe signals used to transmit or receive packet data over HI.

Dedicated LVDS LCD Flat Panel Interface Signal Descriptions

Name	Type	Voltage	Description
ICLKAP	O LVDS	1.25 V± 225 mV	**Channel A differential clock pair output (true):** 245-800 MHz
ICLKAM	O LVDS	1.25 V±225 mV	**Channel A differential clock pair output (compliment):** 245-800 MHz.
IYAP[3:0]	O LVDS	1.25 V±225 mV	**Channel A differential data pair 3:0 output (true):** 245-800MHz.
IYAM[3:0]	O LVDS	1.25 V±225 mV	**Channel A differential data pair 3:0 output (compliment):** 245-800 MHz.
ICLKBP	O LVDS	1.25 V±225 mV	**Channel B differential clock pair output (true):** 245-800 MHz.
ICLKBM	O LVDS	1.25 V±225 mV	**Channel B differential clock pair output (compliment):** 245-800 MHz.
IYBP[3:0]	O LVDS	1.25 V±225 mV	**Channel B differential data pair 3:0 output (true):** 245-800MHz.
IYBM[3:0]	O LVDS	1.25 V± 225 mV	**Channel B differential data pair 3:0 output (compliment):** 245-800 MHz.

Digital Video Output B (DVOB) Port Signal Descriptions

Name	Type	Description
DVOBD[11:0]	O DVO	**DVOB Data:** This data bus is used to drive 12-bit RGB data on each edge of the differential clock signals, DVOBCLK and DVOBCLK#. This provides 24-bits of data per clock period. In dual channel mode, this provides the lower 12-bits of pixel data. DVOBD[11:0] should be left as left as NC (“Not Connected”) if not used.
DVOBHSYNC	O DVO	**Horizontal Sync**: HSYNC signal for the DVOB interface. **DVOBHSYNC** should be left as left as NC (“Not Connected”) if not used.
DVOBVSYNC	O DVO	**Vertical Sync**: VSYNC signal for the DVOB interface. DVOBVSYNC should be left as left as NC (“Not Connected”) if the signal is NOT used when using internal graphics device.
DVOBBLANK#	O DVO	**Flicker Blank or Border Period Indication: DVOBBLANK# is** a programmable output pin driven by the GMCH. When programmed as a blank period indication, this pin indicates active pixels excluding the border. When programmed as a border period indication, this pin indicates active pixel including the border pixels. DVOBBLANK# should be left as left as NC (“Not Connected”) if not used.
DVOBFLDSTL	I DVO	**TV Field and Flat Panel Stall Signa**l. This input can be programmed to be either a TV Field input from the TV encoder or Stall input from the flat panel. DVOB TV Field Signal: When used as a Field input, it synchronizes the overlay field with the TV encoder field when the overlay is displaying an interleaved source. DVOB Flat Panel Stall Signal: When used as the Stall input, it indicates that the pixel pipeline should stall one horizontal line. The signal changes during horizontal blanking. The panel fitting logic, when expanding the image vertically, uses this. DVOBFLDSTL needs to be pulled down if not used.

5.2 Intel 855GM/GME North Bridge(8)

DVOB and DVOC Port Common Signal Descriptions

Name	Type	Description
DVOBCINTR#	I DVO	**DVOBC Interrupt**: This pin is used to signal an interrupt, typically used to indicate a hot plug or unplug of a digital display.
ADDID[7:0]	I DVO	**ADDID[7:0]**: These pins are used to communicate to the Video BIOS when an external device is interfaced to the DVO port. **Note**: Bit[7] needs to be strapped low when an on-board DVO device is present. The other pins should be left as NC.
DVODETECT	I DVO	**DVODETECT**: This strapping signal indicates to the GMCH whether a DVO device is present or not. When a DVO device is connected, then DVODETECT = 0.

Analog CRT Display Signal Descriptions

Pin Name	Type	Description
VSYNC	O CMOS	**CRT Vertical Synchronization**: This signal is used as the vertical sync signal.
HSYNC	O CMOS	**CRT Horizontal Synchronization**: This signal is used as the horizontal sync signal.
RED	O Analog	**Red (Analog Video Output)**: This signal is a CRT Analog video output from the internal color palette DAC. The DAC is designed for a 37.5-§Ù equivalent load on each pin (e.g., 75-§Ù resistor on the board, in parallel with the 75-§Ù CRT load).
RED#	O Analog	**Red# (Analog Output):** Tied to ground.
GREEN	O Analog	**Green (Analog Video Output)**: This signal is a CRT analog video output from the internal color palette DAC. The DAC is designed for a 37.5-§Ù equivalent load on each pin (e.g.,75-§Ù resistor on the board, in parallel with the 75- §Ù CRT load).
GREEN#	O Analog	**Green# (Analog Output):** Tied to ground.
BLUE	O Analog	**Blue (Analog Video Output)** : This signal is a CRT Analog video output from the internal color palette DAC. The DAC is designed for a 37.5-§Ù equivalent load on each pin (e.g., 75- ohm resistor on the board, in parallel with the 75-§Ù CRT load).
BLUE#	O Analog	**Blue# (Analog Output):** Tied to ground.

Digital Video Output C (DVOC) Port Signal Descriptions

Name	Type	Description
DVOCD[11:0]	O DVO	**DVOC Data**: This data bus is used to drive 12-bit RGB data on each edge of the differential clock signals, DVOCCLK and DVOCCLK#. This provides 24-bits of data per clock period. In dual channel mode, this provides the upper 12-bits of pixel data. DVOCD[11:0] should be left as left as NC (“Not Connected”) if not used.
DVOCHSYNC	O DVO	**Horizontal Sync**: HSYNC signal for the DVOC interface. DVOCHSYNC should be left as left as NC (“Not Connected”) if not used.
DVOCVSYNC	O DVO	**Vertical Sync**: VSYNC signal for the DVOC interface. DVOCVSYNC should be left as left as NC (“Not Connected”) if the signal is NOT used when using internal graphics device.
DVOCBLANK#	O DVO	**Flicker Blank or Border Period Indication**: **DVOCBLANK#** is a programmable output pin driven by the GMCH. When programmed as a blank period indication, this pin indicates active pixels excluding the border. When programmed as a border period indication, this pin indicates active pixel including the border pixels. DVOCBLANK# should be left as left as NC (“Not Connected”) if not used.
DVOCFLDSTL	I DVO	**TV Field and Flat Panel Stall Signal**. This input can be programmed to be either a TV Field input from the TV encoder or Stall input from the flat panel. DVOC TV Field Signal: When used as a Field input, it synchronizes the overlay field with the TV encoder field when the overlay is displaying an interleaved source. DVOC Flat Panel Stall Signal: When used as the Stall input, it indicates that the pixel pipeline should stall one horizontal line. The signal changes during horizontal blanking. The panel fitting logic, when expanding the image vertically, uses this. DVOCFLDSTL needs to be pulled down if not used.

5.2 Intel 855GM/GME North Bridge(9)

GPIO Signal Descriptions

GPIO I/F Total	Type	Comments
RSTIN#	I CMOS	**Reset:** Primary Reset, Connected to PCIRST# of ICH4-M.
PWROK	I CMOS	**Power OK**: Indicates that power to GMCH is stable.
AGPBUSY#	O CMOS	**AGPBUSY:** Output of the GMCH IGD to the ICH4-M, which indicates that certain graphics activity is taking place. It will indicate to the ACPI software not to enter the C3 state. It will also cause a C3/C4 exit if C3/C4 was being entered, or was already entered when AGPBUSY# went active. Not active when the IGD is in any ACPI state other than D0.
EXTTS_0	I CMOS	**External Thermal Sensor Input:** This signal is an active low input to the GMCH and is used to monitor the thermal condition around the system memory and is used for triggering a read throttle. The GMCH can be optionally programmed to send a SERR, SCI, or SMI message to the ICH4-M upon the triggering of this signal.
LCLKCTLA	O CMOS	**SSC Chip Clock Control:** Can be used to control an external clock chip with SSC control.
LCLKCTLB	O CMOS	**SSC Chip Data Control:** Can be used to control an external clock chip for SSC control.
PANELVDDEN	O CMOS	**LVDS LCD Flat Panel Power Control:** This signal is used enable power to the panel interface.
PANELBKLTEN	O CMOS	**LVDS LCD Flat Panel Backlight Enable:** This signal is used to enable the backlight inverter (BLI)
PANELBKLTCTL	O CMOS	**LVDS LCD Flat Panel Backlight Brightness Control:** This signal is used as the Pulse Width Modulated (PWM) control signal to control the backlight inverter.
DDCACLK	I/O CMOS	**CRT DDC Clock:** This signal is used as the DDC clock signal between the CRT monitor and the GMCH.
DDCADATA	I/O CMOS	**CRT DDC Data:** This signal is used as the DDC data signal between the CRT monitor and the GMCH.
DDCPCLK	I/O CMOS	**Panel DDC Clock:** This signal is used as the DDC clock signal between the LFP and the GMCH.
DDCPDATA	I/O CMOS	**Panel DDC Data:** This signal is used as the DDC data signal between the LFP and the GMCH.

GPIO Signal Descriptions(Continued)

GPIO I/F Total	Type	Comments
MI2CCLK	I/O DVO	**DVO I2C Clock:** This signal is used as the I2C_CLK for a digital display (i.e. TV-Out Encoder, TMDS transmitter). This signal is tri-stated during a hard reset.
MI2CDATA	I/O DVO	**DVO I2C Data:** This signal is used as the I2C_DATA for a digital display (i.e. TV-Out Encoder, TMDS transmitter). This signal is tri-stated during a hard reset.
MDVICLK	I/O DVO	**DVI DDC Clock:** This signal is used as the DDC clock for a digital display connector (i.e. primary digital monitor). This signal is tri-stated during a hard reset.
MDVIDATA	I/O DVO	**DVI DDC Data:** The signal is used as the DDC data for a digital display connector (i.e. primary digital monitor). This signal is tri-stated during a hard reset.
MDDCDATA	I/O DVO	**DVI DDC Clock:** The signal is used as the DDC data for a digital display connector (i.e. secondary digital monitor). This signal is tri-stated during a hard reset.
MDDCCLK	I/O DVO	**DVI DDC Data:** The signal is used as the DDC clock for a digital display connector (i.e. secondary digital monitor). This signal is tri-stated during a hard reset.

5.3 Intel 82801DBM I/O Controller Hub 4 Mobile (ICH4-M)(1)

Hub Interface Signals

Signal Name	Type	Description
HI[11:0]	I/O	**Hub Interface Signals**
HI_STB/HI_STBS	I/O	**Hub Interface Strobe/ Hub Interface Strobe Second:** One of two differential strobe signals used to transmit and receive data through the hub interface. Hub Interface 1.5 mode this signal is not differential and is the second of the two strobe signals.
HI_STB#/ HI_STBF	I/O	**Hub Interface Strobe Complement / Hub Interface Strobe First:** One of two differential strobe signals used to transmit and receive data through the hub interface. Hub Interface 1.5 mode this signal is not differential and is the first of the two strobe signals.
HICOMP	I/O	**Hub Interface Compensation:** Used for hub interface buffer compensation.
HI_VSWING	I	**Hub Interface Voltage Swing:** Analog input used to control the voltage swing and impedance strength of hub interface pins.

LAN Connect Interface Signals

Signal Name	Type	Description
LAN_CLK	I	**LAN I/F Clock:** Driven by the LAN Connect component. Frequency range is 5 MHz to 50 MHz.
LAN_RXD[2:0]	I	**Received Data:** The LAN Connect component uses these signals to transfer data and control information to the integrated LAN Controller. These signals have integrated weak pull-up resistors.
LAN_TXD[2:0]	O	**Transmit Data**: The integrated LAN Controller uses these signals to transfer data and control information to the LAN Connect component.
LAN_RSTSYNC	O	**LAN Reset/Sync:** The LAN Connect component's Reset and Sync signals are multiplexed onto this pin.

EEPROM Interface Signals

Signal Name	Type	Description
EE_SHCLK	O	**EEPROM Shift Clock**: Serial shift clock output to the EEPROM.
EE_DIN	I	**EEPROM Data In**: Transfers data from the EEPROM to the ICH3. This signal has an integrated pull-up resistor.
EE_DOUT	O	**EEPROM Data Out**: Transfers data from the ICH3 to the EEPROM.
EE_CS	O	**EEPROM Chip Select**: Chip select signal to the EEPROM.

Firmware Hub Interface Signals

Signal Name	Type	Description
FWH[3:0]/ LAD[3:0]	I/O	**Firmware Hub Signals.** Muxed with LPC address signals.
FWH[4]/ LFRAME#	I/O	LFRAME# **Firmware Hub Signals.** Muxed with LPC LFRAME# signal.

PCI Interface Signals

Signal Name	Type	Description
AD[31:0]	I/O	**PCI Address/Data:** AD[31:0] is a multiplexed address and data bus. During the first clock of a transaction, AD[31:0] contain a physical address (32 bits). During subsequent clocks, AD[31:0] contain data. The ICH4 drives all 0s on AD[31:0] during the address phase of all PCI Special Cycles.
C/BE[3:0]#	I/O	**Bus Command and Byte Enables:** The command and byte enable signals are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE[3:0]# define the bus command. During the data phase, C/BE[3:0]# define the Byte Enables. **C/BE[3:0]# Command Type** 0 0 0 0 Interrupt Acknowledge 0 0 0 1 Special Cycle 0 0 1 0 I/O Read 0 0 1 1 I/O Write 0 1 1 0 Memory Read 0 1 1 1 Memory Write 1 0 1 0 Configuration Read 1 0 1 1 Configuration Write 1 1 0 0 Memory Read Multiple 1 1 1 0 Memory Read Line 1 1 1 1 Memory Write and Invalidate All command encodings not shown are reserved. The ICH4 does not decode reserved values, and therefore will not respond if a PCI master generates a cycle using one of the reserved values.
DEVSEL#	I/O	**Device Select:** The ICH4 asserts DEVSEL# to claim a PCI transaction. As an output, the ICH4 asserts DEVSEL# when a PCI master peripheral attempts an access to an internal ICH4 address or an address destined for the hub interface (main memory or AGP). As an input, DEVSEL# indicates the response to an ICH4-initiated transaction on the PCI bus. DEVSEL# is tri-stated from the leading edge of PCIRST#. DEVSEL# remains tri-stated by the ICH4 until driven by a Target device.

5.3 Intel 82801DBM I/O Controller Hub 4 Mobile (ICH4-M)(2)

PCI Interface Signals (Continued)

Signal Name	Type	Description
FRAME#	I/O	**Cycle Frame:** The current Initiator drives FRAME# to indicate the beginning and duration of a PCI transaction. While the Initiator asserts FRAME#, data transfers continue. When the Initiator negates FRAME#, the transaction is in the final data phase. FRAME# is an input to the ICH4 when the ICH4 is the Target, and FRAME# is an output from the ICH4 when the ICH4 is the Initiator. FRAME# remains tri- stated by the ICH4 until driven by an Initiator.
IRDY#	I/O	**Initiator Ready:** IRDY# indicates the ICH4's ability, as an Initiator, to complete the current data phase of the transaction. It is used in conjunction with TRDY#. A data phase is completed on any clock that both IRDY# and TRDY# are sampled asserted. During a write, IRDY# indicates the ICH4 has valid data present on AD[31:0]. During a read, it indicates the ICH4 is prepared to latch data. IRDY# is an input to the ICH4 when the ICH4 is the Target and an output from the ICH4 when the ICH4 is an Initiator. IRDY# remains tri-stated by the ICH4 until driven by an Initiator.
TRDY#	I/O	**Target Ready:** TRDY# indicates the ICH4's ability, as a Target, to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed when both TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that the ICH4, as a Target, has placed valid data on AD[31:0]. During a write, TRDY# indicates that the ICH4, as a Target, is prepared to latch data. TRDY# is an input to the ICH4 when the ICH4 is the Initiator and an output from the ICH4 when the ICH4 is a Target. TRDY# is tri-stated from the leading edge of PCIRST#. TRDY# remains tri-stated by the ICH4 until driven by a target.
PAR	I/O	**Calculated/Checked Parity:** PAR uses “even” parity calculated on 36 bits, AD[31:0] plus C/BE[3:0]#. “Even” parity means that the ICH4 counts the number of 1s within the 36 bits plus PAR and the sum is always even. The ICH4 always calculates PAR on 36 bits regardless of the valid byte enables. The ICH4 generates PAR for address and data phases and only guarantees PAR to be valid one PCI clock after the corresponding address or data phase. The ICH4 drives and tri-states PAR identically to the AD[31:0] lines except that the ICH4 delays PAR by exactly one PCI clock. PAR is an output during the address phase (delayed one clock) for all ICH4 initiated transactions. PAR is an output during the data phase (delayed one clock) when the ICH4 is the Initiator of a PCI write transaction, and when it is the Target of a read transaction. ICH4 checks parity when it is the Target of a PCI write transaction. If a parity error is detected, the ICH4 will set the appropriate internal status bits, and has the option to generate an NMI# or SMI#.

PCI Interface Signals (Continued)

Signal Name	Type	Description
STOP#	I/O	**Stop:** STOP# indicates that the ICH4, as a Target, is requesting the Initiator to stop the current transaction. STOP# causes the ICH4, as an Initiator, to stop the current transaction. STOP# is an output when the ICH4 is a Target and an input when the ICH4 is an Initiator. STOP# is tri-stated from the leading edge of PCIRST#. STOP# remains tri-stated until driven by the ICH4.
PERR#	I/O	**Parity Error:** An external PCI device drives PERR# when it receives data that has a parity error. The ICH4 drives PERR# when it detects a parity error. The ICH4 can either generate an NMI# or SMI# upon detecting a parity error (either detected internally or reported via the PERR# signal).
REQ[4:0]# **REQ[5]#/** REQ[B]#/ GPIO[1]	I	**PCI Requests:** The ICH4 supports up to 6 masters on the PCI bus. REQ[5]# is muxed with PC/PCI REQ[B]# (must choose one or the other, but not both). If not used for PCI or PC/PCI, REQ[5]#/REQ[B]# can instead be used as GPIO[1]. **NOTE:** REQ[0]# is programmable to have improved arbitration latency for for supporting PCI-based 1394 controllers.
GNT[4:0]# **GNT[5]#/** GNT[B]#/ GPIO[17]	O	**PCI Grants:** The ICH4 supports up to 6 masters on the PCI bus. GNT[5]# is muxed with PC/PCI GNT[B]# (must choose one or the other, but not both). If not needed for PCI or PC/PCI, GNT[5]# can instead be used as a GPIO. Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3 power rail. GNT[B]#/GNT[5]#/GPIO[17] has an internal pull-up.
PCICLK	I	**PCI Clock:** This is a 33 MHz clock. PCICLK provides timing for all transactions on the PCI Bus. **NOTE:** This clock does not stop based on STP_PCI# signal. PCICLK only stops based on SLP_S1# or SLP_S3#.
PCIRST#	O	**PCI Reset:** ICH4 asserts PCIRST# to reset devices that reside on the PCI bus. The ICH4 asserts PCIRST# during power-up and when S/W initiates a hard reset sequence through the RC (CF9h) register. The ICH4 drives PCIRST# inactive a minimum of 1 ms after PWROK is driven active. The ICH4 drives PCIRST# active a minimum of 1 ms when initiated through the RC register.
PLOCK#	I/O	**PCI Lock:** This signal indicates an exclusive bus operation and may require multiple transactions to complete. ICH4 asserts PLOCK# when it performs non- exclusive transactions on the PCI bus. Devices on the PCI bus (other than the ICH4) are not permitted to assert the PLOCK# signal.
SERR#	I/OD	**System Error:** SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, the ICH4 has the ability to generate an NMI, SMI#, or interrupt.

5.3 Intel 82801DBM I/O Controller Hub 4 Mobile (ICH4-M)(3)

PCI Interface Signals (Continued)

Signal Name	Type	Description
PME#	I/OD	**PCI Power Management Event:** PCI peripherals drive PME# to wake the system from low-power states S1-M–S5. PME# assertion can also be enabled to generate an SCI from the S0 state. In some cases the ICH4 may drive PME# active due to an internal wake event. The ICH4 will not drive PME# high, but it will be pulled up to VccSus3_3 by an internal pull-up resistor.
CLKRUN#	I/O	**PCI Clock Run:** Used to support PCI Clock Run protocol. Connects to PCI devices that need to request clock re-start, or prevention of clock stopping. **NOTE:** An external pull-up to the core power plane is required.
REQ[A]#/ GPIO[0] **REQ[B]#/** REQ[5]#/ GPIO[1]	I	**PC/PCI DMA Request [A:B]:** This request serializes ISA-like DMA Requests for the purpose of running ISA-compatible DMA cycles over the PCI bus. This is used by devices such as PCI based Super I/O or audio codecs which need to perform legacy 8237 DMA but have no ISA bus. When not used for PC/PCI requests, these signals can be used as General Purpose Inputs. REQ[B]# can instead be used as the 6th PCI bus request.
GNT[A]#/ GPIO[16] **GNT[B]#/** GNT[5]#/ GPIO[17]	O	**PC/PCI DMA Acknowledges [A: B]:** This grant serializes an ISA-like DACK# for the purpose of running DMA/ISA Master cycles over the PCI bus. This is used by devices such as PCI based Super/IO or audio codecs which need to perform legacy 8237 DMA but have no ISA bus. When not used for PC/PCI, these signals can be used as General Purpose Outputs. GNTB# can also be used as the 6th PCI bus master grant output. These signal have internal pull-up resistors.

IDE Interface Signals

Signal Name	Type	Description
PDCS1#, SDCS1#	O	**Primary and Secondary IDE Device Chip Selects for 100 Range:** For ATA command register block. This output signal is connected to the corresponding signal on the primary or secondary IDE connector.
PDCS3#, SDCS3#	O	**Primary and Secondary IDE Device Chip Select for 300 Range:** For ATA control register block. This output signal is connected to the corresponding signal on the primary or secondary IDE connector.
PDA[2:0], SDA[2:0]	O	**Primary and Secondary IDE Device Address:** These output signals are connected to the corresponding signals on the primary or secondary IDE connectors. They are used to indicate which byte in either the ATA command block or control block is being addressed.

IDE Interface Signals (Continued)

Signal Name	Type	Description
PDD[15:0], SDD[15:0]	I/O	**Primary and Secondary IDE Device Data:** These signals directly drive the corresponding signals on the primary or secondary IDE connector. There is a weak internal pull-down resistor on PDD[7] and SDD[7].
PDDREQ, SDDREQ	I	**Primary and Secondary IDE Device DMA Request:** These input signals are directly driven from the DRQ signals on the primary or secondary IDE connector. It is asserted by the IDE device to request a data transfer, and used in conjunction with the PCI bus master IDE function and are not associated with any AT compatible DMA channel. There is a weak internal pull-down resistor on these signals.
PDDACK#, SDDACK#	O	**Primary and Secondary IDE Device DMA Acknowledge:** These signals directly drive the DAK# signals on the primary and secondary IDE connectors. Each is asserted by the ICH4 to indicate to IDE DMA slave devices that a given data transfer cycle (assertion of DIOR# or DIOW#) is a DMA data transfer cycle. This signal is used in conjunction with the PCI bus master IDE function and are not associated with any AT-compatible DMA channel.
PDIOR#/ (PDWSTB/PRDMARDY#) **SDIOR#/** (SDWSTB/SRDMARDY#)	O	**Primary and Secondary Disk I/O Read (PIO and Non-Ultra DMA):** This is the command to the IDE device that it may drive data onto the PDD or SDD lines. Data is latched by the ICH4 on the deassertion edge of PDIOR# or SDIOR#. The IDE device is selected either by the ATA register file chip selects (PDCS1# or SDCS1#, PDCS3# or SDCS3#) and the PDA or SDA lines, or the IDE DMA acknowledge (PDDAK# or SDDAK#). Primary and Secondary Disk Write Strobe (Ultra DMA Writes to Disk): This is the data write strobe for writes to disk. When writing to disk, ICH4 drives valid data on rising and falling edges of PDWSTB or SDWSTB. Primary and Secondary Disk DMA Ready (Ultra DMA Reads from Disk): This is the DMA ready for reads from disk. When reading from disk, ICH4 deasserts PRDMARDY# or SRDMARDY# to pause burst data transfers.
PDIOW#/ (PDSTOP) **SDIOW#/** (SDSTOP)	O	**Primary and Secondary Disk I/O Write (PIO and Non-Ultra DMA):** This is the command to the IDE device that it may latch data from the PDD or SDD lines. Data is latched by the IDE device on the deassertion edge of PDIOW# or SDIOW#. The IDE device is selected either by the ATA register file chip selects (PDCS1# or SDCS1#, PDCS3# or SDCS3#) and the PDA or SDA lines, or the IDE DMA acknowledge (PDDAK# or SDDAK#). Primary and Secondary Disk Stop (Ultra DMA): ICH4 asserts this signal to terminate a burst.

5.3 Intel 82801DBM I/O Controller Hub 4 Mobile (ICH4-M)(4)

IDE Interface Signals (Continued)

Signal Name	Type	Description
PIORDY#/ (PDRSTB/PWDMARDY#) **SIORDY#/** (SDRSTB/SWDMARDY#)	I	**Primary and Secondary I/O Channel Ready (PIO):** This signal will keep the strobe active (PDIOR# or SDIOR# on reads, PDIOW# or SDIOW# on writes) longer than the minimum width. It adds wait states to PIO transfers. Primary and Secondary Disk Read Strobe (Ultra DMA Reads from Disk): When reading from disk, the ICH4 latches data on rising and falling edges of this signal from the disk. Primary and Secondary Disk DMA Ready (Ultra DMA Writes to Disk): When writing to disk, this is de-asserted by the disk to pause burst data transfers.

Interrupt Signals

Signal Name	Type	Description
SERIRQ	I/O	**Serial Interrupt Request:** This pin implements the serial interrupt protocol.
PIRQ[D:A]#	I/OD	**PCI Interrupt Requests:** In Non-APIC Mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described in the Interrupt Steering section. Each PIRQx# line has a separate Route Control Register. In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQ[A]# is connected to IRQ16, PIRQ[B]# to IRQ17, PIRQ[C]# to IRQ18, and PIRQ[D]# to IRQ19. This frees the legacy interrupts.
PIRQ[H:E]#/ GPIO[5:2]	I/OD	**PCI Interrupt Requests:** In Non-APIC Mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described in the Interrupt Steering section. Each PIRQx# line has a separate Route Control Register. In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQ[E]# is connected to IRQ20, PIRQ[F]# to IRQ21, PIRQ[G]# to IRQ22, and PIRQ[H]# to IRQ23. This frees the legacy interrupts. If not needed for interrupts, these signals can be used as GPIO.
IRQ[14:15]	I	**Interrupt Request 14:15:** These interrupt inputs are connected to the IDE drives. IRQ14 is used by the drives connected to the Primary controller and IRQ15 is used by the drives connected to the Secondary controller.
APICCLK	I	**APIC Clock:** This clock operates up to 33.33 MHz.
APICD[1:0]	I/OD	**APIC Data:** These bi-directional open drain signals are used to send and receive data over the APIC bus. As inputs the data is valid on the rising edge of APICCLK. As outputs, new data is driven from the rising edge of the APICCLK.

LPC Interface Signals

Signal Name	Type	Description
LAD[3:0]/ FWH[3:0]	I/O	**LPC Multiplexed Command, Address, Data:** For the LAD[3:0] signals, internal pull-ups are provided.
LFRAME#/ FWH[4]	O	**LPC Frame:** LFRAME# indicates the start of an LPC cycle, or an abort.
LDRQ[1:0]#	I	**LPC Serial DMA/Master Request Inputs:** LDRQ[1:0]# are used to request DMA or bus master access. These signals are typically connected to an external Super I/O device. An internal pull-up resistor is provided on these signals.

USB Interface Signals

Signal Name	Type	Description
USBP0P, USBP0N, USBP1P, USBP1N	I/O	**Universal Serial Bus Port 1:0 Differential:** These differential pairs are used to transmit data/address/command signals for ports 0 and 1. These ports can be routed to USB UHCI Controller #1 or the USB EHCI Controller. **NOTE:** No external resistors are required on these signals. The ICH4 integrates 15 k . pull-downs and provides an output driver impedance of 45 . which requires no external series resistor
USBP2P, USBP2N, USBP3P, USBP3N	I/O	**Universal Serial Bus Port 3:2 Differential:** These differential pairs are used to transmit data/address/command signals for ports 2 and 3. These ports can be routed to USB UHCI Controller #2 or the USB EHCI Controller. **NOTE:** No external resistors are required on these signals. The ICH4 integrates 15 k . pull-downs and provides an output driver impedance of 45 . which requires no external series resistor.
USBP4P, USBP4N, USBP5P, USBP4N	I/O	**Universal Serial Bus Port 5:4 Differential:** These differential pairs are used to transmit data/address/command signals for ports 4 and 5. These ports can be routed to USB UHCI Controller #3 or the USB EHCI Controller **NOTE:** No external resistors are required on these signals. The ICH4 integrates 15 k . pull-downs and provides an output driver impedance of 45 . which requires no external series resistor
OC[5:0]#	I/O	**Overcurrent Indicators:** These signals set corresponding bits in the USB controllers to indicate that an overcurrent condition has occurred.
USBRBIAS	O	**USB Resistor Bias:** Analog connection point for an external resistor to ground. USBRBIAS should be connected to USBRBIAS# as close to the resistor as possible.
USBRBIAS#	I	**USB Resistor Bias Complement:** Analog connection point for an external resistor to ground. USBRBIAS# should be connected to USBRBIAS as close to the resistor as possible.

5.3 Intel 82801DBM I/O Controller Hub 4 Mobile (ICH4-M)(5)

Power Management Interface Signals

Signal Name	Type	Description
THRM#	I	**Thermal Alarm:** This is an active low signal generated by external hardware to start the hardware clock throttling mode. The signal can also generate an SMI# or an SCI.
THRMTRIP#	I	**Thermal Trip:** When low, THRMTRIP# indicates that a thermal trip from the processor occurred; the ICH4 will immediately transition to a S5 state. The ICH4 will not wait for the processor stop grant cycle since the processor has overheated.
SLP_S1#	O	**S1 Sleep Control:** SLP_S1# provides Clock Synthesizer or Power plane control. Optional use is to shut off power to non-critical systems when in the S1- M (Powered On Suspend), S3 (Suspend To RAM), S4 (Suspend to Disk) or S5 (Soft Off) states.
SLP_S3#	O	**S3 Sleep Control:** SLP_S3# is for power plane control. It shuts off power to all non-critical systems when in S3 (Suspend To RAM), S4 (Suspend to Disk), or S5 (Soft Off) states.
SLP_S4#	O	**S4 Sleep Control:** SLP_S4# is for power plane control. It shuts power to all non-critical systems when in the S4 (Suspend to Disk) or S5 (Soft Off) state.
SLP_S5#	O	**S5 Sleep Control:** SLP_S5# is for power plane control. The signal is used to shut power off to all non-critical systems when in the S5 (Soft Off) states.
PWROK	I	**Power OK:** When asserted, PWROK is an indication to the ICH4 that core power and PCICLK have been stable for at least 1 ms. PWROK can be driven asynchronously. When PWROK is negated, the ICH4 asserts PCIRST#. **NOTE:** PWROK must deassert for a minimum of 3 RTC clock periods for the ICH4 to fully reset the power and properly generate the PCIRST# output
PWRBTN#	I	**Power Button:** The Power Button causes SMI# or SCI to indicate a system request to go to a sleep state. If the system is already in a sleep state, this signal causes a wake event. If PWRBTN# is pressed for more than 4 seconds, this causes an unconditional transition (power button override) to the S5 state with only the PWRBTN# available as a wake event. Override occurs even if the system is in the S1-M–S4 states. This signal has an internal pull-up resistor.
RI#	I	**Ring Indicate:** This signal is an input from the modem interface. It can be enabled as a wake event, and this is preserved across power failures.
SYS_RESET#	I	**System Reset:** This pin forces an internal reset after being debounced. The ICH4 will reset immediately if the SMBus is idle; otherwise, it will wait up to 25 ms ± 2 ms for the SMBus to idle before forcing a reset on the system.
RSMRST#	I	**Resume Well Reset:** This signal is used for resetting the resume power plane logic.

Power Management Interface Signals (Continued)

Signal Name	Type	Description
LAN_RST#	I	**LAN Reset:** This signal must be asserted at least 10 ms after the resume well power (VccLAN3_3 and VccLAN1_5 is valid. When deasserted, this signal is an indication that the resume well power is stable.
SUS_STAT#/ LPCPD#	O	**Suspend Status:** This signal is asserted by the ICH4 to indicate that the system will be entering a low power state soon. This can be monitored by devices with memory that need to switch from normal refresh to suspend refresh mode. It can also be used by other peripherals as an indication that they should isolate their outputs that may be going to powered-off planes. This signal is called LPCPD# on the LPC I/F.
C3_STAT#	O	**C3_STAT#:** This signal will typically be configured as C3_STAT#. It is used for indicating to an AGP device that a C3 state transition is beginning or ending. If C3_STAT# functionality is not required, this signal may be used as a GPO. **NOTE:** This signal will be asserted in S1-M on the ICH4-M.
SUSCLK	O	**Suspend Clock:** Output of the RTC generator circuit to use by other chips for refresh clock.
AGPBUSY#	I	**AGP Bus Busy:** To support the C3 state. This signal is an indication that the AGP device is busy. When this signal is asserted, the BM_STS bit will be set. If this functionality is not needed, this signal may be configured as a GPI.
STP_PCI#	O	**Stop PCI Clock:** This signal is an output to the external clock generator for it to turn off the PCI clock. Used to support PCI CLKRUN# protocol. If this functionality is not needed, This signal can be configured as a GPO.
STP_CPU#	O	**Stop CPU Clock:** Output to the external clock generator for it to turn off the processor clock. Used to support the C3 state. If this functionality is not needed, this signal can be configured as a GPO.
BATLOW#	I	**Battery Low:** This signal is an input from the battery to indicate that there is insufficient power to boot the system. Assertion will prevent wake from S1-M–S5 state. Can also be enabled to cause an SMI# when asserted.
CPUPERF#	OD	**CPU Performance:** CPUPERF# is used for Intel SpeedStep technology support. The signal selects which power state to put the processor in.
SSMUXSEL	O	**SpeedStep Mux Select:** SSMUXSEL is used for Intel SpeedStep technology support. The signal selects the voltage level for the processor.
VGATE/ VRMPWRGD	I	**VGATE/VRM Power Good:** VGATE/VRMPWRGD is used for Intel SpeedStep technology support. This is an output from the processor's voltage regulator to indicate that the voltage is stable. This signal may go inactive during an Intel SpeedStep transition.

5.3 Intel 82801DBM I/O Controller Hub 4 Mobile (ICH4-M)(6)

Power Management Interface Signals (Continued)

Signal Name	Type	Description
DPRSLPVR	O	**Deeper Sleep - Voltage Regulator:** This signal is used to lower the voltage of VRM during C4 and S1-M states. When the signal is high, the voltage regulator outputs the lower "Deeper Sleep" voltage. When the signal is low (default), the voltage regulator outputs the higher "Normal" voltage. During PCIRST#, the output driver is disabled and an internal pull-down is enabled. This is needed for implementing a strap on the pin. When PCIRST# deasserts, the output driver is enabled. To guarantee no glitches on the DPRSLPVR pin, the pull-down is disabled after the output driver is fully enabled. **NOTE:** DPRSLPVR is sampled at the rising edge of PWROK as a functional strap.

Processor Interface Signals

Signal Name	Type	Description
A20M#	O	**Mask A20:** A20M# will go active based on either setting the appropriate bit in the Port 92h register, or based on the A20GATE input being active. **Speed Strap:** During the reset sequence, ICH4 drives A20M# high if the corresponding bit is set in the FREQ_STRP register.
CPUSLP#	O	**CPU Sleep:** This signal puts the processor into a state that saves substantial power compared to Stop-Grant state. However, during that time, no snoops occur. The ICH4 can optionally assert the CPUSLP# signal when going to the S1-M state.
FERR#	I	**Numeric Coprocessor Error:** This signal is tied to the coprocessor error signal on the processor. FERR# is only used if the ICH4 coprocessor error reporting function is enabled in the General Control Register (Device 31:Function 0, Offset D0, bit 13). If FERR# is asserted, the ICH4 generates an internal IRQ13 to its interrupt controller unit. It is also used to gate the IGNNE# signal to ensure that IGNNE# is not asserted to the processor unless FERR# is active. FERR# requires an external weak pull-up to ensure a high level when the coprocessor error function is disabled. **NOTE:** FERR# can be used in some states for notification by the processor of pending interrupt events. This functionality is independent of the General Control Register bit setting.
INTR	O	**CPU Interrupt:** INTR is asserted by the ICH4 to signal the processor that an interrupt request is pending and needs to be serviced. It is an asynchronous output and normally driven low. **Speed Strap:** During the reset sequence, ICH4 drives INTR high if the corresponding bit is set in the FREQ_STRP register.

Processor Interface Signals (Continued)

Signal Name	Type	Description
IGNNE#	O	**Ignore Numeric Error:** This signal is connected to the ignore error pin on the processor. IGNNE# is only used if the ICH4 coprocessor error reporting function is enabled in the General Control Register (Device 31:Function 0, Offset D0, bit 13). If FERR# is active, indicating a coprocessor error, a write to the Coprocessor Error Register (F0h) causes the IGNNE# to be asserted. IGNNE# remains asserted until FERR# is negated. If FERR# is not asserted when the Coprocessor Error Register is written, the IGNNE# signal is not asserted. **Speed Strap:** During the reset sequence, ICH4 drives IGNNE# high if the corresponding bit is set in the FREQ_STRP register.
INIT#	O	**Initialization:** INIT# is asserted by the ICH4 for 16 PCI clocks to reset the processor. ICH4 can be configured to support CPU BIST. In that case, INIT# will be active when PCIRST# is active.
NMI	O	**Non-Maskable Interrupt:** NMI is used to force a non-Maskable interrupt to the processor. The ICH4 can generate an NMI when either SERR# or IOCHK# is asserted. The processor detects an NMI when it detects a rising edge on NMI. NMI is reset by setting the corresponding NMI source enable/disable bit in the NMI Status and Control Register. **Speed Strap:** During the reset sequence, ICH4 drives NMI high if the corresponding bit is set in the FREQ_STRP register.
SMI#	O	**System Management Interrupt:** SMI# is an active low output synchronous to PCICLK. It is asserted by the ICH4 in response to one of many enabled hardware or software events.
STPCLK#	O	**Stop Clock Request:** STPCLK# is an active low output synchronous to PCICLK. It is asserted by the ICH4 in response to one of many hardware or software events. When the processor samples STPCLK# asserted, it responds by stopping its internal clock.
RCIN#	I	**Keyboard Controller Reset CPU:** The keyboard controller can generate INIT# to the processor. This saves the external OR gate with the ICH4's other sources of INIT#. When the ICH4 detects the assertion of this signal, INIT# is generated for 16 PCI clocks. **NOTE:** The ICH4 ignores RCIN# assertion during transitions to the S1-M, S3, S4 and S5 states.
A20GATE	I	**A20 Gate:** A20GATE is from the keyboard controller. The signal acts as an alternative method to force the A20M# signal active. It saves the external OR gate needed with various other PCIsets.

5.3 Intel 82801DBM I/O Controller Hub 4 Mobile (ICH4-M)(7)

Processor Interface Signals (Continued)

Signal Name	Type	Description
CPUPWRGD	OD	**CPU Power Good:** This signal should be connected to the processor's PWRGOOD input. To allow for Intel ® SpeedStep™ technology support, this signal is kept high during an Intel SpeedStep technology state transition to prevent loss of processor context. This is an open-drain output signal (external pull-up resistor required) that represents a logical AND of the ICH4's PWROK and VGATE / VRMPWRGD signals.
DPSLP#	O	**Deeper Sleep:** This signal is asserted by the ICH4 to the processor. When the signal is low, the processor enters the Deeper Sleep state by gating off the processor Core clock inside the processor. When the signal is high (default), the processor is not in the Deeper Sleep state. This signal behaves identically to the STP_CPU# signal, but at the processor voltage level.

SMBus Interface Signals

Signal Name	Type	Description
SMBDATA	I/OD	**SMBus Data:** External pull-up is required.
SMBCLK	I/OD	**SMBus Clock:** External pull-up is required.
SMBALERT#/ GPIO[11]	I	**SMBus Alert:** This signal is used to wake the system or generate SMI#. If not used for SMBALERT#, it can be used as a GPI.

System Management Interface Signals

Signal Name	Type	Description
INTRUDER#	I	**Intruder Detect:** Can be set to disable system if box detected open. This signal's status is readable, so it can be used like a GPI if the Intruder Detection is not needed.
SMLINK[1:0]	I/OD	**System Management Link:** SMBus link to optional external system management ASIC or LAN controller. External pull-ups are required. Note that SMLINK[0] corresponds to an SMBus Clock signal, and SMLINK[1] corresponds to an SMBus Data signal.

Real Time Clock Interface Signals

Signal Name	Type	Description
RTCX1	Special	**Crystal Input 1:** This signal is connected to the 32.768 kHz crystal.
RTCX2	Special	**Crystal Input 2:** This signal is connected to the 32.768 kHz crystal.

Other Clock Signals

Signal Name	Type	Description
CLK14	I	**Oscillator Clock:** Used for 8254 timers. It runs at 14.31818 MHz. This clock is permitted to stop during S1-M (or lower) states.
CLK48	I	**48 MHz Clock:** This clock is used to run the USB controller. It runs at 48 MHz. This clock is permitted to stop during S1-M (or lower) states.
CLK66	I	**66 MHz Clock:** This is used to run the hub interface. It runs at 66 MHz. This clock is permitted to stop during S1-M (or lower) states.

Miscellaneous Signals

Signal Name	Type	Description
SPKR	O	**Speaker:** The SPKR signal is the output of counter 2 and is internally "ANDed" with Port 61h bit 1 to provide Speaker Data Enable. This signal drives an external speaker driver device, which in turn drives the system speaker. Upon PCIRST#, its output state is 0. **NOTE:** SPKR is sampled at the rising edge of PWROK as a functional strap.
RTCRST#	I	**RTC Reset:** When asserted, this signal resets register bits in the RTC well and sets the RTC_PWR_STS bit (bit 2 in GEN_PMCON3 register). **NOTES:** 1. Clearing CMOS in an ICH4-based platform can be done by using a jumper on RTCRST# or GPI, or using SAFEMODE strap. Implementations should not attempt to clear CMOS by using a jumper to pull VccRTC low. 2. Unless entering the XOR Chain Test Mode, the RTCRST# input must always be high when all other RTC power planes are on.

5.3 Intel 82801DBM I/O Controller Hub 4 Mobile (ICH4-M)(8)

AC'97 Link Signals

Signal Name	Type	Description
AC_RST#	O	**AC '97 Reset:** This signal is a master hardware reset to external Codec(s).
AC_SYNC	O	**AC '97 Sync:** This signal is a 48 kHz fixed rate sample sync to the Codec(s).
AC_BIT_CLK	I	**AC97 Bit Clock:** This signal is a 12.288 MHz serial data clock generated by the external Codec(s). This signal has an integrated pull-down resistor.
AC_SDOUT	O	**AC97 Serial Data Out:** Serial TDM data output to the Codec(s). **NOTE:** AC_SDOUT is sampled at the rising edge of PWROK as a functional strap.
AC_SDIN[1:0]	I	**AC97 Serial Data In 2:**0: These signals are Serial TDM data inputs from the three Codecs.

NOTE: An integrated pull-down resistor on AC_BIT_CLK is enabled when either: The ACLINK Shutoff bit in the AC'97 Global Control Register is set to 1, or Both Function 5 and Function 6 of Device 31 are disabled. Otherwise, the integrated pull-down resistor is disabled.

General Purpose I/O Signals

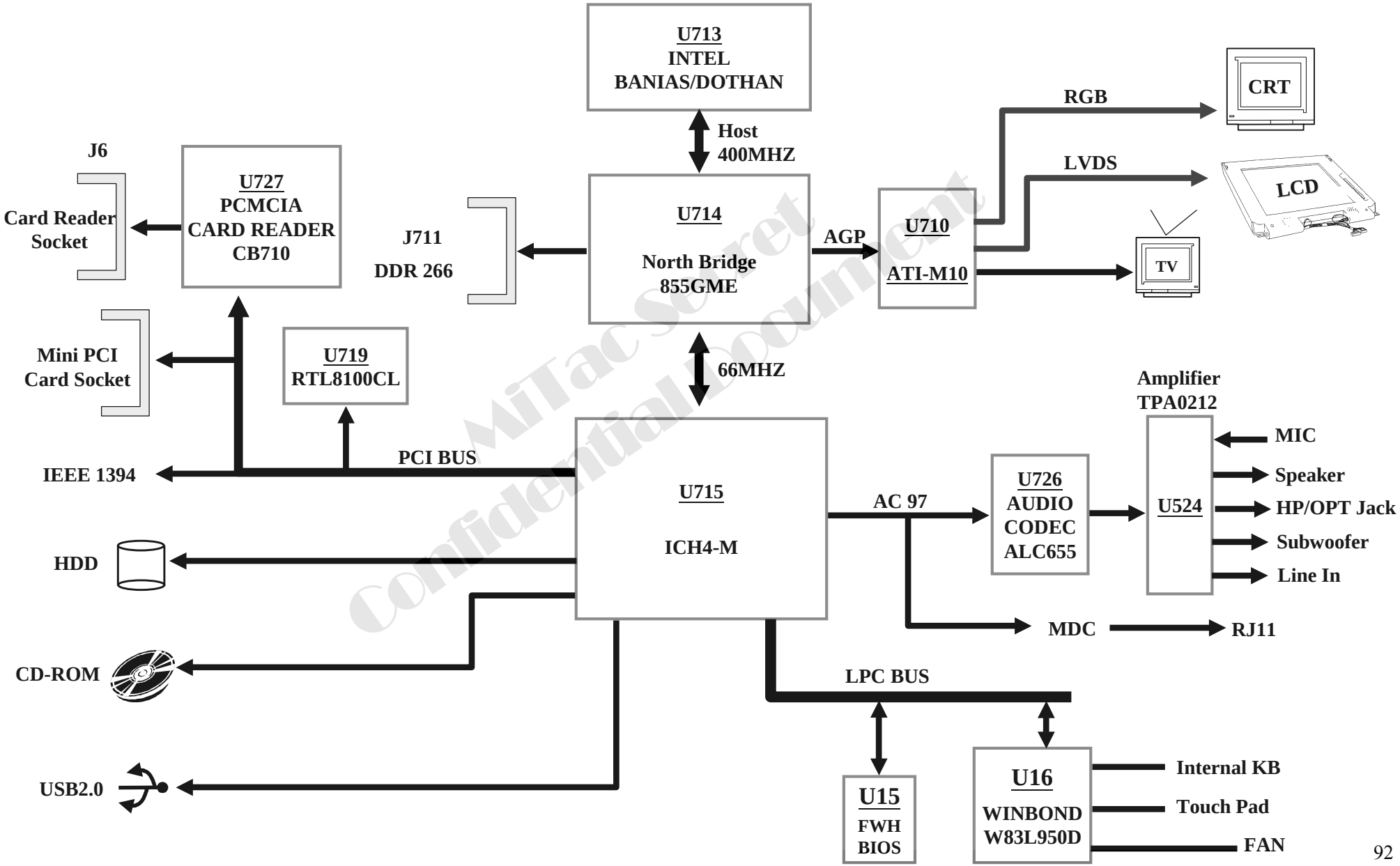
Signal Name	Type	Description
GPIO[43:32]	I/O	Can be input or output. Main power well.
GPIO[31:29]	O	Not implemented.
GPIO[28:27]	I/O	Can be input or output. Resume power well. Unmuxed.
GPIO[26]	I/O	Not implemented.
GPIO[25]	I/O	Can be input or output. Resume power well. Unmuxed.
GPIO[24:18]	I/O	Not Implemented in Mobile (Assign to native Functionality).
GPIO[17:16]	O	Fixed as Output only. Main power well. Can be used instead as PC/PCI GNT[A:B]#. GPIO[17] can also alternatively be used for PCI GNT[5]#. Integrated pull-up resistor.
GPIO[15:14]	I	Not implemented.
GPIO[13:12]	I	Fixed as Input only. Resume power well. Unmuxed.
GPIO[11]	I	Fixed as Input only. Resume power well. Can be used instead as SMBALERT#.
GPIO[10:9]	I	Not implemented.
GPIO[8]	I	Fixed as Input only. Resume power well. Unmuxed.
GPIO[7]	I	Fixed as Input only. Main power well. Unmuxed.
GPIO[6]	I	Not Implemented in Mobile (Assign to Native Functionality)
GPIO[5:2]	I	Fixed as Input only. Main power well. Can be used instead as PIRQ[E:H]#.
GPIO[1:0]	I	Fixed as Input only. Main power well. Can be used instead as PC/PCI REQ[A:B]#. GPIO[1] can also alternatively be used for PCI REQ[5]#.

NOTE: Main power well GPIO are 5V tolerant, except for GPIO[43:32]. Resume power well GPIO are not 5V tolerant.

Power and Ground Signals

Signal Name	Description
VCC3_3	3.3 V supply for core well I/O buffers. This power may be shut off in S3, S4, S5 or G3 states.
VCC1_5	1.5 V supply for core well logic. This power may be shut off in S3, S4, S5 or G3 states.
VCCHI	1.5 V supply for Hub Interface 1.5 logic. 1.8 V supply for Hub Interface 1.0 logic. This power may be shut off in S3, S4, S5 or G3 states.
V5REF	Reference for 5 V tolerance on core well inputs. This power may be shut off in S3, S4, S5 or G3 states.
HIREF	Analog Input. Expected voltages are: • 0.9 V for HI 1.0 (Normal Hub Interface) Series Termination • 350 mV for HI 1.5 (Enhanced Hub Interface) Parallel Termination This power is shut off in S3, S4, S5, and G3 states.
VCCSUS3_3	3.3 V supply for resume well I/O buffers. This power is not expected to be shut off unless the main battery is removed or completely drained and AC power is not available.
VCCSUS1_5	1.5 V supply for resume well logic. This power is not expected to be shut off unless the main battery is removed or completely drained and AC power is not available.
V5REF_SUS	Reference for 5 V tolerance on resume well inputs. This power is not expected to be shut off unless the main battery is removed or completely drained and AC power is not available.
VCCLAN3_3	3.3 V supply for LAN Connect interface buffers. This is a separate power plane that may or may not be powered in S3–S5 states depending upon the presence or absence of AC power and network connectivity. This plane must be on in S0 and S1-M.
VCCLAN1_5	1.5 V supply for LAN Controller logic. This is a separate power plane that may or may not be powered in S3–S5 states depending upon the presence or absence of AC power and network connectivity. This plane must be on in S0 and S1-M.
VCCRTC	3.3 V (can drop to 2.0 V min. in G3 state) supply for the RTC well. This power is not expected to be shut off unless the RTC battery is removed or completely drained. **NOTE:** Implementations should not attempt to clear CMOS by using a jumper to pull VccRTC low. Clearing CMOS in an ICH4-based platform can be done by using a jumper on RTCRST# or GPI, or using SAFEMODE strap.
VCCPLL	1.5 V supply for core well logic. This signal is used for the USB PLL. This power may be shut off in S3, S4, S5 or G3 states.
VBIAS	RTC well bias voltage. The DC reference voltage applied to this pin sets a current that is mirrored throughout the oscillator and buffer circuitry.
V_CPU_IO	Powered by the same supply as the processor I/O voltage. This supply is used to drive the processor interface outputs.
VSS	Grounds.

6. System Block Diagram



7. Maintenance Diagnostics

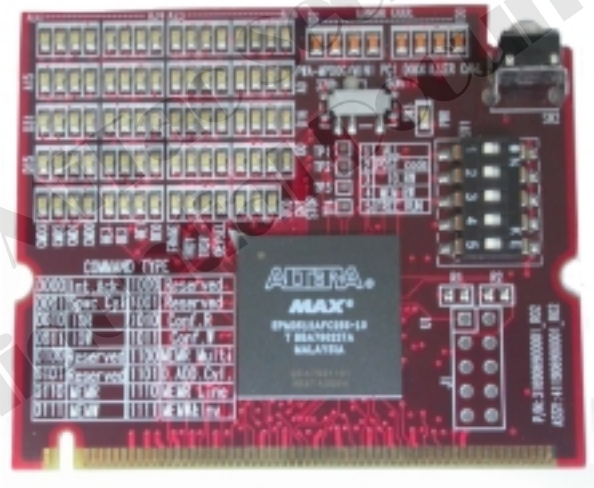
7.1 Introduction

Each time the computer is turned on, the system BIOS runs a series of internal checks on the hardware. This power-on self test (post) allows the computer to detect problems as early as the power-on stage. Error messages of post can alert you to the problems of your computer.If an error is detected during these tests, you will see an error message displayed on the screen. If the error occurs before the display is initialized, then the screen cannot display the error message. Error codes or system beeps are used to identify a post error that occurs when the screen is not available.

The value for the diagnostic port is written at the beginning of the test. Therefore, if the test failed, the user can determine where the problem occurred by reading the last value written to the port by the debug card plug at MINI PCI slot.

7.2 Diagnostic Tool for Mini PCI Slot :

The Mini PCI DOG killer card is a single-step debug tool which utilizes Mini PCI interface (Type III A) and is able to hold a PCI bus cycle so that address, data and control bus states on PCI bus can be inspected. Especially, the tool can help an engineer trace address/data bus for BIOS read cycles as soon as power on and debug open or short circuit problems easily. Usually, this sort of problem will make a PC motherboard fail to boot.



P/N:411906900001
Description: PWA-MPDOG;MINI PCI DOGKELLER CARD
Note: Order it from MIC/TSSC

7.3 Error Codes - 1

Following is a list of error codes in sequent display on the debug board.

POST (HEX)	DESCRIPTION
00h	Boot started
01h	Disable A20 through A20
02h	Initialize CS
03h	Test RAM
04h	Move BL into the RAM
05h	Execution in RAM
06h	Check OVERRIDE option
07h	Shadow System BIOS
08h	Checksum System BIOS ROM
09h	Proceed with Normal Boot
0Ah	Proceed with Crisis Boot
0Fh	Fatal Error
F0h	.... - No RAM
F1h	..._ - RAM test failed
99h	Resume SMRAM not Found
10H	Some Type Of Long Reset
11H	Turn off FASTA20 for POST
12H	Signal Power On Reset
13H	Initialize the Chipset
14H	Search For ISA Bus VGA Adapter
15H	Reset Counter/Timer 1
16H	user register config through CMOS

POST (HEX)	DESCRIPTION
17H	Size Memory
18H	Dispatch To RAM Test
19H	checksum the ROM
1AH	Reset PIC's
1BH	Initialize Video Adapter(s)
1CH	Initialize Video (6845 Regs)
1DH	Initialize Color Adapter
1EH	Initialize Monochrome Adapter
1FH	Test 8237A Page Registers
20H	Test Keyboard
21H	Test Keyboard Controller
22H	Check If CMOS Ram Valid
23H	Test Battery Fail & CMOS X-SUM
24H	Test the DMA controllers
25H	Initialize 8237A Controller
26H	Initialize Int Vectors
27H	RAM Quick Sizing
28H	Protected mode entered safely
29H	RAM test completed
2AH	Protected mode exit successful
2BH	Setup Shadow
2CH	Going To Initialize Video

7.3 Error Codes - 2

Following is a list of error codes in sequent display on the debug board.

POST (HEX)	DESCRIPTION
2DH	Search For Monochrome Adapter
2EH	Search For Color Adapter
2FH	Signon messages displayed
30H	special init of keyboard ctlr
31H	Test If Keyboard Present
32H	Test Keyboard Interrupt
33H	Test Keyboard Command Byte
34H	TEST, Blank and count all RAM
35H	Protected mode entered safely (2).
36H	RAM test complete
37H	Protected mode exit successful
38H	Update OUTPUT port
39H	Setup Cache Controller
3AH	Test If 18.2Hz Periodic Working
3BH	test for RTC ticking
3CH	initialize the hardware vectors
3DH	Search and Init the Mouse
3EH	Update NUMLOCK status
3FH	special init of COMM and LPT ports
40H	Configure the COMM and LPT ports
41H	Initialize the floppies

POST (HEX)	DESCRIPTION
42H	Initialize the hard disk
43H	Initialize option ROMs
44H	OEM's init of power management
45H	Update NUMLOCK status
46H	Test For Coprocessor Installed
47H	OEM functions before boot
48H	Dispatch To Op. Sys. Boot
49H	Jump Into Bootstrap Code
50H	ACPI INIT
51H	PM INIT & GEYSERVILLE CPU INIT
52H	USB HC INIT
F8H	PXE BIOS decomp error
F9H	PCI BIOS decomp error
FAH	PNP BIOS decomp error
FBH	LOGO BIOS decomp error
FCH	LOGO Image decomp error
FDH	Energy Image decomp error
FEH	ROMDEBUG Image decomp error
88H	PM code decomp error
CAH	CPU SMM remap code
CBH	CPU SMM BASE remap Done

7.3 Error Codes - 3

Following is a list of error codes in sequent display on the debug board.

POST (HEX)	DESCRIPTION
D0H	check rom signature, 1.x video
D1H	enable RAM area in regs
D2H	copy ROM to RAM in regs
D3H	update segment range attr
D4H	configure memory registers
D5H	configure I/O registers
D6H	configure IRQ assignments
D7H	turn on PCI device
D8H	2.x video r/w segment
D9H	OEM defined, rom init
DAH	disable add-in rom card decode
DBH	PCI return(config and no video)
DCH	enable RAM area in regs
DDH	copy ROM to RAM in regs
DEH	update segment range attr
DFH	configure memory registers
E0H	configure I/O registers
E1H	configure IRQ assignments
E2H	turn on PCI device
E3H	2.x video r/w segment
E4H	OEM defined, rom init

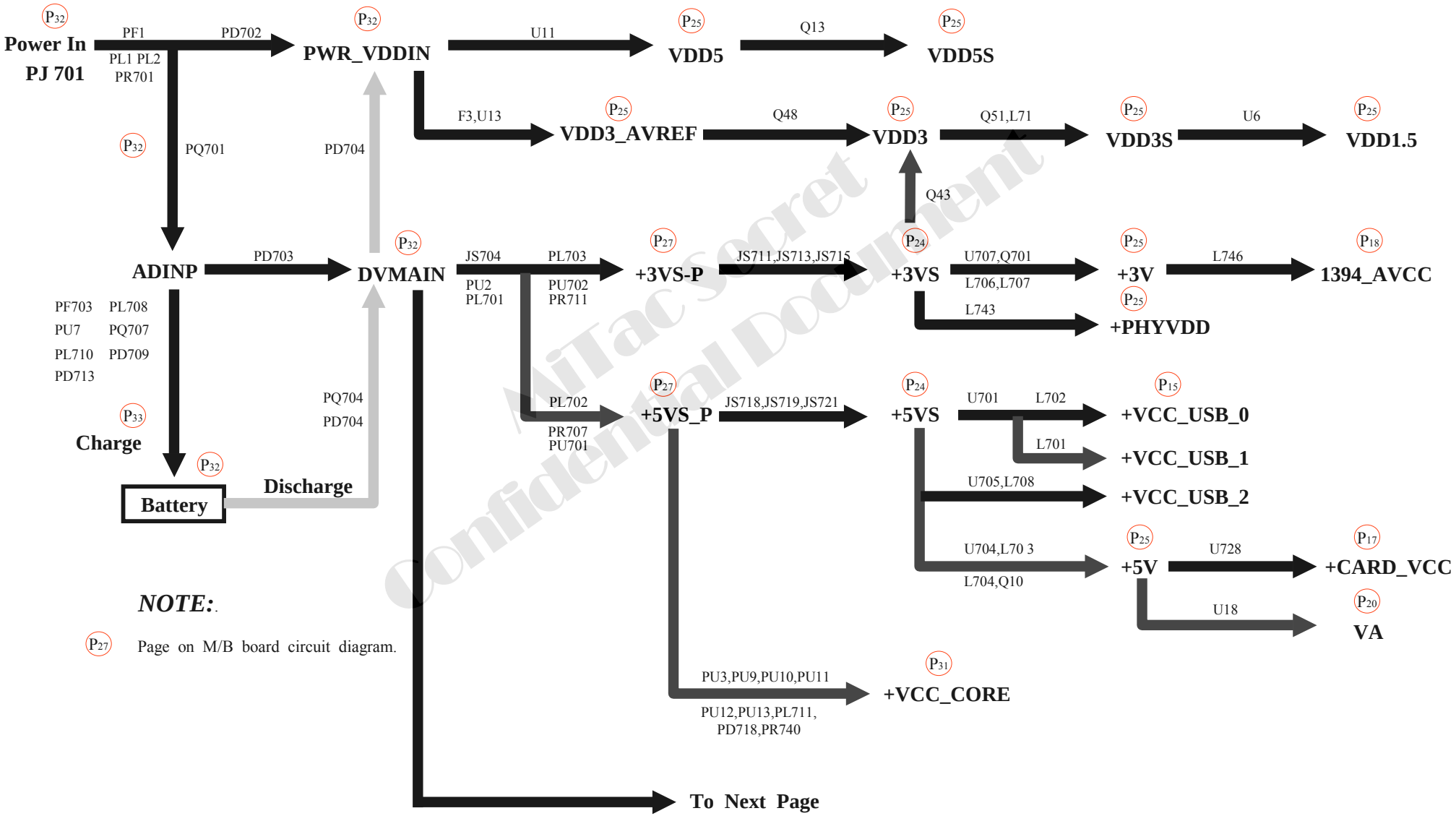
POST (HEX)	DESCRIPTION
E5H	disable add-in rom card decode
E6H	PCI return(config and no video)
E7H	look for PCI bridge device
E8H	search IDE controllers on the PCI bus
E9H	start of cardbus config
A1H	Enable/Verify R/W Status Runtime Data
A2H	Get/Verrify R/W Stattus NVRAM data area
A3H	Resolve System Nodes with the CMOS settings
A4H	Init. var. in the PNP BIOS Runtime Data area
A5H	Hook INT 15
A6H	copy/setup $PnP Install Check in F0000 seg.
A7H	Allow the OEM any Last Minute Hooks
A8H	Write protect RTData Area & NVRAM Copy Buffer
A9H	return from pnp_init proc

8. Trouble Shooting

- 8.1 No Power
- 8.2 Battery Can not Be Charged
- 8.3 No Display
- 8.4 External Monitor No Display
- 8.5 Memory Test Error
- 8.6 Keyboard/Touch pad Test Error
- 8.7 USB Port Test Error
- 8.8 Hard Disk Drive Test Error
- 8.9 CD-ROM Driver Test Error
- 8.10 Audio Failure
- 8.11 LAN Test Error
- 8.12 Modem Test Error
- 8.13 MINI-PCI Test Error
- 8.14 Card Bus&Reader Test Error
- 8.15 IEEE 1394 Failure

8.1 No Power

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



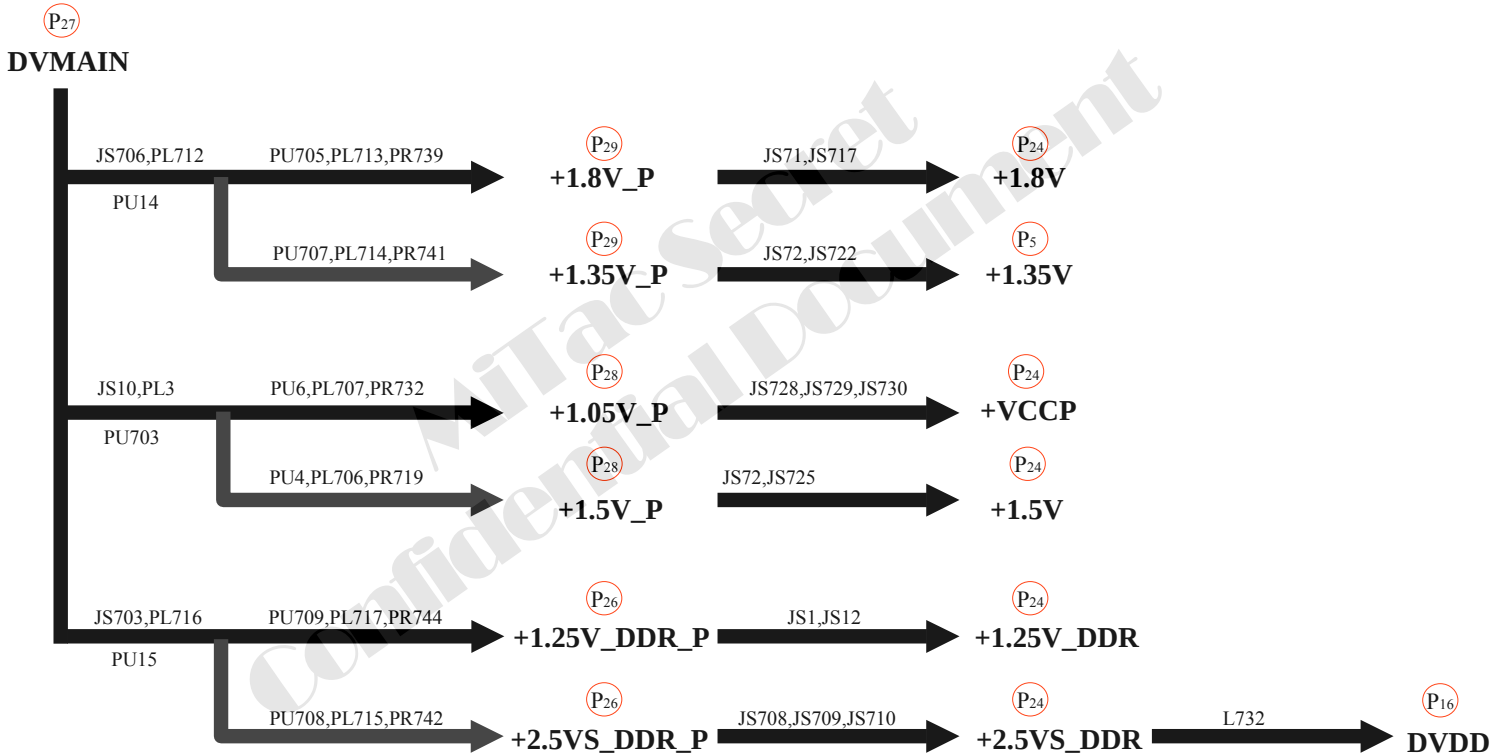
NOTE:.

P27 Page on M/B board circuit diagram.

8.1 No Power

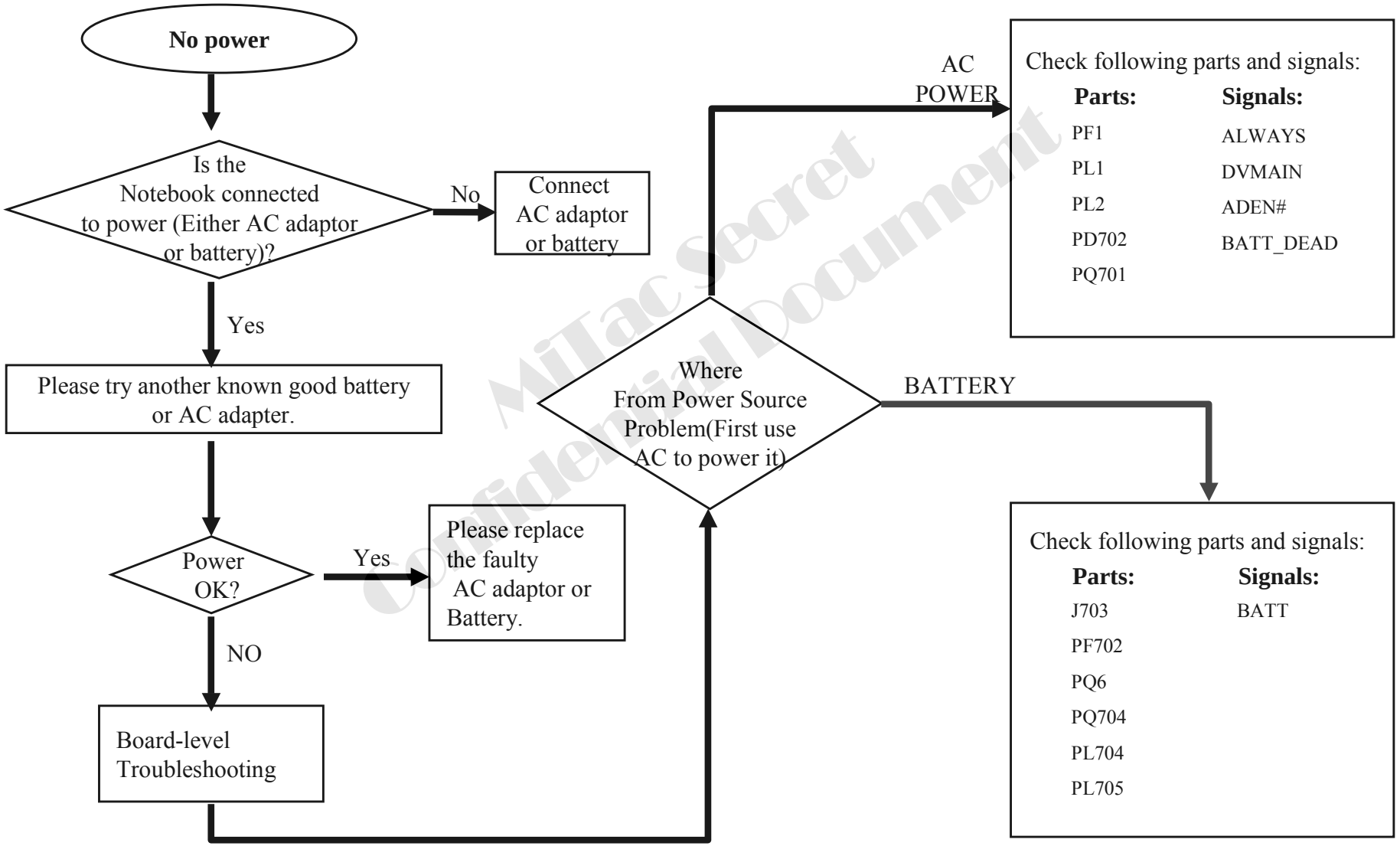
When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.

Continue To Previous Page



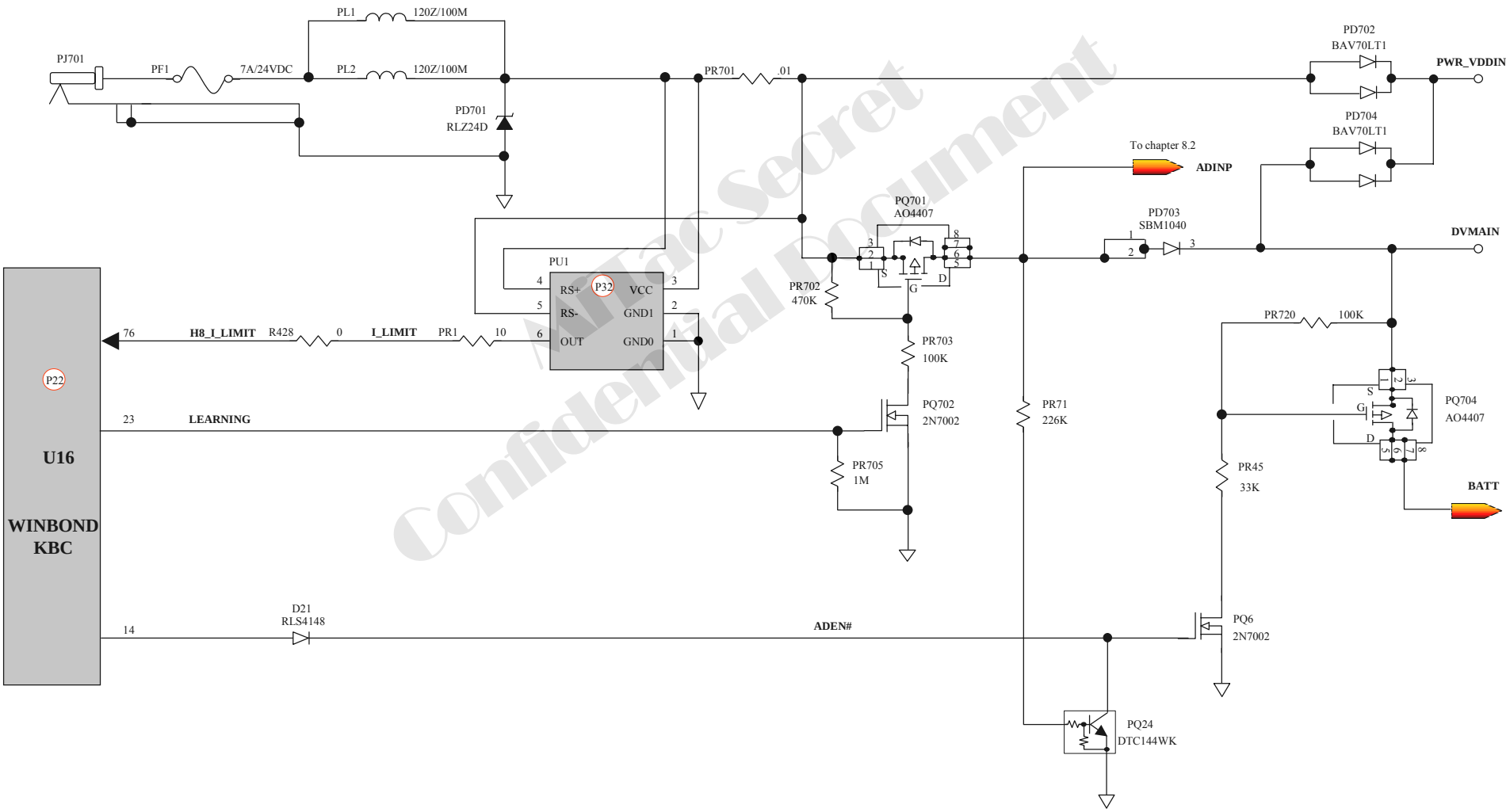
8.1 No Power

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



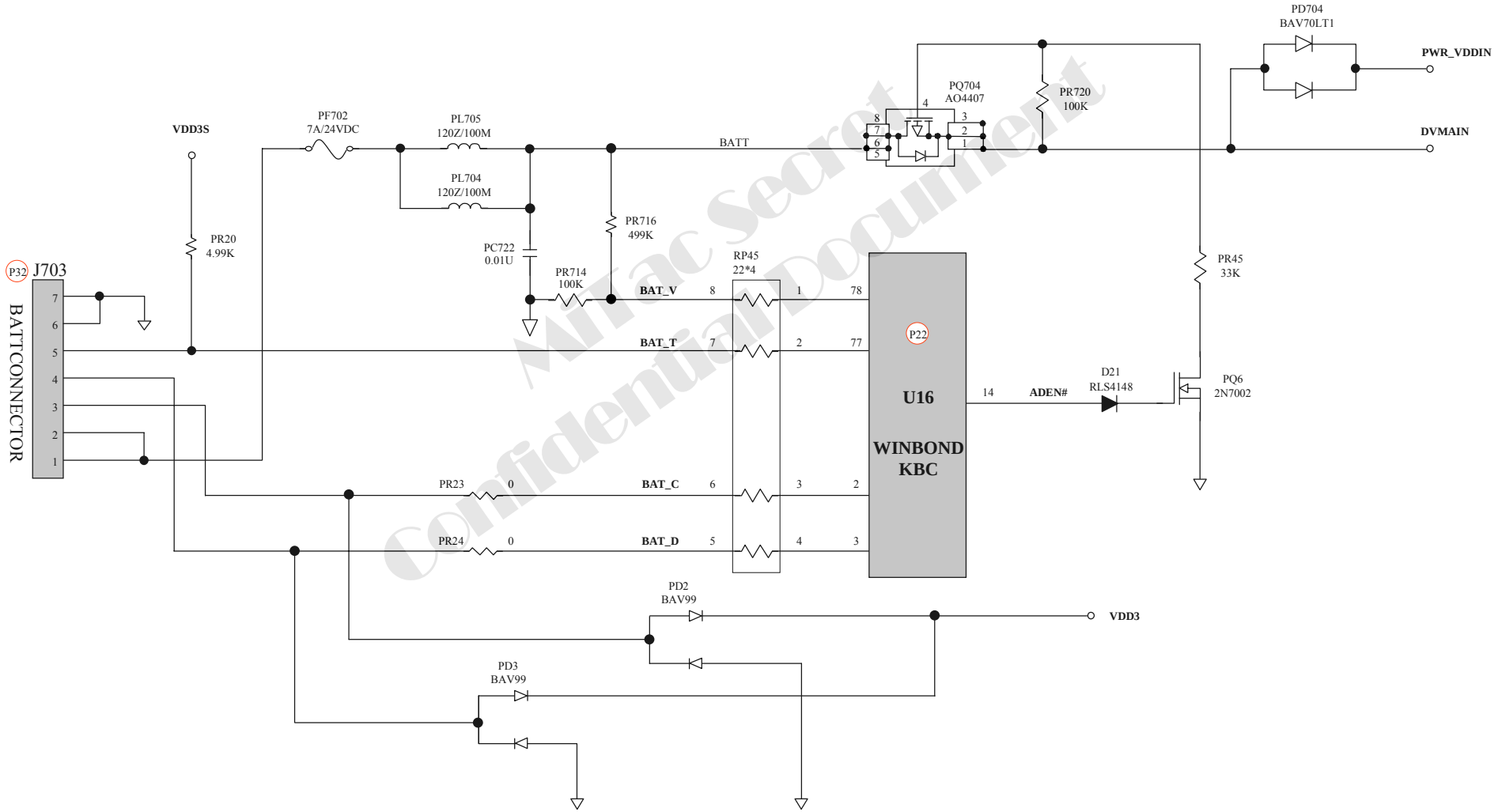
8.1 No Power(1)

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



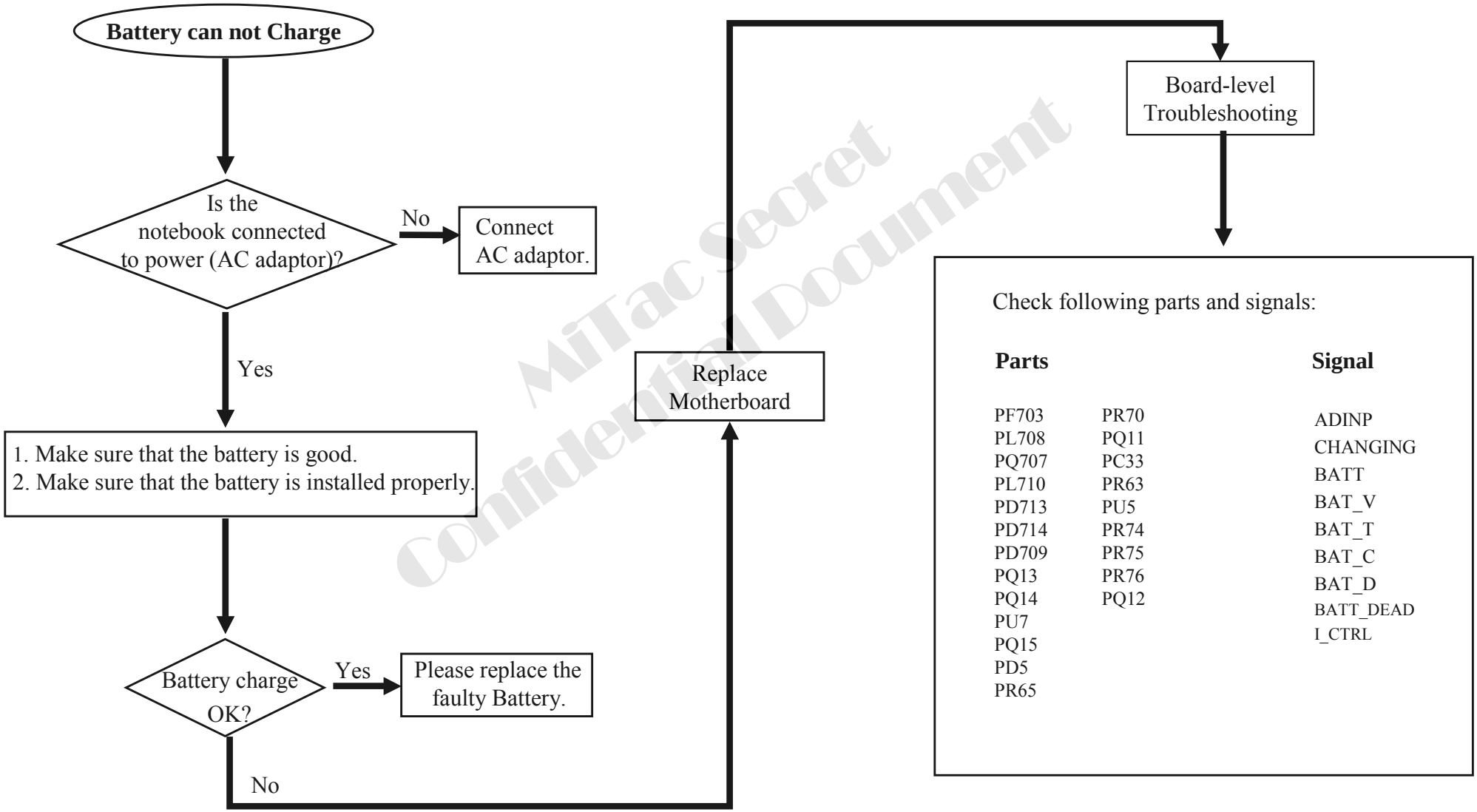
8.1 No Power(2)

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



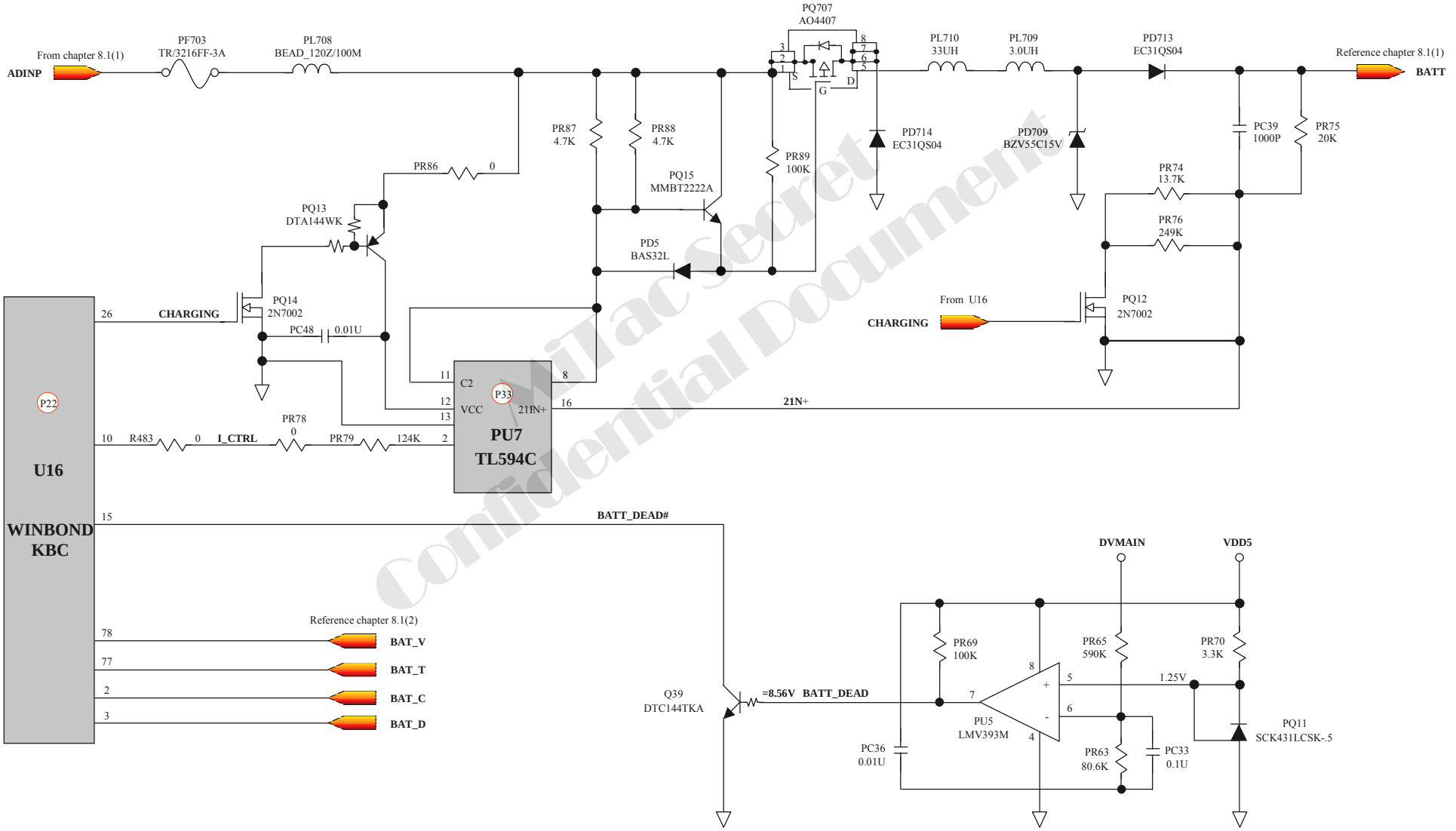
8.2 Battery Can not Be Charged

There are problems in charging the battery.



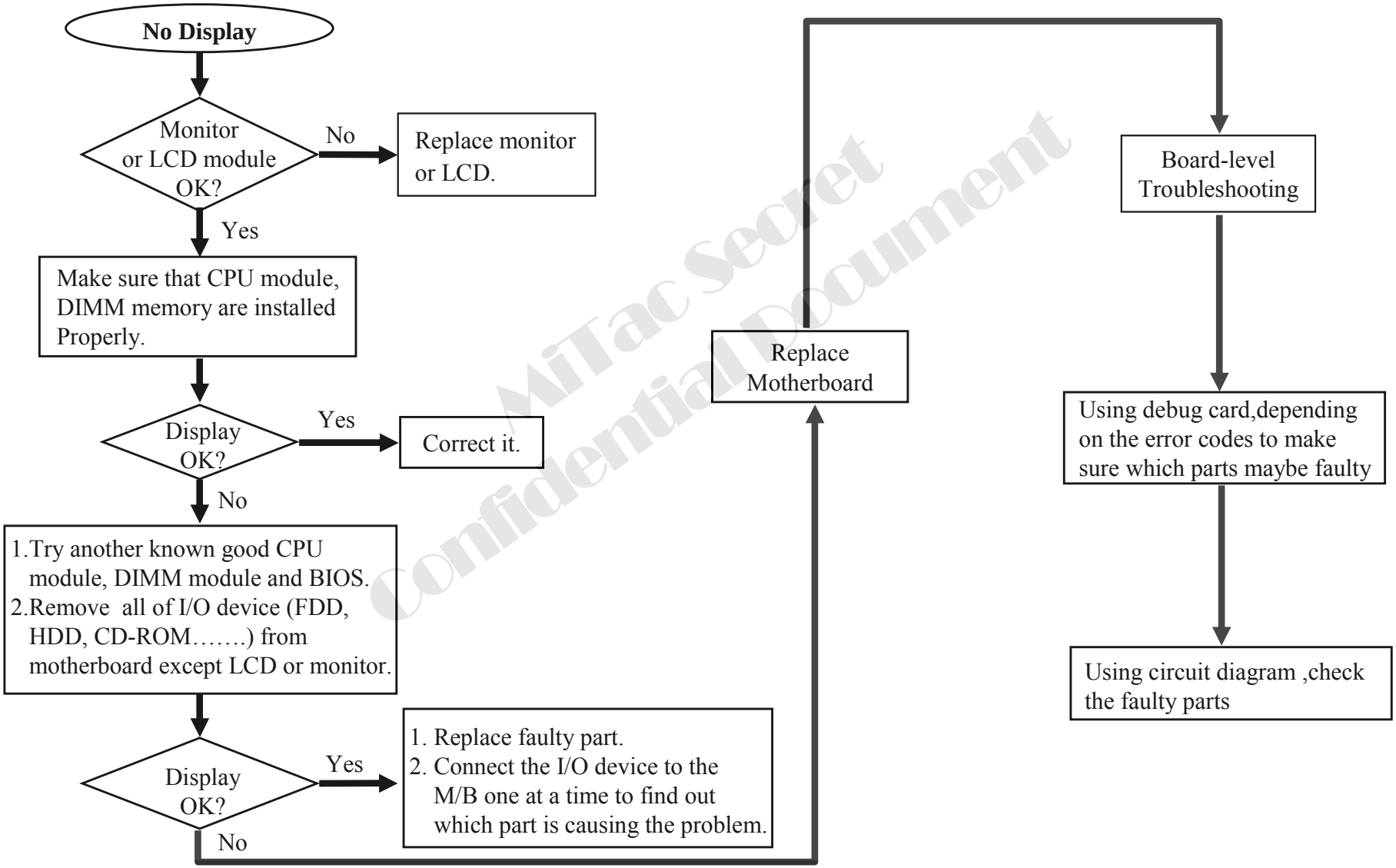
8.2 Battery Can not Be Charged

There are problems in charging the battery.



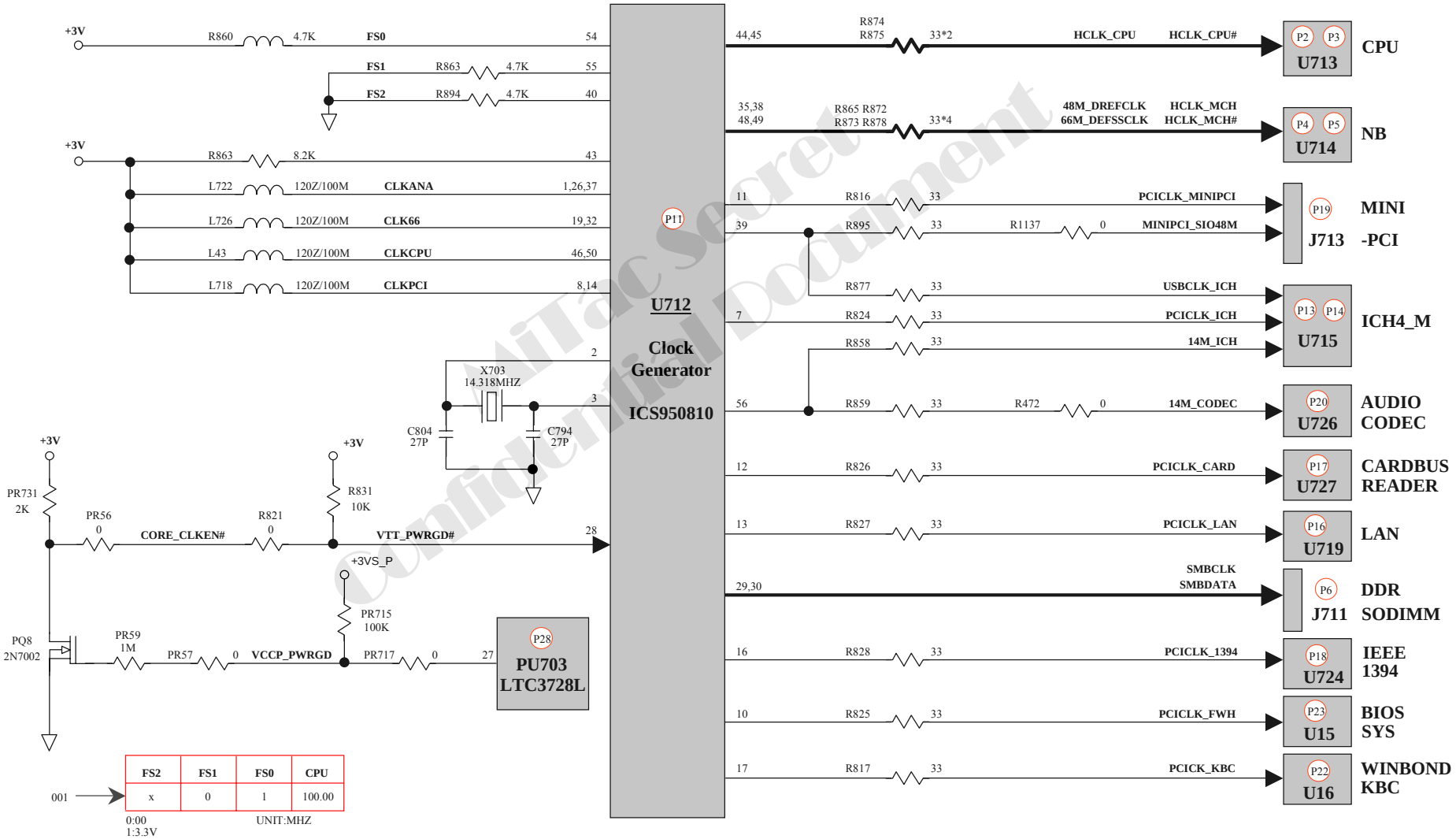
8.3 No Display

There is no display on both LCD and VGA monitor after power on although the LCD and monitor is known-good.



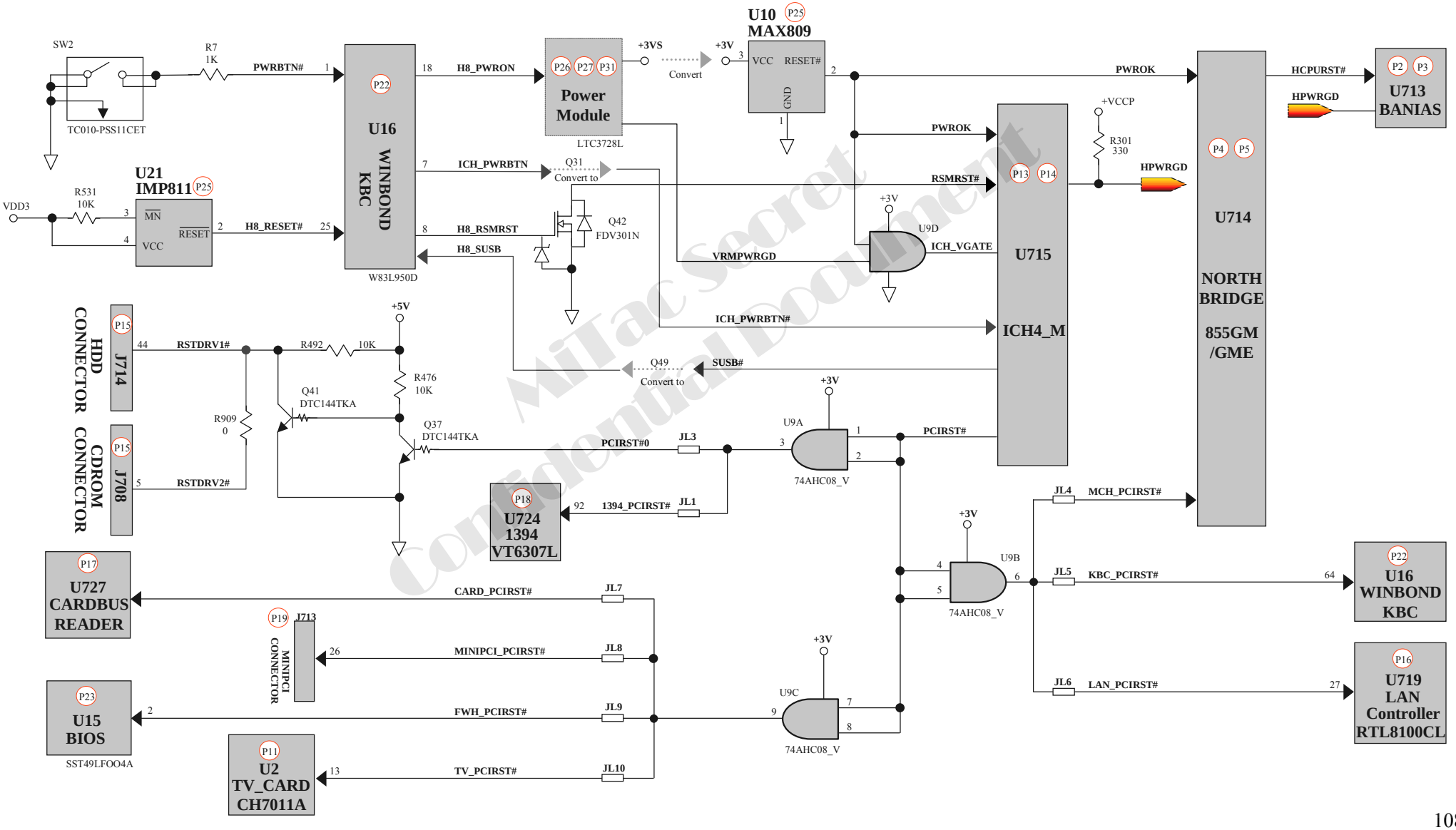
8.3 No Display(1)

****** System Clock Check ******



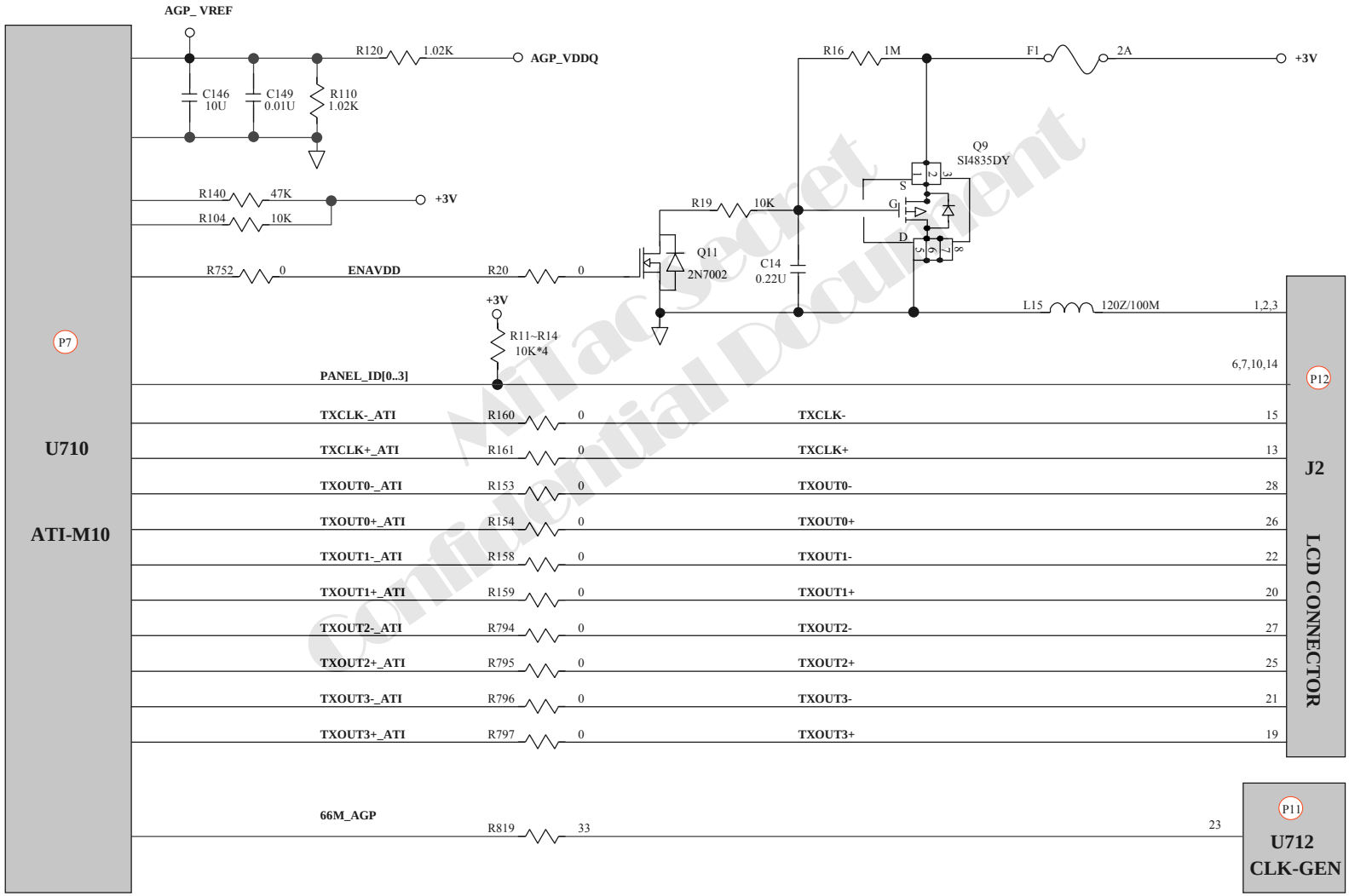
8.3 No Display(2)

****** System Reset Check ******



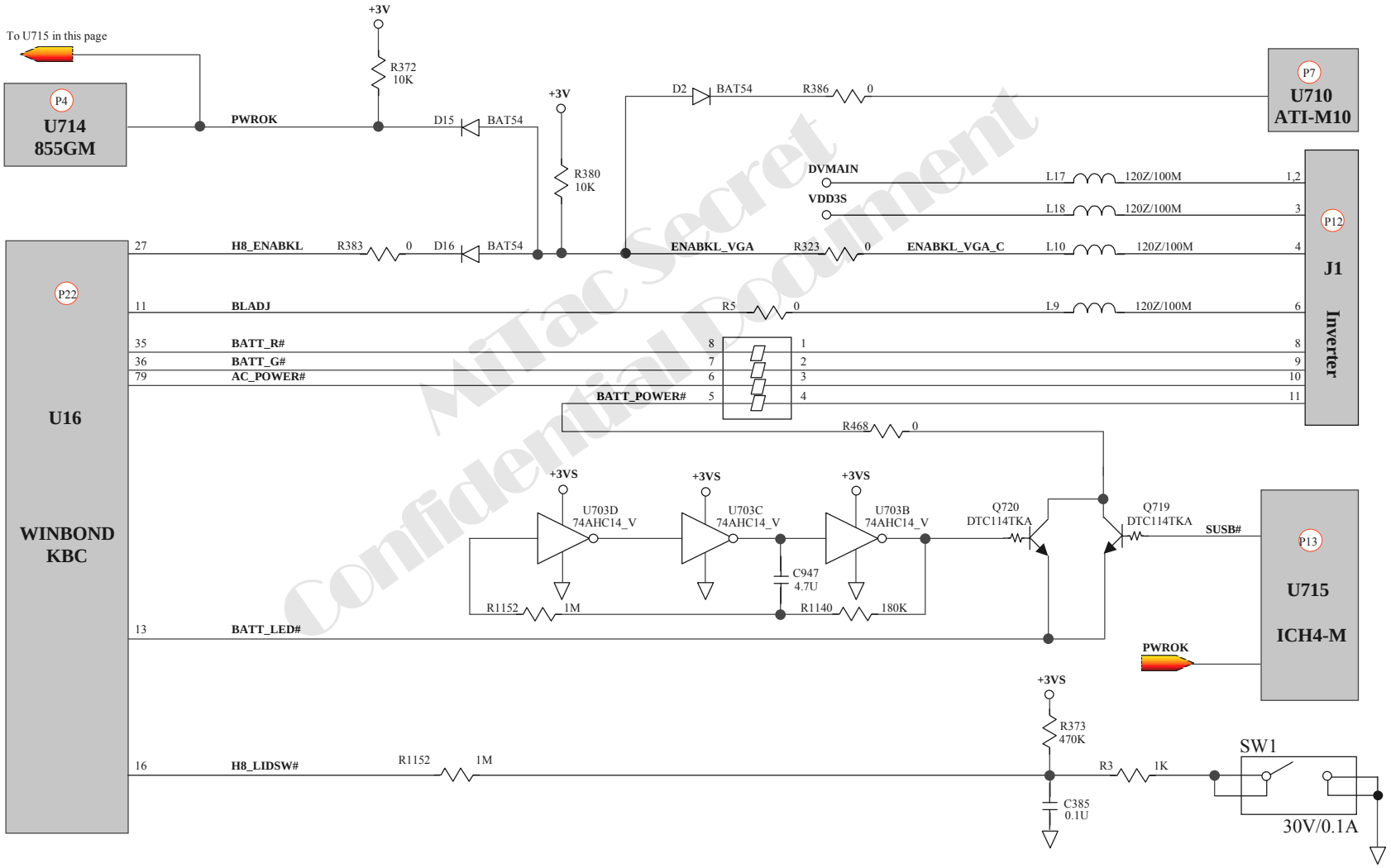
8.3 No Display(3)

****** VGA Controller Checking ******



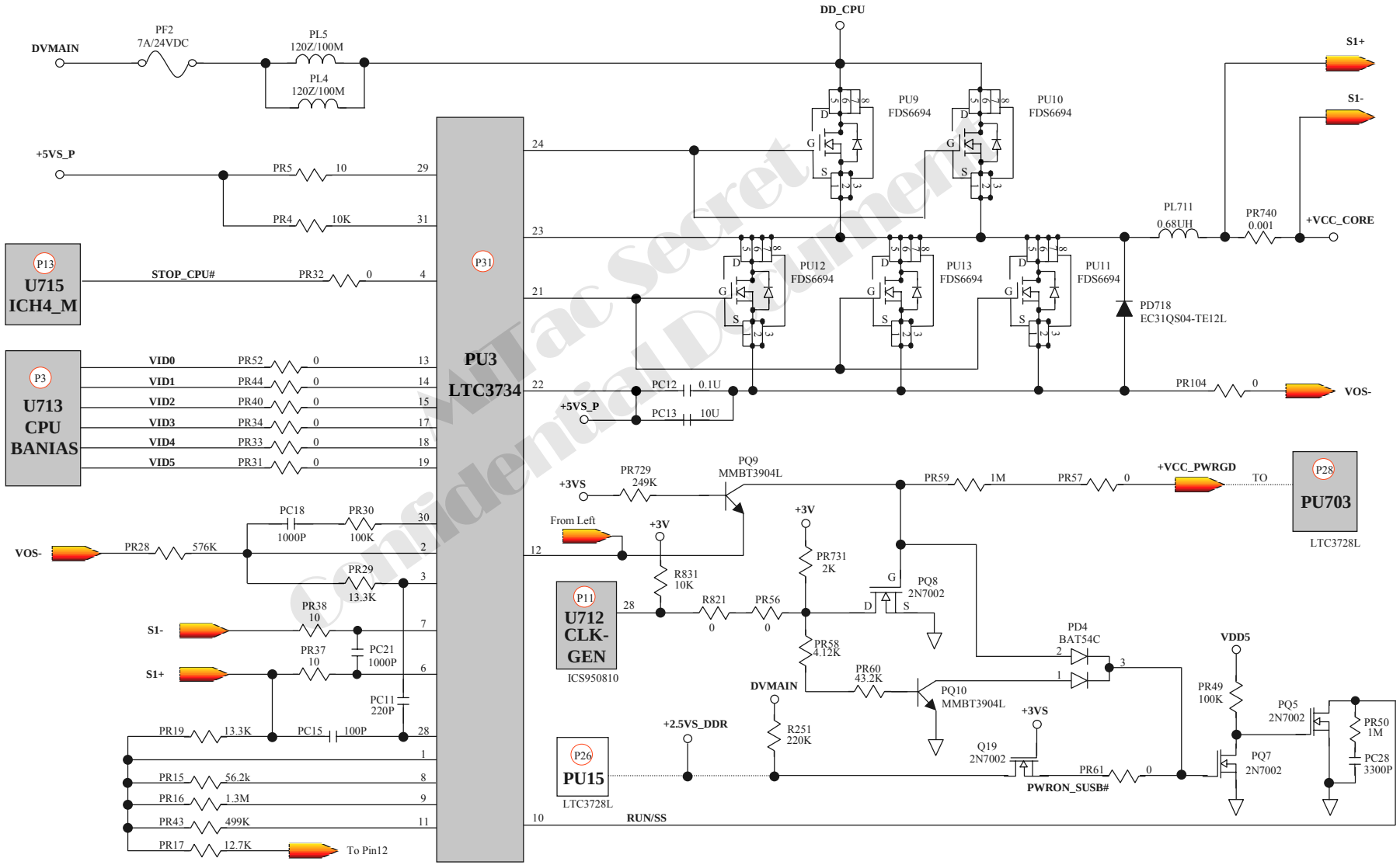
8.3 No Display(4)

****** Back Light & Cover Switch Checking ******



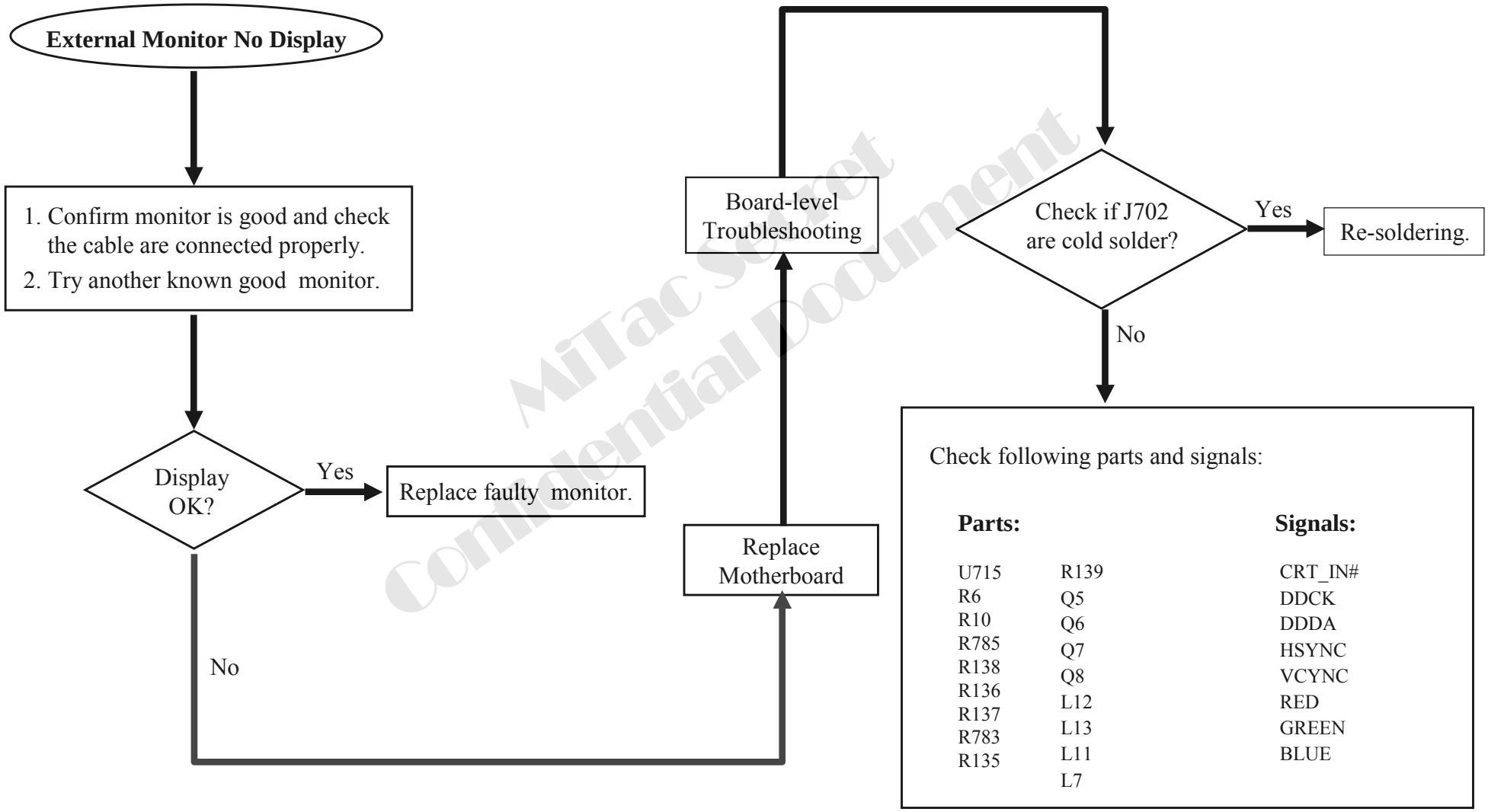
8.3 No Display(5)

CPU Core does not exist .



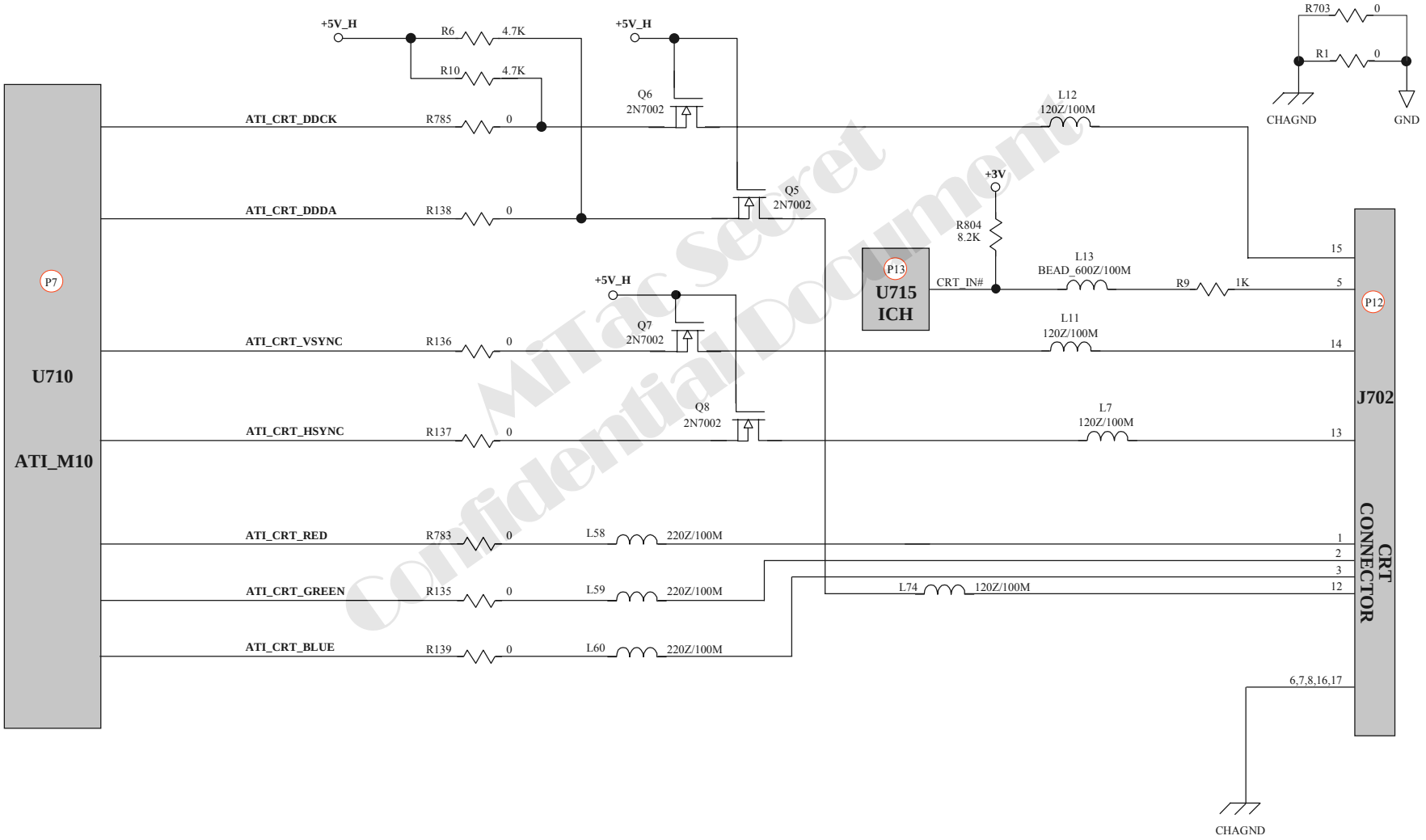
8.4 External Monitor No Display

There is no display or picture abnormal on CRT monitor, but LCD can normally display.



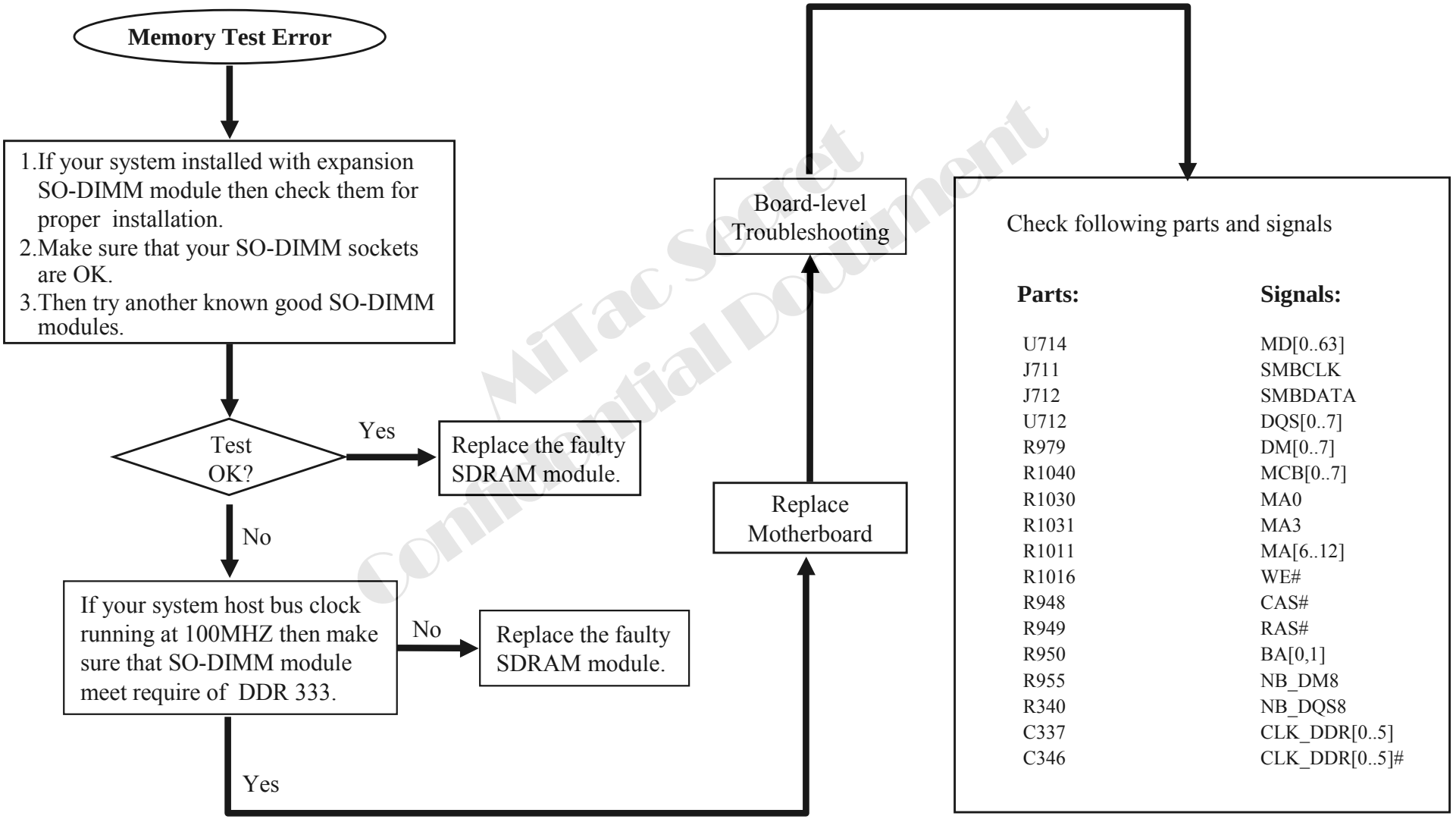
8.4 External Monitor No Display

There is no display or picture abnormal on CRT monitor, but LCD can normally display.



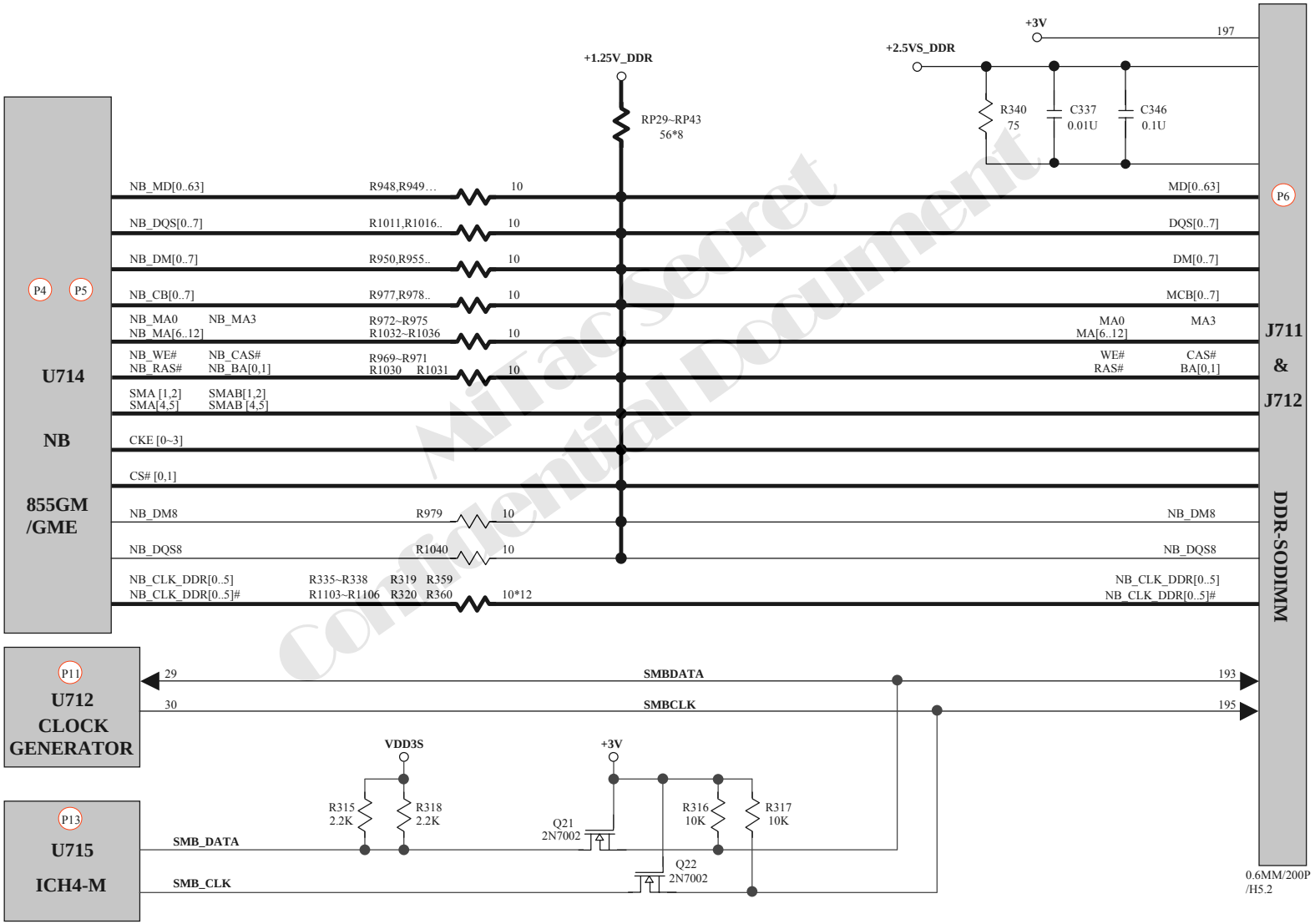
8.5 Memory Test Error

Either on board or extend SDRAM is failure or system hangs up.



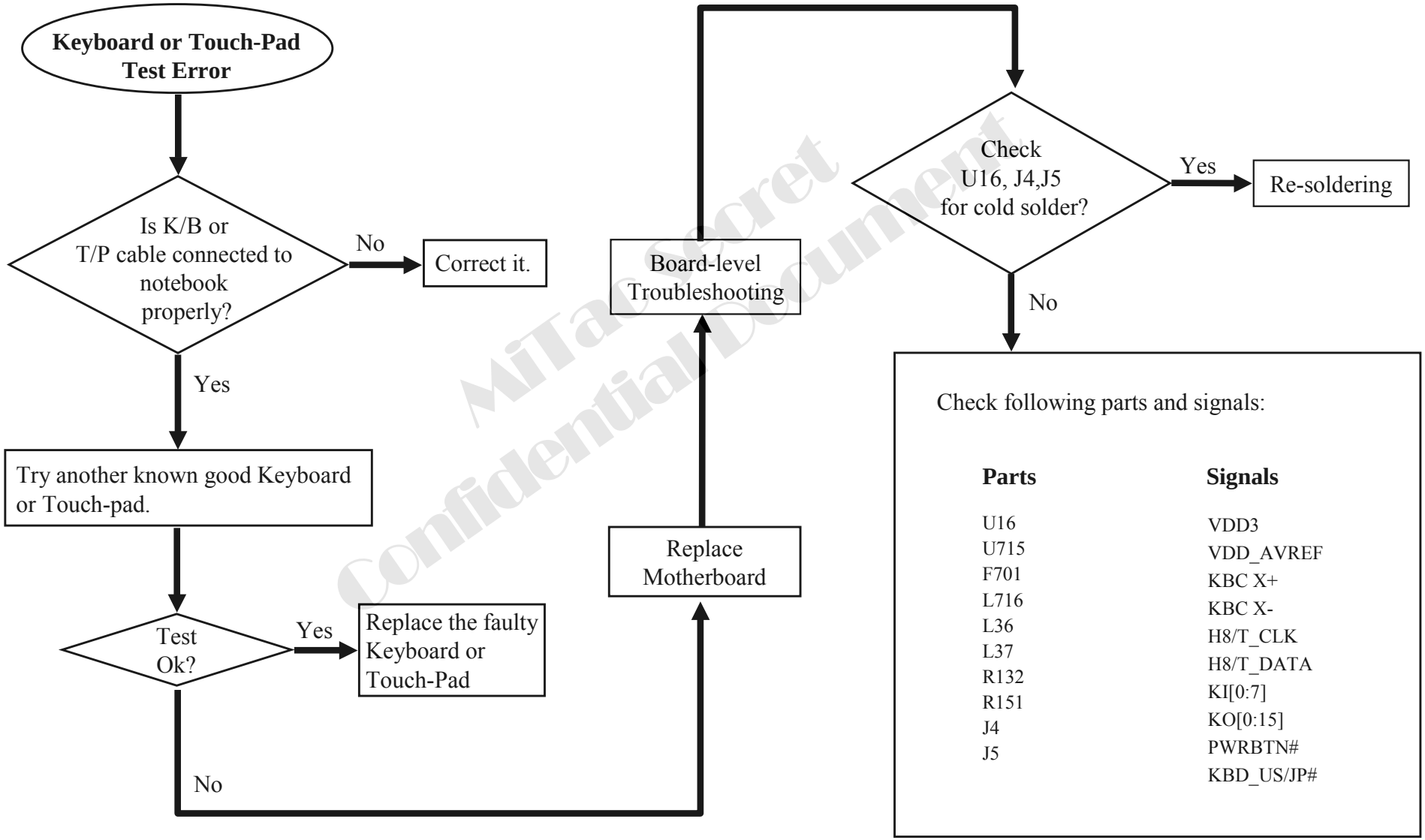
8.5 Memory Test Error

Either on board or extend SDRAM is failure or system hangs up.



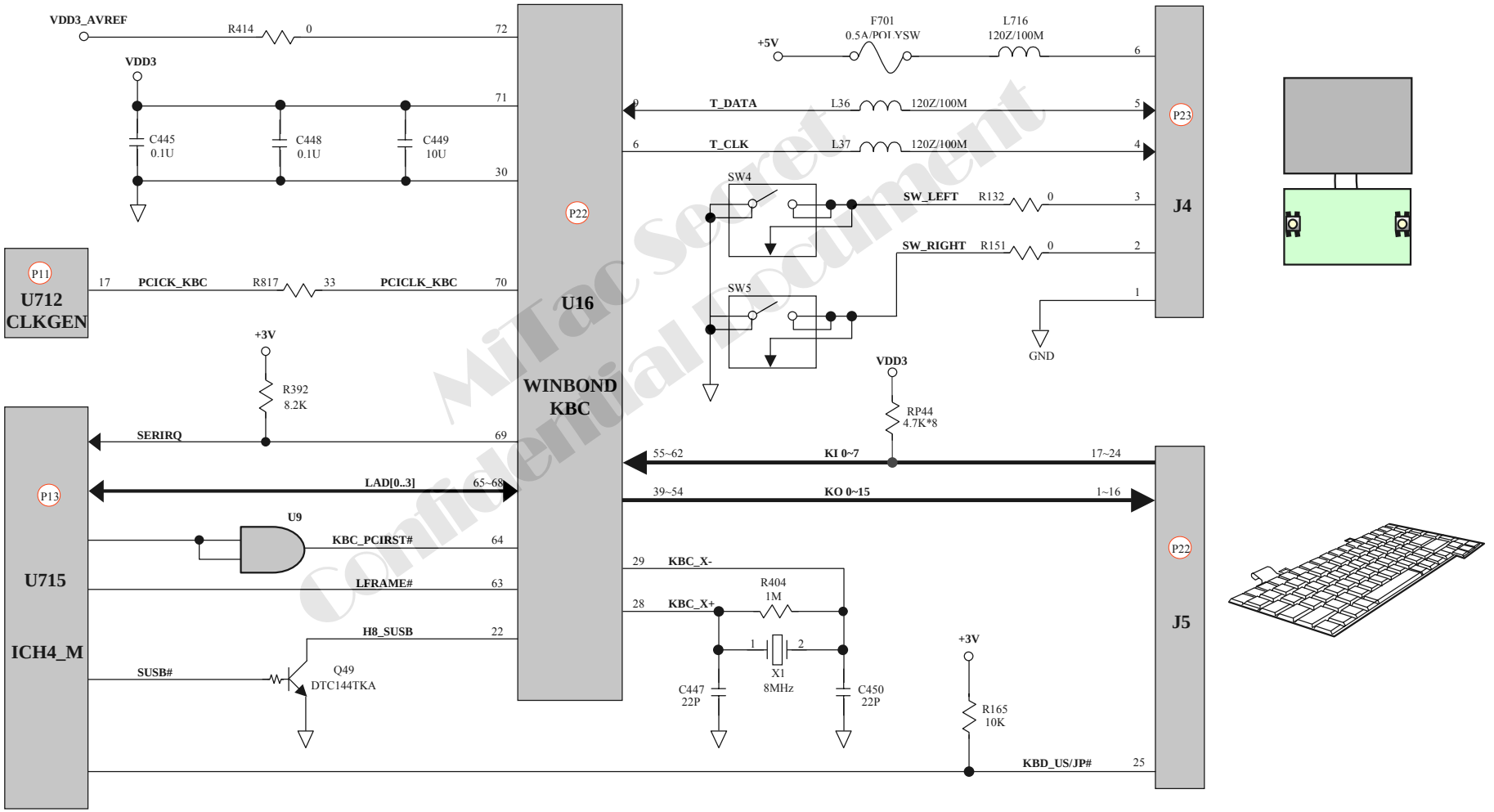
8.6 Keyboard (K/B) /Touch-Pad (T/P) Test Error

Error message of keyboard or touch-pad failure is shown or any key does not work.



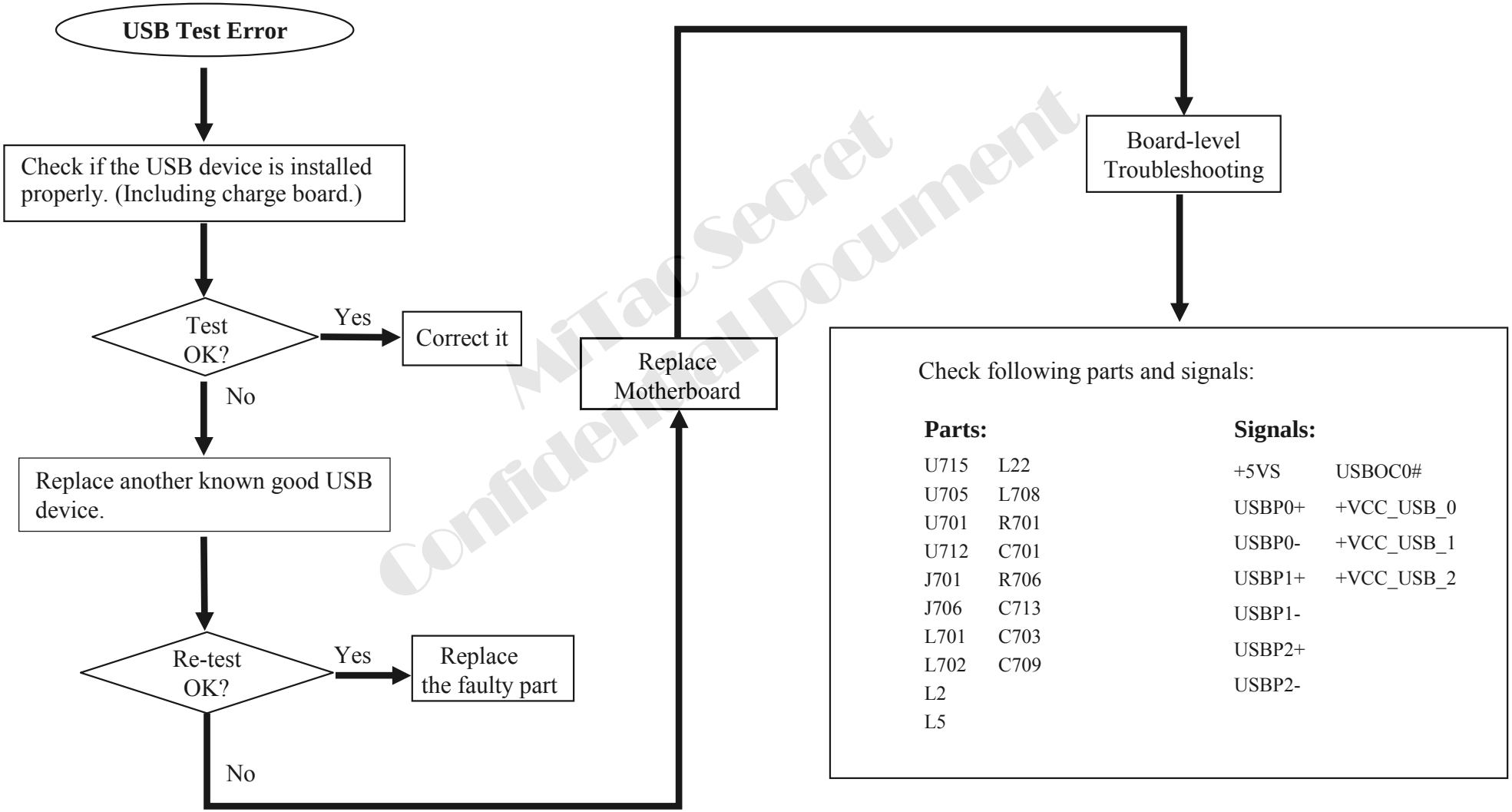
8.6 Keyboard (K/B) /Touch-Pad (T/P) Test Error

Error message of keyboard or touch-pad failure is shown or any key does not work.



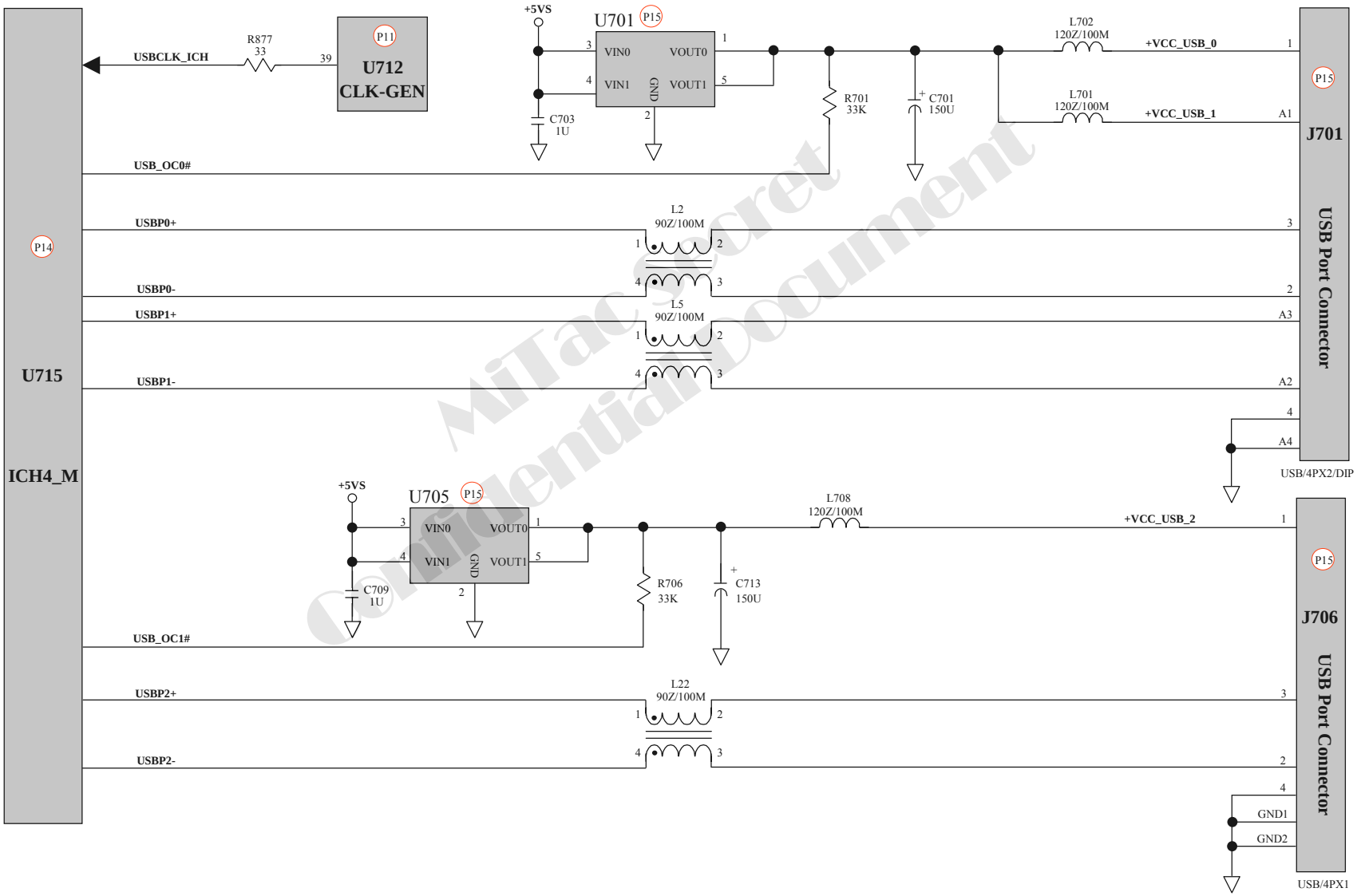
8.7 USB Port Test Error

An error occurs when a USB I/O device is installed.



8.7 USB Port Test Error

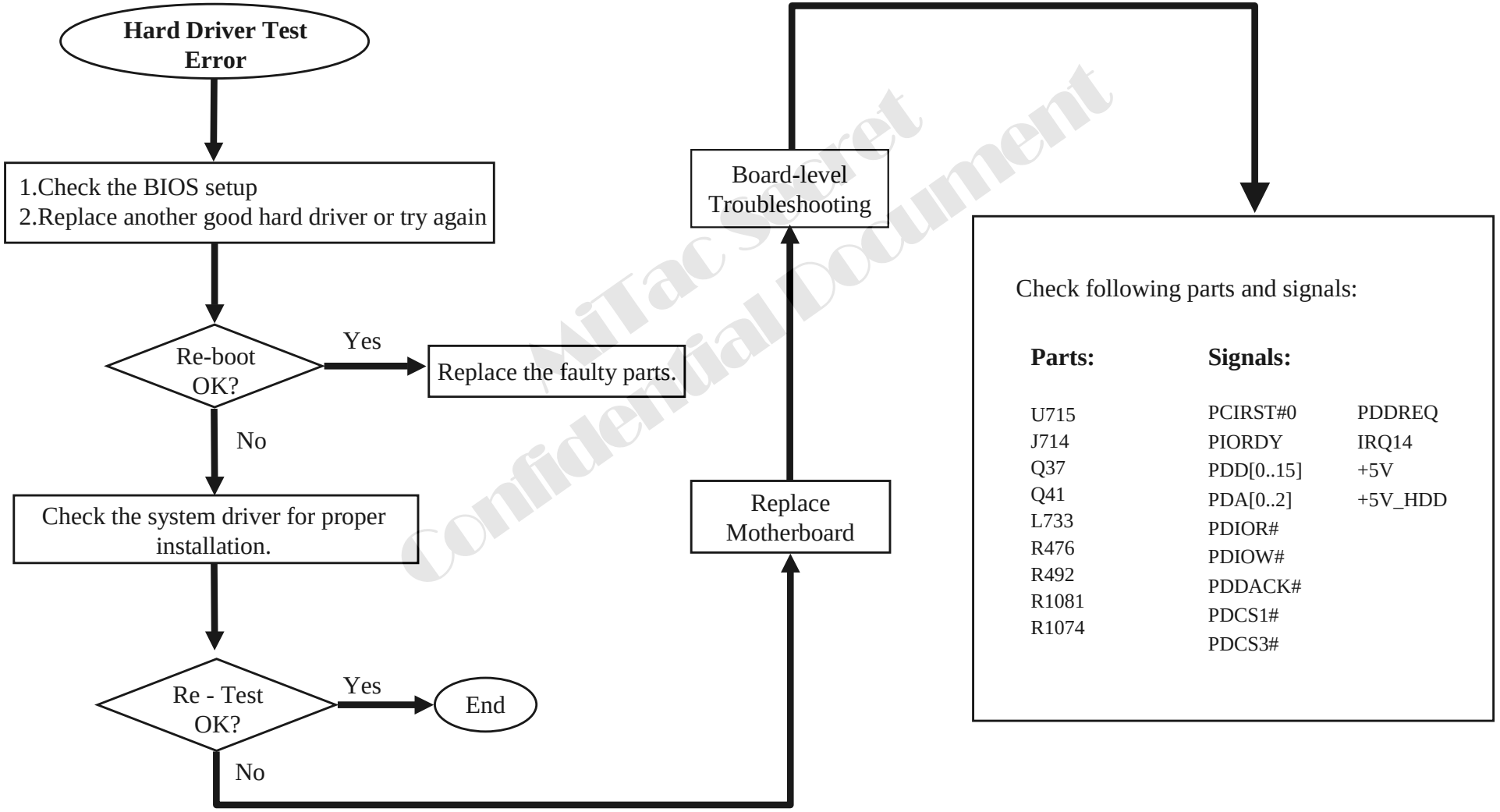
An error occurs when a USB I/O device is installed.



8050 N/B Maintenance

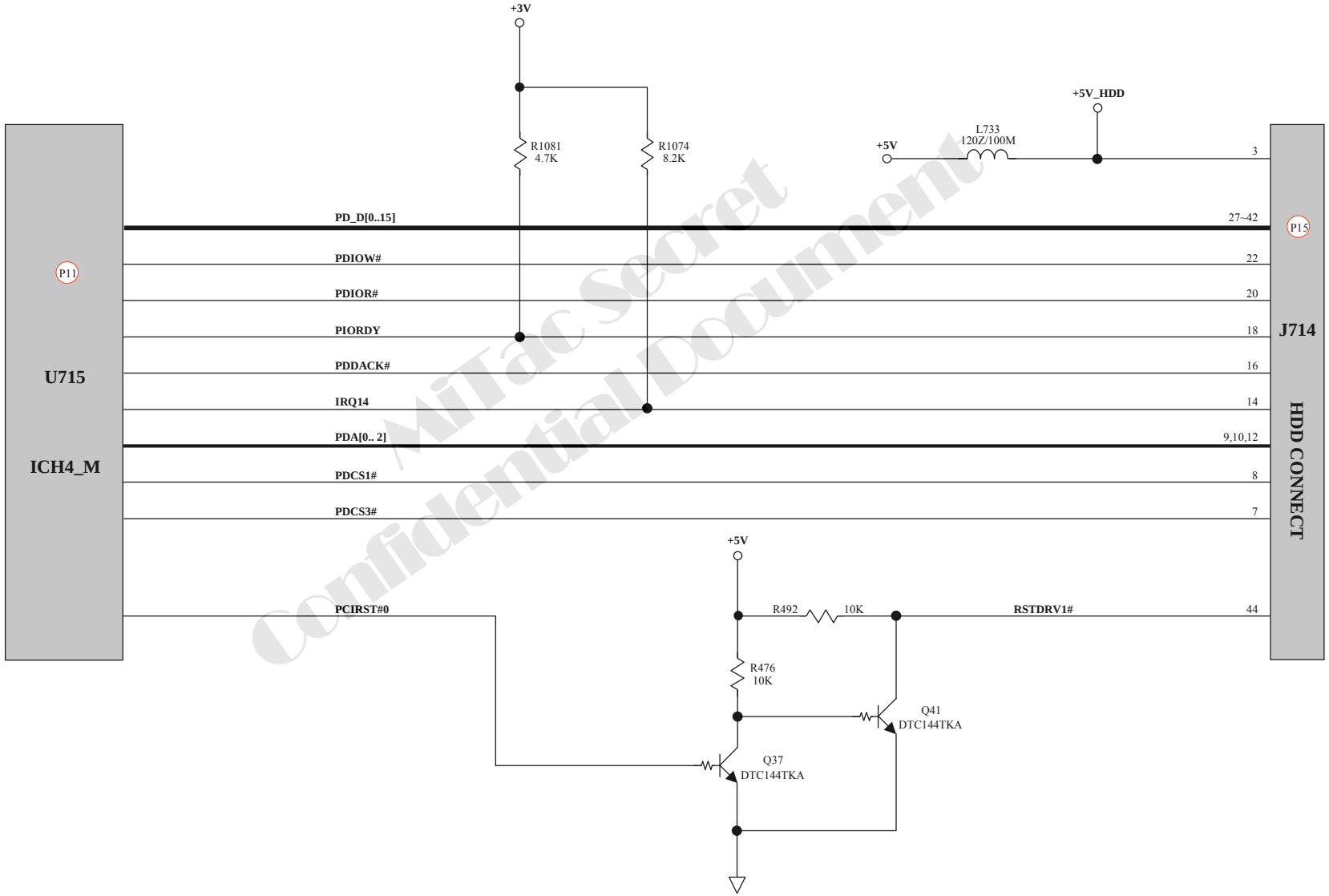
8.8 Hard Disk Drive Test Error

Either an error message is shown, or the drive motor spins non-stop, while reading data from or writing data to hard disk.



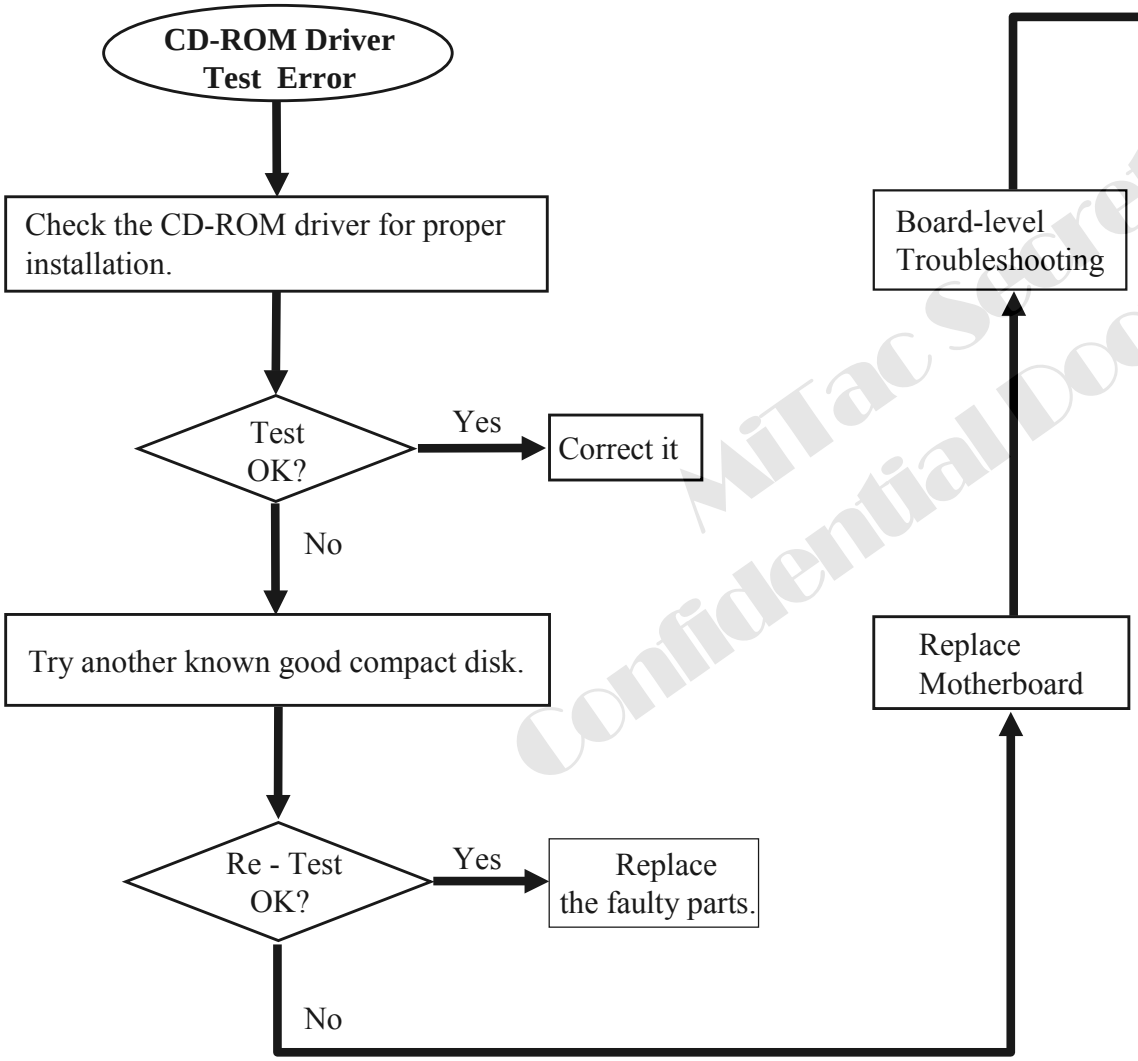
8.8 Hard Disk Drive Test Error

Either an error message is shown, or the drive motor spins non-stop, while reading data from or writing data to hard disk.



8.9 CD-ROM Test Error

CD-ROM driver can't run normally,maybe an error message is shown when reading data from CD-ROM.

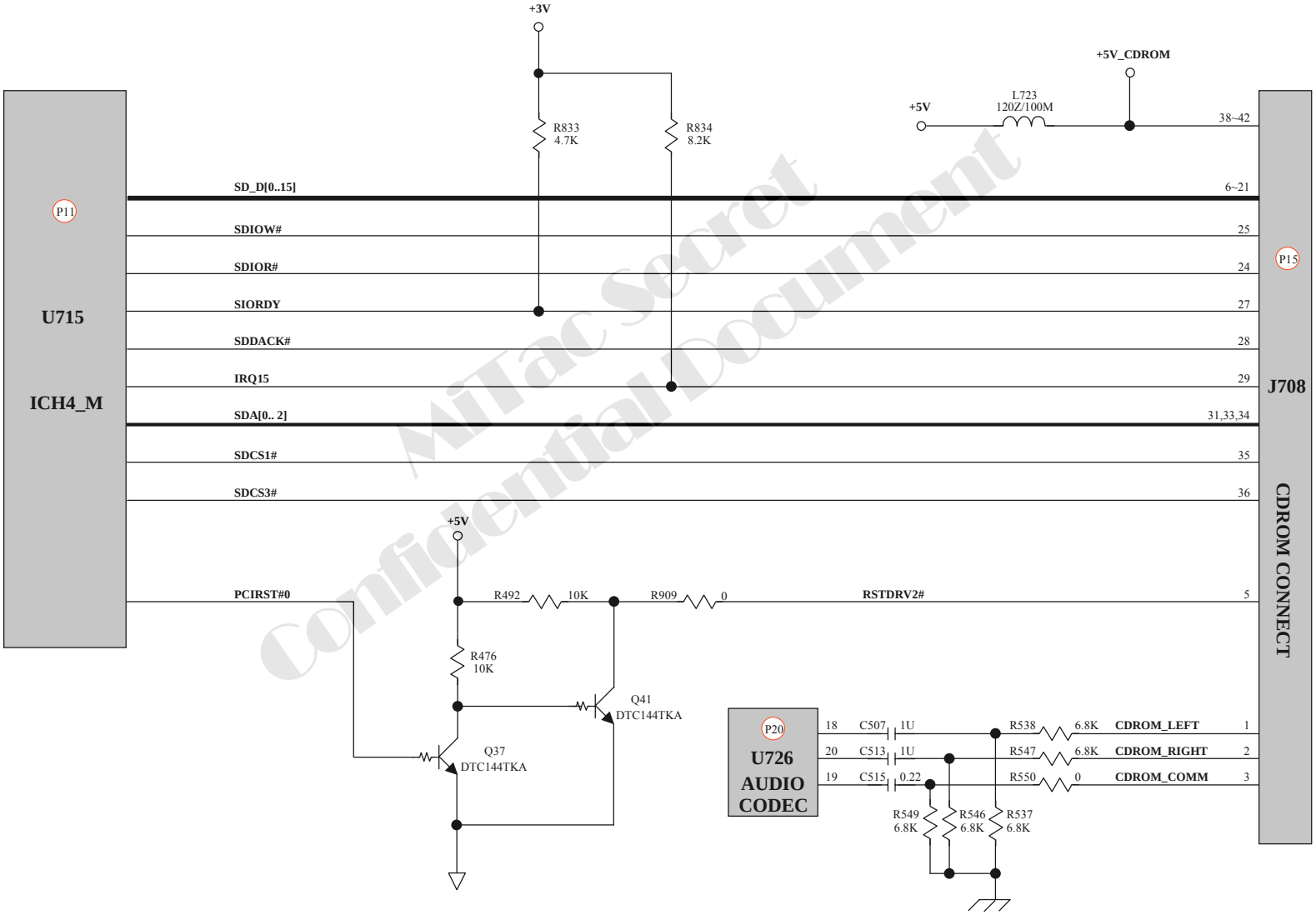


Check following parts and signals:

Parts:	Signals:	
U715	PCIRST#0	CDROM_COMM
J708	RSTDRV2#	
Q37	SIORDY	
Q41	SDD[0..15]	
R492	SDA[0..2]	
R476	SDIOR#	
R909	SDIOW#	
R833	SDDACK#	
R834	SDCS1#	
L723	SDCS3#	
	SDDREQ	
	IRQ15	
	+5V	
	+5V_CDROM	
	CDROM_LEFT	
	CDROM_RIGHT	

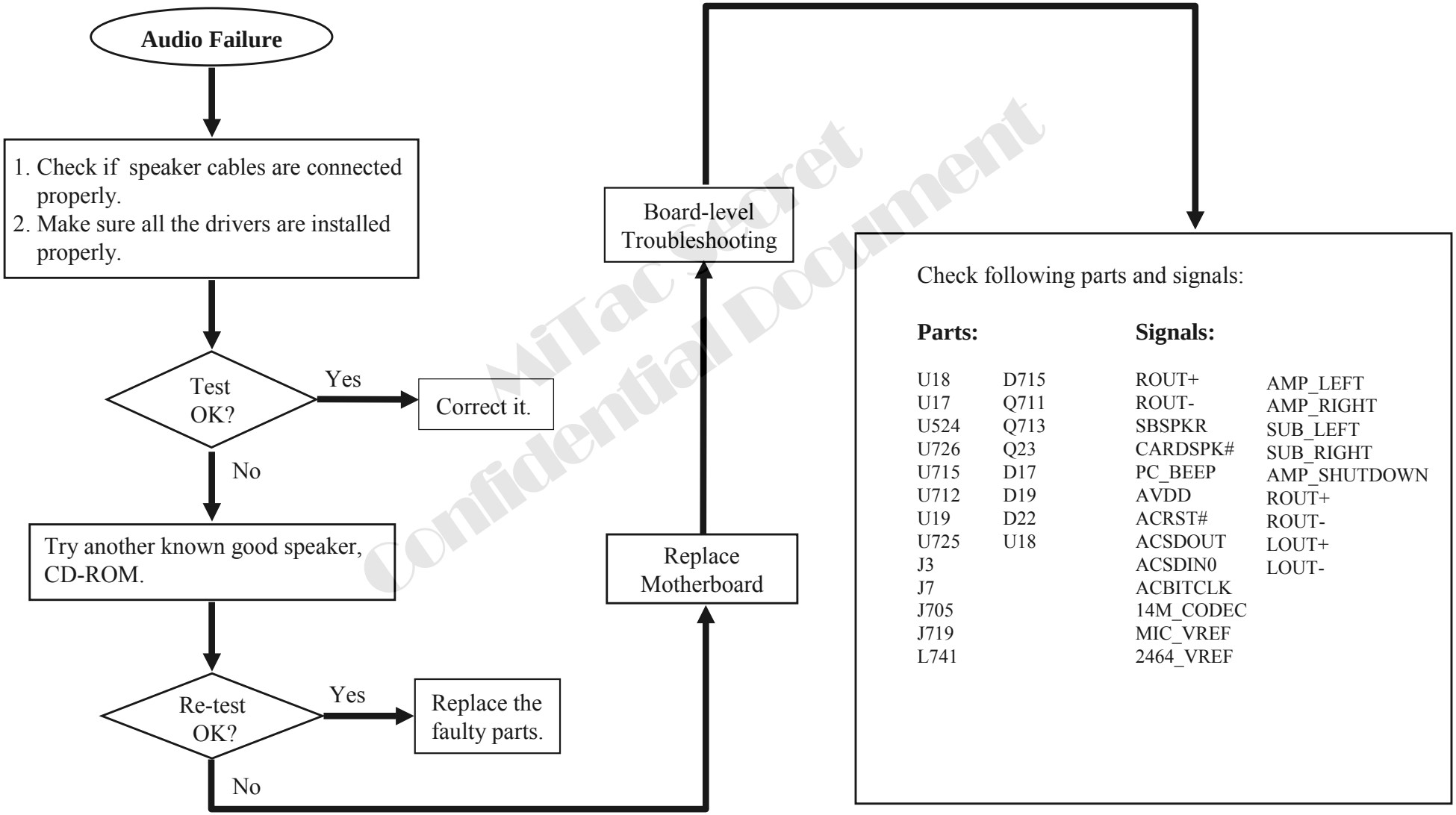
8.9 CD-ROM Test Error

CD-ROM driver can’t run normally,maybe an error message is shown when reading data from CD-ROM.



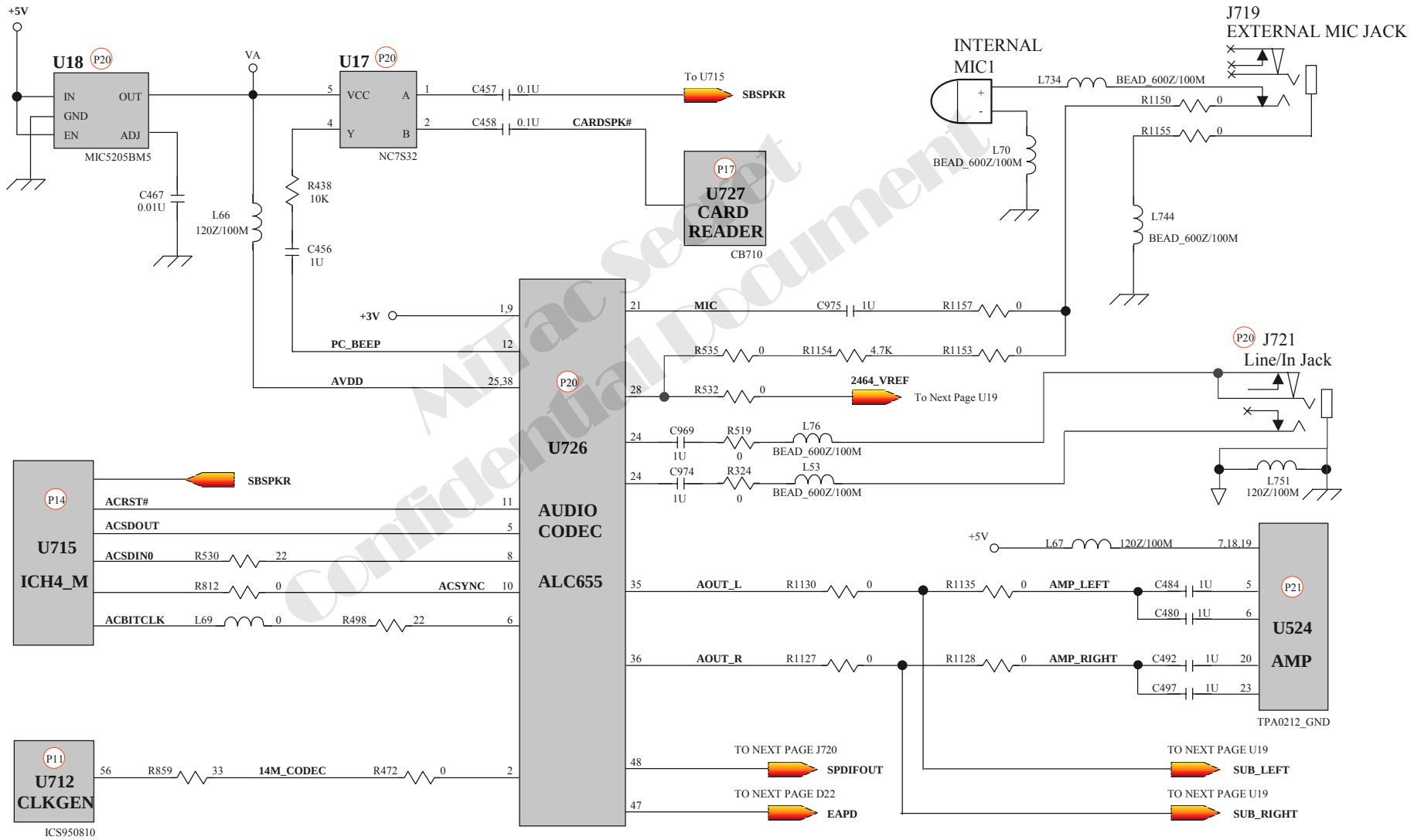
8.10 Audio Failure

There is trouble with the sound from speaker or completely no sound



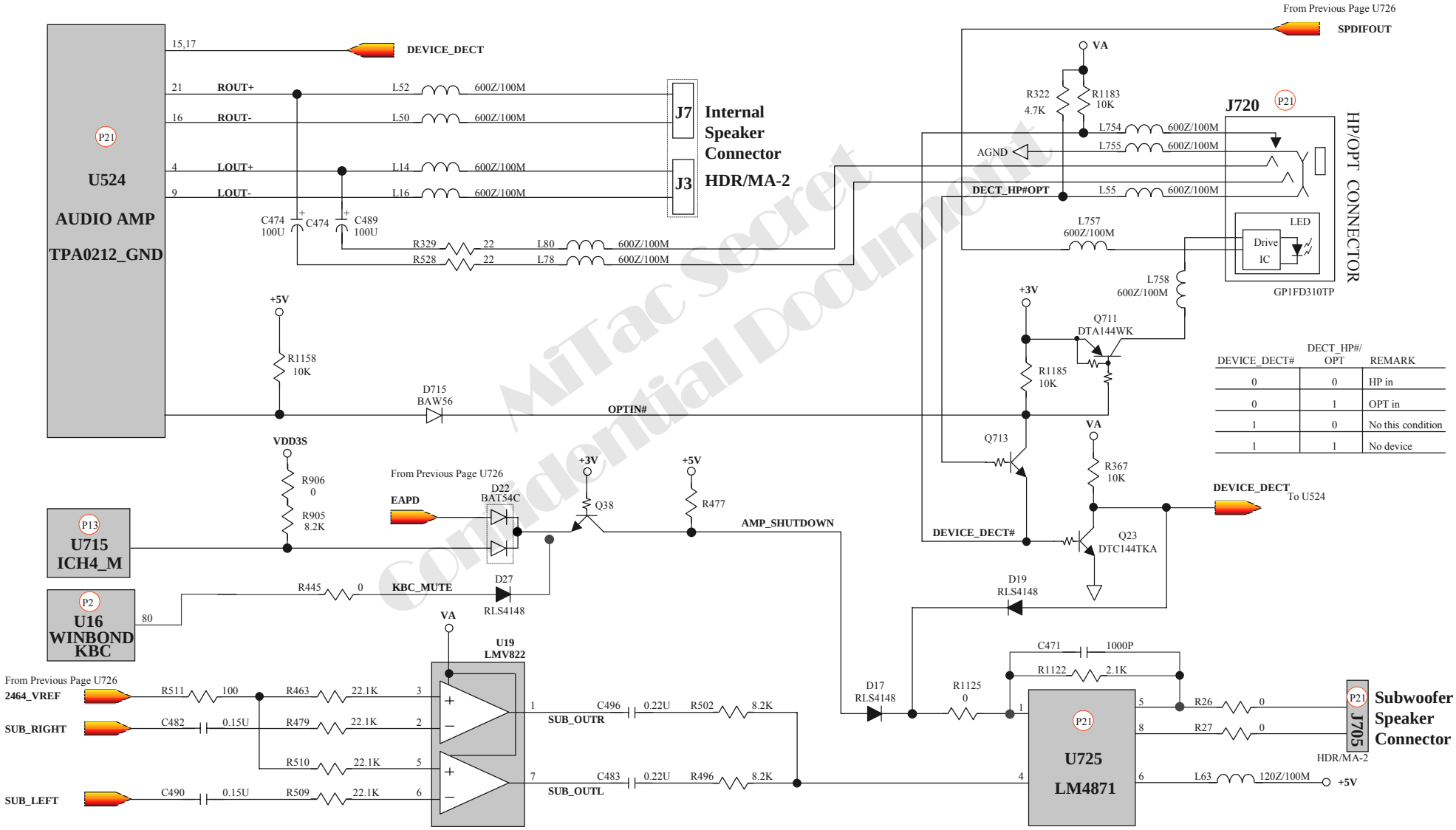
8.10 Audio Failure(Audio Codec)

There is trouble with the sound from speaker or completely no sound



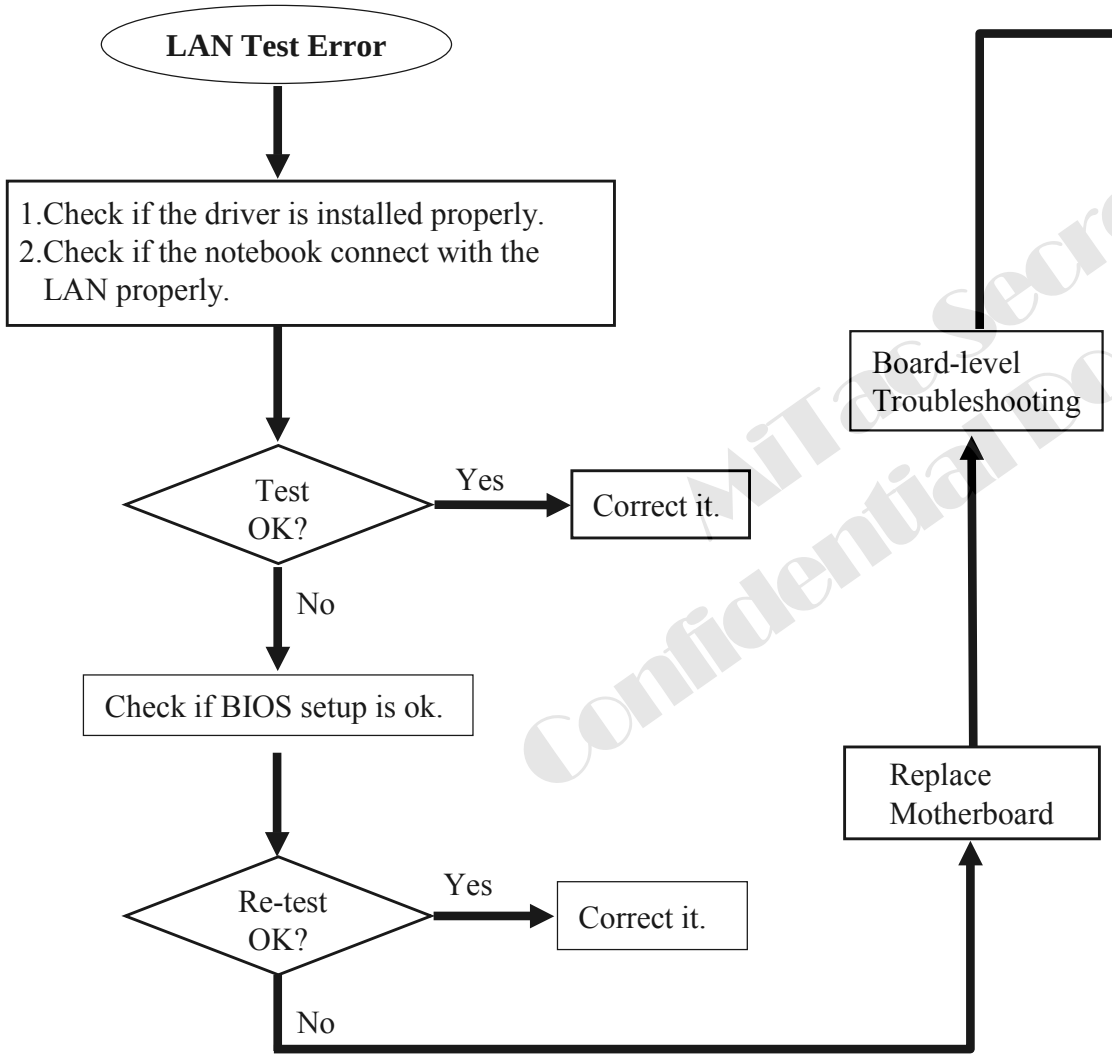
8.10 Audio Failure(Audio Amplifier & Subwoofer)

There is trouble with the sound from speaker or completely no sound



8.11 LAN Test Error

An error occurs when a LAN device is installed.

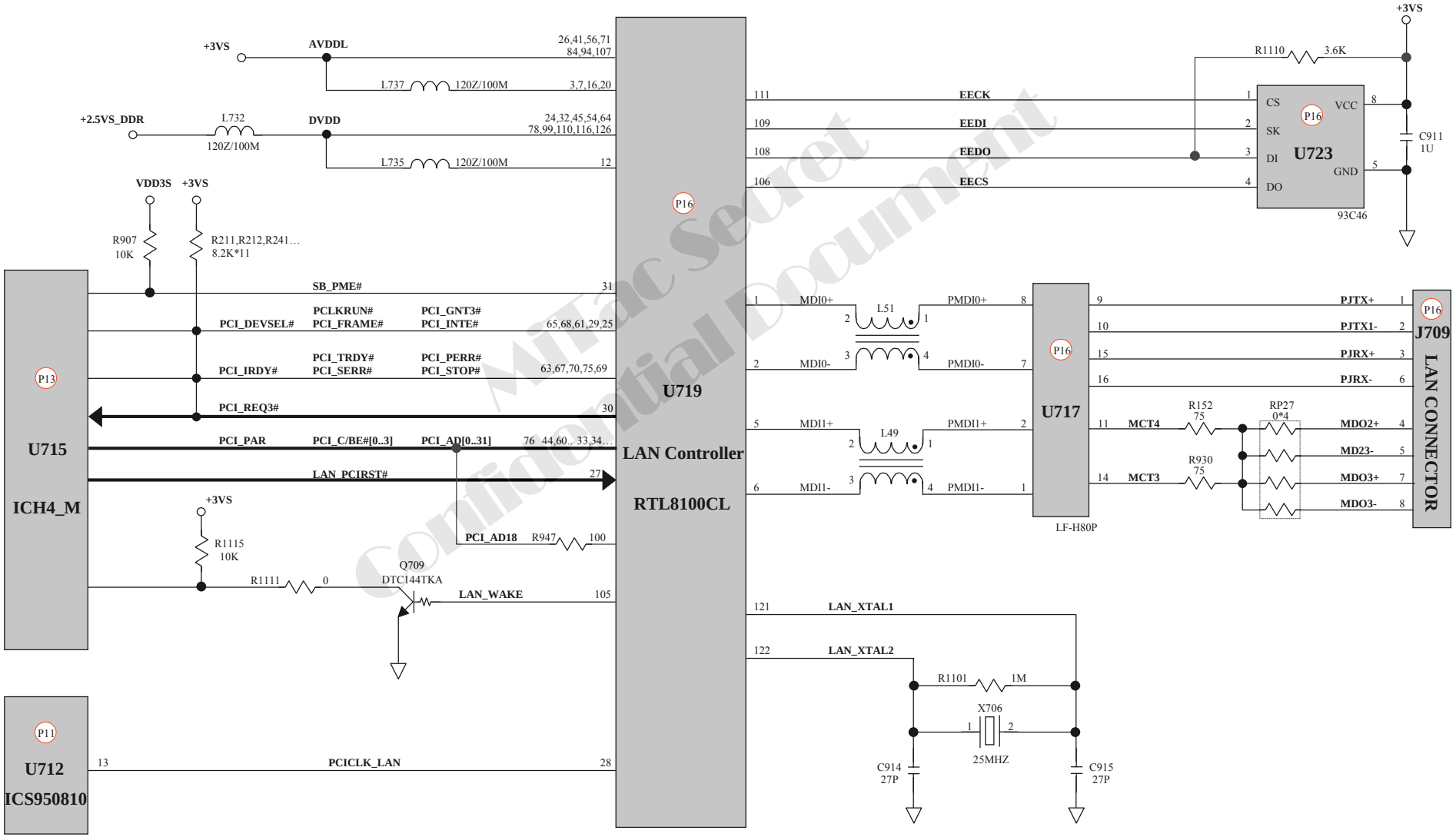


Check following parts and signals:

Parts:	Signals:	
U719	EECK	AVDDL
U717	EEDI	DVDD
U723	EEDO	SB_PME#
J709	EECS	PCLKRUN#
L732	PJRX+	PCI_DEVSEL#
L735	PJRX-	PCI_FRAME#
L737	PJTX1-	PCI_INTE#
L51	PJTX+	PCI_REQ3
L49	LAN_XTANL1	PCI_IRDY#
Q709	LAN_XTANL2	PCI_SERR
X706	PCICLK_LAN	
R1101	LAN_WAKE	
R1111	PCI_AD[0..31]	
R1115	PCI_C/BR#[0..3]	
R907	PCI_PAR	
R211	LAN_PCIRST#	
R212	PCI_STOP#	

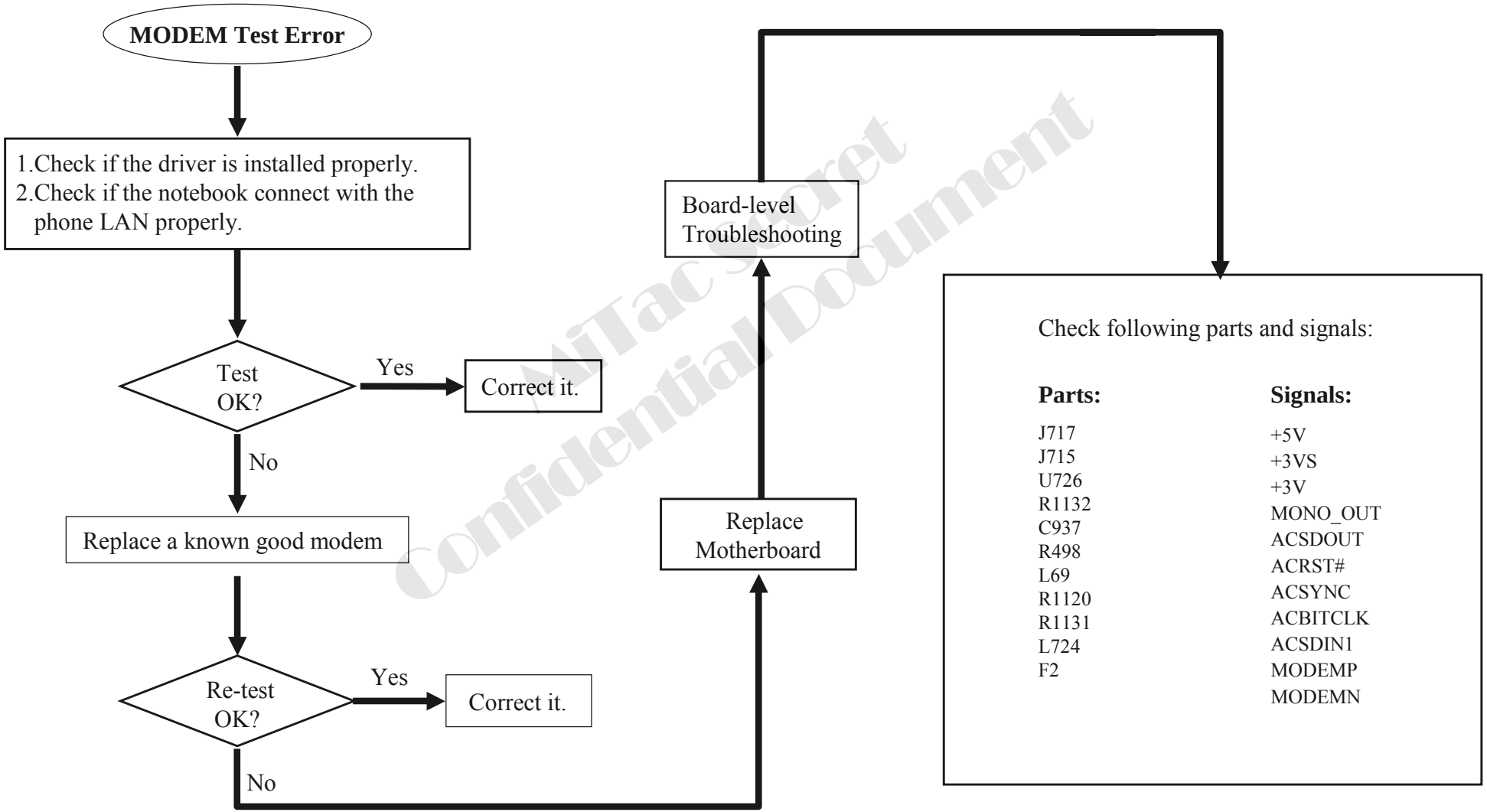
8.11 LAN Test Error

An error occurs when a LAN device is installed.



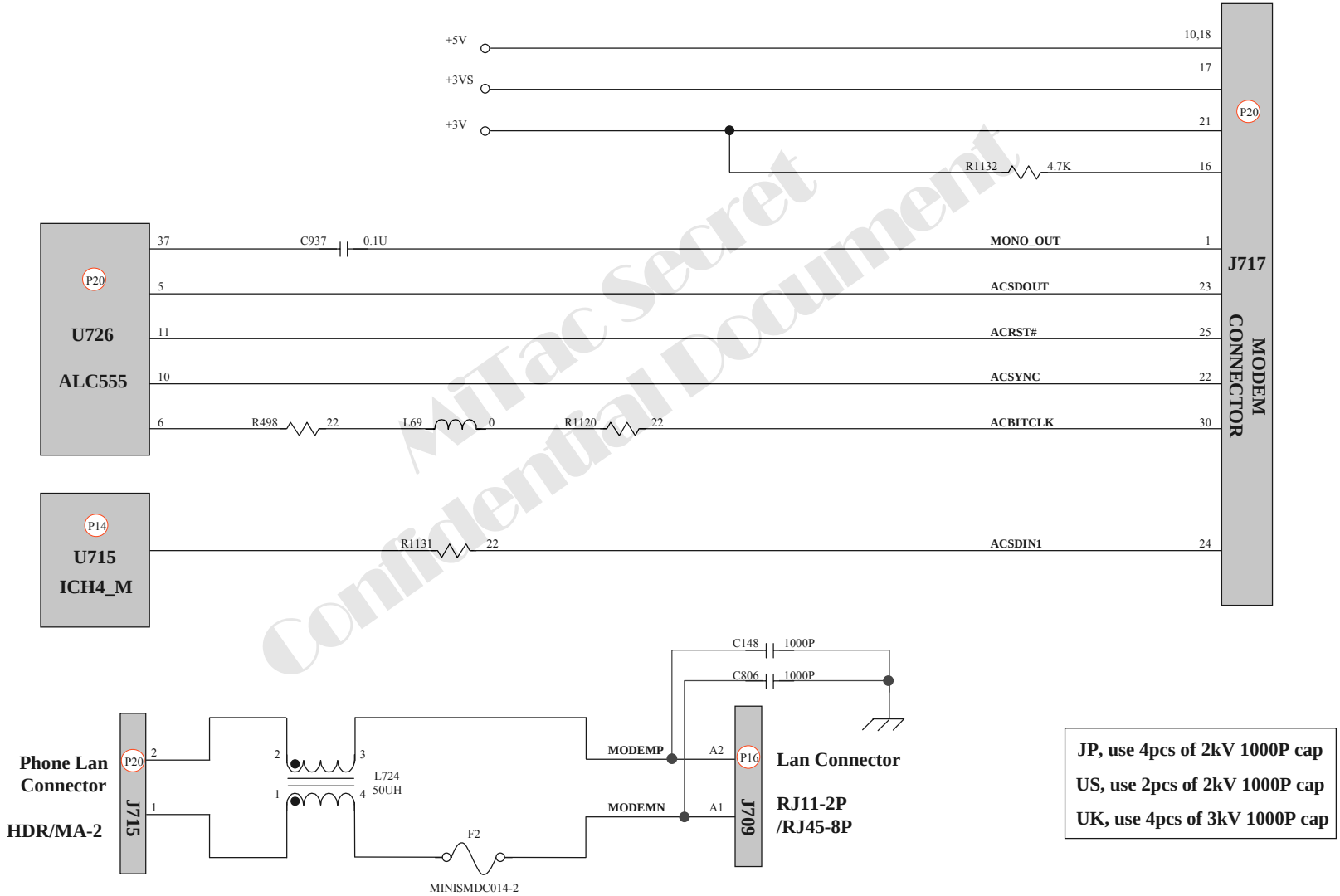
8.12 Modem Test Error

An error occurs when run the modem



8.12 Modem Test Error

An error occurs when run the modem



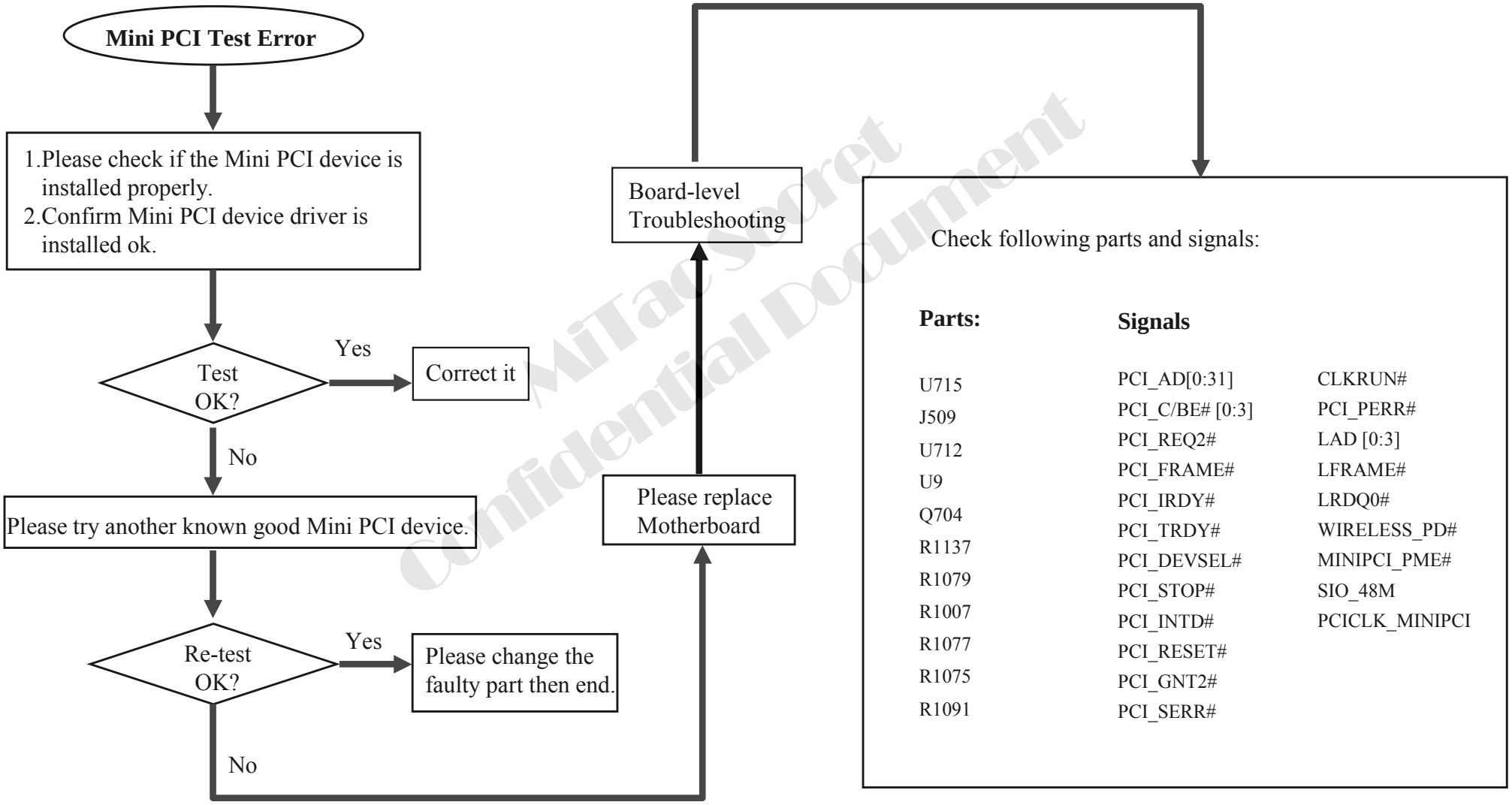
JP, use 4pcs of 2kV 1000P cap

US, use 2pcs of 2kV 1000P cap

UK, use 4pcs of 3kV 1000P cap

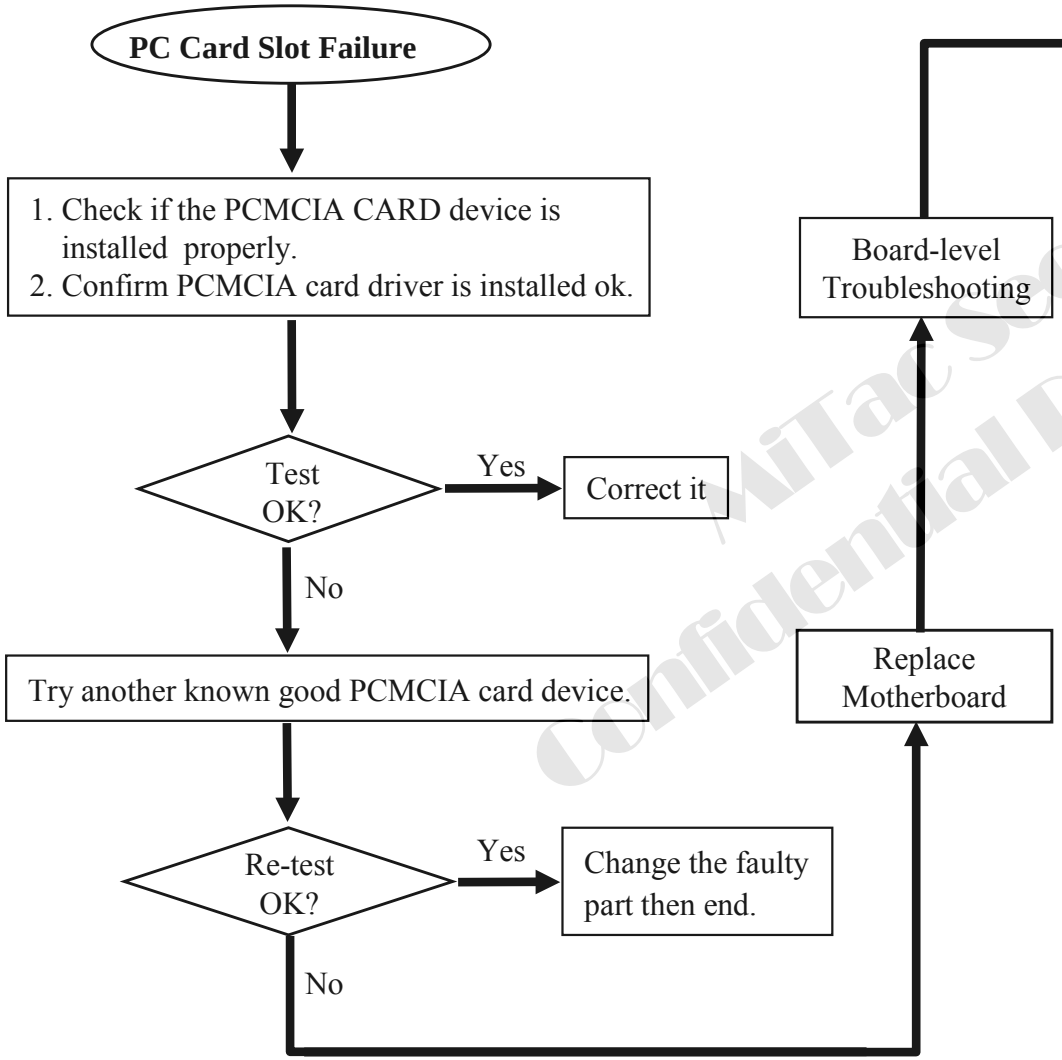
8.13 Mini PCI Test Error

An error message is shown after Mini PCI device is installed or the Mini PCI device does't work.



8.14 CardBus & Reader Test Error

An error occurs when a PC card device is installed.

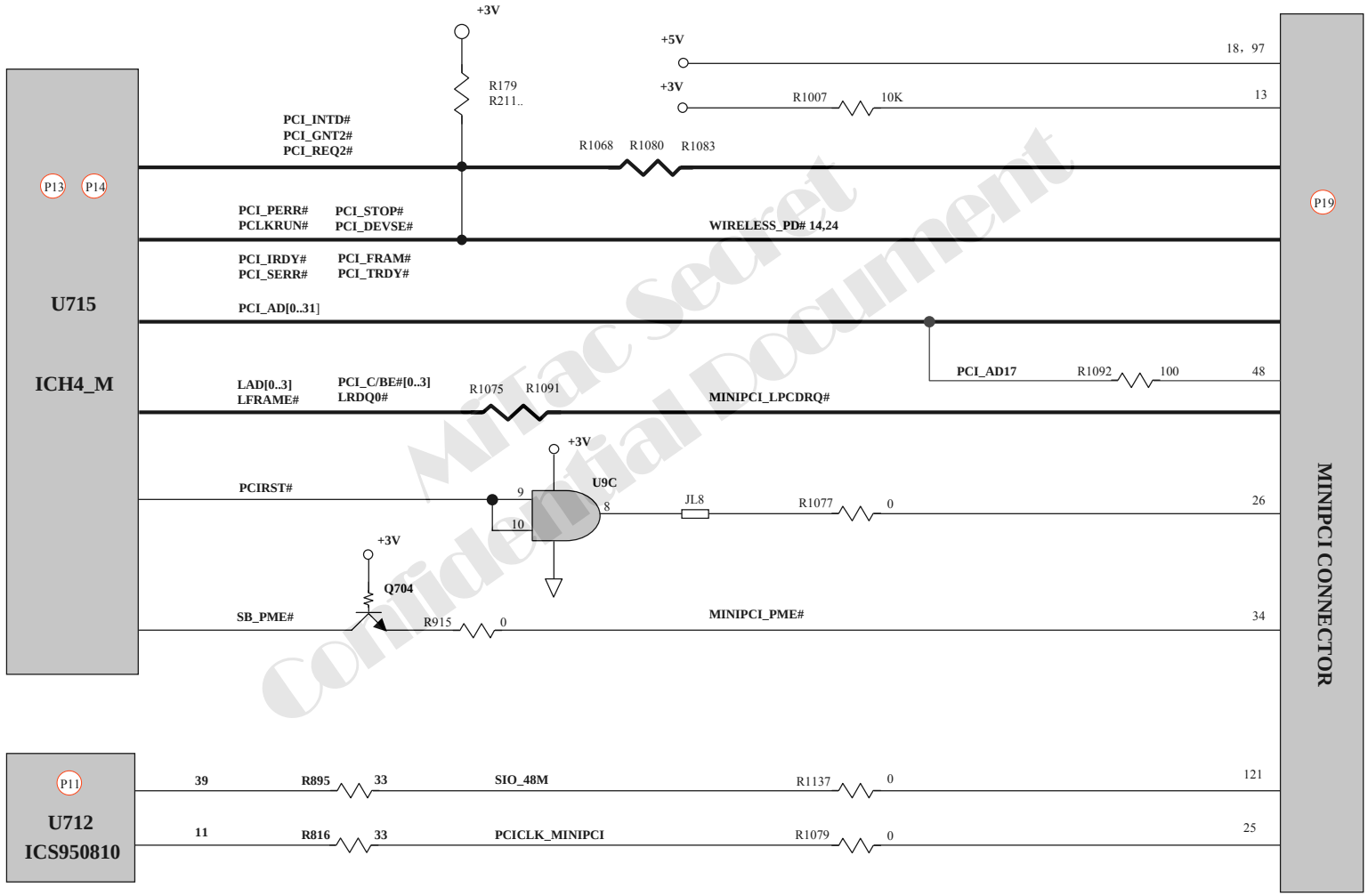


Check following parts and signals:

Parts:	Signals	
U727	AD[0..31]	PCIRST#
J716	C/BE# [0..3]	P_GNT0#
U728	DEVSEL#	PIRQA#
J6	FRAME#	SUSB#
U9	IRDY#	RI#
R186	TRDY#	PCLK_CARD
R180	STOP#	VCC5_EN#
R211	PAR	VCC3_EN#
R212	PERR#	VPPD0
R1121	SERR#	VPPD1
R1129	P_REQ0#	+VPPOUT
R826	SERIRQ	+3V
R1203		+5V

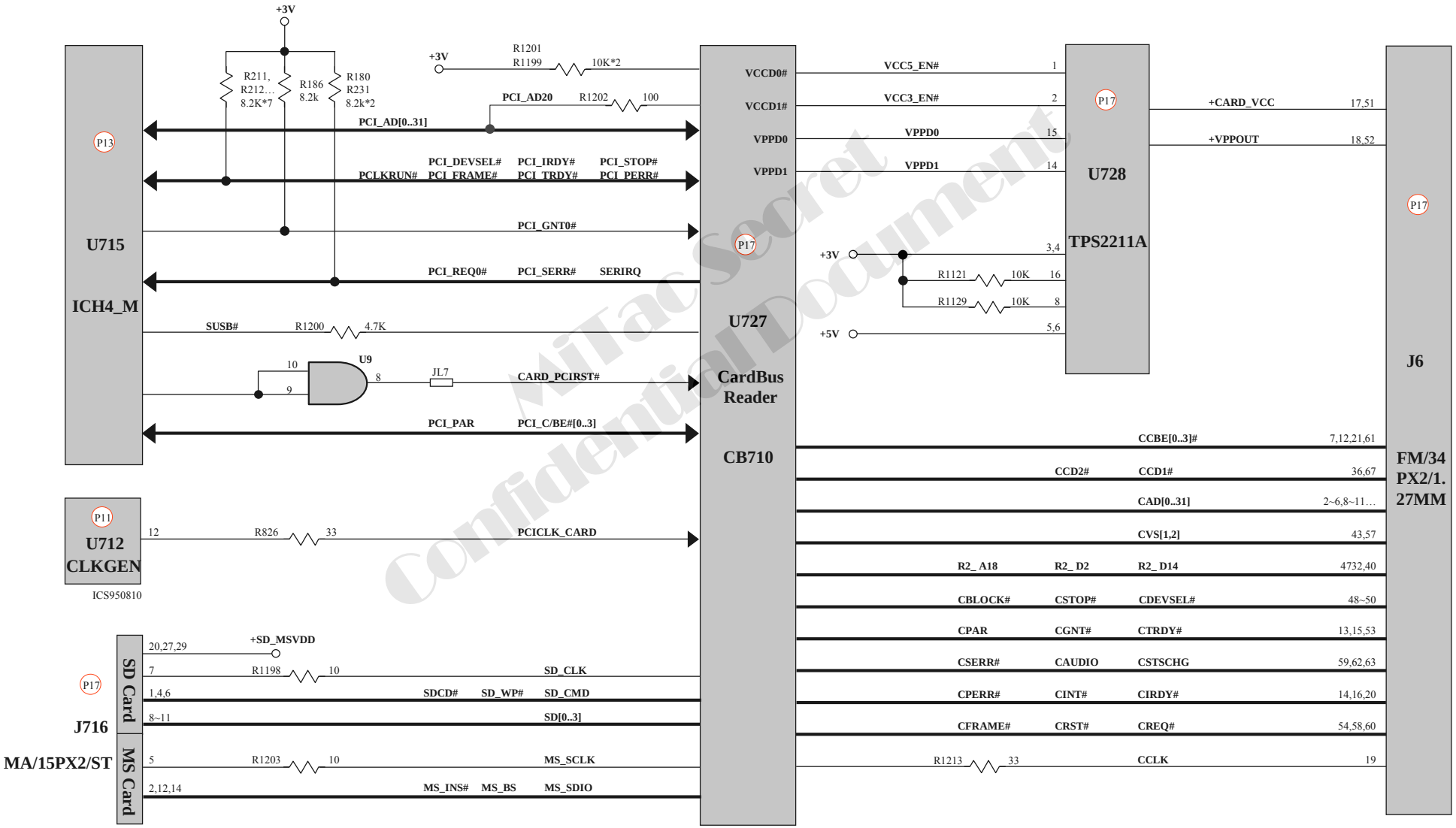
8.13 Mini PCI Test Error

An error message is shown after Mini PCI device is installed or the Mini PCI device doesn't work.



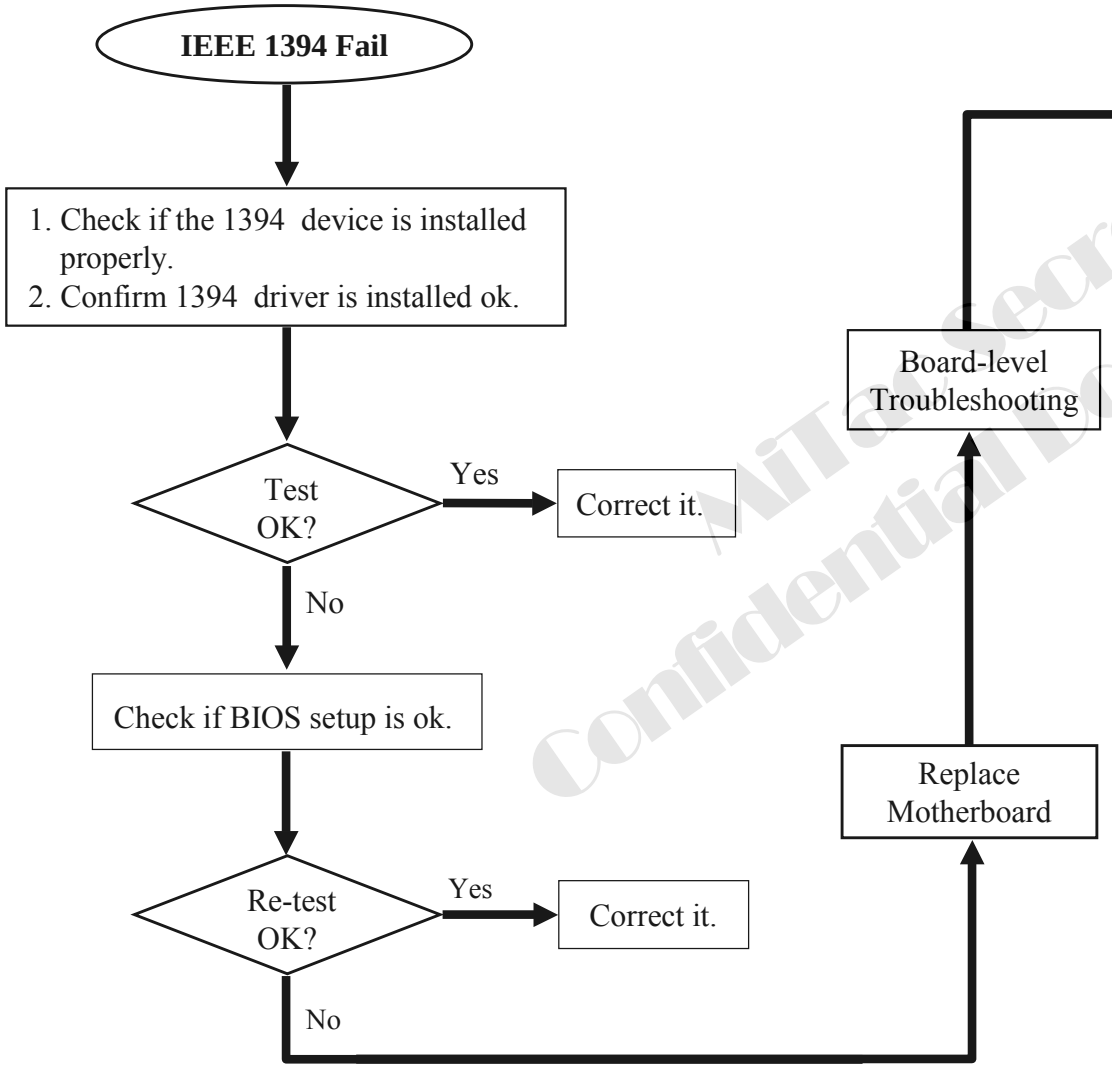
8.14 CardBus & Reader Test Error

An error occurs when a PC card device is installed.



8.15 IEEE 1394 Test Failure

An error occurs when a IEEE 1394 device is installed..

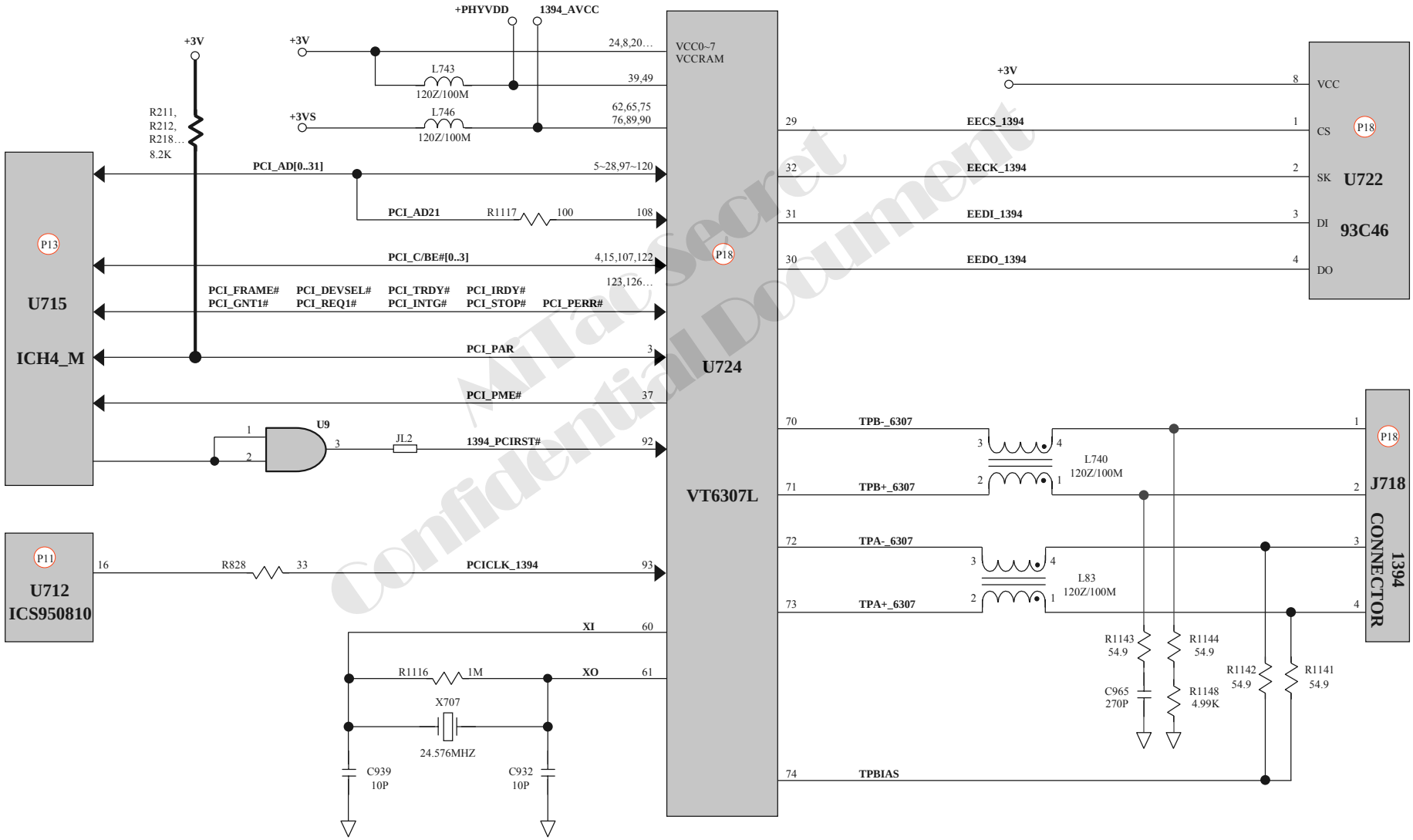


Check following parts and signals:

Parts:	Signals	
U724	PCI_AD[0..31]	1394_PCIRST#
U722	PCI_C/BE# [0..3]	PCI_GNT1#EE
J718	PC_DEVSEL#	CS_1394
U9	PCI_FRAME#	EECK_1394
U712	PCI_IRDY#	EEDI_1394
U715	PCI_TRDY#	EEDO_1394
L743	PCI_STOP#	TPBIAS
L746	PCI_PAR	TPA+_6307
L740	PCI_PERR#	TPA-_6307
L83	PCI_REQ1#	TPB+_6307
R1117	PCI_PME#	TPB-_6307
R828	+3V,+3VS	1394_AVCC
R1116	+PHYVDD	XI
R1142		XO
R1141		
X707		

8.15 IEEE 1394 Test Failure

An error occurs when a IEEE 1394 device is installed..



9. Spare Part List(1)

Part Number	Description	Location(S)
221600020252	CARTON;BATTERY,CAIMAN,PWR	
221600050218	PARTITION;BATTERY,MARLIN,CAIMAN,	
221600050219	PARTITION;TOP/BTM,BATTERY,MARLIN	
221673120003	CARTON;N-B,8060	
221673140001	BOX;AK,8060	
221673150001	PARTITION;AK BOX,8060	
221673150002	CARD BOARD;FRAME,PALLET,8060	
221673150003	CARD BOARD;TOP/BTM,PALLET,8060	
221673150004	PARTITION;PALLET,8060	
222503220001	PE BUBBLE BAG;BATTERY,GRAMPUS	
222670820003	PE BAG;L560*W345,7521N	
224670830002	PALLET;1250*1080*130,7521N	
225600000054	TAPE;INSULATING,POLYESTER FILM,1	
225600000061	TAPE;ADHENSIVE,DOUBLE-FACE,W20,U	
226600030332	SPONGE;320*290*10,CAIMAN,PWR	
227680900002	PAD;LCD/KB,8050	
227680900003	END CAP;NORMAL,L/R,8050	
242600000001	LABEL;PAL,20*5MM,COMMON	
242600000145	LABEL;10*10,BLANK,COMMON	
242600000145	LABEL;10*10,BLANK,COMMON	
242600000157	LABEL;BAR CODE,125*65,COMMON	
242600000232	LABEL;6*6MM,GAL,BLANK,COMMON	
242600000378	LABEL;27*7MM,HI-TEMP 260'C	
242600000385	LABEL;27*10,LAN ID BAR CODE	
242600000433	LABEL;BLANK,11*5MM,COMMON	

Part Number	Description	Location(S)
242600000439	LABEL;25*6,HI-TEMP,COMMON	
242600000452	LABEL;BLANK,7MM*7MM,PRC	
242600000452	LABEL;BLANK,7MM*7MM,PRC	
242664800013	LABEL;CAUTION,INVERT BD,PITCHING	
242668300028	LABEL;32*7MM,POLYESTER FILM,HOPE	
242669600005	LABEL;LOT NUMBER,RACE	
242669900009	LABEL;BLANK,60*80MM,7170	
242670800113	BFM-WORLD MARK;WINXP,7521N	
242678500005	CFM-INTEL;CENTRINO,NOTEBOOK,8081	
242679900005	LABEL;BAR CODE,(25*10MM)*12pcs,8	
242680900001	LABEL;AGENCY-GLOBAL,8050	
242680900002	LABEL;BATT,11.1V/4.4AH,LI,SANYO,	
242680900007	LABEL;17.3*5MM,BLANK,PWR	
271002000301	RES;0 ,1/10W,5% ,0805,SMT	L62,L65,L73,L88,R1,R123,R26,R2
271002472301	RES;4.7K ,1/10W,5% ,0805,SMT	PR704,PR706
271002604011	RES;604 ,1/10W,1% ,0805,SMT	R945,R946
271012000301	RES;0 ,1/8W,5% ,1206,SMT	PR86
271035012711	RES;.012,1W,1%,2010,LR2010,IRC,S	PR707,PR711,PR719,PR732,PR73
271044100101	RES;0.010,1.5W, 1%,2512,SMT;PWR	R6
271045087101	RES;.008 ,1W ,1% ,2512,SMT	PR742
271045107101	RES;.01 ,1W ,1% ,2512,SMT	PR701
271045507103	RES;0.050,1W, 1%,2512,SMT, only	R24A,R24B,R24C
271046017301	RES;.001,2W,5%,2512,CYNTEC,SMT	PR740
271061000002	RES;0 ,1/16W,0402,SMT	PR103,PR104,PR11,PR111,PR120
271061010101	RES;1,1/16W,1%,0402,SMT	PR18

9. Spare Part List(2)

Part Number	Description	Location(S)
271061100102	RES;10,1/16W,1%,0402,SMT	PR37,PR38,PR5
271061100501	RES;10 ,1/16W,5% ,0402,SMT	PR1,PR100,R1000,R1001,R1009,F
271061101103	RES;100 ,1/16W,1% ,0402,SMT	R1092,R1117,R1202,R208,R257,R
271061102105	RES;1K ,1/16W,1% ,0402,SMT	PR121,PR53,R1006,R141,R32,R32
271061102211	RES;1.02K,1/16W,1% ,0402,SMT	R110,R120
271061102303	RES;1K ,1/16W,5% ,0402,SMT	R102,R1136,R1147,R155,R206,R2
271061102312	RES;10.2K,1/16W,1% ,0402,SMT	R496,R502
271061103102	RES;10K ,1/16W,1% ,0402,SMT	PR102,PR119,PR127,PR129,PR4,
271061103501	RES;10K ,1/16W,5% ,0402,SMT	R1007,R104,R1098,R11,R1103,R1
271061104102	RES;100K ,1/16W,1% ,0402,SMT	PR10,PR112,PR114,PR12,PR130,
271061104501	RES;100K ,1/16W,5% ,0402,SMT	PR69,PR703,PR720,PR83,PR89,R
271061105501	RES;1M ,1/16W,5% ,0402,SMT	PR106,PR115,PR123,PR26,PR27,
271061106501	RES;10M ,1/16W,5% ,0402,SMT	R296,R938
271061107411	RES;107K,1/16W,1%,0402,SMT	PR35
271061118211	RES;11.8K,1/16W,1%,0402,SMT	PR116
271061124312	RES;124K,1/16W,1%,0402,SMT	PR79
271061127212	RES;12.7K,1/16W,1%,0402,SMT	PR17
271061133101	RES;13.7K,1/16W,1%,0402,SMT	PR96
271061133311	RES;13.3K,1/16W,1%,0402,SMT	PR19,PR29
271061135101	RES;1.3M,1/16W,1%,0402,SMT	PR16,R1158
271061137371	RES;13.7K,1/16W,.1%,0402,SMT	PR74
271061151102	RES;150 ,1/16W, 1%,0402,SMT	R220,R446,R772,R791,R850,R884
271061152302	RES;15K ,1/16W,5% ,0402,SMT	R1008
271061152501	RES;1.5K ,1/16W,5% ,0402,SMT	R1084
271061153102	RES;15K ,1/16W,1% ,0402,SMT	PR105,PR107,PR122,PR727,PR72

Part Number	Description	Location(S)
271061180101	RES;18.2 ,1/16W,1% ,0402,SMT	R838
271061183102	RES;18K,1/16W,1%,0402,SMT	PR718,R462,R507
271061184302	RES;180K ,1/16W, 5%,0402,SMT	R1140,R288
271061196212	RES;1.96K,1/16W,1%,0402,SMT	PR710
271061196213	RES;19.6K,1/16W,1%,0402,SMT	PR36,PR97,PR99
271061201101	RES;200 ,1/16W, 1%,0402,SMT	R280
271061202102	RES;2K ,1/16W,1% ,0402,SMT	PR101,PR124,PR46,PR725,PR731
271061203102	RES;20K ,1/16W,1% ,0402,SMT	PR117,PR21,PR41,PR722,PR726,
271061203701	RES;20K ,1/16W,.1%,0402,SMT	PR75
271061204102	RES;200K ,1/16W,1% ,0402,SMT	PR54,PR55
271061205212	RES;20.5K,1/16W,1%,0402,SMT	PR113
271061220102	RES;22,1/16W,1% ,0402,SMT	R253
271061220501	RES;22 ,1/16W,5% ,0402,SMT	R105,R1120,R1131,R306,R329,R4
271061221212	RES;2.21K,1/16W,1% ,0402,SMT	R72,R79
271061221312	RES;22.1K,1/16W,1% ,0402,SMT	R463,R479,R509,R510
271061221313	RES;220 ,1/16W, 5%,0402,SMT	R552,R555,R556,R557
271061222101	RES;2.2K,1/16W,1%,0402,SMT	PR6
271061222501	RES;2.2K ,1/16W,5% ,0402,SMT	R315,R318
271061223102	RES;22K,1/16W,1% ,0402,SMT	R325,R520
271061224501	RES;220K ,1/16W,5% ,0402,SMT	R251
271061226311	RES;226K,1/16W,1%,0402,SMT	PR71
271061232111	RES;2.32K,1/16W,1%,0402,SMT	PR39
271061240302	RES;24,1/16W,5%,0402,SMT	R106,R107,R108,R109,R29,R30,R
271061249211	RES;2.49K,1/16W,1% ,0402,SMT	PR77
271061249212	RES;24.9K,1/16W,1%,0402,SMT	PR128,PR98

9. Spare Part List(3)

Part Number	Description	Location(S)
271061249312	RES;249K,1/16W,1%,0402,SMT	PR729,PR76
271061270102	RES;27.4 ,1/16W, 1%,0402,SMT	R133,R213,R291
271061272102	RES;2.7K ,1/16W,1% ,0402,SMT	R448,R449
271061301112	RES;301 ,1/16W,1% ,0402,SMT	R793,R855
271061330501	RES;33 ,1/16W,5% ,0402,SMT	R1213,R77,R78,R816,R817,R818,I
271061331304	RES;330 ,1/16W,5% ,0402,SMT	R1073,R1089,R301
271061332312	RES;3.3K,1/16W,5% ,0402,SMT	PR70
271061333501	RES;33K ,1/16W,5% ,0402,SMT	PR45,R701,R706
271061390501	RES;39, 1/16W, 5%,0402,SMT	R225
271061391103	RES;390,1/16W,1% ,0402,SMT	R876
271061402011	RES;40.2 ,1/16W,1% ,0402,SMT	R119,R832
271061412111	RES;4.12K,1/16W,1%,0402,SMT	PR58
271061432212	RES;43.2K,1/16W,1%,0402,SMT	PR118,PR60,R1187,R1189,R1205
271061470501	RES;47 ,1/16W,5% ,0402,SMT	R750
271061471501	RES;470 ,1/16W,5% ,0402,SMT	R1085,R553,R554,R558
271061472501	RES;4.7K ,1/16W,5% ,0402,SMT	R10,R1081,R1132,R1154,R1200,R
271061473501	RES;47K ,1/16W,5% ,0402,SMT	R140,R442,R443,R702,R708,R929
271061474501	RES;470K ,1/16W,5% ,0402,SMT	PR702,R373
271061499012	RES;49.9 ,1/16W,1% ,0402,SMT	R1082,R1086,R1087,R1090,R209,
271061499212	RES;4.99K,1/16W,1% ,0402,SMT	PR20,R1148
271061499411	RES;499K ,1/16W,1% ,0402,SMT	PR43,PR716
271061510303	RES;51, 1/16W, 5%,0402,SMT	R224,R228,R238,R243,R289
271061549011	RES;54.9 ,1/16W,1% ,0402,SMT	R1141,R1142,R1143,R1144,R142,
271061560501	RES;56 ,1/16W,5% ,0402,SMT	R198,R264,R269,R273,R42,R43,R
271061562102	RES;5.6K ,1/16W, 1%,0402,SMT	R1099,R542

Part Number	Description	Location(S)
271061562212	RES;56.2K,1/16W,1%,0402,SMT	PR15
271061576411	RES;576K ,1/16W,1% ,0402,SMT	PR28
271061590411	RES;590K,1/16W,1%,0402,SMT	PR65
271061604011	RES;60.4 ,1/16W,1% ,0402,SMT	R923,R924
271061619211	RES;6.19K,1/16W,1% ,0402,SMT	PR81
271061634211	RES;6.34K,1/16W,1% ,0402,SMT	R1145
271061634214	RES;63.4K,1/16W,1%,0402,SMT	PR42
271061649212	RES;6.49K,1/16W,1% ,0402,SMT	PR721
271061681501	RES;680 ,1/16W,5% ,0402,SMT	R214
271061682501	RES;6.8K ,1/16W,5% ,0402,SMT	R537,R538,R546,R547
271061750501	RES;75 ,1/16W,5% ,0402,SMT	R152,R271,R277,R767,R768,R769
271061752102	RES;7.5K,1/16W,1%,0402,SMT	PR84
271061753101	RES;75,1/16W,1%,0402,SMT	R334,R340
271061806311	RES;80.6K,1/16W,1% ,0402,SMT	PR63,PR66
271061822501	RES;8.2K ,1/16W,5% ,0402,SMT	PR126,R1004,R1005,R1074,R111
271071000002	RES;0 ,1/16W,5% ,0603,SMT	L69,L719,L728,L744,L747,L751,I
271071101301	RES;100 ,1/16W,5% ,0603,SMT	R11,R12,R14,R15,R16,R20,R21
271071102302	RES;1K ,1/16W,5% ,0603,SMT	R11
271071103302	RES;10K ,1/16W,5% ,0603,SMT	R2
271071103302	RES;10K ,1/16W,5% ,0603,SMT	R1122
271071103302	RES;10K ,1/16W,5% ,0603,SMT	R5,R7,R8
271071104101	RES;100K ,1/16W,1% ,0603,SMT	R18,R22,R23,R9
271071104302	RES;100K ,1/16W,5% ,0603,SMT	R7
271071105301	RES;1M ,1/16W,5% ,0603,SMT	R10,R3
271071127011	RES;127 ,1/16W,1% ,0603,SMT	R14A

9. Spare Part List(4)

Part Number	Description	Location(S)
271071127011	RES;127 ,1/16W,1% ,0603,SMT	R163
271071131101	RES;130 ,1/16W,1% ,0603,SMT	R911
271071152302	RES;1.5K ,1/16W,5% ,0603,SMT	R17
271071152302	RES;1.5K ,1/16W,5% ,0603,SMT	R19
271071181101	RES;180 ,1/16W,1% ,0603,SMT	R777
271071201301	RES;200 ,1/16W,5% ,0603,SMT	R1A,R1B
271071202301	RES;2K ,1/16W,5% ,0603,SMT	R12
271071224301	RES;220K ,1/16W,5% ,0603,SMT	R1
271071274811	RES;27.4 ,1/16W,1% ,0603,SMT	R792,R839
271071301311	RES;301K ,1/16W,1% ,0603,SMT	R13,R3
271071331301	RES;330 ,1/16W,5% ,0603,SMT	R16,R21,R22
271071331301	RES;330 ,1/16W,5% ,0603,SMT	R18,R20,R23
271071331301	RES;330 ,1/16W,5% ,0603,SMT	C14
271071362101	RES;3.6K ,1/16W,1% ,0603,SMT	R1110
271071374812	RES;37.4 ,1/16W,1% ,0603,SMT	R898
271071432111	RES;4.32K,1/16W,1% ,0603,SMT	R10
271071432211	RES;43.2K,1/16W,1% ,0603,SMT	R1
271071472302	RES;4.7K ,1/16W,5% ,0603,SMT	PR87,PR88
271071478101	RES;4.7 ,1/16W,1% ,0603,SMT	PR108,PR109,PR110,PR2,PR3,PR
271071487011	RES;487 ,1/16W,1% ,0603,SMT,MUS	R883
271071487811	RES;48.7 ,1/16W,1% ,0603,SMT	R900
271071499011	RES;499 ,1/16W,1% ,0603,SMT	R764
271071499311	RES;499K ,1/16W,1% ,0603,SMT	R17
271071563101	RES;56K ,1/16W,1% ,0603,SMT	R6
271071622303	RES;620,1/16W,5% ,0603,SMT	R786

Part Number	Description	Location(S)
271071681813	RES;68.1,1/16W,1%,0603,SMT	R903
271071684101	RES;680K ,1/16W,1% ,0603,SMT	R5
271071713102	RES;715 ,1/16W,1% ,0603,SMT	R762
271071753301	RES;75K ,1/16W,5% ,0603,SMT	R8
271071822102	RES;8.2K ,1/16W,1% ,0603,SMT	R14B
271072287011	RES;287 ,1/10W,1% ,0603,SMT	R914
271072474101	RES;470K ,1/10W,1% ,0603,SMT	R4
271571000301	RP;0*8 ,16P ,1/16W,5% ,1606,SM	RP14,RP15,RP6,RP8
271571560302	RP;56*8 ,16P,1/16W,5% ,1606,SMT	RP29,RP30,RP31,RP32,RP33,RP3
271586026101	RES;.02 ,2W,1%,2512,SMT	PR22
271611000301	RP;0*4 ,8P ,1/16W,5% ,0612,SMT	RP10,RP16,RP27,RP718
271611103301	RP;10K*4 ,8P ,1/16W,5% ,0612,SMT	RP719
271611220301	RP;22*4 ,8P ,1/16W,5% ,0612,SMT	RP45
271611240302	RP;24*4 ,8P ,1/16W,5% ,0612,SMT	RP11,RP12,RP13,RP17,RP18,RP1
271611750301	RP;75*4 ,8P ,1/16W,5% ,0612,SMT	RP2
271621103302	RP;10K*8 ,10P,1/32W,5% ,1206,SMT	RP46,RP715
271621472302	RP;4.7K*8,10P,1/32W,5% ,1206,SMT	RP44
272001105403	CAP;1U ,10%,10V ,0805,X7R,SMT	PC3,PC46
272001106702	CAP;10U,6.3V,+- 20%,0805,X5R,SMT	C110,C112,C114,C121,C122,C127
272001475701	CAP;4.7U ,CR,10V ,+80-20%,0805,Y	C311,C517,C871,C941,C947
272002225701	CAP;2.2U ,CR,16V ,+80-20%,0805,Y	C921,C961
272003105701	CAP;1U ,CR,25V ,+80%-20%,0805,	PC701
272005104402	CAP;.1U ,50V,+/-10%,0805,X7R,SMT	PC9
272005104404	CAP;.1U,CR,50V,10%,0805,SMT	PC4,PC51,PC52,PC65,PC66,PC7,
272005104705	CAP ;1U CR 50V +80-20% 0805 Y5V	C14A,C14B,C4A,C4B

9. Spare Part List(5)

Part Number	Description	Location(S)
272010101301	CAP;100P,2KV,5%,1206,NPO,SMT,onl	C18
272010101302	CAP;100P,2KV,5%,1206,NPO,SMT,onl	
272011106701	CAP;10U ,10V,+80-20%,1206,Y5V,S	C166,C174,C238,C271,C355,C772
272012105401	CAP;1U ,CR,16V,10%,1206,X7R,S	C14A,C14B
272021106501	CAP;10U ,10V,20%,1210,X7R,SMT	C475
272023106502	CAP;10U,25V,M,1210,T2.5MM,X5R,SM	PC703,PC704,PC705,PC721,PC73
272023475502	CAP;4.7U,CR,25V,20%,1210,X7R,S	C1
272030050302	CAP;5P,3KV,5%,1808,NPO,SMT,only	C19
272030102401	CAP;1000P,2KV,10%,1808,X7R,SMT	C148,C327,C806
272070475701	CAP;4.7U,CR,6.3V,+80-20%,0603,Y5	C860,C908
272071105403	CAP;1U,10V,10%,0603,X5R,SMT	C10,C4
272071154401	CAP;.15U,CR,10V,10%,0603,X7R,SM	C482,C490
272071225401	CAP;2.2U,CR,6.3V,10%,0603,X5R,	C1001,C151,C161,C239,C24,C283
272071332401	CAP;.33U,10V,10%,0603,X7R,SMT	C2
272072104402	CAP;.1U ,CR,16V,10%,0603,X7R,SM	C17
272072104402	CAP;.1U ,CR,16V,10%,0603,X7R,SM	C12,C6
272072223401	CAP;.022U,16V,10%,0603,X7R,SMT	C471
272072824401	CAP;.082U,16V,10%,0603,X7R,SMT	C16
272073104401	CAP;.1U ,CR,25V,10%,0603,X7R,PR	C22,C7
272073223401	CAP;.022U,CR,25V,10%,0603,X7R,S	C9
272075101401	CAP;100P ,50V,10%,0603,COG,SMT	C20,C21
272075101404	CAP; 0.001U CR 50V 10% 0603 X7R	C13
272075103401	CAP;.01U,CR,50V,10%,0603,X7R,S	C13,C8
272075103401	CAP;.01U,CR,50V,10%,0603,X7R,S	C11,C3
272075103408	CAP ;0.1U CR 50V 10% 0603 X7R S	C10,C11,C12,C15,C3,C5,C6,C7,C8

Part Number	Description	Location(S)
272075222401	CAP;2200P,50V,10%,0603,X7R,SMT	C15A
272075222401	CAP;2200P,50V,10%,0603,X7R,SMT	C5
272075223702	CAP; 0.22U CR 50V +80-20% 0603	C1,C2,C20A,C24,C25
272075471401	CAP;470P ,50V,10%,0603,X7R,SMT	C15B
272075471409	CAP; 0.0047U CR 50V 10% 0603 X7	C4
272075473401	CAP;.047U,50V,10%,0603,X7R,SMT	C313
272102104401	CAP;.1U ,CR,10V,10%,0402,X5R,SM	PC44,PC80
272102105701	CAP;1U ,CR,6.3V,80-20%,0402,Y	C1002,C11,C160,C206,C210,C219
272102224701	CAP;.22U,10V,+80-20%,0402,Y5V,	C14,C483,C496,C515
272102334701	CAP;.33U,CR,10V,+80-20%,0402,Y	C964
272102473402	CAP;.047uF,16V,+-10%,0402,X7R,	C841
272103331401	CAP;33P ,25V,+/-10%,0402,NPO,S	C17,C19,C344
272105100303	CAP;10P ,CR,50V,5%,0402,NPO,SM	C789,C790,C791,C795,C796,C797
272105101401	CAP;100P,50V,5%,0402,COG,SMT	C150,C18,C20,C503
272105101402	CAP;100P,50V,+-10%,0402,NPO,S	C10,C330,C455,C498,C520,C521,
272105102408	CAP;1000P,CR,50V,10%,0402,X7R,SM	C960,C962,PC14,PC17,PC18,PC1
272105102501	CAP;1000P,50V,+/-20%,0402,X7R,S	C100,C1006,C1007,C1008,C101,C
272105103702	CAP;.01U,50V,+80-20%,0402,SMT	C106,C117,C120,C128,C132,C137
272105104701	CAP;.1U ,16V,+80-20%,0402,SMT	C1000,C102,C103,C104,C105,C10
272105181403	CAP;180P,50V,10%,0402,SMT	PC24,PC25,PC61,PC63,PC738
272105220402	CAP;22P ,50V,+-10%,0402,NPO,S	C447,C450,C765,C766,C855,C861
272105221403	CAP;220P,CR,50V,10%,0402,X7R,S	C165,PC11,PC73,PC734,PC75
272105222501	CAP;2200P,50V,+/-20%,0402,X7R,S	C470,C494,C509,C728,C869
272105270303	CAP;27P ,50V,5%,0402,COG,SMT	C794,C804,C914,C915
272105271403	CAP;270P,50V,+-10%,0402,X7R,SMT	C15,C21,C770,C782,C965

9. Spare Part List(6)

Part Number	Description	Location(S)
272105332402	CAP;3300P,50V,10%,0402,SMT	PC28,PC56
272105470402	CAP;47P ,50V ,+ -10%,0402,NPO,S	C1,C143,C144,C154,C172,C2,C4,C
272105471403	CAP;470P ,50V,10%,0402,X7R,SMT	C41,C729,C742,C751
272431157507	CAP;150U ,TPC,6.3V,20%,H1.9,7343	C701,C713,C743,C768,PC712,PC7
272431157512	CAP;150U,6.3V,+/-20%,H2.8,PT,NCC	
272431227402	CAP;220U,2V,-35/+10%,H1.9,S,SP-C	PC775,PC778,PC781,PC784
272431227504	CAP;220U ,4V ,20%,7343,POSCAP,SM	PC729,PC749
272431337506	CAP;330U,4V,20%,7343,SMT	PC787,PC788,PC811,PC815
272601107506	EC;100U ,6.3V,M,9.3*3.6,-55~105'	C466,C474,C489,C951
272625470401	CP;47P*4 ,8P,50V ,10%,1206,NPO,S	CP2
273000130001	FERRITE CHIP;120OHM/100MHZ,1608,	L19,L20,L38,L42,L43,L45,L56,L7
273000130006	FERRITE CHIP;600OHM/100MHZ,.2A,1	L13,L14,L16,L50,L52,L53,L55,L5
273000130015	FERRITE CHIP;220OHM/100MHZ,1608,	L58,L59,L60
273000130039	FERRITE CHIP;130OHM/100MHZ,1608,	L10,L11,L12,L36,L37,L7,L9
273000150002	FERRIET CHIP;120OHM/100MHZ,2012,	L41,L732,L735,L737
273000150013	FERRITE CHIP;120OHM/100MHZ,2012,	L15,L17,L18,L24,L27,L46,L47,L5
273000150033	PHASEOUT;FERRITE CHIP,120OHM/100	L743,L746
273000150307	FERRITE BEAD;120 OHM/100MHZ,3A,0	L26,L28,L29,L30,L31,L32,L33,L3
273000150313	CHOKE COIL;90OHM/100MHZ,20%,2012	L2,L22,L5
273000500092	CHOKE COIL;2.2UH ,20%,16A,3.5MM	PL719
273000500115	CHOKE COIL;400uH MIN,120mΩ MAX;	L724
273000610025	FERRITE ARRAY;120OHM/100MHZ,ONLY	FA2
273000620001	FERRITE ARRAY;600OHM/100MHZ,2520	L49,L51,L740,L83
273000990021	INDUCTOR;33uH,CDRH124,SUMIDA,SMT	PL710
273000990054	INDUCTOR;10UH,D124C,+/-20%,TOKO,	PL702,PL703

Part Number	Description	Location(S)
273000990127	INDUCTOR;IHLP5050CE-01-0.68uH,VI	PL711
273000990184	INDUCTOR;3.0UH,30%,CDRH5D28,H3.0	PL717
273000990185	INDUCTOR;3.9UH,30%,CDRH8D43,H4.5	PL706,PL707,PL715
273000990186	INDUCTOR;3.0UH,30%,CDRH6D28,H2.8	PL709,PL713,PL714
273001050039	XSFORMER;10/100 BASE,LF-H80P,SMT	U717
273001050069	TRANSFORMER;10/100 BASE,NS0013,S	
273001050160	XFMR;CI8.5,25T/2150T,300mH,ONLY	T1
274010800405	XTAL;8Mhz,30PPM,16PF,8*4.5,2P,SM	X1
274011431414	XTAL;14.318MHZ,32PF,50PPM,8*4.5,	X703
274012457406	XTAL;24.576MHZ,16PF,50PPM,8*4.5,	X707
274012500415	XTAL;25MHZ,20PF,30PPM,8.0*4.5,SM	X706
274012700406	XTAL;27MHZ,20PF,20PPM,8.0*4.5,SM	X702
274013276103	XTAL;32.768KHZ,20PPM,12.5PF,CM20	X704
281101015001	IC;MP1015EM-Z,CCFL CTRL,TSSOP20,	U1
282574008005	IC;74AHC08,QUAD 2-I/P AND,TSSOP,	U9
282574014004	IC;74AHC14,HEX INVERTER,TSSOP,14	U703
282574132001	IC;74AHCT1G32,SINGLE OR GAT,SOT2	U17
283449004001	IC;FLASH,512*8,FWH/LPC,PM49FL004	
283450040001	IC;FLASH,512*8,FWH,M50FW040K1,PL	
283467490001	IC;FLASH,512K*8,FWH,SST49LF004A,	
283467490002	IC;FLASH,512K*8,FWH,W39V040FAP,P	
283467530001	IC;EEPROM,S24CC02A,2K,SO8,SMT,ON	
283467540001	IC;EEPROM,M24C02-WMN6T,2K,SO8,SM	IC2
283467540002	IC;EEPROM,M93C46-WMN6T,64*16 BIT	U722,U723
283767540001	IC;K4D263238E,DDR SDRAM,4MX32,BG	U1,U3,U708,U709

9. Spare Part List(7)

Part Number	Description	Location(S)
283767540002	IC;EM6A9320BI-3.6M,DDR SDRAM,4MX	
283767630002	IC;HY8250128323,DDR SDRAM,4MX32,	
284500522001	IC;855GME GMCH,NORTH BRIDGE,BGA,	U714
284500655003	IC;ALC655,AUDIO CODEC,LQFP,48P,S	U726
284501014001	IC;ATI MOBILITY M10-P,A14,AGP,BG	U710
284502779001	IC;P2779A,EMI REDUCTION,SO8	U711
284506307001	IC;VT6307L,PCI-1394,2PORT,LQFP,1	U724
284507460002	IC;ADT7460,TEMPERATURE MTR,QSOP,	U706
284508100009	IC;RTL8100CL,LAN CONTROLLER,LQFP	U719
284582801044	IC;FW82801DBM,ICH4-M,BGA,421P	U715
284583950002	IC;W83L950D-Ver.C,LPC_KBC,LQFP,8	
284595081201	IC;ICS950812,CK408 CLOCK GEN,TSS	U712
286002040001	IC;BQ2040,GAS GAUGE,SO,16P,SMT	IC1
286100212001	IC;TPA0212,AMPLIFIER,TSSOP,24P,S	U524
286100393004	IC;LMV393,DUAL COMPARTOR,SSOP,8P	PU5
286100822002	IC;LMV822,OP AMP,DUAL,CMOS,MSOP,	U19
286104173001	IC;MAX4173F,I-SENSE AMP,SOT23,6P	PU1
286104871002	IC;LM4871LD,AUDIO AMP,4Ohm,2.5W,	U725
286300431014	IC;SC431LCSK-.5,.5%,ADJ REG,SOT2	PQ11
286300594001	IC;TL594C,PWM CONTROL,SO,16P	PU7
286300690001	IC;GMT690B,RESET CIRCUIT,2.93V,S	U10
286300710002	IC;CB710,CARDBUS/CARD READER,LFG	U727
286300812002	IC;S-812C,DECECTOR,SOT-89,PRC	IC3
286301117021	IC;AMS1117,VOL REGULATOR,1A,SOT-	U6
286301414001	IC;MM1414,PROTECTION,TSOP-20A,PR	IC4

Part Number	Description	Location(S)
286301470001	IC;SC1470,PWM CTRL,TSSOP,14P,SMT	PU16
286302211006	IC;CP2211,POWER DISTRI SW,REV.C1	U728
286302951015	IC;LP2951ACM,VOLTAGE REGULATOR,S	U11
286303107001	IC;AMS3107C,3.3V,1%,VOL REGULATO	U13
286303728002	IC;LTC3728LX,PWM CTRL,LTC,5X5 QF	PU14,PU15,PU2,PU703
286303734001	IC;LTC3734,PWM CONTROLLER,32-QFN	PU3
286309167001	IC;RT9167-47CB,200MA LDO REGULAT	U18
286309701001	IC;RT9701,POWER DISTRI SW,SOT23-	U701,U705
286369229301	IC;G692L293T,RESET CIRCUIT,2.93V	U21
288100024002	DIODE;RLZ24D,ZENER,23.63V,5%,SMT	PD701
288100032013	DIODE;BAS32L,VRRM75V,MELF,SOD-80	D24,D7,PD5
288100054001	DIODE;BAT54,30V,200mA,SOT-23	D10,D11,D15,D16,D2
288100054002	DIODE;BAT54C,SCHOTTKY DIODE,SOT2	D22,PD4
288100056005	DIODE;UDZ5.6B,ZENER,5.6V,UMD2,SM	D13
288100056005	DIODE;UDZ5.6B,ZENER,5.6V,UMD2,SM	ZD3,ZD4
288100056017	DIODE;BAW56LT1,70V,215MA,SOT-23,	D704,D715,PD1,PD6,PD7,PD705
288100070006	DIODE;BAV70LT1,70V,225MW,SOT-23,	D12,D18,PD702,PD704
288100099012	DIODE;BAV99LT1,70V,450MA,SOT-23,	PD2,PD3
288100140007	DIODE;B140,40V,1A,SMA,DIODES,SMT	PD706,PD725
288100340008	DIODE;B340LA,40V,3A,SMA,DIODES,S	PD713,PD714,PD718
288101040006	DIODE;SBM1040,10A,SCHOTTKY,POWER	PD703
288104148001	DIODE;RLS4148,200MA,500MW,MELF,S	D17,D19,D21,D27,D703
288105515001	DIODE;BZV55-C15,ZENER,5%,SOD-80,	PD709
288110355001	DIODE;1SS355,80V,100mA,SOD-23,SM	D2
288111544001	DIODE; 1SR-154-400 400V 1.0A	D1

9. Spare Part List(8)

Part Number	Description	Location(S)
288200144008	TRANS;DTA144EKA,PNP,SMT	Q1
288200301001	TRANS;FDV301N,N-CHANNEL,SOT23	Q42
288202215001	TRANS;MUN2215T1,N-MOSFET,SC59,SM	Q719,Q720
288202222019	TRANS;MMBT2222ALT1,NPN,TO236AB,O	PQ15
288202237002	TRANS;MUN2237T1,NPN,SOT-23,SMT,O	PQ24,Q47
288202240001	TRANS;MUN2240T1,NPN,SOT-23,ON	Q12,Q23,Q26,Q27,Q29,Q31,Q32,(
288202301001	TRANS;SI2301DS,P-MOSFET,SOT-23	Q13,Q14,Q24,Q43,Q48,Q51
288203904022	TRANS;MMBT3904L,NPN,Tr35NS,TO236	PQ10,PQ9,Q20,Q708,Q718
288204406001	TRANS;AO4406,N-MOS,.0165OHM,SO8	PU10,PU9
288204407001	TRANS;AO4407,P-MOS,.01OHM,SO8,SM	PQ701,PQ704,PQ707
288204409001	TRANS;AO4409,P-MOSFET,SO-8P,MSL,	Q3,Q5
288204410010	TRANS;AO4410,N-MOSFET,ID=18A,0.0	PU11,PU12,PU13,PU712
288204435003	TRANS;FDS4435,P-MOSFET,35mOHM,SO	Q9,U704,U707
288204800001	TRANS;SI4800DY,N-MOS,.0185OHM,SO	PU710,U7
288204900001	TRANS;AO4900,DUAL N-MOSFET WITH	PU4,PU6,PU702,PU705,PU707,P
288204914001	TRANS;AO4914,DUAL N-MOSFET,WITH	PU701
288221371002	TRANS;MUN2137T1,PNP,SMT,ON	PQ13,Q711
288227002006	TRANS;2N7002LT1,N-CHANNEL FET,ES	PQ1,PQ12,PQ14,PQ16,PQ17,PQ1
291000000029	CON;MINI 4 IN 1 SOCKET CONNECTOR	J2
291000000203	CON;HDR,MA,2P*1,3.5MM,R/A,SMT,SM	J2
291000000706	CON;BATTERY,7P,MA,2.5MM,R/A,C103	J703
291000010209	CON;HDR,MA,2P*1,1.25MM,H4.2,ST,S	J710
291000010303	CON;HDR,MA,3P*1,1.25MM,H4.2,ST,S	J707
291000010619	CON;HDR,MA,6P,ACES,87151-0607,SM	J4
291000013025	CON;HDR,MA,15P*2,ACES,88107-3000	J2

Part Number	Description	Location(S)
291000013027	CON;HDR,MA,15P*2,ACES,88026-3000	J716
291000020204	CON;HDR,MA,2P*1,3.5MM,R/A,SMT,SM	
291000020206	CON;HDR,MA,2P*1,1.25MM,H2.57,R/A	J3,J7,J705,J715
291000021105	CON;HDR,MA,11P*1,ACES,87213-1100	CN1
291000021105	CON;HDR,MA,11P*1,ACES,87213-1100	J1
291000023008	CON;HDR,FM,15P*2,0.8MM.H5,R/A,SM	J717
291000023011	CON;HDR,MA,15P*2,88031-3000,ACES	J1
291000152603	CON;FPC/FFC,26P,1MM,R/A,KBD,SMT	J5
291000251246	MINIPCI SOCKET;124P,R/A,0.8MM,H=	J713
291000256843	CON;IC CARD,68P,UP,STANDOFF 0.0	J6
291000614793	IC SOCKET;UPGA479M,479P,MOLEX	U713
291000622007	CON;DIMM,R/A,200P,.6,H9.2,REVERS	J711
291000811008	CON;PHONE JACK,2 IN 1,7.0MM,ALLT	J709
291000920605	CON;STEREO JACK,6P,W9.5,33184000	J719,J721
294011200016	LED;GREEN,H0.8,0603,CL-190G,SMT	D32,D33,D34,D35,D36,D37,D38
294011200034	LED;GREEN,H.8,0603,19-21VGC/TR,S	LED4,LED5
294011200034	LED;GREEN,H.8,0603,19-21VGC/TR,S	LED3,LED6
294011200043	LED;RE/GR,H0.8,L1.9,W1.6,19-22SR	LED1
294011200043	LED;RE/GR,H0.8,L1.9,W1.6,19-22SR	LED2
294011200069	LED;GREEN,19-21VGC/TR8,LED_CL190	
294011200069	LED;GREEN,19-21VGC/TR8,LED_CL190	
295000010028	FUSE;0.14A/60V,POLY SWITCH,PTC,S	F2
295000010048	FUSE;0.5A/15V,POLY SWITCH,SMD	F701
295000010114	FUSE;FAST,1.75A,63VDC,1206,SMT,P	F1
295000010140	FUSE;FAST,2A,63VDC,1206,SMT,0433	F1

9. Spare Part List(9)

Part Number	Description	Location(S)
295000010141	FUSE;FAST,3A,32VDC,1206,SMT,0433	PF703
295000010163	FUSE;NORMAL,7A/24VDC,0433007,120	PF1,PF2,PF702
295000010183	FUSE;FAST,1.75A,63VDC,1206,SMT,0	
295000100004	FUSE;FAST,1A,63V,1206,THIN FILM	F3
297004010001	SW;PUSH BUTTOM,5P,SPST,12VDC,50m	SW2,SW4,SW5
297120101007	SW;DIP,SPST,4P,24VDC,.025A,SMT	SW701
297140200003	SW;COVER SWITCH,0.1A,30V,4P,T-ME	SW1
310111103029	THERMISTOR;10K,1%,BN35-3H103F,18	RT1
316680900001	PCB;PWA-8050 M BD	R01
316680900006	PCB;PWA-8050/BATT ,PR AND GA BD	
316680900007	PCB;PWA-8050/Transition BD	R00
316681300001	PCB;PWA-INVERTER BD (DA-1A08-A);	R0F
322680900001	CABLE FFC;TP,8050	
323767720004	DDR SODIMM MODULE;256MB,77.10634	
324180786388	IC,CPU,BANIAS,1.5GHZ,MICRO-FCPGA	
331000000302	CON HOLDER;PCMCIA,UP,STANDOFF 0.	J6
331000004009	CON;IEEE1394,MA,4P*1,0.8MM,R/A	J718
331000007025	CONNECTOR;7 PIN,DIP,ALLTOP,C1034	CON1
331000008033	CON;USB,FM,H15.64,R/A,4P*2,2522A	J701
331030044019	CON;HDR,FM.22P*2,R/A,ST,ACE-1A2,	J714
331040004024	CON;HDR,MA,4P*1,H=5.9,R/A,USB,DI	J706
331040050018	CON;HDR,BTB R/A,0.8MM,S-TECH1507	J708
331660020005	DIMM SOCKET;DDR SODIMM 200P, CA0	J712
331710015016	CON;D,FM,15P,3ROW,SUYIN,070912FR	J702
331840010008	CON;STEREO JACK,10P,W/SPDIF,R/A,	J720

Part Number	Description	Location(S)
331870007007	CON;MINI DIN,7P,R/A,W/GROUND,330	J704
331910002006	CON;POWER JACK,2P,20VDC,5A,DIP	PJ701
332110020165	WIRE ;#20AWG,UL1007,L=160mm,RED,	CN1
332110020173	WIRE ;#20AWG,UL1007,L=256mm,BLAC	CN4
332110026150	WIRE ;#26AWG,UL1007,L=208mm,BLUE	CN2
332110026151	WIRE ;#26AWG,UL1007,L=142mm,YELL	CN3
332810000034	PWR CORD;250V/2.5A,2P,BLK,EU,175	
333050000117	SHRINK TUBE;UL,600V,105'C,ID2.5*	
335152000026	CFM-BAT;FUSE,THERMAL,NEC,SF91E	
335152000085	FUSE; 128 DC-7A/50V 139℃only UC	F1
335152000097	FUSE;LR4-73X,POLY SWITCH,PWR	
338536010052	BATTERY;LI,3.7V/2.2AH,18650,SANY	
339115000046	MICROPHONE;-60dB+-2dB,D6.0*H2.7,	MIC1
340680900002	SPEAKER ASSY;L,8050	
340680900003	SPEAKER ASSY;R,8050	
340680900004	COVER ASSY;8050	
340680900005	HOUSING ASSY;8050	
340680900006	BRACKET ASSY;SYSTEM,8050	
340680900008	SHIELDING ASSY;COVER,8050	
340680900009	BRACKET ASSY;TP,8050	
340680900010	COVER ASSY;HDD,8050	
340680900011	HOUSEING ASSY;LCD,8050	
340680900012	COVER ASSY;LCD,8050	
340680900020	BEZEL ASSY;COMBO,QSI,SBW242,8050	
340680900026	SHIELDING ASSY;HDD,8050	

9. Spare Part List(10)

Part Number	Description	Location(S)
340680900027	WLEN ASSY;CABLE,8050	
340680900028	WIRE ASSY;INVERTER,8050	
340680900029	COVER ASSY;MINIPCI,8050	
340680900034	SPEAKER ASSY;WOOFER,NEW,8050	
340680900035	HEATSINK ASSY;DESCRETE,UNP,8050	
340683400029	HEATSINK ASSY;NORTHBRIDGE,8050F	
341677000002	SPRING;SCREW,HEATSINK,LYNX	
341680900001	SPC SCREW;#4-1/4,8050	
342502900001	CONTACT PLATE;W4L27T0.15,7068	
342502900001	CONTACT PLATE;W4L27T0.15,7068	
342503200004	CONTACT PLATE;W4L63T0.15,1/4,T T	
342672200010	BRACKET;CD-ROM,8500	
342672400007	FINGER;EMI GROUNDING SMD FINGER	TP45,TP48,TP50
342677000014	SMT NUT;A40M20-50,EMI STOP,LYNX	MTG701,MTG702
342680900005	HINGE;R,8050	
342680900006	HINGE;L,8050	
342680900009	SMT NUT;A40M20-55,EMI STOP,8050	MTG703,MTG704
342683400005	SPRING;HEATSINK,VGA,8050F	
344680900002	cover;battery,8050	
344680900003	housing;battery,8050	
344680900009	COVER;REAR,R,8050	
344680900010	COVER;REAR,L,8050	
344680900011	COVER;HINGE,R,8050	
344680900015	COVER;CPU,8050	
344680900016	COVER;DDR,8050	

Part Number	Description	Location(S)
344680900048	DUMMY CARD;PCMCIA,8050	
344680900049	COVER;HINGE,L,8050	
345677000018	CONDUCTIVE TAPE;LCD,LYNX	
345677300001	RUBBER;SILICONE RUBBER,T=1.5mm,D	
346503100005	INSULATOR;5,BATTERY ASSY,7521Li	
346503200202	INSULATOR;BATT ASSY,ONE ROUND,BL	
346677000016	SPONGE;RTC,LYNX	
346677300001	INSULATOR;FIBER,UL94V-0,D=17.5mm	
346680900001	INSULATOR;MB,8050	
346680900002	INSULATOR;CARD READER,8050	
346680900005	INSULATOR;INVERTER,LCD,8050	
346680900007	INSULATOR;PCB,ASSY,L105,W12T1.0	
346680900009	INSULATOR;PCMCIA,8050	
346680900010	INSULATOR;DDR,MINIPCI,8050	
346680900011	MYLAR;COVER,LCD,8050	
346680900017	INSULATOR;L16W8.5T0.05MM,DIALAMY	
346681800004	INSULATOR;BATT,ASSY,L129W15T0.25	
347105015007	GASKET;1,05,015,007	
347105030025	GASKET;1,05,030,025	
347105035020	GASKET;1,05,035,020	
347108030008	GASKET;1,08,030,008	
347110003010	GASKET;1,10,003,010	
347110010010	GASKET;1,10,010,010	
361200001018	CLEANNER;YC-336,LIQUID,STENCIL/P	
361400003003	JET-MELT ADHESIVES;3478-Q,5/8in*	

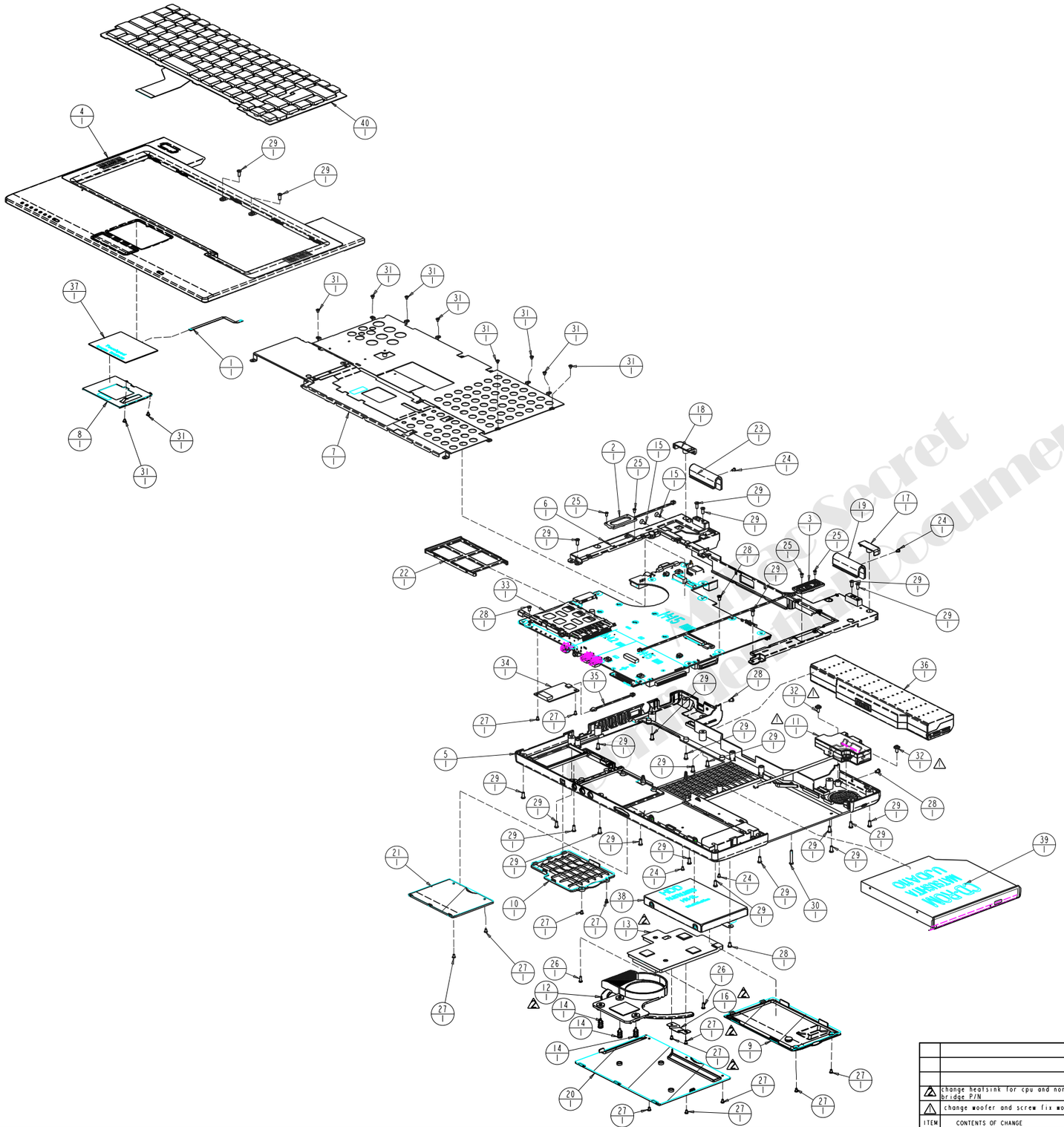
9. Spare Part List(11)

Part Number	Description	Location(S)
361400003005	ADHESIVE;HEAT,TRANSFER,HTA-48(W)	
361400003021	SOLDER CREAM;NOCLEAN,P4020870980	
361400003021	SOLDER CREAM;NOCLEAN,P4020870980	
361400003030	ADHESIVE;ABS+PC PACK,G485,CEMIDA	
365350000003	SOLDER WIRE;0.8MM,SN43/PB43/BI14	
370102010201	SPC-SCREW;M2L2,NIW,K-HD,t=0.8,NL	
370102010303	SPC-SCREW;M2L3,NIW,K-HD(+),NYLOK	
370102010409	SPC-SCREW;M2L4,K-HD(t0.3),NIB/NL	
370102010409	SPC-SCREW;M2L4,K-HD(t0.3),NIB/NL	
370102010502	SPC-SCREW;M2 L5,NIB,K-HD,t0.8,NL	
370102010607	SPC-SCREW;M2L6,K-HD(+),NIW/NLK,H	
370102030301	SPC-SCREW;M2L3,K-HD,1,NIB/NLK	
370102030301	SPC-SCREW;M2L3,K-HD,1,NIB/NLK	
370102610401	SPC-SCREW;M2.6L4,K-HD,t0.8,NIB/N	
370102610401	SPC-SCREW;M2.6L4,K-HD,t0.8,NIB/N	
370102610603	SPC-SCREW;M2.6L6,K-HD,NIB/NLK	
370102610603	SPC-SCREW;M2.6L6,K-HD,NIB/NLK	
370102611601	SPC-SCREW;M2.6*L16,NIB,K-HD	
370103010405	SPC-SCREW;M3L4,NIW,K-HD,T0.3	
371102010252	SCREW;M2L2.5,K-HEAD(+),NIB/NLK	
371102010252	SCREW;M2L2.5,K-HEAD(+),NIB/NLK	
371102610603	SCREW;M2.6L6,FLNG/PAN(+),NIW/NLK	
373101712351	T-SCREW;B,M1.7,L2.35,K-HD,2,NIB	
411680900019	PWA;PWA-8050-4 in 1 TRANSITION B	
411681300001	PWA;PWA-INVERTER BD,DA-1A08-A,PW	

Part Number	Description	Location(S)
411681300002	PWA;PWA-INVERTER BD,SMT,DA-1A08-	
411681300003	PWA;PWA-INVERTER BD,SMT TOP,DA-1	
411681300004	PWA;PWA-INVERTER BD,SMT BOT,DA-1	
411681710001	PWA-PWA-BATT BD;LI,4.4Ah,2P3S,BL	
411681710002	PWA-PWA-BATT BD;SMT,BL3244G095/8	
411682700001	PWA;PWA-8050D,ATIM-A14-64M,MOTHE	
411682700002	PWA;PWA-8050D,ATIM-A14-64M,MOTHE	
411682700003	PWA;PWA-8050D,ATIM-A14-64M,MOTHE	
412155600047	PCB ASSY;MDM,56K,UNIV,F-PACK,WO/	
412673400008	PCB ASSY;MINI-PCI,TYPE IIIB,INTE	
412681300001	PCB ASSY;D/A BD,DA-1A08-A,PWR	
413000020388	LCD;LTN154X1-L02,TFT15.4",XGA,SA	
416268090002	LT PF;SAMSUNG,15.4",LTN154WX,805	
422674300071	WIRE ASSY;MDC,E-NOTE	
422677000008	WIRE ASSY;BATT TO MB,FOR LYNX,MO	J710
422680900003	WIRE CABLE;SAM LTN154X1,8050	
431680900004	CASE KIT;8050D,ATIM	
441674800032	CONTACT PLATE ASSY;W4L27T0.15,S-	
441680900031	LCD ASSY;SAMSUNG,XGA,15.4",LTN15	
441681700001	BATT ASS'Y;11.1V,4.4Ah,LI,BL3244	
441681700002	BATT ASSY;11.1V,4.4Ah,LI,CASE CL	
441681700003	BATT ASSY;11.1V,4.4Ah,LI,CORE PA	
441681710031	CONTACT PLATE ASSY;W4L27T0.15,FU	
442672600031	AC ADPT ASSY;19V,3.16A,DELTA,706	
442680900051	TOUCHPAD MODULE;SYNAPTICS,TM42PU	

9. Spare Part List(12)

Part Number	Description	Location(S)
451680900001	LABEL KIT;N-B,8050	
451680900031	HDD ME KIT;8050	
451680900051	LCD ME KIT;SAMSUNG,15.4",8050	
451680900072	HOUSING KIT;8050,ATIM10/11	
451680900093	HEATSINK ASSY DISCRETE;UNP,8050	
451680900094	HEATSINK ASSY DISCRETE;MPT,8050	
451680900151	ROM ME KIT;8050	
451999900003	HEATSINK DISCRETE OPTION;8050	
461680900006	PACKING KIT;N-B BOX,8050	
481680900001	F/W ASSY;SYS/VGA BIOS,8050,ATIM	U15
481680900002	F/W ASSY;KBD CTRL,8050	U16
523402379038	HD DRIVE,40GB,2.5",MHT2040AT,FUJ	
523430061010	DVD COMBO DRIVE;24X10X8X24,SBW-2	
523468090002	HDD ASSY;40GB,MHT2040AT,FUJITSU,	
523468090029	COMBO ASSY;SBW-242B,QSI,8050	
526268270004	LTX;8050DA/5ACB/40H/9UI9/A5D3A/X	
531020237777	KBD;88,UI,K011818A1,8050,BK	
600100010009	SOLDER WIRE;63/37,0.8,CM,N/C,PRC	
600100010009	SOLDER WIRE;63/37,0.8,CM,N/C,PRC	
600100010009	SOLDER WIRE;63/37,0.8,CM,N/C,PRC	
624200010140	LABEL;5*20,BLANK,COMMON	
		P/N:526268270004



ITEM	PART NO	DESCRIPTION	Q'TY	TYPE	REMARK
1	322680900001	CABLE FFC;TP,8050	1	PART	
2	340680900002	SPEAKER ASSY;L,8050	1	ASSEMBLY	
3	340680900003	SPEAKER ASSY;R,8050	1	ASSEMBLY	
4	340680900004	COVER ASSY;8050	1	ASSEMBLY	
5	340680900005	HOUSING ASSY;8050	1	ASSEMBLY	
6	340680900006	BRACKET ASSY;SYSTEM,8050	1	ASSEMBLY	
7	340680900008	SHIELDING ASSY;COVER,8050	1	ASSEMBLY	
8	340680900009	BRACKET ASSY;TP,8050	1	ASSEMBLY	
9	340680900010	COVER ASSY;HDD,8050	1	ASSEMBLY	
10	340680900029	COVER ASSY;MINIPCI,8050	1	ASSEMBLY	
△1 11	340680900034	SPEAKER ASSY;WOOFER,NEW,8050	1	ASSEMBLY	
△2 12	340680900035	HEATSINK ASSY;DESCRETE,UNP,8050	1	ASSEMBLY	
△2 13	340683400029	HEATSINK ASSY;NORTHBRIDGE,8050F	1	ASSEMBLY	
14	341677000002	SPRING-SCREW-HEATSINK-LYNX	3	PART	
15	341680900001	SPC SCREW;#4-1/4,8050	2	PART	
16	342683400005	SPRING;HEATSINK,VGA,8050F	1	PART	
17	344680900009	COVER;REAR,R,8050	1	PART	
18	344680900010	COVER;REAR,L,8050	1	PART	
19	344680900011	COVER;HINGE,R,8050	1	PART	
20	344680900015	COVER;CPU,8050	1	PART	
21	344680900016	COVER;DDR,8050	1	PART	
22	344680900048	DUMMY CARD;PCMCIA,8050	1	PART	
23	344680900049	COVER;HINGE,L,8050	1	PART	
24	370102010303	SPC-SCREW; M2L3,NIW,K-HD(+),NYLO	4	PART	
25	370102010409	SPC-SCREW;M2L4,K-HD(+0.3),NIB/NL	4	PART	
26	370102010607	SPC-SCREW;M2L6,K-HD(+),NIW/NLK,H	2	PART	
△2 27	370102030301	SPC-SCREW; M2L3,K-HEAD,I,NIB,NLK	13	PART	
28	370102610401	SPC-SCREW;M2.6L4,K-HD,+0.8,NIB/N	5	PART	
29	370102610603	SPC-SCREW; M2.6L6 K-HEAD,NIB/NLK	25	PART	
30	370102611601	SPC-SCREW; M2.6LI6 K-HEAD,NIB	1	PART	
31	371102010252	SCREW;M2L2.5,K-HEAD(+),NIB/NLK	10	PART	
△ 32	371102610603	SCREW;M2.6L6,FLNG/PAN(+),NIW/NLK	2	PART	
33	411682700001	PWA;PWA-8050D,ATIM-AI4-64M,MOTHE	1	ASSEMBLY	
34	412671800001	PCB ASSY;FAXMODEM,56K,MDC,GP2	1	PART	
35	422674300071	WIRE ASSY;MDC,E-NOTE	1	ASSEMBLY	
36	441681700001	8050/II.IV,4.4AH,LI-ION(SANYO 2	1	ASSEMBLY	
37	442680900051	TOUCH PAD;SYNATICS,TM42P-313	1	PART	
38	451680900031	HDD ME KIT;8050	1	ASSEMBLY	
39	451680900033	COMBO MEKIT;KME,UJDA750,8050	1	ASSEMBLY	
40	531082132029	KBD;87,US,CHICONY,8050	1	PART	

ITEM	CONTENTS OF CHANGE	RVS	CHK	APV	M/D/Y
△2	change heatsink for cpu and north-bridge P/N	02			02/13/04
△1	change woofer and screw fix woofer	01			02/06/04

TOL ± RANGE	Pla	Met	Ins	Por	Cab	Pac	Gas	PCB
0~6	0.1	0.1	0.1	0.2	0.5	1	0.5	0.1
6~30	0.1	0.1	.15	.25	1	1	0.5	0.1
30~80	0.1	.15	0.2	0.3	2	1.5	1	0.1
80~180	.15	.15	.25	0.3	2	2	1	.15
180~315	.15	0.2	0.3	0.4	2.5	2	1	.15
315~800	0.2	0.3	0.4	0.5	3	3	2	.15

DATE	10-Sep-03	MATERIAL	SEE NOTES	TREATMENT		REMARK			
UNIT	MM	SCALE	0.40	DRAWING NAME	HOUSING KIT;8050,ATIM10/11				
DRAWN	DESIGNED	CHECKED	APPROVED	MATERIAL NO.	AD 451 6809 00072 R 02				

MiTAC Technology Corp.

model name:STRU-8050 | file name:HOUSING_KIT-8050D | SHEET NO. 1 of 1

8050D R01

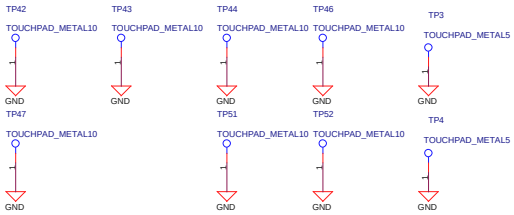
PROJECT CODE- G113
PRODUCT CODE- 6827

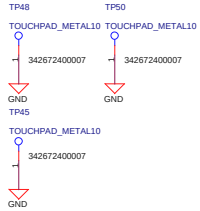
PCB P/N 316680900001
ASSY P/N 411682700001

PCI DEVICE	INTERRUPT	REQ/GNT	IDSEL
LAN	PCI_INTE#	PCI_REQ3# / PCI_GNT3#	AD18
CARDBUS / CARDREADER	PCI_INTB# / PCI_INTC#	PCI_REQ0# / PCI_GNT0#	AD20
IEEE1394	PCI_INTG#	PCI_REQ1# / PCI_GNT1#	AD21
MINIPCI	PCI_INTD#	PCI_REQ2# / PCI_GNT2#	AD17

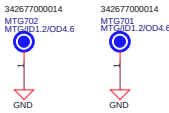
REVISION	TAPEOUT DAY	HISTORY
R00	2003/8/26	
R0A	2003/10/09	1. CHANGE CARDBUS/CARD READER CONTROLLER FROM R5C592 TO CB710 2. USE IEEE1394 CONTROLLER VT6307 INSTEAD OF R5C592 3. ADD SPDIF FUNCTION 4. CHANGE CARDBUS CONNENTOR PLACEMENT FORM COMPONENT SIDE TO SOLDER SIDE 5. CHANGE MDC AND MINIPCI CONNECTORS PLACEMENT FROM SOLDER SIDE TO COMPONENT SIDE 6. CHANGE LVDS ROUTING FAR AWAY POWER SWITCHING SIGNALS
R0B	2003/11/07	1. CHANGE TV CONNECTOR 2. CHANGE BATTERY CONNECTOR
R01	2003/12/16	1. EXCHANGE TV CONNECTOR PIN 6 AND PIN 7 2. ADD POWER CONSUMPTION SAVING CIRCUIT BUT RESERVE 3. CHANGE SOME BEAD TO 0 OHM IN AUDIO REGION 4. CHANGE SOME RESISTOR AND CAPACITANCE TO INCREASE SUBWOOFER GAIN 5. DELETE SOME COMPONENT AROUND TV ENCODER

EMI

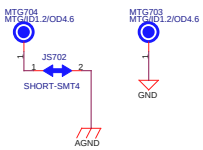




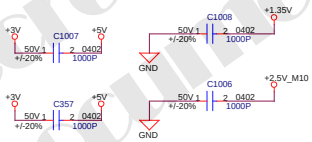
MDC



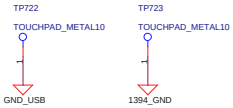
CARDREADER

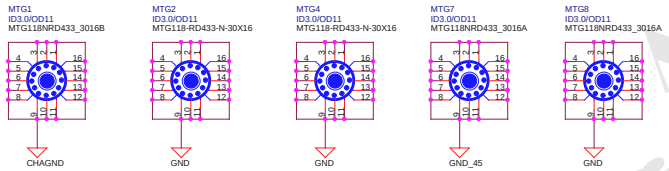


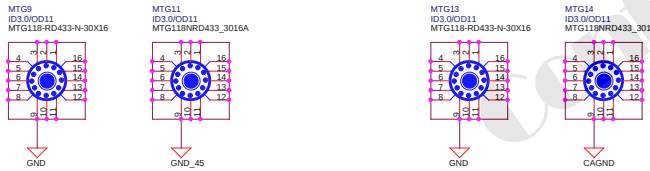
EC

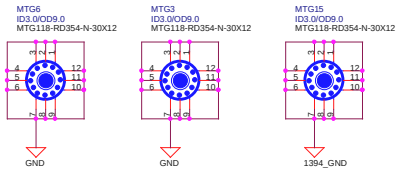


ESD

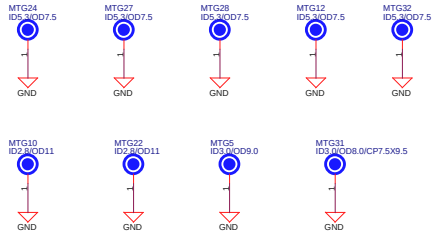




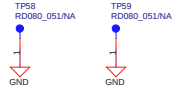


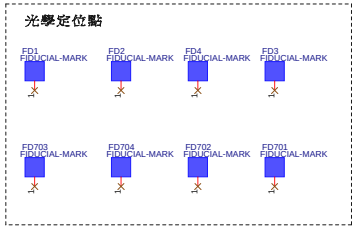


CPU



8050N





DRAWN	DESIGN	CHECK	ISSUES

MiTAC

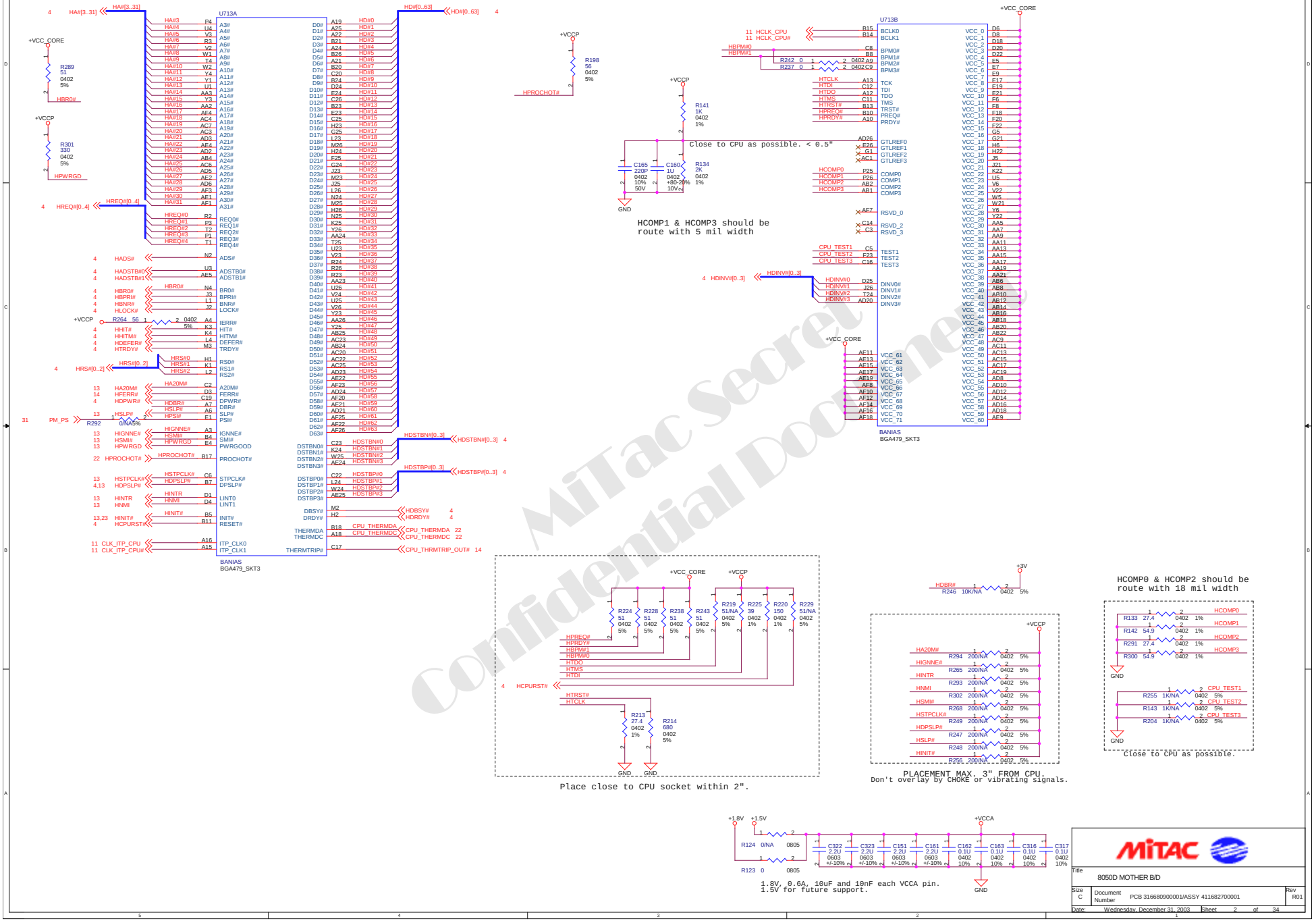
Title: 8050D MOTHER B/D

Size: C | Document Number: PCB 316680900001/ASSY 411682700001 | Rev: R01

Date: Wednesday, December 31, 2003 | Sheet 1 of 34

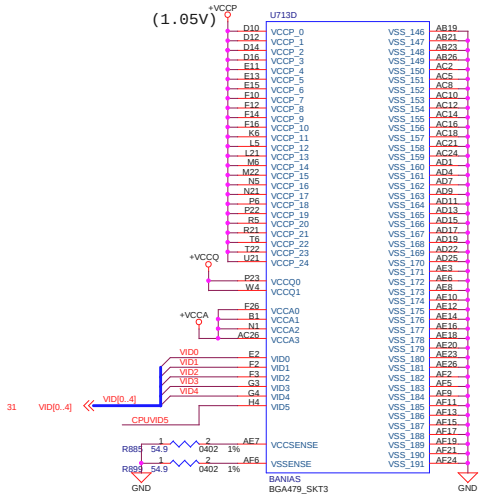
VCC : PROCESSOR CORE POWER SUPPLY.
VCCA : ISOLATE POWER FOR INTERNAL PLL.
VCCP : PROCESSOR I/O POWER SUPPLY.
VCCQ : QUIET POWER SUPPLY FOR ON DIE COMP CKT.

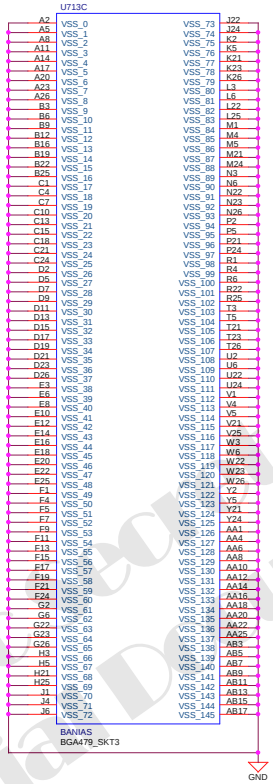
CPU-BANIAS (1/2)

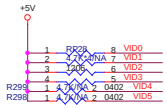


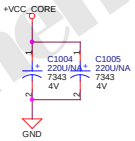
Title	8050D MOTHER B/D
Size C	Document Number PCB 316680900001/ASSY 411682700001 Rev R01
Date: Wednesday, December 31, 2003	Sheet 2 of 34

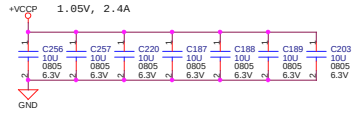
CPU-BANIAS (2/2)

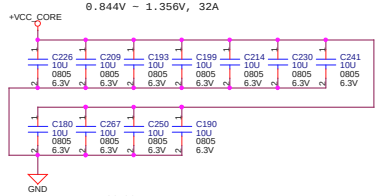


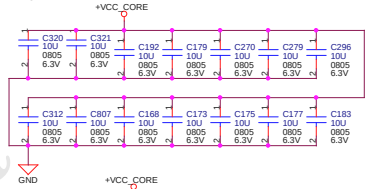


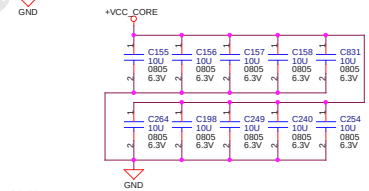


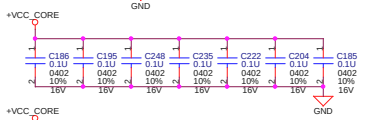


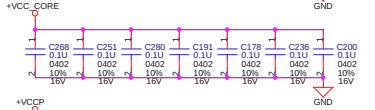


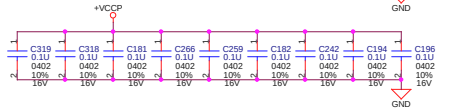


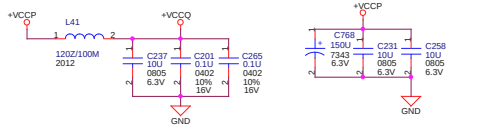


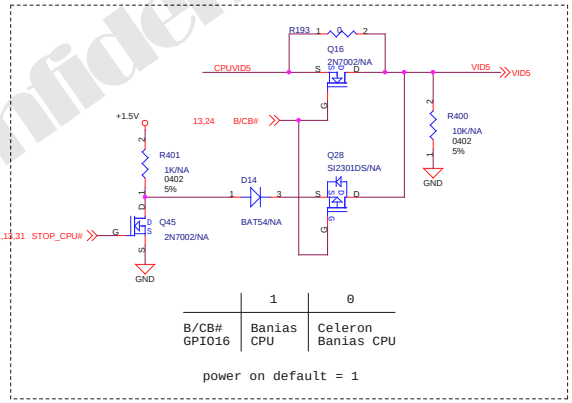












B/CB# GPIO16	1	0
	Banias CPU	Celeron Banias CPU

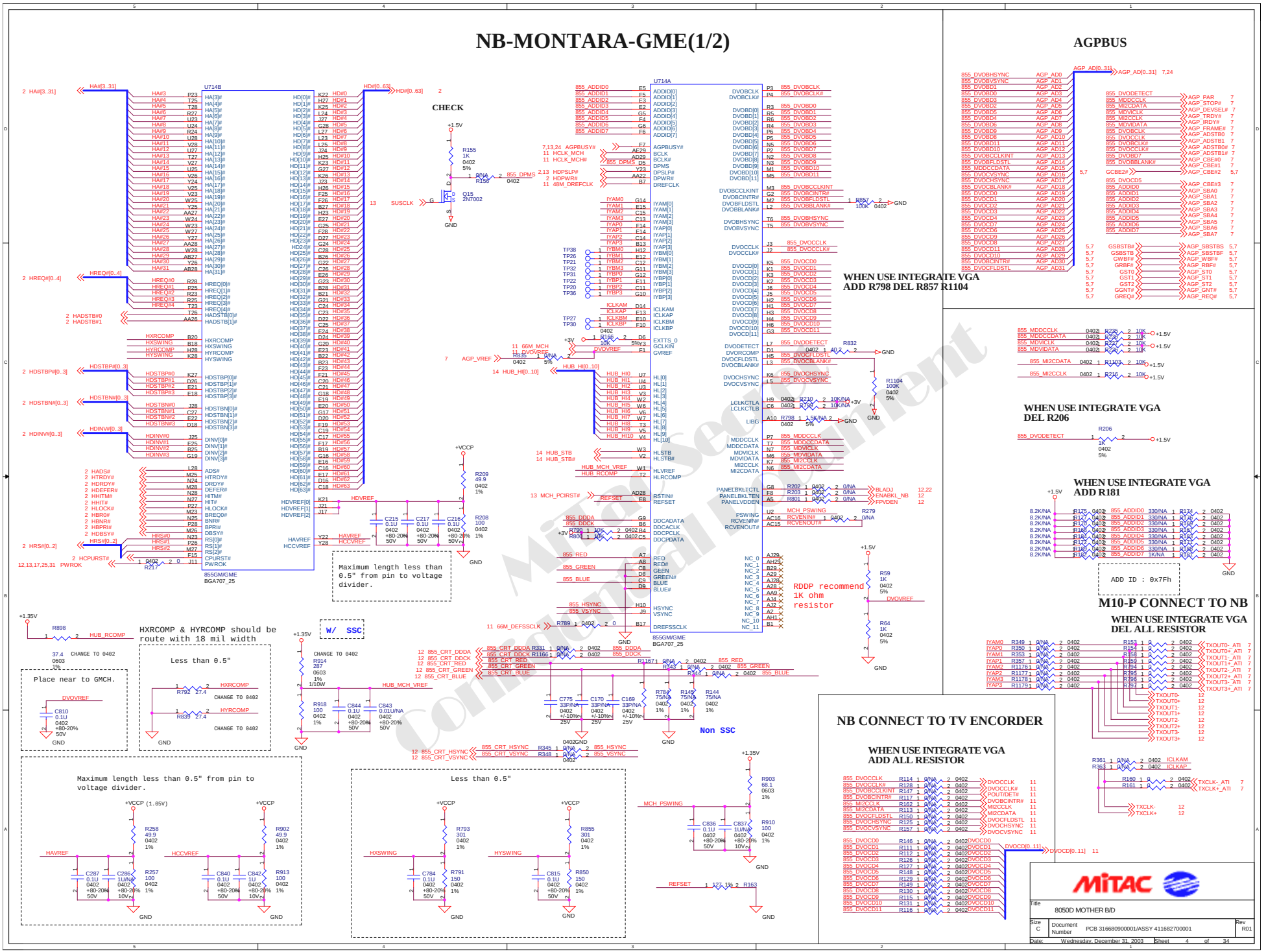
power on default = 1

POWER CONSUMPTION SAVING CIRCUIT

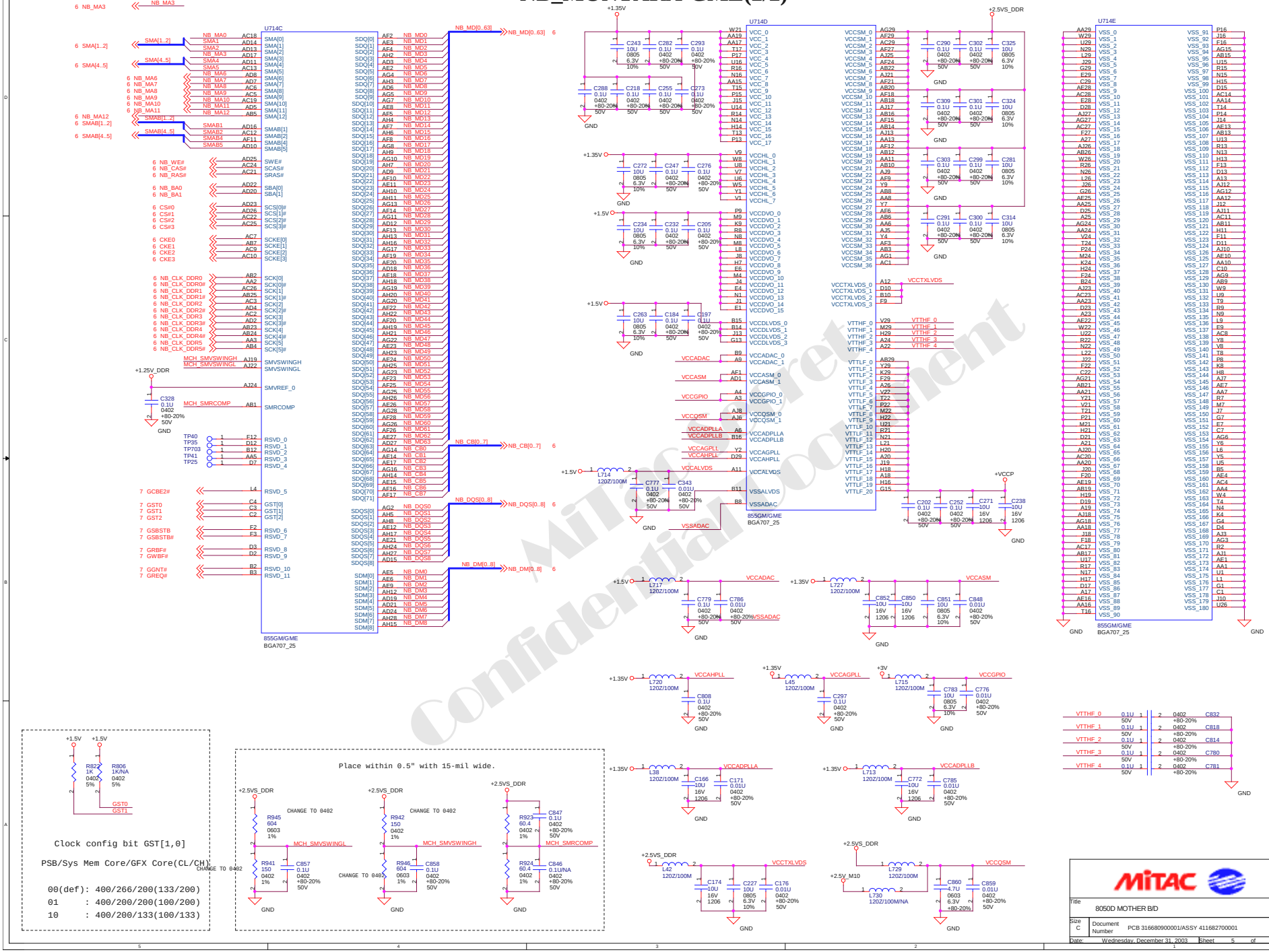
VID 5	4	3	2	1	0	VCC-Core
0	0	0	0	0	0	1.708
0	0	0	0	0	1	1.692
0	0	0	0	1	0	1.676
0	0	0	0	1	1	1.660
0	0	0	1	0	0	1.644
0	0	0	1	0	1	1.628
0	0	0	1	1	0	1.612
0	0	0	1	1	1	1.596
0	0	1	0	0	0	1.580
0	0	1	0	0	1	1.564
0	0	1	0	1	0	1.548
0	0	1	0	1	1	1.532
0	0	1	1	0	0	1.516
0	0	1	1	0	1	1.500
0	0	1	1	1	0	1.484
0	0	1	1	1	1	1.468
0	1	0	0	0	0	1.452
0	1	0	0	0	1	1.436
0	1	0	0	1	0	1.420
0	1	0	0	1	1	1.404
0	1	0	1	0	0	1.388
0	1	0	1	0	1	1.372
0	1	0	1	1	0	1.356
0	1	0	1	1	1	1.340
0	1	1	0	0	0	1.324
0	1	1	0	0	1	1.308
0	1	1	0	1	0	1.292
0	1	1	0	1	1	1.276
0	1	1	1	0	0	1.260
0	1	1	1	0	1	1.244
0	1	1	1	1	0	1.228
0	1	1	1	1	1	1.212

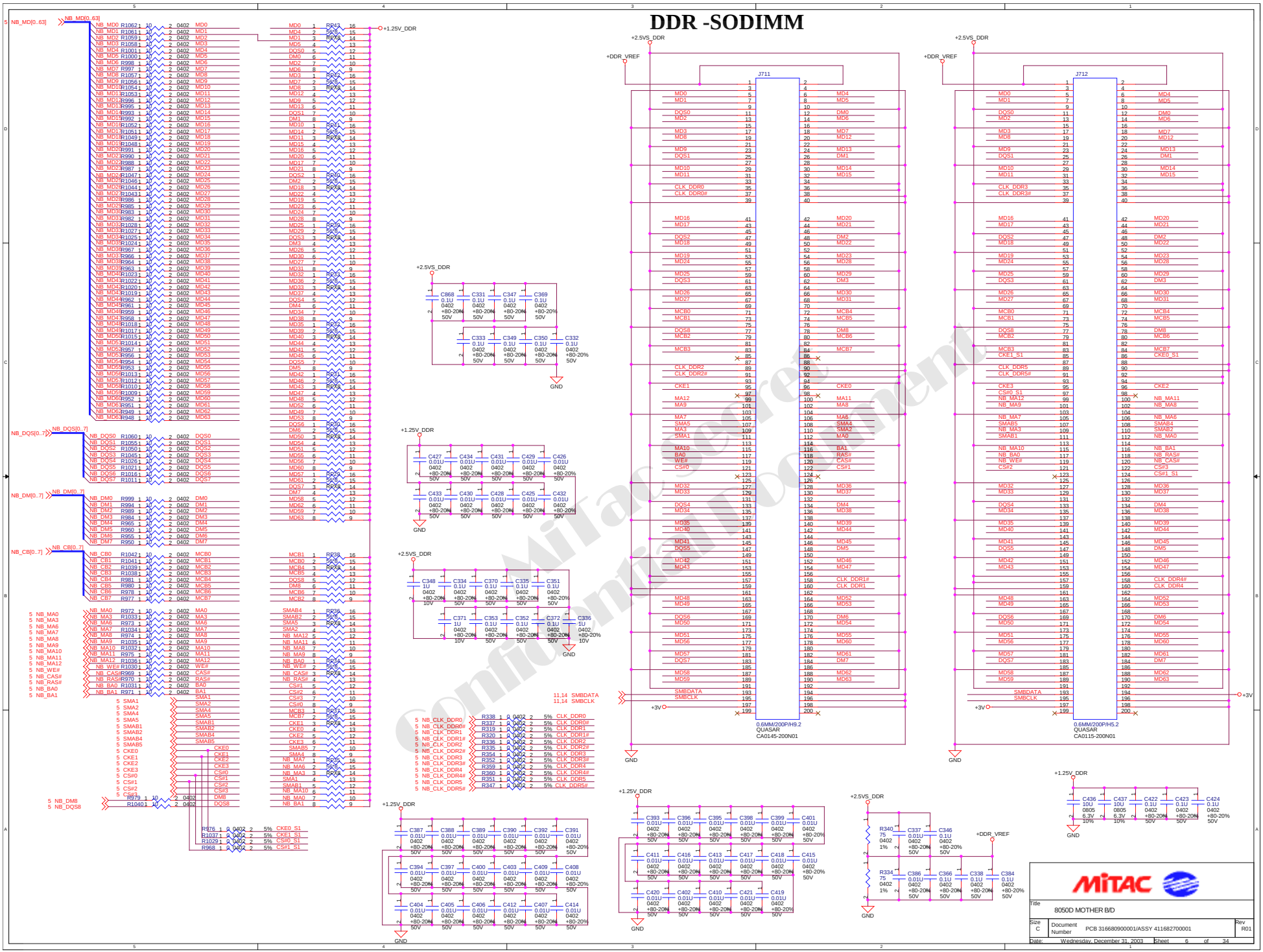
VID 5	4	3	2	1	0	VCC-Core
1	0	0	0	0	0	1.196
1	0	0	0	0	1	1.180
1	0	0	0	1	0	1.164
1	0	0	0	1	1	1.148
1	0	0	1	0	0	1.132
1	0	0	1	0	1	1.116
1	0	0	1	1	0	1.100
1	0	0	1	1	1	1.084
1	0	1	0	0	0	1.068
1	0	1	0	0	1	1.052
1	0	1	0	1	0	1.036
1	0	1	0	1	1	1.020
1	0	1	1	0	0	1.004
1	0	1	1	0	1	0.988
1	0	1	1	1	0	0.972
1	0	1	1	1	1	0.956
1	1	0	0	0	0	0.940
1	1	0	0	0	1	0.924
1	1	0	0	1	0	0.908
1	1	0	0	1	1	0.892
1	1	0	1	0	0	0.876
1	1	0	1	0	1	0.860
1	1	0	1	1	0	0.844
1	1	0	1	1	1	0.828
1	1	1	0	0	0	0.812
1	1	1	0	0	1	0.796
1	1	1	0	1	0	0.780
1	1	1	0	1	1	0.764
1	1	1	1	0	0	0.748
1	1	1	1	0	1	0.732
1	1	1	1	1	0	0.716
1	1	1	1	1	1	0.700

MiTAC
Title: 8050D MOTHER B/D
Size: C | Document Number: PCB 316680900001/ASSY 411682700001 | Rev: R01
Date: Wednesday, December 31, 2003 | Sheet 3 of 34

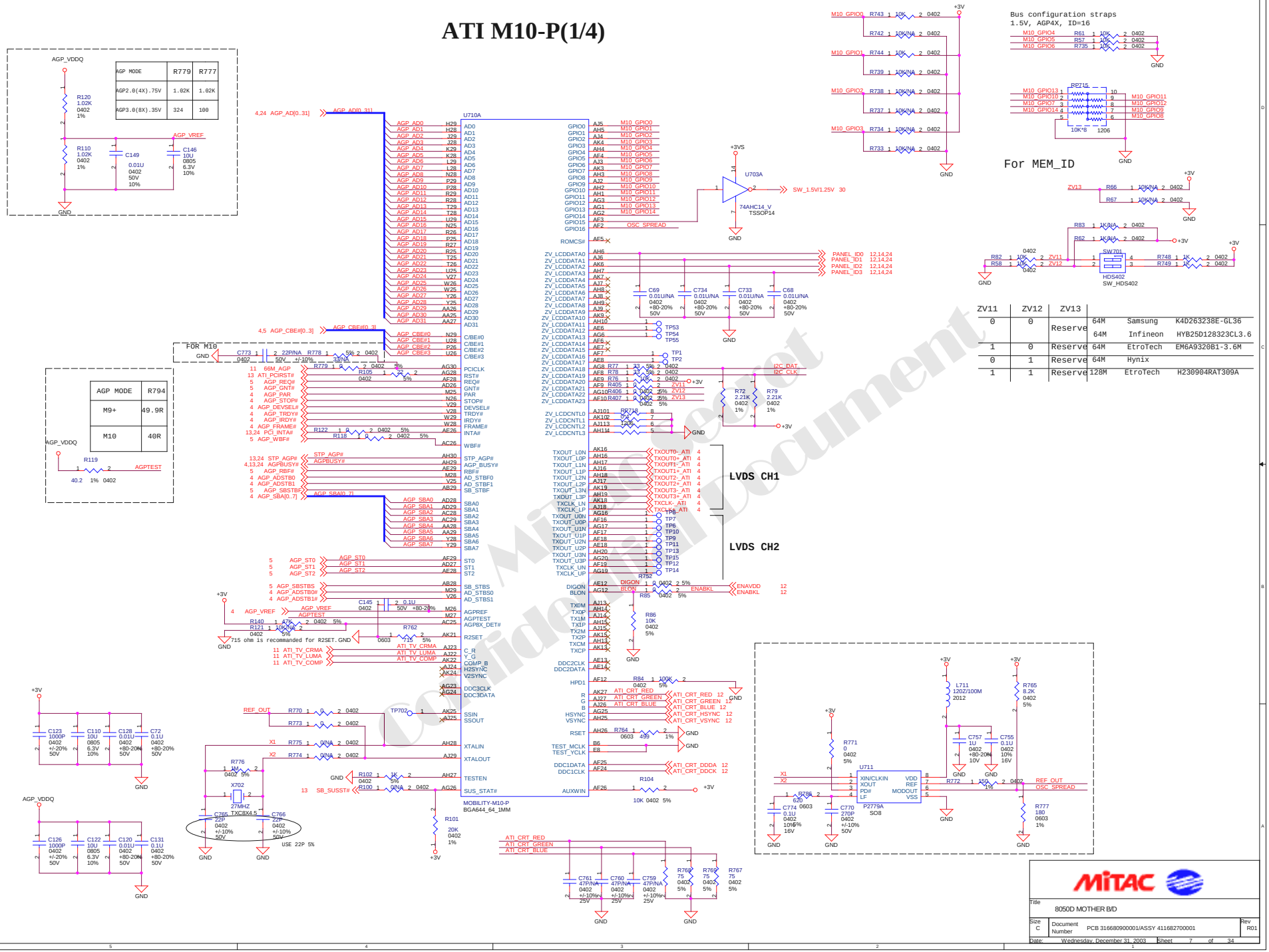


NB_MONTARA-GME(2/2)

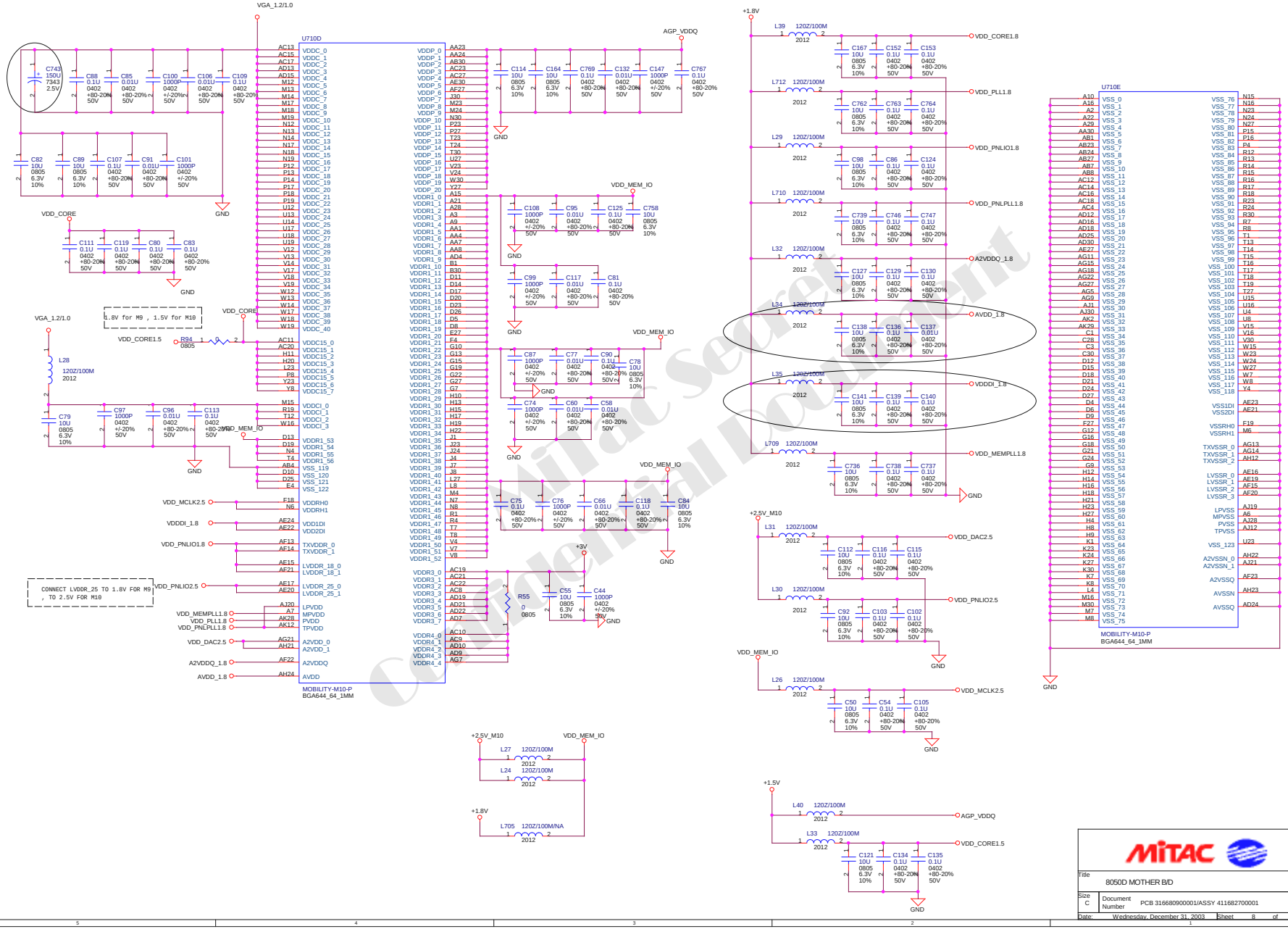




ATI M10-P(1/4)

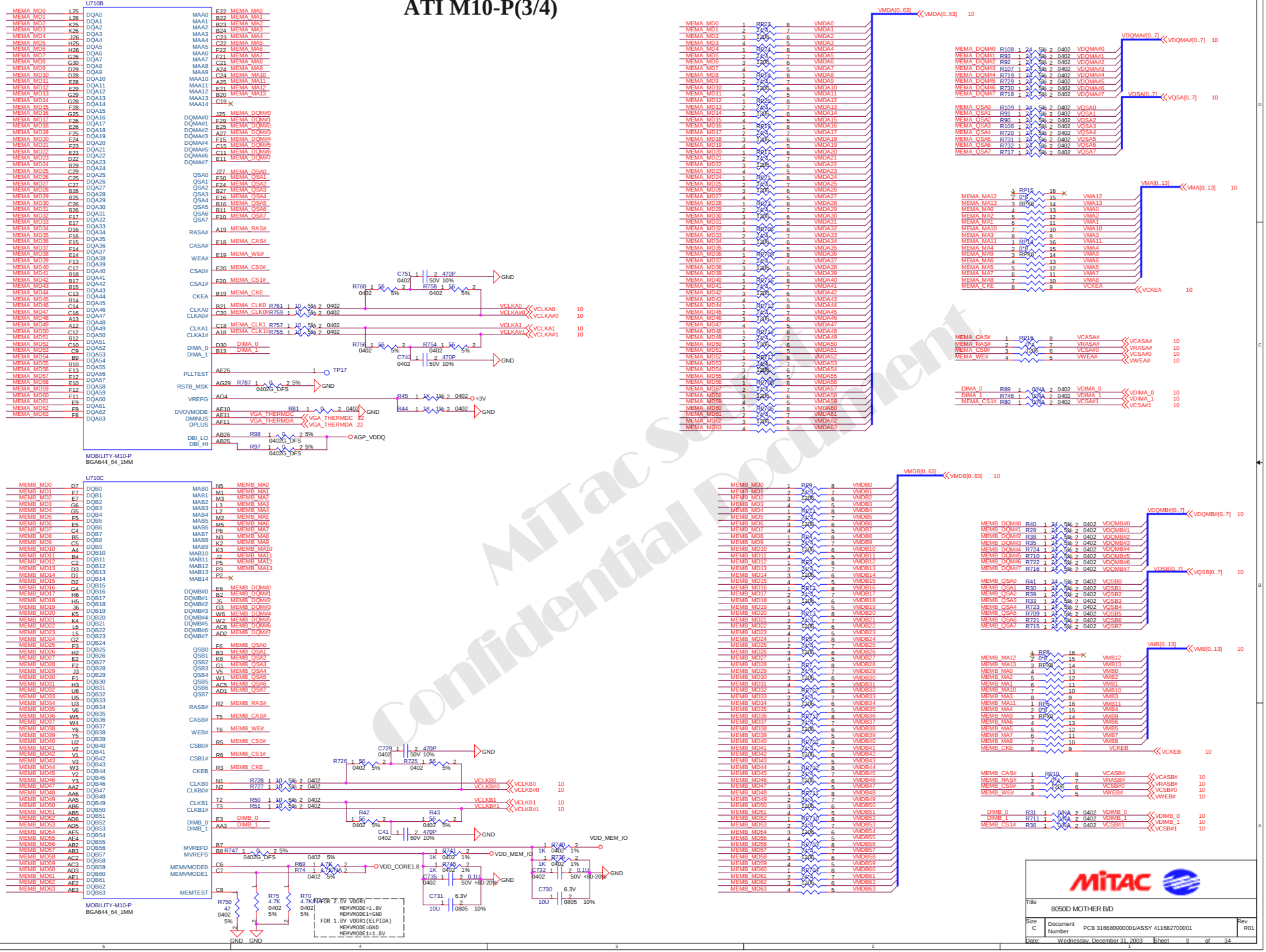


ATI M10-P(2/4)

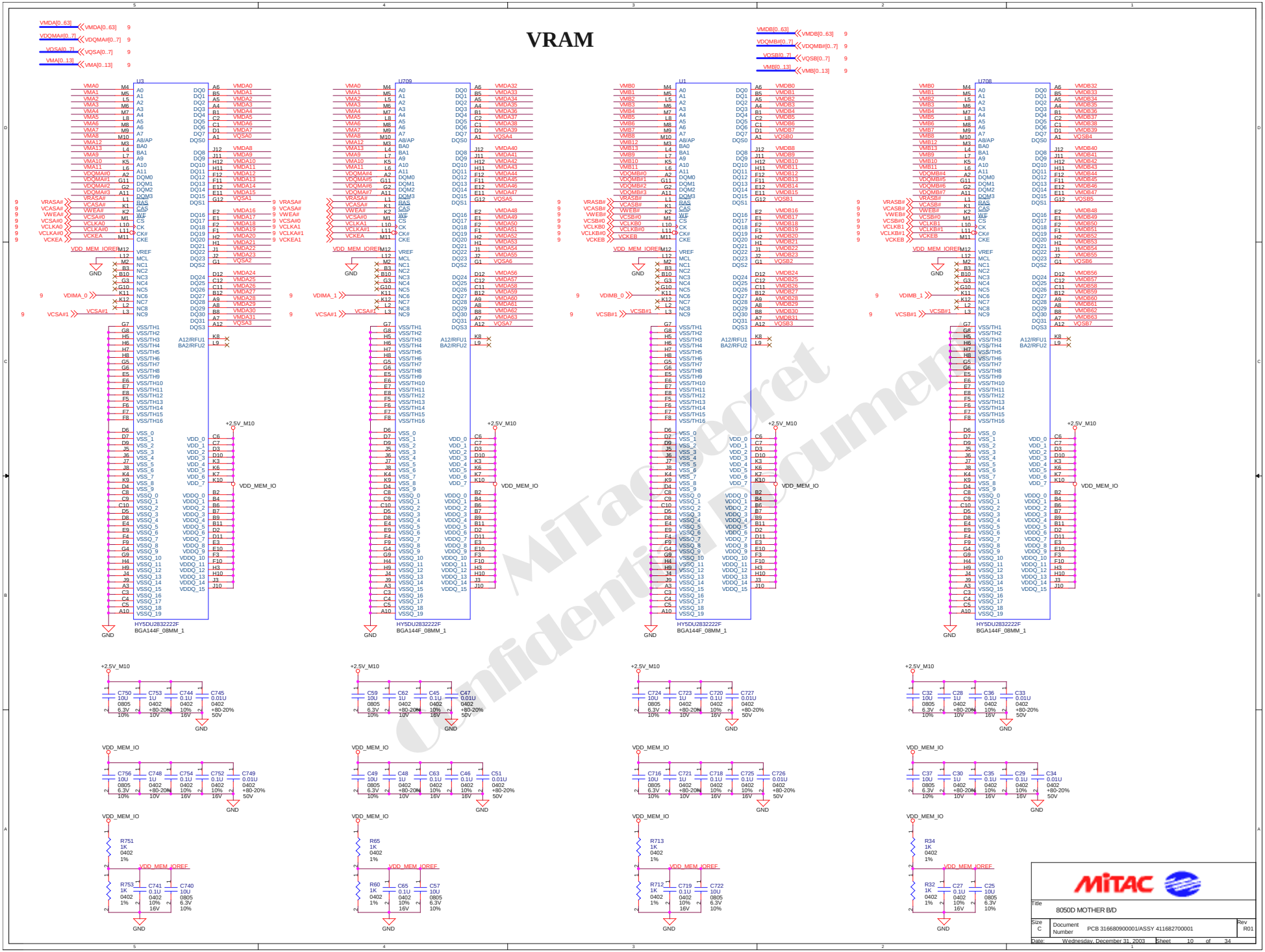


Title	8050D MOTHER B/D	
Size C	Document Number PCB 316680900001/ASSY 411682700001	Rev R01
Date: Wednesday, December 31, 2003	Sheet 8 of 34	

ATI M10-P(3/4)



Title	8050D MOTHER B/D
Size	C
Document Number	PCB 316680900001/ASSY 411682700001
Rev	R01
Date:	Wednesday, December 31, 2003
Sheet	9 of 34



CLOCK SYNTHERIZER

FS2	FS1	FS0	CPU	3V66[5:0]	PCI*
X	0	0	166.66	66.66	33.33
X	0	1	100.00	66.66	33.33
X	1	0	200.00	66.66	33.33
X	1	1	133.33	66.66	33.33
Mid	0	0	Tristate	Tristate	Tristate
Mid	0	1	TCLK/2	TCLK/2	TCLK/2
Mid	1	0	Reserved	Reserved	Reserved
Mid	1	1	Reserved	Reserved	Reserved

001

0:0V
1:3.3V

UNIT: MHz

Layout note: Place crystal within 500 mils of CLK Gen.

WHEN USE INTEGRATE VGA R887/NA

TV ENCODER

WHEN USE INTEGRATE VGA
ADD R763 R766 U2 R1240

MiTAC

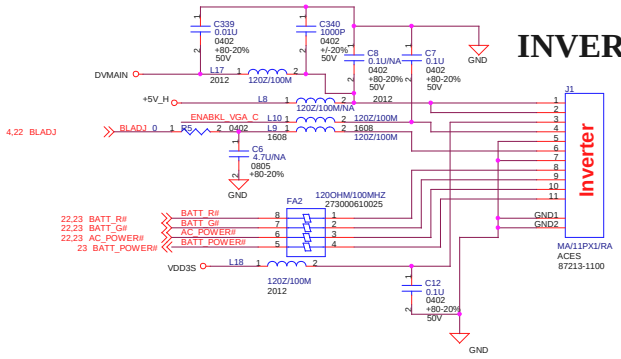
Title: 8050D MOTHER B/D

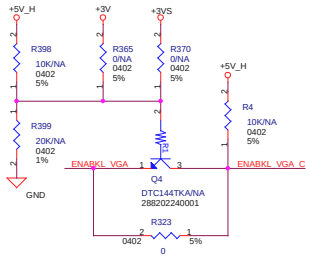
Size: C | Document Number: PCB 316680900001/ASSY 411682700001 | Rev: R01

Date: Wednesday, December 31, 2003 | Sheet 11 of 34

Display (CRT / LCD)

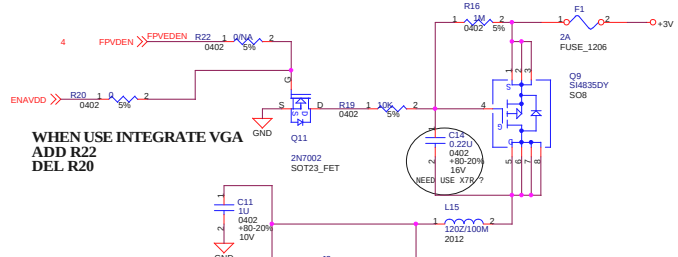
INVERTER



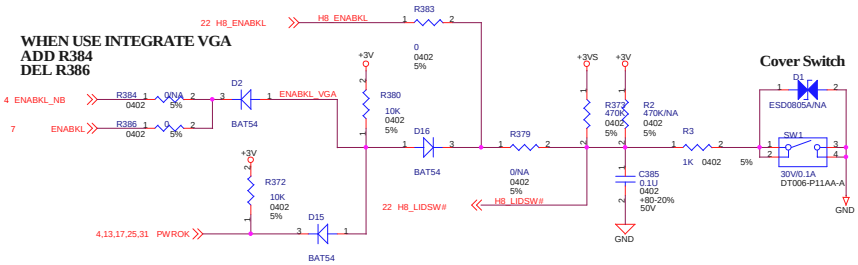


When inverter use +5V ADD Q4,R398,R399,R4 and DEL R323

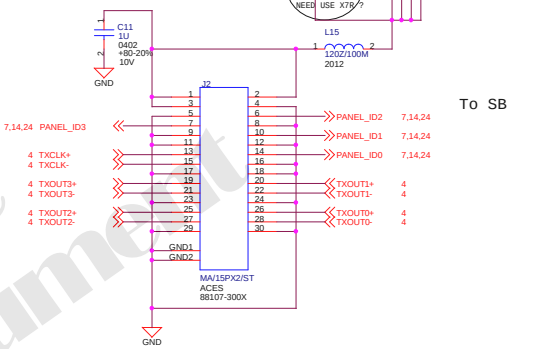
When inverter use +3V ADD R323 and DEL Q4,R398,R399,R4



WHEN USE INTEGRATE VGA
ADD R22
DEL R20



WHEN USE INTEGRATE VGA
ADD R384
DEL R386



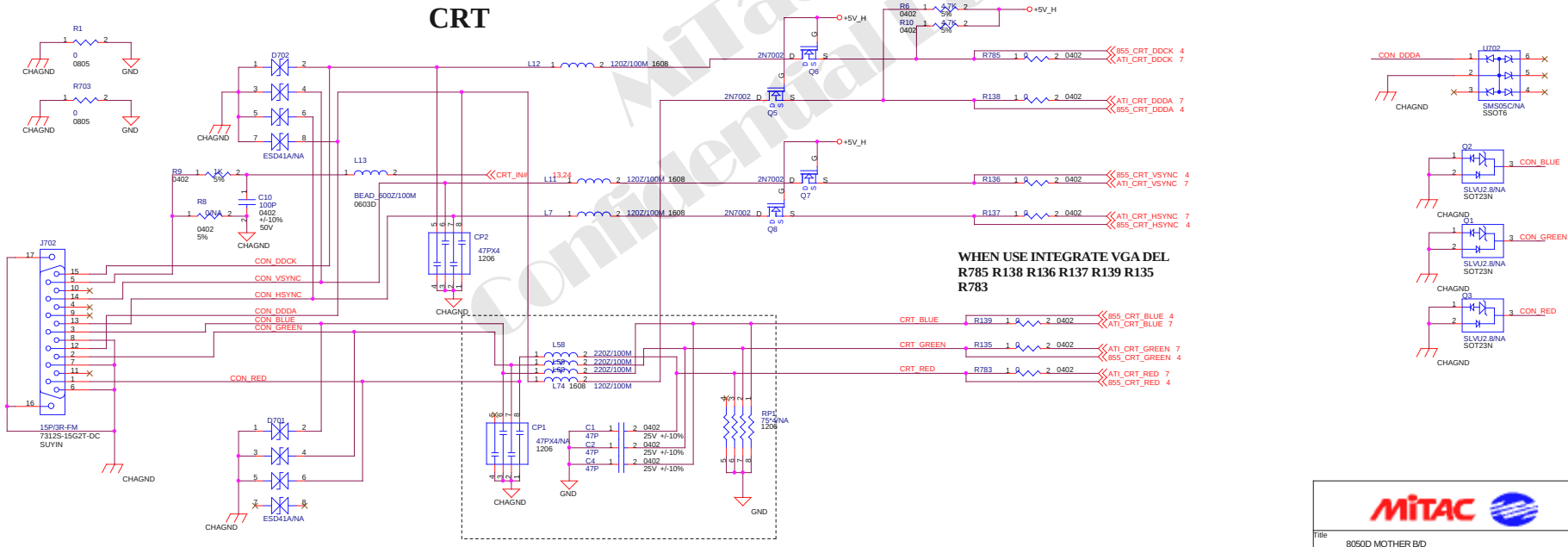
To SB

Pannel ID

LCD_ID0	LCD_ID1	LCD_ID2	PANEL TYPE
0	0	1	
1	0	1	
0	1	1	
0	1	0	
1	1	0	

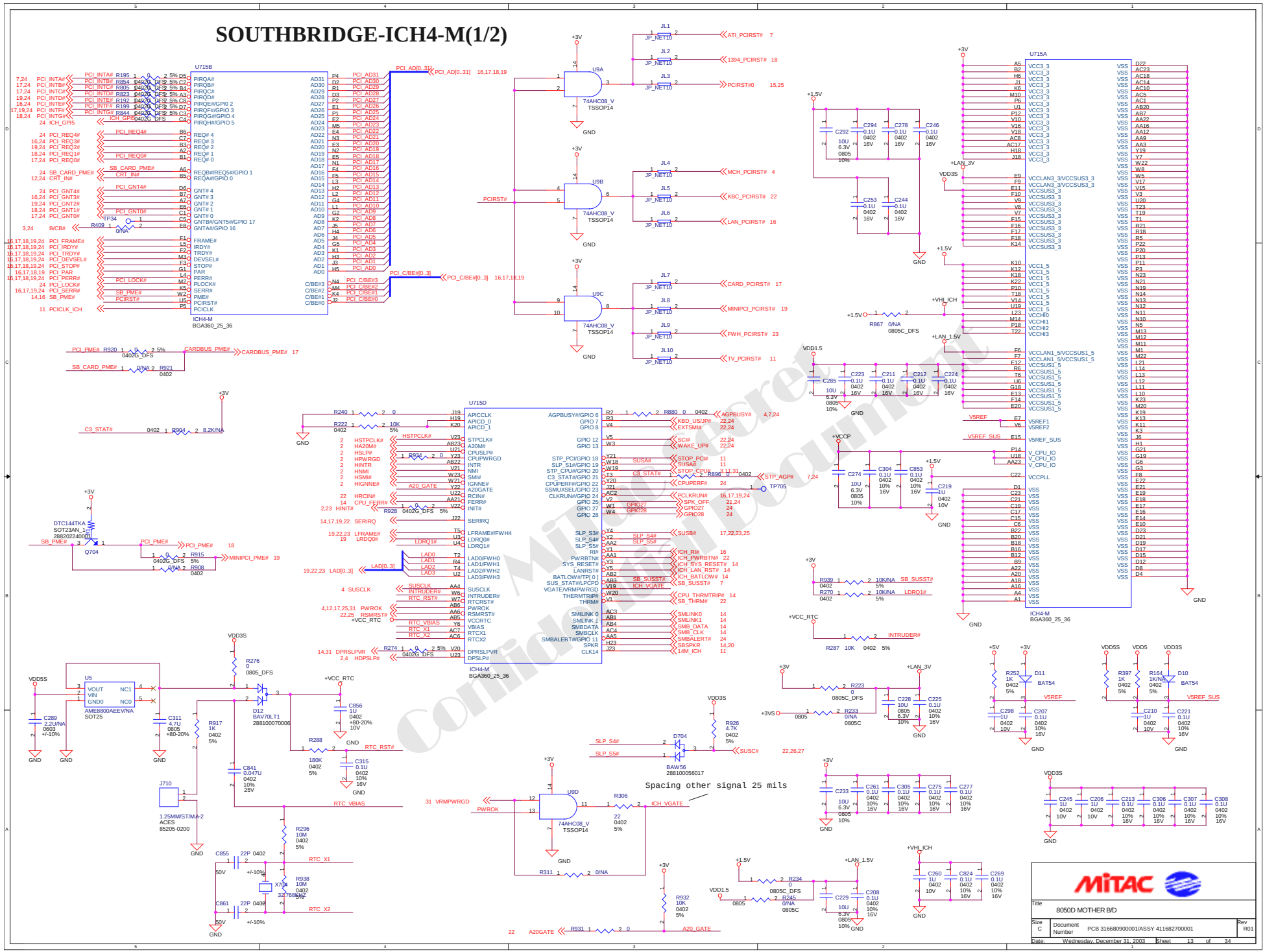
CRT

Check Power Plane is 3VS or 5VS

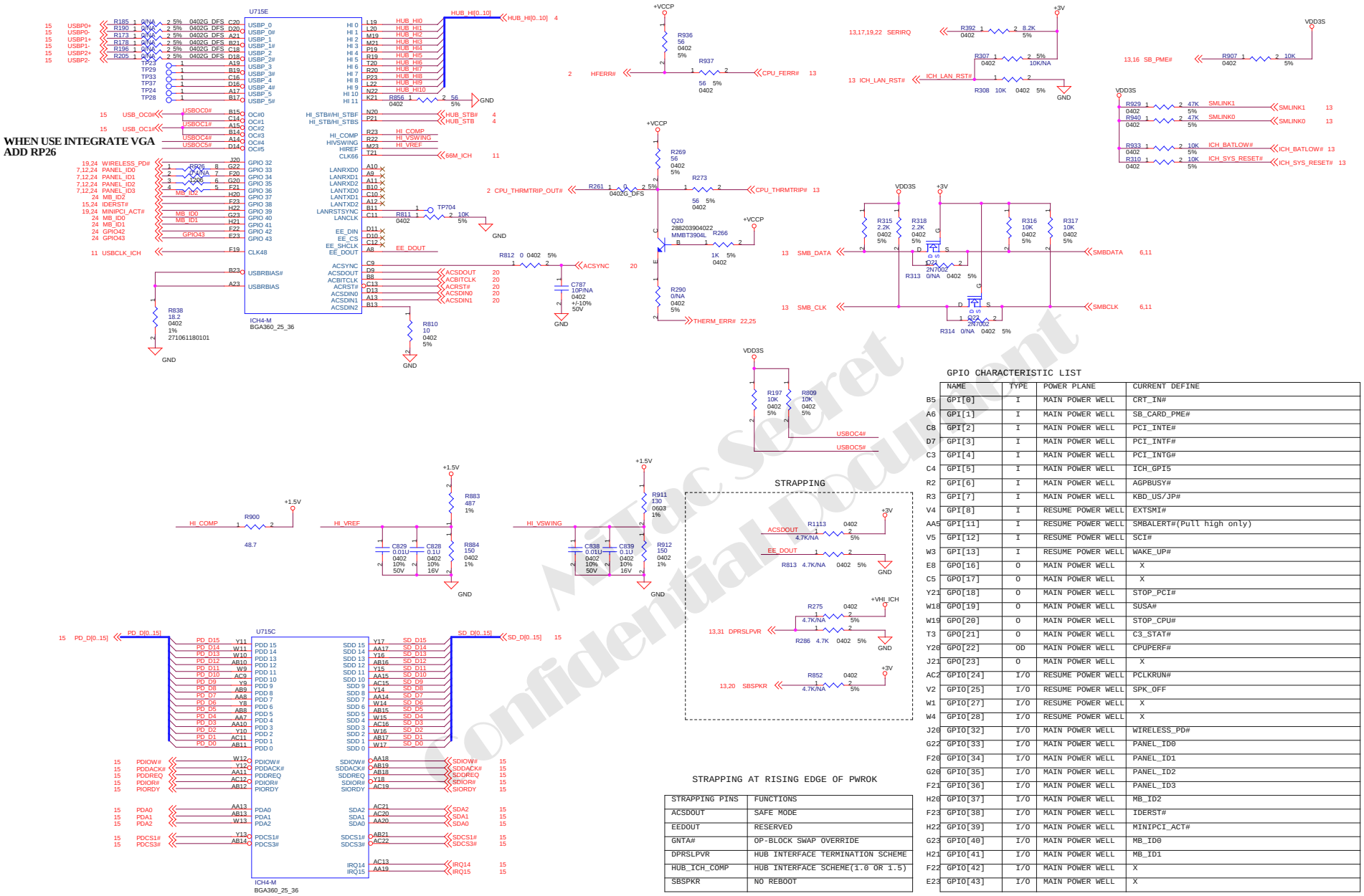


WHEN USE INTEGRATE VGA DEL
R785 R138 R136 R137 R139 R135
R783

Title	8050D MOTHER B/D	
Size C	Document Number PCB 316680900001/ASSY 411682700001	Rev R01
Date: Wednesday, December 31, 2003	Sheet 12 of 34	



SOUTHBRIDGE-ICH4-M(2/2)



GPIO CHARACTERISTIC LIST

	NAME	TYPE	POWER PLANE	CURRENT DEFINE
B5	GPI[0]	I	MAIN POWER WELL	CRT_IN#
A6	GPI[1]	I	MAIN POWER WELL	SB_CARD_PME#
C8	GPI[2]	I	MAIN POWER WELL	PCI_INTE#
D7	GPI[3]	I	MAIN POWER WELL	PCI_INTF#
C3	GPI[4]	I	MAIN POWER WELL	PCI_INTG#
C4	GPI[5]	I	MAIN POWER WELL	ICH_GPI5
R2	GPI[6]	I	MAIN POWER WELL	AGPBUSY#
R3	GPI[7]	I	MAIN POWER WELL	KBD_US/JP#
V4	GPI[8]	I	RESUME POWER WELL	EXTSMI#
AA5	GPI[11]	I	RESUME POWER WELL	SMBALERT#(Pull high only)
V5	GPI[12]	I	RESUME POWER WELL	SCI#
W3	GPI[13]	I	RESUME POWER WELL	WAKE_UP#
E8	GPO[16]	O	MAIN POWER WELL	X
C5	GPO[17]	O	MAIN POWER WELL	X
Y21	GPO[18]	O	MAIN POWER WELL	STOP_PCI#
W18	GPO[19]	O	MAIN POWER WELL	SUSA#
W19	GPO[20]	O	MAIN POWER WELL	STOP_CPU#
T3	GPO[21]	O	MAIN POWER WELL	C3_STAT#
Y20	GPO[22]	OD	MAIN POWER WELL	CPUPERF#
J21	GPO[23]	O	MAIN POWER WELL	X
AC2	GPIO[24]	I/O	RESUME POWER WELL	PCLKRUN#
V2	GPIO[25]	I/O	RESUME POWER WELL	SPK_OFF
W1	GPIO[27]	I/O	RESUME POWER WELL	X
W4	GPIO[28]	I/O	RESUME POWER WELL	X
J20	GPIO[32]	I/O	MAIN POWER WELL	WIRELESS_PD#
G22	GPIO[33]	I/O	MAIN POWER WELL	PANEL_ID0
F20	GPIO[34]	I/O	MAIN POWER WELL	PANEL_ID1
G20	GPIO[35]	I/O	MAIN POWER WELL	PANEL_ID2
F21	GPIO[36]	I/O	MAIN POWER WELL	PANEL_ID3
H20	GPIO[37]	I/O	MAIN POWER WELL	MB_ID2
F23	GPIO[38]	I/O	MAIN POWER WELL	IDERST#
H22	GPIO[39]	I/O	MAIN POWER WELL	MINIPCI_ACT#
G23	GPIO[40]	I/O	MAIN POWER WELL	MB_ID0
H21	GPIO[41]	I/O	MAIN POWER WELL	MB_ID1
F22	GPIO[42]	I/O	MAIN POWER WELL	X
E23	GPIO[43]	I/O	MAIN POWER WELL	X

STRAPPING AT RISING EDGE OF PWROK

STRAPPING PINS	FUNCTIONS
ACSDOUT	SAFE MODE
EEDOUT	RESERVED
GNTA#	OP-BLOCK SWAP OVERRIDE
DPRSLPVR	HUB INTERFACE TERMINATION SCHEME
HUB_ICH_COMP	HUB INTERFACE SCHEME(1.0 OR 1.5)
SBSPKR	NO REBOOT

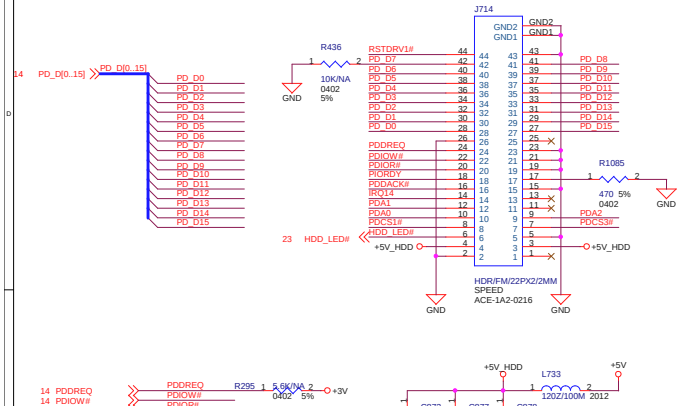
MiTAC

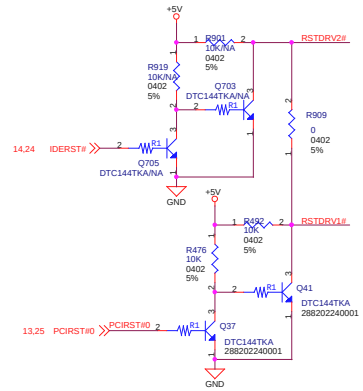
Title: 8050D MOTHER B/D

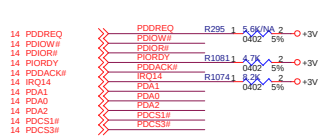
Size: C | Document Number: PCB 316680900001/ASSY 411682700001 | Rev: R01

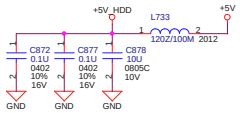
Date: Wednesday, December 31, 2003 | Sheet 14 of 34

HDD- PRIMARY IDE CONNECTOR

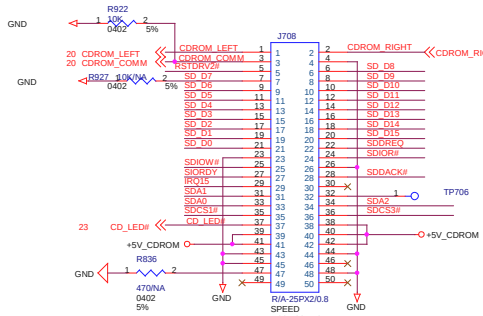


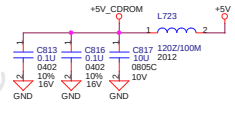




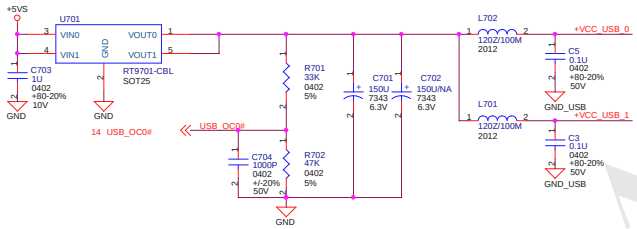


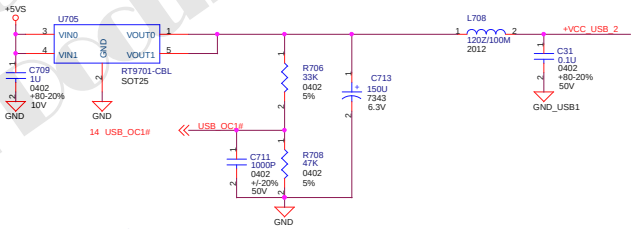
CDROM- SECONDARY IDE CONNECTOR

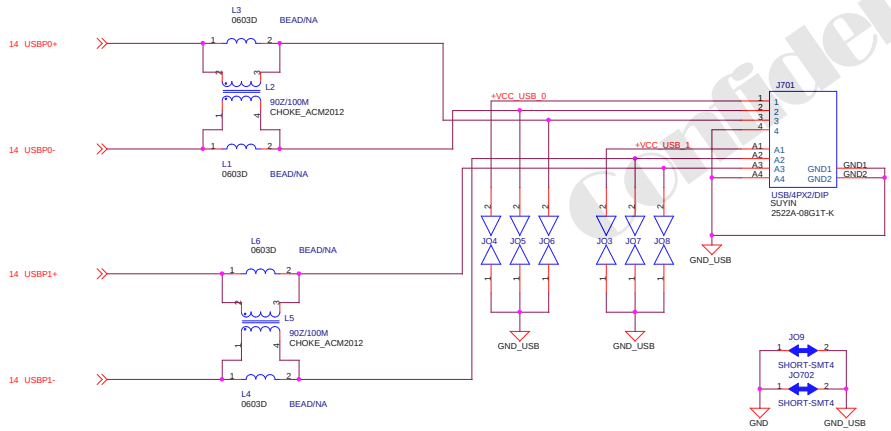


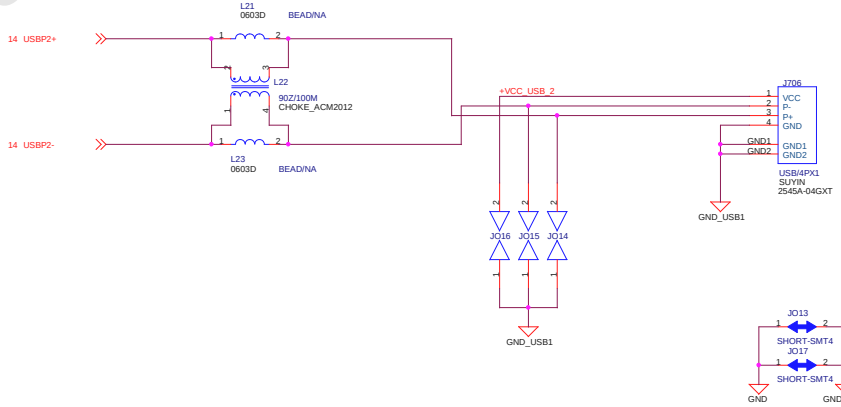


USB CONNECOTR





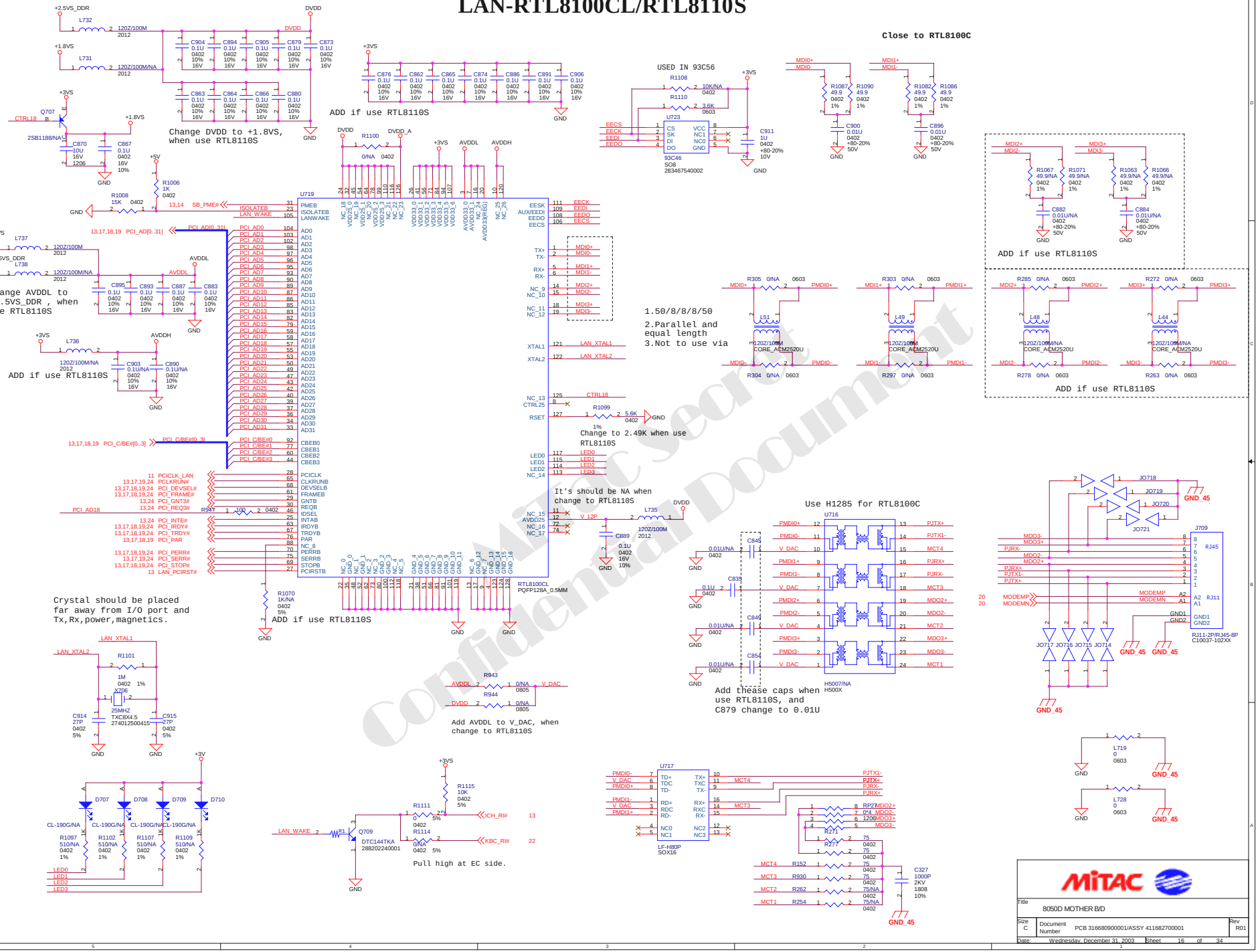


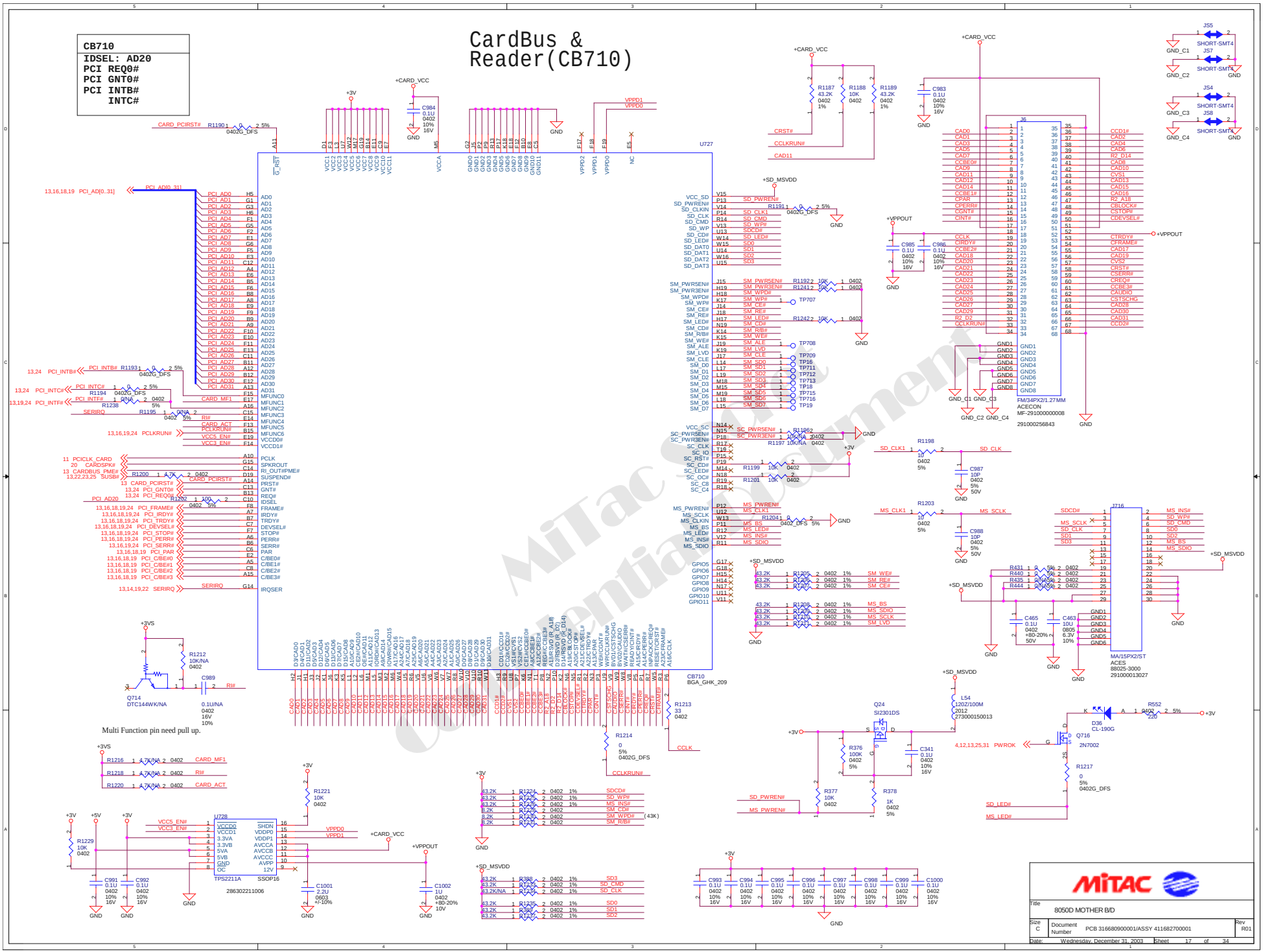


MiTAC

Title	8050D MOTHER B/D	
Size C	Document Number PCB 316680900001/ASSY 411682700001	Rev R01
Date: Wednesday, December 31, 2003	Sheet 15 of 34	

LAN-RTL8100CL/RTL8110S



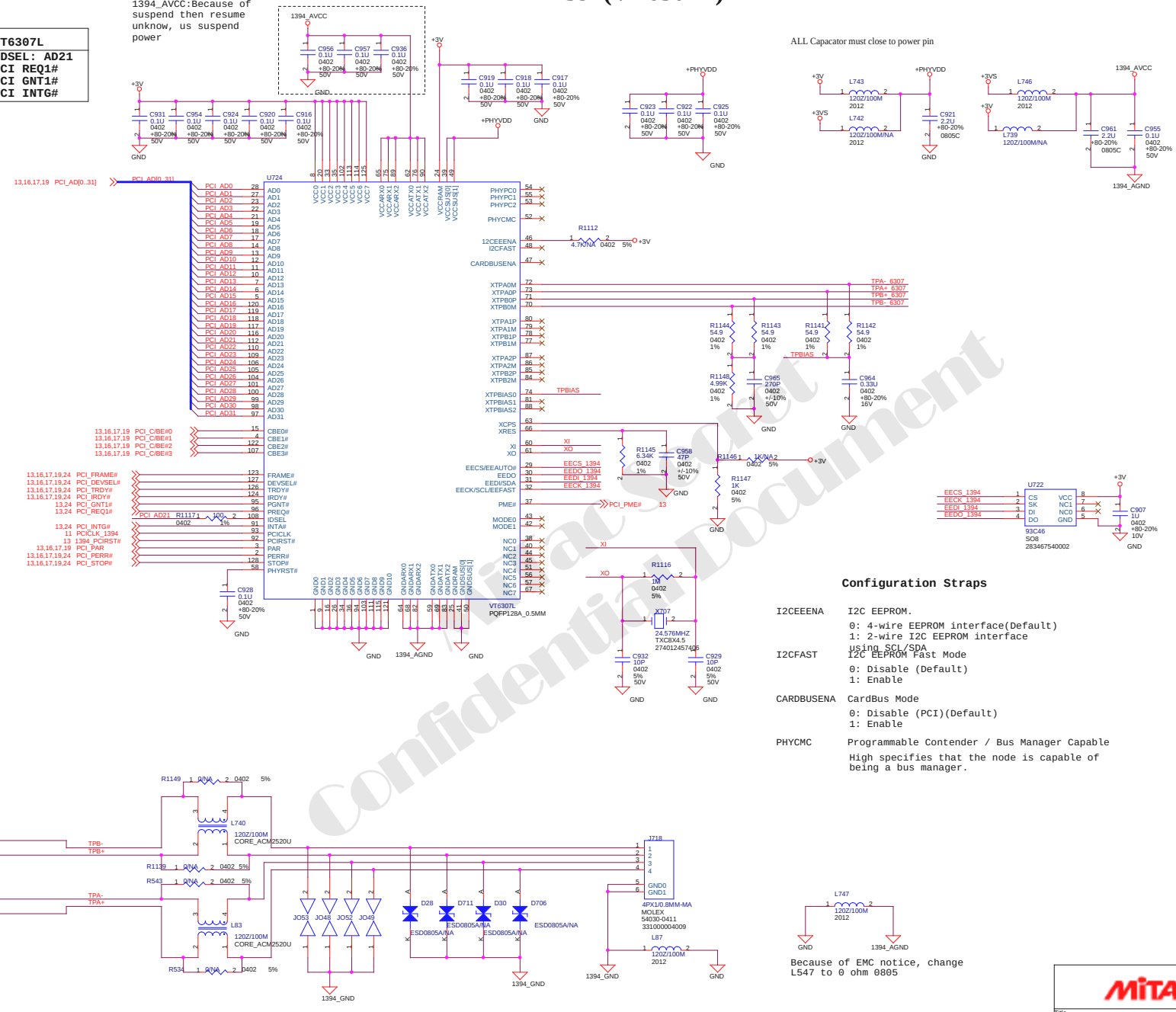


IEEE1394(VT6307L)

VT6307L
IDSEL: AD21
PCI REQ1#
PCI GNT1#
PCI INTG#

1394_AVCC:Because of suspend then resume unknow, us suspend power

ALL Capacator must close to power pin



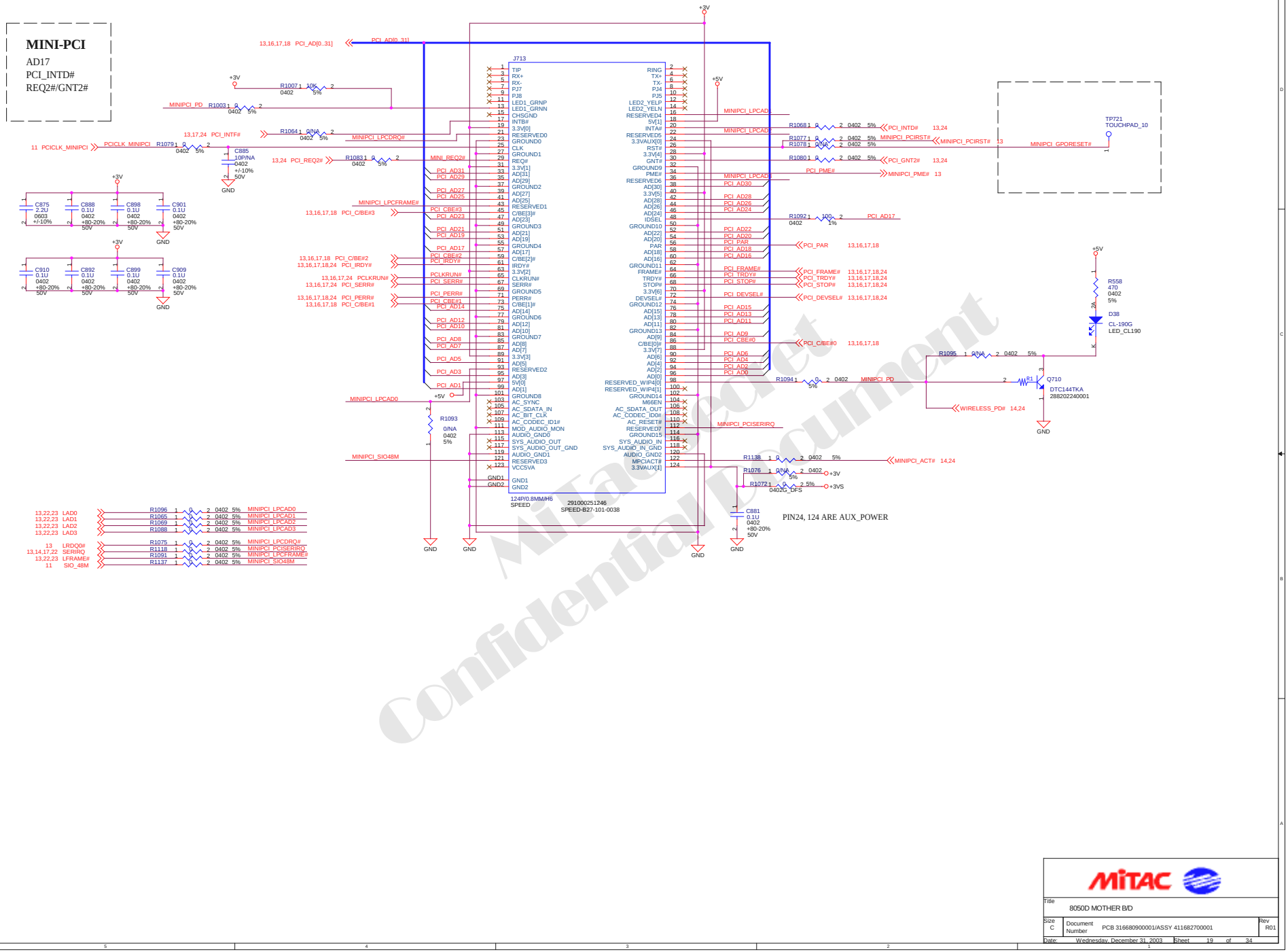
Configuration Straps

I2CEEENA	I2C EEPROM. 0: 4-wire EEPROM interface(Default) 1: 2-wire I2C EEPROM interface using SCL/SDA
I2CFAST	I2C EEPROM Fast Mode 0: Disable (Default) 1: Enable
CARDBUSENA	CardBus Mode 0: Disable (PCI)(Default) 1: Enable
PHYCMC	Programmable Contender / Bus Manager Capable High specifies that the node is capable of being a bus manager.

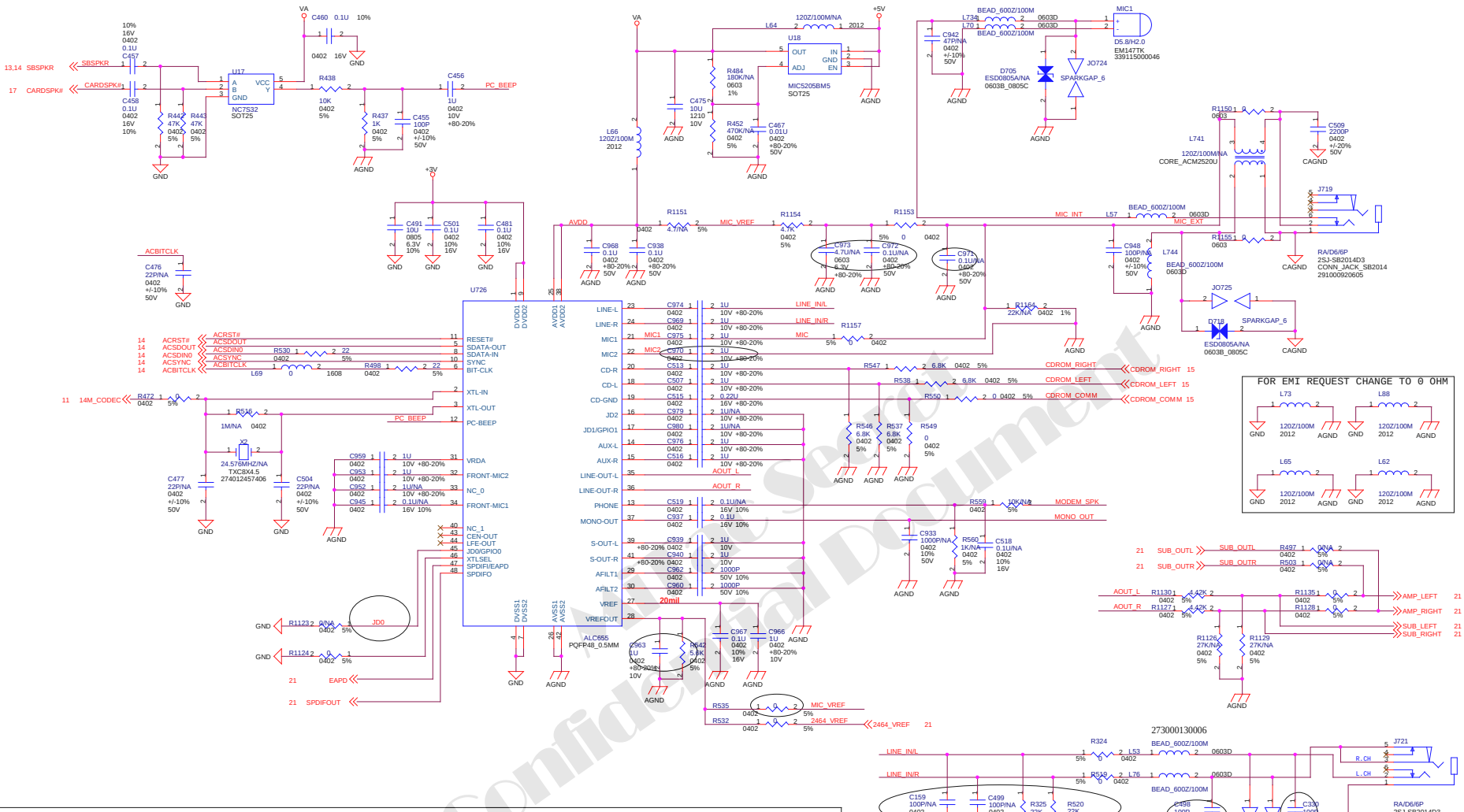
Because of EMC notice, change L547 to 0 ohm 0805

Title	8050D MOTHER B/D
Size	C
Document Number	PCB 316680900001/ASSY 411682700001
Rev	R01
Date:	Wednesday, December 31, 2003
Sheet	18 of 34

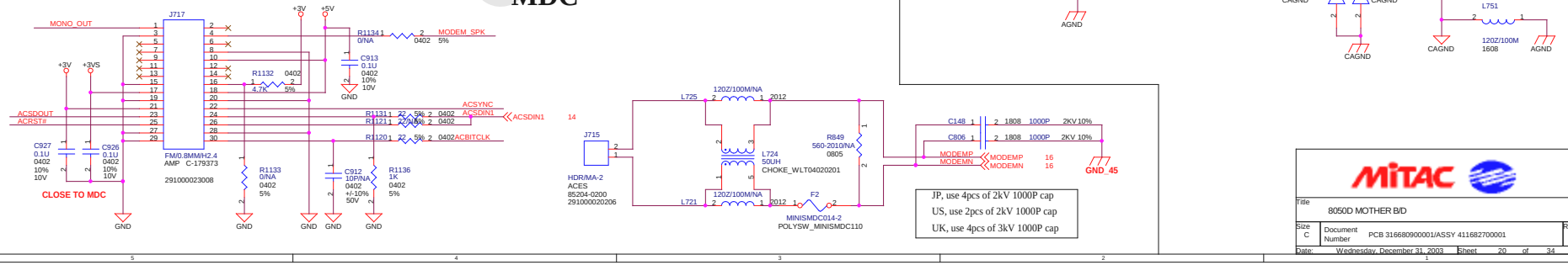
MINI-PCI FROM LYNX-AMD



AUDIO CODEC(ALC655)



MDC



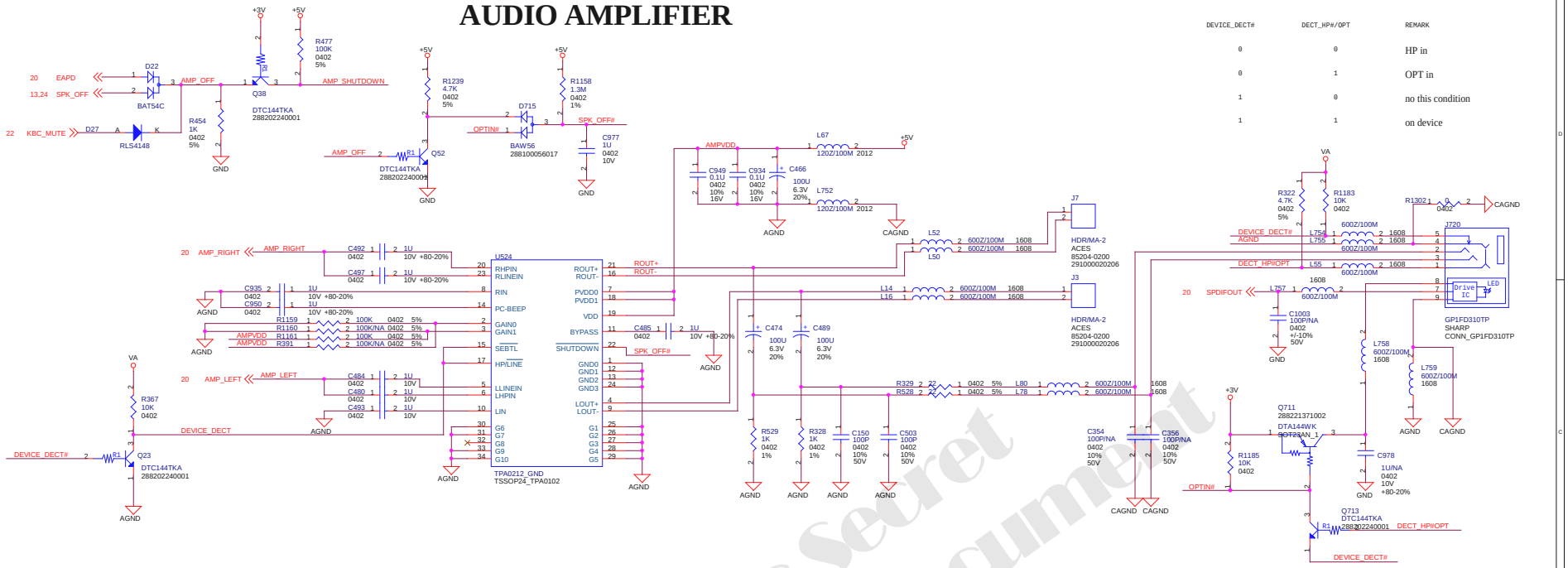
MiTAC

Title: 8050D MOTHER B/D

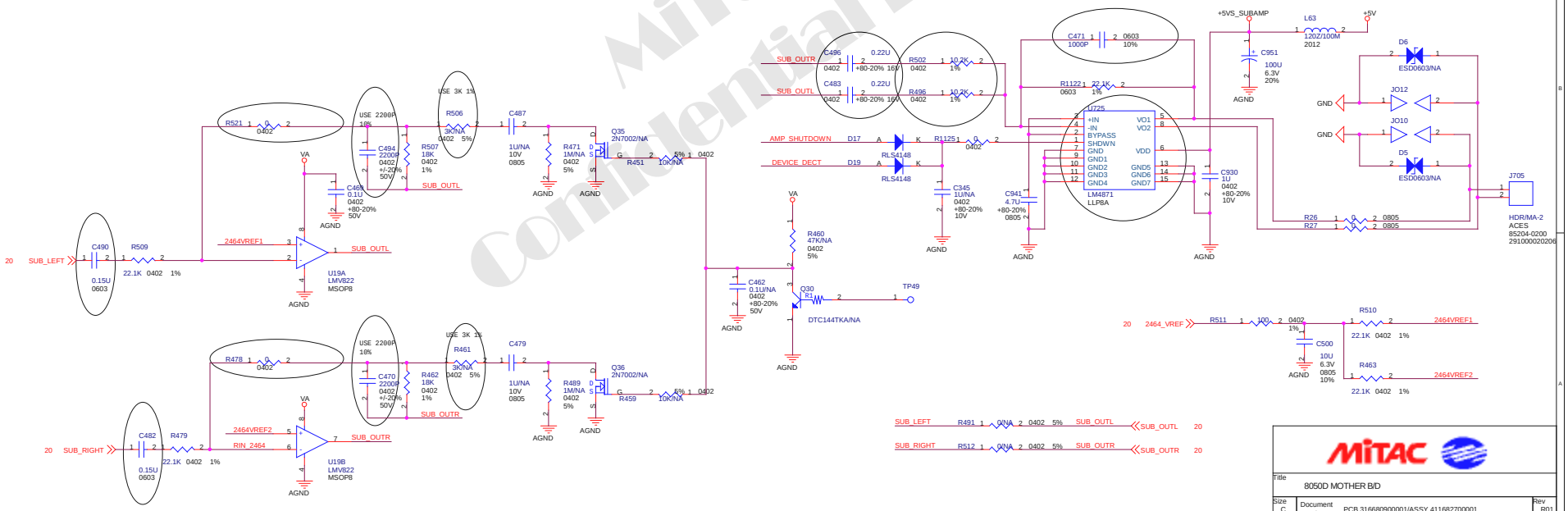
Size: C | Document Number: PCB 316680900001/ASSY 411682700001 | Rev: R01

Date: Wednesday, December 31, 2003 | Sheet 20 of 34

AUDIO AMPLIFIER



SUBWOOFER AMP(LM4871)

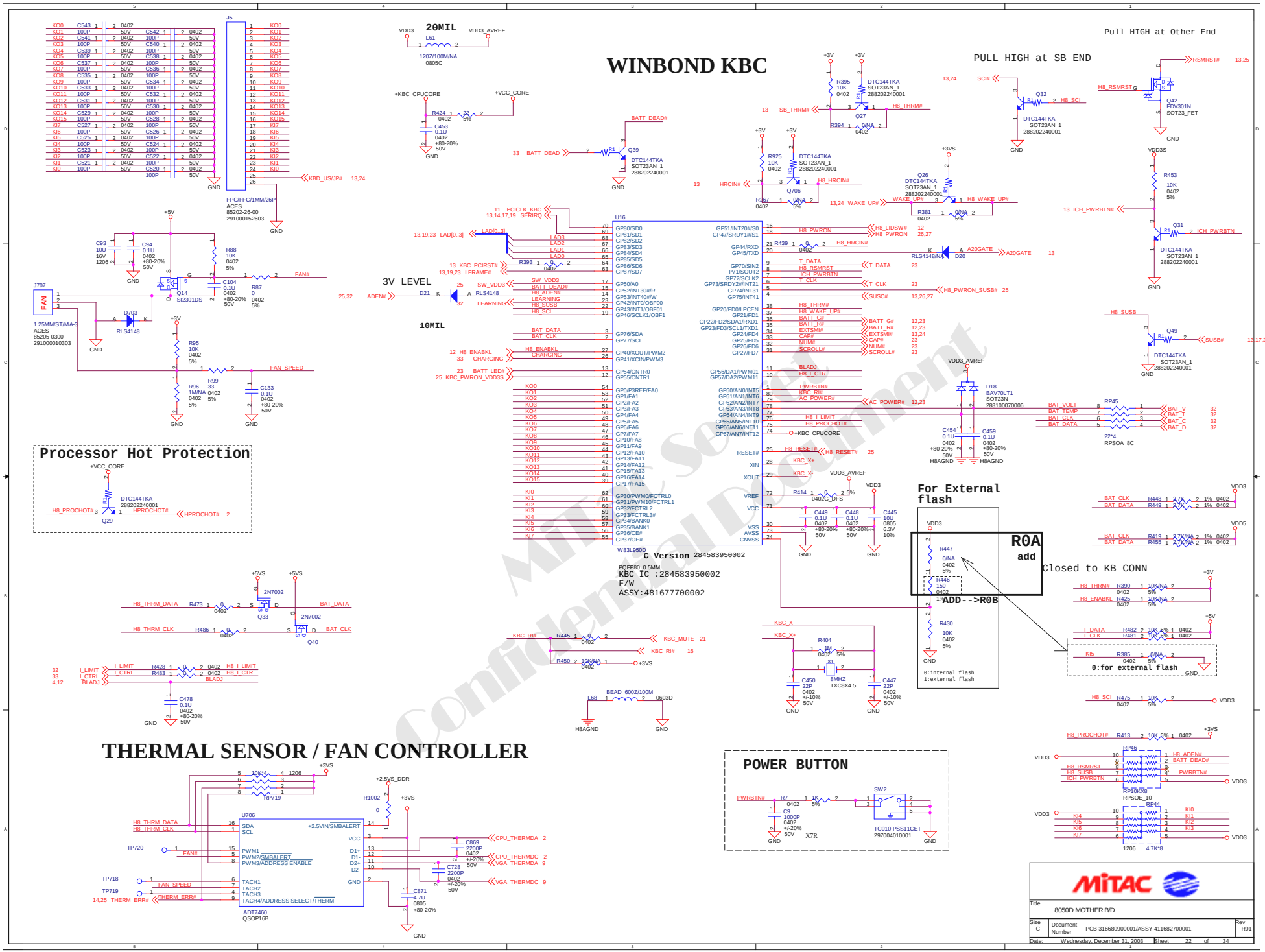


MiTAC

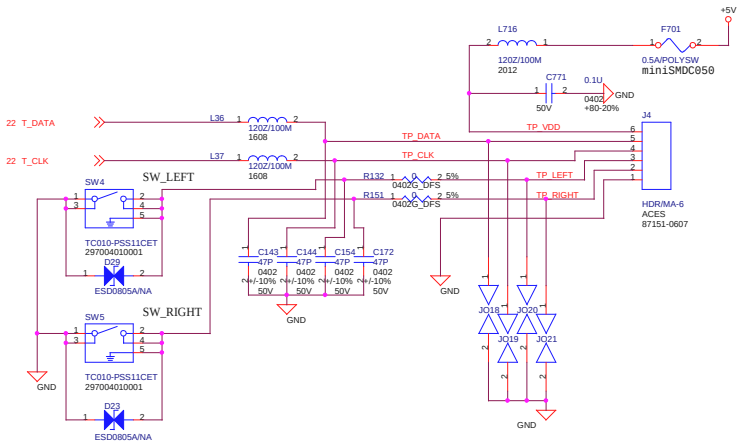
Title: 8050D MOTHER B/D

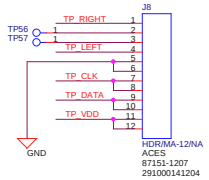
Size	Document Number	Rev
C	PCB 316680900001/ASSY 411682700001	R01

Date: Wednesday, December 31, 2003 Sheet 21 of 34



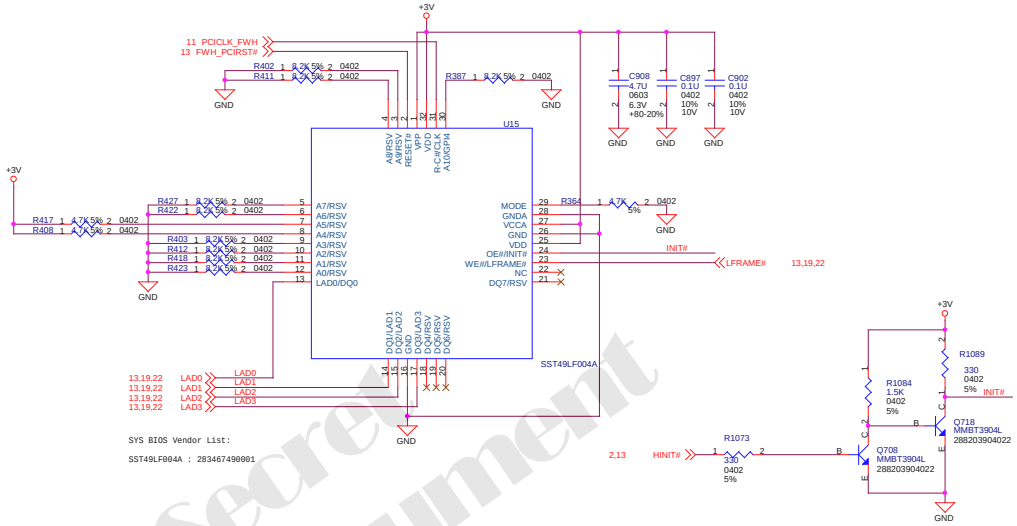
TOUCH_PAD



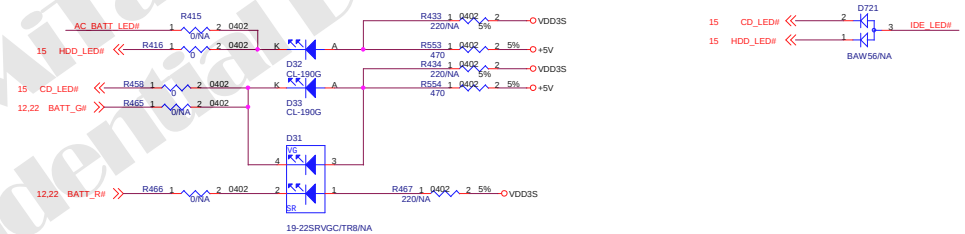


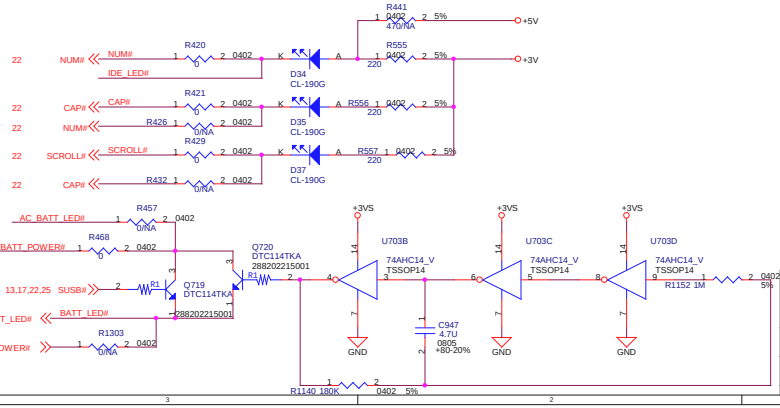
When 8050N ADD J722 and DEL J4
When 8050 ADD J4 and DEL J722

FWH



LED

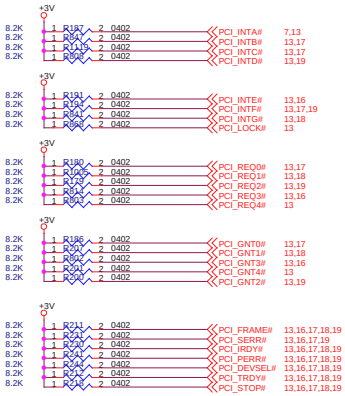




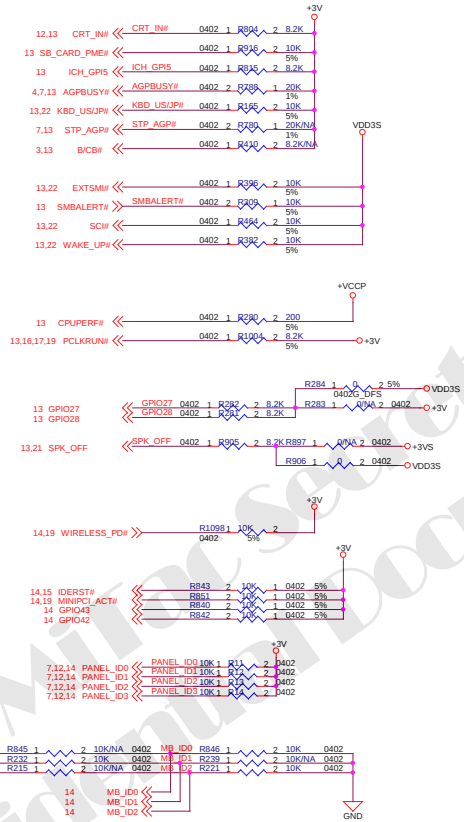
Title	8050D MOTHER B/D		
Size C	Document Number	PCB 316680900001/ASSY 411682700001	Rev R01
Date:	Wednesday, December 31, 2003	Sheet 23 of 34	

PULL -HIGH

PCI PULL HIGH

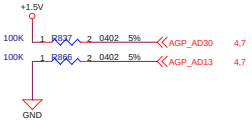


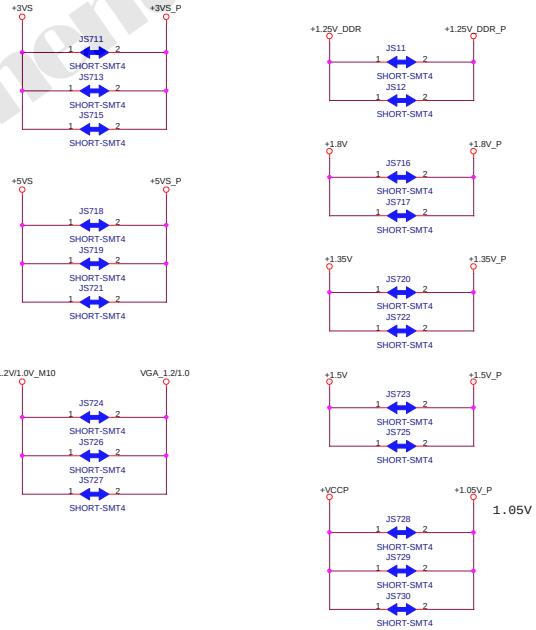
GPIO PULL HIGH



AGP PULL HIGH

WHEN USE INTEGRATE VGA DEL ALL RESISTOR

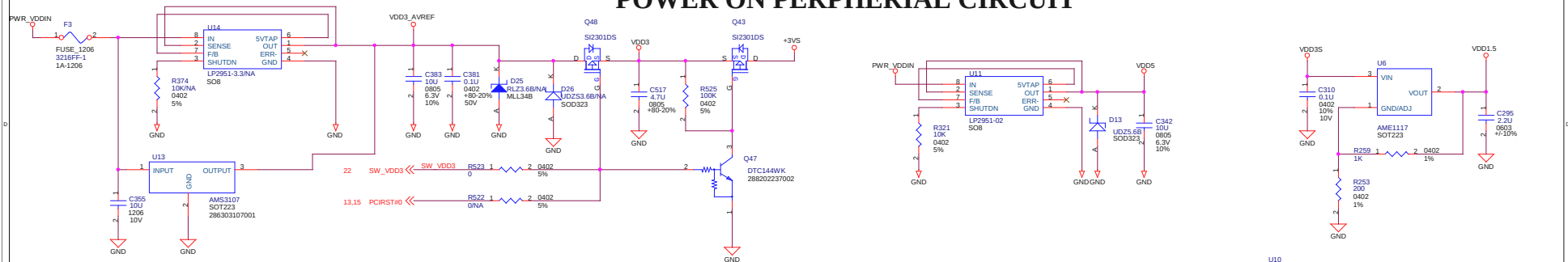




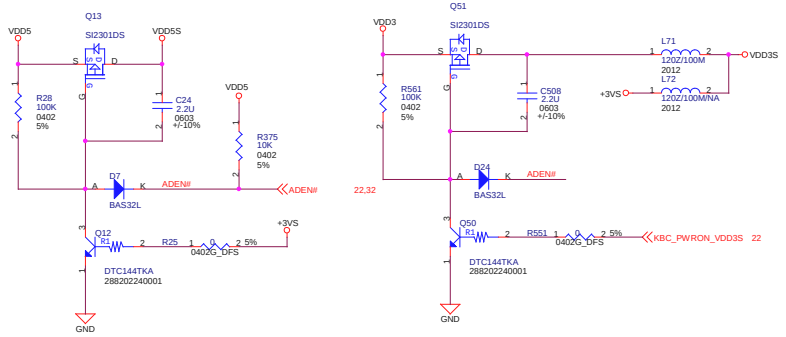
MiTAC

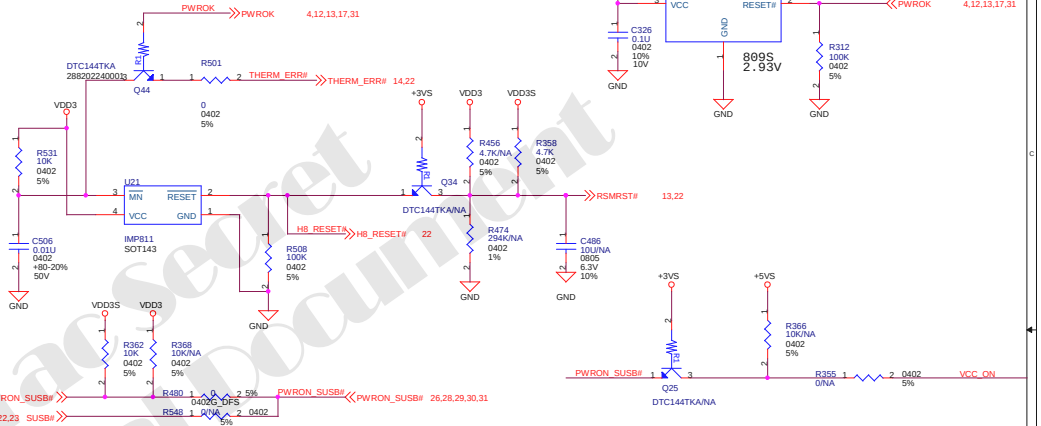
Title	8050D MOTHER B/D	
Size C	Document Number PCB 316680900001/ASSY 411682700001	Rev R01
Date: Wednesday, December 31, 2003	Sheet 24 of 34	

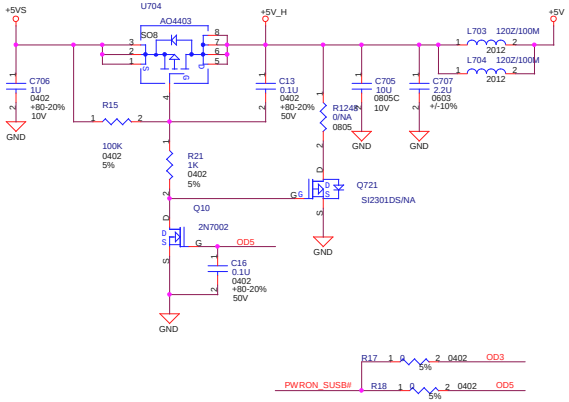
POWER ON PERPHERIAL CIRCUIT

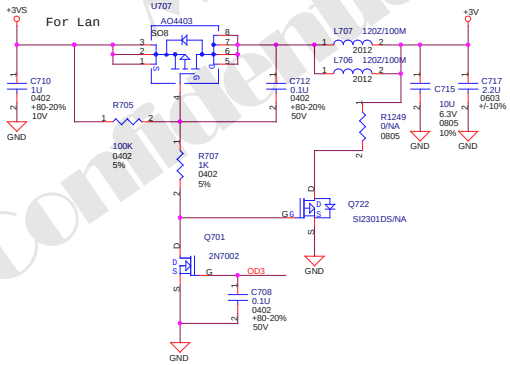


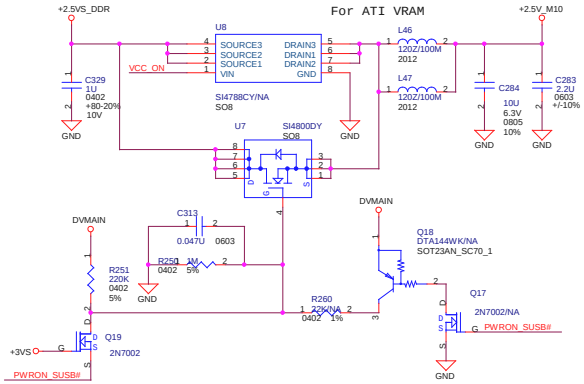
H8 RESET# / RSMRST#







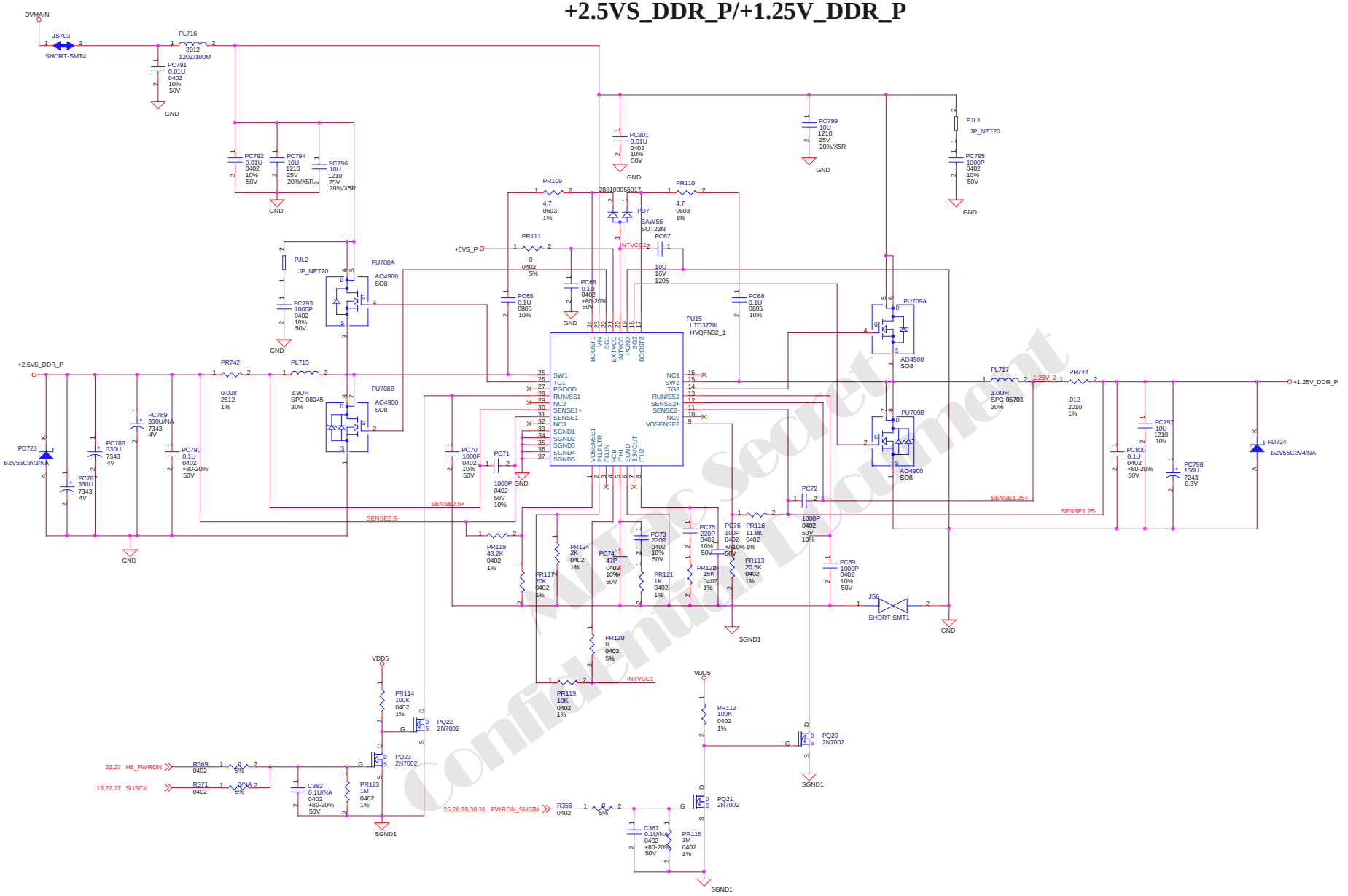


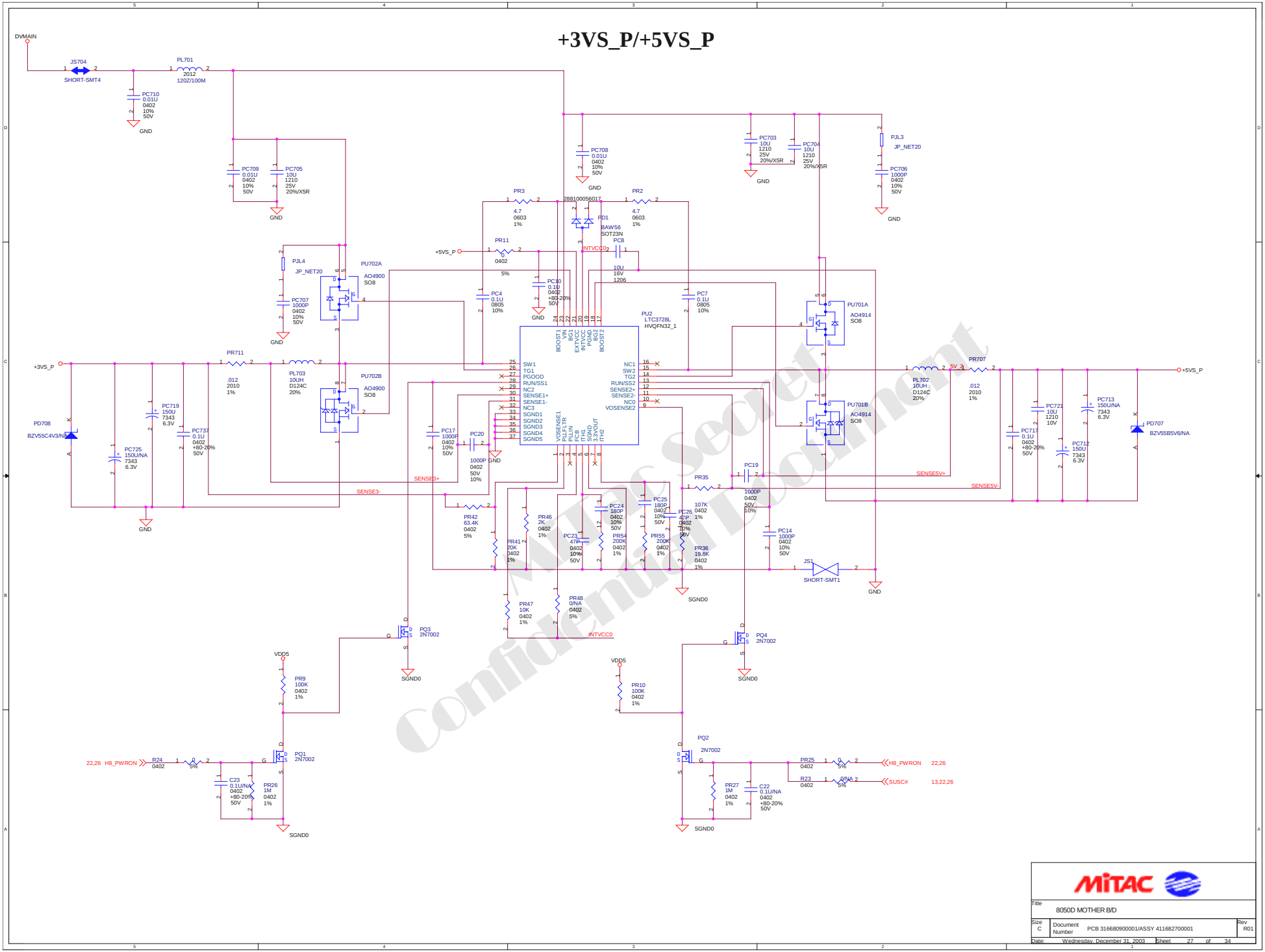


MiTAC

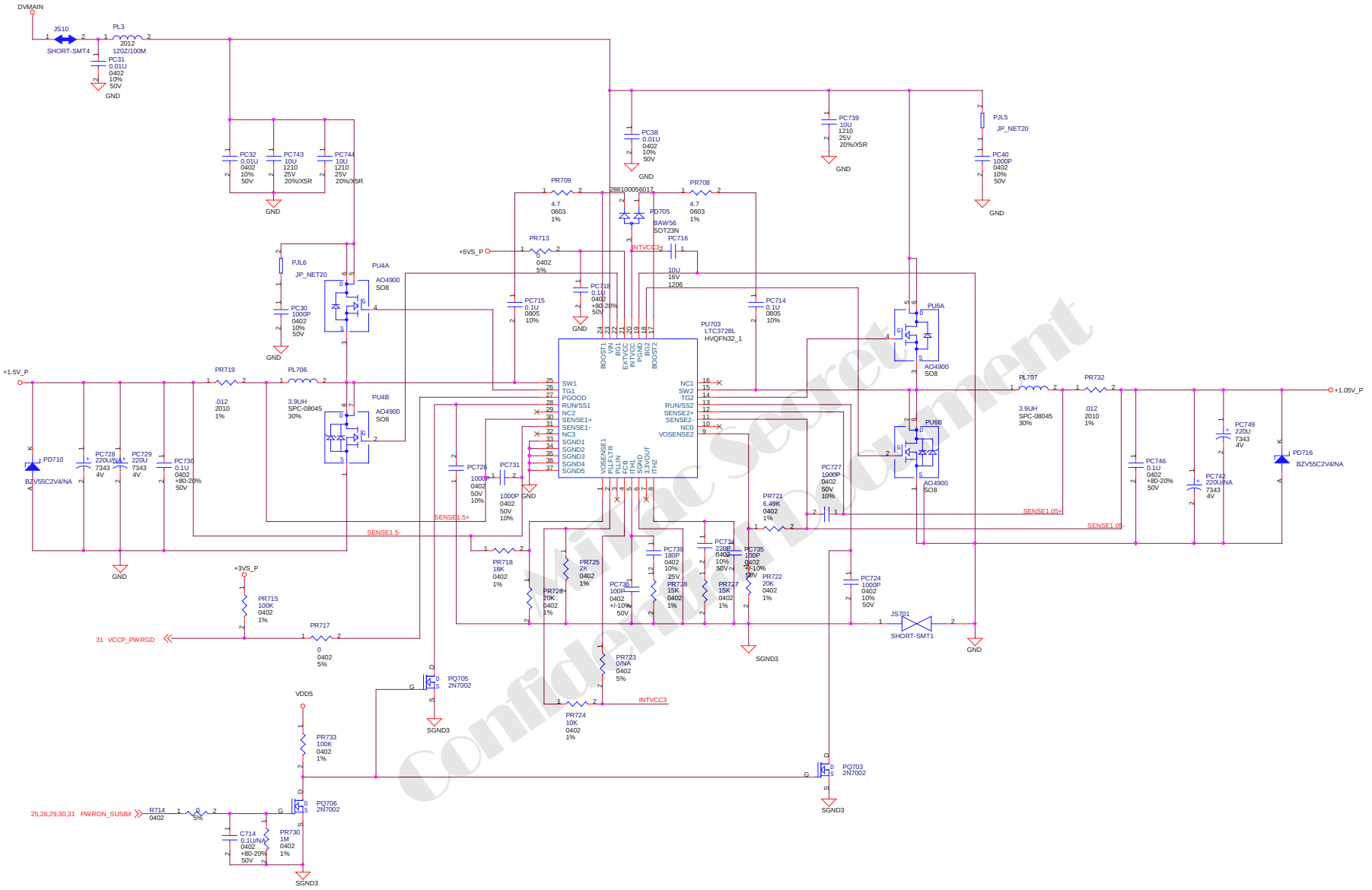
Title	8050D MOTHER B/D	
Size C	Document Number PCB 316680900001/ASSY 411682700001	Rev R01
Date: Wednesday, December 31, 2003	Sheet 25 of 34	

+2.5VS_DDR_P/+1.25V_DDR_P



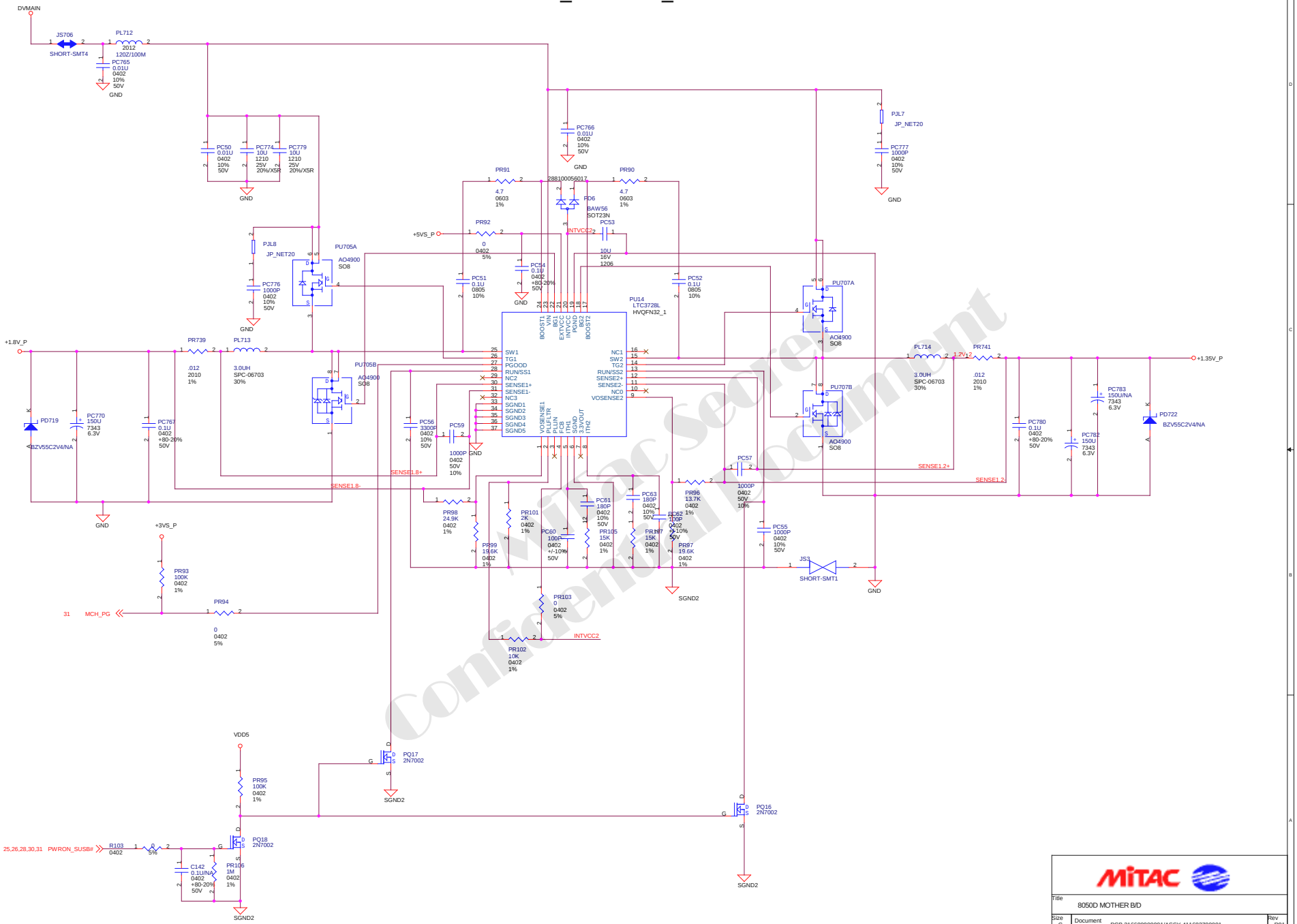


+1.5V_P/+1.05V_P

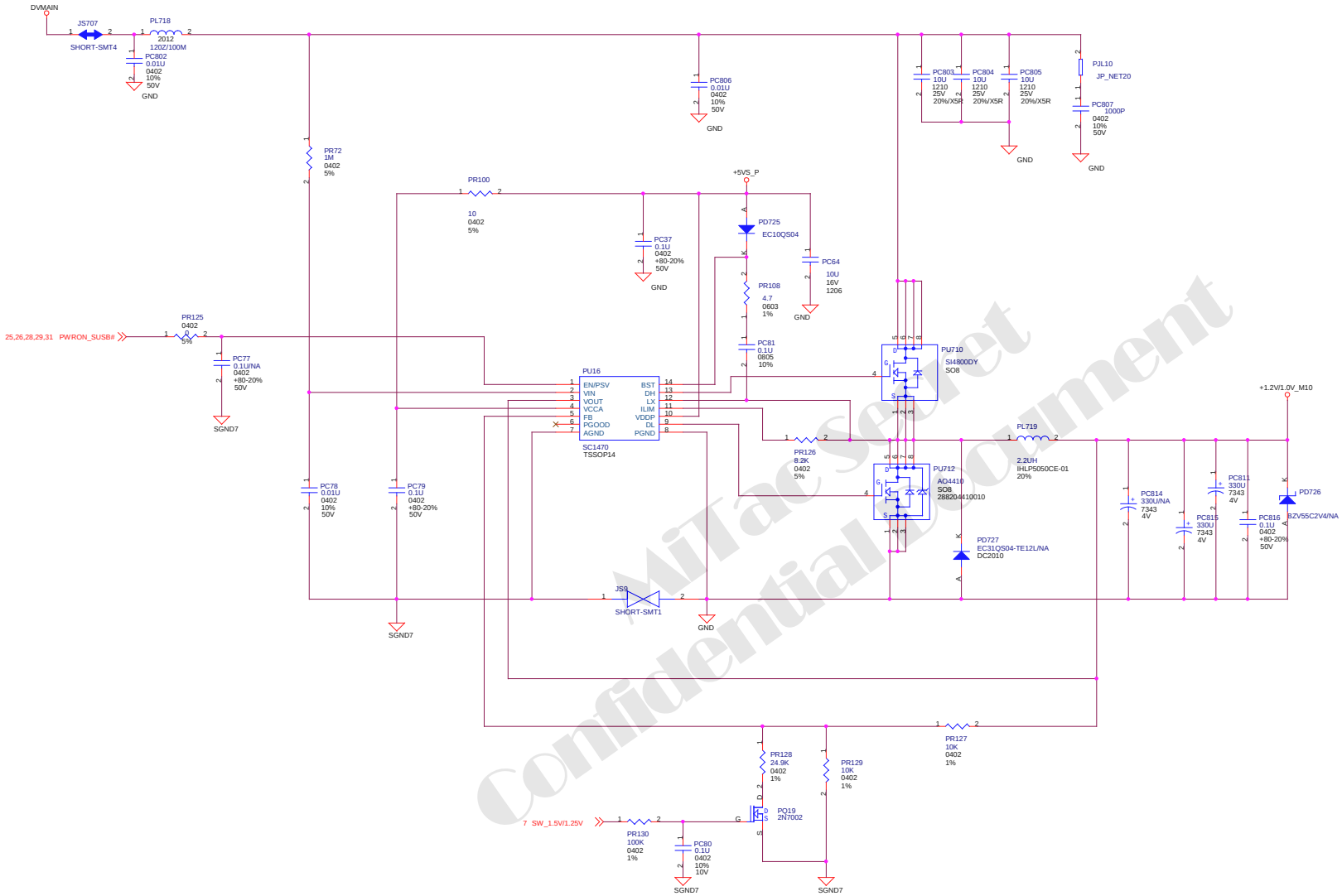


Title	8050D MOTHER B/D	
Size C	Document Number PCB 316680900001/ASSY 411682700001	Rev R01
Date: Wednesday, December 31, 2003	Sheet 28 of 34	

+1.8V_P/+1.35V_P



+1.2V/1.0V_M10

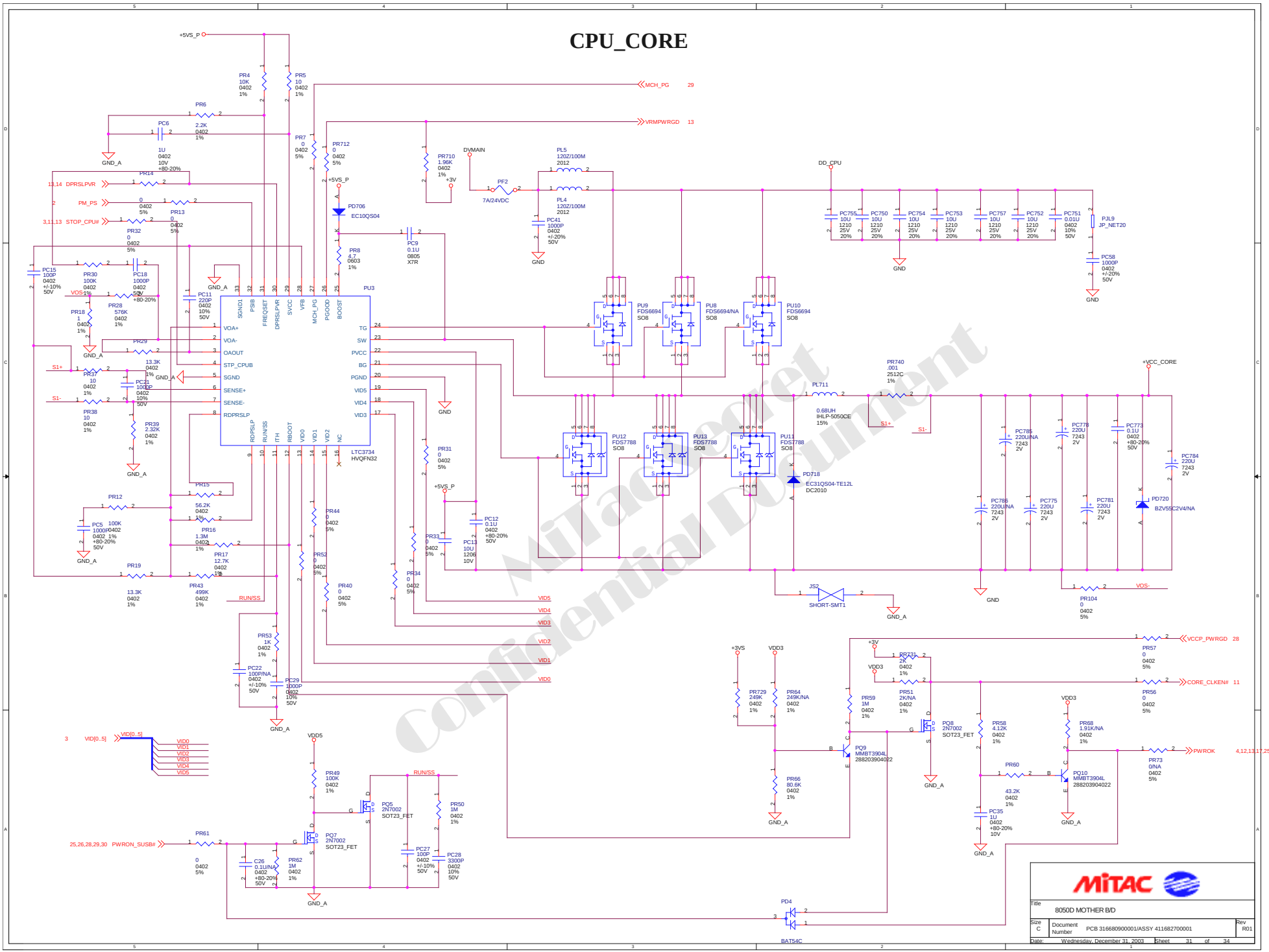


MiTAC

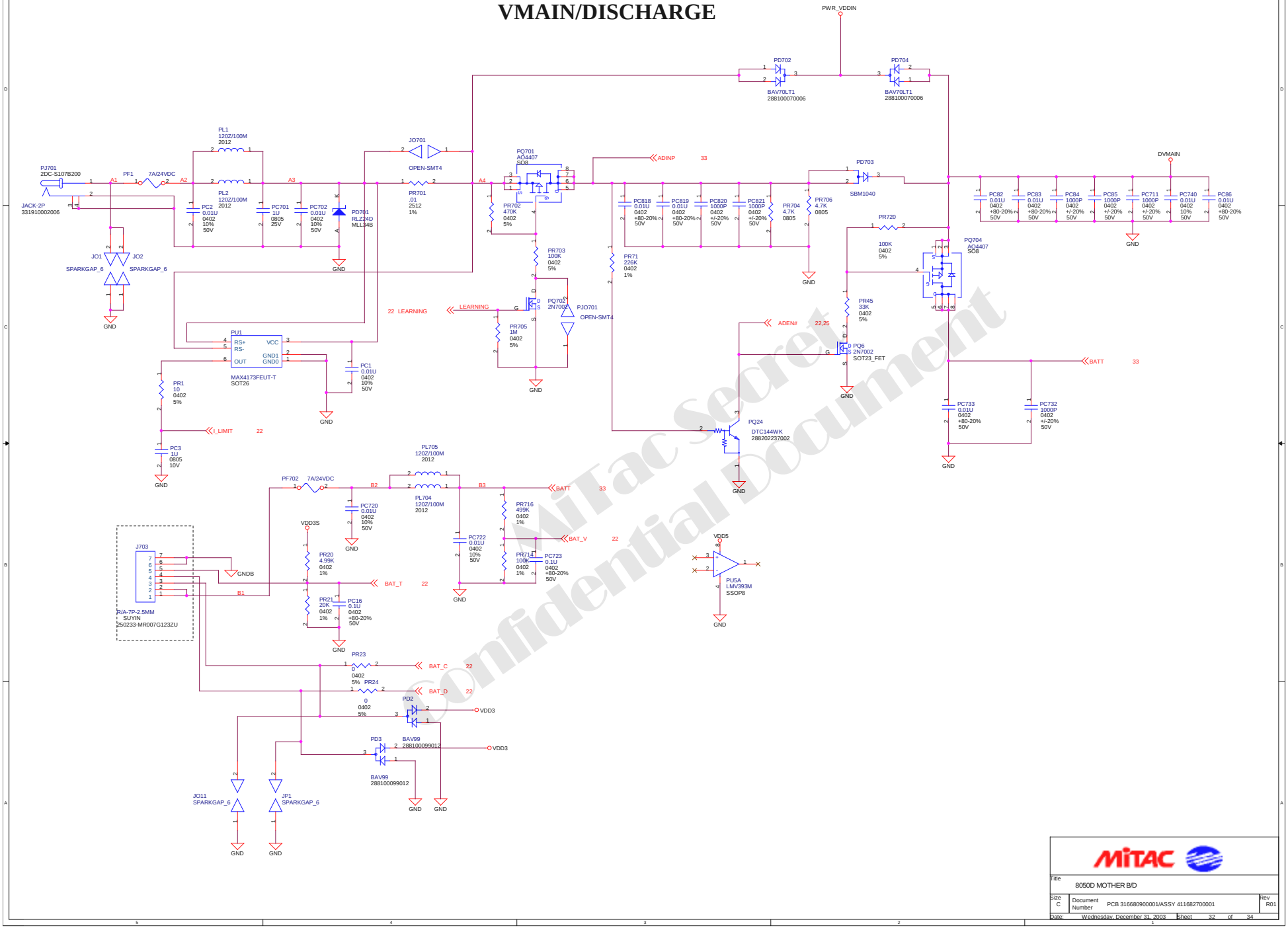
Title: 8050D MOTHER B/D

Size: C | Document Number: PCB 316680900001/ASSY 411682700001 | Rev: R01

Date: Wednesday, December 31, 2003 | Sheet 30 of 34



VMAIN/DISCHARGE



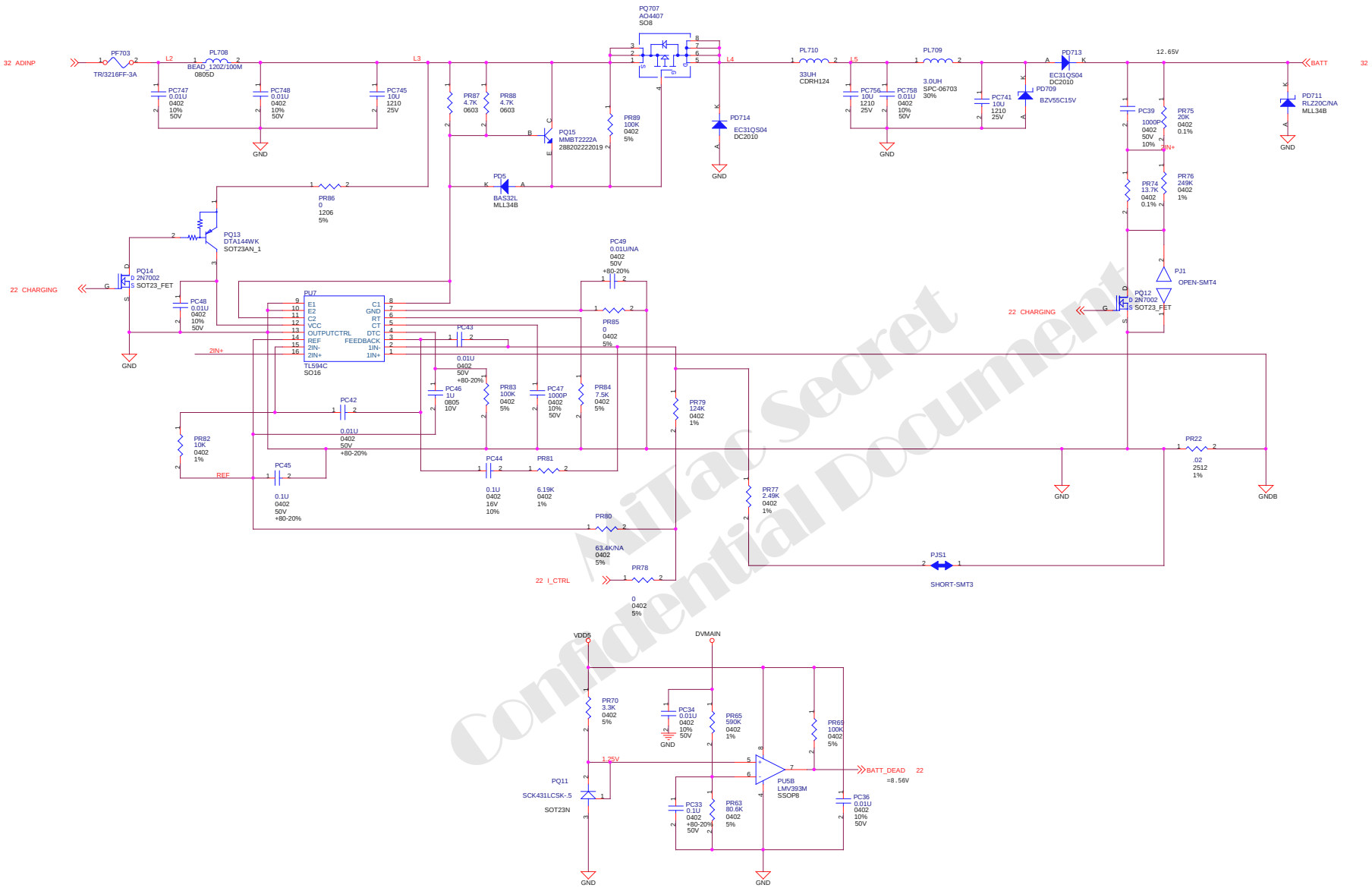
MiTAC

Title: 8050D MOTHER B/D

Size: C | Document Number: PCB 316680900001/ASSY 411682700001 | Rev: R01

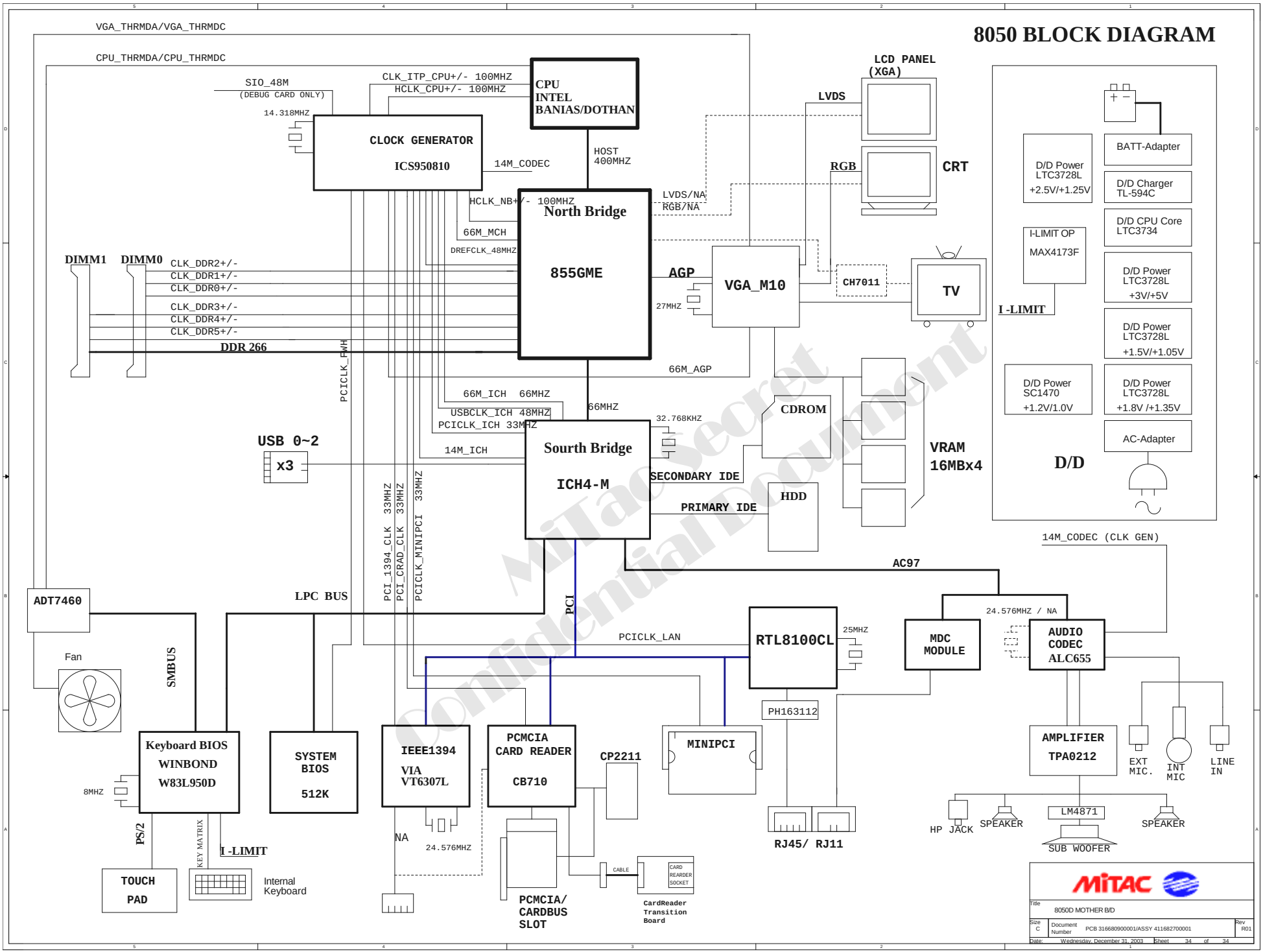
Date: Wednesday, December 31, 2003 | Sheet 32 of 34

CHARGING



MiTAC

Title	8050D MOTHER B/D
Size C	Document Number PCB 316680900001/ASSY 411682700001 Rev R01
Date: Wednesday, December 31, 2003	Sheet 33 of 34



REFERENCE MATERIAL

Intel Mobile Pentium-M Processor/BANIAS Processor	Intel, INC.
“Intel 855GME North Bridge”	Intel, INC.
“Intel ICH-4 South Bridge”	Intel, INC.
WINBOND KBC	WINBOND, LTD.
Clock Syntherizer	ICS,INC
VT6307L IEEE1394 Host Controller	AMPRO Computers, INC
System Explode View	Technology Corp / MiTAC
8050D Hardware Specification	Technology Corp / MiTAC

SERVICE MANUAL FOR 8050D

Sponsoring Editor : Jesse Jan

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Assistant Editor : Ping.Xie

Publisher : MiTAC International Corp.

Address : 1, R&D Road 2, Hsinchu Science-Based Industrial, Hsinchu, Taiwan, R.O.C.

Tel : 886-3-5779250 Fax : 886-3-5781245

First Edition : Mar.2004

E-mail : Willy.Chen @ mic.com.tw

Web : http: //www.mitac.com http: //www.mitacservice.com