SERVICE MANUAL FOR

8011

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MiTAC

8011 N/B Maintenance

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1.1 Introduction

1.1.1 General Description

This document describes the brief introduction for MiTAC 8011 portable notebook computer system.

1.1.2 System Overview

The MiTAC 8011 model is designed for Intel Banias and Celeron processor with 400MHz FSB with Micro-FCPGA package. It can support Banias 1.5G ~ 1.7GHz/Celeron-M 1.3G~1.5GHz/Dothan 1.5G~1.8GHz and 2.0GHz and above.

This system is based on PCI architecture and is fully compatible with IBM PC/AT specification, which has standard hardware peripheral interface. The power management complies with Advanced Configuration and Power Interface (ACPI) 2.0. It also provides easy configuration through CMOS setup, which is built in system BIOS software and can be pop-up by pressing F2 key at system start up or warm reset. System also provides icon LEDs to display system status, such as AC Power indicator, Battery Power indicator, Battery status indicator, HDD,CD-ROM, NUM LOCK, CAP LOCK, SCROLL LOCK, RF on/off. It also equipped with LAN, 56K Fax MODEM, FIR, 3 USB port, IEEE1394, PCMCIA, DVI-D and audio SPDIF, external and internal microphone function.

The memory subsystem supports two expansion DDR SDRAM slot with unbuffered PC1600/PC2100/PC2700 DDR-SDRAM.

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The Montara-GME GMCH Host Memory Controller integrates a high performance host interface for Intel Banias processor, a high performance 2D/3D Graphic Engine, a high performance memory controller, Digital Video port (DVOB & DVOC) interface, and Intel Hub interface Technology connecting with Intel 82801DBM ICH4-M.

The Intel ICH4-M integrates three Universal Serial Bus 2.0 Host Controllers Interface (UHCI), the Audio Controller with AC97 interface, the Ethernet includes a 32-bit PCI controller, the IDE Master/Slave controllers, and Intel Hub interface technology.

The Realtek RTL8100C(L) is a highly integrated, cost-effective single-chip Fast Ethernet controller that provides 32-bit performance, PCI bus master capability, and full compliance with IEEE 802.3u 100Base-T specifications and IEEE 802.3x Full Duplex Flow Control. It also supports the Advanced Configuration Power management Interface (ACPI).

The VT6301S is a single chip PCI Host Controller for IEEE 1394-1995 Release 1.0 and IEEE 1394a P2000. It implements the Link and PHY layers for IEEE 1394-1995 High Performance Serial Bus specification release 1.0 and 1394a P2000. It is compliant with 1394 Open HCI 1.0 and 1.1 with DMA engine support for high performance data transfer via a 32-bit bus master PCEI host bus interface. The VT6301S supports 100, 200 and 400 Mbit/sec transmission via an integrated 1-port PHY. The VT6301S services two types of data packets: asynchronous and isochronous(real time). The 1394 link core performs arbitration requesting, packet generation and checking, and bus cycle master operations. It also has root node capability and performs retry operations.

The CB-1211/1410 is a high performance PCI-to-CardBus controller with package type of 144-pin LQFP, and consisting of 3.3V core logic and 3.3V I/O buffers with 5V tolerance. All card signals are buffered internally to allow hot insertion and removal without external buffering.

The ALC655 is a 16-bit, full duplex AC'97 2.3 compatible six channels audio CODEC designed for PC multimedia

systems, including host/soft audio and AMR/CNR based designs. The ALC655 incorporates proprietary converter technology to meet performance requirements on PC99/2001 systems. The ALC655 CODEC provides three pairs of stereo outputs with 5-Bit volume controls, a mono output, and multiple stereo and mono inputs, along with flexible mixing, gain and mute functions to provide a complete integrated audio solution for PCs. The digital interface circuitry of the ALC655 CODEC operates from a 3.3V power supply for use in notebook and PC applications.

The W83L517D provides one high-speed serial communication ports (UARTs), one of which supports serial Infrared communication. The UART includes a 16-byte send/receive FIFO, a programmable baud rate generator, complete modem control capability, and a processor interrupt system. The UART provides legacy speed with baud rate up to 115.2k bps and also advanced speed with baud rates of 230k, 460k, or 921k bps which support higher speed modems. In addition, the W83L517D provides IR functions: IrDA 1.0 (SIR for 1.152K bps) and IrDA 1.1 (MIR for 1.152M bps or FIR for 4M bps), TV remote IR, (Consumer IR, supporting NEC, RC-5, extended RC-5, and RECS-80 protocols).

The W83L950D is a high performance microcontroller on-chip supporting functions optimized for embedded control. These include ROM, RAM, four types of timers, a serial communication interface, optional I²C bus interface, host interface, A/D converter, D/A converter, I/O ports, and other functions needed in control system configurations, so that compact, high performance systems can be implemented easily.

A full set of software drivers and utilities are available to allow advanced operating systems such as Windows ME, Windows 2000 and Windows XP to take full advantage of the hardware capabilities. Features such as bus mastering IDE, Plug and Play, Advanced Power Management (APM) with application restart, software-controlled power shutdown.

Following chapters will have more detail description for each individual sub-systems and functions.

1.1.3 System Hardware Parts

CPU	Intel Pentium-M Processor CPU Support Intel Celeron-M Processor CPU Support FSB 400 MHz Micro-FCPGA
Core logic	Intel 855GME + ICH4-M chipset
VGA Control	NB Integrate
System BIOS	Flash EPROM 512K (Include System BIOS and VGA BIOS)
Memory	0MB DDR-SDRAM on Board Expandable with combination Of Optional 128MB / 256MB / 256MB /512MB (P) memory Two 200-pin DDR 266/333 SDRAM Memory Module
Video Memory	Share memory 32Mb
Clock Generator	ICS 950812
DVI-D	Sil 1162
IEEE1394	VT6301S
LAN	RTL8100C
PCMCIA	ENE CB1410
Audio System	AC97 CODEC: Advance Logic, Inc, ALC655 Power Amplifier: TI TPA0212
FIR	TFDU6102
Modem	AC97 Link: MDC (Mobile Daughter Card) Askey: V1456VQL-P1(INT)

1.2 Hardware System

1.2.1 Intel Banias processors in Micro-FCPGA package.

- Intel Banias/Dothan Processors with 478 pins Micro-FCPGA package .
- The first Intel mobile processor with the Intel Net Burst micro-architecture which features include hyper-pipelined technology, a rapid execution engine, a 400MHz system, an execution trace cache, advanced dynamic execution, advanced transfer cache, enhanced floating point and multi-media unit, and Streaming SIMD Extensions 2 (SSE2).
- The Streaming SIMD Extensions 2 (SSE2) enable break-through levels of performance in multimedia applications including 3-D graphics, video decoding/encoding, and speech recognition.
- Use Source-Synchronous Transfer (SST) of address and data to improve performance by transferring data four times per bus clock.
- Support Enhanced Intel Speed Step technology, which enables real-time dynamic switching of the voltage and frequency between two performance modes.

1.2.2 Synthesizer

System frequency synthesizer: ICS950812 Programmable output frequency, divider ratios, output rise/fall time, output skew. Programmable spread percentage for EMI control. Watchdog timer technology to reset system if system malfunctions. Programmable watchdog safe frequency. Support I2C Index read/write and block read/write operations. Use external 14.318MHz crystal.

- Provides standard frequencies and additional 5% and 10% over-clocked frequencies
- Supports spread spectrum modulation:No spread, Center Spread (±0.35%, ±0.5%, or ±0.75%), or Down Spread (-0.5%, -1.0%, or -1.5%)
- Offers adjustable PCI early clock via latch inputs
- Selectable 1X or 2X strength for REF via I2C interface
- Efficient power management scheme through PD#, CPU_STOP# and PCI_STOP#.
- Uses external 14.318MHz crystal
- Stop clocks and functional control available through

1.2.3 Montara-GME GMCH IGUI 3D Graphic DDR/SDR Chipset

Montara-GME GMCH IGUI Host Memory Controller integrates a high performance host interface for Intel Banias processor, a high performance 2D/3D Graphic Engine, a high performance memory controller, an AGP 4X interface, and Intel®' I/O Hub architecture INTEL 82801DBM ICH4-M.

Montara-GME GMCH Host Interface features the AGTL & AGTL+ compliant bus driver technology with integrated on-die termination to support Intel Banias processors. Montara-GME GMCH provides a 12-deep In-Order-Queue to support maximum outstanding transactions up to 12. It integrated a high performance 2D/3D Graphic Engine, Video Accelerator and Advanced Hardware Acceleration MPEGI/MPEGII Video Decoder for the Intel Banias series based PC systems. It also integrates a high performance 2.1GB/s DDR266 Memory controller to sustain the bandwidth demand from the integrated GUI or external AGP master, host processor, as well as the multi I/O masters. In addition to integrated GUI, Montara-GME GMCH also can support external AGP slot with AGP 1X/2X/4X capability and Fast Write Transactions. A high bandwidth and mature Intel®' I/O Hub architecture is incorporated to connect

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Montara-GME GMCH and INTEL 82801DBM ICH4-M together. Intel®' I/O Hub architecture is developed into three layers, the Multi-threaded I/O Link Layer delivering 1.2GB bandwidth to connect embedded DMA Master devices and external PCI masters to interface to Multi-threaded I/O Link layer, the Multi-threaded I/O Link Encoder/Decoder in INTEL 82801DBM ICH4-M to transfer data w/ 533 MB/s bandwidth from/to Multi-threaded I/O Link layer to/from Montara-GME GMCH, and the Multi-threaded I/O Link Encoder/Decoder in Montara-GME GMCH to transfer data w/ 533 MB/s from/to Multi-threaded I/O Link layer to/from Intel 82801DBM ICH4-M.

An Unified Memory Controller supporting DDR266 DRAM is incorporated, delivering a high performance data transfer to/from memory subsystem from/to the Host processor, the integrated graphic engine or external AGP master, or the I/O bus masters. The memory controller also supports the Suspend to RAM function by retaining the CKE# pins asserted in ACPI S3 state in which only AUX source deliver power. The Montara-GME GMCH adopts the Shared Memory Architecture, eliminating the need and thus the cost of the frame buffer memory by organizing the frame buffer in the system memory. The frame buffer size can be allocated from 8MB to 64MB.

Features :

- **Processor/Host Bus Support**
  - Intel® Banias processor
  - 2X Address, 4X data
  - Support host bus Dynamic Bus Inversion (DBI)
  - Supports system bus at 400MT/s (100 MHz)
  - 8-deep In-Order-Queue
  - AGTL+ bus driver technology with integrated GTL termination resistors and low voltage operation (1.05V)
  - Support Enhanced Intel SpeedStep Technology and Geyserville III

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- Support for DPWR# signal to Banias processor for PSB power management

- **Memory System**

  - Directly supports one DDR channel, 64-b wide (72-b with ECC).
  - Supports 200-MHz , 266-MHz and 333-MHz DDR devices with max of 2 Double-Sided SO-DIMMs(4 rows populated) with unbuffered PC1600/PC2100/PC2700 DDR(with ECC).
  - Supports 128-Mb, 256-Mb and 512-M bit technologies providing maximum capacity of 1-GB with X16 devices and up to 2-GB with dual stack DDP (using 512-M bit technology)
  - All supported devices have 4 banks.
  - Configurable optional ECC operation (Signal bit Error Correction and multiple bit Error Dectection).
  - Encoding at low CPU utilization

- **System interrupt**

  - Support 8259 and processor system bus interrupt delivery mechanism
  - Support interrupts signaled as upstream Memory Writes from PCI and Hub interface
  - MSI send to the CPU through the System Bus
  - From IOx APIC in ICH4-M provides redirection for urstream interrupts to the system bus

- **Video stream decoder**

  - Improved HW Motion Compensation for MPEG2
  - All format decoder (18 ATSC formats) supported
  - Dynamic Bob and Weave support for Video Streams

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- Software DVD at 60 fields/second and 30 frames/second full screen
- Support for standard definition DVD (i. e. NTSC pixel resolution of 720*480 etc.) quality encoding at low CPU utilization

- **Video Overlay**

- Single high quality scalable overlay and second Sprite to support second overlay
- Multiple overlay functionality provided via Arithmetic Stretch Blt
- 5-tap horizontal,3-tap vertical filtered scaling.
- Direct YUV from Overlay to TV-out
- Independent Gamma Correction
- Independent Brightness / Contrast / Saturation
- Independent Tint / Hue support
- Destination Color keying
- Source Chromakeying
- Maximum source resolution of 1920x1080 pixels
- Maximum overlay clock of 133 MHz/200 MHz (120-Mp/s) provides a pixel resolution up to 1600x1200 at 60-Hz or 1280x1024 at 85 Hz (Please refer to the Montara GM SW PRD rev. 0.8 for detailed display information,i. e. pixel depths,etc)
- Multiple hardware color cursor support (32-bit with alpha and legacy 2-bpp mode)
- Accompanying I2C and DDC channels provided through multiplexed interface.

- **Display**

- Analog Display Support

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- 350 MHz integrated 24-bit RAMDAC that can drive a standard progressive scan analog monitor with pixel resolution up to 1600 x1200 at 85Hz and 2048x1536 at 75Hz.
- Dual independent pipe support
- Concurrent Different image and native display timings on each display device.
- Simultaneous: Same image and native display timings on each display device.
- DVO (DVOB and DVOC) support
  -- Digital video out port DVOB and DVOC with 165-MHz dot clock on each 12-bit interface;two 12-bit channels can be combined to from one dual channel 24-bit interface with an effective dot clock of 330MHz.
  -- The combined DVO B/C ports as well as individual DVO B/C port can drive a variety of DVO devices (TV-Out Encoders.TMDS and LVDS transmitters.Etc.) with pixel resolution up to 1600x1200 at 85Hz and 2048x1536 at 75Hz.
  -- Compliant with DVI Specifiction1.0
- Dedicated LFP (local flat panel) interface
  -- Single or dual channel LVDS panel support up to UXGA panel resolution with frequency range from 25MHz to 112MHz (single channel/dual channel)
  -- SSC support of 0.5%, 1.0%, and 2.5% center and down spread with external SSC clock
  -- Supports data format of 18bpp
  -- LCD panel power sequencing compliant with SPWG timing specification
  -- Compliant with ANSI/TIA/EIA –644-1995 spec
  -- Integrated PWM interface for LCD backlight inverter control
  -- Bi-linear Panel fitting
- Tri-view support through LFP interface, DVOB/DVOC ports and CRT

1.2.4 I/O Controller Hub : Intel 82801DBM

The Intel 82801DBM ICH4-M integrates three Universal Serial Bus 2.0 Host Controllers, the Audio Controller with AC 97 Interface, the IDE Master/Slave controllers, and Intel®' I/O Hub architecture. The PCI to LPC Bridge, I/O Advanced Programmable Interrupt Controller, legacy system I/O and legacy power management functionalities are integrated as well.

The integrated Universal Serial Bus Host Controllers features Dual Independent UHCI Compliant Host controllers with six USB ports delivering 480 Mb/s bandwidth and rich connectivity. Besides, Legacy USB devices as well as over current detection are also implemented.

The Integrated AC97 v2.3 compliance Audio Controller that features a 7-channels of audio speaker out and HSP v.90 modem support. Additionally, the AC97 interface supports 4 separate SDATAIN pins that is capable of supporting multiple audio codecs with one separate modem codec.

The integrated IDE Master/Slave controllers features Dual Independent IDE channels supporting PIO mode transfers up to 16 Mbytes/sec and Ultra DMA 33/66/100. It provides two separate data paths for the dual IDE channels that sustain the high data transfer rate in the multitasking environment.

Intel 82801DBM ICH4-M supports 6 PCI masters and complies with PCI 2.2 specification. It also incorporates the legacy system I/O like: two 82C37 compatible DMA controllers, Channels 0-3 are hardwired to 8 bit, three 8254 compatible programmable 16-bit counters channels 5-7, hardwired keyboard controller and PS2 mouse interface (not use in MiTAC 8080 model), Real Time clock with 512Bytes CMOS SRAM and two 82C59 compatible Interrupt controllers. Besides, the I/O APIC managing up to 14 interrupts with both Serial and FSB interrupt delivery modes is supported.

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The integrated power management module incorporates the ACPI 1.0b compliance functions, the APM 1.2 compliance functions, and the PCI bus power management interface spec. v1.1. Numerous power-up events and power down events are also supported. 21 general purposed I/O pins are provided to give an easy to use logic for specific application. In addition, the Intel 82801DBM ICH4-M supports Deeper Sleep power state for Intel Mobile processor.

A high bandwidth and mature Intel®' I/O Hub architecture is incorporated to connect Montara and Intel 82801DBM ICH4-M Hub interface together. Intel®' I/O Hub architecture is developed.

Features :

- PCI Bus Interface
- Supports PCI Revision 2.2 Specification at 33 MHz
- 133 MB/sec maximum throughput
- Supports up to six master devices on PCI
- One PCI REQ/GNT pair can be given higher arbitration priority (intended for external 1394 host controller)
- Support for 44-bit addressing on PCI using DAC protocol Integrated LAN Controller
- WfM 2.0 and IEEE 802.3 compliant
- LAN Connect Interface (LCI)
- 10/100 M bit/sec Ethernet support_ Integrated IDE Controller
- Supports "Native Mode" register and interrupts
- Independent timing of up to 4 drives, with separate primary and secondary IDE cable connections

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- Ultra ATA/100/66/33, BMIDE and PIO modes
- Tri-state modes to enable swap bay
- USB
- Includes three UHCI host controllers that support six external ports
- New: Includes one EHCI high-speed USB 2.0 Host Controller that supports all six ports
- New: Supports a USB 2.0 high-speed debug port
- Supports wake-up from sleeping states S1–S5
- Supports legacy keyboard/mouse software AC-Link for Audio and Telephony CODECs
- Supports AC ’97 2.3
- New: Third AC_SDATA_IN line for three codec support
- New: Independent bus master logic for seven channels (PCM In/Out, Mic 1 input, Mic 2 input, modem in/out, S/PDIF out)
- Separate independent PCI functions for audio and modem
- Support for up to six channels of PCM audio output (full AC3 decode)
- Supports wake-up events Interrupt Controller
- Support up to eight PCI interrupt pins
- Supports PCI 2.2 message signaled interrupts
- Two cascaded 82C59 with 15 interrupts
- Integrated I/O APIC capability with 24 interrupts

- Supports processor system bus interrupt delivery New: 1.5 V operation with 3.3 V I/O
- 5V tolerant buffers on IDE, PCI, USB over current and legacy signals Timers Based on 82C54
- System timer, refresh request, speaker tone output Power Management Logic
- ACPI 2.0 compliant
- ACPI-defined power states (C1–C2, S3–S5)
- Supports Desktop S1 state (like C2 state, only STPCLK# active)
- ACPI power management timer
- PCI PME# support
- SMI# generation
- All registers readable/restorable for proper resume from 0 V suspend states External Glue Integration
- Integrated pull-up, pull-down and series termination resistors on IDE, processor interface
- Integrated Pull-down and Series resistors on USB Enhanced Hub Interface Buffers Improve Routing flexibility (Not available with all Memory Controller Hubs)

1.2.5 CardBus: CB1410

Features :

3.3V operation with 5V tolerance,144-pin LQFP or 144-ball LFBGA package for CB1410 single slot Cardbus controller

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- **Compliant with**

  - PCI Local Bus Specification, Revision 2.2
  - PCI Bus Power Management Interface Specification, Revision 1.1
  - PCI Mobile Design Guide, Version 1.1
  - Advanced Configuration and Power Interface Specification, Revision 1.0
  - PC 99 System Design Guide
  - PC Card Standard 8.0

- **Interrupt configuration**

  - Supports parallel PCI interrupts
  - Supports parallel IRQ and parallel PCI interrupts
  - Supports serialized IRQ and parallel PCI interrupts
  - Supports serialized IRQ and PCI interrupts

- **Power Management Control Logic**

  - Supports CLKRUN# protocol
  - Supports SUSPEND#
  - Supports PCI PME# from D3, D2, D1 and D0
  - Supports PCI PME# from D3Cold
  - Supports D3STATE# (CB1410 only)

- **Power Switch Interface**

  - CB1410 supports parallel 4 wire power switch interface

- **Misc Control Logic**

  - Supports serial EEPROM interface
  - Supports socket activity LED
  - Supports 5 GPIOs and GPE#
  - Supports standard Zoomed Video Port
  - Supports SPKROUT, CAUDIO and RIOUT#
  - Supports PCI LOCK#

1.2.6 DVI

The SiI 1162 transmitter uses Panel Link Digital technology to support displays ranging from VGA to UXGA resolution in a single link interface. The SiI 1162 transmitter uses a 12-bit interface, taking in one half-pixel per clock edge. Designed to accommodate ultra high speed parallel interfaces such as the Intel DVO port, the SiI 1162 transmitter reduces pin count to a bare minimum and at the same time improves signal timing. The SiI 1162's innovative design eases board design requirements as well. Panel Link Digital technology simplifies PC design by resolving many of the system level issues associated with high-speed mixed signal design, providing the system designer with a digital interface solution that is quicker to market and lower in cost.

Features :

- Scaleable Bandwidth: 25 - 165 mega pixels per second
- Flexible Input Clocking: Single Clock Dual edge or Differential Clock input mode
- I2C Slave Programming Interface
- Low Voltage Interface: 3.0V to 3.6V range and 1.0 tov1.9V range
- Monitor Detection supported through Hot Plug and Receiver Detection
- De-skewing Option: varies clock to data input timing
- Cable Distance Support: over 5 meter DVI cable
- DVI 1.0 Compliant with significantly greater margin than competitive solutions
- Low pin count and smaller 48-pin TSSOP package
- BIOS and driver compatible with SiI 164 transmitter
- Fully programmable through serial port
- Complete Windows and DOS driver support
- Low voltage interface support to graphics device

1.2.7 AC’97 AUDIO SYSTEM: Advance Logic, Inc, ALC655

The ALC655 is a 16-bit, full duplex AC'97 2.3 compatible six channels audio CODEC designed for PC multimedia systems,including host/soft audio and AMR/CNR based designs. The ALC655 incorporates proprietary converter technology to meet performance requirements on PC99/2001 systems. The ALC655 CODEC provides three pairs of

stereo outputs with 5-Bitvolume controls, a mono output, and multiple stereo and mono inputs, along with flexible mixing, gain and mute functions to provide a complete integrated audio solution for PCs. The digital interface circuitry of the ALC655 CODEC operates from a 3.3V power supply for use in notebook and PC applications. The ALC655 integrates 50mW/20ohm headset audio amplifiers at Front-Out and Surr-Out, built-in 14.318M 24.576MHz PLL and PCBEEP generator, those can save BOM costs. The ALC655 also supports the S/PDIF input and output function, which can offer easy connection of PCs to consumer electronic products, such as AC3 decoder/speaker and mini disk devices. ALC655 supports host/soft audio from Intel ICHx chipsets as well as audio controller based VIA/SIS/ALI/AMD/nVIDIA/ATI chipset. Bundled Windows series drivers (WinXP/ME/2000/98/NT), EAX/Direct Sound 3D/ I3DL2/ A3D compatible sound effect utilities (supporting Karaoke, 26-kind of environment sound emulation,10-band equalizer), HRTF 3D positional audio and Sensaura™ 3D (optional) provide an excellent entertainment package and game experience for PC users. Besides, ALC655 includes Realtek's impedance sensing techniques that makes device load on outputs and inputs can be detected

1.2.8 MDC: PCTEL MODEM DAUGHTER CARD PCT2303W (ASKEY V1456VQL-P1)

The PCT2303W chipset is designed to meet the demand of this emerging worldwide AMR/MDC market. The combination of PC-TEL's well proven PCT2303W chipset and the HSP56TM MR software modem driver allows systems manufactures to implement modem functions in PCs at a lower bill of materials (BOM) while maintaining higher system performance.

PC-TEL has streamlined the traditional modem into the Host Signal Processing (HSP) solution. Operating with the Pentium class processors, HSP becomes part of the host computer's system software. It requires less power to operate and less physical space than standard modem solutions. PC-TEL's HSP modem is an easily integrated, cost-effective

communications solution that is flexible enough to carry you into the future.

The PCT2303W chip set is an integrated direct access arrangement (DAA) and Codec that provides a programmable line interface to meet international telephone line requirements. The PCT2303W chip set is available in two 16-pin small outline packages (AC'97 interface on PCT303A and phone-line interface on PCT303W). The chip set eliminates the need for an AFE, an isolation transformer, relays, opto-isolators, and 2-to 4-wire hybrid. The PCT2303W chip set dramatically reduces the number of discrete components and cost required to achieve compliance with international regulatory requirements. The PCT2303W complies with AC'97 Interface specification Rev. 2.1.

The chip set is fully programmable to meet world-wide telephone line interface requirements including those described by CTR21, NET4, JATE, FCC, and various country-specific PTT specifications. The programmable parameters of the PCT2303W chip set include AC termination, DC termination, ringer impedance, and ringer threshold. The PCT2303W chip set has been designed to meet stringent world-wide requirements for out-of-band energy, billing-tone immunity, lightning surges, and safety requirements.

Features :

- Virtual com port with a DTE throughout up to 460.8Kbps.
- G3 Fax compatible
- Auto dial and auto answer
- Ring detection

Codec/DAA Features :

- AC97 2.1 compliant.

- 86dB dynamic range TX/RX paths
- 2-4-wire hybrid
- Integrated ring detector
- High voltage isolation of 4000V
- Support for “Caller ID”
- Compliant with FCC Part68, CTR21, Net4 and JATE
- Low power standby
- Low profile SOIC package 16 pins 10x3x1.55mm
- Low power consumption
- 10mA @ 3.3V operation
- 1mA @ 3.3V power down
- Integrated modem codec

1.2.9 IEEE1394 VT6301S

The VT6301 IEEE 1394 OHCI Host Controller provides high performance serial connectivity. It implements the Link and Phy layers for IEEE 1394-1995 High Performance Serial Bus specification release 1.0 and 1394a-2000. It is compliant with 1394 Open HCI 1.0 and 1.1 with DMA engine support for high performance data transfer via a 32-bit bus master PCI host bus interface. The VT6301 supports 100, 200 and 400 Mbit/sec transmission via an integrated 1-port PHY. The VT6301 services two types of data packets: asynchronous and isochronous (real time). The 1394 link core performs arbitration requesting, packet generation and checking, and bus cycle master operations. It also has root

node capability and performs retry operations. The VT6301 is ready to provide industry-standard IEEE 1394 peripheral connections for desktop and mobile PC platforms. Support for the VT6301 is built into Microsoft Windows 98, Windows ME, Windows 2000, and Windows XP.

Features :

- 32 bit CRC generator and checker for receive and transmit data
- On-chip isochronous and asynchronous receive and transmit FIFOs for packets (2K for general receive plus 2K for isochronous transmit plus 2K for asynchronous transmit)
- 8 isochronous transmit contexts
- 4 isochronous receive contexts
- 3-deep physical post-write queue
- 2-deep physical response queue
- Dual buffer mode enhancements
- Skip Processing enhancements
- Block Read Request handling
- Ack_tardy processing

1.2.10 System Flash Memory (BIOS)

Features :

- Firmware Hub for Intel® 810, 810E, 815, 815E,815EP, 820, 840, 850 Chipsets
- Flexible Erase Capability
- Single 3.0-3.6V Read and Write Operations
- Superior Reliability
- Firmware Hub Hardware Interface Mode

1.2.11 Memory System

64MB, 128MB, 256MB, 512MB (x64) 200-Pin DDR SDRAM SODIMMs :

- JEDEC-standard 200-pin, small-outline, dual in-line memory module (SODIMM)
- Utilizes 200 Mb/s and 266 Mb/s DDR SDRAM components
- 64MB (8 Meg x 64 [H]); 128MB (16 Meg x 64, [H] and [HD]); 256MB (32 Meg x 64 [HD]); 512MB (64 Meg x 64 [HD])
- VDD= VDDQ= +2.5V ±0.2V
- VDDSPD = +2.2V to +5.5V
- 2.5V I/O (SSTL_2 compatible)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs

- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Bidirectional data strobe (DQS) transmitted/received with data—i.e.,source-synchronous data capture
- Differential clock inputs (CK and CK# - can be multiple clocks, CK0/CK0#, CK1/CK1#, etc.)
- Four internal device banks for concurrent operation
- Selectable burst lengths: 2, 4, or 8
- Auto precharge option
- Auto Refresh and Self Refresh Modes
- 15.6µs (MT4VDDT864H, MT8VDDT1664HD), 7.8125µs (MT4VDDT1664H, MT8VDDT3264HD, MT8VDDT6464HD) maximum average periodic refresh interval
- Serial Presence Detect (SPD) with EEPROM
- Fast data transfer rates PC2100 or PC1600
- Selectable READ CAS latency for maximum compatibility
- Gold-plated edge contacts

1.2.12 LAN PHY: RTL8100C(L)

The Realtek RTL8100C(L) is a highly integrated, cost-effective single-chip Fast Ethernet controller that provides 32-bit performance, PCI bus master capability, and full compliance with IEEE 802.3u 100Base-T specifications and IEEE 802.3x Full Duplex Flow Control. It also supports the Advanced Configuration Power management Interface (ACPI), PCI power management for modern operating systems that are capable of Operating System Directed Power Management (OSPM) to achieve the most efficient power management possible. The RTL8100C(L) does not support

CardBus mode as the RTL8139C does. In addition to the ACPI feature, the RTL8100C(L) also supports remote wake-up (including AMD Magic Packet, LinkChg, and Microsoft® wake-up frame) in both ACPI and APM environments. The RTL8100C(L) is capable of performing an internal reset through the application of auxiliary power. When auxiliary power is applied and the main power remains off, the RTL8100C(L) is ready and waiting for the Magic Packet or Link Change to wake the system up. Also, the LWAKE pin provides 4 different output signals including active high, active low, positive pulse, and negative pulse. The versatility of the RTL8100C(L) LWAKE pin provides motherboards with Wake-On-LAN (WOL) functionality. The RTL8100C(L) also supports Analog Auto-Power-down, that is, the analog part of the RTL8100C(L) can be shut down temporarily according to user requirements or when the RTL8100C(L) is in a power down state with the wakeup function disabled. In addition, when the analog part is shut down and the IsolateB pin is low (i.e. the main power is off), then both the analog and digital parts stop functioning and the power consumption of the RTL8100C(L) will be negligible. The RTL8100C(L) also supports an auxiliary power auto-detect function, and will auto-configure related bits of their own PCI power management registers in PCI configuration space.

Features :

- 128 pin QFP/LQFP
- Integrated Fast Ethernet MAC, Physical chip and transceiver in one chip
- 10 Mb/s and 100 Mb/s operation
- Supports 10 Mb/s and 100 Mb/s N-way Auto-negotiation operation
- PCI local bus single-chip Fast Ethernet controller
- Supports 25MHz crystal or 25MHz OSC as the internal clock source. The frequency deviation of either crystal or OSC must be within 50 PPM.

- Compliant to PC99/PC2001 standard
- Supports Wake-On-LAN function and remote wake-up (Magic Packet*, LinkChg and Microsoft® wake-up frame)
- Supports 4 Wake-On-LAN (WOL) signals (active high, active low, positive pulse, and negative pulse)
- Supports auxiliary power-on internal reset, to be ready for remote wake-up when main power still remains off
- Supports auxiliary power auto-detect, and sets the related capability of power management registers in PCI configuration space.
- Includes a programmable, PCI burst size and early Tx/Rx threshold.
- Supports a 32-bit general-purpose timer with the external PCI clock as clock source, to generate timer-interrupt
- Contains two large (2Kbyte) independent receive and transmit FIFOs
- Advanced power saving mode when LAN function or wakeup function is not used
- Uses 93C46 (64*16-bit EEPROM) to store resource configuration, ID parameter, and VPD data.
- Supports LED pins for various network activity indications
- Supports loopback capability
- Half/Full duplex capability
- Supports Full Duplex Flow Control (IEEE 802.3x)

1.2.13 FIR TFDU6102

The TFDU6102 is a low–power infrared transceiver module compliant to the latest IrDA physical layer standard for fast infrared data communication, supporting IrDA speeds up to 4.0 Mbit/s (FIR), HP-SIR[, Sharp ASK[and carrier based remote control modes up to 2 MHz. Integrated within the transceiver module are a photo PIN diode, an infrared

emitter (IRED), and a low–power CMOS control IC to provide a total front–end solution in a single package. Vishay FIR transceivers are available in different package options, including this BabyFace package (TFDU6102), the standard setting, once smallest FIR transceiver available on the market. This wide selection provides flexibility for a variety of applications and space constraints. The transceivers are capable of directly interfacing with a wide variety of I/O devices which perform the modulation/ demodulation function, including National Semiconductor's PC87338, PC87108 and PC87109, SMC's FDC37C669, FDC37N769 and CAM35C44, and Hitachi's SH3. At a minimum, a VCC bypass capacitor are the only external components required implementing a complete solution. TFDU6102 has a tri–state output and is floating in shut–down mode with a weak pull–up.

Features :

- Compliant to the latest IrDA physical layer specification (Up to 4 Mbit/s), HP–SIR), Sharp ASK) and TV Remote Control.
- For 3.0 V and 5.0 V Applications
- Operates from 2.7 V to 5.5 V within specification,
- Low Power Consumption (< 3 mA Supply Current)
- Power Shutdown Mode (< 5 _A Shutdown Current in Full Temperature Range)
- Surface Mount Package
- Universal (9.7 x 4.7 x 4.0 mm3)
- Tri–state–Receiver Output, floating in shutdown with a weak pull–up
- High Efficiency Emitter
- BabyFace (Universal) Package Capable of Surface Mount Soldering to Side and Top View Orientation

- Directly Interfaces with Various Super I/O and Controller Devices
- Built–In EMI Protection – No External Shielding Necessary
- Only One External Component Required
- Backward Pin to Pin Compatible to all Vishay Telefunken SIR and FIR Infrared Transceivers
- Split power supply, transmitter and receiver can be operated from two power supplies with relaxed

1.2.14 Keyboard System: Winbond W83L950D

The Winbond Keyboard controller architecture consists of a Turbo 51 core controller surrounded by various registers, nine general purpose I/O port, 2k+256 bytes of RAM, four timer/counters, dual serial ports, 40K MTP-ROM that is divided into four banks, two SMBus interface for master and slave, Support 4 PWM channels, 2 D-A and 8 A-D converters.

Features :

- 8051 uC based
- Keyboard Controller Embedded Controller
- Supply embedded programmable flash memory (internal ROM size: 40KB) and RAM size is 2 KB.
- Support 4 Timer (8 bit) signal with 3 prescalers.
- Support 2 PWM channels, 2 D-A and 8 A-D converters.
- Reduce Firmware burden by Hardware PS/2 decoding
- Support 72 useful GPIOs totally

- Support Flash utility for on board re-flash
- Support ACPI
- Hardware fast Gate A20 with software programmable

1.3 Other Functions

1.3.1 Hot Key Function

Keys Combination	Feature	Meaning
Fn + F1	Power down	Mini PCI power down
Fn + F2	Reserve	
Fn + F3	Volume Down	
Fn + F4	Volume Up	
Fn + F5	LCD/external CRT switching	Rotate display mode in LCD only, CRT only, and simultaneously display.
Fn + F6	Brightness down	Decreases the LCD brightness
Fn + F7	Brightness up	Increases the LCD brightness
Fn + F8	Disable Touch-pad	
Fn + F10	Battery Low Beep	On/Off Battery Low Beep
Fn + F11	Panel Off/On	Toggle Panel on/off
Fn + F12	Suspend to DRAM / HDD	Force the computer into either Suspend to HDD or Suspend to DRAM mode depending on BIOS Setup.

1.3.2 Power On/Off/Suspend/Resume Button

1.3.2.1 APM Mode

At APM mode, Power button is on/off system power.

1.3.2.2 ACPI Mode

At ACPI mode. Windows power management control panel set power button behavior.You could set “standby”, “power off” or “hibernate”(must enable hibernate function in power Management) to power button function.Continue pushing power button over 4 seconds will force system off at ACPI mode.

1.3.3 Cover Switch

System automatically provides power saving by monitoring Cover Switch. It will save battery power and prolong the usage time when user closes the notebook cover.

At ACPI mode there are four functions to be chosen at windows power management control panel.

1. None
2. Standby
3. Off
4. Hibernate (must enable hibernate function in power management)

1.3.4 LED Indicators

1.3.4.1 Three LED indicators at front side:

From left to right that indicate BATTERY POWER, BATTERY STATUS and AC POWER

BATTERY POWER:

This LED lights green when the notebook is being powered by Battery, and flashes (on 1second, off 1 second) when entered suspend to RAM state with AC powered. The LED is off when the notebook is in power off state or powered by AC adapter.

BATTERY STATUS:

During normal operation, this LED stays off as long as the battery is charged. When the battery charge drops to 10% of capacity, the LED lights red, flashes per 1 second and beeps per 2 second. When AC is connected, this indicator glows green if the battery pack is fully charged or orange (amber) if the battery is being charged.

AC POWER:

This LED lights green when the notebook was powered by AC power line, Flashes (on 1 second,off 1 second) when entered suspend to RAM state with AC powered. The LED is off when the notebook is in power off state or powered by battery.

1.3.4.2 Six LED indicators:

System has six status LED indicators with blue color at left-front side which to display system activity. From left to right that indicate Mini PCI, CD-ROM, HARD DISK, NUM LOCK, CAPS LOCK, SCROLL LOCK.

1.3.4.3 Power button LED:

8011 design LED with white light on Power button. When system power on, the lightness will progress step by step from dark to light. When system power off, the lightness will progress step by step from light to dark. If system into suspend mode, the LED will change lightness from light to dark and come from dark to light continuously.

1.3.5 LED Indicators

1.3.5.1 Three LED indicators at front side:

- System also provides Battery capacity monitoring and gives users a warning signal to alarm they to store data before battery dead. This function also protects system from mal-function while battery capacity is low.
- Battery Warning: Capacity below 10%, Battery Capacity LED flashes per second, system beeps per 2 seconds.
- System will Suspend to HDD after 2 Minutes to protect users data.

1.3.5.2 Battery Low State:

After Battery Warning State, and battery capacity is below 5%, system will generate beep sound for twice per second.

1.3.5.3 Battery Dead State:

When the battery voltage level reaches 11.44 volts, system will shut down automatically in order to extend the battery packs' life.

1.3.6 Fan Power On/off management

FAN is controlled by W83L950D embedded controller-using ADT7460 to sense CPU temperature and PWM control fan speed. Fan speed is depended on CPU temperature. Higher CPU temperature faster Fan Speed.

1.3.7 CMOS Battery

- CR2032 3V 220mAh lithium battery
- When AC in or system main battery inside, CMOS battery will consume no power.
- AC or main battery not exists, CMOS battery life at less (220mAh/5.8uA) 4 years.

1.3.8 Battery Current Limit and Learning

Implanted H/W current limit and battery learning circuit to enhance protection of battery.

1.3.9 I/O Port

- One Power Supply Jack.
- One External CRT with DVI-D connector For CRT or LCD panel Display
- Supports three USB port for all USB devices.
- One MODEM RJ-11 phone jack for PSTN line
- One RJ-45 for LAN.
- One IEEE1394 port
- SPDIF Out Jack.
- Microphone Input Jack.
- FIR interface

1.4 Power Management

The 8011 system has built in several power saving modes to prolong the battery usage for mobile purpose. User can enable and configure different degrees of power management modes via ROM CMOS setup (booting by pressing F2 key). Following are the descriptions of the power management modes supported.

1.4.1 System Management Mode

1.4.1.1 Full On Mode

In this mode, each devices is running with the maximal speed. CPU clock is up to its maximum.

1.4.1.2 Doze Mode

In this mode, CPU will be toggling between on & stop grant mode either. The technology is clock throttling. This can save battery power without loosing much computing capability.

The CPU power consumption and temperature is lower in this mode.

1.4.1.3 Standby Mode

For more power saving, it turns off the peripheral components. In this mode, the following is the status of each device:

CPU: Stop grant LCD: backlight off HDD: spin down

1.4.1.4 Suspend to DRAM and HDD

The most chipset of the system is entering power down mode for more power saving. In this mode, the following is the status of each device:

Suspend to DRAM

- CPU: off
- Intel 855GME: Partial off
- VGA: Suspend
- PCMCIA: Suspend
- Audio: off
- SDRAM: self Refresh

Suspend to HDD

- All devices are stopped clock and power-down
- System status is saved in HDD
- All system status will be restored when powered on again

1.4.2 Other Power Management Functions

1.4.2.1 HDD & Video Access

System has the ability to monitor video and hard disk activity. User can enable monitoring function for video and/or hard disk individually. When there is no video and/or hard disk activity, system will enter next PMU state depending on the application. When the VGA activity monitoring is enabled, the performance of the system will have some impact.

1.5 Appendix 1: Intel 82801DBM ICH4-M GPIO Definitions

Pin Name	MUX Function	GPIO Function	Power Plane
GPIO0	CRT_IN#	GPI	MAIN
GPIO1	SB_CARD_PME#	GPI	MAIN
GPIO2	PCI_INTE#	GPI	MAIN
GPIO3	PCI_INTF#	GPI	MAIN
GPIO4	PCI_INTG#	GPI	MAIN
GPIO5	ICH_GPI5	GPI	MAIN
GPIO6	AGPBUSY#	GPI	MAIN
GPIO7	KBD_US/JP#	GPI	MAIN
GPIO8	EXTSMI#	GPI	RESUME
GPIO11	SMBALERT#	GPI	RESUME
GPIO12	SCI#	GPI	RESUME
GPIO13	WAKE_UP#	GPI	RESUME
GPIO16	X	GPO	MAIN
GPIO17	X	GPO	MAIN
GPIO18	STOP_PCI	GPO	MAIN
GPIO19	SUSA#	GPO	MAIN
GPIO20	STOP_CPU	GPO	MAIN
GPIO21	C3_STAT#	GPO	MAIN
GPIO22	CPUPERF#	OD	MAIN

Pin Name	MUX Function	GPIO Function	Power Plane
GPIO23	X	O	MAIN
GPIO24	PCLKRUN#	GPIO	RESUME
GPIO25	SPK_OFF	GPIO	RESUME
GPIO27	X	GPIO	RESUME
GPIO28	X	GPIO	RESUME
GPIO32	WIRELESS_PD#	GPIO	MAIN
GPIO33	PANEL_ID0	GPIO	MAIN
GPIO34	PANEL_ID1	GPIO	MAIN
GPIO35	PANEL_ID2	GPIO	MAIN
GPIO36	PANEL_ID3	GPIO	MAIN
GPIO37	MB_ID2	GPIO	MAIN
GPIO38	IDERST#	GPIO	MAIN
GPIO39	MINIPCI_ACT#	GPIO	MAIN
GPIO40	MB_ID0	GPIO	MAIN
GPIO41	MB_ID1	GPIO	MAIN
GPIO42	X	GPIO	MAIN
GPIO43	X	GPIO	MAIN

1.6 Appendix 2: W83L950D KBC Pins Definitions-1

Port	pin	Function	Implement
P0	54-47	Scan matrix	KO[0..7]
P1	46-39		KO[8..15]
P3	62-55		KI[0..7]
P2	0	LPC enable	H8_THRM#
	1	GPIO x1	H8_WAKE_UP#
	2	SMBUS1 or UART	BATT_G#
	3		BATT_R#
	4	GPIO x4	EXTSMI#
	5		CAP
	6		NUM
	7		SCROLL
P4	0	Xcin/cout or PWM 2,3	H8_ENABKL
	1		CHARGING
	2	GPIO x2 (INT1)	LEARING
	3		H8_SUSB
	4	KBRST	H8_HRCIN#
	5	A20	A20GATE
	6	GPIO x2	H8_SCI
	7		H8_PWRON

1.6 Appendix 2: W83L950D KBC Pins Definitions-2

Port	pin	Function	Implement
P5	0	GPIO x1	SW_VDD3
	1	GPIO x3 (INT20,30,40)	H8_LIDSW#
	2		BATT_DEAD#
	3		H8_ADEN#
	4	GPIO x2	BATT_POWER#
	5		KBC_PWRON_VDD3S
	6	D/A, PWM 2,3	BLADJ
	7		PWR_BTN_LED
P6	0	A/D (INT5-12)	PWRBTN#
	1		KBC_RI#
	2		AC_ POWER#
	3		BATT_VOLT
	4		BATT_TEMP
	5		H8_I_LIMIT
	6		H8_PROCHOT#
	7		+BC_CPUCORE
P7	0	PS/2 port x3	T_DATA
	1		H8_RSMRST
	2		ICH_PWRBTN
	3		T_CLK
	4		H8_PWRON_SUSB#
	5		SUSC#
	6	SMBUS	BAT_DATA
	7		BAT_CLK

1.6 Appendix 2: W83L950D KBC Pins Definitions-3

Port	pin	Function	Implement
P8	0	LPC interface	PCICLK_KBC
	1		SERIRQ
	2		LAD3
	3		LAD2
	4		LAD1
	5		LAD0
	6		KBC_PCIRST#
	7		LFRAME#

1.7 Appendix 3: MiTAC 8011 Product Specification-1

CPU	Intel Pentium-M Processor CPU Support Intel Celeron-M Processor CPU Support FSB 400 MHz Micro-FCPGA
Core logic	Intel 855GME + ICH4-M chipset
Memory	0MB DDR-SDRAM on Board Expandable with combination of optional 128MB/256MB/512MB(P) memory Two 200-pin DDR 266/333 SDRAM Memory Module
Video Controller	Montara-GME
LVDS	Montara-GME
DVI-D	SiI 1162
PCMCIA	ENE CB1410
LAN Controller & PHY	RTL8100CL
IEEE1394	VIA VT6301S
Fax Modem	AC97 Link :56Kbps MDC Askey: V1456VQL-P1(INT)
Audio	Audio Power Amplifier: TPA0212 AC 97 CODEC: ALC655
ROM Drive	12.7mm Height 8X DVD ROM Drive 24X10X8X24 Combo or above 2X2X1X8X24X10X24 DVD-RW

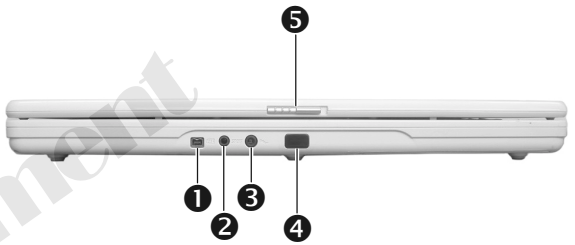
1.7 Appendix 3: MiTAC 8011 Product Specification-2

FDD	None
HDD	1.Fujitsu: (40/60/80GB) 2.Hitachi:40 60 /80 (GB)
Display	15.4" WXGA: 1.CHI MEI:N145l1-L02 2.Samsung:LTN154WX 3.Hitachi: TT39D89VC1FAA
Pointing Device	Intelligence Glide pad w/z 2 buttons
Keyboard	Windows 98 keyboard, multi languages support
KBC	Winbone: W83L950D
Battery (option)	Li-ION: Panasonic cell / SANYO / SAMSUNG: Molice or GLW pack 2200mAH x 4 or 8 Cells

2. System View and Disassembly

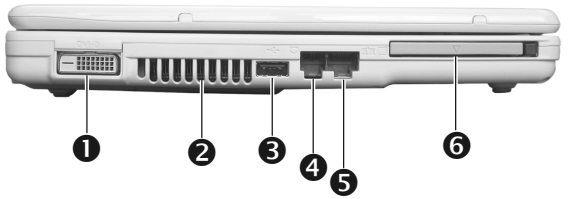
2.1 System View

2.1.1 Front View



❶ IEEE 1394 Connector
❷ Line Out Connector
❸ MIC In Connector
❹ FIR
❺ Top Cover Latch

2.1.2 Left-side View



❶ DVI Port
❷ Ventilation Openings
❸ USB Ports *1
❹ RJ-11 Connector
❺ RJ-45 Connector
❻ PCMCIA Card Socket

2.1.3 Right-side View

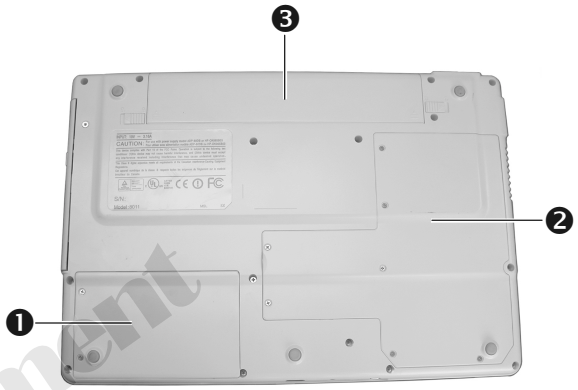
❶ CD-ROM/DVD-ROM Drive
❷ Kensington Lock

2.1.4 Rear View

❶ VGA Port
❷ Power Connector
❸ USB Port*2

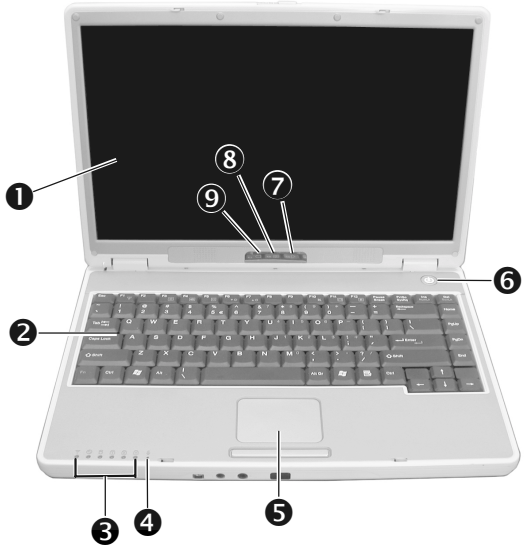
2.1.5 Bottom View

❶ Hard Disk Drive
❷ CPU
❸ Battery Park



2.1.6 Top-open View

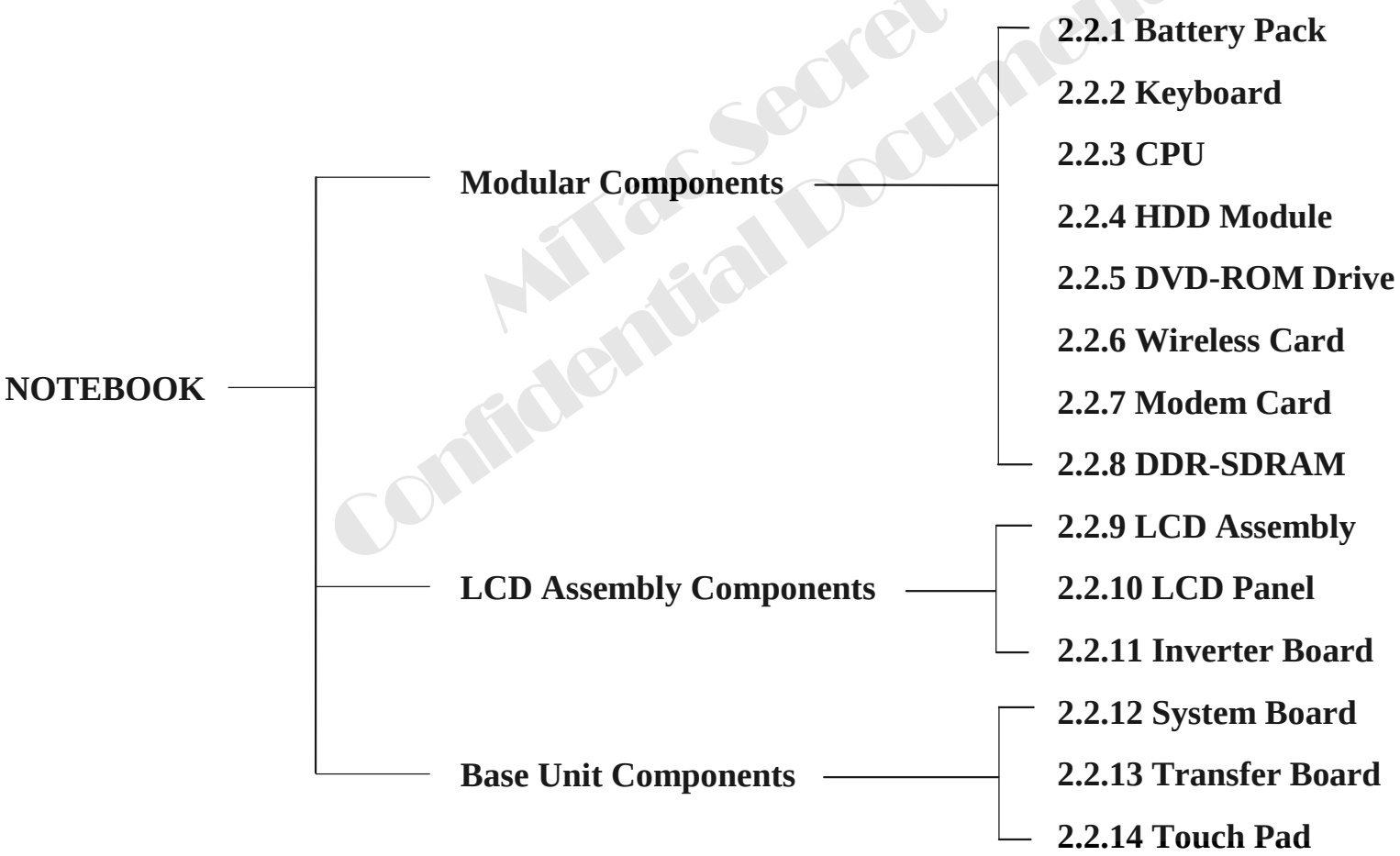
❶ LCD Screen
❷ Keyboard
❸ Device LED indicators
❹ Internal MIC In
❺ Touch Pad
❻ Power Button
❼ Power Indicator
❽ Battery Charge Indicator
❾ Battery Power Indicator



2.2 System Disassembly

The section discusses at length each major component for disassembly/reassembly and show corresponding illustrations.Use the chart below to determine the disassembly sequence for removing components from the notebook.

NOTE: *Before you start to install/replace these modules, disconnect all peripheral devices and make sure the notebook is not turned on or connected to AC power.*



2.2.1 Battery Pack

Disassembly

1. Carefully put the notebook upside down.
2. Slide the two release lever outwards to the "unlock" ( ) position (❶), while take the battery pack out of the compartment (❷). (Figure 2-1)

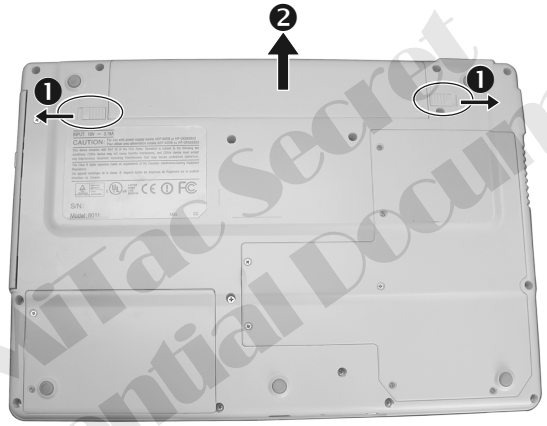


Figure 2-1 Remove the battery pack

Reassembly

1. Replace the battery pack into the compartment. The battery pack should be correctly connected when you hear a clicking sound.
2. Slide the release lever to the "lock" ( ) position.

2.2.2 Keyboard

Disassembly

1. Remove the battery pack. (Refer to section 2.2.1 Disassembly)
2. Push the keyboard cover to loose the locks from the battery compartment. (Figure 2-2)
3. Lift the keyboard cover up. (Figure 2-3)

Figure 2-2 Push the keyboard cover

Figure 2-3 Lift the keyboard cover

4. Slightly lift up the keyboard. (Figure 2-4)
5. Disconnect the cable from the system board, then separate the keyboard. (Figure 2-5)

Figure 2-4 Lift the keyboard

Figure 2-5 Disconnect the cable

Reassembly

1. Reconnect the keyboard cable and fit the keyboard back into place.
2. Replace the keyboard cover.
3. Replace the battery pack. (Refer to section 2.2.1 Reassembly)

2.2.3 CPU

Disassembly

1. Remove the battery pack. (Refer to section 2.2.1 Disassembly)
2. Remove the seven screws fastening the CPU cover. (Figure 2-6)
3. Remove the four spring screws that secure the heatsink upon the CPU and disconnect the fan's power cord from system board. (Figure 2-7)

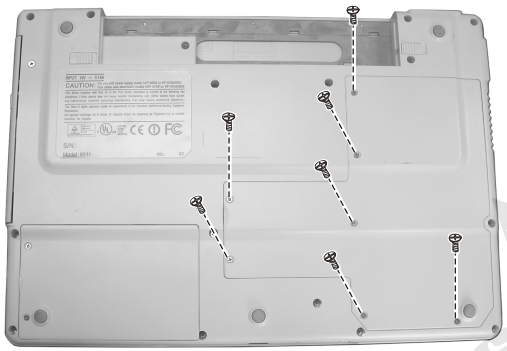


Figure 2-6 Remove the seven screws

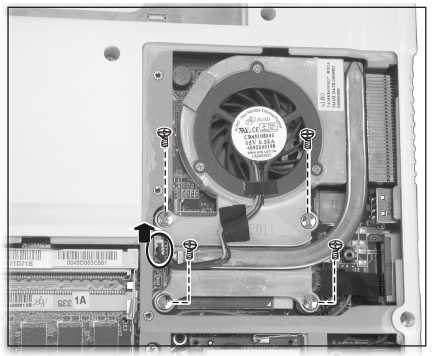


Figure 2-7 Free the heatsink

4. To remove the existing CPU, loosen the screw by a flat screwdriver,upraise the CPU socket to unlock the CPU. (Figure 2-8)

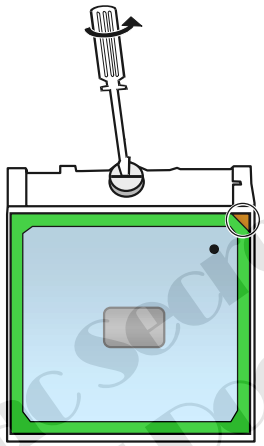


Figure 2-8 Remove the CPU

Reassembly

1. Carefully, align the arrowhead corner of the CPU with the beveled corner of the socket, then insert CPU pins into the holes. Tighten the screw by a flat screwdriver to locking the CPU.
2. Connect the fan's power cord to the system board, fit the heatsink upon the CPU and secure with four spring screws.
3. Replace the CPU cover and secure with seven screws.
4. Replace the battery pack. (Refer to section 2.2.1 Reassembly)

2.2.4 HDD Module

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (Refer to section 2.2.1 Disassembly)
2. Remove the two screws fastening the HDD compartment cover. (Figure 2-9)
3. Remove the one screw and slide the HDD module out of the compartment. (Figure 2-10)

Figure 2-9 Remove the HDD compartment cover

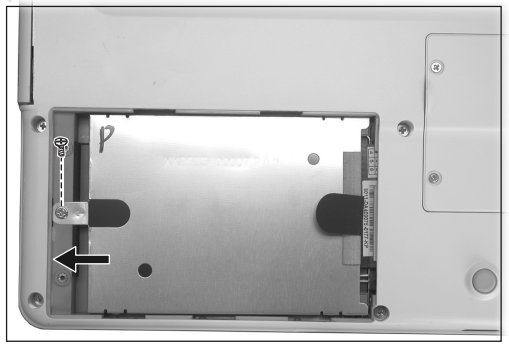


Figure 2-10 Remove HDD module

4. Remove the four screws to separate the hard disk drive from the bracket, remove the hard disk drive. (Figure 2-11)

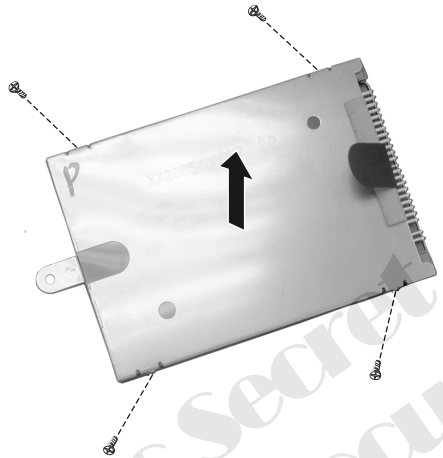


Figure 2-11 Remove hard disk drive

Reassembly

1. Attach the bracket to hard disk drive and secure with four screws.
2. Slide the HDD module into the compartment and secure with one screw.
3. Place the HDD compartment cover and secure with two screws.
4. Replace the battery pack. (Refer to section 2.2.1 Reassembly)

2.2.5 CD/DVD-ROM Drive

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (Refer to section 2.2.1 Disassembly)
2. Remove the one screw fastening the CD/DVD-ROM drive. (Figure 2-12)
3. Insert a small rod, such as a straightened paper clip, into CD/DVD-ROM drive's manual eject hole (❶) and push firmly to release the tray. Then gently pull out the CD/DVD-ROM drive by holding the tray that pops out (❷). (Figure 2-12)

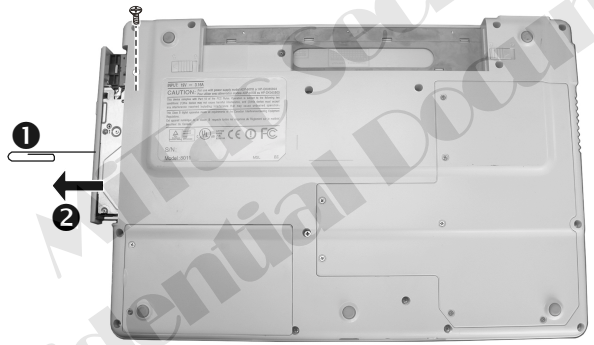


Figure 2-12 Remove the CD/DVD-ROM drive

Reassembly

1. Push the CD/DVD-ROM drive into the compartment and secure with one screw.
2. Replace the battery pack. (Refer to section 2.2.1 Reassembly)

2.2.6 Wireless Card

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (Refer to sections 2.2.1 Disassembly)
2. Remove the seven screws fastening the CPU cover. (Refer to step 2 of section 2.2.3 Disassembly)
3. Disconnect the wireless card's antennae first (❶). Then pull the retaining clips outwards (❷) and remove the wireless card (❸). (Figure 2-13)

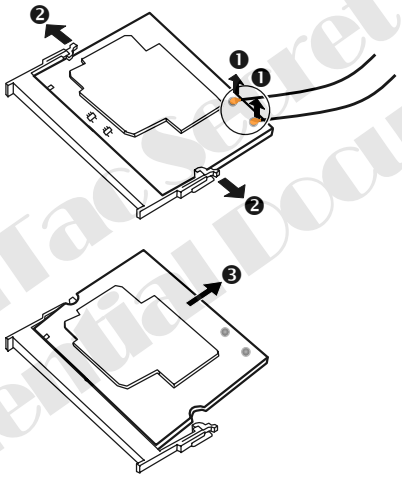


Figure 2-13 Remove the Wireless card

Reassembly

1. To install the wireless card, match the wireless card 's notched part with the socket's projected part and firmly insert it into the socket. Then push down until the retaining clips lock the wireless card into position. Then sure that the antennae fully populated.
2. Replace the CPU cover and secure with seven screws. (Refer to step 3 of section 2.2.3 Reassembly)
3. Replace the battery pack. (Refer to section 2.2.1 Reassembly)

2.2.7 Modem Card

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (Refer to section 2.2.1 Disassembly)
2. Remove the seven screws fastening the CPU cover. (Refer to step 2 of section 2.2.3 Disassembly)
3. Remove the two screws fastening the modem card. (Figure 2-14)
4. Lift up the modem card and disconnect the cord. (Figure 2-15)

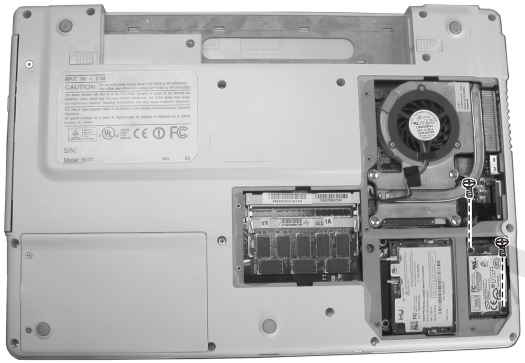


Figure 2-14 Remove the two screws

Figure 2-15 Disconnect the cord

Reassembly

1. Reconnect the cord and fit the modem card.
2. Fasten the modem card by two screws.
3. Replace the CPU cover and secure with seven screws. (Refer to step 3 of section 2.2.3 Reassembly)
4. Replace the battery pack. (Refer to section 2.2.1 Reassembly)

2.2.8 DDR-SDRAM

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (See section 2.2.1 Disassembly)
2. Remove the seven screws fastening the CPU cover. (Refer to step 2 of section 2.2.3 Disassembly)

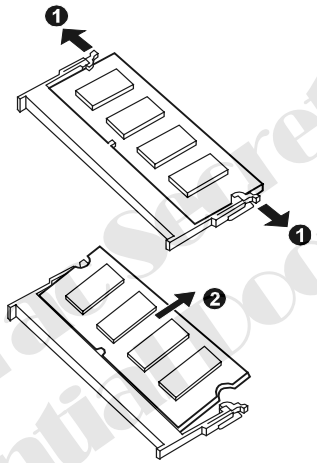


Figure 2-16 Remove the SO-DIMM

3. Pull the retaining clips outwards (❶) and remove the SO-DIMM (❷). (Figure 2-16)

Reassembly

1. To install the DDR, match the DDR's notched part with the socket's projected part and firmly insert the SO-DIMM into the socket at 20-degree angle. Then push down until the retaining clips lock the DDR into position.
2. Replace the CPU cover and secure with seven screws. (Refer to step 3 of section 2.2.3 Reassembly)
3. Replace the battery pack. (See section 2.2.1 Reassembly)

2.2.9 LCD ASSY

Disassembly

1. Remove the battery pack, keyboard, CPU and wireless card. (See sections 2.2.1,2.2.2, 2.2.3 and 2.2.6 Disassembly)
2. Remove the two screws fastening the hinge covers. (Figure 2-17)
3. Remove the two hinge covers, then carefully pull the antenna wires out. (Figure 2-18)

Figure 2-17 Remove the two screws

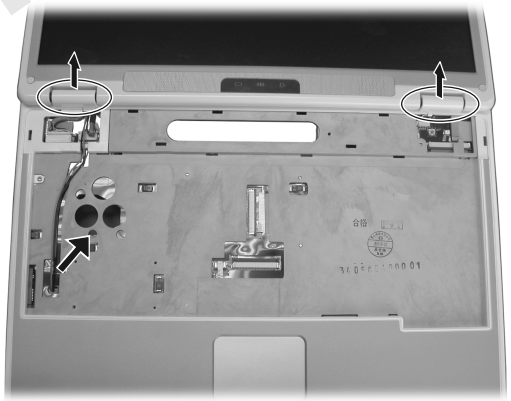


Figure 2-18 Remove the two hinge covers

4. Disconnect the three cables from the motherboard. (Figure 2-19)
5. Remove the four screws, then free the LCD assembly. (Figure 2-20)

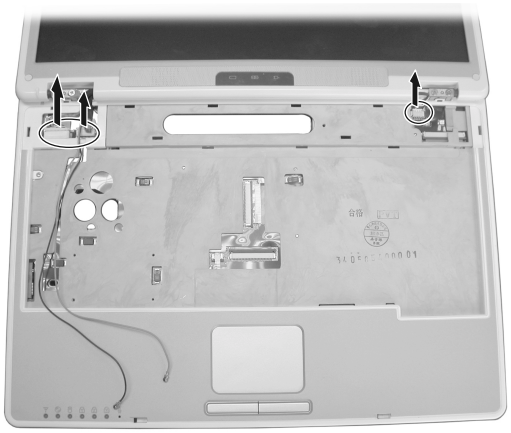


Figure 2-19 Disconnect the three cables

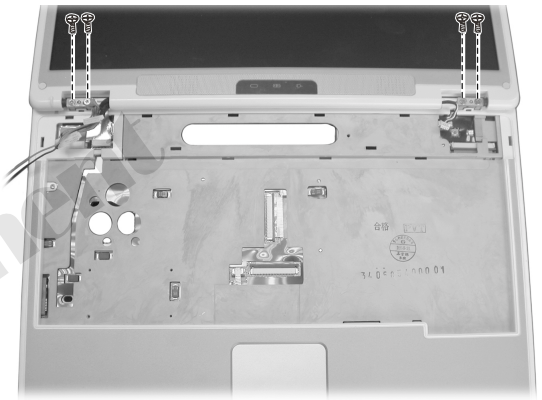


Figure 2-20 Free the LCD assembly

Reassembly

1. Attach the LCD assembly to the base unit and secure with four screws.
2. Replace the antenna wires back into Mini PCI compartment.
3. Reconnect the three cables to the system board. Screw the hinge covers by two screws.
4. Replace the wireless card, CPU, keyboard and battery pack. (Refer to sections 2.2.6, 2.2.3, 2.2.2 and 2.2.1 Reassembly)

2.2.10 LCD Panel

Disassembly

1. Remove the battery, keyboard, CPU, wireless card and LCD assembly. (Refer to section 2.2.1, 2.2.2, 2.2.3, 2.2.6 and 2.2.9 Disassembly)
2. Remove the two rubber pads and two screws on the corners of the panel. (Figure 2-21)
3. Insert a flat screwdriver to the lower part of the LCD cover and gently pry the frame out. Repeat the process until the cover is completely separated from the housing.
4. Remove the eight screws and disconnect the cable. (Figure 2-22)

Figure 2-21 Remove LCD cover

Figure 2-22 Remove the eight screws and disconnect the cable

5. Remove the four screws that secure the LCD brackets. (Figure 2-23)
6. Disconnect the cable to free the LCD panel. (Figure 2-24)

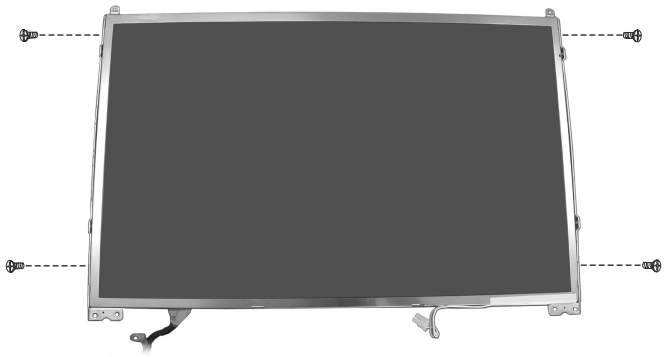


Figure 2-23 Remove the four screws

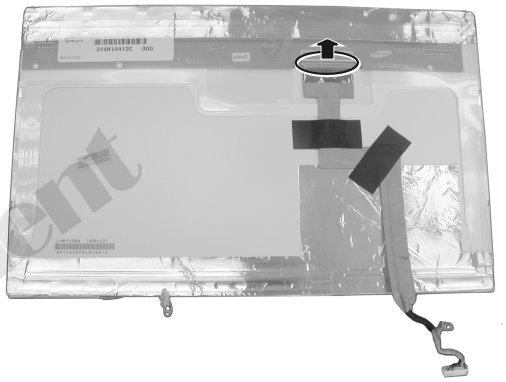


Figure 2-24 Free the LCD panel

Reassembly

1. Replace the cable to the LCD panel.
2. Attach the LCD panel's brackets back to LCD panel and secure with four screws.
3. Replace the LCD panel into LCD housing. And reconnect one cable to inverter board.
4. Fasten the LCD panel by eight screws.
5. Fit the LCD cover and secure with two screws and rubber pads.
6. Replace the LCD assembly, wireless card, CPU, keyboard and battery pack. (See sections 2.2.9, 2.2.6, 2.2.3, 2.2.2 and 2.2.1 Reassembly)

2.2.11 Inverter Board

Disassembly

1. Remove the battery, keyboard, CPU, wireless card and LCD assembly. (Refer to section 2.2.1, 2.2.2, 2.2.3, 2.2.6 and 2.2.9 Disassembly)
2. Remove the LCD cover. (Refer to the steps 1-3 of section 2.2.10 Disassembly)
3. Remove the two screws fastening the inverter board and disconnect the cable, then free the inverter board. (Figure 2-25)

Figure 2-25 Free the inverter board

Reassembly

1. Reconnect the cable. Fit the inverter board back into place and secure with two screws.
2. Replace the LCD cover. (Refer to section 2.2.10 Reassembly)
3. Replace the LCD assembly. (Refer to section 2.2.9 Reassembly)
4. Replace the wireless card, CPU, keyboard and battery pack. (Refer to sections 2.2.6, 2.2.3, 2.2.2 and 2.2.1 Reassembly)

2.2.12 System Board

Disassembly

1. Remove the battery, keyboard, CPU, hard disk drive, CD/DVD-ROM drive, wireless card and LCD assembly. (Refer to sections 2.2.1, 2.2.2, 2 .2.3, 2.2.4, 2.2.5, 2.2.6 and 2.2.9 Disassembly)
2. Disconnect the touch pad's cable and the transfer board's cable from the system board. (Figure 2-26)
3. Remove the one screw fastening the housing. (Figure 2-27)

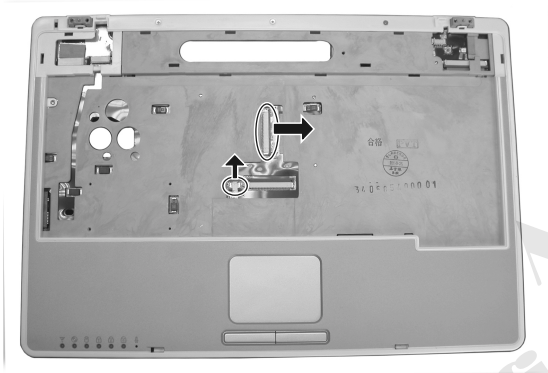


Figure 2-26 Disconnect the two cables

Figure 2-27 Remove the one screw

4. Remove the twenty-one screws fastening the housing, then free the housing. (Figure 2-28)
5. Remove the four screws fastening the system board, then free the system board. (Figure 2-29)

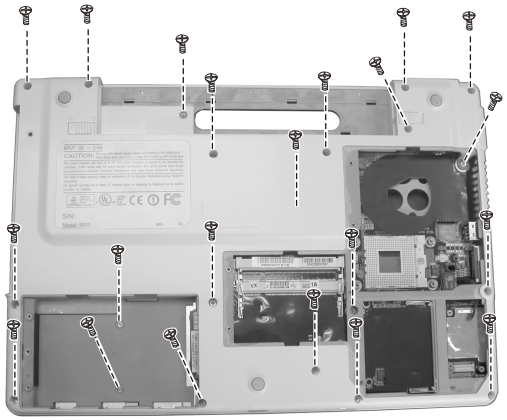


Figure 2-28 Free the housing

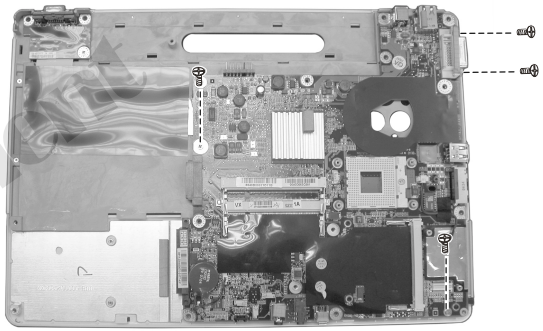


Figure 2-29 Free the system board

Reassembly

1. Replace the system board back into the top cover and secure with four screws .
2. Replace the housing and secure with twenty-two screws.
3. Turn over the base unit, then reconnect the touch pad's cable and the transfer board's cable.
4. Replace the LCD assembly, wireless card, CD/DVD-ROM, hard disk drive, CPU, keyboard and battery pack. (Refer to previous section reassembly)

2.2.13 Transfer Board

Disassembly

1. Remove the battery, keyboard, CPU, hard disk drive, CD/DVD-ROM drive, wireless card, LCD assembly and the system board. (Refer to sections 2.2.1, 2.2.2, 2 .2.3, 2.2.4, 2.2.5, 2.2.6, 2.2.9 and 2.2.12 Disassembly)
2. Remove the three screws, then free the transfer board. (Figure 2-30)

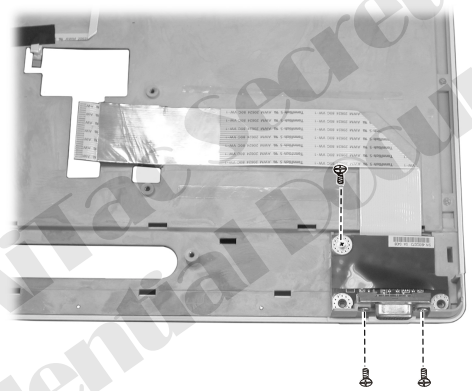


Figure 2-30 Free the transfer board

Reassembly

1. Replace the transfer board back into the top cover and secure with three screws .
2. Replace the system board, LCD assembly, wireless card, CD/DVD-ROM, hard disk drive, CPU, keyboard and battery pack. (Refer to previous section reassembly)

2.2.14 Touch Pad

Disassembly

1. Remove the battery pack, keyboard, CPU, hard disk drive, CD/DVD-ROM drive, wireless card, LCD assembly, the system board and the transfer board. (See sections 2.2.1, 2.2.2, 2.2.3, 2.2.4, 2.2.5, 2.2.6, 2.2.9, 2.2.12 and 2.2.13 Disassembly)
2. Remove the three screws fastening the top cover. (Figure 2-31)
3. Remove the four screws and free the IO bracket. (Figure 2-32)

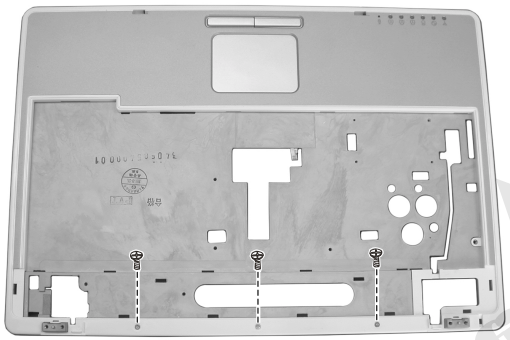


Figure 2-31 Remove the three screws

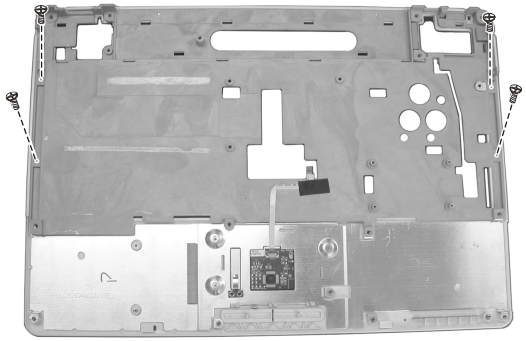


Figure 2-32 Free the IO bracket

4. Remove the three screws fastening the shielding, then free the touch pad. (Figure 2-33)

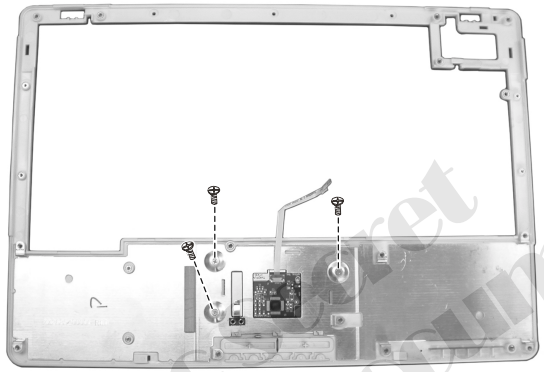


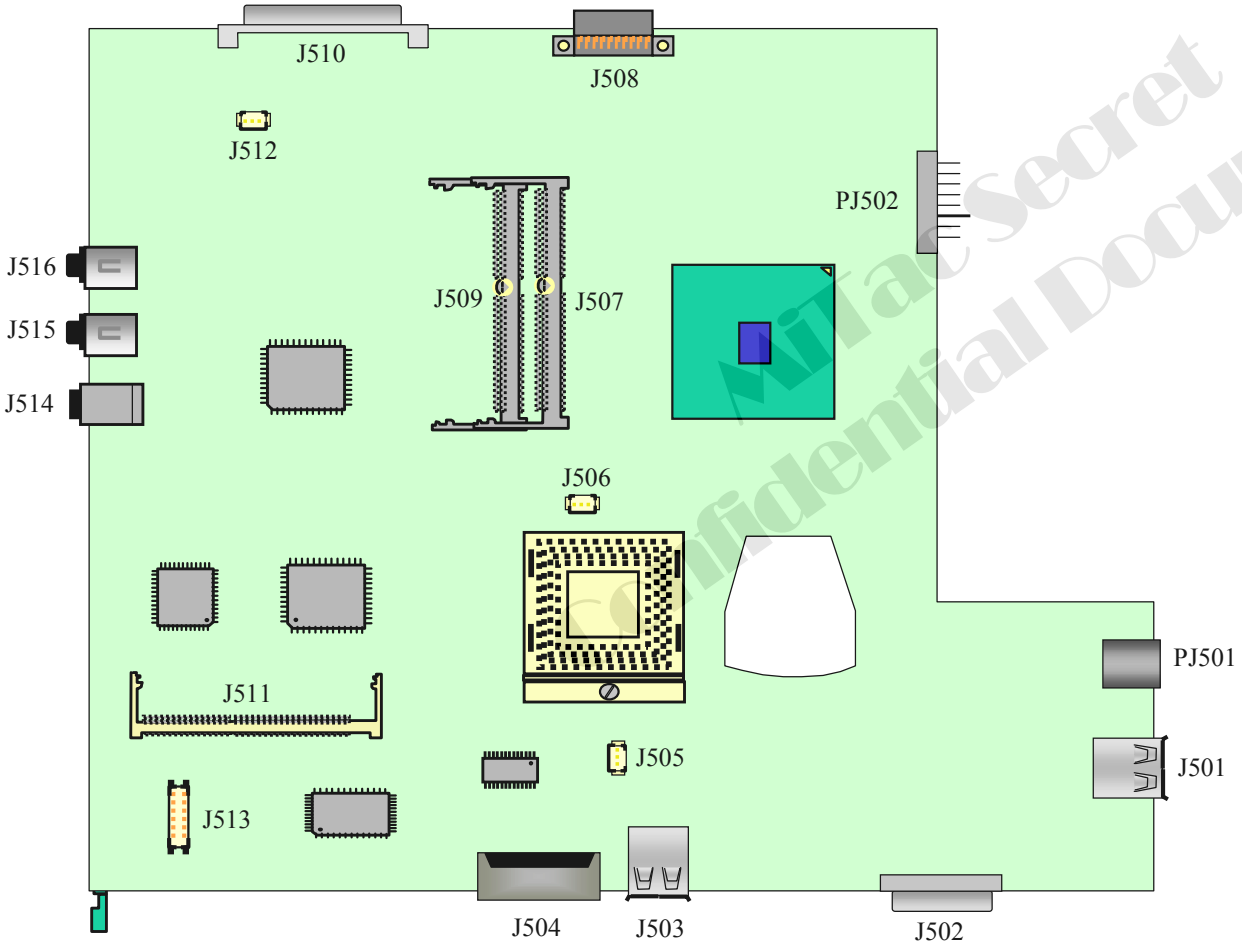
Figure 2-33 Free the touch pad

Reassembly

1. Replace the touch pad, then fit the shielding and secure with three screws.
2. Replace the IO bracket back into the top cover and secure with seven screws.
3. Replace the battery pack, keyboard, CPU, hard disk drive, CD/DVD-ROM drive, wireless card, LCD assembly, the system board and the transfer board. (See sections previous section reassembly)

3. Definition & Location of Connectors / Switches

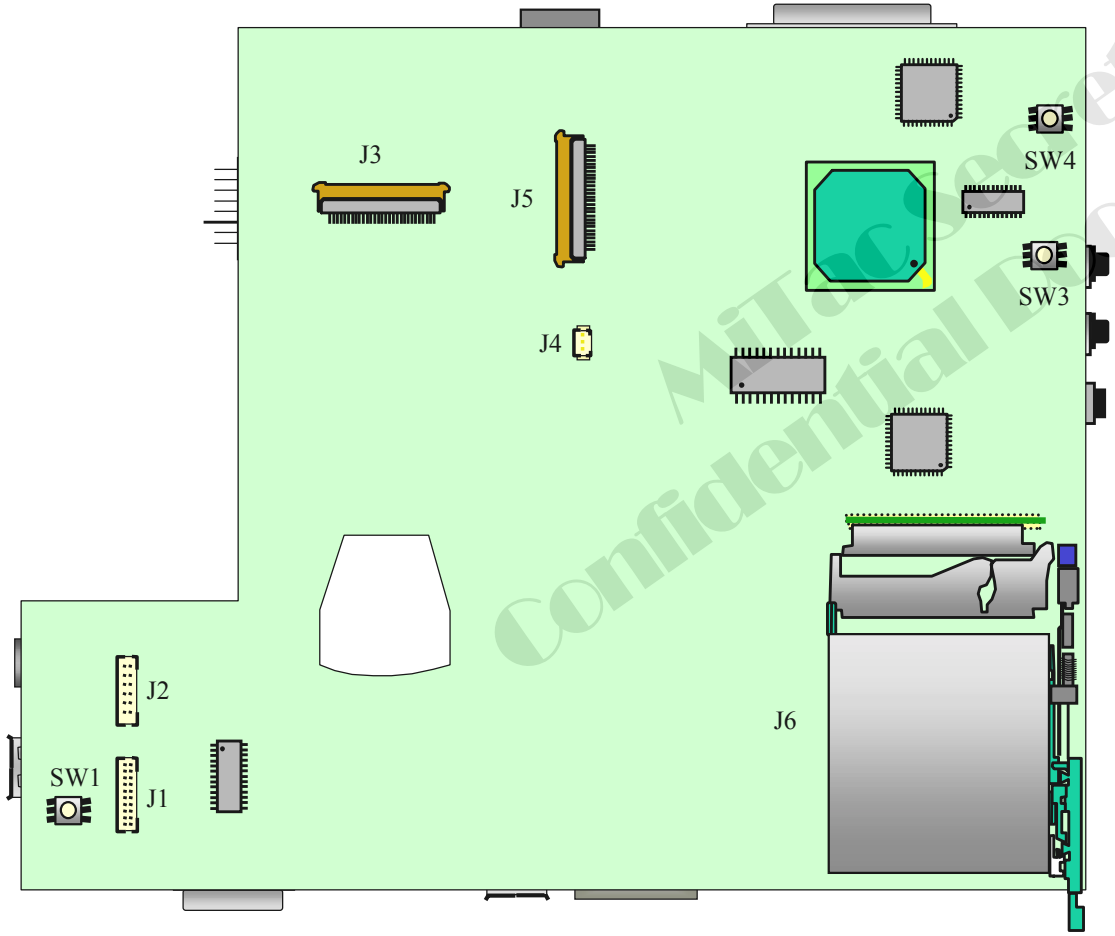
3.1 Main Board (Side A)



- J501,J503 : USB Port Connector
- J502 : DVI-D Connector
- J504 : RJ11 & RJ45 Connector
- J505 : MDC Jump Wire Connector
- J506 : CPU Fan Connector
- J507,J509 : Extend DDR SDRAM Socket
- J508 : Secondary EIDE Connector
- J510 : Primary EIDE Connector
- J511 : Mini PCI Socket
- J512 : RTC Battery Connector
- J513 : MDC Board Connector
- J514 : IEEE 1394 Connector
- J515 : SPDIF Out Jack
- J516 : MIC In Jack
- PJ501 : Power Connector
- PJ502 : Battery Connector

3. Definition & Location of Connectors/ Switches

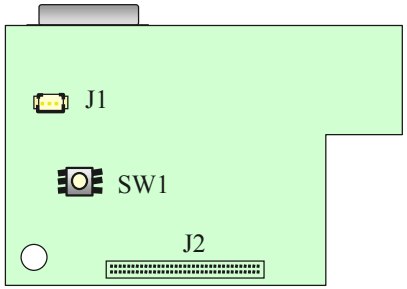
3.1 Main Board (Side B)



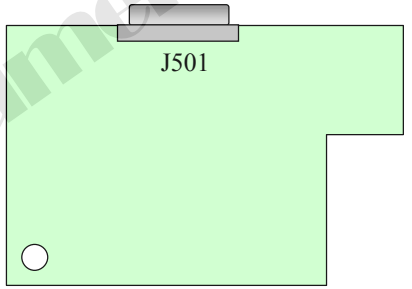
- J1 : LCD Connector
- J2 : LCD Inverter Board Connector
- J3 : Transmitter Board Connector
- J4 : Touch-Pad Connector
- J5 : Internal Keyboard Connector
- J6 : PCMCIA/CARDBUS Slot
- SW1 : Cover Switch Button
- SW3 : Touch-Pad Left Button
- SW4 : Touch-Pad Right Button

3. Definition & Location of Connectors / Switches

3.2 Transmitter Board



SIDE A

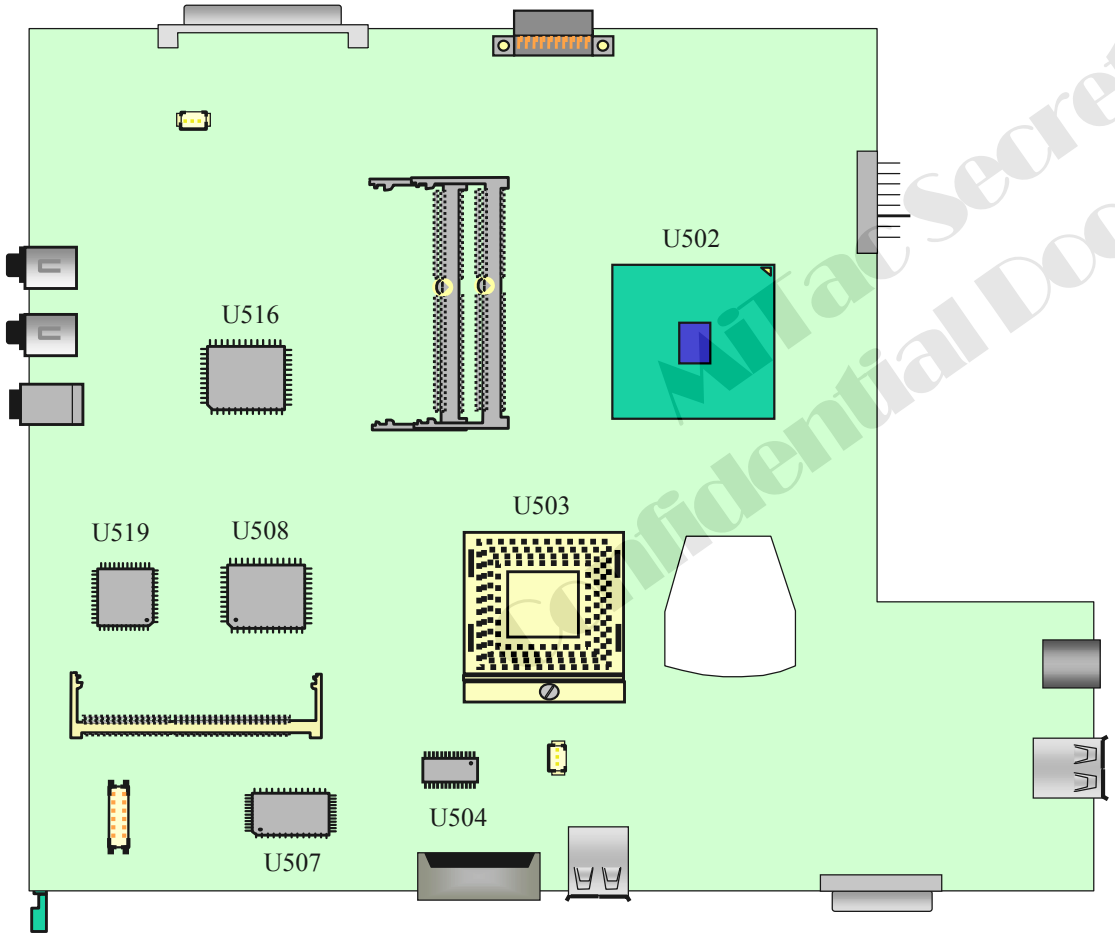


SIDE B

- J1 : Internal Speaker Connector
- J2 : Transmitter Board Connector
- SW1 : Power Button
- J501 : External VGA Connector

4. Definition & Location of Major Components

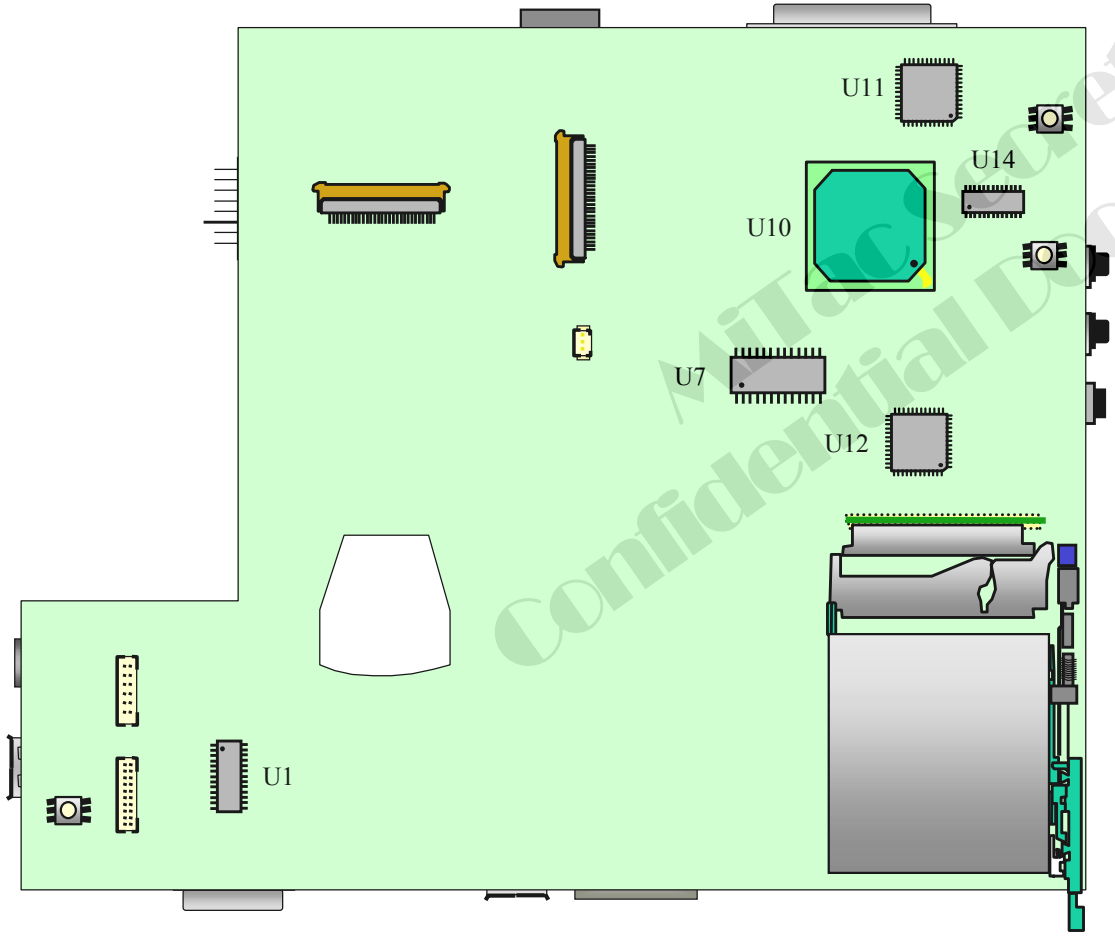
4.1 Main Board (Side A)



- U502 : Intel 855GME
- U503 : Intel Banias Processor Socket
- U504 : LF-H80P
- U507 : RTL8100CL LAN Controller
- U508 : CB1410 CardBus Controller
- U516 : SIO W83L517D
- U519 : VIA VT6301S IEEE1394 Controller

4. Definition & Location of Major Components

4.1 Main Board (Side B)



- U1 : SII1162 DVI-D Transmitter
- U7 : ICS950812 Clock Synthesizer
- U10 : Intel 82801DBM I/O Controller Hub
- U11 : WINBOND W83L950D Keyboard BIOS
- U12 : SST49LF004A System BIOS
- U14 : TPA0212 Audio Amplifier

5. Pin Descriptions of Major Components

5.1 Intel Banias Pentium M Processor-1

Signal Name	Type	Description
A[31:3]#	I/O	A[31:3]# (Address) define a 2 32 -byte physical memory address space. In sub-phase 1 of the address phase, these pins transmit the address of a transaction. In sub-phase 2, these pins transmit transaction type information. These signals must connect the appropriate pins of both agents on the Intel Pentium M processor system bus. A[31:3]# are source synchronous signals and are latched into the receiving buffers by ADSTB[1:0]#. Address signals are used as straps which are sampled before RESET# is deasserted.
A20M#	I	If A20M# (Address-20 Mask) is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-Mbyte boundary. Assertion of A20M# is only supported in real mode. A20M# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.
ADS#	I/O	ADS# (Address Strobe) is asserted to indicate the validity of the transaction address on the A[31:3]# and REQ[4:0]# pins. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction.
ADSTB[1:0]#	I/O	Address strobes are used to latch A[31:3]# and REQ[4:0]# on their rising and falling edges. Strobes are associated with signals as shown below. Signals / Associated Strobe REQ[4:0]#, A[16:3]# / ADSTB[0]# A[31:17]# / ADSTB[1]#
BCLK[1:0]	I	The differential pair BCLK (Bus Clock) determines the system bus frequency. All processor system bus agents must receive these signals to drive their outputs and latch their inputs.
BNR#	I/O	BNR# (Block Next Request) is used to assert a bus stall by any bus agent that is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions.
BPM[2:0]# **BPM[3]**	O I/O	BPM[3:0]# (Breakpoint Monitor) are breakpoint and performance monitor signals. They are outputs from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance. BPM[3:0]# should connect the appropriate pins of all Intel Pentium M processor system bus agents. This includes debug or performance monitoring tools.

Signal Name	Type	Description
BPRI#	I	BPRI# (Bus Priority Request) is used to arbitrate for ownership of the processor system bus. It must connect the appropriate pins of both processor system bus agents. Observing BPRI# active (as asserted by the priority agent) causes the other agent to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed, then releases the bus by deasserting BPRI#.
BR0#	I/O	BR0# is used by the processor to request the bus. The arbitration is done between the Intel Pentium M processor (Symmetric Agent) and the MCH-M (High Priority Agent) of the Intel 855PM or Intel 855GM chipset.
COMPP3:0]	Analog	COMP[3:0] must be terminated on the system board using precision (1% tolerance) resistors. Refer to the platform design guides for more implementation details.
D[63:0]#	I/O	D[63:0]# (Data) are the data signals. These signals provide a 64-bit data path between the processor system bus agents, and must connect the appropriate pins on both agents. The data driver asserts DRDY# to indicate a valid data transfer. D[63:0]# are quad-pumped signals and will thus be driven four times in a common clock period. D[63:0]# are latched off the falling edge of both DSTBP[3:0]# and DSTBN[3:0]#. Each group of 16 data signals correspond to a pair of one DSTBP# and one DSTBN#. The following table shows the grouping of data signals to data strobes and DINV#. **Quad-Pumped Signal Groups** Data Group / DSTBN#/DSTBP# / DINV# D[15:0]# / 0 / 0 D[31:16]# / 1 / 1 D[47:32]# / 2 / 2 D[63:48]# / 3 / 3 Furthermore, the DINV# pins determine the polarity of the data signals. Each group of 16 data signals corresponds to one DINV# signal. When the DINV# signal is active, the corresponding data group is inverted and therefore sampled active high.
DBR#	O	DBR# (Data Bus Reset) is used only in processor systems where no debug port is implemented on the system board. DBR# is used by a debug port interposer so that an in-target probe can drive system reset. If a debug port is implemented in the system, DBR# is a no connect. DBR# is not a processor signal.

5.1 Intel Banias Pentium M Processor-2

<table>
<tr><th>Signal Name</th><th>Type</th><th>Description</th></tr>
<tr><td>DBSY#</td><td>I/O</td><td>DBSY# (Data Bus Busy) is asserted by the agent responsible for driving data on the processor system bus to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted. This signal must connect the appropriate pins on both processor system bus agents.</td></tr>
<tr><td>DEFER#</td><td>I</td><td>DEFER# is asserted by an agent to indicate that a transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or Input/Output agent. This signal must connect the appropriate pins of both processor system bus agents.</td></tr>
<tr><td>DINV[3:0]#</td><td>I/O</td><td>DINV[3:0]# (Data Bus Inversion) are source synchronous and indicate the polarity of the D[63:0]# signals. The DINV[3:0]# signals are activated when the data on the data bus is inverted. The bus agent will invert the data bus signals if more than half the bits, within the covered group, would change level in the next cycle.
DINV[3:0]# Assignment To Data Bus
<table>
<tr><th>Bus Signal</th><th>Data Bus Signals</th></tr>
<tr><td>DINV[3]#</td><td>D[63:48]#</td></tr>
<tr><td>DINV[2]#</td><td>D[47:32]#</td></tr>
<tr><td>DINV[1]#</td><td>D[31:16]#</td></tr>
<tr><td>DINV[0]#</td><td>D[15:0]#</td></tr>
</table></td></tr>
<tr><td>DPSLP#</td><td>I</td><td>DPSLP# when asserted on the platform causes the processor to transition from the Sleep state to the Deep Sleep state. In order to return to the Sleep state, DPSLP# must be deasserted. DPSLP# is driven by the ICH4-M component and also connects to the MCH-M component of the Intel 855PM or Intel 855GM chipset.</td></tr>
<tr><td>DRDY#</td><td>I/O</td><td>DRDY# (Data Ready) is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-common clock data transfer, DRDY# may be deasserted to insert idle clocks. This signal must connect the appropriate pins of both processor system bus agents.</td></tr>
<tr><td>DSTBN[3:0]#</td><td>I/O</td><td>Data strobe used to latch in D[63:0]#.
<table>
<tr><th>Signals</th><th>Associated Strobe</th></tr>
<tr><td>D[15:0]#, DINV[0]#</td><td>DSTBN[0]#</td></tr>
<tr><td>D[31:16]#, DINV[1]#</td><td>DSTBN[1]#</td></tr>
<tr><td>D[47:32]#, DINV[2]#</td><td>DSTBN[2]#</td></tr>
<tr><td>D[63:48]#, DINV[3]#</td><td>DSTBN[3]#</td></tr>
</table></td></tr>
<tr><td>DSTBP[3:0]#</td><td>I/O</td><td>Data strobe used to latch in D[63:0]#.
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</table></td></tr>
</table>

<table>
<tr><th>Signal Name</th><th>Type</th><th>Description</th></tr>
<tr><td>DPWR#</td><td>I</td><td>DPWR# is a control signal from the Intel 855PM and Intel 855GM chipsets used to reduce power on the Intel Pentium M data bus input buffers.</td></tr>
<tr><td>FERR#/PBE#</td><td>O</td><td>FERR# (Floating-point Error)/PBE#(Pending Break Event) is a multiplexed signal and its meaning is qualified by STPCLK#. When STPCLK# is not asserted, FERR#/PBE# indicates a floating point when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel 80387 coprocessor, and is included for compatibility with systems using MS-DOS* type floating-point error reporting. When STPCLK# is asserted, an assertion of FERR#/PBE# indicates that the processor has a pending break event waiting for service. The assertion of FERR#/PBE# indicates that the processor should be returned to the Normal state. When FERR#/PBE# is asserted, indicating a break event, it will remain asserted until STPCLK# is deasserted. Assertion of PREQ# when STPCLK# is active will also cause an FERR# break event.</td></tr>
<tr><td>GTLREF</td><td>I</td><td>GTLREF determines the signal reference level for AGTL+ input pins. GTLREF should be set at 2/3 V_{CCP}. GTLREF is used by the AGTL+ receivers to determine if a signal is a logical 0 or logical 1.</td></tr>
<tr><td>HIT#
HITM#</td><td>I/O
I/O</td><td>HIT# (Snoop Hit) and HITM# (Hit Modified) convey transaction snoop operation results. Either system bus agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.</td></tr>
<tr><td>IERR#</td><td>O</td><td>IERR# (Internal Error) is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the processor system bus. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#, BINIT#, or INIT#.</td></tr>
<tr><td>IGNNE#</td><td>I</td><td>IGNNE# (Ignore Numeric Error) is asserted to force the processor to ignore a numeric error and continue to execute noncontrol floating-point instructions. If IGNNE# is deasserted, the processor generates an exception on a noncontrol floating-point instruction if a previous floating-point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 (CR0) is set.
IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.</td></tr>
<tr><td>REQ[4:0]#</td><td>I/O</td><td>REQ[4:0]# (Request Command) must connect the appropriate pins of both processor system bus agents. They are asserted by the current bus owner to define the currently active transaction type. These signals are source synchronous to ADSTB[0]#.</td></tr>
</table>

5.1 Intel Banias Pentium M Processor-3

Signal Name	Type	Description
INIT#	I	INIT# (Initialization), when asserted, resets integer registers inside the processor without affecting its internal caches or floating-point registers. The processor then begins execution at the power on Reset vector configured during power on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output Write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction. INIT# must connect the appropriate pins of both processor system bus agents. If INIT# is sampled active on the active to inactive transition of RESET#, then the processor executes its Built-in Self-Test (BIST)
LINT[1:0]	I	LINT[1:0] (Local APIC Interrupt) must connect the appropriate pins of all APIC Bus agents. When the APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a nonmaskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium processor. Both signals are asynchronous. Both of these signals must be software configured using BIOS programming of the APIC register space and used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration.
LOCK#	I/O	LOCK# indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins of both processor system bus agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction to the end of the last transaction. When the priority agent asserts BPRI# to arbitrate for ownership of the processor system bus, it will wait until it observes LOCK# deasserted. This enables symmetric agents to retain ownership of the processor system bus throughout the bus locked operation and ensure the atomicity of lock.
PRDY#	O	Probe Ready signal used by debug tools to determine processor debug readiness.
PREQ#	I	Probe Request signal used by debug tools to request debug operation of the processor.
PROCHOT#	O	PROCHOT# (Processor Hot) will go active when the processor temperature monitoring sensor detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit has been activated, if enabled. This signal may require voltage translation on the motherboard.
PSI#	O	Processor Power Status Indicator signal. This signal is asserted when the processor is in a lower state (Deep Sleep and Deeper Sleep).

Signal Name	Type	Description
PWRGOOD	I	PWRGOOD (Power Good) is a processor input. The processor requires this signal as a clean indication that the clocks and power supplies are stable and within their specifications. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD. The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout the boundary scan operation.
ITP_CLK[1:0]	I	ITP_CLK[1:0] are copies of BCLK that are used only in processor systems where no debug port is implemented on the system board. ITP_CLK[1:0] are used as BCLK[1:0] references for a debug port implemented on an interposer. If a debug port is implemented in the system, ITP_CLK[1:0] are no connects. These are not processor signals.
RESET#	I	Asserting the RESET# signal resets the processor to a known state and invalidates its internal caches without writing back any of their contents. For a power-on Reset, RESET# must stay active for at least two milliseconds after VCC and BCLK have reached their proper specifications. On observing active RESET#, both system bus agents will deassert their outputs within two clocks. All processor straps must be valid within the specified setup time before RESET# is deasserted.
RS[2:0]#	I	RS[2:0]# (Response Status) are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of both processor system bus agents.
RSVD	-	These pins are RESERVED and must be left unconnected on the board. However, it is recommended that routing channels to these pins on the board be kept open for possible future use. Please refer to the platform design guides for more details.
SLP#	I	SLP# (Sleep), when asserted in Stop-Grant state, causes the processor to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts. The processor will recognize only assertion of the RESET# signal, deassertion of SLP#, and removal of the BCLK input while in Sleep state. If SLP# is deasserted, the processor exits Sleep state and returns to Stop-Grant state, restarting its internal clock signals to the bus and processor core units. If DPSLP# is asserted while in the Sleep state, the processor will exit the Sleep state and transition to the Deep Sleep state.

5.1 Intel Banias Pentium M Processor-4

Signal Name	Type	Description
SMI#	I	SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, the processor saves the current state and enter System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler. If SMI# is asserted during the deassertion of RESET# the processor will tristate its outputs.
STPCLK#	I	STPCLK# (Stop Clock), when asserted, causes the processor to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the system bus and APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.
TCK	I	TCK (Test Clock) provides the clock input for the processor Test Bus (also known as the Test Access Port).
TDI	I	TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.
TDO	O	TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.
TEST1, TEST2, TEST3	I	TEST1, TEST2, and TEST3 must be left unconnected but should have a stuffing option connection to V SS separately using 1-k, pull-down resisitors.
THERMDA	Other	Thermal Diode Anode.
THERMDC	Other	Thermal Diode Cathode.
THERMTRIP#	O	The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all execution when the junction temperature exceeds approximately 125°C. This is signalled to the system by the THERMTRIP# (Thermal Trip) pin.
TMS	I	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools.
TRDY#	I	TRDY# (Target Ready) is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of both system bus agents.
TRST#	I	TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset.

Signal Name	Type	Description
VCC	I	Processor core power supply.
VCCA[3:0]	I	VCCA provides isolated power for the internal processor core PLL's.
VCCP	I	Processor I/O Power Supply.
VCCQ[1:0]	I	Quiet power supply for on die COMP circuitry. These pins should be connected to VCCP on the motherboard. However, these connections should enable addition of decoupling on the VCCQ lines if necessary.
VCCSENSE	O	VCCSENSE is an isolated low impedance connection to processor core power (VCC). It can be used to sense or measure power near the silicon with little noise.
VID[5:0]	O	VID[5:0] (Voltage ID) pins are used to support automatic selection of power supply voltages (Vcc). Unlike some previous generations of processors, these are CMOS signals that are driven by the Intel Pentium M processor. The voltage supply for these pins must be valid before the VR can supply Vcc to the processor. Conversely, the VR output must be disabled until the voltage supply for the VID pins becomes valid. The VID pins are needed to support the processor voltage specification variations.
VSSSENSE	O	VSSSENSE is an isolated low impedance connection to processor core VSS. It can be used to sense or measure ground near the silicon with little noise.

5.2 Intel 82855GME Graphics and Memory Controller Hub-1

Host Interface Signal Descriptions

Signal Name	Type	Description
ADS#	I/O AGTL+	**Address Strobe:** The system bus owner asserts ADS# to indicate the first of two cycles of a request phase. The GMCH can assert this signal for snoop cycles and interrupt messages.
BNR#	I/O AGTL+	**Block Next Request:** Used to block the current request bus owner from issuing a new request. This signal is used to dynamically control the CPU bus pipeline depth.
BPRI#	O AGTL+	**Bus Priority Request:** The GMCH is the only Priority Agent on the system bus. It asserts this signal to obtain the ownership of the address bus. This signal has priority over symmetric bus requests and will cause the current symmetric owner to stop issuing new transactions unless the HLOCK# signal was asserted.
BREQ0#	I/O AGTL+	**Bus Request 0#:** The GMCH pulls the processor bus BREQ**0#** signal low during **CPURST#.** The signal is sampled by the processor on the active-to-inactive transition of CPURST#. The minimum setup time for this signal is 4 BCLKs. The minimum hold time is 2 clocks and the maximum hold time is 20 BCLKs. BREQ0# should be tristated after the hold time requirement has been satisfied. During regular operation, the GMCH will use BREQ0# as an early indication for FSB Address and Ctl input buffer and sense amp activation.
CPURST#	O AGTL+	**CPU Reset:** The CPURST# pin is an output from the GMCH. The GMCH asserts CPURST# while RESET# (PCIRST# from ICH4-M) is asserted and for approximately 1 ms after RESET# is deasserted. The CPURS**T#** allows the processor to begin execution in a known state. Note that the ICH4-M must provide CPU strap set-up and hold-times around CPURST#. This requires strict synchronization between GMCH, CPURST# deassertion and ICH4-M driving the straps.
DBSY#	I/O AGTL+	**Data Bus Busy:** Used by the data bus owner to hold the data bus for transfers requiring more than one cycle.
DEFER#	O AGTL+	**Defer:** GMCH will generate a deferred response as defined by the rules of the GMCH's Dynamic Defer policy. The GMCH will also use the DEFER# signal to indicate a CPU retry response.

Host Interface Signal Descriptions(Continued)

Signal Name	Type	Description
DINV[3:0]#	I/O AGTL+	**Dynamic Bus Inversion:** Driven along with the HD[63:0]# signals. Indicates if the associated signals are inverted or not. DINV[3:0]# are asserted such that the number of data bits driven electrically low (low voltage) within the corresponding 16-bit group never exceeds 8. **DINV# Data Bits** DINV[3]# HD[63:48]# DINV[2]# HD[47:32]# DINV[1]# HD[31:16]# DINV[0]# HD[16:0]#
DPSLP#	I CMOS	**Deep Sleep #:** This signal comes from the ICH4-M device, providing an indication of C3 and C4 state control to the CPU. Deassertion of this signal is used as an early indication for C3 and C4 wake up (to active HPLL). Note that this is a low-voltage CMOS buffer operating on the FSB VTT power plane.
DRDY#	I/O AGTL+	**Data Ready:** Asserted for each cycle that data is transferred.
HA[31:3]#	I/O AGTL+	**Host Address Bus:** HA[31:3]# connects to the CPU address bus. During processor cycles the HA[31:3]# are inputs. The GMCH drives HA[31:3]# during snoop cycles on behalf of Hub interface. HA[31:3]# are transferred at 2x rate. Note that the address is inverted on the CPU bus.
HADSTB[1:0]#	I/O AGTL+	**Host Address Strobe:** HA[31:3]# connects to the CPU address bus. During CPU cycles, the source synchronous strobes are used to transfer HA[31:3]# and HREQ[4:0]# at the 2x transfer rate. **Strobe Address Bits** HADSTB[0]# HA[16:3]#, HREQ[4:0]# HADSTB[1]# HA[31:17]#
HD[63:0]#	I/O AGTL+	**Host Data:** These signals are connected to the CPU data bus. HD[63:0]# are transferred at 4x rate. Note that the data signals are inverted on the CPU bus.

5.2 Intel 82855GME Graphics and Memory Controller Hub-2

Host Interface Signal Descriptions (Continued)

Signal Name	Type	Description
HDSTBP[3:0]# **HDSTBN[3:0]#**	I/O AGTL+	**Differential Host Data Strobes:** The differential source synchronous strobes are used to **transfer HD[63:0]# and DINV[3:0]# at** the 4x transfer rate. **Strobe Data Bits** HDSTBP[3]#, HDSTBN[3]# HD[63:48]#, DINV[3]# HDSTBP[2]#, HDSTBN[2]# HD[47:32]#, DINV[2]# HDSTBP[1]#, HDSTBN[1]# HD[31:16]#, DINV[1]# HDSTBP[0]#, HDSTBN[0]# HD[15:0]#, DINV[0]#
HIT#	I/O AGTL+	**Hit:** Indicates that a caching agent holds an unmodified version of the requested line. Also, driven in conjunction with HITM# by the target to extend the snoop window.
HITM#	I/O AGTL+	**Hit Modified:** Indicates that a caching agent holds a modified version of the requested line and that this agent assumes responsibility for providing the line. Also, driven in conjunction with HIT# to extend the snoop window.
HLOCK#	I/O AGTL+	**Host Lock:** All CPU bus cycles sampled with the assertion of HLOCK# and ADS#, until the negation of HLOCK# must be atomic, i.e. no Hub interface snoopable access to system memory is allowed when HLOCK# is asserted by the CPU.
HREQ[4:0]#	I/O AGTL+	**Host Request Command:** Defines the attributes of the request. HREQ[4:0]# are transferred at 2x rate. Asserted by the requesting agent during both halves of the Request Phase. In the first half the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second half the signals carry additional information to define the complete transaction type. The transactions supported by the GMCH Host Bridge are defined in the Host Interface section of this document.
HTRDY#	O AGTL+	**Host Target Ready:** Indicates that the target of the processor transaction is able to enter the data transfer phase.
RS[2:0]#	O AGTL+	**Response Status:** Indicates the type of response according to the following the table: **RS[2:0]# Response type** 000 Idle state 001 Retry response 010 Deferred response 011 Reserved (not driven by GMCH) 100 Hard Failure (not driven by GMCH) 101 No data response 110 Implicit Write back 111 Normal data response

DDR SDRAM Interface Descriptions

Signal Name	Type	Description
SCS[3:0]#	O SSTL_2	**Chip Select:** These pins select the particular DDR SDRAM components during the active state. **NOTE:** There is one SCS# per DDR-SDRAM Physical SO-DIMM device row. These signals can be toggled on every rising System Memory Clock edge (SCMDCLK).
SMA[12:0]	O SSTL_2	**Multiplexed Memory Address:** These signals are used to provide the multiplexed row and column address to the DDR SDRAM.
SBA[1:0]	O SSTL_2	**Bank Select (Memory Bank Address):** These signals define which banks are selected within each DDR SDRAM row. The SMA and SBA signals combine to address every possible location within a DDR SDRAM device.
SRAS#	O SSTL_2	**DDR Row Address Strobe: SRAS#** may be heavily loaded and requires tw0 DDR SDRAM clock cycles for setup time to the DDR SDRAMs. Used with SCAS# and SWE# (along with SCS#) to define the system memory commands.
SCAS#	O SSTL_2	**DDR Column Address Strobe:** SCAS# may be heavily loaded and requires two clock cycles for setup time to the DDR SDRAMs. Used with SRAS# and SWE# (along with SCS#) to define the system memory commands.
SWE#	O SSTL_2	**Write Enable:** Used with SCAS# and SRAS# (along with SCS#) to define the DDR SDRAM commands. SWE# is asserted during writes to DDR SDRAM. SWE# may be heavily loaded and requires two clock cycles for setup time to the DDR SDRAMs.
SDQ[71:0]	I/O SSTL_2	**Data Lines:** These signals are used to interface to the DDR SDRAM data bus. **NOTE:** ECC error detection is supported: by the SDQ[71:64] signals.

5.2 Intel 82855GME Graphics and Memory Controller Hub-3

DDR SDRAM Interface Descriptions (Continued)

Signal Name	Type	Description
SDQS[8:0]	I/O SSTL_2	**Data Strobes:** Data strobes are used for capturing data. During writes, SDQS is centered on data. During reads, SDQS is edge aligned with data. The following list matches the data strobe with the data bytes. There is an associated data strobe (DQS) for each data signal (DQ) and check bit (CB) group. SDQS[7] -> SDQ[63:56] SDQS[6] -> SDQ[55:48] SDQS[5] -> SDQ[47:40] SDQS[4] -> SDQ[39:32] SDQS[3] -> SDQ[31:24] SDQS[2] -> SDQ[23:16] SDQS[1] -> SDQ[15:8] SDQS[0] -> SDQ[7:0] **NOTE:** ECC error detection is supported by the SDQS[8] signal.
SCKE[3:0]	O SSTL_2	**Clock Enable:** These pins are used to signal a self-refresh or power down command to the DDR SDRAM array when entering system suspend. SCKE is also used to dynamically power down inactive DDR SDRAM rows. There is one SCKE per DDR SDRAM row. These signals can be toggled on every rising SCK edge.
SMAB[5,4,2,1]	O SSTL_2	**Memory Address Copies:** These signals are identical to SMA[5,4,2,1] and are used to reduce loading for selective CPC(clock-per-command). These copies are not inverted.
SDM[8:0]	O SSTL_2	**Data Mask:** When activated during writes, the corresponding data groups in the DDR SDRAM are masked. There is one SDM for every eight data lines. SDM can be sampled on both edges of the data strobes. **NOTE:** ECC error detection is supported by the SDM[8] signal.
RCVENOUT#	O SSTL_2	**Clock Output:** Reserved, NC.
RCVENIN#	O SSTL_2	**Clock Input:** Reserved, NC.

AGP Addressing Signal Descriptions

Signal Name	Type	Description
GPIPE#	I AGP	**Pipelined Read:** This signal is asserted by the AGP master to indicate a full width address is to be enqueued on by the target using the **AD** bus. One address is placed in the AGP request queue on each rising clock edge while **PIPE#** is asserted. When **PIP**E# is deasserted no new requests are queued across the AD bus. **During SBA Operation:** This signal is **not used** if SBA (Side Band Addressing) is selected. **During FRAME# Operation:** This signal is **not used** during AGP FRAME# operation. **PIPE#** is a sustained tri-state signal from masters (graphics controller), and is an input to the GMCH.
GSBA[7:0]	I AGP	**Side-band Address:** These signals are used by the AGP master (graphics controller) to pass address and command to the GMCH. The **SBA** bus and AD bus operate independently. That is, transactions can proceed on the **SBA** bus and the AD bus simultaneously. **During PIPE# Operation:** These signals are **not used** during PIPE# operation. **During FRAME# Operation:** These signals are **not used** during AGP FRAME# operation. **NOTE:** When sideband addressing is disabled, these signals are isolated (no external/internal pull-ups are required).

5 contains two mechanisms to queue requests by the AGP master. Note that the master can only use one mechanism. The master may not switch methods without a full reset of the system. When PIPE# is used to queue addresses the master isnot allowed to queue addresses using the SBA bus. For example, during configuration time, if the master indicates that it can use either mechanism, the configuration software will indicate which mechanism the master will use. Once this choice has been made, the master will continue to use the mechanism selected until the master is reset (and reprogrammed) to use the other mode. This change of modes is not a dynamic mechanism, but rather a static decision when the device is first being configured after reset

5.2 Intel 82855GME Graphics and Memory Controller Hub-4

AGP Status Signal Descriptions

Signal Name	Type	Description		
GST[2:0]	O AGP	**Status:** Provides information from the arbiter to an AGP Master on what it may do. **ST[2:0]** only have meaning to the master when its **GNT#** is asserted. When **GNT#** is deasserted these signals have no meaning and must be gnored.	**ST[2:0**	**Meaning**
			000	Previously requested low priority read data is being returned to the master arbiter to an AGP
			001	Previously requested high priority read data is being returned to the master
			010	The master is to provide low priority write data for a previously queued write command
			011	The master is to provide high priority write data for a previously queued write command.
			100	Reserved
			101	Reserved
			110	Reserved
			111	The master has been given permission to start a bus transaction. The master may queue AGP requests by asserting **PIPE#** or start a PCI transaction by asserting **FRAME#**

AGP Flow Control Signals

Signal Name	Type	Description
GRBF#	I AGP	**Read Buffer Full:** Read buffer full indicates if the master is ready to accept previously requested low priority read data. When **RBF#** is asserted the GMCH is not allowed to initiate the return low priority read data. That is, the GMCH can finish returning the data for the request currently being serviced. **RBF#** is only sampled at the beginning of a cycle. If the AGP master is always ready to accept return read data then it is not required to implement this signal. **During FRAME# Operation:** This signal is not used during AGP FRAME# operation.
GWBF#	I AGP	**Write-Buffer Full:** indicates if the master is ready to accept Fast Write data from the GMCH. When **WBF#** is asserted the GMCH is not allowed to drive Fast Write data to the AGP master. **WBF#** is only sampled at the beginning of a cycle. If the AGP master is always ready to accept fast write data then it is not required to implement this signal. **During FRAME# Operation:** This signal is not used during AGP FRAME# operation.

5.2 Intel 82855GME Graphics and Memory Controller Hub-5

AGP/PCI Signals-Semantics Descriptions (Continued)

Signal Name	Type	Description
GTRDY#	I/O AGP	**G_TRDY#:** Target Ready. **During PIPE# and SBA Operation:** Not used while enqueueing requests via AGP SBA and PIPE#, but used during the data phase of PIPE# and SBA transactions. **During FRAME# Operation:** G_TRDY# is an input when the GMCH acts as an AGP initiator and is an output when the GMCH acts as a FRAME#-based AGP target. The assertion of G_TRDY# indicates the target's ability to complete the current data phase of the transaction. **During Fast Write Operation:** In Fast Write mode, G_TRDY# indicates the AGP-compliant target is ready to receive write data for the entire transaction (when the transfer size is less than or equal to 32 bytes) or is ready to transfer the initial or subsequent block (32 bytes) of data when the transfer size is greater than 32 bytes. The target is allowed to insert wait states after each block (32 bytes) is transferred on write transactions.
GSTOP#	I/O AGP	**G_STOP#:** Stop. **During PIPE# and SBA Operation:** This signal is not used during PIPE# or SBA operation. **During FRAME# Operation:** G_STOP# is an input when the GMCH acts as a FRAME#-based AGP initiator and is an output when the GMCH acts as a FRAME#-based AGP target. G_STOP# is used for disconnect, retry, and abort sequences on the AGP interface.
GDEVSEL#	I/O AGP	**G_ DEVSEL#: Device Select.** **During PIPE# and SBA Operation:** This signal is not used during PIPE# or SBA operation. **During FRAME# Operation:** G_DEVSEL#, when asserted, indicates that a FRAME#-based AGP target device has decoded its address as the target of the current access. The GMCH asserts G_DEVSEL# based on the DDR SDRAM address range being accessed by a PCI initiator. As an input, G_DEVSEL# indicates whether the AGP master has recognized a PCI cycle to it.
GREQ#	I AGP	**G_REQ#:** Request. **During SBA Operation:** This signal is not used during SBA operation. **During PIPE# and FRAME# Operation:** G_REQ#, when asserted, indicates that the AGP master is requesting use of the AGP interface to run a FRAME#- or PIPE#-based operation.

AGP/PCI Signals-Semantics Descriptions (Continued)

Signal Name	Type	Description
GGNT#	O AGP	**G_GNT#: Grant.** **During SBA, PIPE# and FRAME# Operation:** G_GNT#, along with the information on the ST[2:0] signals (status bus), indicates how the AGP interface will be used next. Refer to the *AGP Interface Specification, Revision 2.0* for further explanation of the ST[2:0] values and their meanings.
GAD[31:0]	I/O AGP	**G_AD[31:0]: Address/Data Bus.** **During PIPE# and FRAME# Operation:** The G_AD[31:0] signals are used to transfer both address and data information on the AGP interface. **During SBA Operation:** The G_AD[31:0] signals are used to transfer data on the AGP interface.
GCBE#[3:0]	I/O AGP	**Command/Byte Enable.** **During FRAME# Operation:** During the address phase of a transaction, the G_CBE[3:0]# signals define the bus command. During the data phase, the G_CBE[3:0]# signals are used as byte enables. The byte enables determine which byte lanes carry meaningful data. The commands issued on the G_CBE# signals during FRAME#-based AGP transactions are the same G_CBE# command described in the PCI 2.2 specification. **During PIPE# Operation:** When an address is enqueued using PIPE#, the C/BE# signals carry command information. The command encoding used during PIPE#-based AGP is *different* than the command encoding used during FRAME#-based AGP cycles (or standard PCI cycles on a PCI bus). **During SBA Operation:** These signals are not used during SBA operation.
GPAR	I/O AGP	**Parity.** **During FRAME# Operation:** G_PAR is driven by the GMCH when it acts as a FRAME#-based AGP initiator during address and data phases for a write cycle, and during the address phase for a read cycle. G_PAR is driven by the GMCH when it acts as a FRAME#-based AGP target during each data phase of a FRAME#-based AGP memory read cycle. Even parity is generated across G_AD[31:0] and G_CBE[3:0]#. **During SBA and PIPE# Operation:** This signal is not used during SBA and PIPE# operation.

PCIRST# from the ICH4-M is assumed to be connected to RSTIN# and is used to reset AGP interface logic within the GMCH. The AGP agent will also typically use PCIRST# provided by the ICH4-M as an input to reset its internal logic.

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AGP/PCI Signals-Semantics Descriptions

Signal Name	Type	Description
GFRAME#	I/O AGP	**G_FRAME:** Frame. **During PIPE# and SBA Operation:** Not used by AGP SBA and PIPE# operations. **During Fast Write Operation:** Used to frame transactions as an output during Fast Writes. **During FRAME# Operation:** G_FRAME# is an output when the GMCH acts as an initiator on the AGP Interface. G_FRAME# is asserted by the GMCH to indicate the beginning and duration of an access. G_FRAME# is an input when the GMCH acts as a FRAME#-based AGP target. As a FRAME#-based AGP target, the GMCH latches the C/BE[3:0]# and the AD[31:0] signals on the first clock edge on which GMCH samples FRAME# active.
GIRDY#	I/O AGP	**G_IRDY#: Initiator Ready.** **During PIPE# and SBA Operation:** Not used while enqueueing requests via AGP SBA and PIPE#, but used during the data phase of PIPE# and SBA transactions. **During FRAME# Operation:** G_IRDY# is an output when GMCH acts as a FRAME#-based AGP initiator and an input when the GMCH acts as a FRAME#-based AGP target. The assertion of G_IRDY# indicates the current FRAME#-based AGP bus initiator's ability to complete the current data phase of the transaction. **During Fast Write Operation:** In Fast Write mode, G_IRDY# indicates that the AGP-compliant master is ready to provide all write data for the current transaction. Once G_IRDY# is asserted for a write operation, the master is not allowed to insert wait states. The master is never allowed to insert a wait state during the initial data transfer (32 bytes) of a write transaction. However, it may insert wait states after each 32-byte block is transferred.

AGP Strobe Descriptions

Signal Name	Type	Description
GADSTB[0]	I/O AGP	**Address/Data Bus Strobe-0:** provides timing for 2x and 4x data on **AD[15:0]** and **C/BE[1:0]#** signals. The agent that is providing the data will drive this signal.
GADSTB#[0]	I/O AGP	**Address/Data Bus Strobe-0 Complement:** With AD STB0, forms a differential strobe pair that provides timing information for the **AD[15:0]** and **C/BE[1:0]#** signals. The agent that is providing the data will drive this signal.
GADSTB[1]	I/O AGP	**Address/Data Bus Strobe-1:** Provides timing for 2x and 4x data on **AD[31:16]** and **C/BE[3:2]#** signals. The agent that is providing the data will drive this signal.
GADSTB#[1]	I/O AGP	**Address/Data Bus Strobe-1 Complement:** With AD STB1, forms a differential strobe pair that provides timing information for the AD[15:0] and C/BE[1:0]# signals in 4X mode. The agent that is providing the data will drive this signal.
GSBSTB	I AGP	**Sideband Strobe:** Provides timing for 2x and 4x data on the **SBA[7:0]** bus. It is driven by the AGP master after the system has been configured for 2x or 4x sideband address mode.
GSBSTB#	I AGP	**Sideband Strobe Complement:** The differential complement to the **SB_STB** signal. It is used to provide timing 4x mode.

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Hub Interface Signals

Signal Name	Type	Description
HL[10:0]	I/O Hub	**Packet Data:** Data signals used for HI read and write operations.
HLSTB	I/O Hub	**Packet Strobe:** One of two differential strobe signals used to transmit or receive packet data over HI.
HLSTB#	I/O Hub	**Packet Strobe Complement**: One of two differential strobe signals used to transmit or receive packet data over HI.

Dedicated LVDS LCD Flat Panel Interface Signal Descriptions

Name	Type	Voltage	Description
ICLKAP	O LVDS	1.25 V± 225 mV	**Channel A differential clock pair output (true):** 245-800 MHz
ICLKAM	O LVDS	1.25 V±225 mV	**Channel A differential clock pair output (compliment):** 245-800 MHz.
IYAP[3:0]	O LVDS	1.25 V±225 mV	**Channel A differential data pair 3:0 output (true):** 245-800MHz.
IYAM[3:0]	O LVDS	1.25 V±225 mV	**Channel A differential data pair 3:0 output (compliment):** 245-800 MHz.
ICLKBP	O LVDS	1.25 V±225 mV	**Channel B differential clock pair output (true):** 245-800 MHz.
ICLKBM	O LVDS	1.25 V±225 mV	**Channel B differential clock pair output (compliment):** 245-800 MHz.
IYBP[3:0]	O LVDS	1.25 V±225 mV	**Channel B differential data pair 3:0 output (true):** 245-800MHz.
IYBM[3:0]	O LVDS	1.25 V± 225 mV	**Channel B differential data pair 3:0 output (compliment):** 245-800 MHz.

Digital Video Output B (DVOB) Port Signal Descriptions

Name	Type	Description
DVOBD[11:0]	O DVO	**DVOB Data:** This data bus is used to drive 12-bit RGB data on each edge of the differential clock signals, DVOBCLK and DVOBCLK#. This provides 24-bits of data per clock period. In dual channel mode, this provides the lower 12-bits of pixel data. DVOBD[11:0] should be left as left as NC (“Not Connected”) if not used.
DVOBHSYNC	O DVO	**Horizontal Sync**: HSYNC signal for the DVOB interface. **DVOBHSYNC** should be left as left as NC (“Not Connected”) if not used.
DVOBVSYNC	O DVO	**Vertical Sync**: VSYNC signal for the DVOB interface. DVOBVSYNC should be left as left as NC (“Not Connected”) if the signal is NOT used when using internal graphics device.
DVOBBLANK#	O DVO	**Flicker Blank or Border Period Indication: DVOBBLANK# is** a programmable output pin driven by the GMCH. When programmed as a blank period indication, this pin indicates active pixels excluding the border. When programmed as a border period indication, this pin indicates active pixel including the border pixels. DVOBBLANK# should be left as left as NC (“Not Connected”) if not used.
DVOBFLDSTL	I DVO	**TV Field and Flat Panel Stall Signa**l. This input can be programmed to be either a TV Field input from the TV encoder or Stall input from the flat panel. DVOB TV Field Signal: When used as a Field input, it synchronizes the overlay field with the TV encoder field when the overlay is displaying an interleaved source. DVOB Flat Panel Stall Signal: When used as the Stall input, it indicates that the pixel pipeline should stall one horizontal line. The signal changes during horizontal blanking. The panel fitting logic, when expanding the image vertically, uses this. DVOBFLDSTL needs to be pulled down if not used.

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DVOB and DVOC Port Common Signal Descriptions

Name	Type	Description
DVOBCINTR#	I DVO	**DVOBC Interrup**t: This pin is used to signal an interrupt, typically used to indicate a hot plug or unplug of a digital display.
ADDID[7:0]	I DVO	**ADDID[7:0]**: These pins are used to communicate to the Video BIOS when an external device is interfaced to the DVO port. **Not**e: Bit[7] needs to be strapped low when an on-board DVO device is present. The other pins should be left as NC.
DVODETECT	I DVO	**DVODETEC**T: This strapping signal indicates to the GMCH whether a DVO device is present or not. When a DVO device is connected, then DVODETECT = 0.

Analog CRT Display Signal Descriptions

Pin Name	Type	Description
VSYNC	O CMOS	**CRT Vertical Synchronizatio**n: This signal is used as the vertical sync signal.
HSYNC	O CMOS	**CRT Horizontal Synchronizatio**n: This signal is used as the horizontal sync signal.
RED	O Analog	**Red (Analog Video Output**): This signal is a CRT Analog video output from the internal color palette DAC. The DAC is designed for a 37.5-§Ù equivalent load on each pin (e.g., 75-§Ù resistor on the board, in parallel with the 75-§Ù CRT load).
RED#	O Analog	**Red# (Analog Output):** Tied to ground.
GREEN	O Analog	**Green (Analog Video Output**): This signal is a CRT analog video output from the internal color palette DAC. The DAC is designed for a 37.5-§Ù equivalent load on each pin (e.g.,75-§Ù resistor on the board, in parallel with the 75- §Ù CRT load).
GREEN#	O Analog	**Green# (Analog Output):** Tied to ground.
BLUE	O Analog	**Blue (Analog Video Output)** : This signal is a CRT Analog video output from the internal color palette DAC. The DAC is designed for a 37.5-§Ù equivalent load on each pin (e.g., 75- ohm resistor on the board, in parallel with the 75-§Ù CRT load).
BLUE#	O Analog	**Blue# (Analog Output):** Tied to ground.

Digital Video Output C (DVOC) Port Signal Descriptions

Name	Type	Description
DVOCD[11:0]	O DVO	**DVOC Dat**a: This data bus is used to drive 12-bit RGB data on each edge of the differential clock signals, DVOCCLK and DVOCCLK#. This provides 24-bits of data per clock period. In dual channel mode, this provides the upper 12-bits of pixel data. DVOCD[11:0] should be left as left as NC (“Not Connected”) if not used.
DVOCHSYNC	O DVO	**Horizontal Sync**: HSYNC signal for the DVOC interface. DVOCHSYNC should be left as left as NC (“Not Connected”) if not used.
DVOCVSYNC	O DVO	**Vertical Sync**: VSYNC signal for the DVOC interface. DVOCVSYNC should be left as left as NC (“Not Connected”) if the signal is NOT used when using internal graphics device.
DVOCBLANK#	O DVO	**Flicker Blank or Border Period Indicatio**n: **DVOCBLANK#** is a programmable output pin driven by the GMCH. When programmed as a blank period indication, this pin indicates active pixels excluding the border. When programmed as a border period indication, this pin indicates active pixel including the border pixels. DVOCBLANK# should be left as left as NC (“Not Connected”) if not used.
DVOCFLDSTL	I DVO	**TV Field and Flat Panel Stall Signa**l. This input can be programmed to be either a TV Field input from the TV encoder or Stall input from the flat panel. DVOC TV Field Signal: When used as a Field input, it synchronizes the overlay field with the TV encoder field when the overlay is displaying an interleaved source. DVOC Flat Panel Stall Signal: When used as the Stall input, it indicates that the pixel pipeline should stall one horizontal line. The signal changes during horizontal blanking. The panel fitting logic, when expanding the image vertically, uses this. DVOCFLDSTL needs to be pulled down if not used.

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GPIO Signal Descriptions

GPIO I/F Total	Type	Comments
RSTIN#	I CMOS	**Reset:** Primary Reset, Connected to PCIRST# of ICH4-M.
PWROK	I CMOS	**Power OK**: Indicates that power to GMCH is stable.
AGPBUSY#	O CMOS	**AGPBUSY:** Output of the GMCH IGD to the ICH4-M, which indicates that certain graphics activity is taking place. It will indicate to the ACPI software not to enter the C3 state. It will also cause a C3/C4 exit if C3/C4 was being entered, or was already entered when AGPBUSY# went active. Not active when the IGD is in any ACPI state other than D0.
EXTTS_0	I CMOS	**External Thermal Sensor Input:** This signal is an active low input to the GMCH and is used to monitor the thermal condition around the system memory and is used for triggering a read throttle. The GMCH can be optionally programmed to send a SERR, SCI, or SMI message to the ICH4-M upon the triggering of this signal.
LCLKCTLA	O CMOS	**SSC Chip Clock Control:** Can be used to control an external clock chip with SSC control.
LCLKCTLB	O CMOS	**SSC Chip Data Control:** Can be used to control an external clock chip for SSC control.
PANELVDDEN	O CMOS	**LVDS LCD Flat Panel Power Control:** This signal is used enable power to the panel interface.
PANELBKLTEN	O CMOS	**LVDS LCD Flat Panel Backlight Enable:** This signal is used to enable the backlight inverter (BLI)
PANELBKLTCTL	O CMOS	**LVDS LCD Flat Panel Backlight Brightness Control:** This signal is used as the Pulse Width Modulated (PWM) control signal to control the backlight inverter.
DDCACLK	I/O CMOS	**CRT DDC Clock:** This signal is used as the DDC clock signal between the CRT monitor and the GMCH.
DDCADATA	I/O CMOS	**CRT DDC Data:** This signal is used as the DDC data signal between the CRT monitor and the GMCH.
DDCPCLK	I/O CMOS	**Panel DDC Clock:** This signal is used as the DDC clock signal between the LFP and the GMCH.
DDCPDATA	I/O CMOS	**Panel DDC Data:** This signal is used as the DDC data signal between the LFP and the GMCH.

GPIO Signal Descriptions(Continued)

GPIO I/F Total	Type	Comments
MI2CCLK	I/O DVO	**DVO I2C Clock:** This signal is used as the I2C_CLK for a digital display (i.e. TV-Out Encoder, TMDS transmitter). This signal is tri-stated during a hard reset.
MI2CDATA	I/O DVO	**DVO I2C Data:** This signal is used as the I2C_DATA for a digital display (i.e. TV-Out Encoder, TMDS transmitter). This signal is tri-stated during a hard reset.
MDVICLK	I/O DVO	**DVI DDC Clock:** This signal is used as the DDC clock for a digital display connector (i.e. primary digital monitor). This signal is tri-stated during a hard reset.
MDVIDATA	I/O DVO	**DVI DDC Data:** The signal is used as the DDC data for a digital display connector (i.e. primary digital monitor). This signal is tri-stated during a hard reset.
MDDCDATA	I/O DVO	**DVI DDC Clock:** The signal is used as the DDC data for a digital display connector (i.e. secondary digital monitor). This signal is tri-stated during a hard reset.
MDDCCLK	I/O DVO	**DVI DDC Data:** The signal is used as the DDC clock for a digital display connector (i.e. secondary digital monitor). This signal is tri-stated during a hard reset.

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Hub Interface Signals

Signal Name	Type	Description
HI[11:0]	I/O	**Hub Interface Signals**
HI_STB/HI_STBS	I/O	**Hub Interface Strobe/ Hub Interface Strobe Second:** One of two differential strobe signals used to transmit and receive data through the hub interface. Hub Interface 1.5 mode this signal is not differential and is the second of the two strobe signals.
HI_STB#/ HI_STBF	I/O	**Hub Interface Strobe Complement / Hub Interface Strobe First:** One of two differential strobe signals used to transmit and receive data through the hub interface. Hub Interface 1.5 mode this signal is not differential and is the first of the two strobe signals.
HICOMP	I/O	**Hub Interface Compensation:** Used for hub interface buffer compensation.
HI_VSWING	I	**Hub Interface Voltage Swing:** Analog input used to control the voltage swing and impedance strength of hub interface pins.

LAN Connect Interface Signals

Signal Name	Type	Description
LAN_CLK	I	**LAN I/F Clock:** Driven by the LAN Connect component. Frequency range is 5 MHz to 50 MHz.
LAN_RXD[2:0]	I	**Received Data:** The LAN Connect component uses these signals to transfer data and control information to the integrated LAN Controller. These signals have integrated weak pull-up resistors.
LAN_TXD[2:0]	O	**Transmit Data**: The integrated LAN Controller uses these signals to transfer data and control information to the LAN Connect component.
LAN_RSTSYNC	O	**LAN Reset/Sync:** The LAN Connect component's Reset and Sync signals are multiplexed onto this pin.

EEPROM Interface Signals

Signal Name	Type	Description
EE_SHCLK	O	**EEPROM Shift Clock**: Serial shift clock output to the EEPROM.
EE_DIN	I	**EEPROM Data In**: Transfers data from the EEPROM to the ICH3. This signal has an integrated pull-up resistor.
EE_DOUT	O	**EEPROM Data Out**: Transfers data from the ICH3 to the EEPROM.
EE_CS	O	**EEPROM Chip Select**: Chip select signal to the EEPROM.

Firmware Hub Interface Signals

Signal Name	Type	Description
FWH[3:0]/ LAD[3:0]	I/O	**Firmware Hub Signals.** Muxed with LPC address signals.
FWH[4]/ LFRAME#	I/O	LFRAME# **Firmware Hub Signals.** Muxed with LPC LFRAME# signal.

PCI Interface Signals

Signal Name	Type	Description
AD[31:0]	I/O	**PCI Address/Data:** AD[31:0] is a multiplexed address and data bus. During the first clock of a transaction, AD[31:0] contain a physical address (32 bits). During subsequent clocks, AD[31:0] contain data. The ICH4 drives all 0s on AD[31:0] during the address phase of all PCI Special Cycles.
C/BE[3:0]#	I/O	**Bus Command and Byte Enables:** The command and byte enable signals are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE[3:0]# define the bus command. During the data phase, C/BE[3:0]# define the Byte Enables. **C/BE[3:0]# Command Type** 0 0 0 0 Interrupt Acknowledge 0 0 0 1 Special Cycle 0 0 1 0 I/O Read 0 0 1 1 I/O Write 0 1 1 0 Memory Read 0 1 1 1 Memory Write 1 0 1 0 Configuration Read 1 0 1 1 Configuration Write 1 1 0 0 Memory Read Multiple 1 1 1 0 Memory Read Line 1 1 1 1 Memory Write and Invalidate All command encodings not shown are reserved. The ICH4 does not decode reserved values, and therefore will not respond if a PCI master generates a cycle using one of the reserved values.
DEVSEL#	I/O	**Device Select:** The ICH4 asserts DEVSEL# to claim a PCI transaction. As an output, the ICH4 asserts DEVSEL# when a PCI master peripheral attempts an access to an internal ICH4 address or an address destined for the hub interface (main memory or AGP). As an input, DEVSEL# indicates the response to an ICH4-initiated transaction on the PCI bus. DEVSEL# is tri-stated from the leading edge of PCIRST#. DEVSEL# remains tri-stated by the ICH4 until driven by a Target device.

5.3 Intel 82801DBM I/O Controller Hub 4 Mobile-2

PCI Interface Signals (Continued)

Signal Name	Type	Description
FRAME#	I/O	**Cycle Frame:** The current Initiator drives FRAME# to indicate the beginning and duration of a PCI transaction. While the Initiator asserts FRAME#, data transfers continue. When the Initiator negates FRAME#, the transaction is in the final data phase. FRAME# is an input to the ICH4 when the ICH4 is the Target, and FRAME# is an output from the ICH4 when the ICH4 is the Initiator. FRAME# remains tri- stated by the ICH4 until driven by an Initiator.
IRDY#	I/O	**Initiator Ready:** IRDY# indicates the ICH4's ability, as an Initiator, to complete the current data phase of the transaction. It is used in conjunction with TRDY#. A data phase is completed on any clock that both IRDY# and TRDY# are sampled asserted. During a write, IRDY# indicates the ICH4 has valid data present on AD[31:0]. During a read, it indicates the ICH4 is prepared to latch data. IRDY# is an input to the ICH4 when the ICH4 is the Target and an output from the ICH4 when the ICH4 is an Initiator. IRDY# remains tri-stated by the ICH4 until driven by an Initiator.
TRDY#	I/O	**Target Ready:** TRDY# indicates the ICH4's ability, as a Target, to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed when both TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that the ICH4, as a Target, has placed valid data on AD[31:0]. During a write, TRDY# indicates that the ICH4, as a Target, is prepared to latch data. TRDY# is an input to the ICH4 when the ICH4 is the Initiator and an output from the ICH4 when the ICH4 is a Target. TRDY# is tri-stated from the leading edge of PCIRST#. TRDY# remains tri-stated by the ICH4 until driven by a target.
PAR	I/O	**Calculated/Checked Parity:** PAR uses “even” parity calculated on 36 bits, AD[31:0] plus C/BE[3:0]#. “Even” parity means that the ICH4 counts the number of 1s within the 36 bits plus PAR and the sum is always even. The ICH4 always calculates PAR on 36 bits regardless of the valid byte enables. The ICH4 generates PAR for address and data phases and only guarantees PAR to be valid one PCI clock after the corresponding address or data phase. The ICH4 drives and tri-states PAR identically to the AD[31:0] lines except that the ICH4 delays PAR by exactly one PCI clock. PAR is an output during the address phase (delayed one clock) for all ICH4 initiated transactions. PAR is an output during the data phase (delayed one clock) when the ICH4 is the Initiator of a PCI write transaction, and when it is the Target of a read transaction. ICH4 checks parity when it is the Target of a PCI write transaction. If a parity error is detected, the ICH4 will set the appropriate internal status bits, and has the option to generate an NMI# or SMI#.

PCI Interface Signals (Continued)

Signal Name	Type	Description
STOP#	I/O	**Stop:** STOP# indicates that the ICH4, as a Target, is requesting the Initiator to stop the current transaction. STOP# causes the ICH4, as an Initiator, to stop the current transaction. STOP# is an output when the ICH4 is a Target and an input when the ICH4 is an Initiator. STOP# is tri-stated from the leading edge of PCIRST#. STOP# remains tri-stated until driven by the ICH4.
PERR#	I/O	**Parity Error:** An external PCI device drives PERR# when it receives data that has a parity error. The ICH4 drives PERR# when it detects a parity error. The ICH4 can either generate an NMI# or SMI# upon detecting a parity error (either detected internally or reported via the PERR# signal).
REQ[4:0]# **REQ[5]#/** REQ[B]#/ GPIO[1]	I	**PCI Requests:** The ICH4 supports up to 6 masters on the PCI bus. REQ[5]# is muxed with PC/PCI REQ[B]# (must choose one or the other, but not both). If not used for PCI or PC/PCI, REQ[5]#/REQ[B]# can instead be used as GPIO[1]. **NOTE:** REQ[0]# is programmable to have improved arbitration latency for for supporting PCI-based 1394 controllers.
GNT[4:0]# **GNT[5]#/** GNT[B]#/ GPIO[17]	O	**PCI Grants:** The ICH4 supports up to 6 masters on the PCI bus. GNT[5]# is muxed with PC/PCI GNT[B]# (must choose one or the other, but not both). If not needed for PCI or PC/PCI, GNT[5]# can instead be used as a GPIO. Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3 power rail. GNT[B]#/GNT[5]#/GPIO[17] has an internal pull-up.
PCICLK	I	**PCI Clock:** This is a 33 MHz clock. PCICLK provides timing for all transactions on the PCI Bus. **NOTE:** This clock does not stop based on STP_PCI# signal. PCICLK only stops based on SLP_S1# or SLP_S3#.
PCIRST#	O	**PCI Reset:** ICH4 asserts PCIRST# to reset devices that reside on the PCI bus. The ICH4 asserts PCIRST# during power-up and when S/W initiates a hard reset sequence through the RC (CF9h) register. The ICH4 drives PCIRST# inactive a minimum of 1 ms after PWROK is driven active. The ICH4 drives PCIRST# active a minimum of 1 ms when initiated through the RC register.
PLOCK#	I/O	**PCI Lock:** This signal indicates an exclusive bus operation and may require multiple transactions to complete. ICH4 asserts PLOCK# when it performs non- exclusive transactions on the PCI bus. Devices on the PCI bus (other than the ICH4) are not permitted to assert the PLOCK# signal.
SERR#	I/OD	**System Error:** SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, the ICH4 has the ability to generate an NMI, SMI#, or interrupt.

5.3 Intel 82801DBM I/O Controller Hub 4 Mobile-3

PCI Interface Signals (Continued)

Signal Name	Type	Description
PME#	I/OD	**PCI Power Management Event:** PCI peripherals drive PME# to wake the system from low-power states S1-M–S5. PME# assertion can also be enabled to generate an SCI from the S0 state. In some cases the ICH4 may drive PME# active due to an internal wake event. The ICH4 will not drive PME# high, but it will be pulled up to VccSus3_3 by an internal pull-up resistor.
CLKRUN#	I/O	**PCI Clock Run:** Used to support PCI Clock Run protocol. Connects to PCI devices that need to request clock re-start, or prevention of clock stopping. **NOTE:** An external pull-up to the core power plane is required.
REQ[A]#/ GPIO[0] **REQ[B]#/** REQ[5]#/ GPIO[1]	I	**PC/PCI DMA Request [A:B]:** This request serializes ISA-like DMA Requests for the purpose of running ISA-compatible DMA cycles over the PCI bus. This is used by devices such as PCI based Super I/O or audio codecs which need to perform legacy 8237 DMA but have no ISA bus. When not used for PC/PCI requests, these signals can be used as General Purpose Inputs. REQ[B]# can instead be used as the 6th PCI bus request.
GNT[A]#/ GPIO[16] **GNT[B]#/** GNT[5]#/ GPIO[17]	O	**PC/PCI DMA Acknowledges [A: B]:** This grant serializes an ISA-like DACK# for the purpose of running DMA/ISA Master cycles over the PCI bus. This is used by devices such as PCI based Super/IO or audio codecs which need to perform legacy 8237 DMA but have no ISA bus. When not used for PC/PCI, these signals can be used as General Purpose Outputs. GNTB# can also be used as the 6th PCI bus master grant output. These signal have internal pull-up resistors.

IDE Interface Signals

Signal Name	Type	Description
PDCS1#, SDCS1#	O	**Primary and Secondary IDE Device Chip Selects for 100 Range:** For ATA command register block. This output signal is connected to the corresponding signal on the primary or secondary IDE connector.
PDCS3#, SDCS3#	O	**Primary and Secondary IDE Device Chip Select for 300 Range:** For ATA control register block. This output signal is connected to the corresponding signal on the primary or secondary IDE connector.
PDA[2:0], SDA[2:0]	O	**Primary and Secondary IDE Device Address:** These output signals are connected to the corresponding signals on the primary or secondary IDE connectors. They are used to indicate which byte in either the ATA command block or control block is being addressed.

IDE Interface Signals (Continued)

Signal Name	Type	Description
PDD[15:0], SDD[15:0]	I/O	**Primary and Secondary IDE Device Data:** These signals directly drive the corresponding signals on the primary or secondary IDE connector. There is a weak internal pull-down resistor on PDD[7] and SDD[7].
PDDREQ, SDDREQ	I	**Primary and Secondary IDE Device DMA Request:** These input signals are directly driven from the DRQ signals on the primary or secondary IDE connector. It is asserted by the IDE device to request a data transfer, and used in conjunction with the PCI bus master IDE function and are not associated with any AT compatible DMA channel. There is a weak internal pull-down resistor on these signals.
PDDACK#, SDDACK#	O	**Primary and Secondary IDE Device DMA Acknowledge:** These signals directly drive the DAK# signals on the primary and secondary IDE connectors. Each is asserted by the ICH4 to indicate to IDE DMA slave devices that a given data transfer cycle (assertion of DIOR# or DIOW#) is a DMA data transfer cycle. This signal is used in conjunction with the PCI bus master IDE function and are not associated with any AT-compatible DMA channel.
PDIOR#/ (PDWSTB/PRDMARDY#) **SDIOR#/** (SDWSTB/SRDMARDY#)	O	**Primary and Secondary Disk I/O Read (PIO and Non-Ultra DMA):** This is the command to the IDE device that it may drive data onto the PDD or SDD lines. Data is latched by the ICH4 on the deassertion edge of PDIOR# or SDIOR#. The IDE device is selected either by the ATA register file chip selects (PDCS1# or SDCS1#, PDCS3# or SDCS3#) and the PDA or SDA lines, or the IDE DMA acknowledge (PDDAK# or SDDAK#). Primary and Secondary Disk Write Strobe (Ultra DMA Writes to Disk): This is the data write strobe for writes to disk. When writing to disk, ICH4 drives valid data on rising and falling edges of PDWSTB or SDWSTB. Primary and Secondary Disk DMA Ready (Ultra DMA Reads from Disk): This is the DMA ready for reads from disk. When reading from disk, ICH4 deasserts PRDMARDY# or SRDMARDY# to pause burst data transfers.
PDIOW#/ (PDSTOP) **SDIOW#/** (SDSTOP)	O	**Primary and Secondary Disk I/O Write (PIO and Non-Ultra DMA):** This is the command to the IDE device that it may latch data from the PDD or SDD lines. Data is latched by the IDE device on the deassertion edge of PDIOW# or SDIOW#. The IDE device is selected either by the ATA register file chip selects (PDCS1# or SDCS1#, PDCS3# or SDCS3#) and the PDA or SDA lines, or the IDE DMA acknowledge (PDDAK# or SDDAK#). Primary and Secondary Disk Stop (Ultra DMA): ICH4 asserts this signal to terminate a burst.

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IDE Interface Signals (Continued)

Signal Name	Type	Description
PIORDY#/ (PDRSTB/PWDMARDY#) **SIORDY#/** (SDRSTB/SWDMARDY#)	I	**Primary and Secondary I/O Channel Ready (PIO):** This signal will keep the strobe active (PDIOR# or SDIOR# on reads, PDIOW# or SDIOW# on writes) longer than the minimum width. It adds wait states to PIO transfers. Primary and Secondary Disk Read Strobe (Ultra DMA Reads from Disk): When reading from disk, the ICH4 latches data on rising and falling edges of this signal from the disk. Primary and Secondary Disk DMA Ready (Ultra DMA Writes to Disk): When writing to disk, this is de-asserted by the disk to pause burst data transfers.

Interrupt Signals

Signal Name	Type	Description
SERIRQ	I/O	**Serial Interrupt Request:** This pin implements the serial interrupt protocol.
PIRQ[D:A]#	I/OD	**PCI Interrupt Requests:** In Non-APIC Mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described in the Interrupt Steering section. Each PIRQx# line has a separate Route Control Register. In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQ[A]# is connected to IRQ16, PIRQ[B]# to IRQ17, PIRQ[C]# to IRQ18, and PIRQ[D]# to IRQ19. This frees the legacy interrupts.
PIRQ[H:E]#/ GPIO[5:2]	I/OD	**PCI Interrupt Requests:** In Non-APIC Mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described in the Interrupt Steering section. Each PIRQx# line has a separate Route Control Register. In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQ[E]# is connected to IRQ20, PIRQ[F]# to IRQ21, PIRQ[G]# to IRQ22, and PIRQ[H]# to IRQ23. This frees the legacy interrupts. If not needed for interrupts, these signals can be used as GPIO.
IRQ[14:15]	I	**Interrupt Request 14:15:** These interrupt inputs are connected to the IDE drives. IRQ14 is used by the drives connected to the Primary controller and IRQ15 is used by the drives connected to the Secondary controller.
APICCLK	I	**APIC Clock:** This clock operates up to 33.33 MHz.
APICD[1:0]	I/OD	**APIC Data:** These bi-directional open drain signals are used to send and receive data over the APIC bus. As inputs the data is valid on the rising edge of APICCLK. As outputs, new data is driven from the rising edge of the APICCLK.

LPC Interface Signals

Signal Name	Type	Description
LAD[3:0]/ FWH[3:0]	I/O	**LPC Multiplexed Command, Address, Data:** For the LAD[3:0] signals, internal pull-ups are provided.
LFRAME#/ FWH[4]	O	**LPC Frame:** LFRAME# indicates the start of an LPC cycle, or an abort.
LDRQ[1:0]#	I	**LPC Serial DMA/Master Request Inputs:** LDRQ[1:0]# are used to request DMA or bus master access. These signals are typically connected to an external Super I/O device. An internal pull-up resistor is provided on these signals.

USB Interface Signals

Signal Name	Type	Description
USBP0P, USBP0N, USBP1P, USBP1N	I/O	**Universal Serial Bus Port 1:0 Differential:** These differential pairs are used to transmit data/address/command signals for ports 0 and 1. These ports can be routed to USB UHCI Controller #1 or the USB EHCI Controller. **NOTE:** No external resistors are required on these signals. The ICH4 integrates 15 k . pull-downs and provides an output driver impedance of 45 . which requires no external series resistor
USBP2P, USBP2N, USBP3P, USBP3N	I/O	**Universal Serial Bus Port 3:2 Differential:** These differential pairs are used to transmit data/address/command signals for ports 2 and 3. These ports can be routed to USB UHCI Controller #2 or the USB EHCI Controller. **NOTE:** No external resistors are required on these signals. The ICH4 integrates 15 k . pull-downs and provides an output driver impedance of 45 . which requires no external series resistor.
USBP4P, USBP4N, USBP5P, USBP4N	I/O	**Universal Serial Bus Port 5:4 Differential:** These differential pairs are used to transmit data/address/command signals for ports 4 and 5. These ports can be routed to USB UHCI Controller #3 or the USB EHCI Controller **NOTE:** No external resistors are required on these signals. The ICH4 integrates 15 k . pull-downs and provides an output driver impedance of 45 . which requires no external series resistor
OC[5:0]#	I/O	**Overcurrent Indicators:** These signals set corresponding bits in the USB controllers to indicate that an overcurrent condition has occurred.
USBRBIAS	O	**USB Resistor Bias:** Analog connection point for an external resistor to ground. USBRBIAS should be connected to USBRBIAS# as close to the resistor as possible.
USBRBIAS#	I	**USB Resistor Bias Complement:** Analog connection point for an external resistor to ground. USBRBIAS# should be connected to USBRBIAS as close to the resistor as possible.

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Power Management Interface Signals

Signal Name	Type	Description
THRM#	I	**Thermal Alarm:** This is an active low signal generated by external hardware to start the hardware clock throttling mode. The signal can also generate an SMI# or an SCI.
THRMTRIP#	I	**Thermal Trip:** When low, THRMTRIP# indicates that a thermal trip from the processor occurred; the ICH4 will immediately transition to a S5 state. The ICH4 will not wait for the processor stop grant cycle since the processor has overheated.
SLP_S1#	O	**S1 Sleep Control:** SLP_S1# provides Clock Synthesizer or Power plane control. Optional use is to shut off power to non-critical systems when in the S1- M (Powered On Suspend), S3 (Suspend To RAM), S4 (Suspend to Disk) or S5 (Soft Off) states.
SLP_S3#	O	**S3 Sleep Control:** SLP_S3# is for power plane control. It shuts off power to all non-critical systems when in S3 (Suspend To RAM), S4 (Suspend to Disk), or S5 (Soft Off) states.
SLP_S4#	O	**S4 Sleep Control:** SLP_S4# is for power plane control. It shuts power to all non-critical systems when in the S4 (Suspend to Disk) or S5 (Soft Off) state.
SLP_S5#	O	**S5 Sleep Control:** SLP_S5# is for power plane control. The signal is used to shut power off to all non-critical systems when in the S5 (Soft Off) states.
PWROK	I	**Power OK:** When asserted, PWROK is an indication to the ICH4 that core power and PCICLK have been stable for at least 1 ms. PWROK can be driven asynchronously. When PWROK is negated, the ICH4 asserts PCIRST#. **NOTE:** PWROK must deassert for a minimum of 3 RTC clock periods for the ICH4 to fully reset the power and properly generate the PCIRST# output
PWRBTN#	I	**Power Button:** The Power Button causes SMI# or SCI to indicate a system request to go to a sleep state. If the system is already in a sleep state, this signal causes a wake event. If PWRBTN# is pressed for more than 4 seconds, this causes an unconditional transition (power button override) to the S5 state with only the PWRBTN# available as a wake event. Override occurs even if the system is in the S1-M–S4 states. This signal has an internal pull-up resistor.
RI#	I	**Ring Indicate:** This signal is an input from the modem interface. It can be enabled as a wake event, and this is preserved across power failures.
SYS_RESET#	I	**System Reset:** This pin forces an internal reset after being debounced. The ICH4 will reset immediately if the SMBus is idle; otherwise, it will wait up to 25 ms ± 2 ms for the SMBus to idle before forcing a reset on the system.
RSMRST#	I	**Resume Well Reset:** This signal is used for resetting the resume power plane logic.

Power Management Interface Signals (Continued)

Signal Name	Type	Description
LAN_RST#	I	**LAN Reset:** This signal must be asserted at least 10 ms after the resume well power (VccLAN3_3 and VccLAN1_5 is valid. When deasserted, this signal is an indication that the resume well power is stable.
SUS_STAT#/ LPCPD#	O	**Suspend Status:** This signal is asserted by the ICH4 to indicate that the system will be entering a low power state soon. This can be monitored by devices with memory that need to switch from normal refresh to suspend refresh mode. It can also be used by other peripherals as an indication that they should isolate their outputs that may be going to powered-off planes. This signal is called LPCPD# on the LPC I/F.
C3_STAT#	O	**C3_STAT#:** This signal will typically be configured as C3_STAT#. It is used for indicating to an AGP device that a C3 state transition is beginning or ending. If C3_STAT# functionality is not required, this signal may be used as a GPO. **NOTE:** This signal will be asserted in S1-M on the ICH4-M.
SUSCLK	O	**Suspend Clock:** Output of the RTC generator circuit to use by other chips for refresh clock.
AGPBUSY#	I	**AGP Bus Busy:** To support the C3 state. This signal is an indication that the AGP device is busy. When this signal is asserted, the BM_STS bit will be set. If this functionality is not needed, this signal may be configured as a GPI.
STP_PCI#	O	**Stop PCI Clock:** This signal is an output to the external clock generator for it to turn off the PCI clock. Used to support PCI CLKRUN# protocol. If this functionality is not needed, This signal can be configured as a GPO.
STP_CPU#	O	**Stop CPU Clock:** Output to the external clock generator for it to turn off the processor clock. Used to support the C3 state. If this functionality is not needed, this signal can be configured as a GPO.
BATLOW#	I	**Battery Low:** This signal is an input from the battery to indicate that there is insufficient power to boot the system. Assertion will prevent wake from S1-M–S5 state. Can also be enabled to cause an SMI# when asserted.
CPUPERF#	OD	**CPU Performance:** CPUPERF# is used for Intel SpeedStep technology support. The signal selects which power state to put the processor in.
SSMUXSEL	O	**SpeedStep Mux Select:** SSMUXSEL is used for Intel SpeedStep technology support. The signal selects the voltage level for the processor.
VGATE/ VRMPWRGD	I	**VGATE/VRM Power Good:** VGATE/VRMPWRGD is used for Intel SpeedStep technology support. This is an output from the processor's voltage regulator to indicate that the voltage is stable. This signal may go inactive during an Intel SpeedStep transition.

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Power Management Interface Signals (Continued)

Signal Name	Type	Description
DPRSLPVR	O	**Deeper Sleep - Voltage Regulator:** This signal is used to lower the voltage of VRM during C4 and S1-M states. When the signal is high, the voltage regulator outputs the lower "Deeper Sleep" voltage. When the signal is low (default), the voltage regulator outputs the higher "Normal" voltage. During PCIRST#, the output driver is disabled and an internal pull-down is enabled. This is needed for implementing a strap on the pin. When PCIRST# deasserts, the output driver is enabled. To guarantee no glitches on the DPRSLPVR pin, the pull-down is disabled after the output driver is fully enabled. **NOTE:** DPRSLPVR is sampled at the rising edge of PWROK as a functional strap.

Processor Interface Signals

Signal Name	Type	Description
A20M#	O	**Mask A20:** A20M# will go active based on either setting the appropriate bit in the Port 92h register, or based on the A20GATE input being active. **Speed Strap:** During the reset sequence, ICH4 drives A20M# high if the corresponding bit is set in the FREQ_STRP register.
CPUSLP#	O	**CPU Sleep:** This signal puts the processor into a state that saves substantial power compared to Stop-Grant state. However, during that time, no snoops occur. The ICH4 can optionally assert the CPUSLP# signal when going to the S1-M state.
FERR#	I	**Numeric Coprocessor Error:** This signal is tied to the coprocessor error signal on the processor. FERR# is only used if the ICH4 coprocessor error reporting function is enabled in the General Control Register (Device 31:Function 0, Offset D0, bit 13). If FERR# is asserted, the ICH4 generates an internal IRQ13 to its interrupt controller unit. It is also used to gate the IGNNE# signal to ensure that IGNNE# is not asserted to the processor unless FERR# is active. FERR# requires an external weak pull-up to ensure a high level when the coprocessor error function is disabled. **NOTE:** FERR# can be used in some states for notification by the processor of pending interrupt events. This functionality is independent of the General Control Register bit setting.
INTR	O	**CPU Interrupt:** INTR is asserted by the ICH4 to signal the processor that an interrupt request is pending and needs to be serviced. It is an asynchronous output and normally driven low. **Speed Strap:** During the reset sequence, ICH4 drives INTR high if the corresponding bit is set in the FREQ_STRP register.

Processor Interface Signals (Continued)

Signal Name	Type	Description
IGNNE#	O	**Ignore Numeric Error:** This signal is connected to the ignore error pin on the processor. IGNNE# is only used if the ICH4 coprocessor error reporting function is enabled in the General Control Register (Device 31:Function 0, Offset D0, bit 13). If FERR# is active, indicating a coprocessor error, a write to the Coprocessor Error Register (F0h) causes the IGNNE# to be asserted. IGNNE# remains asserted until FERR# is negated. If FERR# is not asserted when the Coprocessor Error Register is written, the IGNNE# signal is not asserted. **Speed Strap:** During the reset sequence, ICH4 drives IGNNE# high if the corresponding bit is set in the FREQ_STRP register.
INIT#	O	**Initialization:** INIT# is asserted by the ICH4 for 16 PCI clocks to reset the processor. ICH4 can be configured to support CPU BIST. In that case, INIT# will be active when PCIRST# is active.
NMI	O	**Non-Maskable Interrupt:** NMI is used to force a non-Maskable interrupt to the processor. The ICH4 can generate an NMI when either SERR# or IOCHK# is asserted. The processor detects an NMI when it detects a rising edge on NMI. NMI is reset by setting the corresponding NMI source enable/disable bit in the NMI Status and Control Register. **Speed Strap:** During the reset sequence, ICH4 drives NMI high if the corresponding bit is set in the FREQ_STRP register.
SMI#	O	**System Management Interrupt:** SMI# is an active low output synchronous to PCICLK. It is asserted by the ICH4 in response to one of many enabled hardware or software events.
STPCLK#	O	**Stop Clock Request:** STPCLK# is an active low output synchronous to PCICLK. It is asserted by the ICH4 in response to one of many hardware or software events. When the processor samples STPCLK# asserted, it responds by stopping its internal clock.
RCIN#	I	**Keyboard Controller Reset CPU:** The keyboard controller can generate INIT# to the processor. This saves the external OR gate with the ICH4's other sources of INIT#. When the ICH4 detects the assertion of this signal, INIT# is generated for 16 PCI clocks. **NOTE:** The ICH4 ignores RCIN# assertion during transitions to the S1-M, S3, S4 and S5 states.
A20GATE	I	**A20 Gate:** A20GATE is from the keyboard controller. The signal acts as an alternative method to force the A20M# signal active. It saves the external OR gate needed with various other PCIsets.

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Processor Interface Signals (Continued)

Signal Name	Type	Description
CPUPWRGD	OD	**CPU Power Good:** This signal should be connected to the processor's PWRGOOD input. To allow for Intel ® SpeedStep™ technology support, this signal is kept high during an Intel SpeedStep technology state transition to prevent loss of processor context. This is an open-drain output signal (external pull-up resistor required) that represents a logical AND of the ICH4's PWROK and VGATE / VRMPWRGD signals.
DPSLP#	O	**Deeper Sleep:** This signal is asserted by the ICH4 to the processor. When the signal is low, the processor enters the Deeper Sleep state by gating off the processor Core clock inside the processor. When the signal is high (default), the processor is not in the Deeper Sleep state. This signal behaves identically to the STP_CPU# signal, but at the processor voltage level.

SMBus Interface Signals

Signal Name	Type	Description
SMBDATA	I/OD	**SMBus Data:** External pull-up is required.
SMBCLK	I/OD	**SMBus Clock:** External pull-up is required.
SMBALERT#/ GPIO[11]	I	**SMBus Alert:** This signal is used to wake the system or generate SMI#. If not used for SMBALERT#, it can be used as a GPI.

System Management Interface Signals

Signal Name	Type	Description
INTRUDER#	I	**Intruder Detect:** Can be set to disable system if box detected open. This signal's status is readable, so it can be used like a GPI if the Intruder Detection is not needed.
SMLINK[1:0]	I/OD	**System Management Link:** SMBus link to optional external system management ASIC or LAN controller. External pull-ups are required. Note that SMLINK[0] corresponds to an SMBus Clock signal, and SMLINK[1] corresponds to an SMBus Data signal.

Real Time Clock Interface Signals

Signal Name	Type	Description
RTCX1	Special	**Crystal Input 1:** This signal is connected to the 32.768 kHz crystal.
RTCX2	Special	**Crystal Input 2:** This signal is connected to the 32.768 kHz crystal.

Other Clock Signals

Signal Name	Type	Description
CLK14	I	**Oscillator Clock:** Used for 8254 timers. It runs at 14.31818 MHz. This clock is permitted to stop during S1-M (or lower) states.
CLK48	I	**48 MHz Clock:** This clock is used to run the USB controller. It runs at 48 MHz. This clock is permitted to stop during S1-M (or lower) states.
CLK66	I	**66 MHz Clock:** This is used to run the hub interface. It runs at 66 MHz. This clock is permitted to stop during S1-M (or lower) states.

Miscellaneous Signals

Signal Name	Type	Description
SPKR	O	**Speaker:** The SPKR signal is the output of counter 2 and is internally "ANDed" with Port 61h bit 1 to provide Speaker Data Enable. This signal drives an external speaker driver device, which in turn drives the system speaker. Upon PCIRST#, its output state is 0. **NOTE:** SPKR is sampled at the rising edge of PWROK as a functional strap.
RTCRST#	I	**RTC Reset:** When asserted, this signal resets register bits in the RTC well and sets the RTC_PWR_STS bit (bit 2 in GEN_PMCON3 register). **NOTES:** 1. Clearing CMOS in an ICH4-based platform can be done by using a jumper on RTCRST# or GPI, or using SAFEMODE strap. Implementations should not attempt to clear CMOS by using a jumper to pull VccRTC low. 2. Unless entering the XOR Chain Test Mode, the RTCRST# input must always be high when all other RTC power planes are on.

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AC'97 Link Signals

Signal Name	Type	Description
AC_RST#	O	**AC '97 Reset:** This signal is a master hardware reset to external Codec(s).
AC_SYNC	O	**AC '97 Sync:** This signal is a 48 kHz fixed rate sample sync to the Codec(s).
AC_BIT_CLK	I	**AC97 Bit Clock:** This signal is a 12.288 MHz serial data clock generated by the external Codec(s). This signal has an integrated pull-down resistor.
AC_SDOUT	O	**AC97 Serial Data Out:** Serial TDM data output to the Codec(s). **NOTE:** AC_SDOUT is sampled at the rising edge of PWROK as a functional strap.
AC_SDIN[1:0]	I	**AC97 Serial Data In 2:**0: These signals are Serial TDM data inputs from the three Codecs.

NOTE: An integrated pull-down resistor on AC_BIT_CLK is enabled when either: The ACLINK Shutoff bit in the AC'97 Global Control Register is set to 1, or Both Function 5 and Function 6 of Device 31 are disabled. Otherwise, the integrated pull-down resistor is disabled.

General Purpose I/O Signals

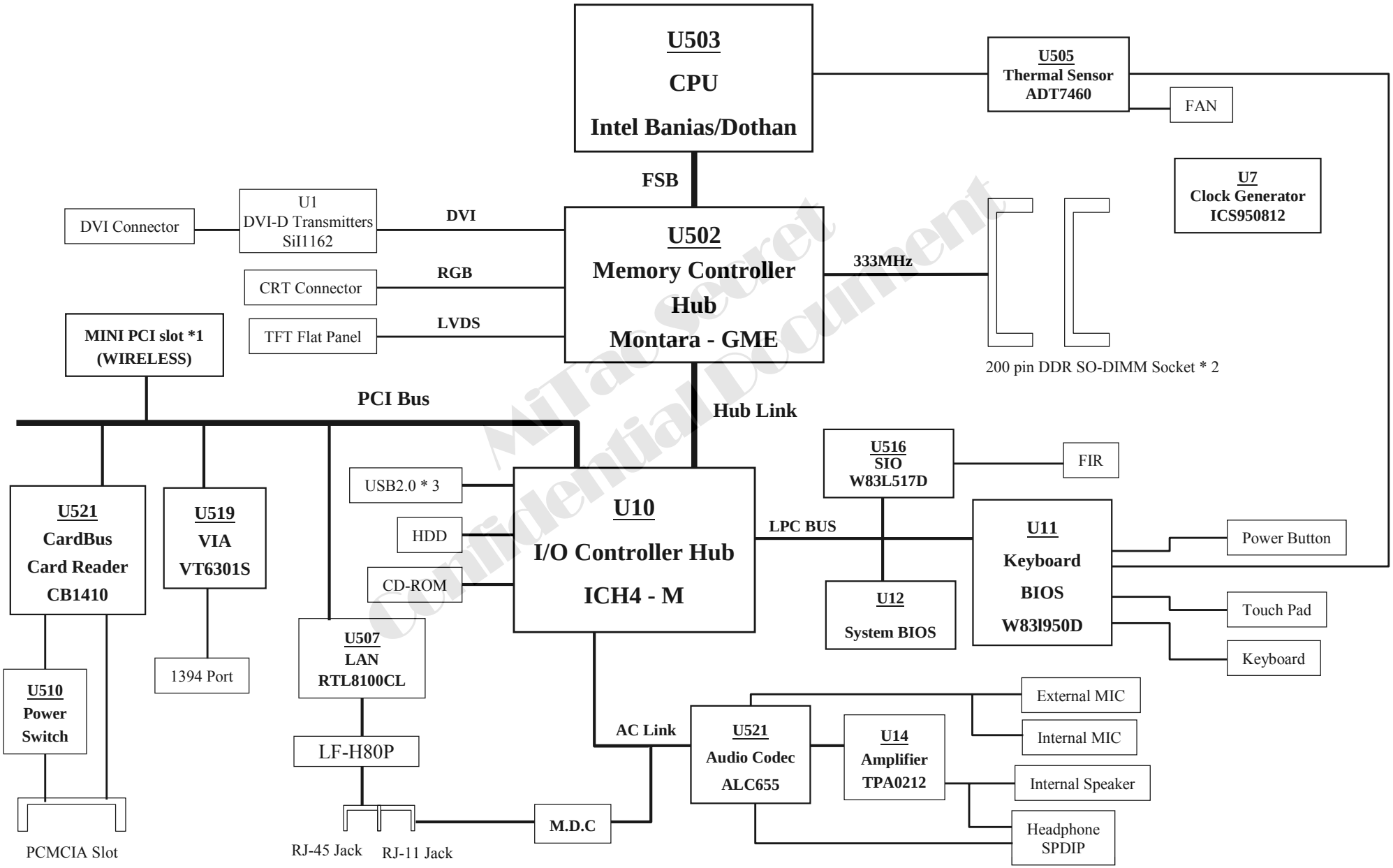
Signal Name	Type	Description
GPIO[43:32]	I/O	Can be input or output. Main power well.
GPIO[31:29]	O	Not implemented.
GPIO[28:27]	I/O	Can be input or output. Resume power well. Unmuxed.
GPIO[26]	I/O	Not implemented.
GPIO[25]	I/O	Can be input or output. Resume power well. Unmuxed.
GPIO[24:18]	I/O	Not Implemented in Mobile (Assign to native Functionality).
GPIO[17:16]	O	Fixed as Output only. Main power well. Can be used instead as PC/PCI GNT[A:B]#. GPIO[17] can also alternatively be used for PCI GNT[5]#. Integrated pull-up resistor.
GPIO[15:14]	I	Not implemented.
GPIO[13:12]	I	Fixed as Input only. Resume power well. Unmuxed.
GPIO[11]	I	Fixed as Input only. Resume power well. Can be used instead as SMBALERT#.
GPIO[10:9]	I	Not implemented.
GPIO[8]	I	Fixed as Input only. Resume power well. Unmuxed.
GPIO[7]	I	Fixed as Input only. Main power well. Unmuxed.
GPIO[6]	I	Not Implemented in Mobile (Assign to Native Functionality)
GPIO[5:2]	I	Fixed as Input only. Main power well. Can be used instead as PIRQ[E:H]#.
GPIO[1:0]	I	Fixed as Input only. Main power well. Can be used instead as PC/PCI REQ[A:B]#. GPIO[1] can also alternatively be used for PCI REQ[5]#.

NOTE: Main power well GPIO are 5V tolerant, except for GPIO[43:32]. Resume power well GPIO are not 5V tolerant.

Power and Ground Signals

Signal Name	Description
VCC3_3	3.3 V supply for core well I/O buffers. This power may be shut off in S3, S4, S5 or G3 states.
VCC1_5	1.5 V supply for core well logic. This power may be shut off in S3, S4, S5 or G3 states.
VCCHI	1.5 V supply for Hub Interface 1.5 logic. 1.8 V supply for Hub Interface 1.0 logic. This power may be shut off in S3, S4, S5 or G3 states.
V5REF	Reference for 5 V tolerance on core well inputs. This power may be shut off in S3, S4, S5 or G3 states.
HIREF	Analog Input. Expected voltages are: • 0.9 V for HI 1.0 (Normal Hub Interface) Series Termination • 350 mV for HI 1.5 (Enhanced Hub Interface) Parallel Termination This power is shut off in S3, S4, S5, and G3 states.
VCCSUS3_3	3.3 V supply for resume well I/O buffers. This power is not expected to be shut off unless the main battery is removed or completely drained and AC power is not available.
VCCSUS1_5	1.5 V supply for resume well logic. This power is not expected to be shut off unless the main battery is removed or completely drained and AC power is not available.
V5REF_SUS	Reference for 5 V tolerance on resume well inputs. This power is not expected to be shut off unless the main battery is removed or completely drained and AC power is not available.
VCCLAN3_3	3.3 V supply for LAN Connect interface buffers. This is a separate power plane that may or may not be powered in S3–S5 states depending upon the presence or absence of AC power and network connectivity. This plane must be on in S0 and S1-M.
VCCLAN1_5	1.5 V supply for LAN Controller logic. This is a separate power plane that may or may not be powered in S3–S5 states depending upon the presence or absence of AC power and network connectivity. This plane must be on in S0 and S1-M.
VCCRTC	3.3 V (can drop to 2.0 V min. in G3 state) supply for the RTC well. This power is not expected to be shut off unless the RTC battery is removed or completely drained. **NOTE:** Implementations should not attempt to clear CMOS by using a jumper to pull VccRTC low. Clearing CMOS in an ICH4-based platform can be done by using a jumper on RTCRST# or GPI, or using SAFEMODE strap.
VCCPLL	1.5 V supply for core well logic. This signal is used for the USB PLL. This power may be shut off in S3, S4, S5 or G3 states.
VBIAS	RTC well bias voltage. The DC reference voltage applied to this pin sets a current that is mirrored throughout the oscillator and buffer circuitry.
V_CPU_IO	Powered by the same supply as the processor I/O voltage. This supply is used to drive the processor interface outputs.
VSS	Grounds.

6. System Block Diagram



7. Maintenance Diagnostics

7.1 Introduction

Each time the computer is turned on, the system bios runs a series of internal checks on the hardware. This power-on self test (post) allows the computer to detect problems as early as the power-on stage. Error messages of post can alert you to the problems of your computer.

If an error is detected during these tests, you will see an error message displayed on the screen. If the error occurs before the display is initialized,then the screen cannot display the error message. Error codes or system beeps are used to identify a post error that occurs when the screen is not available.

The value for the diagnostic port (378H) is written at the beginning of the test. Therefore, if the test failed, the user can determine where the problem occurred by reading the last value written to port 378H by the 378H port debug board plug at Mini PCI Slot.

7.2 Error Codes-1

Following is a list of error codes in sequent display on the PIO debug board.

Code	POST Routine Description
10h	Some type of lone reset
11h	Turn off FAST A20 for POST
12h	Signal power on reset
13h	Initialize the chipset
14h	Search for ISA Bus VGA adapter
15h	Reset counter / Timer 1
16h	User register config through CMOS
17h	Size memory
18h	Dispatch to RAM test
19h	Check sum the ROM
1Ah	Reset PIC's
1Bh	Initialize video adapter(s)
1Ch	Initialize video (6845Regs)
1Dh	Initialize color adapter
1Eh	Initialize monochrome adapter
1Fh	Test 8237A page registers

Code	POST Routine Description
20h	Test keyboard
21h	Test keyboard controller
22h	Check if CMOS RAM valid
23h	Test battery fail & CMOS X-SUM
24h	Test the DMA controller
25h	Initialize 8237A controller
26h	Initialize int vectors
27h	RAM quick sizing
28h	Protected mode entered safely
29h	RAM test completed
2Ah	Protected mode exit successful
2Bh	Setup shadow
2Ch	Going to initialize video
2Dh	Search for monochrome adapter
2Eh	Search for color adapter
2Fh	Sign on messages displayed

7.2 Error Codes-2

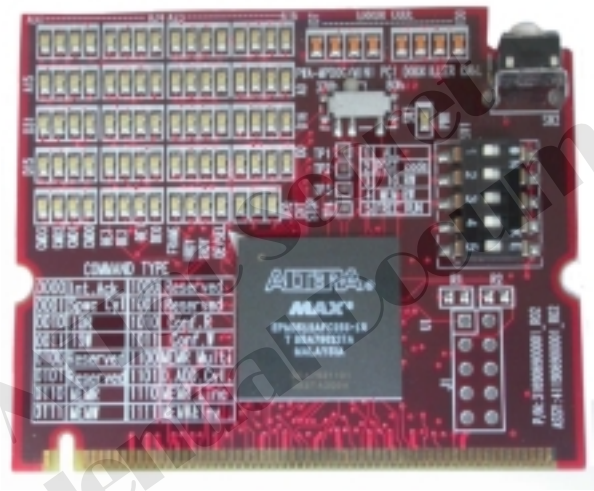
Following is a list of error codes in sequent display on the PIO debug board.

Code	POST Routine Description
30h	Special init of keyboard ctlr
31h	Test if keyboard Present
32h	Test keyboard Interrupt
33h	Test keyboard command byte
34h	Test, blank and count all RAM
35h	Protected mode entered safely(2)
36h	RAM test complete
37h	Protected mode exit successful
38h	Update output port
39h	Setup cache controller
3Ah	Test if 18.2Hz periodic working
3Bh	Test for RTC ticking
3Ch	Initialize the hardware vectors
3Dh	Search and init the mouse
3Eh	Update NUMLOCK status
3Fh	Special init of COMM and LPT ports

Code	POST Routine Description
40h	Configure the COMM and LPT ports
41h	Initialize the floppies
42h	Initialize the hard disk
43h	Initialize option ROMs
44h	OEM's init of power management
45h	Update NUMLOCK status
46h	Test for coprocessor installed
47h	OEM functions before boot
48h	Dispatch to operate system boot
49h	Jump into bootstrap code

7.3 Debug Tool

7.3.1 Diagnostic Tool for Mini PCI Slot :



P/N:411906900001
Description: PWA; PWA-378 Port Debug BD
Note: Order it from MIC/TSSC

8. Trouble Shooting

- 8.1 No Power*1
- 8.2 No Display*2
- 8.3 VGA Controller Failure LCD No Display
- 8.4 External Monitor No Display
- 8.5 Memory Test Error
- 8.6 Keyboard (K/B) Touch-Pad (T/P) Test Error
- 8.7 Hard Driver Test Error
- 8.8 CD-ROM Driver Test Error
- 8.9 USB Port Test Error
- 8.10 Audio Failure
- 8.11 LAN Test Error
- 8.12 PC Card & 1394 Socket Failure

8011 N/B Maintenance

*1: No power definition

Base on ACPI Spec. We define the no power as while we press the power button, the system can't leave S5 status or none the PG signal send out from power supply.

Judge condition:

- Check whether there are any voltage feedback control to turn off the power.
- Check whether no CPU power will cause system can't leave S5 status.

If there are not any diagram match these condition, we should stop analyzing the schematic in power supply sending out the PG signal. If yes, we should add the effected analysis into no power chapter.

*2: No display definition

Base on the digital IC three basic working conditions: working power, reset, Clock. We define the no display as while system leave S5 status but can't get into S0 status.

Judge condition:

- Check which power will cause no display.
- Check which reset signal will cause no display.
- Check which Clock signal will cause no display

Base on these three conditions to analyze the schematic and edit the no display chapter.

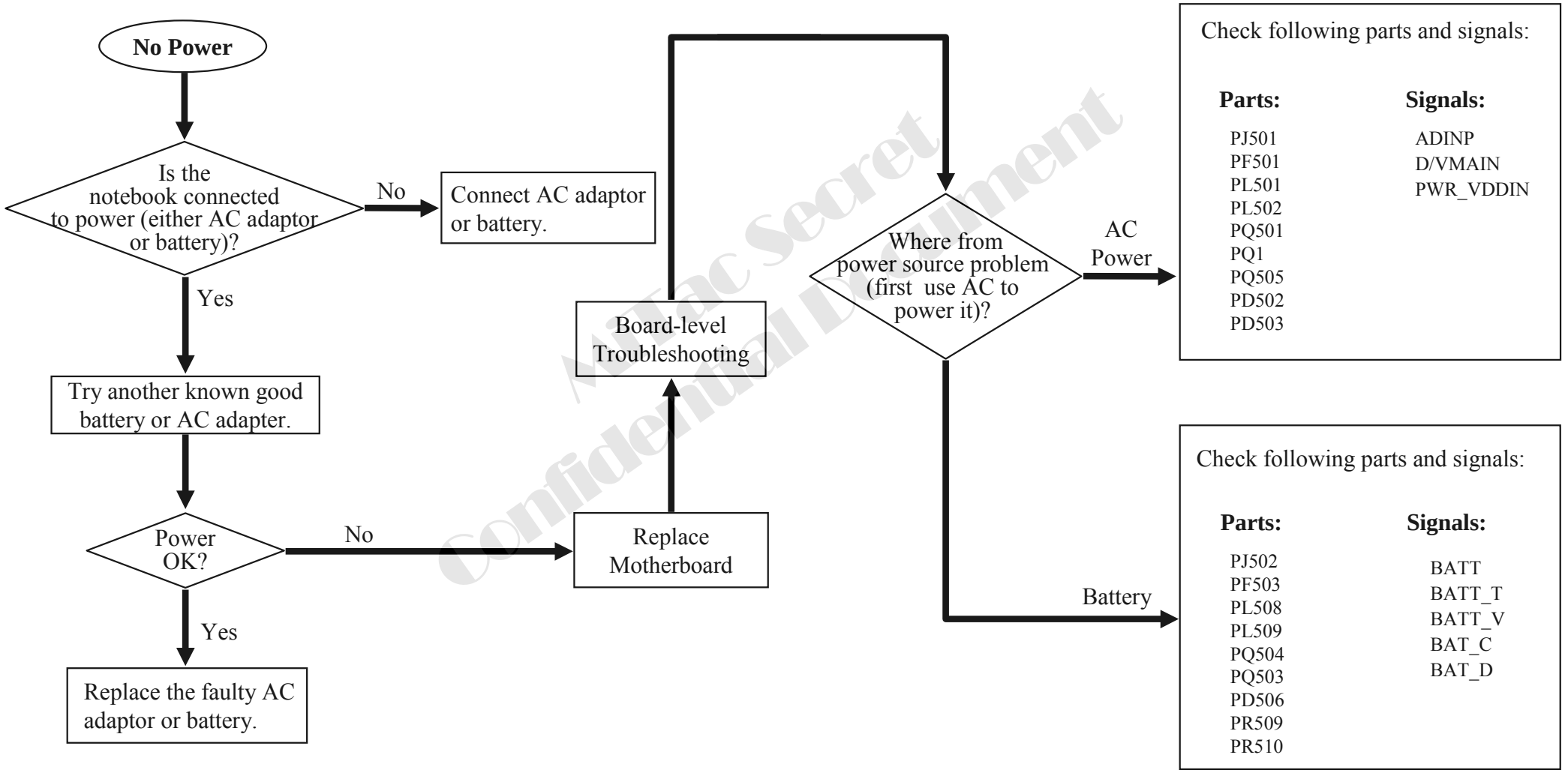
Keyword:

- S5: *Soft Off*
- S0: *Working*

For detail please refer the ACPI specification

8.1 No Power-1

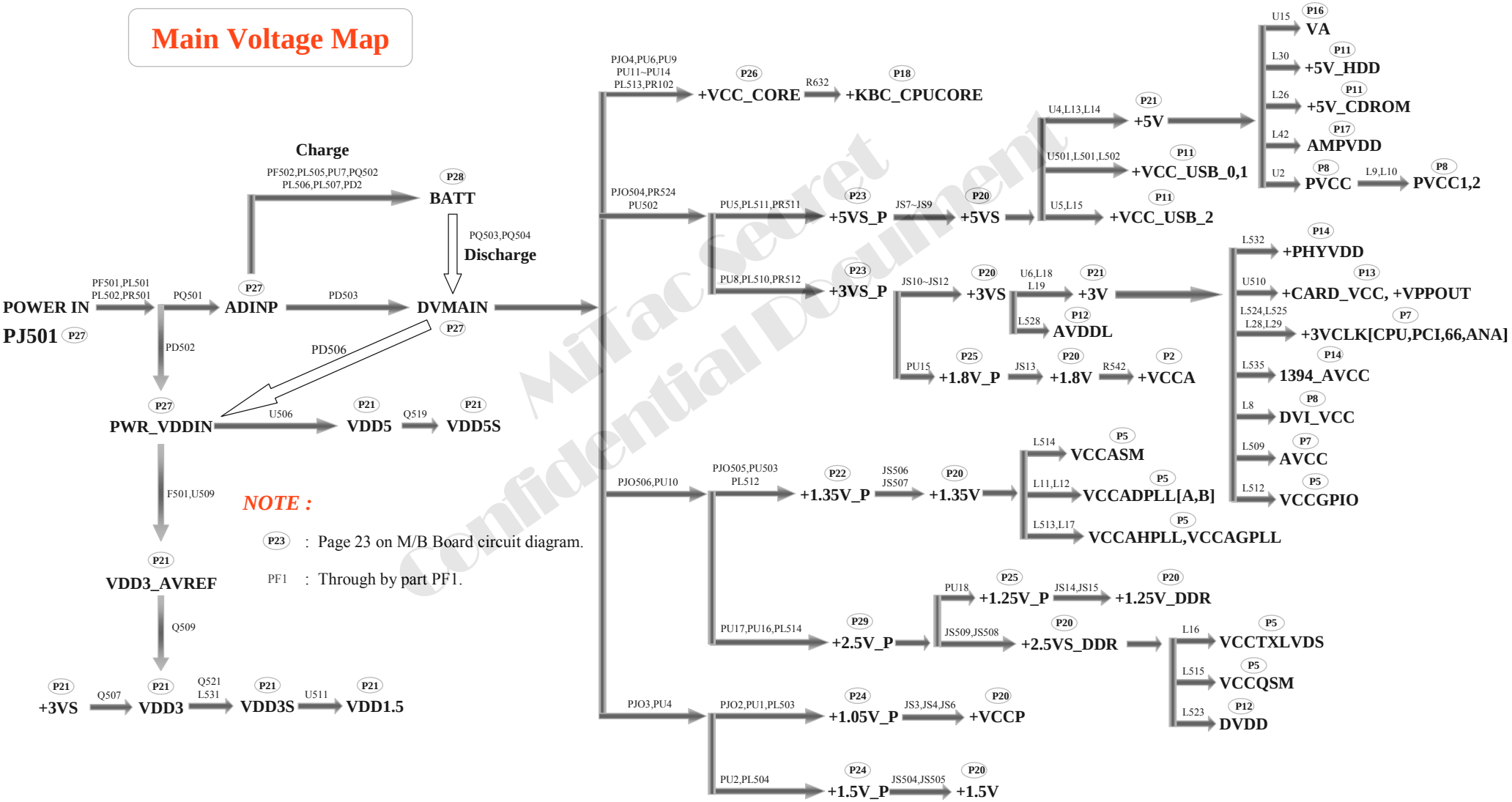
When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



8.1 No Power-2

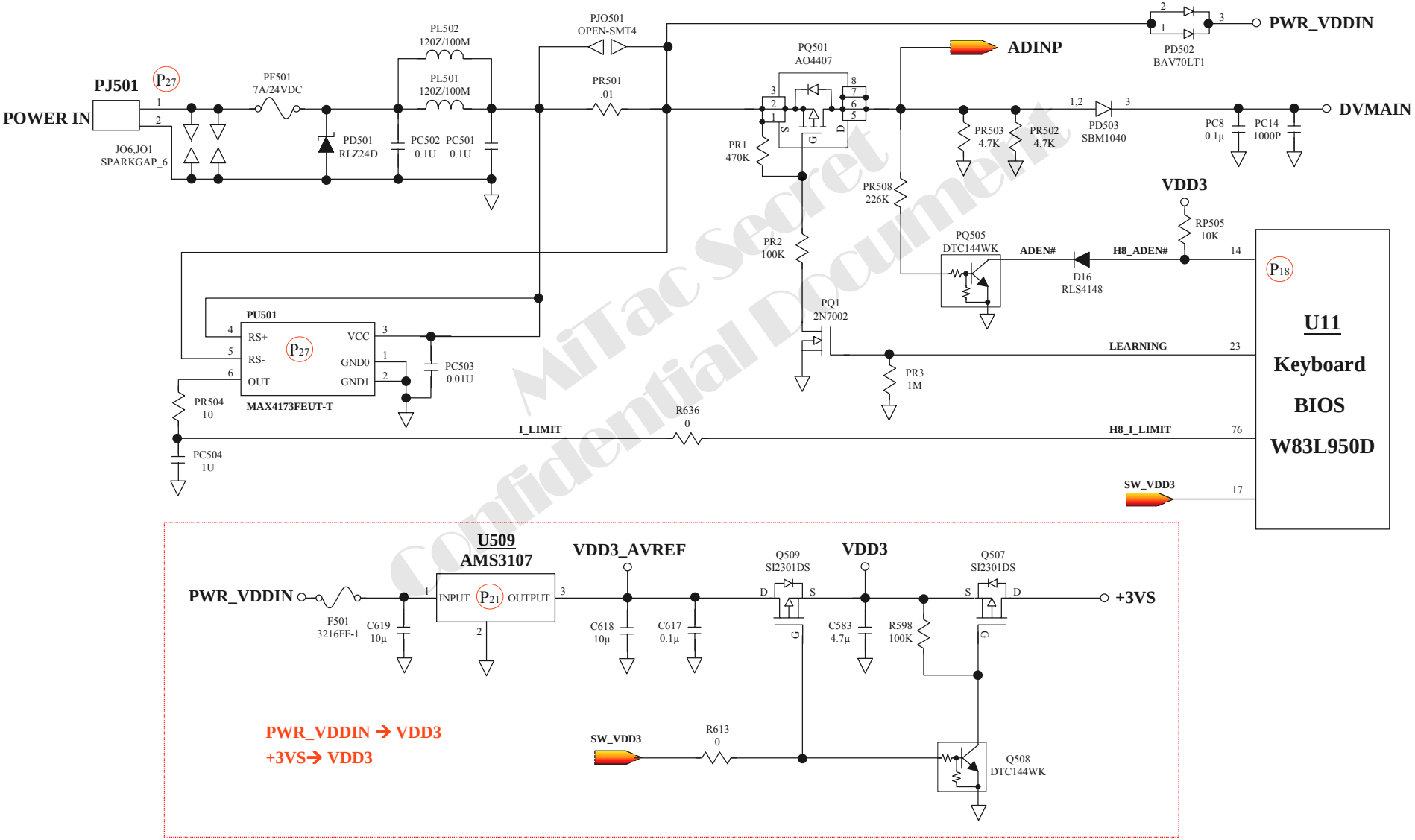
When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.

Main Voltage Map



8.1 No Power-3

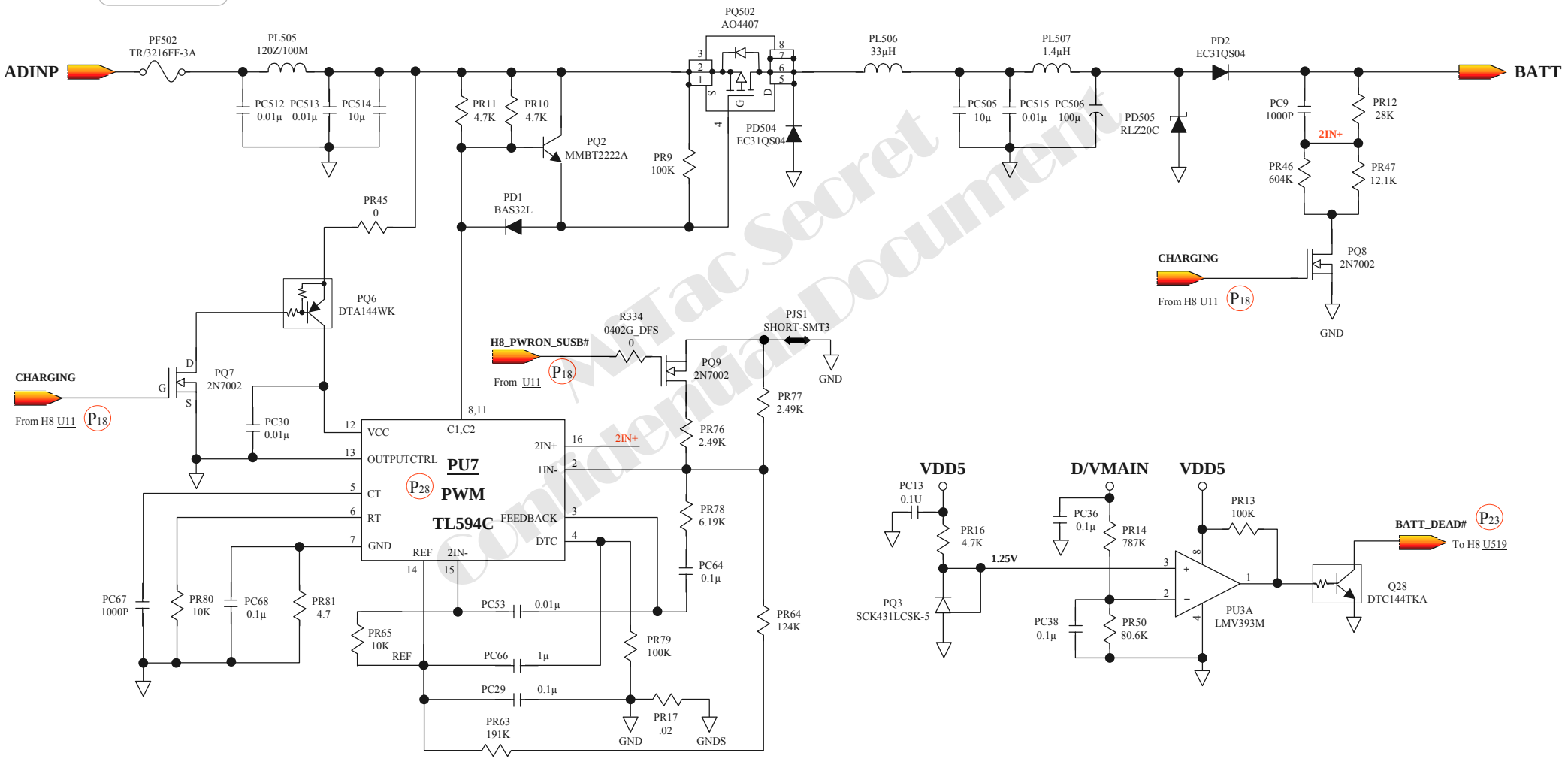
When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



8.1 No Power-4

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.

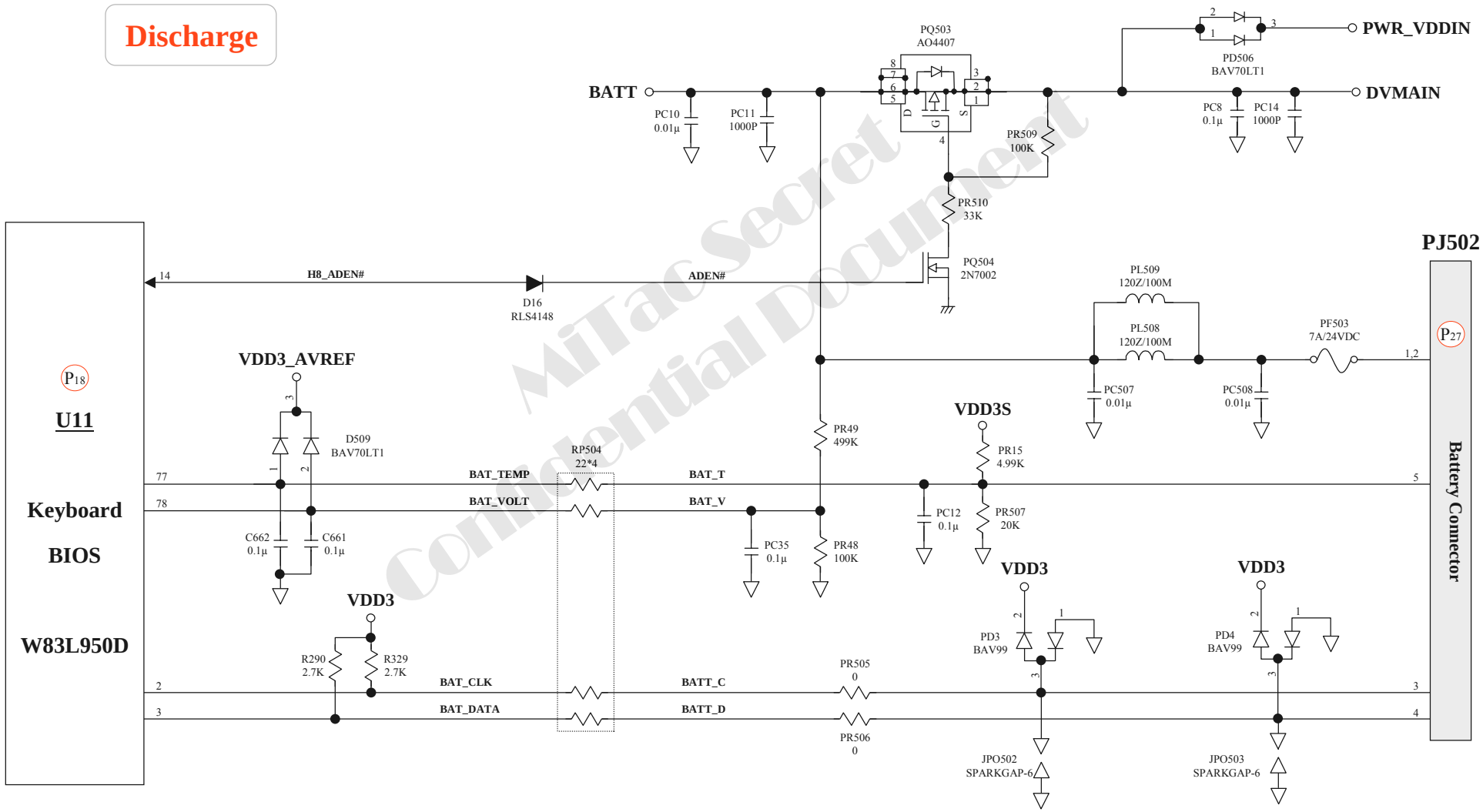
Charge



8.1 No Power-5

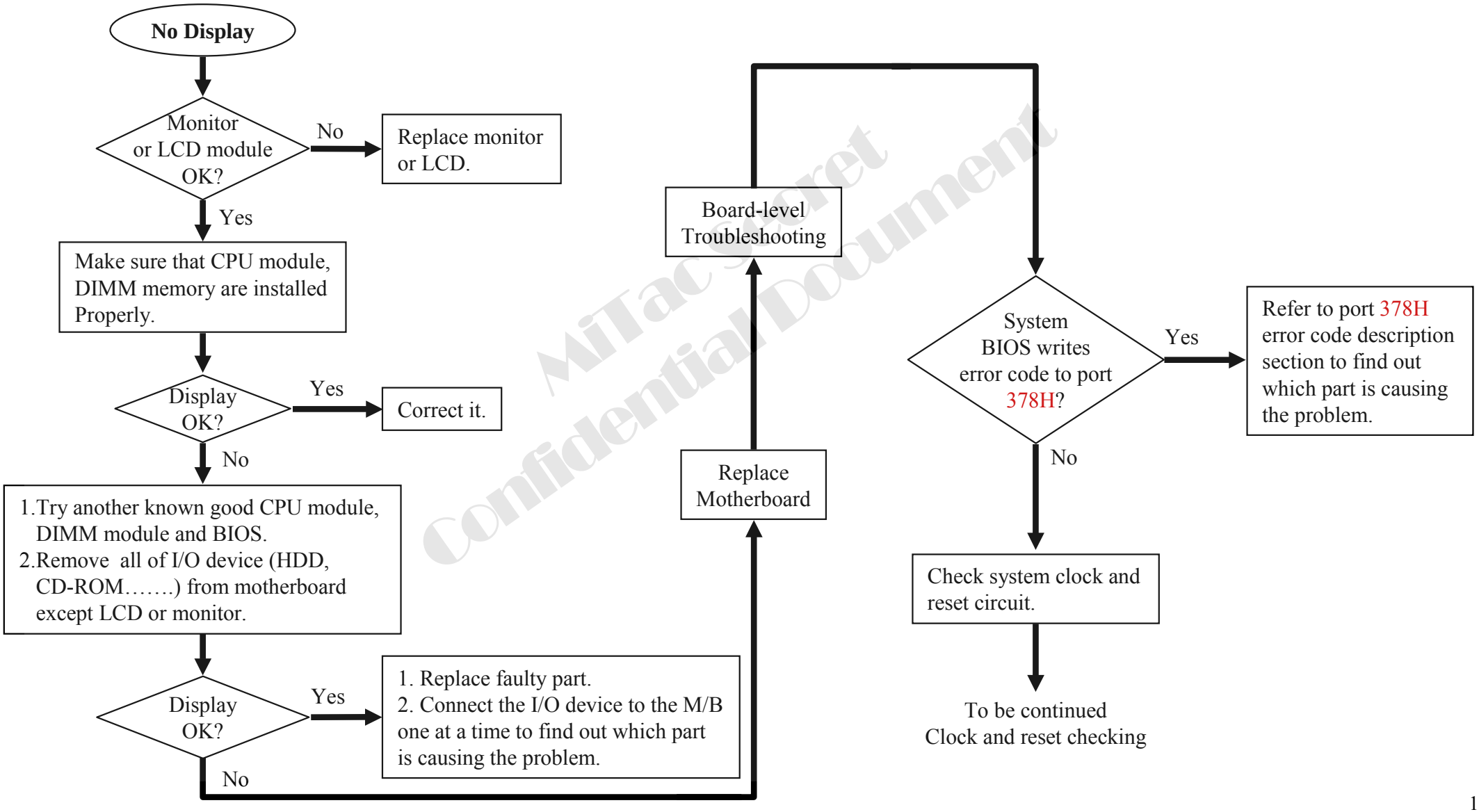
When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.

Discharge



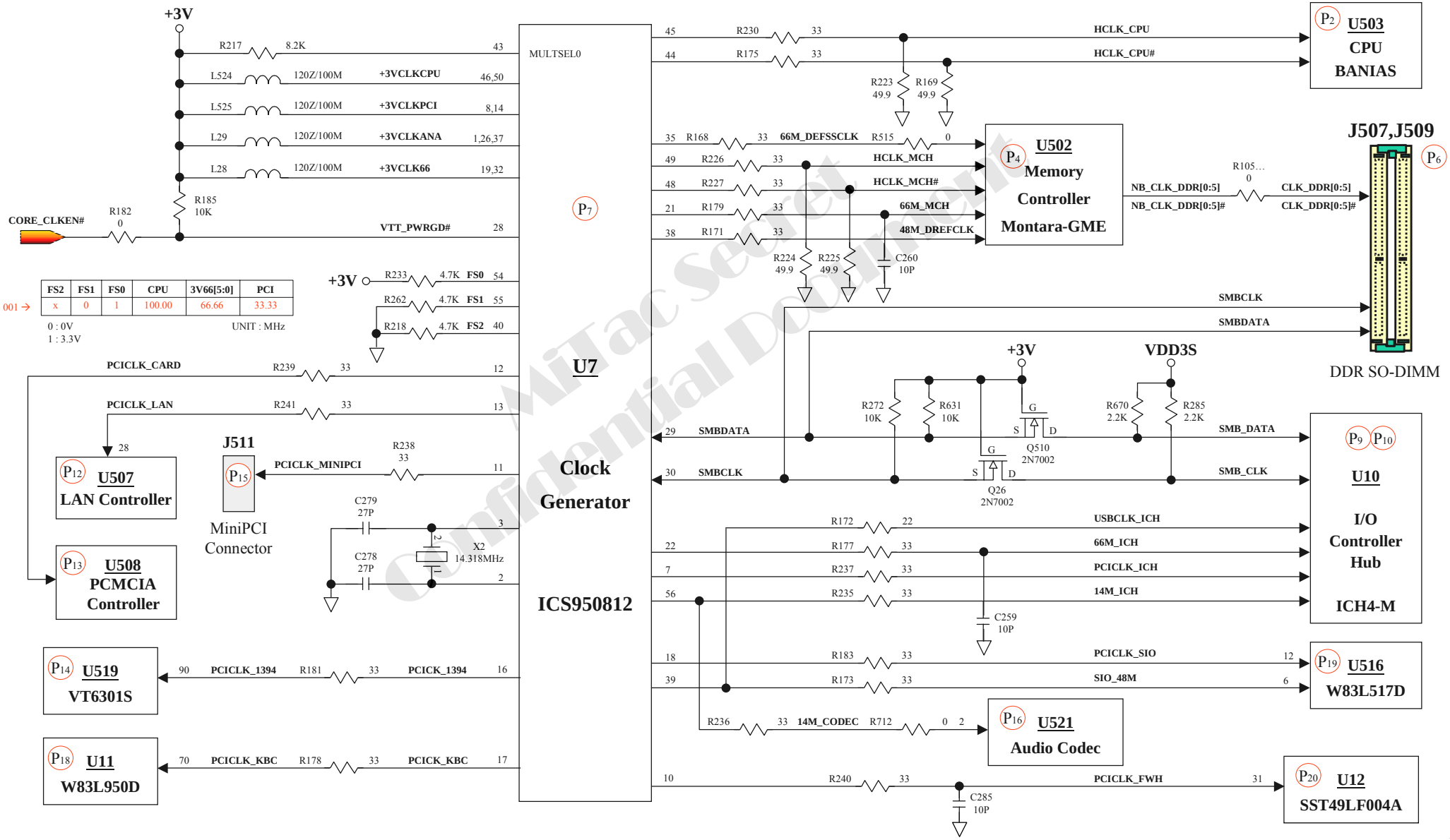
8.2 No Display-1

There is no display on both LCD and VGA monitor after power on.



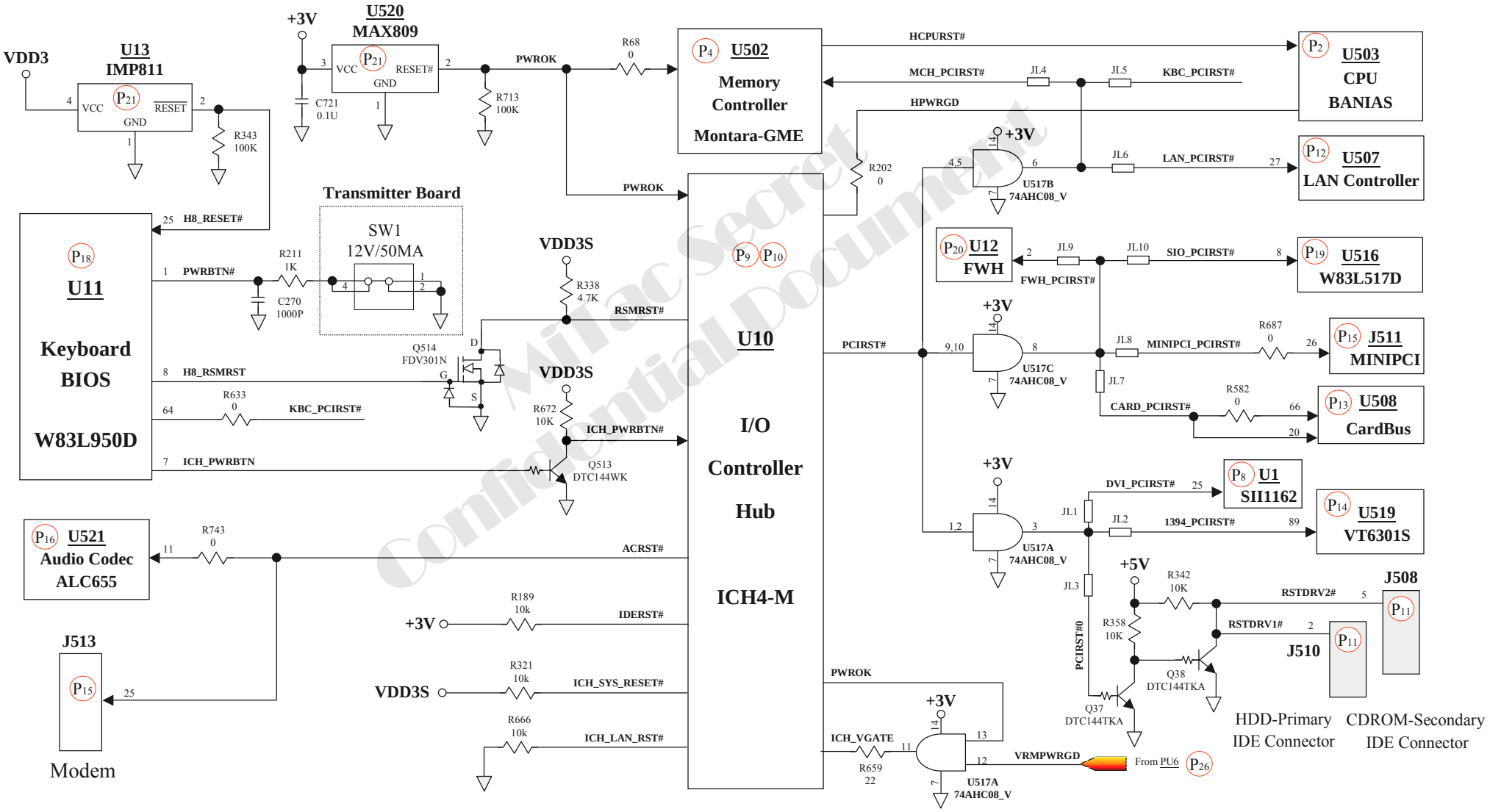
8.2 No Display-2

****** System Clock Check ******



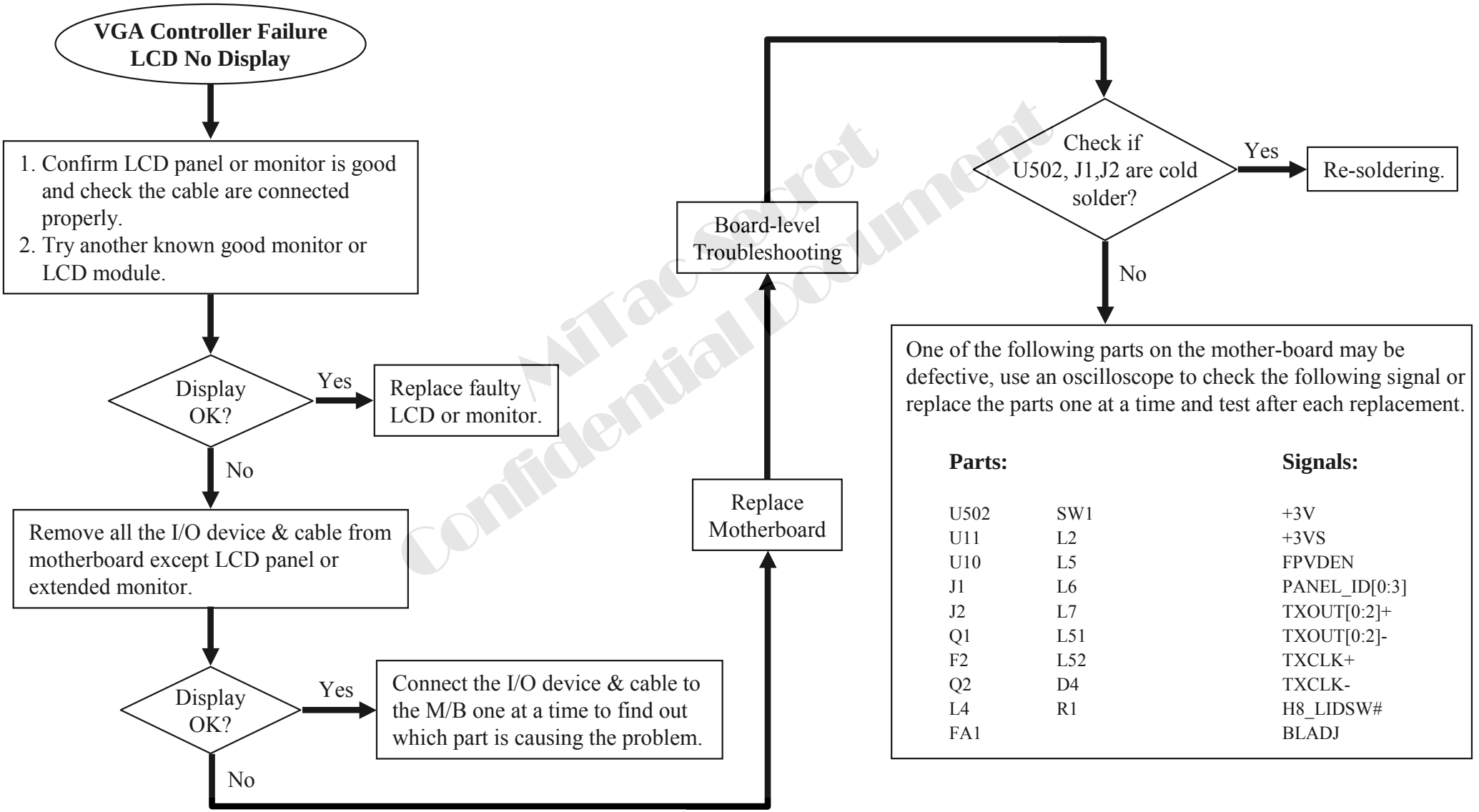
8.2 No Display-3

****** Power Good & Reset Circuit Check ******



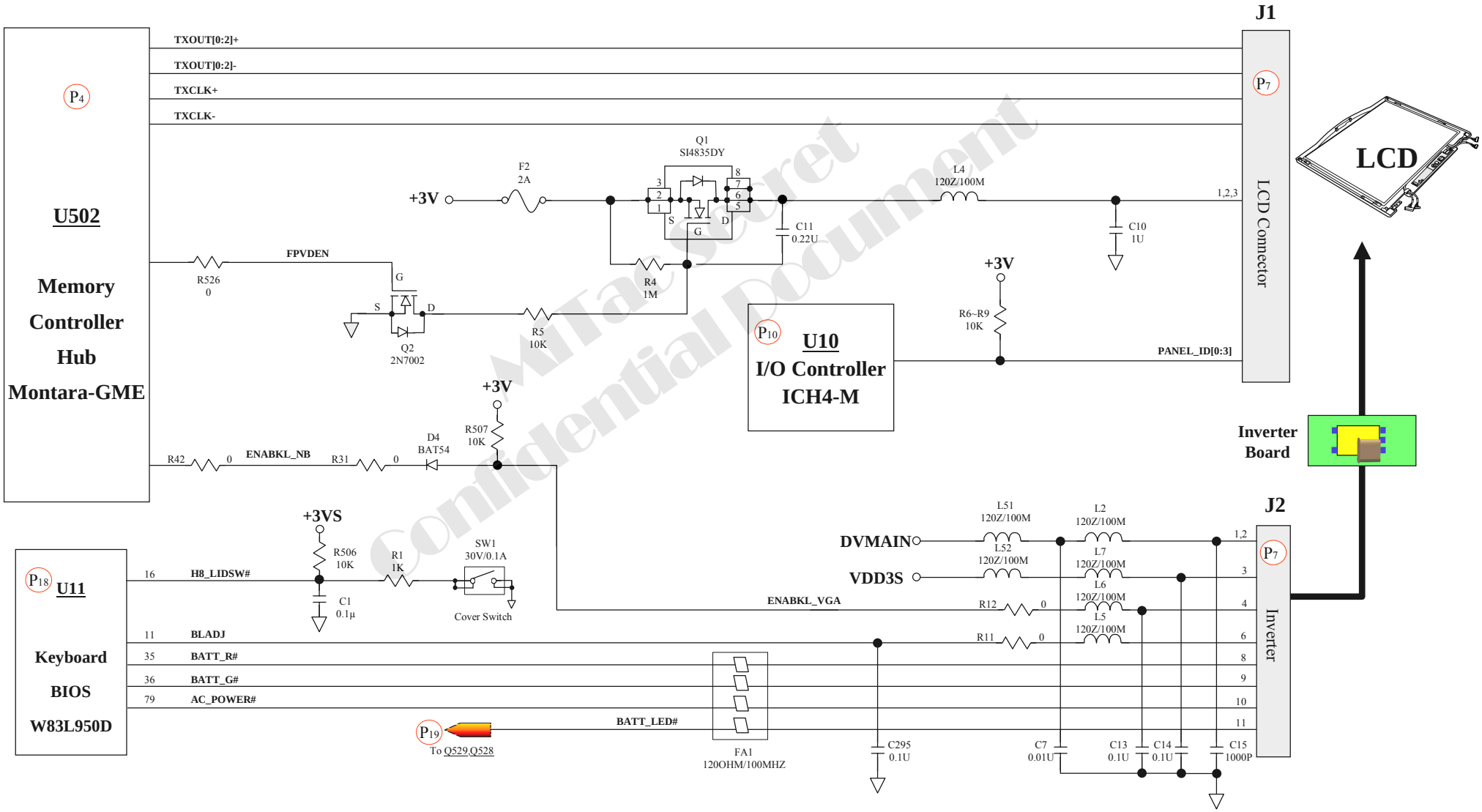
8.3 VGA Controller Failure LCD No Display-1

There is no display or picture abnormal on LCD although power-on-self-test is passed.



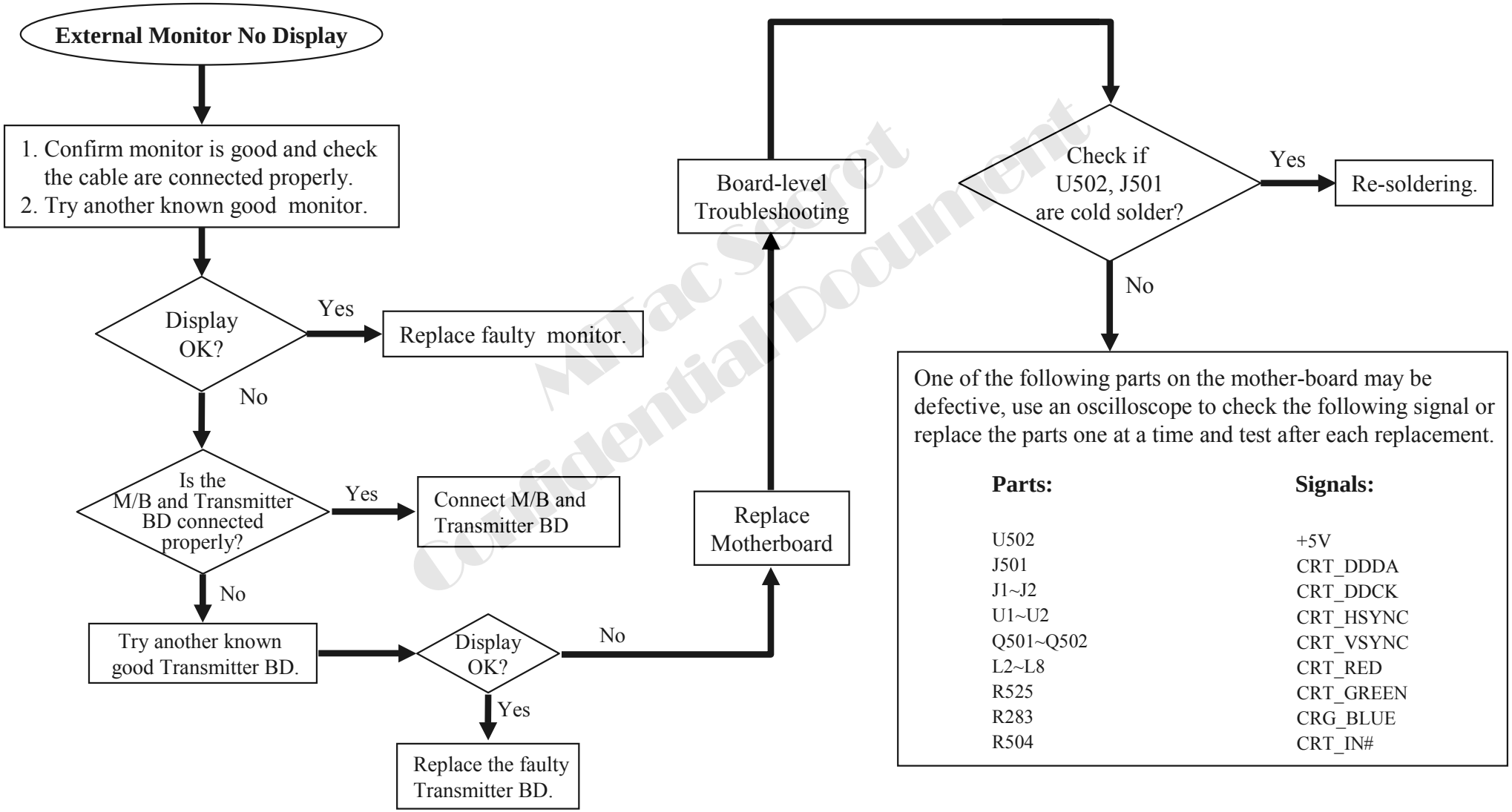
8.3 VGA Controller Failure LCD No Display-2

There is no display or picture abnormal on LCD although power-on-self-test is passed.



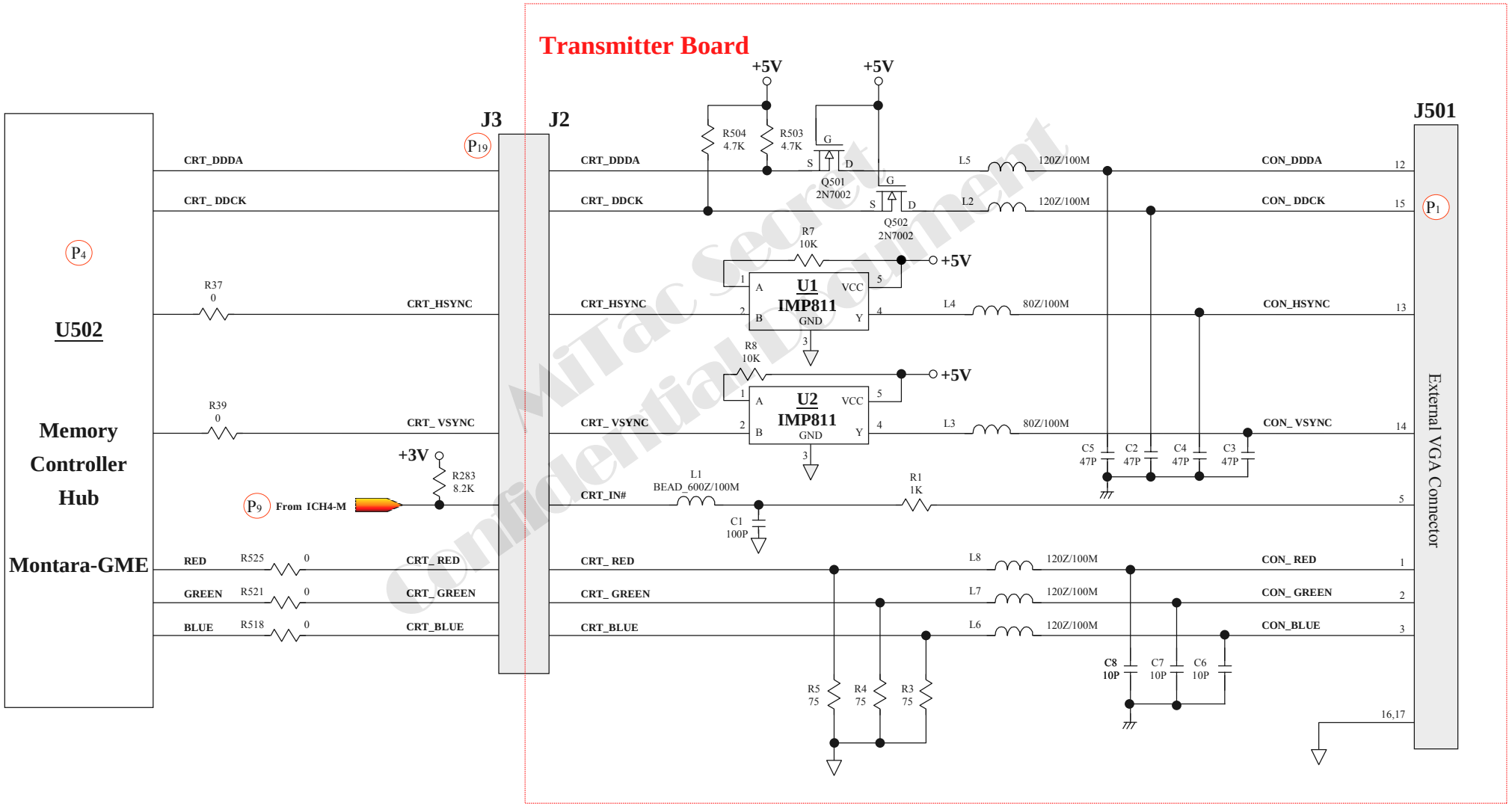
8.4 External Monitor No Display-1

There is no display or picture abnormal on CRT monitor, but it is OK for LCD.



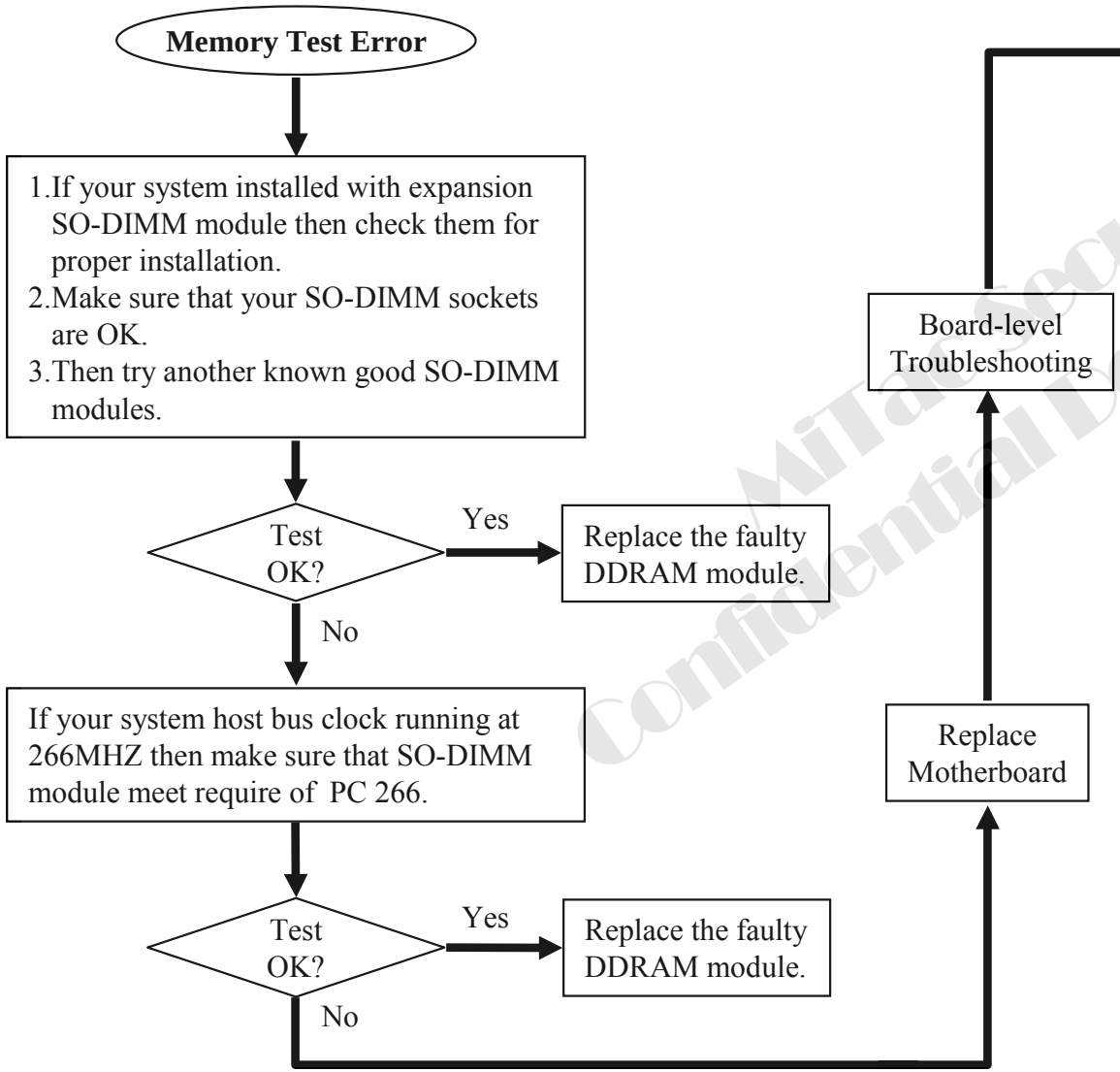
8.4 External Monitor No Display-2

There is no display or picture abnormal on CRT monitor, but it is OK for LCD.



8.5 Memory Test Error-1

Extend DDRAM is failure or system hangs up.

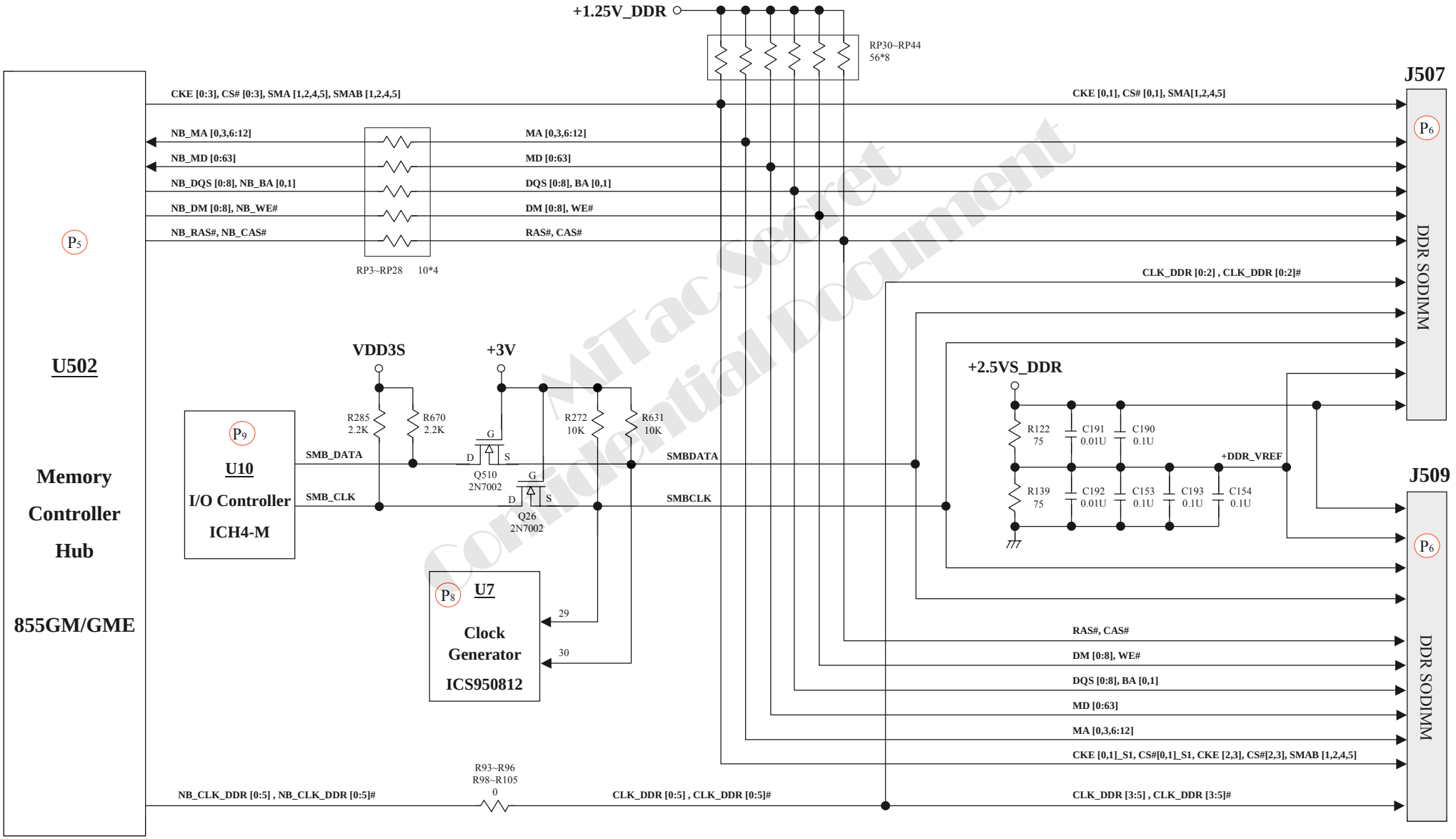


One of the following components or signals on the motherboard may be defective ,Use an oscilloscope to check the signals or replace the parts one at A time and test after each replacement.

Parts:	**Signals:**	
RP3~RP28	+1.25V_DDR	SMB_DATA
RP30~RP44	+2.5VS_DDR	SMB_CLK
R98~R105	+DDR_VREF	CLK_DDR [0:5]
R93~R96	CKE [0:3]	CLK_DDR [0:5]#
U502	CS# [0:3]	
U10	SMA [1,2,4,5]	
U7	SMAB [1,2,4,5]	
J507	NB_MA [0,3,6:12]	
J509	NB_MD [0:63]	
Q510	NB_DQS [0:8]	
Q26	NB_BA [0,1]	
R285	NB_DM [0:8]	
R670	NB_RAS#	
R272	NB_CAS#	
	NB_WE#	

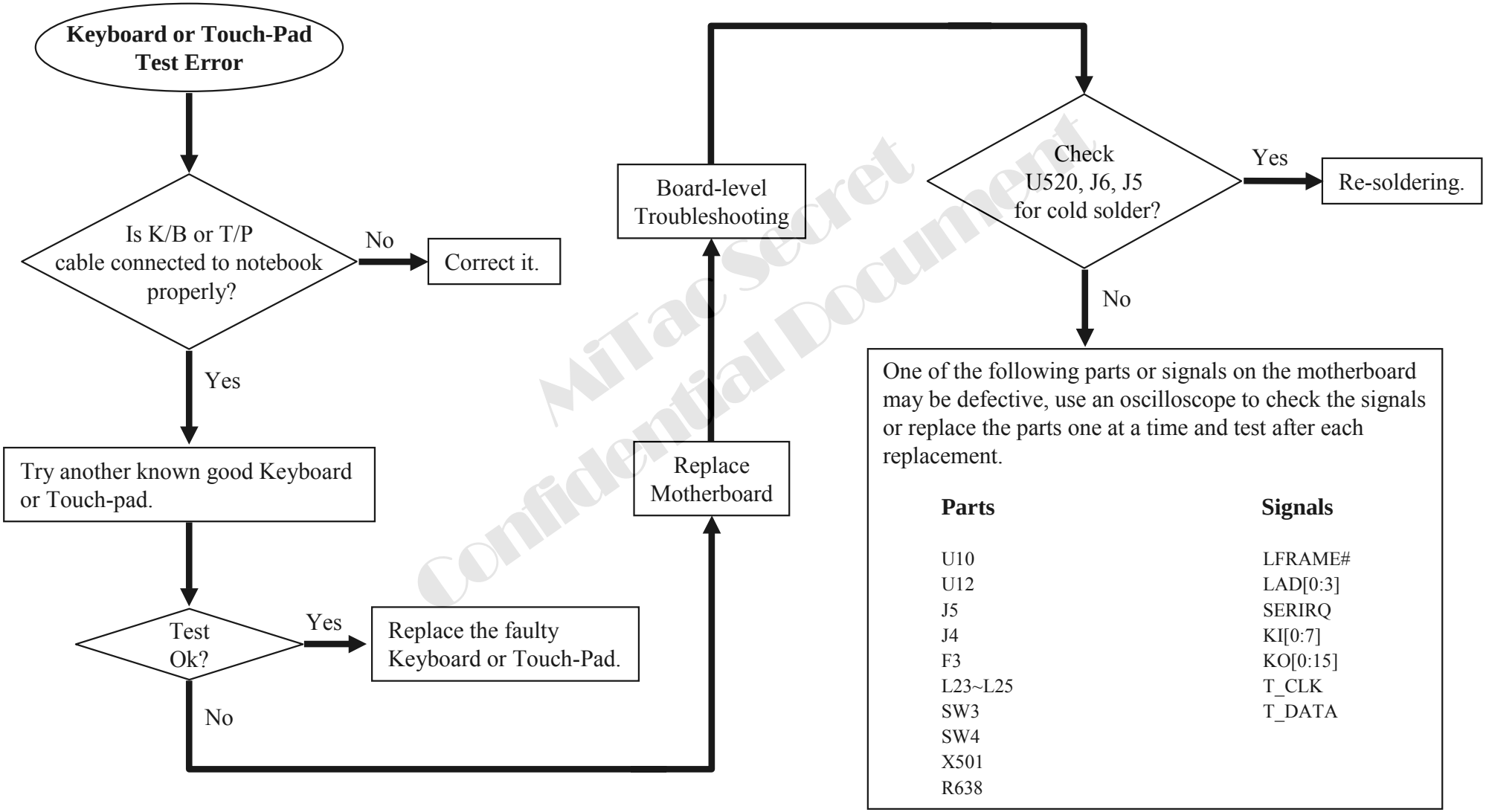
8.5 Memory Test Error-2

Extend DDRAM is failure or system hangs up.



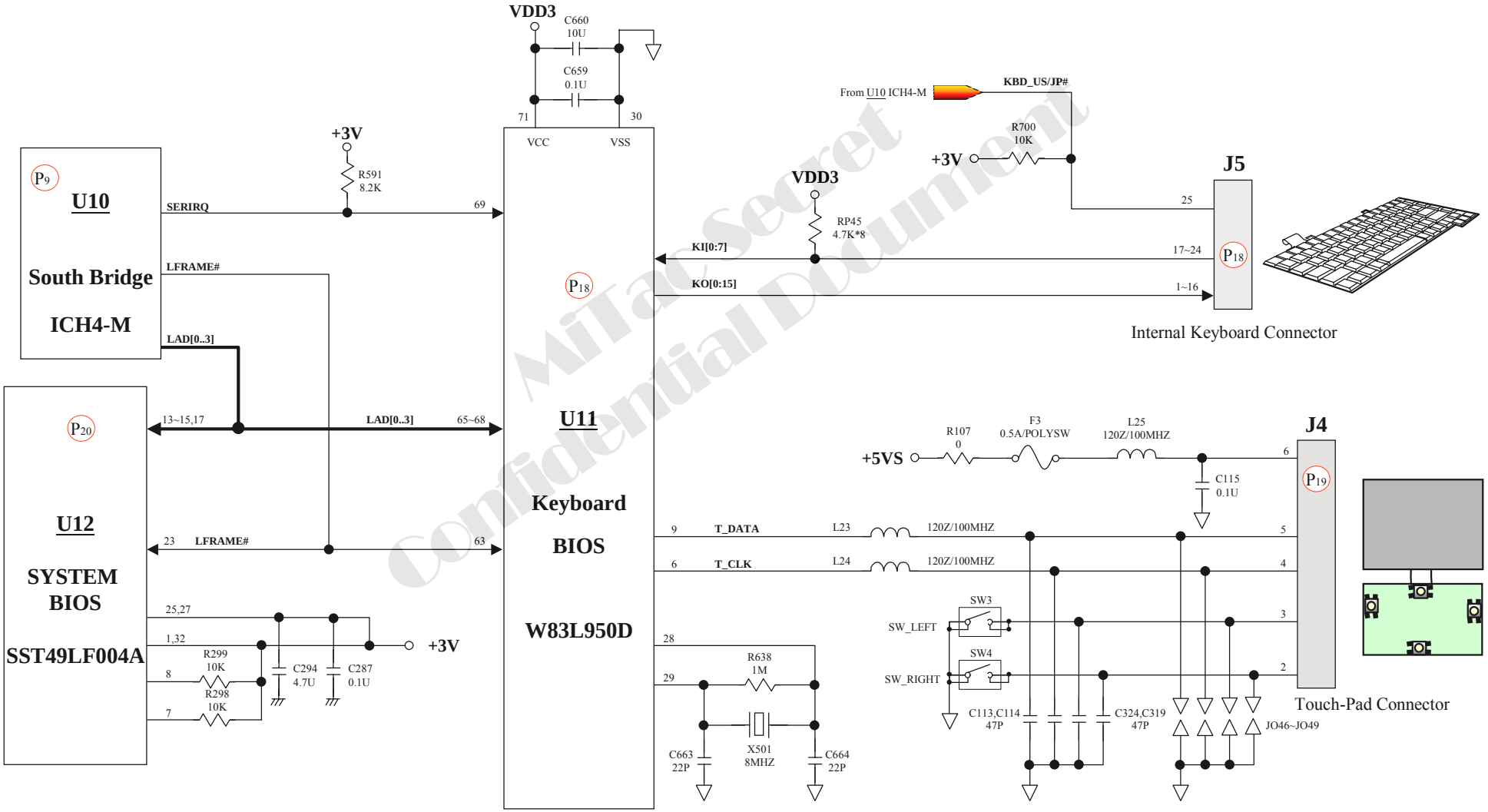
8.6 Keyboard (K/B) Touch-Pad (T/P) Test Error-1

Error message of keyboard or touch-pad failure is shown or any key does not work.



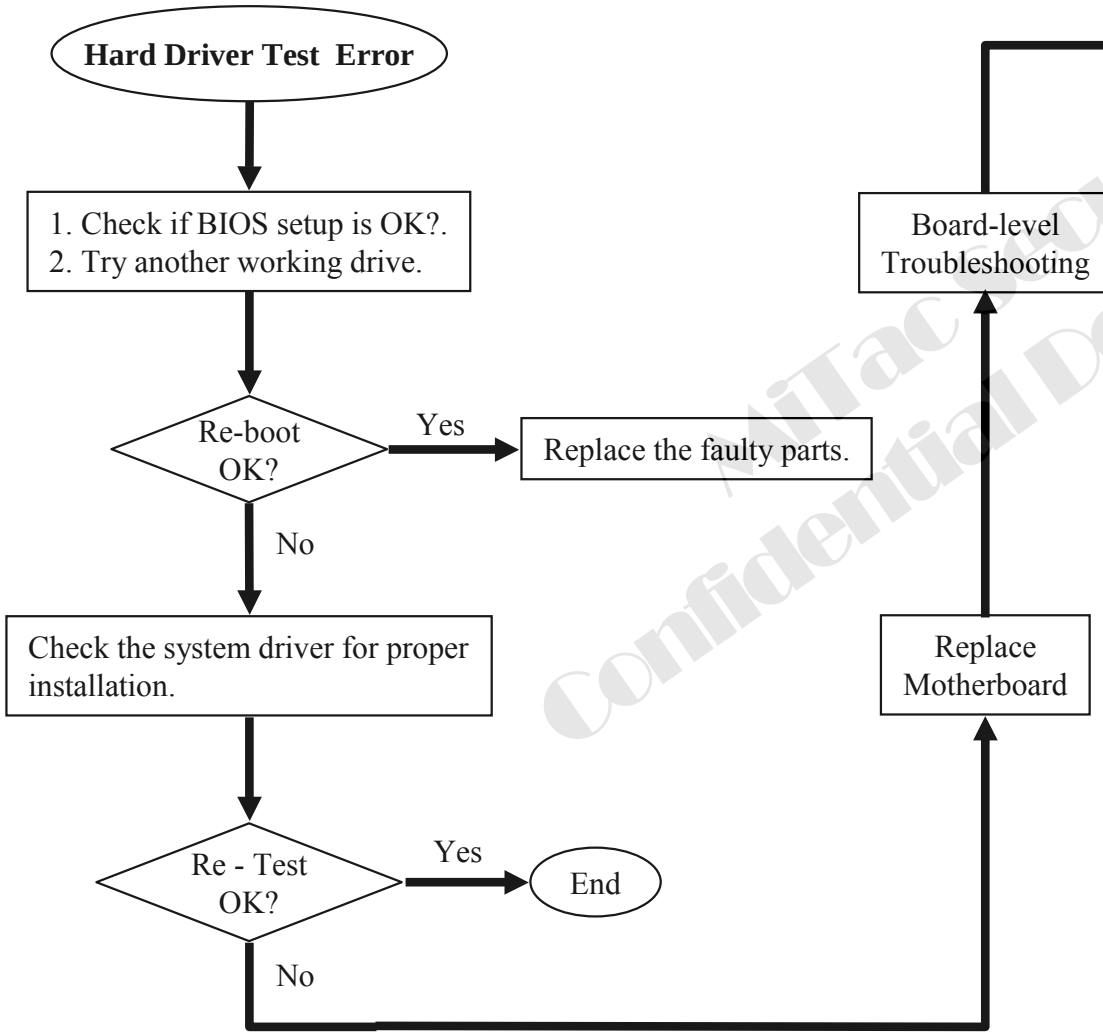
8.6 Keyboard (K/B) Touch-Pad (T/P) Test Error-2

Error message of keyboard or touch-pad failure is shown or any key does not work.



8.7 Hard Drive Test Error-1

Either an error message is shown, or the drive motor spins non-stop, while reading data from or writing data to hard disk.

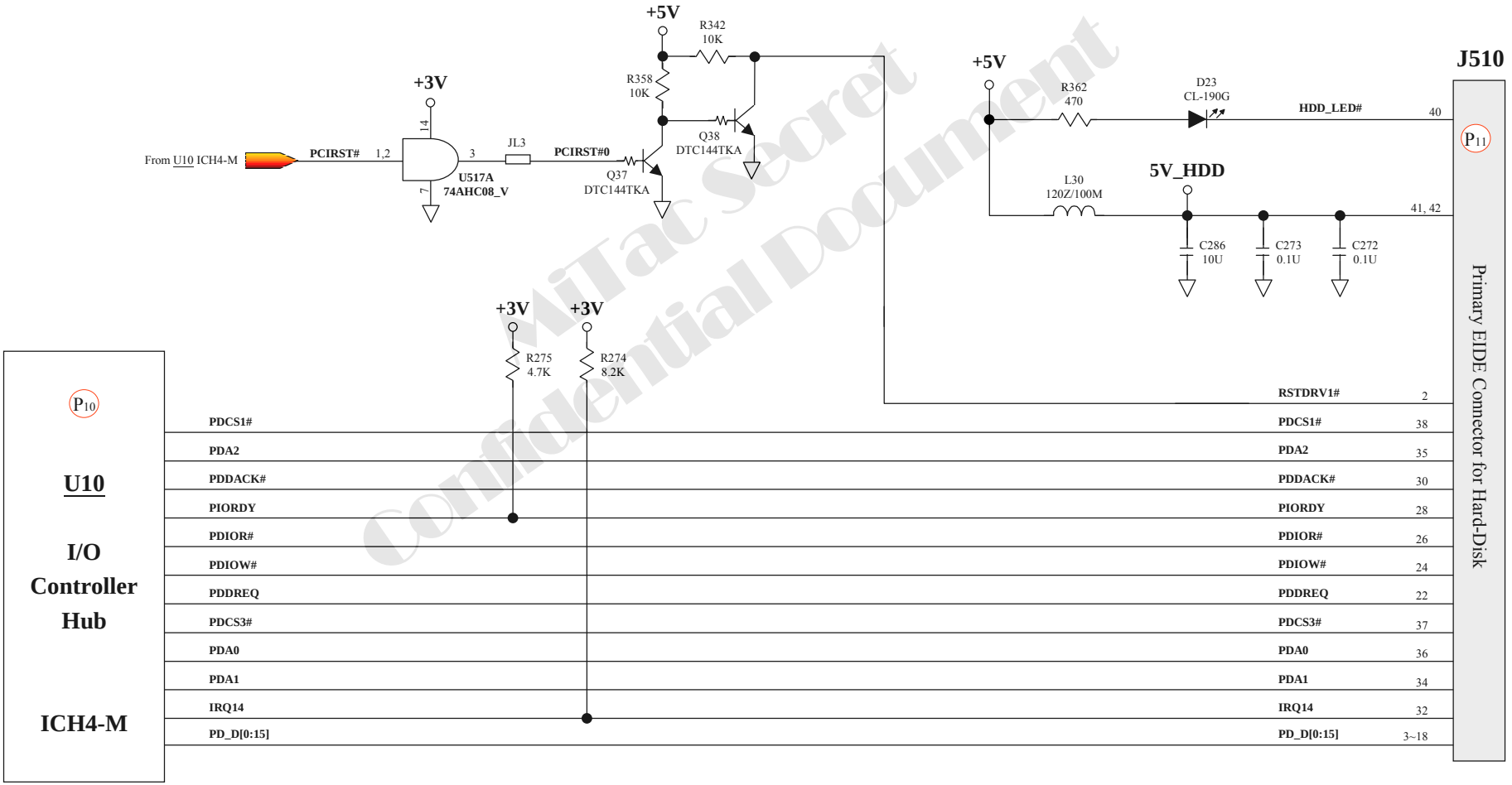


One of the following parts or signals on the motherboard may be defective, use an oscilloscope to check the signals or replace the parts one at a time and test after each replacement.

Parts:	**Signals:**
U517	+5V
U10	5V_HDD
J510	HDD_LED#
Q37	PD_D[0:15]
Q38	PCIRST#
R275	PDCS1#
L30	PDA[0:2]
D17	PDDACK#
R274	PIORDY
R342	PDIOR#
	PDIOW#
	PDDREQ
	IRQ14

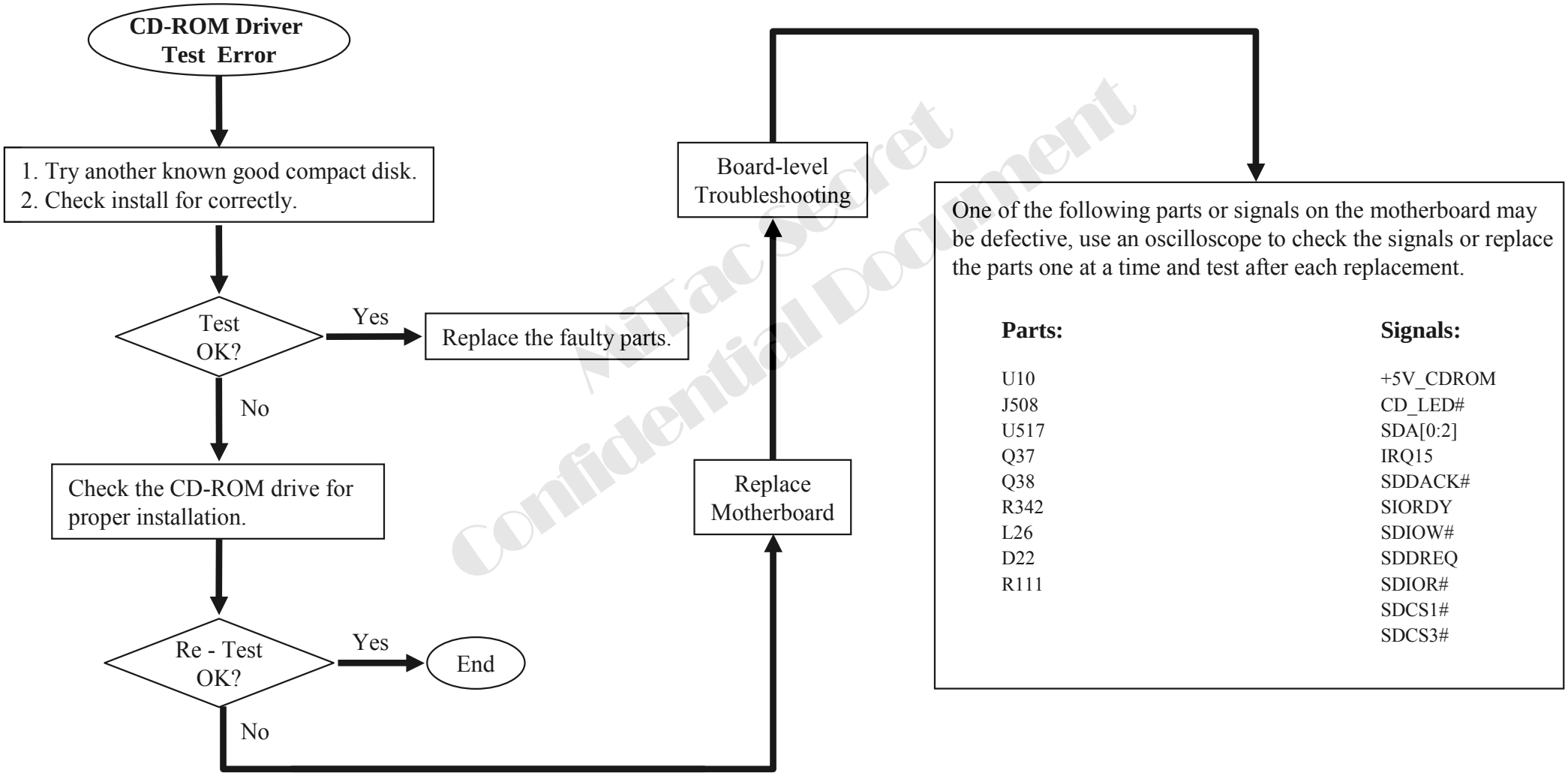
8.7 Hard Drive Test Error-2

Either an error message is shown, or the drive motor spins non-stop, while reading data from or writing data to hard disk.



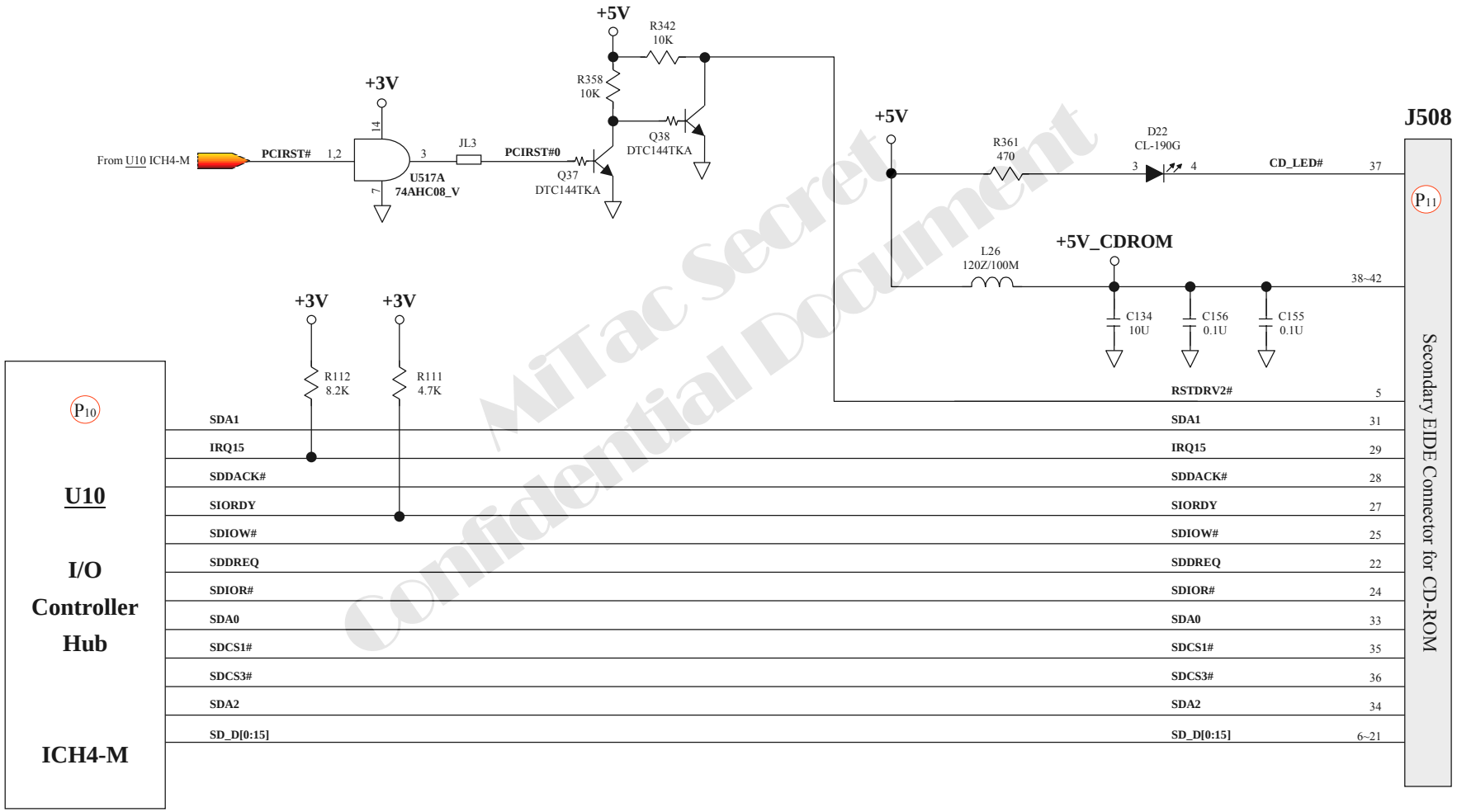
8.8 CD-ROM Drive Test Error-1

An error message is shown when reading data from CD-ROM drive.



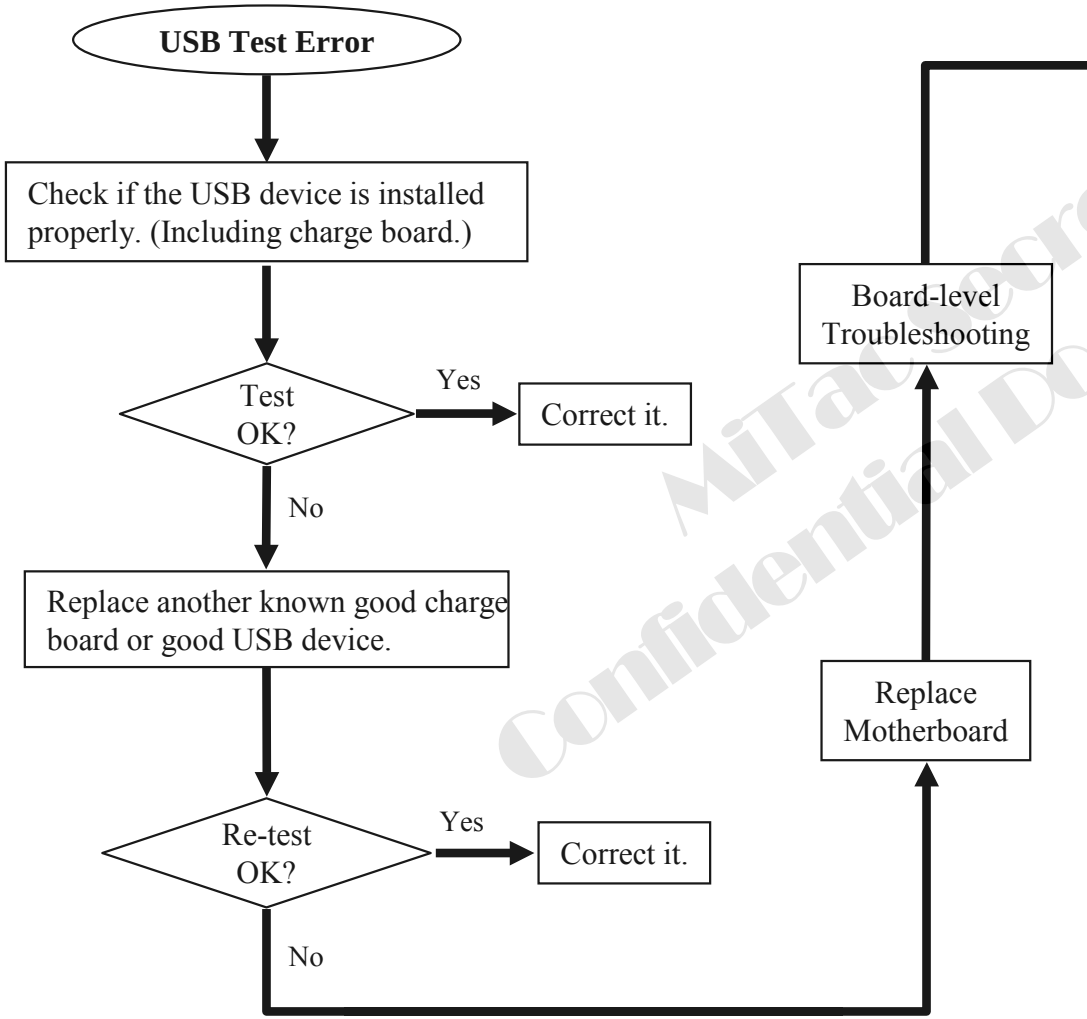
8.8 CD-ROM Drive Test Error-2

An error message is shown when reading data from CD-ROM drive.



8.9 USB Test Error-1

An error occurs when a USB I/O device is installed.

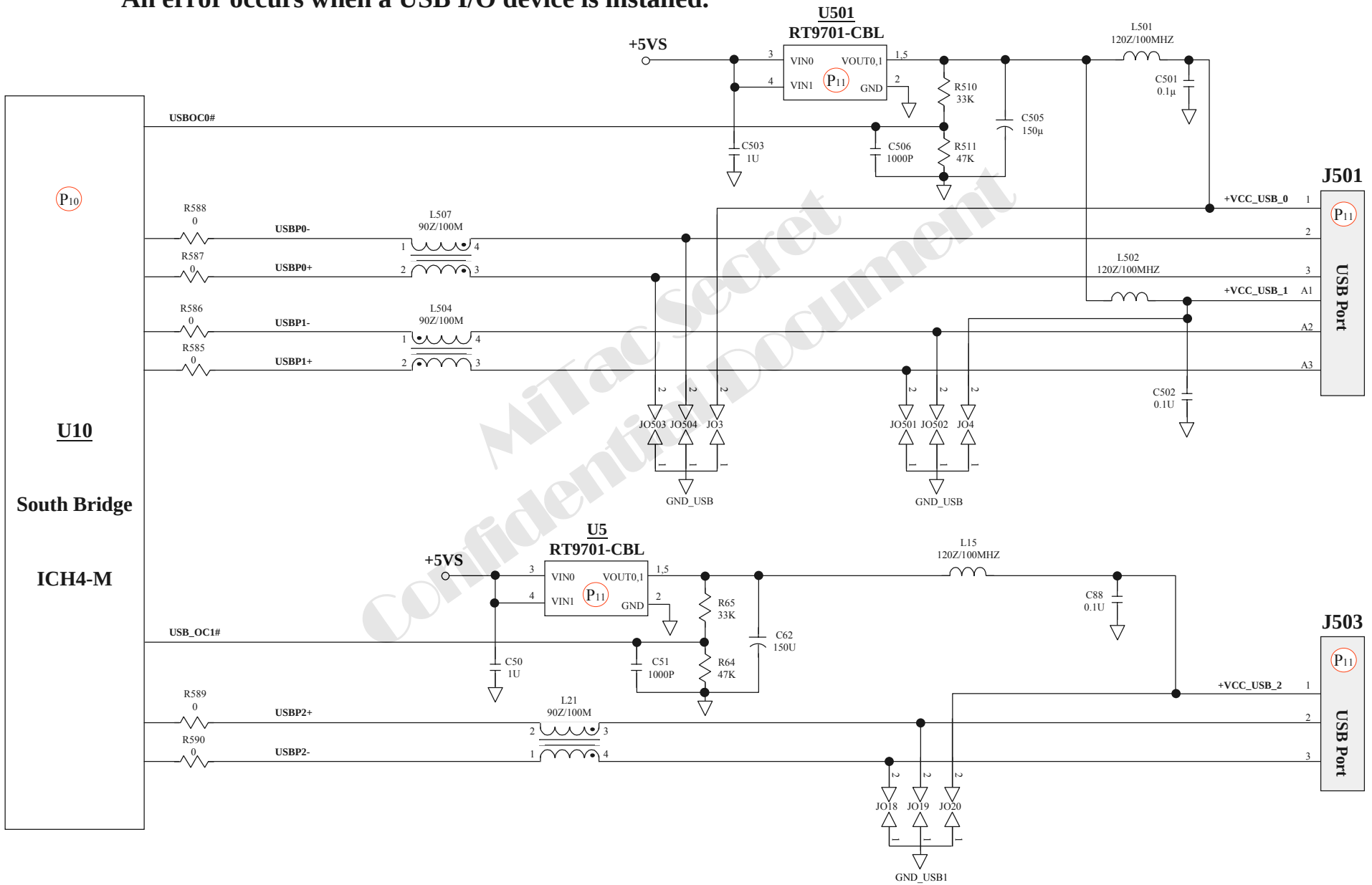


Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:		**Signals:**
U10	R588	+5VS
J501	R585	+VCC_USB_ [0:2]
J503	C88	USBP[0:2]+
U501	R510	USBP[0:2] -
U5	L15	USBOC1#
L507		USBOC0#
L504		
L501		
L502		
L21		

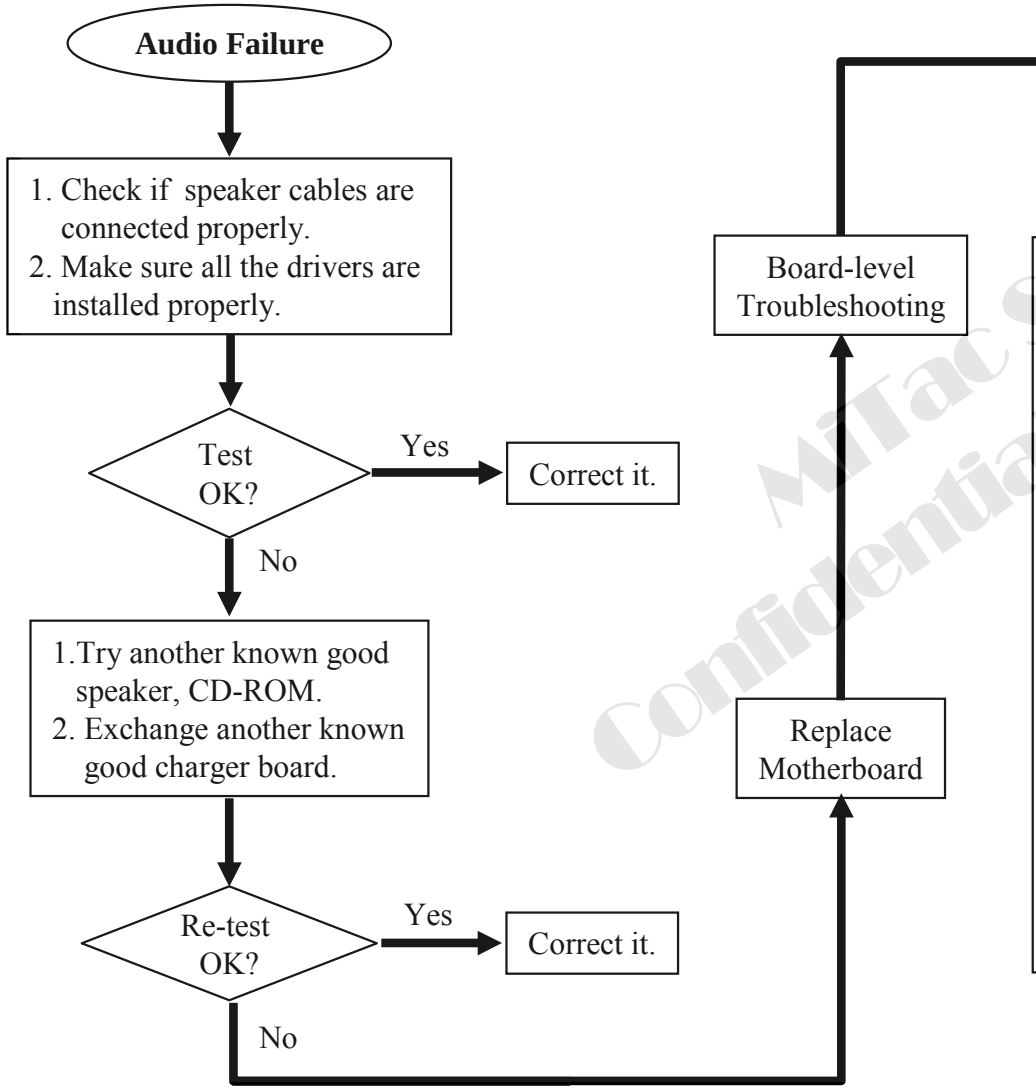
8.9 USB Test Error-2

An error occurs when a USB I/O device is installed.



8.10 Audio Failure-1

No sound from speaker after audio driver is installed.



Check the following parts for cold solder or one of the following parts on the motherboard may be defective,use an oscilloscope to check the following signal or replace parts one at a time and test after each replacement.

1.If no sound cause of line out, check the following parts & signals:

Parts:	Signals:
U10	AMP_RIGHT
U521	AMP_LEFT
U14	DEVICE_DECT
J515	DECT_HP#OPT
U524	
Q518	
Q33	
Q34	
L48	

2. If no sound cause of MIC, check the following parts & signals:

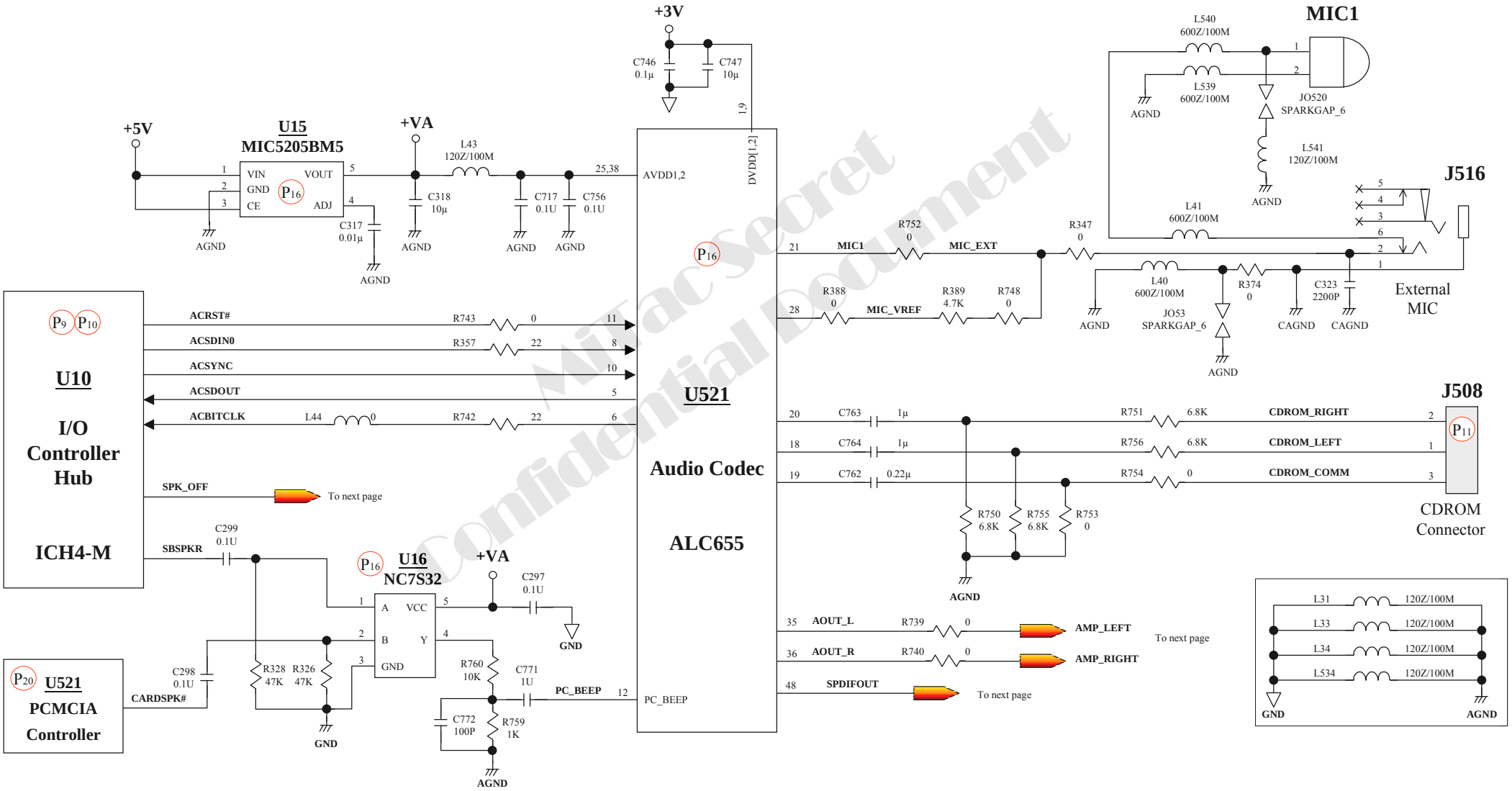
Parts:	Signals:
U10	+3V
U521	MIC1
J516	
L540	

3. If no sound cause of CD-ROM, check the following parts & signals:

Parts:	Signals:
U521	CDROM_LEFT
J508	CDROM_RIGHT
R751	CDROM_COMM
R756	
R754	

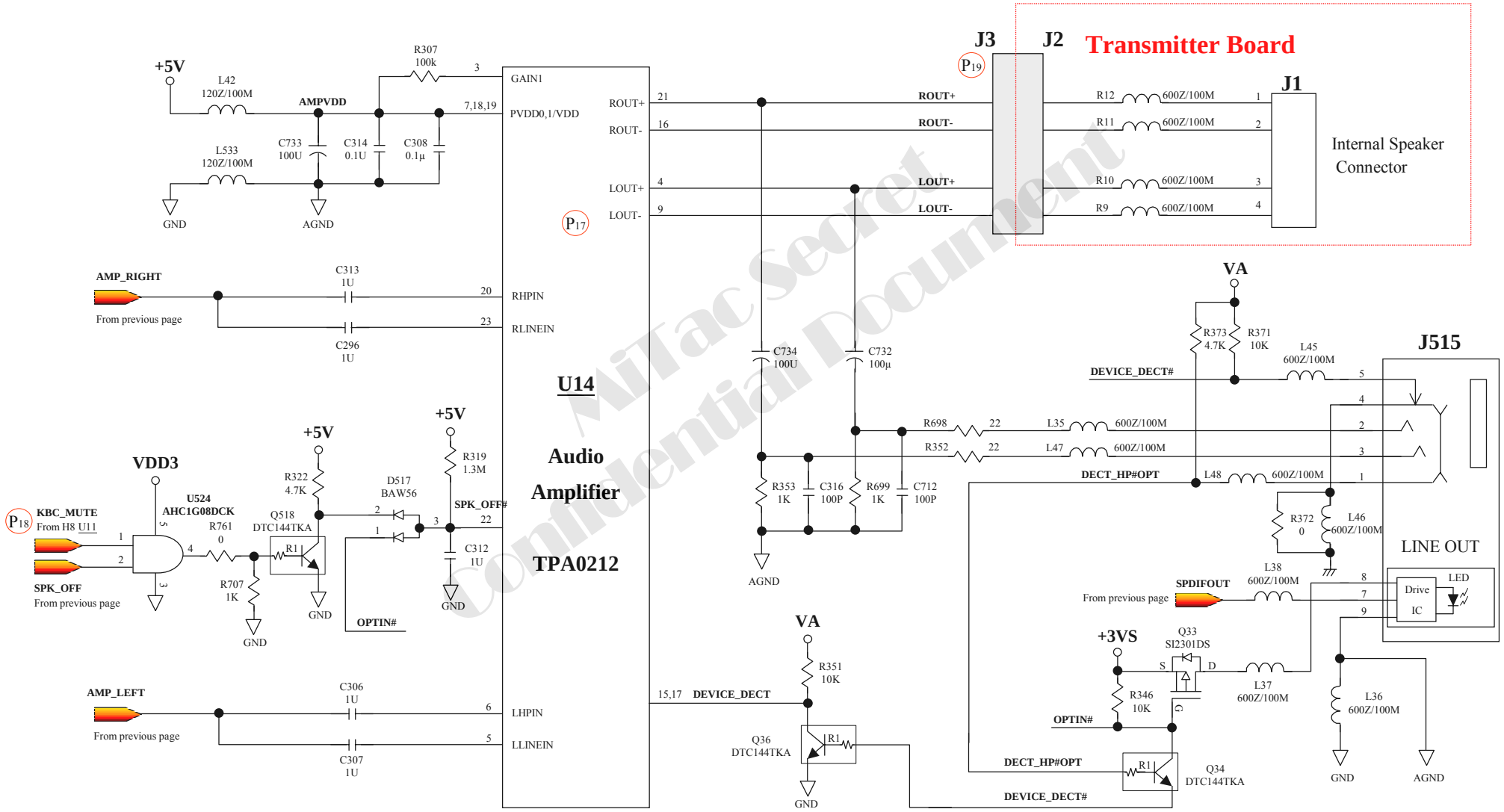
8.10 Audio Failure-2(Audio In)

No sound from speaker after audio driver is installed.



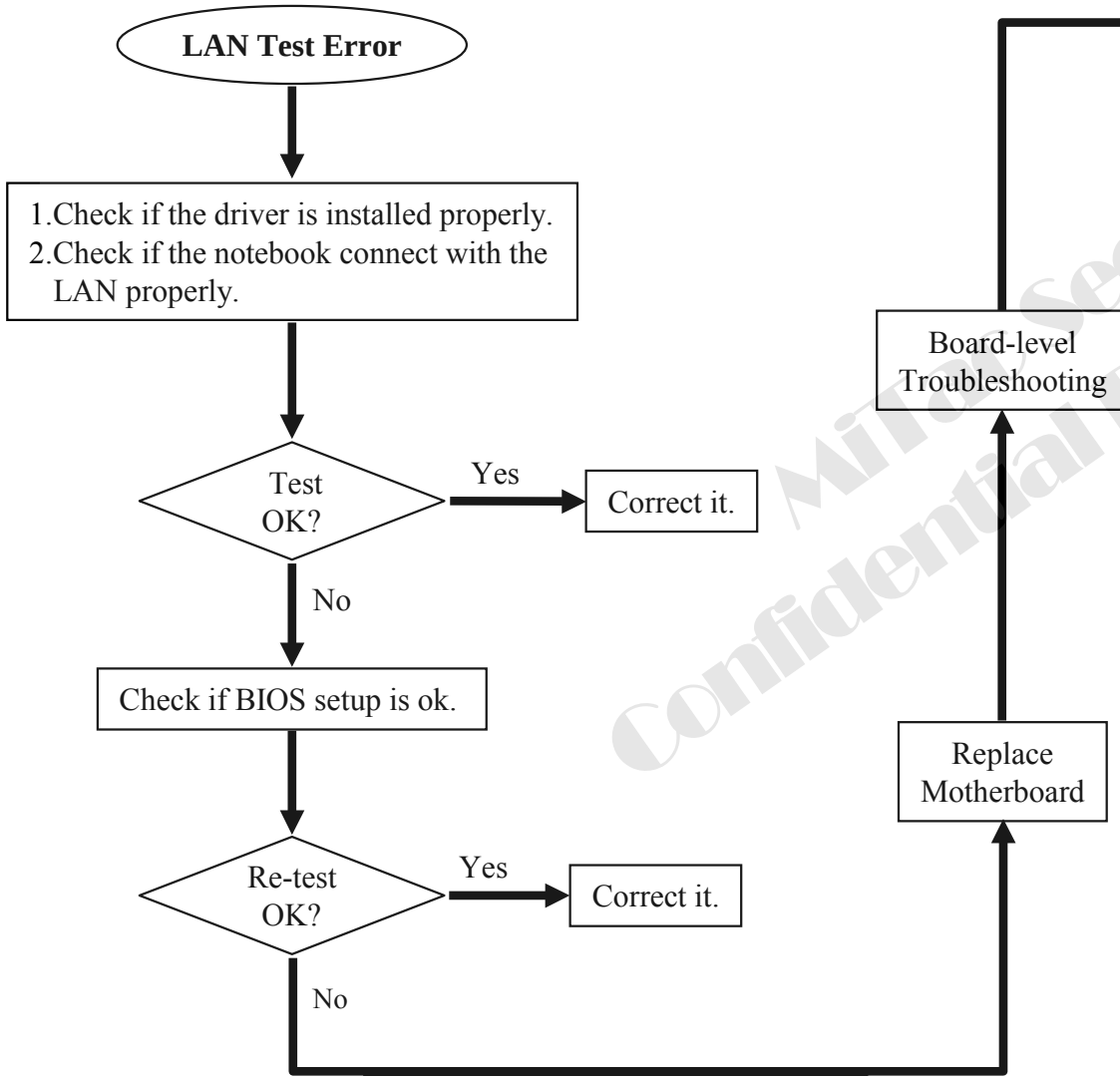
8.10 Audio Failure-3(Audio Out)

No sound from speaker after audio driver is installed.



8.11 LAN Test Error-1

An error occurs when a LAN device is installed.

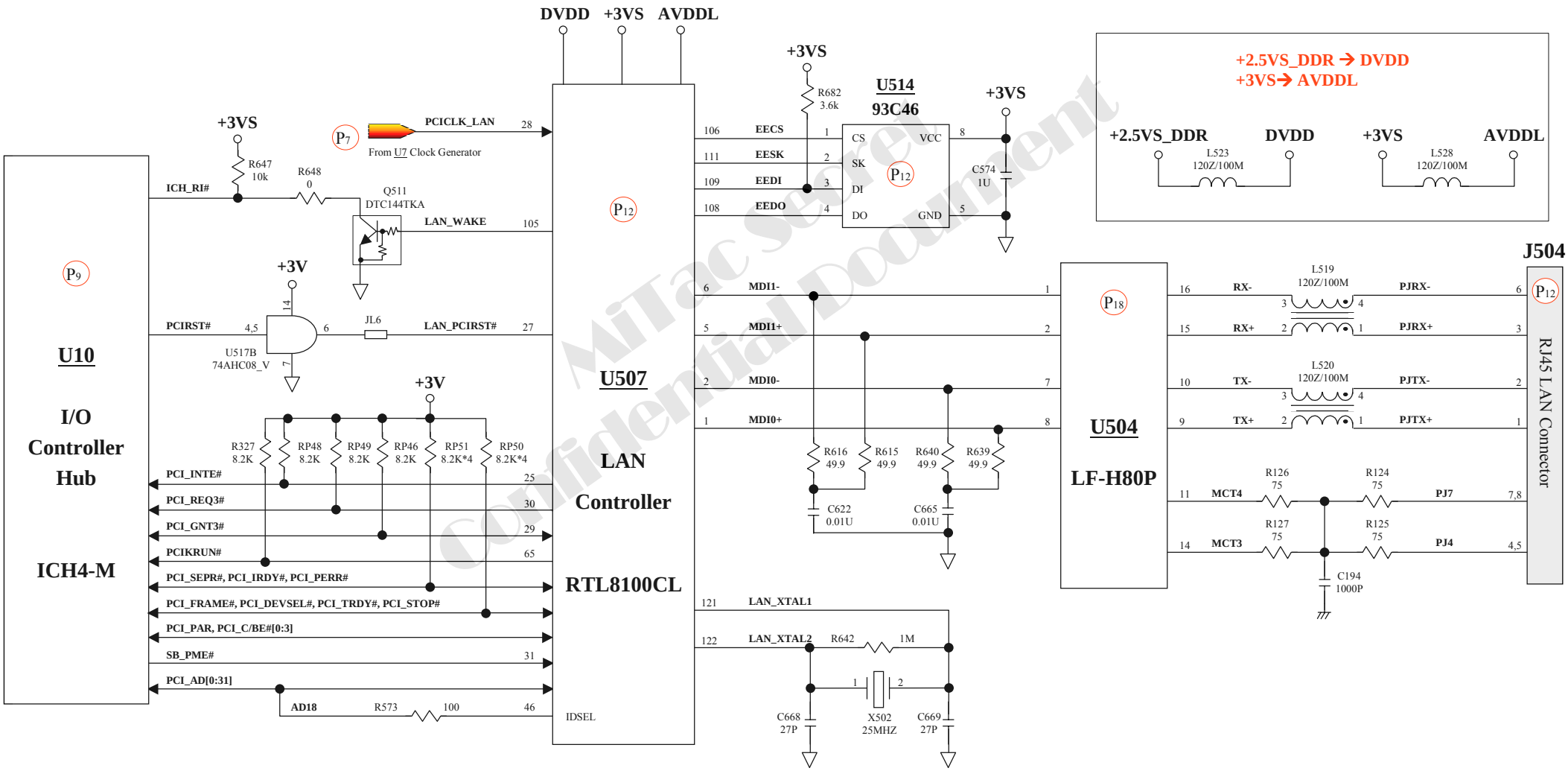


Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:	**Signals:**	
U10	+3VS	PCI_GNT3#
U507	DVDD	PCI_PAR
U517	AVDDL	PCI_AD[0:31]
U514	LAN_WAKE	PCI_C/BE#]0:3]
J504	PCIRST#	RJRX+
Q511	PCI_REQ3	RJRX-
L519	PCI_FRAME#	RJTX+
L520	PCI_DEVSEL#	RJTX-
R639	PCI_TRDY#	EECS
X502	PCI_IRDY#	EESK
	SB_PME#	EEDI
	PCI_STOP#	EEDO

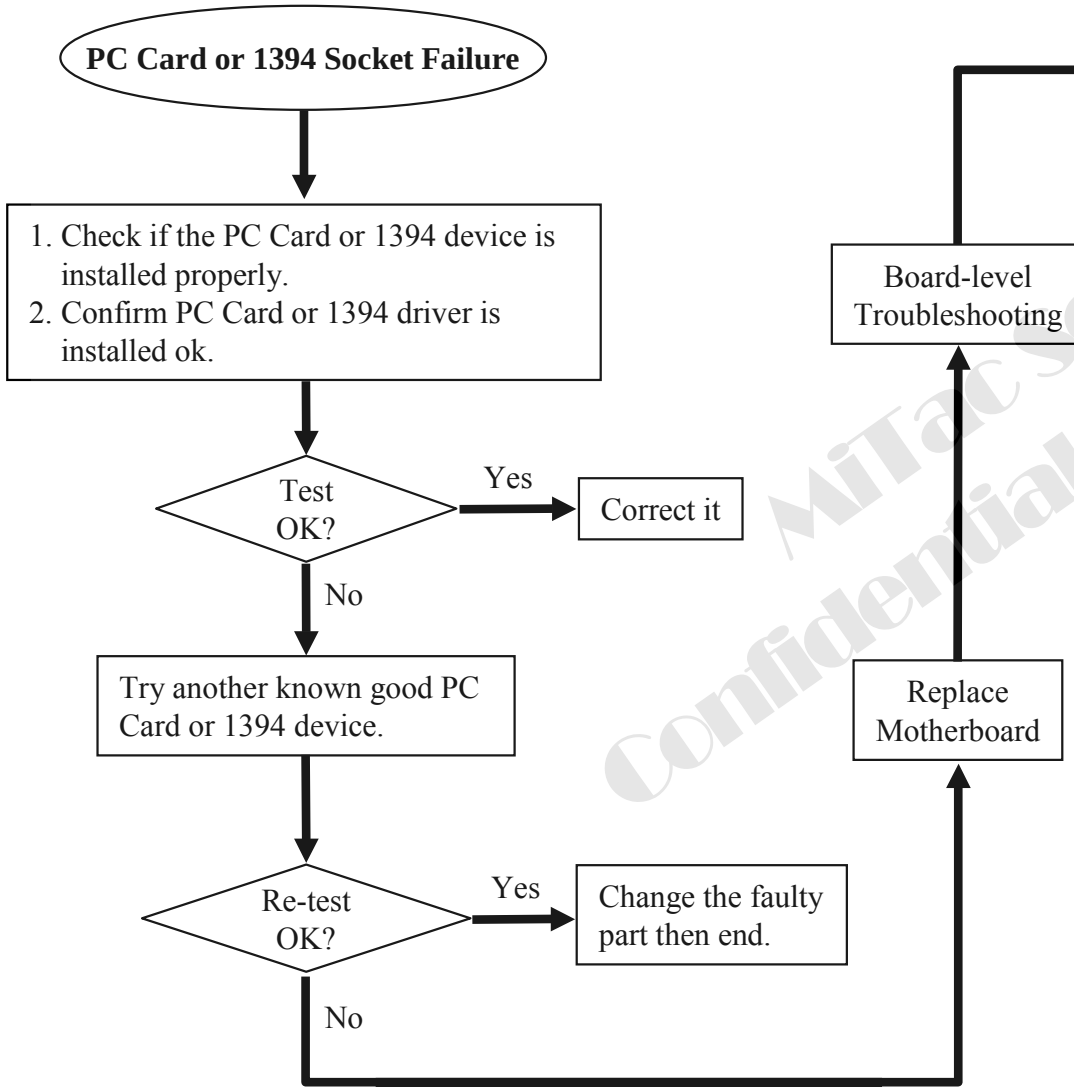
8.11 LAN Test Error-2

An error occurs when a LAN device is installed.



8.12 PC Card & 1394 Socket Failure-1

An error occurs when a PC card or 1394 device is installed.



Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:

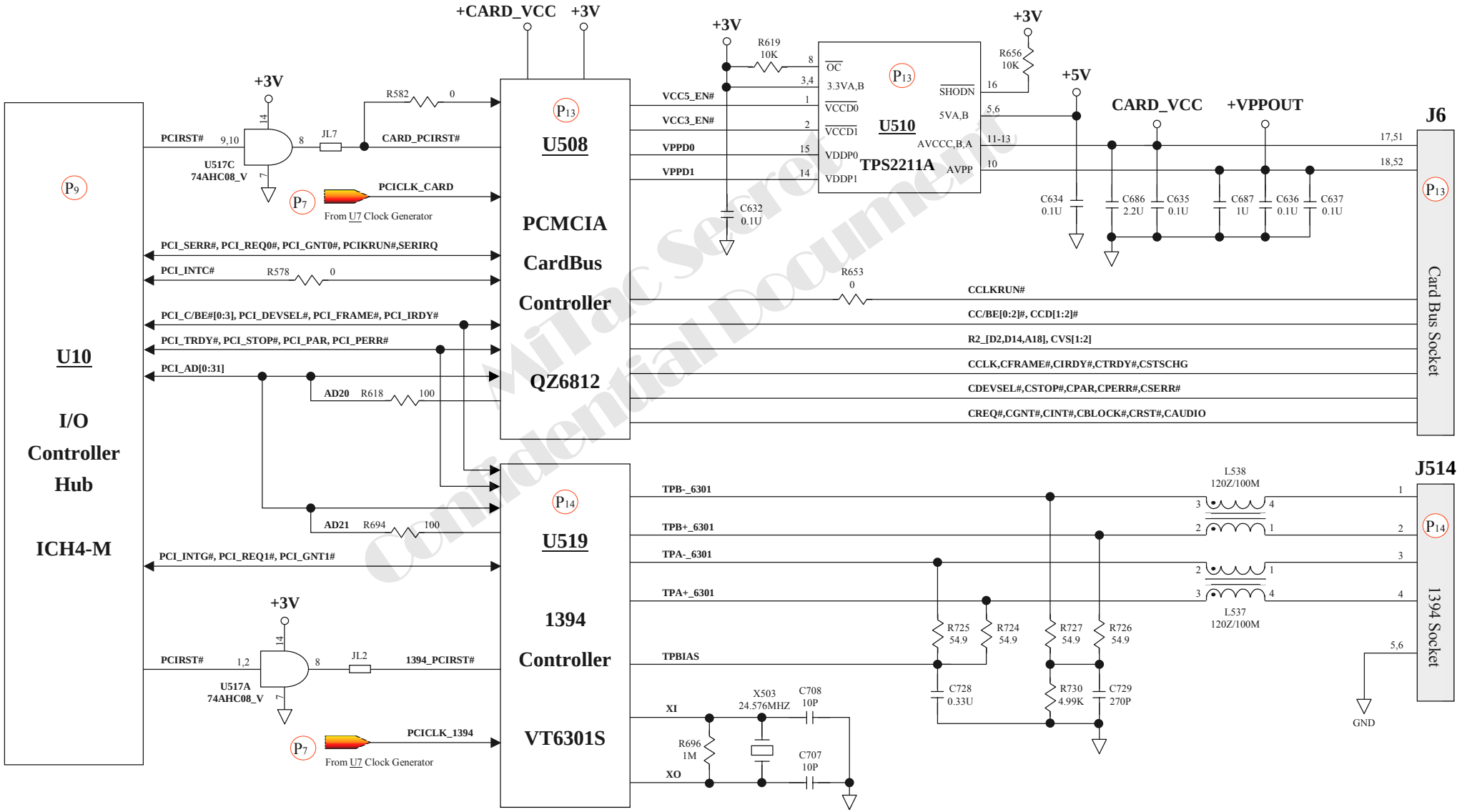
U10
U508
U519
J6
J514
U517
U510
L537
L538
X503
R694
R656
R725

Signals

PCICLK_CARD
PCIRST#
PCI_REQ0#
PCI_SERR#
PCI_PERR#
PCI_DEVSEL#
PCI_FRAME#
PCI_IRDY#
PCI_TRDY#
PCI_STOP#
PCLKRUN#
PCI_PME#
PCI_GNT1#
PCI_PAR
SERIRQ
PCI_AD[0:31]
PCI_C/BE#[0:3]
VCC5_EN#
VCC3_EN#
VPPD0
VPPD1
TPB-_6301
TPB+_6301
TPA-_6301
TPA+_6301
TPBIAS

8.12 PC Card & 1394 Socket Failure-2

An error occurs when a PC card or 1394 device is installed.



9. Spare Parts List - 1

Part Number	Description	Location(S)
221679920001	CARTON;NON-BRAND,8640C	
221679950002	CARD BOARD;TOP/BTM,PALLET,8640C	
221679950003	CARD BOARD;FRAME,PALLET,8640C	
221679950004	PARTITION;PALLET,8640C	
221680950001	PARTITION;EZ IN CARTON,8050	
222141720001	PE BUBBLE BAG;BATTERY,CAPRICORN	
222600020049	PE BAG;50*70MM,W/SEAL,COMMON	
222600020310	PE BAG;70X100MM,W/SEAL,COMMON	
222670820003	PE BAG;L560*W345,7521N	
222671330003	PE BAG;LCD BRACKET,STINGRAY	
222677700001	PE BUBBLE BAG;360x150MM,GHARIAL-	
222677700002	PE BUBBLE BAG;160x190MM,GHARIAL-	
224670830002	PALLET;1250*1080*130,7521N	
225600000276	TAPE;INSULATING,POLYESTER FILM,1	
227685400002	END CAP;L,EZ PACKING,8011	
227685400003	PAD;LCD/KB,8011	
227685400005	END CAP;R,EZ PACKING,8011	
242600000001	LABEL;PAL,20*5MM,COMMON	
242600000145	LABEL;10*10,BLANK,COMMON	
242600000157	LABEL;BAR CODE,125*65,COMMON	
242600000232	LABEL;6*6MM,GAL,BLANK,COMMON	
242600000378	LABEL;27*7MM,HI-TEMP 260'C	
242600000380	LABEL;10*8MM,BIOS,HI-TEMP 260	
242600000385	LABEL;27*10,LAN ID BAR CODE	
242600000433	LABEL;BLANK,11*5MM,COMMON	

Part Number	Description	Location(S)
242600000452	LABEL;BLANK,7MM*7MM,PRC	
242600000452	LABEL;BLANK,7MM*7MM,PRC	
242664800013	LABEL;CAUTION,INVERT BD,PITCHING	
242668300028	LABEL;32*7MM,POLYESTER FILM,HOPE	
242670800113	BFM-WORLD MARK;WINXP,7521N	
242677100002	CFM-NEC;CENTRINO,NB,LYNX-BANIAS	
242677100035	CFM-INTEL;STANDARD,CARTON,LYNX-B	
242677300001	LABLE;40*6mm,BLANK, WHITE,COMMON	
242679900005	LABEL;BAR CODE,(25*10MM)*12pcs,8	
242685400003	LABEL;ID1,BATT/WHITE,14.8V/2.2AH	
242685400009	LABEL;AGENCY-GLOBAL,WHITE,8011	
271001478301	RES;4.7 ,1/8W,5% ,0805,SMT,SN-(	R385
271002000301	RES;0 ,1/10W,5% ,0805,SMT	R501,R502
271002000301	RES;0 ,1/10W,5% ,0805,SMT	L31,L33,L34,L533,L534,R107,R3
271002100301	RES;10 ,1/10W,5% ,0805,SMT	PR56
271002102301	RES;1K ,1/10W,5% ,0805,SMT	R540,R63
271002472301	RES;4.7K ,1/10W,5% ,0805,SMT	PR502,PR503
271002478301	RES;4.7 ,1/10W,5% ,0805,SMT	PR520,PR525
271012000301	RES;0 ,1/8W,5% ,1206,SMT	PR45
271045087101	RES;.008 ,1W ,1% ,2512,SMT	PR511
271045107101	RES;.01 ,1W ,1% ,2512,SMT	PR501,PR512
271046017301	RES;.001,2W,5%,2512,CYNTEC,SMT	PR102
271046257101	RES;.025 ,2W ,1% ,2512,SMT,PRC	R18
271061000002	RES;0 ,1/16W,0402,SMT	R100,R101,R102,R103,R104,R105
271061100501	RES;10 ,1/16W,5% ,0402,SMT	R6

9. Spare Parts List - 2

Part Number	Description	Location(S)
271061101103	RES;100 ,1/16W,1% ,0402,SMT	R573,R618,R694
271061102105	RES;1K ,1/16W,1% ,0402,SMT	R15,R17,R30,R353,R599,R699
271061102303	RES;1K ,1/16W,5% ,0402,SMT	R1
271061102303	RES;1K ,1/16W,5% ,0402,SMT	R707,R728,R759
271061103501	RES;10K ,1/16W,5% ,0402,SMT	R7,R8
271061103501	RES;10K ,1/16W,5% ,0402,SMT	R13,R14,R185,R346,R351,R371,R
271061104501	RES;100K ,1/16W,5% ,0402,SMT	R307,R311
271061105501	RES;1M ,1/16W,5% ,0402,SMT	R642,R696
271061135101	RES;1.3M,1/16W,1%,0402,SMT	R319
271061152302	RES;15K ,1/16W,5% ,0402,SMT	R600
271061220501	RES;22 ,1/16W,5% ,0402,SMT	R352,R357,R698,R742
271061222501	RES;2.2K ,1/16W,5% ,0402,SMT	R26,R27,R508,R509
271061270103	RES;27,1/16W,1% ,0402,SMT	R518,R521,R525
271061300131	RES;300 ,1/16W,5% ,0402,SMT	R21,R22,R23,R25
271061330501	RES;33 ,1/16W,5% ,0402,SMT	R168,R171,R172,R173,R175,R177
271061391103	RES;390,1/16W,1% ,0402,SMT	R219
271061432212	RES;43.2K,1/16W,1%,0402,SMT	R606,R655
271061472501	RES;4.7K ,1/16W,5% ,0402,SMT	R503,R504
271061472501	RES;4.7K ,1/16W,5% ,0402,SMT	R218,R233,R262,R322,R323,R373
271061473501	RES;47K ,1/16W,5% ,0402,SMT	R326,R328
271061499012	RES;49.9 ,1/16W,1% ,0402,SMT	R169,R223,R224,R225,R615,R616
271061499212	RES;4.99K,1/16W,1% ,0402,SMT	R730
271061549011	RES;54.9 ,1/16W,1% ,0402,SMT	R724,R725,R726,R727
271061562102	RES;5.6K ,1/16W, 1%,0402,SMT	R602
271061562501	RES;5.6K ,1/16W,5% ,0402,SMT	R736

Part Number	Description	Location(S)
271061634211	RES;6.34K,1/16W,1% ,0402,SMT	R729
271061682501	RES;6.8K ,1/16W,5% ,0402,SMT	R750,R751,R755,R756
271061750501	RES;75 ,1/16W,5% ,0402,SMT	R124,R125,R126,R127
271061753101	RES;75,1/16W,1%,0402,SMT	R3,R4,R5
271061753101	RES;75,1/16W,1%,0402,SMT	R122,R139
271061822501	RES;8.2K ,1/16W,5% ,0402,SMT	R217
271071000002	RES;0 ,1/16W,5% ,0603,SMT	R3
271071000002	RES;0 ,1/16W,5% ,0603,SMT	L36,L40,L44,L46,L521,L522,PR1
271071100302	RES;10 ,1/16W,5% ,0603,SMT	PR19,PR504,PR524,R243
271071101101	RES;100 ,1/16W,1% ,0603,SMT	R543,R546,R547,R623,R652,R67,
271071101301	RES;100 ,1/16W,5% ,0603,SMT	R37
271071102102	RES;1K ,1/16W,1% ,0603,SMT	PR528,PR55,PR84,R550
271071102302	RES;1K ,1/16W,5% ,0603,SMT	R19
271071102302	RES;1K ,1/16W,5% ,0603,SMT	R1,R142,R208,R211,R49,R52,R53
271071102302	RES;1K ,1/16W,5% ,0603,SMT	R35,R39,R43,R46
271071103101	RES;10K ,1/16W,1% ,0603,SMT	PR65,PR80,PR82,PR96,R554,R55
271071103302	RES;10K ,1/16W,5% ,0603,SMT	PR29,PR30,R131,R140,R186,R188
271071103302	RES;10K ,1/16W,5% ,0603,SMT	R3,R4
271071104101	RES;100K ,1/16W,1% ,0603,SMT	PR107,PR13,PR18,PR48
271071104101	RES;100K ,1/16W,1% ,0603,SMT	R7
271071104302	RES;100K ,1/16W,5% ,0603,SMT	R13
271071104302	RES;100K ,1/16W,5% ,0603,SMT	PR2,PR509,PR67,PR79,PR8,PR9,
271071104302	RES;100K ,1/16W,5% ,0603,SMT	R11,R15,R2,R38,R44,R48
271071105301	RES;1M ,1/16W,5% ,0603,SMT	PR3,PR38,PR39,PR513,PR522,PR
271071105301	RES;1M ,1/16W,5% ,0603,SMT	R40

9. Spare Parts List - 3

Part Number	Description	Location(S)
271071106301	RES;10M ,1/16W,5% ,0603,SMT	R270,R271
271071121211	RES;12.1K,1/16W,1% ,0603,SMT	PR47
271071122102	RES;1.2K ,1/16W,1% ,0603,SMT	PR33,PR98
271071124311	RES;124K ,1/16W,1% ,0603,SMT	PR64
271071127011	RES;127 ,1/16W,1% ,0603,SMT	R40
271071131101	RES;130 ,1/16W,1% ,0603,SMT	R198
271071133111	RES;1.33K,1/16W,1% ,0603,SMT	PR4
271071137211	RES;13.7K,1/16W,1% ,0603,SMT	PR87
271071151101	RES;150 ,1/16W,1% ,0603,SMT	R162,R196,R199,R514,R537,R557
271071152101	RES;1.5K ,1/16W,1% ,0603,SMT	R27,R30,R32
271071152302	RES;1.5K ,1/16W,5% ,0603,SMT	R215,R516
271071169111	RES;1.69K,1/16W,1% ,0603,SMT	PR515
271071169211	RES;16.9K,1/16W,1% ,0603,SMT	R1
271071182213	RES;18.2,1/16W,1%,0603,SMT	R187
271071182214	RES;18.2K,1/16W,1%,0603,SMT	PR97
271071183101	RES;18K ,1/16W,1% ,0603,SMT	PR41
271071184301	RES;180K ,1/16W,5% ,0603,SMT	R669,R744
271071191314	RES;191K ,1/16W,1% ,0603,SMT	PR63
271071196111	RES;1.96K,1/16W,1% ,0603,SMT	PR61
271071201301	RES;200 ,1/16W,5% ,0603,SMT	PR101,PR103,R206
271071202102	RES;2K ,1/16W,1% ,0603,SMT	R551
271071202301	RES;2K ,1/16W,5% ,0603,SMT	R21
271071203101	RES;20K ,1/16W,1% ,0603,SMT	PR507
271071203302	RES;20K ,1/16W,5% ,0603,SMT	R308
271071204302	RES;200K ,1/16W,5% ,0603,SMT	R212

Part Number	Description	Location(S)
271071220101	RES;22 ,1/16W,1% ,0603,SMT	R621
271071221301	RES;220 ,1/16W,5% ,0603,SMT	R364,R366,R369
271071221302	RES;22 ,1/16W,5% ,0603,SMT	R632,R659,R718,R721
271071222302	RES;2.2K ,1/16W,5% ,0603,SMT	R285,R670
271071224301	RES;220K ,1/16W,5% ,0603,SMT	R4
271071225301	RES;2.2M,1/16W,5% ,0603,SMT	R34,R36
271071226311	RES;226K ,1/16W,1% ,0603,SMT	PR508
271071244301	RES;240K ,1/16W,5% ,0603,SMT	R41
271071249111	RES;2.49K,1/16W,1% ,0603,SMT	PR76,PR77
271071261212	RES;26.1K,1/16W,1%,0603,SMT	PR42
271071267211	RES;26.7K,1/16W,1% ,0603,SMT	PR90
271071272301	RES;2.7K ,1/16W,5% ,0603,SMT	R290,R329
271071273101	RES;27K ,1/16W,1% ,0603,SMT	R11
271071274111	RES;2.74K,1/16W,1% ,0603,SMT	PR53
271071274911	RES;27.4 ,1/16W,1% ,0603,SMT	R108,R120,R163,R512,R538
271071283101	RES;28K ,1/16W,1% ,0603,SMT	PR12
271071301011	RES;301 ,1/16W,1% ,0603,SMT	R513,R536
271071301311	RES;301K ,1/16W,1% ,0603,SMT	R23,R5
271071301311	RES;301K ,1/16W,1% ,0603,SMT	PR22
271071330302	RES;33 ,1/16W,5% ,0603,SMT	R563
271071331101	RES;330 ,1/16W,1% ,0603,SMT	R84
271071331301	RES;330 ,1/16W,5% ,0603,SMT	R133,R214,R259
271071333301	RES;33K ,1/16W,5% ,0603,SMT	PR510,R510,R65
271071344101	RES;340K ,1/16W,1% ,0603,SMT	R42
271071357211	RES;35.7K,1/16W,1% ,0603,SMT	PR526

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Part Number	Description	Location(S)
271071362101	RES;3.6K ,1/16W,1% ,0603,SMT	R682
271071374211	RES;37.4K,1/16W,1% ,0603,SMT	PR44
271071374812	RES;37.4 ,1/16W,1% ,0603,SMT	R549
271071390302	RES;39 ,1/16W,5% ,0603,SMT	R159
271071394301	RES;390K ,1/16W,5% ,0603,SMT	R7,R9
271071402811	RES;40.2 ,1/16W,1% ,0603,SMT	R531
271071432111	RES;4.32K,1/16W,1% ,0603,SMT	R17
271071470301	RES;47 ,1/16W,5% ,0603,SMT	R210
271071471101	RES;470 ,1/16W,1% ,0603,SMT	R33,R35,R37
271071471302	RES;470 ,1/16W,5% ,0603,SMT	PR105,PR40,PR517,PR521,PR62,
271071471302	RES;470 ,1/16W,5% ,0603,SMT	R1,R14,R17
271071472101	RES;4.7K ,1/16W,1% ,0603,SMT	PR16
271071472302	RES;4.7K ,1/16W,5% ,0603,SMT	PR10,PR11,R111,R258,R275,R298
271071473301	RES;47K ,1/16W,5% ,0603,SMT	R286,R324,R511,R64
271071474301	RES;470K ,1/16W,5% ,0603,SMT	PR1,R506
271071478101	RES;4.7 ,1/16W,1% ,0603,SMT	PR81
271071487011	RES;487 ,1/16W,1% ,0603,SMT,MUS	R197
271071487811	RES;48.7 ,1/16W,1% ,0603,SMT	R200
271071499111	RES;4.99K,1/16W,1% ,0603,SMT	PR15,PR51,PR514,PR95,R18
271071499211	RES;49.9K,1/16W,1% ,0603,SMT	PR20
271071499311	RES;499K ,1/16W,1% ,0603,SMT	PR49
271071499811	RES;49.9 ,1/16W,1% ,0603,SMT	R544,R66,R82
271071510301	RES;51 ,1/16W,5% ,0603,SMT	R118,R154,R155,R157,R158
271071511101	RES;510 ,1/16W,1% ,0603,SMT	PR527
271071512101	RES;5.1K ,1/16W,1% ,0603,SMT	PR52

Part Number	Description	Location(S)
271071549811	RES;54.9 ,1/16W,1% ,0603,SMT	R109,R119,R91,R92
271071560301	RES;56 ,1/16W,5% ,0603,SMT	R147,R166,R205,R207,R246,R247
271071561101	RES;560 ,1/16W,1% ,0603,SMT	R2,R31,R34,R36
271071562201	RES;56.2K,1/16W,1% ,0603,SMT	PR31,PR36,PR523
271071562301	RES;5.6K ,1/16W,5% ,0603,SMT	R45
271071604112	RES;604,1/16W,1% ,0603,SMT	R556,R559
271071604311	RES;604K ,1/16W,1% ,0603,SMT	PR46
271071604811	RES;60.4 ,1/16W,1% ,0603,SMT	R552,R553
271071619111	RES;6.19K,1/16W,1% ,0603,SMT	PR78
271071625301	RES;6.2M ,1/16W,5% ,0603,SMT	PR32
271071649111	RES;6.49K,1/16W,1% ,0603,SMT	PR43
271071665211	RES;66.5K,1/16W,1% ,0603,SMT	PR5
271071681301	RES;680 ,1/16W,5% ,0603,SMT	R164
271071681813	RES;68.1,1/16W,1%,0603,SMT	R545R545R545R545R545R545
271071698311	RES;698K ,1/16W,1% ,0603,SMT	R5
271071713102	RES;715 ,1/16W,1% ,0603,SMT	R35
271071753301	RES;75K ,1/16W,5% ,0603,SMT	R15
271071787311	RES;787K ,1/16W,1% ,0603,SMT	PR14
271071806211	RES;80.6K,1/16W,1% ,0603,SMT	PR50
271071822301	RES;8.2K ,1/16W,5% ,0603,SMT	R112,R257,R274,R277,R278,R279
271072151101	RES;150 ,1/10W,1% ,0603,SMT	R25
271072287011	RES;287 ,1/10W,1% ,0603,SMT	R548
271072383011	RES;383 ,1/10W,1% ,0603,SMT	R24
271571330301	RP;33*8 ,16P ,1/16W,5% ,1606,SM	RP1,RP2
271571560302	RP;56*8 ,16P,1/16W,5% ,1606,SMT	RP30,RP31,RP32,RP33,RP34,RP3

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Part Number	Description	Location(S)
271586026101	RES;.02 ,2W,1%,2512,SMT	PR17
271591100301	RP;10*4,8P,1/16W,5%,0804,SMT	RP10,RP11,RP12,RP13,RP14,RP1
271611103301	RP;10K*4 ,8P ,1/16W,5% ,0612,SMT	RP501
271611220301	RP;22*4 ,8P ,1/16W,5% ,0612,SMT	RP504
271611822301	RP;8.2K*4,8P ,1/16W,5% ,0612,SMT	RP46,RP47,RP48,RP49,RP50,RP5
271621102302	RP;1K*8 ,10P,1/32W,5% ,1206,SMT	RP503
271621103302	RP;10K*8 ,10P,1/32W,5% ,1206,SMT	RP505
271621472302	RP;4.7K*8,10P,1/32W,5% ,1206,SMT	RP45
272001105403	CAP;1U ,10%,10V ,0805,X7R,SMT	PC1,PC16,PC504,PC66,PC70
272001106702	CAP;10U,6.3V,+- 20%,0805,X5R,SMT	C100,C101,C102,C103,C104,C105
272001475701	CAP;4.7U ,CR,10V ,+80-20%,0805,Y	C569,C583,C714,C750
272002225701	CAP;2.2U ,CR,16V ,+80-20%,0805,Y	C685,C725,C753
272002474401	CAP;.47U ,CR,16V ,10%,0805,X7R,S	C13,C14
272002475702	CAP;4.7U ,CR,16V ,+80-20%,Y5V,08	C2
272003105401	CAP;1U ,CR,25V ,10%,0805,X7R,S	PC529,PC60
272005104402	CAP;.1U ,50V,+/-10%,0805,X7R,SMT	PC2,PC22,PC48,PC528,PC533,PC
272010101302	CAP;100P,2KV,5%,1206,NPO,SMT ,onl	C41
272011106407	CAP;10U,10V,+/-10%,1206,X5R,SMT,	PC21,PC42,PC510,PC518,PC532,
272011106701	CAP;10U ,10V,+80-20%,1206,Y5V,S	C40,C42,C516,C54,C543,C546,C5
272011106709	CAP;10U ,10V,+80-20%,1206,Y5 SM	
272011226401	CAP;22U,6.3V,+-20%,1206,X5R,SMT	PC87,PC90
272012105401	CAP;1U ,CR,16V ,10%,1206,X7R,S	C27,C29
272013475402	CAP;4.7U ,25V ,10%,1206,X5R,SMT,	PC15,PC34,PC49,PC5,PC50,PC51
272021106501	CAP;10U ,10V ,20%,1210,X7R,SMT	C318
272023106502	CAP;10U,25V,M,1210,T2.5MM,X5R,SM	PC505,PC514

Part Number	Description	Location(S)
272023475401	CAP;4.7U ,25V ,10%,1210,X5R,SMT	C1
272030102401	CAP;1000P,2KV,10%,1808,X7R,SMT	C194
272070475701	CAP;4.7U,CR,6.3V,+80-20%,0603,Y5	C294,C554,C754
272071105403	CAP;1U ,10V ,10%,0603,X5R,SMT	C17,C5
272071105701	CAP;1U ,CR,10V ,80-20%,0603,Y5	C10,C49,C503,C531,C538,C599,C
272071225401	CAP;2.2U ,CR,6.3V ,10%,0603,X5R,	C135,C170,C196,C261,C277,C47,
272071332401	CAP;.33U ,10V ,10%,0603,X7R,SMT	C45
272072104402	CAP;.1U ,CR,16V,10%,0603,X7R,SM	C21,C33,C9
272072224402	CAP;.22U ,16V ,10%,0603,X7R,SMT	PC17
272072224701	CAP;.22U ,16V ,+80-20%,0603,Y5V,	C11
272072473401	CAP;.047U,16V ,10%,0603,X7R,SMT	C691
272072474701	CAP;.47U ,16V,+80-20%,0603,Y5V,S	C1,C23,C28
272072683404	CAP;.068U ,16V ,10%,0603,X7R,SMT	C31
272073104703	CAP;.1U ,25V,+80-20%,0603,X7R,S	C11,C19,C8
272073223401	CAP;.022U,CR,25V ,10%,0603,X7R,S	C15
272075100401	CAP;10P ,50V ,10%,0603,COG,SMT	C513,C514,C515
272075101401	CAP;100P ,50V ,10%,0603,COG,SMT	PC45
272075101701	CAP;100P ,50V ,+ -10%,0603,NPO,S	C2
272075102403	CAP;1000P,CR,50V,10%,0603,X7R,SM	PC11,PC14,PC19,PC23,PC26,PC2
272075102701	CAP;1000P,50V ,+/-20%,0603,X7R,S	C15,C270,C506,C51
272075103401	CAP;.01U ,CR,50V ,10%,0603,X7R,S	C13,C25,C3
272075103401	CAP;.01U ,CR,50V ,10%,0603,X7R,S	PC10,PC20,PC24,PC3,PC30,PC50
272075103702	CAP;.01U ,50V,+80-20%,0603,Y5V,S	C266,C267,C301,C39,C43,C511,C
272075104701	CAP;.1U ,50V,+80-20%,0603,Y5V,S	C1,C110,C111,C112,C115,C116,C
272075104703	CAP;.1U ,50V,+80-20%,0603,Y5V,S	C3,C4,C5,C6,C24,C26

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Part Number	Description	Location(S)
272075152401	CAP;1500P,CR,50V,10%,0603,X7R,SM	PC77
272075220301	CAP;22P ,50V ,5% ,0603,COG,SMT	C292,C293,C663,C664
272075221401	CAP;220P ,CR,50V ,10%,0603,X7R,S	C39
272075221401	CAP;220P ,CR,50V ,10%,0603,X7R,S	C539
272075222401	CAP;2200P,50V ,10%,0603,X7R,SMT	C37,C43
272075222701	CAP;2200P,50V ,+/-20%,0603,X7R,S	C568
272075222701	CAP;2200P,50V ,+/-20%,0603,X7R,S	C20,C21,C22,C29
272075331301	CAP;330P ,CR,50V,5% ,0603,NPO,SM	PC56,PC58
272075470401	CAP;47P ,50V ,10%,0603,COG,SMT	C113,C114,C319,C324,PC44
272075472701	CAP;4700P,50V ,+ -20%,0603,X7R,S	C7
272075472701	CAP;4700P,50V ,+ -20%,0603,X7R,S	PC46
272102100401	CAP;10P ,50V ,+-10%,0402,NPO,SM	C6,C7,C8
272102100401	CAP;10P ,50V ,+-10%,0402,NPO,SM	C259,C260
272102104401	CAP;.1U ,CR,10V,10%,0402,X5R,SM	C18,C19,C21,C23,C24,C27,C8
272102105701	CAP;1U ,CR,6.3V ,80-20%,0402,Y	C183,C185,C187,C296,C306,C307
272102224701	CAP;.22U ,10V ,+80-20%,0402,Y5V,	C762
272102334701	CAP;.33U ,CR,10V ,+80-20%,0402,Y	C728
272103331401	CAP;33P ,25V ,+/-10%,0402,NPO,S	C10,C11,C9
272103331401	CAP;33P ,25V ,+/-10%,0402,NPO,S	C325,C326,C329
272105100303	CAP;10P ,CR,50V ,5%,0402,NPO,SM	C281,C282,C284,C285,C594,C676
272105101401	CAP;100P ,50V ,5%,0402,COG,SMT	C316,C712,C772
272105101402	CAP;100P ,50V ,+ -10%,0402,NPO,S	C1
272105102408	CAP;1000P,CR,50V,10%,0402,X7R,SM	C736,C743
272105103702	CAP;.01U ,50V,+80-20%,0402,SMT	C16,C191,C192,C198,C199,C200,
272105104701	CAP;.1U ,16V,+80-20%,0402,SMT	C153,C154,C157,C17,C172,C173,

Part Number	Description	Location(S)
272105222501	CAP;2200P,50V ,+/-20%,0402,X7R,S	C323
272105270303	CAP;27P ,50V ,5%,0402,COG,SMT	C278,C279,C668,C669
272105271403	CAP;270P ,50V,+-10%,0402,X7R,SMT	C729
272105470401	CAP;47P ,50V ,10%,0402,COG,SMT	C2,C3,C4,C5
272105470402	CAP;47P ,50V ,+ -10%,0402,NPO,S	C731
272431157507	CAP;150U ,TPC,6.3V,20%,H1.9,7343	C152,C505,C62,PC43,PC516
272431227402	CAP;220U,2V,-35/+10%,H1.9,S,SP-C	PC539,PC80,PC81,PC83,PC84,PC
272431227504	CAP;220U ,4V ,20%,7343,POSCAP,SM	C557
272431227510	CAP;220U ,TPC,4V,20%,H1.9,7343,S	PC509,PC517,PC540,PC541
272431227528	CAP;220U,2.5V,TPE-MC,20%,POSCAP,	PC32
272431337511	CAP;330U,2V,20%,7343,ESR7m,H2.8m	PC549
272601107506	EC;100U ,6.3V,M,9.3*3.6,-55~105'	C732,C733,C734
272990100301	CAP;10P,3000V,+- 5%,NPO,SMT	C35
272993106001	CAP;10U,25V,2.2mm,X5R,KYOCERA,SM	
273000111002	CHOKE COIL;120OHM/100MHZ,20%,321	L39,L519,L520,L537,L538
273000130001	FERRITE CHIP;120OHM/100MHZ,1608,	L5,L6,L7,L8
273000130006	FERRITE CHIP;600OHM/100MHZ,.2A,1	L1,L10,L11,L12,L9
273000130038	FERRITE CHIP;600OHM/100MHZ,1608,	L35,L37,L38,L41,L45,L47,L48,L5
273000130039	FERRITE CHIP;130OHM/100MHZ,1608,	L2
273000130039	FERRITE CHIP;130OHM/100MHZ,1608,	L23,L24,L28,L29,L5,L524,L525,L
273000130122	FERRITE CHIP;80OHM/100MHZ,1608,S	L3,L4
273000150001	FERRITE CHIP;220OHM/100MHZ,2012,	L1
273000150013	FERRITE CHIP;120OHM/100MHZ,2012,	PL501,PL502,PL505,PL508,PL50
273000150033	PHASEOUT;FERRITE CHIP,120OHM/100	L10,L25,L3,L42,L43,L49,L50,L50
273000150313	CHOKE COIL;90OHM/100MHZ,20%,2012	L21,L504,L507

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Part Number	Description	Location(S)
273000150332	FERRIET CHIP;120OHM/100MHZ,2012,	L11,L12,L13,L14,L15,L16,L17,L1
273000500084	CHOKE COIL;400UH(REF),D.2*1,10.5	
273000500096	CHOCK COIL;4.7UH.20mOHM,25%,4.5A	PL514
273000500115	CHOKE COIL;400uH MIN,120mΩ MAX;	L517
273000610025	FERRITE ARRAY;120OHM/100MHZ,ONLY	FA1
273000990127	INDUCTOR;IHLP5050CE-01-0.68uH,VI	PL513
273000990163	INDUCTOR;6.2UH,20%,A916CY-6R2M,S	PL504
273000990248	INDUCTOR;1.4UH,20%,SMI-43M-1R4	PL507
273000990249	INDUCTOR;10UH,30%,SPC-08045-100	PL510,PL511
273000990250	INDUCTOR;4.7UH,30%,SPC-08045-4R7	PL503,PL512
273000990272	INDUCTOR;33UH,30%,SPC-10039P-330	PL506
273001050039	XSFORMER;10/100 BASE,LF-H80P,SMT	U504
273001050175	XFMR;CI8.5,25T/2150T,292mH,Varni	
273001050188	XFMR;CI8.5,25/2150,290mH,ONLY SH	T1
274011431449	XTAL;14.318MHZ,32PF,50PPM,8*4.5,	X2
274012457430	XTAL;24.576MHZ,16PF,50PPM,8*4.5,	X503
274012500424	XTAL;25MHZ,20PF,30PPM,8.0*4.5,2P	X502
274013276103	XTAL;32.768KHZ,20PPM,12.5PF,CM20	X1
274018000303	XTAL;8MHZ,30PPM,16PF,8*4.5,2P,SM	X501
281101015001	IC;MP1015EM-Z,CCFL CTRL,TSSOP20,	U1
281307085001	IC;NC7SZ08P5,2-INPUT & GATE,SC70	U1,U2
281307085001	IC;NC7SZ08P5,2-INPUT & GATE,SC70	U524
282574008005	IC;74AHC08,QUAD 2-I/P AND,TSSOP,	U517
282574014004	IC;74AHC14,HEX INVERTER,TSSOP,14	U522
282574132001	IC;74AHCT1G32,SINGLE OR GAT,SOT2	U16

Part Number	Description	Location(S)
283449004001	IC;FLASH,512*8,FWH/LPC,PM49FL004	
283450040001	IC;FLASH,512*8,FWH,M50FW040K1,PL	
283467490001	IC;FLASH,512K*8,FWH,SST49LF004A,	
283467490002	IC;FLASH,512K*8,FWH,W39V040FAP,P	
283467540001	IC;EEPROM,M24C02-WMN6T,2K,SO8,SM	U2
283467540002	IC;EEPROM,M93C46-WMN6T,64*16 BIT	U514,U515
283468290003	IC;FLASH,512*8,FWH/LPC,AT49LH004	
284183517003	IC;SIO,W83L517D,B REVERSION,LQFP	U516
284500522001	IC;855GME GMCH,NORTH BRIDGE,BGA,	U502
284500655003	IC;ALC655,AUDIO CODEC,LQFP,48P,S	U521
284501162001	IC;SII1162,PANEL LINK TRANSMITTE	U1
284501410007	IC;PCI1410A,PCI/CARDBUS,PQFP,144	U508
284506301001	IC;VT6301S,1394 one port control	U519
284507460002	IC;ADT7460,TEMPERATURE MTR,QSOP,	U505
284508100009	IC;RTL8100CL,LAN CONTROLLER,LQFP	U507
284508807001	IC;AME8807AEHA,600mA,CMOS LDO,AM	PU15
284582801044	IC;FW82801DBM,ICH4-M,BGA,421P	U10
284583950002	IC;W83L950D-Ver.C,LPC_KBC,LQFP,8	
284595081201	IC;ICS950812,CK408 CLOCK GEN,TSS	U7
286002040001	IC;BQ2040,GAS GAUGE,SO,16P,SMT	U3
286100212001	IC;TPA0212,AMPLIFIER,TSSOP,24P,S	U14
286100393004	IC;LMV393,DUAL COMPARTOR,SSOP,8P	PU3
286104173001	IC;MAX4173F,I-SENSE AMP,SOT23,6P	PU501
286300431014	IC;SC431LCSK-.5,.5%,ADJ REG,SOT2	PQ3
286300594001	IC;TL594C,PWM CONTROL,SO,16P	PU7

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Part Number	Description	Location(S)
286300690001	IC;GMT690B,RESET CIRCUIT,2.93V,S	U520
286300812002	IC;S-812C,DECECTOR,SOT-89,PRC	U1
286301117052	IC;G1117,VOL REGULATOR,1A,SOT-22	U511
286301403001	IC;SC1403,CONTROLLER,TSSOP-28	PU502
286301414001	IC;MM1414,PROTECTION,TSOP-20A,PR	U5
286301907001	IC;MAX1907A,PWM CONTROLLER,40-QF	PU6
286302211004	IC;TPS2211A,POWER INTERFACE SW,S	U510
286302951016	IC;AMS2951CS,150MA VLOTAGE REGUL	U506
286302996001	IC;G2996,DDR,GMT,SOP8FD,SMT	PU18
286303107001	IC;AMS3107C,3.3V,1%,VOL REGULATO	U509
286306227002	IC;ISL6227CA, PWM CONTROLLER SSO	PU10,PU4
286308800006	IC;AME8800AEEV,VOL REG.,SOT23-5,	U2
286309167001	IC;RT9167-47CB,200MA LDO REGULAT	U15
286309701001	IC;RT9701,POWER DISTRI SW,SOT23-	U5,U501
286369229301	IC;G692L293T,RESET CIRCUIT,2.93V	U13
288006102001	FIR;TFDU6102,SIDE/TOP VIEW,8P,SM	U523
288100018003	DIODE;UDZS18B,ZENER,18V,SOD-323,	ZD3,ZD4
288100020001	DIODE;RLZ20C,ZENER,19.23V,5%,SMT	PD505
288100024002	DIODE;RLZ24D,ZENER,23.63V,5%,SMT	PD501
288100032013	DIODE;BAS32L,VRRM75V,MELF,SOD-80	D511,D512,PD1
288100034004	DIODE;SSA34,40V,3A,SMA	PD504
288100034007	DIODE;SCD34,40V,3A,2010,SECOS	PD2,PD8,PD9
288100054001	DIODE;BAT54,30V,200mA,SOT-23	D4,D5,D501,D502,D507,D508
288100056003	DIODE;BAW56,70V,215mA,SOT-23	D15,D517,PD507,PD508,PD6
288100056005	DIODE;UDZ5.6B,ZENER,5.6V,UMD2,SM	D504

Part Number	Description	Location(S)
288100056005	DIODE;UDZ5.6B,ZENER,5.6V,UMD2,SM	ZD1,ZD2,ZD5
288100099001	DIODE;BAV99,70V,450MA,SOT-23	D501,D502,D503
288100099001	DIODE;BAV99,70V,450MA,SOT-23	PD3,PD4
288100140008	DIODE;SCS140P,40V,1A,SECOS,SMT	PD7
288100701002	DIODE;BAV70LT1,70V,225MW,SOT-23	D509,D510,PD5,PD502,PD506
288101040006	DIODE;SBM1040,10A,SCHOTTKY,POWER	PD503
288104148001	DIODE;RLS4148,200MA,500MW,MELF,S	D16,D3,D503,D520
288200114009	TRANS;DDTC114TCA,N-MOSFET,SOT-23	Q528,Q529
288200144001	TRANS;DTC144WK,NPN,SOT-23,SMT	Q508
288200144003	TRANS;DTC144TKA,N-MOSFET,SOT-23	Q23,Q24,Q25,Q28,Q29,Q32,Q34,(
288200144009	TRANS;DDTC144WCA,NPN,SOT-23,SMT	
288200144009	TRANS;DDTC144WCA,NPN,SOT-23,SMT	PQ505
288200144010	TRANS;DDTA144WCA,PNP,SOT-23,SMT	PQ6
288200144011	TRANS;DDTC144TCA,NPN,SOT-23,SMT	
288200301001	TRANS;FDV301N,N-CHANNEL,SOT23	Q514
288202222001	TRANS;MMBT2222AL,NPN,TO236AB	PQ2,Q17,Q18
288202301006	TRANS;AM2301P,P-MOSFET,SOT-23	Q14,Q33,Q505,Q507,Q509,Q519,(
288203414001	TRANS;AO3414,N-CHANNEL FET,SOT-2	Q10,Q504
288203904010	TRANS;MMBT3904L,NPN,Tr35NS,TO236	Q19,Q20,Q21,Q3
288204403008	TRANS;AO4403,P-MOSFET,46mOHM (VG	
288204406001	TRANS;AO4406,N-MOS,.0165OHM,SO8	PU13,PU14
288204407001	TRANS;AO4407,P-MOS,.01OHM,SO8,SM	PQ501,PQ502,PQ503
288204409001	TRANS;AO4409,P-MOSFET,SO-8P,MSL,	Q1A,Q2
288204422001	TRANS;AO4422,24mOHM,N-MOSFET,SOI	PU17
288204435003	TRANS;FDS4435,P-MOSFET,35mOHM,SO	Q1,U4,U6

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Part Number	Description	Location(S)
288204702002	TRANS;AO4702, N-MOSFET,WITH SCHO	PU16
288204900001	TRANS;AO4900,DUAL N-MOSFET WITH	PU1,PU2,PU5,PU503,PU8
288206676005	TRANS;FDS6676S,14.5A,30V,9mOHM,S	PU11,PU12,PU9
288227002001	TRANS;2N7002LT1,N-CHANNEL FET,SO	PQ4,PQ5,PQ9
288227002006	TRANS;2N7002LT1,N-CHANNEL FET,ES	Q501,Q502
288227002006	TRANS;2N7002LT1,N-CHANNEL FET,ES	PQ1,PQ504,PQ7,PQ8,Q11,Q15,Q
291000000203	CON;HDR,MA,2P*1,3.5MM,R/A,SMT,SM	CN2
291000010209	CON;HDR,MA,2P*1,1.25MM,H4.2,ST,S	J512
291000010228	CON;HDR,MA,2P*1,1.25MM,H4.2,ST,S	
291000010303	CON;HDR,MA,3P*1,1.25MM,H4.2,ST,S	J506
291000010619	CON;HDR,MA,6P,ACES,87151-0607,SM	J4
291000013025	CON;HDR,MA,15P*2,ACES,88107-3000	J1
291000020206	CON;HDR,MA,2P*1,1.25MM,H2.57,R/A	J505
291000020225	CON;HDR,MA,2P*1,1.25MM,H2.57,R/A	
291000020312	CON;HDR,MA,3P*1,1.25MM,H4.75MM,S	
291000020408	CON;HDR,MA,4P,1.25MM,H3.5MM,R/A,	J1
291000021105	CON;HDR,MA,11P*1,ACES,87213-1100	CN1
291000021105	CON;HDR,MA,11P*1,ACES,87213-1100	J2
291000023008	CON;HDR,FM,15P*2,0.8MM.H5,R/A,SM	J513
291000152610	CON;FPC/FFC,26P,1MM,H=2.0,R/A,85	J2
291000152610	CON;FPC/FFC,26P,1MM,H=2.0,R/A,85	J3,J5
291000251202	MINIPCI SOCKET;124P,R/A,0.8MM,H=	
291000251246	MINIPCI SOCKET;124P,R/A,0.8MM,H=	J511
291000256843	CON;IC CARD,68P,UP,STANDOFF 0.0	J6
291000614793	IC SOCKET;UPGA479M,479P,MOLEX	U503

Part Number	Description	Location(S)
291000622007	CON;DIMM,R/A,200P,.6,H9.2,REVERS	J507
291000622015	DIMM SOCKET; DDR,200P,REVERSE TY	
291000622016	DIMM SOCKET; DDR,200P,H=9.2mm,SM	
291000811008	CON;PHONE JACK,2 IN 1,7.0MM,ALLT	J504
291000920607	CON;STEREO JACK,6P,W9.5,93310000	J516
294011200069	LED;GREEN,19-21VGC/TR8,LED_CL190	LED3,LED4,LED5,LED6
294011200070	LED;RED/GREEN,19-22SRVGC/TR8,LED	LED1,LED2
294011200150	LED;BLUE,H0.55,LTST-C191TBKT,SMT	D21,D22,D23,D24,D25,D26
294011200250	LED;WHITE,3.2X2.7,H1.8,67-21UWC,	D3
295000010009	FUSE;NORMAL,5A/32VDC,3216,SMT	L51,L52
295000010020	FUSE;NORMAL,7A/24VDC,1206,SMT	
295000010028	FUSE;0.14A/60V,POLY SWITCH,PTC,S	F4
295000010048	FUSE;0.5A/15V,POLY SWITCH,SMD	F3
295000010105	FUSE;1A,NORMAL,1206,SMT	F1
295000010140	FUSE;FAST,2A,63VDC,1206,SMT,0433	F2
295000010141	FUSE;FAST,3A,32VDC,1206,SMT,0433	PF502
295000010154	FUSE;FAST,1.25A,63V,1206,SMT,043	F1
295000010163	FUSE;NORMAL,7A/24VDC,0433007,120	PF501,PF503
295000010193	FUSE;FAST,7A/32V,1206,SMT	
295000100004	FUSE;FAST,1A,63V,1206,THIN FILM	F501
297004010001	SW;PUSH BUTTOM,5P,SPST,12VDC,50m	SW3,SW4
297140200001	SW;SCROLL BUTTON,TMEC,TC017-PS-1	SW1
297140200003	SW;COVER SWITCH,0.1A,30V,4P,T-ME	SW1
310111103035	THERMISTOR;10K,1%,RA,DISK,103AT-	
312271006358	EC;100U,25V,RA,M,D6.3*7,SGX,SANY	PC506

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Part Number	Description	Location(S)
316685400002	PCB;PWA-INVERTER BD(DA-1A08-D01	R0B
316685400003	PCB;PWA-8011/M BD	R01
316685400004	PCB;PWA-8011/Transmitter BD	
316685400006	PCB;PWA-8011/BATTERY GAUGE BD,PW	
323768240003	DDR SODIMM MODULE;256MB,DDR400,I	
324180786897	IC;CPU,DOTHAN,1.50GHZ,PN 715,FSB	
331000000314	CON HOLDER;PCMCIA,R-BTN ,MPT,929	J6
331000004009	CON;IEEE1394,MA,4P*1,0.8MM,R/A	
331000004050	CON;IEEE1394,MA,4P*1,0.8MM,R/A;M	J514
331000007025	CONNECTOR;7 PIN,DIP,ALLTOP,C1034	
331000007050	CON;BATTERY,7P,MA,2.5MM,H=4MM,R/	PJ502
331000008089	CON;USB,FM,H15.64,R/A,4P*2,SUYIN	J501
331000024007	CON;DVI-D,FM,24P,070939FR024S504	J502
331040004031	CON;HDR,MA,4P*1,H=5.9,R/A,USB,DI	J503
331040044024	CON;HDR,FM,22P*2,2MM,R/A,DIP,200	J510
331040050018	CON;HDR,BTB R/A,0.8MM,S-TECH1507	J508
331660020005	DIMM SOCKET;DDR SODIMM 200P, CA0	J509
331720015006	CON;D,FM,15P,2.29,R/A,3ROW	J501
331840010008	CON;STEREO JACK,10P,W/SPDIF,R/A,	J515
331910002006	CON;POWER JACK,2P,20VDC,5A,DIP	PJ501
332110028157	WIRE;#28,UL1061,103MM,YELLOW,YIY	
332110028173	WIRE;#28,UL1061,45MM,ORANGE,PWR	
332110028175	WIRE;#28,UL1061,169mm,BLUE,PWR	
332810000033	PWR CORD;125V/7A,2P,BLACK,AMERIC	
333020000012	SHRINK TUBE;300V,125'C,ID2.5T0.1	

Part Number	Description	Location(S)
333025000004	SHRINK TUBE;300V,125,I.D=2.5,T=0	
333025000012	SHRINK TUBE;600V,125'C,ID3.5L35,	
333025000013	SHRINK TUBE;600V,125'C,ID3.5L63,	
335152000033	FUSE;15V/3.8A,POLY SWITCH	
335152000060	FUSE;THERMAL FUSE,G7F510,93'C,PR	
335612000004	THERMAL CUTOFFS;378,8A/50VDC,139	
338536010052	BATTERY;LI,3.7V/2.2AH,18650,SANY	
339115000046	MICROPHONE;-62dB+-2dB,D6.0*H2.7,	MIC1
340685400001	BRACKET ASSY;SYSTEM,8011	
340685400002	COVER ASSY;8011	
340685400003	COVER ASSY;CPU,8011	
340685400004	COVER ASSY;HDD,8011	
340685400005	COVER ASSY;KB,8011	
340685400006	COVER ASSY;LCD,8011	
340685400007	HEATSINK ASSY;CPU,8011	
340685400008	HOUSING ASSY;8011	
340685400009	HOUSING ASSY;LCD,8011	
340685400010	SHIELDING ASSY;COVER,8011	
340685400011	SHIELDING ASSY;HDD,8011	
340685400012	SPEAKER ASSY;R,8011	
340685400020	BEZEL ASSY;DVD,MKE,SR-8178-CMT,8	
340685400040	HEATSINK ASSY-FORCECON;CPU,8011	
341677000002	SPRING;SCREW,HEATSINK,LYNX	
341680900001	SPC SCREW;#4-1/4,8050	
342503200005	CONTACT PLATE;W4L30T0.15,GRAMPUS	

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Part Number	Description	Location(S)
342503400002	CONTACT PLATE;W5L9T0.13,7170LI,P	
342503400005	CONTACT PLATE;W5L24T0.13,7170LI,	
342672200010	BRACKET;CD-ROM,8500	
342677000014	SMT NUT;A40M20-50,EMI STOP,LYNX	MTG501,MTG502
342685400001	BRACKET;LCD,SAMSUNG,R,8011	
342685400002	BRACKET;LCD,SAMSUNG,L,8011	
342685400004	HINGE;R,8011	
342685400005	HINGE;L,8011	
342685400008	HINGE-JARLLY;R,8011	
342685400009	HINGE-JARLLY;L,8011	
342685400012	CONTACT PLATE;W5L45T0.13mm,PCB,P	
342685400013	CONTACT PLATE;W5L75T0.13mm,PCB,P	
343677100001	HEATSINK;NORTHBRIDGE,BANIAS,LYNX	
344684000040	DUMMY CARD;PCMCIA,8050M	
344685400004	COVER;BATTERY,8011	
344685400008	COVER;HINGE,R,8011	
344685400009	COVER;HINGE,L,8011	
344685400014	HOUSING;BATTERY,8011	
346503100001	INSULATOR;BATT ASSY,THERMAL FUSE	
346503100005	INSULATOR;5,BATTERY ASSY,7521Li	
346503200201	INSULATOR;FOR 2CELL/2ADHESIVE,WE	
346503200202	INSULATOR;BATT ASSY,ONE ROUND,BL	
346677000012	MYLAR;COVER,LCD,LYNX	
346677000016	SPONGE;RTC,LYNX	
346684000014	INSULATOR;RJ11,BACK,8050M	

Part Number	Description	Location(S)
346685400001	INSULATOR;DAUGHTER,8011	
346685400002	INSULATOR;DDR,MINIPCI,8011	
346685400003	INSULATOR;HEATSINK,8011	
346685400004	INSULATOR;INVERTER,8011	
346685400005	INSULATOR;MB,8011	
346685400006	INSULATOR;PCMCIA,8011	
346685400010	INSULATOR;CDRW,8011	
346685400011	INSULATOR;DAUGHTER,BACK,8011	
346685400013	INSULATOR;FIBER,PCB,8011,PWR	
346685400014	INSULATOR;FIBER,2CELL-DOUBLE,801	
346685400015	INSULATOR;KB CONN,8011	
346685400017	AL FOIL;LCD,UP,8011	
346685400018	AL FOIL;LCD,DOWN,8011	
347104020035	GASKET;1,04,020,035	
347104030012	GASKET;1,04,030,012	
347107070014	GASKET;1,07,070,014	
347108025006	GASKET;1,08,025,006	
347108030008	GASKET;1,08,030,008	
347108035008	GASKET;1,08,035,008	
347110010018	GASKET;1,10,010,018	
361200001018	CLEANNER;YC-336,LIQUID,STENCIL/P	
361200002018	FLUX;FLS0016T-5,ALPHA,MULTI-LAYE	
361400003003	JET-MELT ADHESIVES;3478-Q,5/8in*	
361400003005	ADHESIVE;HEAT,TRANSFER,HTA-48(W)	
361400003021	SOLDER CREAM;NOCLEAN,P4020870980	

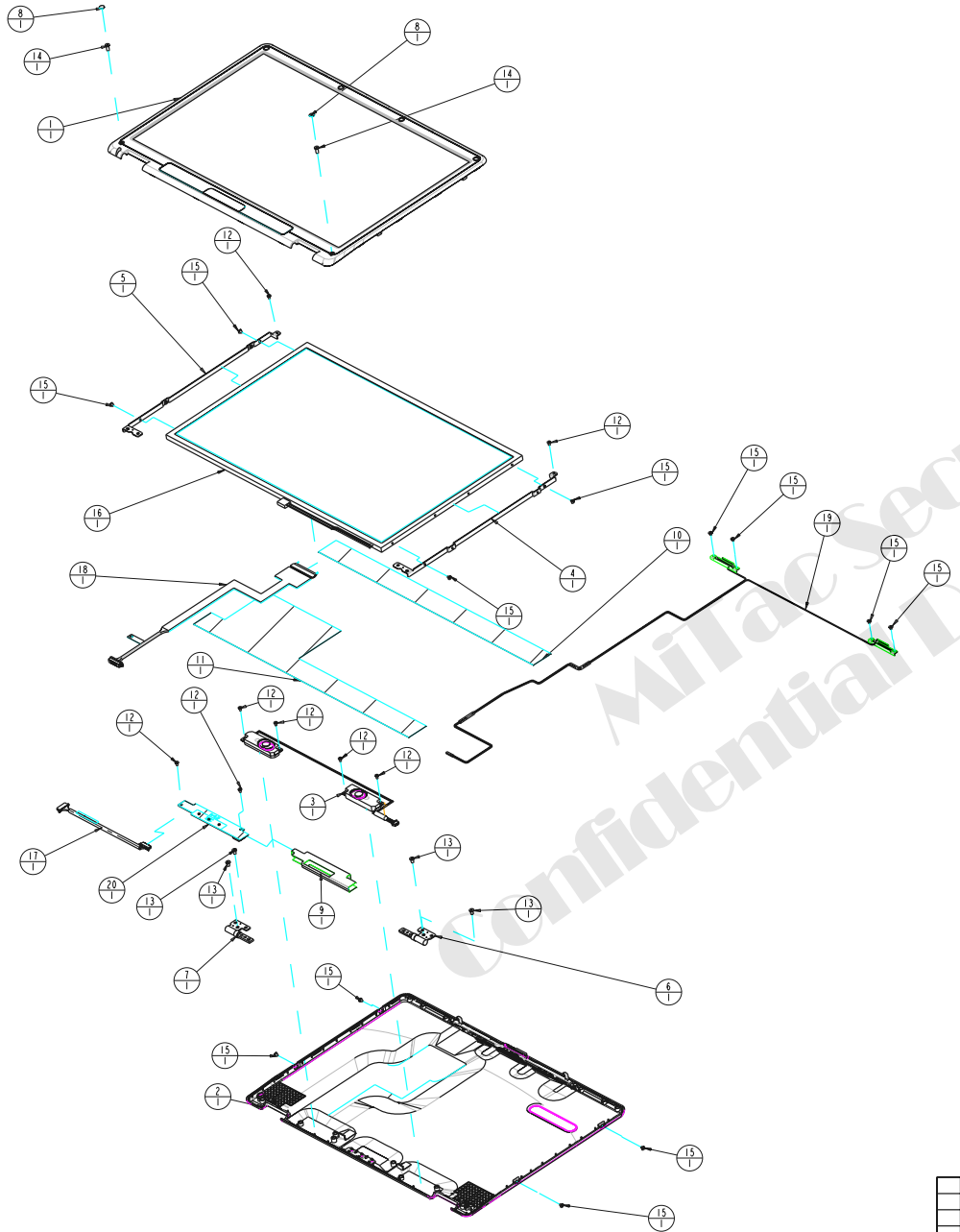
9. Spare Parts List - 12

Part Number	Description	Location(S)
361400003021	SOLDER CREAM;NOCLEAN,P4020870980	
361400003030	ADHESIVE;ABS+PC PACK,G485,CEMIDA	
370102010201	SPC-SCREW;M2L2,NIW,K-HD,t=0.8,NL	
370102010303	SPC-SCREW;M2L3,NIW,K-HD(+),NYLOK	
370102010303	SPC-SCREW;M2L3,NIW,K-HD(+),NYLOK	
370102010312	SPC-SCREW;M2L3,KHD(+0)t0.3,NIW/N	
370102010502	SPC-SCREW;M2 L5,NIB,K-HD,t0.8,NL	
370102030301	SPC-SCREW;M2L3,K-HD,1,NIB/NLK	
370102030301	SPC-SCREW;M2L3,K-HD,1,NIB/NLK	
370102610303	SPC-SCREW;M2.6L3,KHD,D4.4,t0.45,	
370102610401	SPC-SCREW;M2.6L4,K-HD,t0.8,NIB/N	
370102610405	SPC-SCREW;M2.6L4,NIW,K-HD,t=0.8,	
370102610405	SPC-SCREW;M2.6L4,NIW,K-HD,t=0.8,	
370102631202	SPC-SCREW;M2.6L6,K-HD,NIW/NLK	
370102631202	SPC-SCREW;M2.6L6,K-HD,NIW/NLK	
370103010405	SPC-SCREW;M3L4,NIW,K-HD,T0.3	
371102010252	SCREW;M2L2.5,K-HEAD(+),NIB/NLK	
371102010252	SCREW;M2L2.5,K-HEAD(+),NIB/NLK	
373101713502	T-SCREW;B.M1.7L3.5,HD04t0.25,0,B	
373101722501	T-SCREW;B,M1.7,L2.5,KHD(+),T0.5,	
411685400001	PWA;PWA-8011,MOTHER BD	
411685400002	PWA;PWA-8011,MOTHER BD,T/U	
411685400003	PWA;PWA-8011,MOTHER BD,SMT	
411685400004	PWA;PWA-8011,Transmitter BD,T/U	
411685400005	PWA;PWA-8011,Transmitter BD,SMT	

Part Number	Description	Location(S)
411685400011	PWA;PWA-8011/BATT SANYO CELL,4SI	
411685400012	PWA;PWA-8011/BATT SANYO CELL,4SI	
411685400015	PWA;PWA-INVERTER BD(DA-1A08-D01	
412678800001	PCB ASSY;FAX MODEM 56K,1456VQL4A	
412686200001	PCB ASSY;WIRELESS LAN CARD,WM3B2	
413000020523	LCD;LTN140W1-L01,14" WXGA TFT L	
416268540001	LF PF;14",WXGA,SAM,8011 ID1	
422674300071	WIRE ASSY;MDC,E-NOTE	
422677000008	WIRE ASSY;BATT TO MB,FOR LYNX,MO	J512
422685400001	CABLE FFC;DAUGHTER,8011	
422685400002	CABLE FFC;TP,8011	
422685400003	WIRE ASSY;INVERTER,8011	
422685400004	WIRE ASSY;LCD,SAMSUNG,8011	
422685400005	WIRE ASSY;WLAN,8011	
422685400006	WIRE ASSY-COMAX;INVERTER,8011	
422685400007	WIRE ASSY-COMAX;LCD,SAMSUNG,8011	
431685400001	CASE KIT;8011 ID1	
441685400003	BATT ASSY;LI,14.8V,2200mAH,SANYO	
441685400005	LCD ASSY;14",WXGA,SAM,8011 ID1	
442680900051	TOUCHPAD MODULE;SYNAPTICS,TM42PU	
442681400053	AC ADPT ASSY;19V,3.42A,DELTA AD	
442685400001	BATTERY ASSY;LI-ION,14.8V/2.2AH,	
442685400004	PWA;PWA-8011/INVERTER BD,DA-1A08	
451685400002	LABEL KIT;N-B,8011 ID1	
451685400031	LCD ME KIT;14",WXGA,SAM,,8011 ID	

9. Spare Parts List - 13

Part Number	Description	Location(S)
451685400051	HOUSING KIT;8011 ID1	
451685400071	ODD ME KIT;8011 ID1	
451685400091	HDD ME KIT;8011	
451685400092	HEATSINK ME KIT;8011	
461685400007	PACKING KIT;N-B,COMPACT,8011	
481685400001	F/W ASSY;SYS/VGA BIOS,8011	U12
481685400002	F/W ASSY;KBD CTRL,8011	U11
523400861006	DVD DRIVE; MKE SR-8178,8081	
523402379051	HDD DRIVE;40GB,2.5",MHT2040AT,V4	
523468540001	DVD ASSY;KME,SR-8178,8011 ID1	
523468540036	HDD ASSY;40GB,FUJI,MHT2040AT,801	
526268540002	LTX;8011/4AEB/40F/1UKX/A5F3A/XL	
531068540011	KBD;88,UI,K011718M5,JME,8011	
600100010009	SOLDER WIRE;63/37,0.8,CM,N/C,PRC	
600100010009	SOLDER WIRE;63/37,0.8,CM,N/C,PRC	
600100010009	SOLDER WIRE;63/37,0.8,CM,N/C,PRC	
624200010140	LABEL;5*20,BLANK,COMMON	
624200010140	LABEL;5*20,BLANK,COMMON	
624200010140	LABEL;5*20,BLANK,COMMON	
627207522141	CAP;220P ,50V ,10%,0603,X7R,SMT	C25
628820014401	TRANS;DTA144EKA,PNP,100MA,50V,SO	Q6,Q7
		P/N:526268540002



ITEM	PART NO	DESCRIPTION	Q'TY	TYPE	REMARK
1	340685400006	COVER ASSY;LCD,8011	1	ASSEMBLY	
2	340685400009	HOUSING ASSY;LCD,8011	1	ASSEMBLY	
3	340685400012	SPEAKER ASSY;R,8011	1	ASSEMBLY	
4	342685400001	BRACKET;LCD,SAMSUNG-R,8011	1	PART	
5	342685400002	BRACKET;LCD,SAMSUNG-L,8011	1	PART	
6	342685400004	HINGE;R,8011	1	PART	
7	342685400005	HINGE;L,8011	1	PART	
8	346677000012	MYLAR;COVER,LCD,LYNX	2	PART	
9	346685400004	INSULATOR;INVERTER,8011	1	PART	
10	346685400017	AL FOIL;LCD,UP,8011	1	PART	
11	346685400018	AL FOIL;LCD,DOWN,8011	1	PART	
12	370102010303	SPC-SCREW; M2L3,NIW,K-HD(+),NYLO	8	PART	
13	370102610401	SPC-SCREW; M2.6L4 K-HEAD,NIB,NLK	4	PART	
14	370102631202	SPC-SCREW;M2.6L6,K-HD,NIW/NLK	2	PART	
15	371102010252	SCREW;M2L2.5,K-HEAD(+),NIB/NLK	12	PART	
16	416000020523	LCD;LTN140WI-L01,14"	1	PART	
17	422685400003	WIRE ASSY;INVERTER,8011	1	ASSEMBLY	
18	422685400004	WIRE ASSY;LCD,SAMSUNG,8011	1	ASSEMBLY	
19	422685400005	WIRE ASSY;WLAN,8011	1	ASSEMBLY	
20	442685400004	PWA;PWA-8011/INVERTER BD,DA-1A0	1	ASSEMBLY	

ITEM	CONTENTS OF CHANGE	RVS	CHK	APV	M/D/Y
					/ /
					/ /
					/ /
					/ /
					/ /

TOL ± RANGE	Pla	Met	Ins	Por	Cab	Pac	Gas	PCB
0-6	0.1	0.1	0.1	0.2	0.5	1	0.5	0.1
6-30	0.1	0.1	.15	.25	1	1	0.5	0.1
30-80	0.1	.15	0.2	0.3	2	1.5	1	0.1
80-180	.15	.15	.25	0.3	2	2	1	.15
180-315	.15	0.2	0.3	0.4	2.5	2	1	.15
315-800	0.2	0.3	0.4	0.5	3	3	2	.15

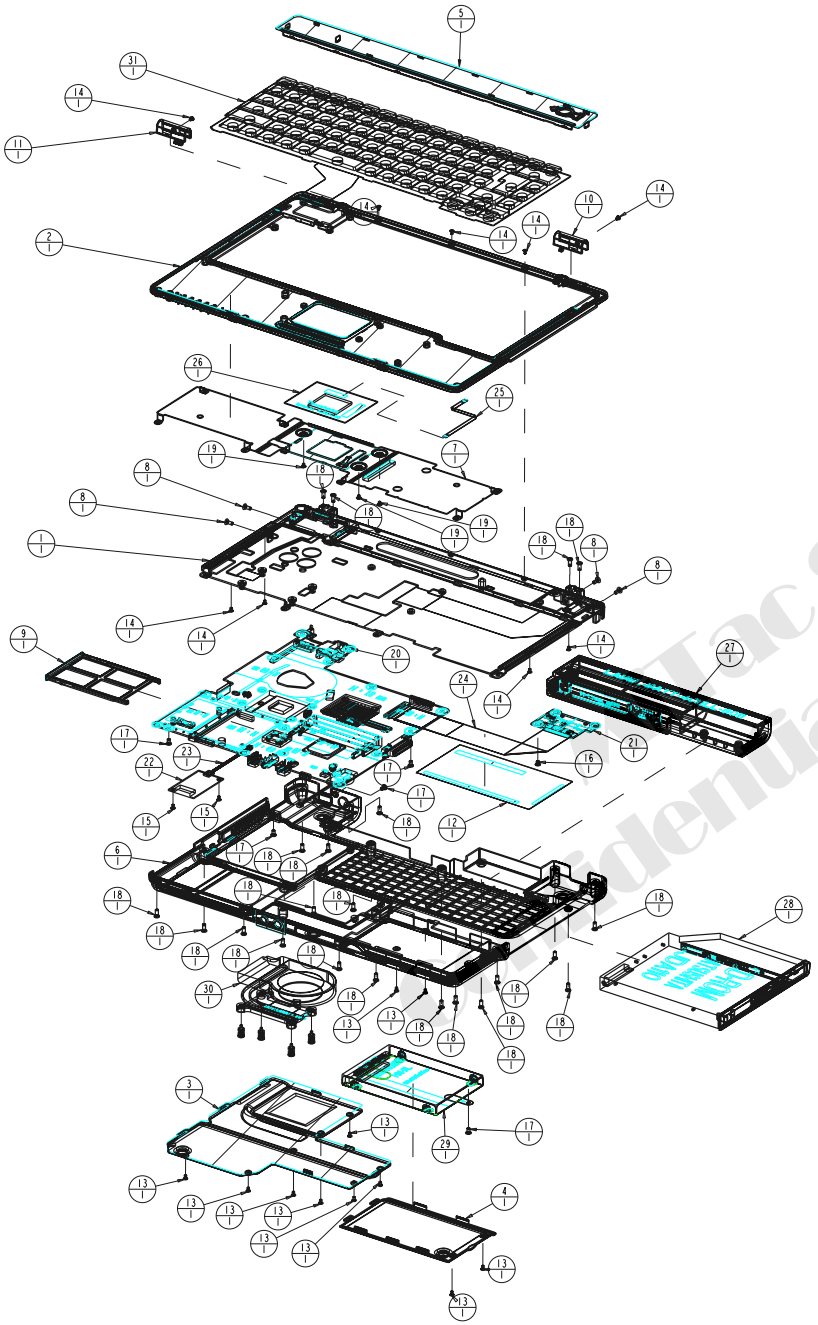
DATE	12-Jul-04	MATERIAL	SEE NOTES	TREATMENT		REMARK	
UNIT	MM	SCALE	0.40	DRAWING NAME	LCD ME KIT;14",WXGA,SAM,8011		IDI
DRAWN	DESIGNED	CHECKED	APPROVED	MATERIAL NO.	MF 451 6854 00031 R 00		

MiTAC Technology Corp.

model name:LCD_ME_KIT-8011

file name:LCD_ME_KIT-8011

SHEET NO. 1 of 1



ITEM	PART NO	DESCRIPTION	Q'TY	TYPE	REMARK
1	340685400001	BRACKET ASSY;SYSTEM,8011	1	ASSEMBLY	
2	340685400002	COVER ASSY;8011	1	ASSEMBLY	
3	340685400003	COVER ASSY;CPU,8011	1	ASSEMBLY	
4	340685400004	COVER ASSY;HDD,8011	1	ASSEMBLY	
5	340685400005	COVER ASSY;KB,8011	1	ASSEMBLY	
6	340685400008	HOUSING ASSY;8011	1	ASSEMBLY	
7	340685400010	SHIELDING ASSY;COVER,8011	1	ASSEMBLY	
8	341680900001	SPC SCREW;#4-1/4,8050	4	PART	
9	344684000040	DUMMY CARD;PCMCIA,8050M	1	PART	
10	344685400008	COVER;HINGE,R,8011	1	PART	
11	344685400009	COVER;HINGE,L,8011	1	PART	
12	346685400010	INSULATOR;CDRW,8011	1	PART	
13	370102010303	SPC-SCREW; M2L3,NIW,K-HD(+),NYLO	11	PART	
14	370102010312	SPC-SCREW;M2L3,KHD(+0)+0.3,NIW/N	9	PART	
15	370102030301	SPC-SCREW; M2L3,K-HEAD,1,NIB,NLK	2	PART	
16	370102610303	SPC-SCREW;M2.6L3,KHD,D4.4+0.45,N	1	PART	
17	370102610405	SPC-SCREW; M2.6L4 K-HEAD,NIW	5	PART	
18	370102631202	SPC-SCREW;M2.6L6,K-HD,NIW/NLK	22	PART	
19	371102010252	SCREW;M2L2.5,K-HEAD(+),NIB/NLK	3	PART	
20	411685400001	PWA;PWA-8011,MOTHER BD	1	ASSEMBLY	
21	411685400004	PWA;PWA-8011,TRANSMITTER BD,T/U	1	ASSEMBLY	
22	412671800001	PCB ASSY;FAXMODEM,56K,MDC,GP2	1	PART	
23	422674300071	WIRE ASSY;MDC,E-NOTE	1	ASSEMBLY	
24	422685400001	CABLE FFC;DAUGHTER,8011	1	PART	
25	422685400002	CABLE FFC;TP,8011	1	PART	
26	442680900051	TOUCH PAD;SYNATICS,TM42P-313	1	PART	
27	442685400002	batt;assy,8011	1	ASSEMBLY	
28	451685400078	DVD+RW ME KIT;QSI,SDW-041,8011	1	ASSEMBLY	
29	451685400091	HDD ME KIT;8011	1	ASSEMBLY	
30	451685400092	HEATSINK ME KIT ASSY;CPU,8011	1	ASSEMBLY	
31	531020237661	KBD;89,US,K011718M1,LYNX	1	PART	

ITEM	CONTENTS OF CHANGE	RVS	CHK	APV	M/D/Y

TOL ± RANGE	Pla	Met	Ins	Por	Cab	Pac	Gas	PCB
0-6	0.1	0.1	0.1	0.2	0.5	1	0.5	0.1
6-30	0.1	0.1	.15	.25	1	1	0.5	0.1
30-80	0.1	.15	0.2	0.3	2	1.5	1	0.1
80-180	.15	.15	.25	0.3	2	2	1	.15
180-315	.15	0.2	0.3	0.4	2.5	2	1	.15
315-800	0.2	0.3	0.4	0.5	3	3	2	.15

DATE	09-Jul-04	MATERIAL	SEE NOTES	TREATMENT		REMARK
UNIT	MM	SCALE	0.45	DRAWING NAME	HOUSING KIT;8011	
DRAWN	DESIGNED	CHECKED	APPROVED	MATERIAL NO.	MF 451685400051 R00	

MiTAC Technology Corp.

model name:8011-STRU

file name:HOUSING_KIT-8011

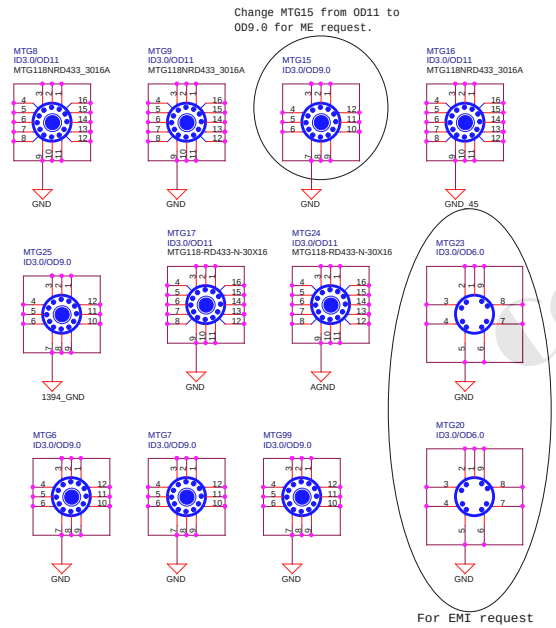
8011 R01

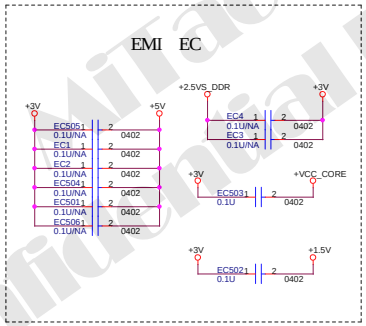
PROJECT CODE- G140
PRODUCT CODE- 6854

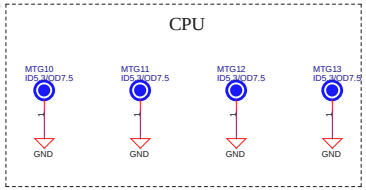
PCB P/N:316685400003
ASSY P/N:411685400003

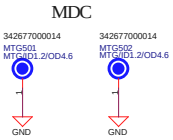
PCI DEVICE	INTERRUPT	REQ/GNT	IDSEL
LAN	PCI_INTE#	PCI_REQ3# / PCI_GNT3#	AD18
CARDBUS	PCI_INTC#	PCI_REQ0# / PCI_GNT0#	AD20
IEEE1394	PCI_INTG#	PCI_REQ1# / PCI_GNT1#	AD21
MINIPCI	PCI_INTD#	PCI_REQ2# / PCI_GNT2#	AD17

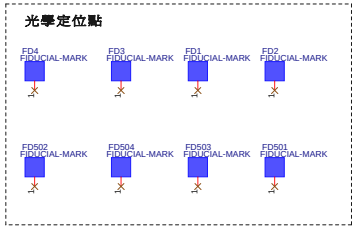
REVISION	TAPEOUT DAY	HISTORY
R00	2004/5/7	
R0B	2004/8/5	1.CardBus IC change from CB1410 to PCI1410. 2.Change DVI_CLK+/- signal each other for SiI11162. 3.Change DVI connector from DVI-I to DVI-D. 4.Modify DDC_CLK and DDC_DATA signal error. 5.Reserve some DVI component for cost down. 6.Modify +CARD_VCC name error for CardBus. 7.Modify audio mute schematic for popo issue. 8.Resever SHARP common design schematic. 9.Add EMI solution circuit for EMI request.
R01	2004/9/6	1.Remove AMS3107 near 10U cap(C619) for inrush current issue. 2.Remove near PCMCIA slot test point to avoid slot short. 3.Change MTG15 from OD11 to OD9.0 for ME request. 4.Remove all M/B finger for EMI request.











DRAWN	DESIGN	CHECK	ISSUES

MiTAC

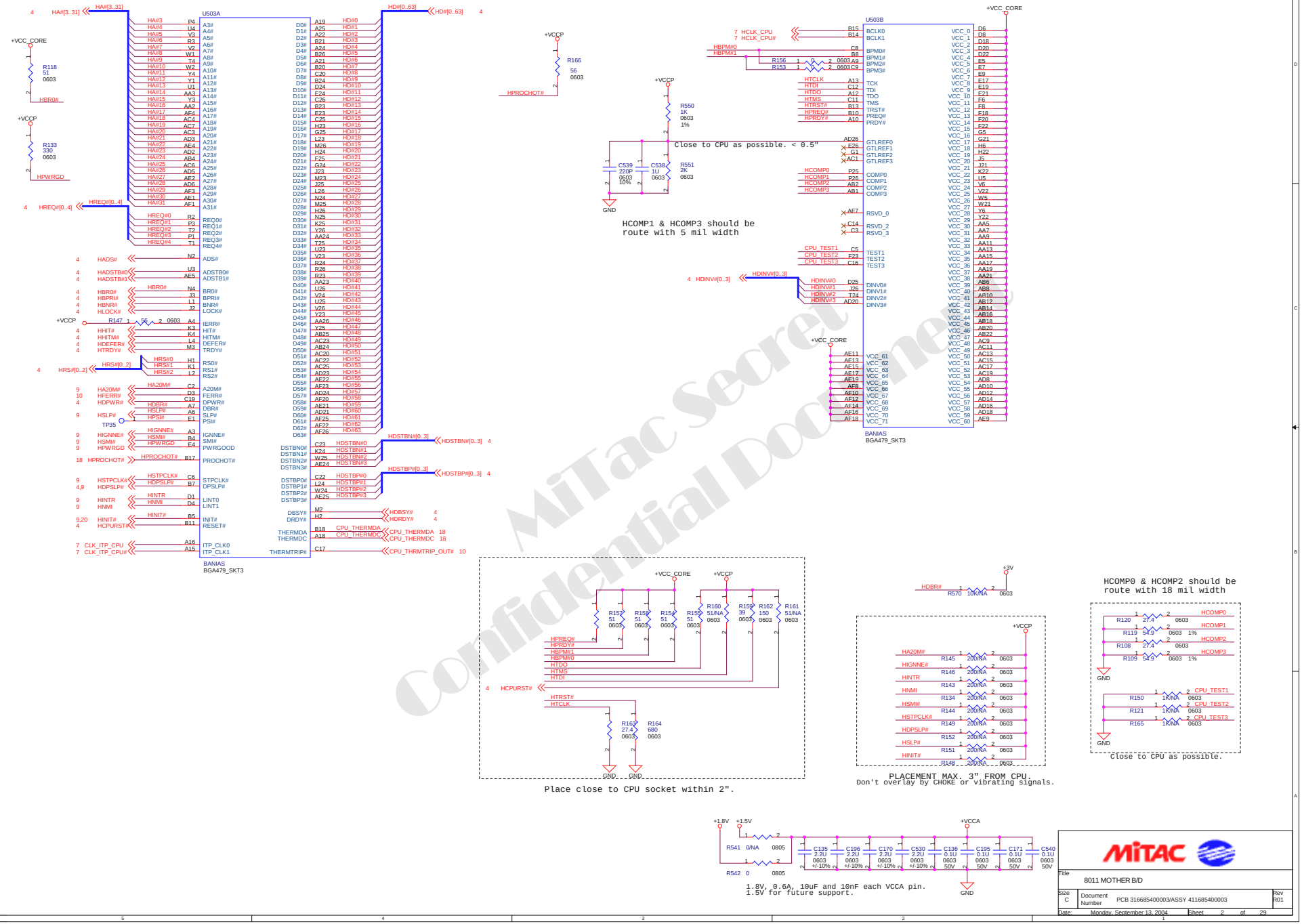
Title: 8011 MOTHER B/D

Size: C | Document Number: PCB 316685400003/ASSY 411685400003 | Rev: R01

Date: Monday, September 13, 2004 | Sheet 1 of 29

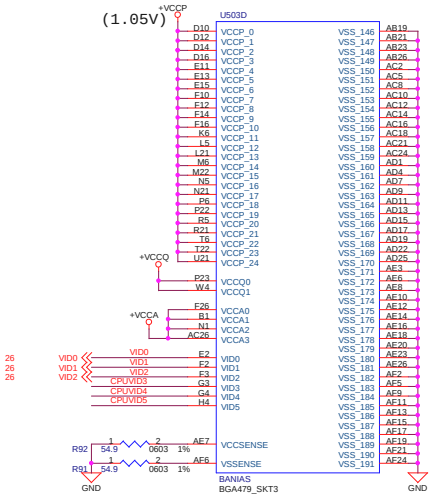
VCC : PROCESSOR CORE POWER SUPPLY.
VCCA : ISOLATE POWER FOR INTERNAL PLL.
VCCP : PROCESSOR I/O POWER SUPPLY.
VCCQ : QUIET POWER SUPPLY FOR ON DIE COMP CKT.

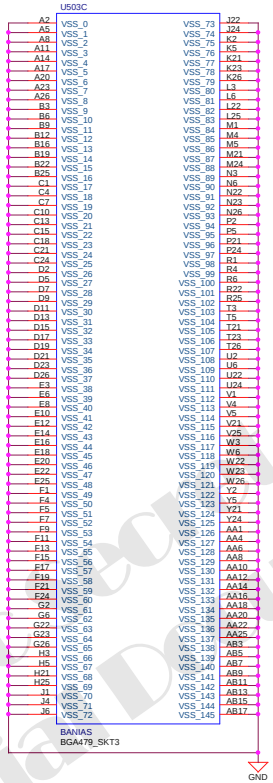
CPU-BANIAS (1/2)

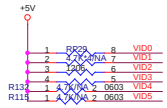


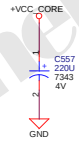
Title	8011 MOTHER B/D
Size C	Document Number PCB 316685400003/ASSY 411685400003 Rev R01
Date: Monday, September 13, 2004	Sheet 2 of 29

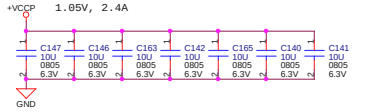
CPU-BANIAS (2/2)

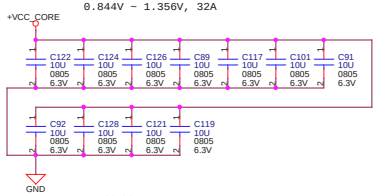


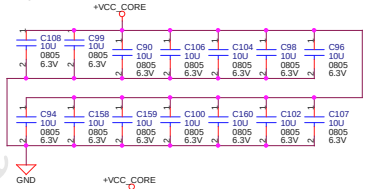


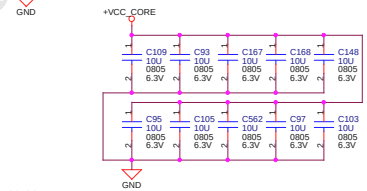


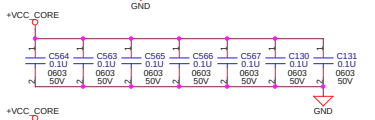


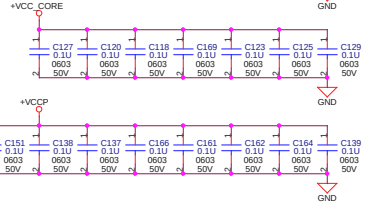


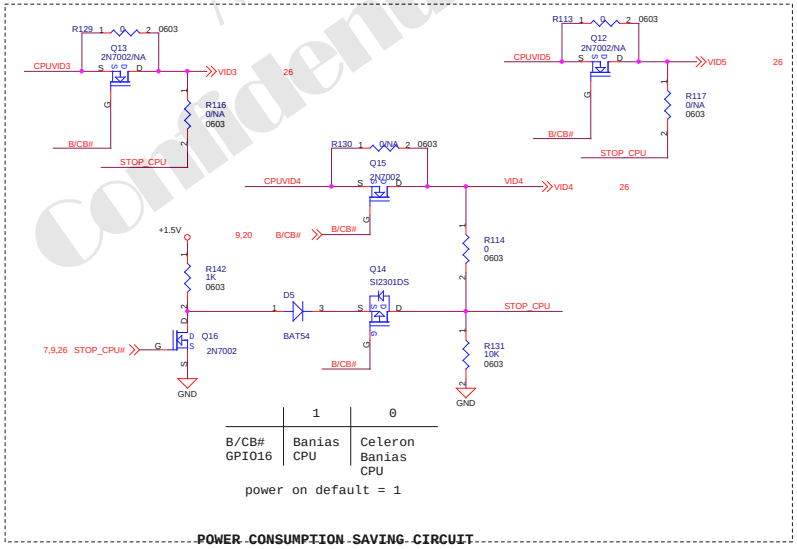












B/CB# GPIO16	1	0
	Banias CPU	Celeron Banias CPU

power on default = 1

POWER CONSUMPTION SAVING CIRCUIT

VID

5	4	3	2	1	0	VCC-Core
0	0	0	0	0	0	1.708
0	0	0	0	0	1	1.692
0	0	0	0	1	0	1.676
0	0	0	0	1	1	1.660
0	0	0	1	0	0	1.644
0	0	0	1	0	1	1.628
0	0	0	1	1	0	1.612
0	0	0	1	1	1	1.596
0	0	1	0	0	0	1.580
0	0	1	0	0	1	1.564
0	0	1	0	1	0	1.548
0	0	1	0	1	1	1.532
0	0	1	1	0	0	1.516
0	0	1	1	0	1	1.500
0	0	1	1	1	0	1.484
0	0	1	1	1	1	1.468
0	1	0	0	0	0	1.452
0	1	0	0	0	1	1.436
0	1	0	0	1	0	1.420
0	1	0	0	1	1	1.404
0	1	0	1	0	0	1.388
0	1	0	1	0	1	1.372
0	1	0	1	1	0	1.356
0	1	0	1	1	1	1.340
0	1	1	0	0	0	1.324
0	1	1	0	0	1	1.308
0	1	1	0	1	0	1.292
0	1	1	0	1	1	1.276
0	1	1	1	0	0	1.260
0	1	1	1	0	1	1.244
0	1	1	1	1	0	1.228
0	1	1	1	1	1	1.212

VID

5	4	3	2	1	0	VCC-Core
1	0	0	0	0	0	1.196
1	0	0	0	0	1	1.180
1	0	0	0	1	0	1.164
1	0	0	0	1	1	1.148
1	0	0	1	0	0	1.132
1	0	0	1	0	1	1.116
1	0	0	1	1	0	1.100
1	0	0	1	1	1	1.084
1	0	1	0	0	0	1.068
1	0	1	0	0	1	1.052
1	0	1	0	1	0	1.036
1	0	1	0	1	1	1.020
1	0	1	1	0	0	1.004
1	0	1	1	0	1	0.988
1	0	1	1	1	0	0.972
1	0	1	1	1	1	0.956
1	1	0	0	0	0	0.940
1	1	0	0	0	1	0.924
1	1	0	0	1	0	0.908
1	1	0	0	1	1	0.892
1	1	0	1	0	0	0.876
1	1	0	1	0	1	0.860
1	1	0	1	1	0	0.844
1	1	0	1	1	1	0.828
1	1	1	0	0	0	0.812
1	1	1	0	0	1	0.796
1	1	1	0	1	0	0.780
1	1	1	0	1	1	0.764
1	1	1	1	0	0	0.748
1	1	1	1	0	1	0.732
1	1	1	1	1	0	0.716
1	1	1	1	1	1	0.700

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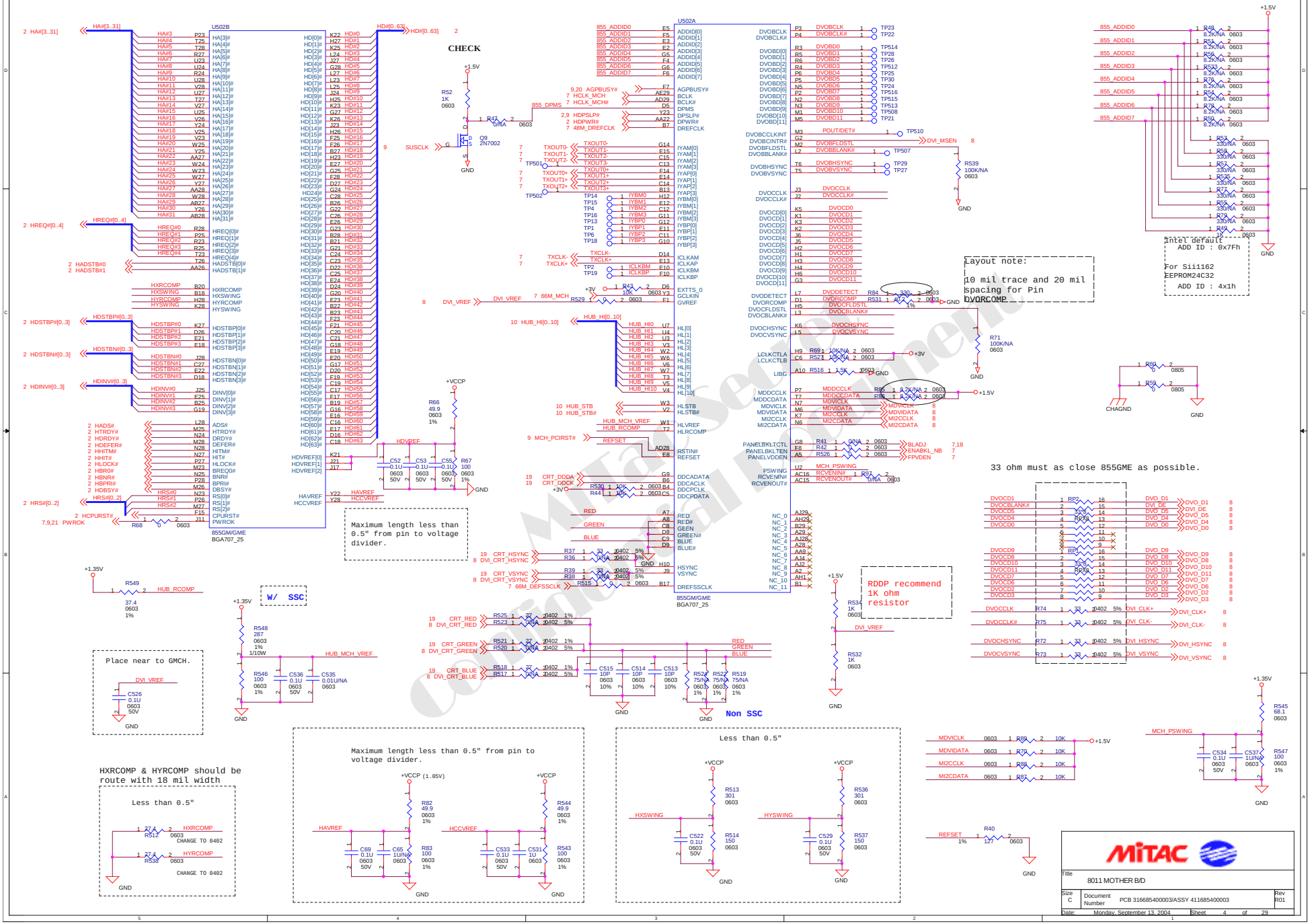
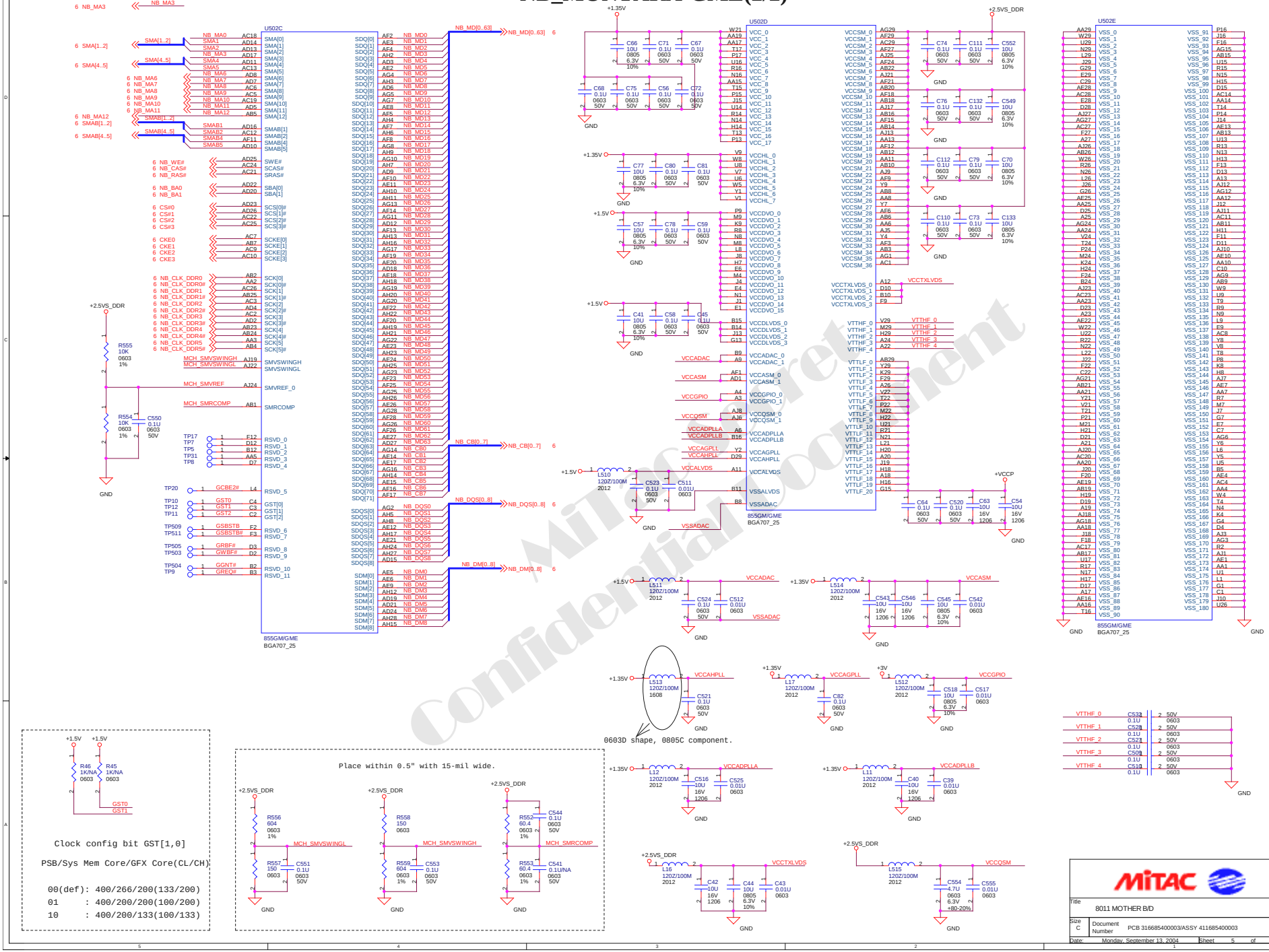
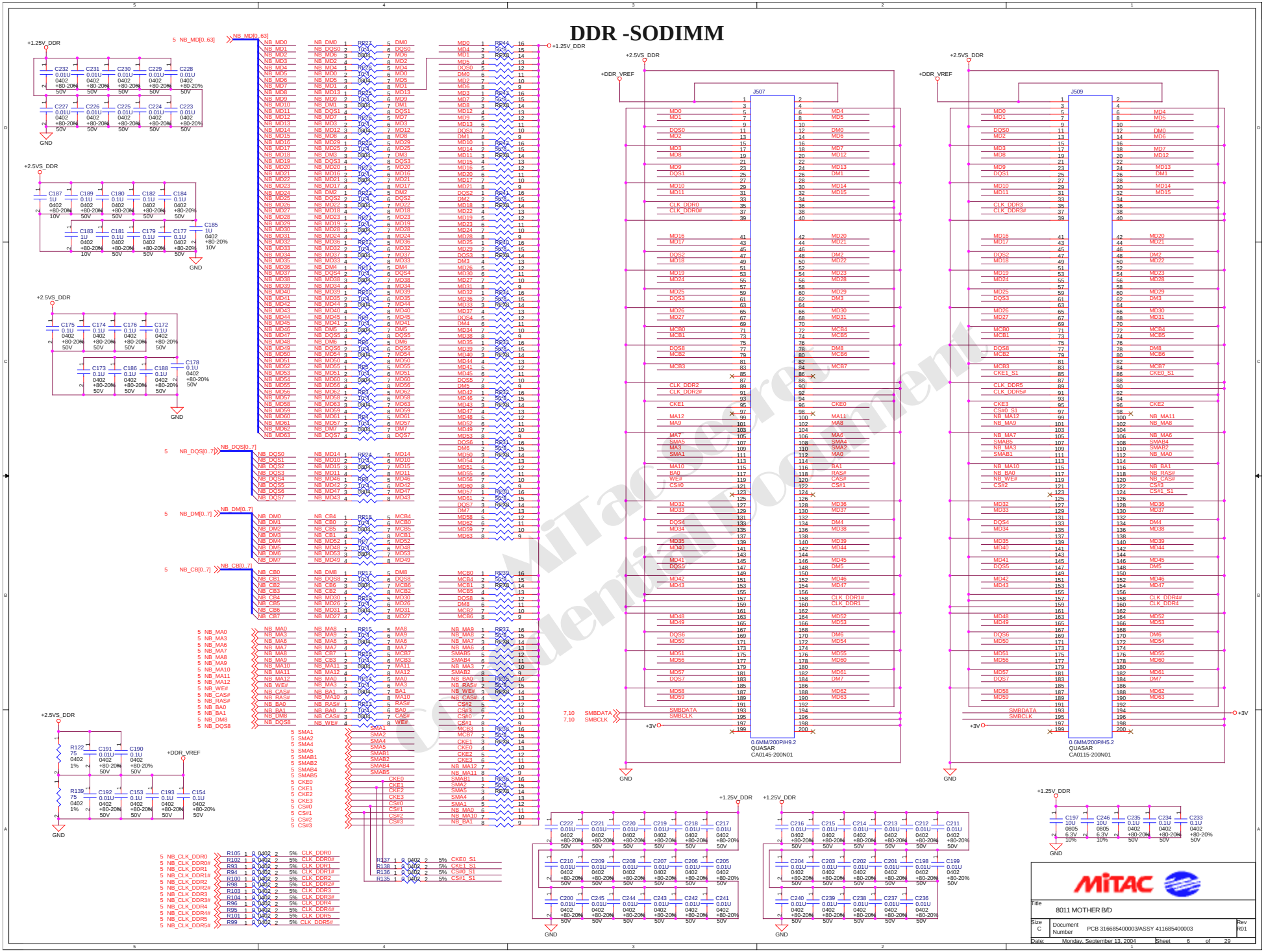
NB-MONTARA-GME(1/2)



NB_MONTARA-GME(2/2)





CLOCK SYNTHERIZER

001 →

FS2	FS1	FS0	CPU	3V66[5:0]	PCI*
X	0	0	166.66	66.66	33.33
X	0	1	100.00	66.66	33.33
X	1	0	200.00	66.66	33.33
X	1	1	133.33	66.66	33.33
Mid	0	0	Tristate	Tristate	Tristate
Mid	0	1	TCLK/2	TCLK/2	TCLK/2
Mid	1	0	Reserved	Reserved	Reserved
Mid	1	1	Reserved	Reserved	Reserved

0:0V
1:3.3V

UNIT: MHz

Layout note: Place crystal within 500 mils of CLK Gen.

U7
ICS950812
TSSOP56

INVERTER

FUSE 5A,0805C_1206 shape

Inverter
MA/11PX1/RA
ACES
87213-1100

Display LCD

When inverter use +5V ADD Q4,R398,R399,R4 and DEL R323

When inverter use +3V ADD R323 and DEL Q4,R398,R399,R4

Cover Switch

Pannel ID

LCD_ID0	LCD_ID1	LCD_ID2	PANEL TYPE
0	0	1	
1	0	1	
0	1	1	
0	1	0	
1	1	0	

To SB

MA/15PX2/ST
ACES
88107-300X

MiTAC

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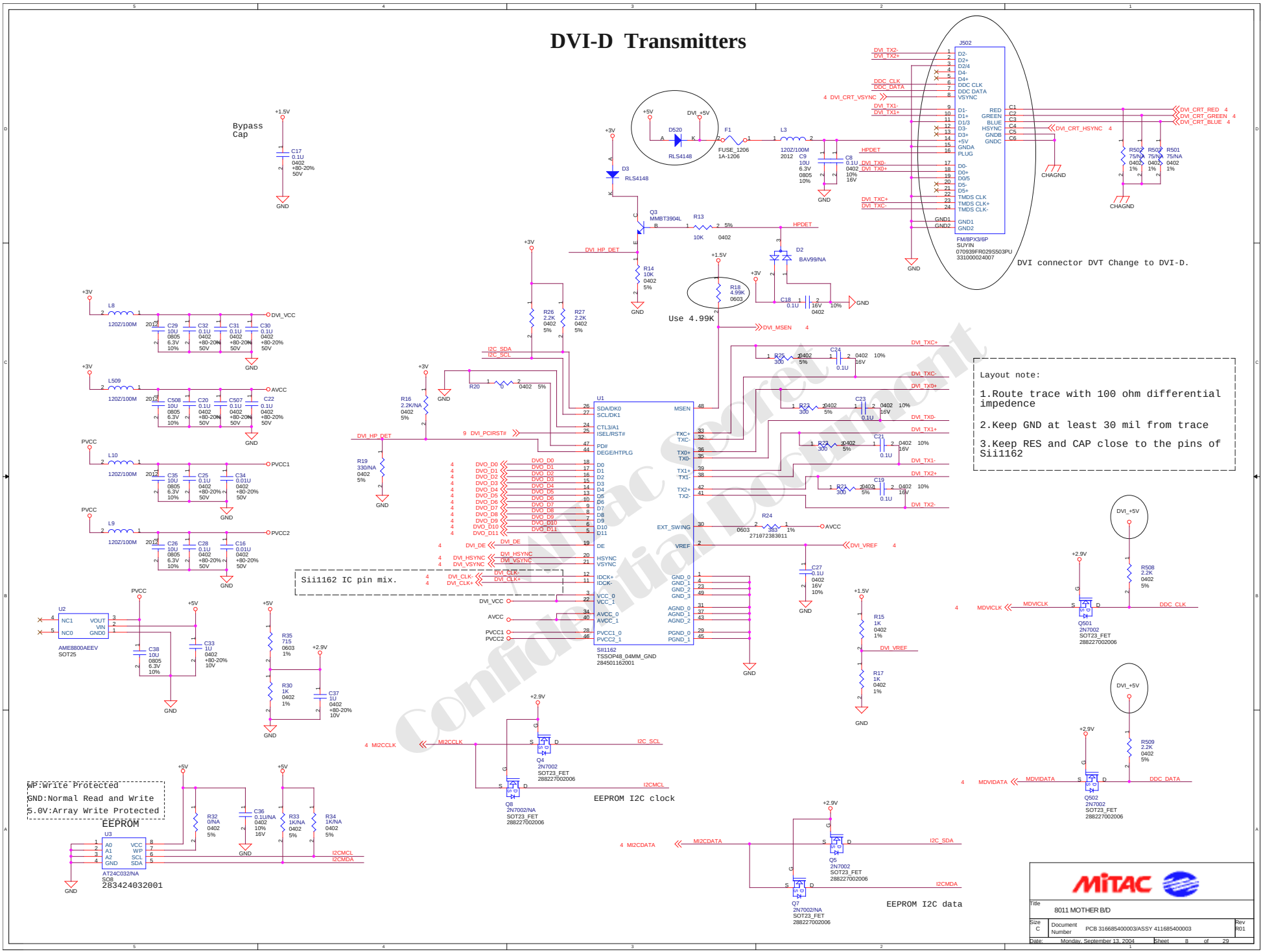
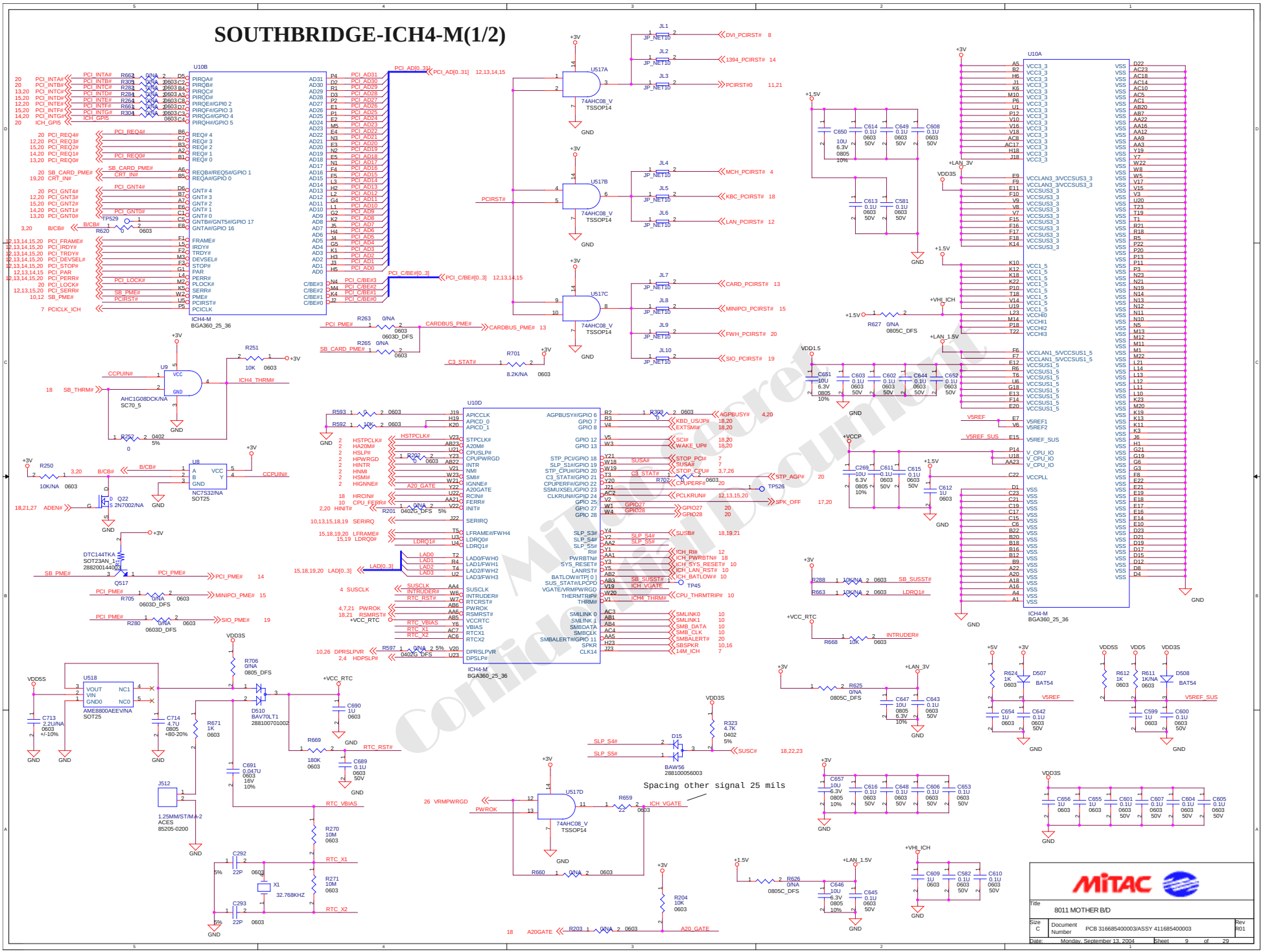
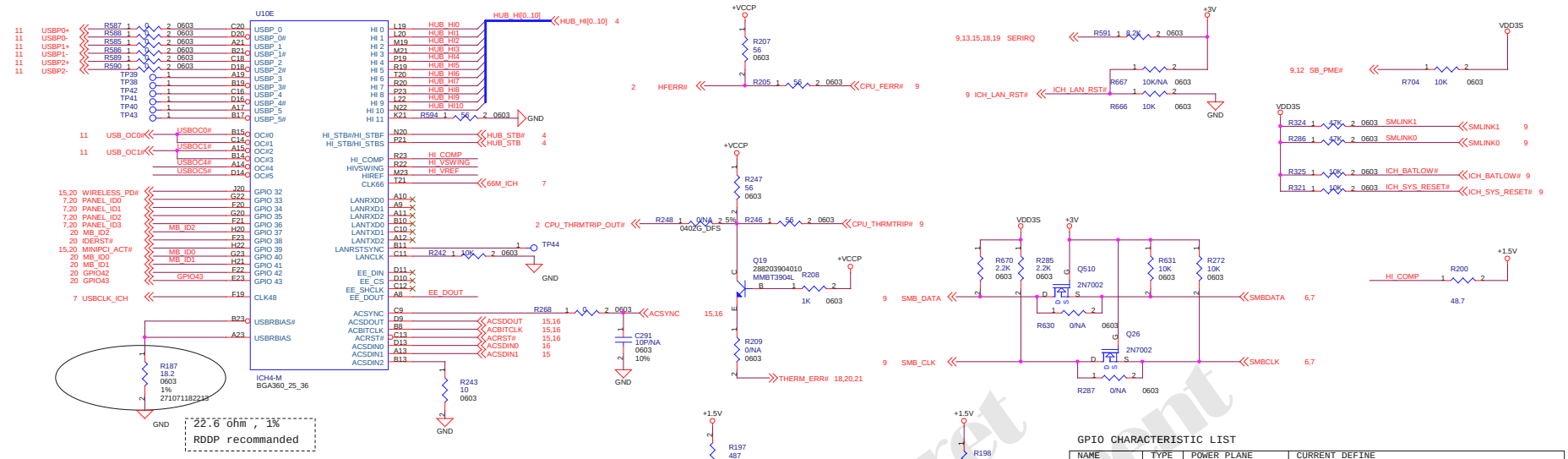
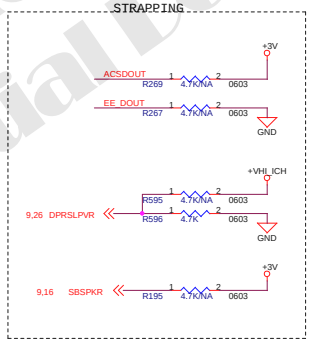




SOUTHBRIDGE-ICH4-M(2/2)



STRAPPING



STRAPPING AT RISING EDGE OF PWROK

STRAPPING PINS	FUNCTIONS
ACSDOUT	SAFE MODE
EEDOUT	RESERVED
GNTA#	OP-BLOCK SWAP OVERRIDE
DPRSLPVR	HUB INTERFACE TERMINATION SCHEME
HUB_ICH_COMP	HUB INTERFACE SCHEME(1.0 OR 1.5)
SBSPKR	NO REBOOT

GPIO CHARACTERISTIC LIST

	NAME	TYPE	POWER PLANE	CURRENT DEFINE
B5	GPI[0]	I	MAIN POWER WELL	CRT_IN#
A6	GPI[1]	I	MAIN POWER WELL	SB_CARD_PME#
C8	GPI[2]	I	MAIN POWER WELL	PCI_INTE#
D7	GPI[3]	I	MAIN POWER WELL	PCI_INTF#
C3	GPI[4]	I	MAIN POWER WELL	PCI_INTG#
C4	GPI[5]	I	MAIN POWER WELL	ICH_GPI5
R2	GPI[6]	I	MAIN POWER WELL	AGPBUSY#
R3	GPI[7]	I	MAIN POWER WELL	KBD_US/JP#
V4	GPI[8]	I	RESUME POWER WELL	EXTSMI#
AA5	GPI[11]	I	RESUME POWER WELL	SMBALERT#(Pull high only)
V5	GPI[12]	I	RESUME POWER WELL	SCI#
W3	GPI[13]	I	RESUME POWER WELL	WAKE_UP#
E8	GPO[16]	O	MAIN POWER WELL	X
C5	GPO[17]	O	MAIN POWER WELL	X
Y21	GPO[18]	O	MAIN POWER WELL	STOP_PCI#
W18	GPO[19]	O	MAIN POWER WELL	SUSA#
W19	GPO[20]	O	MAIN POWER WELL	STOP_CPU#
T3	GPO[21]	O	MAIN POWER WELL	C3_STAT#
Y20	GPO[22]	OD	MAIN POWER WELL	CPUPERF#
J21	GPO[23]	O	MAIN POWER WELL	X
AC2	GPIO[24]	I/O	RESUME POWER WELL	PCLKRUN#
V2	GPIO[25]	I/O	RESUME POWER WELL	SPK_OFF
W1	GPIO[27]	I/O	RESUME POWER WELL	X
W4	GPIO[28]	I/O	RESUME POWER WELL	X
J20	GPIO[32]	I/O	MAIN POWER WELL	WIRELESS_PD#
G22	GPIO[33]	I/O	MAIN POWER WELL	PANEL_ID0
F20	GPIO[34]	I/O	MAIN POWER WELL	PANEL_ID1
G20	GPIO[35]	I/O	MAIN POWER WELL	PANEL_ID2
F21	GPIO[36]	I/O	MAIN POWER WELL	PANEL_ID3
H20	GPIO[37]	I/O	MAIN POWER WELL	MB_ID2
F23	GPIO[38]	I/O	MAIN POWER WELL	IDERST#
H22	GPIO[39]	I/O	MAIN POWER WELL	MINIPCI_ACT#
G23	GPIO[40]	I/O	MAIN POWER WELL	MB_ID0
H21	GPIO[41]	I/O	MAIN POWER WELL	MB_ID1
F22	GPIO[42]	I/O	MAIN POWER WELL	X
E23	GPIO[43]	I/O	MAIN POWER WELL	X

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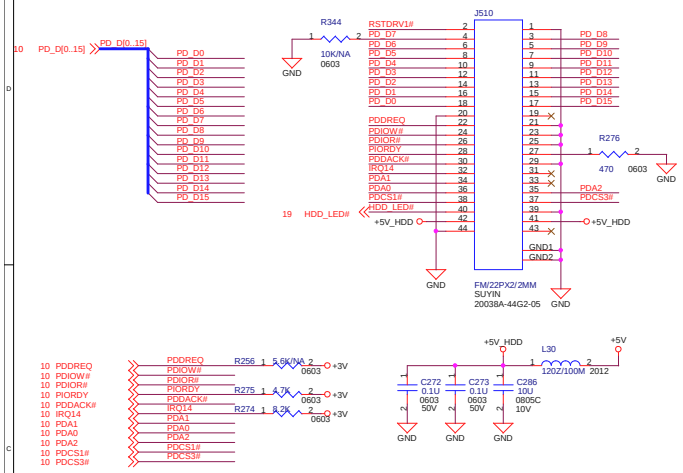
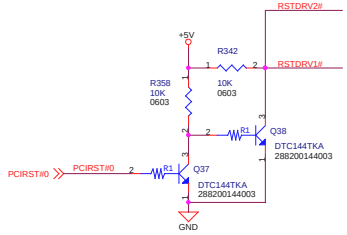
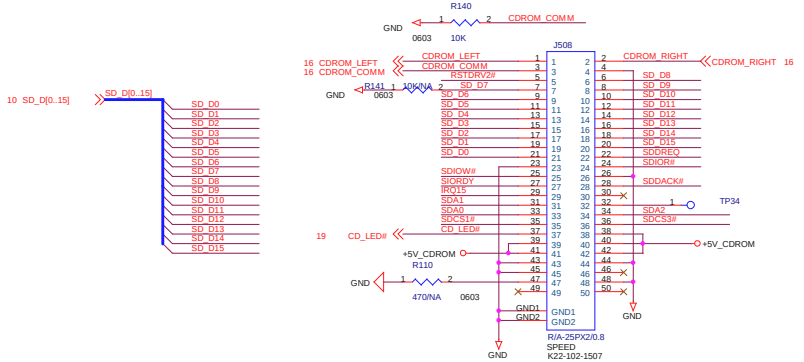
HDD- PRIMARY IDE CONNECTOR

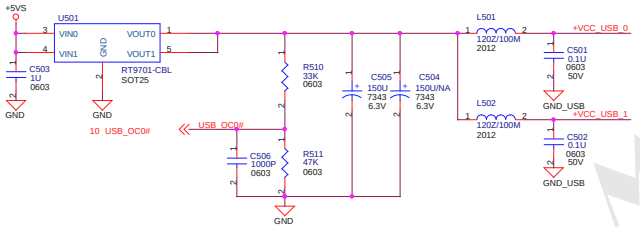


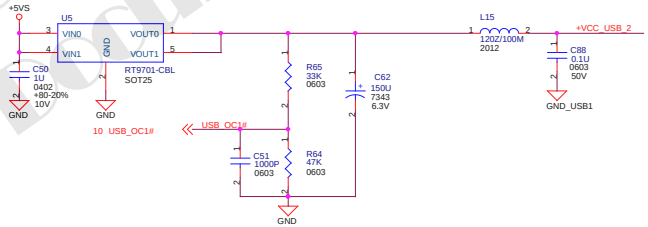


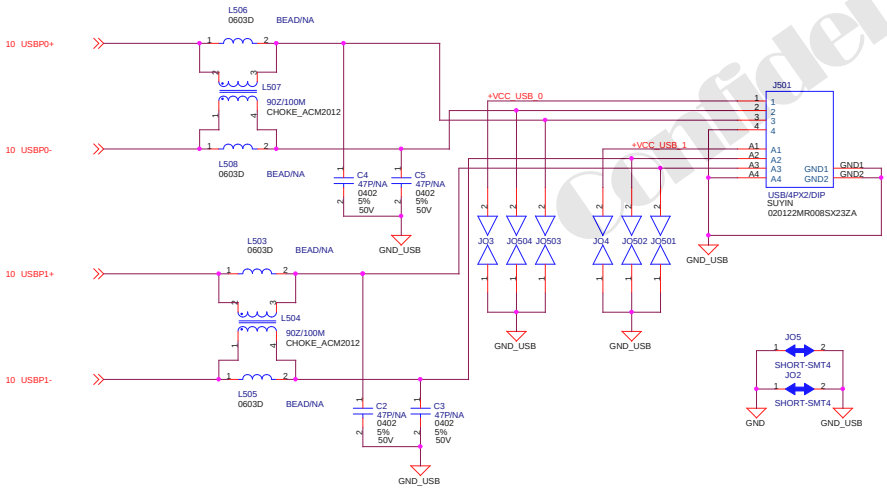
CDROM- SECONDARY IDE CONNECTOR

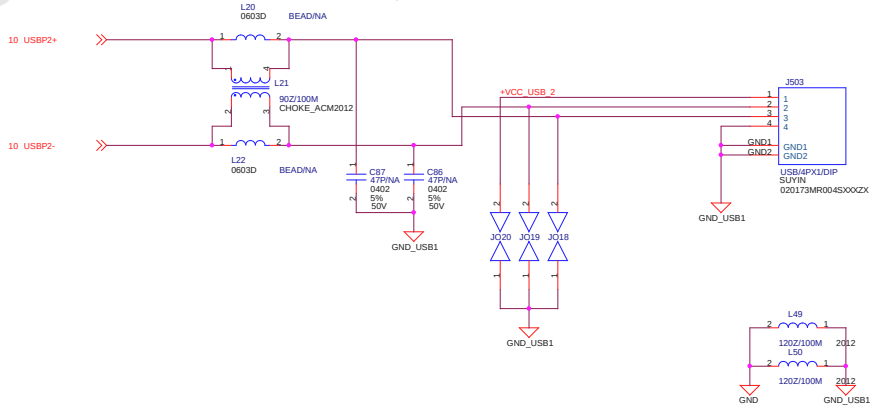


USB CONNECOTR









MiTac Secret
Confidential Document

MiTAC

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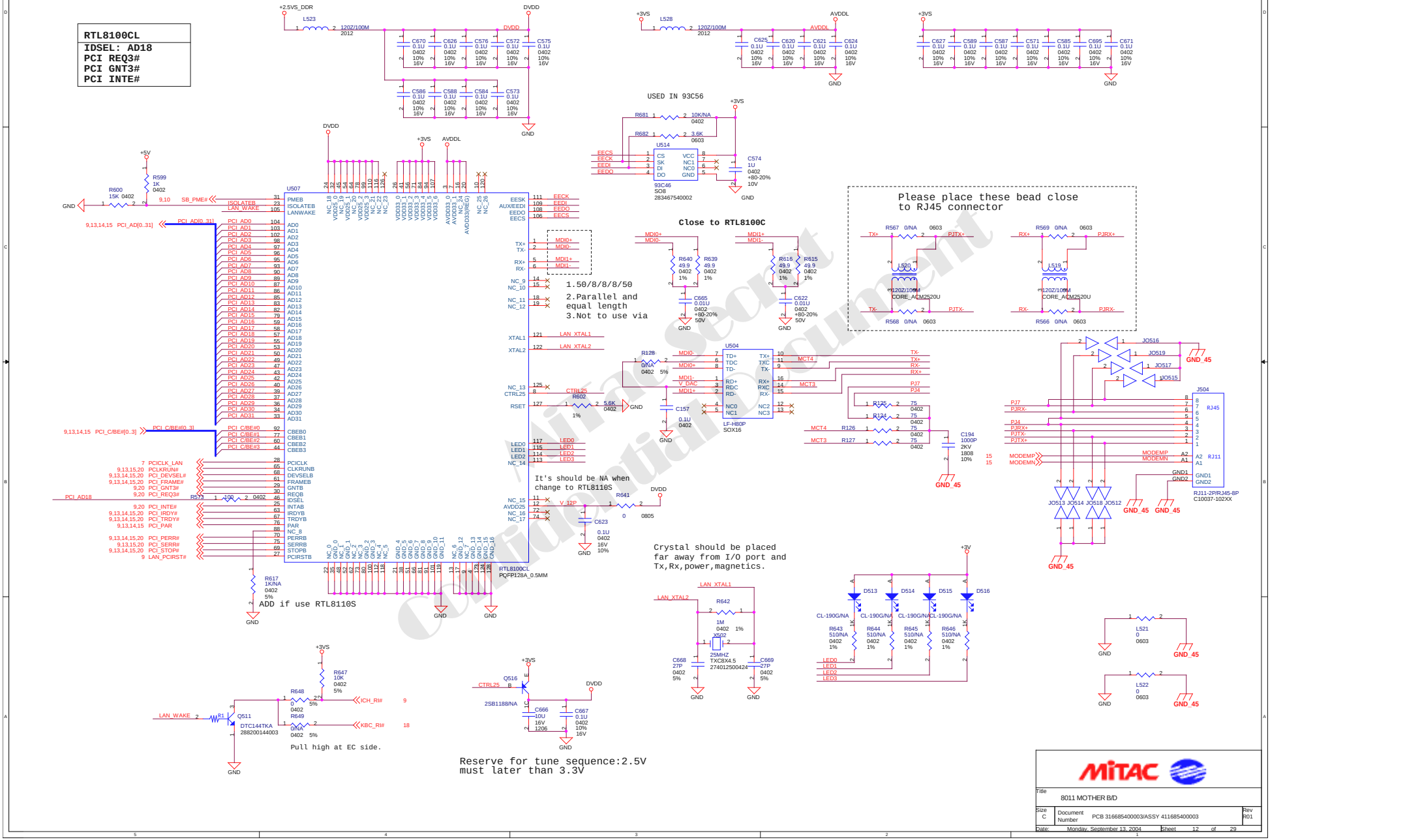
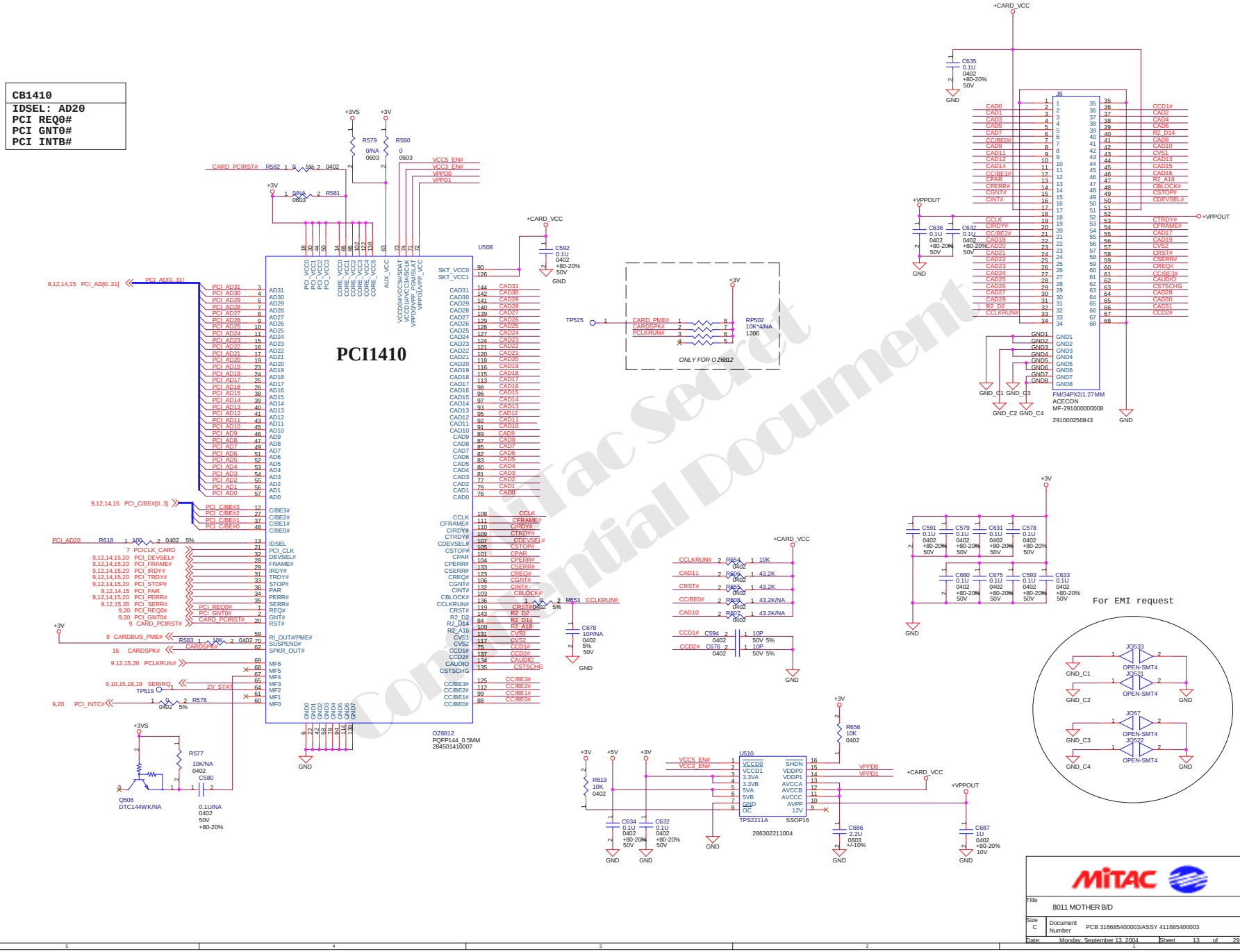
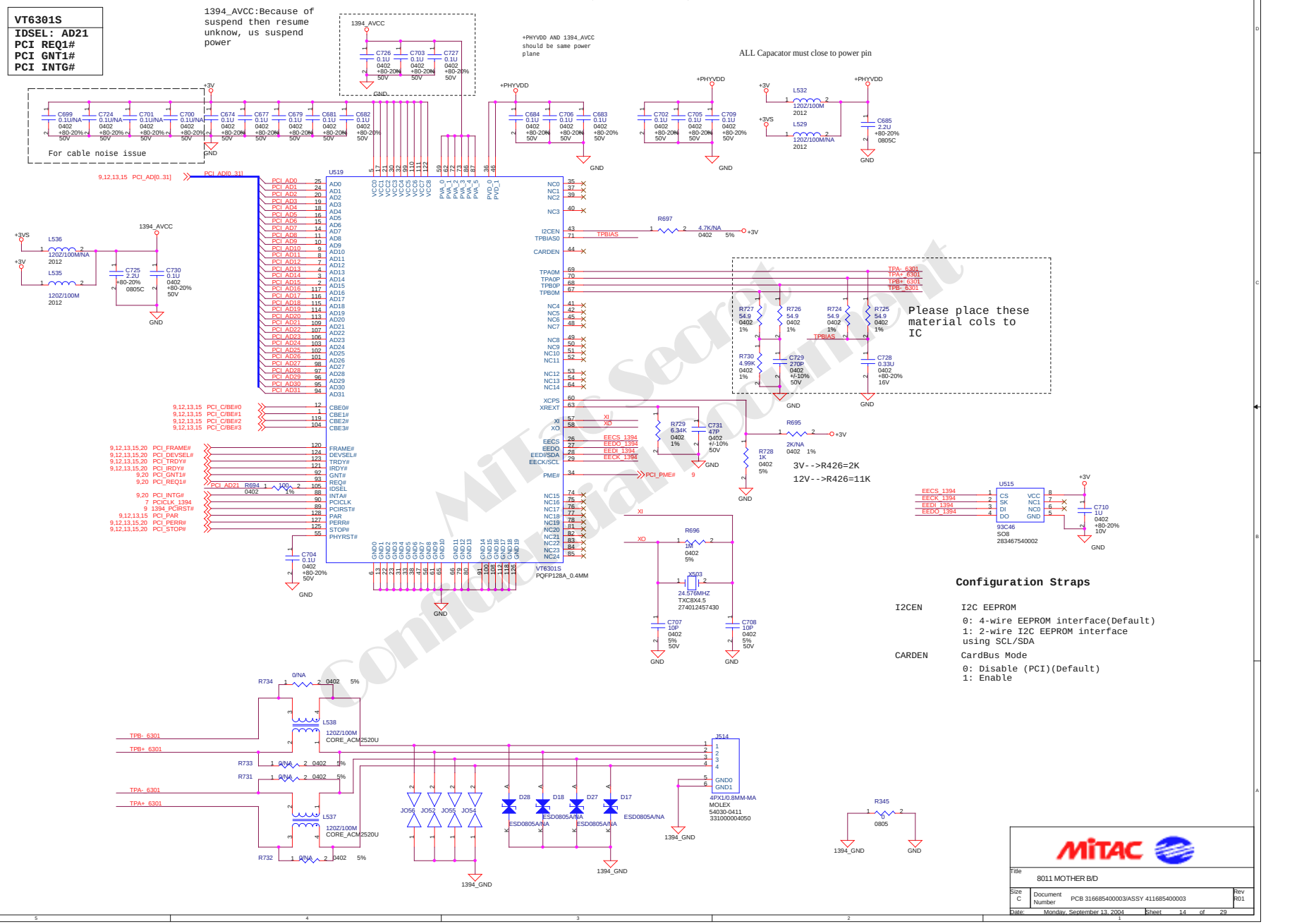
LAN-RTL8100CL



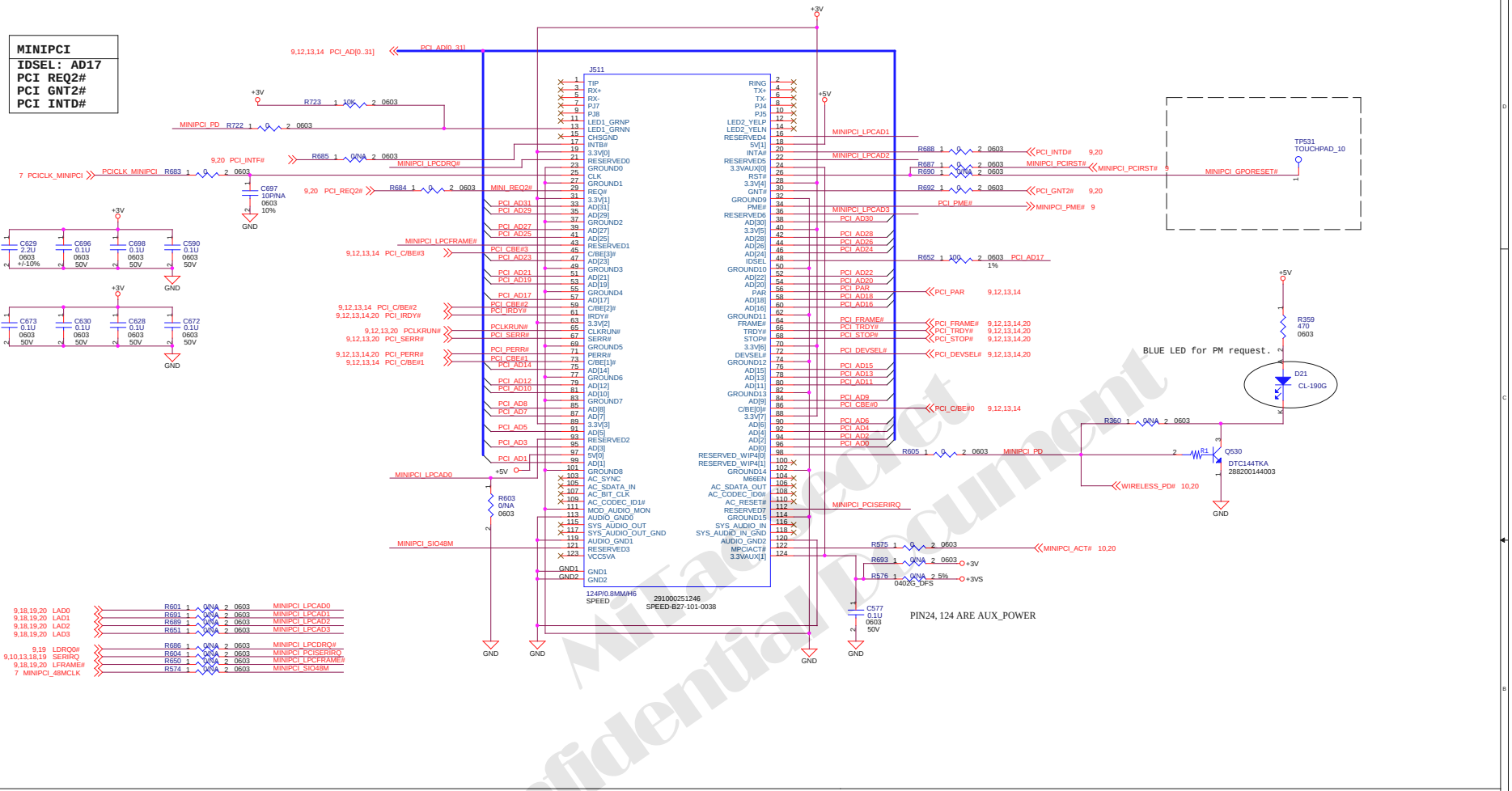
CardBus (PCI1410)



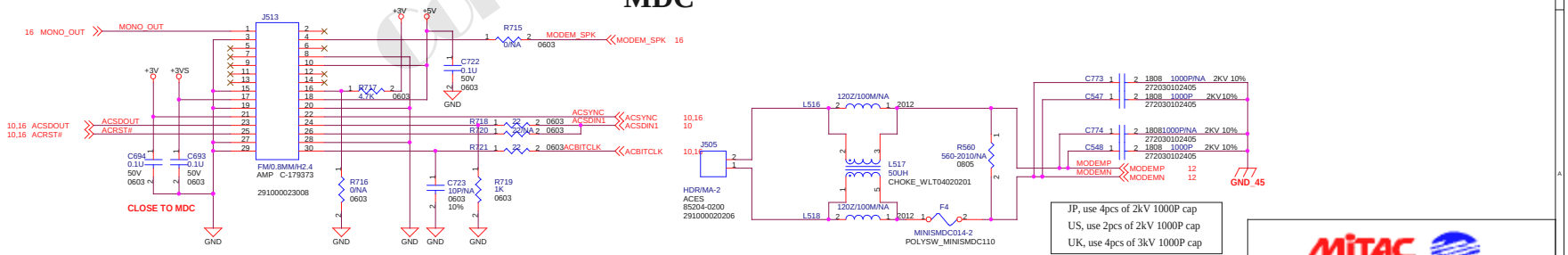
IEEE1394(VT6301S)



MINI-PCI



MDC



MiTAC Secret Confidential Document

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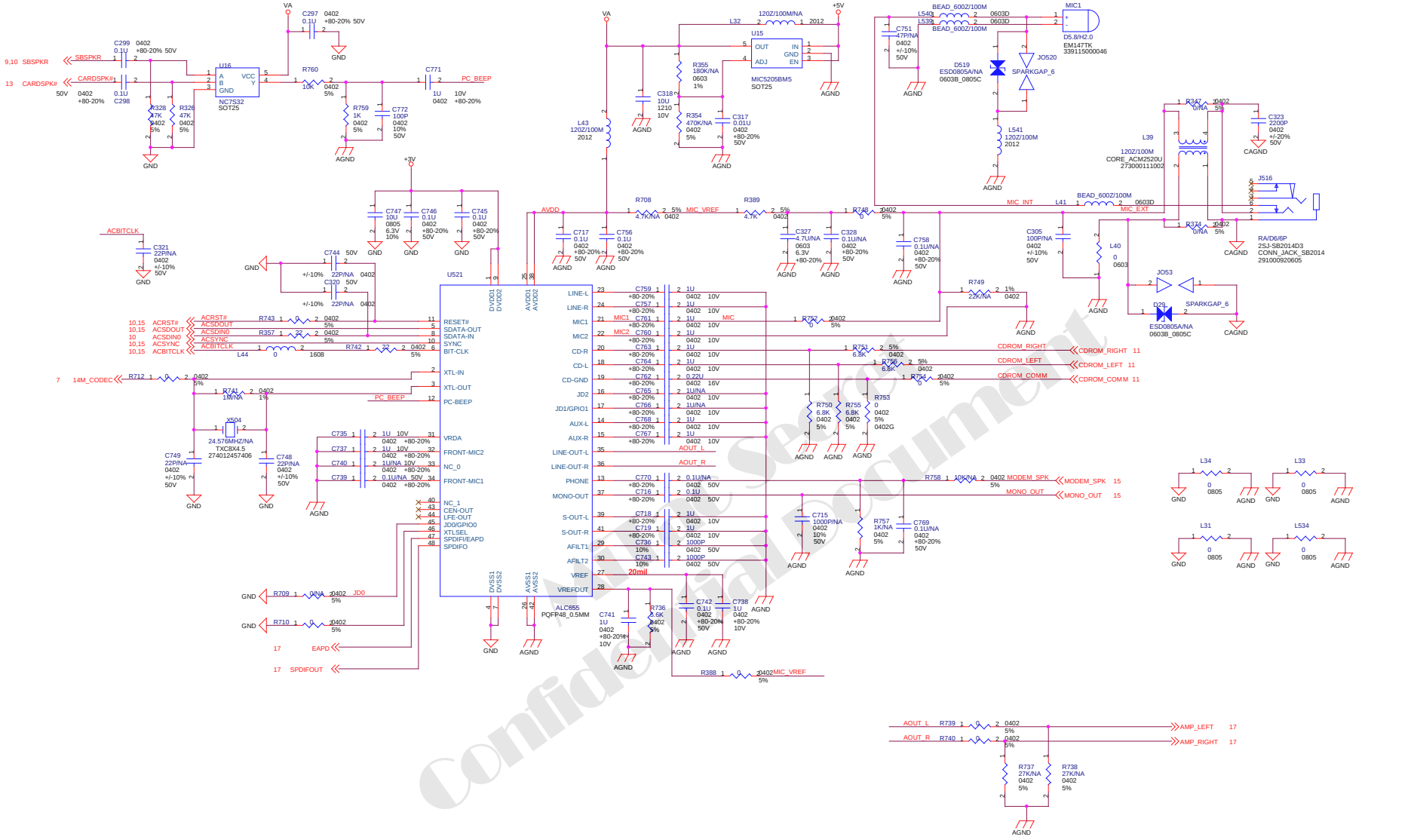
AUDIO CODEC(ALC655)



MiTAC

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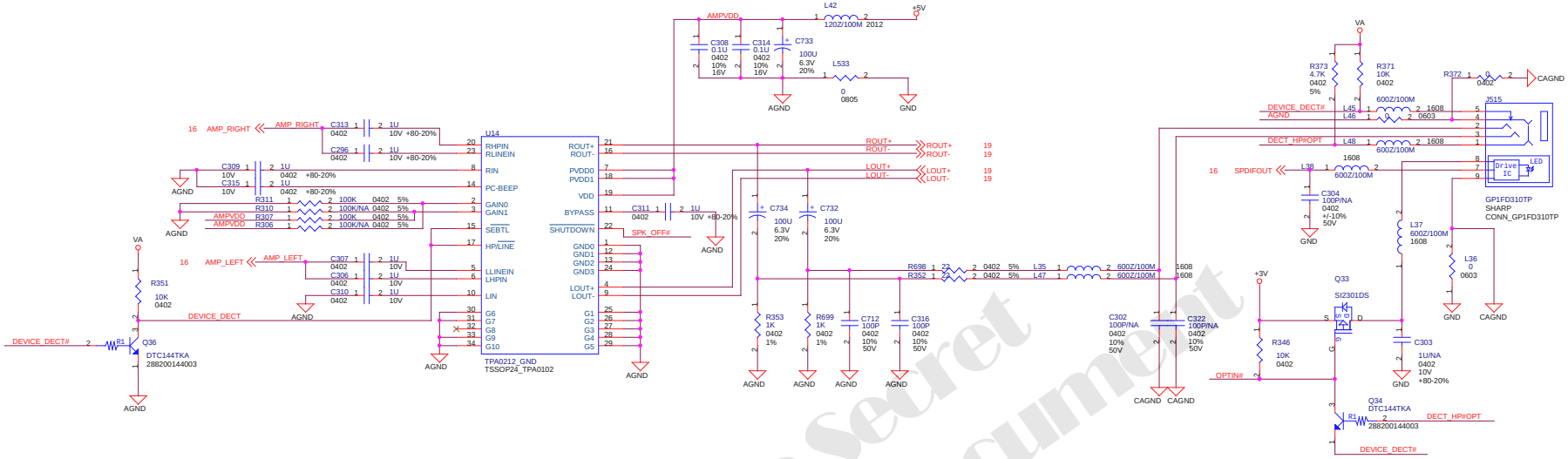
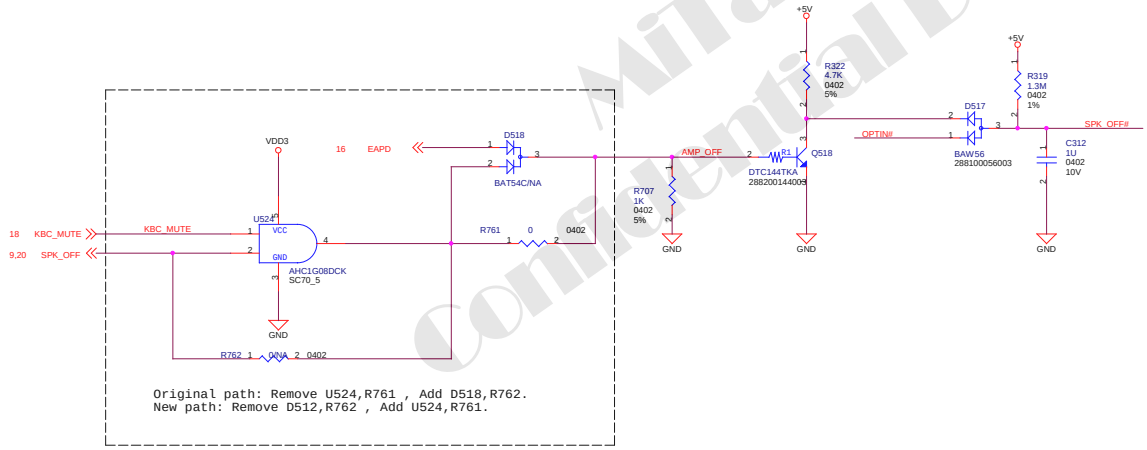
AUDIO AMPLIFIER

DEVICE_DECT#	DECT_HP#/OPT	REMARK
0	0	HP in
0	1	OPT in
1	0	no this condition
1	1	on device





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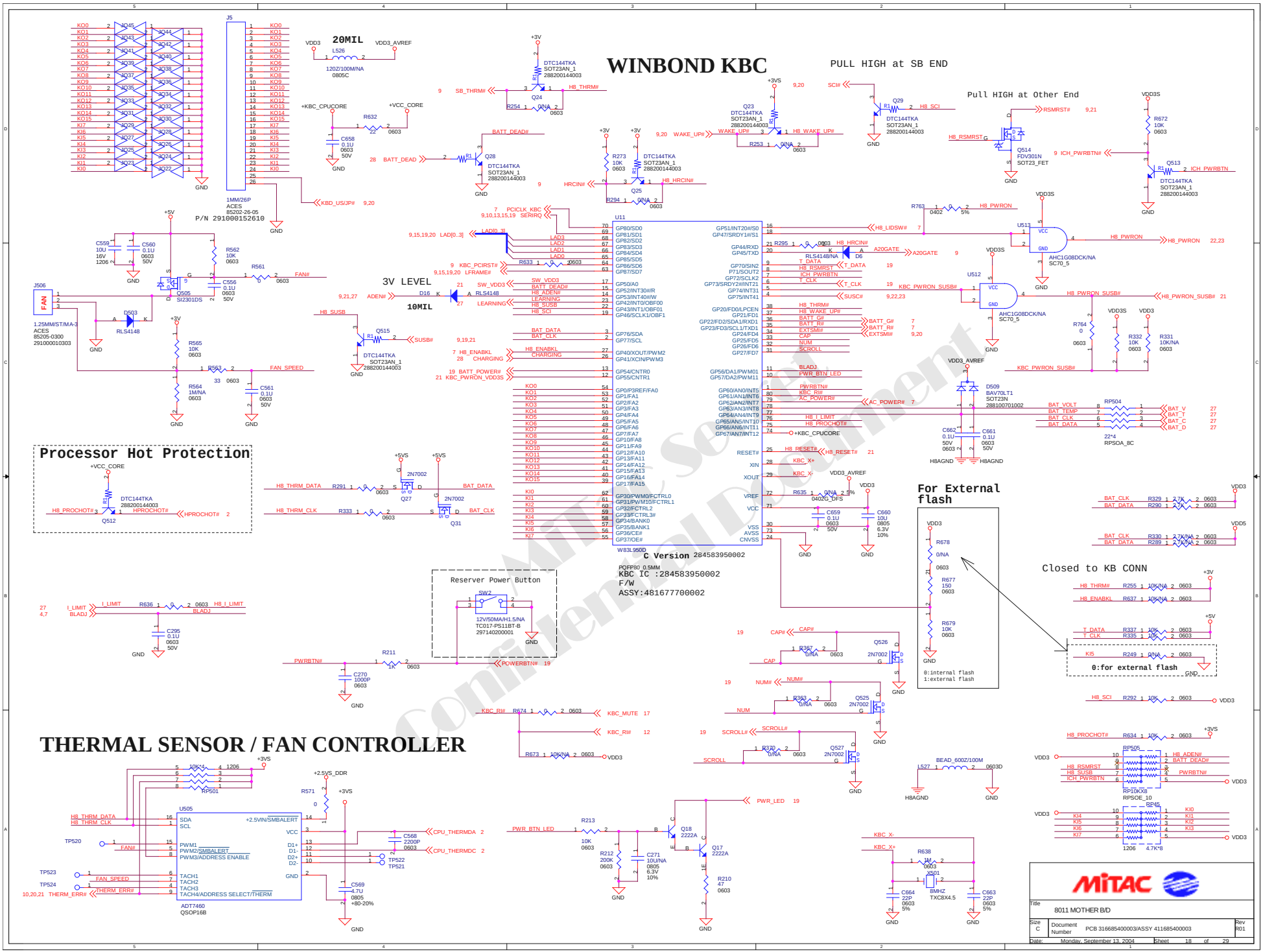
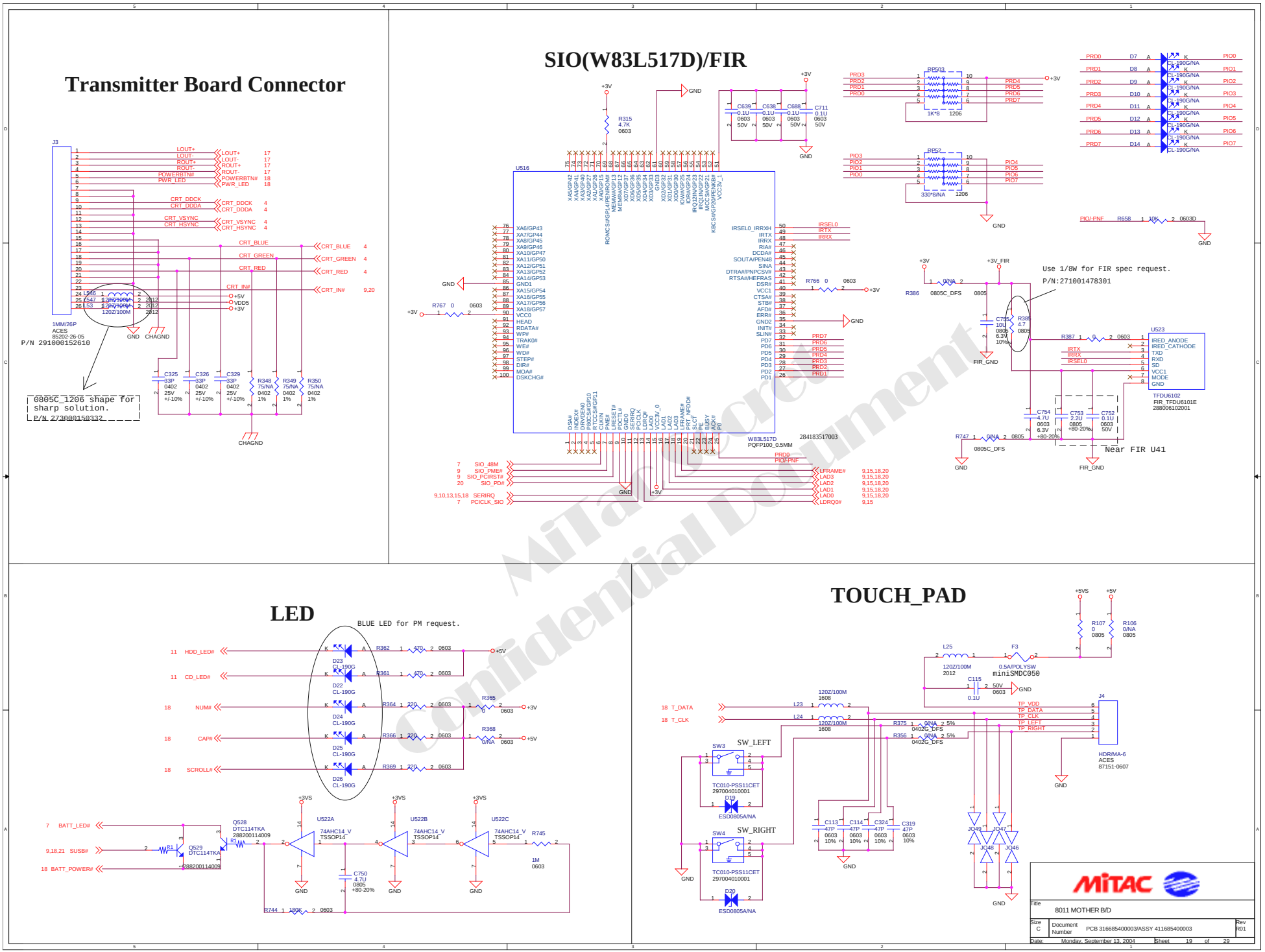
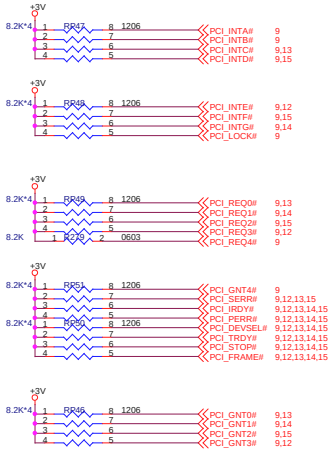


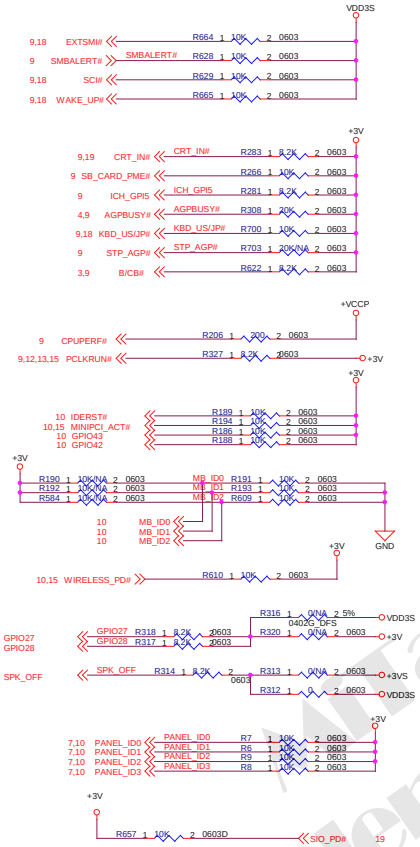


PULL -HIGH

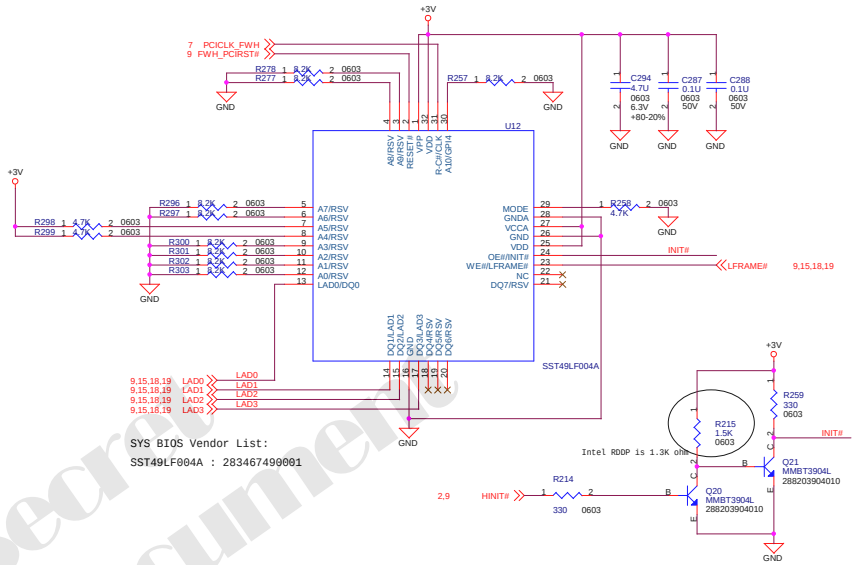
PCI PULL HIGH

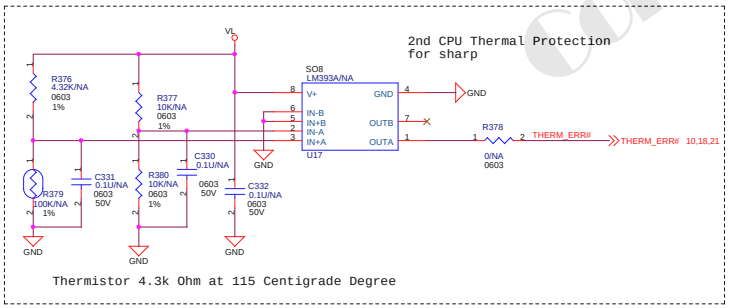


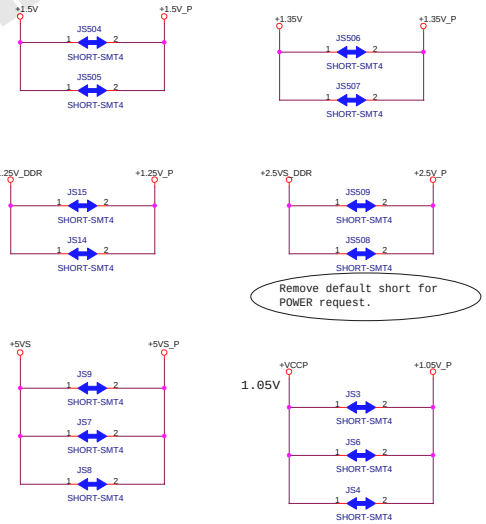
GPIO PULL HIGH



FWH







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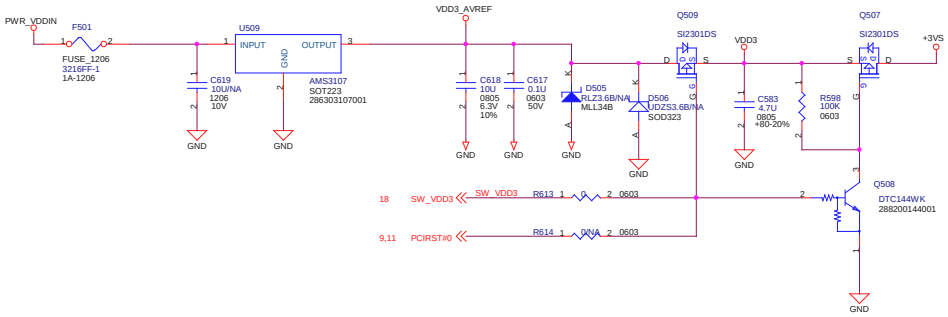
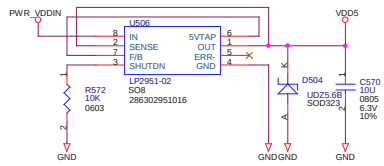
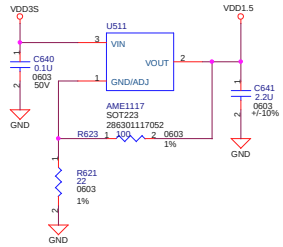
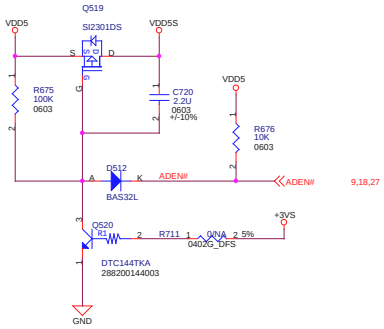
POWER ON PERPHERIAL CIRCUIT

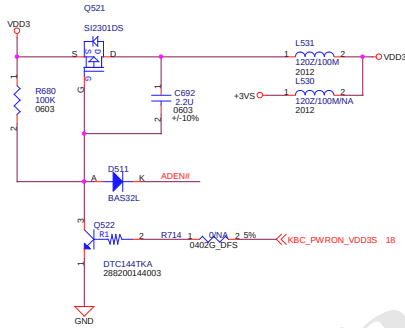


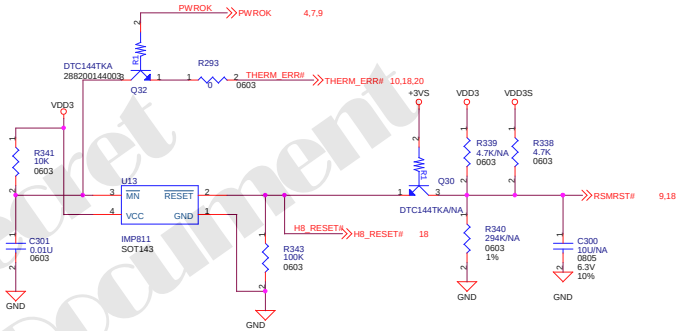


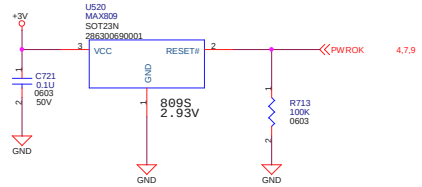


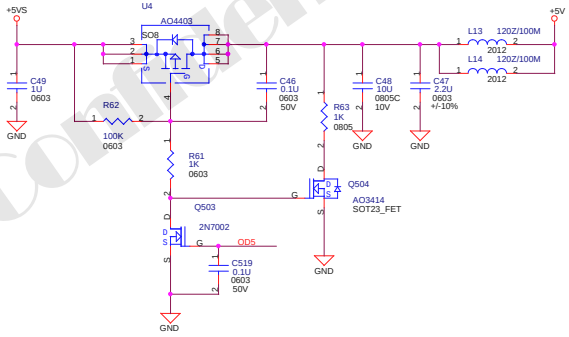
H8 RESET# / RSMRST#

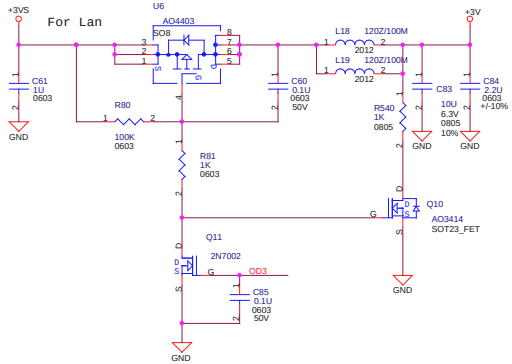


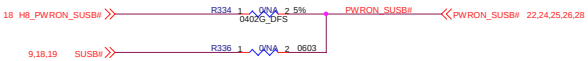












MiTAC

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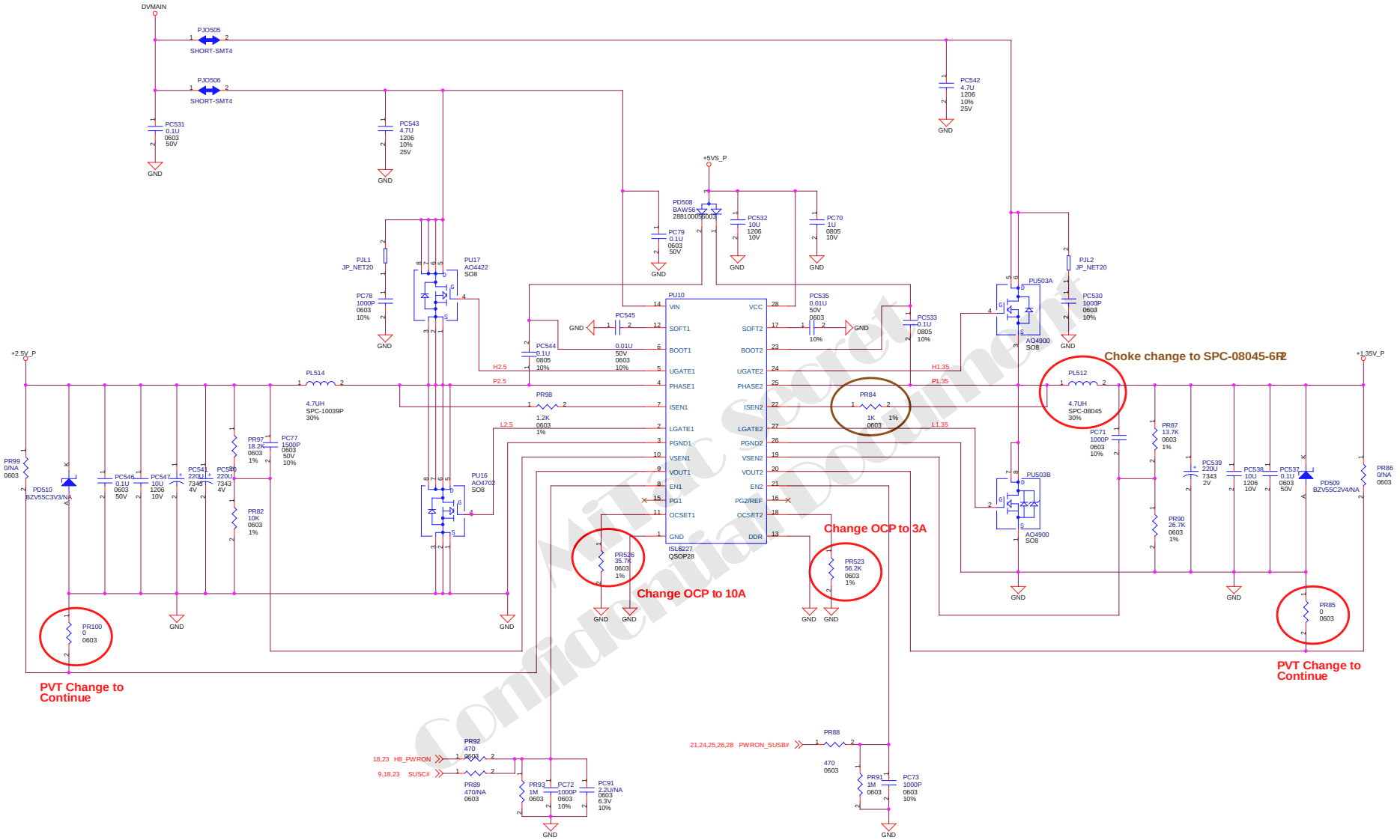
+2.5V_P/+1.35V_P



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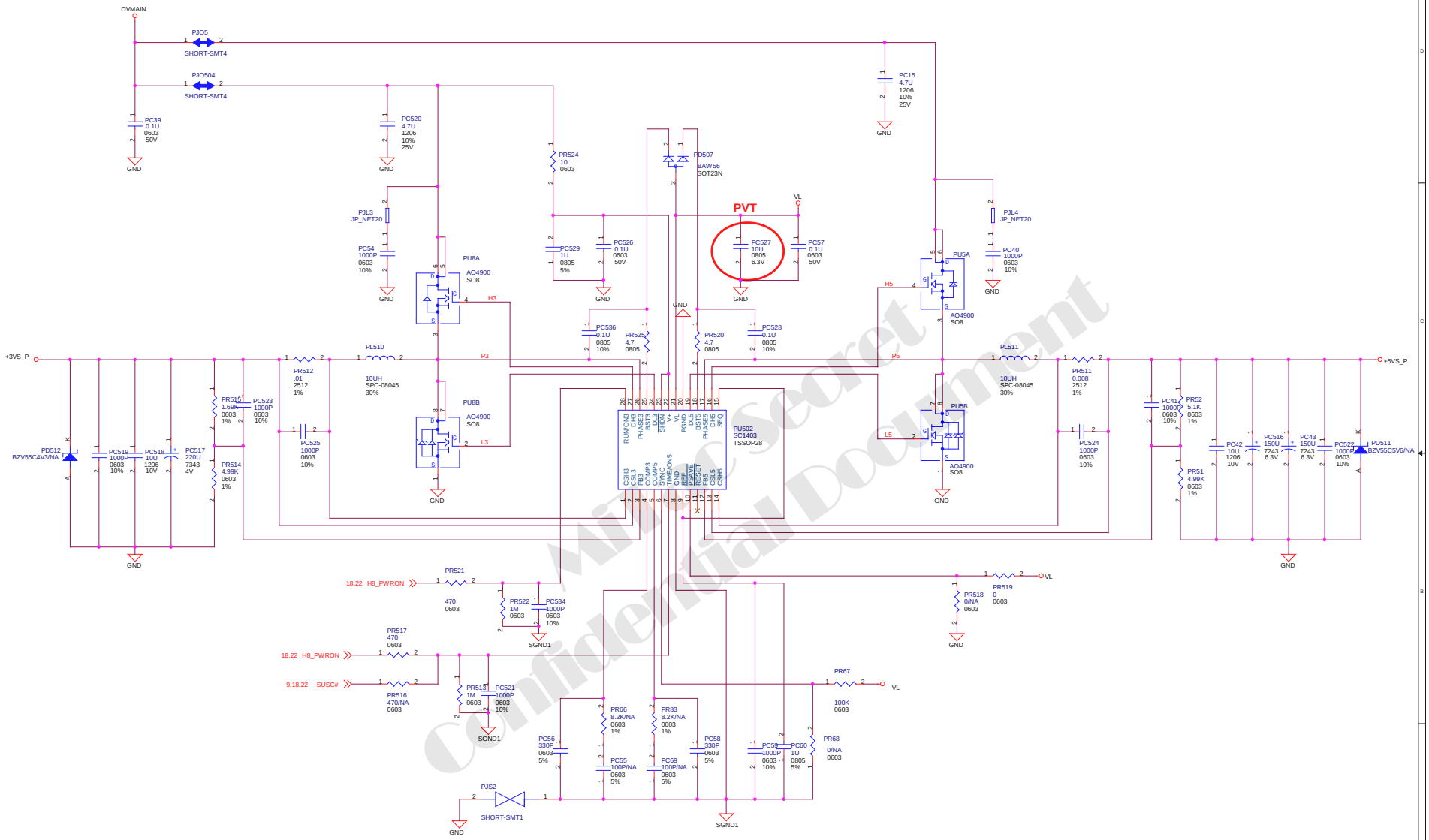
+3VS_P/+5VS_P



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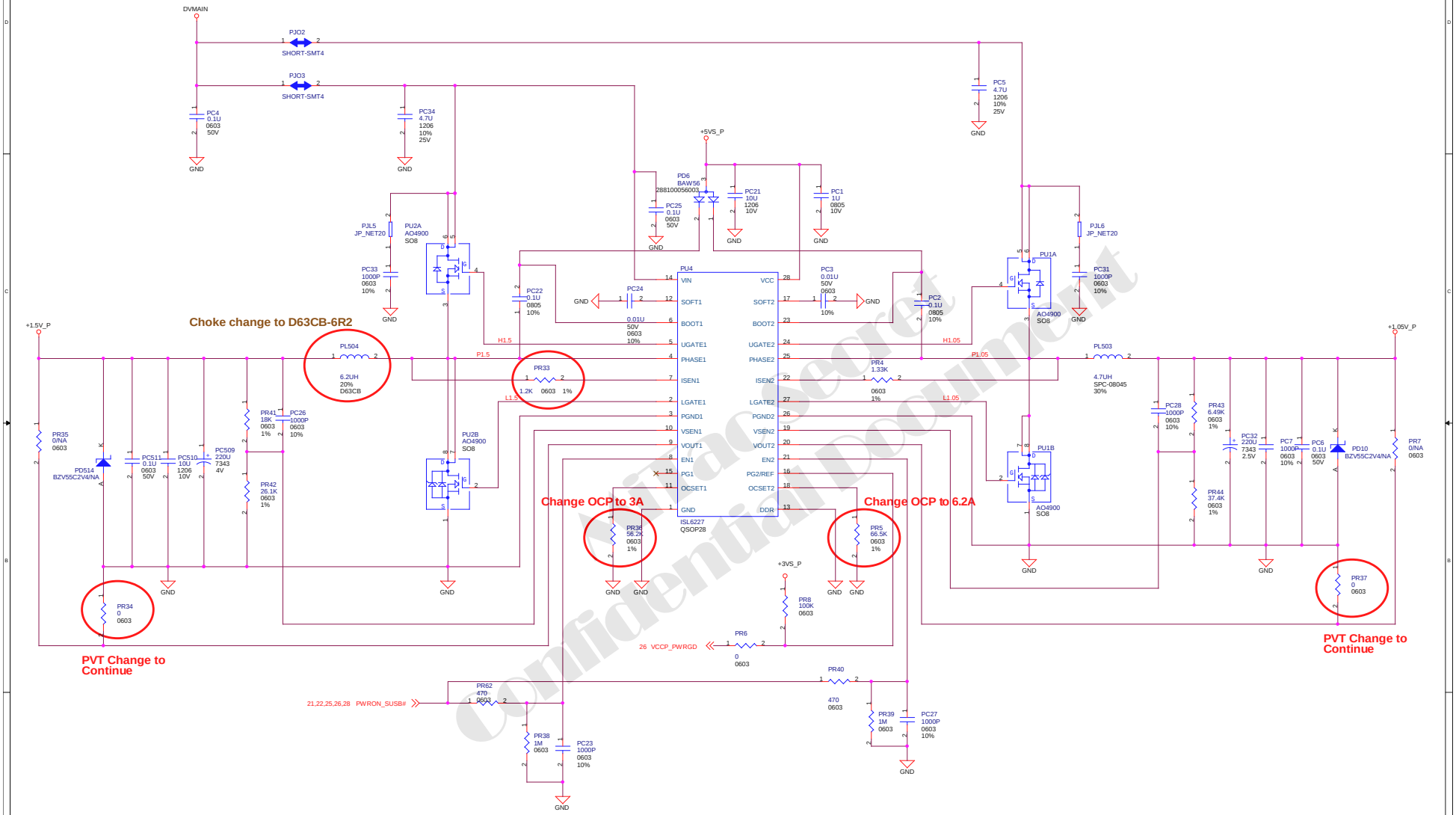
+1.5V_P/+1.05V_P



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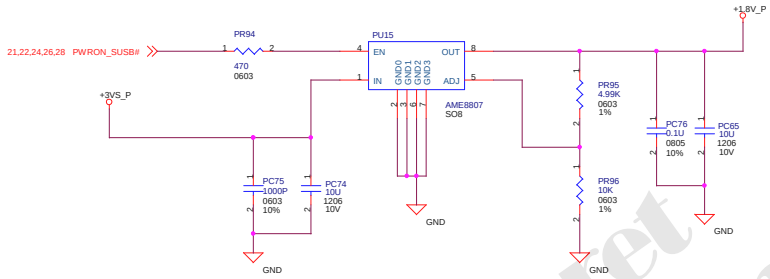
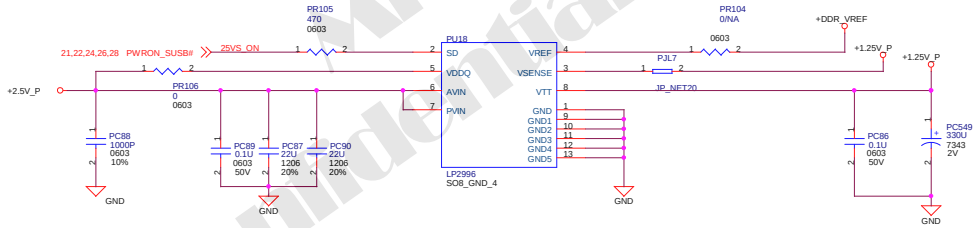
+1.8V_P/+1.25V_P





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Size: C | Document Number: PCB 316685400003/ASSY 411685400003 | Rev: R01

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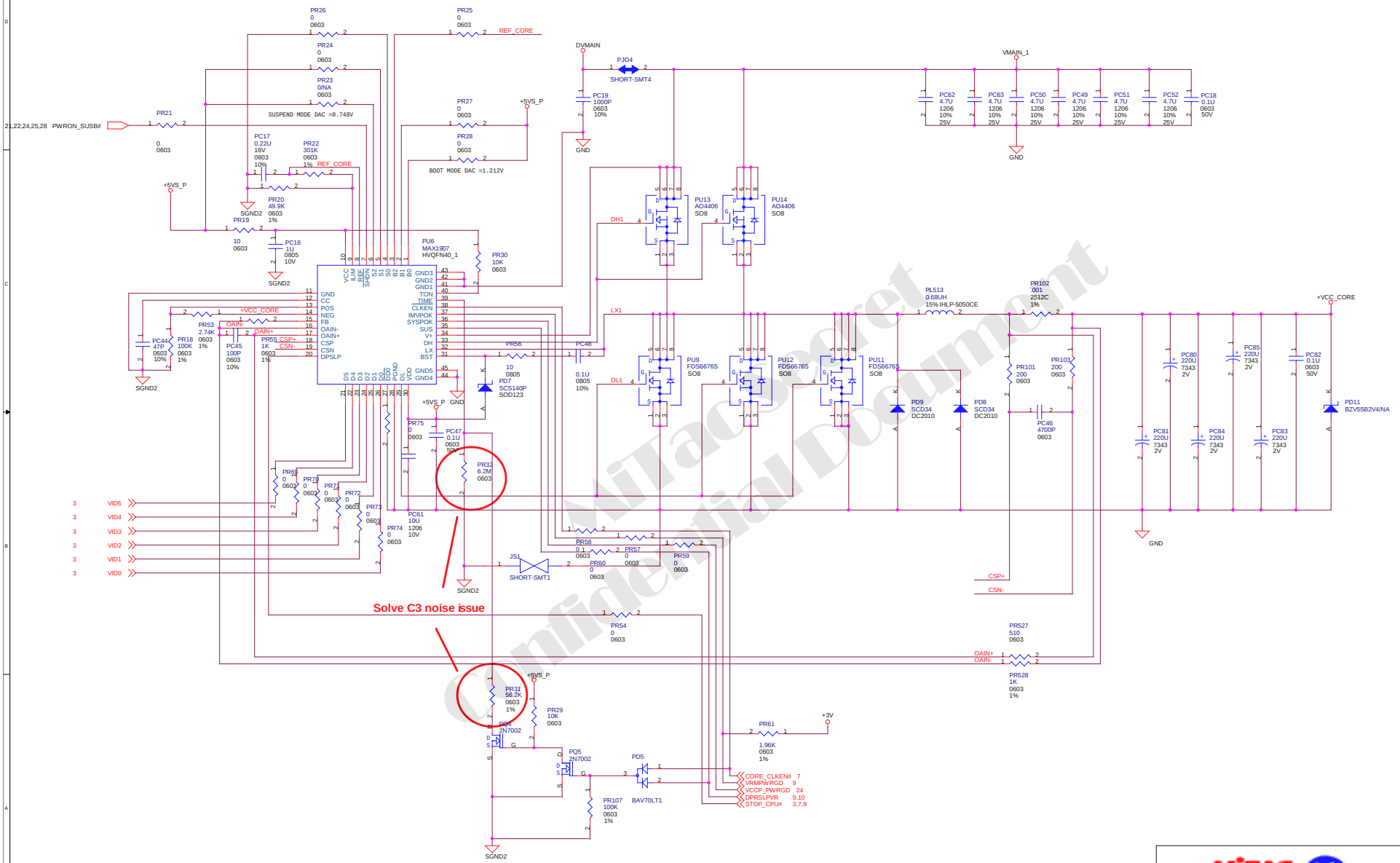
CPU_CORE



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Size	C
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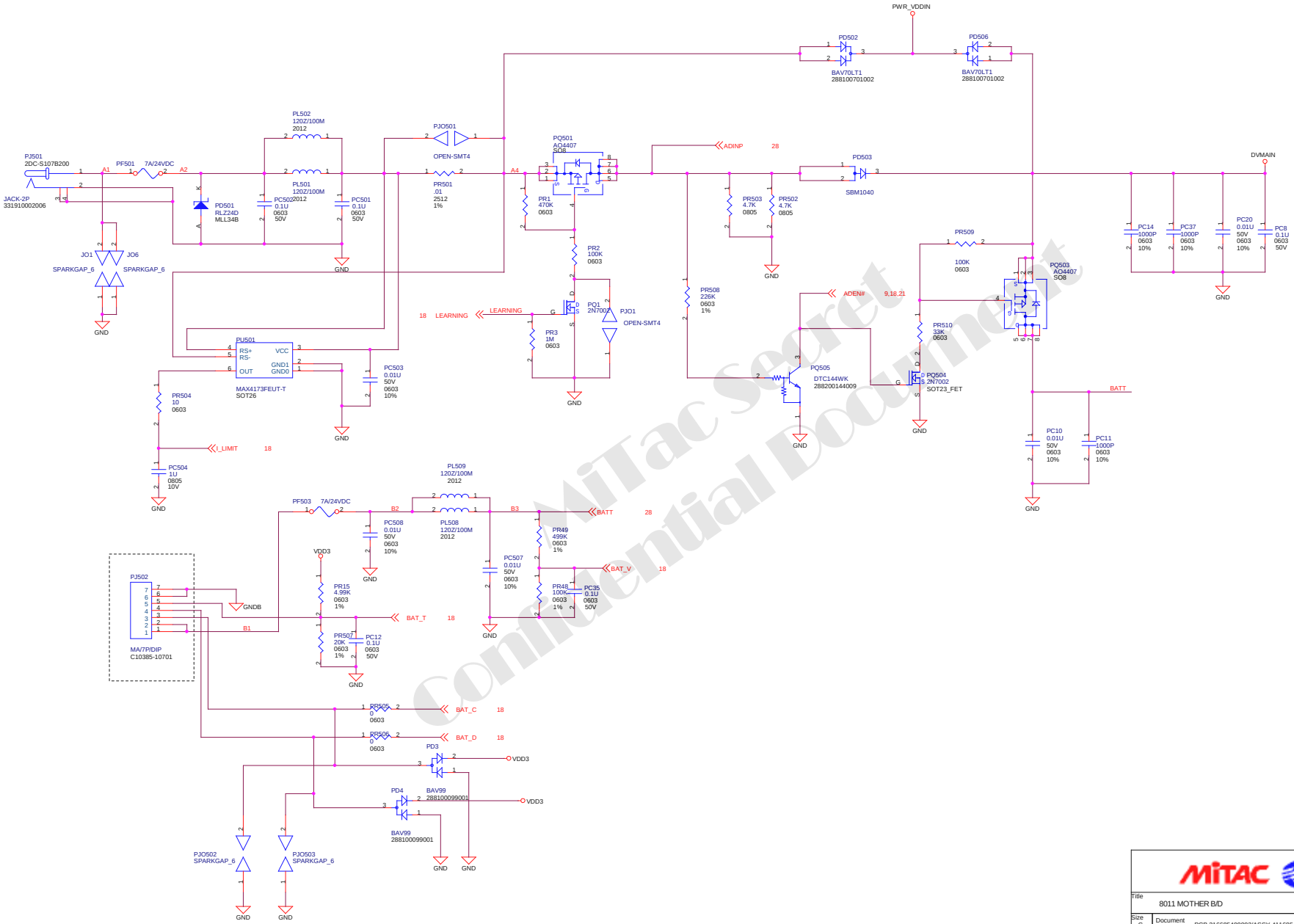
VMAIN/DISCHARGE



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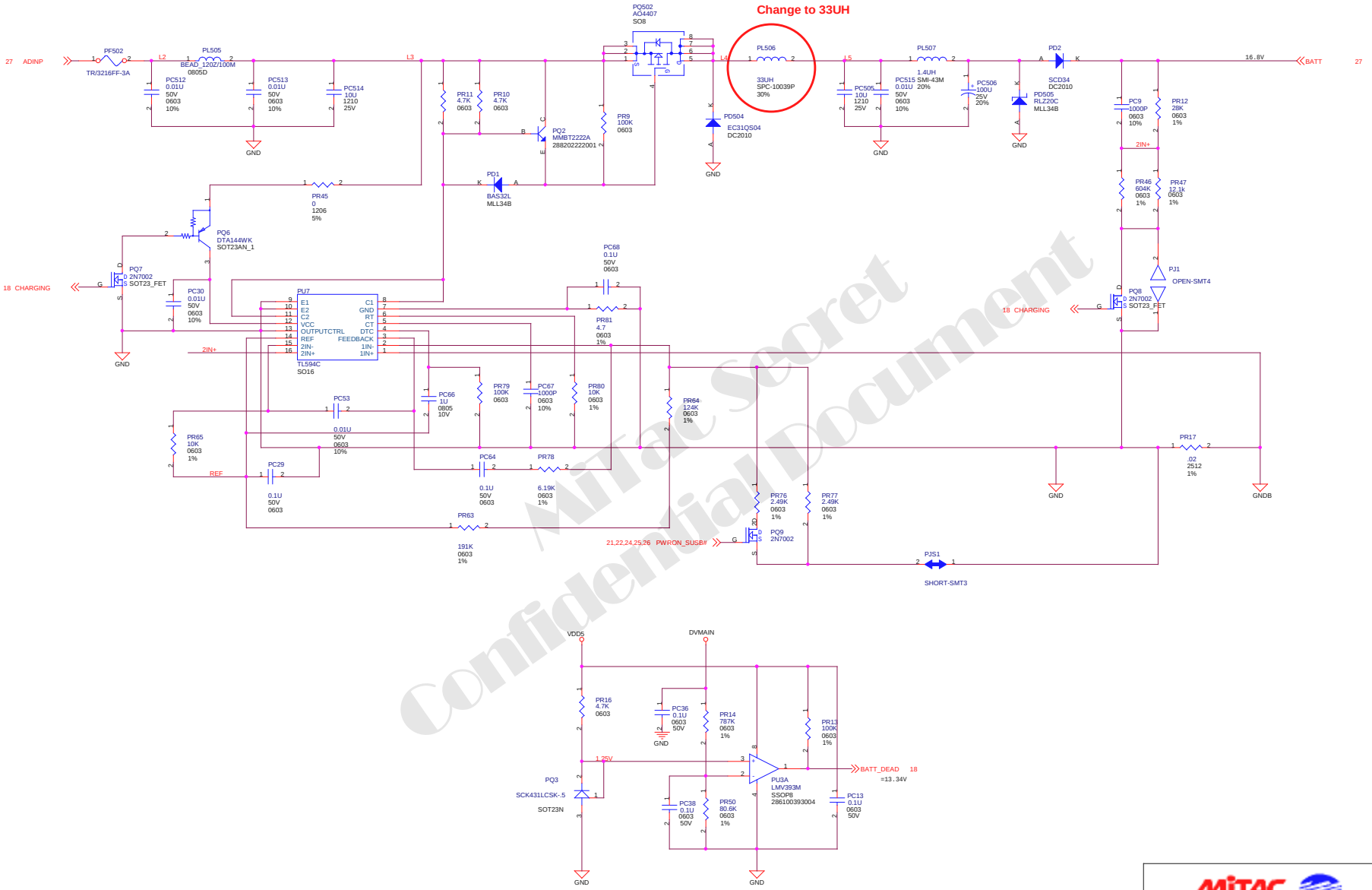
CHARGING



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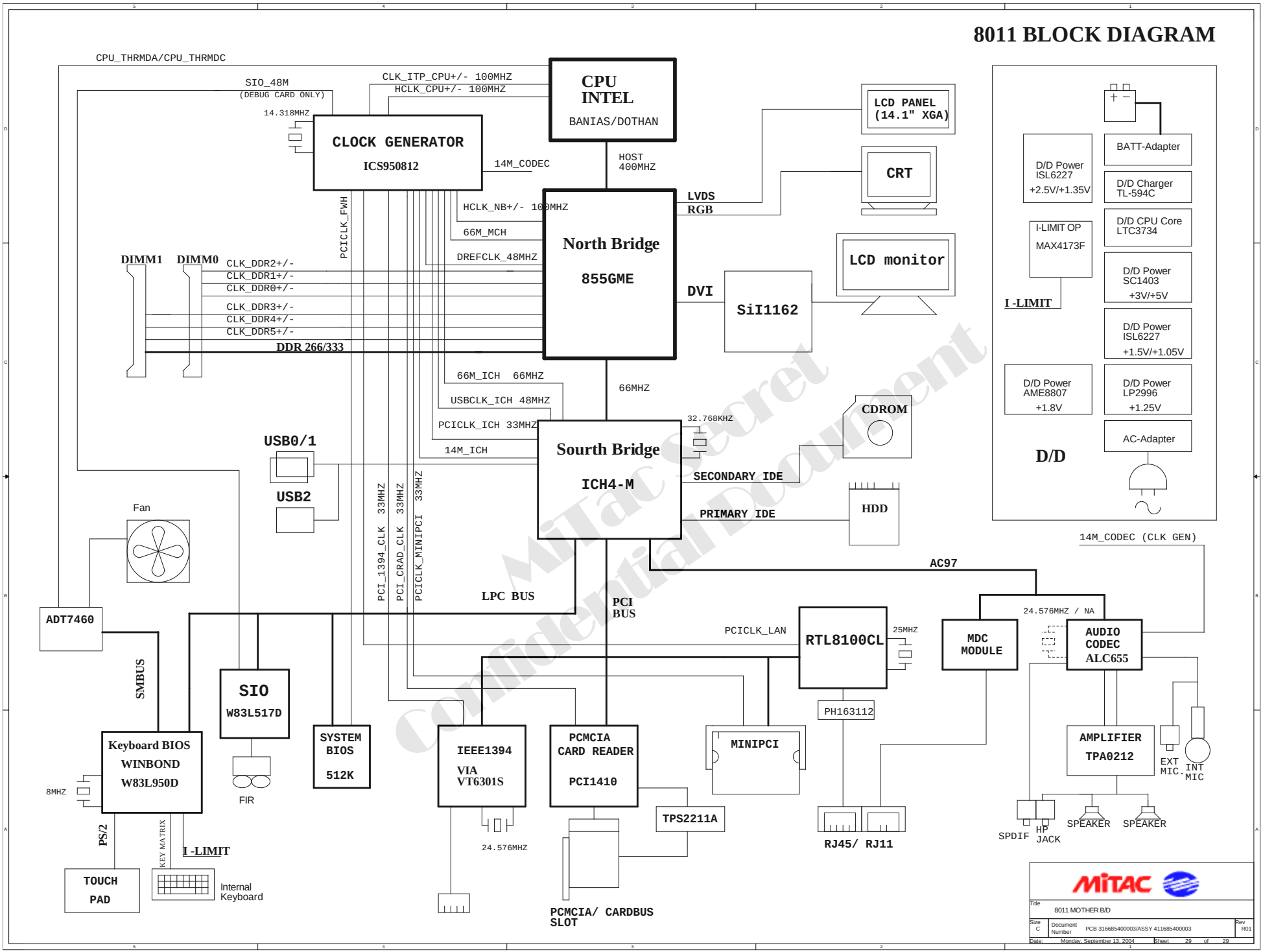


8011 Transmitter Board

光學定位點

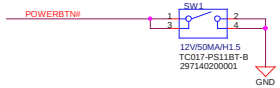
FD1 FIDUCIAL-MARK
FD2 FIDUCIAL-MARK
FD501 FIDUCIAL-MARK
FD502 FIDUCIAL-MARK

MTG1 ID3.0/OD9.0
MTG3 ID3.0/OD9.0
MTG4 ID3.0/OD9.0
GND

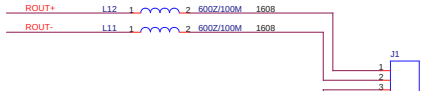
POWER LED

WHITE LIGHT

POWER BUTTON



Right Audio connector



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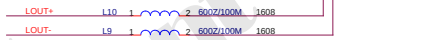
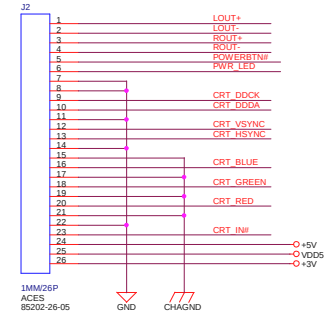
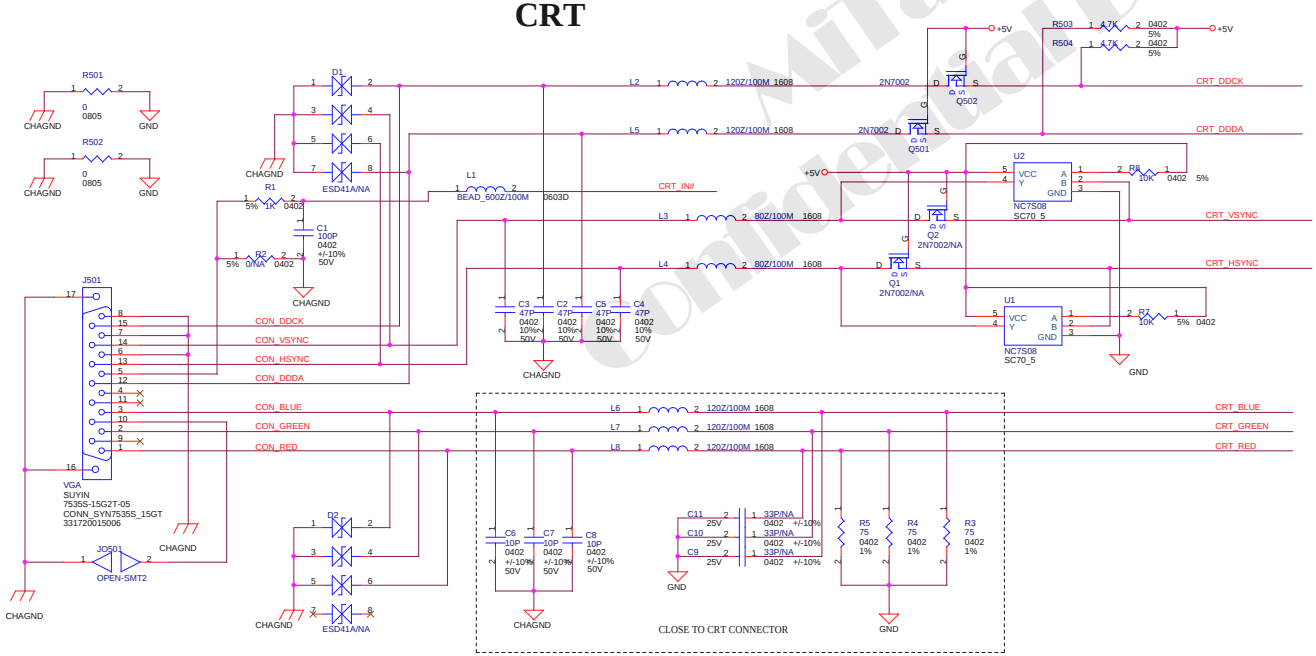




P/N 291000152610

CRT



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Title	8011 transmitter B/D	
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Reference Material

❖ Intel Banias Pentium M Processor	Intel.INC
❖ Intel 82855GM Memory Controller Hub (GMCH)	Intel.INC
❖ Intel 82201DBM I/O Controller Hub Mobile (ICH-4)	Intel.INC
❖ Clock Generator ICS950812	ICS.INC
❖ Keyboard BIOS WINBOND W83L950D	WIN.INC
❖ 8011 Hardware Engineering Specification	Technology.Corp./MiTAC

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