MS-7031

Version 10A
For Fujitsu-Siemens

Intel Northwood & Prescott mPGA478B Processor
ATi RS350 (IGP) + SB300 (IXP) Chipset

System Chipset:	**ATi RS350 - RADEON IGP (North Bridge)** **ATi SB300 - IXP300 (South Bridge)**
On Board Chipset:	**BIOS -- XBus EEPROM 4M** **AC'97 Codec -- ALC655** **LPC Super I/O -- Winbond 627 THF Ver:C** **LAN - Realtek RTL8100C** **1394 -- VIA6307**
Main Memory:	**DDR CLOCK BUFFER** **ICS ICS9P750 SSOP** **DDR * 4**
Expansion Slots:	**AGP4X/8X SLOT * 1** **PCI2.3 SLOT * 3**
Intersil PWM:	**Controller: HIP6556A** **Driver: HIP6602+HIP6601**
Regulators:	**MS-7**

MODEL Config.	ORCAD Config.	Function	Option	ERP Number
MS7031-10A	CFGMS7031-F1	LAN + 1394	FIL	601-7031-

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Title	COVER SHEET	
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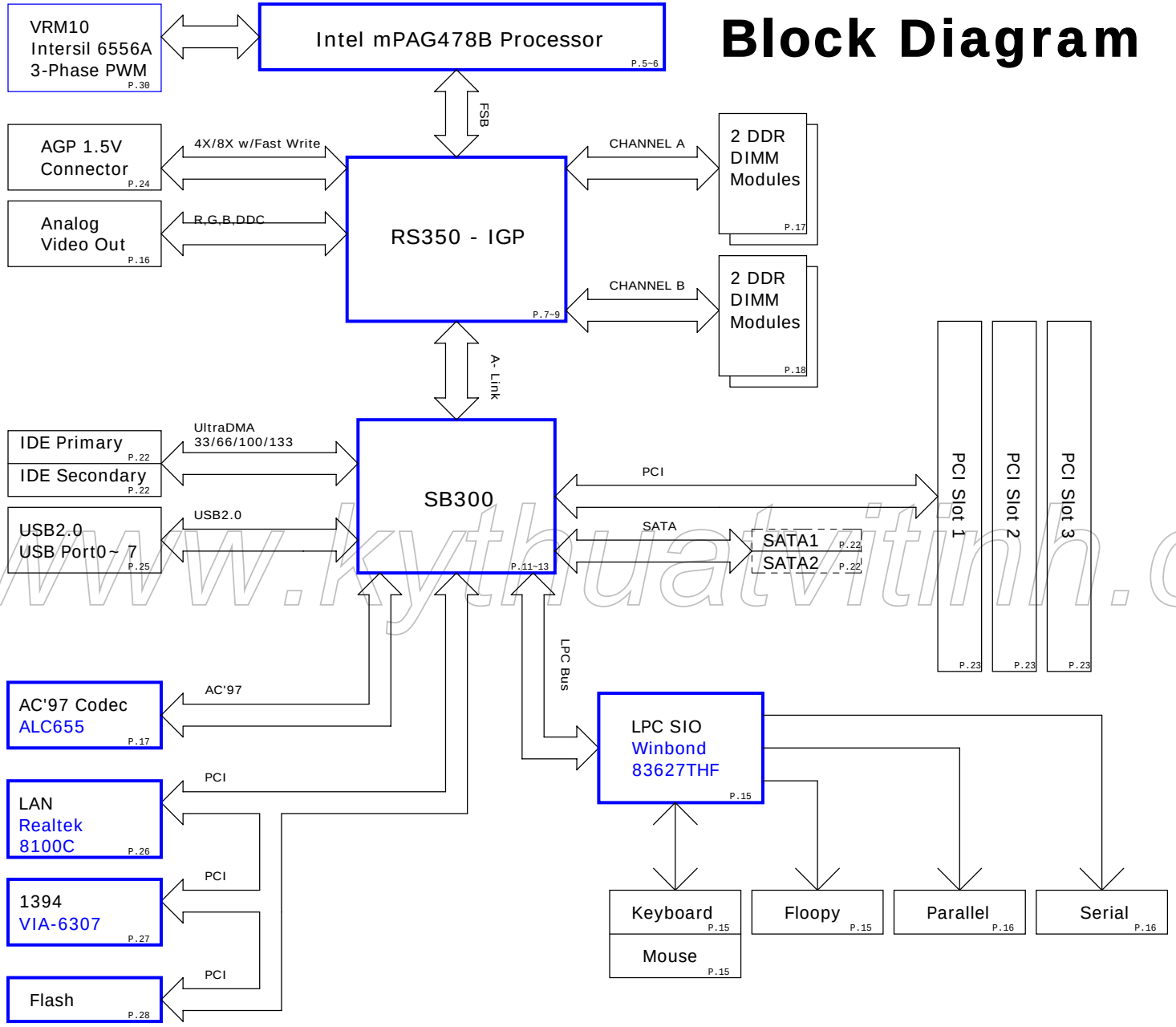
Block Diagram



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Title	BLOCK DIAGRAM	
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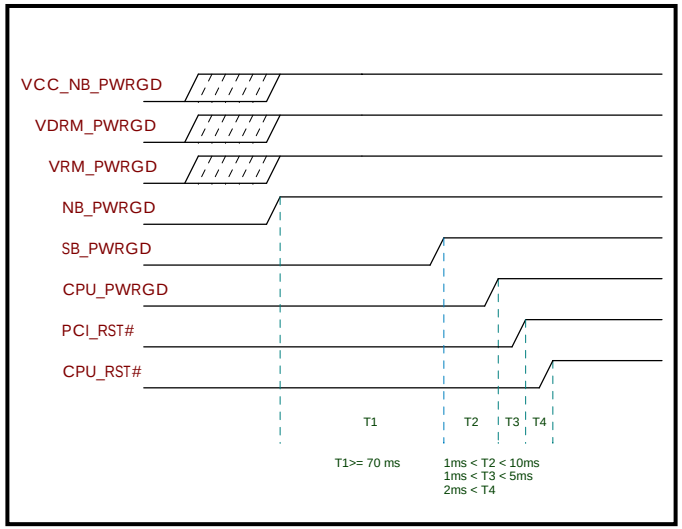
POWER SEQUENCE



I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR DIMM A0	A0	1 0 1 0 0 0 0 X
DDR DIMM B0	A4	1 0 1 0 0 1 0 X
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 X
DDR CLOCK BUFFER	D4	1 1 0 1 0 1 0 X

Revision History (Changes From V0C To V0D)	
Sheet	**Desciption**
	SMBus Layout Midify
	DC Power Midify
	PCIRST Layout Midify
	SMBus Layout Midify
	VRM Circuit Midify

Revision History (Changes From V0D To V100)	
Sheet	**Desciption**
	Thermal-trip Circuit Midify
	Throttling Circuit Midify
	VRM Circuit Midify

Revision History (Changes From V100 To V10A)	
Sheet	**Desciption**
	USB Connector with Flange in Black
	1394 Connector with Flange in White
	JCD1 to AUX_IN

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Title: REVISION HISTORY - 1

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POWER RAILS

	POWER	VOLTAGE	ACTIVE SCOPE	ROUTING
SYSTEM	+12V	+12V	OFF IN S3-S5	80 mils/20 mils
	-12V	-12V	OFF IN S3-S5	40 mils/20 mils
	VCC5	+5V	OFF IN S3-S5	PLANE
	VCC3	+3.3V	OFF IN S3-S5	PLANE
	VCC5_SB	+5V	S0-S5(ON)	80 mils/40 mils
	VCC3_SB	+3.3V	S0-S5(ON)	40 mils
	USB_STR1	+5V	S0-S3(ON)	80 mils
	USB_STR2	+5V	S0-S3(ON)	80 mils
	CLK_VDD	+3.3V	OFF IN S3-S5	PLANE/TRACE
Processor	VCCP	VID[0..5]	OFF IN S3-S5	PLANE
	VCC_VID	+1.2V	OFF IN S3-S5	20 mils
RS350 NB	1.VCCP	VCCP	OFF IN S3-S5	PLANE(I/O POWER FOR CPU)
	2.VCC_NB	+1.6V	OFF IN S3-S5	PLANE(CORE POWER)
	3.VCC_DDR	+2.5V	S0-S3(ON)	PLANE(I/O POWER FOR DDR)
	4.VCC_AGP	+1.5V	OFF IN S3-S5	PLANE(I/O POWER FOR AGP)
	5.VDDL	+3.3V	OFF IN S3-S5	PLANE(I/O POWER FOR A-LINK)
	6.VCC1.8_NB	+1.8V	OFF IN S3-S5	40 mils(CORE TRANSFORM)
	7.AVDD	+2.5V	OFF IN S3-S5	20 mils(I/O POWER FOR DAC)
	8.AVDDI	+1.8V	OFF IN S3-S5	20 mils(DIGITAL POWER FOR DAC)
	9.AVDDQ	+1.8V	OFF IN S3-S5	20 mils(POWER FOR DAC BAND GAP REFERANCE)
	10.PLLVDD	+1.8V	OFF IN S3-S5	20 mils(PLL POWER)
	11.CPVDD	+1.8V	OFF IN S3-S5	20 mils(CPU PLL POWER)
	12.MPVDD	+1.8V	OFF IN S3-S5	20 mils(MEMORY PLL POWER)
	13.VTT_DDR	+1.25V	OFF IN S3-S5	60/60 mils(DDR TERMINATION POWER)
SB300 SB	1.VDDQ	+3.3V	OFF IN S3-S5	PLANE(3.3V I/O POWER)
	2.VCC_18	+1.8V	OFF IN S3-S5	PLANE(CORE_POWER)
	3.VCC3_SB	+3.3V	S0-S5(ON)	20 mils
	4.VCC18_SUS	+1.8V	S0-S5(ON)	20 mils
	5.APIC_POWER	VCCP	OFF IN S3-S5	10 mils(CPU I/O)
	6.AVDD_CK	+1.8V	OFF IN S3-S5	10 mils(PLL POWER)
	7.5V_REF	+5V	OFF IN S3-S5	10 mils(PCI CLAMP VOLTAGE)
	8.3.3V_AVDDC	+3.3V	S0-S5(ON)	10 mils(USB PLL POWER)
	9.USB_AVDD	+3.3V	S0-S5(ON)	20 mils(USB PHY POWER)
	10.AVDD_SATA	+1.8V	OFF IN S3-S5	20 mils(SERIAL PHY POWER)
	11.PLVDD_SATA	+1.8V	OFF IN S3-S5	10 mils(SERIAL ATA PLL POWER)
	12.XTLVDD_SATA	+3.3V	OFF IN S3-S5	10 mils(SERIAL ATA XTAL POWER)

	POWER	VOLTAGE	ACTIVE SCOPE	ROUTING
IEEE-1394	P3VA	+3.3V	OFF IN S3-S5	20mils
	P3VD	+3.3V	OFF IN S3-S5	20mils
	BUS_PWR	+12V	OFF IN S3-S5	40/40mils
10/100 LAN	VDD33	+3.3V	S0-S5(ON)	PLANE/TRACE
	VDD25	+2.5V	S0-S5(ON)	PLANE/TRACE
AC97	+5VR	+5V	OFF IN S3-S5	20mils
	DVDD	+3.3V	OFF IN S3-S5	10mils

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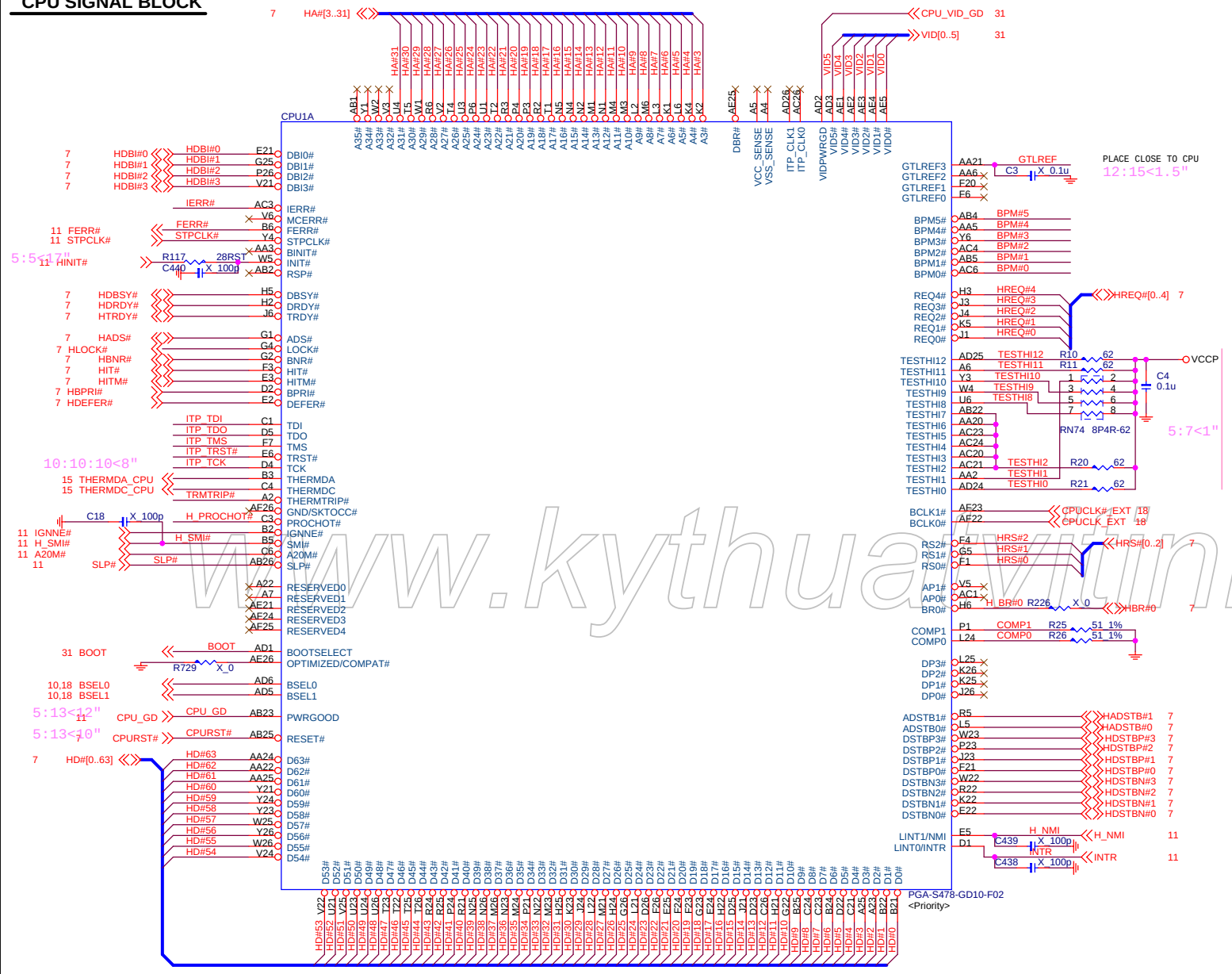
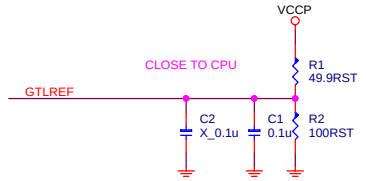
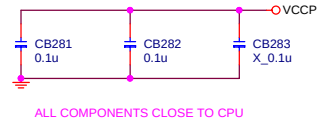
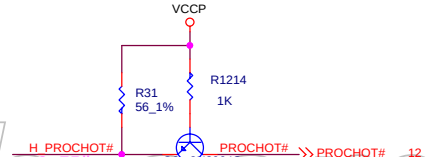
CPU SIGNAL BLOCK

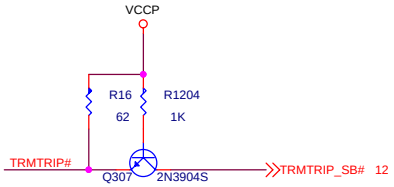


CPU GTL REFERNCE VOLTAGE BLOCK



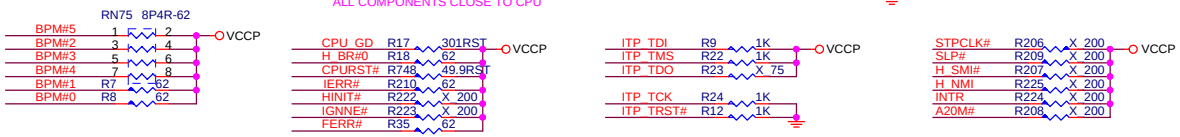






CPU STRAPPING RESISTORS

ALL COMPONENTS CLOSE TO CPU



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Title	Intel mPGA478B - Signals	
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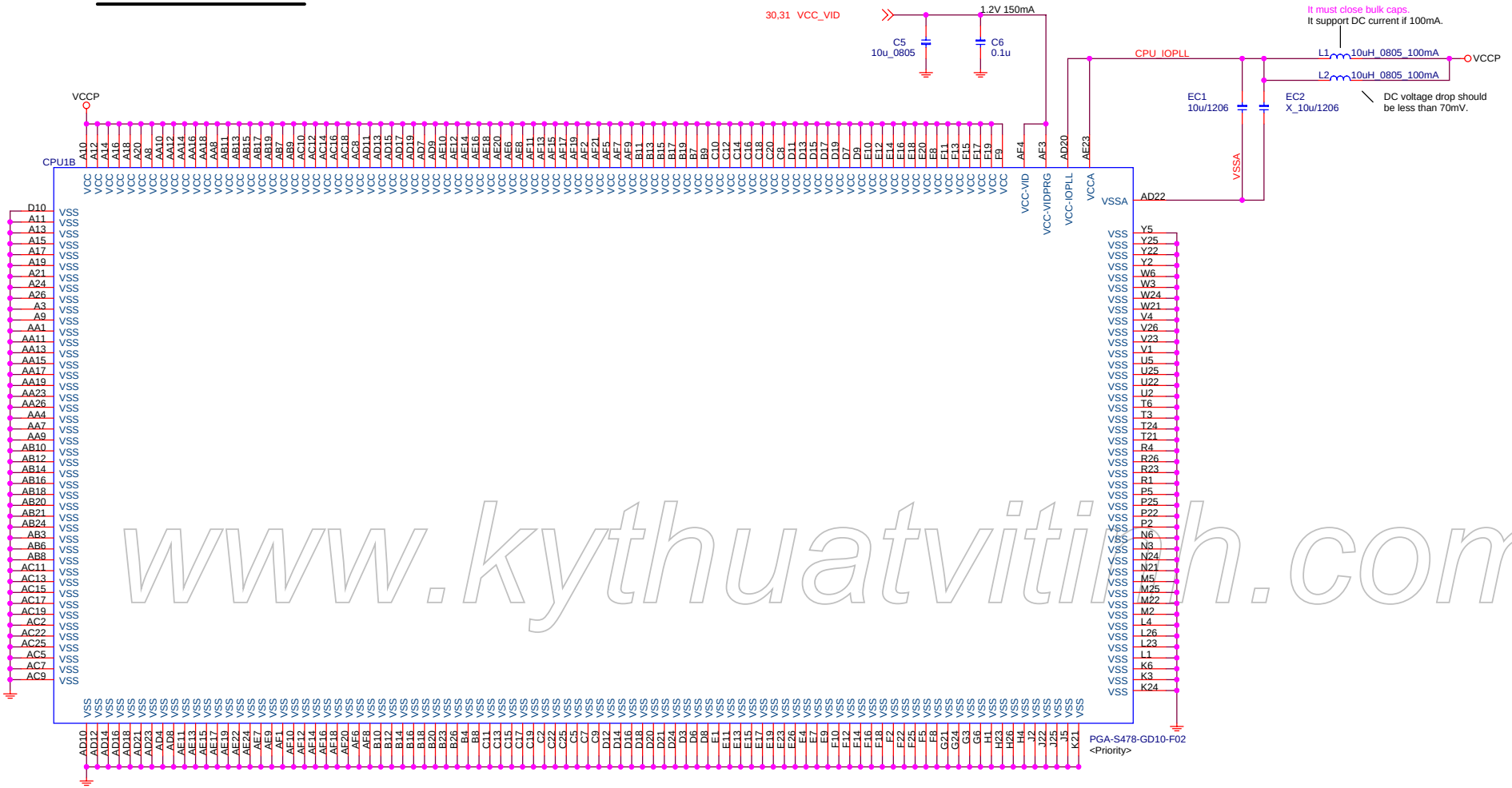
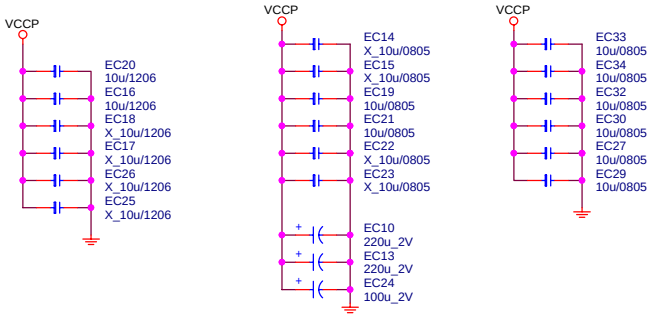
CPU VOLTAGE BLOCK



CPU DECOUPLING CAPACITORS



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Title	Intel mPGA478B - Power	
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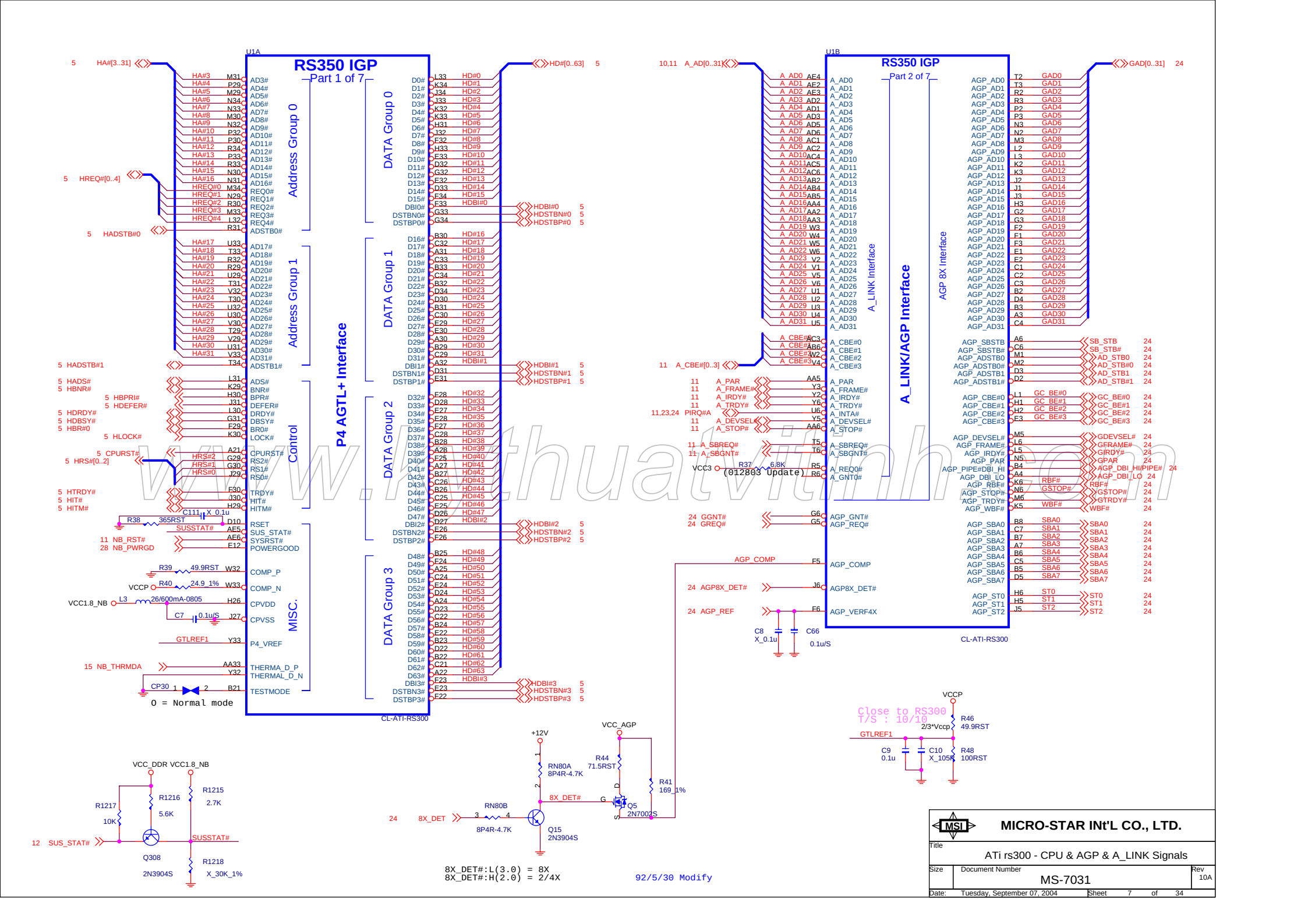

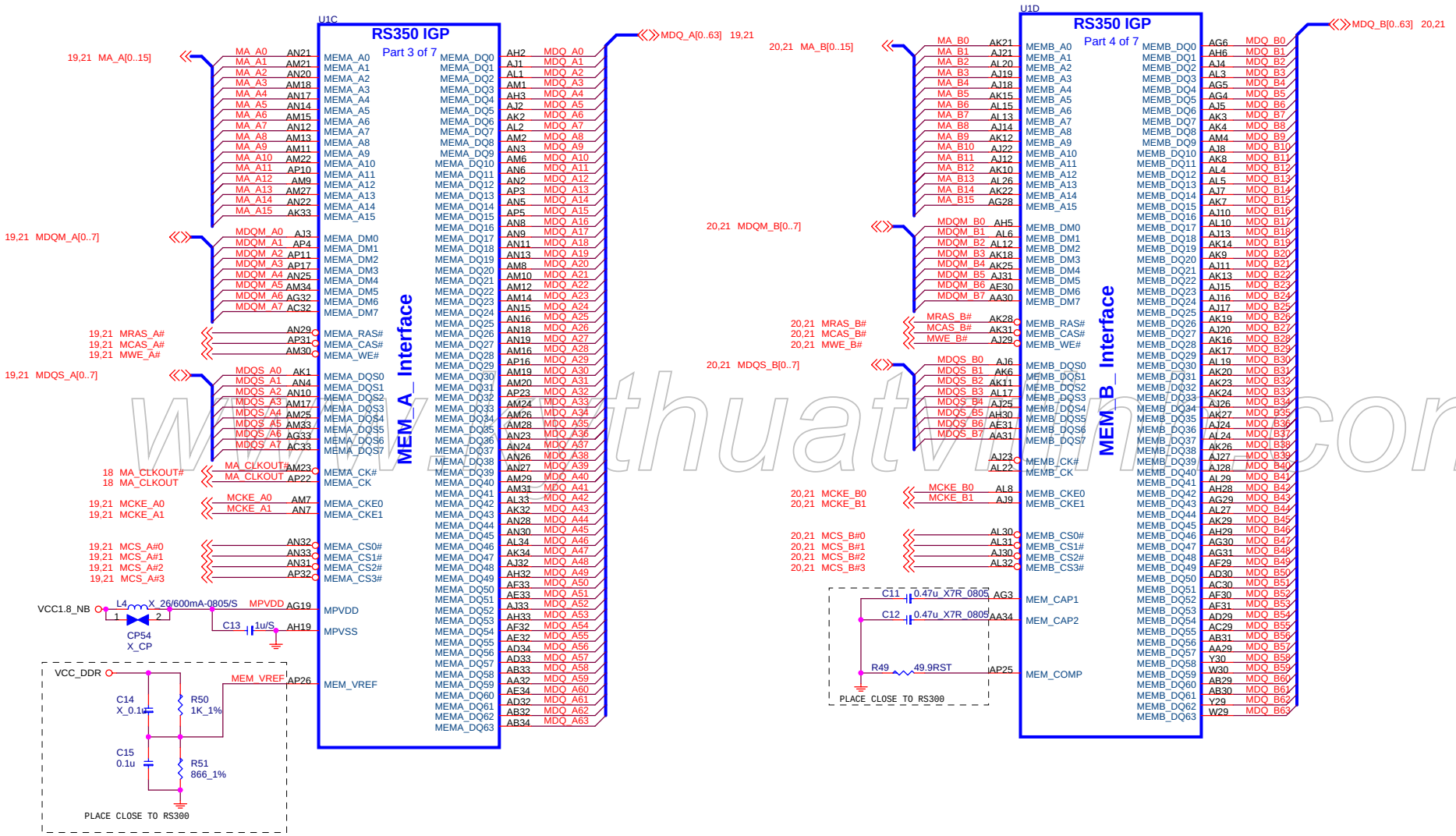

CL-ATI-RS300

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Title: ATi IGP - Memory Signals		
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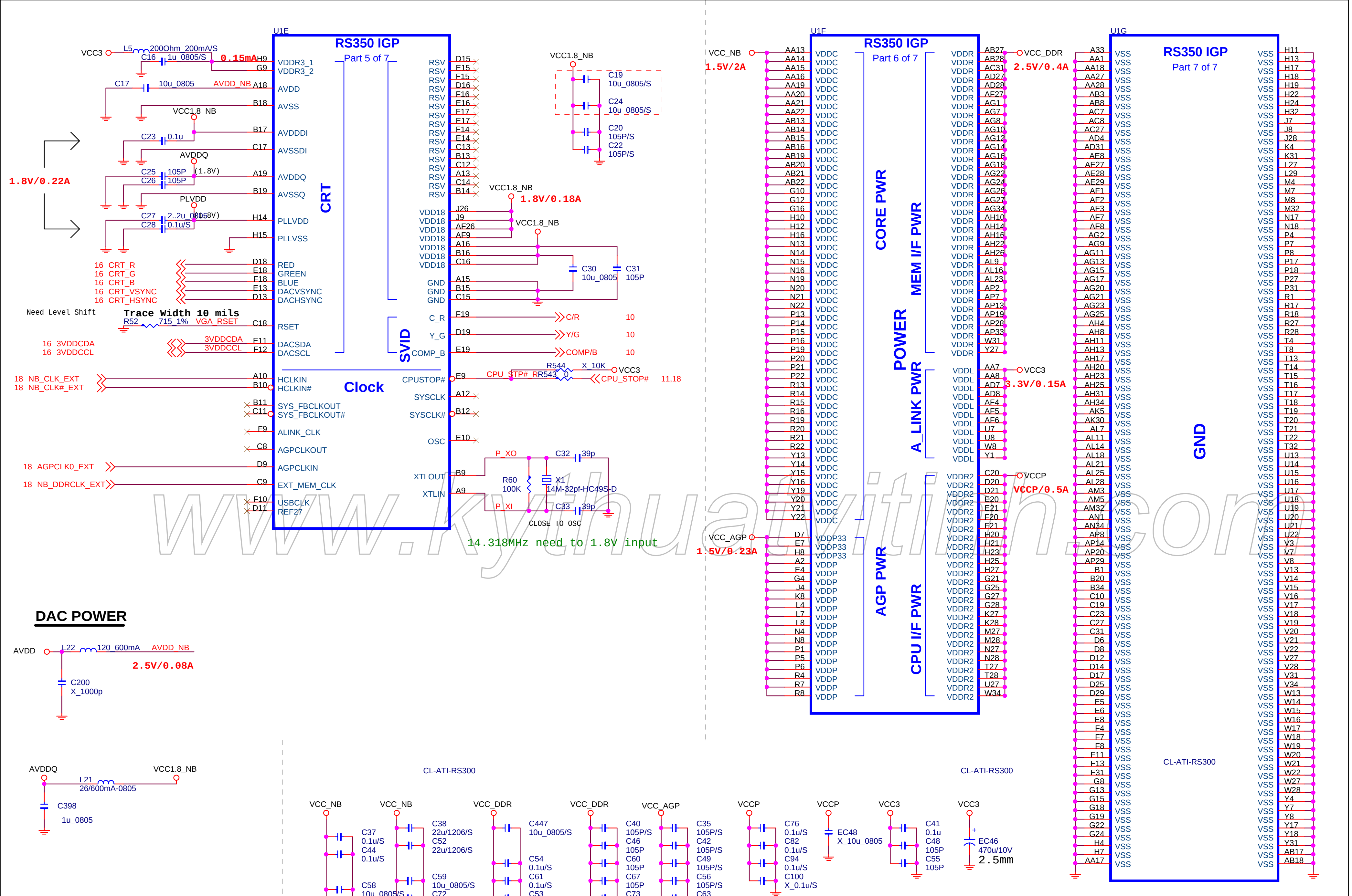

MICRO-STAR INt'L CO., LTD.

Title	ATi IGP - Video & Clock & Power Signals	
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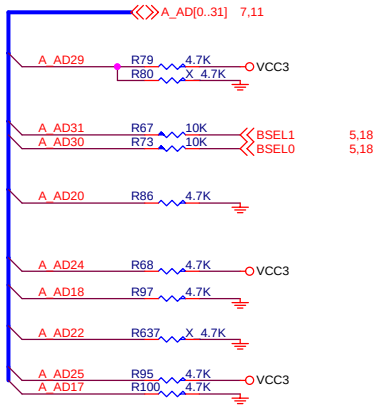
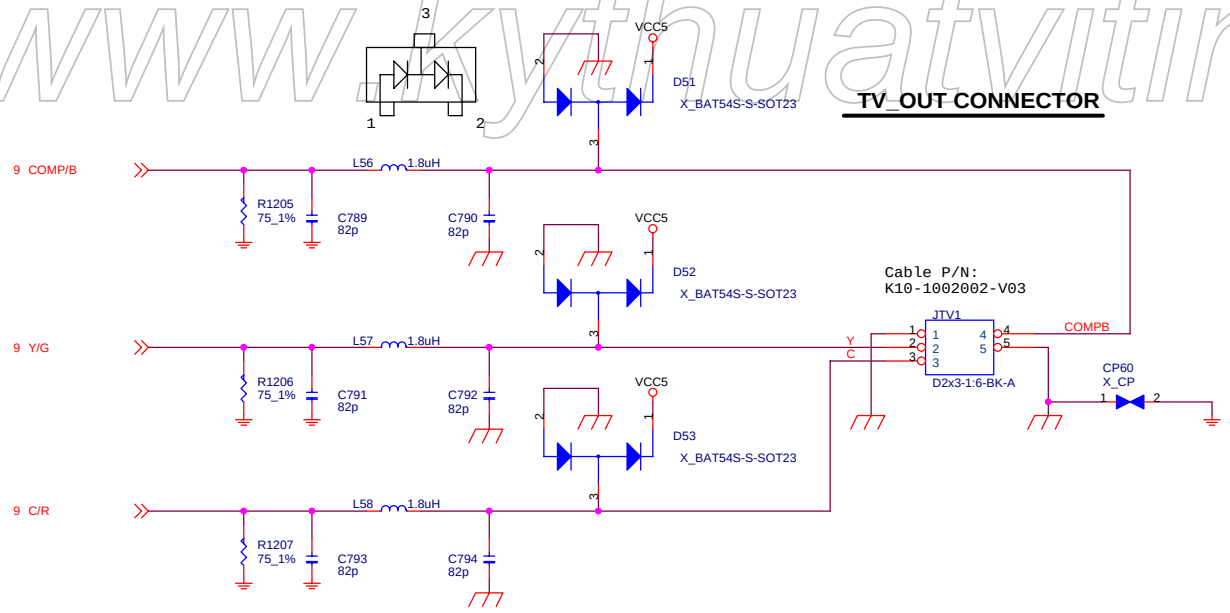



```
* AD29 : STRAP CONFIGURATION
0 : REDUCEDE SET (DEFAULT)
1 : FULL SET

* AD[31:30] : FSB CLK SPEED
00 : 100 MHZ
01 : 133 MHZ     (DEFAULT)
10 : 200 MHZ
11 : 166 MHZ

AD20 : INTERNAL CLK GEN. ENABLE
0 : EXTERNAL CLK GEN.
1 : INTERNAL CLK GEN. (DEFAULT)

* AD24 : NORTHWOOD CPU

* AD18 : Disabled PHASE CALIBRATION

* A_AD22
  0: OSC deives OSC clock to SB(14.318MHz)
  1: OSC Drives Alink Clock to SB(66MHz)

* AD[25:17] : CPU = 1.45V
```


TV_OUT CONNECTOR



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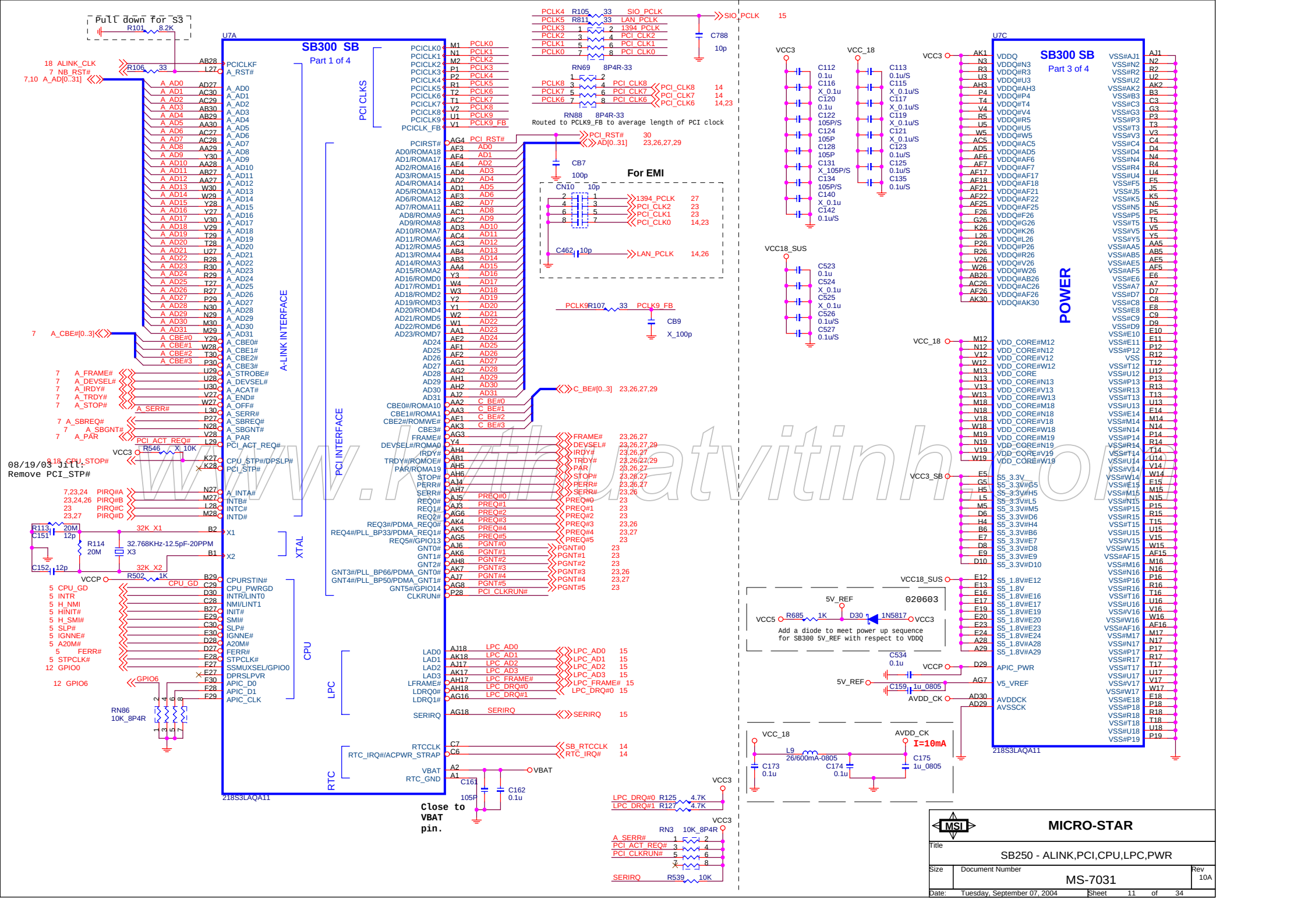
SB300 SB
Part 1 of 4
SB300 SB
Part 3 of 4
POWER
218S3LAQA11
218S3LAQA11
A-LINK INTERFACE
PCI INTERFACE
PCI CLKS
CPU
LPC
XTAL
RTC
For EMI
Pull down for S3
08/19/03 Jill:
Remove PCI_STP#
Close to VBAT pin.
I=10mA
Add a diode to meet power up sequence for SB300 5V_REF with respect to VDDQ
MICRO-STAR
SB250 - ALINK,PCI,CPU,LPC,PWR
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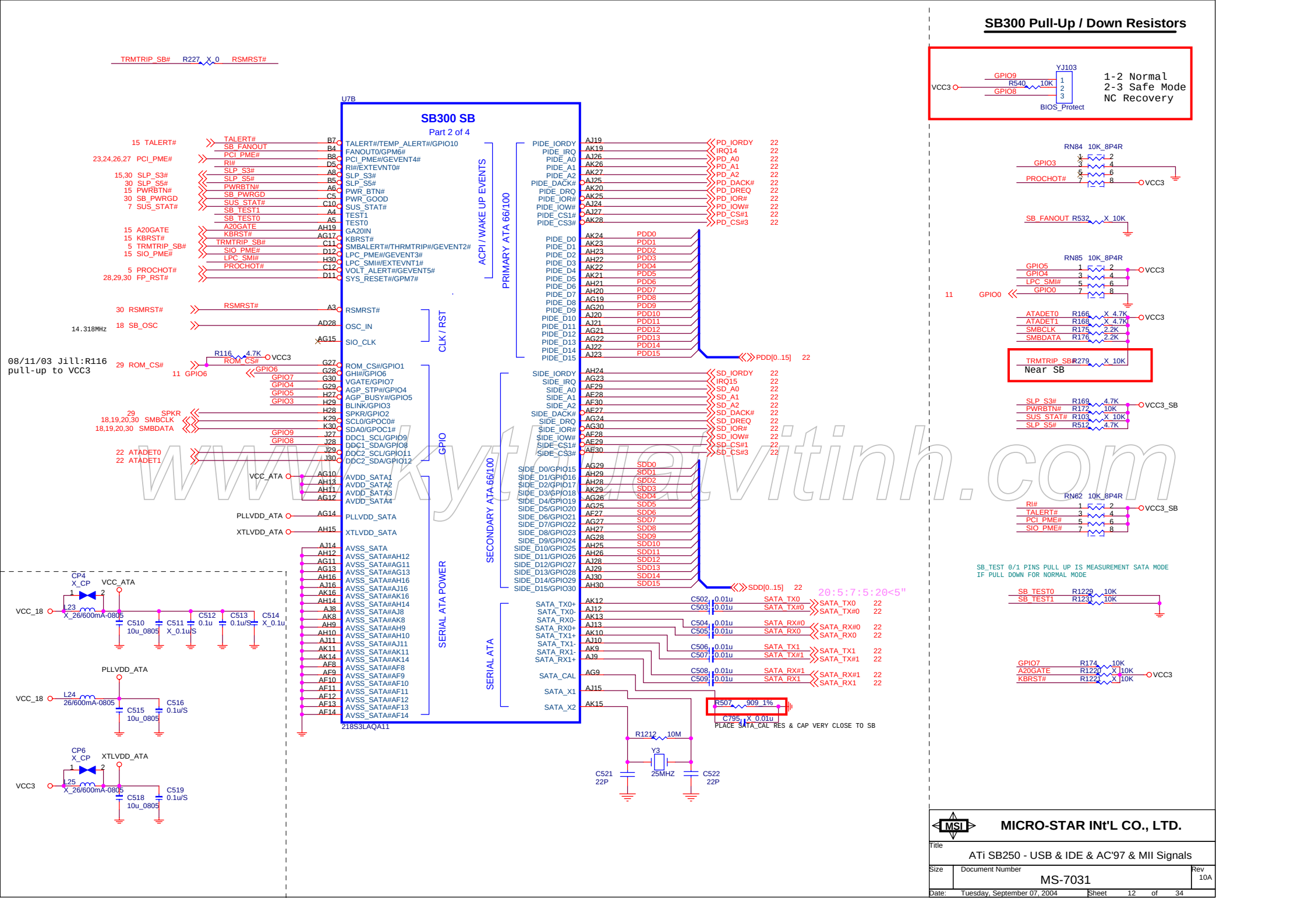
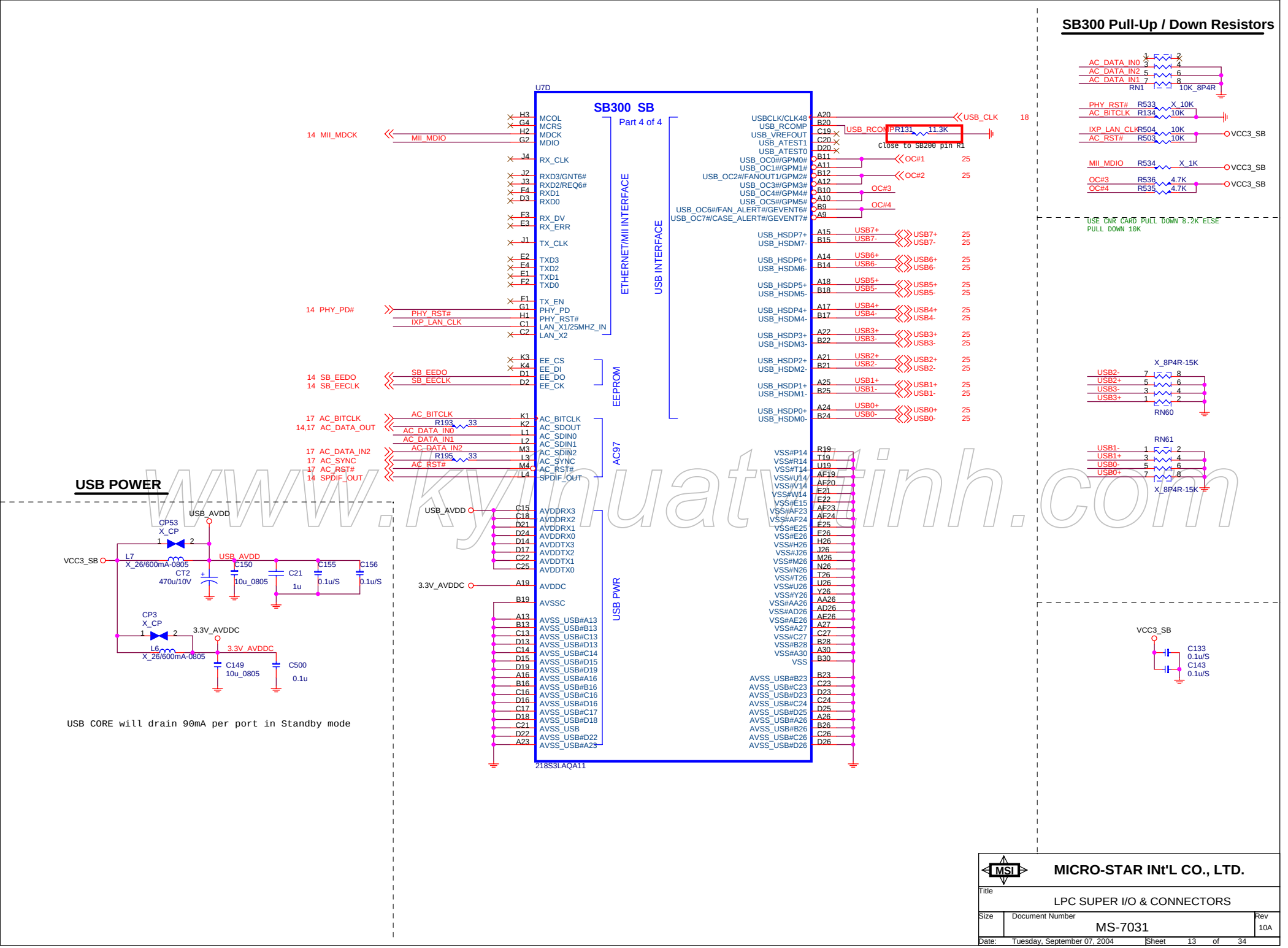
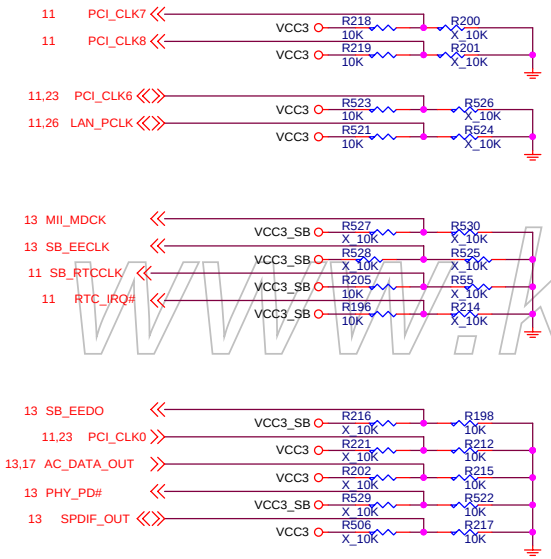




REQUIRED SYSTEM STRAPS

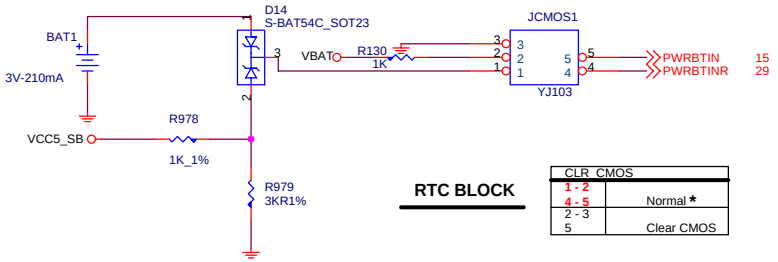
(LAN_PCLK = PCI_CLK5)

	ACPOWER	EEDO	PCI_CLK7 PCI_CLK8	PCI_CLK0	AC_SOUT	SPDIF_OUT	PCI_CLK6 PCI_CLK5	PHY_PD#	MDCK	EECK
STRAP HIGH	MANUAL PWR ON (DEFAULT)	USE hardcoded DEBUG STRAPS	ROM TYPE 11 =PCI ROM (DEFAULT) 10 =PMC LPC ROM 01 =NORMAL LPC ROM 00 =FWH ROM	INIT ACTIVE HIGH	USE 33MHZ NB BUS.	SIO 24MHz	PCI FB_CLK DELAY 11 =0ps DELAY(DEFAULT) 10 =300ps DELAY 01 =600ps DELAY 00 =900ps DELAY	PHY_PD ACTIVE HIGH	ETHERNET EEPROM=4K IXP200 ONLY (DEFAULT)	ETHERNET USE 25MHZ XTAL (DEFAULT)
STRAP LOW	AUTO PWR ON	IGNORE DEBUG ATRAPS (DEFAULT)		INIT# ACTIVE LOW (DEFAULT)	USE 66MHZ NB BUS. (DEFAULT)	SIO 48MHz (DEFAULT)		PHY_PD# ACTIVE LOW (DEFAULT)	ETHERNET EEPROM=16K IXP200, IXP250	ETHERNET USE 25MHZ OSC



DEBUG STRAPS

	PDACK#	AD31	AD30	AD29	AD28	AD27	AD26	AD25
STRAP HIGH	USE SHORT RESET	PULL CHANGE PUMP CTRL BIT1 HI	PULL CHANGE PUMP CTRL BIT0 HI (DEFAULT)	PULL VCO CTRL BIT1 HI	PULL VCO CTRL BIT0 HI (DEFAULT)	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL
STRAP LOW	USE LONG RESET (DEFAULT)	PULL CHANGE PUMP CTRL BIT1 LOW (DEFAULT)	PULL CHANGE PUMP CTRL BIT0 LOW	PULL VCO CTRL BIT1 LOW (DEFAULT)	PULL VCO CTRL BIT0 LOW	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)



RTC BLOCK

CLR_CMOS	
1 - 2 4 - 5	Normal *
2 - 3 5	Clear CMOS

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Title: ATi SB250 - STRAPS Signals

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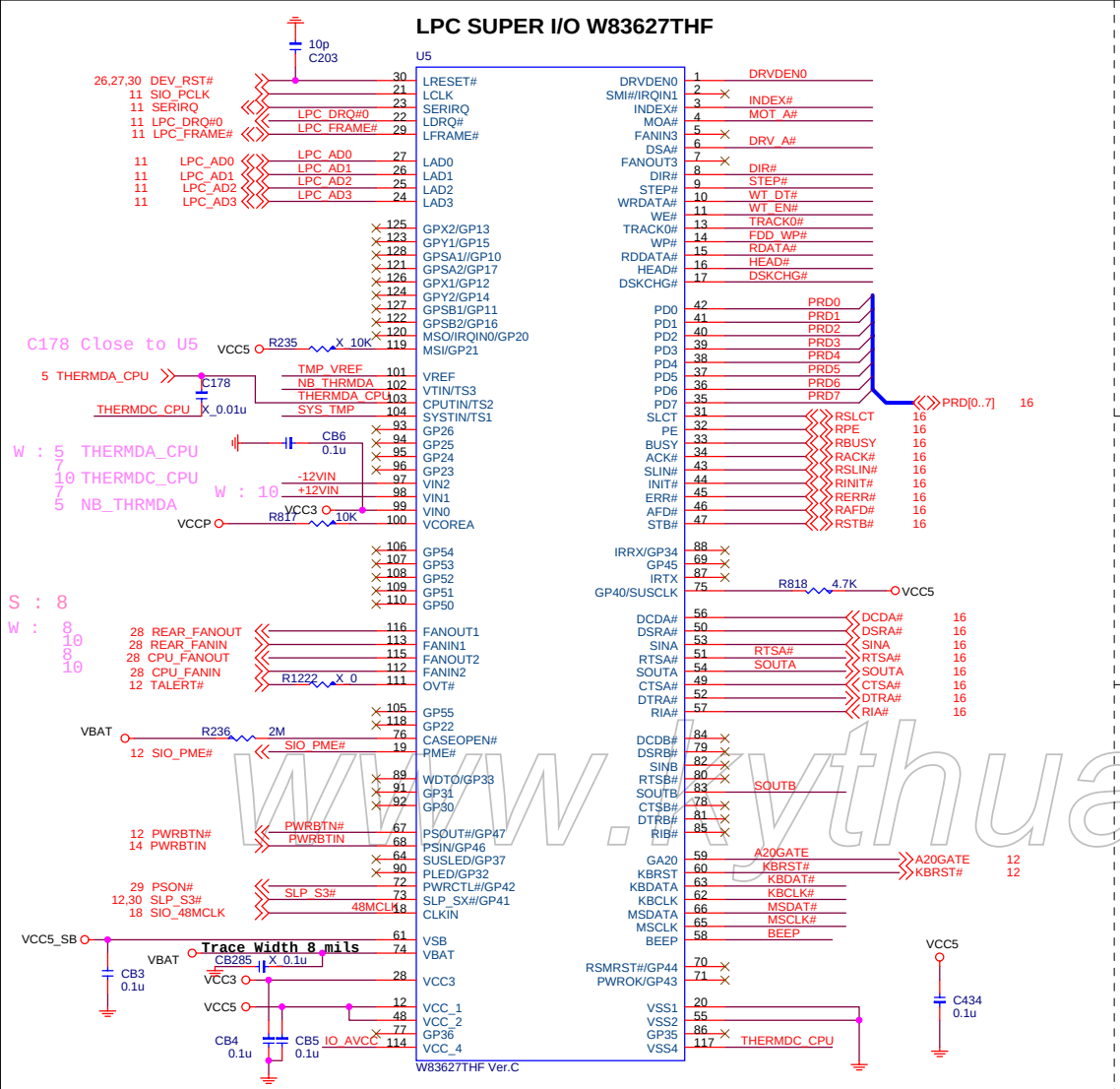

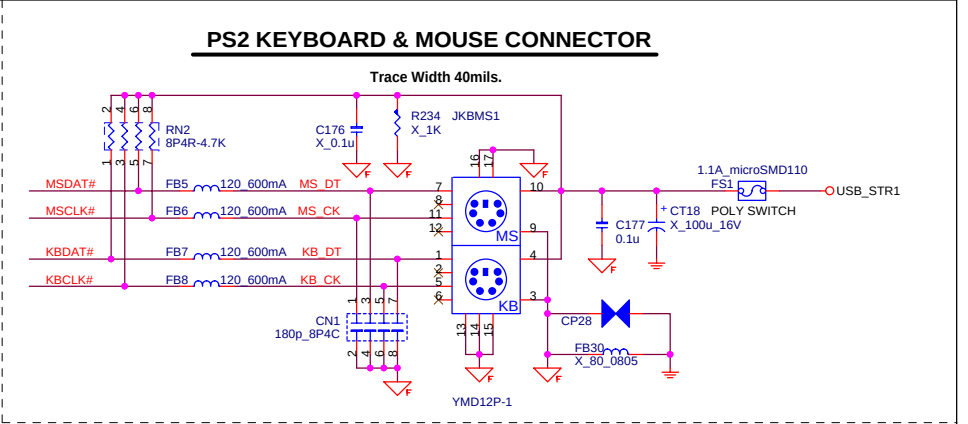

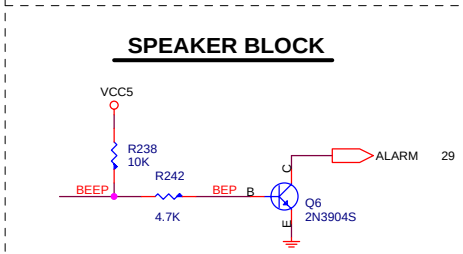

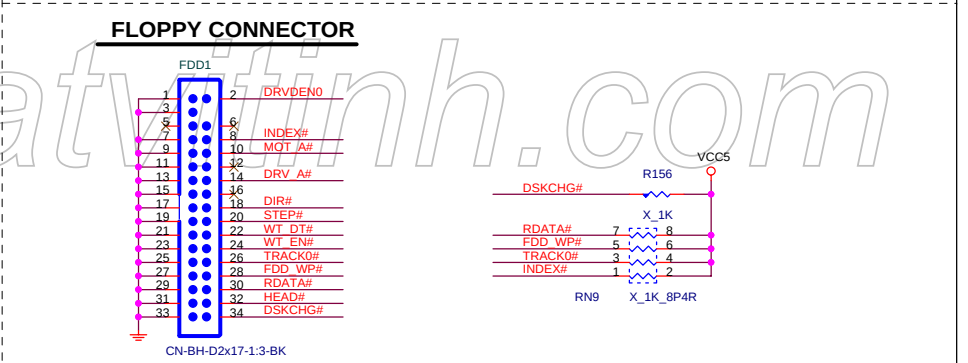

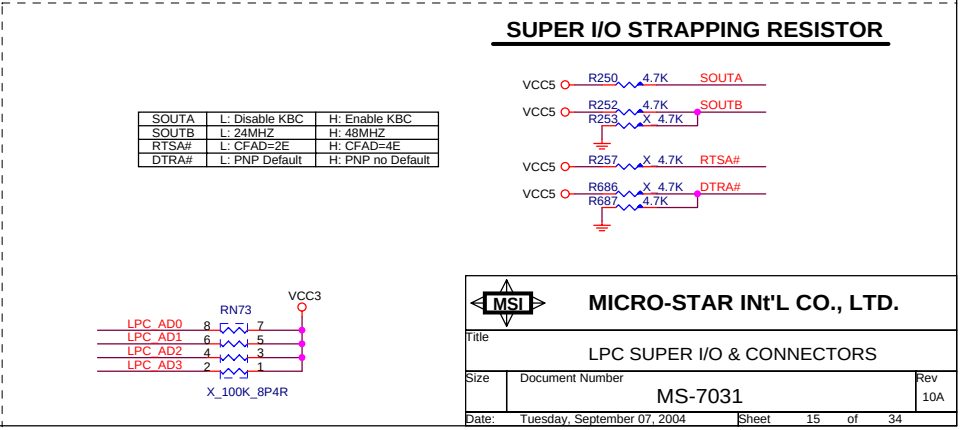

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Title: LPC SUPER I/O & CONNECTORS

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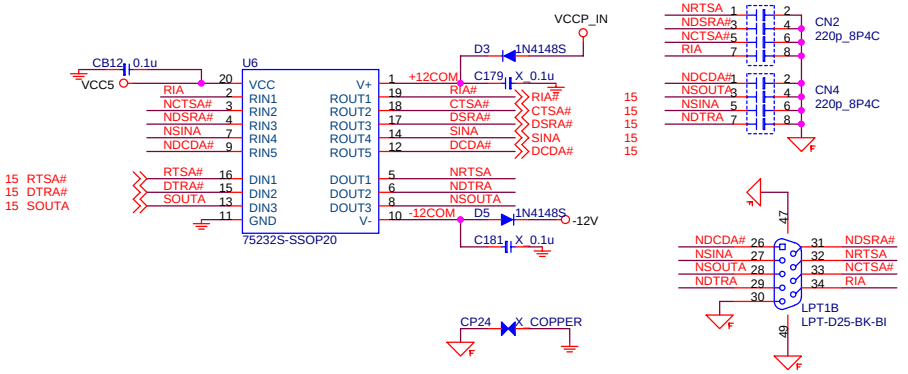
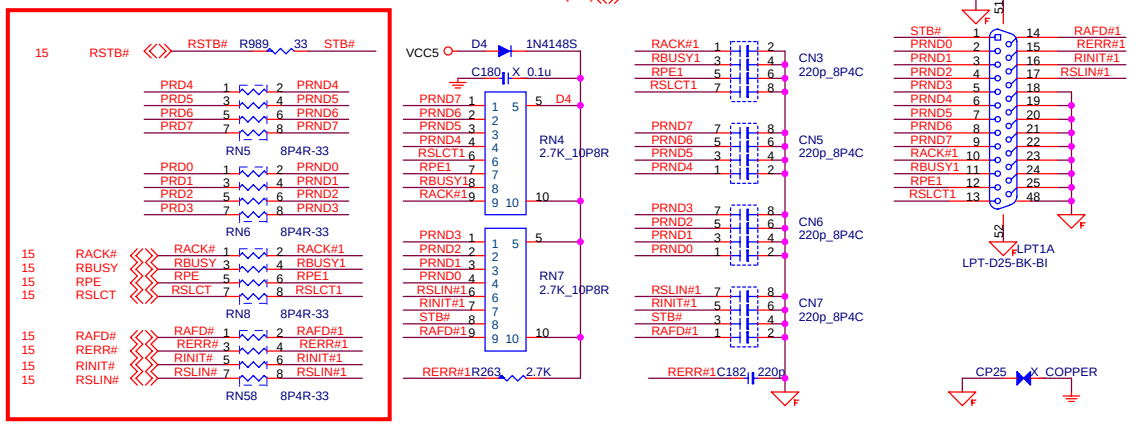
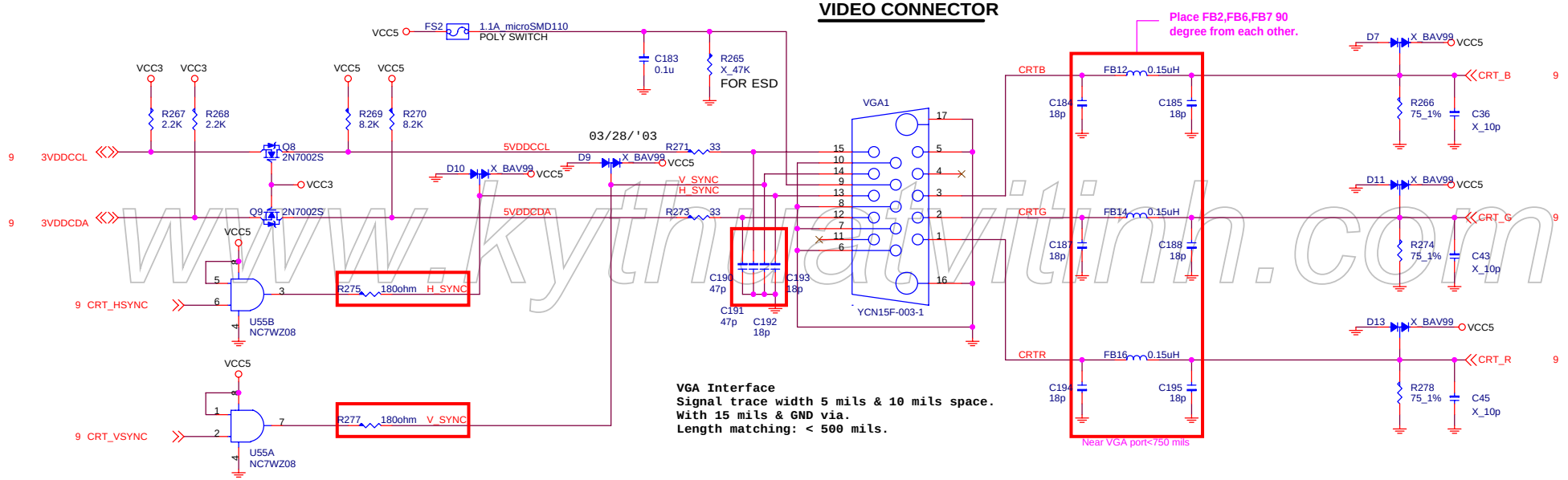
SERIAL PORT 1



PARALLAL PORT



VIDEO CONNECTOR



VGA Interface
Signal trace width 5 mils & 10 mils space.
With 15 mils & GND via.
Length matching: < 500 mils.

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Title	LPT, COM PORT, FDD & VGA , TV CONNECTORSs	
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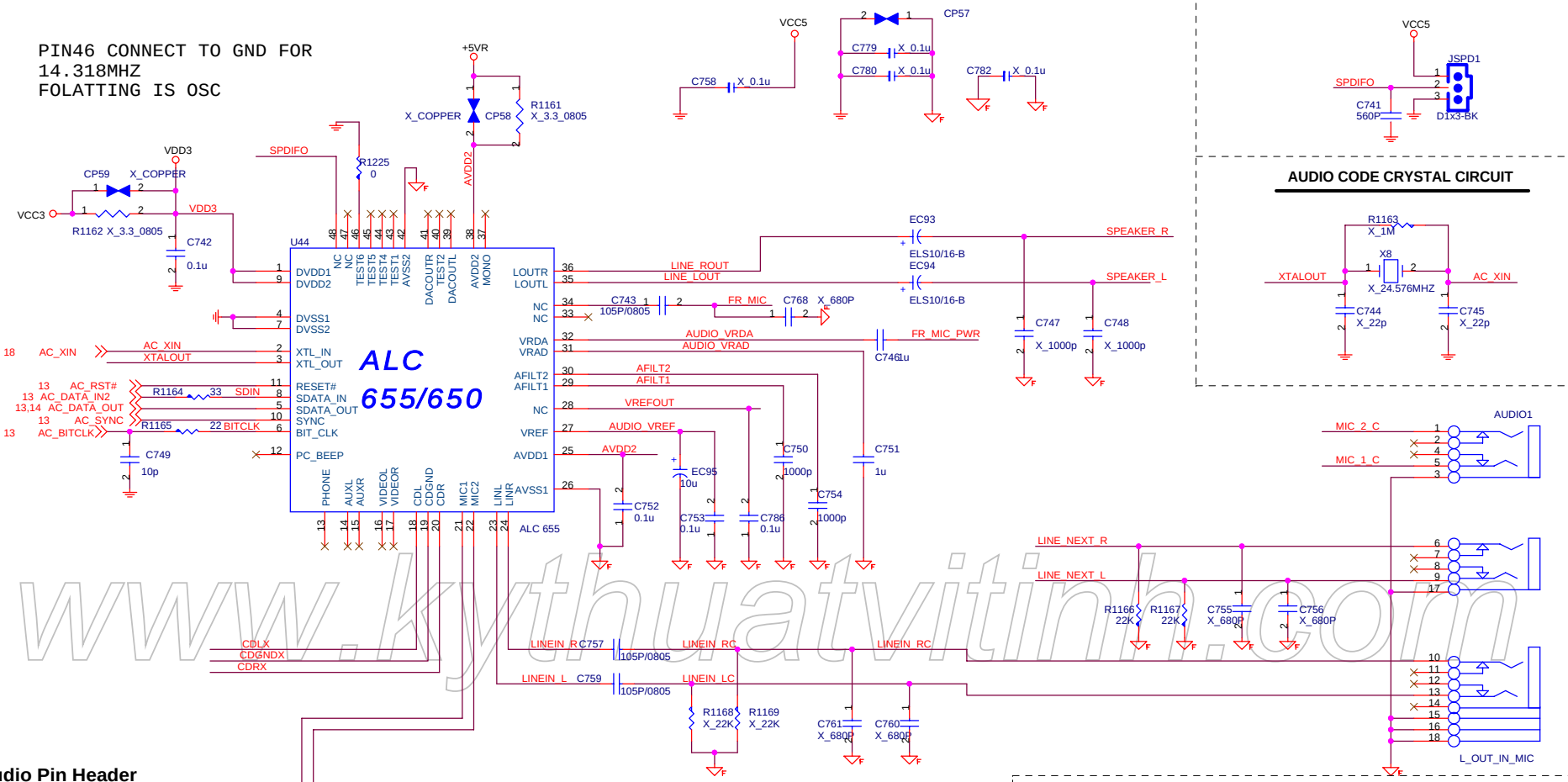
ALC650/655 AC97 CODEC

PIN46 CONNECT TO GND FOR
14.318MHZ
FOLATTING IS OSC

FOR EMI

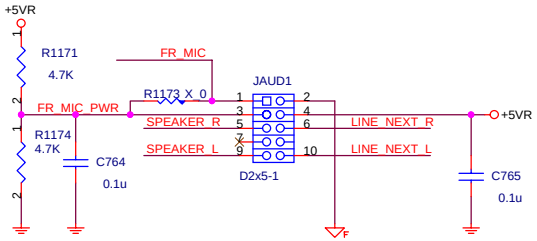


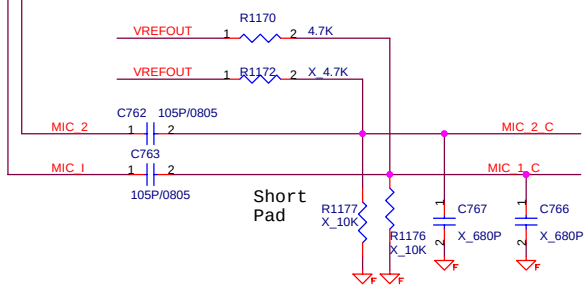
SPDIF CONNECTOR

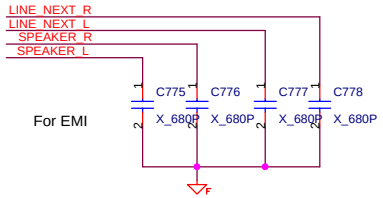
For ALC 650/655

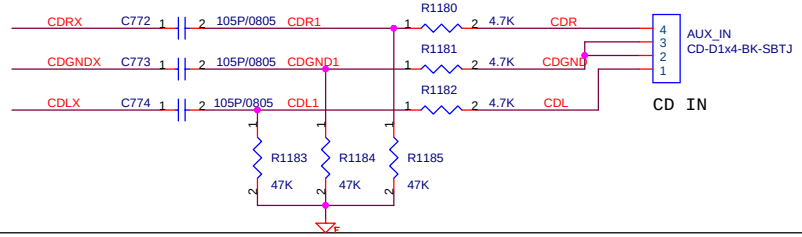
AUDIO CODE CRYSTAL CIRCUIT

Front Audio Pin Header

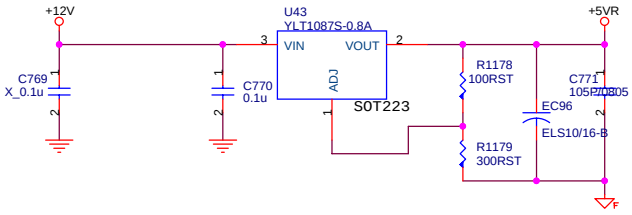








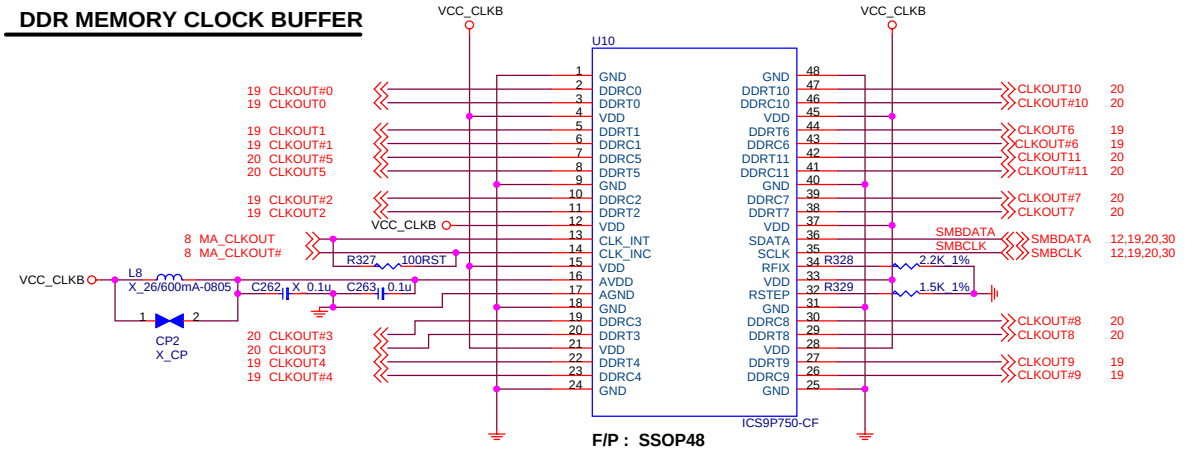
AUDIO CODE REGULATORS



Micro Star Restricted Secret

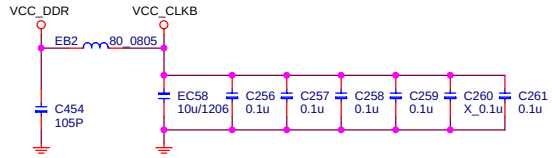
Title	AC' 97 CODEC & AUDIO Connectors	Rev 10A
Document Number	MS-7031	
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, September 07, 2004	
	Sheet 17 of 34	

DDR MEMORY CLOCK BUFFER



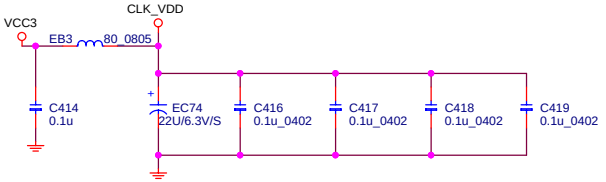
F/P : SSOP48

CLOCK BUFFER DECOUPLING CAP.

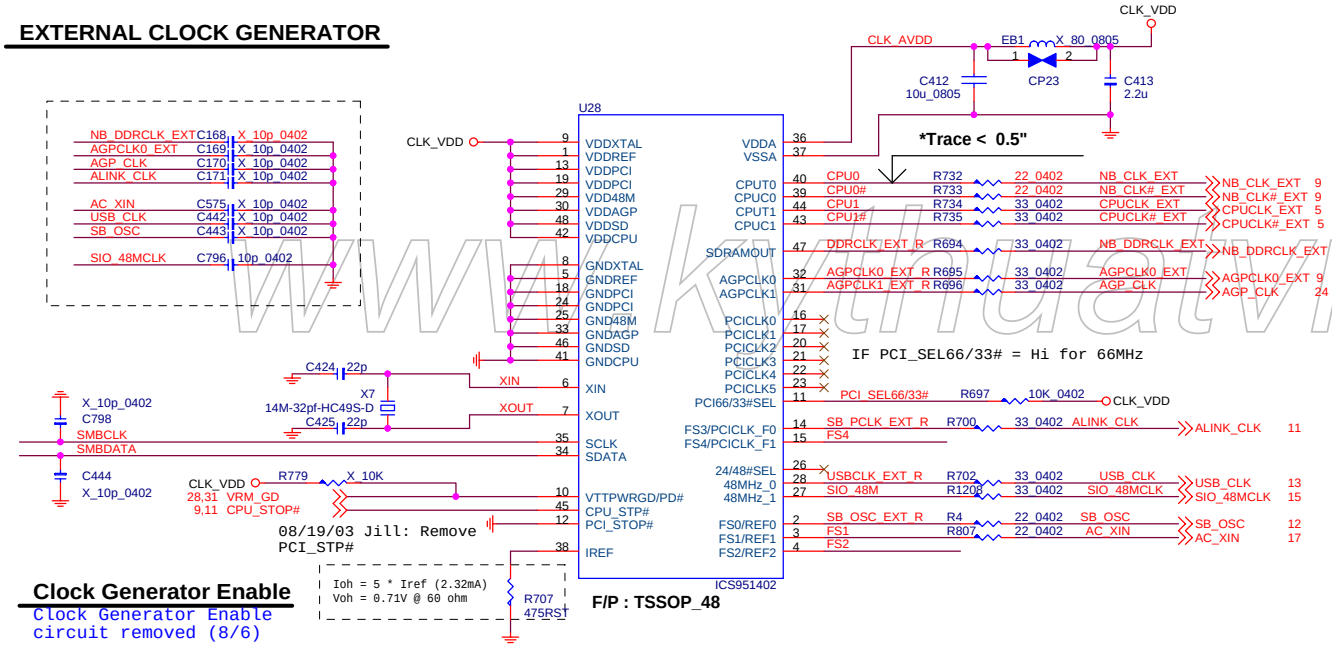


Change to 0805

CLOCK GENERATOR DECOUPLING CAP.



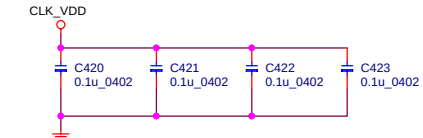
EXTERNAL CLOCK GENERATOR



F/P : TSSOP_48

Clock Generator Enable

Clock Generator Enable circuit removed (8/6)

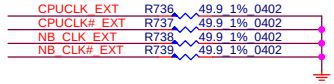


NOTE : CONNECT DDR CLOCKGROUP AS BELOW :

1) DIMM1 : CLKOUT 0/#0 +CLKOUT 4/#4 + CLKOUT 9/#9

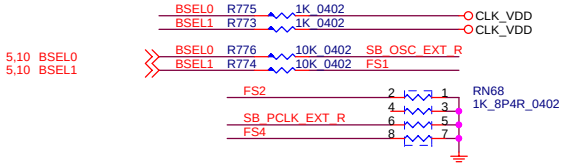
3) DIMM3 : CLKOUT 8/#8 +CLKOUT 7/#7 + CLKOUT 3/#3

Shut Source Termination Resistors



Trace less 0.2"

49.9ohm for 50ohm M/B impedance



S4	S3	S2	BSEL1 S1	BSEL0 S0	CPU	MEM	AGP	PCIsel=0	PCIsel=1	
0	0	0	0	0	100	100	66.6	33.3	66.6	
0	0	0	0	1	133	133	66.6	33.3	66.6	CPU/SDRAM
0	0	0	1	0	200	200	66.6	33.3	66.6	SYNC
0	0	0	1	1	166	166	66.6	33.3	66.6	

RESISTORS CONFIGURATION FOR INTERNAL AND EXTERNAL CLOCK

MSI MICRO-STAR INt'L CO., LTD.

Title: EXTERNAL CLOCK & DDR CLOCK BUFFER

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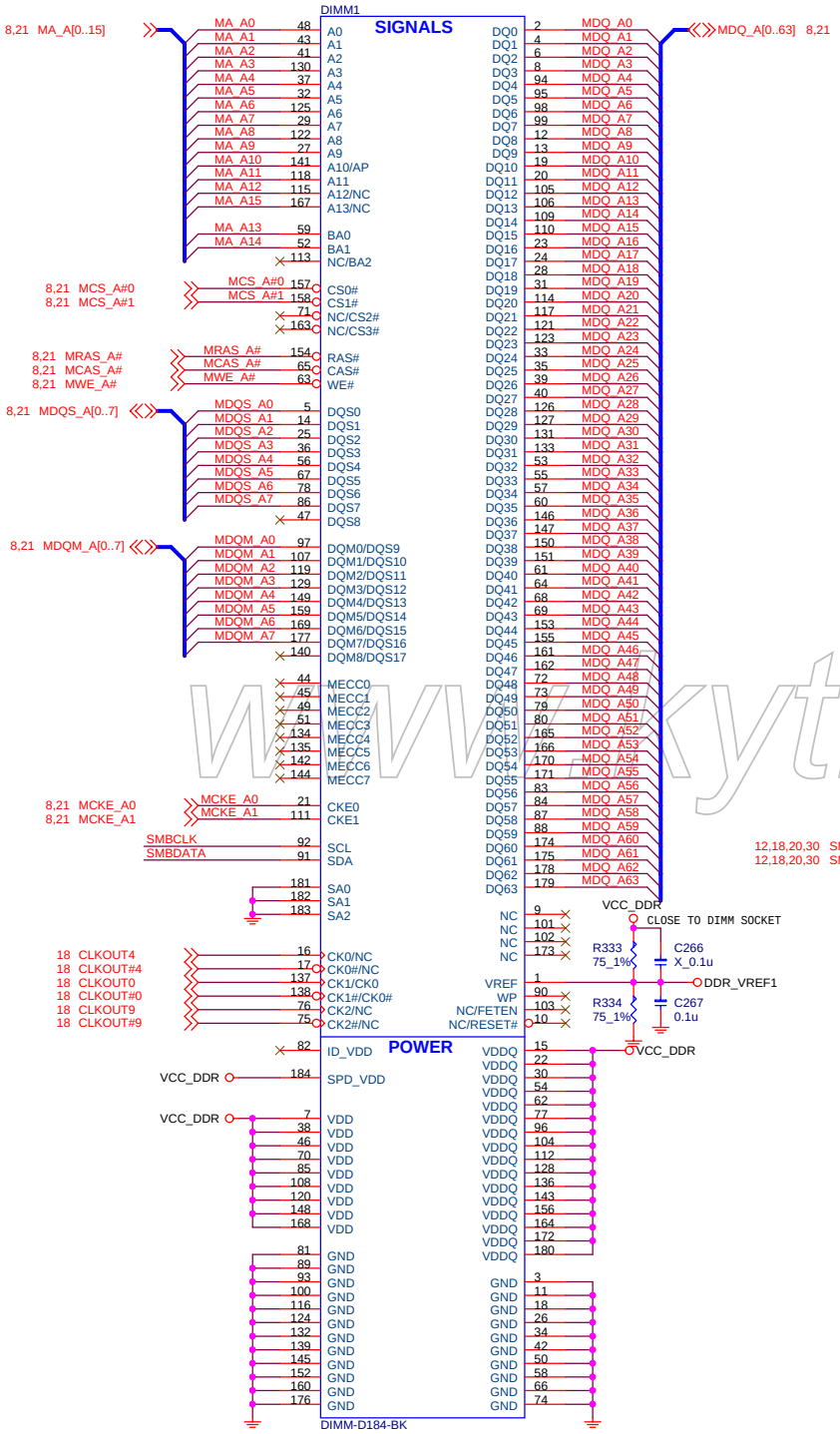
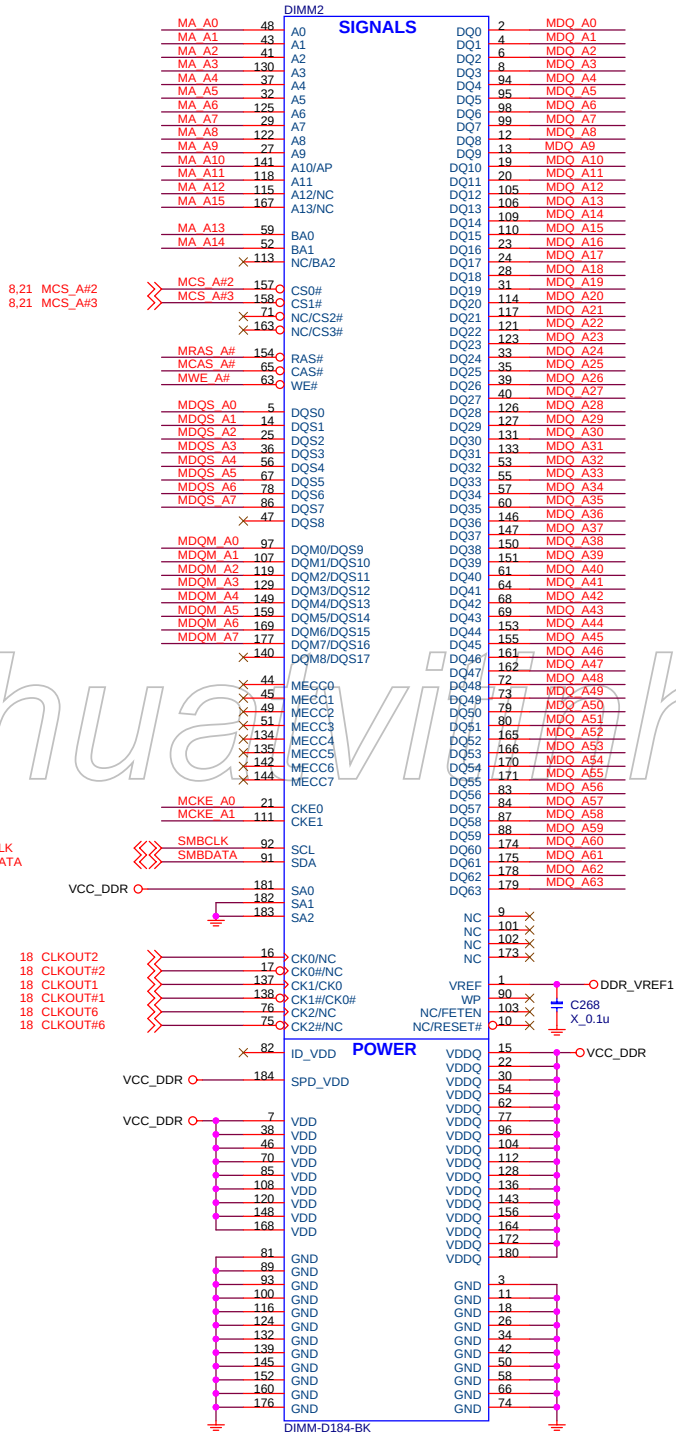
DDR DIMM1



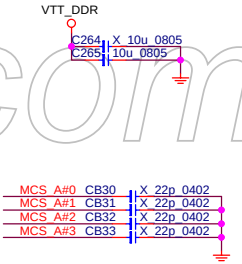
ADDR.=1010000B(A0H)

DDR DIMM2



ADDR.=1010001B(A2H)

DECOUPLING CAPACITORS



MICRO-STAR INt'L CO., LTD.

Title: DDR DIMM 1 & 2 CHANNEL A

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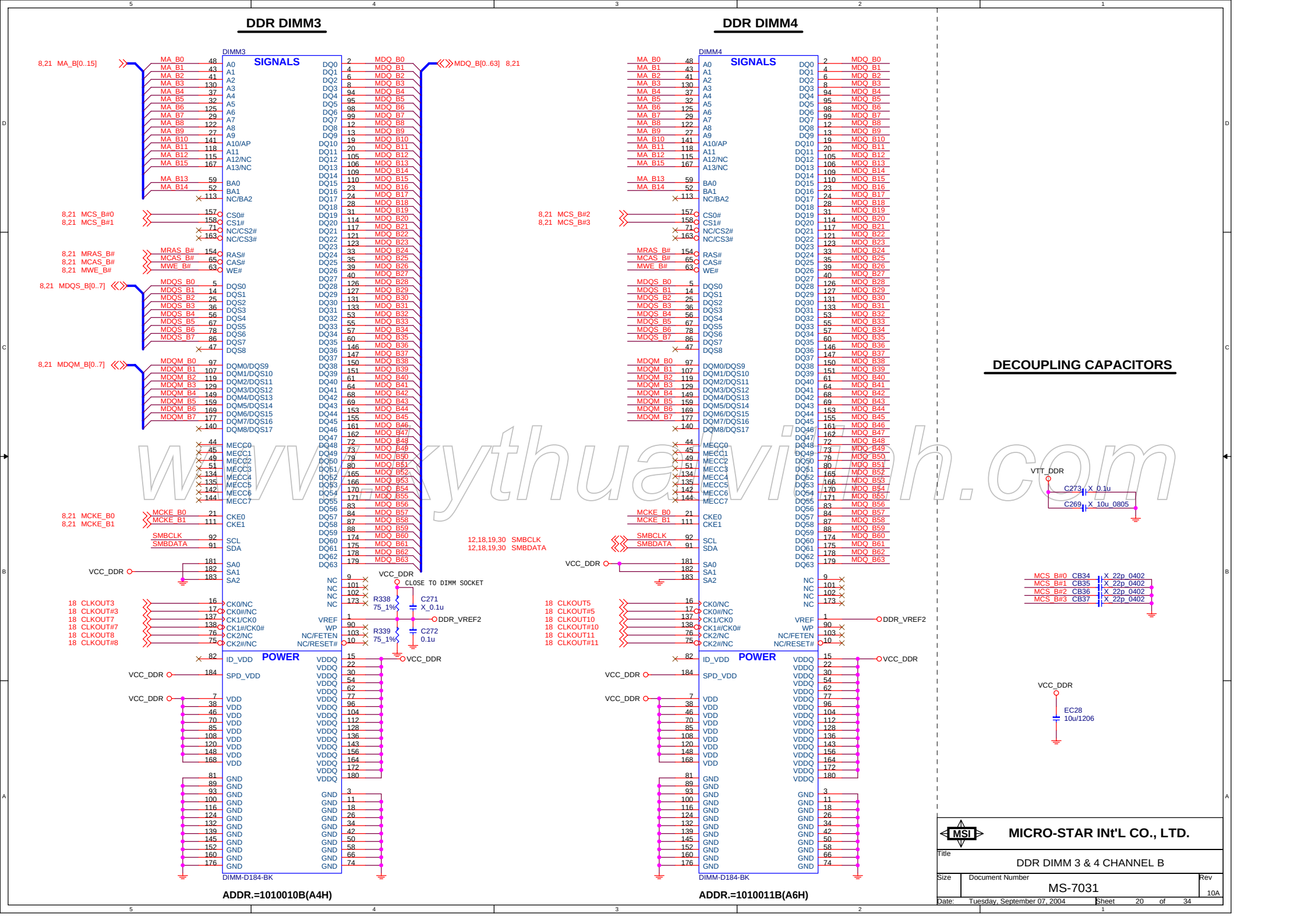
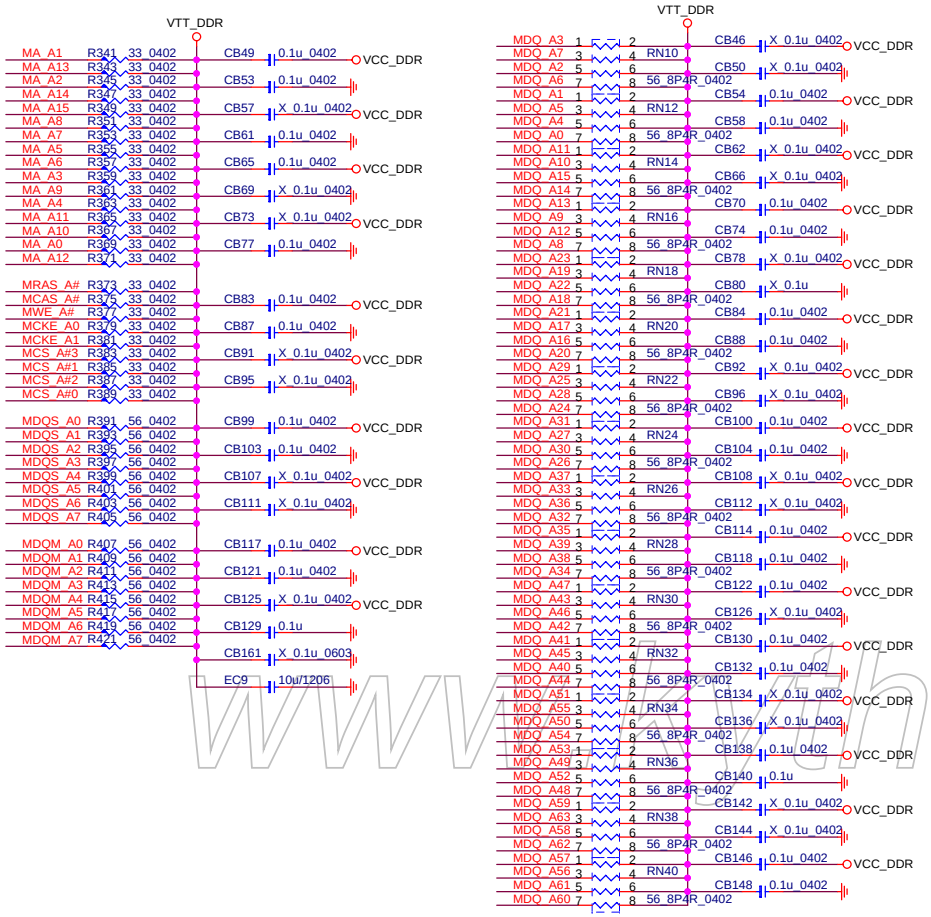

DDR DIMM3
DDR DIMM4
DECOUPLING CAPACITORS
DIMM3
DIMM4
SIGNALS
POWER
DIMM-D184-BK
ADDR.=1010010B(A4H)
ADDR.=1010011B(A6H)
MICRO-STAR INt'L CO., LTD.
DDR DIMM 3 & 4 CHANNEL B
MS-7031
Tuesday, September 07, 2004
www.kythuatvinh.com

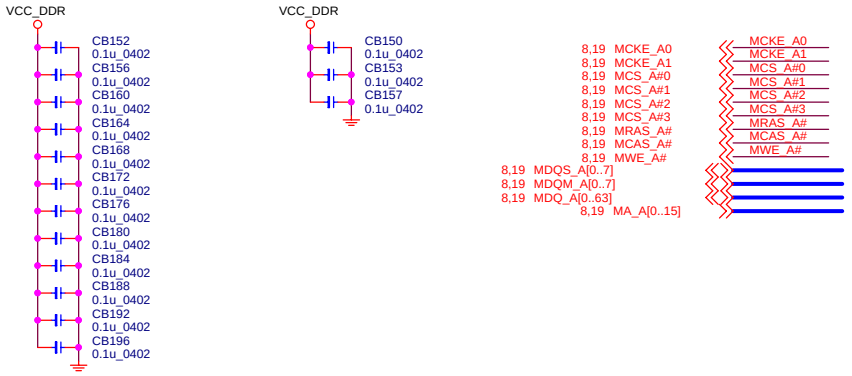
DDR Channel_A Terminational Resisitors



DDR Channel_B Terminational Resisitors

DDR Channel_A DECOUPLING CAPACITORS

Place these decoupling capacitors close to VTT_DDR termination resistors.
One decoupling capacitor for each R-pack.

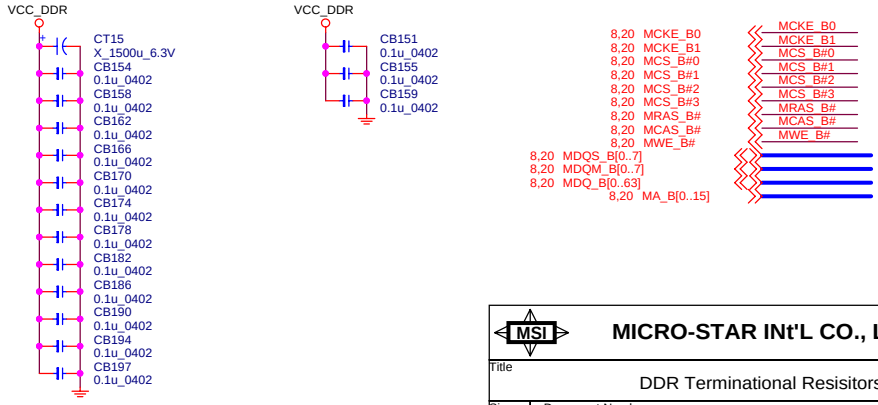


For Ch_A DIMM1

For Ch_A DIMM2

DDR Channel_B DECOUPLING CAPACITORS

Place these decoupling capacitors close to VTT_DDR termination resistors.
One decoupling capacitor for each R-pack.



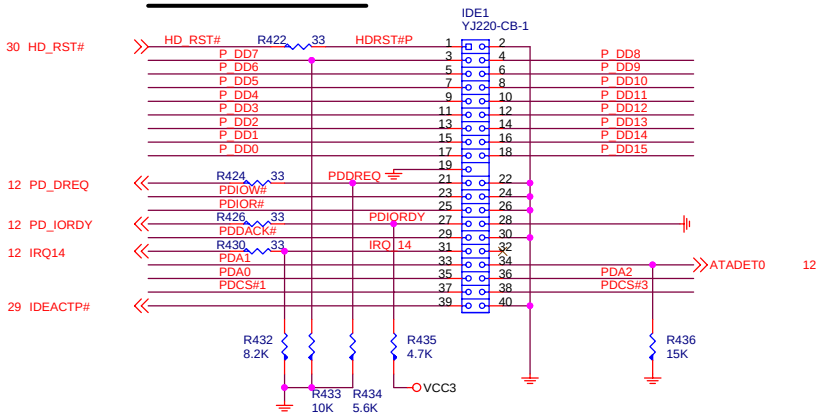
For Ch_B DIMM1

For Ch_B DIMM2

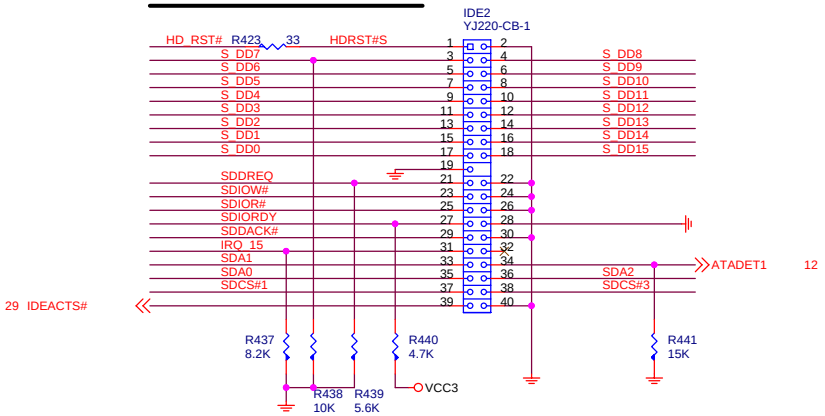
MICRO-STAR INt'L CO., LTD.

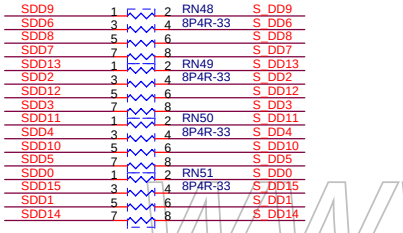
Title	DDR Terminational Resisitors	
Size	Document Number MS-7031	Rev 10A
Date: Tuesday, September 07, 2004	Sheet 21 of 34	

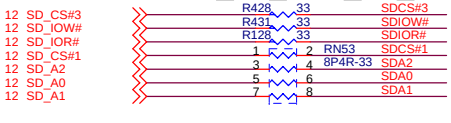
PRIMARY IDE BLOCK

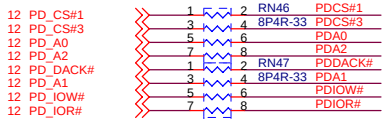


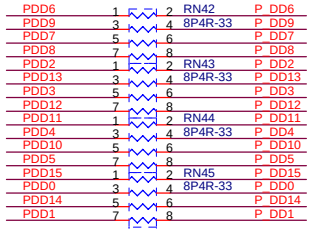
SECONDARY IDE BLOCK





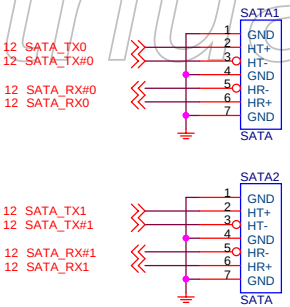






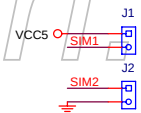
12 PDD[0..15]
12 SDD[0..15]

SERIAL ATA CONNECTOR BLOCK

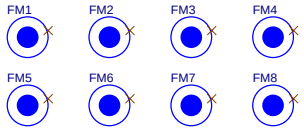


20:5:7:5:20<5"

Simulation



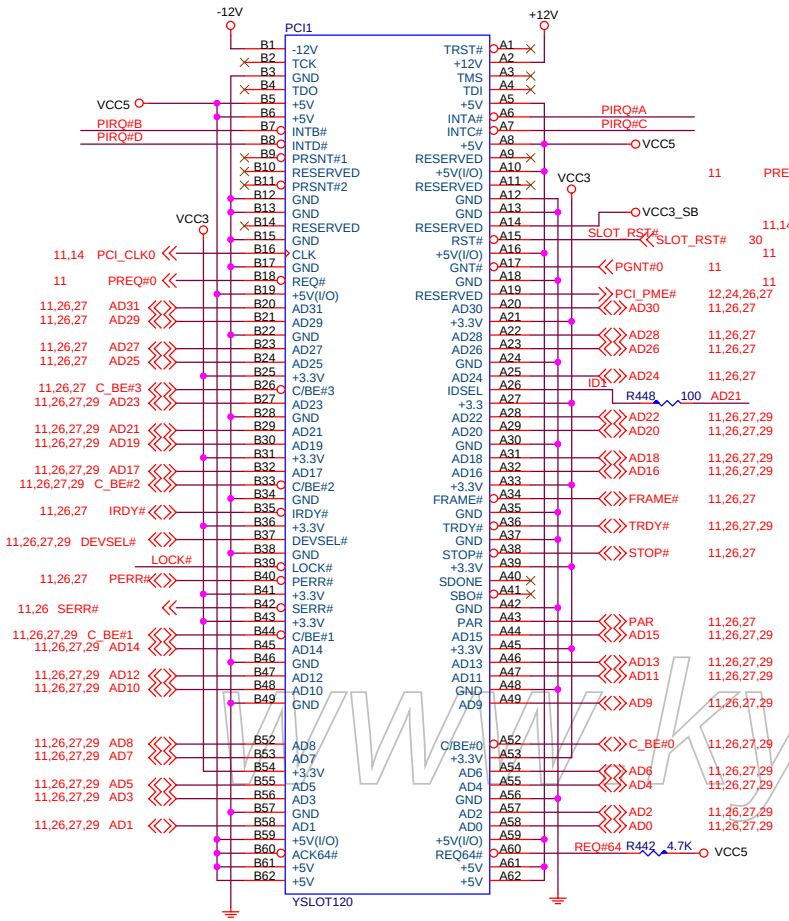
Optics Orientation Holes



MSI MICRO-STAR INt'L CO., LTD.

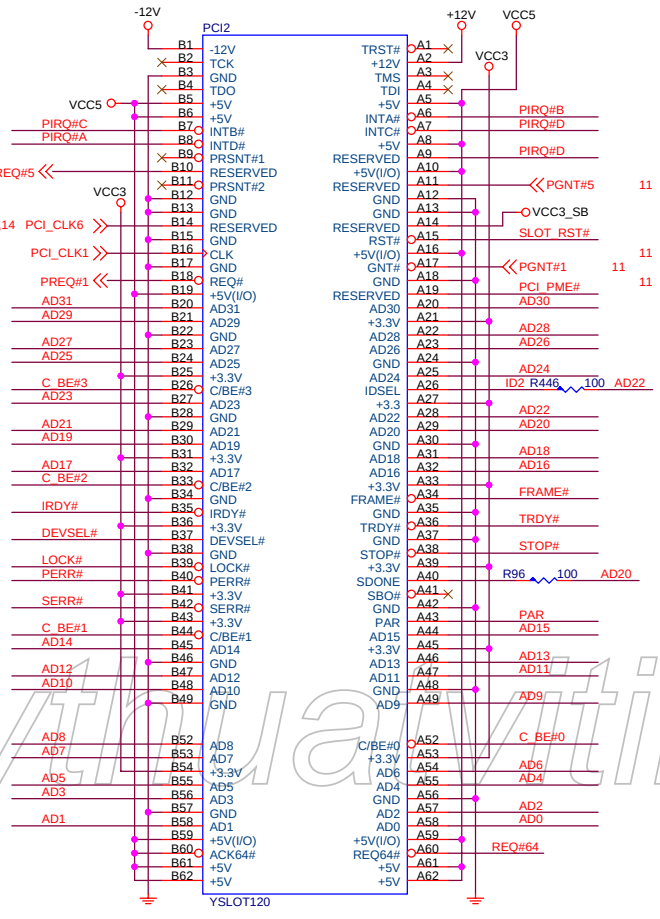
Title	IDE CONNECTORS	
Size	Document Number MS-7031	Rev 10A
Date: Tuesday, September 07, 2004	Sheet 22 of 34	

PCI SLOT 1 (PCI VER: 2.2 COMPLY)



IDSEL = AD21
MASTER = PREQ#0
PIRQ#A

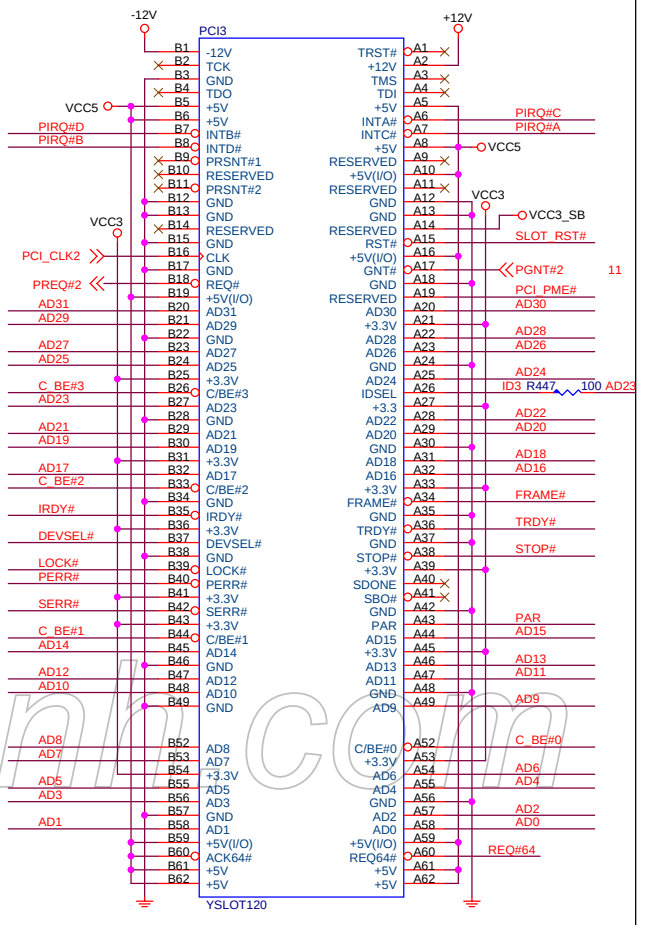
PCI SLOT 2 (PCI VER: 2.2 COMPLY)



IDSEL = AD22
MASTER = PREQ#1
PIRQ#B

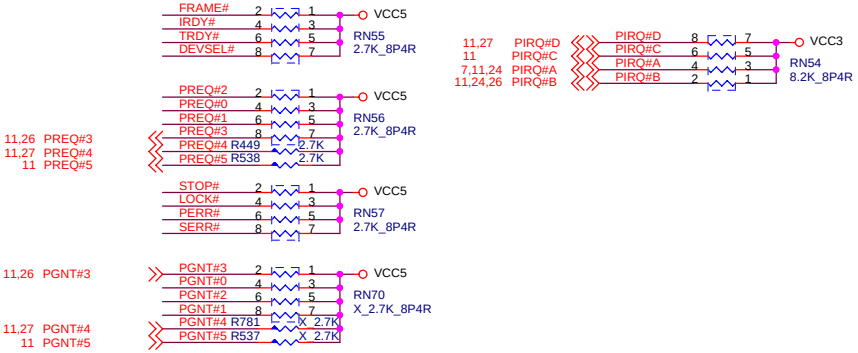
IDSEL = AD20
MASTER = PREQ#5
PIRQ#D

PCI SLOT 3 (PCI VER: 2.2 COMPLY)

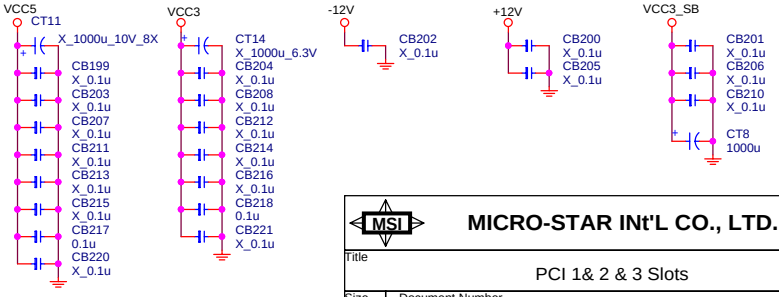


IDSEL = AD23
MASTER = PREQ#2
PIRQ#C

PCI PULL-UP / DOWN RESISTORS



PCI SLOT DECOUPLING CAPACITORS



MSI **MICRO-STAR INt'L CO., LTD.**

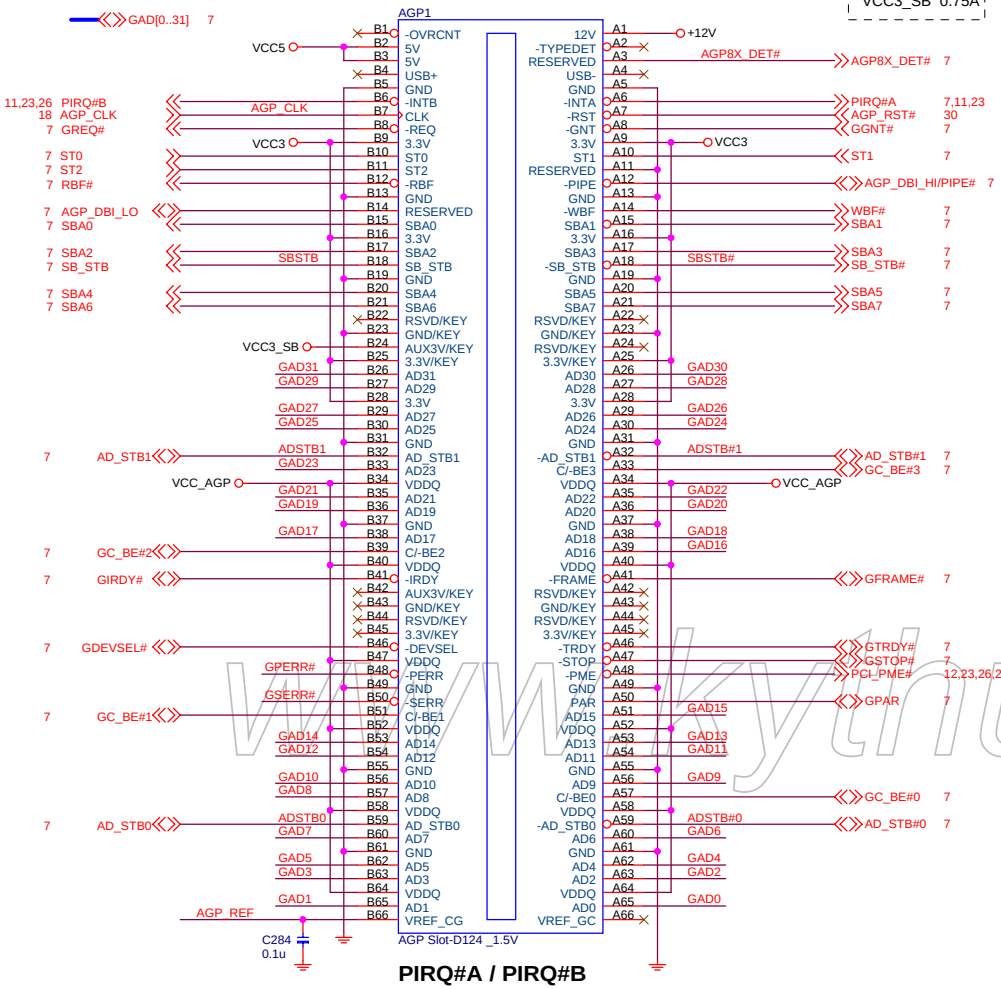
Title	PCI 1& 2 & 3 Slots	
Size	Document Number MS-7031	Rev 10A
Date: Tuesday, September 07, 2004	Sheet 23 of 34	

AGP 1.5V 1X/2X/4X/8X SLOT(AGP VER:3.0)

VCC5 = 60mils trace / 15 mils space

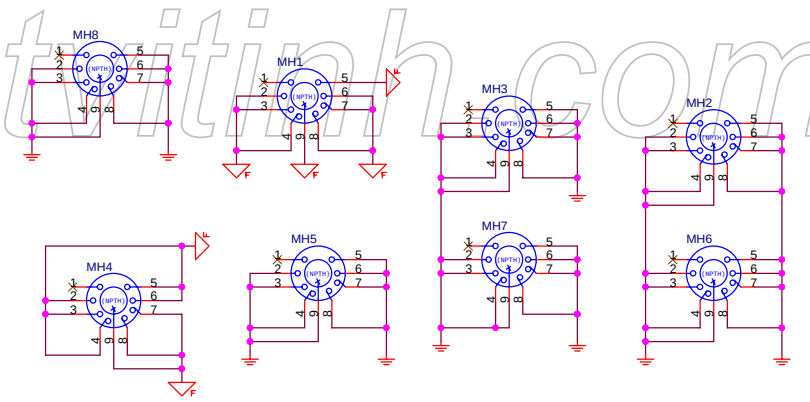
AGP Slot Imax

VCCq	8.0A
VCC3	6.0A
VCC12	1.0A
VCC5	2.0A
VCC3_SB	0.75A



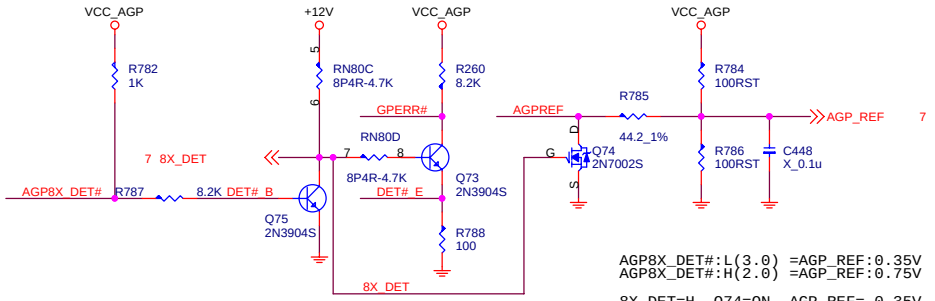
PIRQ#A / PIRQ#B

Mounting Holes



RS300 AGP Reference Voltage Circuit

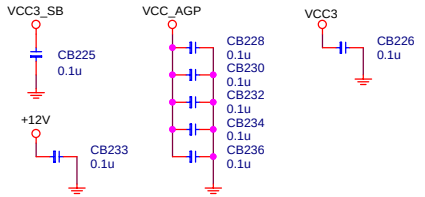
(Place close to AGP1)



AGP8X_DET#:L(3.0) =AGP_REF:0.35V
AGP8X_DET#:H(2.0) =AGP_REF:0.75V

8X_DET=H, Q74=ON, AGP_REF= 0.35V
8X_DET=L, Q74=OFF, AGP_REF= 0.75V

AGP SLOT DECOUPLING CAPACITORS



AGP TERMINATION RESISTORS

LESS 10MILS STUB TRACE LENGTH MUST BE FOLLOWING.

Place these resistors between PCI and AGP slot

MICRO-STAR INt'L CO., LTD.

Title	AGP 1.5V SLOT & FAN CONNECTORS	
Size	Document Number: MS-7031	Rev: 10A
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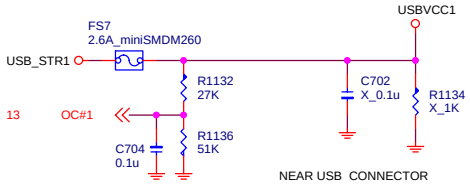
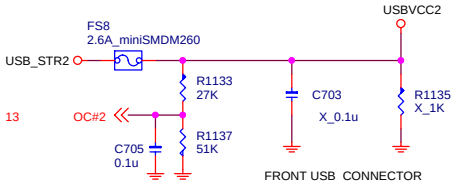
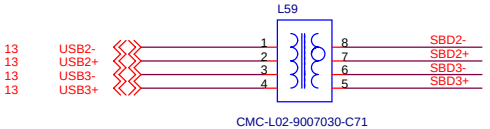
POWER CIRCUIT FOR USB PORT 0,1,2,3

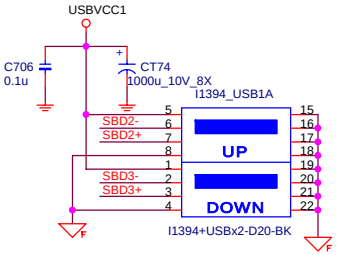


POWER CIRCUIT FOR USB PORT 4,5,6,7

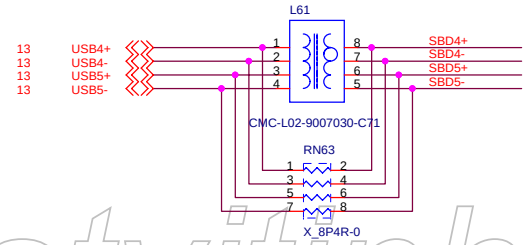


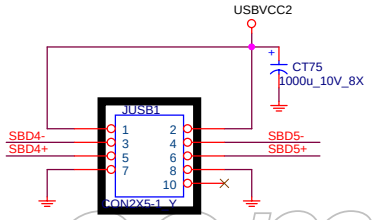
REAR PANEL USB CONNECTOR FOR USB PORT 0,1



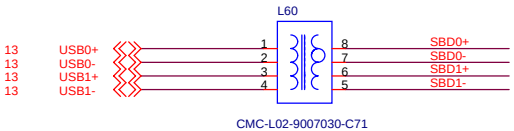


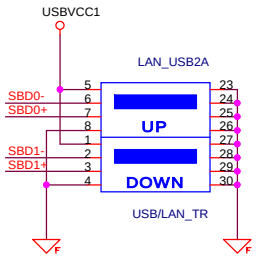
FRONT PANEL USB CONNECTOR FOR USB PORT 4,5

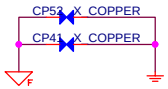




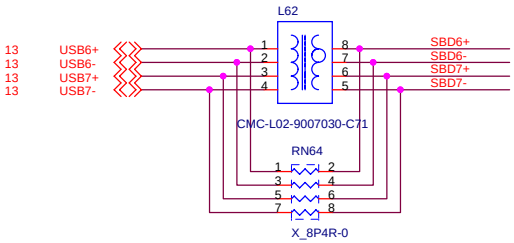
REAR PANEL USB CONNECTOR FOR USB PORT 2,3

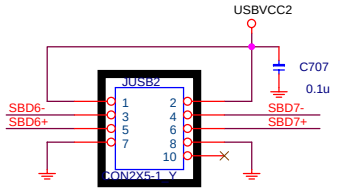






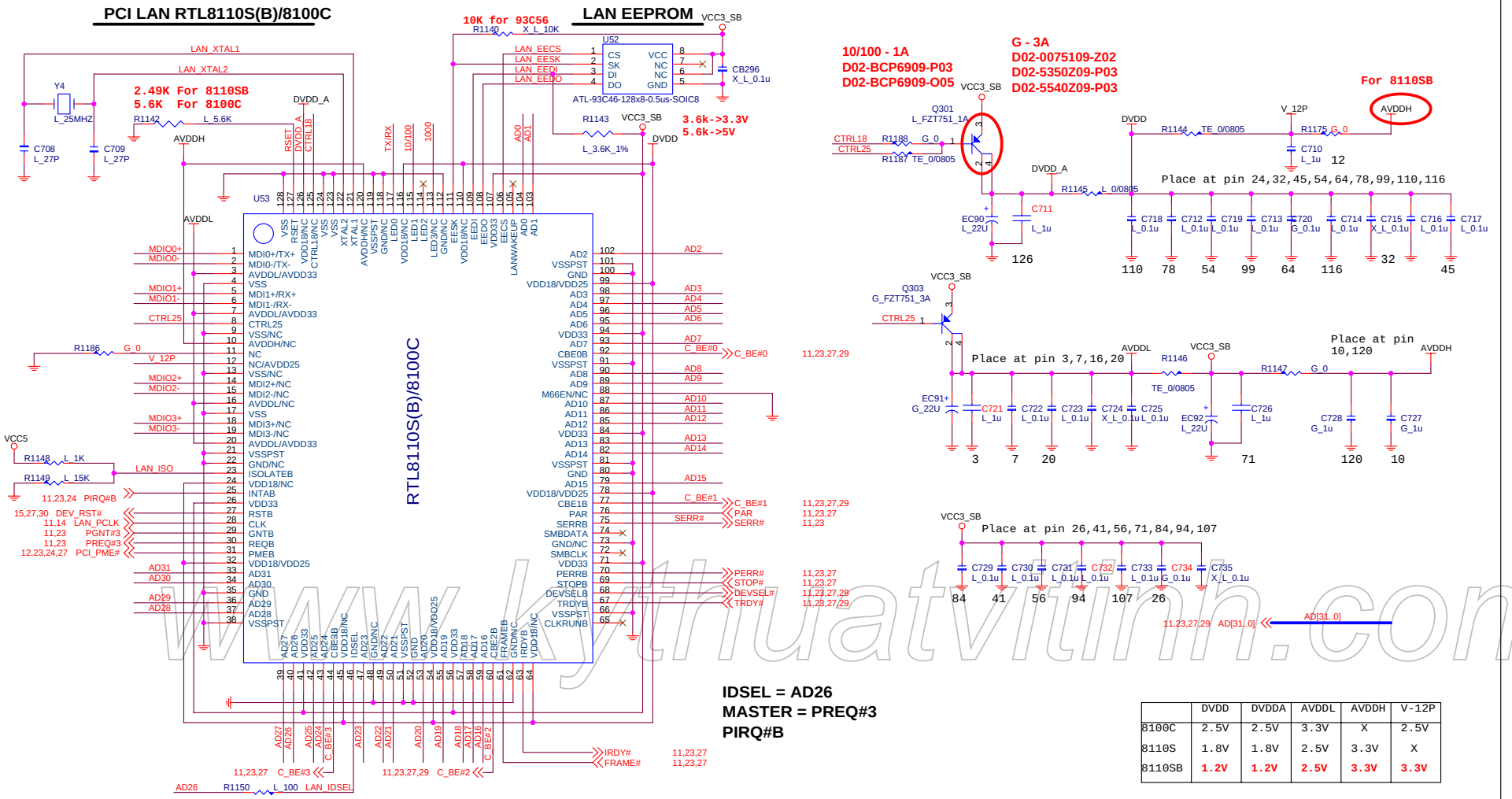
FRONT PANEL USB CONNECTOR FOR USB PORT 6,7





MSI **MICRO-STAR INt'L CO., LTD.**

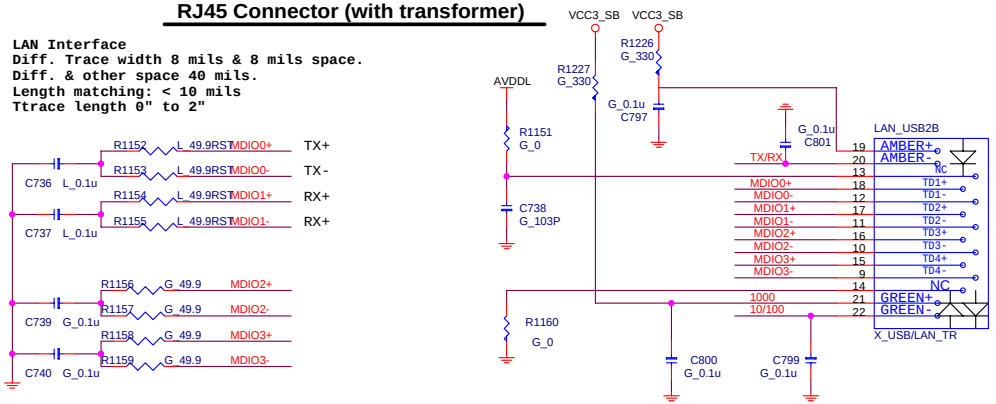
Title	USB Connectors	
Size	Document Number MS-7031	Rev 10A
Date: Tuesday, September 07, 2004	Sheet 25 of 34	



	DVDD	DVDDA	AVDDL	AVDDH	V-12P
8100C	2.5V	2.5V	3.3V	X	2.5V
8110S	1.8V	1.8V	2.5V	3.3V	X
8110SB	**1.2V**	**1.2V**	**2.5V**	**3.3V**	**3.3V**

RJ45 Connector (with transformer)

LAN Interface
Diff. Trace width 8 mils & 8 mils space.
Diff. & other space 40 mils.
Length matching: < 10 mils
Ttrace length 0" to 2"



G :N58-22F0031
L :N58-18F0031-S42 / WO LED

Part Value Selection:

G: 8110SB LAN(1000M)
TE: 8100C LAN(10/100M)

L: With LAN option
X: No Stuff

Micro Star Restricted Secret

Title	Realtek 8100C / 8110S PCI LAN Controller
Document Number	MS-7031
Rev	10A
Last Revision Date:	Tuesday, September 07, 2004
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MICRO-STAR INT'L CO.,LTD.
No. 69, Li-De St, Jung-He City,
Taipei Hsien, Taiwan
http://www.msi.com.tw

IEEE-1394

P3VD
C645 I_0.1u
C646 X_I_1u
P3VA
C647 I_0.1u
C648 I_0.1u
C649 I_0.1u

VCC3
NEAR EACH POWER PIN
C656 I_0.1u
C657 I_0.1u
C658 I_0.1u
C659 I_0.1u
C660 I_0.1u
C652 I_0.1u
C653 X_I_0.1u
C654 X_I_0.1u
C655 I_0.1u

FRONT 1394 PORT 1

TPBIAS1
R1064 I_54.9_1%
R1065 I_54.9_1%
C663 I_1u
TPA1+
TPA1-
TPB1+
TPB1-
R1066 I_4.99K_1%
R1067 I_54.9_1%
C664 I_270p
R1069 I_54.9_1%
(T/S/S=7/10/10)
Place close to pin 97
(Less then 500 mils)

VCCP_IN
D47 I_1N5817
FS6 I_1.5A_miniSMDM150/24
1394_VCC1
CB292 I_104p
J1394_USB1B
PWR
TPA+
TPA-
TPB+
TPB-
GND
I1394+USBx2-D20-BK

TPBIAS2
R1072 I_54.9_1%
R1073 I_54.9_1%
C667 I_1u
TPA2+
TPA2-
R1074 I_4.99K_1%
R1075 I_54.9_1%
C668 I_270p
R1076 I_54.9_1%
TPB2+
TPB2-
(T/S/S=7/10/10)
Place close to pin 111
(Less then 500 mils)

FS5 I_1.5A_miniSMDM150/24
1394_VCC2
BUS_PWR
+12V
D46 I_1N5817
C650 I_0.1u
C651 I_1000p

VCC3 P3VD
CP37
FB106 X_120S_0805
VCC3 P3VA
CP38
FB107 X_120S_0805
CP40
FB108 X_80_0805

J1394_1
I_CON2X5-1_G
TPA2+
TPB2+
1394_VCC2
TPA2-
TPB2-
1394_VCC2
CB291 I_0.1u

VCC3
P3VD
P3VA
U47
I_VT6307-CD
B07-0630704-V01

AD31 AD30 AD29 AD28 AD27 AD26 AD25 AD24 AD23 AD22 AD21 AD20 AD19 AD18 AD17 AD16 AD15 AD14 AD13 AD12 AD11 AD10 AD9 AD8 AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0
C_BE#3 C_BE#2 C_BE#1 C_BE#0
PAR FRAME# IRDY# TRDY# STOP# DEVSEL# PREQ#4 PGNT#4 PERR# PIRQ#D
1394_PCLK
DEV_RST#
PME#

XTPBIAS0 XTPA0P XTPA0M XTPB0P XTPB0M
XTPBIAS1 XTPA1P XTPA1M XTPB1P XTPB1M
XTPBIAS2 XTPA2P XTPA2M XTPB2P XTPB2M
TPBIAS1 TPA1+ TPA1- TPB1+ TPB1-
TPBIAS2 TPA2+ TPA2- TPB2+ TPB2-
BUS_PWR
R1061 I_11K_1%
R1062 I_1K_1%
XCPS
R1063 I_6.34K_1%
C661 I_47p
XREXT
D6/CMCJMP
PHYRESET
C662 I_0.1u
CTL0/PC0JMP CTL1/PC1JMP D7/PC2JMP
LINKON/TSIJMP LREQ/TSOJMP
D5 D4 D3 D2 D1 D0 MODE0 MODE1 SCLK LPS/CMC NC
For 24C02
R1068 I_2.7K
P3VD
SCL/EECK SDA/EEDI EEDO EECS
EECK
EEDI
R1104 X_I_2.7K
VCC3
For X_EEPROM
XI XO
C665 I_10p
R1071 I_1M
Y2 I_24.576MHZ
C666 I_10p

PIRQ#D
IDSEL = AD25
MASTER = PREQ4

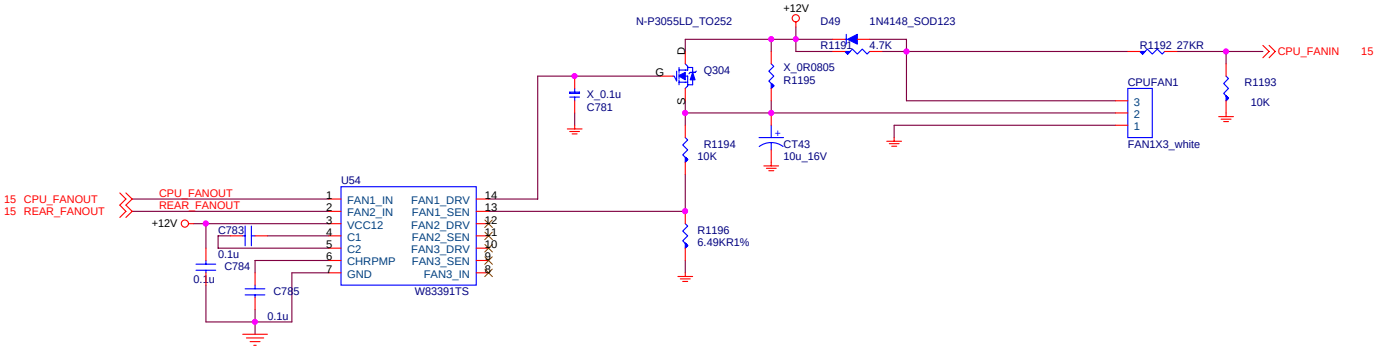
1394-EEPROM 24C02

VCC3
U48
R1077 I_2.7K
R1078 I_2.7K
EEDI
EECK
A2 A1 A0 WP SDA SCL GND VCC
I_24C02
R1079 X_I_5K
VCC3

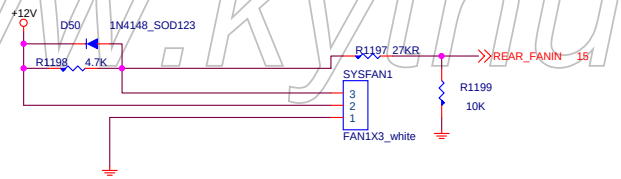
11,23,26,29 AD[31..0]
AD[31..0]

MICRO-STAR
Title: VIA VT-6307
Size: Document Number: MS-7031 Rev: 10A
Date: Tuesday, September 07, 2004 Sheet 27 of 34

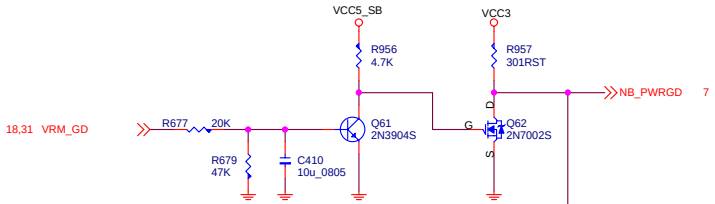
CPU FAN



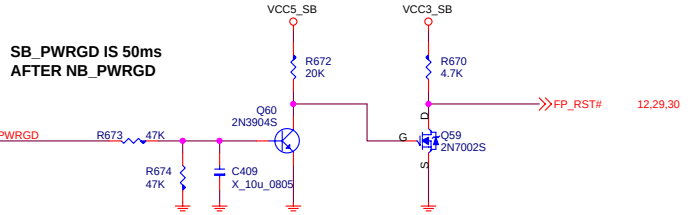
SYSTEM FAN



RS300 POWER GOOD CIRCUIT



SB300 POWER GOOD CIRCUIT



MSI	MICRO-STAR INt'L CO., LTD.	
Title	ATX Connector & Front Panel	
Size	Document Number: MS-7031	Rev: 10A
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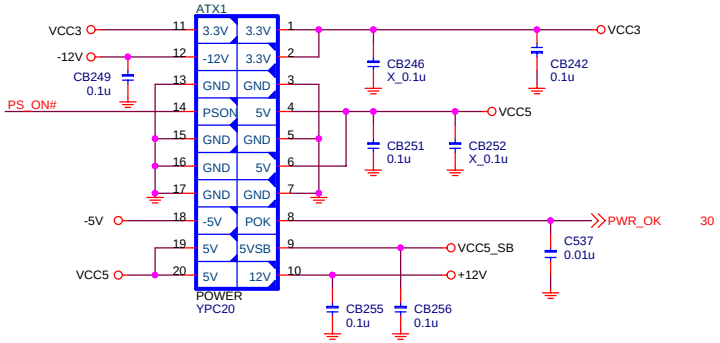
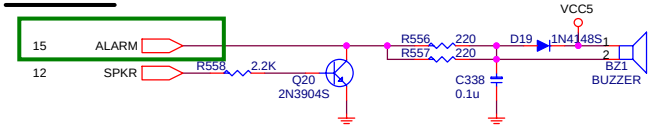
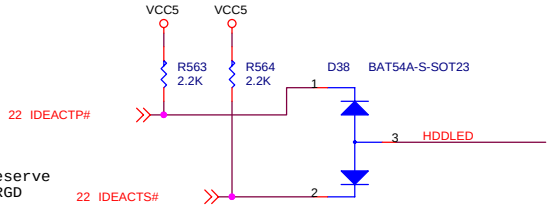
ATX CONNECTOR



BUZZER

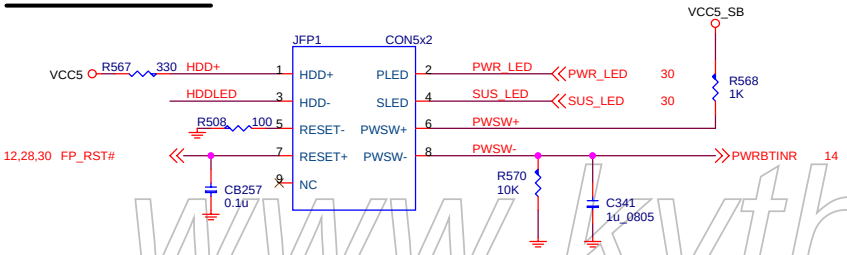


IDE LED

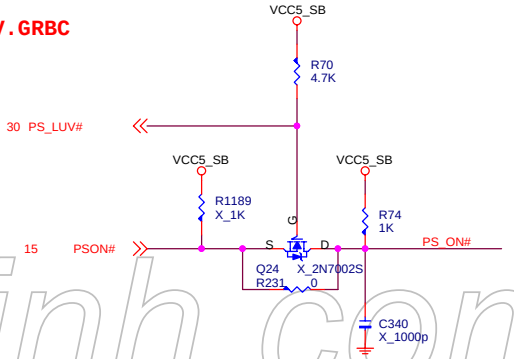


This circuit can be reserve if NB_PWRDG and SB_PWRGD implement into MS-5.

Intel Front Panel

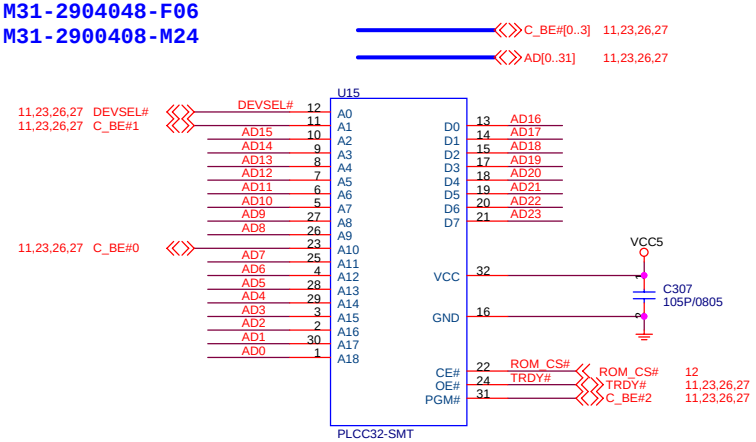


For MS-7 V.GRBC

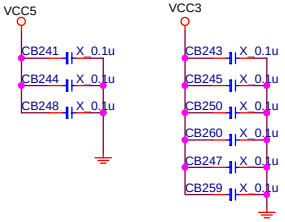


XBus ROM BLOCK

M31-2904088-M24
M31-2904048-F06
M31-2900408-M24

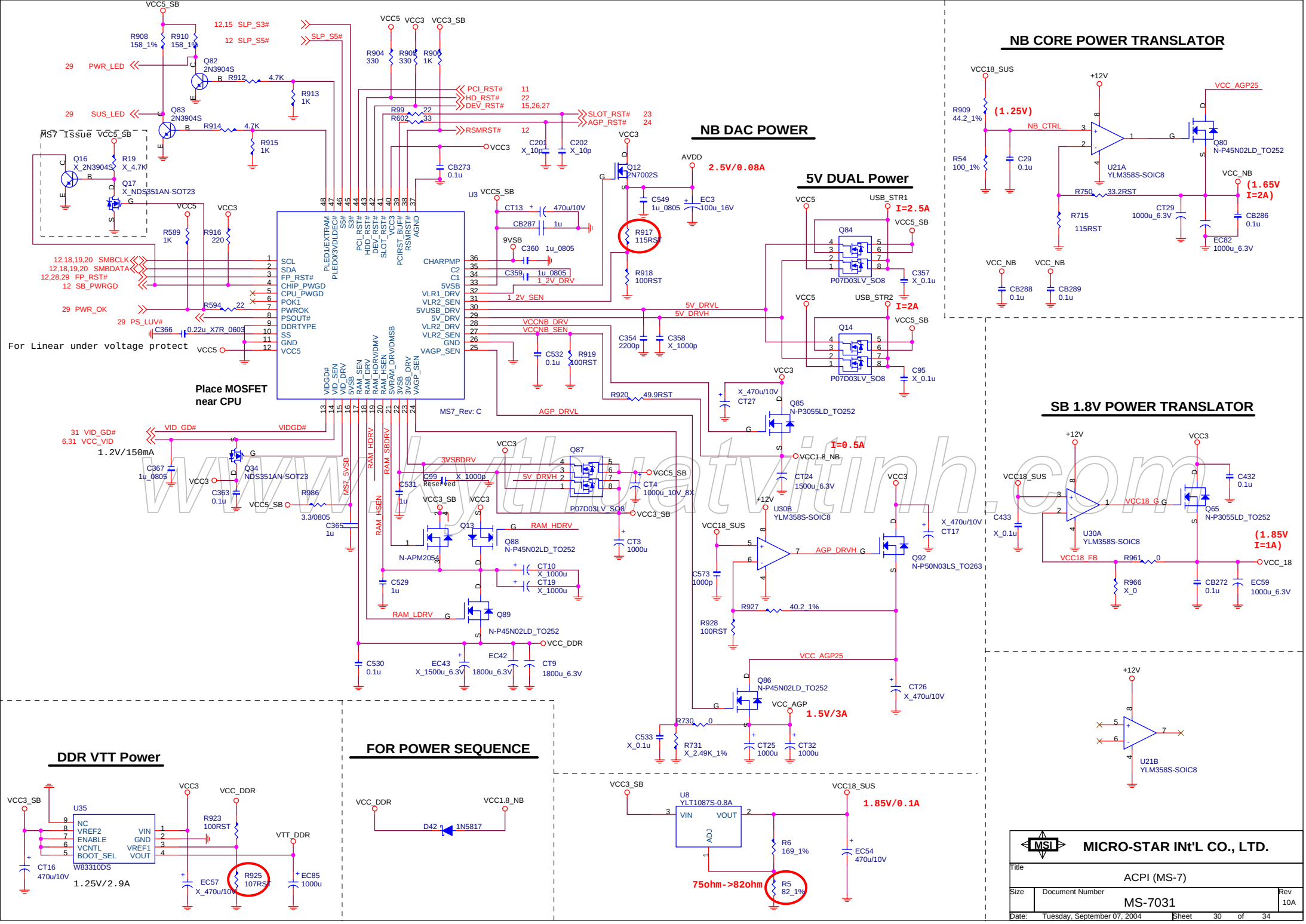


For EMI



MICRO-STAR INt'L CO., LTD.

Title	ATX,Front Panel & X-BUS ROM	
Size	Document Number MS-7031	Rev 10A
Date: Tuesday, September 07, 2004	Sheet 29 of 34	


NB DAC POWER
5V DUAL Power
NB CORE POWER TRANSLATOR
SB 1.8V POWER TRANSLATOR
DDR VTT Power
FOR POWER SEQUENCE
MS7 Issue
Place MOSFET near CPU
For Linear under voltage protect
2.5V/0.08A
I=2.5A
I=2A
I=0.5A
(1.25V)
(1.65V I=2A)
(1.85V I=1A)
1.2V/150mA
1.25V/2.9A
1.5V/3A
1.85V/0.1A
75ohm->82ohm
MICRO-STAR INt'L CO., LTD.
ACPI (MS-7)
MS-7031
Tuesday, September 07, 2004