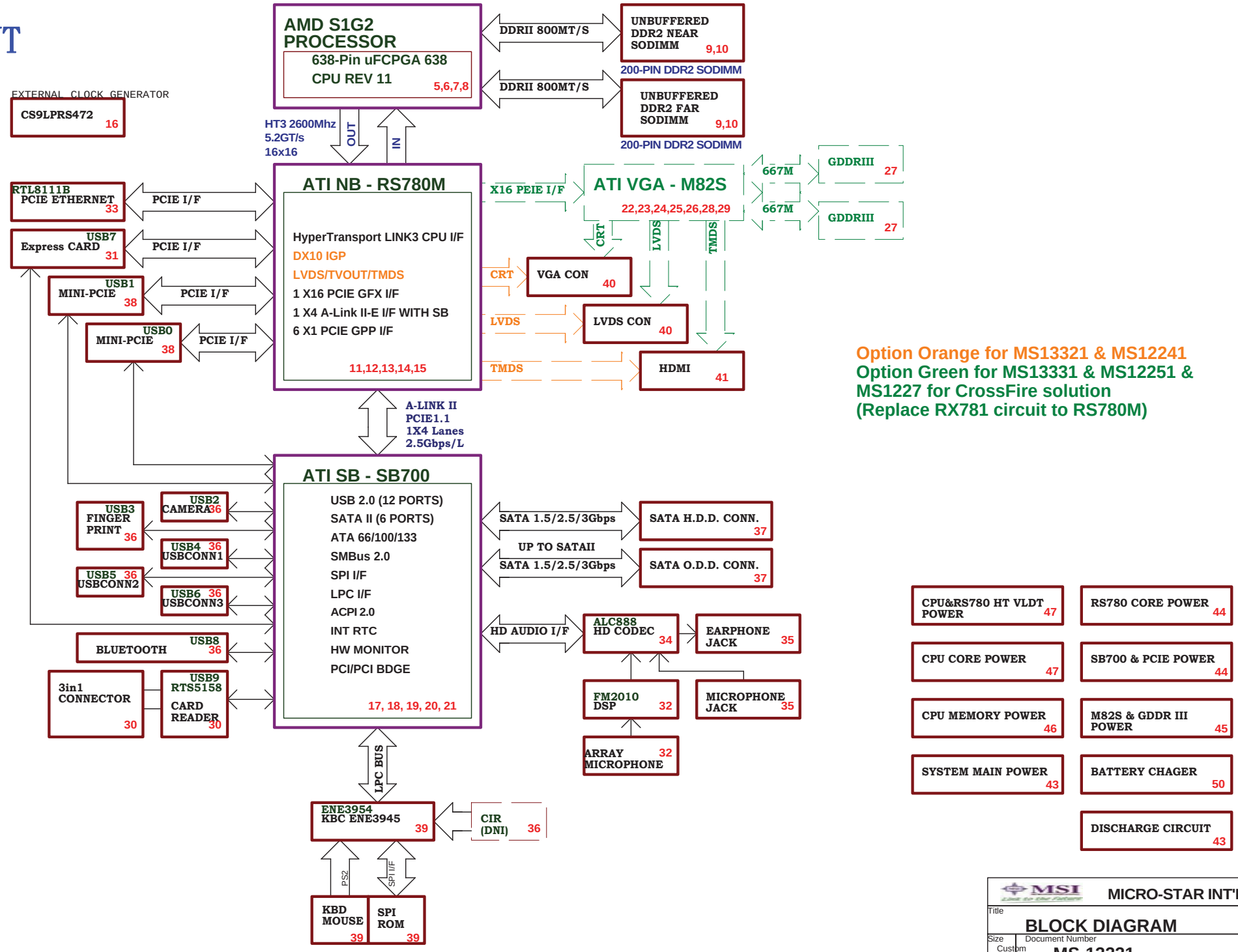
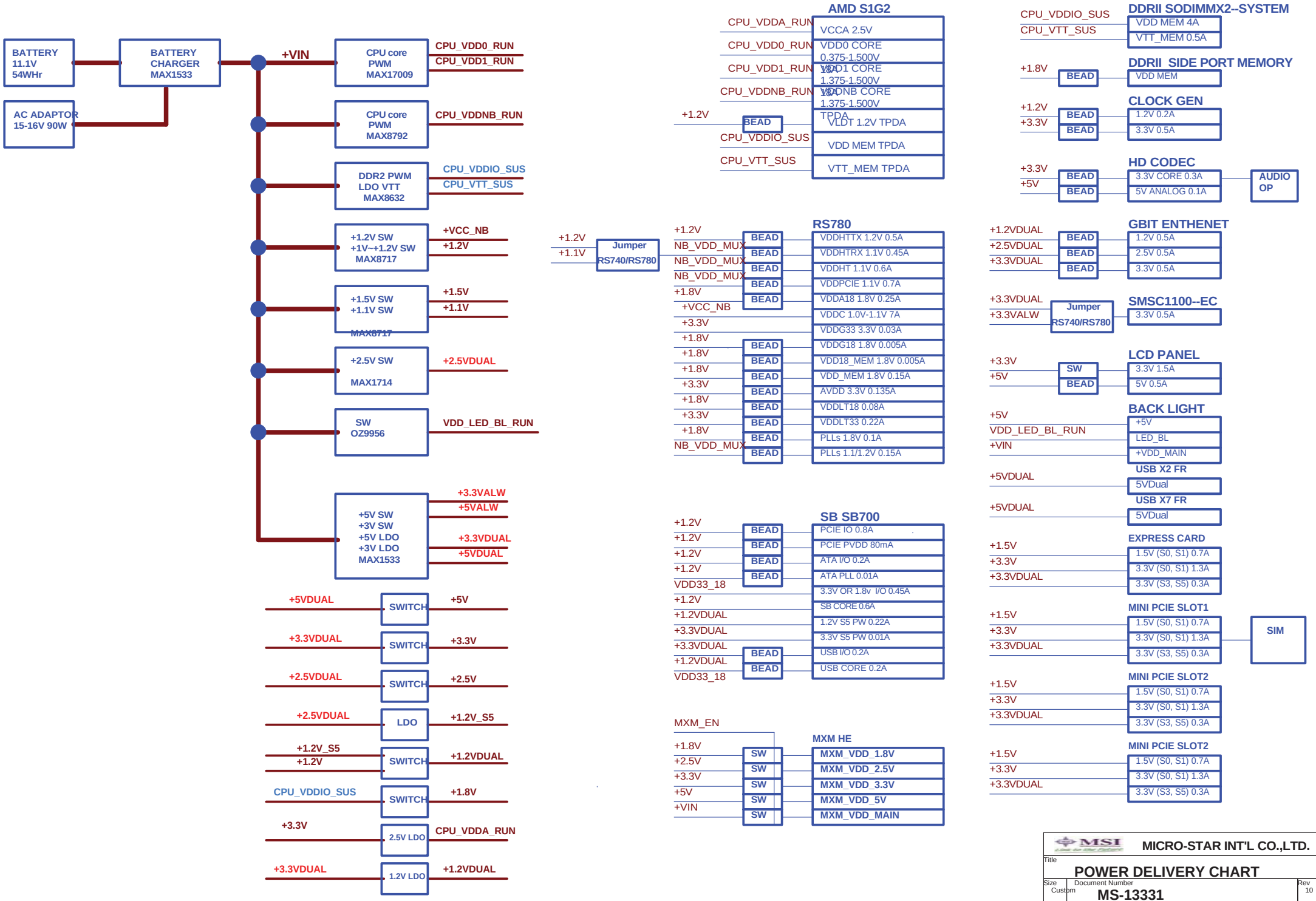


MICRO-STAR INT'L CO.,LTD.

Title: BLOCK DIAGRAM

Size: Custom | Document Number: MS-13331 | Rev: 10

Date: Friday, March 28, 2008 | Sheet 1 of 55

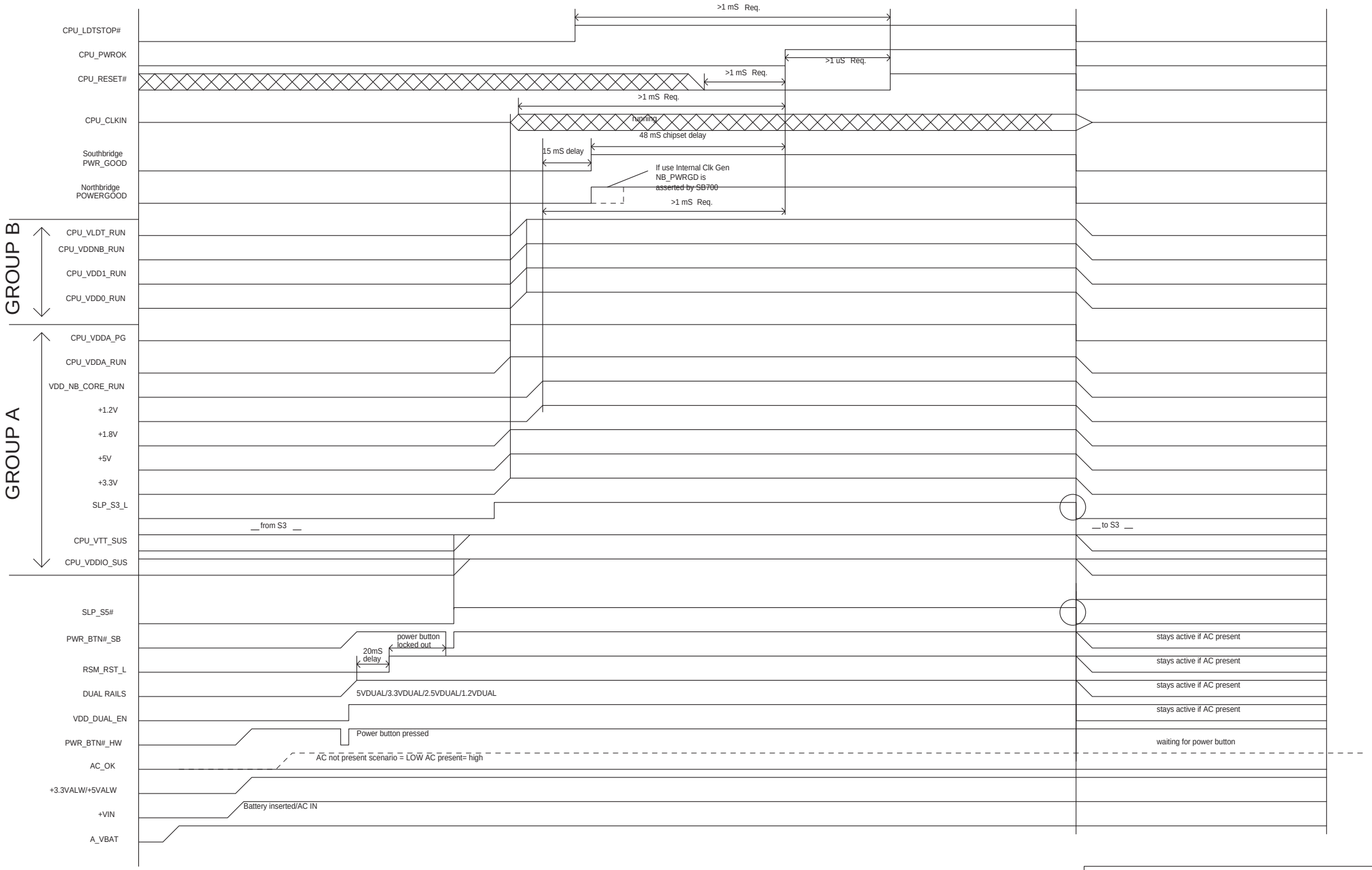


MICRO-STAR INT'L CO.,LTD.

Title: POWER DELIVERY CHART

Size: Custom | Document Number: MS-13331 | Rev: 10

Date: Friday, March 28, 2008 | Sheet 2 of 55

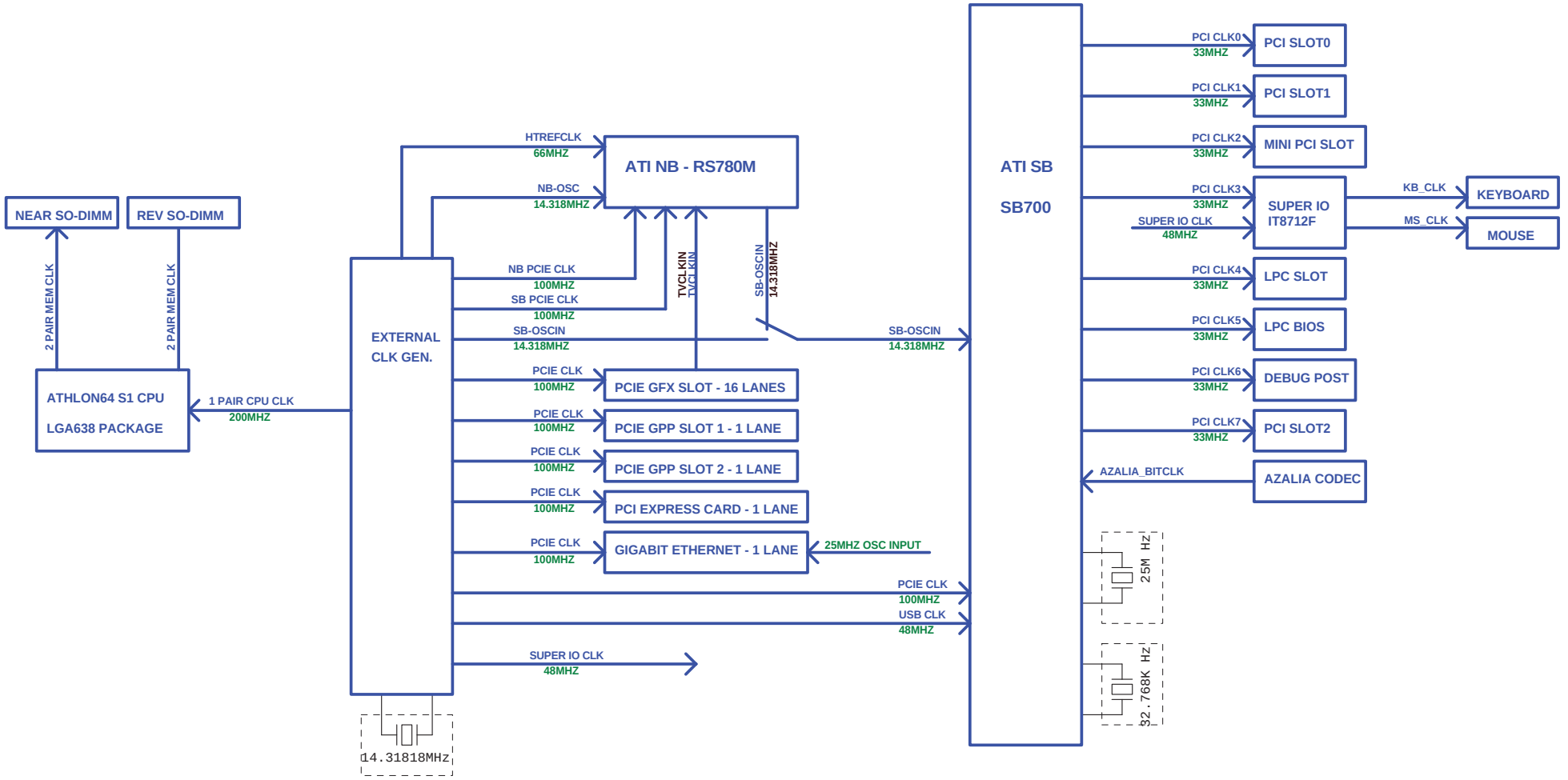


MICRO-STAR INT'L CO.,LTD.

Title: POWER SEQUENCE CHART

Size: Custom | Document Number: MS-13331 | Rev: 10

Date: Friday, March 28, 2008 | Sheet 3 of 55

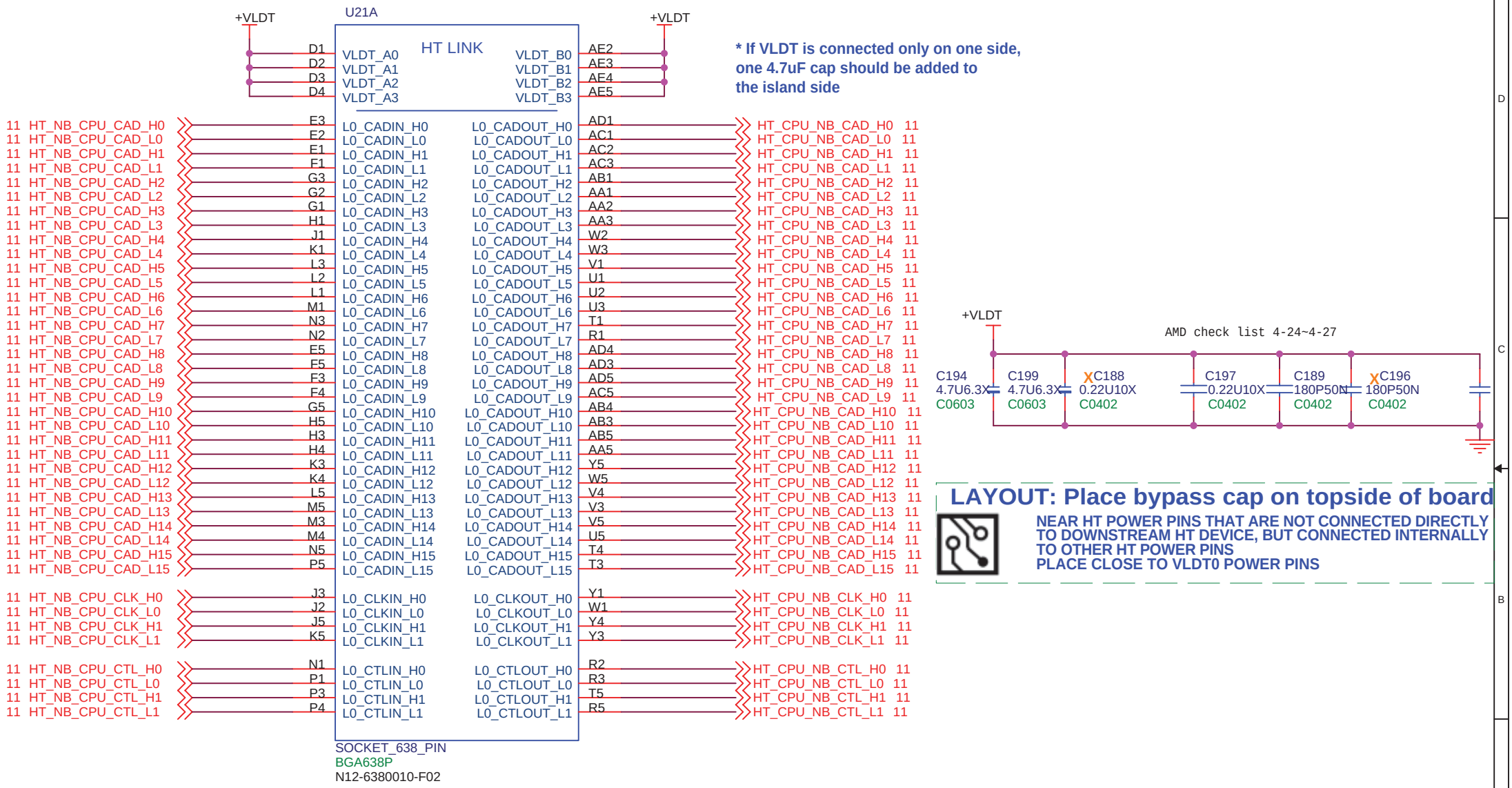


MICRO-STAR INT'L CO.,LTD.

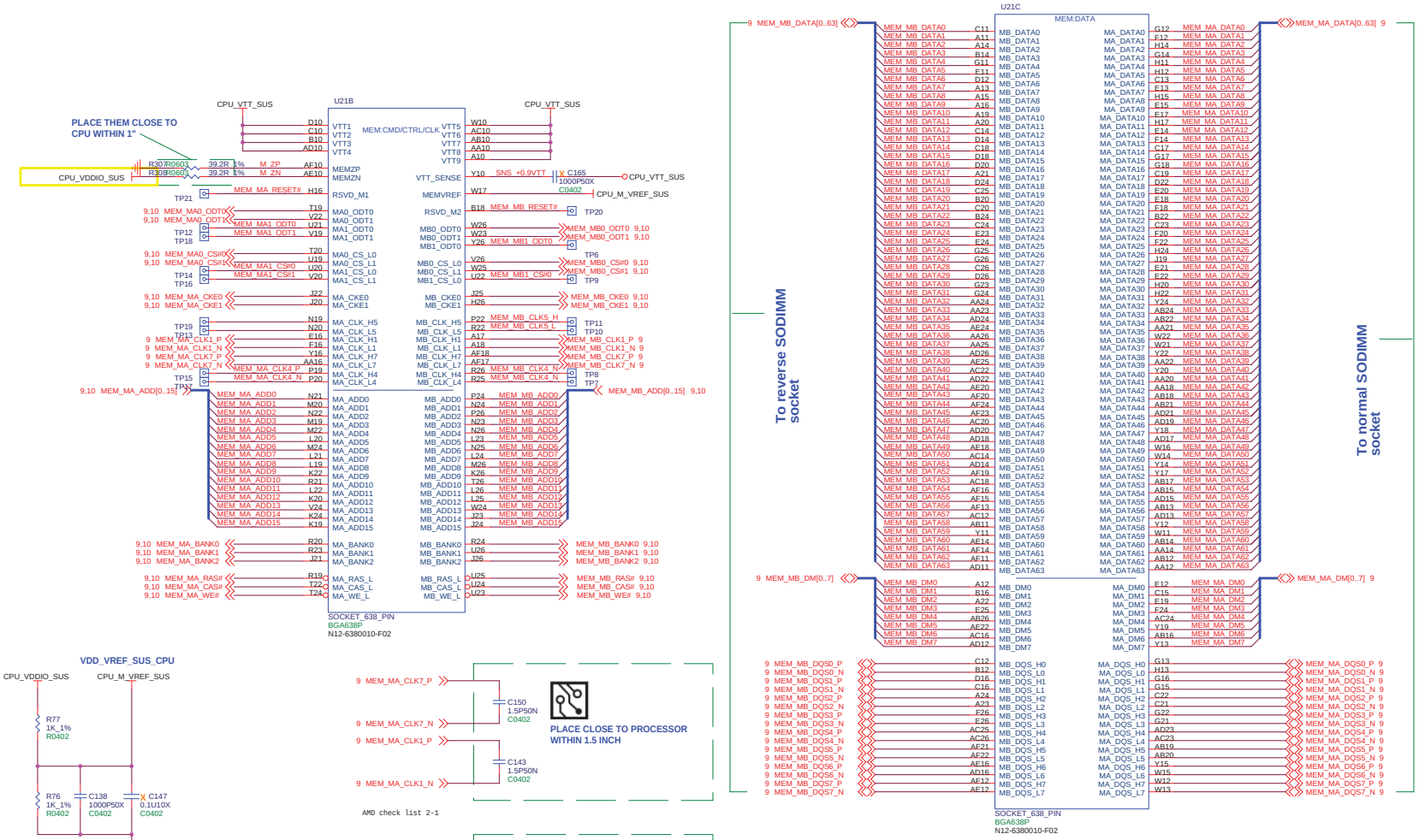
Title: CLOCK DISTRIBUTION

Size: Custom | Document Number: MS-13331 | Rev: 10

Date: Friday, March 28, 2008 | Sheet 4 of 55



Processor Memory Interface



MICRO-STAR INT'L CO.,LTD.			
Title: SOCKET S1G2 DDR2 MEMORY I/F			
Size: C	Document Number: MS-13331		Rev: 10
Date: Friday, March 28, 2008	Sheet 6 of 55		

CPU_VDDA_2.5_RUN

maximun
40 ohm

VDDA 2.5V ==> Max Current 250mA

LAYOUT: ROUTE VDDA TRACE APPROX. 50 mils WIDE (USE 2x25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

del Q10 R81

MVT

Keep trace from resisor to CPU within 0.6"
keep trace from caps to CPU within 1.2"

If unused, the ALERT_L pin is left unconnected

place them to CPU within 1.5"

PWM

route as differential as short as possible testpoint under package

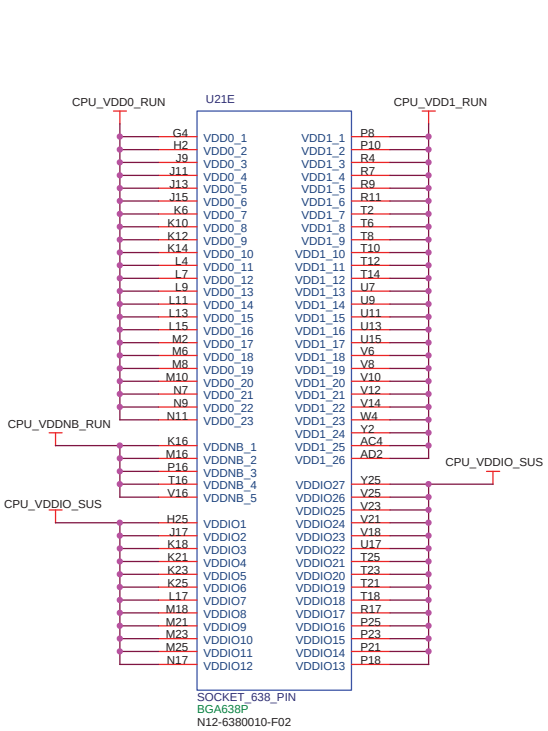
Cap close to thermal sensor

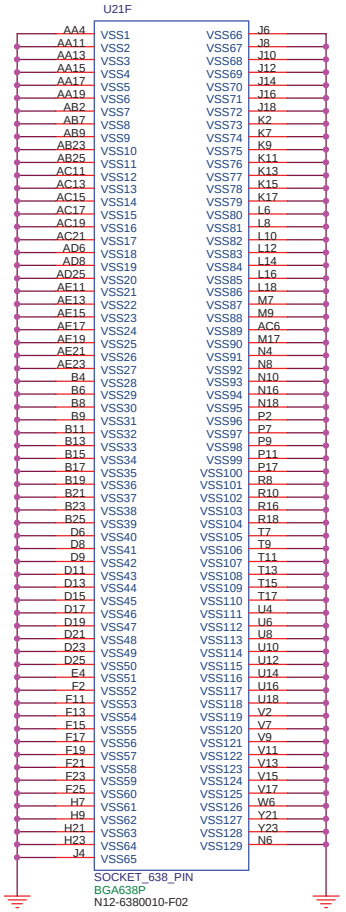
Close to CPU socket

SOCKET_638_PIN
BGA638P
N12-6380010-F02

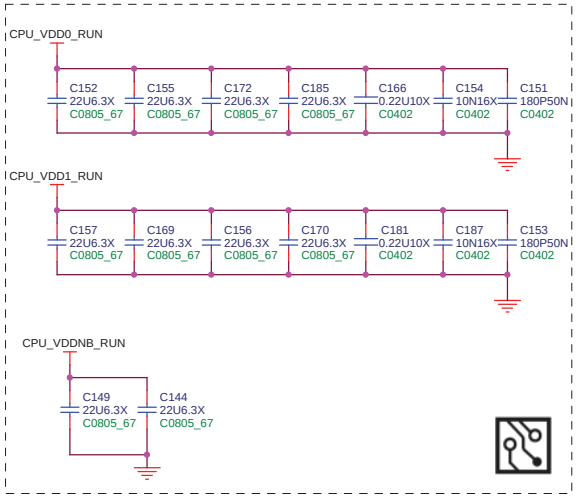
EMC1402
MSOP8_T
D0F-0140202-S32

MICRO-STAR INT'L CO.,LTD.	
Title	SOCKET S1G2 CTRL
Size: Custom	Document Number: MS-13331
Rev	10
Date: Friday, March 28, 2008	Sheet 7 of 55

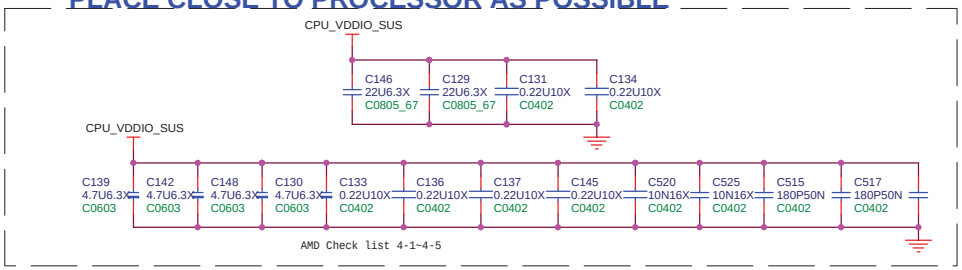


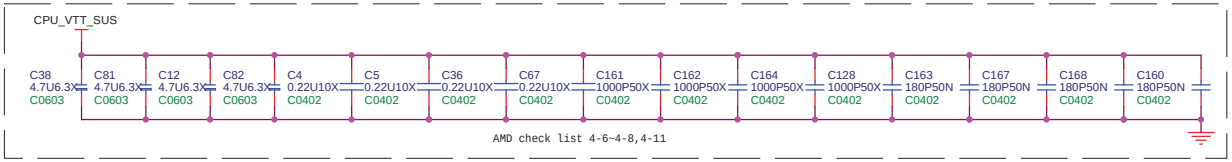


BOTTOMSIDE DECOUPLING



DECOUPLING BETWEEN PROCESSOR AND DIMMs
PLACE CLOSE TO PROCESSOR AS POSSIBLE





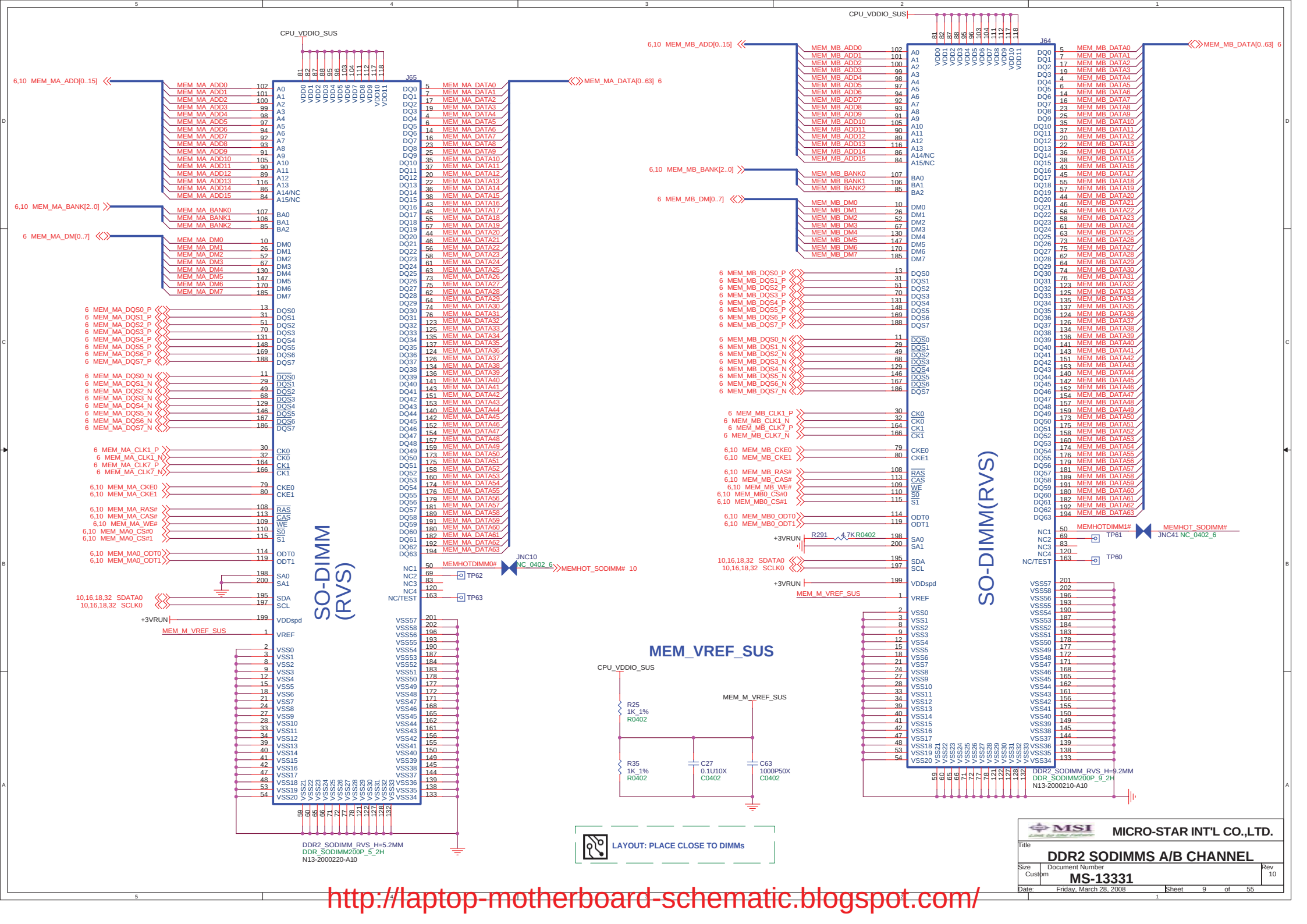
PROCESSOR POWER AND GROUND

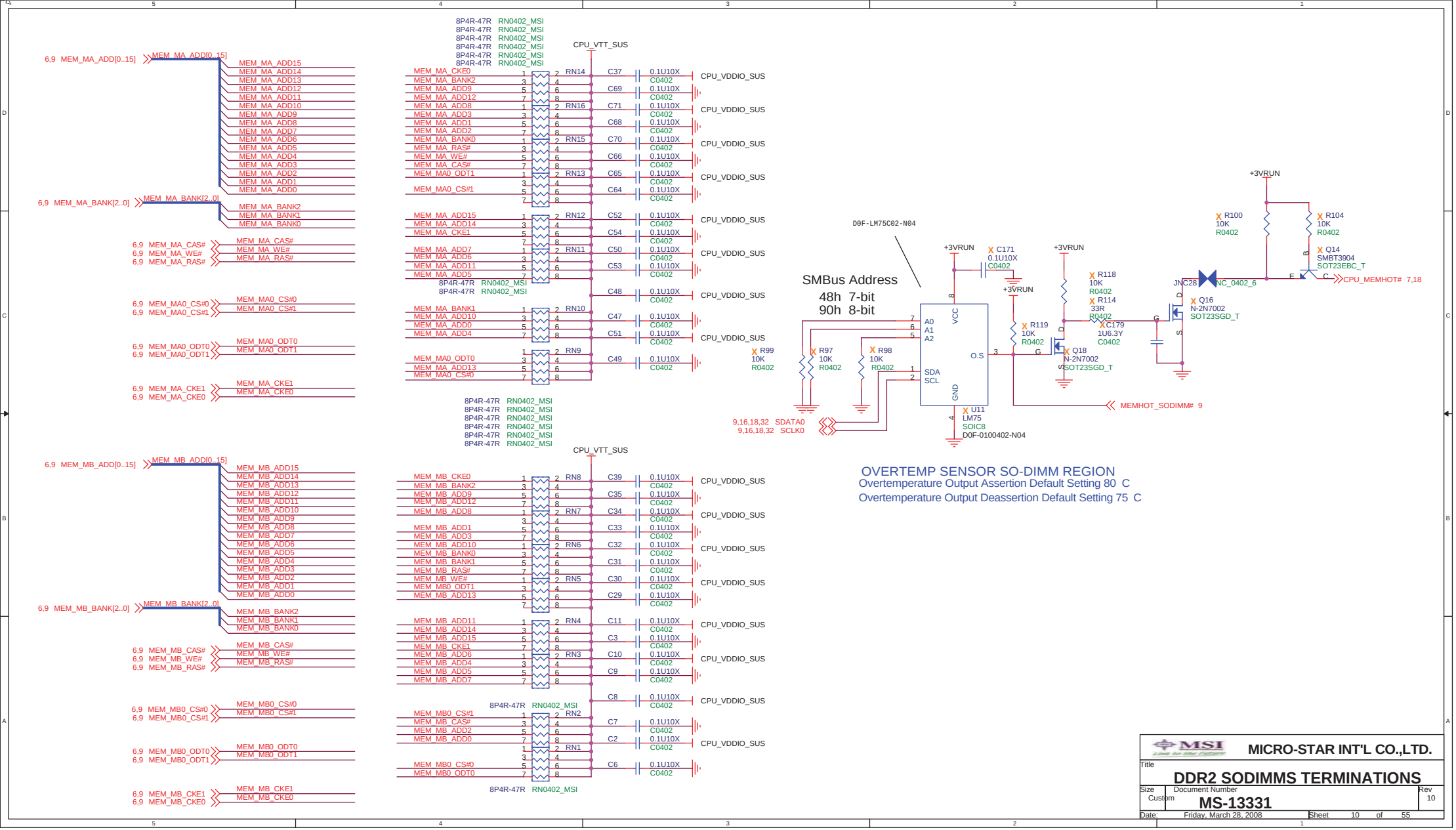
MICRO-STAR INT'L CO.,LTD.

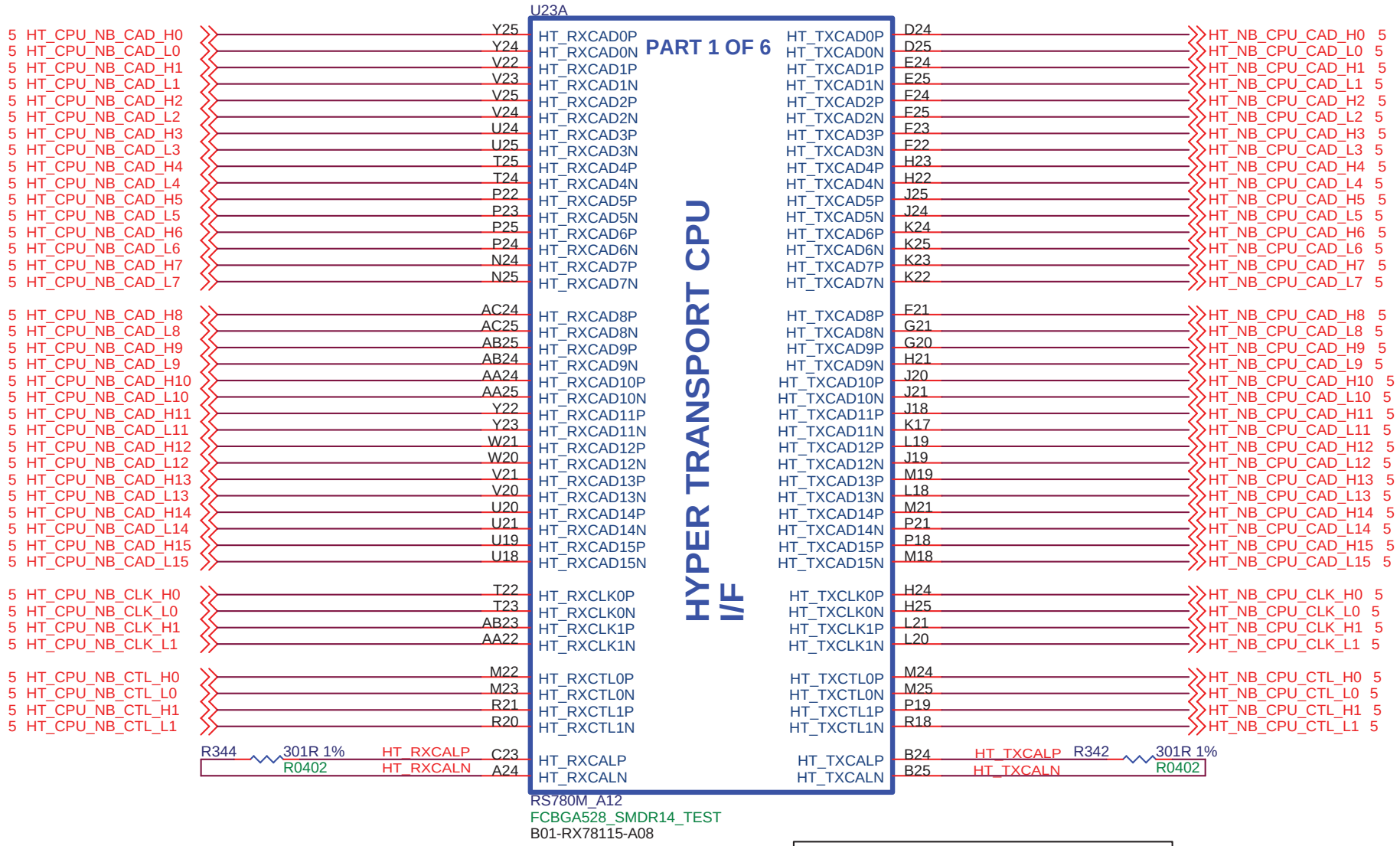
Title: SOCKET S1G2 PWR & GND

Size: Custom | Document Number: MS-13331 | Rev: 10

Date: Friday, March 28, 2008 | Sheet 8 of 55







1333 U23 = B01-RX78105-A08 (RX781)
1332 U23 = B01-RS78025-A08 (RS780M)
CroseFire U23 = B01-RS78025-A08 (RS780M)

B01-RS78025-A08 RS780M (A12)
B01-RS78065-A08 RS780MN (A13)
B01-RX78105-A08 RX781(A12)
B01-RX78115-A08 RX781(A13)

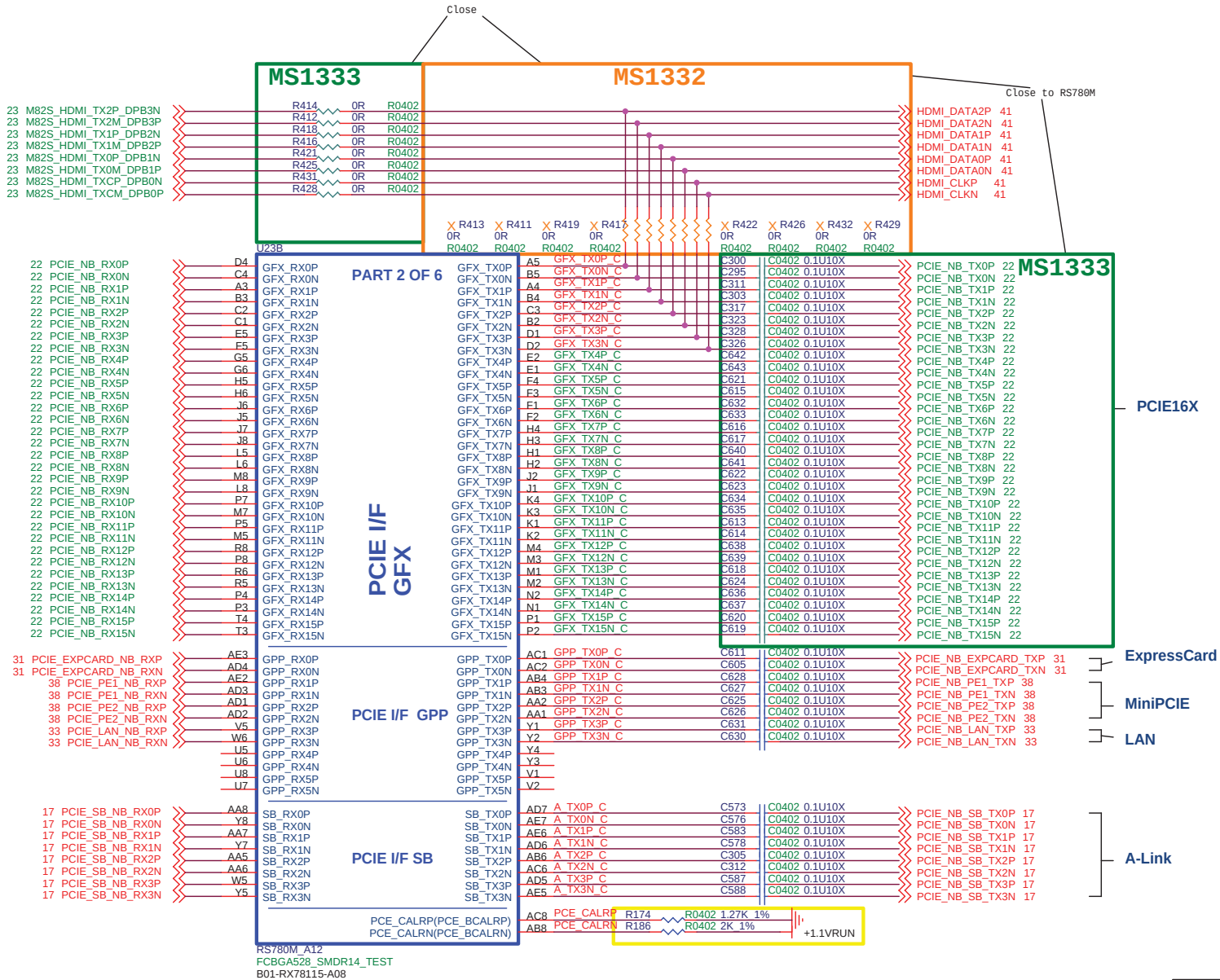
MSI MICRO-STAR INTERNATIONAL Link to the Future

MICRO-STAR INT'L CO.,LTD.

Title: RX/RS780 HT LINK I/F

Size	Document Number	Rev
A	MS-13331	10

Date: Friday, March 28, 2008 Sheet 11 of 55

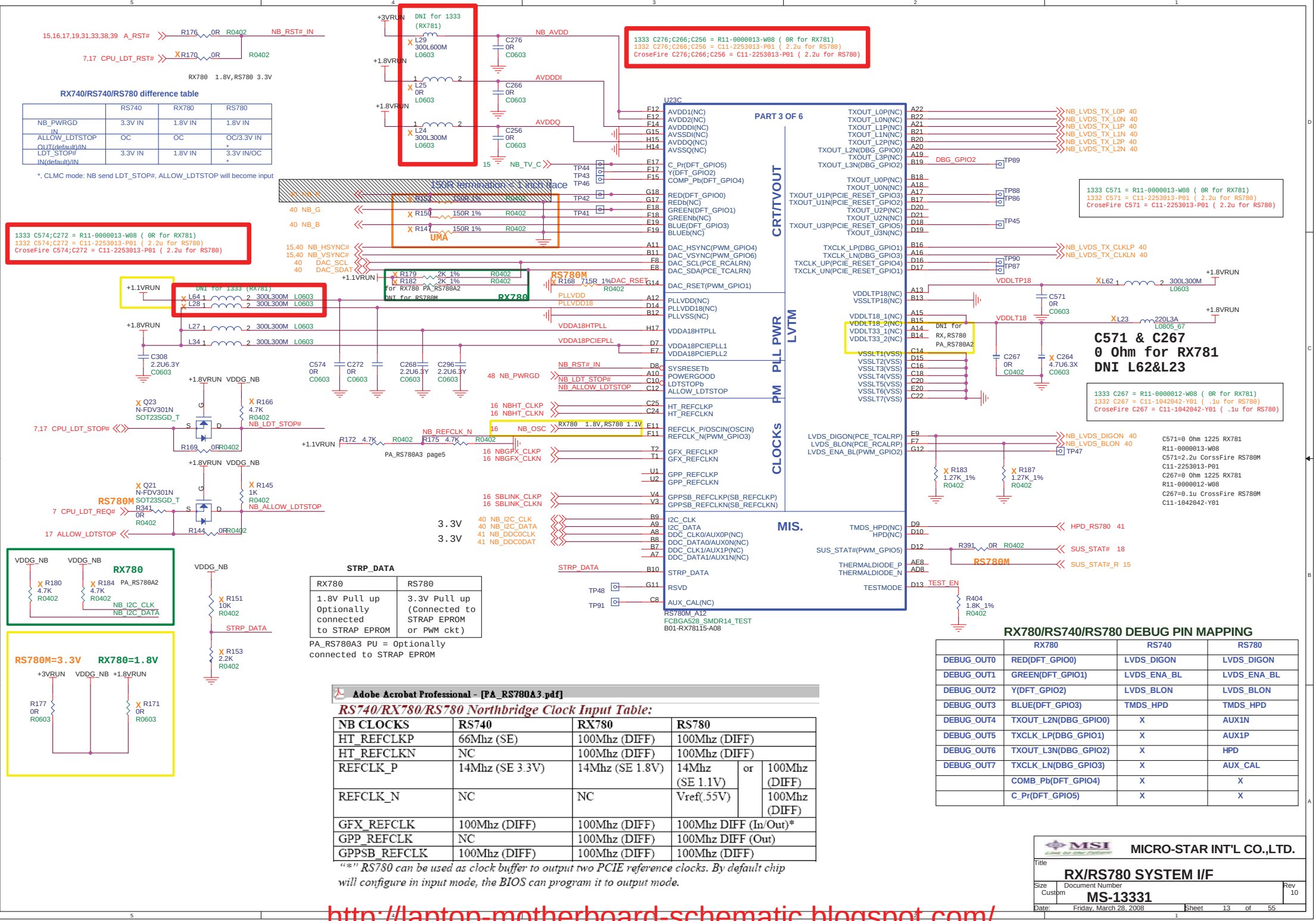


MICRO-STAR INT'L CO.,LTD.

Title: RX/RS780 PCI-E LINK&GPP

Size: B | Document Number: MS-13331 | Rev: 10

Date: Friday, March 28, 2008 | Sheet 12 of 55


RX740/RS740/RS780 difference table
RS740 RX780 RS780
NB_PWRGD IN 3.3V IN 1.8V IN 1.8V IN
ALLOW_LDTSTOP OUT(default)/IN OC OC OC/3.3V IN *
LDT_STOP# IN(default)/IN 3.3V IN 1.8V IN 3.3V IN/OC *
*, CLMC mode: NB send LDT_STOP#, ALLOW_LDTSTOP will become input
RX780 1.8V,RS780 3.3V
1333 C276;C266;C256 = R11-0000013-W08 (0R for RX781)
1332 C276;C266;C256 = C11-2253013-P01 (2.2u for RS780)
CroseFire C276;C266;C256 = C11-2253013-P01 (2.2u for RS780)
1333 C574;C272 = R11-0000013-W08 (0R for RX781)
1332 C574;C272 = C11-2253013-P01 (2.2u for RS780)
CroseFire C574;C272 = C11-2253013-P01 (2.2u for RS780)
150R termination < 1 inch trace
UMA
RS780M
RX780
PART 3 OF 6
U23C
CRT/TVOUT
PLL PWR
LVTM
PM
CLOCKS
MIS.
1333 C571 = R11-0000013-W08 (0R for RX781)
1332 C571 = C11-2253013-P01 (2.2u for RS780)
CroseFire C571 = C11-2253013-P01 (2.2u for RS780)
C571 & C267
0 Ohm for RX781
DNI L62&L23
1333 C267 = R11-0000012-W08 (0R for RX781)
1332 C267 = C11-1042042-Y01 (.1u for RS780)
CroseFire C267 = C11-1042042-Y01 (.1u for RS780)
C571=0 Ohm 1225 RX781
R11-0000013-W08
C571=2.2u CorssFire RS780M
C11-2253013-P01
C267=0 Ohm 1225 RX781
R11-0000012-W08
C267=0.1u CrossFire RS780M
C11-1042042-Y01
STRP_DATA
RX780 RS780
1.8V Pull up Optionally connected to STRAP EPROM
3.3V Pull up (Connected to STRAP EPROM or PWM ckt)
PA_RS780A3 PU = Optionally connected to STRAP EPROM
RS780M=3.3V RX780=1.8V
RX780/RS740/RS780 DEBUG PIN MAPPING
DEBUG_OUT0 RED(DFT_GPIO0) LVDS_DIGON LVDS_DIGON
DEBUG_OUT1 GREEN(DFT_GPIO1) LVDS_ENA_BL LVDS_ENA_BL
DEBUG_OUT2 Y(DFT_GPIO2) LVDS_BLON LVDS_BLON
DEBUG_OUT3 BLUE(DFT_GPIO3) TMDS_HPD TMDS_HPD
DEBUG_OUT4 TXOUT_L2N(DBG_GPIO0) X AUX1N
DEBUG_OUT5 TXCLK_LP(DBG_GPIO1) X AUX1P
DEBUG_OUT6 TXOUT_L3N(DBG_GPIO2) X HPD
DEBUG_OUT7 TXCLK_LN(DBG_GPIO3) X AUX_CAL
COMB_Pb(DFT_GPIO4) X X
C_Pr(DFT_GPIO5) X X
Adobe Acrobat Professional - [PA_RS780A3.pdf]
RS740/RX780/RS780 Northbridge Clock Input Table:
NB CLOCKS RS740 RX780 RS780
HT_REFCLKP 66Mhz (SE) 100Mhz (DIFF) 100Mhz (DIFF)
HT_REFCLKN NC 100Mhz (DIFF) 100Mhz (DIFF)
REFCLK_P 14Mhz (SE 3.3V) 14Mhz (SE 1.8V) 14Mhz (SE 1.1V) or 100Mhz (DIFF)
REFCLK_N NC NC Vref(.55V) 100Mhz (DIFF)
GFX_REFCLK 100Mhz (DIFF) 100Mhz (DIFF) 100Mhz DIFF (In/Out)*
GPP_REFCLK NC 100Mhz (DIFF) 100Mhz DIFF (Out)
GPPSB_REFCLK 100Mhz (DIFF) 100Mhz (DIFF) 100Mhz (DIFF)
"*" RS780 can be used as clock buffer to output two PCIE reference clocks. By default chip will configure in input mode, the BIOS can program it to output mode.
MICRO-STAR INT'L CO.,LTD.
RX/RS780 SYSTEM I/F
MS-13331
Rev 10
Date: Friday, March 28, 2008
Sheet 13 of 55
http://laptop-motherboard-schematic.blogspot.com/

RS740/RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVDD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDDG18	+1.8V	+1.8V	+1.8V	PLLVDD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVDD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V/1.5V	NC	+1.8V/1.5V	VDDLTP18	+1.8V	NC	+1.8V
VDDG33	+3.3V	NC	+3.3V	VDDLT18	+1.8V	NC	+1.8V
IOPLLVDD18	+1.8V	NC	+1.8V	VDDLT33	+3.3V	NC	NC

U23F
RS780M_A12
FCBGA528_SMDR14_TEST
B01-RX78115-A08

PART 6/6
GROUND

NB_VDD_MUX=>+1.1VRUN

U23E
PART 5/6
POWER
RS780M_A12
FCBGA528_SMDR14_TEST
B01-RX78115-A08

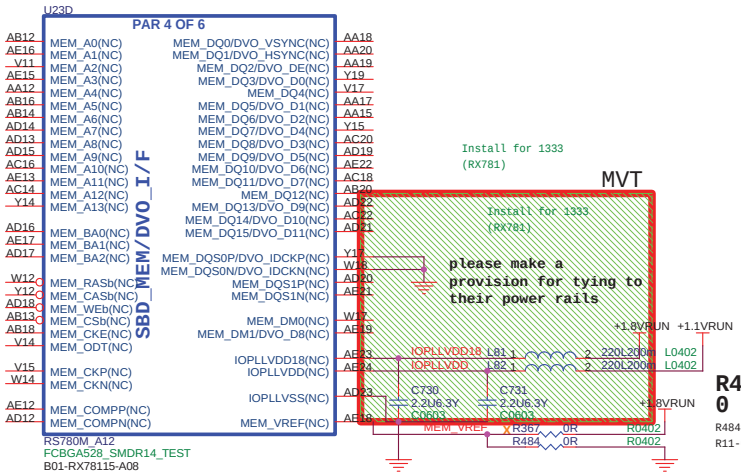
Isolated power for side-port memory or DVO interface

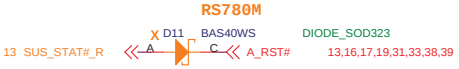
1.8V power for side port memory or DVO interface

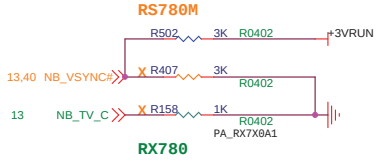
1333 C570 = R11-0000013-W08 (install 0R for RX781)

C278
0 Ohm for RX781
C578=0 Ohm 1225 RX781
R11-0000012-W08
C578=0.1u CrossFire RS780M
C11-1042042-Y01 (DNI)

MICRO-STAR INT'L CO.,LTD.
Title: RX/RS780 POWER & GND
Size: Custom | Document Number: MS-13331 | Rev: 10
Date: Friday, March 28, 2008 | Sheet 14 of 55







RS740/RX780/RS780: LOAD_EEPROM_STRAPS

```
Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use
default values if not connected
RX780: pin DFT_GPIO1
RS780: pin SUS_STAT#
```

STRAP_DEBUG_BUS_GPIO_ENABLEb

```
Enables the Test Debug Bus using GPIO.
1 : Enable (RX780, RS780)
0 : Disable (RX780, RS780)
PIN: RX780-->NB_TV_C (pin DFT_GPIO5) ; RS780--> VSYNC# (pin VSYNC)
```

RX740: DFT_GPIO[4:2]: STRAP_PCIE_GPP_CFG[2:0]

```
These pin straps are used to configure PCI-E GPP mode.
000 : 00001
001 : 00010
010 : 01011
011 : 00100
100 : 01010
101 : 01100
111 : 01011
```

RX780: STRAP_PCIE_GPP_CFG[2:0] (Pins:RX780_DFT_GPIO[4:2])

```
111: 1-1-1-1-1-1 Mode L default
110: 1-1-1-1-1-1 Mode L
101: 2-0-2-0-2-0 Mode C2
100: 2-0-2-0-1-1 Mode K
011: 2-0-1-1-1-1 Mode E
010: 1-1-1-1-1-1 Mode L
001: 4-0-0-0-1-1 Mode C
000: 4-0-0-0-2-0 Mode B
```

RS780: STRAP_PCIE_GPP_CFG[2:0] (configurable thru register settings only)

```
1-1-1-1-1-1 Mode L default
1-1-1-1-1-1 Mode L
2-0-2-0-2-0 Mode C2
2-0-2-0-1-1 Mode K
2-0-1-1-1-1 Mode E
1-1-1-1-1-1 Mode L
4-0-0-0-1-1 Mode C
4-0-0-0-2-0 Mode B
```

Adobe Acrobat Professional - [PA_RS780A3.pdf]

RS740/RX780/RS780 Straps:

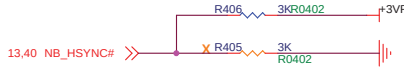
STRAP Name	RS740	RX780	RS780	Comments
Load EPROM Straps	DFT_GPIO1	DFT_GPIO1	SUS_STAT#	Load Straps from EPROM connected through Strap and I2C_Clk pins
Strap_Debug_Bus_EN#	DFT_GPIO5	DFT_GPIO5	VSYNC	Enables debug bus over Memory I/O pins or/and GPIOs
GPPSB_LINK_Config	DFT_GPIO[4:2]	DFT_GPIO[4:2]	Register settings only	Configures A-Link and GPP
Srap_Debug_Bus_PCIE_EN#	Not applicable	DFT_GPIO0	Register settings only	Enable Debug bus over x16 PCIE interface
SidePort_EN#	DFT_GPIO0	Not applicable	HSYNC	Enables side port

Adobe Acrobat Professional - [42221_rs780m_ds_nda_0.02.pdf]

Pin Name	Type	Power Domain	Ground Domain	Functional Description
SUS_STAT#	I	VDD33	VSS	Suspend Status. SUS_STAT# from the south bridge is connected to the pin to gate the sideport memory I/Os while power is ramping up and the POWERGOOD signal to the RS780M is still low.

RS740/RX780/RS780: STRAP_SIDE-PORT MEMORY ENABLE

```
Enables Side port memory
1 : Disable (RS740/RS780)
0 : Enable (RS740/RS780)
RS780: pin HSYNC
RX780: Not Applicable
```



Adobe Acrobat Professional - [42221_rs780m_ds_nda_0.02.pdf]

Pin Name	Type	Power Domain	Ground Domain	Integrated Termination	Functional Description
DAC_HSYNC	A-O	VDD33	VSS	50kΩ programmable: PU/PD/none	Display Horizontal Sync
DAC_VSYNC	A-O	VDD33	VSS	50kΩ programmable: PU/PD/none	Display Vertical Sync

DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLEb

```
Enables Test debug bus over PCIE bus
(Applicable to RX780 & RS780 Only)
1. Disable (can be enabled thru nbcfg register)
0 : Enable
RX780: pin DFT_GPIO0
RS780: configurable thru register setting only
```

DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLEb

```
RX780: Enables the Test Debug Bus using PCIE bus
1 : Disable ( Can still be enabled using nbcfg register access )
0 : Enable

RS740/RS780: Enables Side port memory ( RS780 use HSYNC#)
1.  Disable (RS740)  Enable (RS780)
0 : Enable (RS740)   Disable(RS780)
```

Adobe Acrobat Professional - [42223_rx780_ds_nda_0.02.pdf]

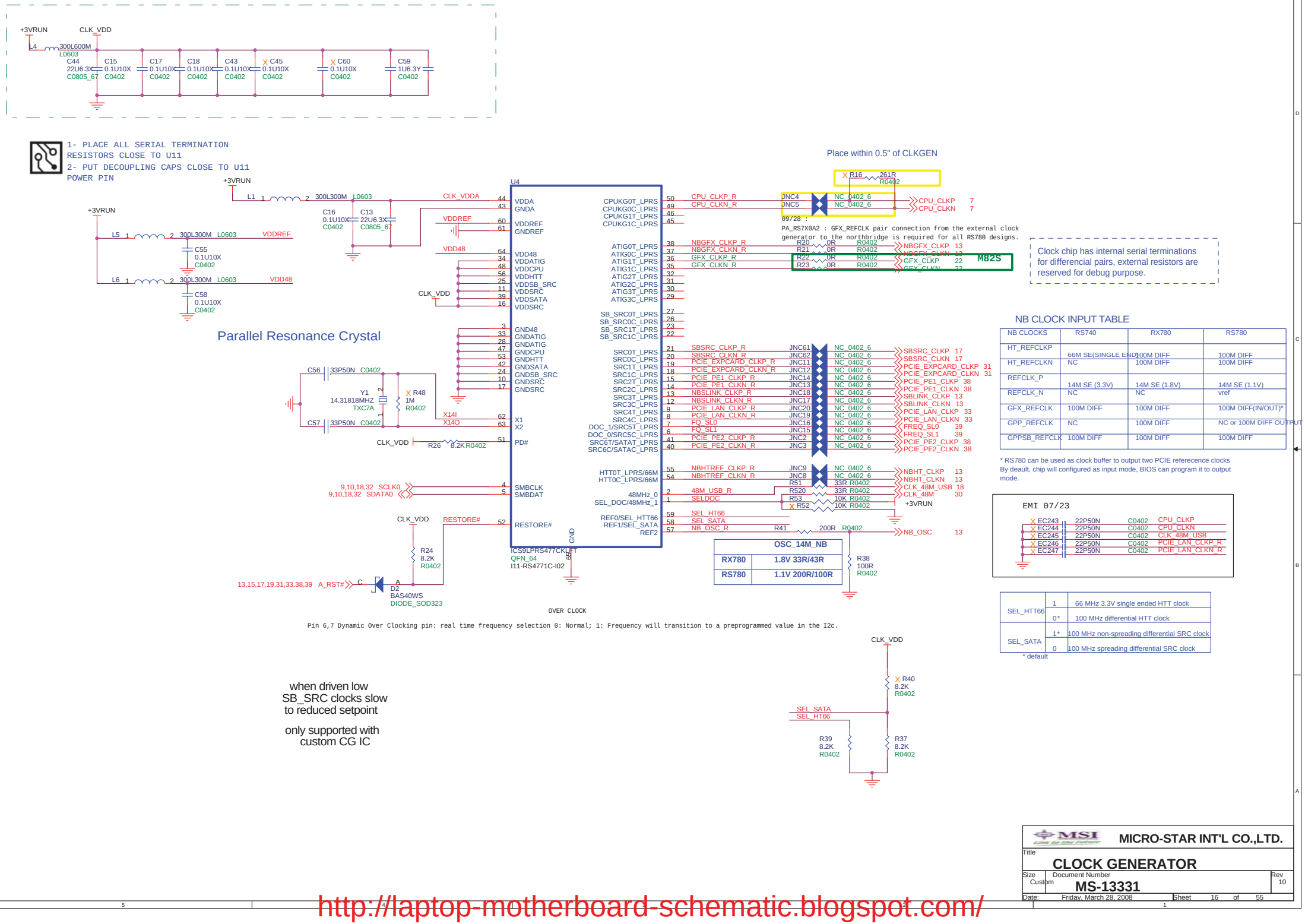
Pin Name	Type	Power Domain	Ground Domain	Integrated Termination	Functional Description
DFT_GPIO[5:0]	I/O	VDD18	VSS	Pull Up	Outputs for DFT TESTMODE. The pins cannot be used for general GPIO functions.

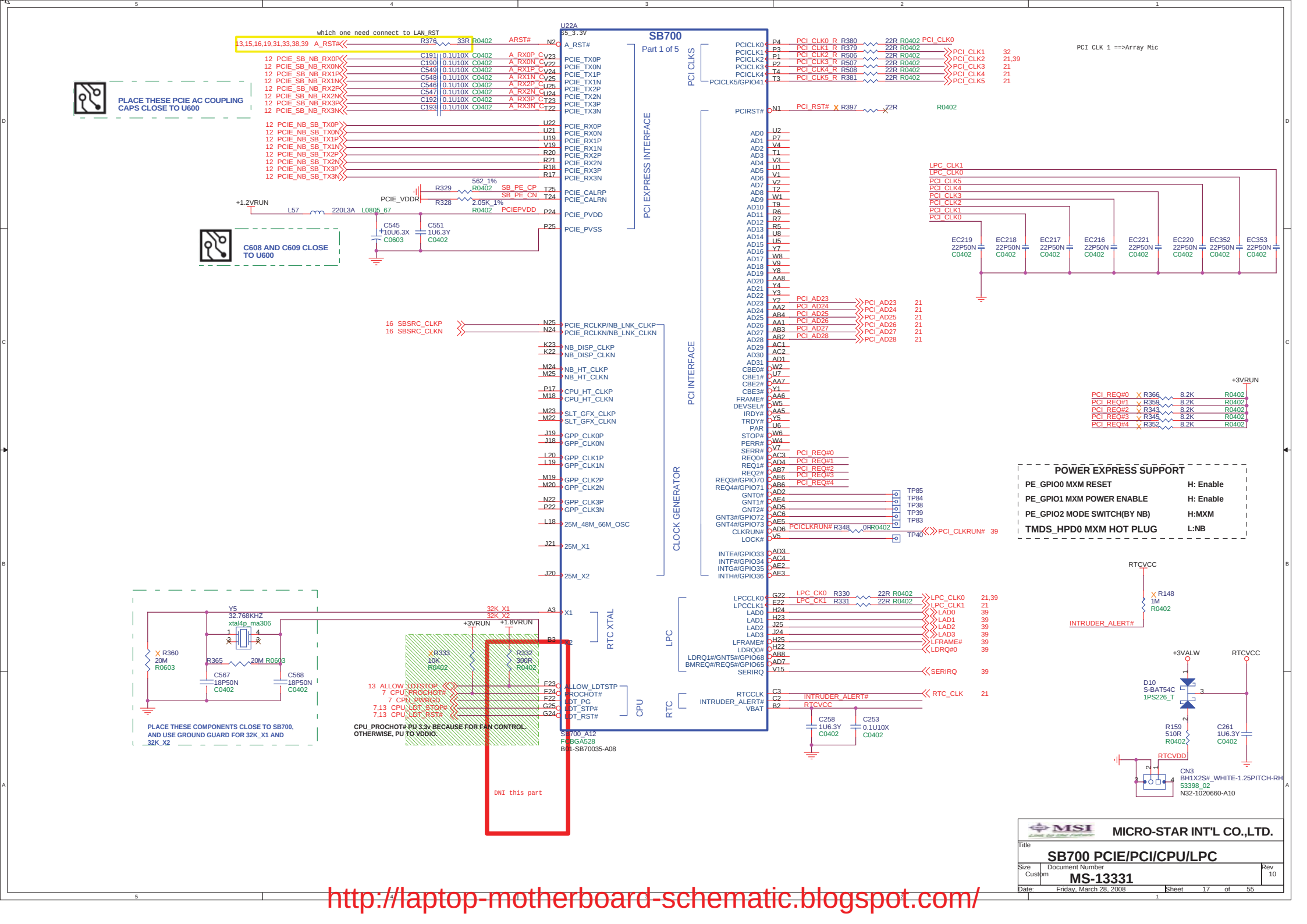
MSI MICRO-STAR INT'L CO.,LTD.

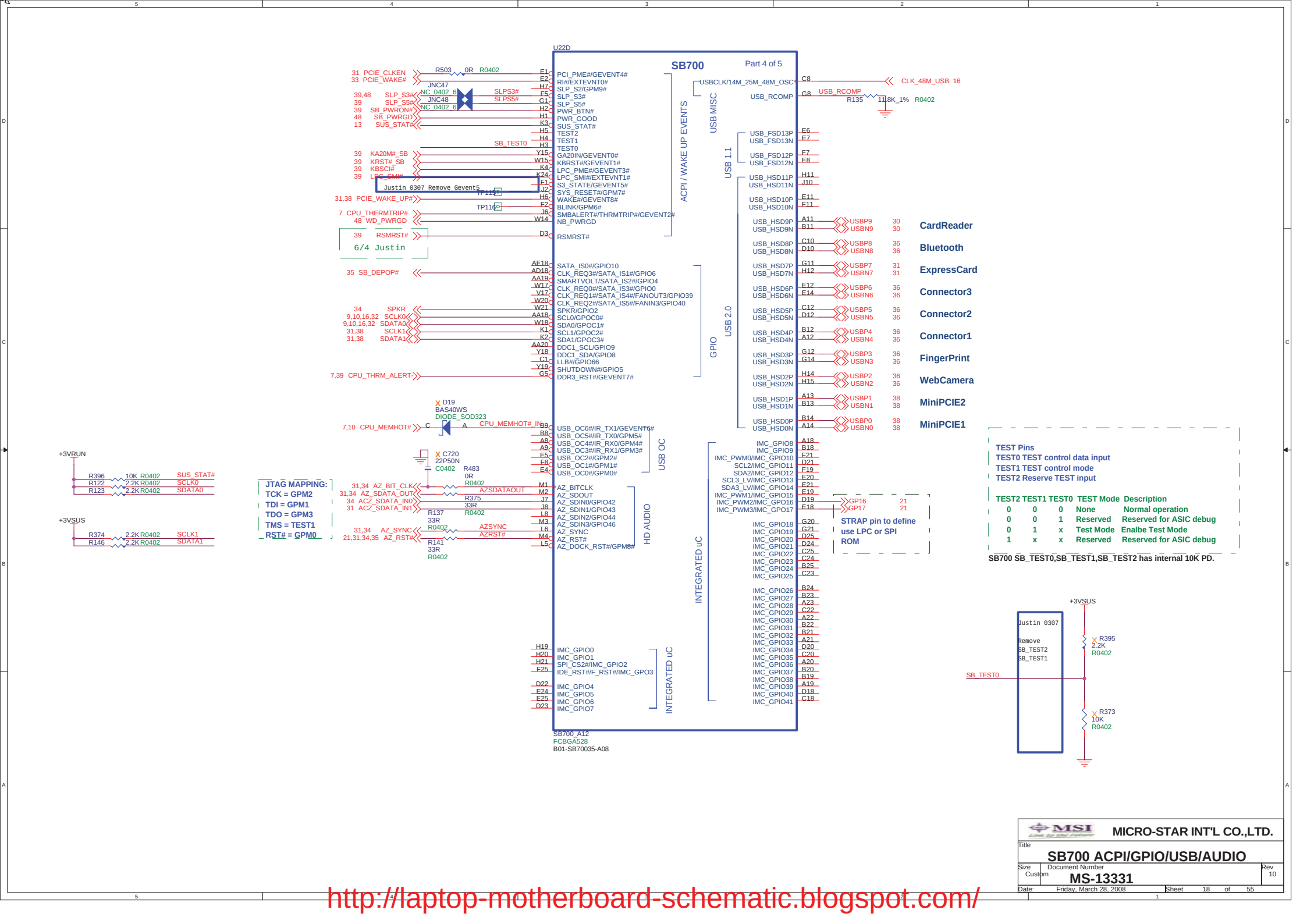
Title: RX/RS780-DVO

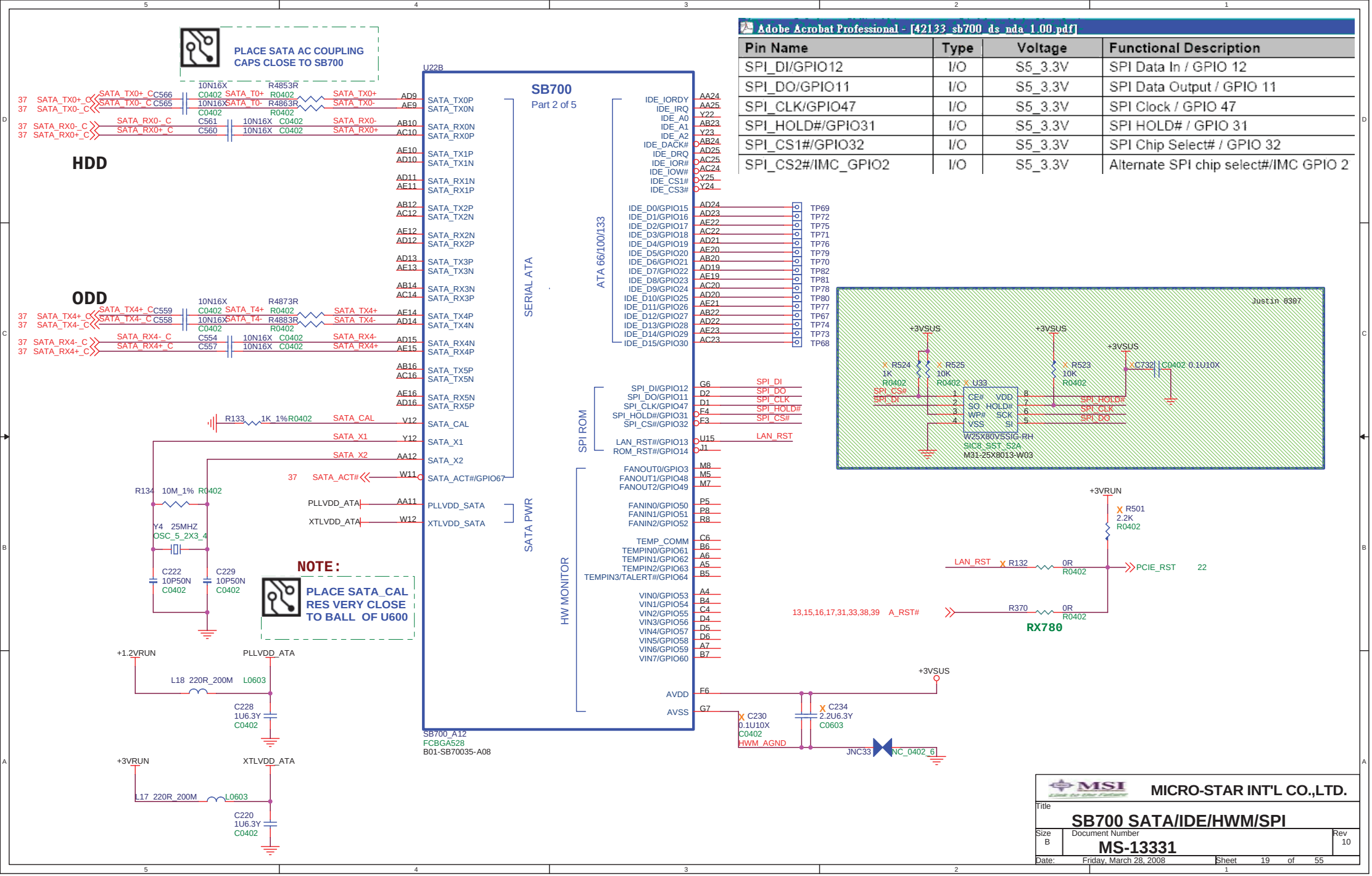
Size: Custom | Document Number: MS-13331 | Rev: 10

Date: Friday, March 28, 2008 | Sheet 15 of 55









Adobe Acrobat Professional - [42133_sb700_ds_nda_1.00.pdf]

Pin Name	Type	Voltage	Functional Description
SPI_DI/GPIO12	I/O	S5_3.3V	SPI Data In / GPIO 12
SPI_DO/GPIO11	I/O	S5_3.3V	SPI Data Output / GPIO 11
SPI_CLK/GPIO47	I/O	S5_3.3V	SPI Clock / GPIO 47
SPI_HOLD#/GPIO31	I/O	S5_3.3V	SPI HOLD# / GPIO 31
SPI_CS1#/GPIO32	I/O	S5_3.3V	SPI Chip Select# / GPIO 32
SPI_CS2#/IMC_GPIO2	I/O	S5_3.3V	Alternate SPI chip select#/IMC GPIO 2

MICRO-STAR INT'L CO.,LTD.

Title: SB700 SATA/IDE/HWM/SPI

Size: B | Document Number: MS-13331 | Rev: 10

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PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

For SB700_A12

X R136 0R R0603

+1.2VRUN +1.2VSUS R131 0R R0603

SB_VDD

U22C

SB700

Part 3 of 5

VDD33_18
+1.8V : FLASH MEMORY MODE(DEFAULT)
+3.3V : IDE MODE

Please make a provision for tying to +3.3V_S0

POWER

PCI/GPIO I/O
CORE S0
IDE/FLSH I/O
CLKGEN I/O
A-LINK I/O
3.3V_S5 I/O
SATA I/O
CORE S5
USB I/O
PLL

+1.2V_CKVDD

PCIE_VDDR

AVDD_SATA

AVDD_USB

+3VSUS

+5VRUN

+3VRUN

+1.2VSUS

+3.3V_AVDDC

+1.2V_CKVDD

AVDDCK_3.3V

AVDDCK_1.2V

SB700_A12
FCBGA528
B01-SB70035-A08

U22E

SB700

GROUND

Part 5 of 5

SB700_A12
FCBGA528
B01-SB70035-A08

MSI MICRO-STAR INT'L CO.,LTD.

Title: SB700 POWER & GND

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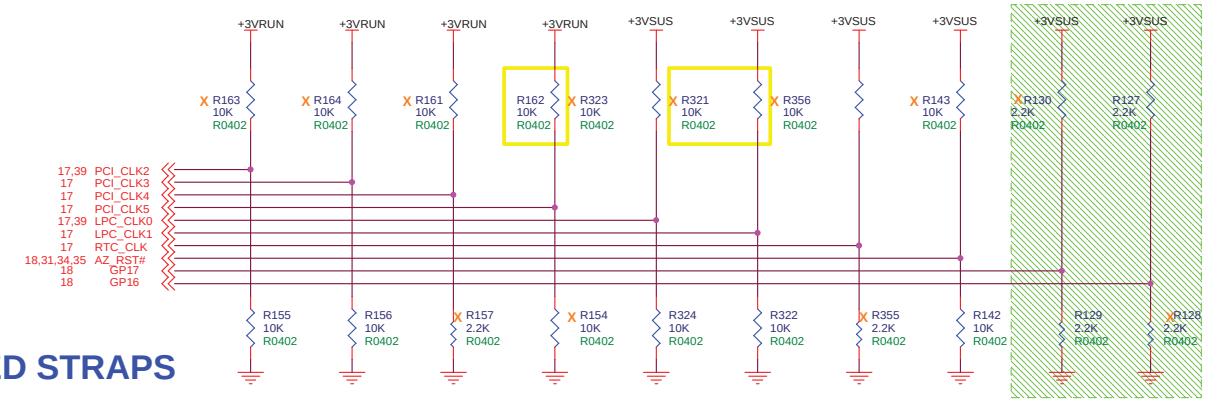
NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

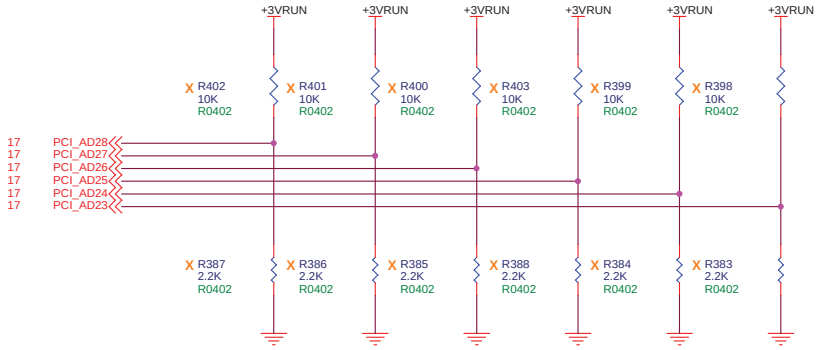


REQUIRED STRAPS

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST	GP17 GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	EC ENABLED	CLKGEN ENABLED	INTERNAL RTC DEFAULT	ENABLE PCI MEM BOOT	H,H = Reserved L,H = LPC ROM (DEFAULT) H,L = SPI ROM L,L = FWH ROM
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			EC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI MEM BOOT DEFAULT	

DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



Use 2.2K PD.

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

MICRO-STAR INT'L CO.,LTD.

Title: SB700 STRAPS

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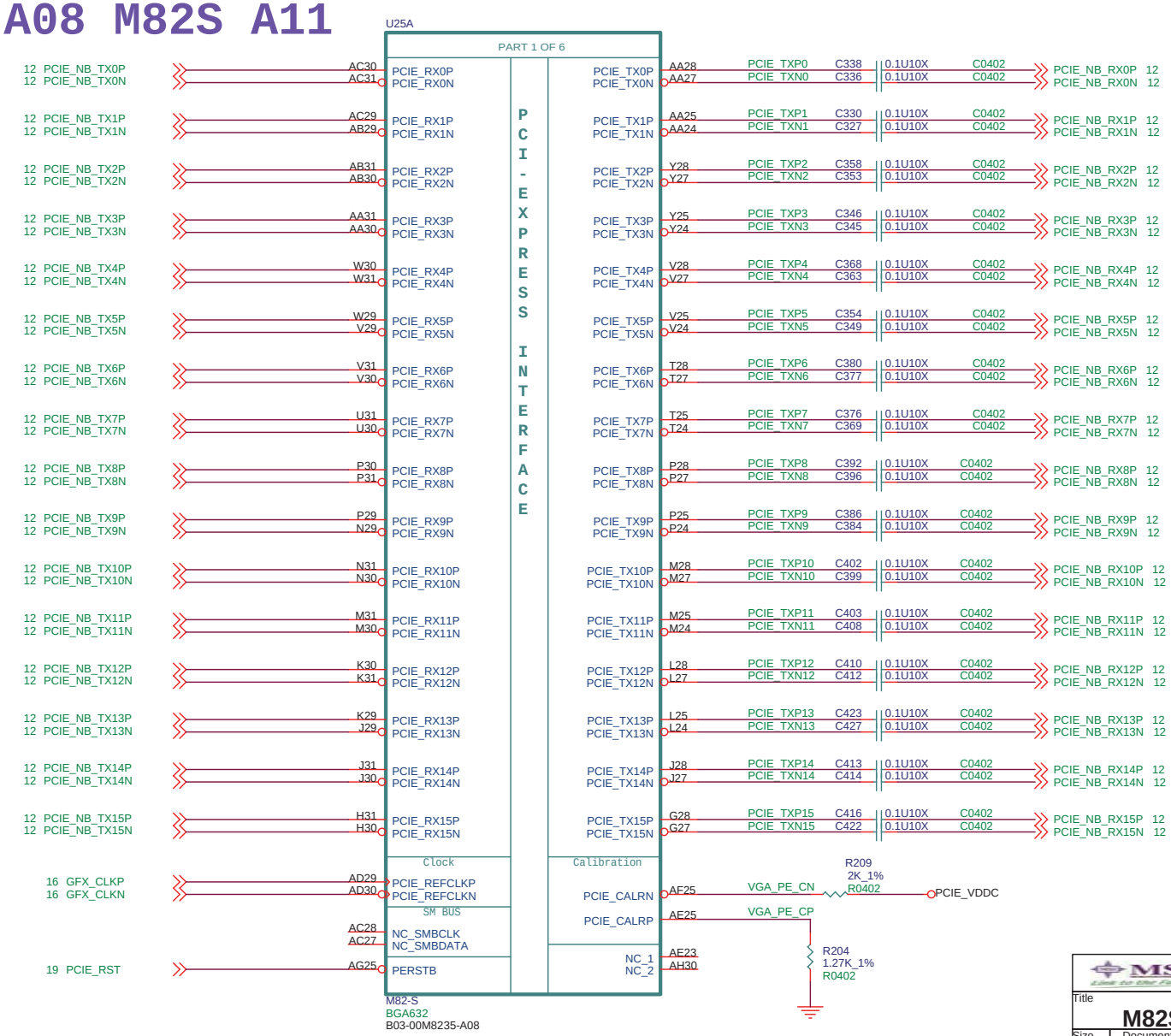
B03-00M8235-A08 M82-SCE A11
B03-00M8205-A08 M82S A11



MICRO-STAR INT'L CO.,LTD.

Title: M82S PCI-E LINK

Size: B | Document Number: MS-13331 | Rev: 10

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DVALID
1.)Transport stream data valid input or general purpose I/O
Note: Can be left unconnected if not used.
2.)This signals is also used for video capture and as an initialization pin strap.
3.)Internal use only. Other logic must not affect this signal during RESET.

PSYNC VGA_DIS(Internal pulldown)
VGA Disable determines whether or not the card will be recognized as the system's VGA controller (via the SUBCLASS field in the PCI configuration space).
0 – VGA Controller capacity enabled
1 – The device will not be recognized as the system's VGA controller

THE PINS WITH TEST POINTS ARE REQUIRED TO BE ACCESSIBLE FOR DEBUG AND BOUNDRY SCAN PURPOSES USING TEST POINT VIAS IF UNUSED OR COMPONENT PADS

ENSURE DEBUG_ACCESS STRAP IS ALSO ACCESSIBLE
SEE CONFIG STRAPPING PAGE

ACCESS TO ATI DEBUG PORT IS MANDATORY ON INITIAL PROTOTYPE DESIGNS

GPIO_17_THERMAL_INT
Thermal monitor interrupt.
GPIO_17_THERMAL_INT is used for ASIC temperature control. It is connected to the ALERTb signal of the thermal monitor which measures the temperature of the ASIC. If the ASIC temperature falls outside a defined range, the ALERTb signal is asserted. Low level on GPIO_17_THERMAL_INT causes M74/M72 to generate an interrupt (the polarity of this interrupt is programmable – the default is active low). Software can then activate the implemented temperature control scheme.

Power Control signals control the core voltage regulator.
At Reset, these signals will be inputs with weak internal pull-down resistors.
VBIOS can define these signals to be either 3.3V outputs or open drain outputs.
The output state (high/low) of these signals is programmable for each PowerPlay state.

Back Bias (BB) control:
When GPIO_21_BB_EN = 0V then back bias is disabled on the PCB (ie BPP=VDDC and BBN=VSS).
When GIO_21_BB_EN = 3.3V then back bias is enabled on the PCB.
Can function as a GPIO if not required for BB control.

GPIO_22_ROMCSB
BIOS_ROM_EN
Enable external BIOS ROM device
0 - Disable external BIOS ROM device
1 - Enable external BIOS ROM device

VREFG VOLTAGE DIVIDER IS (VREFG = VDDR4,5(1.8V) / 3 = .6V)

PLACE VREF DIVIDER AND CAP CLOSE TO ASIC

GPIO_23_CLKREQB DRIVES LOW DURING RESET

U25B
PART 2 OF 6
M82-S
BGA632
B03-00M8235-A08

INTEGRATED TMDS/DP PORT
EXT TMDS DVO
GENERAL PURPOSE I/O
DAC1 / CRT
DAC2 (TV/CRT2)
SERIAL BUSES
PLL & XTAL
TEST
THERMAL

HDMI

CRT

WITH M8x ASIC
INSTALL M8x STRAP RESISTORS AND
DO NOT INSTALL M7x STRAP RESISTORS

IF HOT PLUG DETECT IS NOT REQUIRED
REMOVE ALL THIS LOGIC EXCEPT
FOR 100K PULL DOWN

OPTIONAL 0 OHM STRAPS TO GROUND FOR RB,GB,BB AND R2B,G2B,B2B
SEE DAC1_RGB AND DAC2_RGB SHEETS

PLACE OR RESISTORS CLOSE TO ASIC

Close to M82S
Cap close to thermal sensor
M82S
EMC1402 MSOP8_T

3.3V TO 5V LEVEL SHIFT LOGIC REQUIRED
IF DDC1,DDC2 USED ON M8x OR DDC1,DDC2,DDC3 USED ON M7x
DDC3,DDC4 ARE 5V TOLERANT ON M8x

CRT	3.3V	
LVDS	3.3V	
HDMI	5V	

MICRO-STAR INT'L CO.,LTD.

Title: M82S I/O
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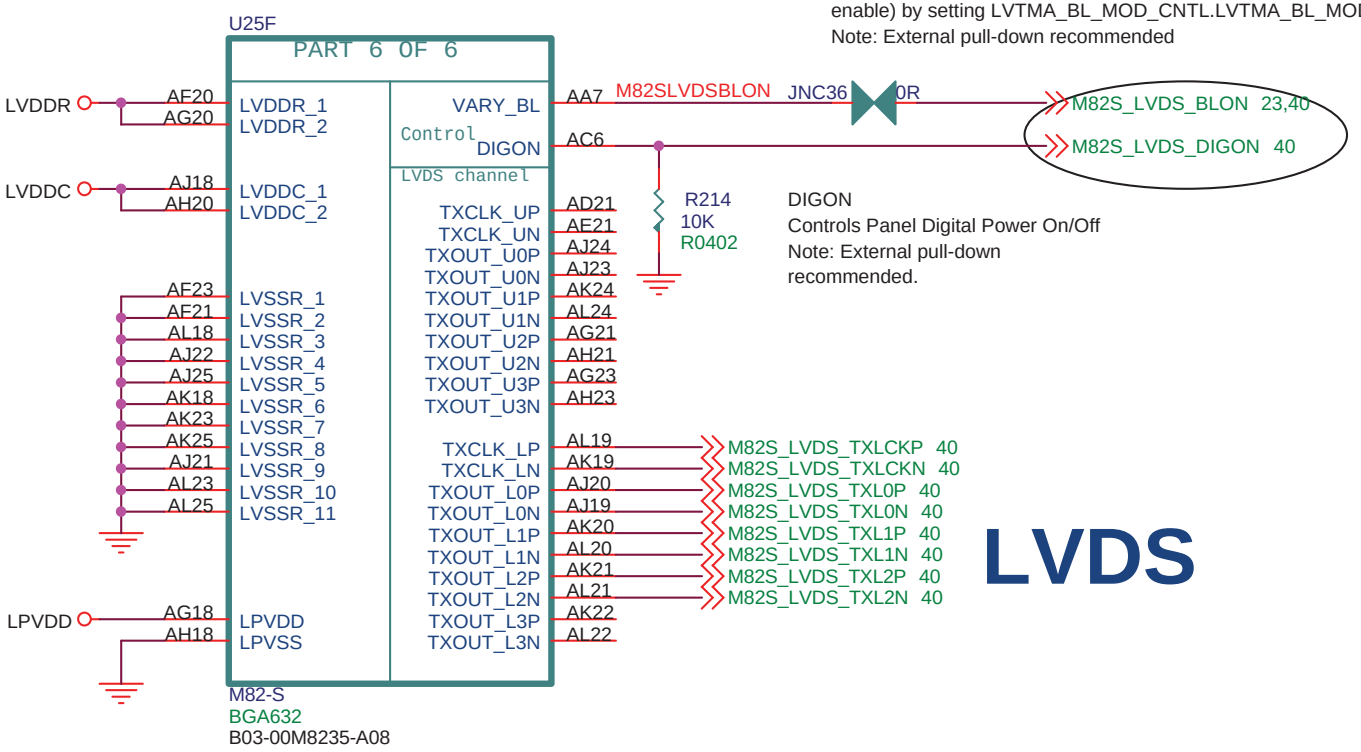
VARY_BL
LCD PWM (Pulse Width Modulated) output to adjust LCD brightness. Active high.
LVTMA_BL_MOD_CNTL.LVTMA_BL_MOD_LEVEL can be used to control the backlight level by means of pulse width modulation.
Alternatively, VARY_BL can be used to control backlight on/off (backlight enable) by setting LVTMA_BL_MOD_CNTL.LVTMA_BL_MOD_EN = 0.
Note: External pull-down recommended



DIGON
Controls Panel Digital Power On/Off
Note: External pull-down recommended.

LVDS

MICRO-STAR INT'L CO.,LTD.

Title: M82S LVDS

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U25E

Part 5 of 6

PCI-Express GND

PCIE_VSS_1 … PCIE_VSS_32 (AA26, AA29, AC26, AD31, AE29, AE30, AE31, F28, G26, G29, G30, G31, H29, J25, J26, L26, L29, L30, L31, M26, M29, P26, R29, R30, R31, T26, U29, V26, Y26, Y29, Y30, Y31)

VSS_1 … VSS_32 (A13, A2, C18, A24, A30, AA1, AA11, AA14, AA17, AA20, AA6, AC2, AC7, AE3, AL4, AD14, AF12, AF14, AD16, AD18, AE6, AG2, AE9, AH25, AK1, AK31, AJ6, AL2, AL30, B1, C13)

VSS_33 … VSS_102 (B25, J8, B5, D11, C17, C22, C27, D29, C3, C6, D3, D28, F29, D4, F11, F12, F14, F16, F18, F20, F21, F23, F25, F7, F9, G3, G6, H23, J3, J4, J6, K1, L12, L15, L18, L21, L6, M11, M14, M17, M20, M6, P12, P15, P18, P21, P6, AC21, R14, R17, R20, T6, U1, U12, U15, U18, U21, AE20, V14, V17, V20, P2, V6, W2, Y12, Y15, Y18, Y21, Y6, M9)

CORE GND

M82-S
BGA632
B03-00M8235-A08

U25D

PART 4 OF 6

1.8VGA

C415 10U6.3X C0603
C420 10U6.3X C0603
C419 10U6.3X C0603
C418 10U6.3X C0603

C393 1U6.3Y C0402
C425 1U6.3Y C0402
C365 1U6.3Y C0402
C406 1U6.3Y C0402

C434 1U6.3Y C0402
C400 1U6.3Y C0402
C433 1U6.3Y C0402
C340 1U6.3Y C0402

VDDR1_1 … VDDR1_18 (A15, A22, A28, A4, A8, B8, C9, D1, H1, H11, H12, H14, H16, H18, H20, H21, B31, M1)

VDD_CT_1 … VDD_CT_8 (AA9, Y9, V9, T9, J11, J20, J21, L9)

VDD_CT

3.3V_DELAY

(3.3V @ 50MA VDDR3)

C579 10U6.3X C0603
C352 1U6.3Y C0402
C347 1U6.3Y C0402
C355 1U6.3Y C0402

VDDR3_1 … VDDR3_4 (AC18, AC16, AC14, AC12)

1.8VGA

L78 300L300M L0603

C645 0.1U10X C0402
C417 1U6.3Y C0402

+VDDR4

VDDR4_1, VDDR4_2 (AF1, AF2)

VDDR5_1, VDDR5_2 (AE1, AE2)

+VDDR5

L79 300L300M L0603

C429 10U6.3X C0603
C397 1U6.3Y C0402
C409 1U6.3Y C0402

RSVD_1 … RSVD_4 (M2, M3, L4, AD11)

VDD_MEM_CLK0
VDD_MEM_CLK1

VDDRH_1, VDDRH_2 (A10, A19)

VSSRH_1, VSSRH_2 (B10, B19)

-BBN
VSS-1.0V to VSS

-BBN

C367 1U6.3Y C0402
C375 1U6.3Y C0402

BBN_1, BBN_2 (V11, U11)

+BBP

C378 1U6.3Y C0402
C379 1U6.3Y C0402

BBP_1, BBP_2 (R11, P11)

+BBP
VDDC
VDDC+1.0V

I/O Internal

Memory I/O

PCI-Express

Core

Back Bias

POWER

PCIE_VDDR_1 … PCIE_VDDR_8 (AE30, AE31, AF29, AF27, AF28, AG29, AG30, AG31) → M82S_PCIE_VDDR

PCIE_VDDC_1 … PCIE_VDDC_12 (AA23, AC24, AC25, AE26, AE27, AE28, L23, M23, P23, T23, V23, Y23) → PCIE_VDDC

VDDC_1 … VDDC_33 (L11, L14, L17, L20, M12, M15, M18, M21, AC20, P14, P17, P20, R12, R15, R18, R21, AD20, U14, U17, U20, V12, V15, V18, V21, Y11, Y14, Y17, Y20, AA12, AA15, AA18, AA21, P9) → M82S_VDD_CORE

C391 10U6.3X C0603
C360 1U6.3Y C0402
C364 1U6.3Y C0402
C348 1U6.3Y C0402
C373 1U6.3Y C0402
C357 1U6.3Y C0402

C390 10U6.3X C0603
C371 1U6.3Y C0402
C356 10U6.3X C0603
C374 1U6.3Y C0402
C362 1U6.3Y C0402

C350 10U6.3X C0603
C385 1U6.3Y C0402
C381 1U6.3Y C0402
C389 1U6.3Y C0402
C351 1U6.3Y C0402

VDDCI_1 … VDDCI_4 (J12, J14, J16, J18) → M82S_VDDCI

C404 10U6.3X C0603
C395 1U6.3Y C0402
C405 1U6.3Y C0402
C394 1U6.3Y C0402
L41 220R_200M L0603

M82-S
BGA632
B03-00M8235-A08

VDD_CT (External TMDS enabled External TMDS enabled 120mA)
Level translation between core and I/O, excluding memory receivers.
VDD_CT must remain powered whenever the ASIC is powered.

VDDR4
DVOA_MSB_VMODE register bit; '1' - 3.3V(default); '0' - 1.8V

VDDR5
DVOA_LSB_VMODE register bit; '1' -3.3V(default); '0' - 1.8V

VDDRH
Dedicated power pins for memory clock pads for each channel.
Should have the same voltage level as VDDR1.

VDDC>VDDR1>PCIE_VDDC>VDDR3

Back Bias Pins
Back bias is a new feature which will require additional engineering verification and characterization. Prototype designs need to provide the option
to disable/by-pass this feature.

+BBP
Back Bias Enabled: (GPIO_21_BB_EN = 3.3V): 1.5V or 1.8V
Back Bias Disabled: (GPIO_21_BB_EN = 0V): VDDC
Connect to VBBP back bias regulator / generator.
If back bias is not used, connect directly to VDDC.

-BBN
Back Bias Enabled: (GPIO_21_BB_EN = 3.3V): -0.55V or -0.85V
Back Bias Disabled: (GPIO_21_BB_EN = 0V): VSS
Connect to VBBN back bias regulator / generator.
If back bias is not used connect directly to VSS.

3.3V_DELAY
+3VRUN
Q46 P-NDS352AP SOT23SGD_T
R410 100K R0402
44,48 VCCNB_PG
R178 47K R0402
XC287 0.1U10X C0402
Q24 N-2N7002 SOT23SGD_T
OPTIONAL RC NETWORK TO FINE TUNE POWER SEQUENCING

MICRO-STAR INT'L CO.,LTD.		
Title: M82S PWR&GND		
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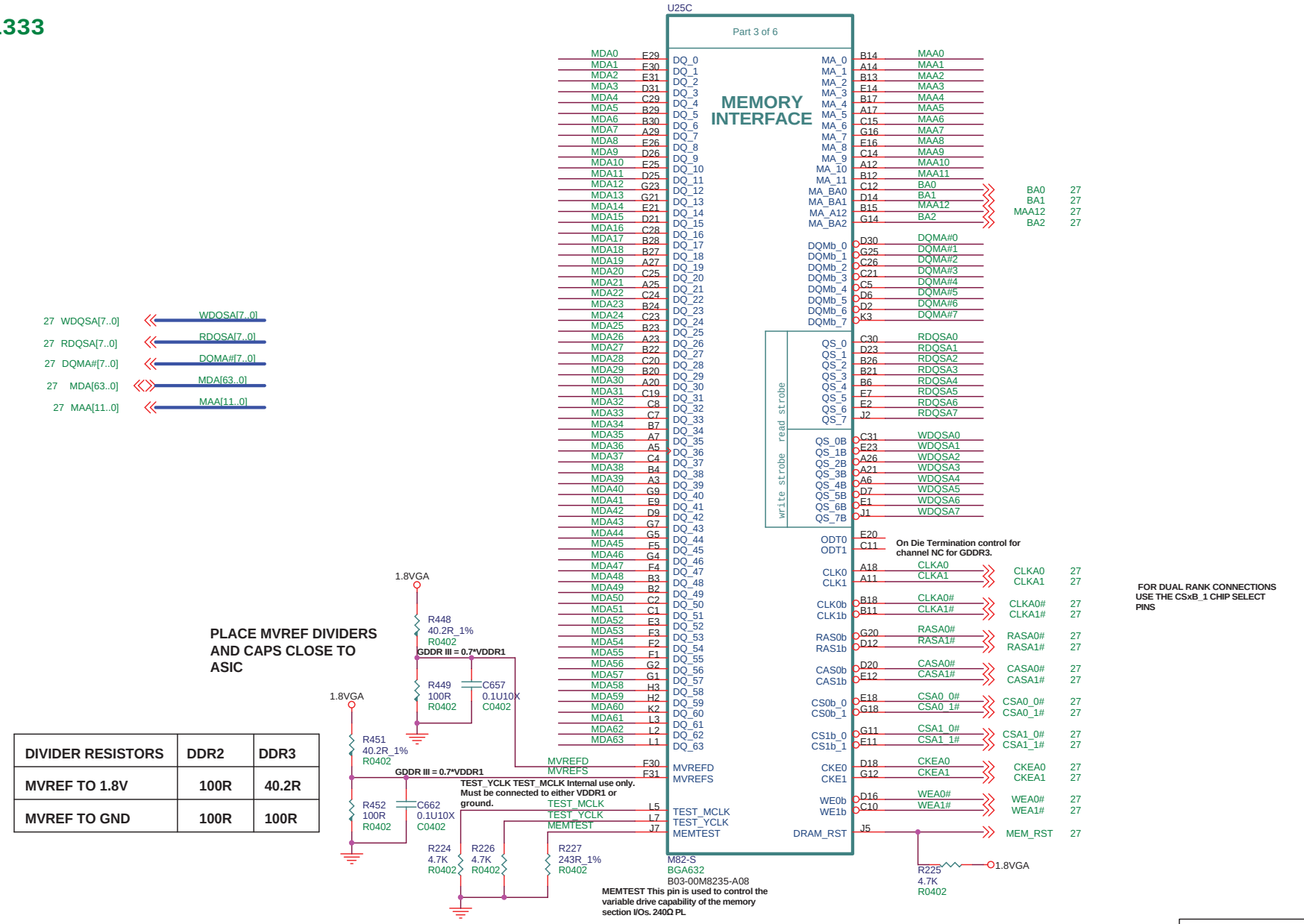

DIVIDER RESISTORS	DDR2	DDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R

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Title: M82S MEMORY

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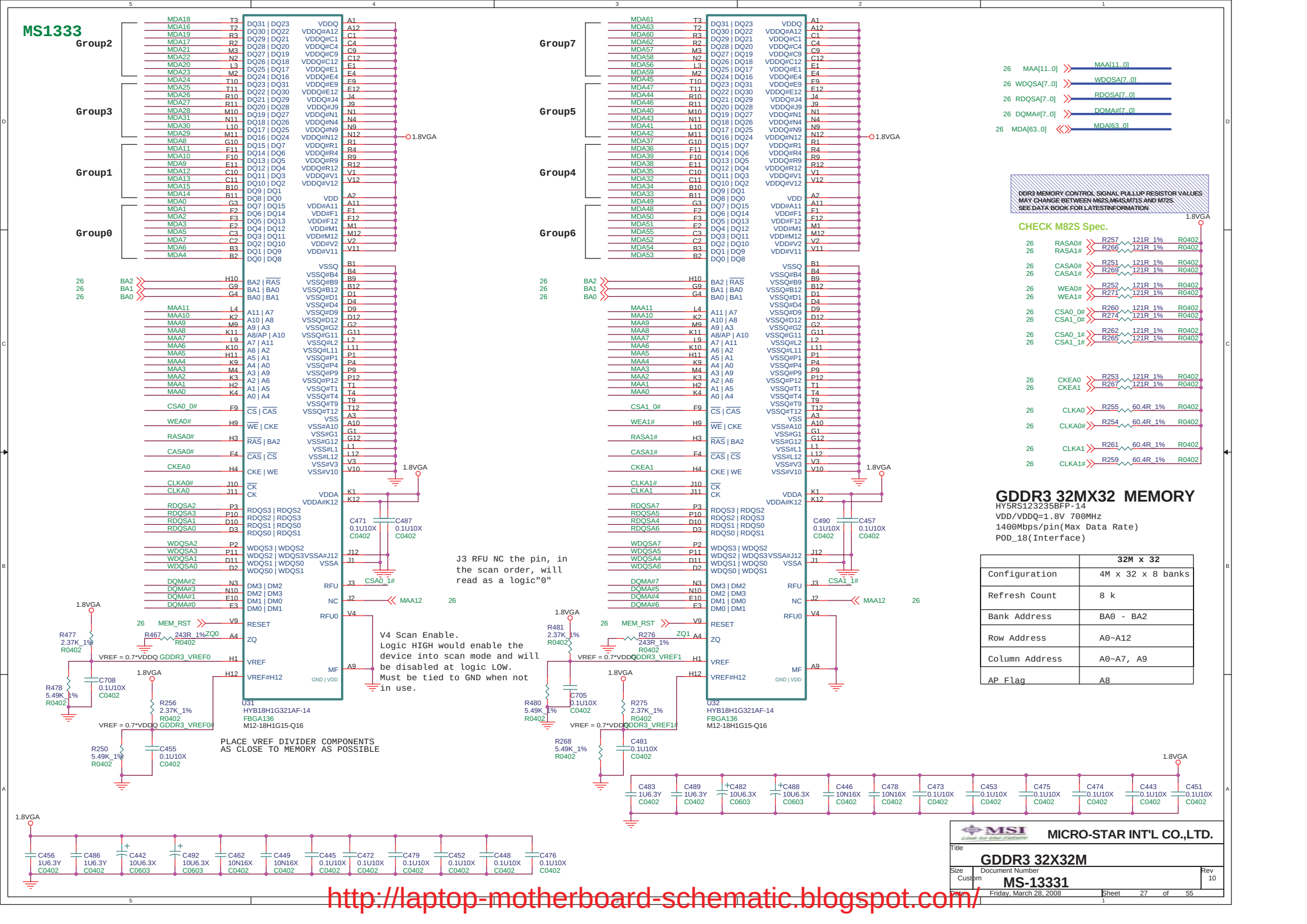

GDDR3 32MX32 MEMORY

HY5RS123235BFP-14
VDD/VDDQ=1.8V 700MHz
1400Mbps/pin(Max Data Rate)
POD_18(Interface)

	32M x 32
Configuration	4M x 32 x 8 banks
Refresh Count	8 k
Bank Address	BA0 - BA2
Row Address	A0~A12
Column Address	A0~A7, A9
AP Flag	A8

MICRO-STAR INT'L CO.,LTD.

Title: GDDR3 32X32M

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1.8VGA — L33 300L300M L0603 — LVDDR (3.3V @ 250MA LVDDR)
C306 10U6.3X C0603; C313 1U6.3Y C0402; C321 0.1U10X C0402

X R192 0R R0603

1.8VGA — L35 60L1_1000M L1206_113 — LVDDC (1.8V @ 100MA LVDDC) (1.8V @ 400MA LVDDC,LVDDR)
C320 10U6.3X C0603; C334 0.1U10X C0402; C337 0.1U10X C0402

1.8VGA — L32 220R_200M L0603 — LPVDD (1.8V @ 20MA LPVDD)
C302 10U6.3X C0603; C319 1U6.3Y C0402; C329 0.1U10X C0402 *

1.8VGA — L37 220R_200M L0603 — DPLL_PVDD (1.8V @ 40MA DPLL_PVDD)
C309 10U6.3X C0603; C315 1U6.3Y C0402; C332 0.1U10X C0402 *

1.8VGA — L39 220R_200M L0603 — PCIE_PVDD (1.8V @ 40MA PCIE_PVDD)
C324 10U6.3X C0603; C331 1U6.3Y C0402; C335 0.1U10X C0402 *

3.3V_DELAY — L38 220R_200M L0603 — A2VDD (3.3V @ 135MA A2VDD)
C304 10U6.3X C0603; C318 0.1U10X C0402; C339 1000P50X C0402

1.8VGA — L67 220R_200M L0603 — A2VDDQ (1.8V @ 2MA A2VDDQ)
C590 10U6.3X C0603; C597 1U6.3Y C0402; C602 0.1U10X C0402 *

1.8VGA — L68 220R_200M L0603 — VDDDI (1.8V @ 100MA VDD1DI,VDD2DI)
C592 10U6.3X C0603; C599 0.1U10X C0402; C608 1000P50X C0402 *

1.8VGA — L69 220R_200M L0603 — M82S_AVDD (1.8V @ 65MA AVDD)
C593 10U6.3X C0603; C598 0.1U10X C0402; C606 1000P50X C0402

+1.1VRUN — L70 220R_200M L0603 — DPA_VDDR (1.8V @ 100MA EACH SINGLE LINK) (1.1V @ 200MA EACH SINGLE LINK)
C594 10U6.3X C0603; C600 1U6.3Y C0402; C609 0.1U10X C0402

+1.1VRUN — L66 220R_200M L0603 — DPB_VDDR
C591 10U6.3X C0603; C596 1U6.3Y C0402; C603 0.1U10X C0402

1.8VGA — L71 220R_200M L0603 — DPA_PVDD (1.8V @ 20MA TPVDD EACH SINGLE LINK)
C595 10U6.3X C0603; C601 0.1U10X C0402; C610 1000P50X C0402 *

1.8VGA — L42 220R_200M L0603 — VDD_CT (VDD_CT 1.8V @ 110MA (VDD_CT)
C411 10U6.3X C0603; C407 0.1U10X C0402; C401 1000P50X C0402

1.8VGA — L30 60L1_1000M L1206_113 — M82S_PCIE_VDDR (1.8V @ 400MA PCIE_VDDR)
C307 10U6.3X C0603; C314 1U6.3Y C0402; C322 0.1U10X C0402

PLACE ALL DECOUPLING AS CLOSE TO ASIC AS POSSIBLE

1.8VGA — L73 220R_200M L0603 — VDD_MEM_CLK0 (1.8V @ MA VDDRHA_1 INCLUDED IN VDDR1)
C682 10U6.3X C0603; C683 1U6.3Y C0402; C684 0.1U10X C0402

1.8VGA — L44 220R_200M L0603 — VDD_MEM_CLK1 (1.8V @ MA VDDRHA_2 INCLUDED IN VDDR1)
C431 10U6.3X C0603; C437 1U6.3Y C0402; C436 0.1U10X C0402

FOR M7x
INSTALL LVDDR TO +3.3V AND
LVDDC TO 1.8V
WITH SEPARATE FILTERS
DO NOT INSTALL STRAP RESISTOR
FOR M8x
INSTALL LVDDR AND LVDDC TO +1.8V
WITH THE ONE LVDDC FILTER
DO NOT INSTALL LVDDR FILTER
INSTALL STRAP RESISTOR

FOR M8x
INSTALL DPA_VDDR TO +1.1V AND
DPB_VDDR TO +1.1V
WITH SEPARATE FILTERS
DO NOT INSTALL STRAP RESISTOR
FOR M7x
INSTALL DPA_VDDR AND DPB_VDDR TO +1.8V
WITH THE ONE DPA_VDDR FILTER
DO NOT INSTALL DPB_VDDR FILTER
INSTALL STRAP RESISTOR

PLACE ALL DECOUPLING CAPS
CLOSE TO THE ASIC
* AND RUN DEDICATED TRACES
FROM ASIC PINS
TO JOIN THE GROUND PLANE
WITH ONE VIA AT THE CAP

+1.1VRUN — L63 220L3A L0805_67 — PCIE_VDDC (PCIE_VDDC 1.1V @ 1A)
C575 10U6.3X C0603; C584 1U6.3Y C0402; C359 0.1U10X C0402
C398 1U6.3Y C0402; C370 1U6.3Y C0402; C387 1U6.3Y C0402

L36 220R_200M L0603 — DPLL_VDDC (DPLL_VDDC 1.1V @ 100 MA)
C310 10U6.3X C0603; C316 1U6.3Y C0402 *

M82S_VDD_CORE — L45 300L300M L0603 — MPVDD (.95V-1.1V @ 230MA MPVDD)
C435 10U6.3X C0603; C438 1U6.3Y C0402; C439 0.1U10X C0402 *

THE OPTIMAL +BBP OFFSET VOLTAGE
(POWERPLAY VDDC MINUS 1.5V OR 1.8V RAIL)
IS YET TO BE DETERMINED

THE OPTIMAL -BBN OFFSET VOLTAGE
(0V MINUS -.6V TO -.9V)
IS YET TO BE DETERMINED
BUT MAX1673 DIVIDER RESISTORS
MUST BE ADJUSTED FOR THE SAME
OFFSET AS +BBP

BB_ENA = 0V FOR BACK BIASING DISABLED
MAX1673 SHUTDOWN
-BBN = 0V VIA MAX1673 INTERNAL 1 OHM TO GROUND
N FET A = OFF, P FET B = OFF, N FET C = ON
+BBP = VDD_CORE

1.8VGA — L80 220R_200M L0603 — DPB_PVDD
C724 0.1U10X C0402; C725 1000P50X C0402

M82S_VDD_CORE (+1.8V 0R +1.1V @ 1A MAX)
+5VRUN
X Q28 N-SI2304DS SOT23SGD_T
X Q29 P-SI2301DS SOT23SGD_T
X R216 100K R0402
FET C 1.7A
FET B 1.8A
M82S_VDD_CORE
R213 0R R0402
23 BB_ENA
X PQ28 N-2N7002 SOT23SGD_T
X R203 10K R0402
+BBP
X C366 1U6.3Y C0402

+3VRUN
X U16 MAX1673ESA SOIC8
LIN/SKIP# IN; CAP+ GND; CAP- FB; SHDN# OUT
X C333 2.2U6.3Y C0603 BB_ENA
X C325 10U6.3X C0603
X R194 100K R0402
X R200 17.4K_1% R0402

-BB_VGA= -(+3VRUN) * R2138 / R2134

-BBN
X C343 10U6.3X C0603
X C342 10U6.3X C0603
R206 0R R0402

BB_ENA = +3.3V FOR BACK BIASING ENABLED
MAX1673 ENABLED
-BBN = -.85V
N FET A = ON, P FET B = ON, N FET C = OFF
+BBP = +1.8V

MICRO-STAR INT'L CO.,LTD.

Title	M82S_PWR_&FILTER	
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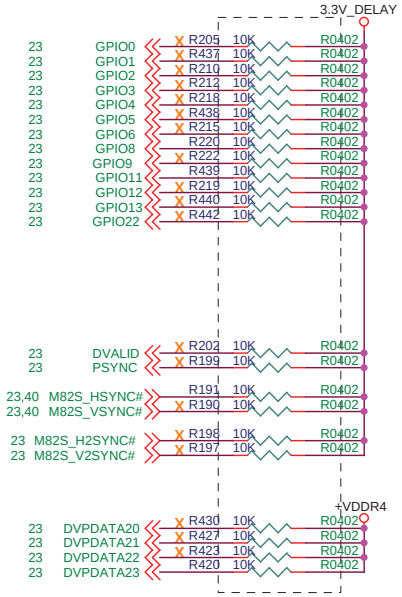
CHECK M82S Spec. and Reference Schematic and ATi FAE



Only populate the required straps, see table and databook

GPIO22=0 GPIO_9 GPIO_[13:11]= CONFIG[3:0]
a) If BIOS_ROM_EN = 1, then Config[3:0] defines the ROM type. See "ROM Configurations"
b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. (Config 3 = don't care).

R440 R219 R439

Size of the primary memory apertures	CONFIG[3:0]
128MB	x000
256MB	x001
64MB	x010
32MB	x011
512MB	x100
1GB	x101
2GB	x110
4GB	x111

DVPDATA23 R420	DVPDATA22 R423	DVPDATA21 R427	MEM_TYPE
0	0	0	Hynix 16MX32
0	0	1	
0	1	0	
0	1	1	
1	0	0	QIMONDA 32MX32
1	0	1	SANGSUNG 32MX32
1	1	0	
1	1	1	

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE
RSVD = ATI RESERVED
(DO NOT INSTALL)

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	M8x	M7x
BIF_MSI_DIS	VIP1	MESSAGE SIGNAL INTERRUPT ENABLED	NA	0
BIF_AUDIO_EN	VIP3	ENABLE HD AUDIO	NA	X
BIF_64BAR_EN_A	VIP5	64 BIT BARS DISABLED	NA	0
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	X	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X	X
BIF_DEBUG_ACCESS	GPIO4	DEBUG SIGNALS MUXED OUT	0	0
BIF_AUDIO_EN	GPIO8	ENABLE HD AUDIO	X	RSVD
BIF_GEN2_EN_A	GPIO5	Allows either PCIe 2.5GT/s or 5.0GT/s operation	X	0
BIOS_ROM_EN	GPIO_22_ROMCSB	DISABLE EXTERNAL BIOS ROM	NA	X
ROMIDCFG(3:0)	GPIO[13:11,9]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XX X X	X X X X
VIP_DEVICE_STRAP_ENA	M82S_VSYNC#	IGNORE VIP DEVICE STRAPS = LOW	0	0
BIF_VGA DIS	PSYNC	VGA ENABLED = LOW	0	0
BIF_HDMI_EN	M82S_HSYNC#	HDMI ENABLE = HIGHT (SEE NOTE 2)	X	X
DEBUG_ I2C_ENABLE	GPIO6	Internal use only	0	0
MEM_TYPE	ANY UNUSED GPIO OR DVP THAT ARE NOT CONFIG STRAPS FOR EXAMPLE DVPDATA20:23 IN THIS DESIGN	MEMORY TYPE,MAKE AND SIZE INFO	X X X X	X X X X

ATI RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESE

GPIO2 GPIO3 DVALID H2SYNC V2SYNC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GENERICC GPIO21_BB_EN GPIO_28_TDO

NOTE 1: HD AUDIO MUST ONLY BE ENABLED ON SYSTEMS THAT ARE LEGALLY ENTITLED. IT IS THE RESPONSIBILITY OF THE SYSTEM DESIGNER TO ENSURE ENTITLEMENT

NOTE 2: HDMI MUST ONLY BE ENABLED ON SYSTEMS THAT ARE LEGALLY ENTITLED. IT IS THE RESPONSIBILITY OF THE SYSTEM DESIGNER TO ENSURE ENTITLEMENT

COMPONENTS SHOWN ARE EXAMPLES ONLY AND NOT NECESSARILY QUALIFIED

MICRO-STAR INT'L CO.,LTD.

Title: M82S CONGIF STARP

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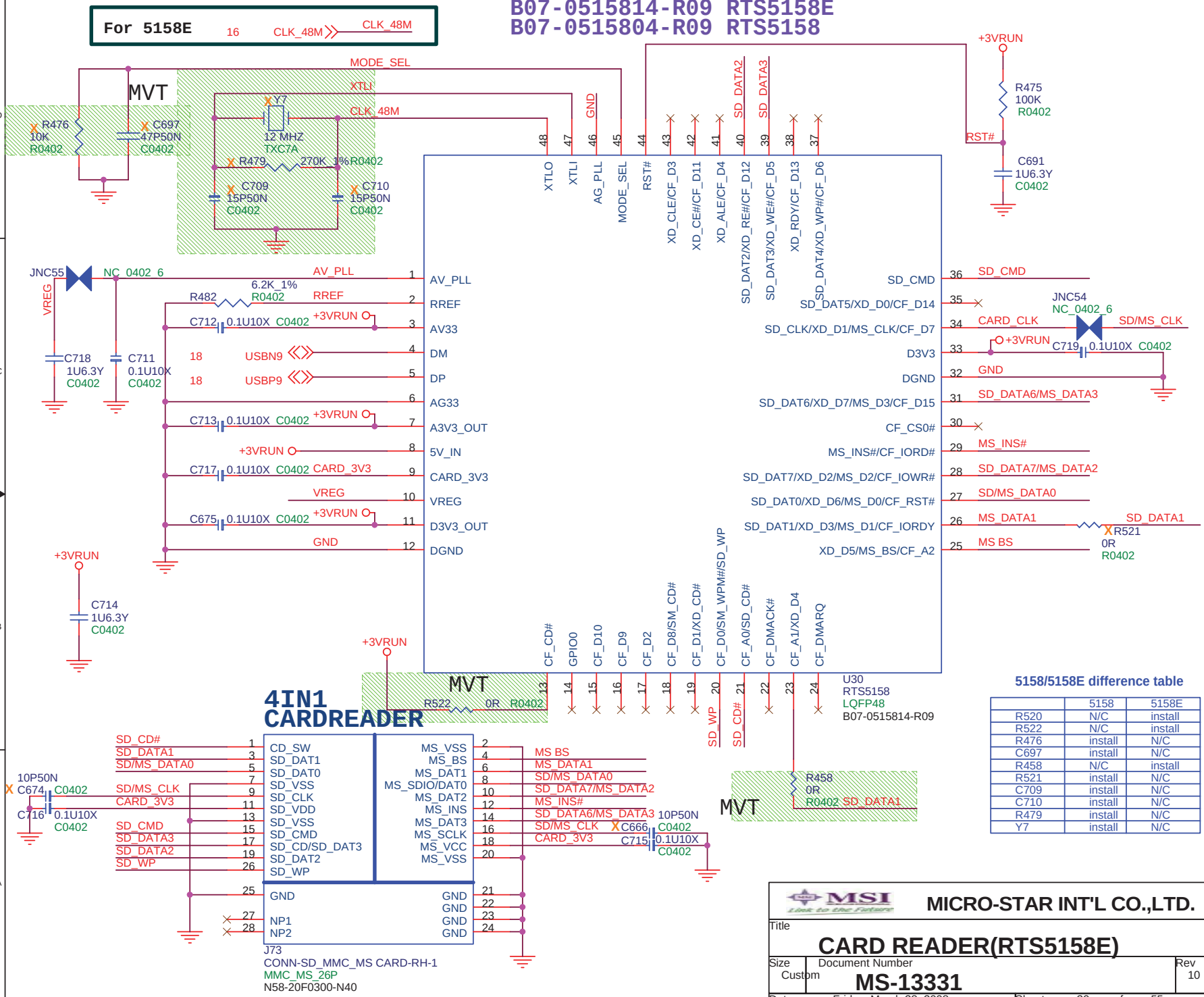
B07-0515814-R09 RTS5158E
B07-0515804-R09 RTS5158

For 5158E 16 CLK_48M >> CLK_48M



5158/5158E difference table

	5158	5158E
R520	N/C	install
R522	N/C	install
R476	install	N/C
C697	install	N/C
R458	N/C	install
R521	install	N/C
C709	install	N/C
C710	install	N/C
R479	install	N/C
Y7	install	N/C

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Title: CARD READER(RTS5158E)

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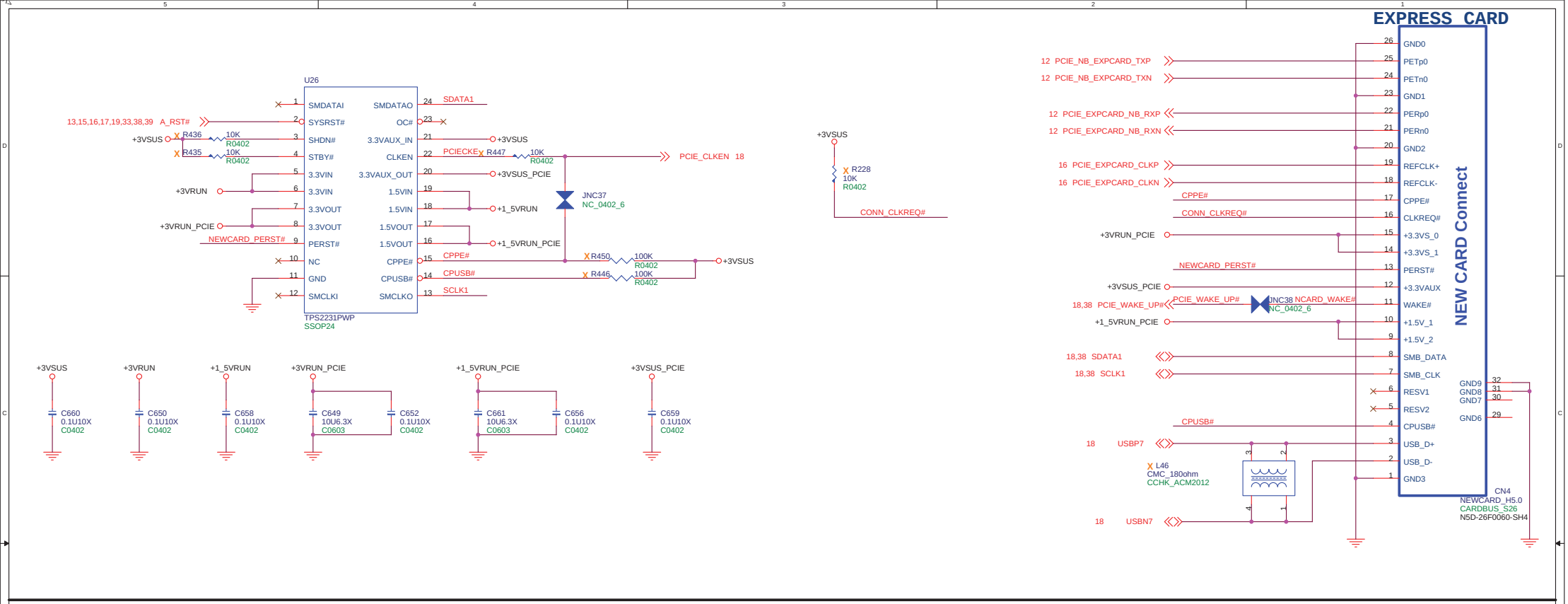

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Title: NEW CARD & MDC

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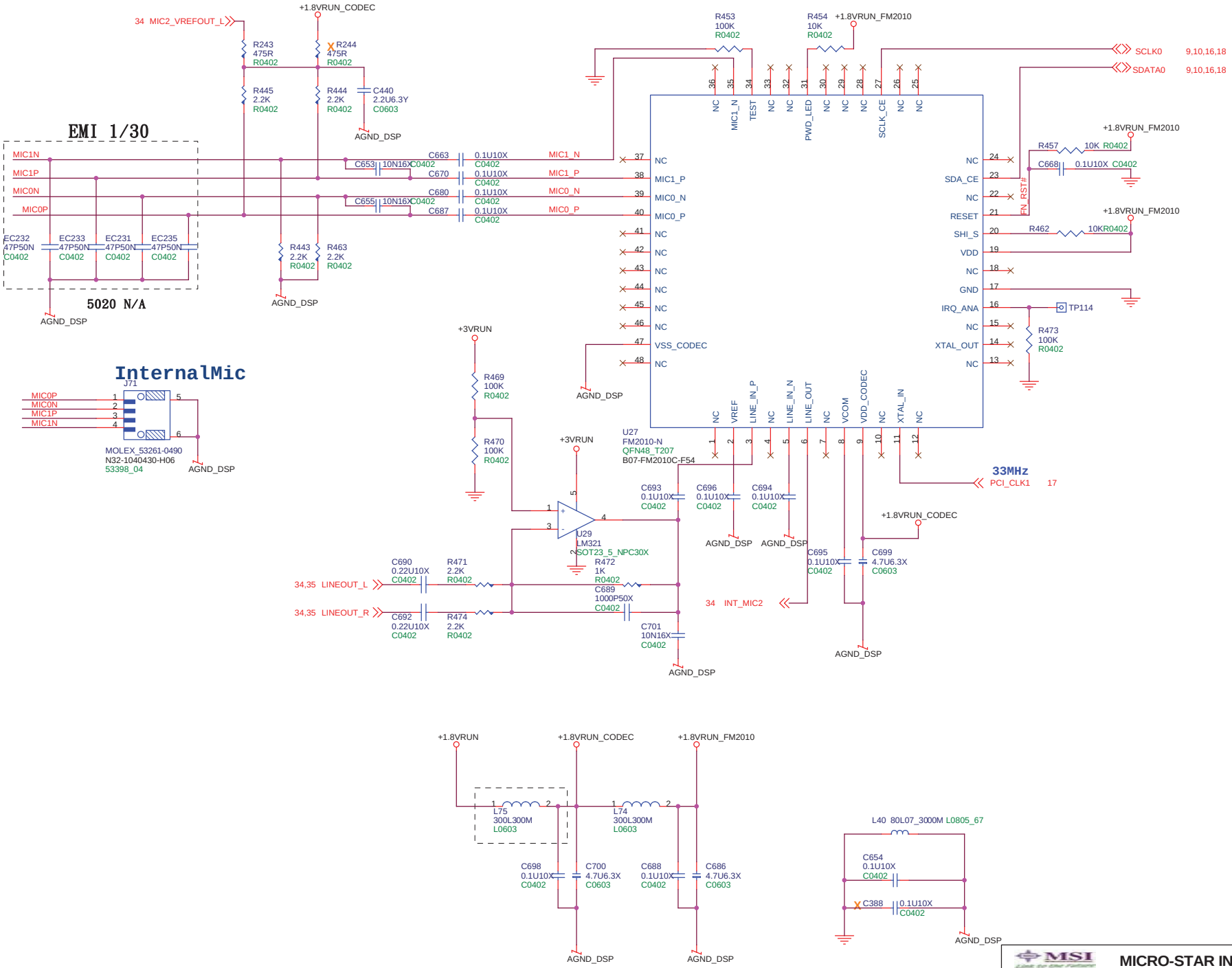

MICRO-STAR INT'L CO.,LTD.	
Title	Array Mic FM2010
Size: Custom	Document Number: MS-13331
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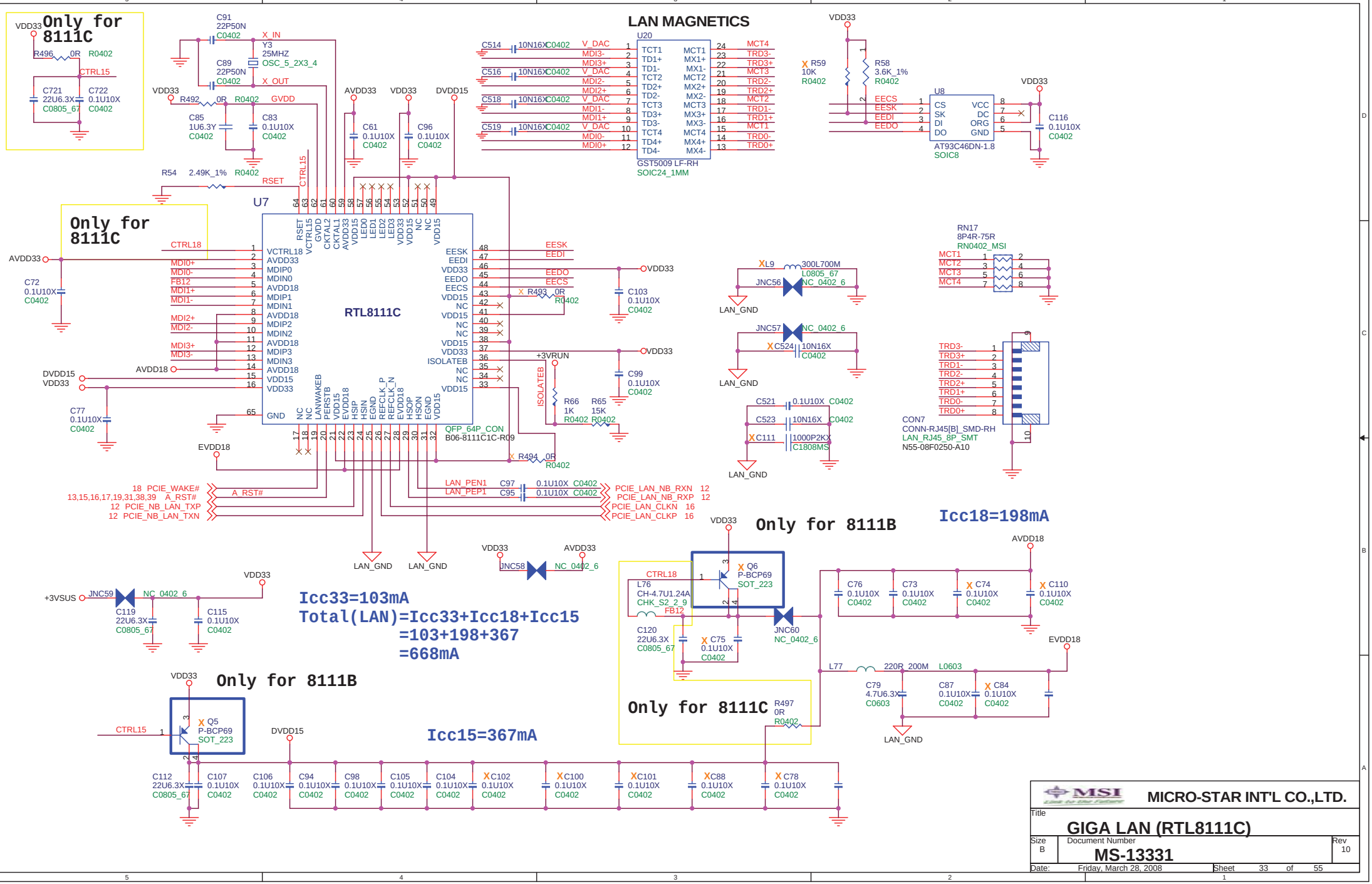
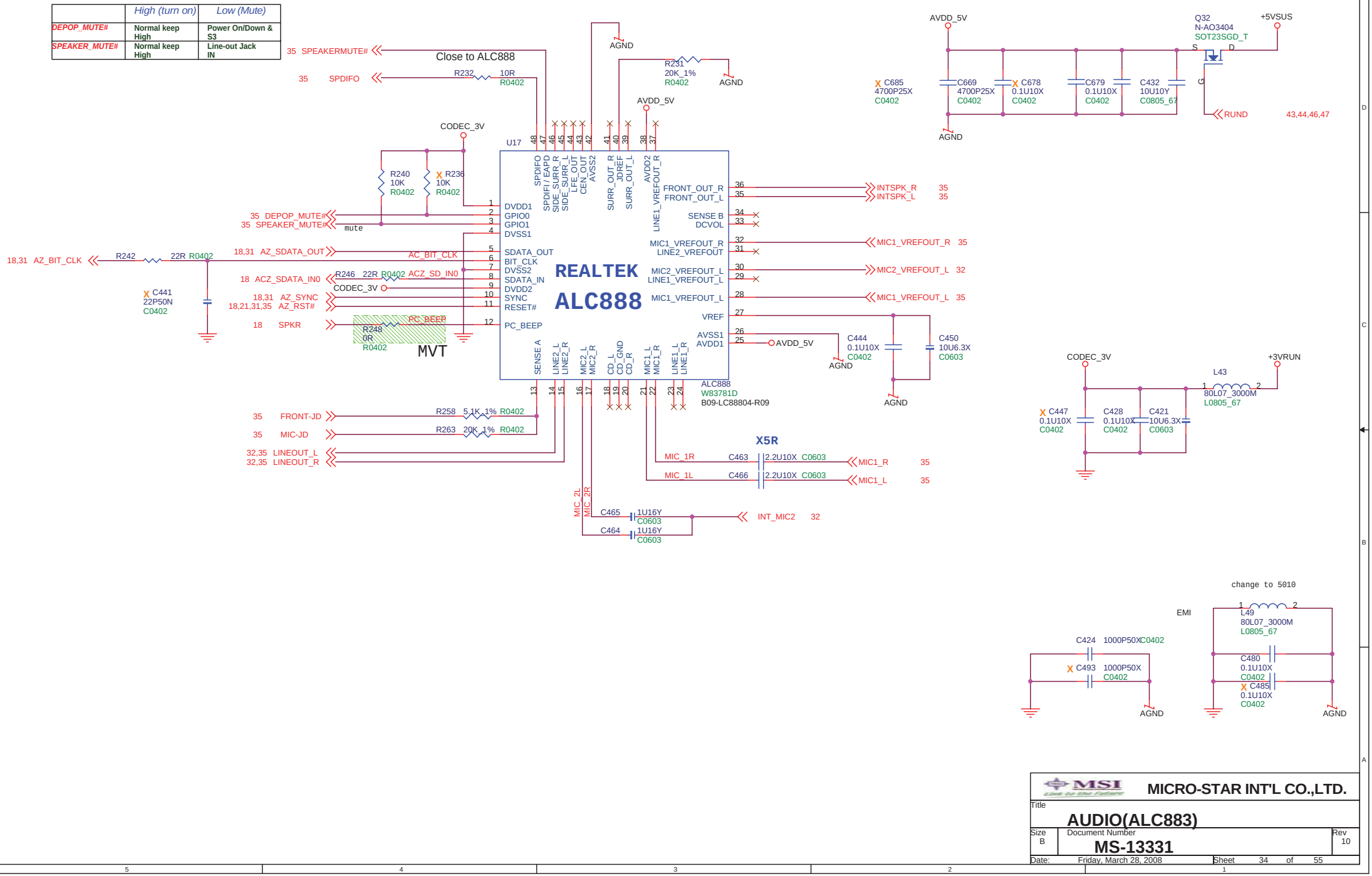
Date: Friday, March 28, 2008	Sheet 32 of 55



	High (turn on)	Low (Mute)
DEPOP_MUTE#	Normal keep High	Power On/Down & S3
SPEAKER_MUTE#	Normal keep High	Line-out Jack IN



MICRO-STAR INT'L CO.,LTD.

Title: AUDIO(ALC883)

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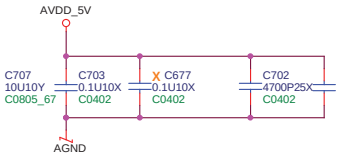
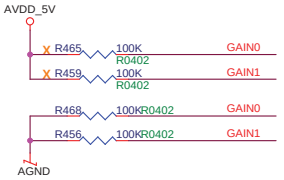
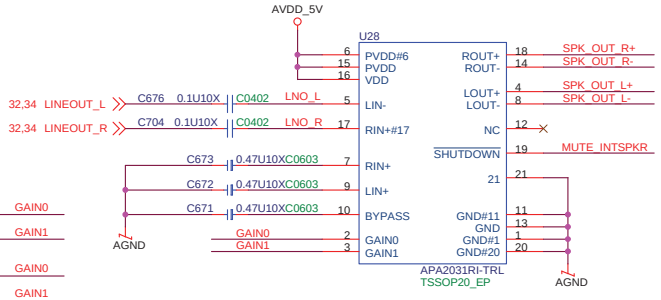
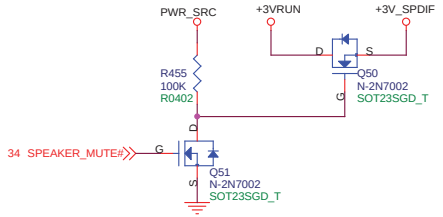


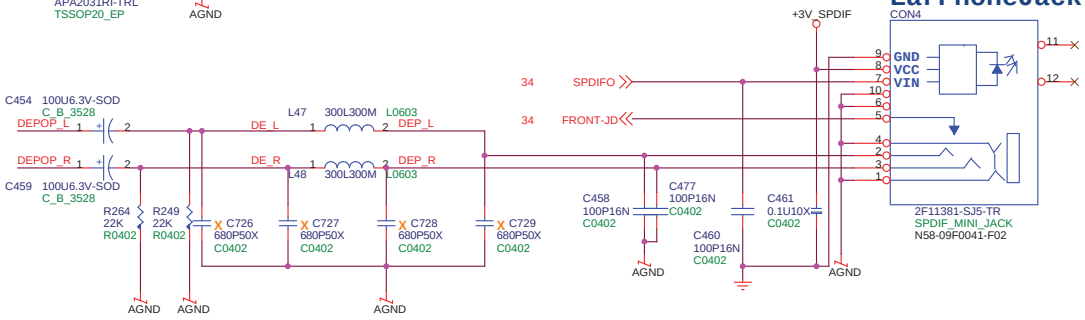
	GAIN0	GAIN1	SE/BTL#
6dB	0	0	0
10dB	0	1	0
15.6dB	1	0	0
21.6dB	1	1	0
4.3dB	X	X	1

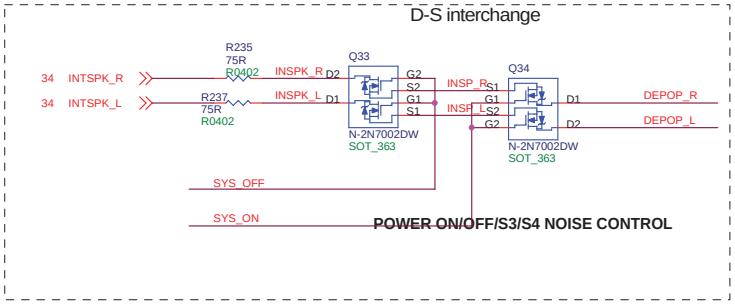




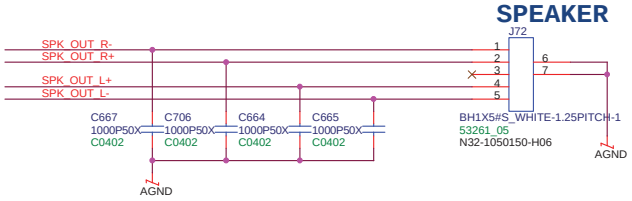


EarPhoneJack

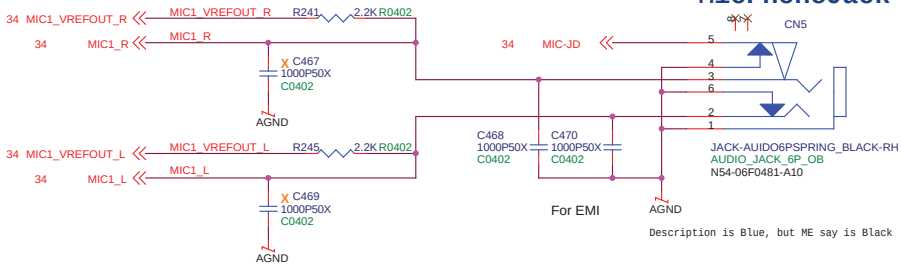


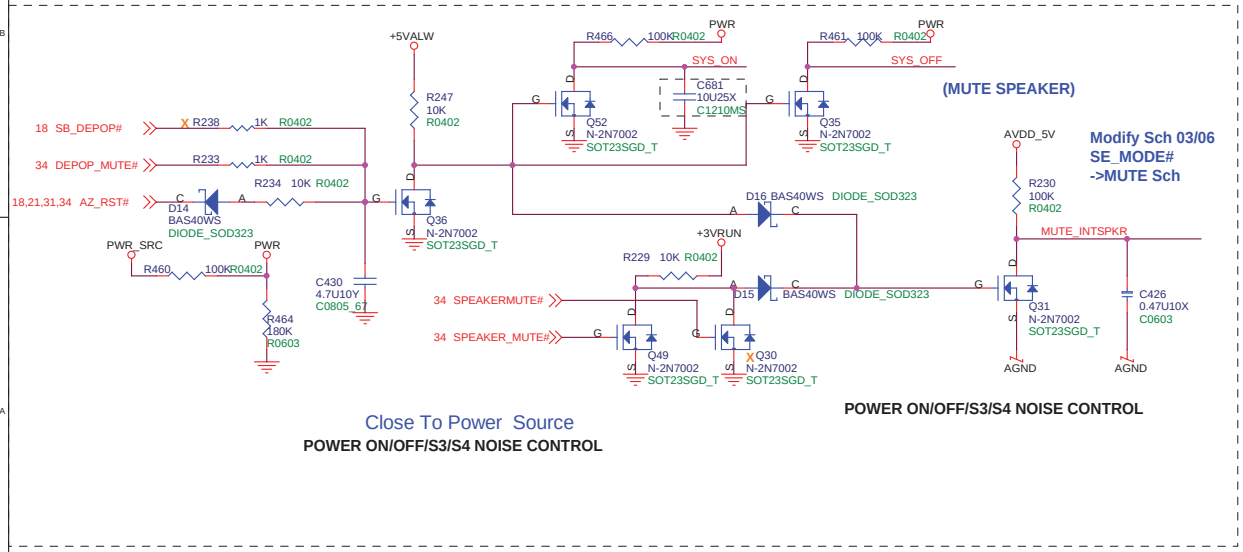


SPEAKER



MicPhoneJack





Mobile Configuation:

(3 external jacks, 1 internal Mic, 2 sets stereo internal speaker)

Pin Assignment	Location	Re-tasking
FRONT(pin-35/36)	SPDIF jack, AMP	SPDIF output, AMP output(Int.SPKR), ?
SURR (pin-39/41)	X	X
CEN/LFE (pin-43/44)	X	X
SIDESURR (pin-45/46)	X	X
LINE1 (pin-23/24)	Line-in jack	Line input, ?
MIC1 (pin-21/22)	MIC-in jack	Mic input, ?
MIC2 (pin-16/17)	Int.MIC	Int.Mic input

MICRO-STAR INT'L CO.,LTD.

Title: AMP & SPK & MIC & SPK

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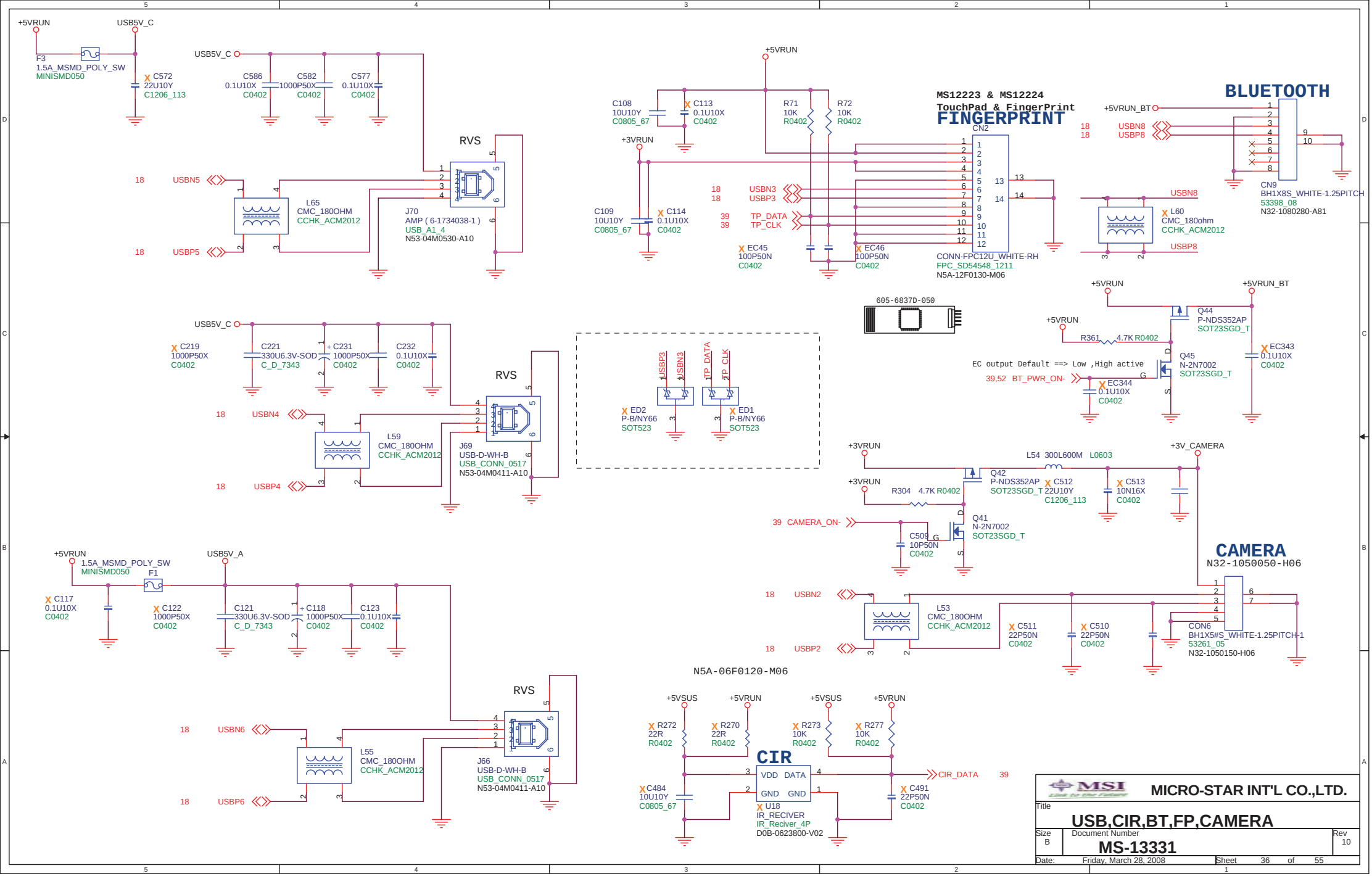
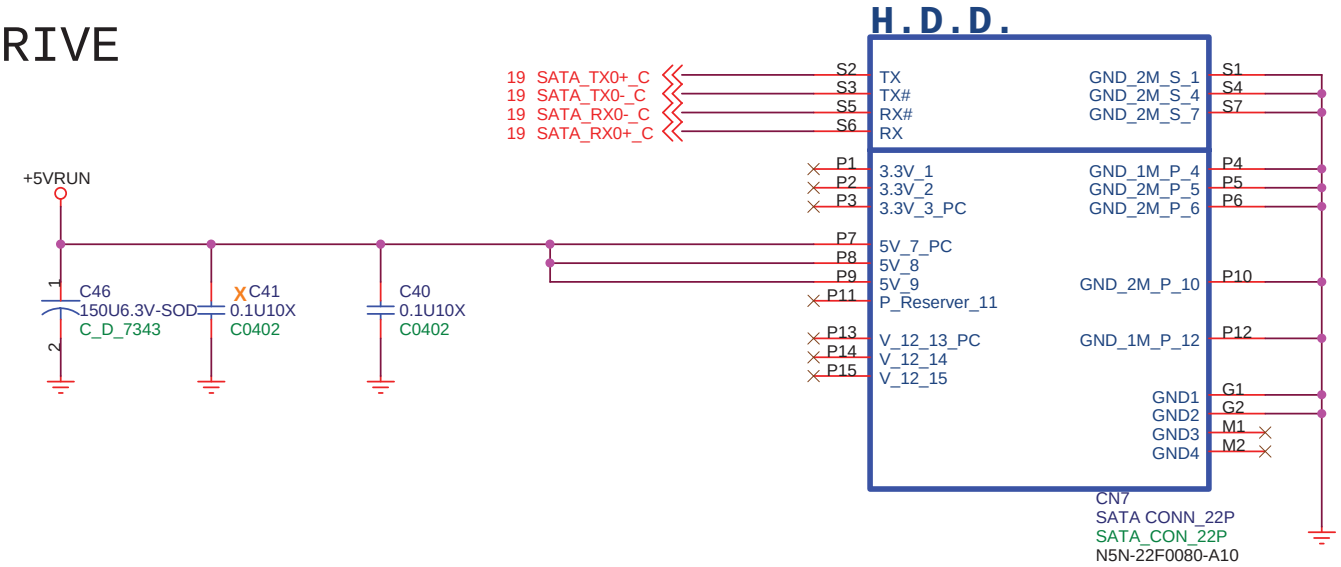
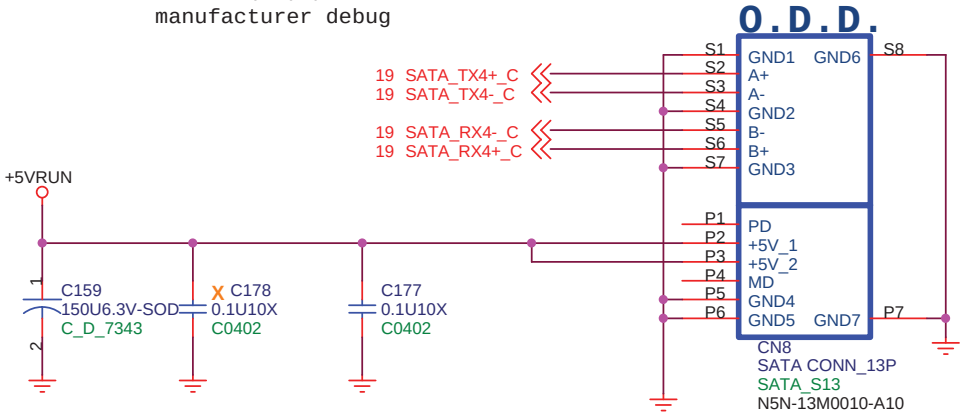
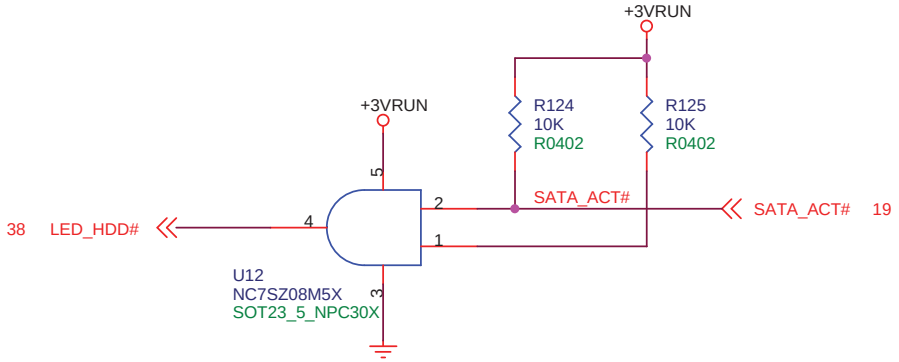


2.5"HD DRIVE



The MD (P4) pin is for ODD manufacturer debug





The PD (P1) pin is for host GIO to detect if the ODD is present or not. In the drive, the pin is “pull-low”. So when host side detects this pin as high,then no device; when host side detect this pin as low, then the device present.

MICRO-STAR INT'L CO.,LTD.

Title: SATA HDD/PATA CDROM CONN

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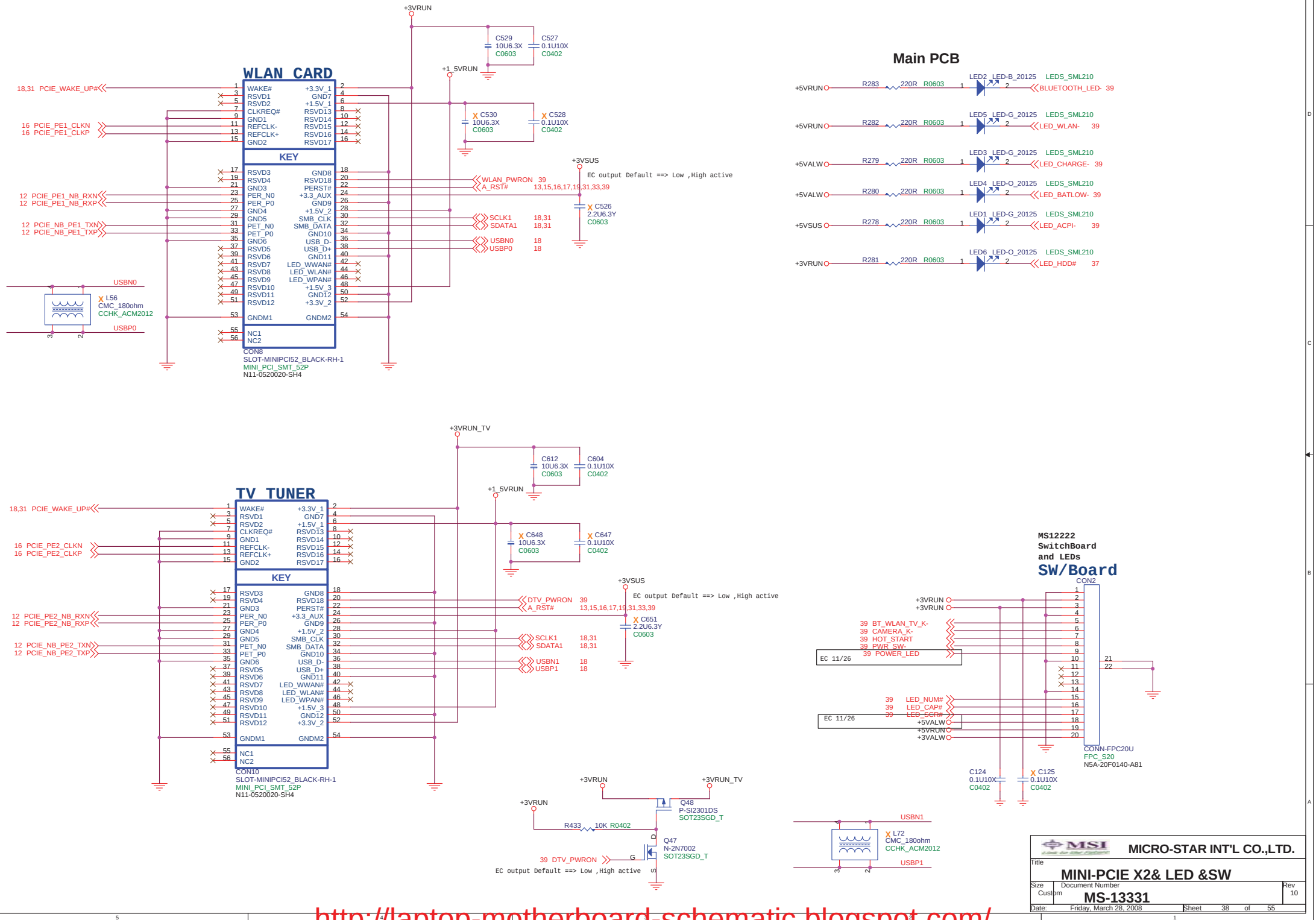
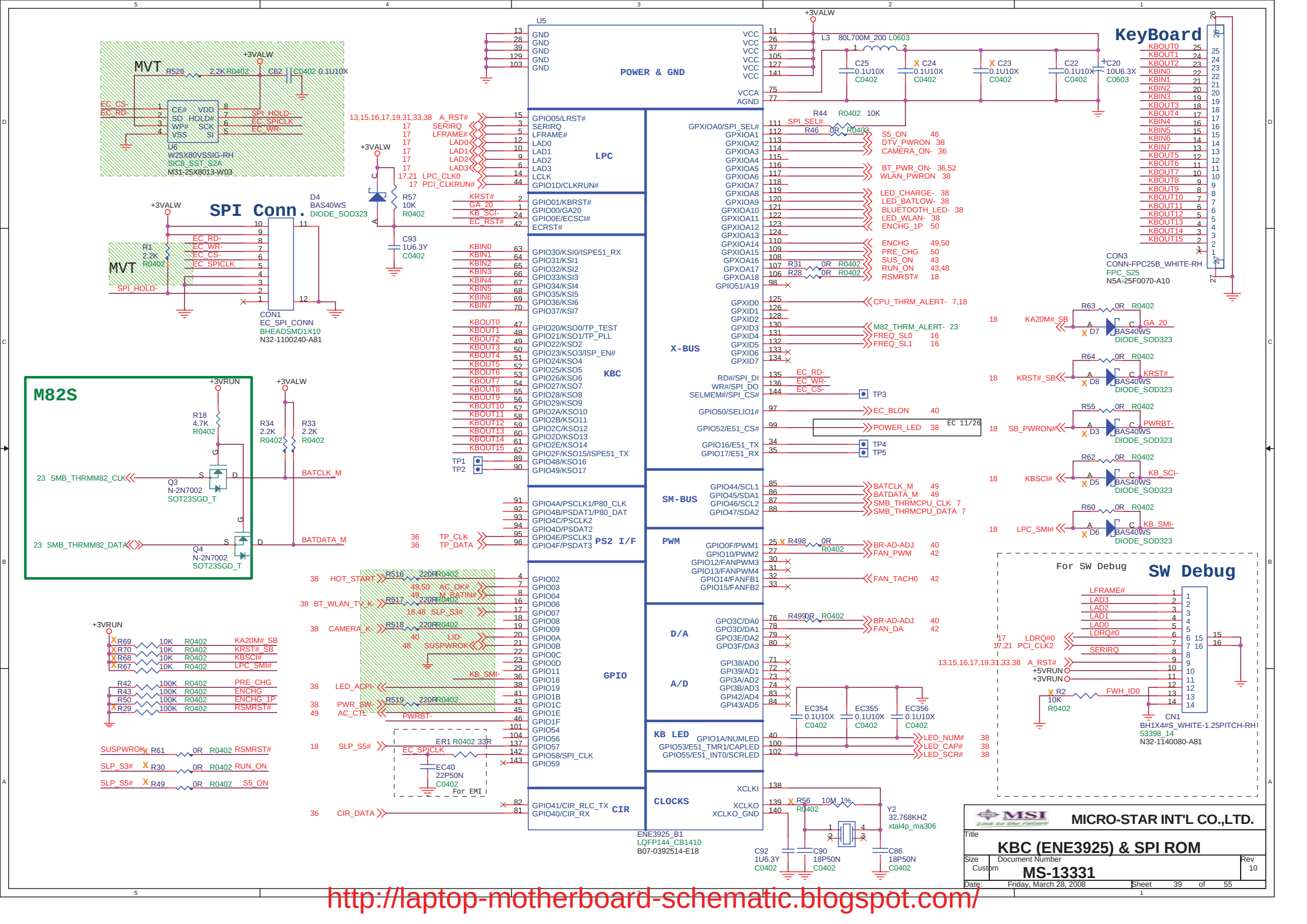
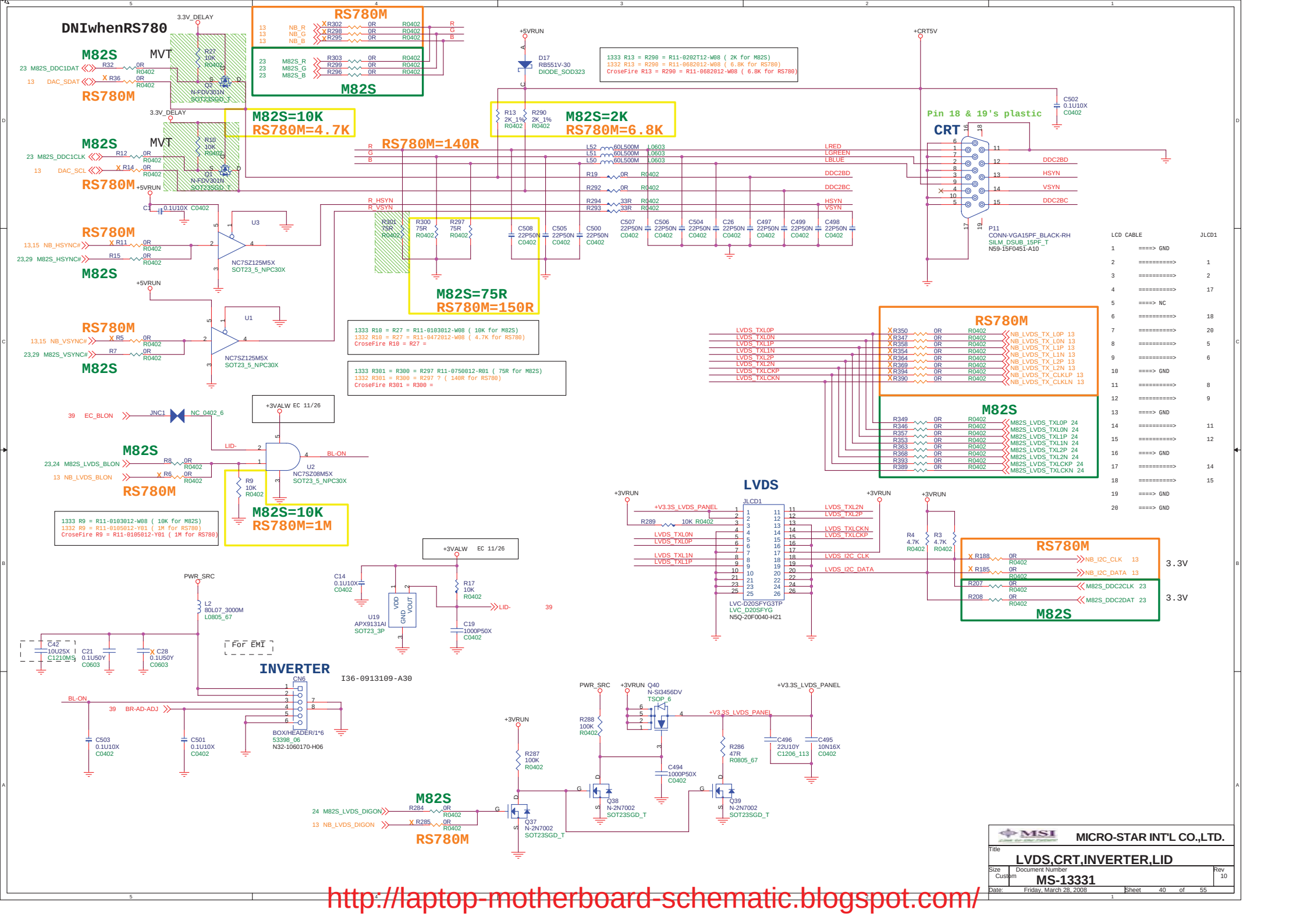

WLAN_CARD
TV_TUNER
Main PCB
MS12222
SwitchBoard
and LEDs
SW/Board
MINI-PCIE X2& LED &SW
MICRO-STAR INT'L CO.,LTD.
MS-13331
Friday, March 28, 2008
http://laptop-motherboard-schematic.blogspot.com/




DNIwhenRS780
RS780M
M82S
M82S=10K
RS780M=4.7K
M82S=2K
RS780M=6.8K
RS780M=140R
M82S=75R
RS780M=150R
M82S=10K
RS780M=1M
LVDS
INVERTER
I36-0913109-A30
CRT
Pin 18 & 19's plastic
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LVDS,CRT,INVERTER,LID
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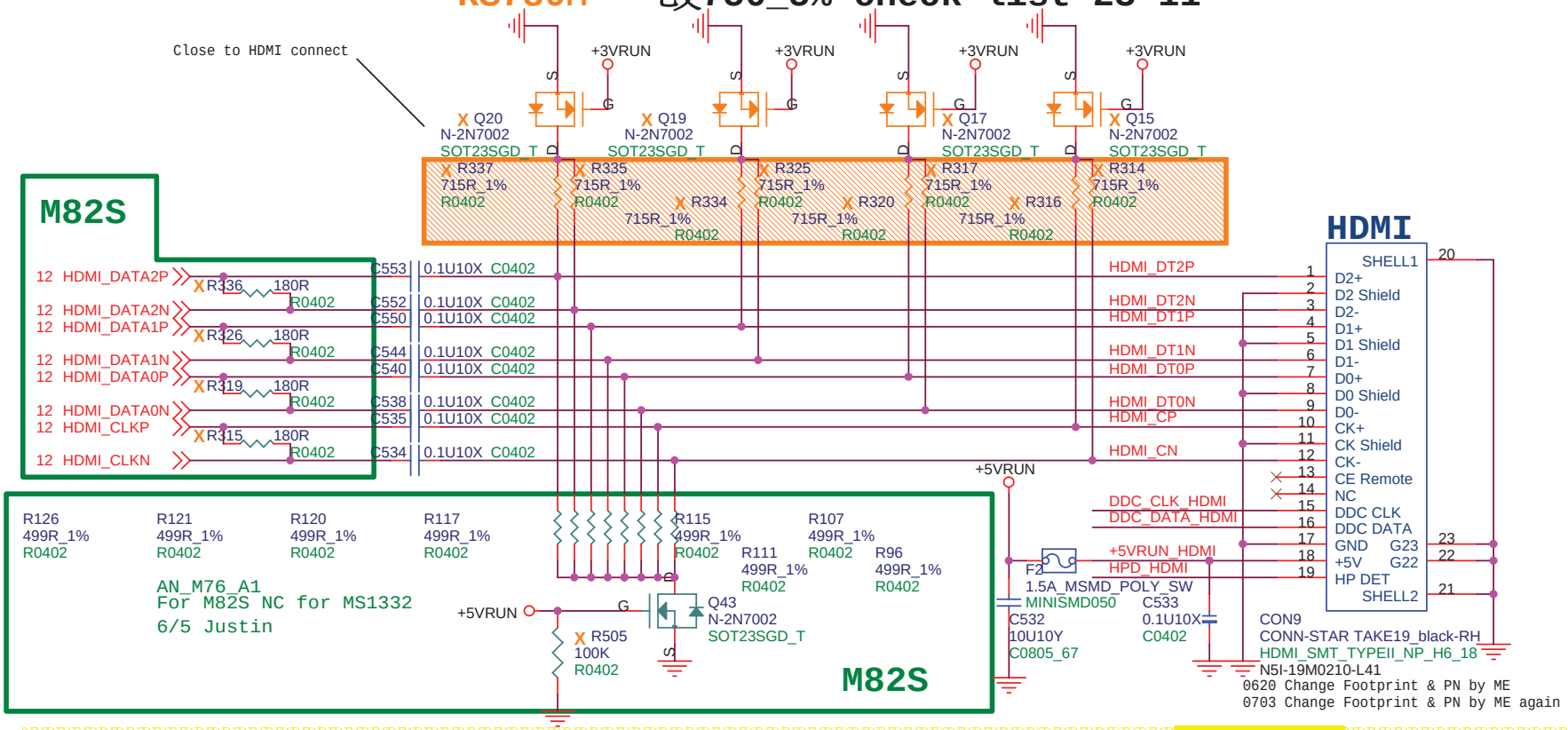
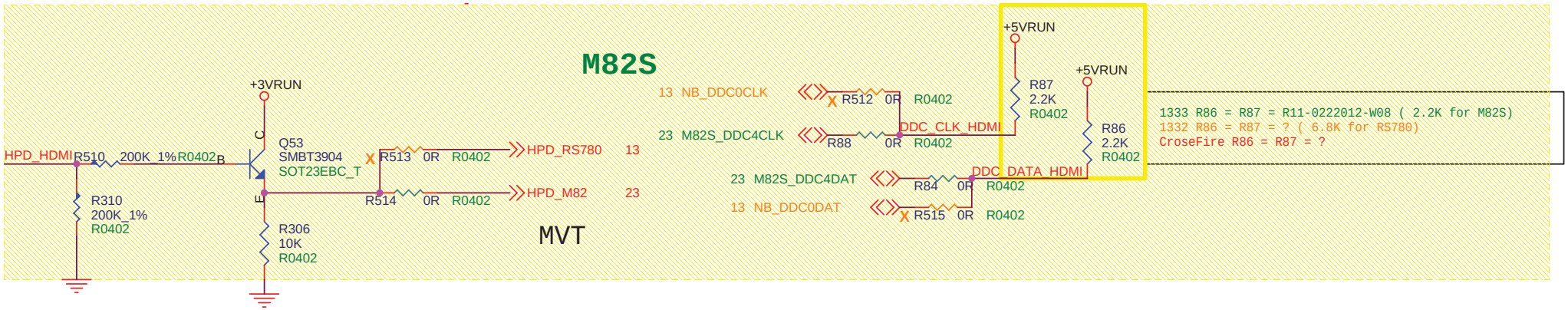
RS780M 改750_5% check list 23-11





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Title: PWRGD

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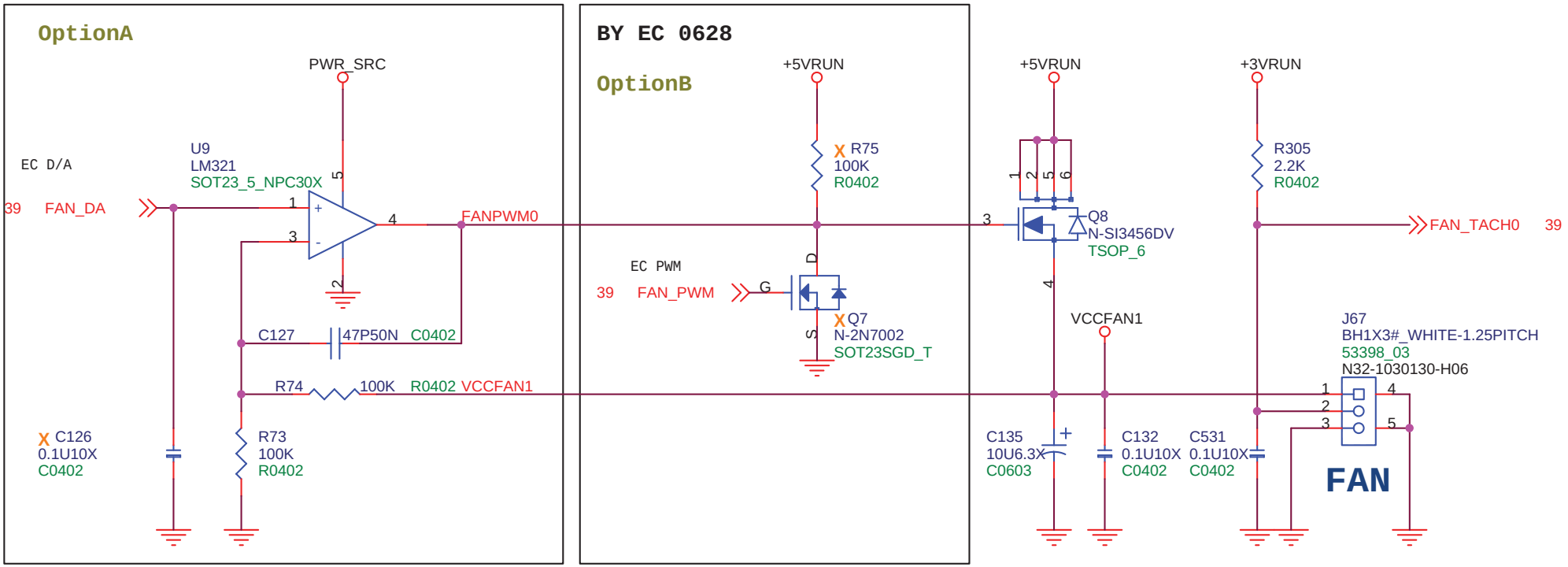

MICRO-STAR INT'L CO.,LTD.

Title: FAN

Size	Document Number	Rev
A	MS-13331	10

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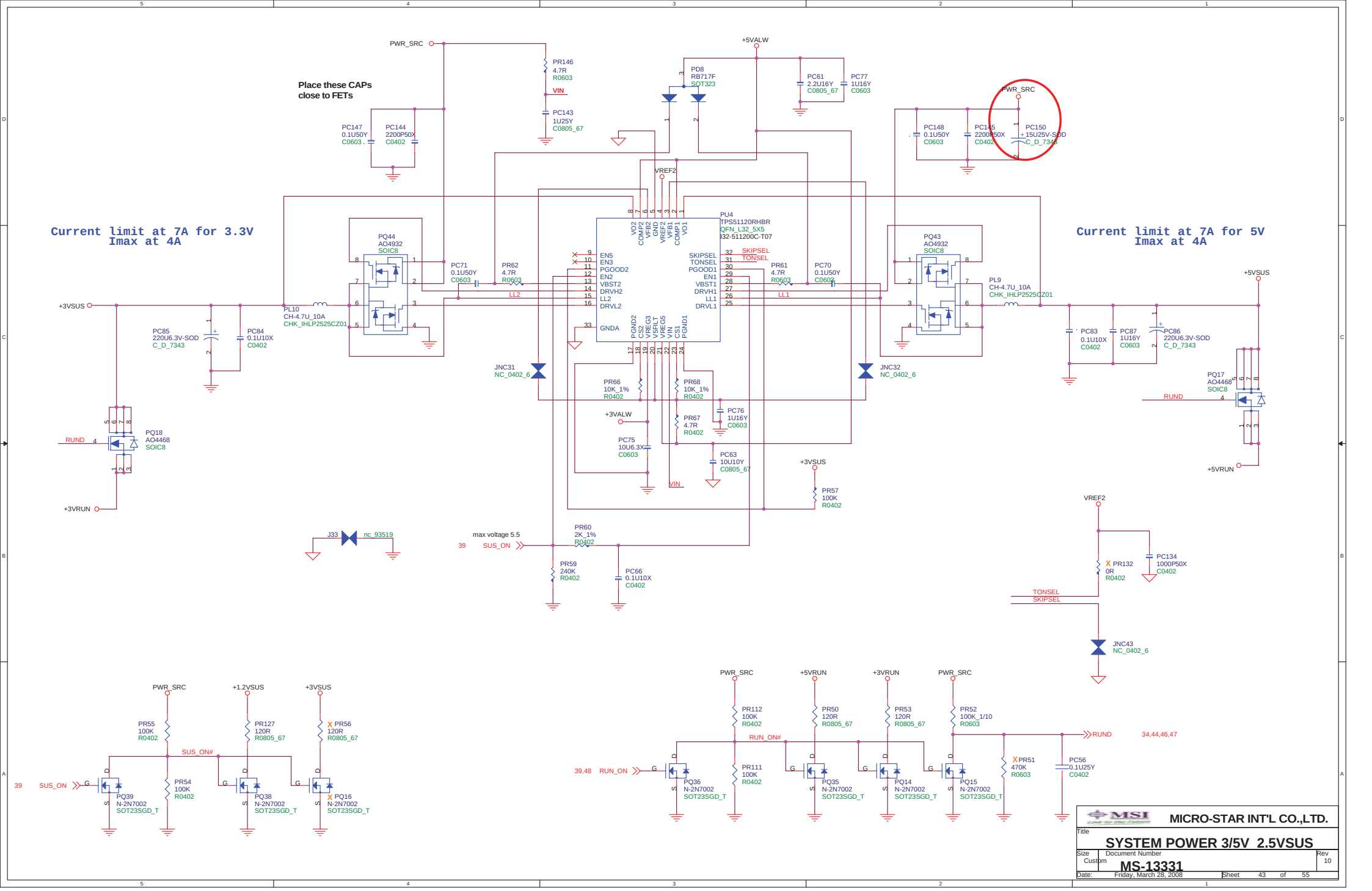
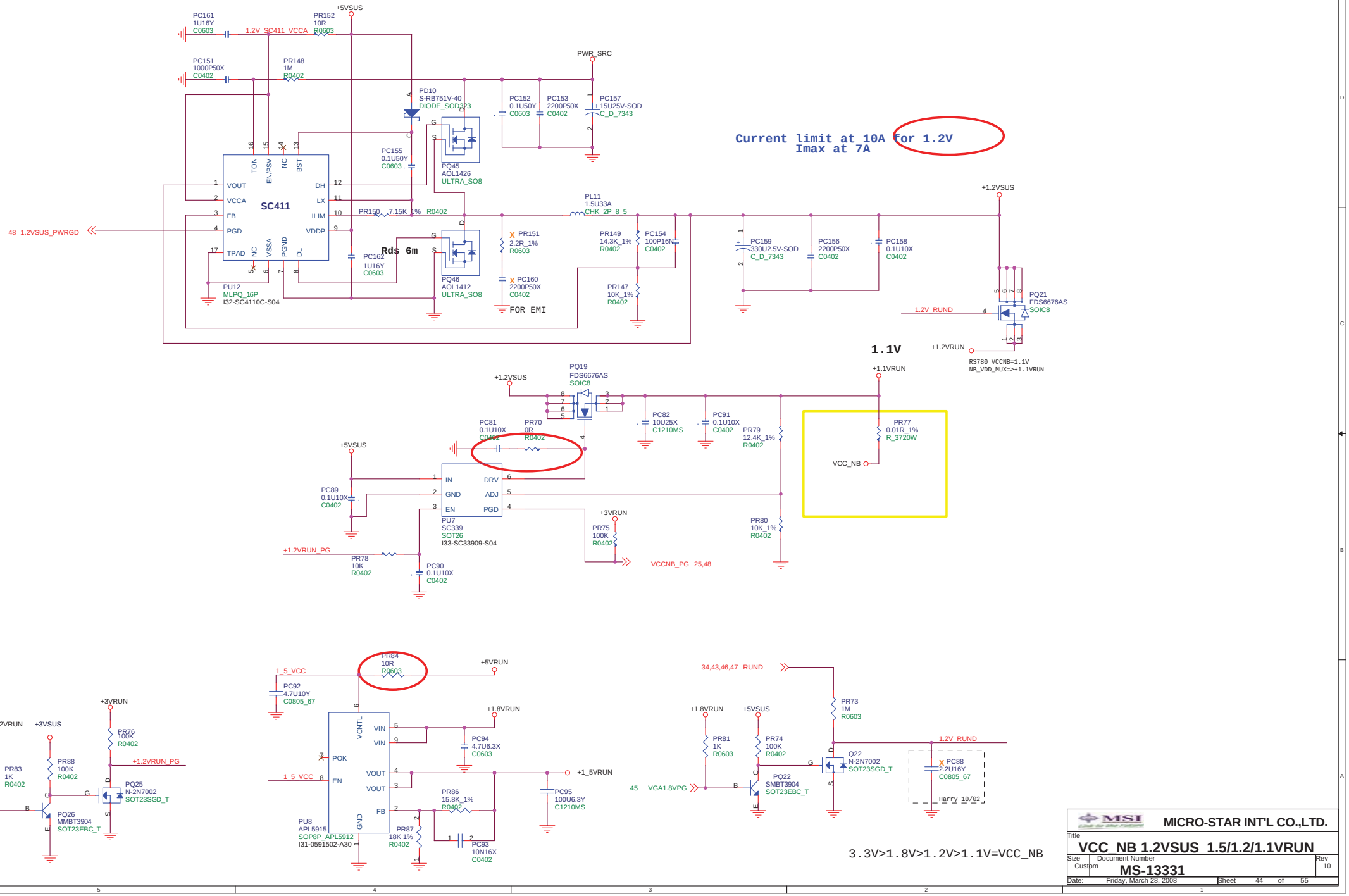
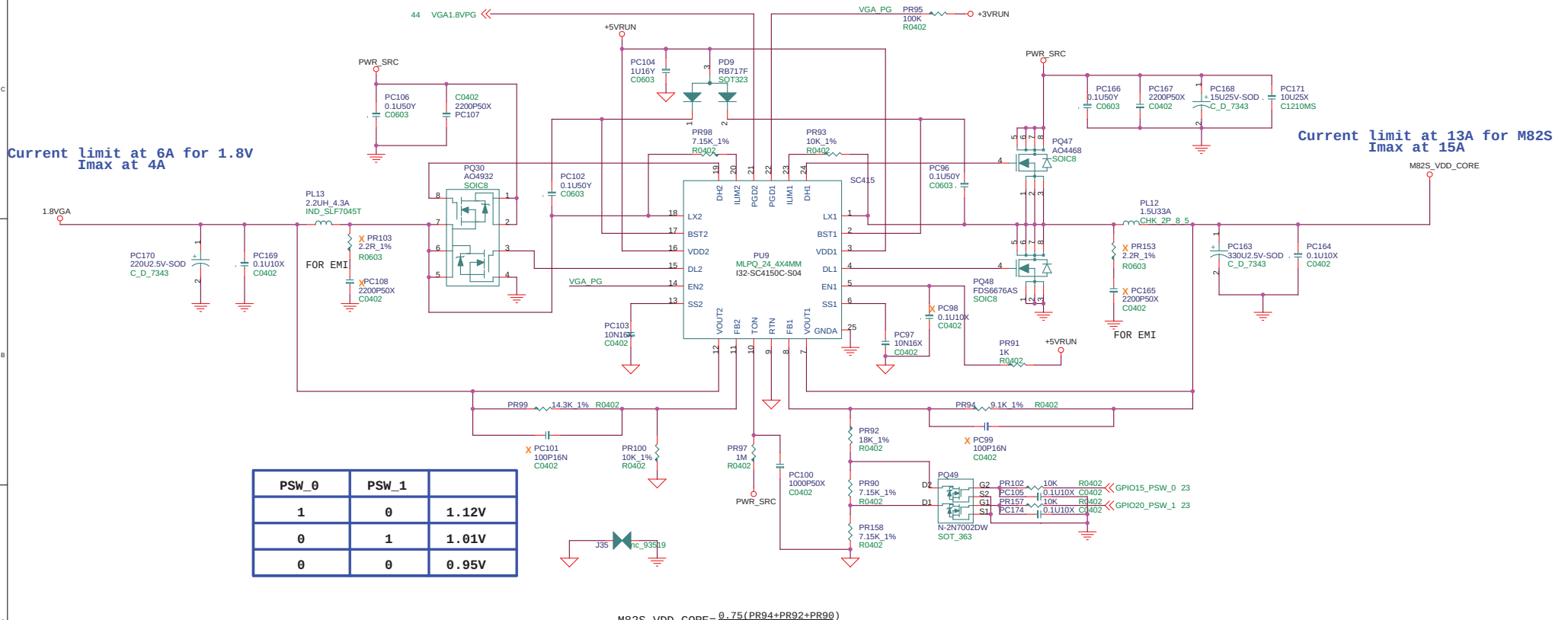




M82S

M82S_VDDC>1.8VRUN>1.2VRUN>1.1VRUN



PSW_0	PSW_1	
1	0	1.12V
0	1	1.01V
0	0	0.95V

$$M82S\_VDD\_CORE=\frac{0.75(PR94+PR92+PR90)}{PR92+PR90}$$

MICRO-STAR INT'L CO.,LTD.

Title: VGA POWER

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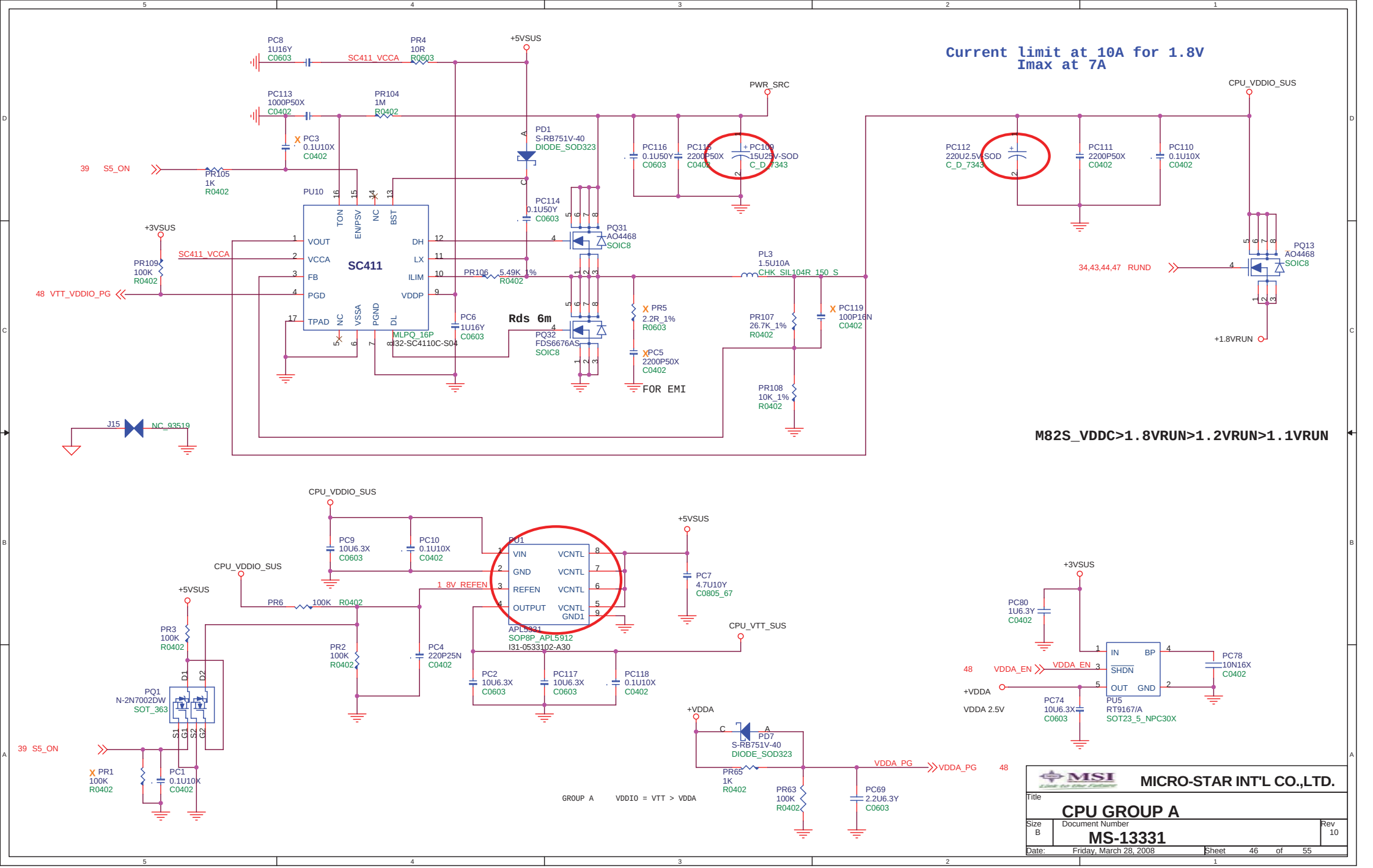
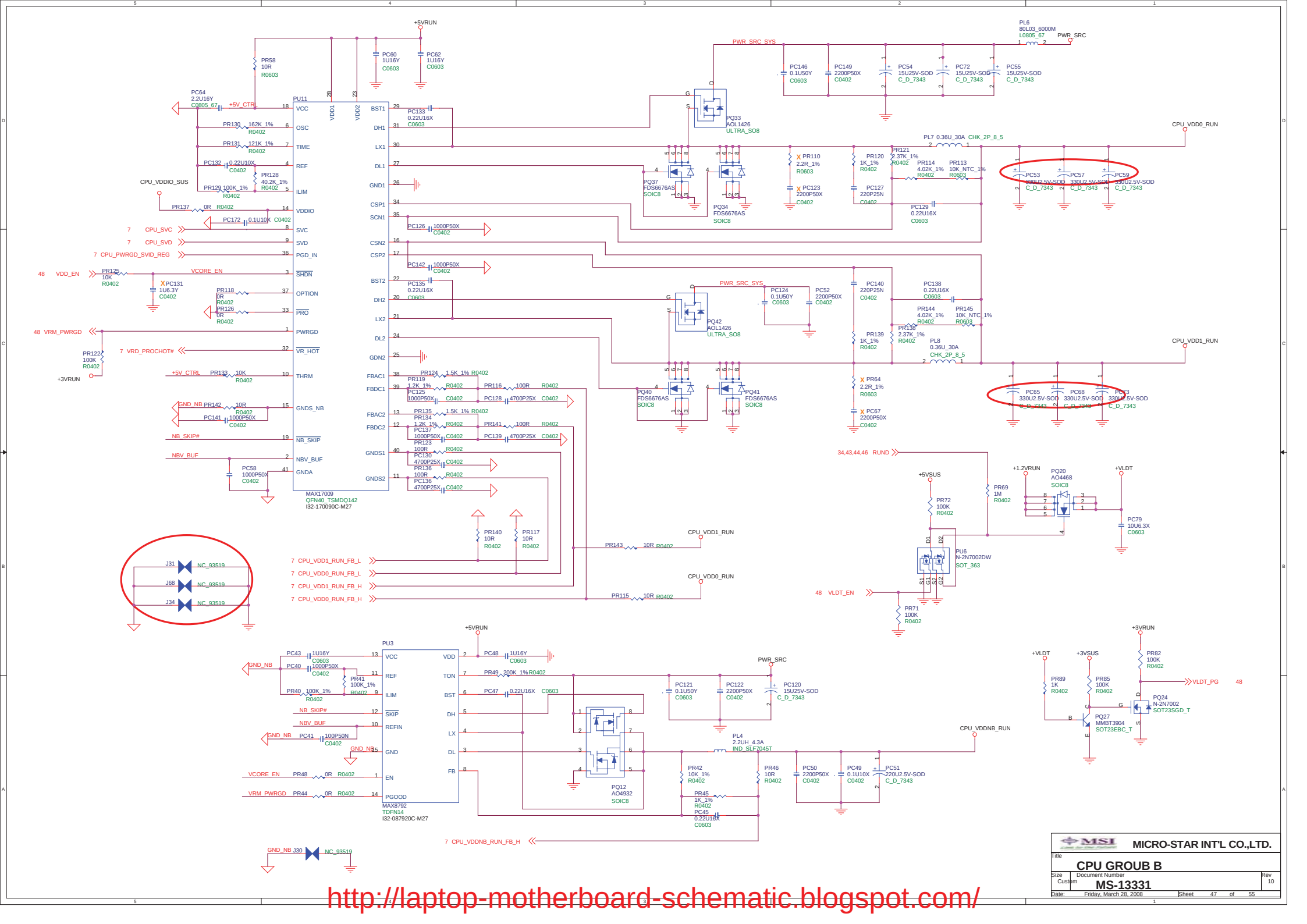
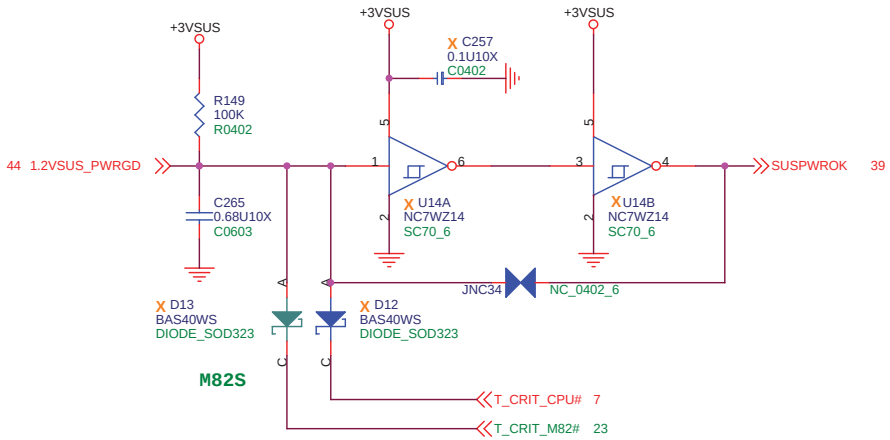
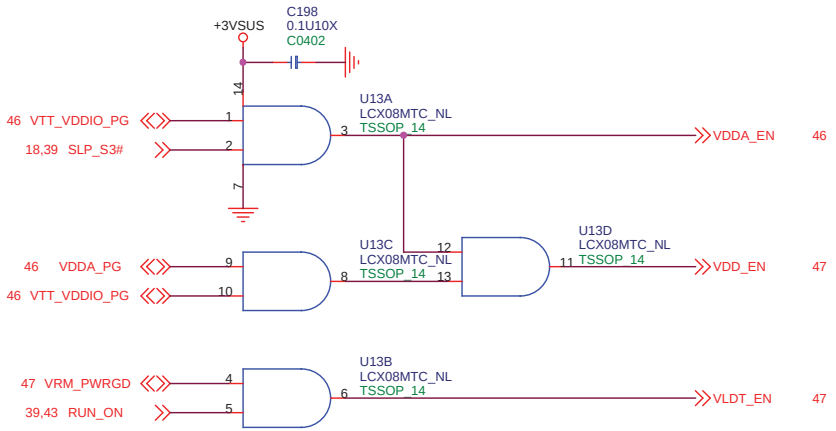
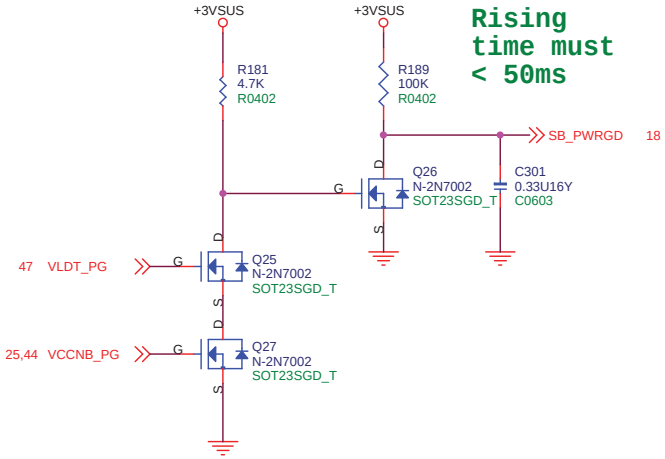
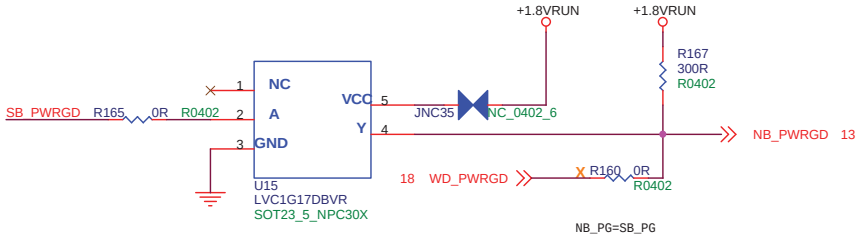




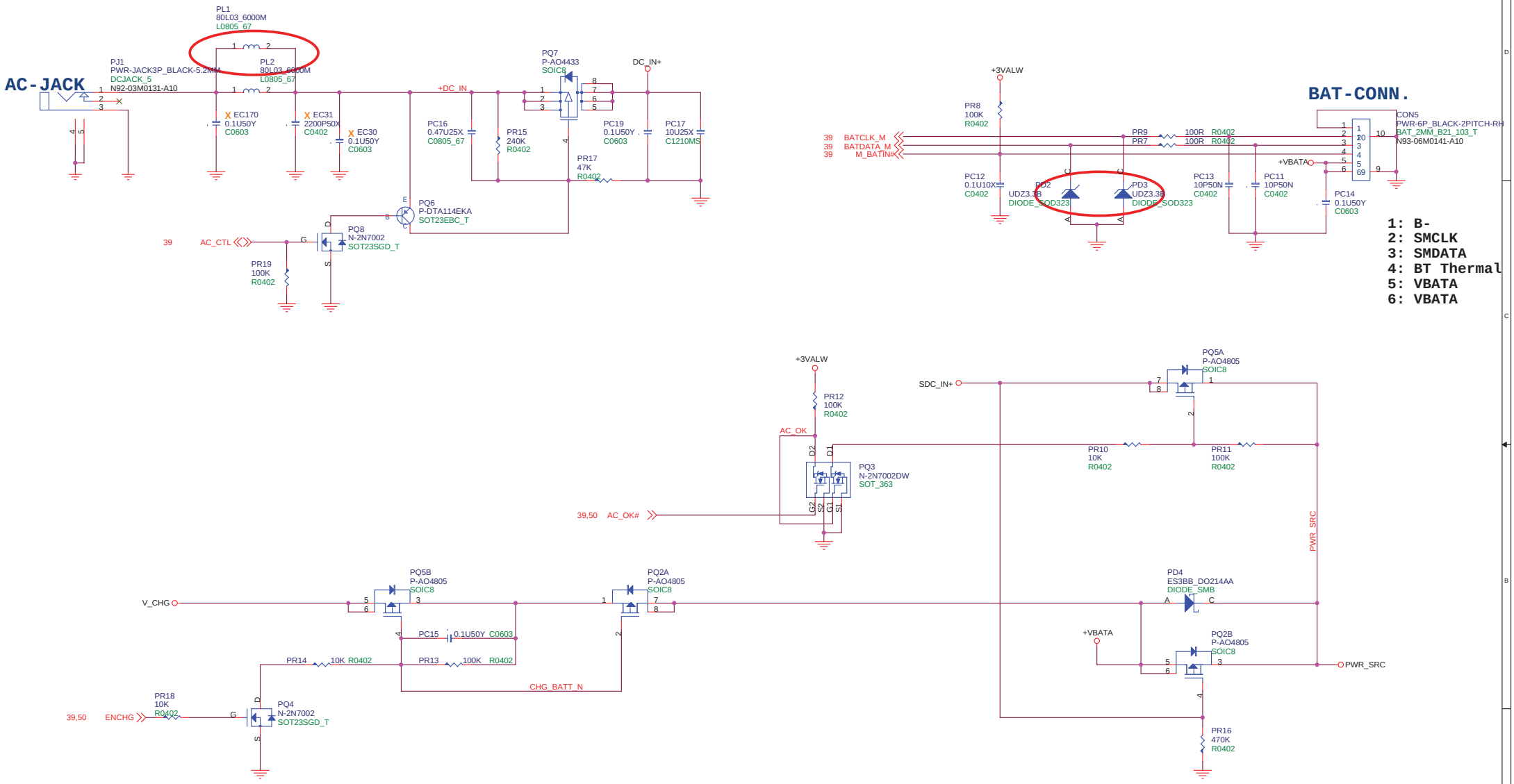








MICRO-STAR INT'L CO.,LTD.		
Title: PWRGD		
Size: B	Document Number: MS-13331	Rev: 10
Date: Friday, March 28, 2008	Sheet 48 of 55	



MICRO-STAR INT'L CO.,LTD.

Title: **Battery Select**

Size: Custom | Document Number: **MS-13331** | Rev: 10

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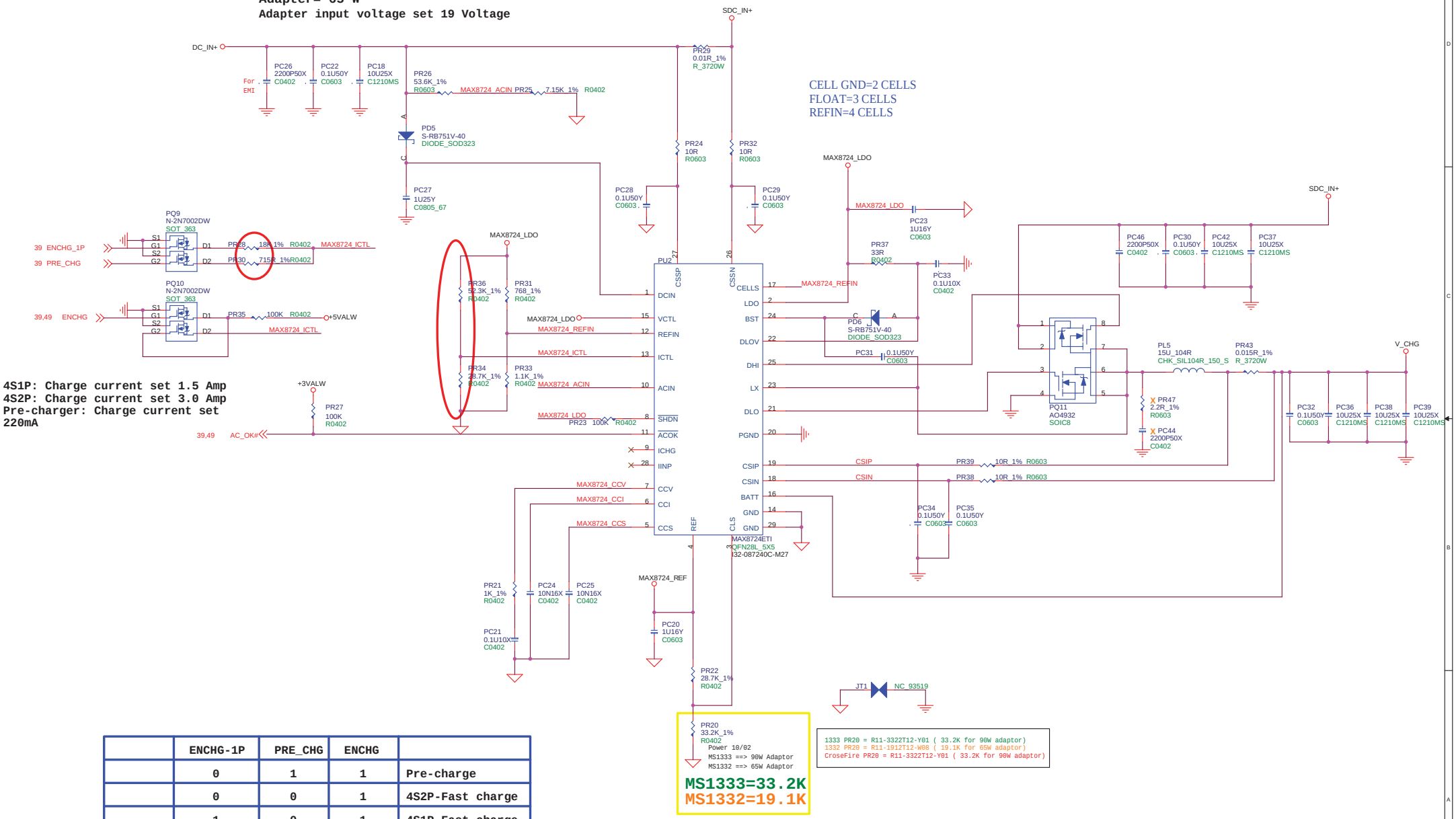
Adapter= 65 W
Adapter input voltage set 19 Voltage



4S1P: Charge current set 1.5 Amp
4S2P: Charge current set 3.0 Amp
Pre-charger: Charge current set 220mA

	ENCHG-1P	PRE_CHG	ENCHG	
	0	1	1	Pre-charge
	0	0	1	4S2P-Fast charge
	1	0	1	4S1P-Fast charge
	X	X	0	STOP CHARGE

MICRO-STAR INT'L CO.,LTD.

Title: M_Battery Charger

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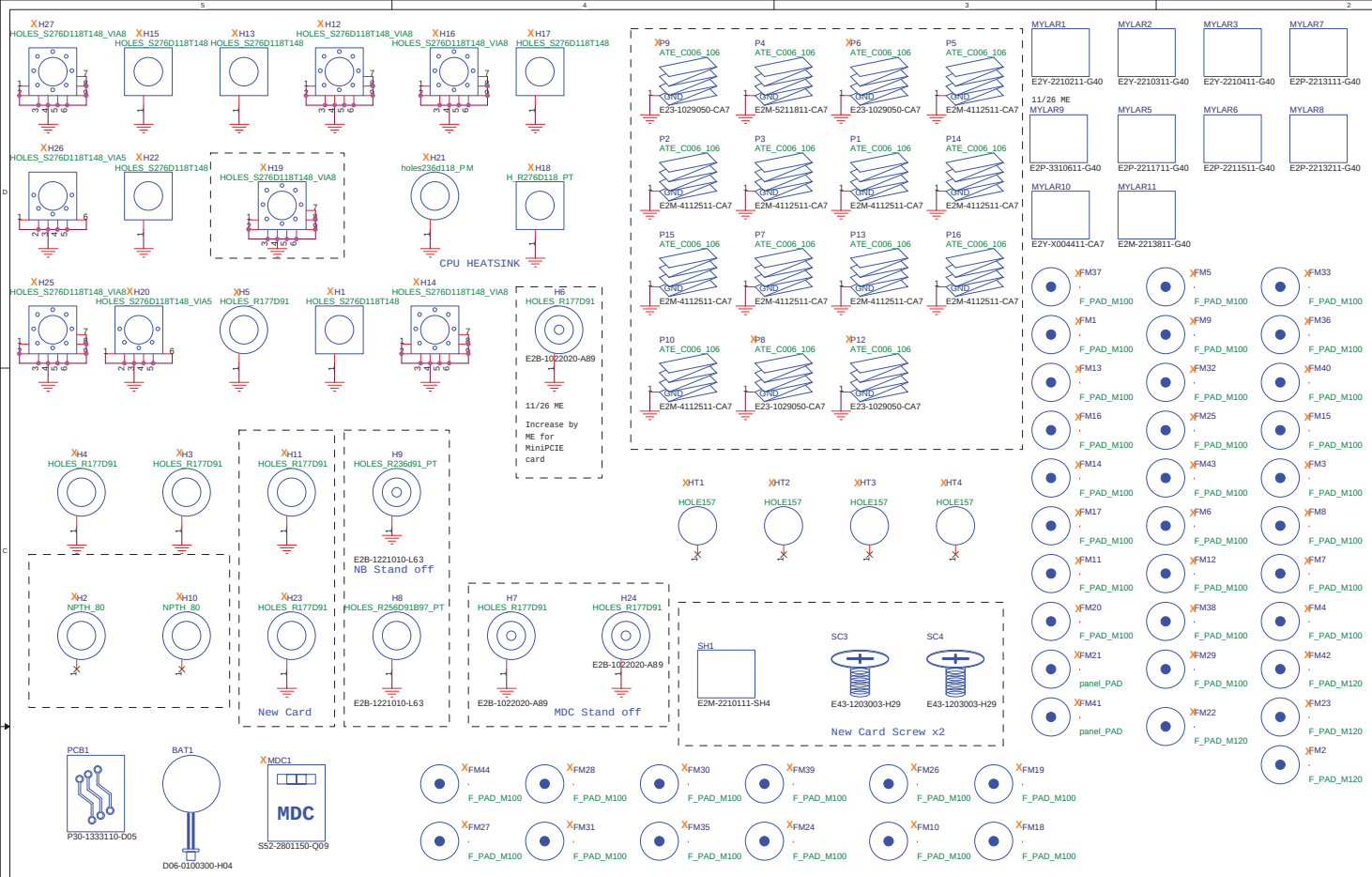
Date: Friday, March 28, 2008 | Sheet 50 of 55



Confirm footprint and hight with EMI & ME
2P1、P16、P7、P10 for 960MHz (E2M-4112511-CA7)
3P2、P3 for data strobe (E2M-4112511-CA7)
4P4、P5 for 865MHz (E2M-4112511-CA7)
5P15 for 865MHz (E2M-4112511-CA7)
6P14、P13 for 865MHz (E23-1003110-CA7)

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Title	ME Parts	
Size C	Document Number MS-13331	Rev 10
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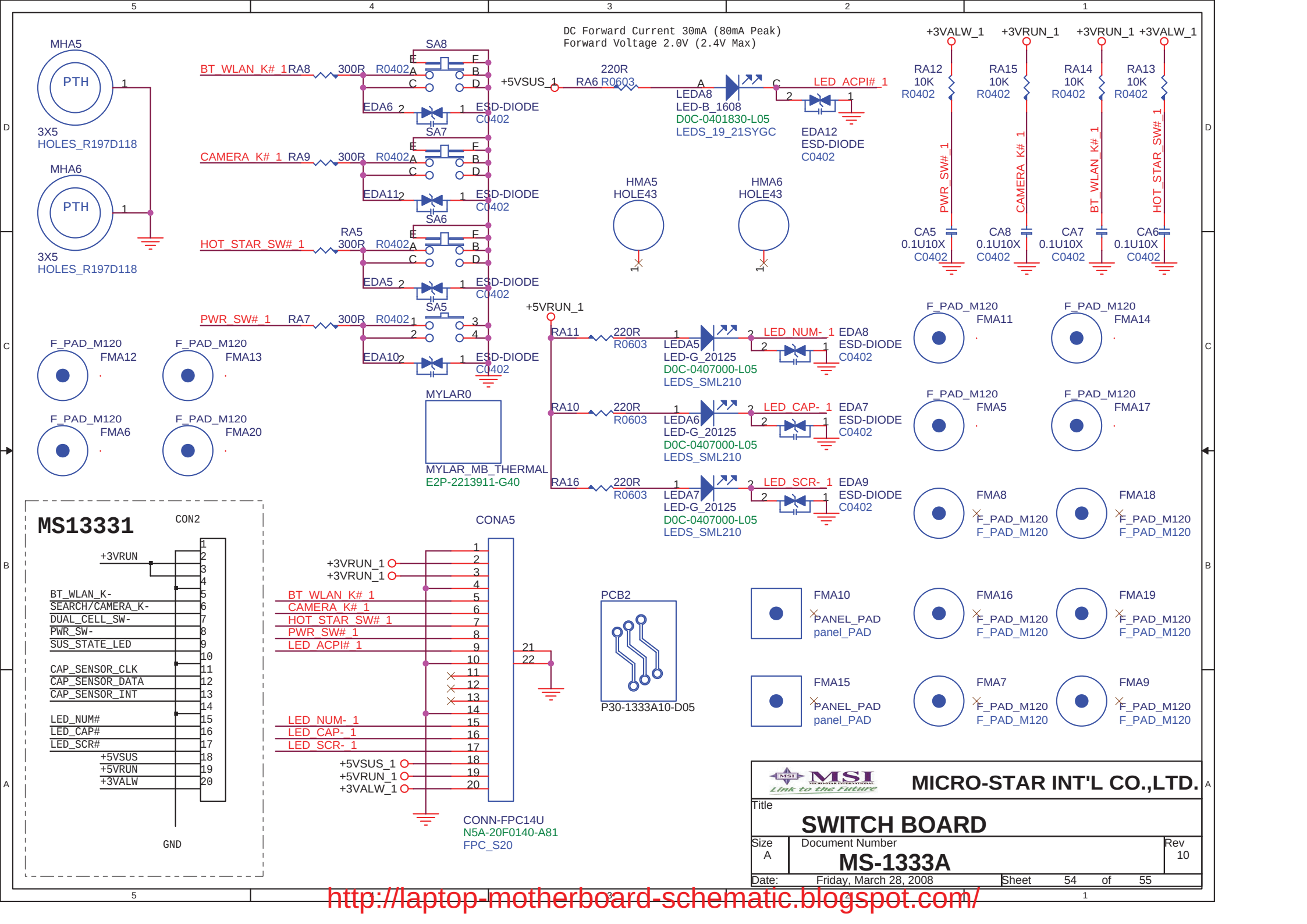

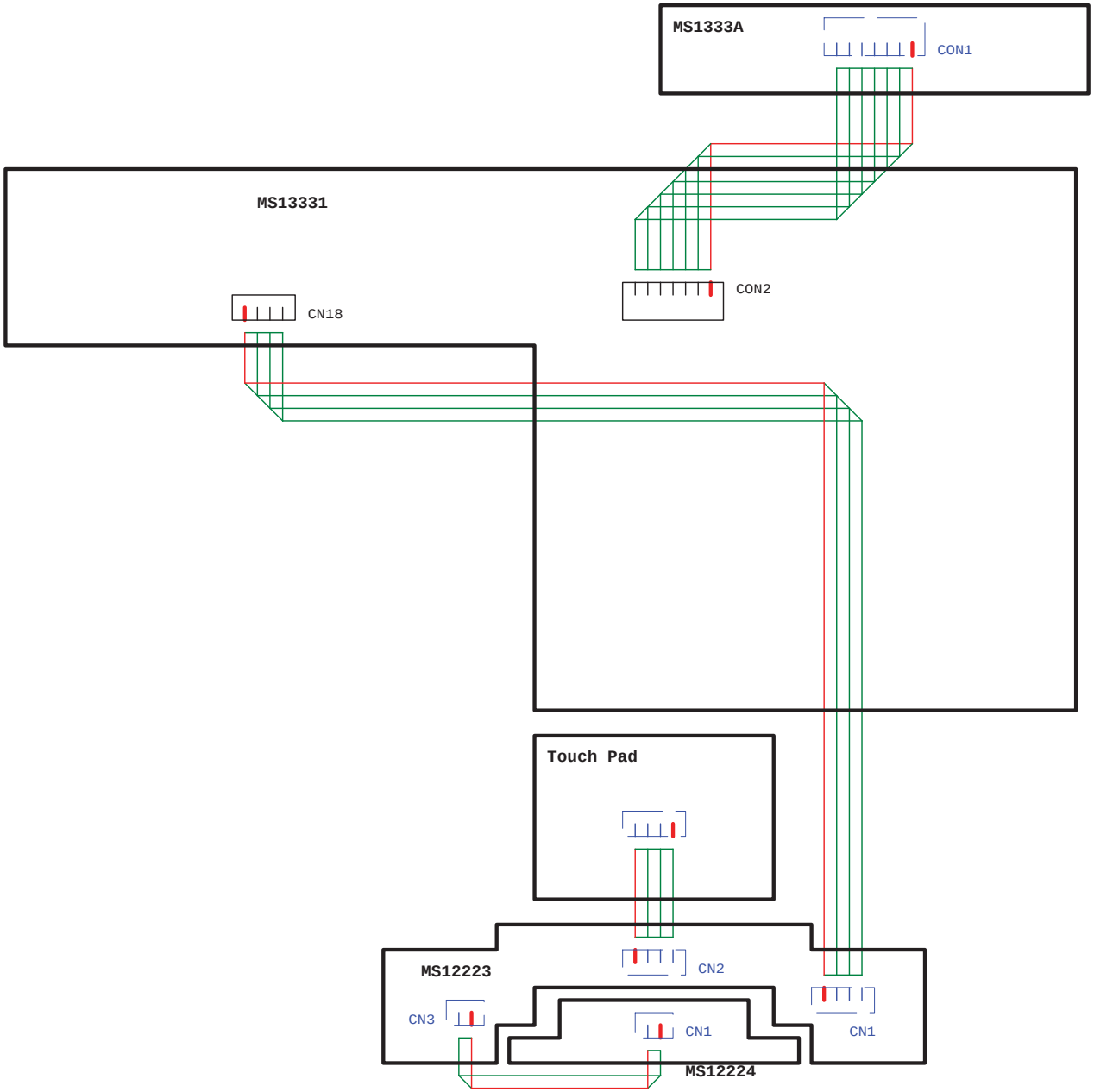

MS12221 Top side (black)
MS12222 Button side (blue)
MS12223 Button side (blue)
MS12224 Button side (blue)
Touch Pad Button side (blue)

FPC_S20
N5A-20F0140-A81

FPC_SD54548
N5A-12F0130-M06

FPC_6P_54550
N5A-06F0160-A81

Title: MS122XX architecture		
Size: B	Document Number: <Doc>	Rev: 1.0
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