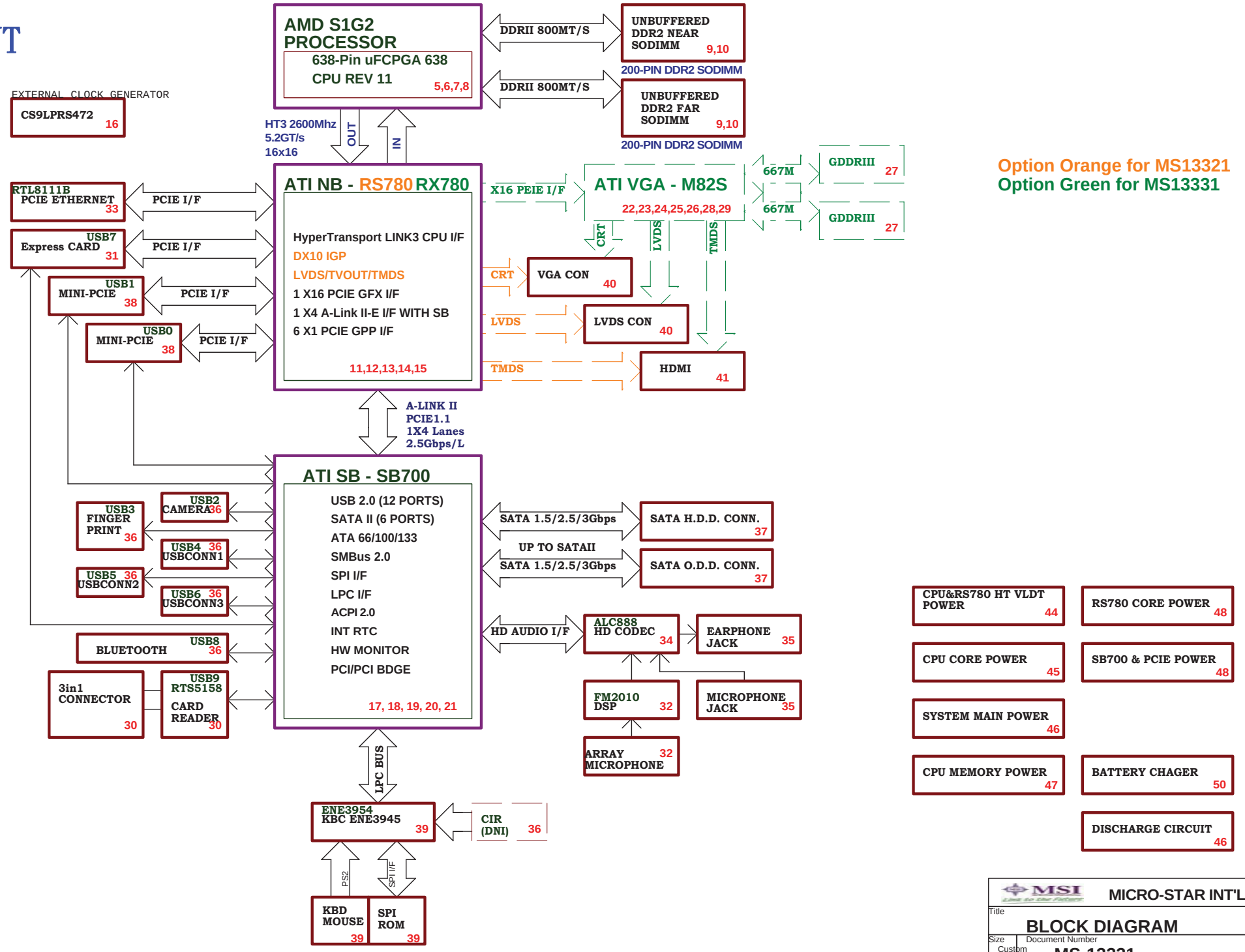
DVT



Option Orange for MS13321
Option Green for MS13331

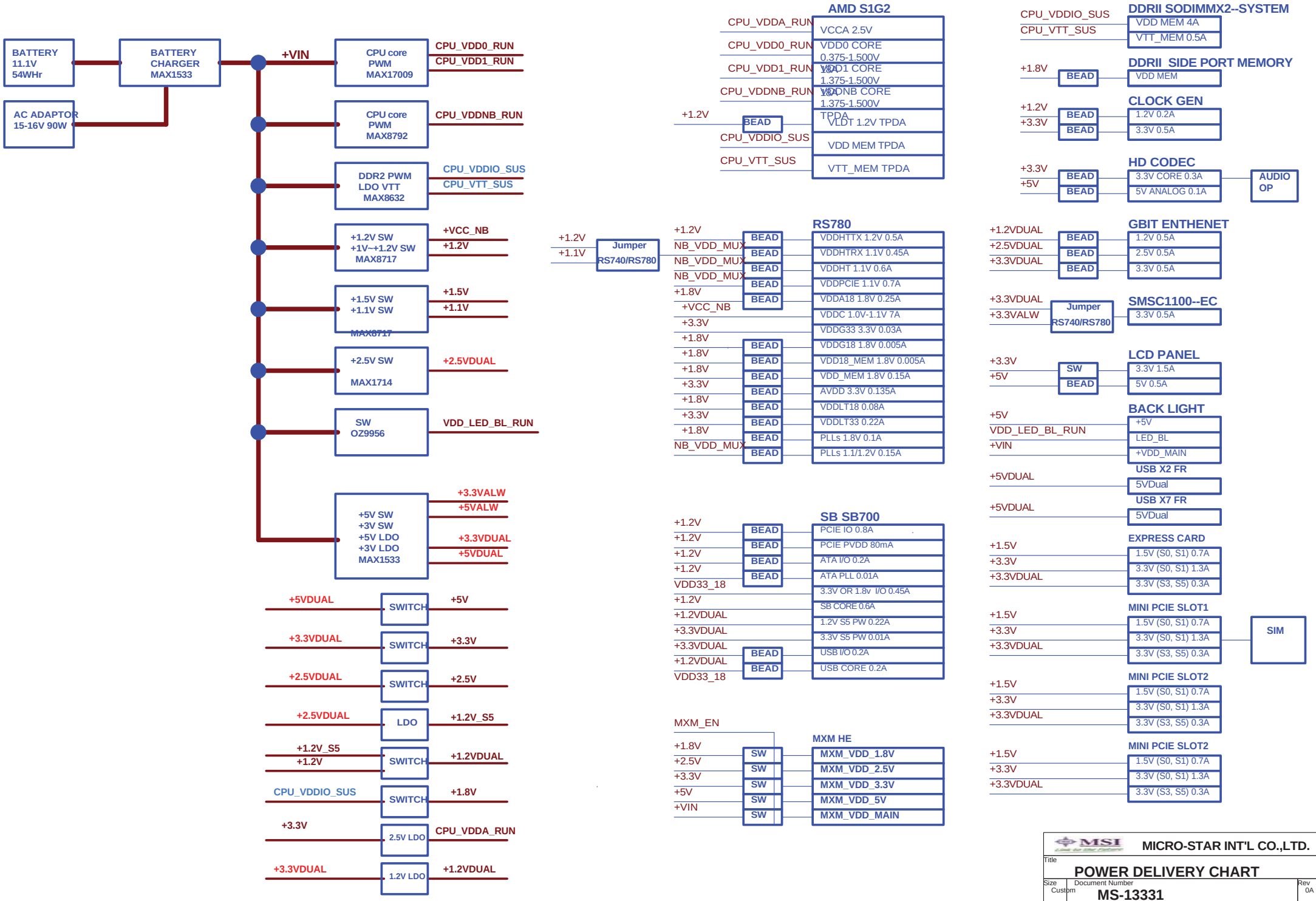
CPU&RS780 HT VLDT POWER 44
RS780 CORE POWER 48
CPU CORE POWER 45
SB700 & PCIE POWER 48
SYSTEM MAIN POWER 46
CPU MEMORY POWER 47
BATTERY CHAGER 50
DISCHARGE CIRCUIT 46

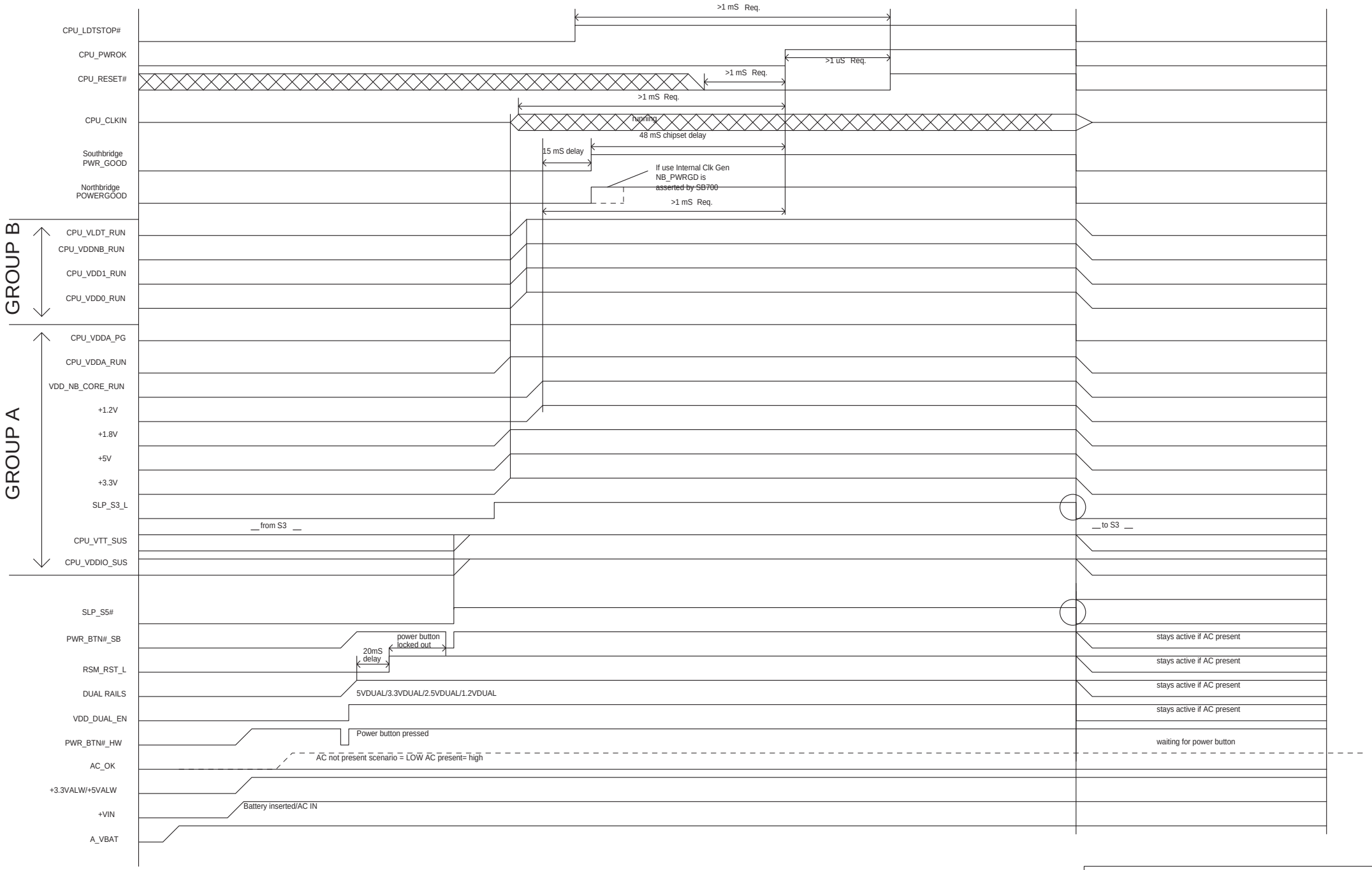
MSI MICRO-STAR INT'L CO.,LTD.

Title: BLOCK DIAGRAM

Size: Custom | Document Number: MS-13331 | Rev: 0A

Date: Monday, August 20, 2007 | Sheet 1 of 55



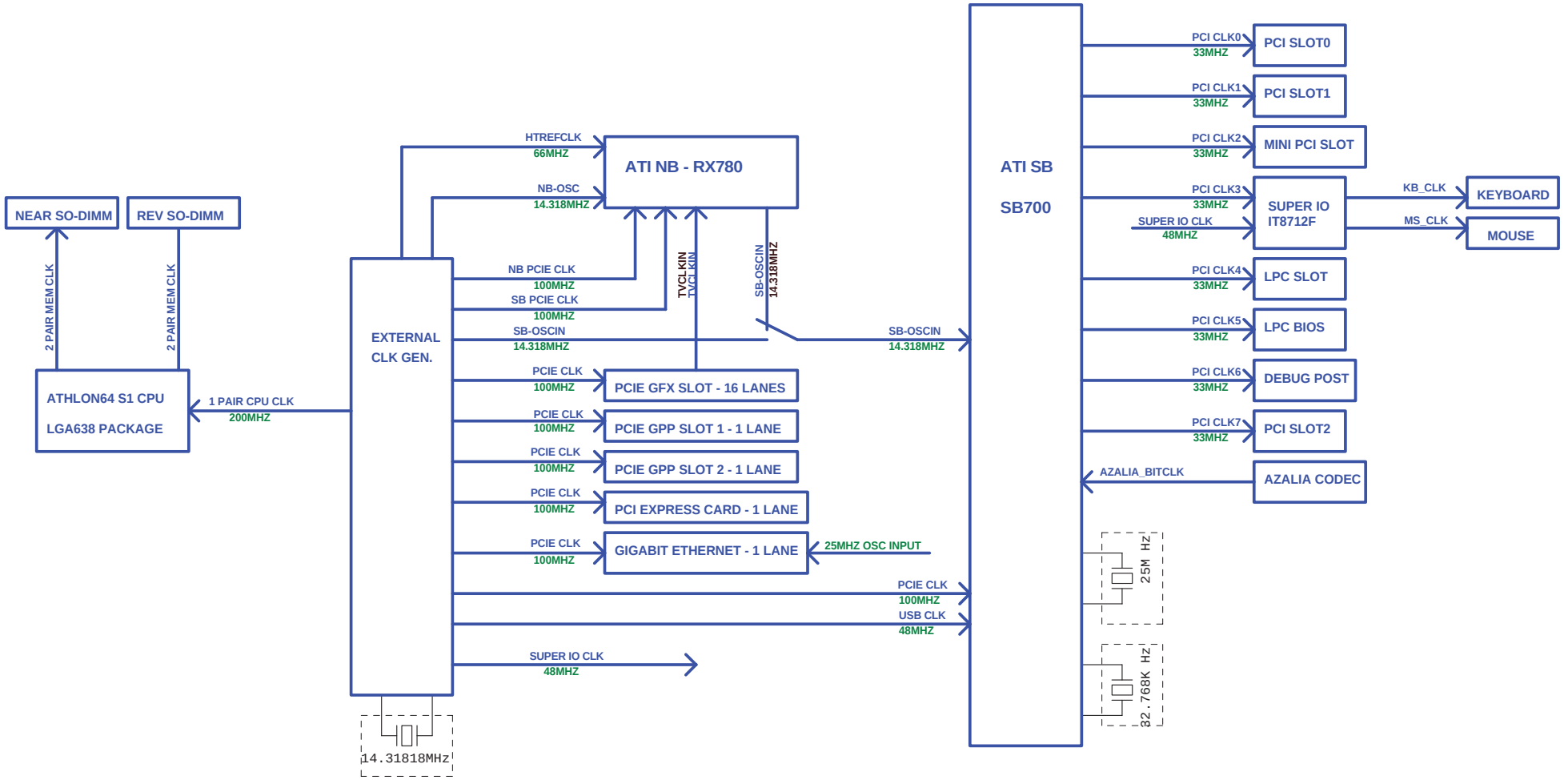


MICRO-STAR INT'L CO.,LTD.

Title: POWER SEQUENCE CHART

Size: Custom | Document Number: MS-13331 | Rev: 0A

Date: Monday, August 20, 2007 | Sheet 3 of 55

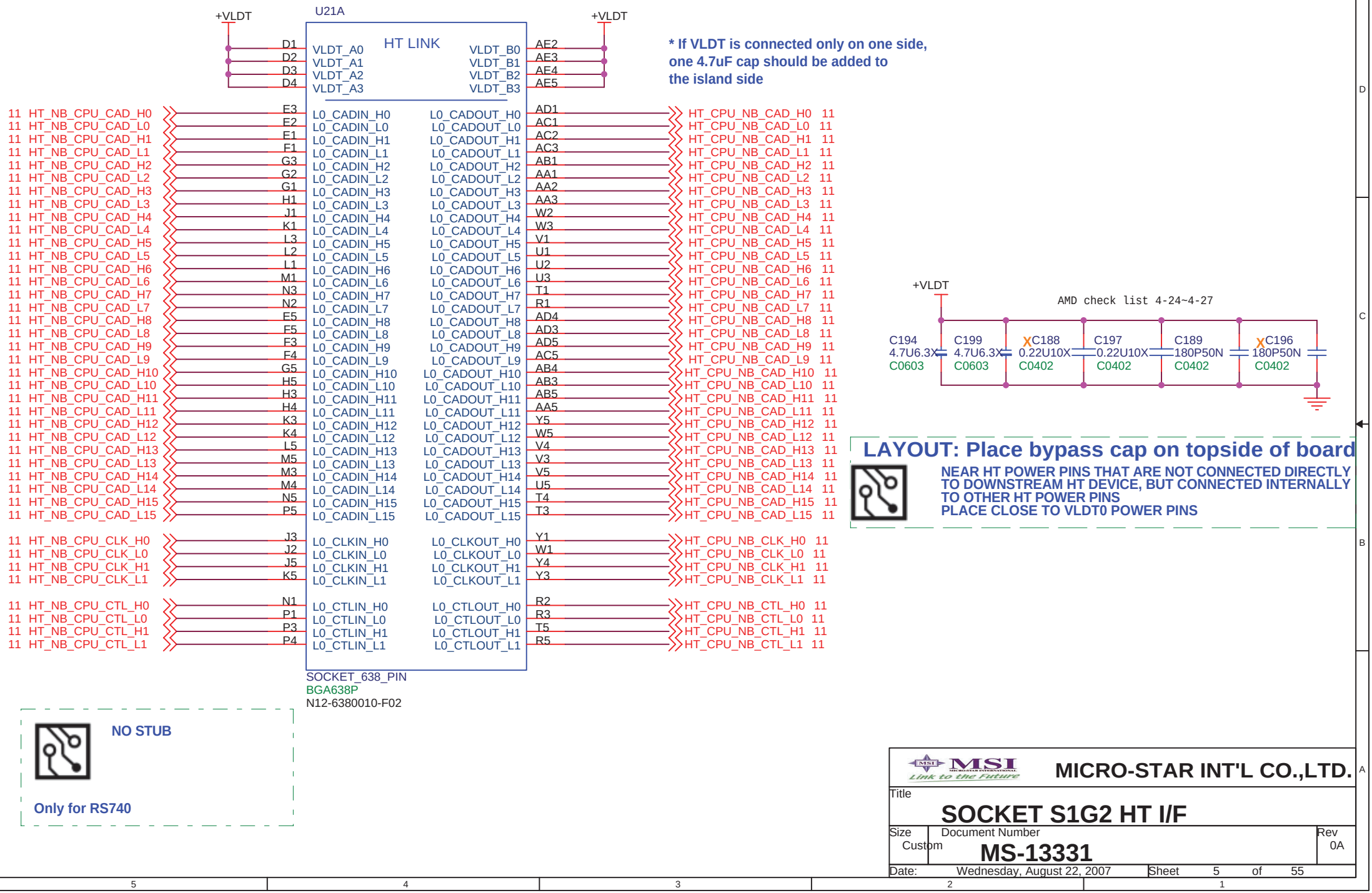


MICRO-STAR INT'L CO.,LTD.

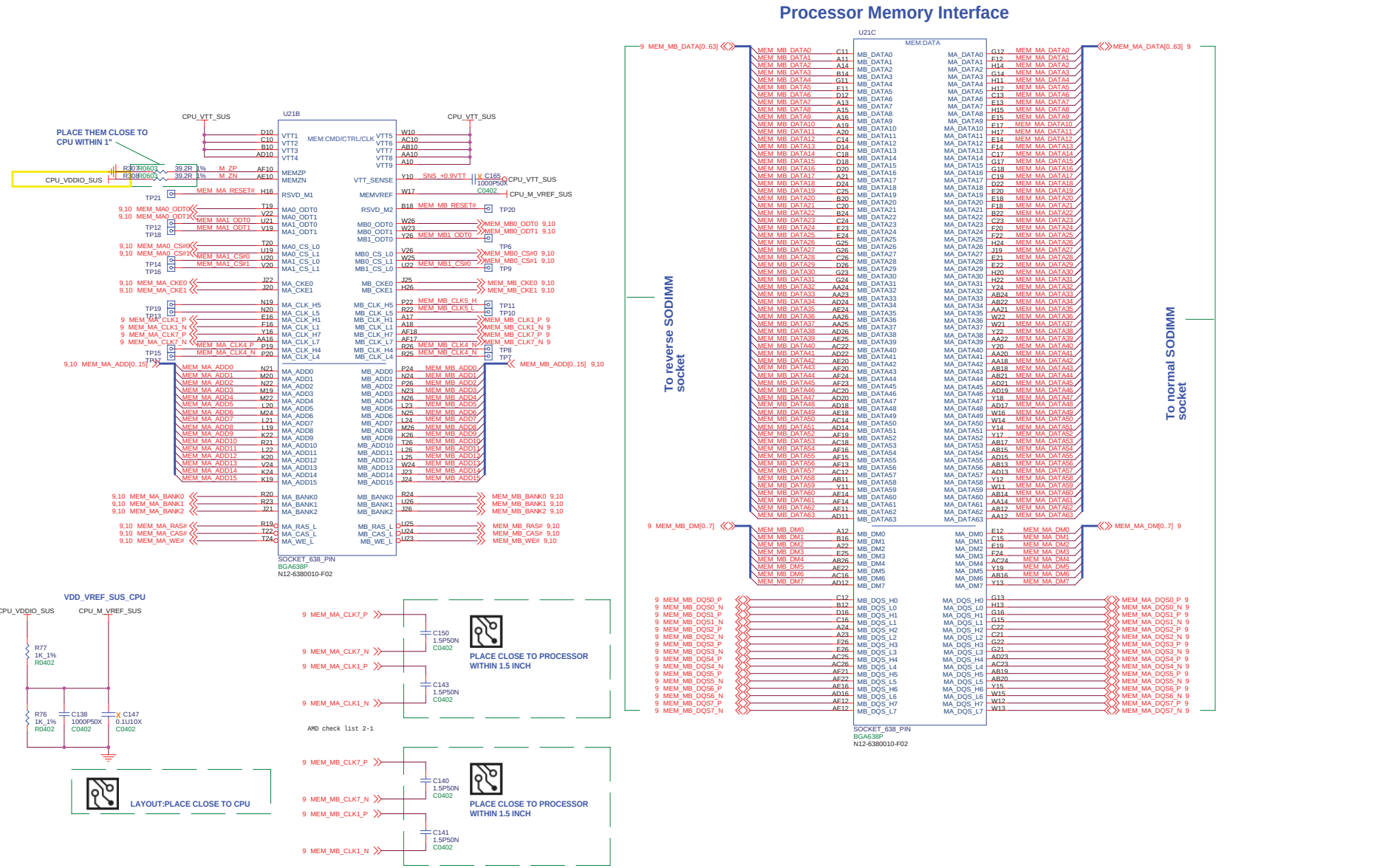
Title: CLOCK DISTRIBUTION

Size: Custom | Document Number: MS-13331 | Rev: 0A

Date: Monday, August 20, 2007 | Sheet 4 of 55



Processor Memory Interface



CPU_VDDA_2.5_RUN

maximun
40 ohm

VDDA 2.5V ==> Max Current 250mA

LAYOUT: ROUTE VDDA TRACE APPROX. 50 mils WIDE (USE 2x25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

+VDDA
AMD check list 4-22
L110L1000m_50 L0402
C176 4.7U6.3X C0603
C173 3300P50X C0402
C175 0.22U10X C0402

16 CPU_CLKP
16 CPU_CLKN
C542 3900P50X C0603
C543 3900P50X C0603
R318 169R_1% R0402

CPU_VDDA_RUN
Keep trace from resisor to CPU within 0.6"
keep trace from caps to CPU within 1.2"

U21D
F8 VDDA1
F9 VDDA2
A9 CLKIN_H
A8 CLKIN_L
CPU_CLKIN_SC_P
CPU_CLKIN_SC_N
B7 RESET_L
A7 PWROK
F10 LDTSTOP_L
C6 LDTREQ_L
LDT_RST#
PWRGD
LDT_STOP#
CPU_LDT_REQ#_CPU
AF4 SIC
AE5 SID
AE6 ALERT_L
CPU_SIC
CPU_SID
CPU_ALERT
R6 HT_REF0
P6 HT_REF1
CPU_HTREF0
CPU_HTREF1
R112 44.2R 1%R0603
R116 44.2R 1%R0603
TP33
If unused, the ALERT_L pin is left unconnected
place them to CPU within 1.5"
+VLDT

PWM
47 CPU_VDD0_RUN_FB_H
47 CPU_VDD0_RUN_FB_L
47 CPU_VDD1_RUN_FB_H
47 CPU_VDD1_RUN_FB_L
F6 VDD0_FB_H
E6 VDD0_FB_L
Y6 VDD1_FB_H
AB6 VDD1_FB_L

CPU_DBRDY
CPU_TMS
CPU_TCK
CPU_TRST#
CPU_TDI
CPU_TEST23_TSTUPD
CPU_TEST18_PLLTEST0
CPU_TEST19_PLLTEST1
CPU_TEST25_H_BYPASSCLK_H
CPU_TEST25_L_BYPASSCLK_L
CPU_TEST21_SCANEN
CPU_TEST20_SCANCLK2
CPU_TEST24_SCANCLK1
CPU_TEST22_SCANSHIFTEN
CPU_TEST12_SCANSHIFTENB
CPU_TEST27_SINGLECHAIN
CPU_TEST9_ANALOGIN
CPU_TEST6_DIECRACKMON
TP22 TP27 TP26 TP25 TP65 TP31 TP32

G10 DBRDY
AA9 TMS
AC9 TCK
AD9 TRST_L
AF9 TDI
AD7 TEST23
H10 TEST18
G9 TEST19
E9 TEST25_H
E8 TEST25_L
AB8 TEST21
AF7 TEST20
AE7 TEST24
AE8 TEST22
AC8 TEST12
AF8 TEST27
C2 TEST9
AA6 TEST6

A3 RSVD1
A5 RSVD2
B3 RSVD3
B5 RSVD4
C1 RSVD5
H18 RSVD10
H19 RSVD9
AA7 RSVD8
D5 RSVD7
C5 RSVD6

SOCKET_638_PIN
BGA638P
N12-6380010-F02

KEY1 M11
KEY2 W18
SVC A6 CPU_SVC_R
SVD A4 CPU_SVD_R
THERMTRIP_L AF6 CPU_THERMTRIP# 1.8V
PROCHOT_L AC7 CPU_PROCHOT# 1.8V
MEMHOT_L AA8 CPU_MEMHOT# 1.8V
THERMDC W7 CPU_THERMDC
THERMDA W8 CPU_THERMDA

R78 300R R0402
R80 300R R0402
R83 300R R0402
CPU_VDDIO_SUS
R79 10K R0402
R81 10K R0402
R82 10K R0402
Q11 SMBT3904 SOT23EBC_T
Q10 SMBT3904 SOT23EBC_T
Q12 SMBT3904 SOT23EBC_T
CPU_MEMHOT# 10,18
CPU_PROCHOT# 17
CPU_THERMTRIP# 18

47 VRD_PROCHOT#
JNC26 NC_0402_6
CPU_PROCHOT#_1.8V

PWM
VDDIO_FB_H W9 VDDIO 46
VDDIO_FB_L Y9
VDDNB_FB_H H6 CPU_VDDNB_RUN_FB_H 47
VDDNB_FB_L G6
DBREQ_L E10 CPU_DBREQ#
TDO AE9 CPU_TDO
TEST28_H J7 CPU_TEST28_H_PLLCHRZ_P
TEST28_L H8 CPU_TEST28_L_PLLCHRZ_N
TEST17 D7 CPU_TEST17_BP3
TEST16 E7 CPU_TEST16_BP2
TEST15 F7 CPU_TEST15_BP1
TEST14 C7 CPU_TEST14_BP0
TEST7 C3 CPU_TEST7_ANALOG_T
TEST10 K8 CPU_TEST10_ANALOGOUT
TEST8 C4 CPU_TEST8_DIG_T
TEST29_H C9 CPU_TEST29_H_FBCLKOUT_P
TEST29_L C8 CPU_TEST29_L_FBCLKOUT_N

TP23 TP64 TP35 TP30 TP66 TP34 TP37 TP29 TP36 TP28 TP24

route as differential as short as possible testpoint under package

CPU_VDDIO_SUS
CPU_TEST25_H_BYPASSCLK_H R311 510R R0402
CPU_TEST27_SINGLECHAIN R90 300R R0402
CPU_TEST21_SCANEN R105 300R R0402
CPU_TEST20_SCANCLK2 R92 300R R0402
CPU_TEST24_SCANCLK1 R93 300R R0402
CPU_TEST22_SCANSHIFTEN R91 300R R0402
CPU_TEST12_SCANSHIFTENB R109 300R R0402
CPU_TEST15_BP1 R113 300R R0402
CPU_TEST14_BP0 R327 300R R0402
CPU_TEST19_PLLTEST1 R108 300R R0402
CPU_TEST18_PLLTEST0 R95 300R R0402
CPU_TEST25_L_BYPASSCLK_L R313 510R R0402
CPU_TEST9_ANALOGIN R338 0R R0402

CPU_VDDIO_SUS
R103 390R R0402
R110 390R R0402
R94 1K R0402
CPU_ALERT
CPU_SIC
CPU_SID

+1.8VRUN +1.8VRUN +1.8VRUN
R339 300R R0402
R106 300R R0402
R340 300R R0402
17 CPU_PWRGD
13,17 CPU_LDT_STOP#
13,17 CPU_LDT_RST#
CPU_LDT_REQ#_CPU
JNC44 NC_0402_6 PWRGD
JNC27 NC_0402_6 LDT_STOP#
JNC45 NC_0402_6 LDT_RST#
JNC46 NC_0402_6 CPU_LDT_REQ# 13

Cap close to thermal sensor
+3VSUS
CPU_THERMDA
C158 2200P50X C0402
CPU_THERMDC
48 T_CRIT_CPU#
U10
1 VDD
2 D+
3 D-
4 T_CRIT_A#
8 SMBCLK
7 SMBDATA
6 ALERT#
5 GND
SMB_THRMCPU_CLK 8 SMB_THRMCPU_CLK 39
SMB_THRMCPU_DATA 7 SMB_THRMCPU_DATA 39
CPU_THRM_ALERT- 6 CPU_THRM_ALERT- 18,39
C200 0.1U10X C0402
LM86CIMMXNOPB_MSOP8-RH
MSOP8_T
Close to CPU socket

RN18 8P4R-10K RN0402_MSI
+3VSUS
1 2 T_CRIT_CPU#
3 4 SMB_THRMCPU_CLK
5 6 SMB_THRMCPU_DATA
7 8 CPU_THRM_ALERT-

CPU_VDDIO_SUS
R102 1K R0402
R312 1K R0402
R101 2.2K R0402
CPU_SVC_R JNC30 NC_0402_6 CPU_SVC 47
CPU_SVD_R JNC42 NC_0402_6 CPU_SVD 47
PWRGD JNC29 NC_0402_6 CPU_PWRGD_SVID_REG 47
CPU_PWRGD Pull up to 1.8VRun

PWM

MSI MICRO-STAR INT'L CO.,LTD.
Title: SOCKET S1G2 CTRL
Size: Custom
Document Number: MS-13331
Rev: 0A
Date: Wednesday, August 22, 2007
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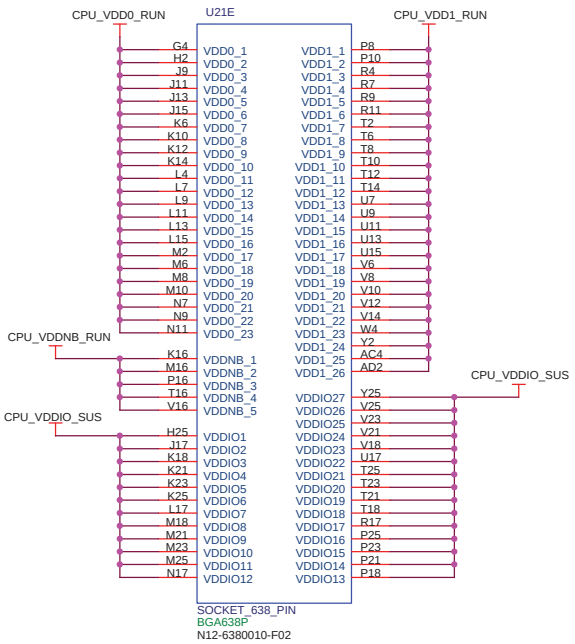
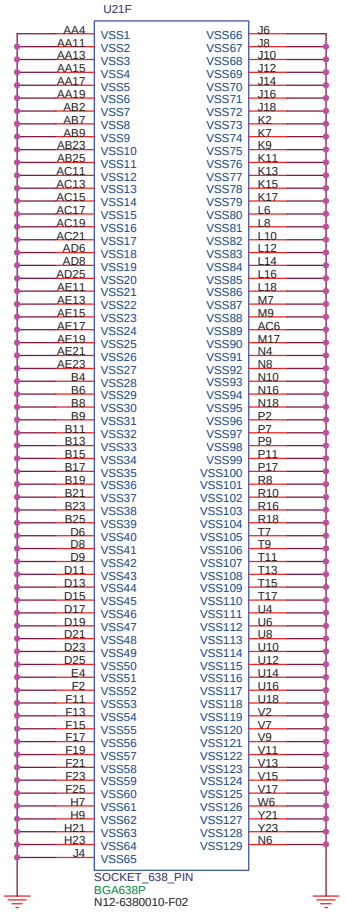
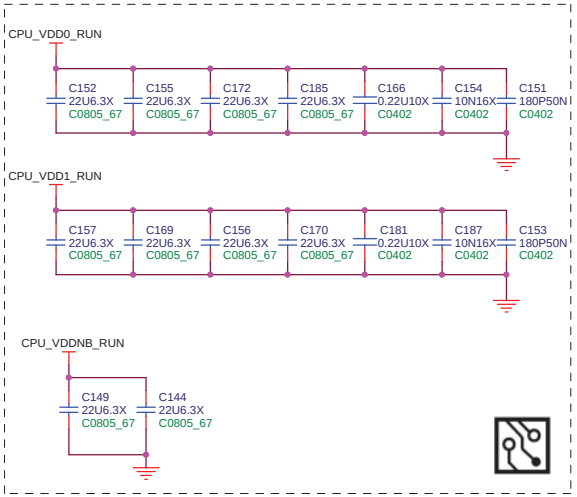
PROCESSOR POWER AND GROUND

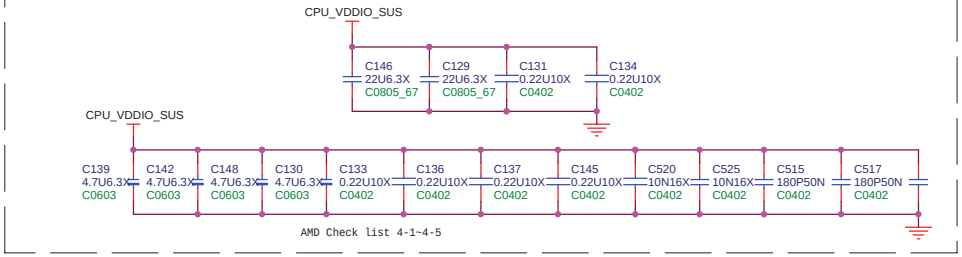


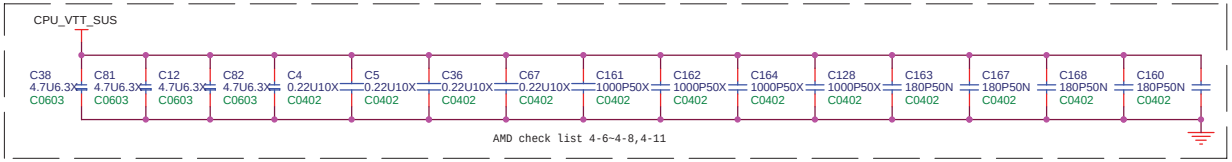


BOTTOMSIDE DECOUPLING



DECOUPLING BETWEEN PROCESSOR AND DIMMs
PLACE CLOSE TO PROCESSOR AS POSSIBLE



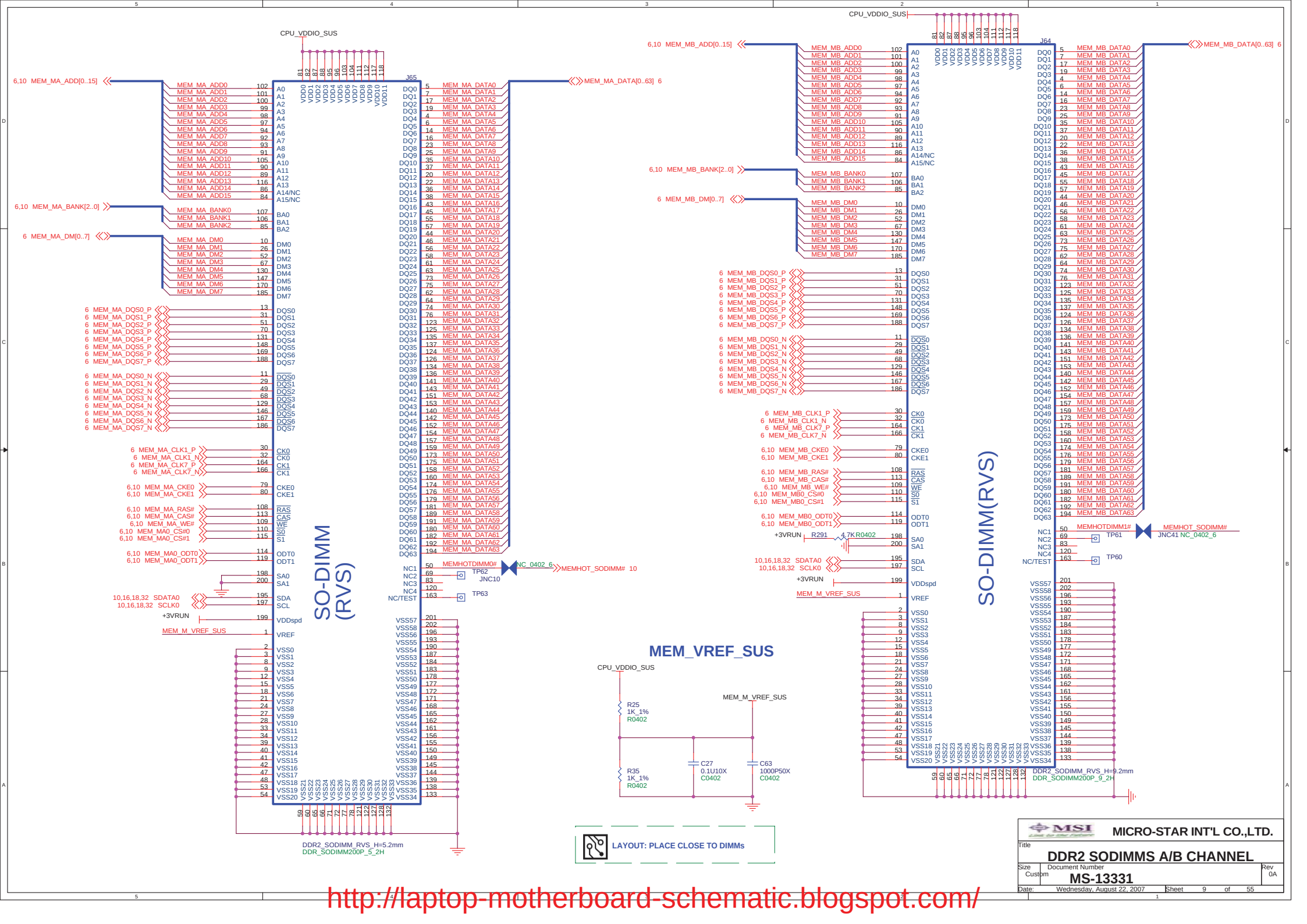


MICRO-STAR INT'L CO.,LTD.

Title: SOCKET S1G2 PWR & GND

Size: Custom | Document Number: MS-13331 | Rev: 0A

Date: Wednesday, August 22, 2007 | Sheet 8 of 55

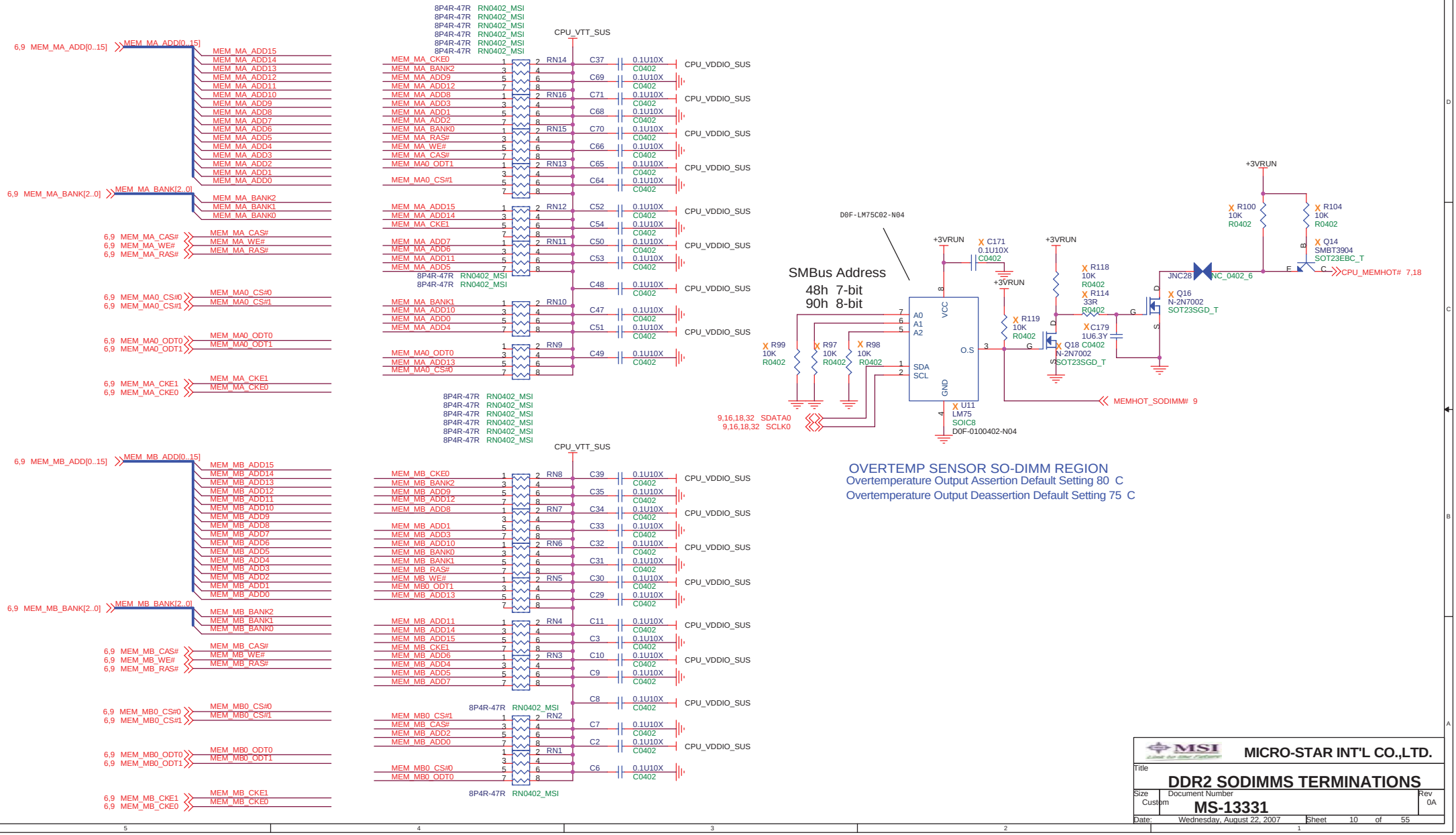


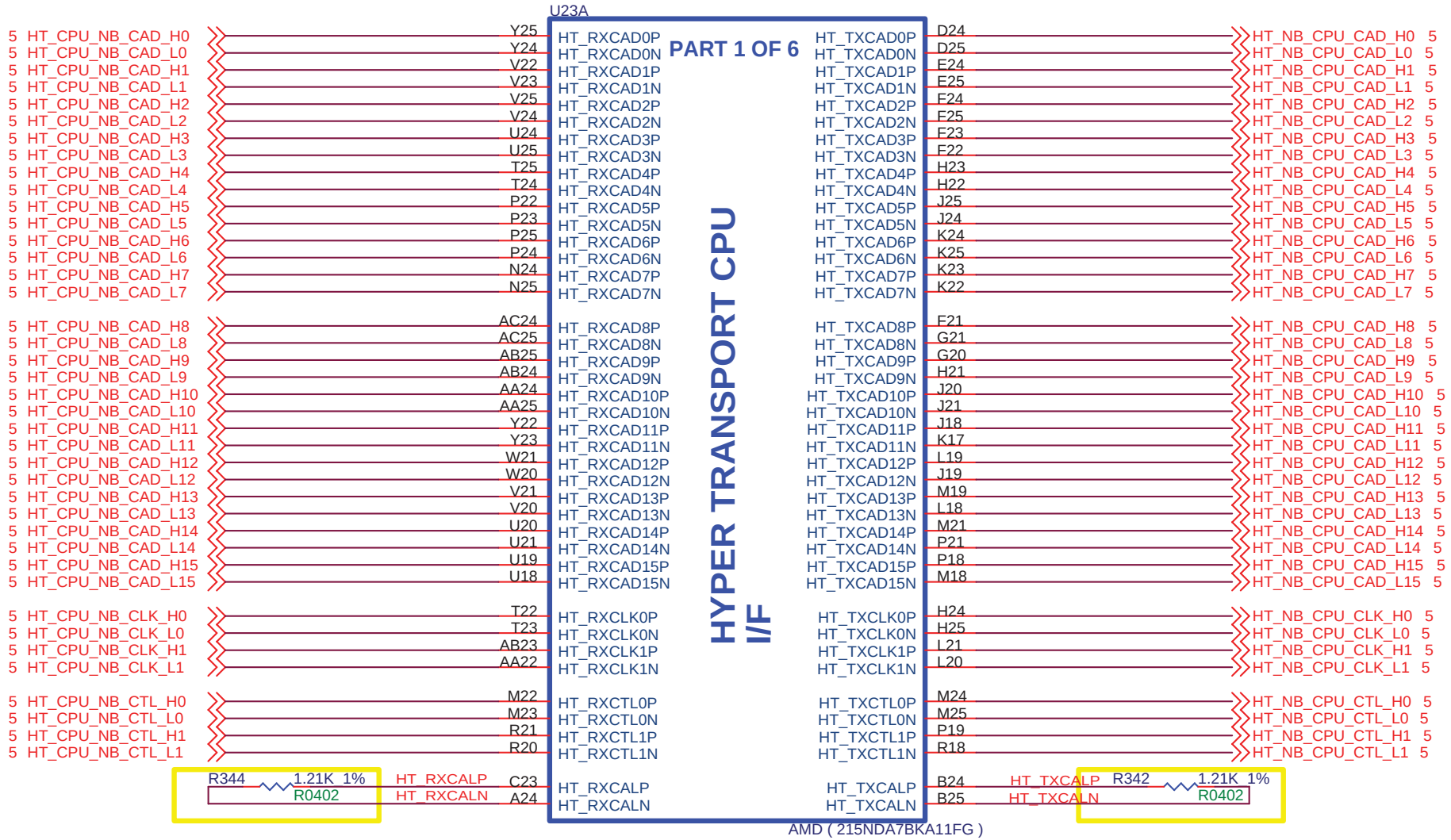
MICRO-STAR INT'L CO.,LTD.

Title: DDR2 SODIMMS A/B CHANNEL

Size: Custom | Document Number: MS-13331 | Rev: 0A

Date: Wednesday, August 22, 2007 | Sheet 9 of 55





Adobe Acrobat Professional - [PA_RS780A3.pdf]

RS740/RX780/RS780 HT Link Differences:

Pin Name	RS740	RX780	RS780
HT_RXCALP	49.9R to GND	1.21K from HT_RXCALP to HT_RXCALN	301R from HT_RXCALP to HT_RXCALN
HT_RXCALN	49.9R to VDDHT	1.21K from HT_RXCALP to HT_RXCALN	301R from HT_RXCALP to HT_RXCALN
HT_TXCALP HT_TXCALN	100R from HT_TXCALP to HT_TXCALN	1.21K from HT_TXCALP to HT_TXCALN	301R from HT_TXCALP to HT_TXCALN

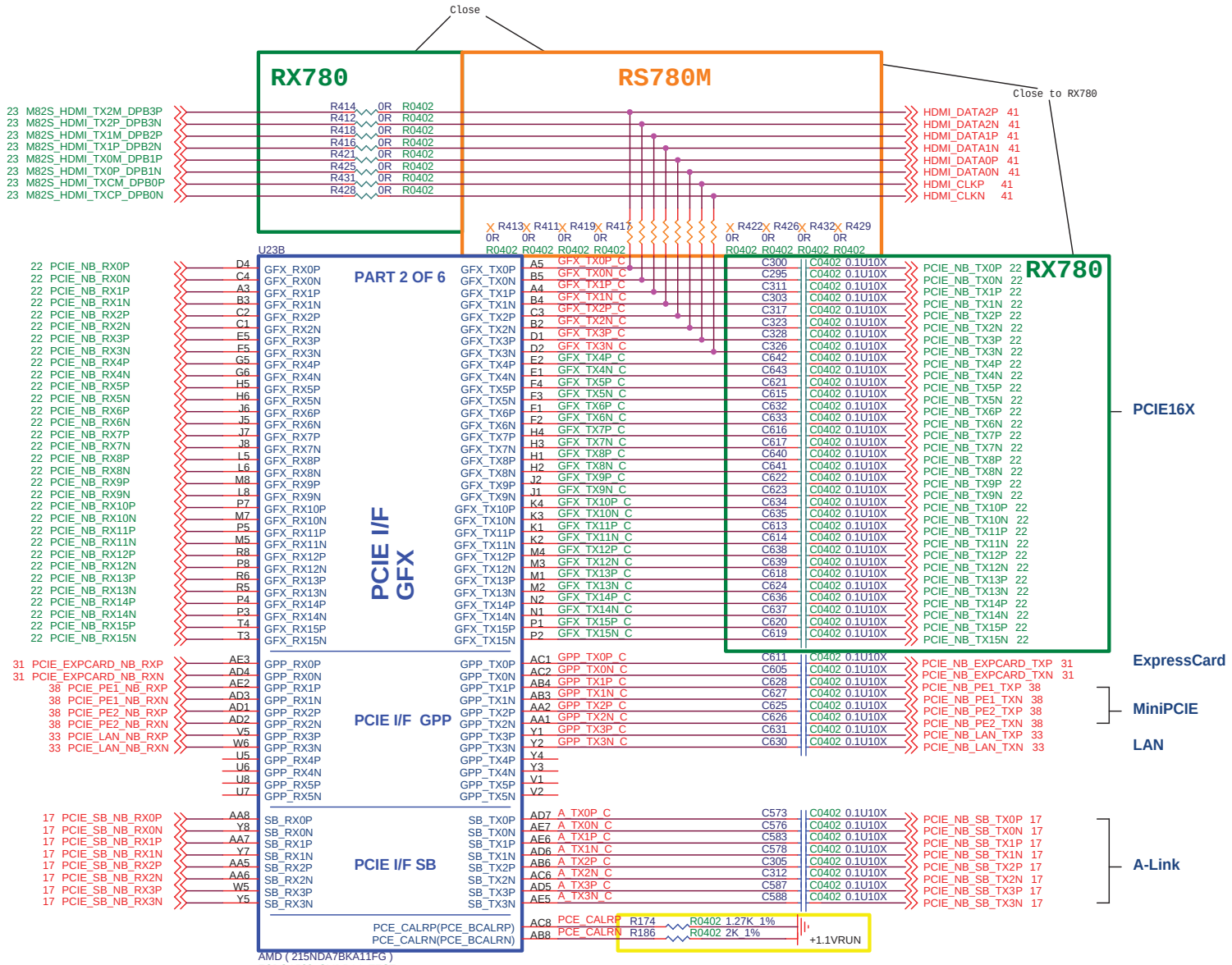
MSI Link to the Future

MICRO-STAR INT'L CO.,LTD.

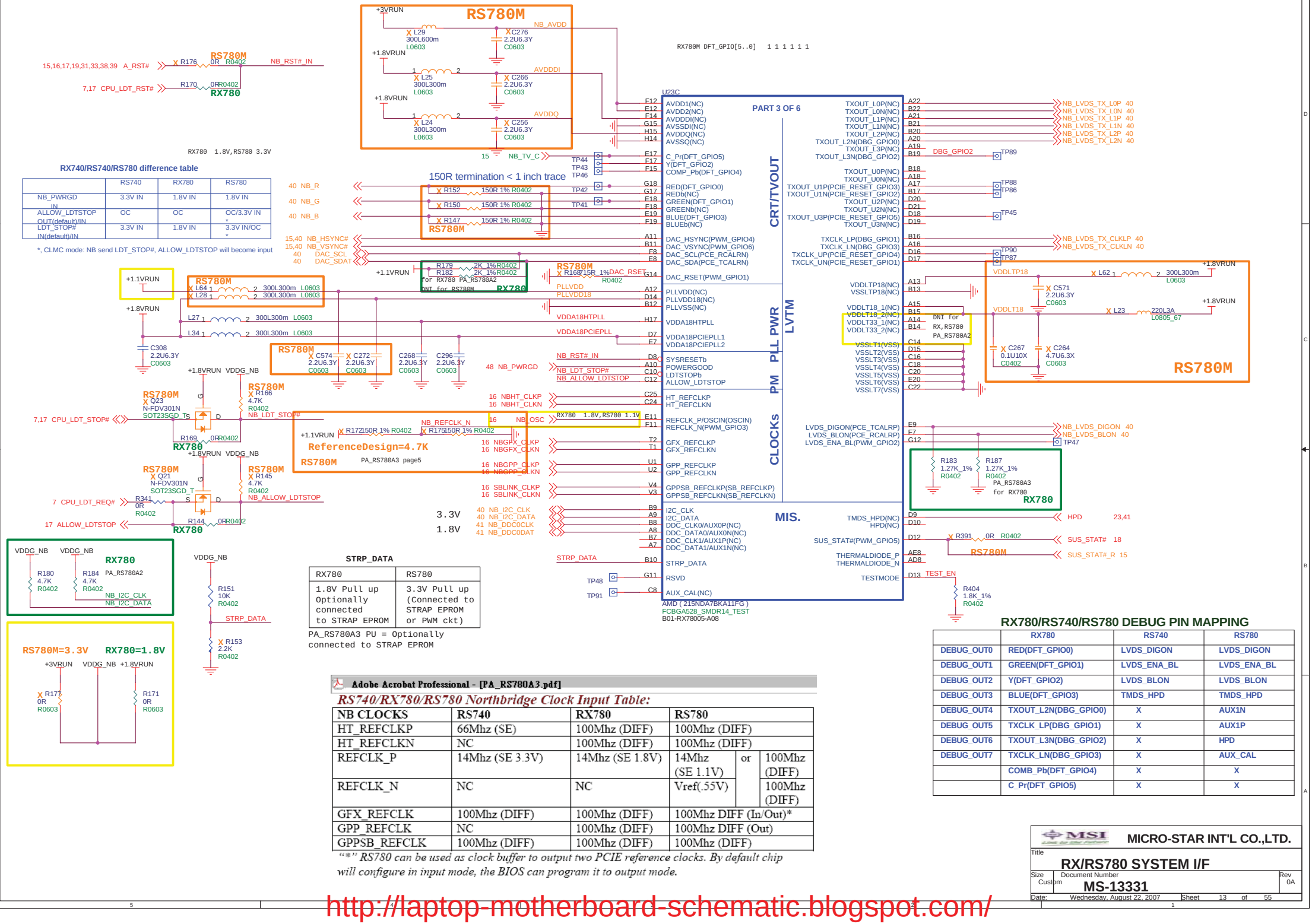
Title: RX/RS780 HT LINK I/F

Size: A | Document Number: MS-13331 | Rev: 0A

Date: Wednesday, August 22, 2007 | Sheet 11 of 55



Company	MICRO-STAR INT'L CO.,LTD.
Title	RX/RS780 PCI-E LINK&GPP
Size	B
Document Number	MS-13331
Rev	0A
Date:	Wednesday, August 22, 2007
Sheet	12 of 55



STRP_DATA

RX780	RS780
1.8V Pull up Optionally connected to STRAP EPROM	3.3V Pull up (Connected to STRAP EPROM or PWM ckt)

Adobe Acrobat Professional - [PA_RS780A3.pdf]

RS740/RX780/RS780 Northbridge Clock Input Table:

NB CLOCKS	RS740	RX780	RS780		
HT_REFCLKP	66Mhz (SE)	100Mhz (DIFF)	100Mhz (DIFF)		
HT_REFCLKN	NC	100Mhz (DIFF)	100Mhz (DIFF)		
REFCLK_P	14Mhz (SE 3.3V)	14Mhz (SE 1.8V)	14Mhz (SE 1.1V)	or	100Mhz (DIFF)
REFCLK_N	NC	NC	Vref(.55V)		100Mhz (DIFF)
GFX_REFCLK	100Mhz (DIFF)	100Mhz (DIFF)	100Mhz DIFF (In/Out)*		
GPP_REFCLK	NC	100Mhz (DIFF)	100Mhz DIFF (Out)		
GPPSB_REFCLK	100Mhz (DIFF)	100Mhz (DIFF)	100Mhz (DIFF)		

"" RS780 can be used as clock buffer to output two PCIE reference clocks. By default chip will configure in input mode, the BIOS can program it to output mode.*

MICRO-STAR INT'L CO.,LTD.

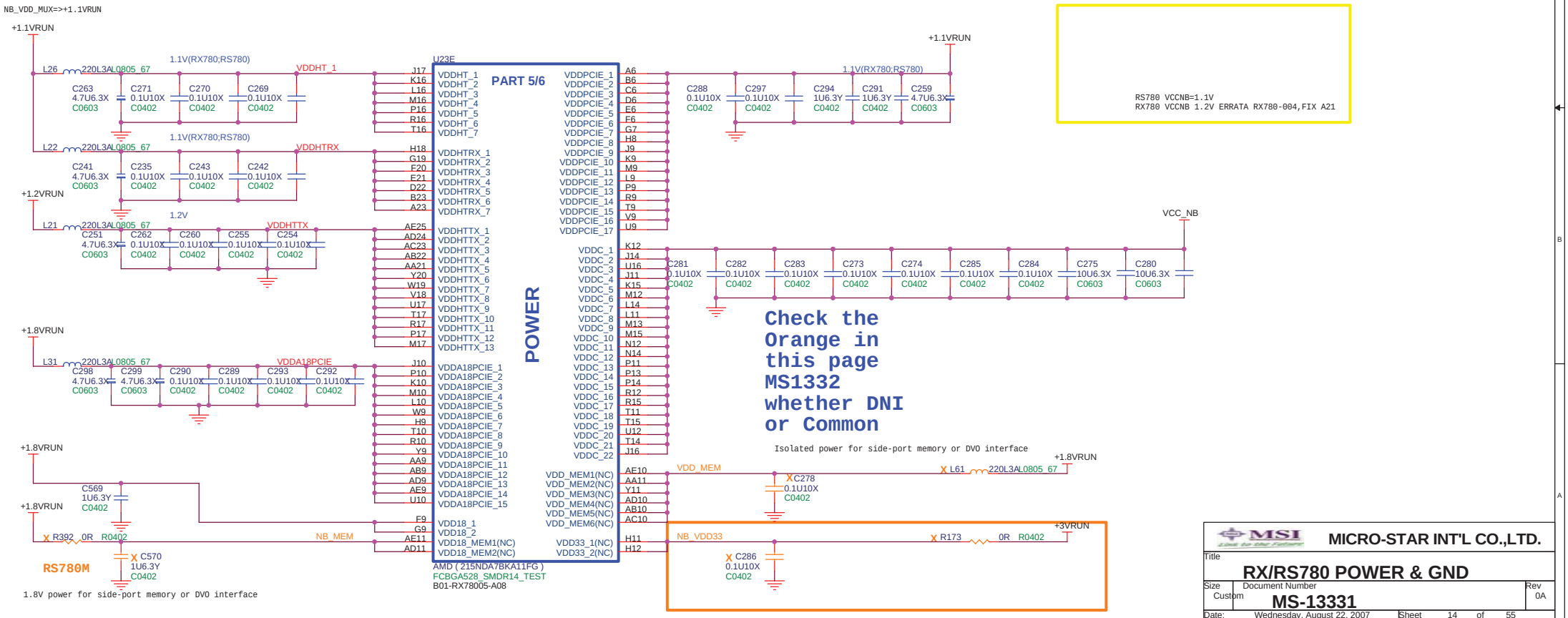
Title: RX/RS780 SYSTEM I/F

Size: Custom | Document Number: MS-13331 | Rev: 0A

Date: Wednesday, August 22, 2007 | Sheet 13 of 55

RS740/RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVDD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDDG18	+1.8V	+1.8V	+1.8V	PLLVDD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVDD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V/1.5V	NC	+1.8V/1.5V	VDDLTP18	+1.8V	NC	+1.8V
VDDG33	+3.3V	NC	+3.3V	VDDLT18	+1.8V	NC	+1.8V
IOPLLVDD18	+1.8V	NC	+1.8V	VDDLT33	+3.3V	NC	NC



MSI	MICRO-STAR INT'L CO.,LTD.		
Title	RX/RS780 POWER & GND		
Size: Custom	Document Number: MS-13331		Rev: 0A
Date: Wednesday, August 22, 2007	Sheet 14 of 55		

U23D

PAR 4 OF 6

SBD_MEM/DVO_I/F

AB12	MEM_A0(NC)	MEM_DQ0/DVO_VSYNC(NC)	AA18
AE16	MEM_A1(NC)	MEM_DQ1/DVO_HSYNC(NC)	AA20
V11	MEM_A2(NC)	MEM_DQ2/DVO_DE(NC)	AA19
AE15	MEM_A3(NC)	MEM_DQ3/DVO_D0(NC)	Y19
AA12	MEM_A4(NC)	MEM_DQ4(NC)	V17
AB16	MEM_A5(NC)	MEM_DQ5/DVO_D1(NC)	AA17
AB14	MEM_A6(NC)	MEM_DQ6/DVO_D2(NC)	AA15
AD14	MEM_A7(NC)	MEM_DQ7/DVO_D4(NC)	Y15
AD13	MEM_A8(NC)	MEM_DQ8/DVO_D3(NC)	AC20
AD15	MEM_A9(NC)	MEM_DQ9/DVO_D5(NC)	AD19
AC16	MEM_A10(NC)	MEM_DQ10/DVO_D6(NC)	AE22
AE13	MEM_A11(NC)	MEM_DQ11/DVO_D7(NC)	AC18
AC14	MEM_A12(NC)	MEM_DQ12(NC)	AB20
Y14	MEM_A13(NC)	MEM_DQ13/DVO_D9(NC)	AD22
		MEM_DQ14/DVO_D10(NC)	AC22
AD16	MEM_BA0(NC)	MEM_DQ15/DVO_D11(NC)	AD21
AE17	MEM_BA1(NC)		
AD17	MEM_BA2(NC)	MEM_DQS0P/DVO_IDCKP(NC)	Y17
		MEM_DQS0N/DVO_IDCKN(NC)	W18
W12	MEM_RASb(NC)	MEM_DQS1P(NC)	AD20
Y12	MEM_CASb(NC)	MEM_DQS1N(NC)	AE21
AD18	MEM_WEb(NC)		
AB13	MEM_CSb(NC)	MEM_DM0(NC)	W17
AB18	MEM_CKE(NC)	MEM_DM1/DVO_D8(NC)	AE19
V14	MEM_ODT(NC)		
		IOPLLVDD18(NC)	AE23 IOPLLVDD18
V15	MEM_CKP(NC)	IOPLLVDD(NC)	AE24 IOPLLVDD
W14	MEM_CKN(NC)		
		IOPLLVSS(NC)	AD23
AE12	MEM_COMPP(NC)		
AD12	MEM_COMPN(NC)	MEM_VREF(NC)	AE18 MEM_VREF

AMD (215NDA7BKA11FG)
FCBGA528_SMDR14_TEST
B01-RX78005-A08

Check the Orange in this page MS1332 whether DNI or Common

please make a provision for tying to their power rails

+1.8VRUN +1.1VRUN

X R362 0R R0402 IOPLLVDD18
X R351 0R R0402 IOPLLVDD

+1.8VRUN

X R367 0R R0402 MEN_VREF

RS780M

13 SUS_STAT#_R — X D11 BAS40WS DIODE_SOD323 A C — A_RST# 13,16,17,19,31,33,38,39

RS780M

13,40 NB_VSYNC# — X R407 3K R0402

13 NB_TV_C — X R158 1K R0402

PA_RX7X0A1

RX780

RS740/RX780/RS780: LOAD_EEPROM_STRAPS

```
Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use
default values if not connected
RX780: pin DFT_GPIO1
RS780: pin SUS_STAT#
```

STRAP_DEBUG_BUS_GPIO_ENABLEb

```
Enables the Test Debug Bus using GPIO.
1 : Enable (RX780, RS780)
0 : Disable (RX780, RS780)
PIN: RX780-->NB_TV_C (pin DFT_GPIO5) ; RS780--> VSYNC# (pin VSYNC)
```

RX740: DFT_GPIO[4:2]: STRAP_PCIE_GPP_CFG[2:0]

```
These pin straps are used to configure PCI-E GPP mode.
000 : 00001
001 : 00010
010 : 01011
011 : 00100
100 : 01010
101 : 01100
111 : 01011
```

RX780: STRAP_PCIE_GPP_CFG[2:0] (Pins:RX780_DFT_GPIO[4:2])

```
111: 1-1-1-1-1-1 Mode L default
110: 1-1-1-1-1-1 Mode L
101: 2-0-2-0-2-0 Mode C2
100: 2-0-2-0-1-1 Mode K
011: 2-0-1-1-1-1 Mode E
010: 1-1-1-1-1-1 Mode L
001: 4-0-0-0-1-1 Mode C
000: 4-0-0-0-2-0 Mode B
```

RS780: STRAP_PCIE_GPP_CFG[2:0] (configurable thru register settings only)

```
1-1-1-1-1-1 Mode L default
1-1-1-1-1-1 Mode L
2-0-2-0-2-0 Mode C2
2-0-2-0-1-1 Mode K
2-0-1-1-1-1 Mode E
1-1-1-1-1-1 Mode L
4-0-0-0-1-1 Mode C
4-0-0-0-2-0 Mode B
```

Adobe Acrobat Professional - [PA_RS780A3.pdf]

RS740/RX780/RS780 Straps:

STRAP Name	RS740	RX780	RS780	Comments
Load EPROM Straps	DFT_GPIO1	DFT_GPIO1	SUS_STAT#	Load Straps from EPROM connected through Strap and I2C_Clk pins
Strap_Debug_Bus_EN#	DFT_GPIO5	DFT_GPIO5	VSYNC	Enables debug bus over Memory I/O pins or/and GPIOs
GPPSB_LINK_Config	DFT_GPIO[4:2]	DFT_GPIO[4:2]	Register settings only	Configures A-Link and GPP
Srap_Debug_Bus_PCIE_EN#	Not applicable	DFT_GPIO0	Register settings only	Enable Debug bus over x16 PCIE interface
SidePort_EN#	DFT_GPIO0	Not applicable	HSYNC	Enables side port

Adobe Acrobat Professional - [42221_rs780m_ds_nda_0.02.pdf]

Pin Name	Type	Power Domain	Ground Domain	Functional Description
SUS_STAT#	I	VDD33	VSS	Suspend Status. SUS_STAT# from the south bridge is connected to the pin to gate the sideport memory I/Os while power is ramping up and the POWERGOOD signal to the RS780M is still low.

RS740/RX780/RS780: STRAP_SIDE-PORT MEMORY ENABLE

```
Enables Side port memory
1 : Disable (RS740/RS780)
0 : Enable (RS740/RS780)
RS780: pin HSYNC
RX780: Not Applicable
```

RS780M

13,40 NB_HSYNC# — X R406 3KR0402 +3VRUN — X R405 3KR0402

Adobe Acrobat Professional - [42221_rs780m_ds_nda_0.02.pdf]

Pin Name	Type	Power Domain	Ground Domain	Integrated Termination	Functional Description
DAC_HSYNC	A-O	VDD33	VSS	50kΩ programmable: PU/PD/none	Display Horizontal Sync
DAC_VSYNC	A-O	VDD33	VSS	50kΩ programmable: PU/PD/none	Display Vertical Sync

DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLEb

```
Enables Test debug bus over PCIE bus
(Applicable to RX780 & RS780 Only)
1. Disable (can be enabled thru nbcfg register)
0 : Enable
RX780: pin DFT_GPIO0
RS780: configurable thru register setting only
```

DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLEb

```
RX780: Enables the Test Debug Bus using PCIE bus
1 : Disable ( Can still be enabled using nbcfg register access )
0 : Enable

RS740/RS780: Enables Side port memory ( RS780 use HSYNC#)
1.  Disable (RS740)  Enable (RS780)
0 : Enable (RS740)   Disable(RS780)
```

Adobe Acrobat Professional - [42223_rx780_ds_nda_0.02.pdf]

Pin Name	Type	Power Domain	Ground Domain	Integrated Termination	Functional Description
DFT_GPIO[5:0]	I/O	VDD18	VSS	Pull Up	Outputs for DFT TESTMODE. The pins cannot be used for general GPIO functions.

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Title: RX/RS780-DVO

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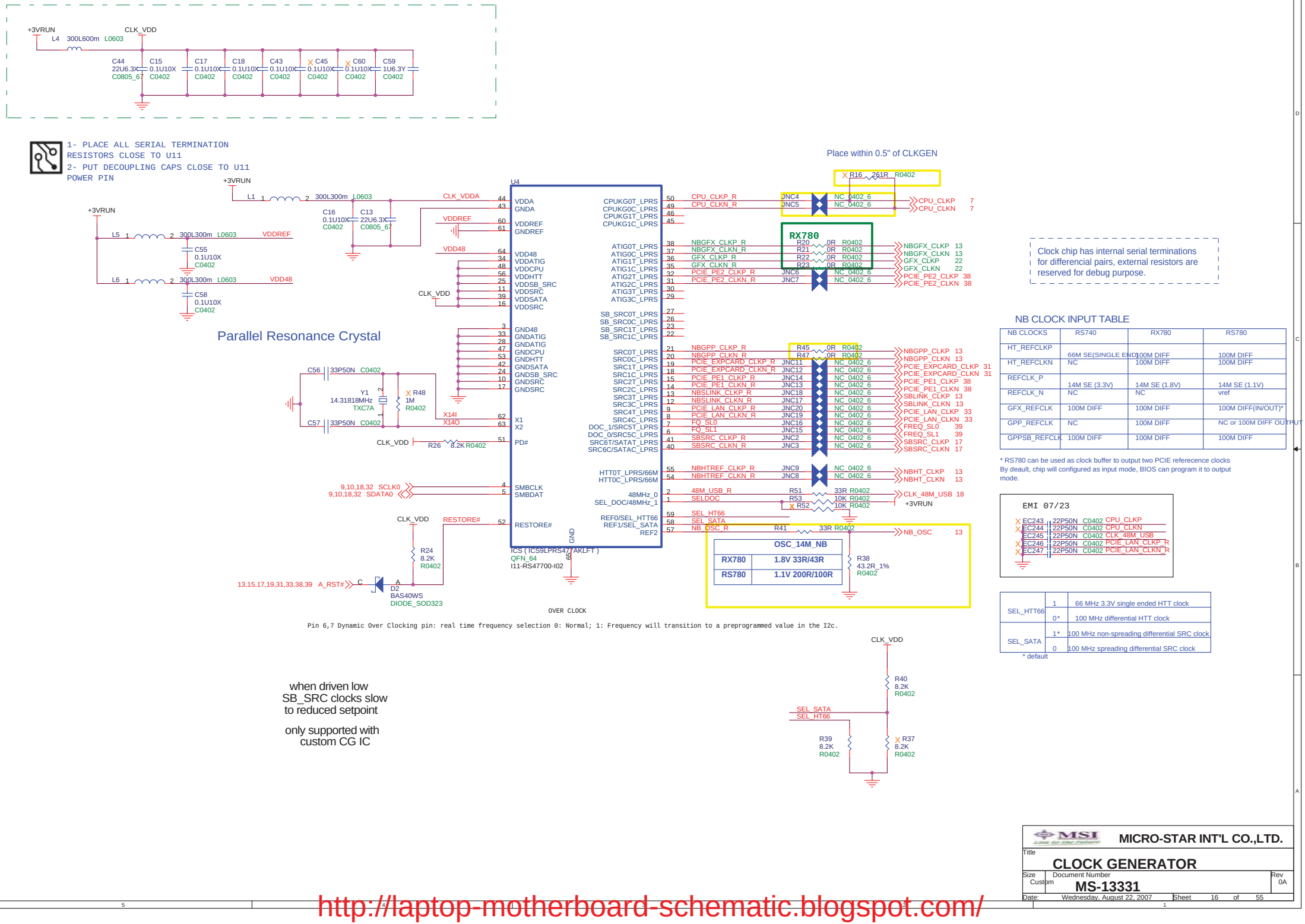

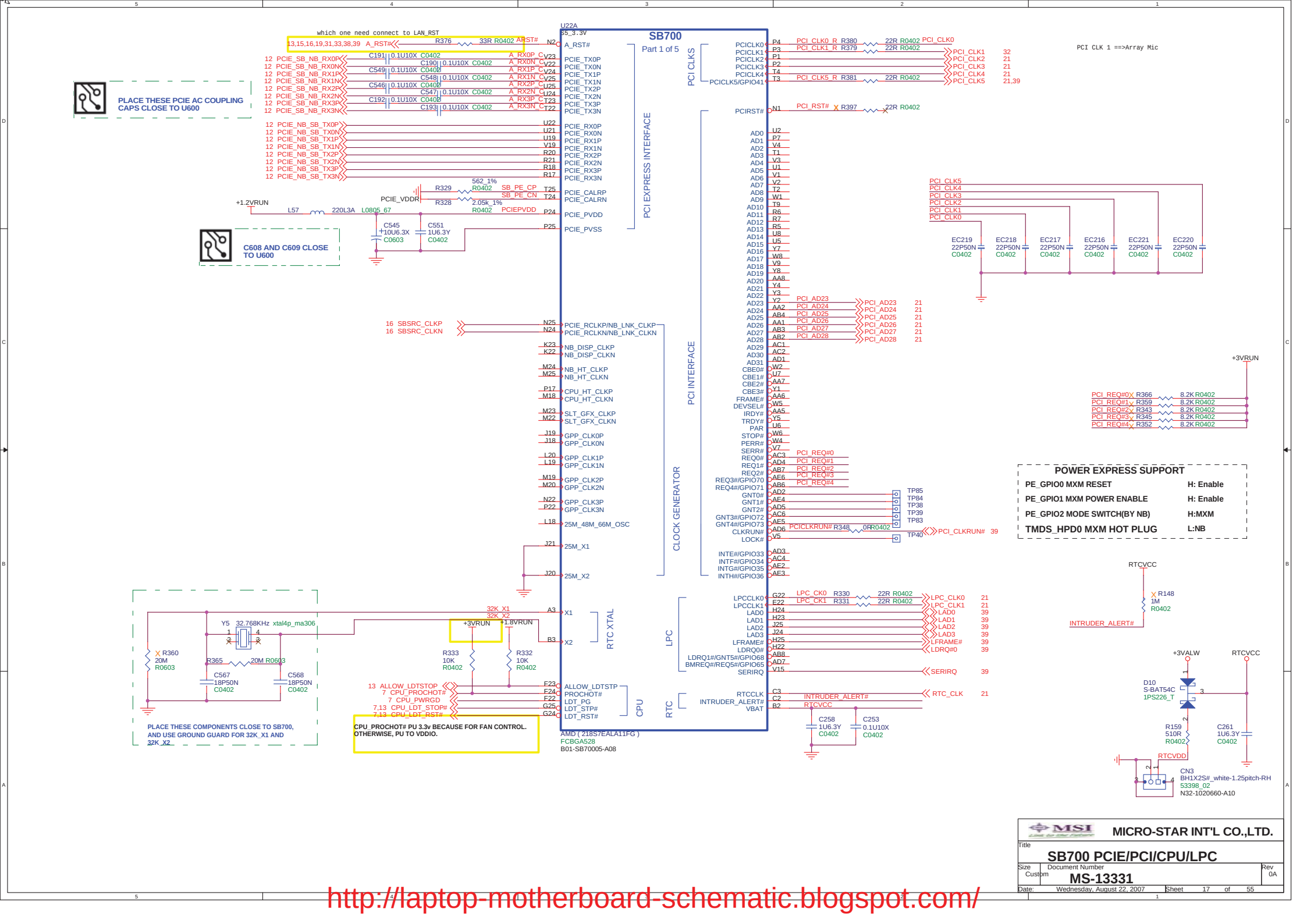
SB700
Part 1 of 5
U22A
PCI CLKS
PCI EXPRESS INTERFACE
PCI INTERFACE
CLOCK GENERATOR
LPC
RTC XTAL
CPU
RTC
PLACE THESE PCIE AC COUPLING CAPS CLOSE TO U600
C608 AND C609 CLOSE TO U600
PLACE THESE COMPONENTS CLOSE TO SB700, AND USE GROUND GUARD FOR 32K_X1 AND 32K_X2
CPU_PROCHOT# PU 3.3v BECAUSE FOR FAN CONTROL. OTHERWISE, PU TO VDDIO.
PCI CLK 1 ==>Array Mic
POWER EXPRESS SUPPORT
PE_GPIO0 MXM RESET H: Enable
PE_GPIO1 MXM POWER ENABLE H: Enable
PE_GPIO2 MODE SWITCH(BY NB) H:MXM
TMDS_HPD0 MXM HOT PLUG L:NB
AMD (218S7EALA11FG)
FCBGA528
B01-SB70005-A08
MICRO-STAR INT'L CO.,LTD.
SB700 PCIE/PCI/CPU/LPC
MS-13331
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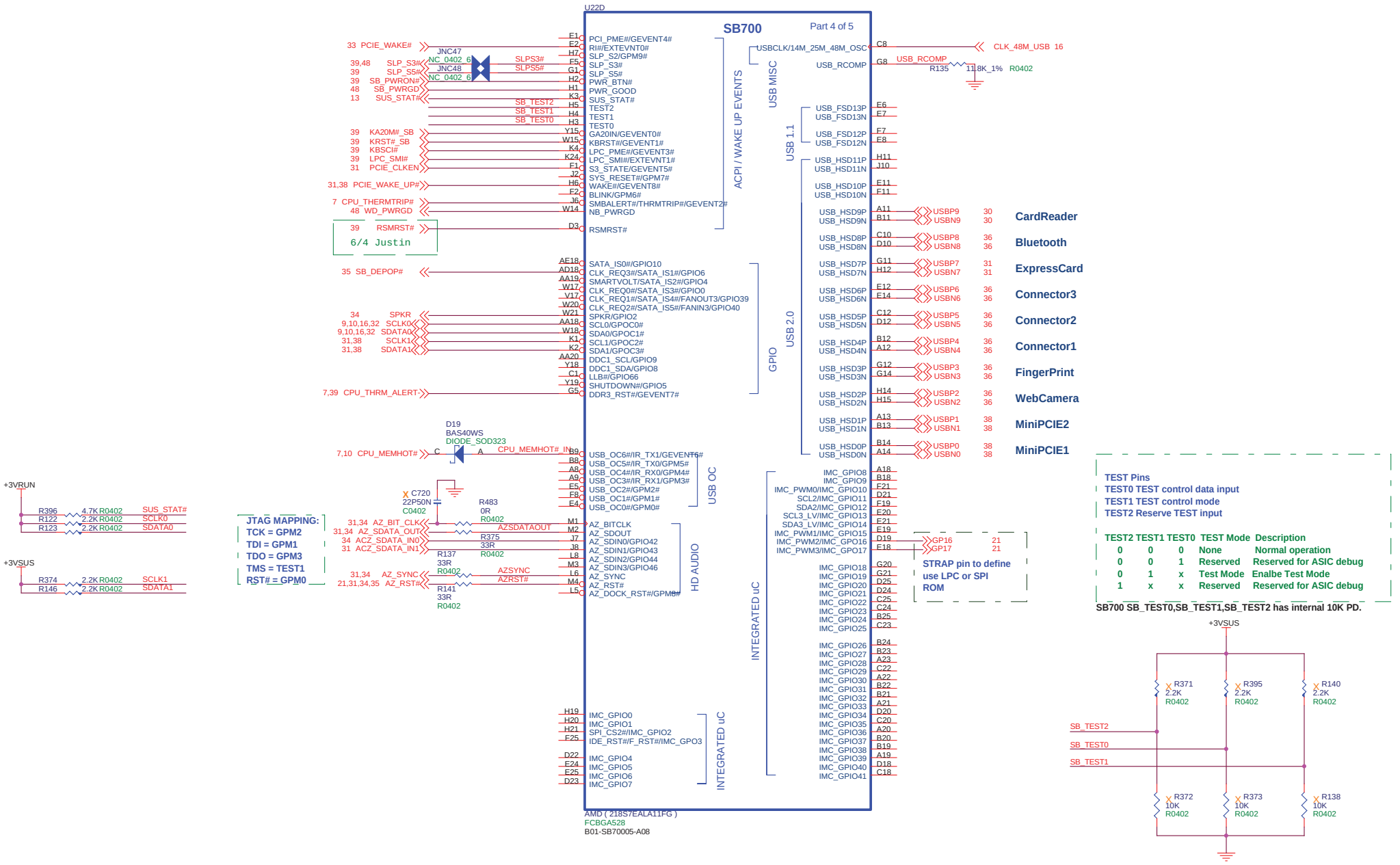
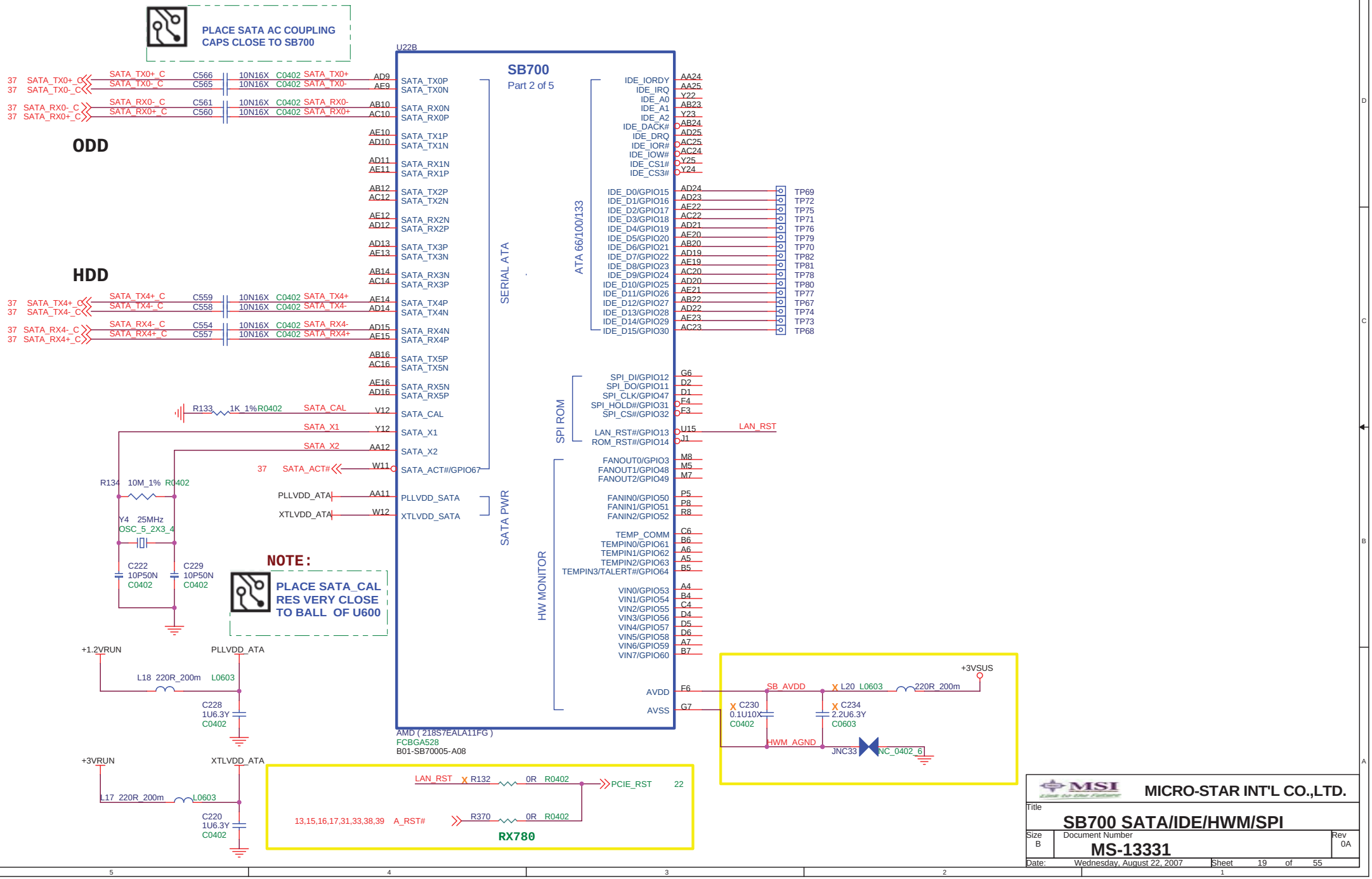
http://laptop-motherboard-schematic.blogspot.com/





PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

ERRATA PA_SB700AA1

VDD33_18
+1.8V : FLASH MEMORY MODE(DEFAULT)
+3.3V : IDE MODE

Please make a provision for tying to +3.3V_S0

SB700 Part 3 of 5

POWER

SB700 Part 5 of 5

GROUND

AMD (218S7EALA11FG)
FCBGA528
B01-SB70005-A08

Title	SB700 POWER & GND
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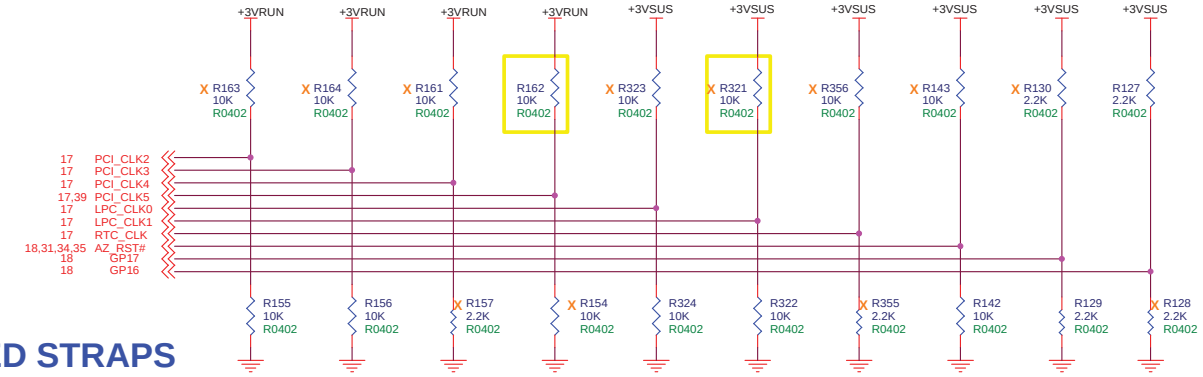
MICRO-STAR INT'L CO.,LTD.

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

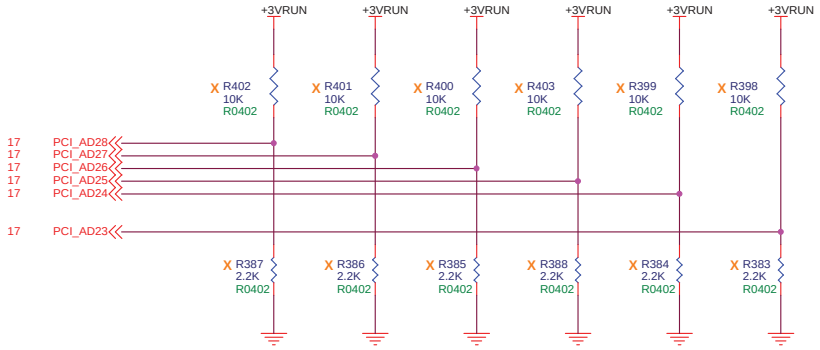


REQUIRED STRAPS

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST	GP17 GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	H,H = Reserved L,H = LPC ROM (DEFAULT) H,L = SPI ROM L,L = FWH ROM
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT	

DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



Use 2.2K PD.

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

MICRO-STAR INT'L CO.,LTD.

Title: SB700 STRAPS

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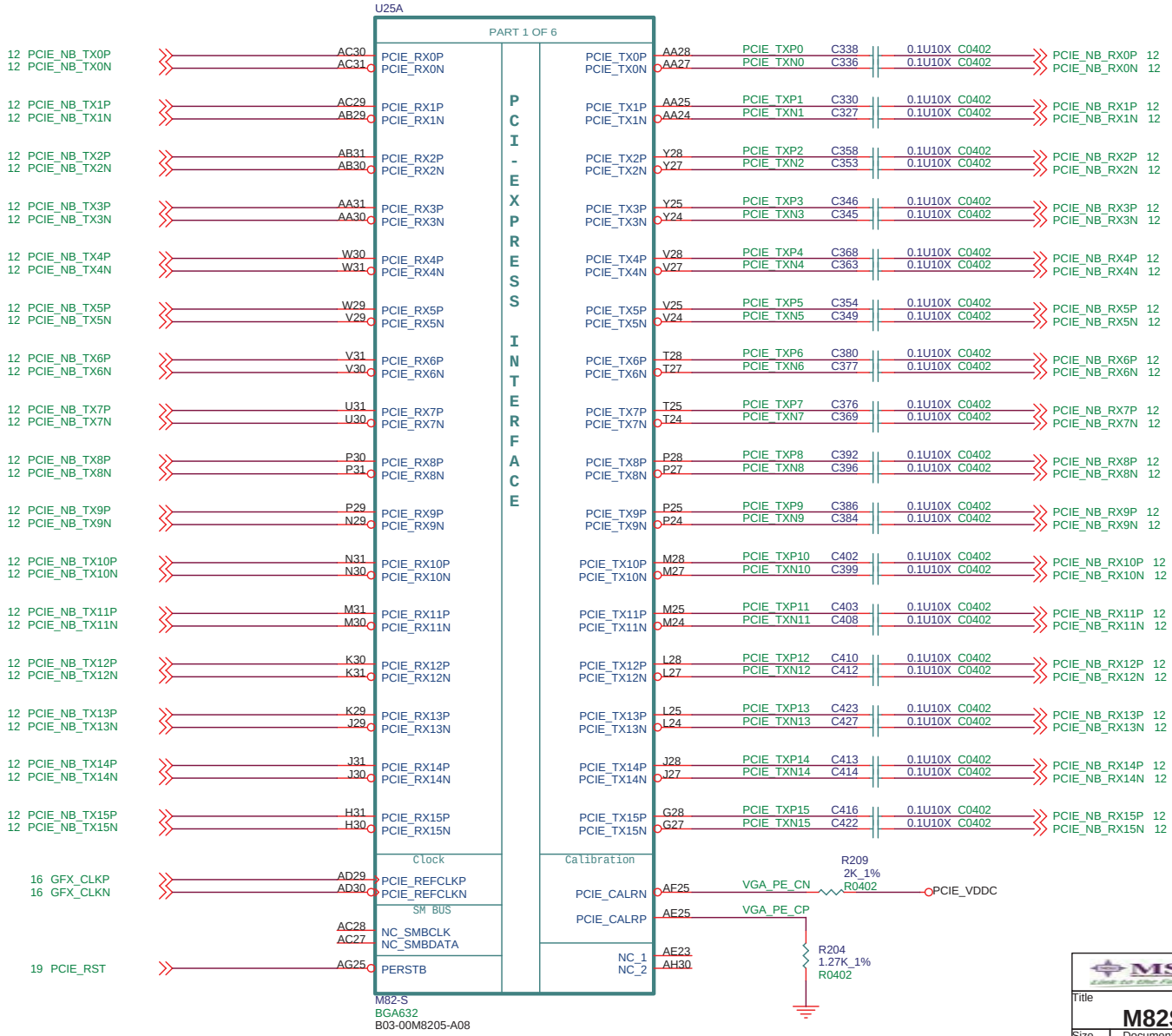

MICRO-STAR INT'L CO.,LTD.

Title: M82S PCI-E LINK

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RX780

DVALID
1.)Transport stream data valid input or general purpose I/O
Note: Can be left unconnected if not used.
2.)This signals is also used for video capture and as an initialization pin strap.
3.)Internal use only. Other logic must not affect this signal during RESET.

PSYNC VGA_DIS(Internal pulldown)
VGA Disable determines whether or not the card will be recognized as the system's VGA controller (via the SUBCLASS field in the PCI configuration space).
0 – VGA Controller capacity enabled
1 – The device will not be recognized as the system's VGA controller

U25B
PART 2 OF 6
INTEGRATED TMDS/DP PORT
EXT TMDS DVO
GENERAL PURPOSE I/O
DAC1 / CRT
DAC2 (TV/CRT2)
SERIAL BUSES
PLL & XTAL
TEST
THERMAL
M82-S
BGA632
B03-00M8205-A08

HDMI

CRT

THE PINS WITH TEST POINTS ARE REQUIRED TO BE ACCESSIBLE FOR DEBUG AND BOUNDRY SCAN PURPOSES USING TEST POINT VIAS IF UNUSED OR COMPONENT PADS

ENSURE DEBUG_ACCESS STRAP IS ALSO ACCESSIBLE SEE CONFIG STRAPPING PAGE

ACCESS TO ATI DEBUG PORT IS MANDATORY ON INITIAL PROTOTYPE DESIGNS

WITH M8x ASIC INSTALL M8x STRAP RESISTORS AND DO NOT INSTALL M7x STRAP RESISTORS

IF HOT PLUG DETECT IS NOT REQUIRED REMOVE ALL THIS LOGIC EXCEPT FOR 100K PULL DOWN

OPTIONAL 0 OHM STRAPS TO GROUND FOR RB,GB,BB AND R2B,G2B,B2B SEE DAC1_RGB AND DAC2_RGB SHEETS

PLACE OR RESISTORS CLOSE TO ASIC

GPIO_17_THERMAL_INT
Thermal monitor interrupt.
GPIO_17_THERMAL_INT is used for ASIC temperature control. It is connected to the ALERTb signal of the thermal monitor which measures the temperature of the ASIC. If the ASIC temperature falls outside a defined range, the ALERTb signal is asserted. Low level on GPIO_17_THERMAL_INT causes M74/M72 to generate an interrupt (the polarity of this interrupt is programmable – the default is active low). Software can then activate the implemented temperature control scheme.

Power Control signals control the core voltage regulator.
At Reset, these signals will be inputs with weak internal pull-down resistors.
VBIOS can define these signals to be either 3.3V outputs or open drain outputs.
The output state (high/low) of these signals is programmable for each PowerPlay state.

Back Bias (BB) control:
When GPIO_21_BB_EN = 0V then back bias is disabled on the PCB (ie BPP=VDDC and BBN=VSS).
When GIO_21_BB_EN = 3.3V then back bias is enabled on the PCB.
Can function as a GPIO if not required for BB control.

GPIO_22_ROMCSB
BIOS_ROM_EN
Enable external BIOS ROM device
0 - Disable external BIOS ROM device
1 - Enable external BIOS ROM device

GPIO_23_CLKREQB DRIVES LOW DURING RESET

VREFG VOLTAGE DIVIDER IS (VREFG = VDDR4,5(1.8V) / 3 = .6V)

PLACE VREF DIVIDER AND CAP CLOSE TO ASIC

Close to M82S
Cap close to thermal sensor
LM86CIMMXNOPB_MSOP8-RH
MSOP8_T

3.3V TO 5V LEVEL SHIFT LOGIC REQUIRED
IF DDC1,DDC2 USED ON M8x OR DDC1,DDC2,DDC3 USED ON M7x
DDC3,DDC4 ARE 5V TOLERANT ON M8x

CRT	3.3V	
LVDS	3.3V	
HDMI	5V	

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Title: M82S I/O
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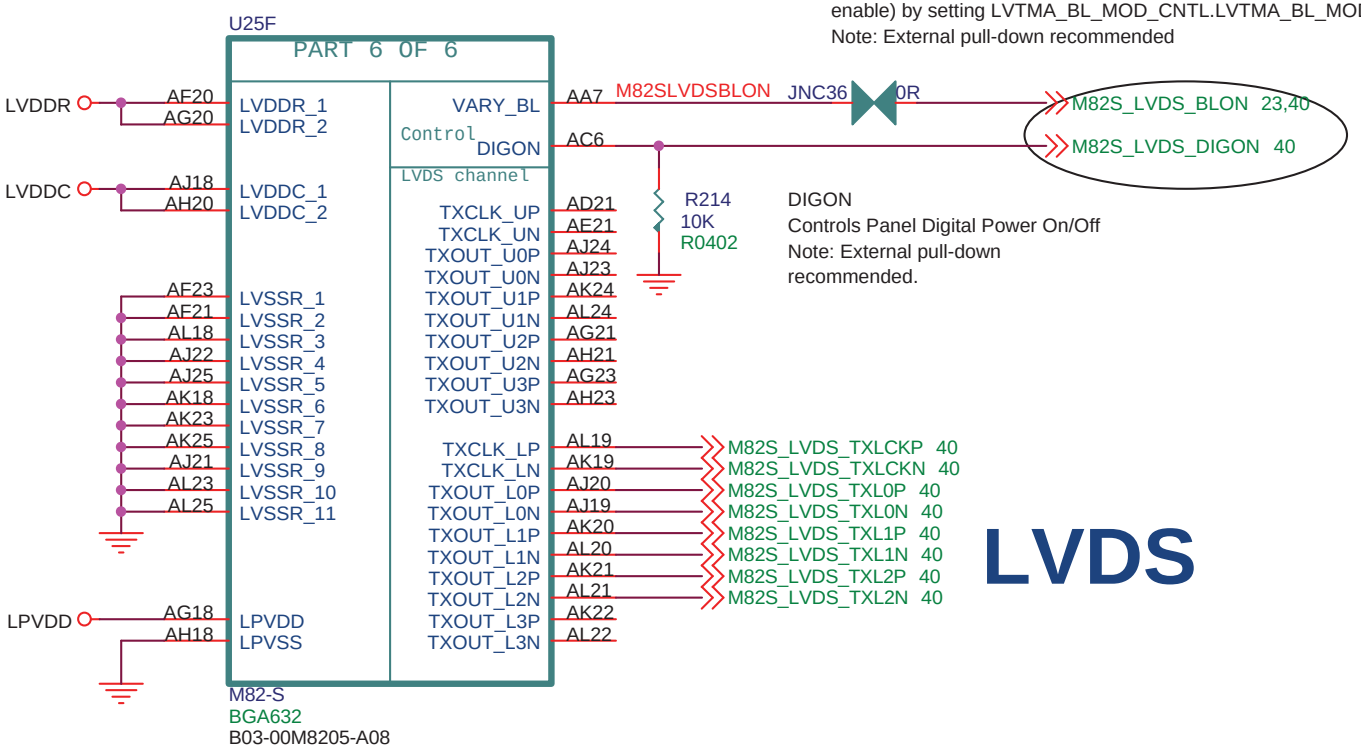
VARY_BL
LCD PWM (Pulse Width Modulated) output to adjust LCD brightness. Active high.
LVTMA_BL_MOD_CNTL.LVTMA_BL_MOD_LEVEL can be used to control the backlight level by means of pulse width modulation.
Alternatively, VARY_BL can be used to control backlight on/off (backlight enable) by setting LVTMA_BL_MOD_CNTL.LVTMA_BL_MOD_EN = 0.
Note: External pull-down recommended



DIGON
Controls Panel Digital Power On/Off
Note: External pull-down recommended.

LVDS

MICRO-STAR INT'L CO.,LTD.

Title: M82S LVDS

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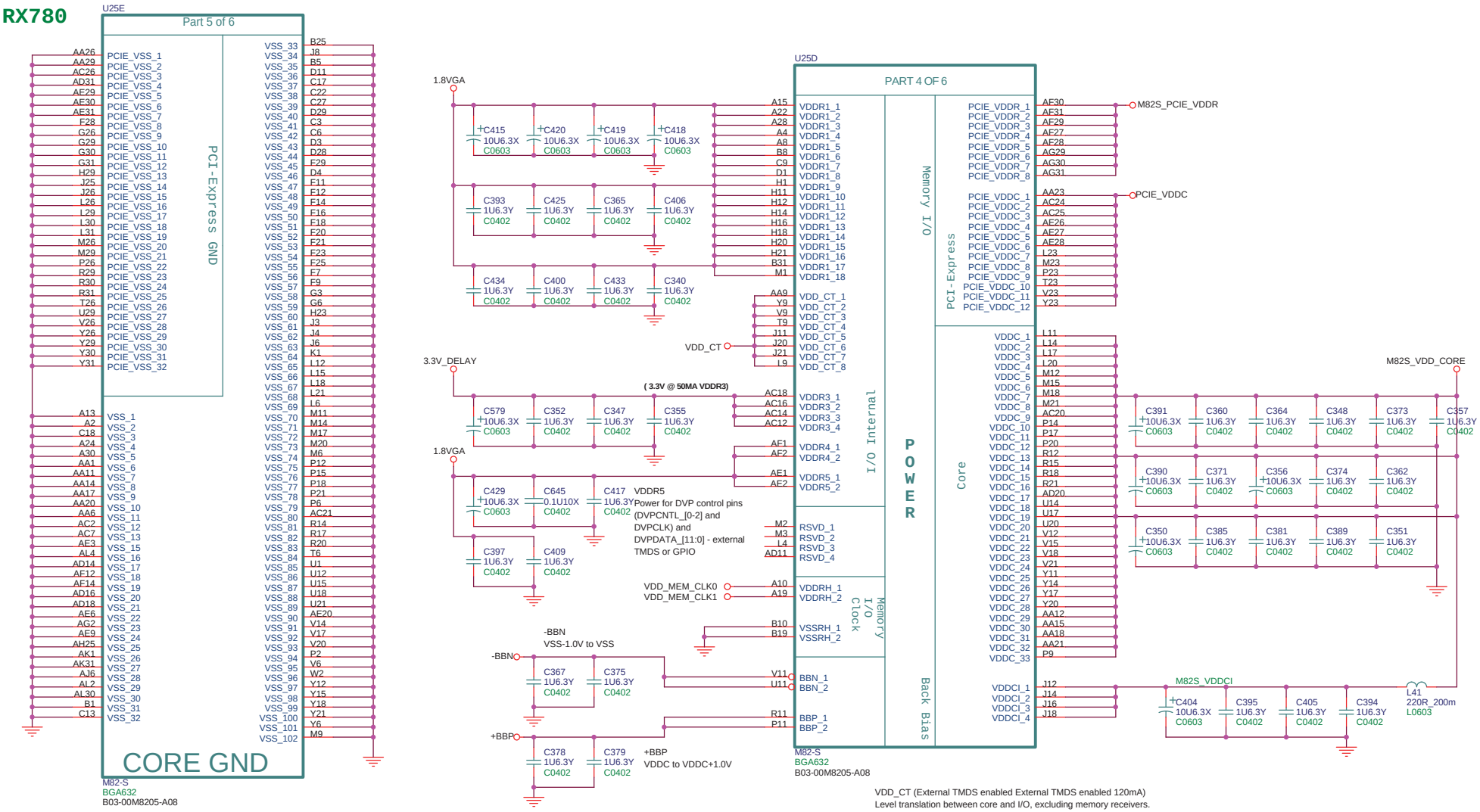
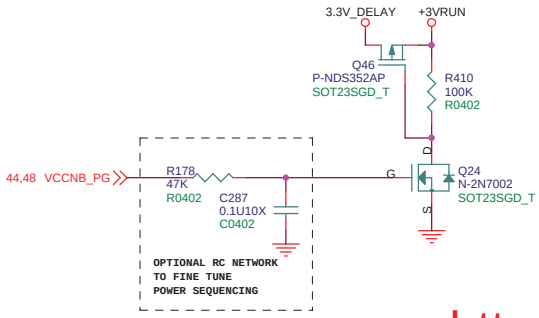


VDDC>VDDR1>PCIE_VDDC>VDDR3



Back Bias Pins
Back bias is a new feature which will require additional engineering verification and characterization. Prototype designs need to provide the option
to disable/by-pass this feature.

+BBP
Back Bias Enabled: (GPIO_21_BB_EN = 3.3V): 1.5V or 1.8V
Back Bias Disabled: (GPIO_21_BB_EN = 0V): VDDC
Connect to VBBP back bias regulator / generator.
If back bias is not used, connect directly to VDDC.

-BBN
Back Bias Enabled: (GPIO_21_BB_EN = 3.3V): -0.55V or -0.85V
Back Bias Disabled: (GPIO_21_BB_EN = 0V): VSS
Connect to VBBN back bias regulator / generator.
If back bias is not used connect directly to VSS.

VDD_CT (External TMDS enabled External TMDS enabled 120mA)
Level translation between core and I/O, excluding memory receivers.
VDD_CT must remain powered whenever the ASIC is powered.

VDDR4
DVOA_MSB_VMODE register bit; '1' - 3.3V(default); '0' - 1.8V

VDDR5
DVOA_LSB_VMODE register bit; '1' -3.3V(default); '0' - 1.8V

VDDRH
Dedicated power pins for memory clock pads for each channel.
Should have the same voltage level as VDDR1.

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Title: M82S PWR&GND

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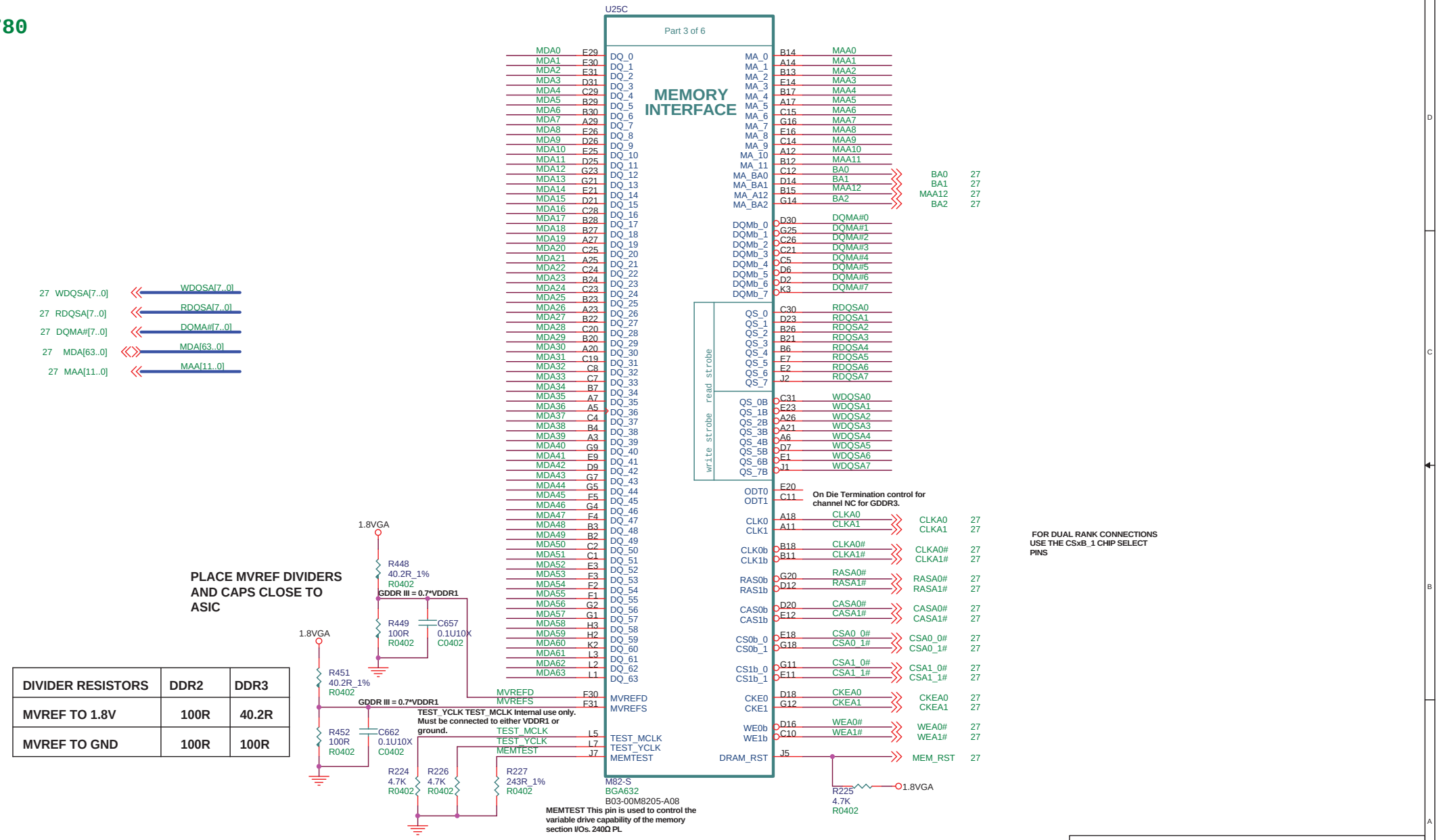

DIVIDER RESISTORS	DDR2	DDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R

MICRO-STAR INT'L CO.,LTD.

Title: M82S MEMORY

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Group2 Group3 Group1 Group0 Group7 Group5 Group4 Group6

U31 HY5RS123235BFP-14 FBGA136 M12-5RS1225-H23

U32 HY5RS123235BFP-14 FBGA136 M12-5RS1225-H23

J3 RFU NC the pin, in the scan order, will read as a logic"0"

V4 Scan Enable. Logic HIGH would enable the device into scan mode and will be disabled at logic LOW. Must be tied to GND when not in use.

PLACE VREF DIVIDER COMPONENTS AS CLOSE TO MEMORY AS POSSIBLE

DDR3 MEMORY CONTROL SIGNAL PULLUP RESISTOR VALUES MAY CHANGE BETWEEN M62S,M64S,M71S AND M72S. SEE DATA BOOK FOR LATESTINFORMATION

CHECK M82S Spec.

GDDR3 32MX32 MEMORY

HY5RS123235BFP-14
VDD/VDDQ=1.8V 700MHz
1400Mbps/pin(Max Data Rate)
POD_18(Interface)

	32M x 32
Configuration	4M x 32 x 8 banks
Refresh Count	8 k
Bank Address	BA0 - BA2
Row Address	A0~A12
Column Address	A0~A7, A9
AP Flag	A8

MICRO-STAR INT'L CO.,LTD.

Title: GDDR3 32X32M

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L33 300L300m 1 2 L0603 — 1.8VGA → LVDDR (3.3V @ 250MA LVDDR)
C306 10U6.3X C0603; C313 1U6.3Y C0402; C321 0.1U10X C0402

X R192 0R R0603

L35 60L1_1000m L1206_113 — 1.8VGA → LVDDC (1.8V @ 100MA LVDDC) (1.8V @ 400MA LVDDC,LVDDR)
C320 10U6.3X C0603; C334 0.1U10X C0402; C337 0.1U10X C0402

L32 220R_200m L0603 — 1.8VGA → LPVDD (1.8V @ 20MA LPVDD)
C302 10U6.3X C0603; C319 1U6.3Y C0402; C329 0.1U10X C0402 *

L37 220R_200m L0603 — 1.8VGA → DPLL_PVDD (1.8V @ 40MA DPLL_PVDD)
C309 10U6.3X C0603; C315 1U6.3Y C0402; C332 0.1U10X C0402 *

L39 220R_200m L0603 — 1.8VGA → PCIE_PVDD (1.8V @ 40MA PCIE_PVDD)
C324 10U6.3X C0603; C331 1U6.3Y C0402; C335 0.1U10X C0402 *

3.3V_DELAY

L38 220R_200m L0603 — → A2VDD (3.3V @ 135MA A2VDD)
C304 10U6.3X C0603; C318 0.1U10X C0402; C339 1000P50X C0402

L67 220R_200m L0603 — 1.8VGA → A2VDDQ (1.8V @ 2MA A2VDDQ)
C590 10U6.3X C0603; C597 1U6.3Y C0402; C602 0.1U10X C0402 *

L68 220R_200m L0603 — 1.8VGA → VDDDI (1.8V @ 100MA VDD1DI,VDD2DI)
C592 10U6.3X C0603; C599 0.1U10X C0402; C608 1000P50X C0402 *

L69 220R_200m L0603 — 1.8VGA → M82S_AVDD (1.8V @ 65MA AVDD)
C593 10U6.3X C0603; C598 0.1U10X C0402; C606 1000P50X C0402

L70 220R_200m L0603 — +1.1VRUN → DPA_VDDR (1.8V @ 100MA EACH SINGLE LINK) (1.1V @ 200MA EACH SINGLE LINK)
C594 10U6.3X C0603; C600 1U6.3Y C0402; C609 0.1U10X C0402

L66 220R_200m L0603 — +1.1VRUN → DPB_VDDR
C591 10U6.3X C0603; C596 1U6.3Y C0402; C603 0.1U10X C0402

L71 220R_200m L0603 — 1.8VGA → TPVDD (1.8V @ 20MA TPVDD EACH SINGLE LINK)
C595 10U6.3X C0603; C601 0.1U10X C0402; C610 1000P50X C0402 *

L42 220R_200m L0603 — 1.8VGA → VDD_CT (VDD_CT 1.8V @ 110MA (VDD_CT)
C411 10U6.3X C0603; C407 0.1U10X C0402; C401 1000P50X C0402

L30 60L1_1000m L1206_113 — 1.8VGA → M82S_PCIE_VDDR (1.8V @ 400MA PCIE_VDDR)
C307 10U6.3X C0603; C314 1U6.3Y C0402; C322 0.1U10X C0402

PLACE ALL DECOUPLING AS CLOSE TO ASIC AS POSSIBLE

L73 220R_200m L0603 — 1.8VGA → VDD_MEM_CLK0 (1.8V @ MA VDDRHA_1 INCLUDED IN VDDR1)
C682 10U6.3X C0603; C683 1U6.3Y C0402; C684 0.1U10X C0402

L44 220R_200m L0603 — 1.8VGA → VDD_MEM_CLK1 (1.8V @ MA VDDRHA_2 INCLUDED IN VDDR1)
C431 10U6.3X C0603; C437 1U6.3Y C0402; C436 0.1U10X C0402

FOR M7x
INSTALL LVDDR TO +3.3V AND LVDDC TO 1.8V
WITH SEPARATE FILTERS
DO NOT INSTALL STRAP RESISTOR
FOR M8x
INSTALL LVDDR AND LVDDC TO +1.8V
WITH THE ONE LVDDC FILTER
DO NOT INSTALL LVDDR FILTER
INSTALL STRAP RESISTOR

FOR M8x
INSTALL DPA_VDDR TO +1.1V AND DPB_VDDR TO +1.1V
WITH SEPARATE FILTERS
DO NOT INSTALL STRAP RESISTOR
FOR M7x
INSTALL DPA_VDDR AND DPB_VDDR TO +1.8V
WITH THE ONE DPA_VDDR FILTER
DO NOT INSTALL DPB_VDDR FILTER
INSTALL STRAP RESISTOR

PLACE ALL DECOUPLING CAPS CLOSE TO THE ASIC AND RUN DEDICATED TRACES FROM ASIC PINS TO JOIN THE GROUND PLANE WITH ONE VIA AT THE CAP *

+1.1VRUN L63 220L3A L0805_67 → PCIE_VDDC (PCIE_VDDC 1.1V @ 1A)
C575 10U6.3X C0603; C584 1U6.3Y C0402; C359 0.1U10X C0402
C398 1U6.3Y C0402; C370 1U6.3Y C0402; C387 1U6.3Y C0402

L36 220R_200m L0603 → DPLL_VDDC (DPLL_VDDC 1.1V @ 100 MA)
C310 10U6.3X C0603; C316 1U6.3Y C0402; C341 0.1U10X C0402 *

M82S_VDD_CORE L45 300L300m 1 2 L0603 → MPVDD (.95V-1.1V @ 230MA MPVDD)
C435 10U6.3X C0603; C438 1U6.3Y C0402; C439 0.1U10X C0402 *

THE OPTIMAL +BBP OFFSET VOLTAGE (POWERPLAY VDDC MINUS 1.5V OR 1.8V RAIL) IS YET TO BE DETERMINED

THE OPTIMAL -BBN OFFSET VOLTAGE (0V MINUS -.6V TO -.9V) IS YET TO BE DETERMINED BUT MAX1673 DIVIDER RESISTORS MUST BE ADJUSTED FOR THE SAME OFFSET AS +BBP

M82S_VDD_CORE — (+1.8V 0R +1.1V @ 1A MAX) — 1.8VGA
+5VRUN
R216 100K R0402
Q28 N-SI2304DS SOT23SGD_T (S, D, G, (+1.1V))
Q29 P-SI2301DS SOT23SGD_T
FET C 1.7A
FET B 1.8A
M82S_VDD_CORE
X R213 0R R0402
+BBP
C366 1U6.3Y C0402
23 BB_ENA
PQ28 N-2N7002 SOT23SGD_T (G, D, S)
R203 10K R0402

+3VRUN
U16 MAX1673ESA SOIC8 (LIN/SKIP#, CAP+, CAP-, SHDN#, IN, GND, FB, OUT)
C333 2.2U6.3Y C0603 BB_ENA
C325 10U6.3X C0603
R194 100K R0402
R200 17.4K_1% R0402
-BBN
C343 10U6.3X C0603; C342 10U6.3X C0603; X R206 0R R0402

-BB_VGA= -(+3VRUN) * R2138 / R2134

BB_ENA = 0V FOR BACK BIASING DISABLED
MAX1673 SHUTDOWN
-BBN = 0V VIA MAX1673 INTERNAL 1 OHM TO GROUND
N FET A = OFF, P FET B = OFF, N FET C = ON
+BBP = VDD_CORE

BB_ENA = +3.3V FOR BACK BIASING ENABLED
MAX1673 ENABLED
-BBN = -.85V
N FET A = ON, P FET B = ON, N FET C = OFF
+BBP = +1.8V

MSI MICRO-STAR INT'L CO.,LTD.

Title	M82S_PWR_& FILTER	
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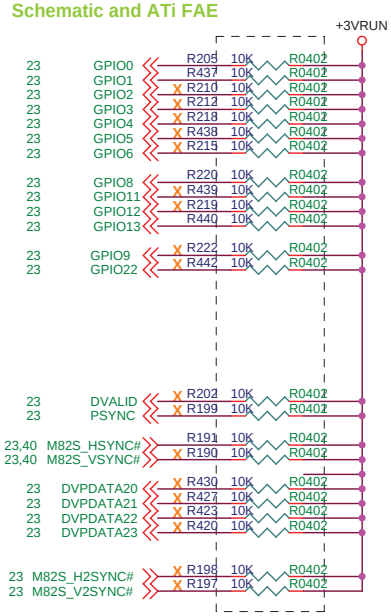
RX780

CHECK M82S Spec. and Reference Schematic and ATi FAE



Only populate the required straps, see table and databook

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE
RSVD = ATI RESERVED
(DO NOT INSTALL)

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	M8x	M7x
BIF_MSI_DIS	VIP1	MESSAGE SIGNAL INTERRUPT ENABLED	NA	0
BIF_AUDIO_EN	VIP3	ENABLE HD AUDIO (M7x) = HIGHT	NA	X
BIF_64BAR_EN_A	VIP5	64 BIT BARS DISABLED	NA	0
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING = HIGH	X	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED = HIGH	1	X
BIF_DEBUG_ACCESS	GPIO4	DEBUG SIGNALS MUXED OUT	0	0
BIF_AUDIO_EN	GPIO8	ENABLE HD AUDIO (M8x) = HIGH	X	RSVD
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device	0	0
BIOS_ROM_EN	GPIO_22_ROMCSB	DISABLE EXTERNAL BIOS ROM	NA	X
ROMIDCFG(3:0)	GPIO[13:11,9]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XX XX	X X X X
VIP_DEVICE_STRAP_ENA	M82S_VSYNC#	IGNORE VIP DEVICE STRAPS = LOW	0	0
BIF_VGA DIS	PSYNC	VGA ENABLED = LOW	0	0
BIF_HDMI_EN	M82S_HSYNC#	HDMI ENABLE = HIGHT (SEE NOTE 2)	X	X
MEM_TYPE	ANY UNUSED GPIO OR DVP THAT ARE NOT CONFIG STRAPS FOR EXAMPLE DVPDATA20:23 IN THIS DESIGN	MEMORY TYPE,MAKE AND SIZE INFO	X X X X	X X X X
BIF_GEN2_EN_A	GPIO5	Debug use only (disables PCI-E 5.0 GT/s negotiation) = LOW	0	

NOTE 1: HD AUDIO MUST ONLY BE ENABLED ON SYSTEMS THAT ARE LEGALLY ENTITLED. IT IS THE RESPONSIBILITY OF THE SYSTEM DESIGNER TO ENSURE ENTITLEMENT

NOTE 2: HDMI MUST ONLY BE ENABLED ON SYSTEMS THAT ARE LEGALLY ENTITLED. IT IS THE RESPONSIBILITY OF THE SYSTEM DESIGNER TO ENSURE ENTITLEMENT

GPIO22=0 GPIO_9 GPIO_[13:11]= CONFIG[3:0]
a) If BIOS_ROM_EN = 1, then Config[3:0] defines the ROM type. See "ROM Configurations"
b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. (Config 3 = don't care).

Size of the primary memory apertures	CONFIG[3:0]
128MB	x000
256MB	x001
64MB	x010
32MB	x011
512MB	x100
1GB	x101
2GB	x110
4GB	x111

ATI RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESE

GPIO2 GPIO3 GPIO5 GPIO6 DVALID H2SYNC V2SYNC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GENERICC GPIO21_BB_EN GPIO_28_TDO

COMPONENTS SHOWN ARE EXAMPLES ONLY AND NOT NECESSARILY QUALIFIED

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Title: M82S CONGIF STARP

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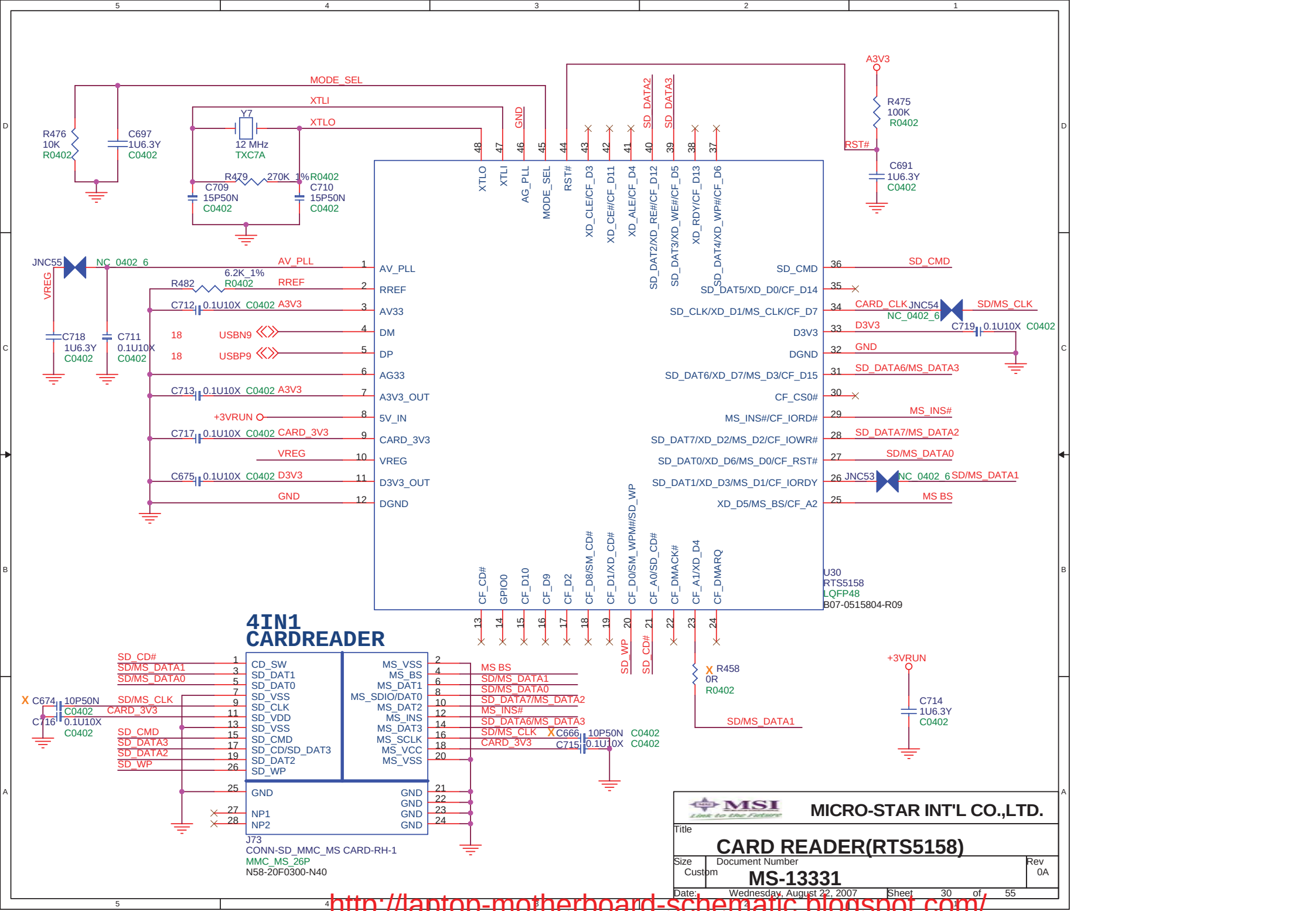

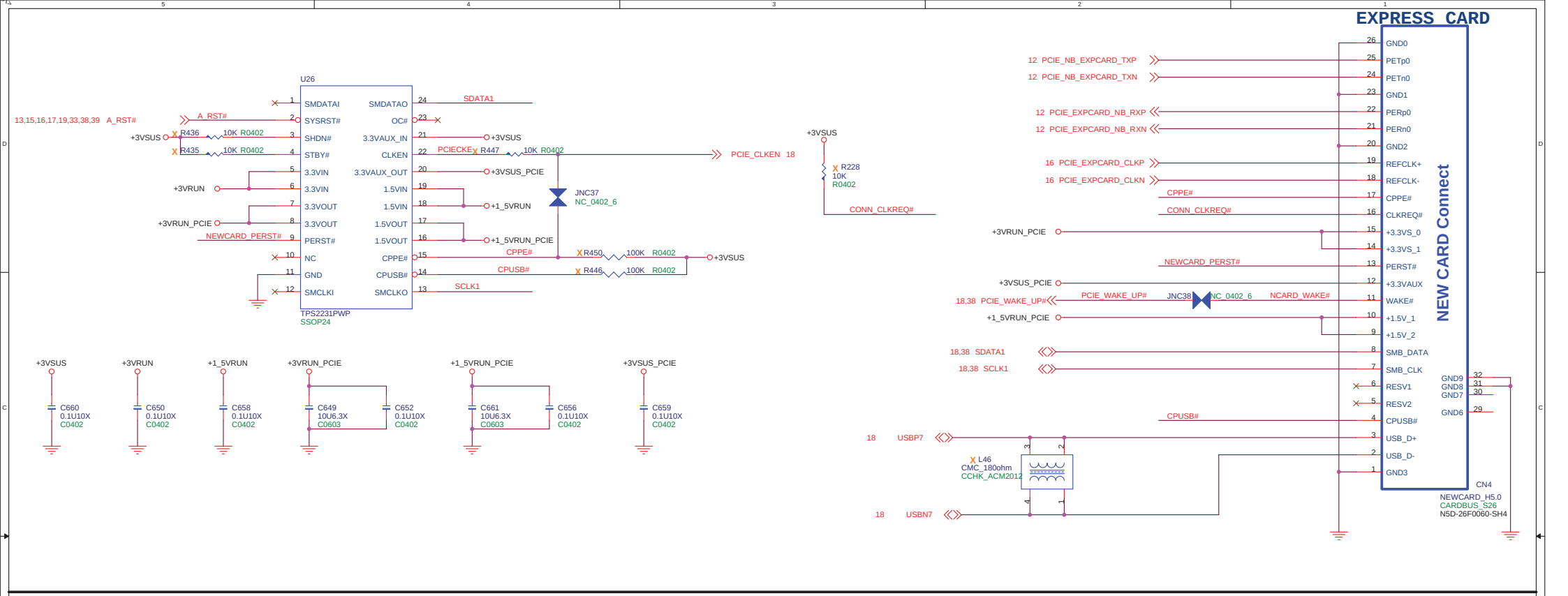

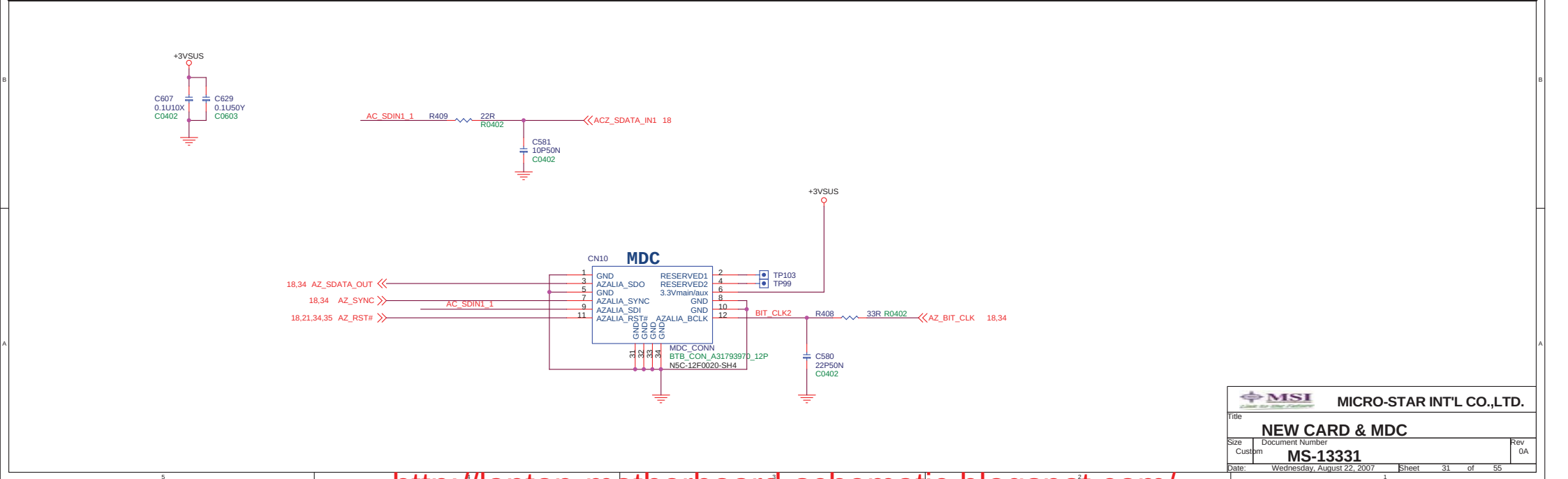

MICRO-STAR INT'L CO.,LTD.

Title: NEW CARD & MDC

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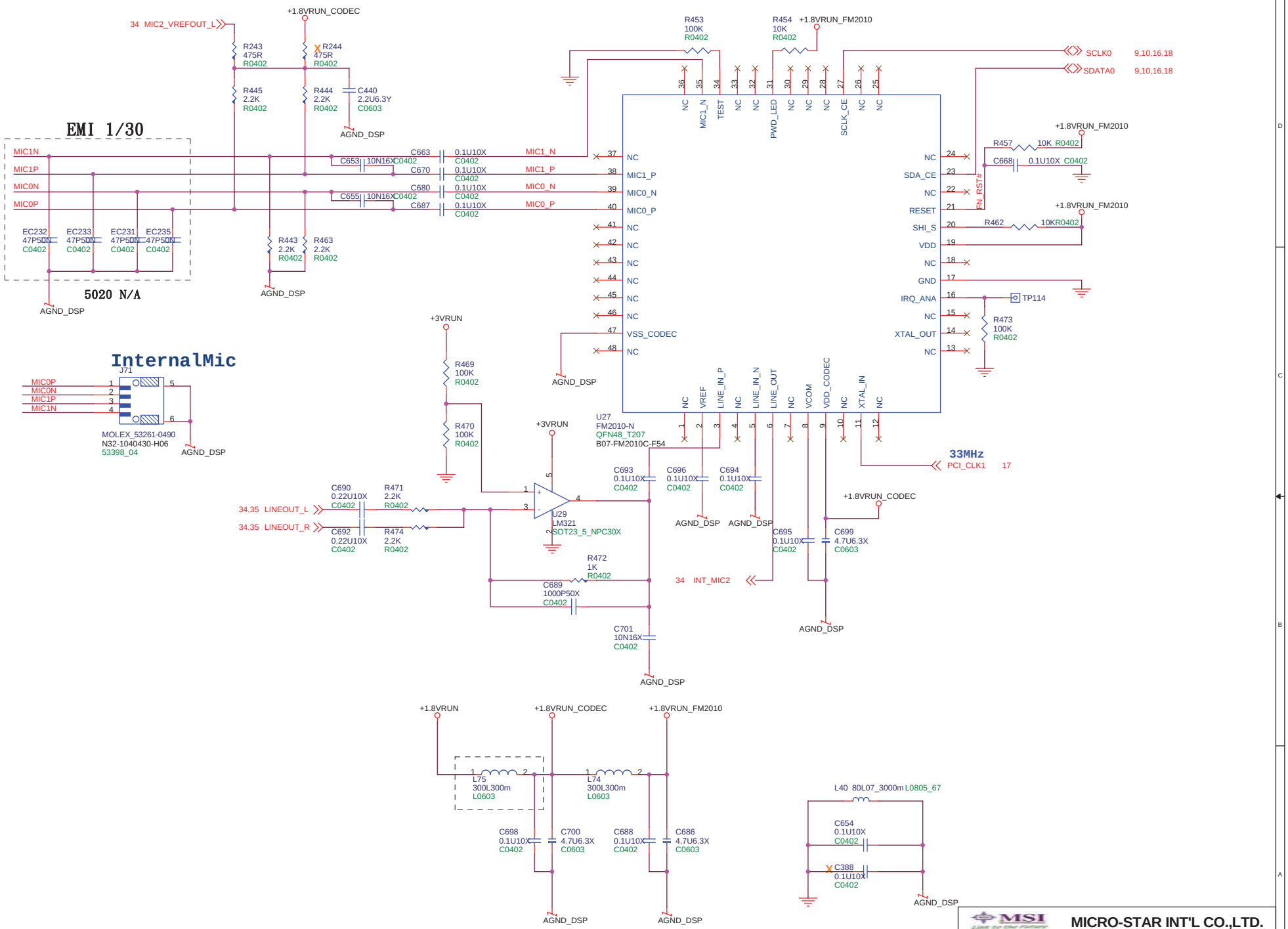

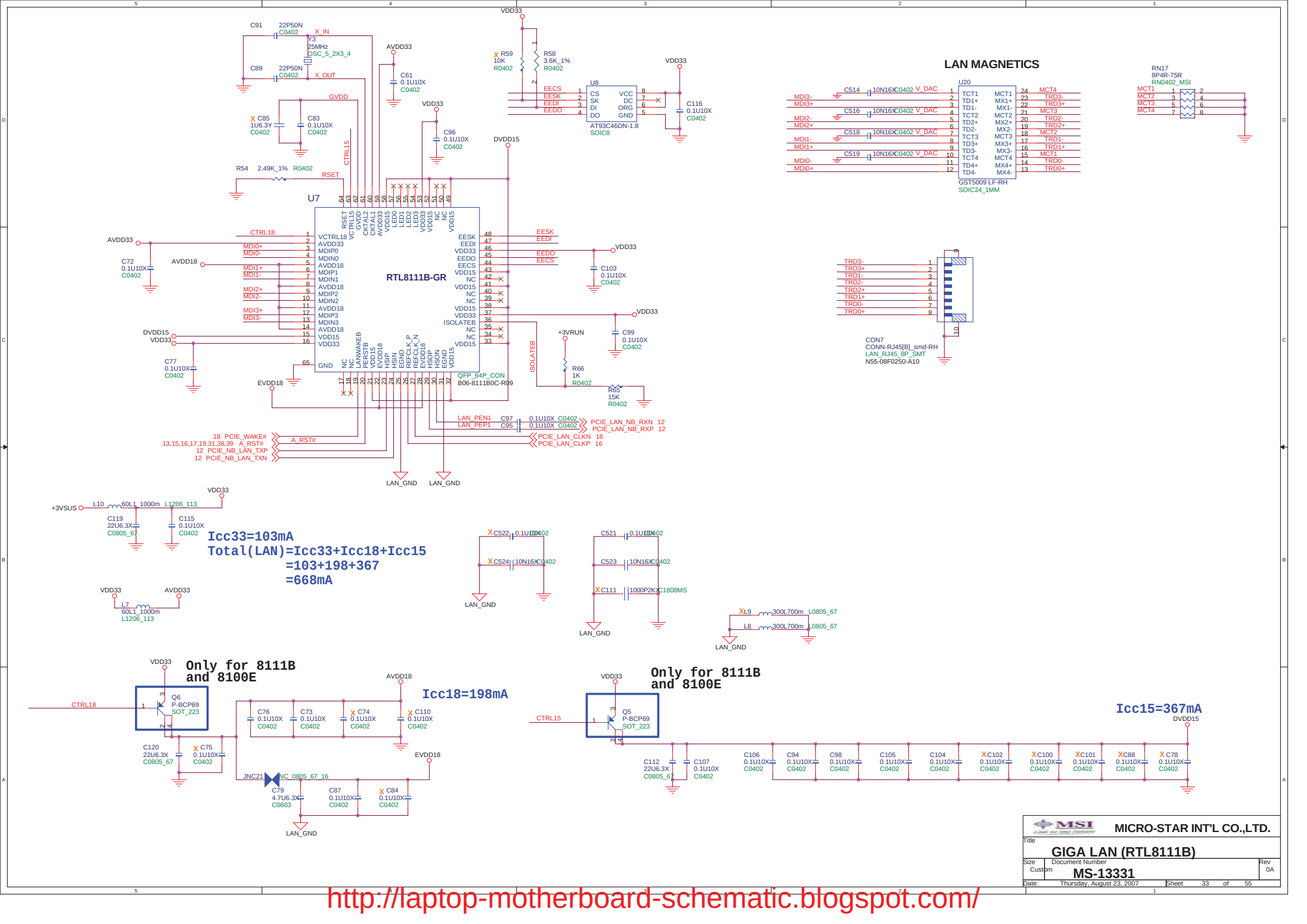
LAN MAGNETICS
U7
RTL8111B-GR
QFP_64P_CON
B06-8111B0C-R09
U8
AT93C46DN-1.8
SOIC8
U20
GST5009 LF-RH
SOIC24_1MM
CON7
CONN-RJ45[B]_smd-RH
LAN_RJ45_8P_SMT
N55-08F0250-A10
Icc33=103mA
Total(LAN)=Icc33+Icc18+Icc15
=103+198+367
=668mA
Only for 8111B
and 8100E
Icc18=198mA
Only for 8111B
and 8100E
Icc15=367mA
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GIGA LAN (RTL8111B)
MS-13331
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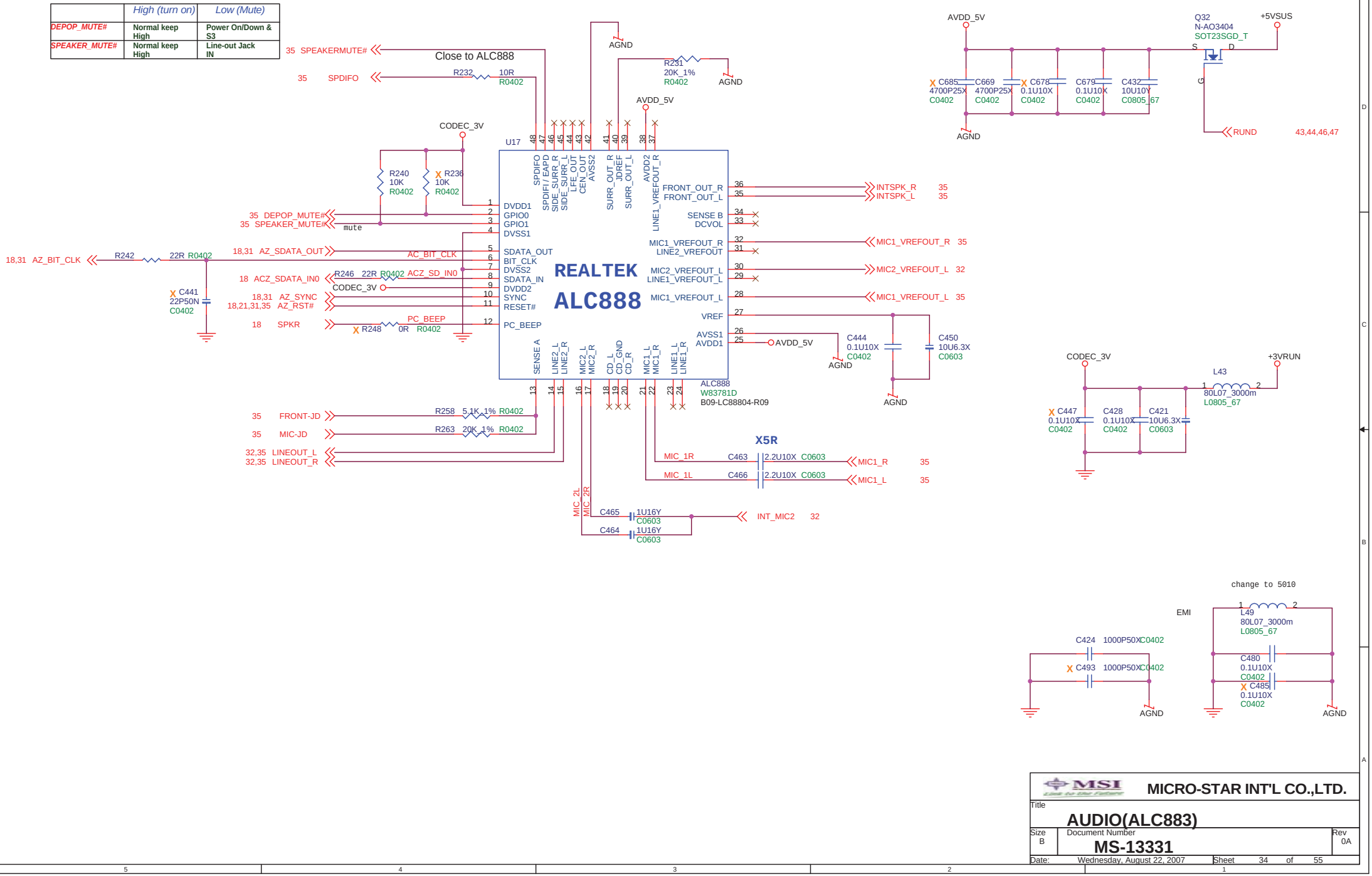
	High (turn on)	Low (Mute)
DEPOP_MUTE#	Normal keep High	Power On/Down & S3
SPEAKER_MUTE#	Normal keep High	Line-out Jack IN



MSI	MICRO-STAR INT'L CO.,LTD.	
Title	AUDIO(ALC883)	
Size B	Document Number MS-13331	Rev 0A
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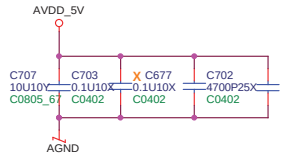
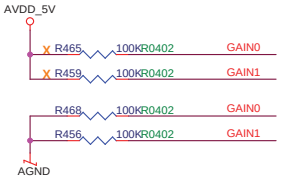
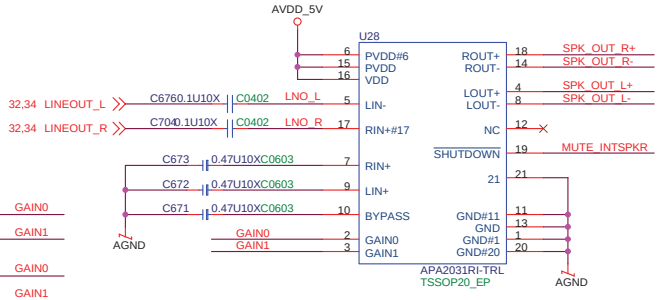
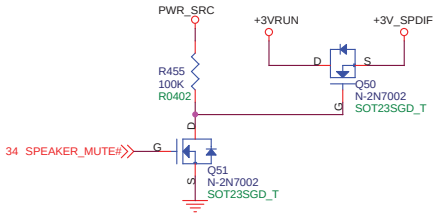


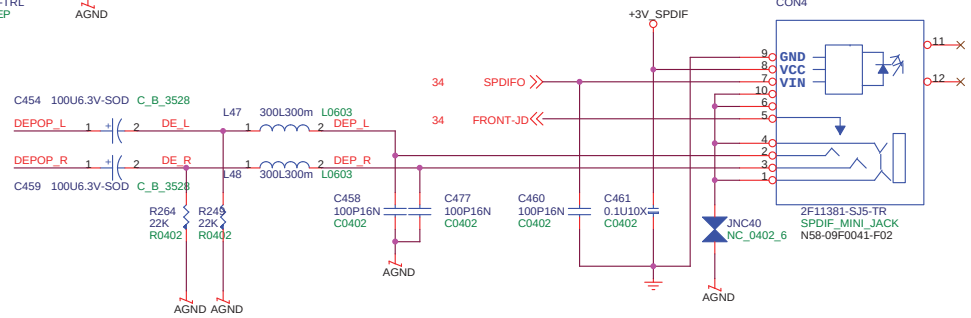
	GAIN0	GAIN1	SE/BTL#
6dB	0	0	0
10dB	0	1	0
15.6dB	1	0	0
21.6dB	1	1	0
4.3dB	X	X	1

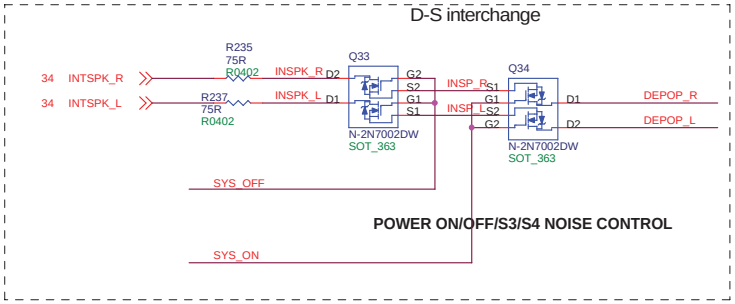




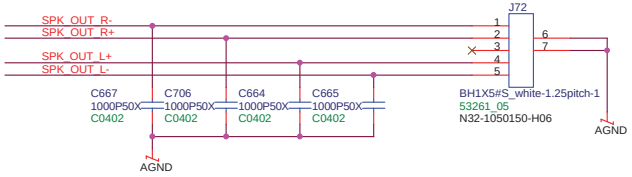


EarPhoneJack

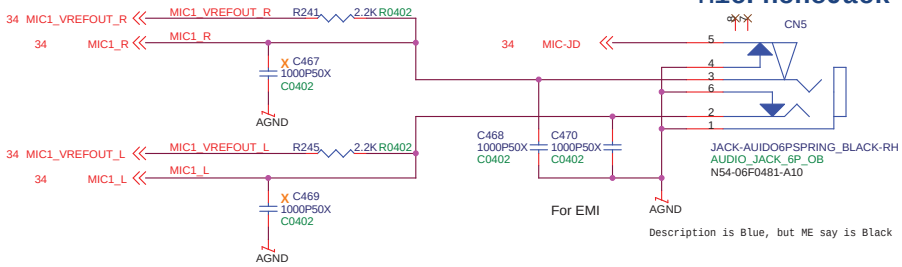


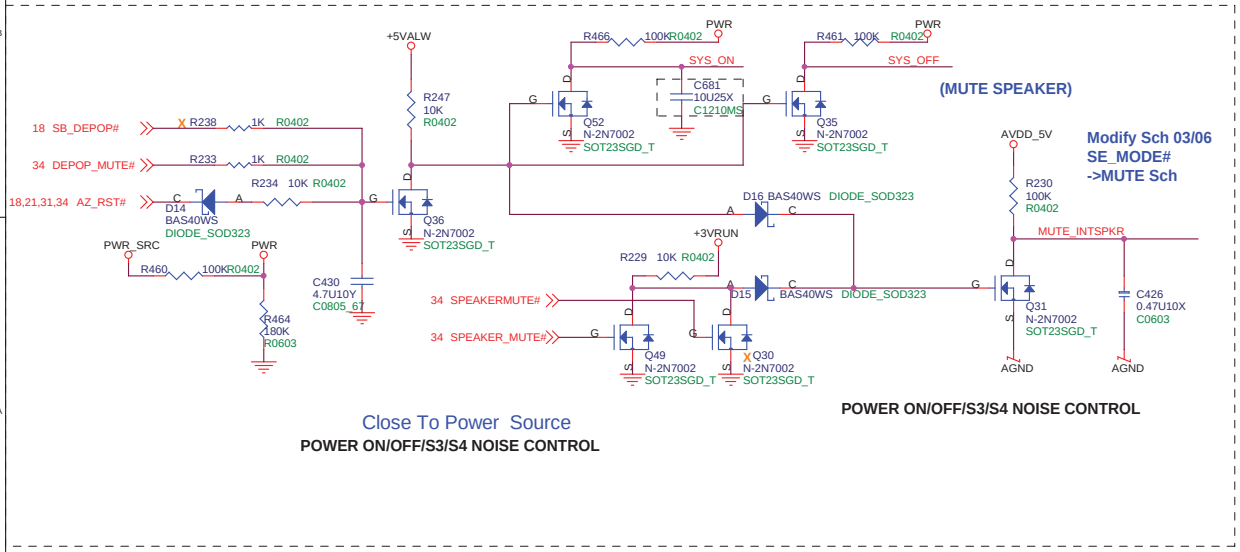


SPEAKER



MicPhoneJack





Mobile Configuation:

(3 external jacks, 1 internal Mic, 2 sets stereo internal speaker)

Pin Assignment	Location	Re-tasking
FRONT(pin-35/36)	SPDIF jack, AMP	SPDIF output, AMP output(Int.SPKR), ?
SURR (pin-39/41)	X	X
CEN/LFE (pin-43/44)	X	X
SIDESURR (pin-45/46)	X	X
LINE1 (pin-23/24)	Line-in jack	Line input, ?
MIC1 (pin-21/22)	MIC-in jack	Mic input, ?
MIC2 (pin-16/17)	Int.MIC	Int.Mic input

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Title: AMP & SPK & MIC & SPK

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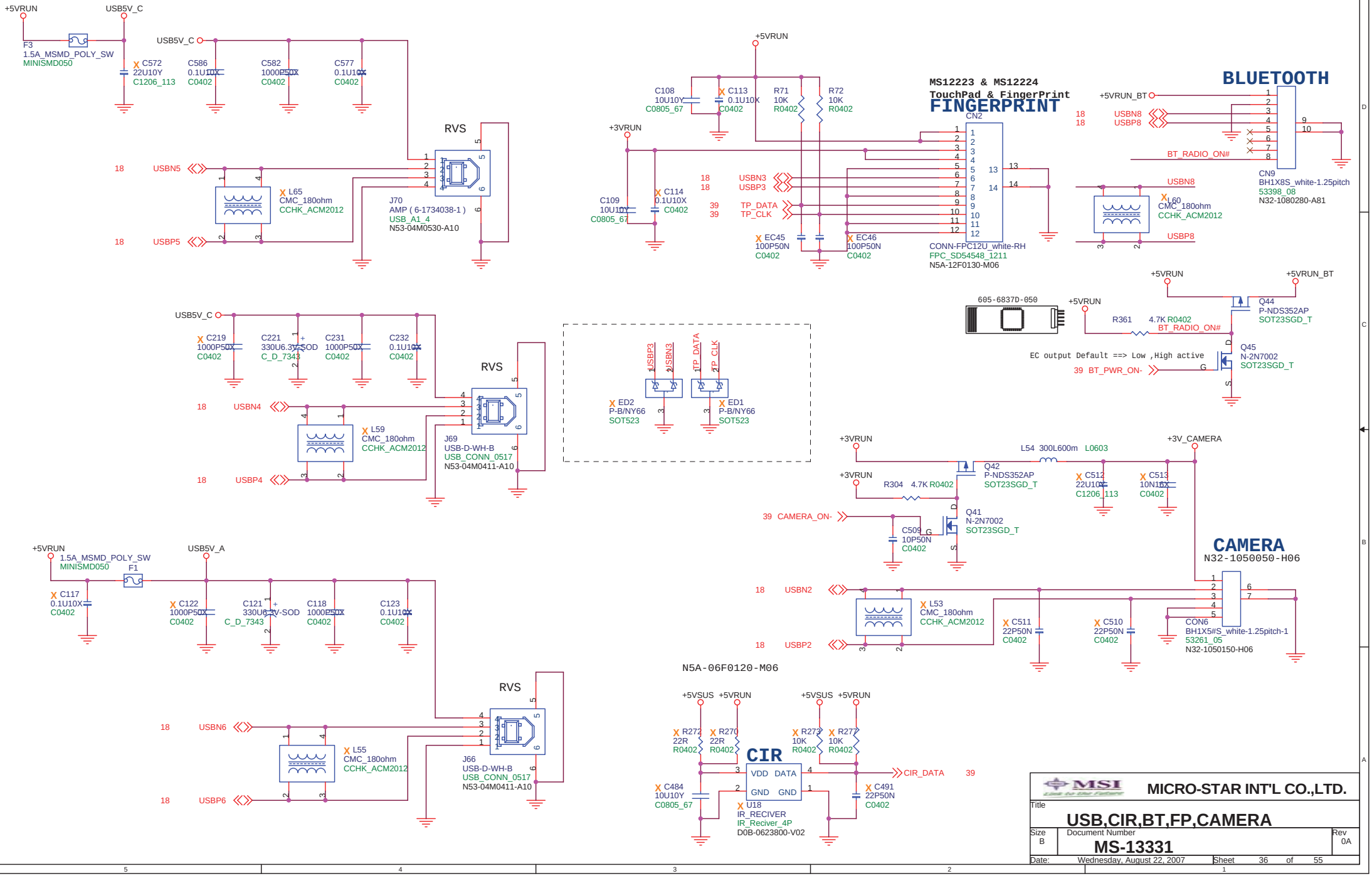
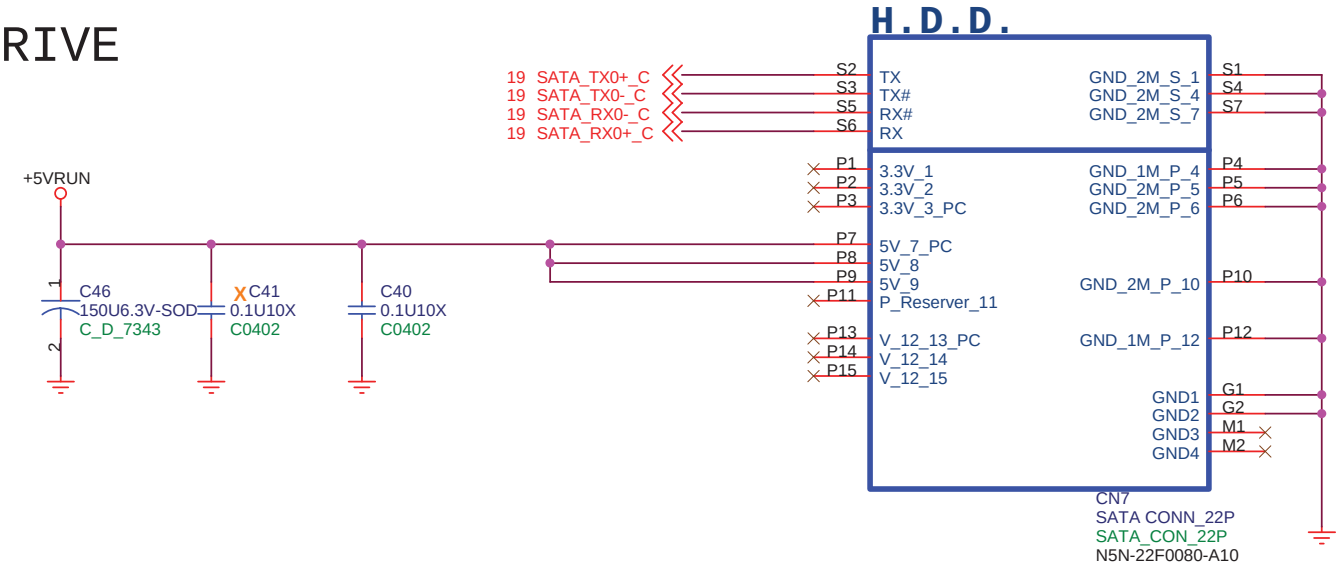
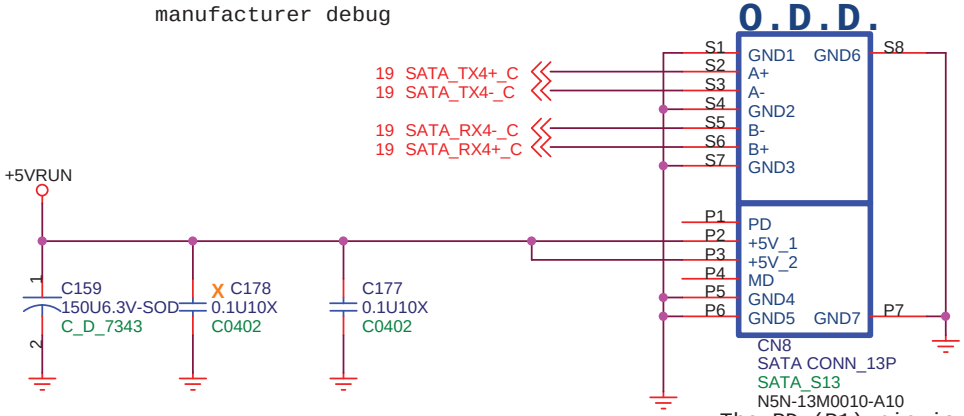


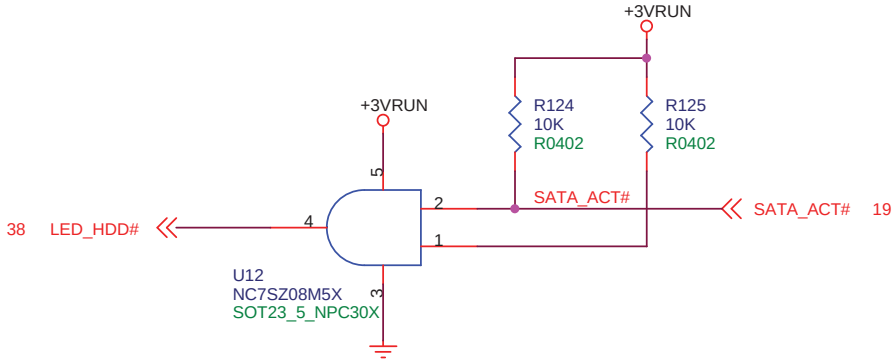
2.5"HD DRIVE



PN & FOOTPRINT N/A

The MD (P4) pin is for ODD manufacturer debug





The PD (P1) pin is for host GIO to detect if the ODD is present or not. In the drive, the pin is “pull-low”. So when host side detects this pin as high,then no device; when host side detect this pin as low, then the device present.

MICRO-STAR INT'L CO.,LTD.

Title: SATA HDD/PATA CDROM CONN

Size	Document Number	Rev
Custom	MS-13331	0A

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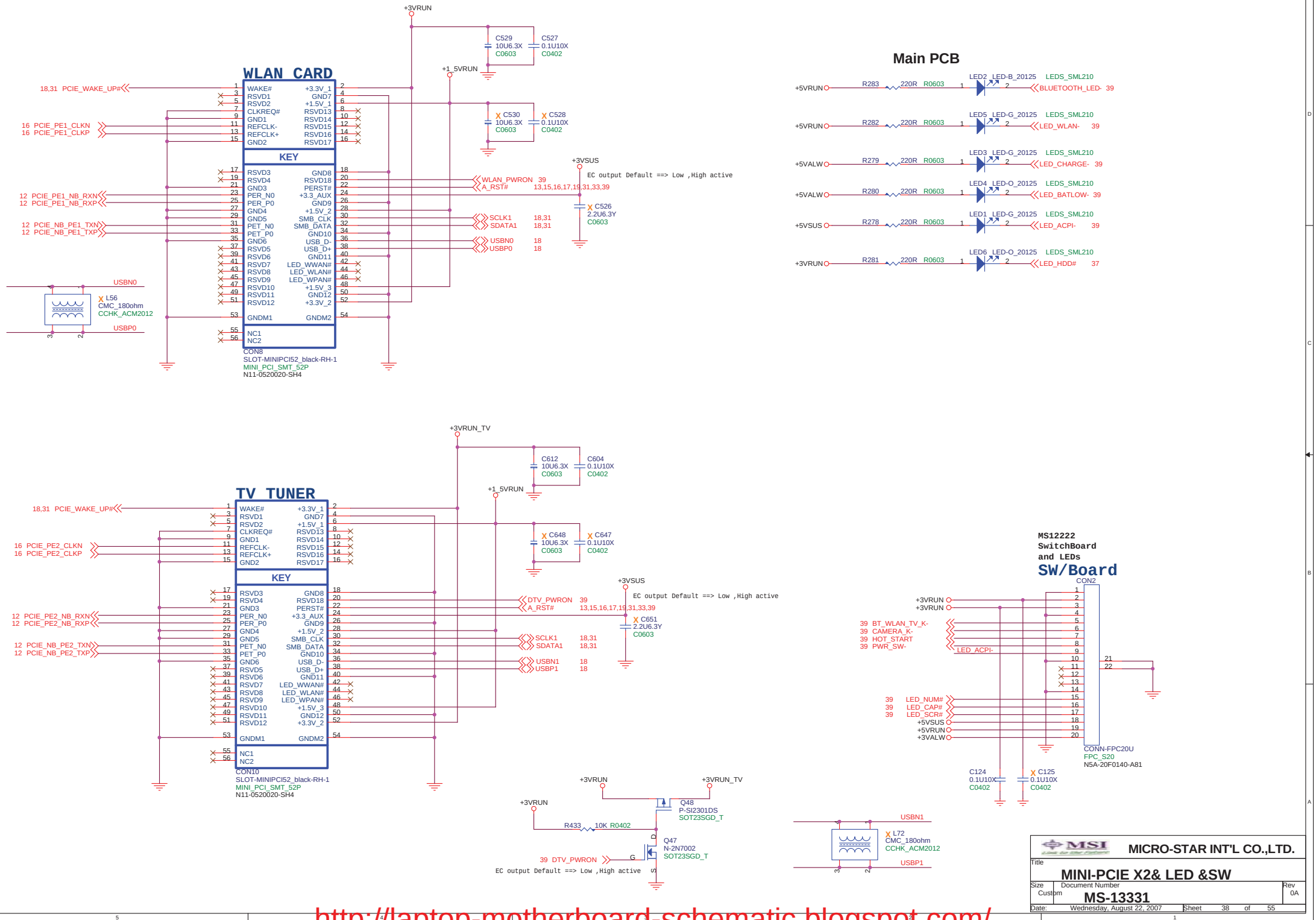

MICRO-STAR INT'L CO.,LTD.

Title: MINI-PCIE X2& LED &SW

Size: Custom | Document Number: MS-13331 | Rev: 0A

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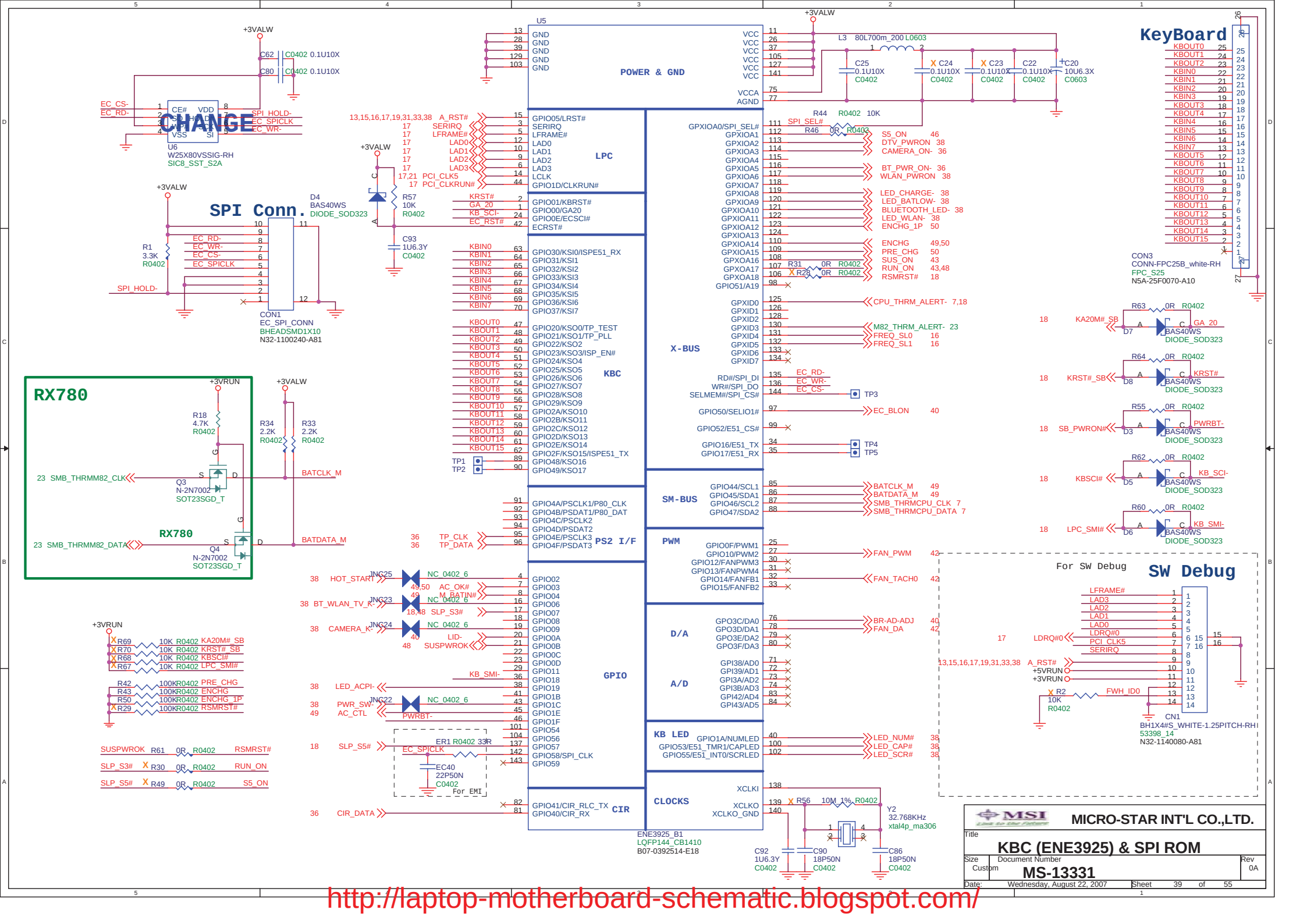
CHANGE
SPI Conn.
RX780
KeyBoard
SW Debug
For SW Debug
POWER & GND
LPC
KBC
X-BUS
SM-BUS
PWM
PS2 I/F
GPIO
D/A
A/D
KB LED
CLOCKS
CIR
MICRO-STAR INT'L CO.,LTD.
KBC (ENE3925) & SPI ROM
MS-13331
Wednesday, August 22, 2007
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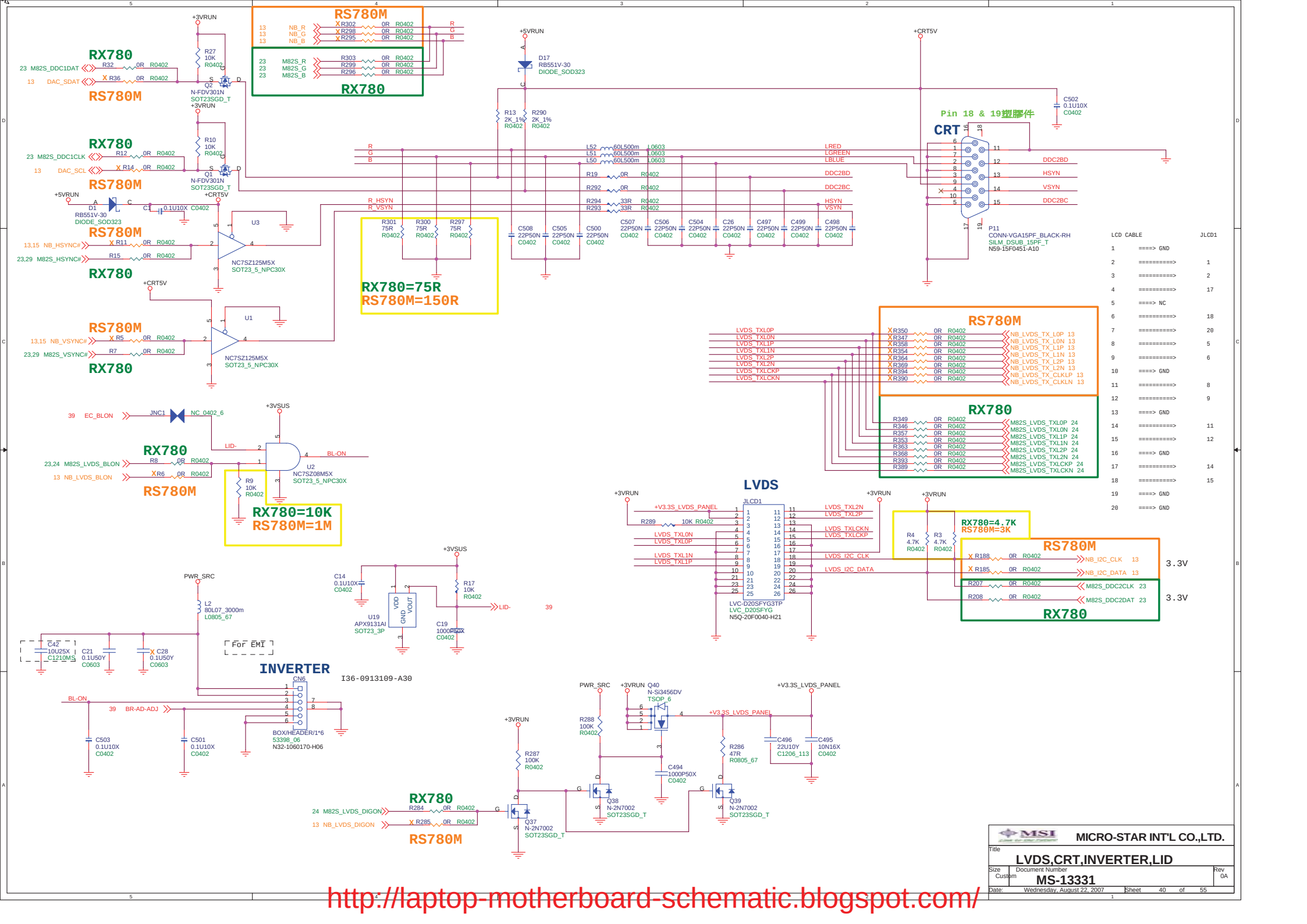
RS780M
RX780
RS780M
RX780
RS780M
RX780
RS780M
RX780
RS780M
RX780
RS780M
RX780
RS780M
RX780
RX780=75R
RS780M=150R
RX780=10K
RS780M=1M
RX780=4.7K
RS780M=3K
LVDS
INVERTER
I36-0913109-A30
CRT
Pin 18 & 19塑膠件
P11
CONN-VGA15PF_BLACK-RH
SILM_DSUB_15PF_T
N59-15F0451-A10
LCD CABLE
JLCD1
MICRO-STAR INT'L CO.,LTD.
LVDS,CRT,INVERTER,LID
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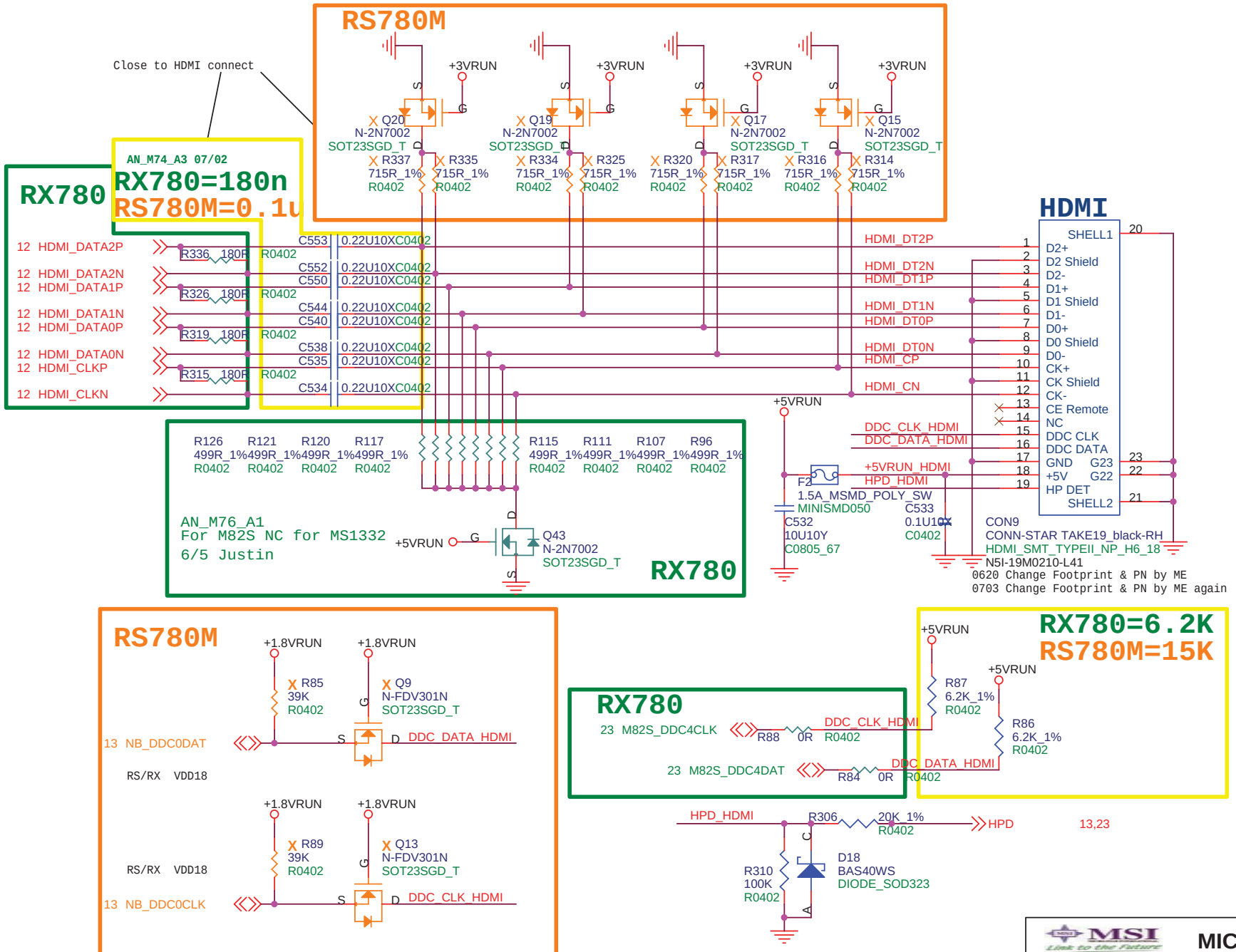

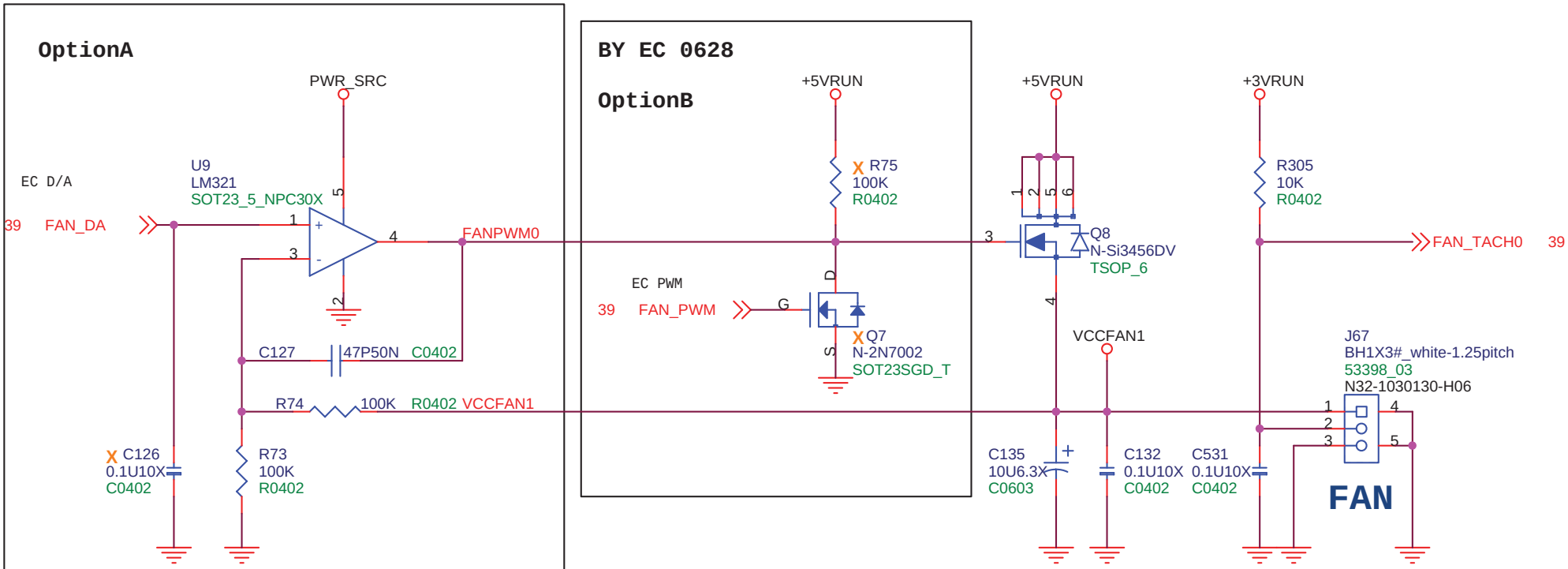

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Title: FAN

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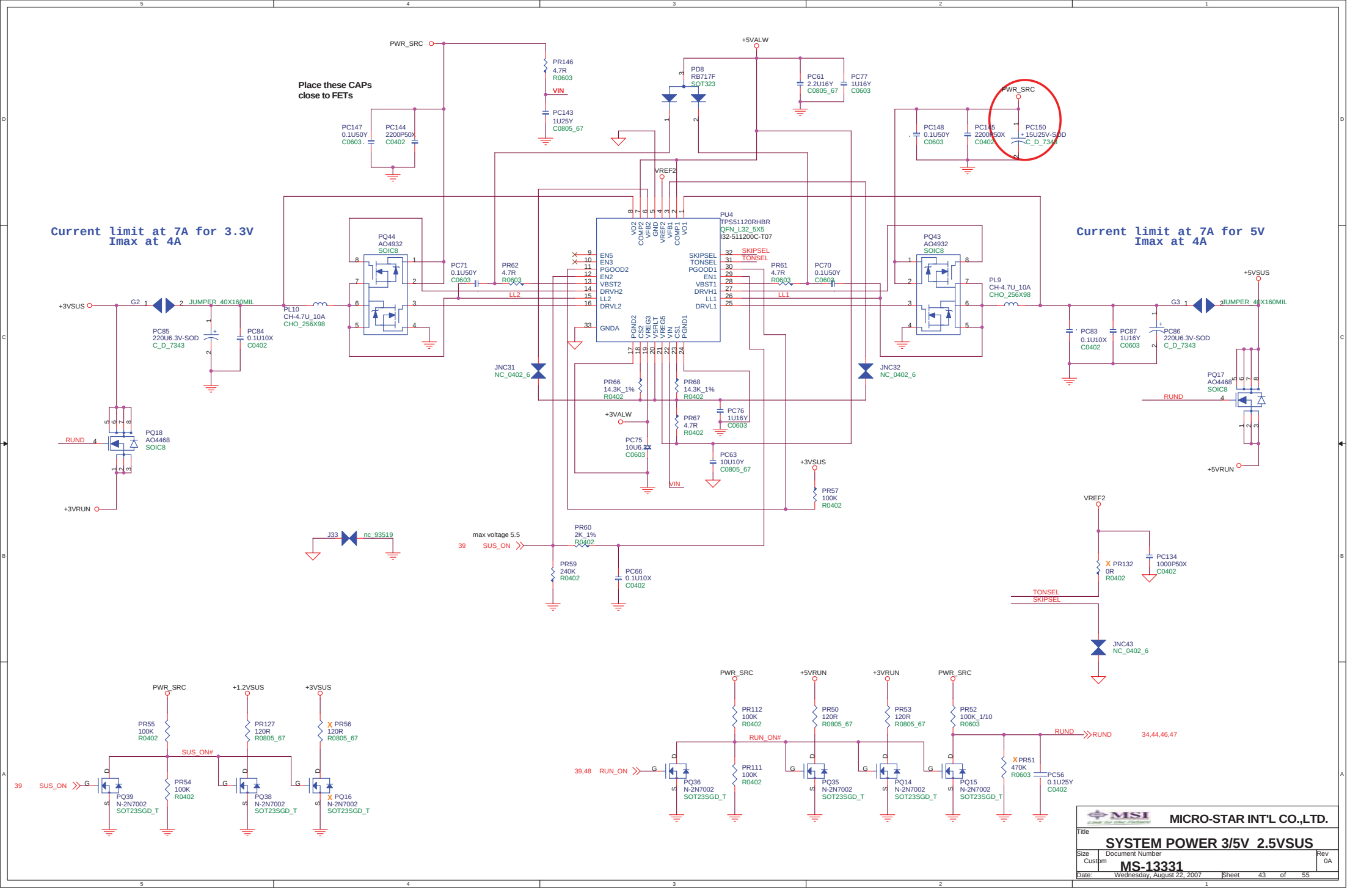

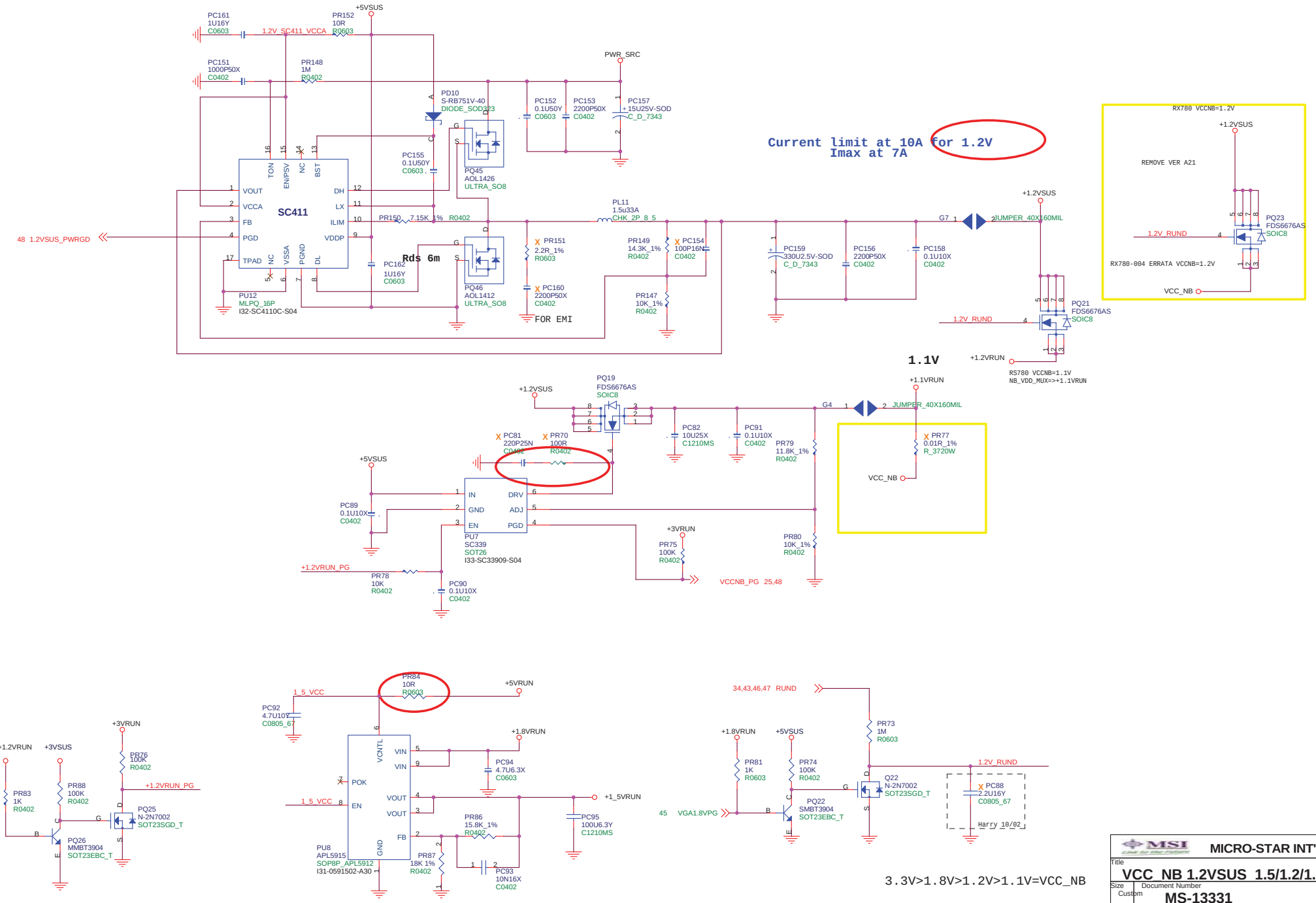

MSI	MICRO-STAR INT'L CO.,LTD.
Title	VCC_NB 1.2VSUS 1.5/1.2/1.1VRUN
Size: Custom	Document Number: MS-13331
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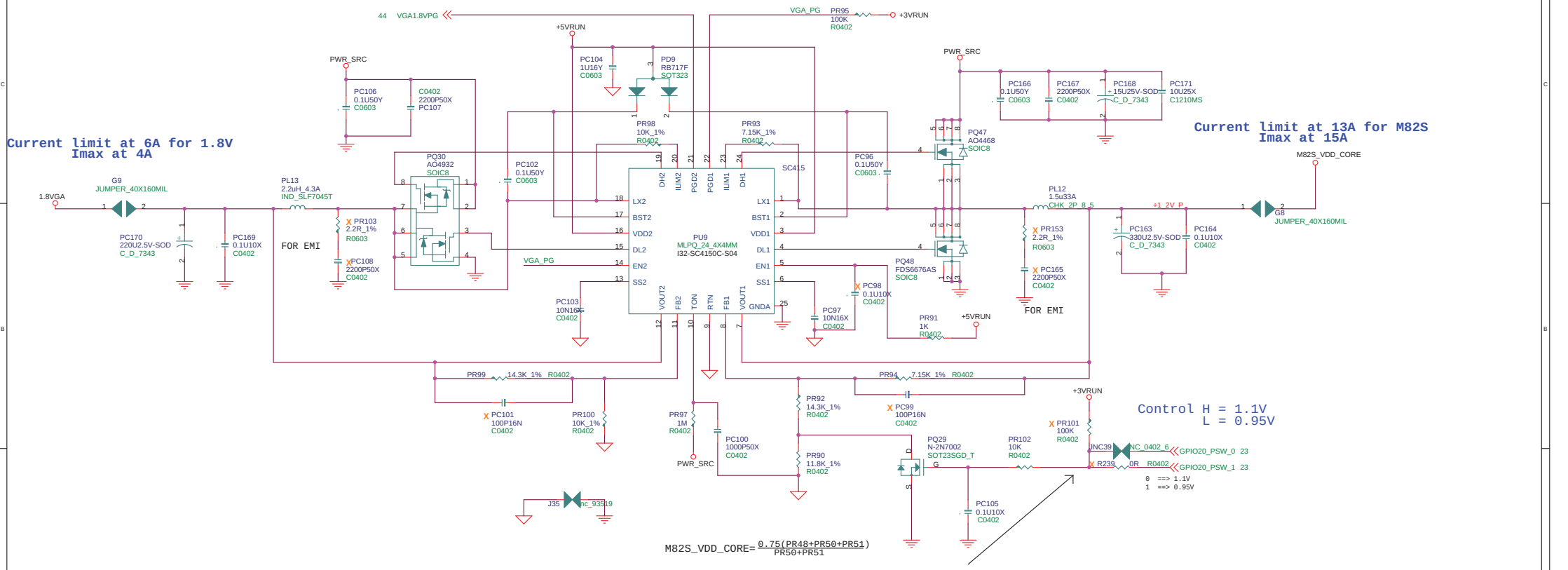
RX780

M82S_VDDC>1.8VRUN>1.2VRUN>1.1VRUN



MICRO-STAR INT'L CO.,LTD.

Title: VGA POWER

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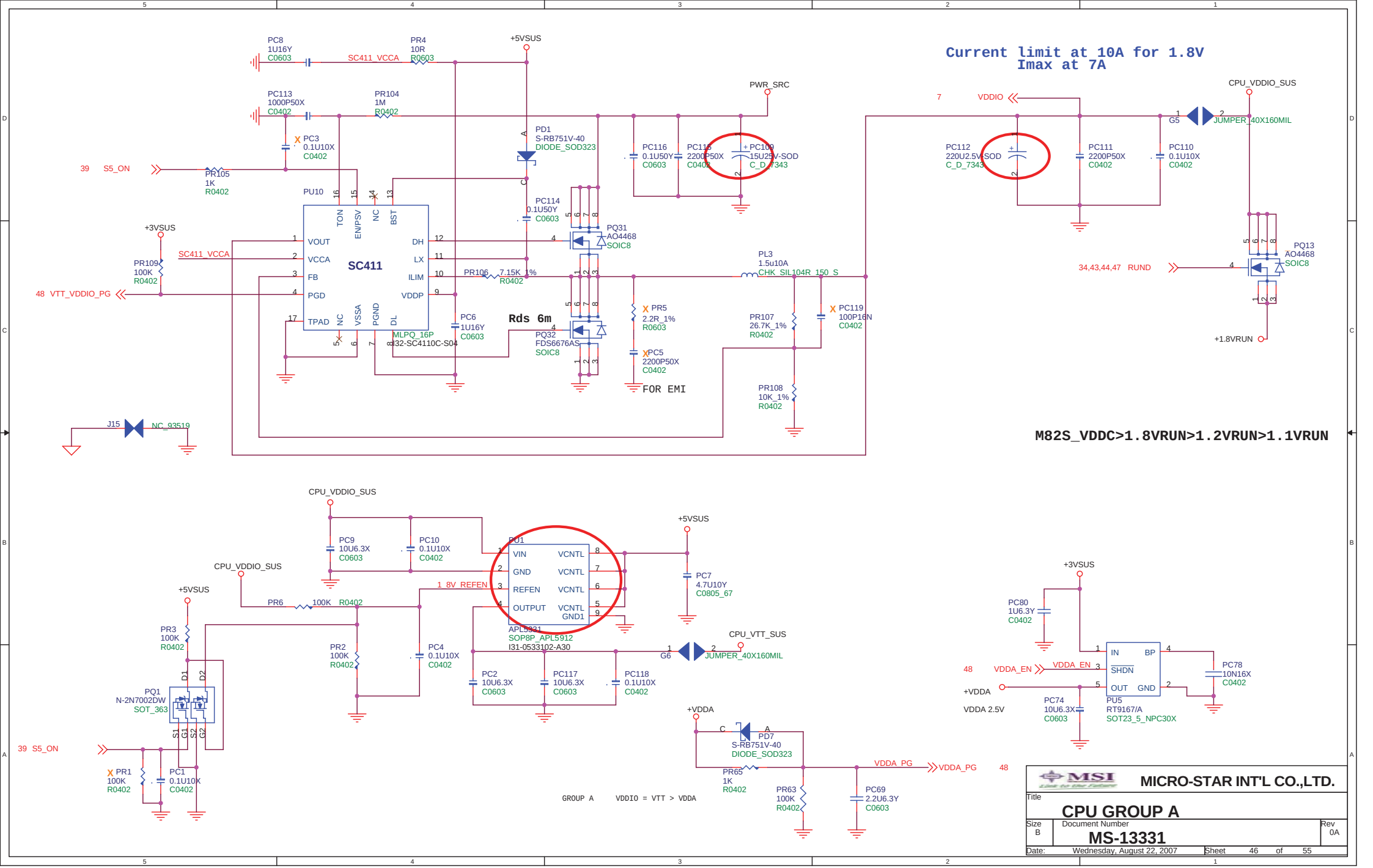

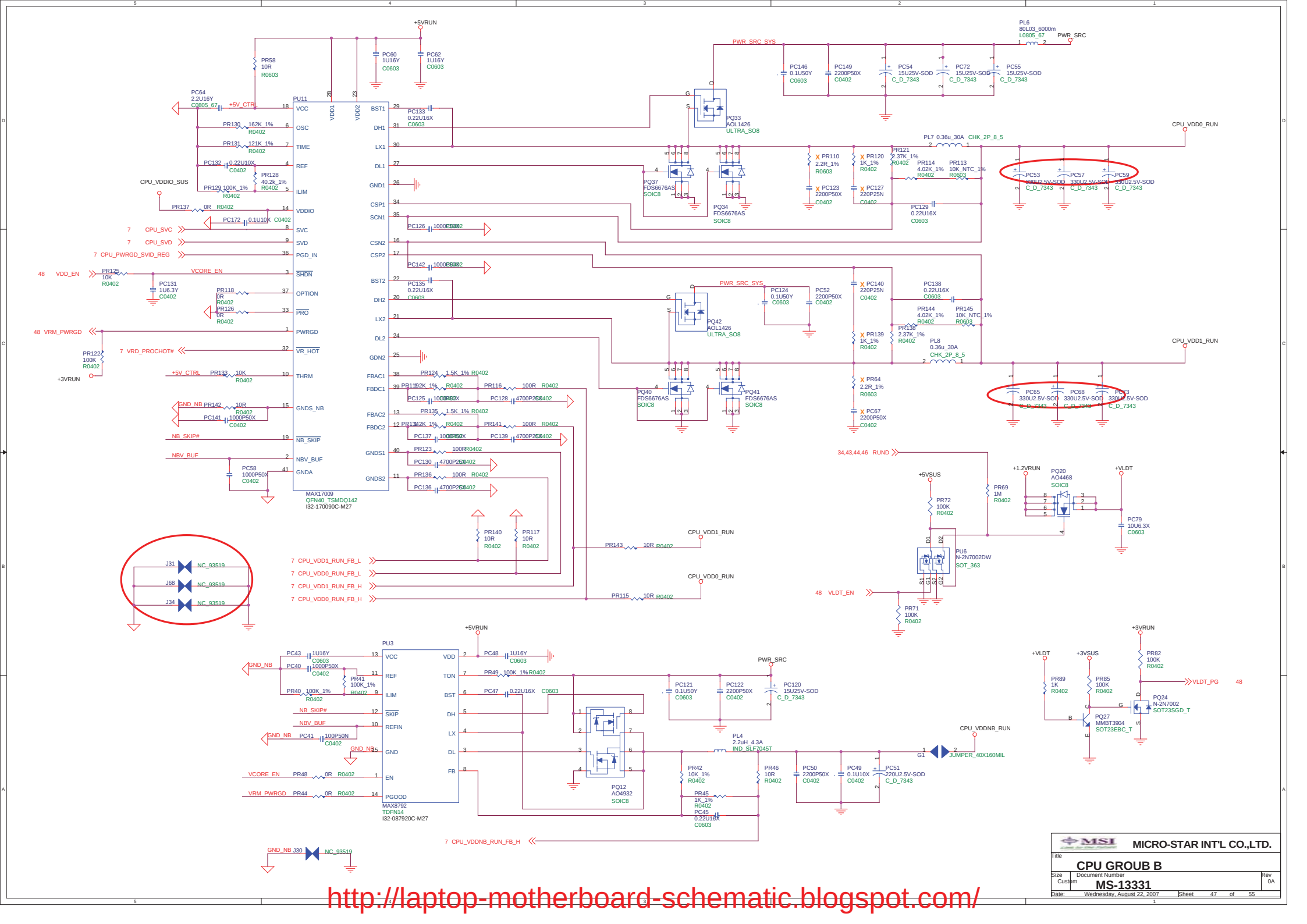
+5VRUN
PU11
MAX17009
QFN40_TSMDQ142
I32-170090C-M27
PWR_SRC_SYS
PWR_SRC
PL6
80L03_6000m
L0805_67
PQ33
AOL1426
ULTRA_SO8
PQ37
FDS6676AS
SOIC8
PQ34
FDS6676AS
SOIC8
PL7 0.36u_30A CHK_2P_8_5
CPU_VDD0_RUN
PQ42
AOL1426
ULTRA_SO8
PQ40
FDS6676AS
SOIC8
PQ41
FDS6676AS
SOIC8
PL8
0.36u_30A
CHK_2P_8_5
CPU_VDD1_RUN
CPU_VDDIO_SUS
VCORE_EN
VDD_EN
VRM_PWRGD
CPU_SVC
CPU_SVD
CPU_PWRGD_SVID_REG
VRD_PROCHOT#
NB_SKIP#
NBV_BUF
GND_NB
+3VRUN
+5V_CTRL
34,43,44,46 RUND
+5VSUS
+1.2VRUN
+VLDT
PQ20
AO4468
SOIC8
PU6
N-2N7002DW
SOT_363
VLDT_EN
PU3
MAX8792
TDFN14
I32-087920C-M27
PWR_SRC
CPU_VDDNB_RUN
JUMPER_40X160MIL
+3VSUS
PQ24
N-2N7002
SOT23SGD_T
PQ27
MMBT3904
SOT23EBC_T
VLDT_PG
7 CPU_VDDNB_RUN_FB_H
MICRO-STAR INT'L CO.,LTD.
CPU GROUB B
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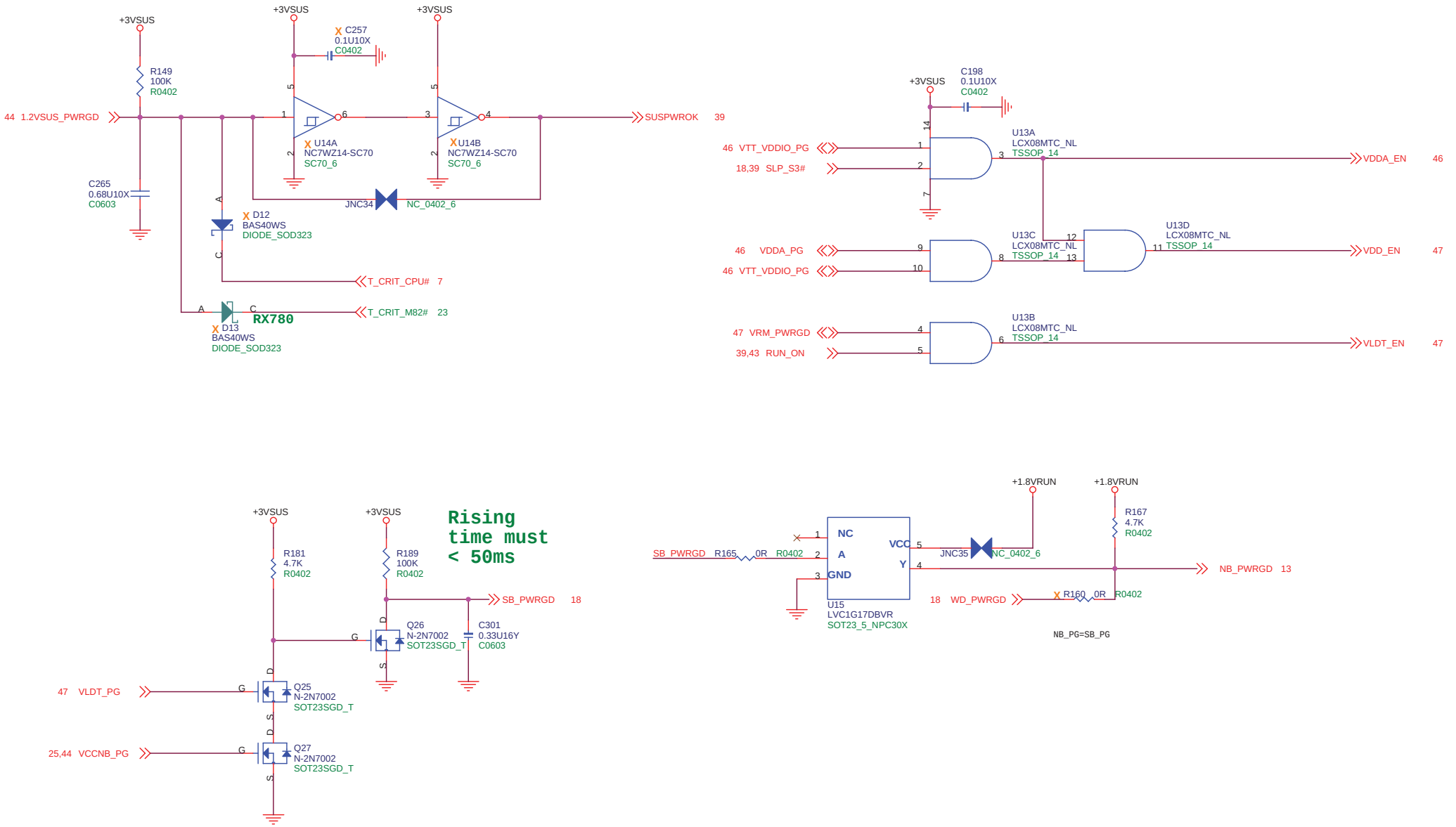

MICRO-STAR INT'L CO.,LTD.

Title: PWRGD

Size: B | Document Number: MS-13331 | Rev: 0A

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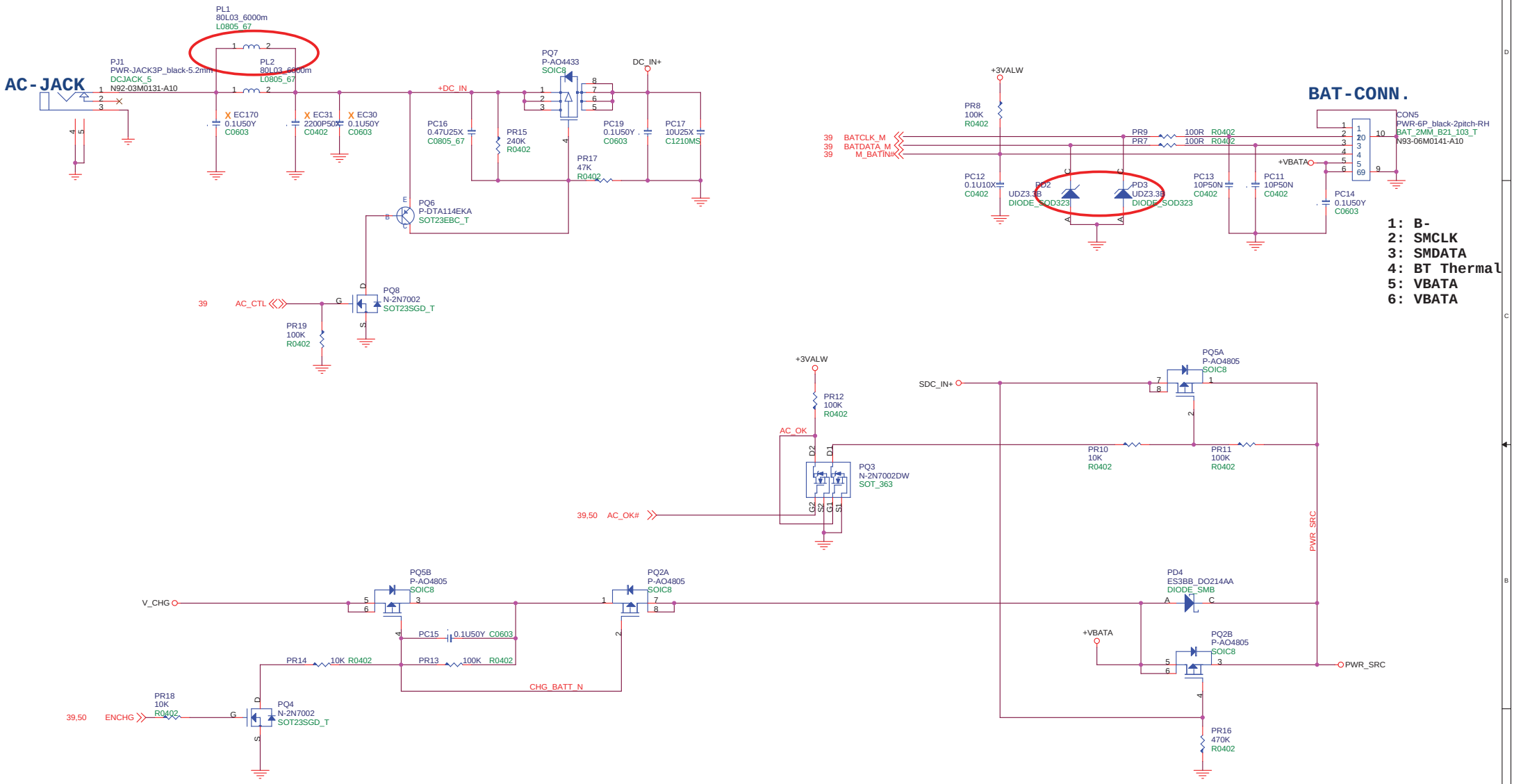

MICRO-STAR INT'L CO.,LTD.

Title: **Battery Select**

Size: Custom | Document Number: **MS-13331** | Rev: 0A

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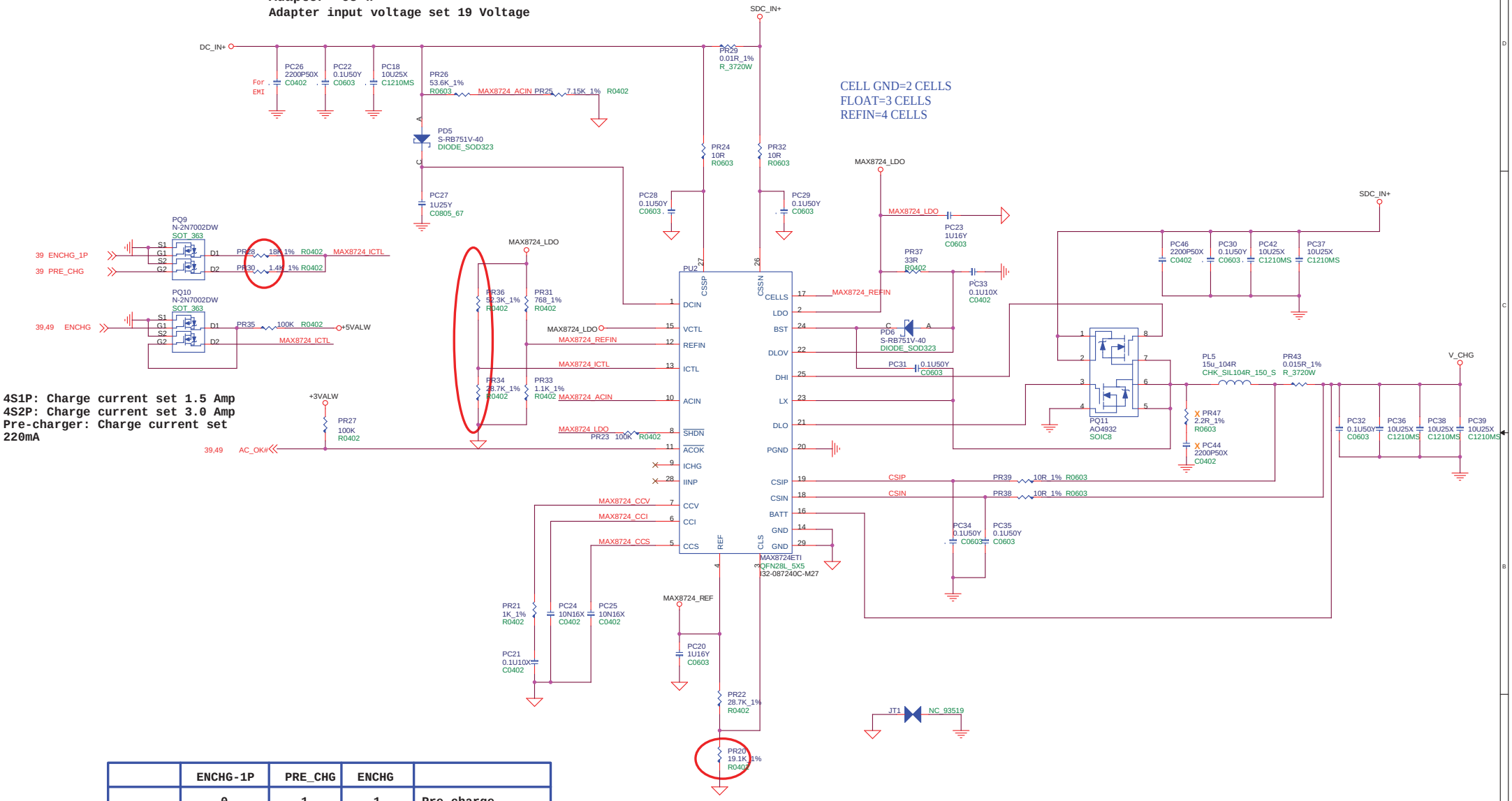
Adapter= 65 W
Adapter input voltage set 19 Voltage



4S1P: Charge current set 1.5 Amp
4S2P: Charge current set 3.0 Amp
Pre-charger: Charge current set 220mA

	ENCHG-1P	PRE_CHG	ENCHG	
	0	1	1	Pre-charge
	0	0	1	4S2P-Fast charge
	1	0	1	4S1P-Fast charge
	X	X	0	STOP CHARGE

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Title: M_Battery Charger

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