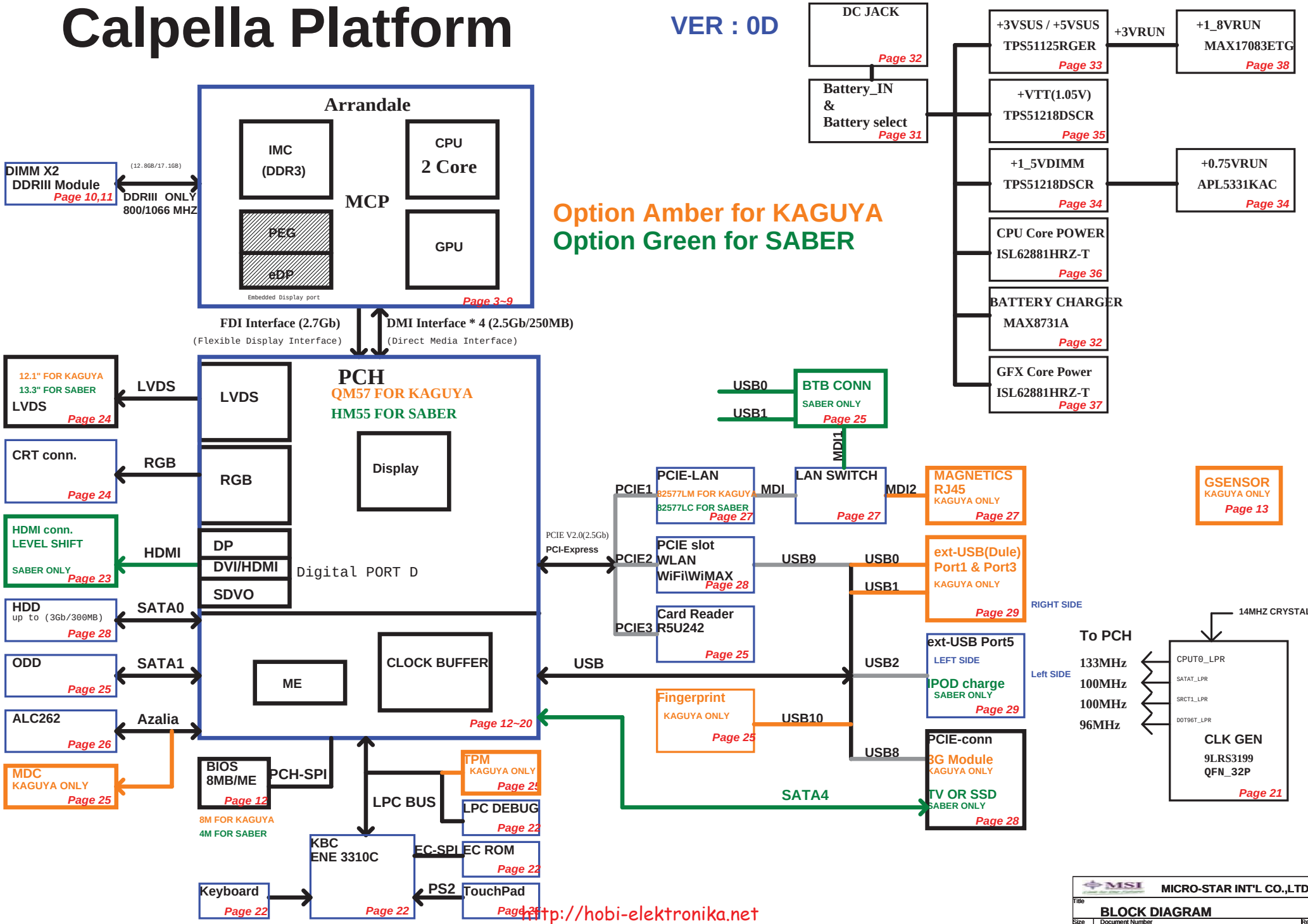
Calpella Platform

VER : 0D



MICRO-STAR INT'L CO.,LTD.

Title: BLOCK DIAGRAM

Size: Custom | Document Number: MS-1251 | Rev: 0D

Date: Friday, October 15, 2010 | Sheet 1 of 39

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails

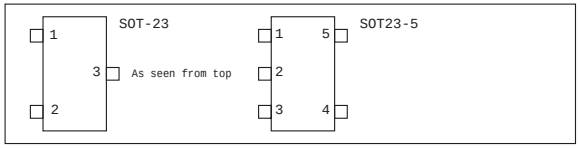
Voltage	Description	Control Signal
PWR_SRC	AC ADAPTER OR BATTERY IN	
+5VALW	5.0V always on power rail	PWR_SRC
+3VALW	3.3V always on power rail	PWR_SRC
+5VSUS	5.0V power rail	SUS_ON
+3VSUS	3.3V power rail	SUS_ON
+1_5VDIMM	1.5V power rail DDR (off in S4-S5)	PM_SLP_S4#
+5VRUN	5.0V switched power rail (off in S3-S5)	PM_SLP_S3#
+3VRUN	3.3V switched power rail (off in S3-S5 / M0)	PM_SLP_S3#
+1_8VRUN	1.8V Power rail Processor of VCCPLL1(off in S3-S5)	PM_SLP_S3#
+1_5VRUN	1.5V switched power rail (off in S3-S5)	RUND
+0_75VRUN	0.75V DDR Termination voltage (off in S3-S5)	PM_SLP_S3#
+VTT	1.05 rail for Processor & PCH (off in S3-S5 /M0)	PM_SLP_S3#
+VCC_GFXCORE	0.4V to 1.25V Power rail Graphics Core(off in S3-S5)	GFXVR_EN_R
+VCC_CORE	0.25V to 1.5V Core Voltage for Processor	VR_ON
+V1.1M	1.05V rail for PCH	PM_SLP_M#
+V3.3M	3.3V power rail LAN	PM_SLP_LAN#

Net Naming Conventions

Suffix
`#` = Active Low Signal

Prefix
`H` = Host
`M` = DDR Memory
`TP` = Test Point (does not connect anywhere else)

PCB Footprints

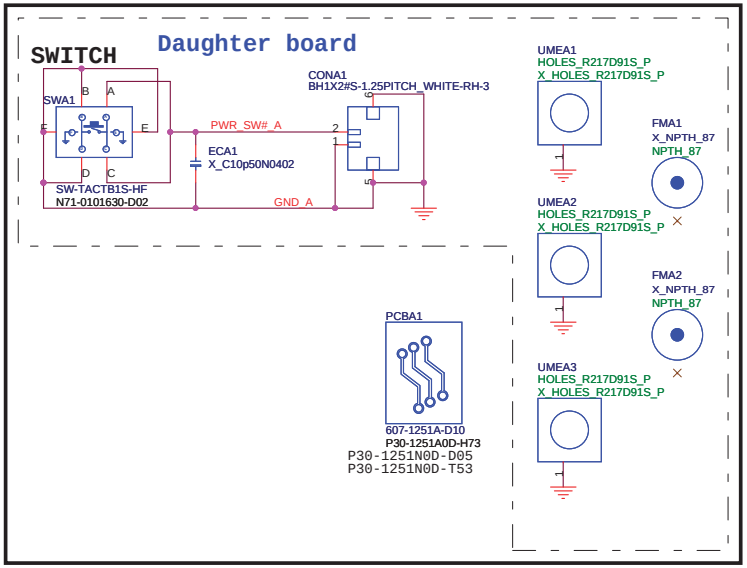


POWER STATES

POWER STATES

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	SLP_M#	SLP_LAN#	+V*ALWAYS	+V3.3M +V1.05_LAN_M	+V1.05M	+*VSUS	+*VRUN	+VTT	Clocks
S0(Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON	ON	ON
S3(Suspend to RAM) /M3	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	OFF	OFF	OFF
S4(Suspend to Disk) /M3	LOW	LOW	HIGH	HIGH	HIGH	ON	ON	ON	ON	OFF	OFF	OFF
S5 (Soft OFF) /M3	LOW	LOW	LOW	HIGH	HIGH	ON	ON	ON	ON	OFF	OFF	OFF
S3(Suspend to RAM) /Moff	LOW	HIGH	HIGH	LOW	LOW	ON	OFF	OFF	ON	OFF	OFF	OFF
S4(Suspend to Disk) /Moff	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF	OFF	OFF
S5 (Soft OFF) /Moff	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF	OFF	OFF
S3(Suspend to RAM) /Moff w/WOL_EN	LOW	HIGH	HIGH	LOW	HIGH	ON	ON	OFF	ON	OFF	OFF	OFF
S4(Suspend to Disk) /Moff w/WOL_EN	LOW	LOW	HIGH	LOW	HIGH	ON	ON	OFF	ON	OFF	OFF	OFF
S5 (Soft OFF) /Moff w/WOL_EN	LOW	LOW	LOW	LOW	HIGH	ON	ON	OFF	ON	OFF	OFF	OFF

Note : WHEN AC MODE , System turn on then +V*SUS will always keep high



MSI MICRO-STAR INT'L CO.,LTD.

Title: PLATFORM

Size: Custom | Document Number: MS-1251 | Rev: 0D

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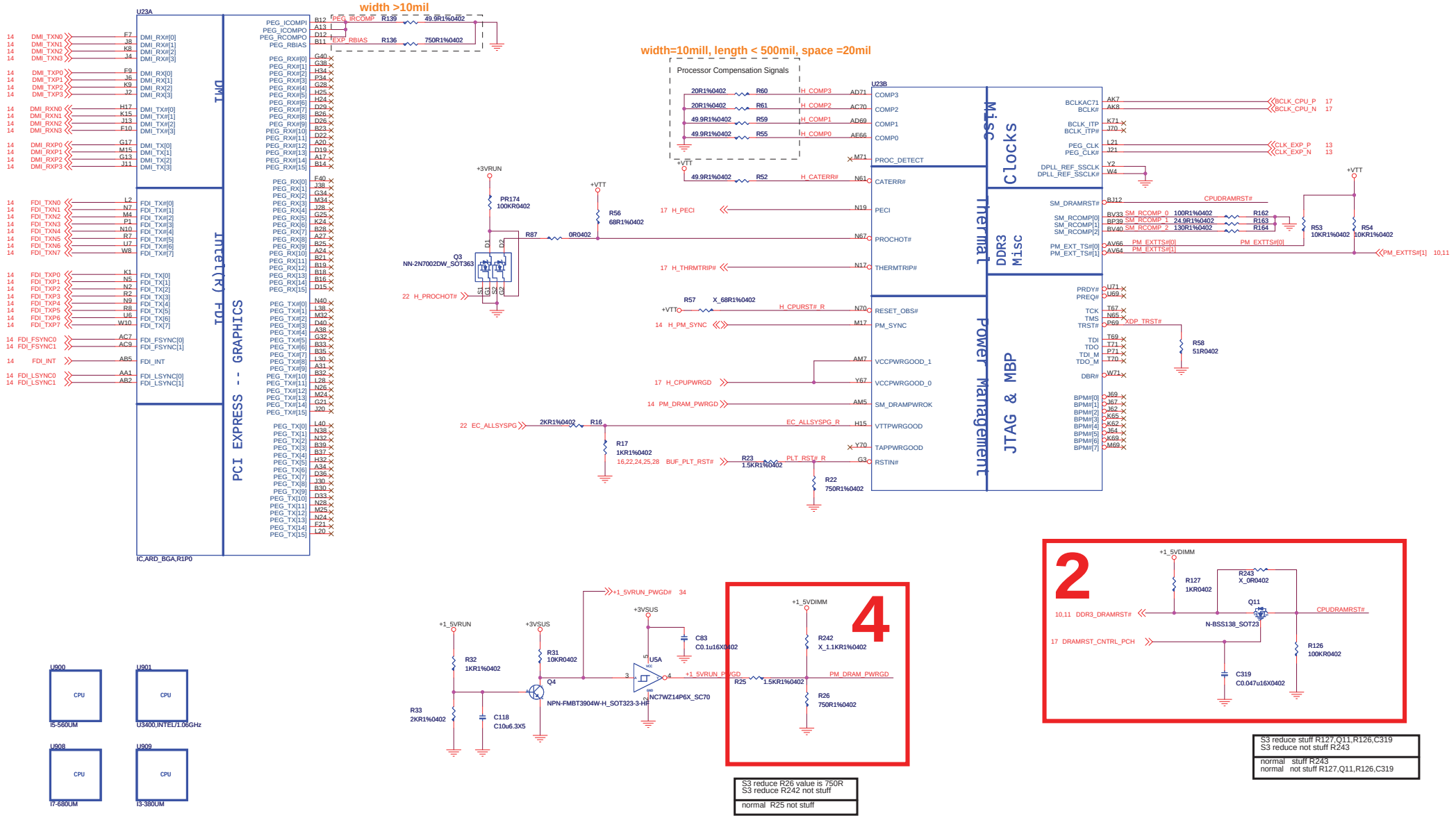
ARRANDALE BGA PROCESSOR (CLK,MISC,JTAG)



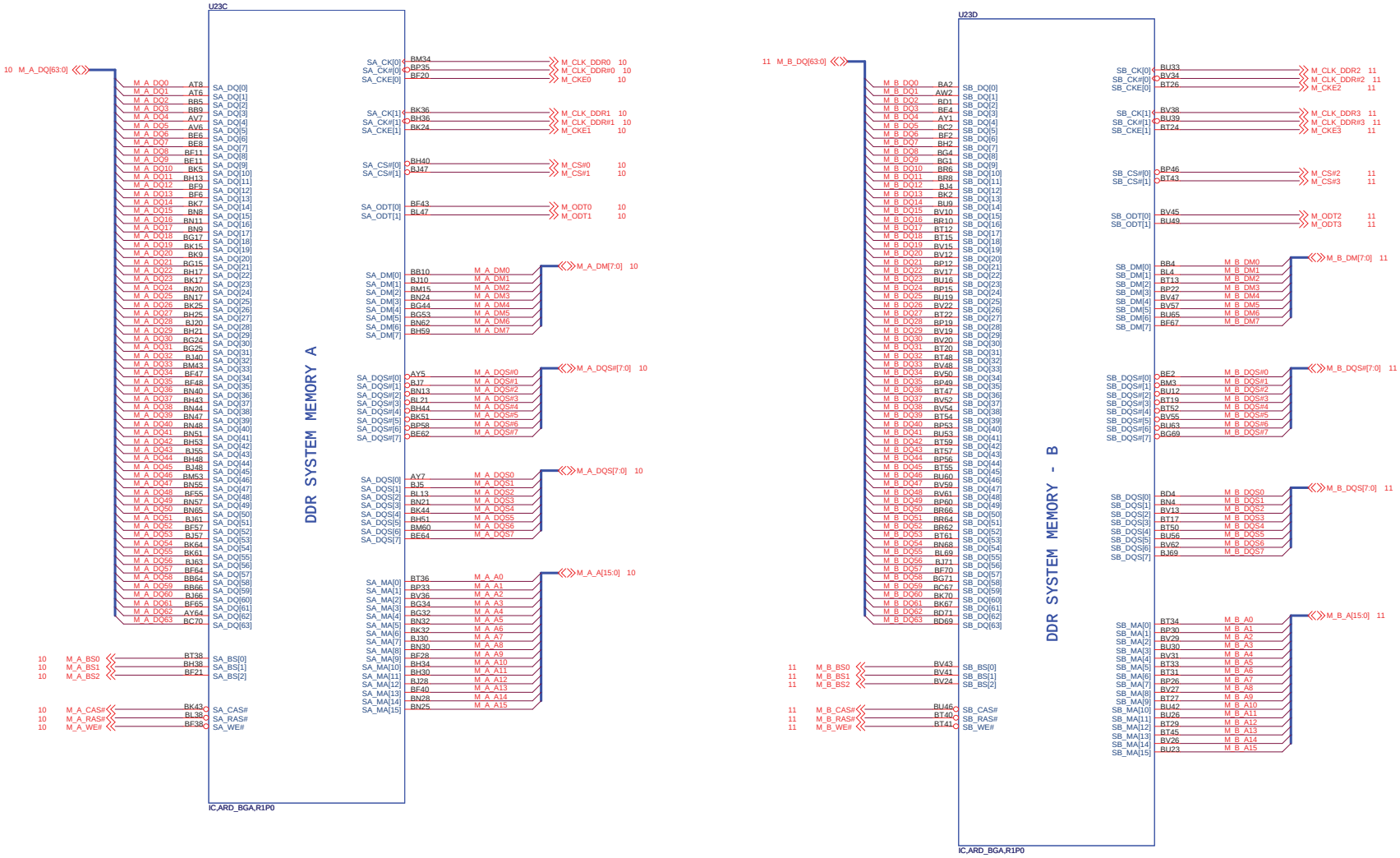
MICRO-STAR INT'L CO.,LTD.

Title: PROCESSOR-1 (HOST BUS)

Size: Custom | Document Number: MS-1251 | Rev: 0D

Date: Friday, October 15, 2010 | Sheet 3 of 39

ARRANDALE BGA PROCESSOR (DDR3)



MICRO-STAR INT'L CO.,LTD.

Title: PROCESSOR-2 (DDR3)

Size: C | Document Number: MS-1251 | Rev: 0D

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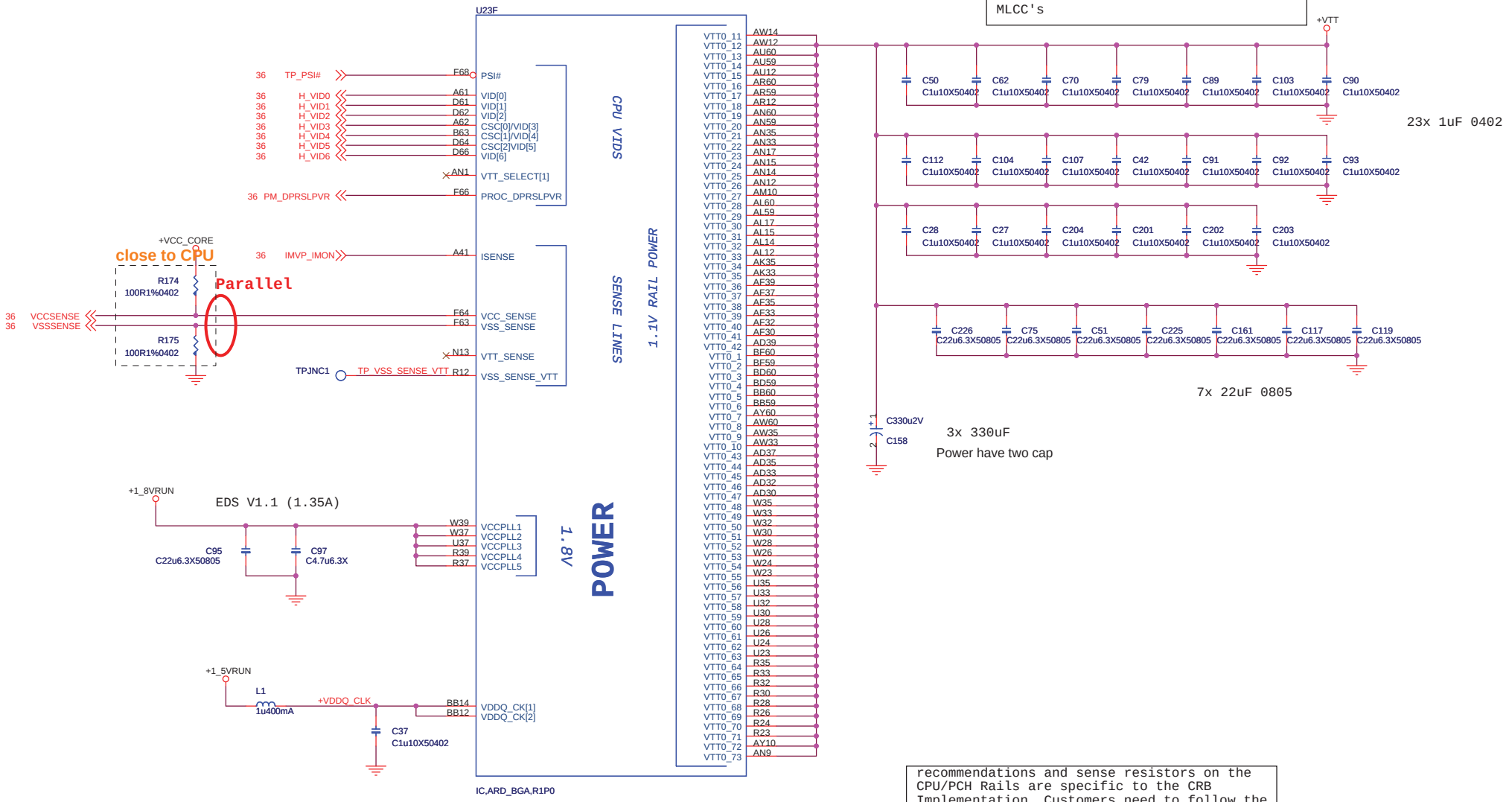
ARRANDALE BGA PROCESSOR (POWER)

Layout Note: Place 2 NO_STUFF caps on TOP and the 7 caps on BOTTOM.

Layout Note: Swap the placement location for bulks and these MLCC's



recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide
Please note that the VTT Rail Values are Arrandale VTT=1.05V

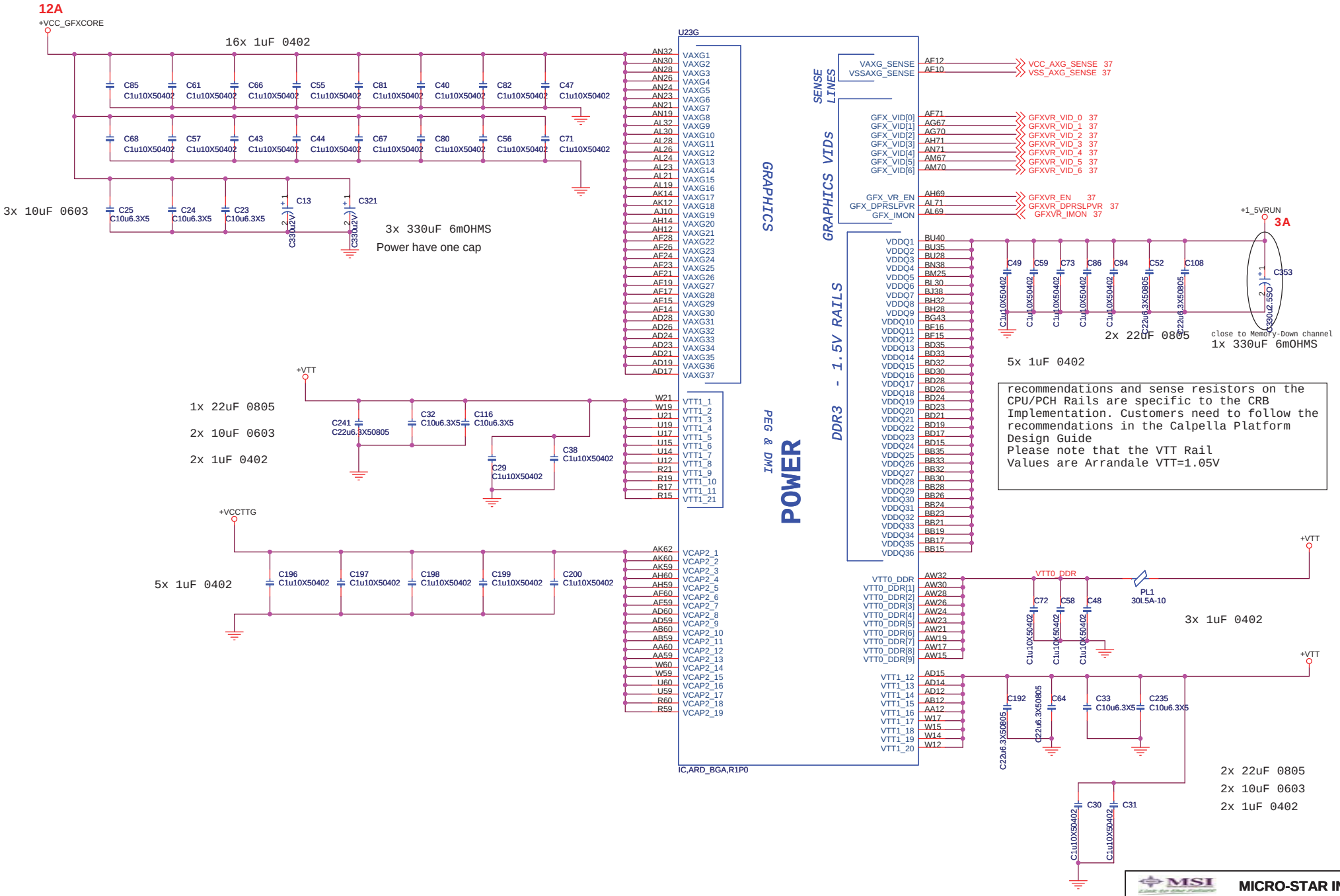
MICRO-STAR INT'L CO.,LTD.

Title: PROCESSOR-3 (VTT_CORE POWER)

Size: A3 | Document Number: MS-1251 | Rev: 0D

Date: Friday, October 15, 2010 | Sheet 5 of 39

ARRANDALE BGA PROCESSOR (GRAPHICS POWER)



http://hobi-elektronika.net

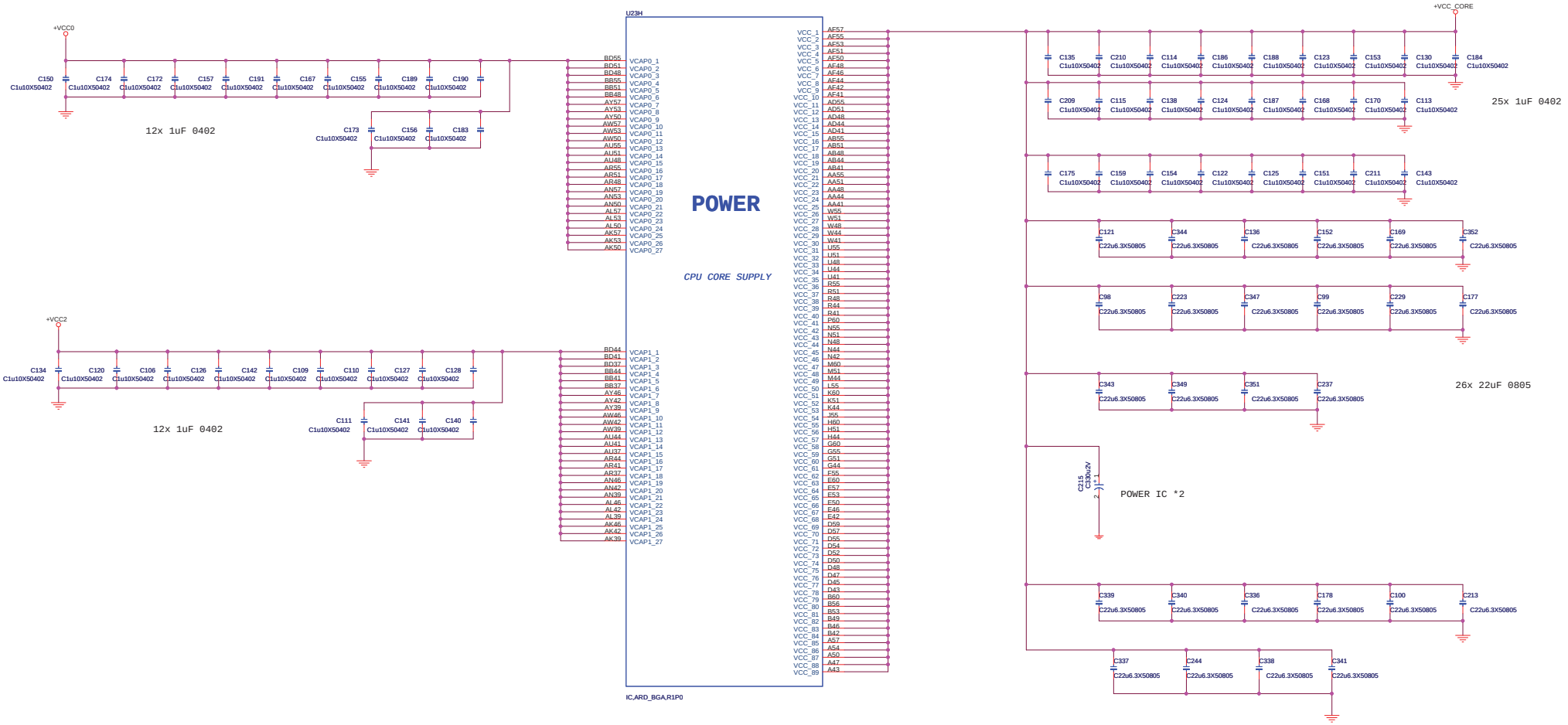
MICRO-STAR INT'L CO.,LTD.

Title: PROCESSOR-4 (GRAPHICS POWER)

Size	Document Number	Rev
A3	MS-1251	0D

Date: Friday, October 15, 2010 Sheet 6 of 39

ARRANDALE BGA PROCESSOR (VCORE POWER)



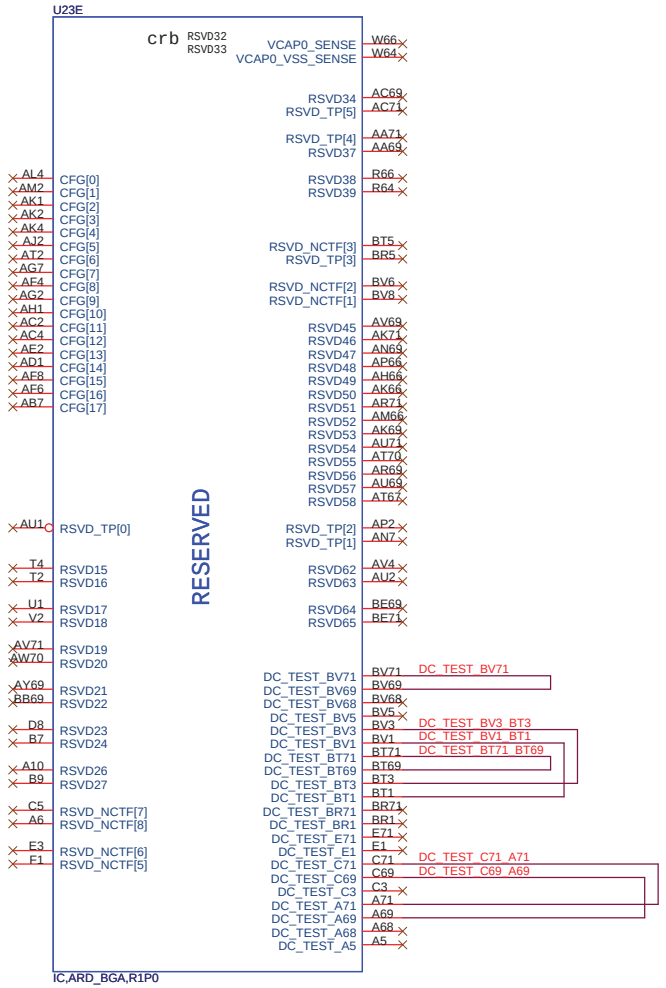
MICRO-STAR INT'L CO.,LTD.

Title: PROCESSOR-5 (CPU CORE)

Size: A2 | Document Number: MS-1251 | Rev: 0D

Date: Friday, October 15, 2010 | Sheet 7 of 39

ARRANDALE BGA PROCESSOR (RESERVED)



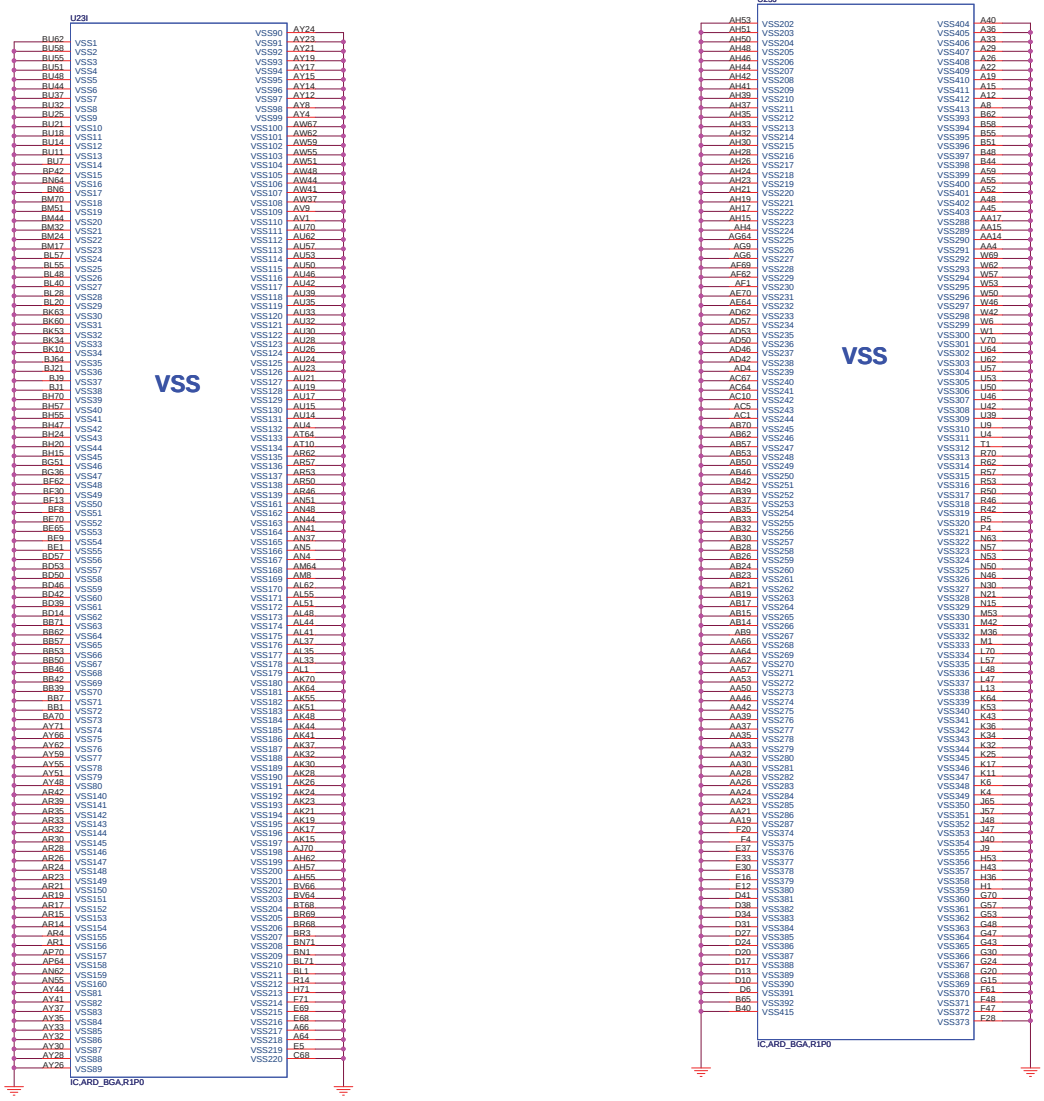
MICRO-STAR INT'L CO.,LTD.

Title: PROCESSOR-6 (RESERVE)

Size	Document Number	Rev
A3	MS-1251	0D

Date: Friday, October 15, 2010 Sheet 8 of 39

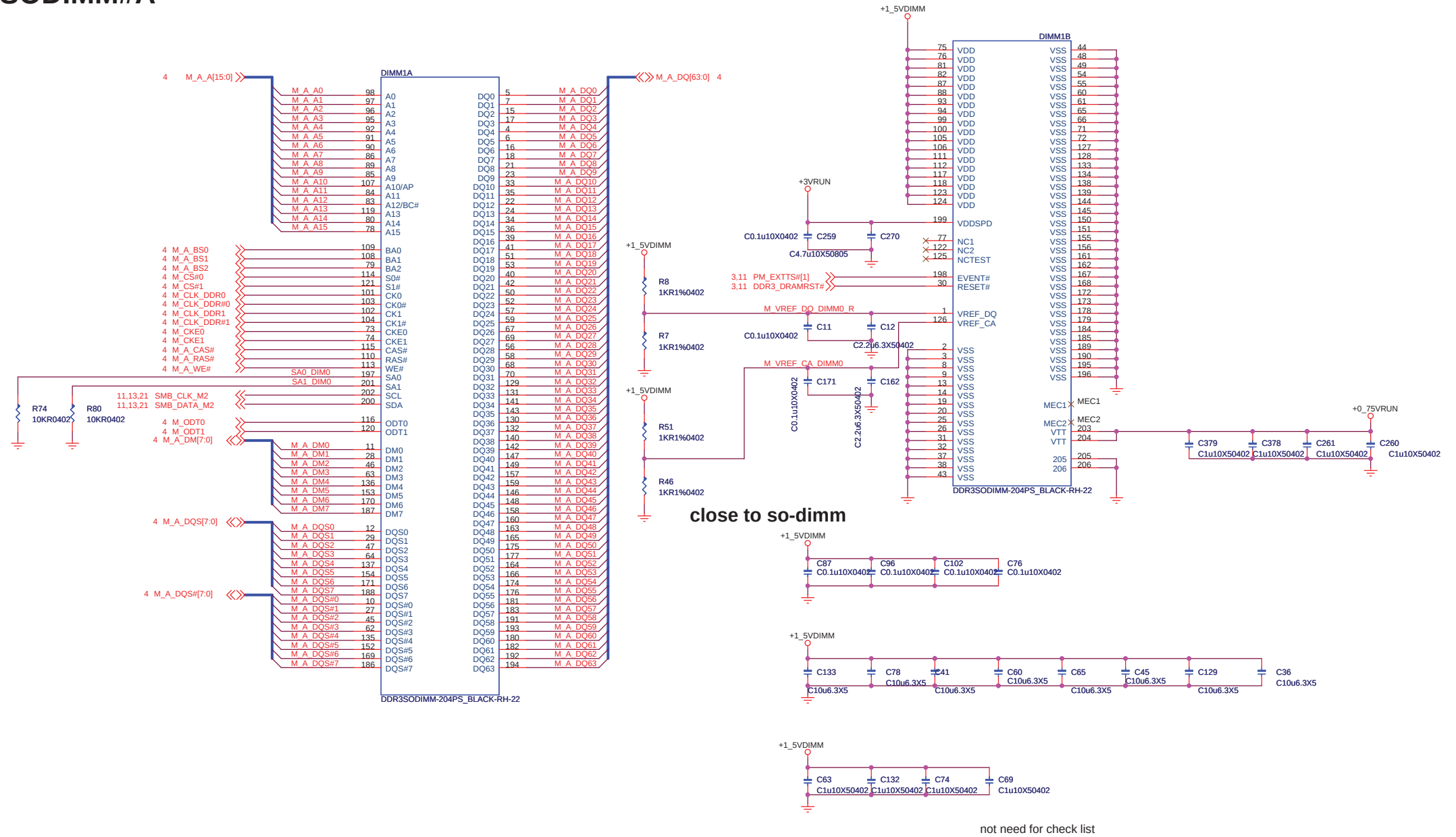
ARRANDALE BGA PROCESSOR (GND)



MICRO-STAR INT'L CO.,LTD.

Title	PROCESSOR-7 (GND)	
Size: A2	Document Number: MS-1251	Rev: 0D
Date: Friday, October 15, 2010	Sheet 9 of 39	

SODIMM#A



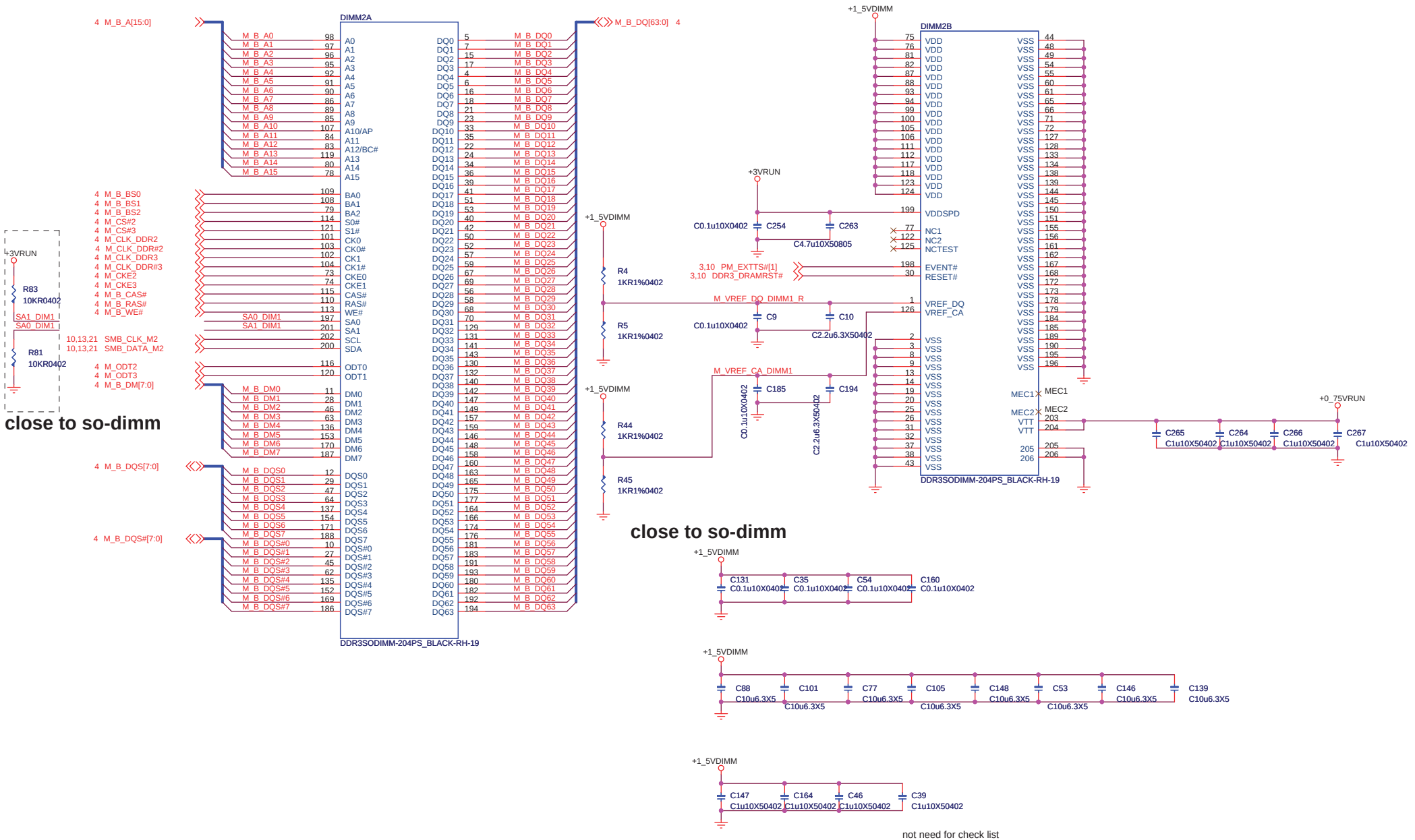
MICRO-STAR INT'L CO.,LTD.

Title: DDR3 SODIMM0

Size: A3 | Document Number: MS-1251 | Rev: 0D

Date: Friday, October 15, 2010 | Sheet 10 of 39

SODIMM#B



MICRO-STAR INT'L CO.,LTD.

Title: DDR3 SODIMM1

Size: A3 | Document Number: MS-1251 | Rev: 0D

Date: Friday, October 15, 2010 | Sheet 11 of 39

IBEXPEAK - M (HDA,JTAG,SATA)

Cap values depend on Xtal

Place near PCH, within 1000 mils

RTC Rechargeable battery

Enable Intel Anti-Theft Technology: Connect to Vcc3_3 with 8.2-k weak pull-up resistor.

NOTE: SATA Port 2,3 may not be available in all Ibex Peak SKUs.

It is good design practice to use root port (port 0) for the SATA ports used on the board so you can disable rest of the ports to get more power. Disabling each additional port could save upto 150mW

H.D.D

O.D.D

KAGUYA ONLY

SABER ONLY

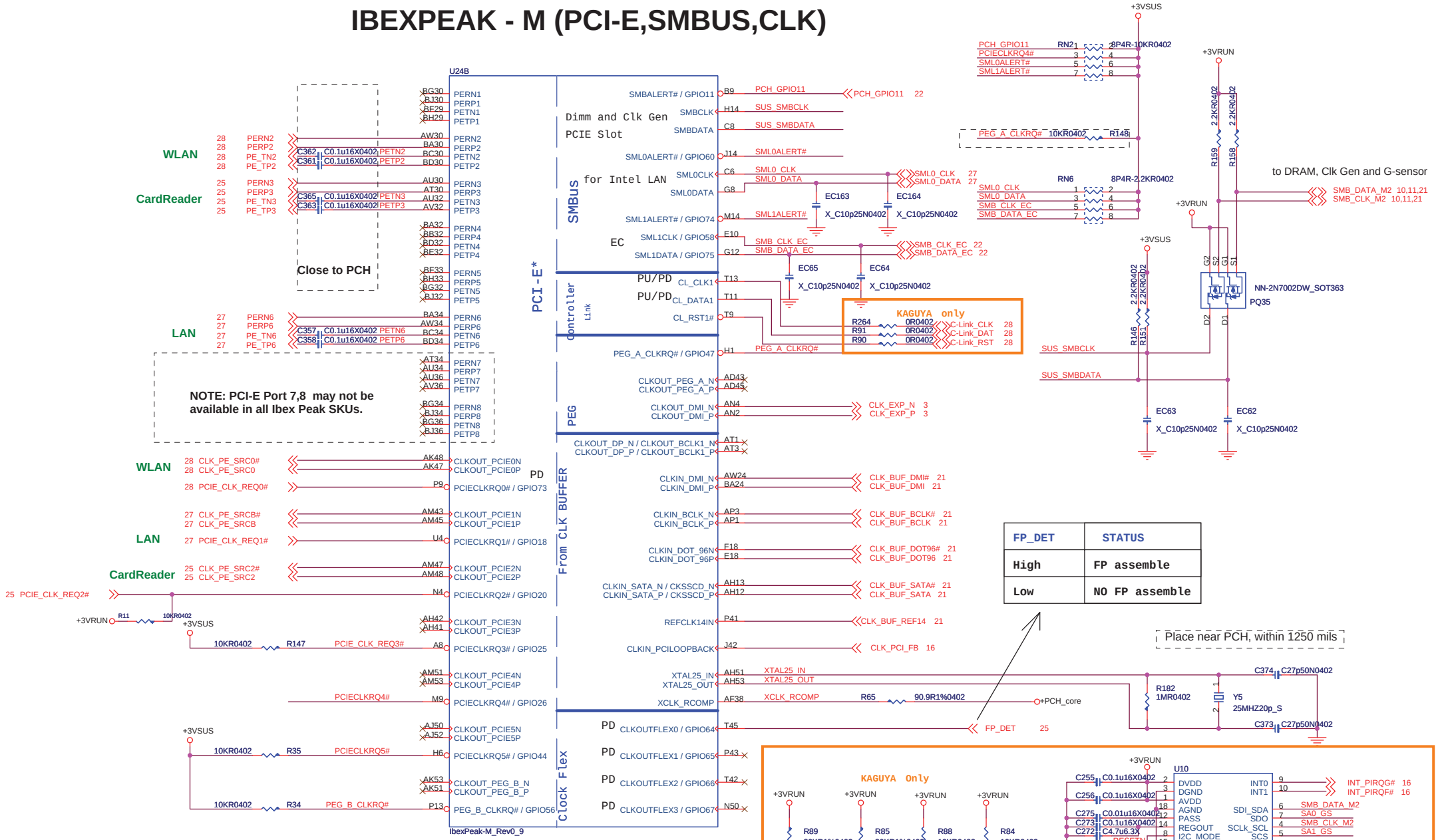
MICRO-STAR INT'L CO.,LTD.

Title: PCH-1 (HDA,JTAG,SATA)

Size: A3 | Document Number: MS-1251 | Rev: 0D

Date: Monday, October 18, 2010 | Sheet 12 of 39

IBEXPEAK - M (PCI-E,SMBUS,CLK)



FP_DET	STATUS
High	FP assemble
Low	NO FP assemble

PCIECLKRQ1# / GPIO18 PCIECLKRQ2# / GPIO20	RUN Well
PCIECLKRQ0# and PCIECLKRQ3# ~ PCIECLKRQ7# PEG_A_CLKRQ# PEG_B_CLKRQ#	SUS Well

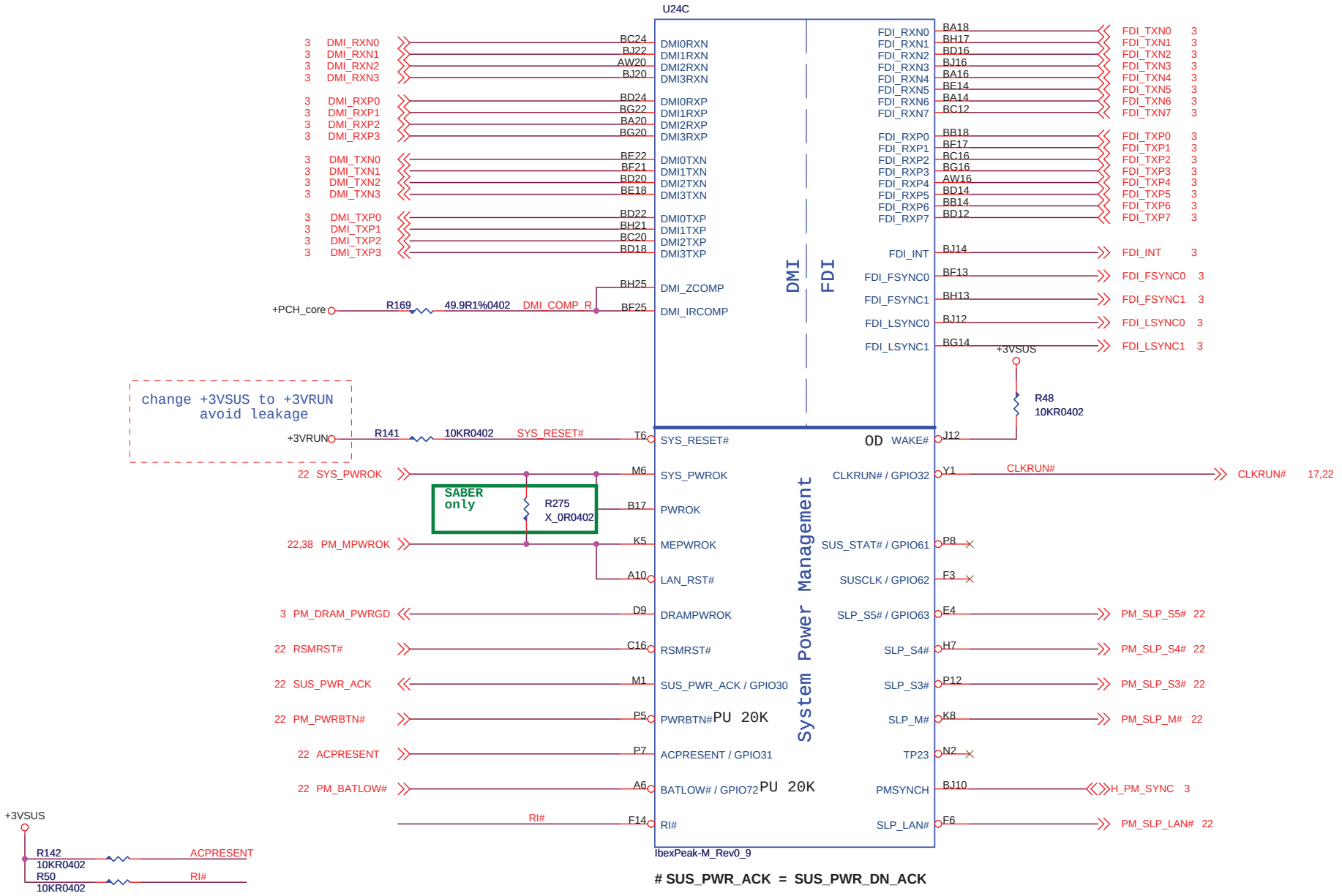
MICRO-STAR INT'L CO.,LTD.

Title: PCH-2 (PCI-E,SMBUS,CLK)

Size: A3 | Document Number: MS-1251 | Rev: 0D

Date: Friday, October 15, 2010 | Sheet 13 of 39

IBEXPEAK - M (DMI,FDI,GPIO)



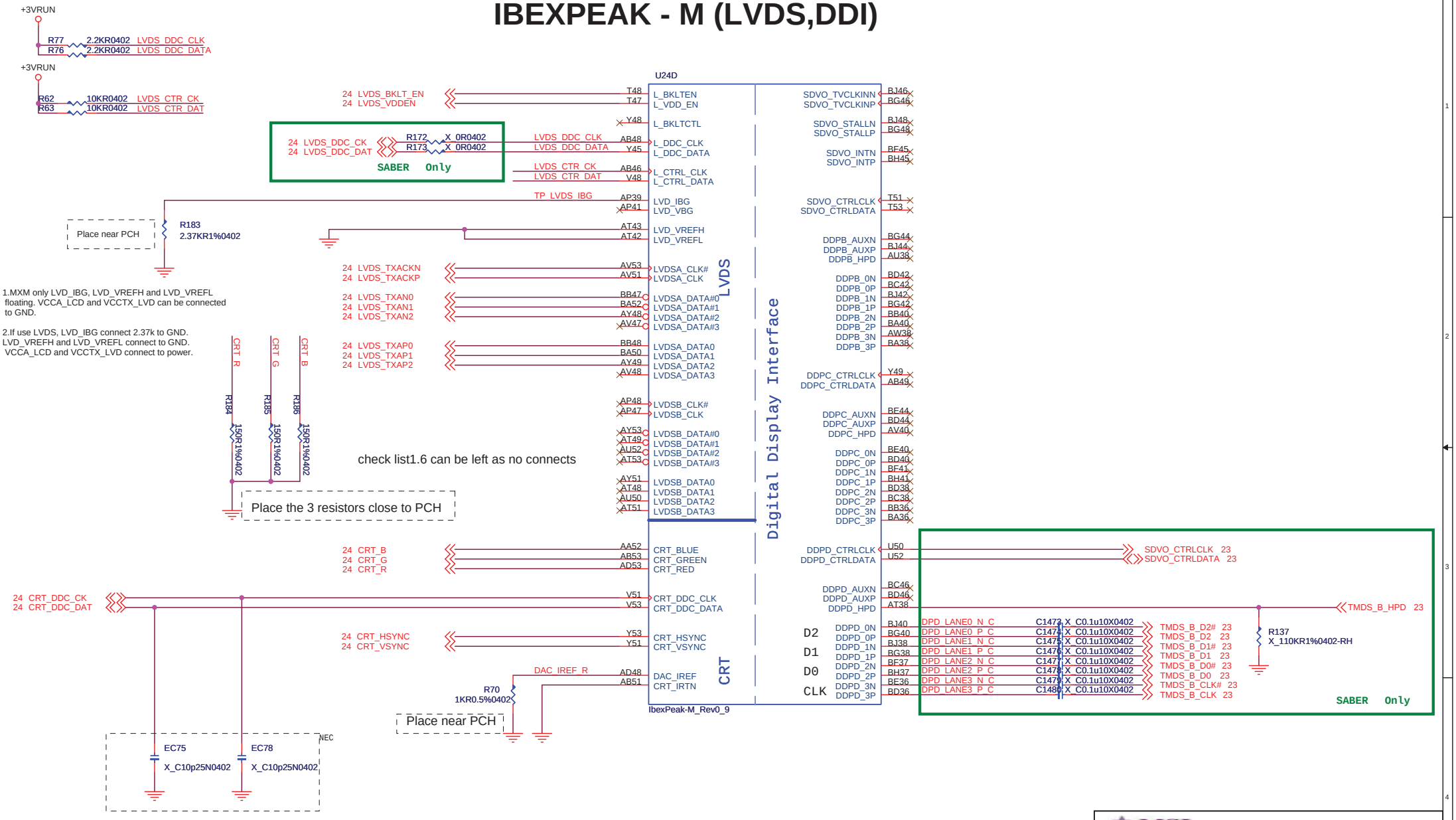
 # SUS_PWR_ACK = SUS_PWR_DN_ACK

Active High output signal asserted by the IntelR ME to the Embedded Controller, when it does not require the PCH Suspend well to be powered.

MICRO-STAR INT'L CO.,LTD.

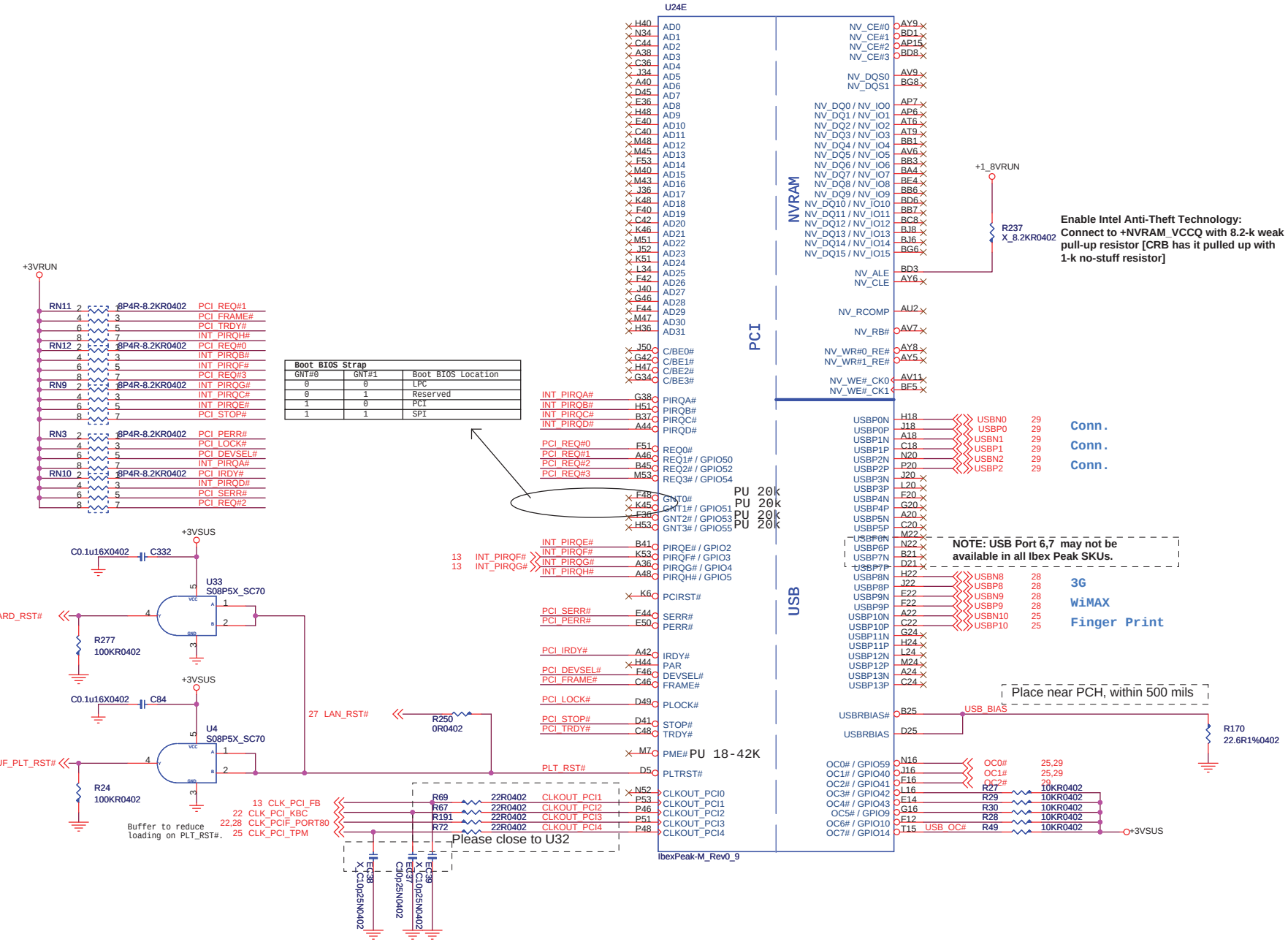
Title	PCH-3 (DMI,FDI,GPIO)	
Size: Custom	Document Number: MS-1251	Rev: 0D
Date: Friday, October 15, 2010	Sheet 14 of 39	

IBEXPEAK - M (LVDS,DDI)



MSI	MICRO-STAR INT'L CO.,LTD.	
Title	PCH-4 (LVDS,DDI)	
Size B	Document Number MS-1251	Rev 0D
Date: Friday, October 15, 2010	Sheet 15 of 39	

IBEXPEAK - M (PCI,USB,NVRAM)



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MICRO-STAR INT'L CO.,LTD.

Title: PCH-5 (PCI,USB,NVRAM)

Size: A3 | Document Number: MS-1251 | Rev: 0D

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IBEXPEAK - M (GPIO,VSS_NCTF,RSVD)

ODD_DET	STATUS
High	NO ODD assemble
Low	ODD assemble

GPIO15:
This signal is required to be pulled up in order to enable TLS. If this signal is pulled down or left floating IntelR RPAT and IntelR AMT with TLS will not be functional.

2

BIOS change code GPIO46 to GPIO24

U24F

IbexPeak-M_Rev0_9

KAGUYA			SABER		
MB_ID0	MB_ID1		MB_ID0	MB_ID1	
0	0	Normal model	0	0	Normal model
0	1	3G model	0	1	
1	0		1	0	
1	1		1	1	

NetName	ON	OFF
PW_CLEAR#	CLEAR PASSWORD	NORMAL
RTCVCC	CLEAR CMOS	NORMAL

NEC

Retain 25-MHz crystal footprint on your platform.
---Though FCIM will not be available, retaining the footprint will allow Intel and customer to test and evaluate FCIM for future platforms.
---25-MHz crystal and associated capacitor footprints only are requested – components do not need to be populated.
---Keep 1K Ohm resistor un-stuffed to GND on Ibex Peak GPIO8.

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MICRO-STAR INT'L CO.,LTD.

Title: PCH-6 (GPIO,VSS_NCTF,RSVD)

Size: A3 | Document Number: MS-1251 | Rev: 0D

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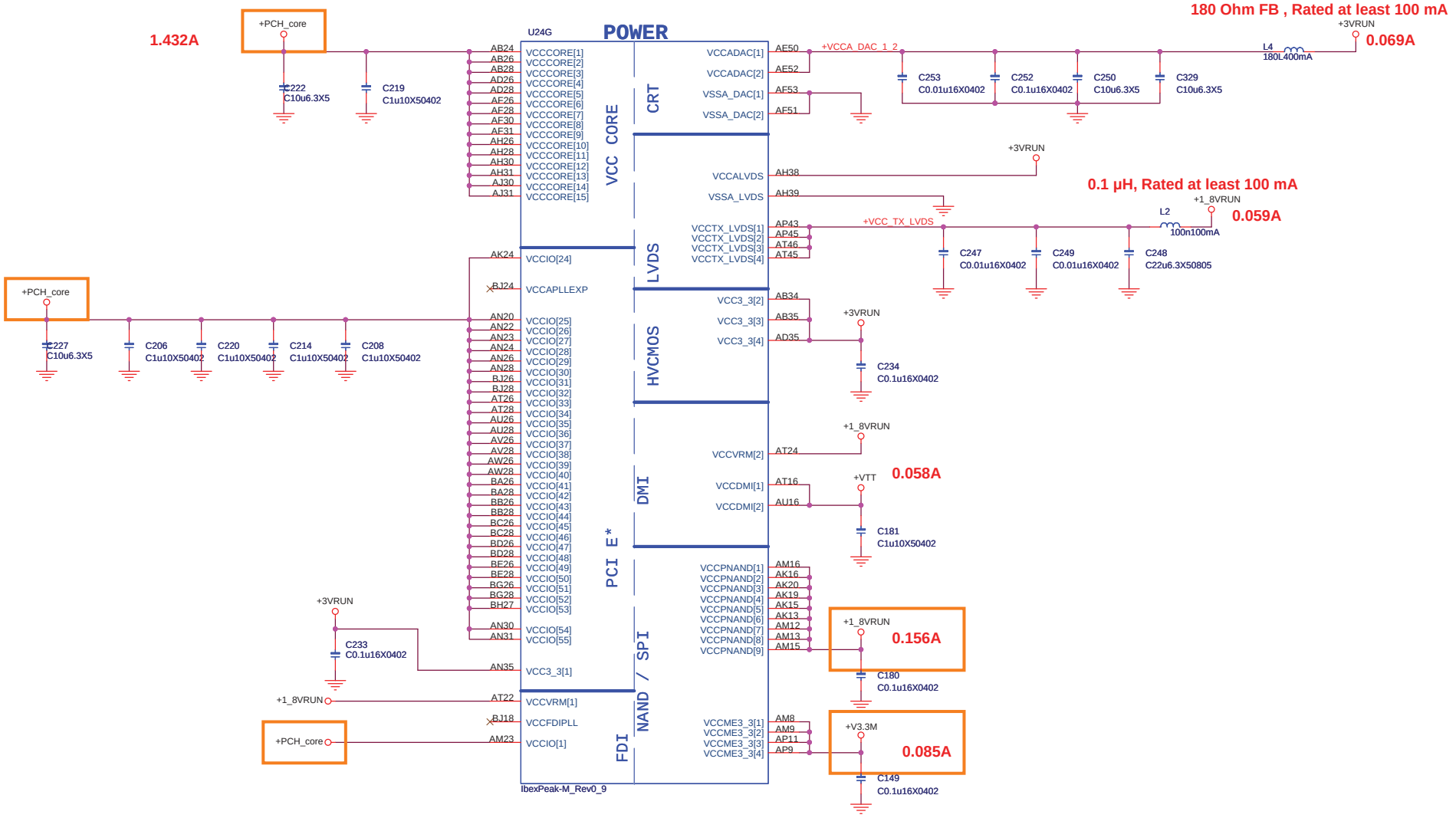
IBEXPEAK - M (POWER)



The VCCVRM rail (1.8 V/1.5 V) powers an internal voltage regulator module (VRM) that regulates clean 1.05-V voltage supply for analog rails (VCCACIk, VccapllEXP, VCCFDIPLL, and VCCSATAPLL). This solution will allow us to remove the LC filter requirements for those rails, thereby reducing platform BOM cost. VCCVRM is enabled by default via internal pull up to GPIO27, therefore GPIO27 should be left as No Connect. The following diagram shows implementation details on how to enable and disable VccVRM.

MICRO-STAR INT'L CO.,LTD.

Title: PCH-7 (POWER)

Size: A3 | Document Number: MS-1251 | Rev: 0D

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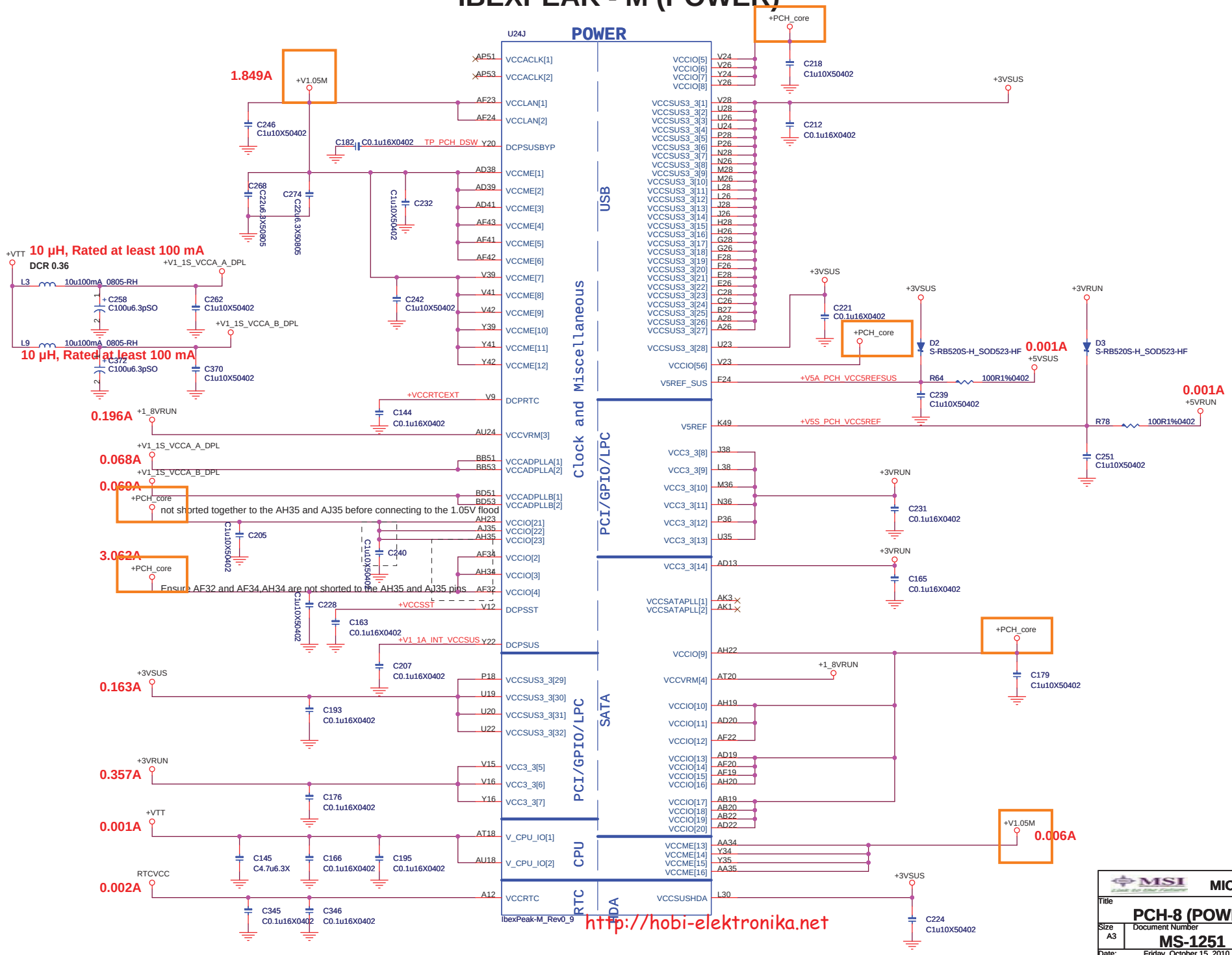
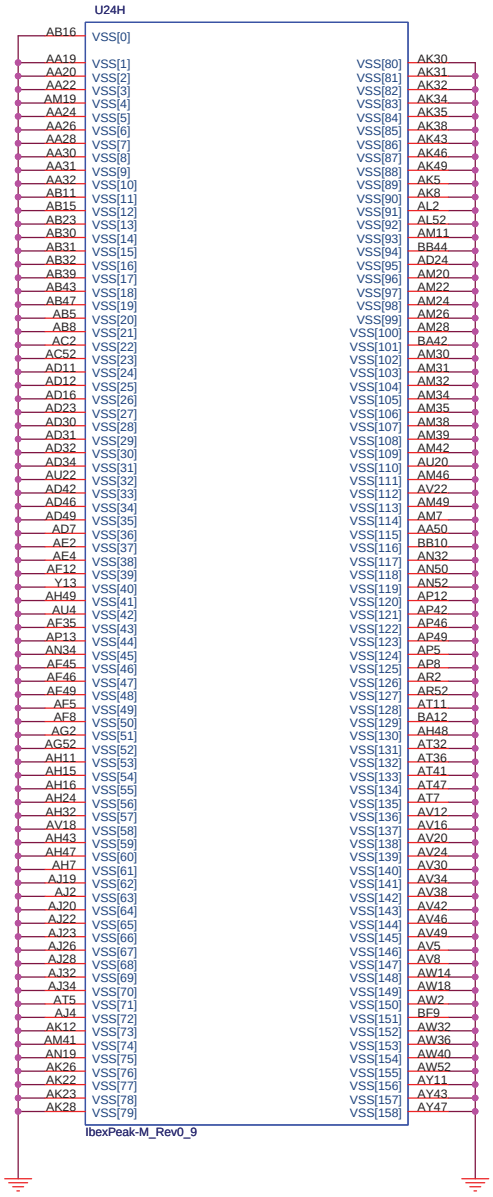
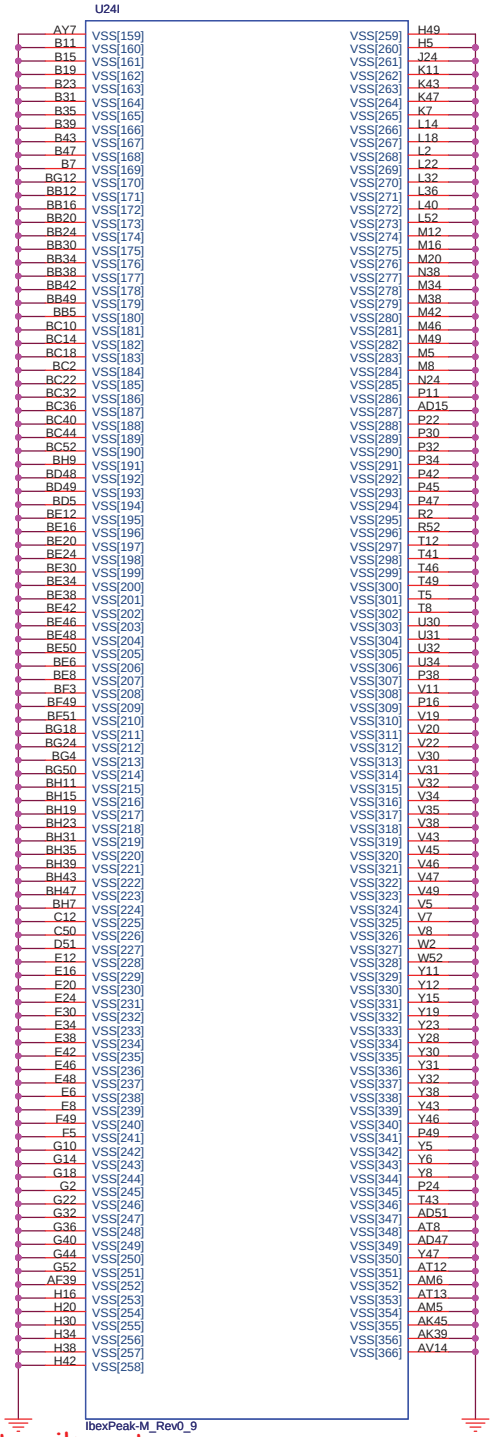
IBEXPEAK - M (POWER)



IBEXPEAK - M (GND)





MICRO-STAR INT'L CO.,LTD.

Title: PCH-9 (GND)

Size: A3 | Document Number: MS-1251 | Rev: 0D

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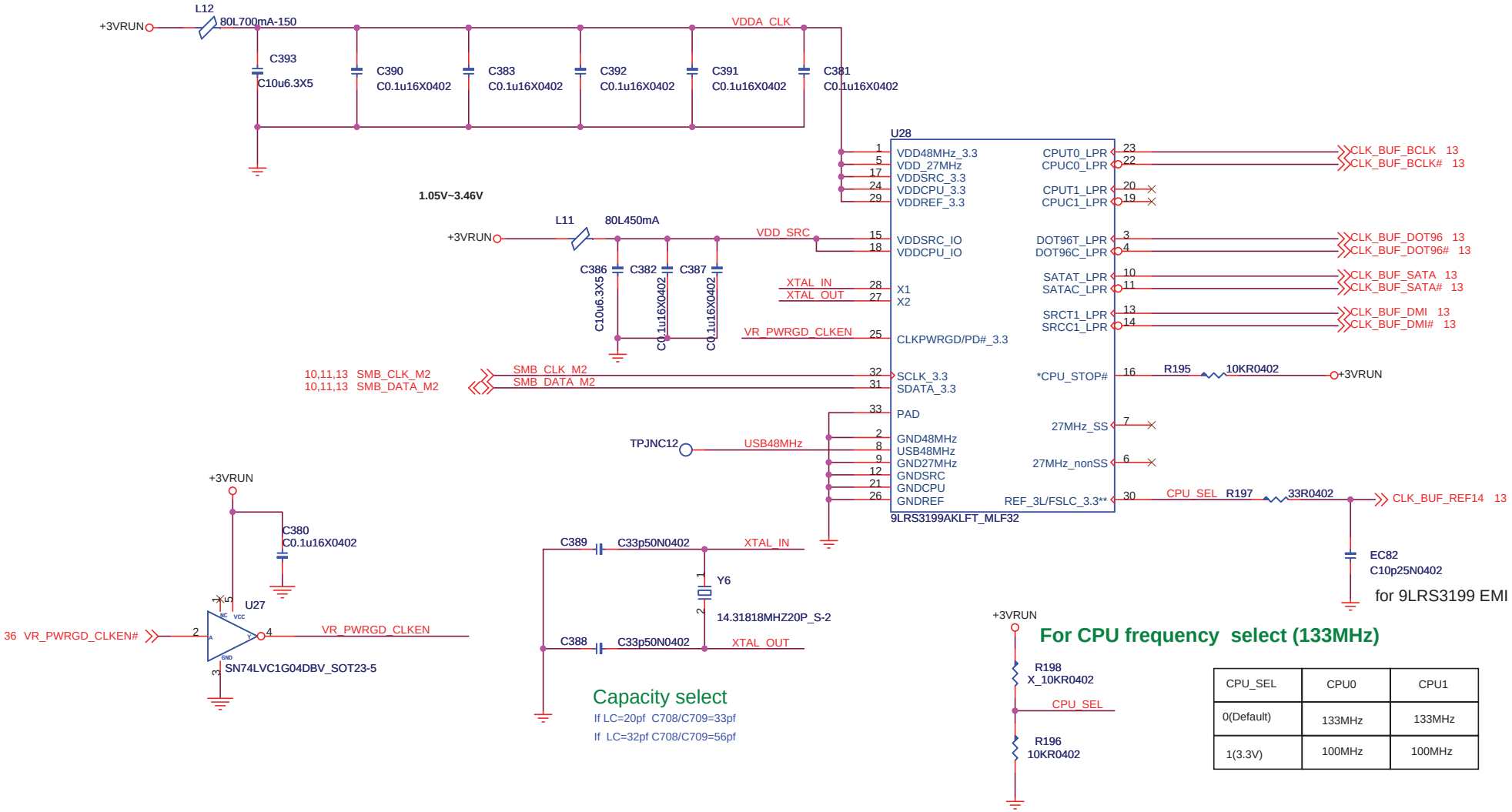

CPU_SEL	CPU0	CPU1
0(Default)	133MHz	133MHz
1(3.3V)	100MHz	100MHz

Table 1: CPU Frequency Select Table

FS_LC B0b7	CPU MHz	SRC MHz	REF MHz	USB MHz	DOT MHz
0 (Default)	133.33	100.00	14.318	48.00	96.00
1	100.00				

1. FS_LC is a low-threshold input.Please see V_{IL_FS} and V_{IH_FS} specifications in the Input/Supply/Common Output Parameters Table for correct values.

MICRO-STAR INT'L CO.,LTD.

Title: Clock Generator(9LRS3199)

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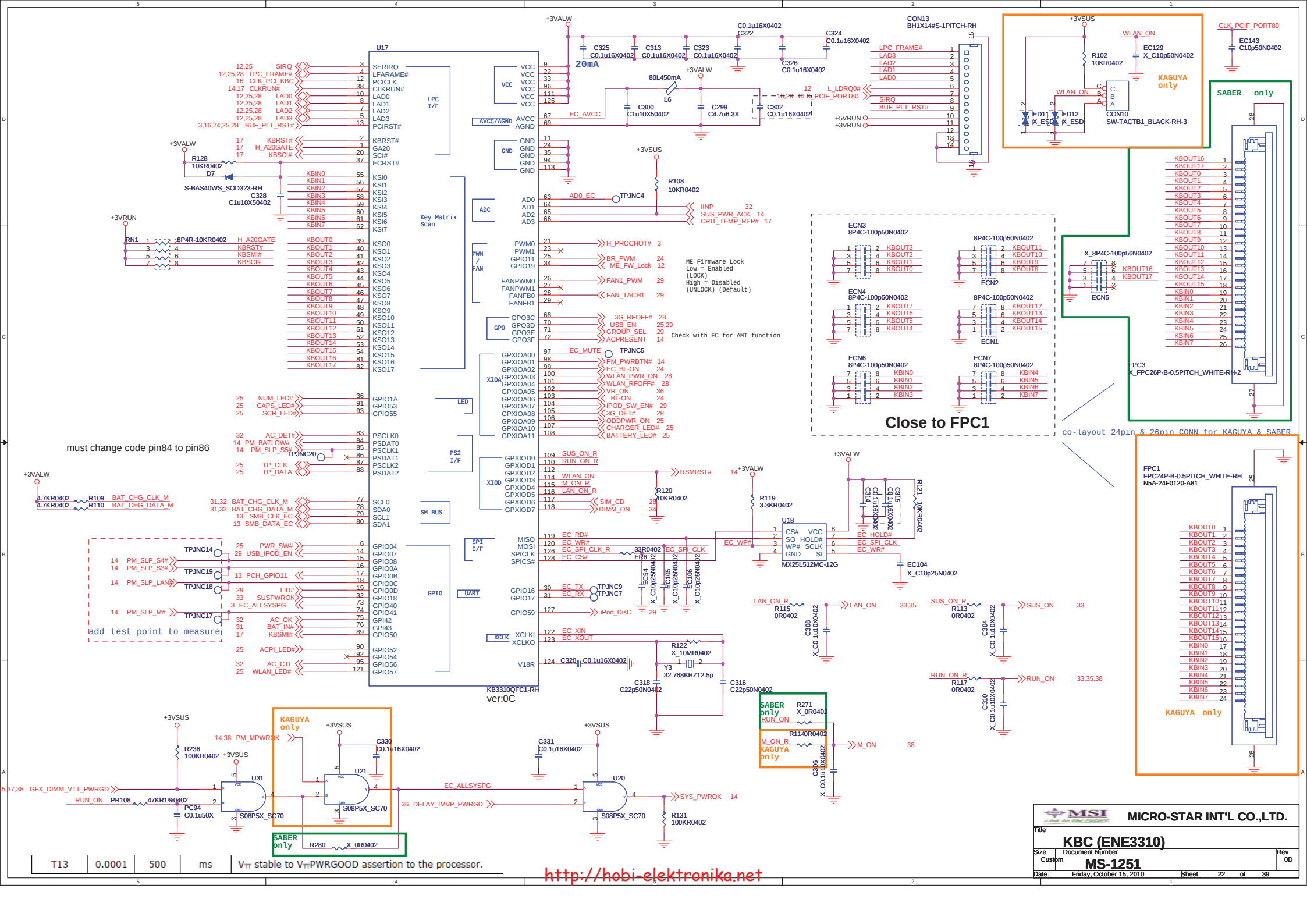
U17
KB3310QFC1-RH
ver:0C
must change code pin84 to pin86
add test point to measure
Close to FPC1
co-layout 24pin & 26pin CONN for KAGUYA & SABER
KAGUYA only
SABER only
20mA
80L450mA
ME Firmware Lock
Low = Enabled
(LOCK)
High = Disabled
(UNLOCK) (Default)
Check with EC for AMT function
MX25L512MC-12G
MICRO-STAR INT'L CO.,LTD.
KBC (ENE3310)
MS-1251
Friday, October 15, 2010
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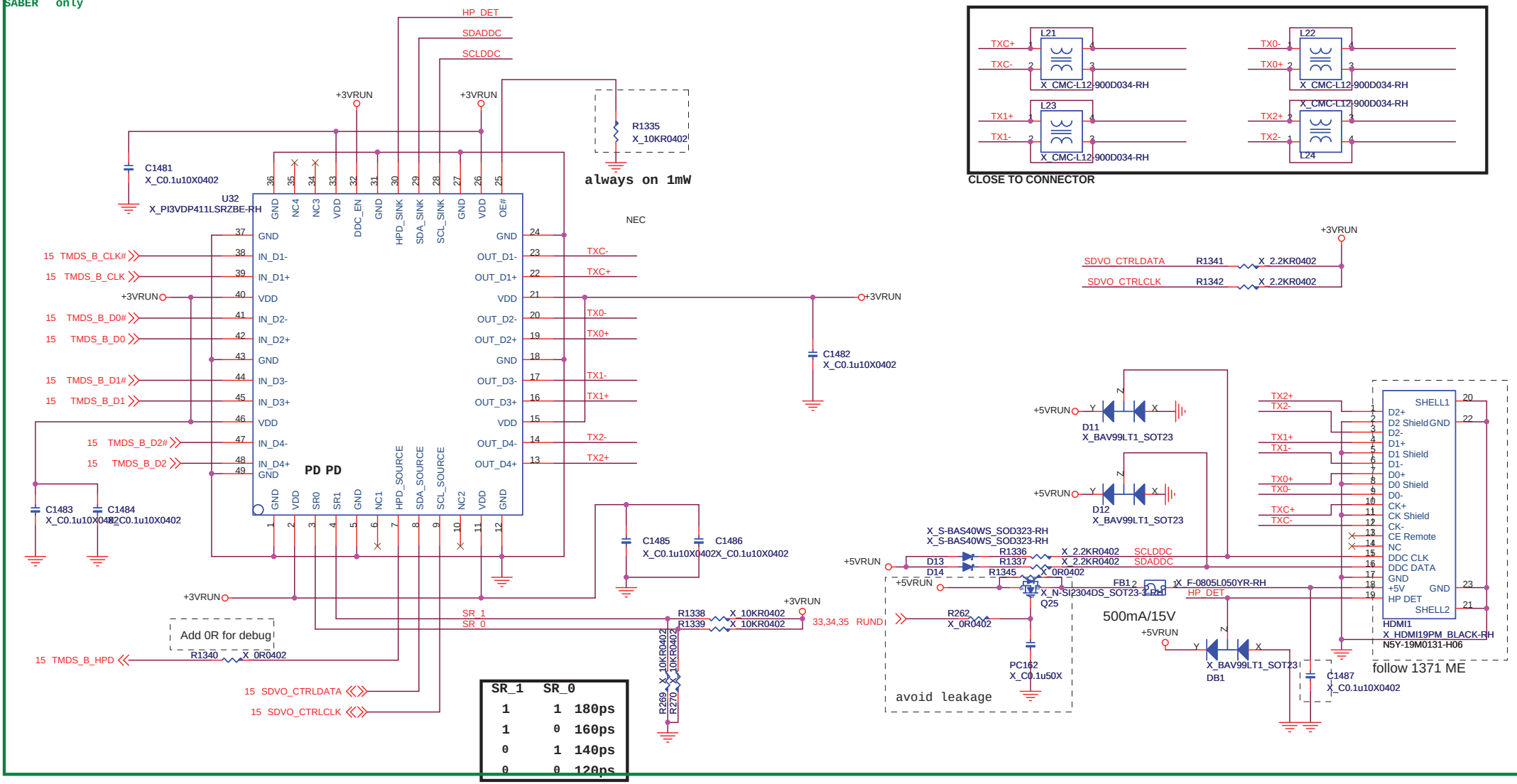
HDMI Level shift for SABER

HP_DET
PLUGGED 5V
UNPLUGGED 0V

SABER only



SR_1	SR_0	
1	1	180ps
1	0	160ps
0	1	140ps
0	0	120ps

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Title: HDMI Level shift

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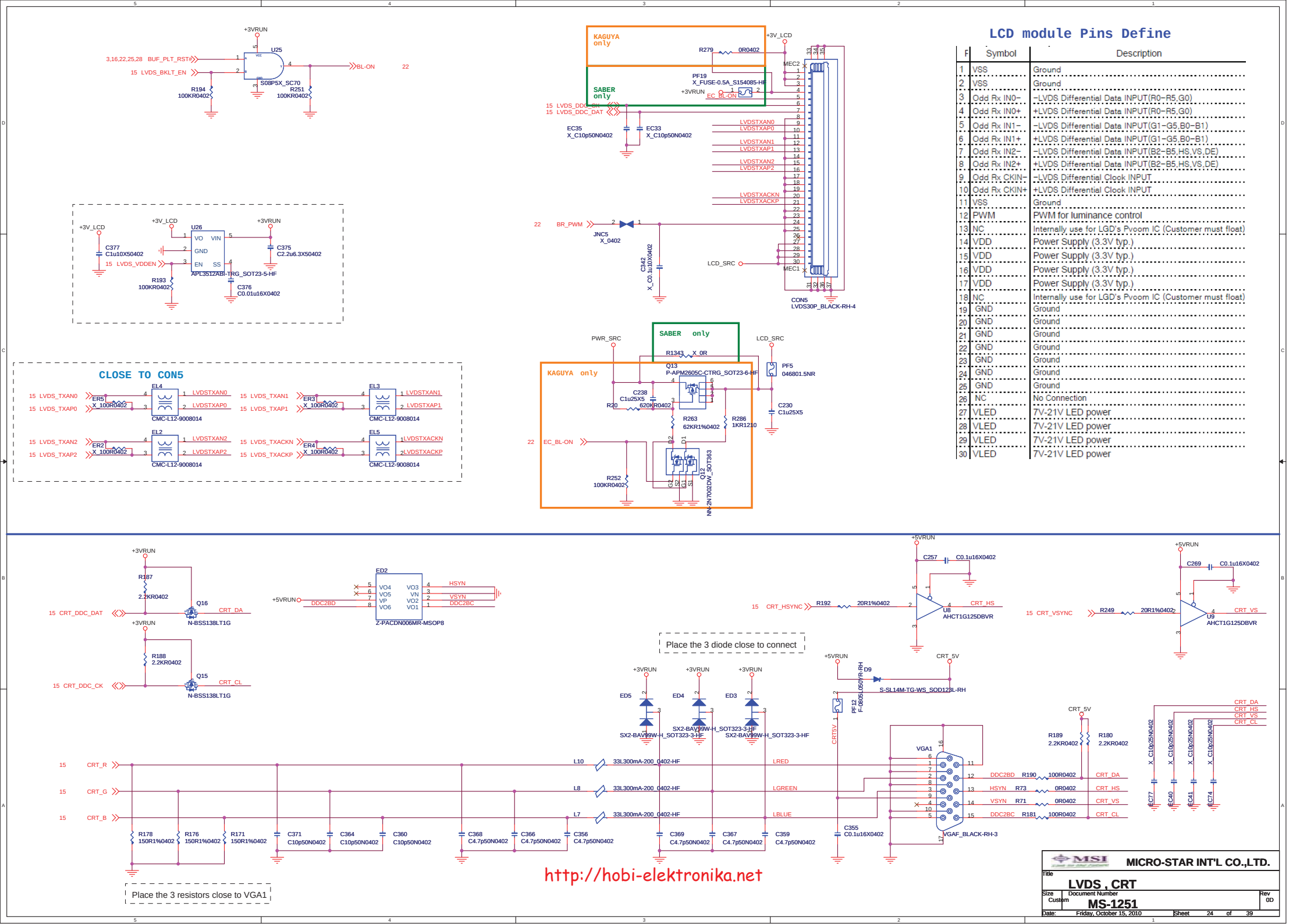
LCD module Pins Define
F | Symbol | Description
1 | VSS | Ground
2 | VSS | Ground
3 | Odd Rx IN0− | −LVDS Differential Data INPUT(R0−R5,G0)
4 | Odd Rx IN0+ | +LVDS Differential Data INPUT(R0−R5,G0)
5 | Odd Rx IN1− | −LVDS Differential Data INPUT(G1−G5,B0−B1)
6 | Odd Rx IN1+ | +LVDS Differential Data INPUT(G1−G5,B0−B1)
7 | Odd Rx IN2− | −LVDS Differential Data INPUT(B2−B5,HS,VS,DE)
8 | Odd Rx IN2+ | +LVDS Differential Data INPUT(B2−B5,HS,VS,DE)
9 | Odd Rx CKIN− | −LVDS Differential Clock INPUT
10 | Odd Rx CKIN+ | +LVDS Differential Clock INPUT
11 | VSS | Ground
12 | PWM | PWM for luminance control
13 | NC | Internally use for LGD's Pvoom IC (Customer must float)
14 | VDD | Power Supply (3.3V typ.)
15 | VDD | Power Supply (3.3V typ.)
16 | VDD | Power Supply (3.3V typ.)
17 | VDD | Power Supply (3.3V typ.)
18 | NC | Internally use for LGD's Pvoom IC (Customer must float)
19 | GND | Ground
20 | GND | Ground
21 | GND | Ground
22 | GND | Ground
23 | GND | Ground
24 | GND | Ground
25 | GND | Ground
26 | NC | No Connection
27 | VLED | 7V-21V LED power
28 | VLED | 7V-21V LED power
29 | VLED | 7V-21V LED power
30 | VLED | 7V-21V LED power
KAGUYA only
SABER only
CLOSE TO CON5
Place the 3 diode close to connect
Place the 3 resistors close to VGA1
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LVDS , CRT
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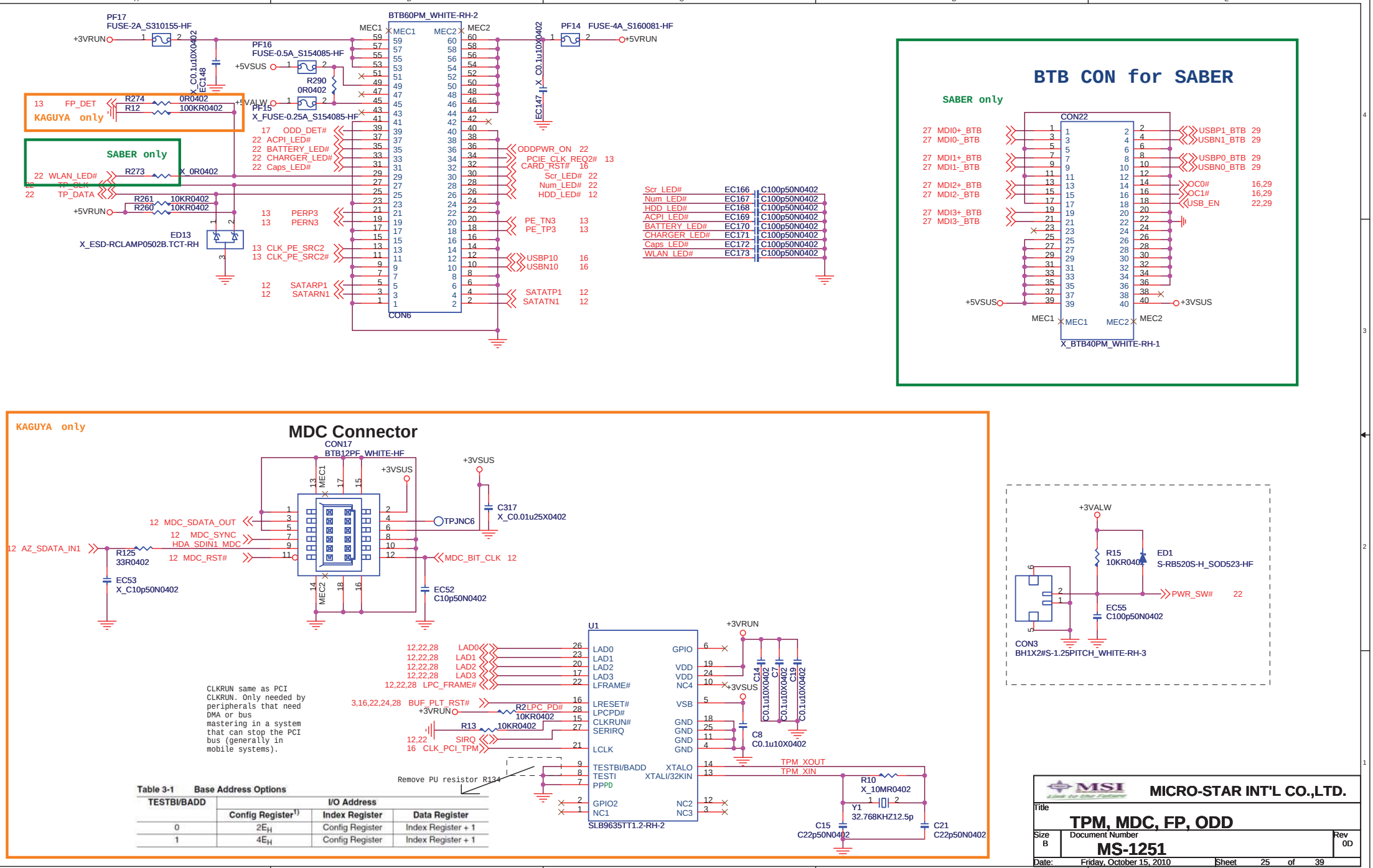
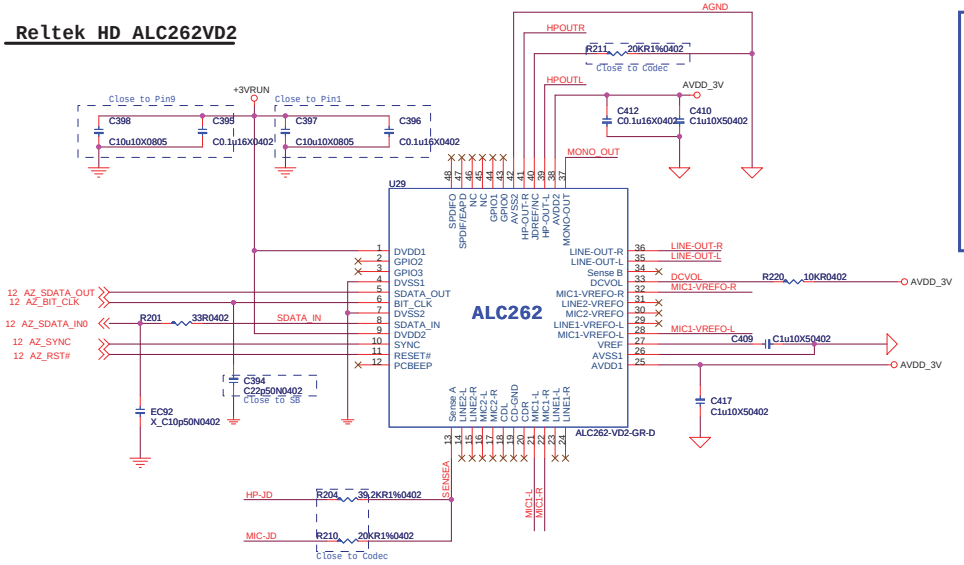
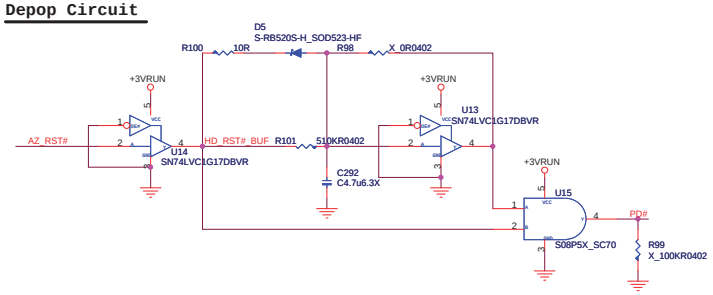


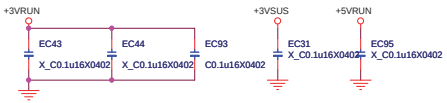
Reltek HD ALC262VD2

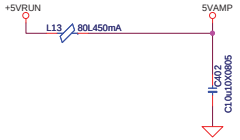


Depop Circuit

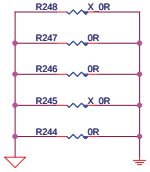


AUDIO CODE REGULATORS

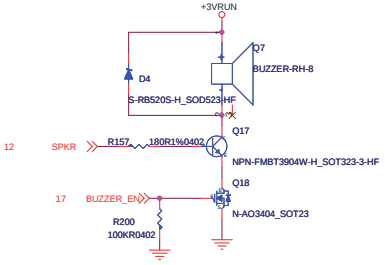


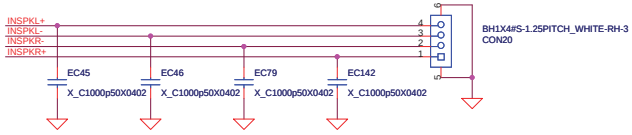


For EMI reserve

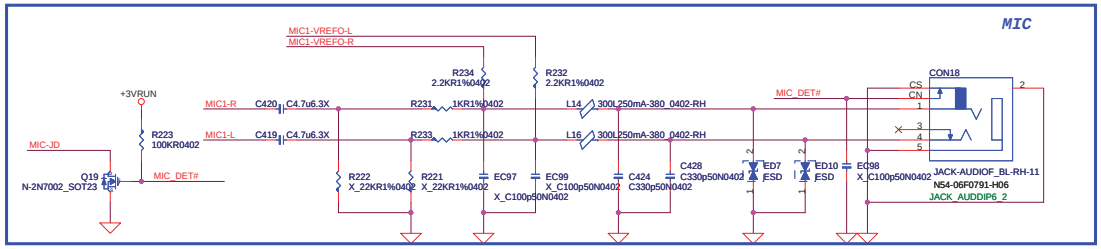


Buzzer

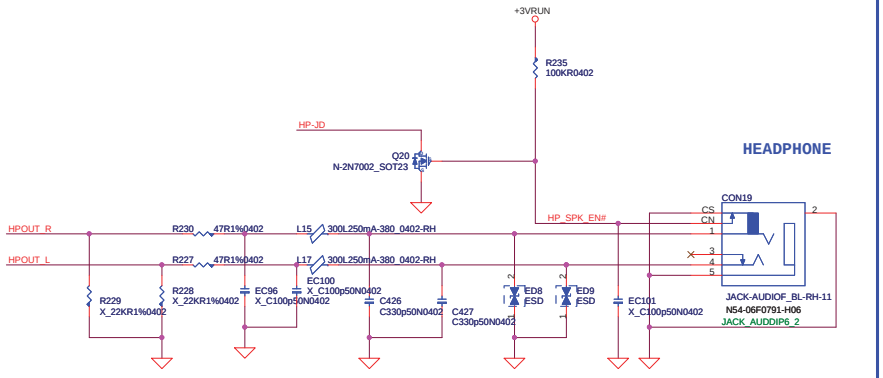




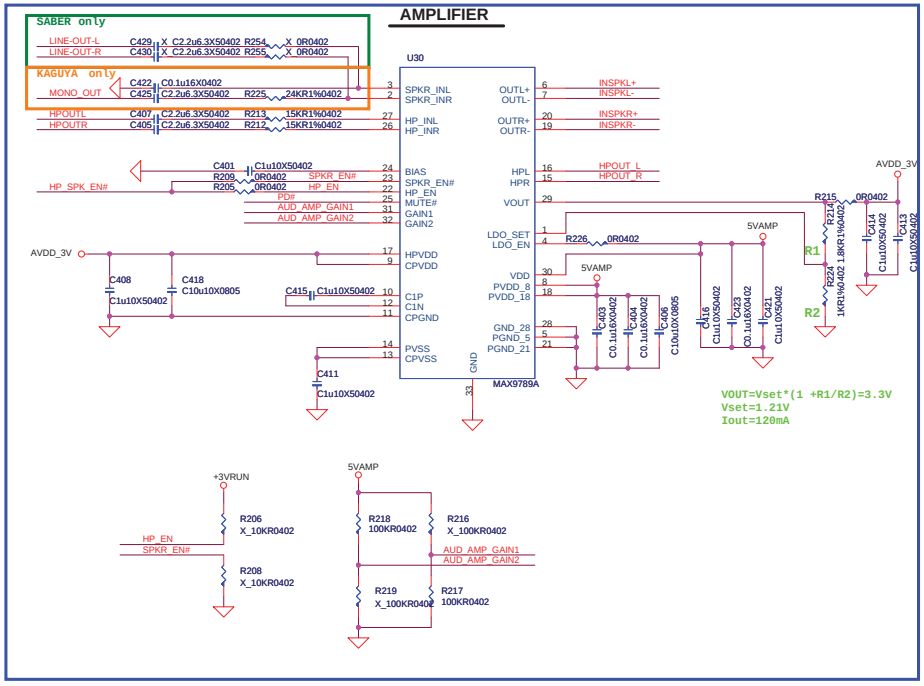
MIC



HEADPHONE



AMPLIFIER



MICRO-STAR INT'L CO.,LTD.

Title: Audio (ALC262) & Jacks

Size: C | Document Number: MS-1251 | Rev: 0D

Date: Friday, October 15, 2010 | Sheet 26 of 39

SEL	Function
L	A_X to $_XB_1$; LED_Z to $_ZLED_1$
H	A_X to $_XB_2$; LED_Z to $_ZLED_2$

KAGUYA ONLY
U906
PHY
82577LM-HF

SABER ONLY
U907
PHY
82577LC-HF

add

U22
TS3L500AERHUR_TQFN56-RH

KAGUYA only
R179 10KR0402

SABER only
R253 X_0R0402

SABER connect to BTB

VDDO power decoupling
+V3.3M
C303 C10u6.3X5
C305 C0.1u16X0402

U16
82577LM-HF

+3VRUN
R111 10KR0402

PCIE
MDI
SMBUS
LED
JTAG

17 PM_LANPHY_ENABLE
change +3VSUS to +V3.3M
R103 10KR0402
R105 X 10KR0402

Y2 25MHZ20p_S
C294 C10p50N0402
C293 C33p50N0402
C296 C33p50N0402

R118 1KR0402
R107 3.01KR1%0402

Default solution:
Shared with PCH VTT SVR

VDD1P0 ==>1.0 V dc supply.
Note: Can also be connected to the PCH 1.1 V dc Switching Voltage Regulator (SVR).

C312 C10u6.3X5
C295 C0.1u16X0402

KAGUYA only

LAN Connector
LAN MAGNETICS

T1
NA0069RLF-RH

CON14
LAN-RJ45-RH-22

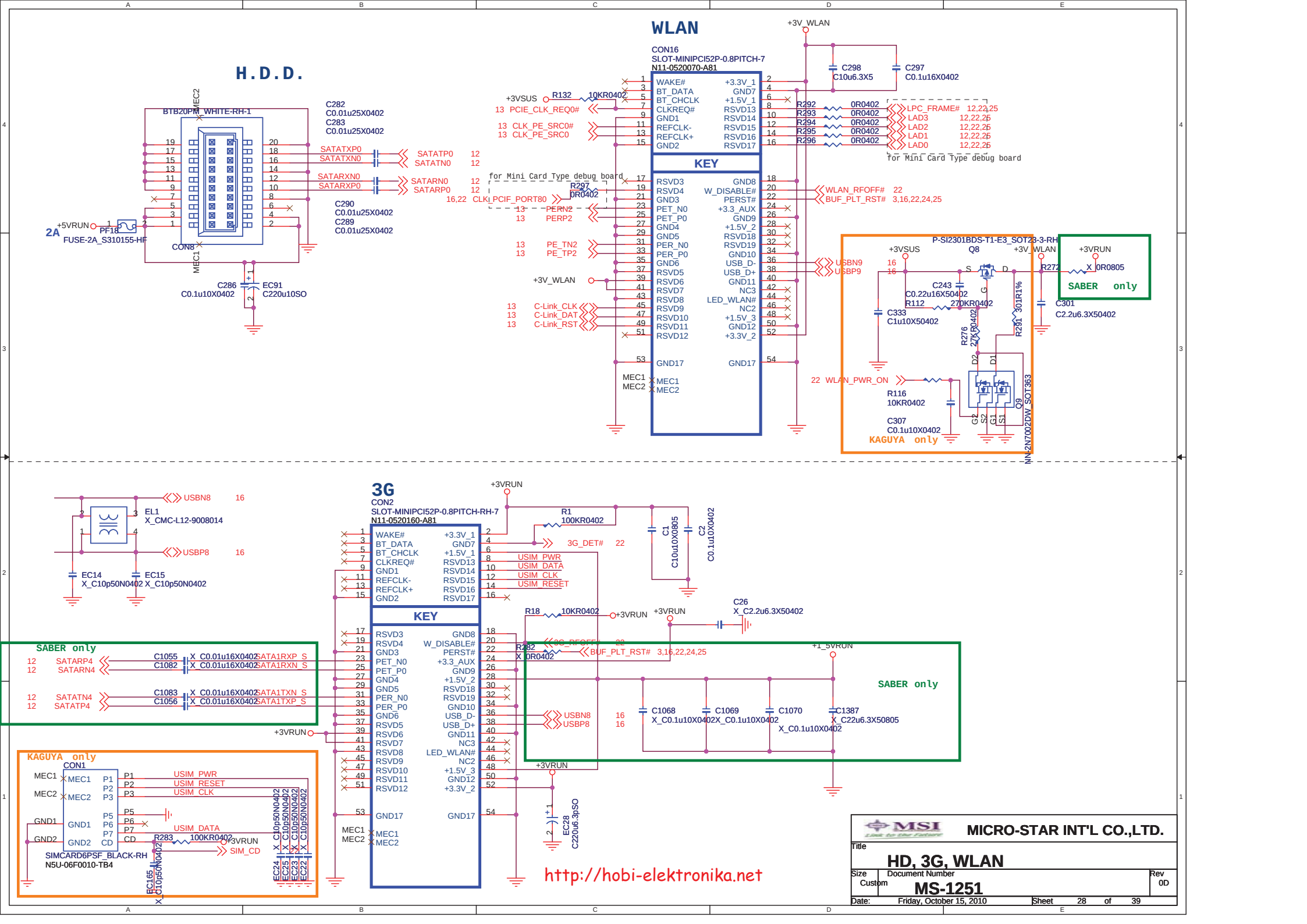
ER15 0R
ER16 0R
EC18 C0.1u16X0402
EC20 C0.1u16X0402
LAN_GND

As close As possable to T1
change
75R0402
EC48 C1000p2KX1206

http://hobi-elektronika.net

MSI MICRO-STAR INT'L CO.,LTD.

Title: LAN (Intel 82577LM)
Size: Custom
Document Number: MS-1251
Rev: 0D
Date: Friday, October 15, 2010
Sheet 27 of 39


H.D.D.
BTB20PM_WHITE-RH-1
CON8
MEC1
MEC2
C282
C0.01u25X0402
C283
C0.01u25X0402
C290
C0.01u25X0402
C289
C0.01u25X0402
SATATXP0
SATATXN0
SATARXN0
SATARXP0
SATATP0
SATATN0
SATARN0
SATARP0
+5VRUN
2A
PF18
FUSE-2A_S310155-HF
C286
C0.1u10X0402
EC91
C220u10SO
WLAN
CON16
SLOT-MINIPCI52P-0.8PITCH-7
N11-0520070-A81
KEY
+3V_WLAN
C298
C10u6.3X5
C297
C0.1u16X0402
+3VSUS
R132
10KR0402
PCIE_CLK_REQ0#
CLK_PE_SRC0#
CLK_PE_SRC0
R292
R293
R294
R295
R296
0R0402
LPC_FRAME#
LAD3
LAD2
LAD1
LAD0
12,22,25
for Mini Card Type debug board
R297
0R0402
CLKI_PCIF_PORT80
PERN2
PERP2
PE_TN2
PE_TP2
C-Link_CLK
C-Link_DAT
C-Link_RST
WLAN_RFOFF#
BUF_PLT_RST#
3,16,22,24,25
USBN9
USBP9
P-SI2301BDS-T1-E3_SOT23-3-RH
Q8
C243
C0.22u16X50402
R112
270KR0402
C333
C1u10X50402
R276
27KR0402
R291
301R1%
R272
X_0R0805
SABER only
C301
C2.2u6.3X50402
NN-2N7002DW_SOT363
Q9
WLAN_PWR_ON
R116
10KR0402
C307
C0.1u10X0402
KAGUYA only
3G
CON2
SLOT-MINIPCI52P-0.8PITCH-RH-7
N11-0520160-A81
+3VRUN
R1
100KR0402
3G_DET#
C1
C10u10X0805
C2
C0.1u10X0402
USIM_PWR
USIM_DATA
USIM_CLK
USIM_RESET
R18
10KR0402
C26
X_C2.2u6.3X50402
R232
X_0R0402
3G_RFOFF#
+1_5VRUN
C1068
X_C0.1u10X0402
C1069
X_C0.1u10X0402
C1070
X_C0.1u10X0402
C1387
X_C22u6.3X50805
USBN8
USBP8
EL1
X_CMC-L12-9008014
EC14
X_C10p50N0402
EC15
X_C10p50N0402
SATARP4
SATARN4
SATATN4
SATATP4
C1055
C1082
C1083
C1056
X_C0.01u16X0402
SATA1RXP_S
SATA1RXN_S
SATA1TXN_S
SATA1TXP_S
CON1
SIMCARD6PSF_BLACK-RH
N5U-06F0010-TB4
R283
100KR0402
SIM_CD
EC165
EC24
EC25
EC23
EC22
EC28
C220u6.3pSO
http://hobi-elektronika.net
MICRO-STAR INT'L CO.,LTD.
Title
HD, 3G, WLAN
Size
Custom
Document Number
MS-1251
Rev
0D
Date:
Friday, October 15, 2010
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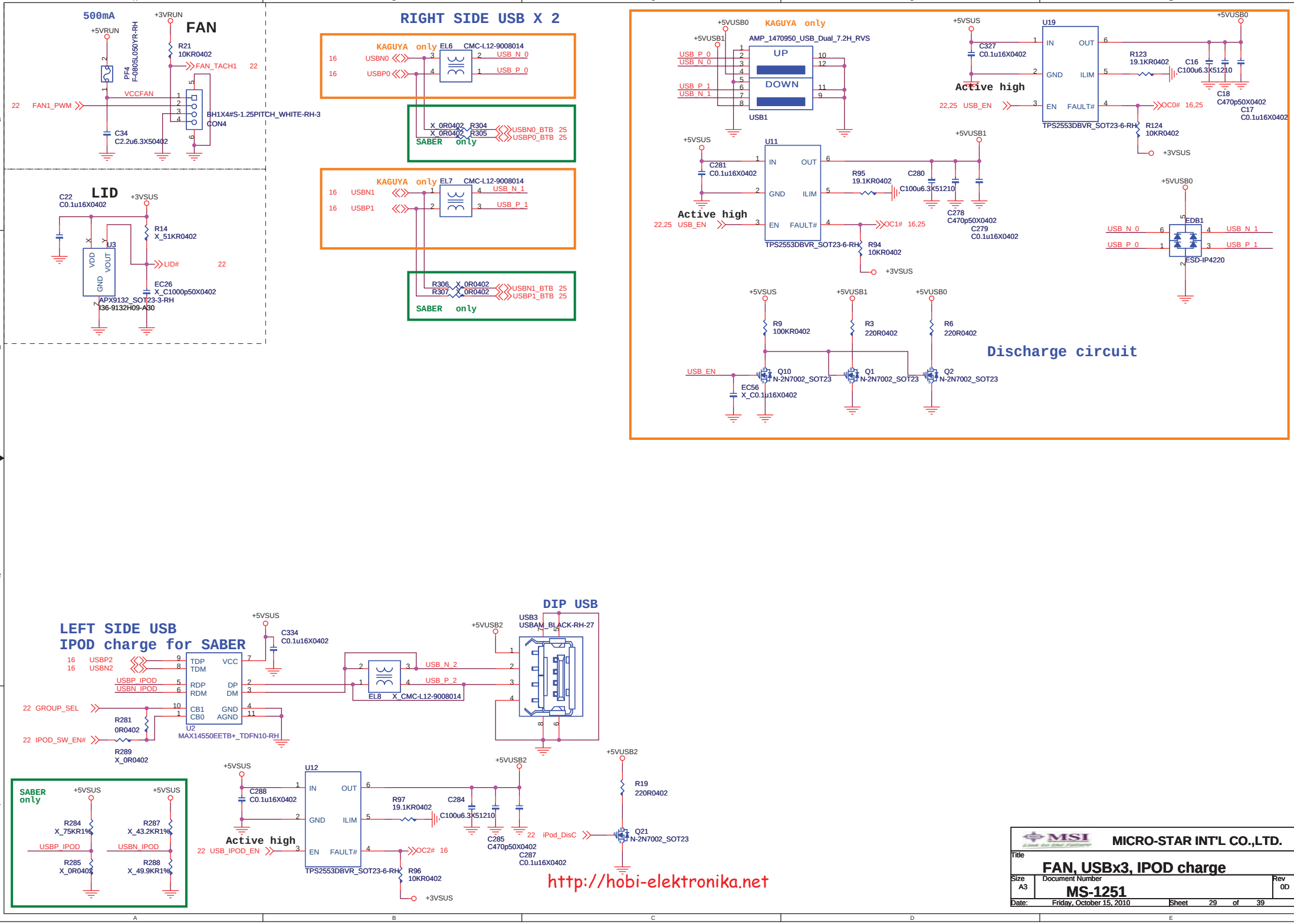
28
of
39


500mA
FAN
+5VRUN
+3VRUN
R21
10KR0402
FAN_TACH1
22
VCCFAN
22 FAN1_PWM
PF4
F0805L050YR-RH
BH1X4#S-1.25PITCH_WHITE-RH-3
CON4
C34
C2.2u6.3X50402
LID
C22
C0.1u16X0402
+3VSUS
R14
X_51KR0402
U3
VDD
VOUT
GND
LID#
EC26
X_C1000p50X0402
APX9132_SOT23-3-RH
136-9132H09-A30
RIGHT SIDE USB X 2
KAGUYA only
EL6
CMC-L12-9008014
16 USBN0
16 USBP0
USB_N_0
USB_P_0
X_0R0402 R304
X_0R0402 R305
USBN0_BTB 25
USBP0_BTB 25
SABER only
EL7
CMC-L12-9008014
16 USBN1
16 USBP1
USB_N_1
USB_P_1
R306 X_0R0402
R307 0R0402
USBN1_BTB 25
USBP1_BTB 25
SABER only
+5VUSB0
KAGUYA only
+5VUSB1
AMP_1470950_USB_Dual_7.2H_RVS
UP
DOWN
USB1
USB_P_0
USB_N_0
USB_P_1
USB_N_1
+5VSUS
C327
C0.1u16X0402
U19
IN
OUT
GND
ILIM
EN
FAULT#
TPS2553DBVR_SOT23-6-RH
Active high
22,25 USB_EN
OC0# 16,25
R123
19.1KR0402
C16
C100u6.3X51210
C18
C470p50X0402
C17
C0.1u16X0402
R124
10KR0402
+3VSUS
U11
C281
C0.1u16X0402
R95
19.1KR0402
C280
C100u6.3X51210
C278
C470p50X0402
C279
C0.1u16X0402
Active high
22,25 USB_EN
OC1# 16,25
R94
10KR0402
+3VSUS
EDB1
USB_N_0
USB_P_0
USB_N_1
USB_P_1
ESD-IP4220
R9
100KR0402
R3
220R0402
R6
220R0402
USB_EN
Q10
N-2N7002_SOT23
Q1
N-2N7002_SOT23
Q2
N-2N7002_SOT23
EC56
X_C0.1u16X0402
Discharge circuit
LEFT SIDE USB
IPOD charge for SABER
DIP USB
+5VSUS
C334
C0.1u16X0402
16 USBP2
16 USBN2
USBP_IPOD
USBN_IPOD
TDP
TDM
RDP
RDM
CB1
CB0
VCC
DP
DM
GND
AGND
U2
MAX14550EETB+_TDFN10-RH
22 GROUP_SEL
22 IPOD_SW_EN#
R281
0R0402
R289
X_0R0402
EL8
X_CMC-L12-9008014
USB_N_2
USB_P_2
+5VUSB2
USB3
USBAM_BLACK-RH-27
SABER only
+5VSUS
+5VSUS
R284
X_75KR1%
R287
X_43.2KR1%
USBP_IPOD
USBN_IPOD
R285
X_0R0402
R288
X_49.9KR1%
+5VSUS
C288
C0.1u16X0402
U12
IN
OUT
GND
ILIM
EN
FAULT#
TPS2553DBVR_SOT23-6-RH
Active high
22 USB_IPOD_EN
OC2# 16
R97
19.1KR0402
C284
C100u6.3X51210
C285
C470p50X0402
C287
C0.1u16X0402
R96
10KR0402
+3VSUS
+5VUSB2
R19
220R0402
22 iPod_DisC
Q21
N-2N7002_SOT23
http://hobi-elektronika.net
MSI
MICRO-STAR INT'L CO.,LTD.
Title
FAN, USBx3, IPOD charge
Size
A3
Document Number
MS-1251
Rev
0D
Date:
Friday, October 15, 2010
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29
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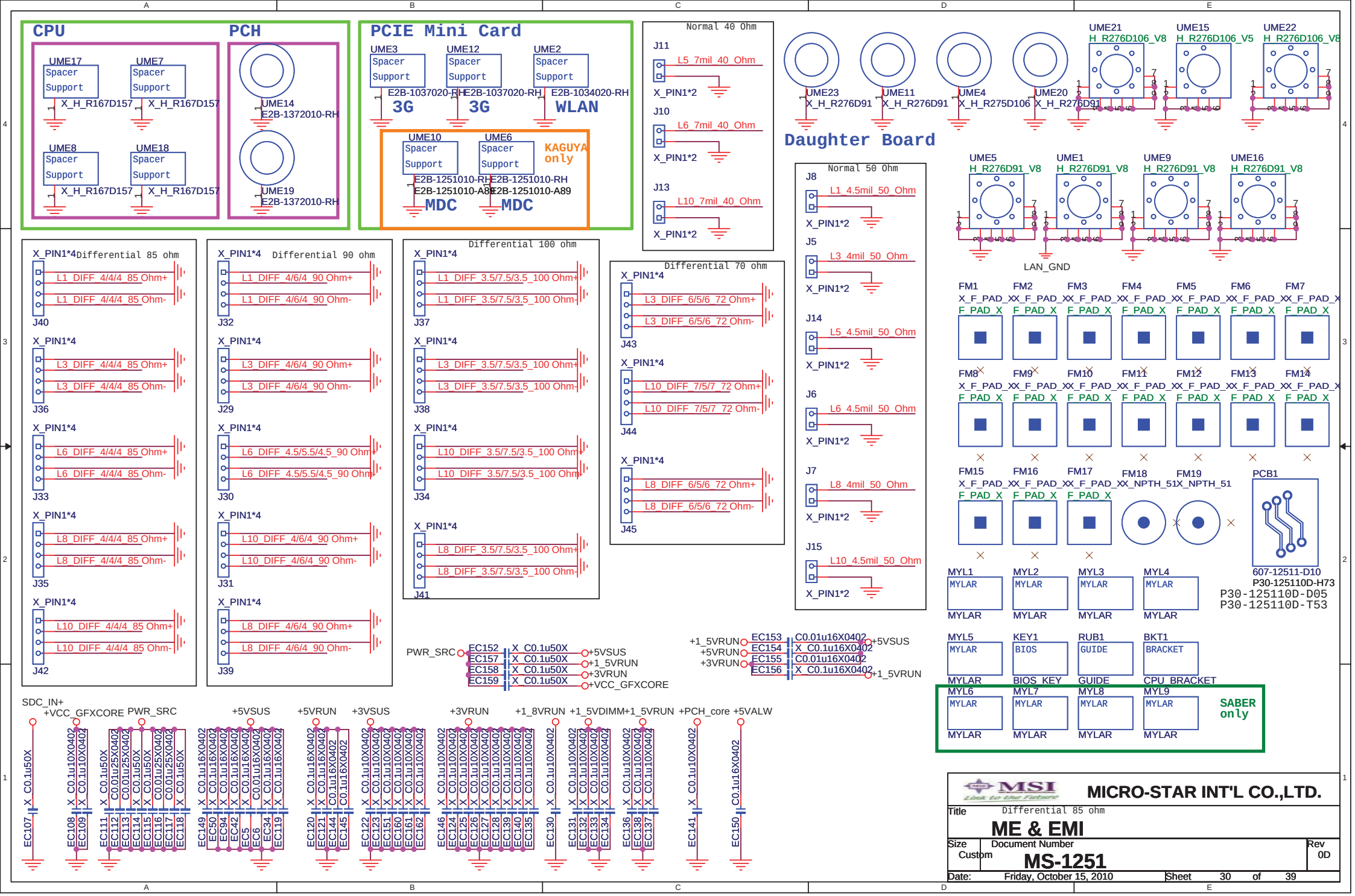
39

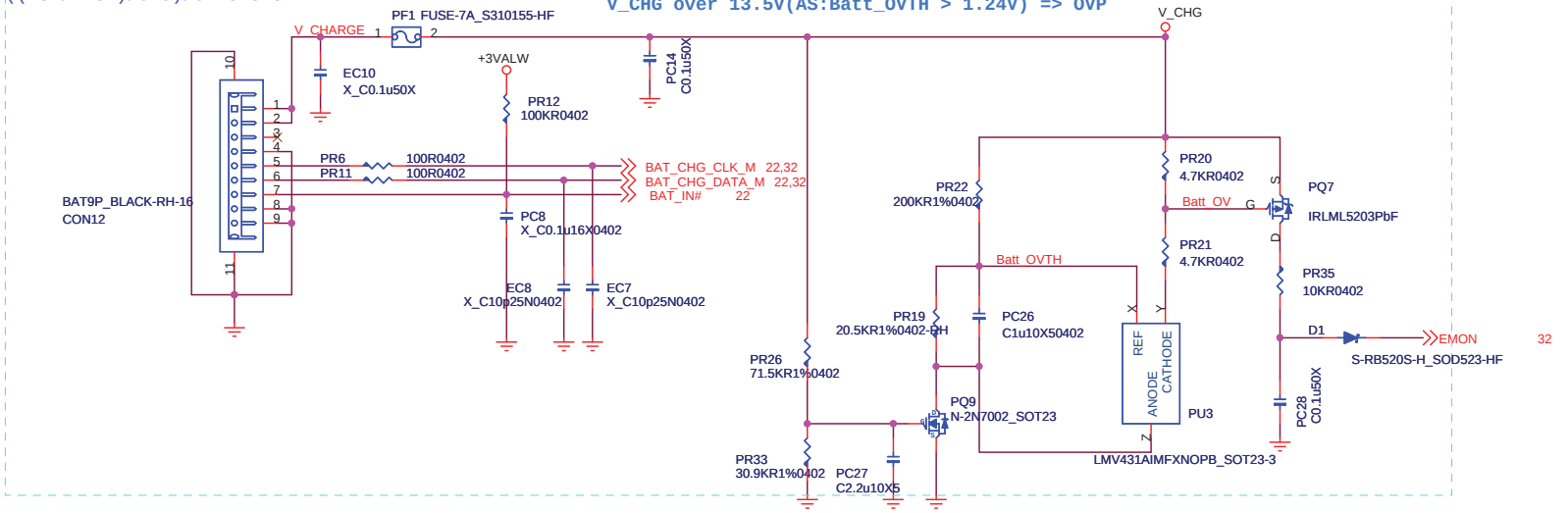


BATTERY CONNECTOR & Battery OVP

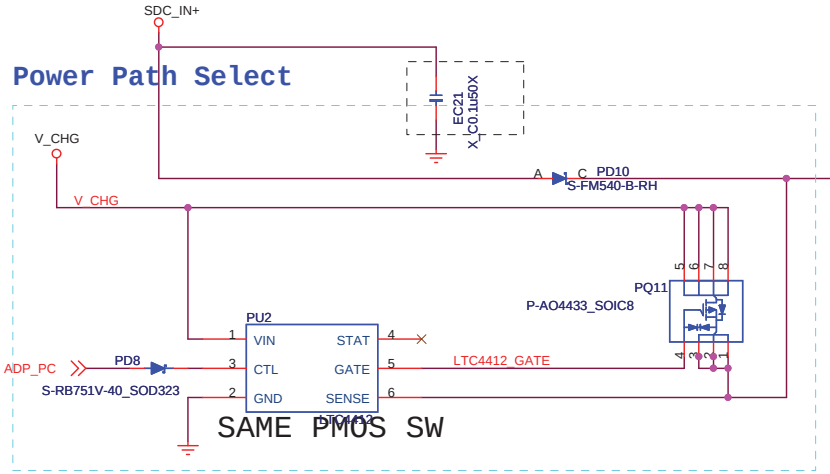
battery fuse select
((45W/7.5V)/0.9)/0.75=8.8A

close to JBAT1

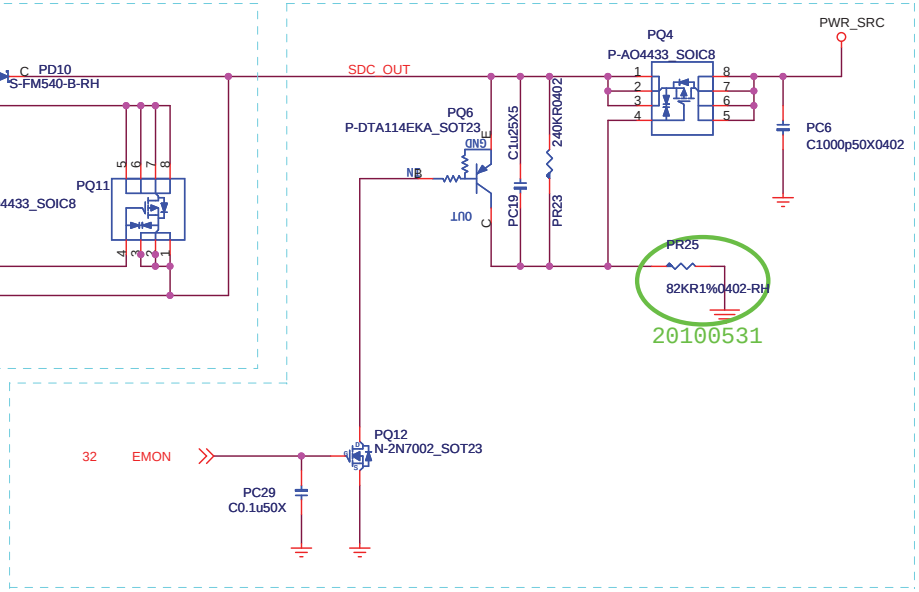
V_CHG over 13.5V(AS:Batt_OVTH > 1.24V) => OVP



Power Path Select



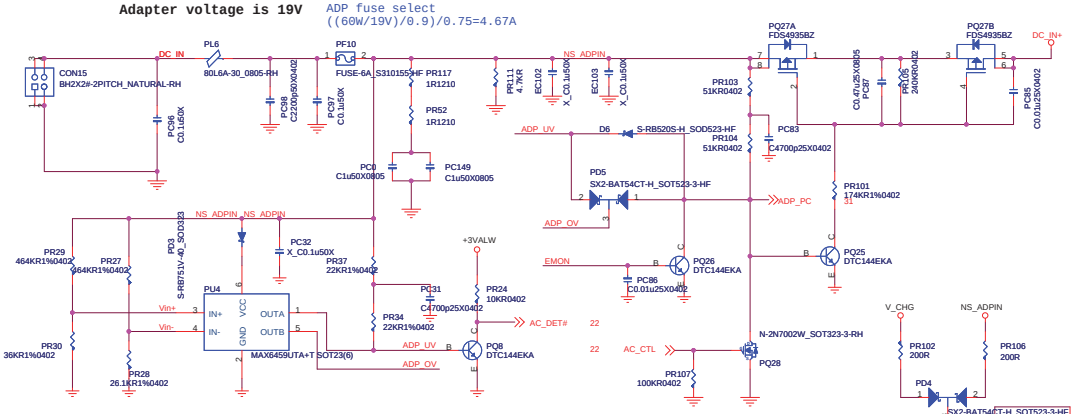
PWR_SRC CUT OFF Protect



MSI	MICRO-STAR INT'L CO.,LTD.		
Title	BATTERY SELECT		
Size B	Document Number MS-1251		Rev 0D
Date: Friday, October 15, 2010	Sheet 31 of 39		

Adapter= 60W
Adapter voltage is 19V

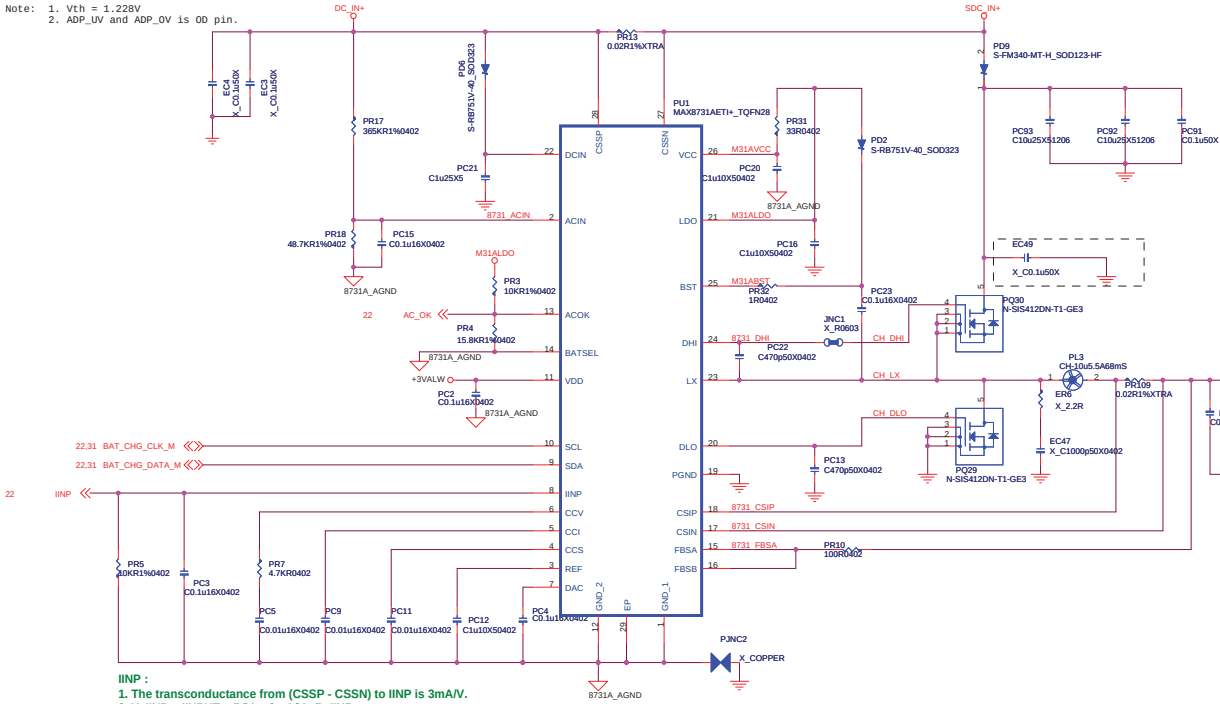
ADP fuse select
((60W/19V)/0.9)/0.75=4.67A



Normal=19V , UVP = 17V , OVP = 23.05V

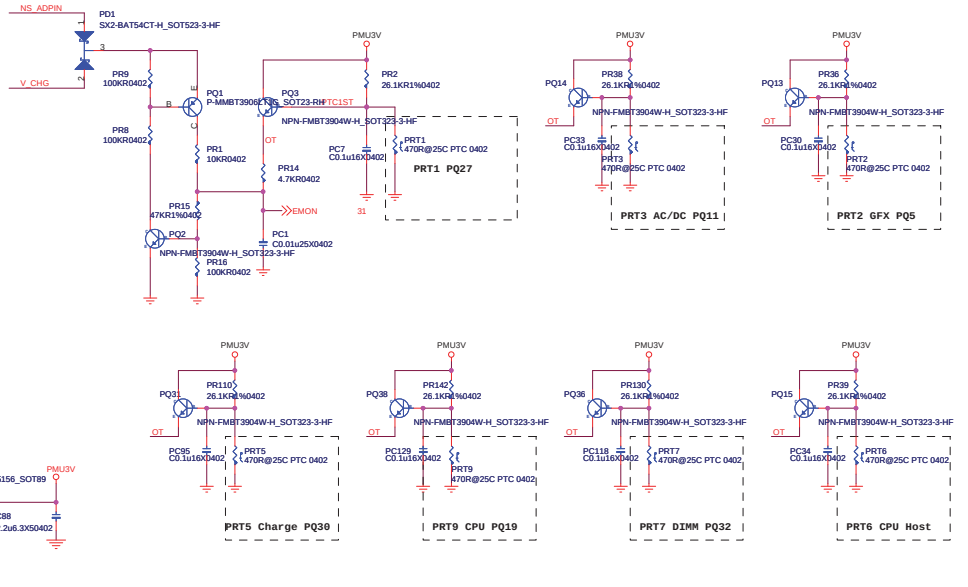
	ADP_UV	ADP_OV	State
Vin+ > Vth	1	X	X
Vin+ < Vth	0	X	UVP
Vin- > Vth	X	0	OVP
Vin- < Vth	X	1	X

Note: 1. Vth = 1.228V
2. ADP_UV and ADP_OV is OD pin.



IINP :
1. The transconductance from (CSSP - CSSN) to IINP is 3mA/V.
2. V_IINP = IINPUT x RS1 x 3mA/V xR_IINP

charger fuse select
((2.3A/0.9)/0.75=3.4A

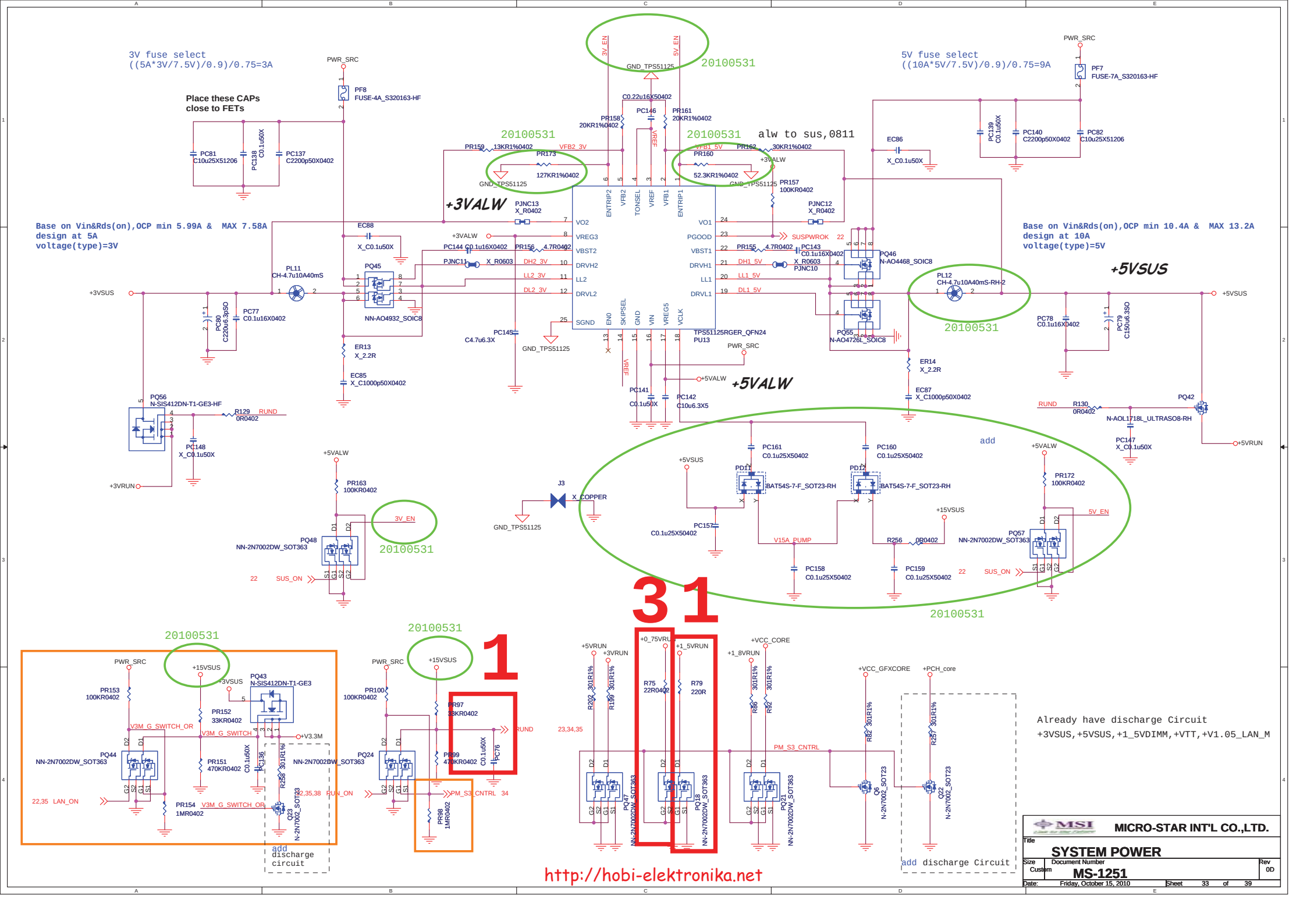


MICRO-STAR INT'L CO.,LTD.

Title: AC_IN & BATTERY CHARGER

Size	Document Number	Rev
A2	MS-1251	0D

Date: Friday, October 15, 2010 Sheet 32 of 39


3V fuse select
((5A*3V/7.5V)/0.9)/0.75=3A
Place these CAPs
close to FETs
PWR_SRC
PF8
FUSE-4A_S320163-HF
PC81
C10u25X51206
PC138
C0.1u50X
PC137
C2200p50X0402
20100531
3V_EN
5V_EN
GND_TPS51125
C0.22u16X50402
PC146
PR158
20KR1%0402
PR161
20KR1%0402
PR159
13KR1%0402
VFB2_3V
PR173
127KR1%0402
VFB1_5V
PR160
52.3KR1%0402
PR162
30KR1%0402
+3VALW
PR157
100KR0402
alw to sus,0811
5V fuse select
((10A*5V/7.5V)/0.9)/0.75=9A
PF7
FUSE-7A_S320163-HF
PC139
C0.1u50X
PC140
C2200p50X0402
PC82
C10u25X51206
EC86
X_C0.1u50X
+3VALW
PJNC13
X_R0402
PJNC12
X_R0402
ENTRIP2
VFB2
TONSEL
VREF
VFB1
ENTRIP1
VO2
VREG3
VBST2
DRVH2
LL2
DRVL2
SGND
VO1
PGOOD
VBST1
DRVH1
LL1
DRVL1
SUSPWROK
22
DH2_3V
LL2_3V
DL2_3V
DH1_5V
LL1_5V
DL1_5V
EN0
SKIPSEL
GND
VIN
VREG5
VCLK
VREF
TPS51125RGER_QFN24
PU13
Base on Vin&Rds(on),OCP min 5.99A & MAX 7.58A
design at 5A
voltage(type)=3V
EC88
X_C0.1u50X
PC144
C0.1u16X0402
PR156
4.7R0402
PJNC11
X_R0603
PC145
C4.7u6.3X
PL11
CH-4.7u10A40mS
PQ45
NN-AO4932_SOIC8
+3VSUS
PC90
C220u6.3pSO
PC77
C0.1u16X0402
ER13
X_2.2R
EC85
X_C1000p50X0402
PC141
C0.1u50X
PC142
C10u6.3X5
+5VALW
PWR_SRC
Base on Vin&Rds(on),OCP min 10.4A & MAX 13.2A
design at 10A
voltage(type)=5V
+5VSUS
PL12
CH-4.7u10A40mS-RH-2
PC155
4.7R0402
PC143
C0.1u16X0402
PJNC10
X_R0603
PQ46
N-AO4468_SOIC8
PQ55
N-AO4726L_SOIC8
ER14
X_2.2R
EC87
X_C1000p50X0402
PC78
C0.1u16X0402
PC79
C150u6.3SO
+5VSUS
PQ56
N-SIS412DN-T1-GE3-HF
R129
0R0402
RUND
PC148
X_C0.1u50X
+3VRUN
PQ42
N-AOL1718L_ULTRASO8-RH
R130
0R0402
PC147
X_C0.1u50X
+5VRUN
PR163
100KR0402
PQ48
NN-2N7002DW_SOT363
3V_EN
22
SUS_ON
J3
X_COPPER
GND_TPS51125
add
PC161
C0.1u25X50402
PC160
C0.1u25X50402
PD11
PD12
BAT54S-7-F_SOT23-RH
+15VSUS
PC157
C0.1u25X50402
V15A_PUMP
PR256
0R0402
PC158
C0.1u25X50402
PC159
C0.1u25X50402
PR172
100KR0402
PQ57
NN-2N7002DW_SOT363
5V_EN
SUS_ON
31
1
20100531
PWR_SRC
+15VSUS
+3VSUS
PQ43
N-SIS412DN-T1-GE3
PR153
100KR0402
PR152
33KR0402
V3M_G_SWITCH_OR
V3M_G_SWITCH
+V3.3M
PQ44
NN-2N7002DW_SOT363
PR151
470KR0402
C0.1u50X
PC136
PR255
301R1%
NN-2N7002DW_SOT363
22,35 LAN_ON
PR154
1MR0402
Q23
N-2N7002_SOT23
add
discharge
circuit
PR100
100KR0402
PR97
33KR0402
RUND
PQ24
PR99
470KR0402
C0.1u50X
PC76
22,35,38 RUN_ON
PM_S3_CNTRL
34
PR98
1MR0402
+5VRUN
+3VRUN
+0_75VRUN
+1_5VRUN
+1_8VRUN
+VCC_CORE
+VCC_GFXCORE
+PCH_core
R202
301R1%
R199
301R1%
R75
22R0402
R79
220R
R86
301R1%
R82
301R1%
R84
301R1%
R81
301R1%
23,34,35
PM_S3_CNTRL
PQ47
NN-2N7002DW_SOT363
PQ18
NN-2N7002DW_SOT363
PQ21
NN-2N7002DW_SOT363
Q6
N-2N7002_SOT23
Q22
N-2N7002_SOT23
add discharge Circuit
Already have discharge Circuit
+3VSUS,+5VSUS,+1_5VDIMM,+VTT,+V1.05_LAN_M
http://hobi-elektronika.net
MSI
MICRO-STAR INT'L CO.,LTD.
Title
SYSTEM POWER
Size
Custom
Document Number
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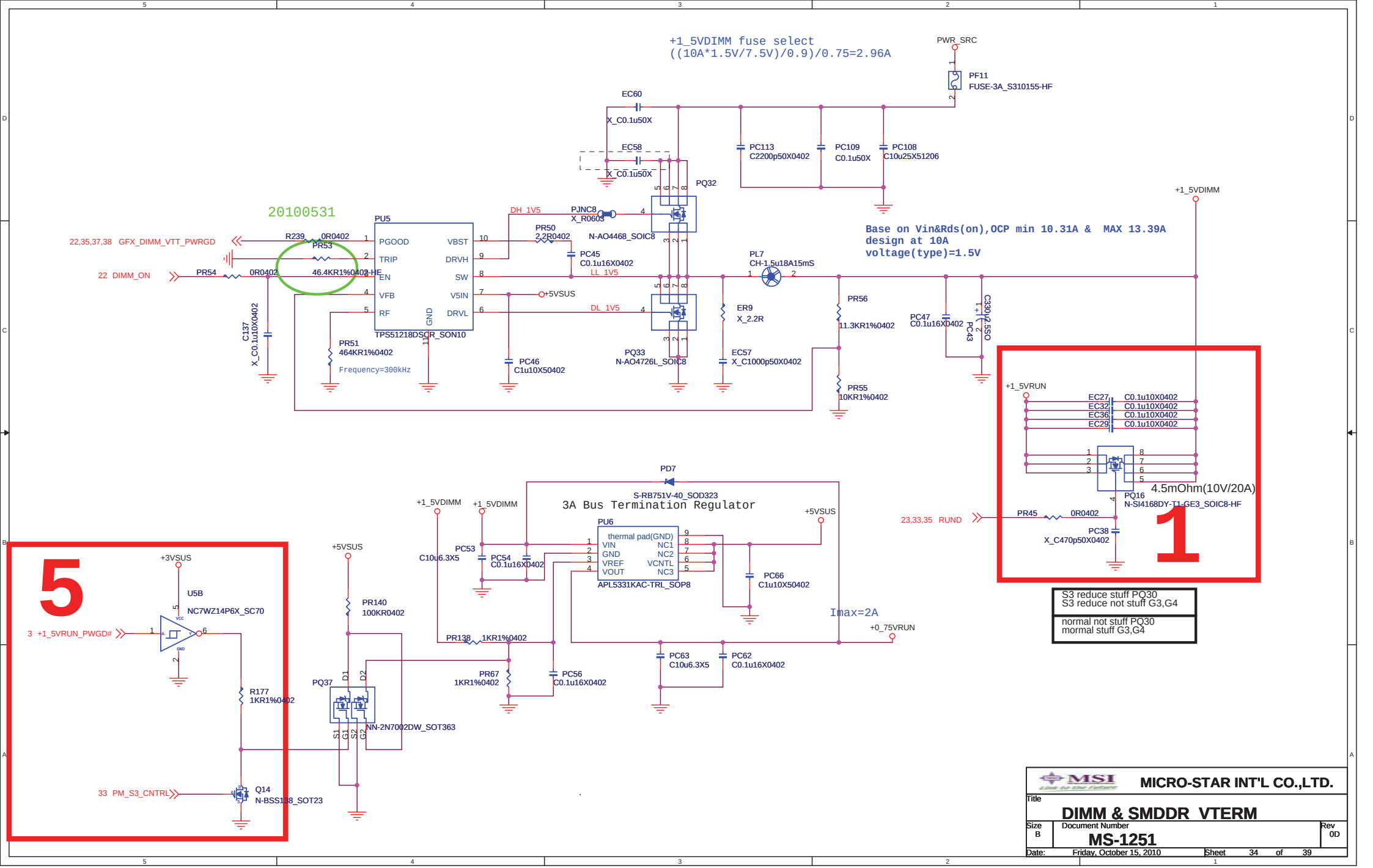
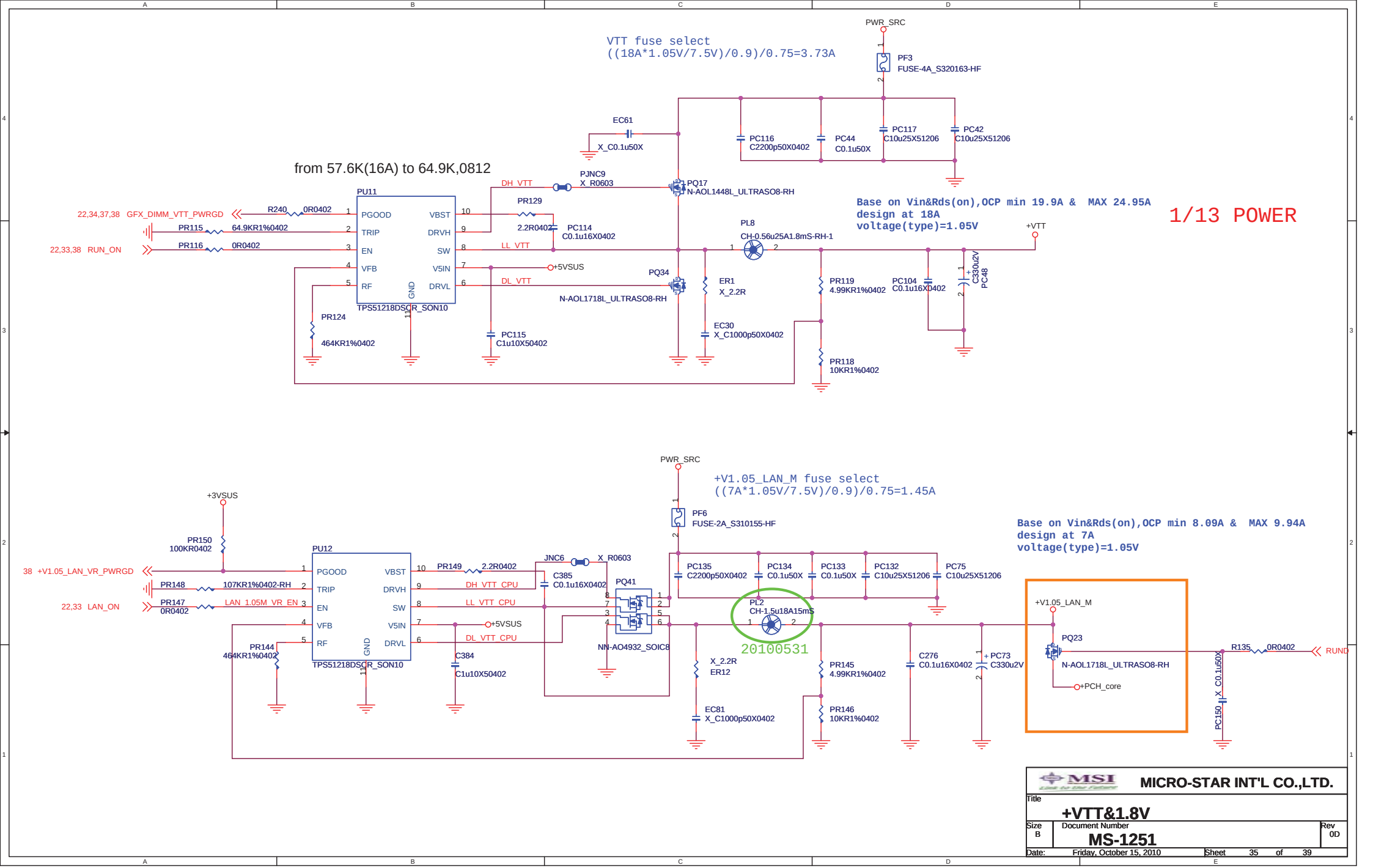




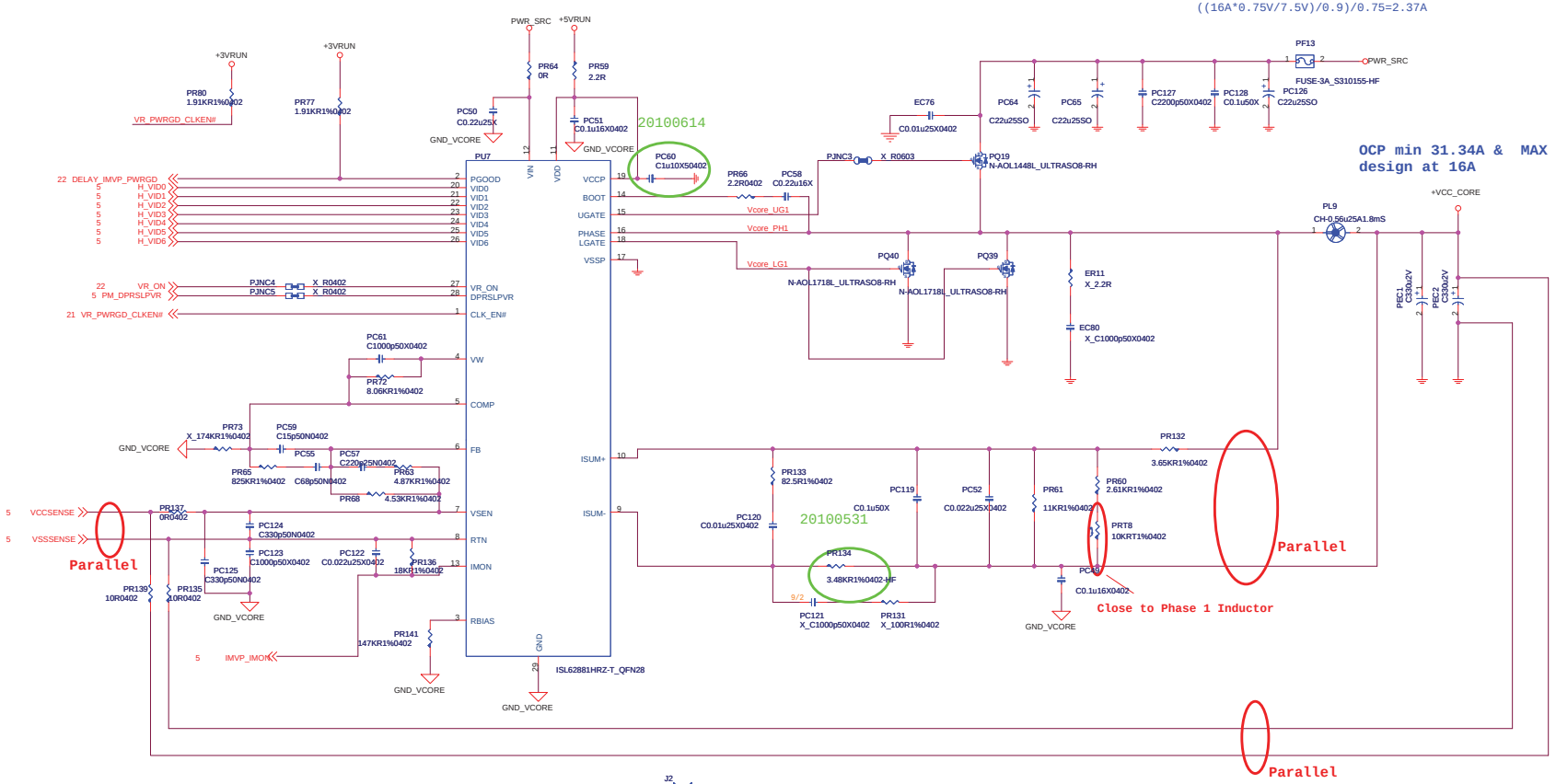
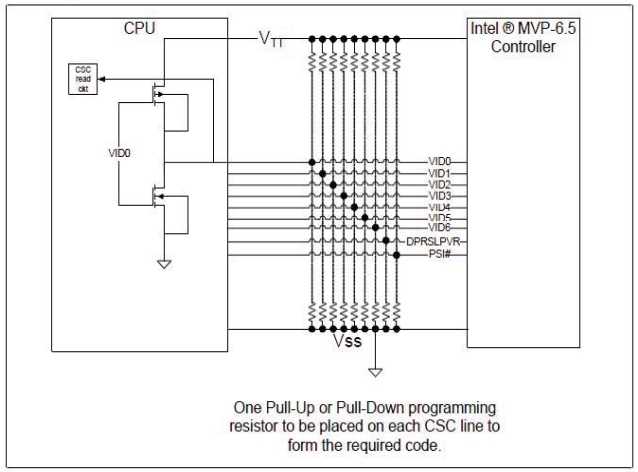
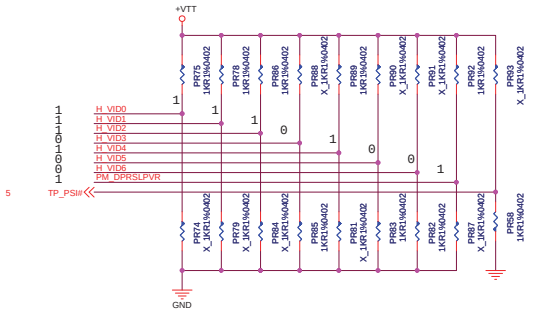


Figure 12. CSC Implementation



VID[6:0]=1,1,1,0,1,0,0,1
DPRSLPVR=1(default) , IMVP6.5
VID[2:0] for MSID (Market Segment ID)
VID[5:3] for CSC, CRB default '010' = 30A (Iccmax)



VID[5:3] will be used to provide IMON gain setting to CPU during POC

CPU SKU, ICC_CORE-MAX Maximum CPU Core Current	IMAX (IMON=900 mV)	CPU Gain Setting Set on Platform Via POC Lines	Equivalent Gain
Feature disabled		000	
ICC_CORE-MAX <= 20A	20A	001	45
20A< ICC_CORE-MAX <= 30A	30A	010	30
30A< ICC_CORE-MAX <= 40A	40A	011	22.5
40A< ICC_CORE-MAX <= 50A	50A	100	18
50A< ICC_CORE-MAX <= 60A	60A	101	15
60A< ICC_CORE-MAX <= 70A	70A	110	12.857
70A< ICC_CORE-MAX <= 90A	90A	111	10

NOTES:

1. VID[2:0] "Reserved " – default VID[2:0]='111' – option to change default should be provided on the motherboard.
2. VID[5:3] will be used to provide IMON gain setting to CPU during CSC (see Section 5).
3. VID[6] "Reserved" – default VID [6]='0' - option to change default should be provided on the motherboard.
4. DPRSLPVR will be used to identify type of CPU core VR controller. DPRSLPVR='1' for IMVP-6.5-compliant controller.
5. PSI# - "Reserved" – default PSI#='0' - option to change default should be provided on the motherboard.

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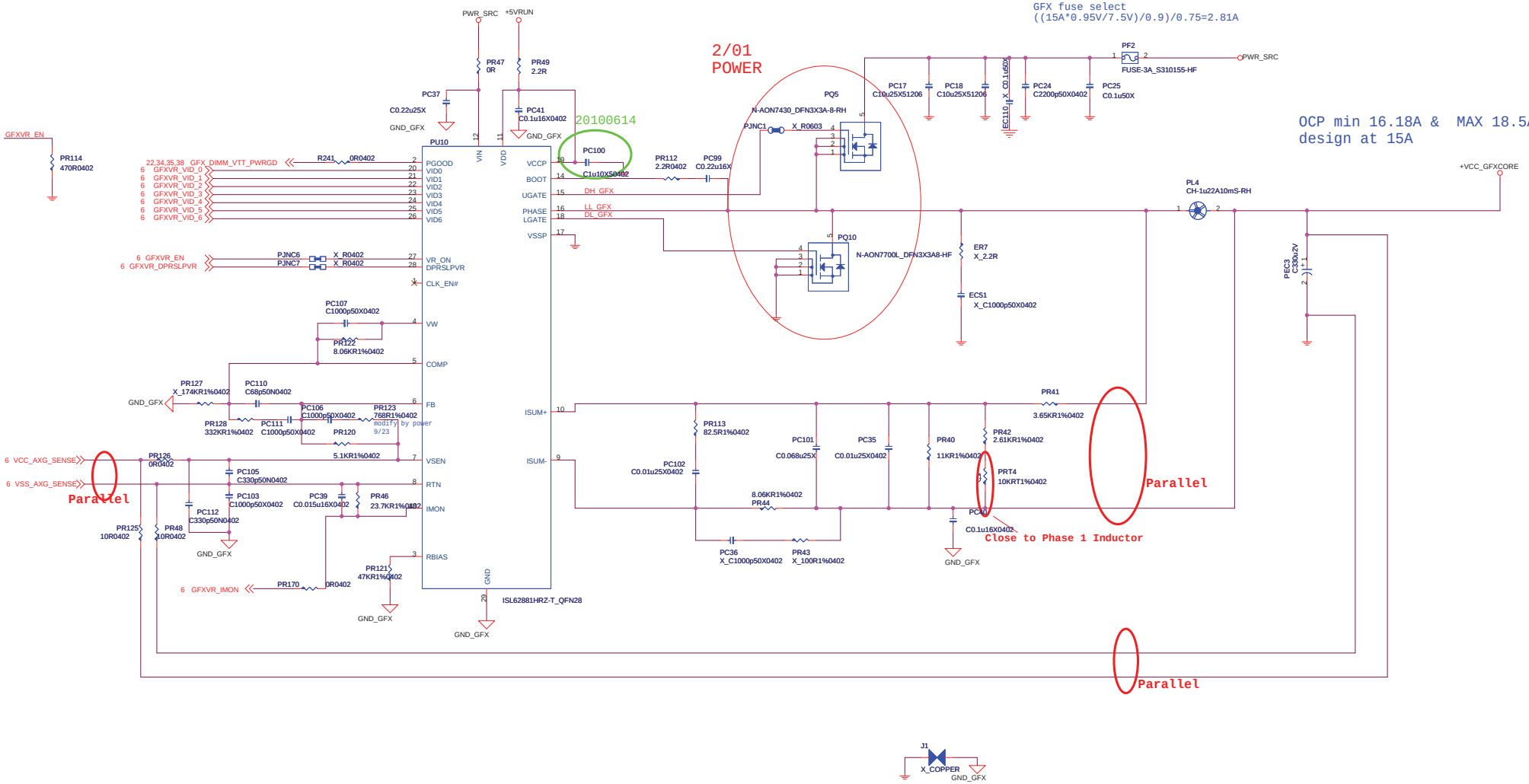

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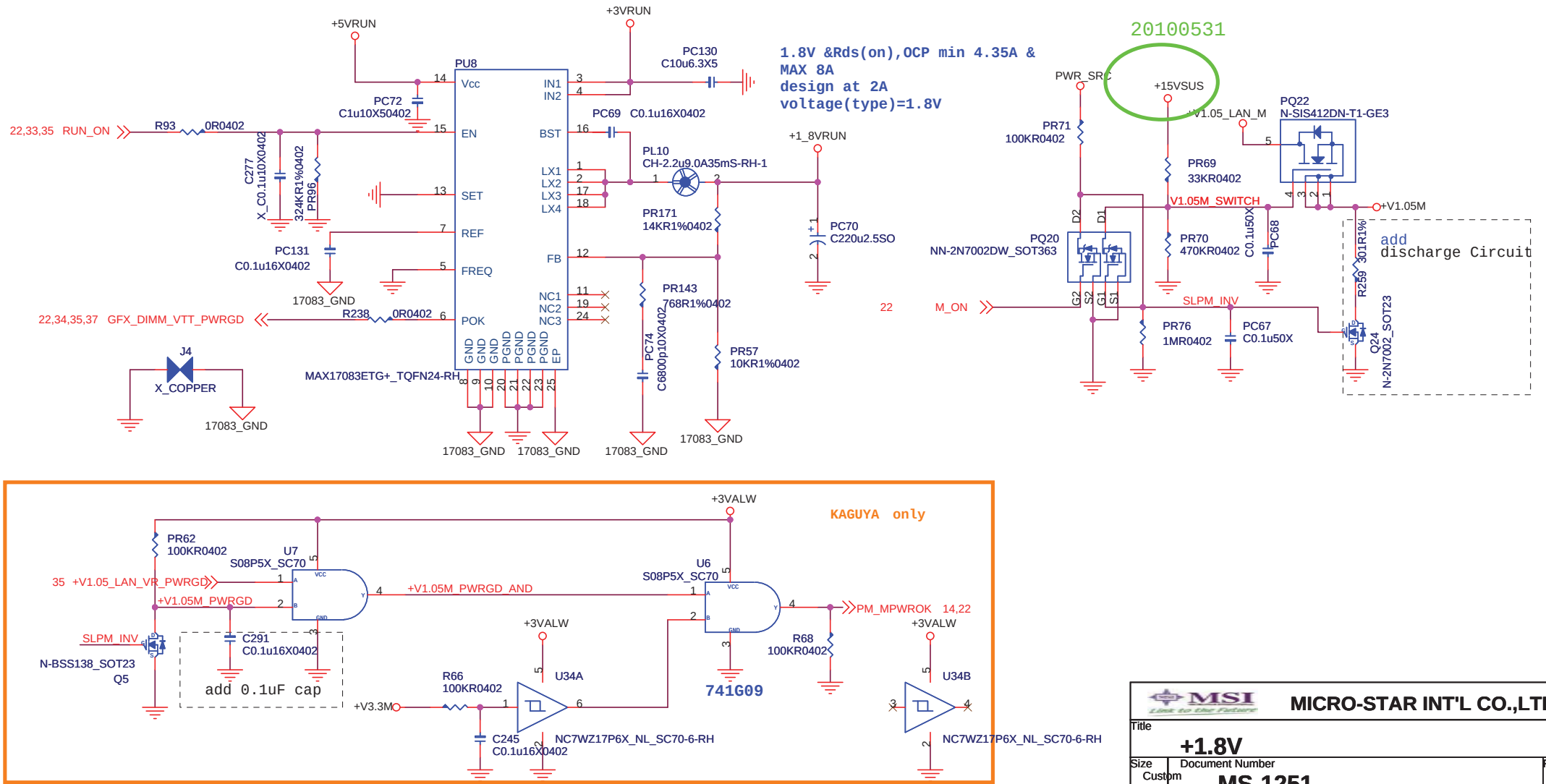

MSI Link to the Future

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0A->0B

1. Change Intel LAN port form PCIE port1 to port6
2. Install R125 for MDC function
3. NC R134 and R237
4. Change PR53 to 46.4K
5. Change PR160 to 39.2K
6. Change PRT8 PRT4 to Mureta components
7. Remove PU resistor R137 for TPM address setting
8. Modify R157 to 180 Ohm to match buzzer spec
9. Remove G1
10. Chane R141 PU Power from +3VSUS to +3VRUN
11. Change PCH GPIO port to GPIO8 and GPIO13 for G-sensor INT0 and INT1 function
12. Add debug board solution in PCIE mini card CON14
13. Change Finger print detect function R12 from daughter board to Main board
14. Change Touch pad PU resistor R260 and R261 form daughter board to Main board
15. Change PM_LANPHY_ENABLE PU power form +3VSUS to +V3.3M
16. Increase HDMI circuit page23
17. Increase U22 LAN switch chip
18. Increase CON22 BTB connector for SABER daughter board
19. Increase SATA4 for SABER PCIE-slot SSD solution
20. Remove BIOS ROM socket
21. Increaes FPC3 for SABER Keyboard
22. Change CON5 pins assignment for match both panel 13" & 12"
23. Change CON11 to 4 pins connector for SABER and KAGUYA
24. spreat 3V 5V OCP control circuit Increase PR172 PQ57
25. change RUND volteage Increase charge pump circuit PC157 PC158 PC159 PC160 PC161 PD11 PD12 R256
26. change 3V ocp set PR173
27. change 5V ocp set PR160
28. modify 5V choke temperature heat change PL12
29. change dimm ocp set PR53
30. modify +V1.05_LAN_M response change choke PL2
31. change CPU ocp set PR134
32. change CPU VDDP decoupling capacitor PC60
33. change GFX VDDP decoupling capacitor PC100
34. change EC50, EC17, to 0Ohm ER15 and ER16
35. separate RN4 to R265, R266, R267 and R268 for layout
36. Change R34 pull high power form +3VRUN to +3VSUS
37. Increase ECN5 for SABER
38. Increase U34
39. Increase PR94, PR95, PR174
40. Change R214, R224 to 1% tolerance
41. Change R225 to 24K1%
42. Increase C329 for CRT ripple
43. Increase C238 and R263.
44. Change PF6 to 2A
45. Increase R90, R91, R264 for KAGUYA
46. Increase R127
47. Increase R272
48. Increase R274 for KAGUYA FP_DET, R373 for SABER WLAN_LED#
49. Change power source form +3VSUS to +3VRUN (U13, U14, U15, R223, R235)
50. Increase R275
51. Increase U33, R277 and C332 for CARD_RST#
52. Increase R278 for ODD_DET#
53. Change PL12 to CH-2.2u14A
54. Change PR160 to 45.3KR1%

0B->0C

1. Exchange SATA HDD TX and RX signal
2. Increase R280 for SABER power sequence
3. Increase G1 for SABER
4. Increase R282 for SABER
5. Change HDD connector CON8
6. Increase KEY1, MYL1, MYL2 and CPU bracket BKT1 by ME
7. Increase EMI cap EC166~EC173
8. Increase C333 install C243=0.22u R112=270K R276=27K C301-2.2ufor avoid +3V_WLAN inruscurrent
9. Increase R286 and install C238=0.1u R20=270K R263=27K for avoid LCD_SRC inruscurrent
10. Increase ED13, and install EC6,EC112,EC113,EC116,EC117,EC153,EC155,EC76 10nF bye EMI
11. Increase ECN6,ECN7 by EMI
12. Change C410 form 10u to 1u
13. Increase net SIM_CD and R283 for SIM detect function
14. Change RGP Phi solution C356 c360 c364 c366 c368 c371 to 4.7pf,C359 C367 C369 to 10pf
15. Change USB switch IC U2 to MAX14550EETB for Ipod charger solution.

0C->0D

1. Increase R290 and NC PF15
2. Change C301 form 1uF to 2.2uF, C243 form 0.1uF to 0.22uF
3. Change R272 form 0603 to 0805
4. Remove ECB1,ECB2,EC84,EC83,EC89,EC90.
5. Change C238 form 0402 to 0603
6. Change C376 to 0.01u
7. Change C238 form 0.1u to 1u
9. Change Q9 and increase R291
10. Change PC119 from 0.22u to 0.1u

0D ->10

1. change UME15, UME21, UME22 footprint to H_R276D106_V8
2. change PC35 from 4700p to 0.01uF, PR120 from 6.04K to 5.1K
3. increase mylar6, mylar7, mylar8, mylar9
4. Remove L18, L19, L20; change C356, C366, C368 to 4.7p; change C359, C367, C369 to 4.7p and C360, C364, C371 to 10p
5. increase 0R R292~R296
6. change R20 to 620K and R263 to 62K

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