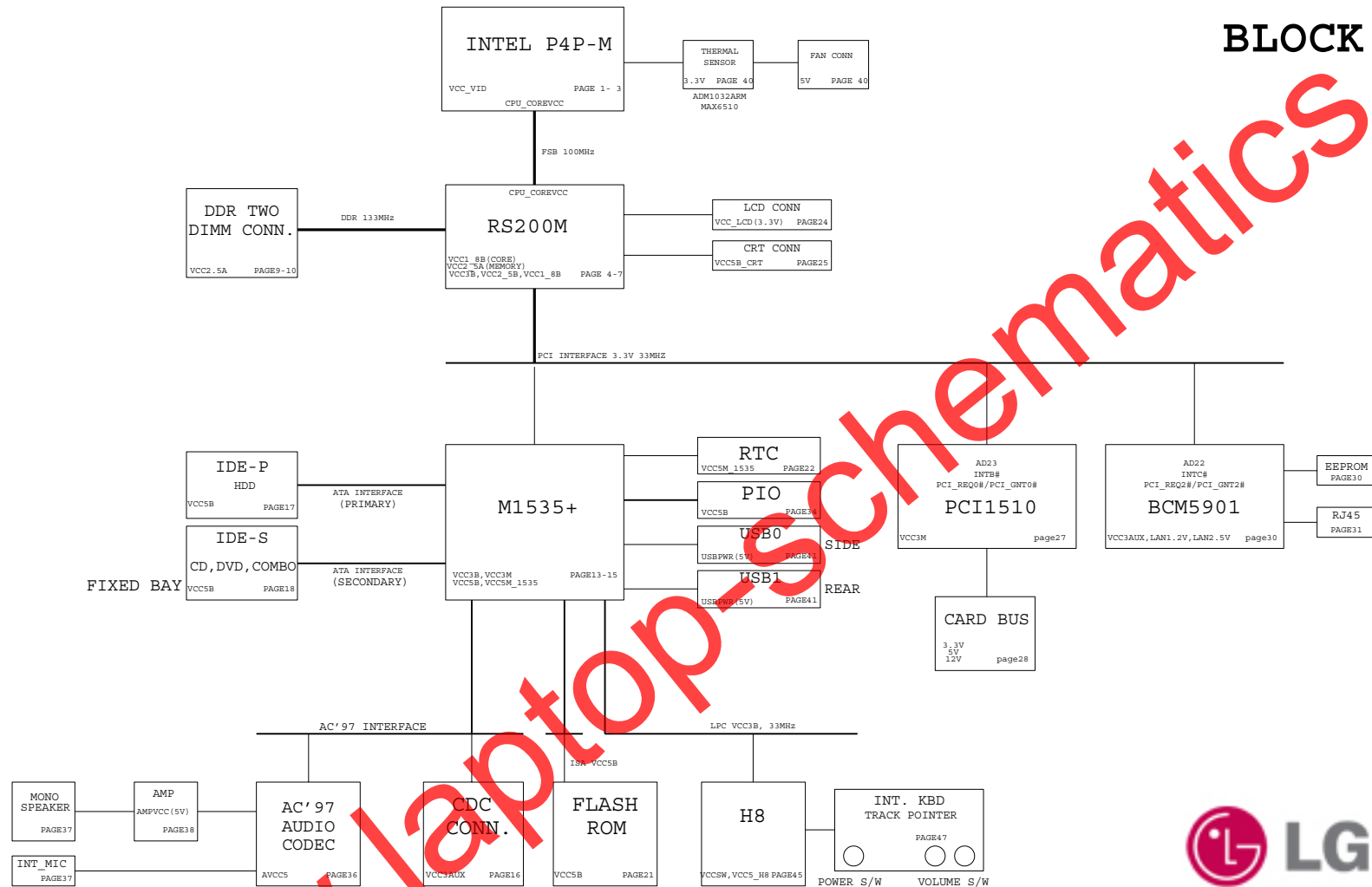
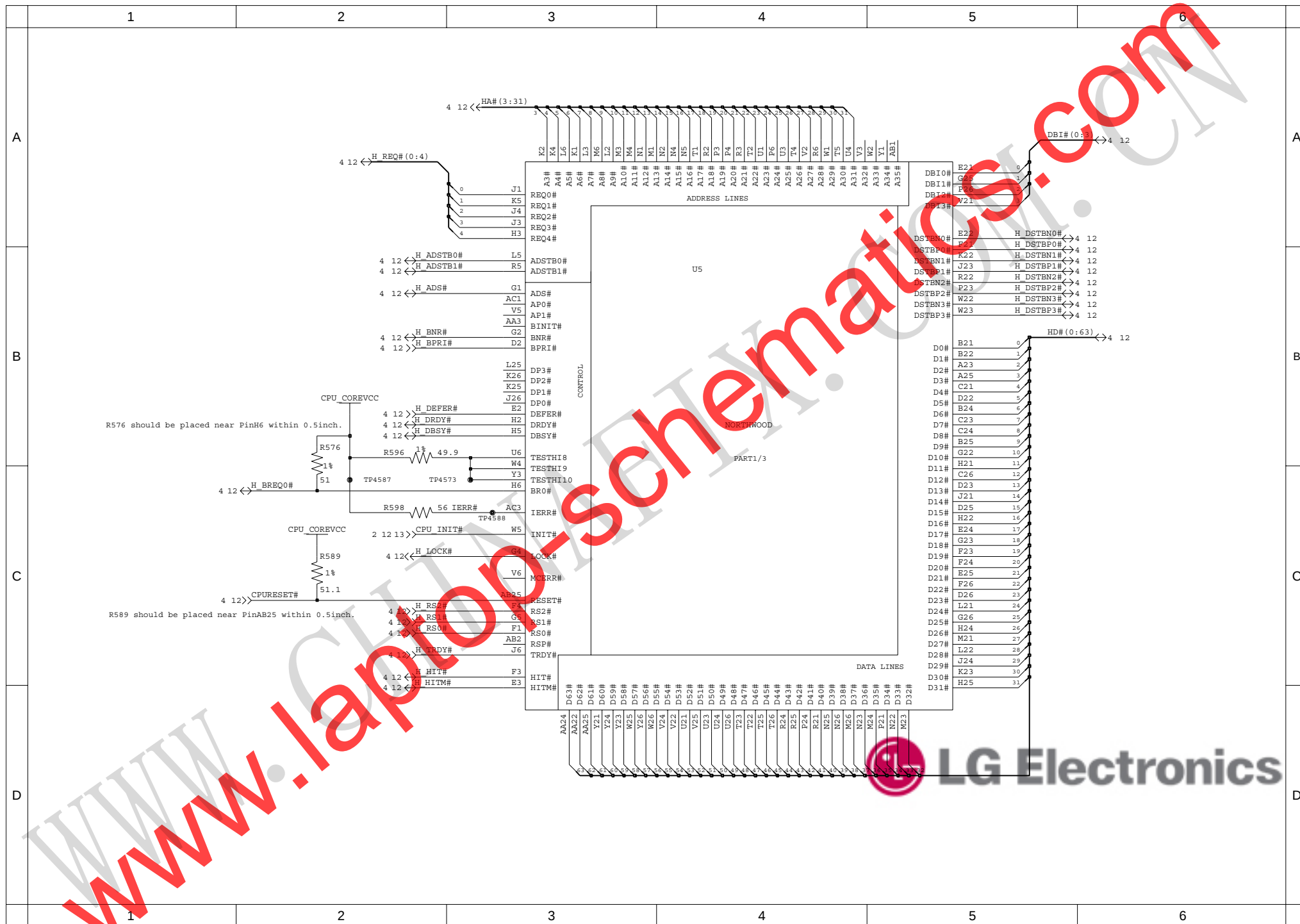
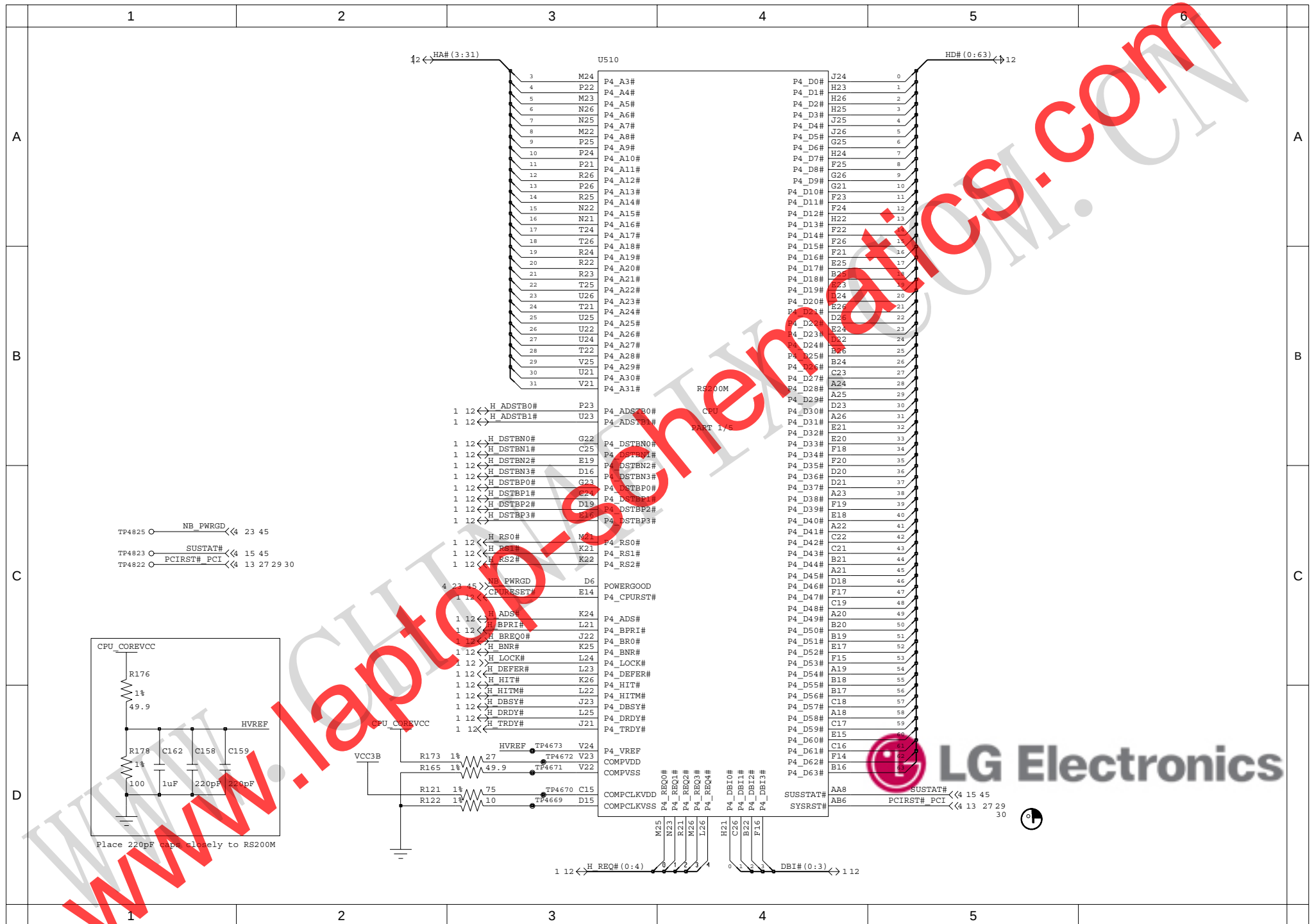


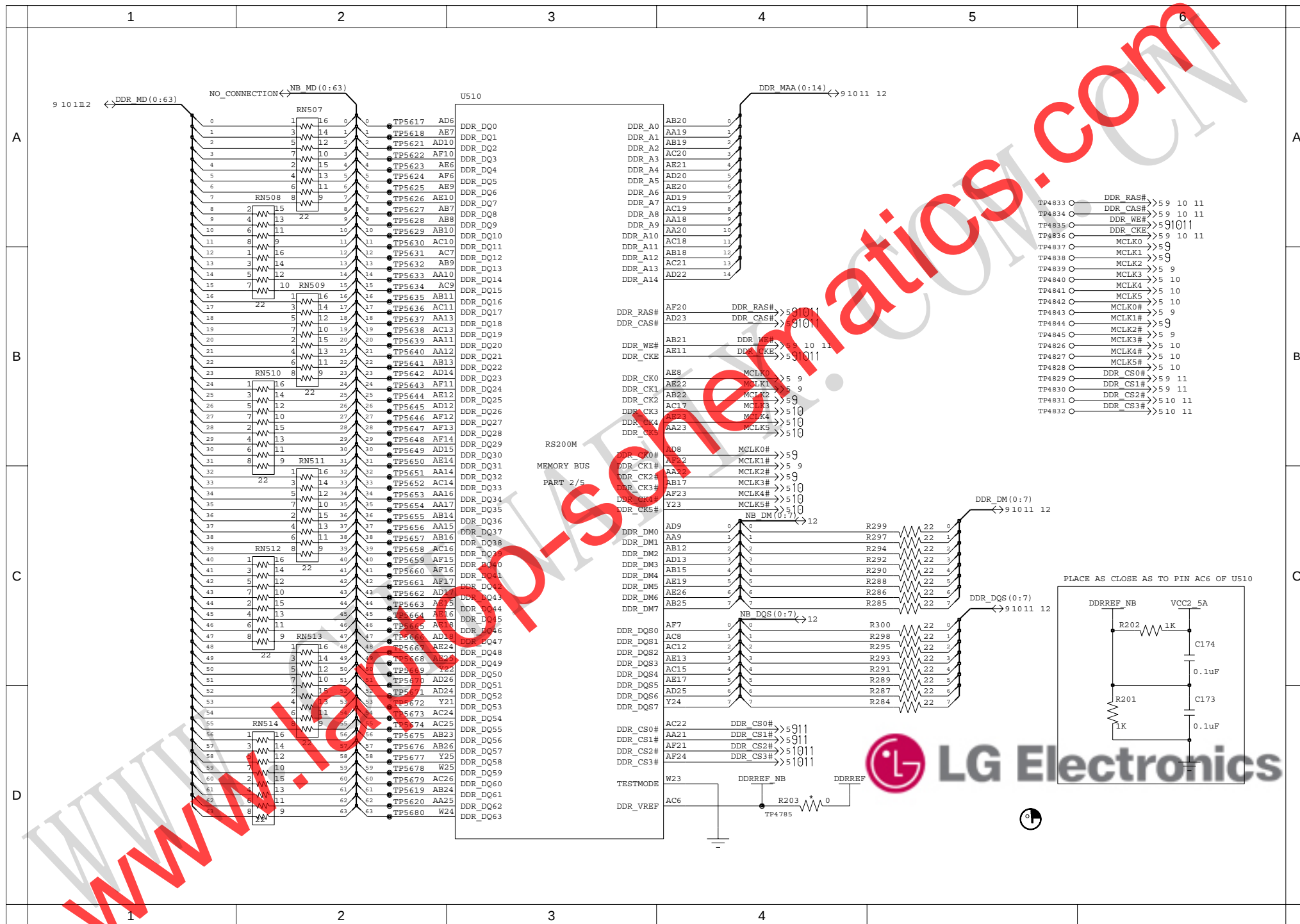
BLOCK DIAGRAM

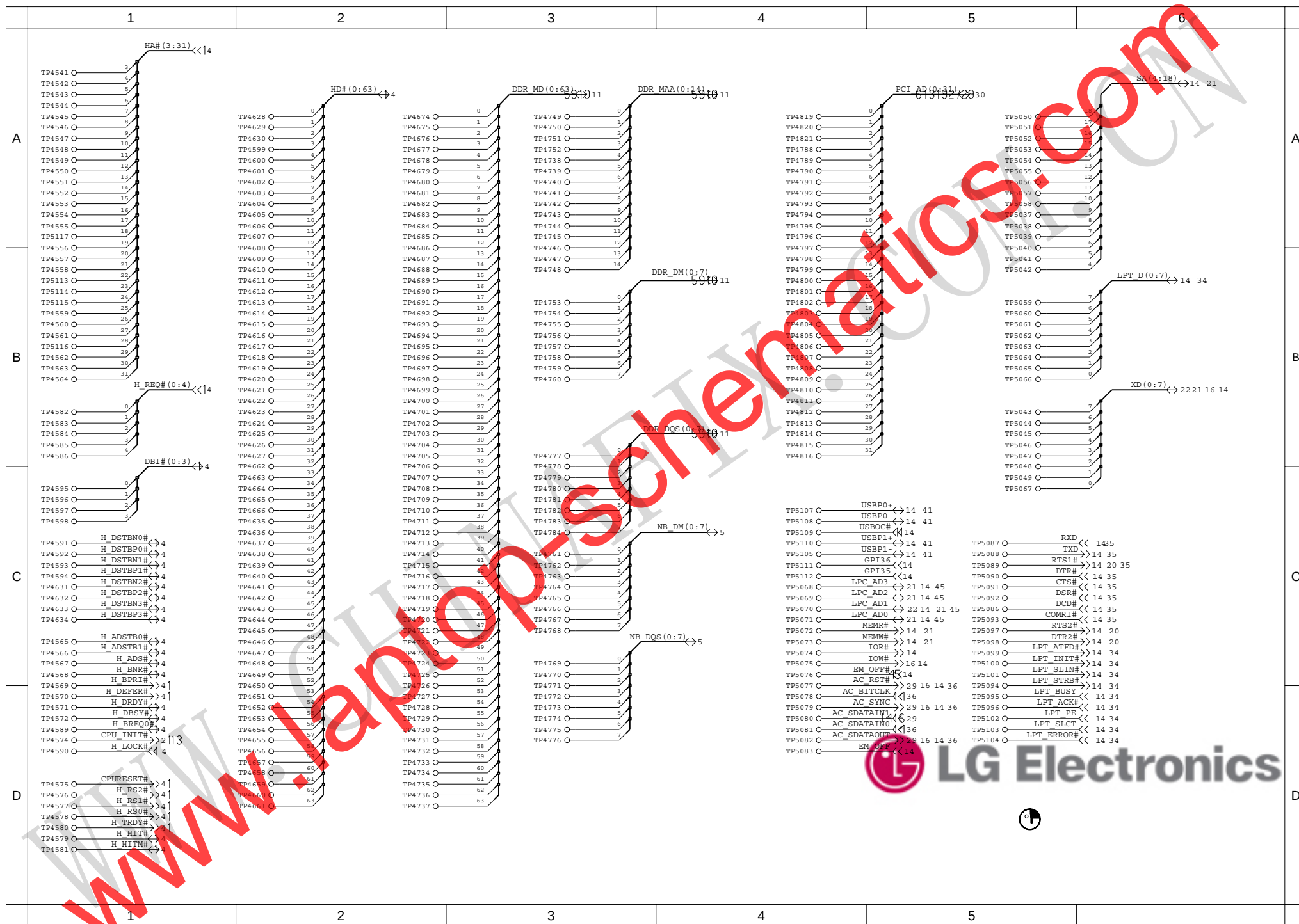


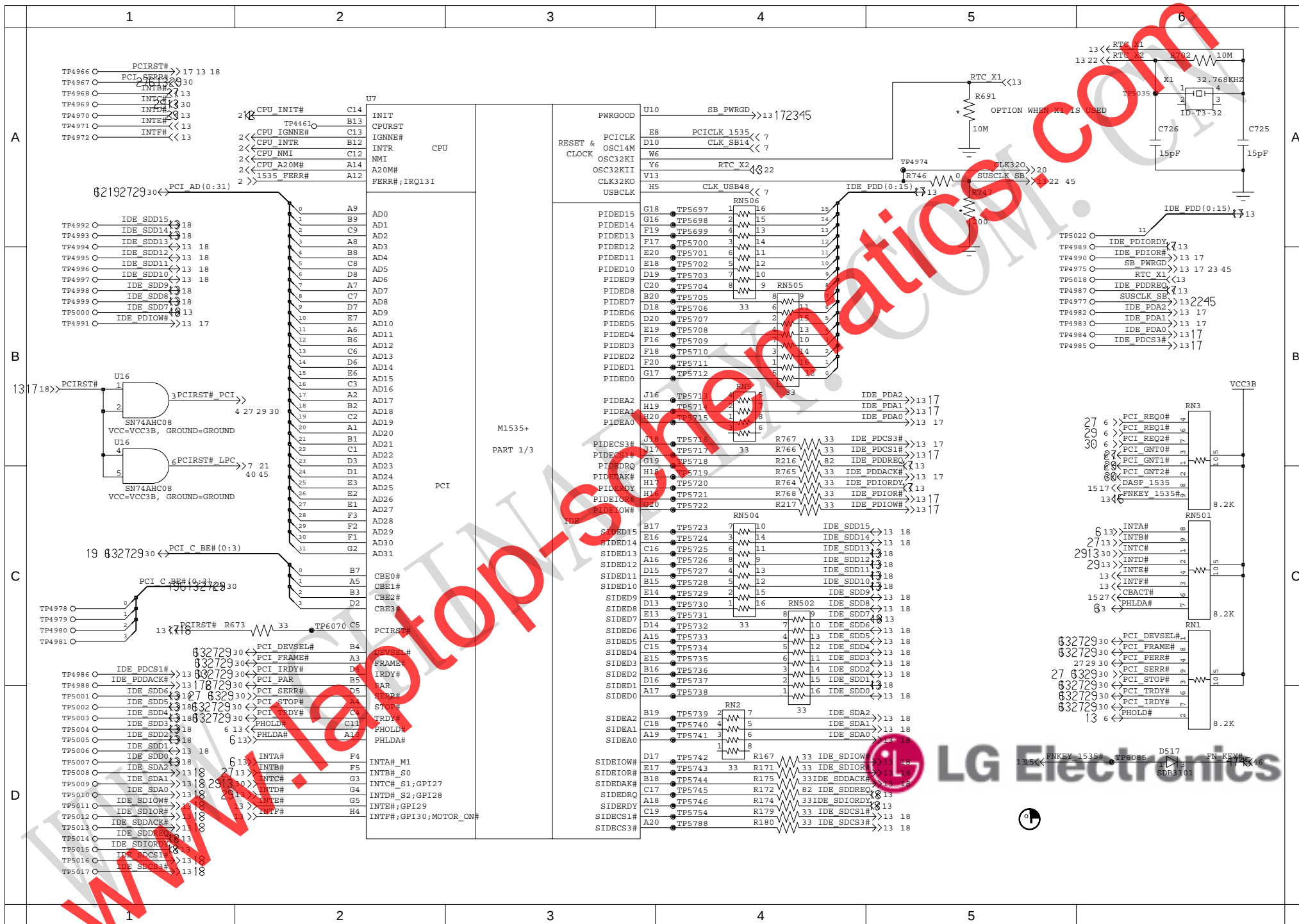


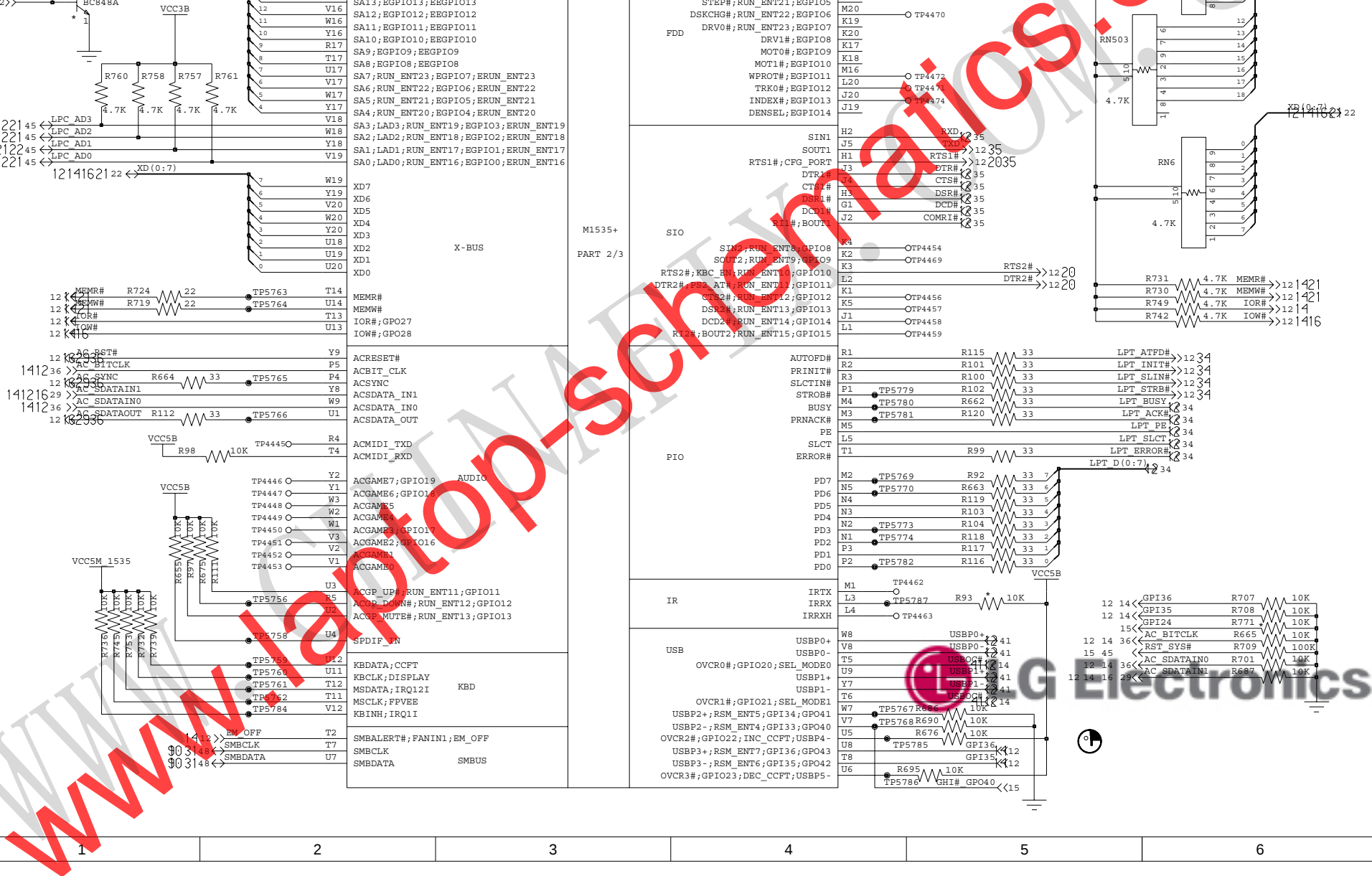


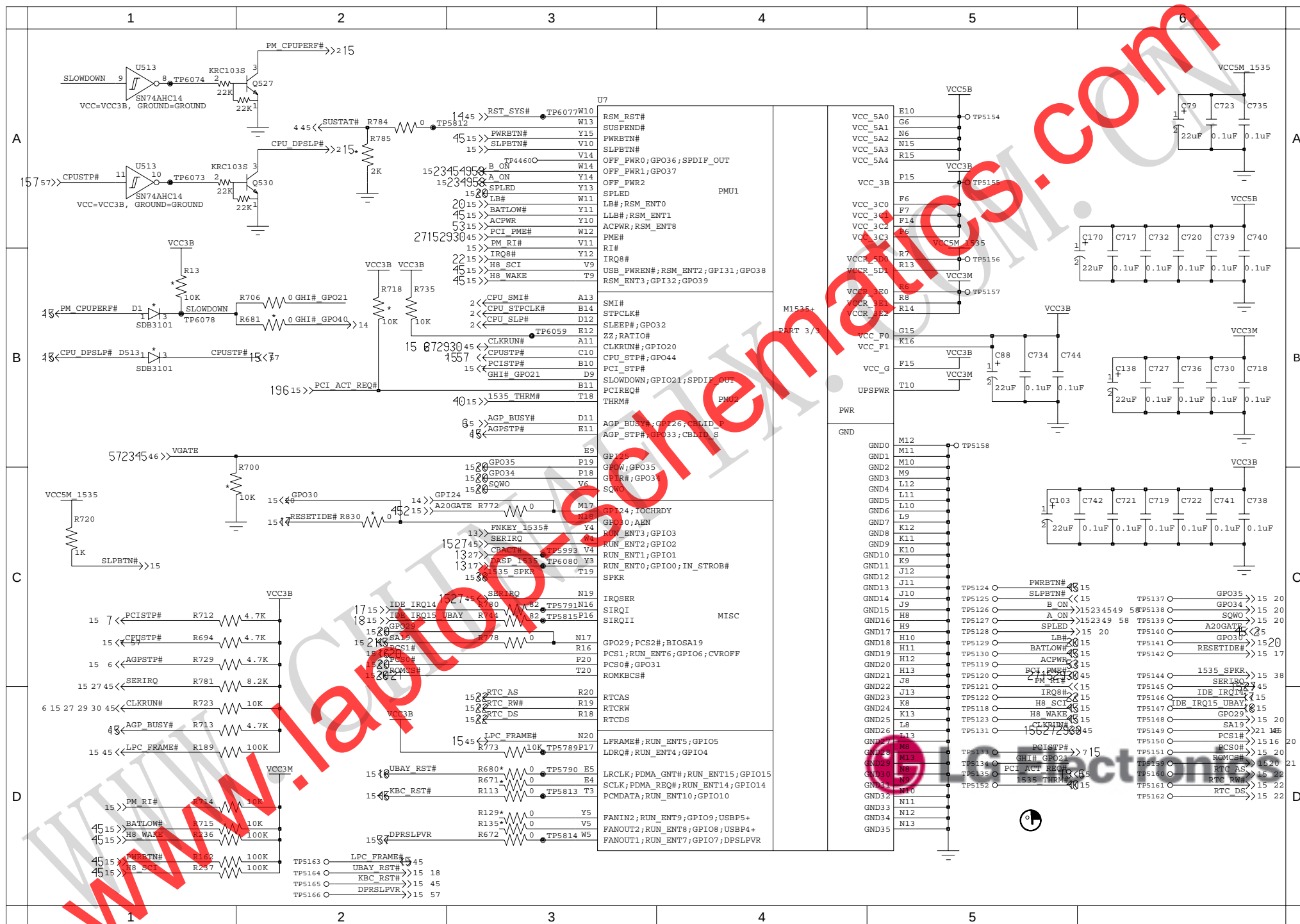


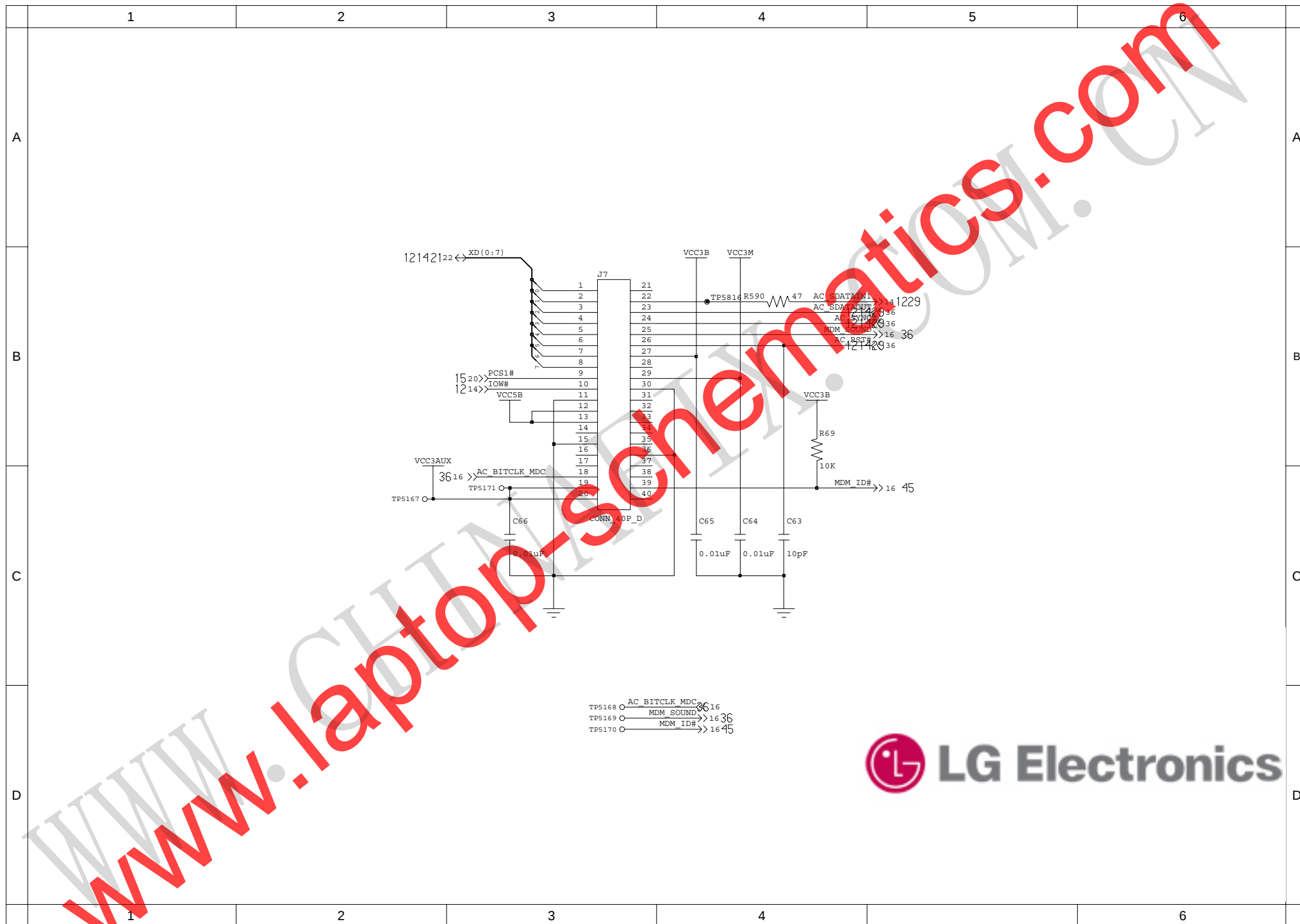


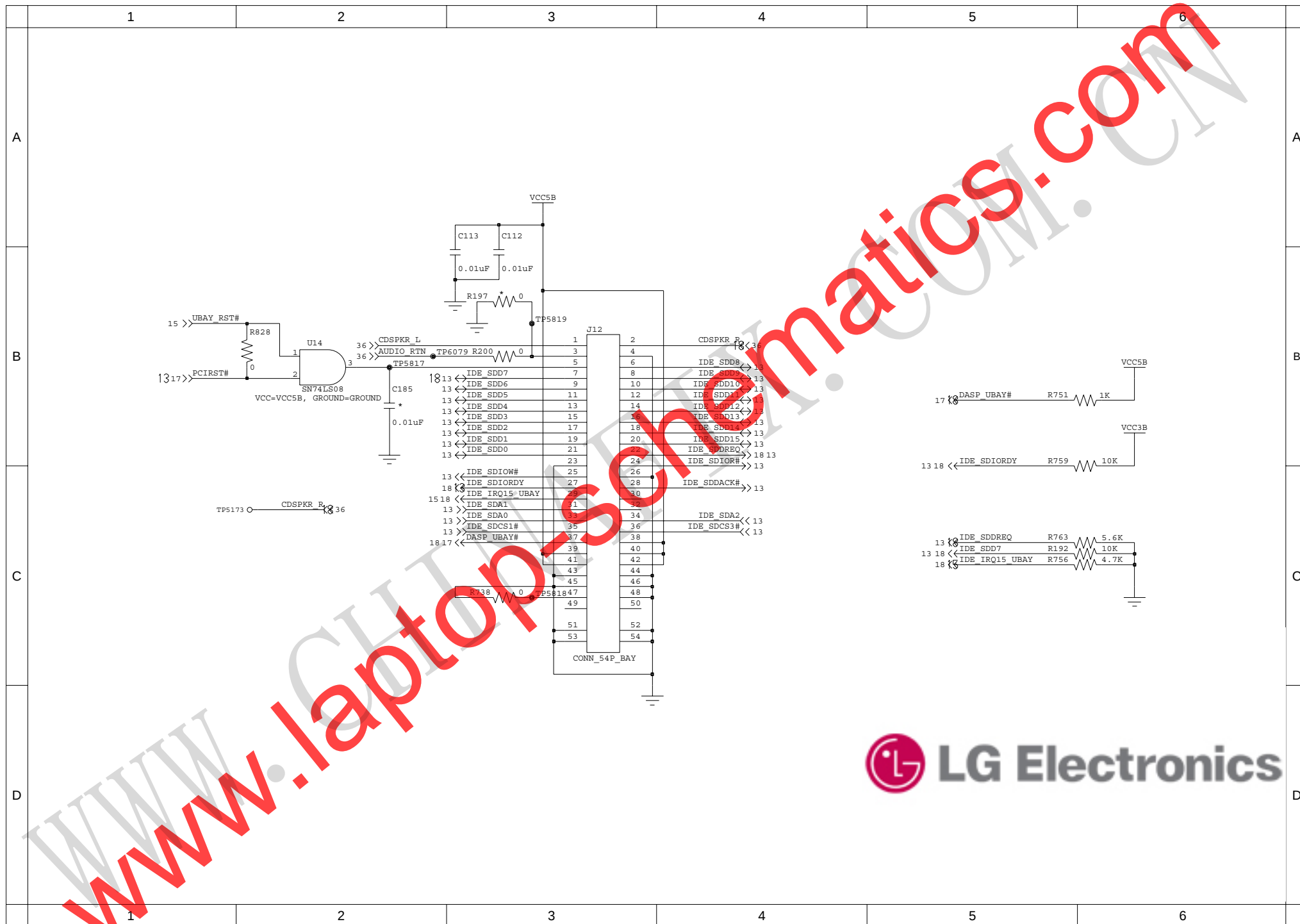




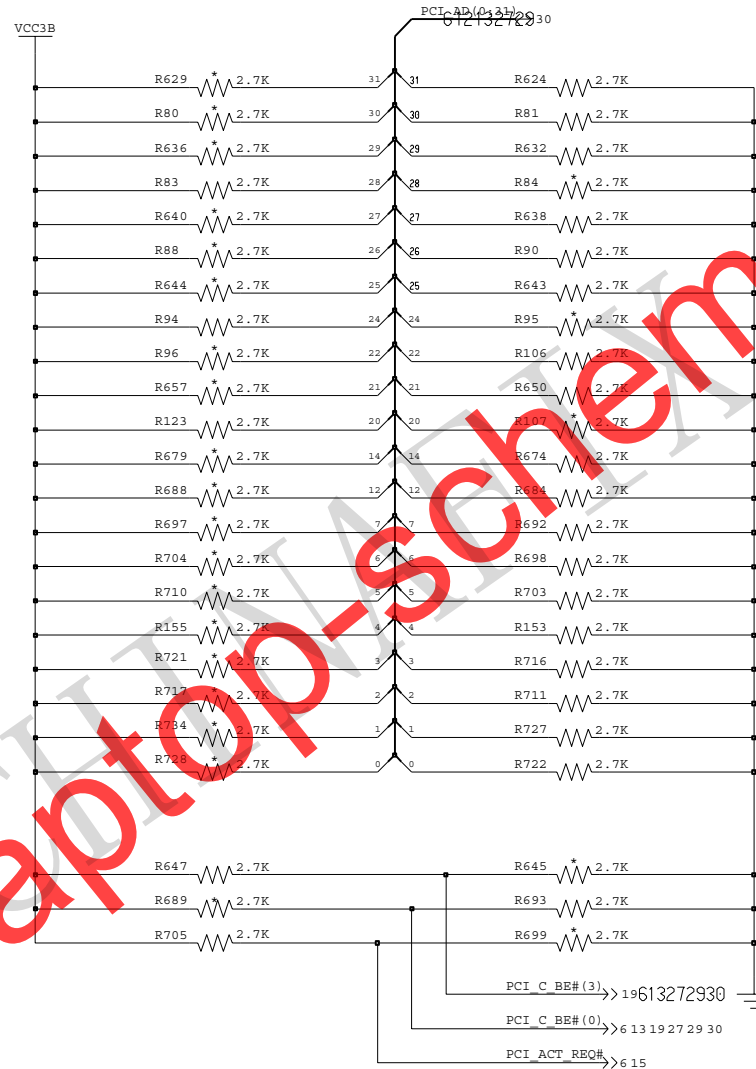








RS200M Strapping Options



AD(31:30) FSB Speed	
00	100 MHz
01	133 MHz
10	166 MHz
11	200 MHz

AD(31:30) FSB Clock Speed

AD29 : Strap Configuration
1: Reduced Set / 0: Full Set

AD28 : Enable Spread Spectrum
1: Enable SS / 0: Disable SS

AD27 : Disable MCERR# Observations
1: Disable / 0: Enable

AD26 : Disable Bus Parking
1: Disable / 0: Enable

AD25 : Disable BINIT# Observations
1: Disable / 0: Enable

AD24 : Enable IOQ Pipelining
1: IOQ=12 / 0: IOQ=1

AD22 : REF27 Function
1: 27MHz REF Input / 0: PCICLK5 Output

AD21 : Clock Bypass
1: Test Mode / 0: Normal Mode

AD20 : PCI Clock Expansion (REQ3# & GNT3#)
1: PCICLK3 & PCICLK4 / 0: REQ & GNT Pair

AD14 : P4 Voltage Detection
1: 1.7V DT CPU / 0: 1.2V NT CPU

AD12 : Flat Panel ID4
FP_ID4

AD11 : Flat Panel ID3
FP_ID3

AD10 : Flat Panel ID2
FP_ID2

AD5 : Flat Panel ID1
FP_ID1

AD4 : Flat Panel ID0
FP_ID0

AD3 : A-Link Enable
1: A-Link / 0: PCI-33

AD2 : Auto Calibration Enable
1: Disable / 0: Enable

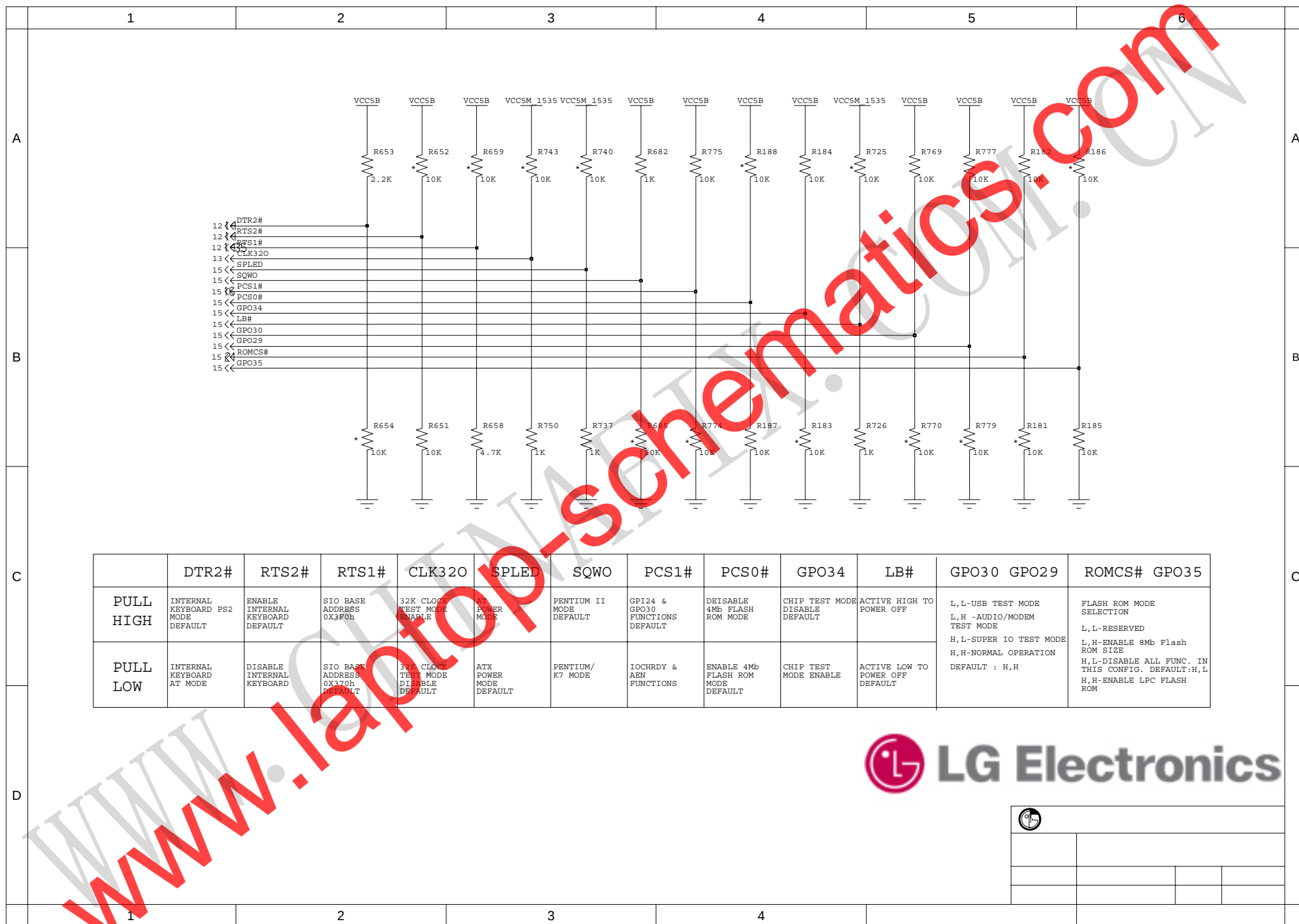
AD1 : CPU Reset Forced to Be Shortened
1: Test Mode / 0: Normal Mode

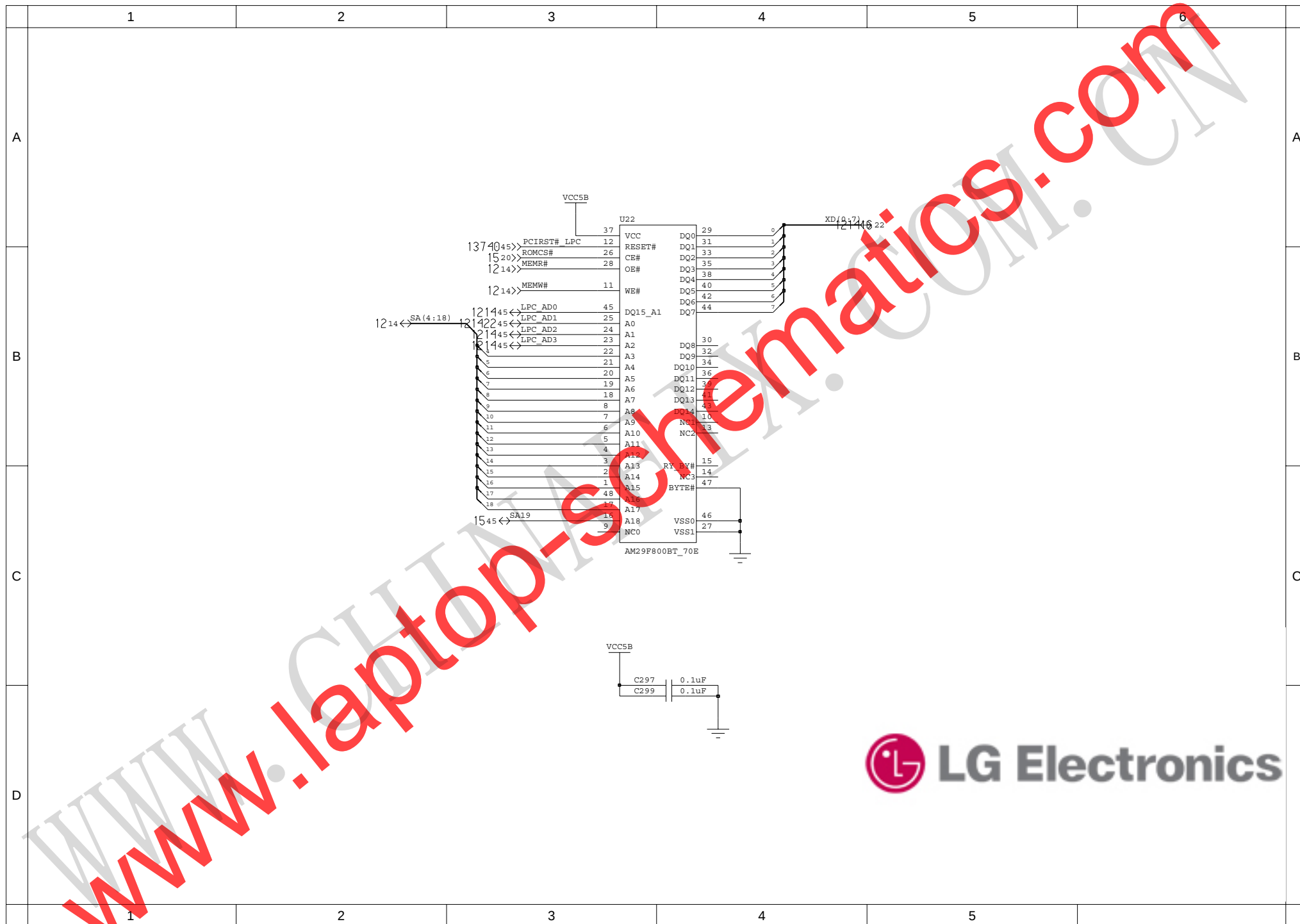
AD0 : Default CFG for GC Enable bit & AGPCLKOUT
1: '0' & 66MHz AGP / 0: '0' & 33MHz PCI

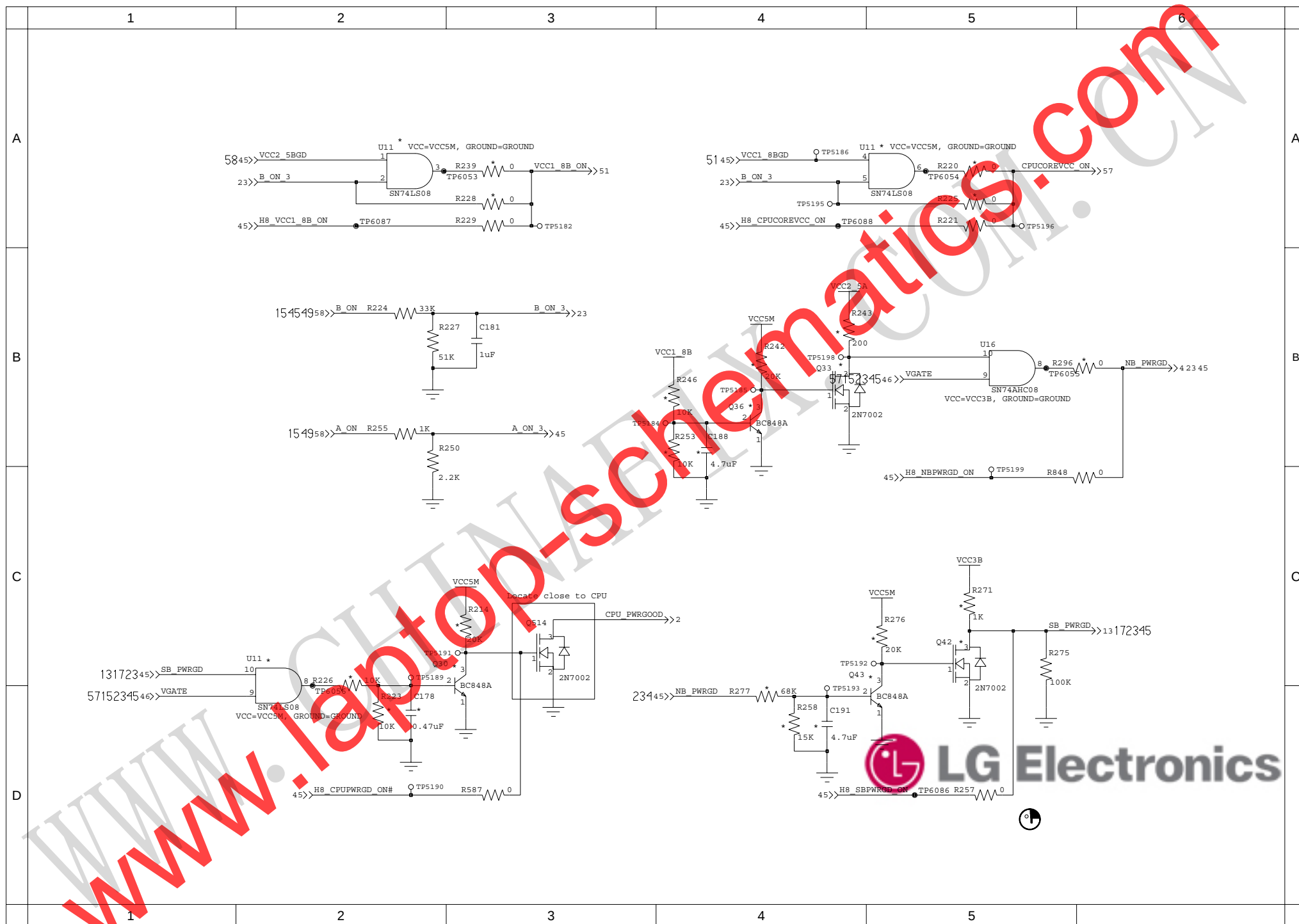
PCI_CBE3# : Production Test
1: Normal / 0: Production Test

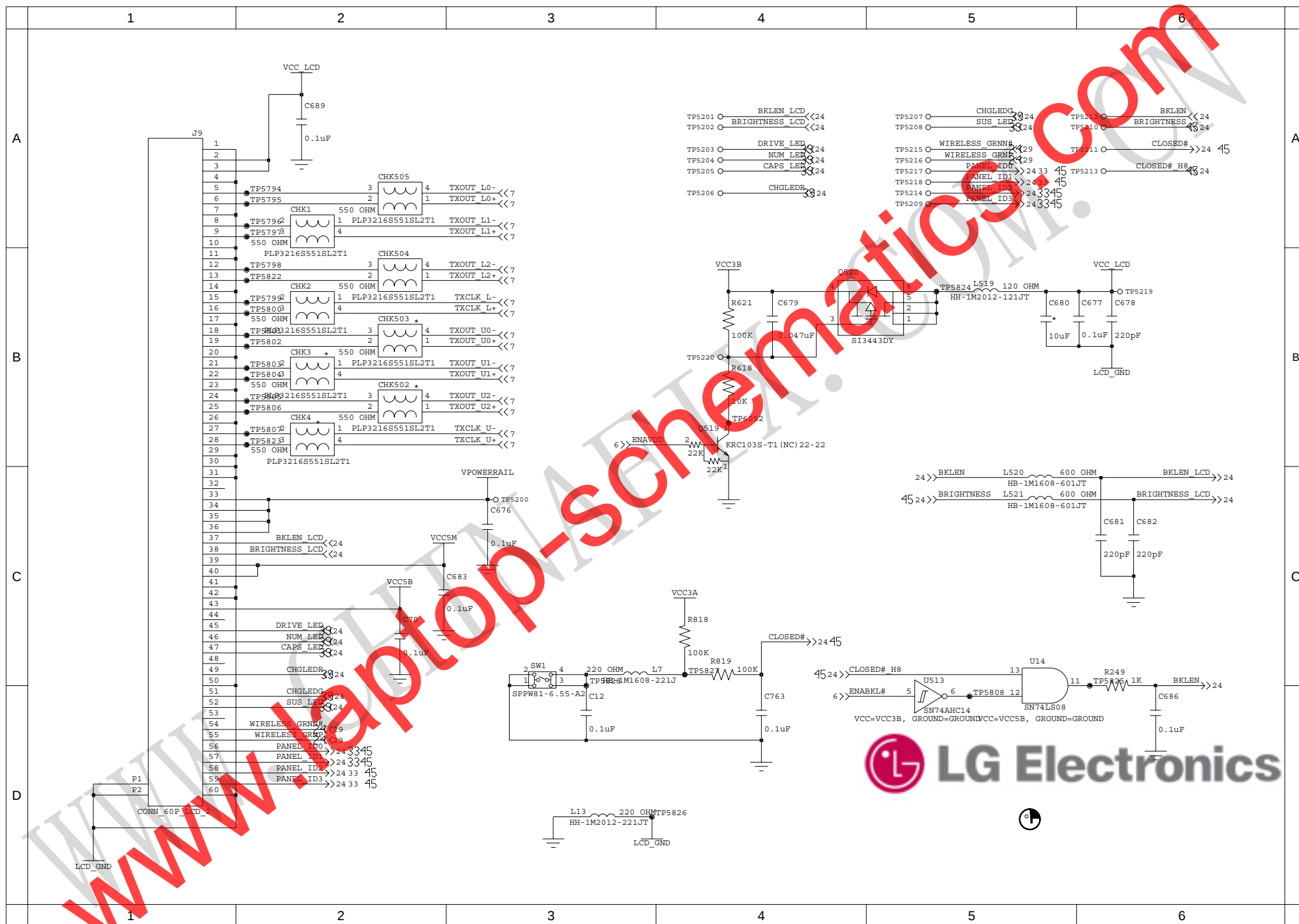
PCI_CBE0# : Reserved
Set to 0 (only for A11,A12, A13)

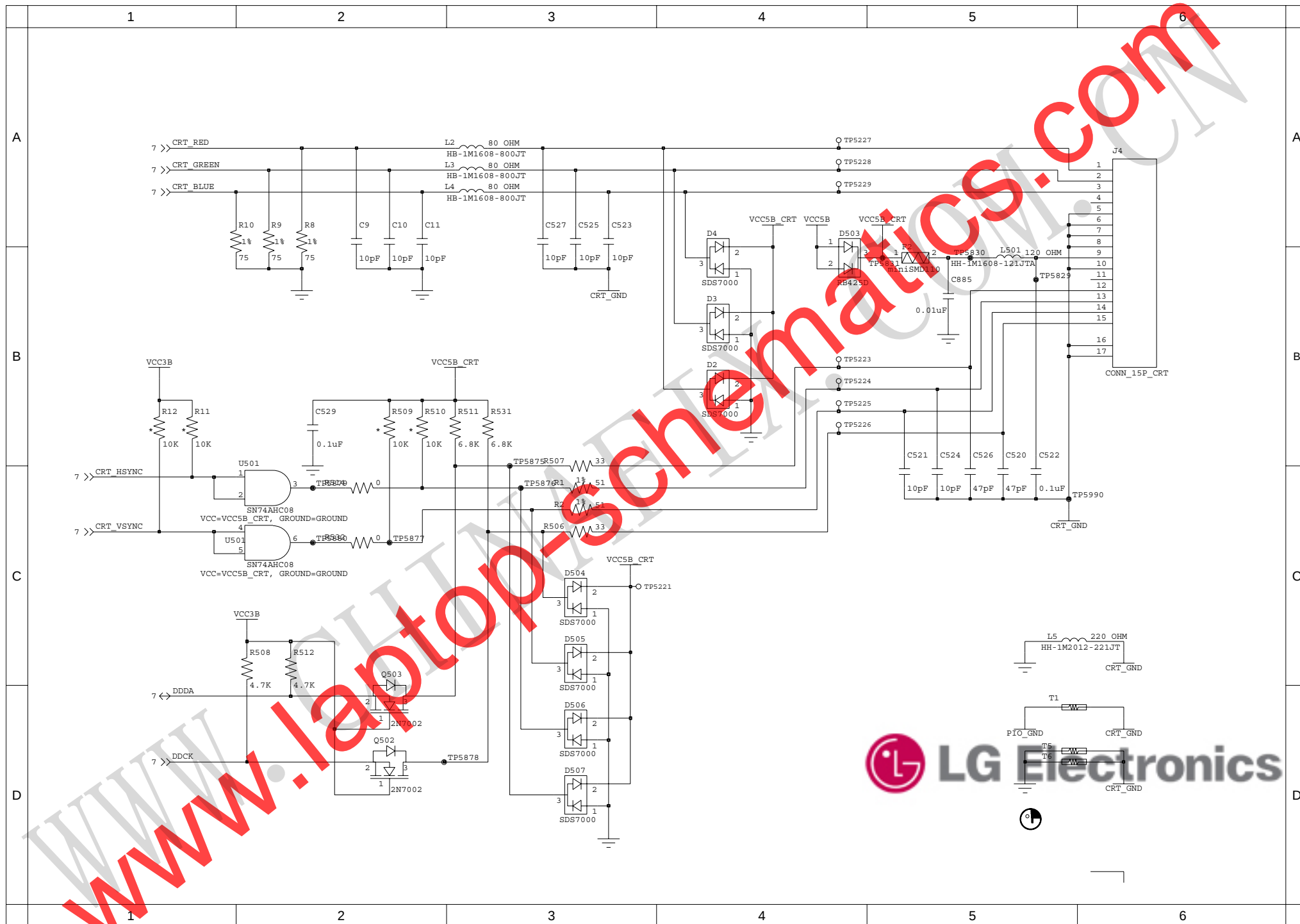
PCI_ACT_REQ# : Internal Clock Generator Enable
1: Int. Clock / 0: Ext. Clock

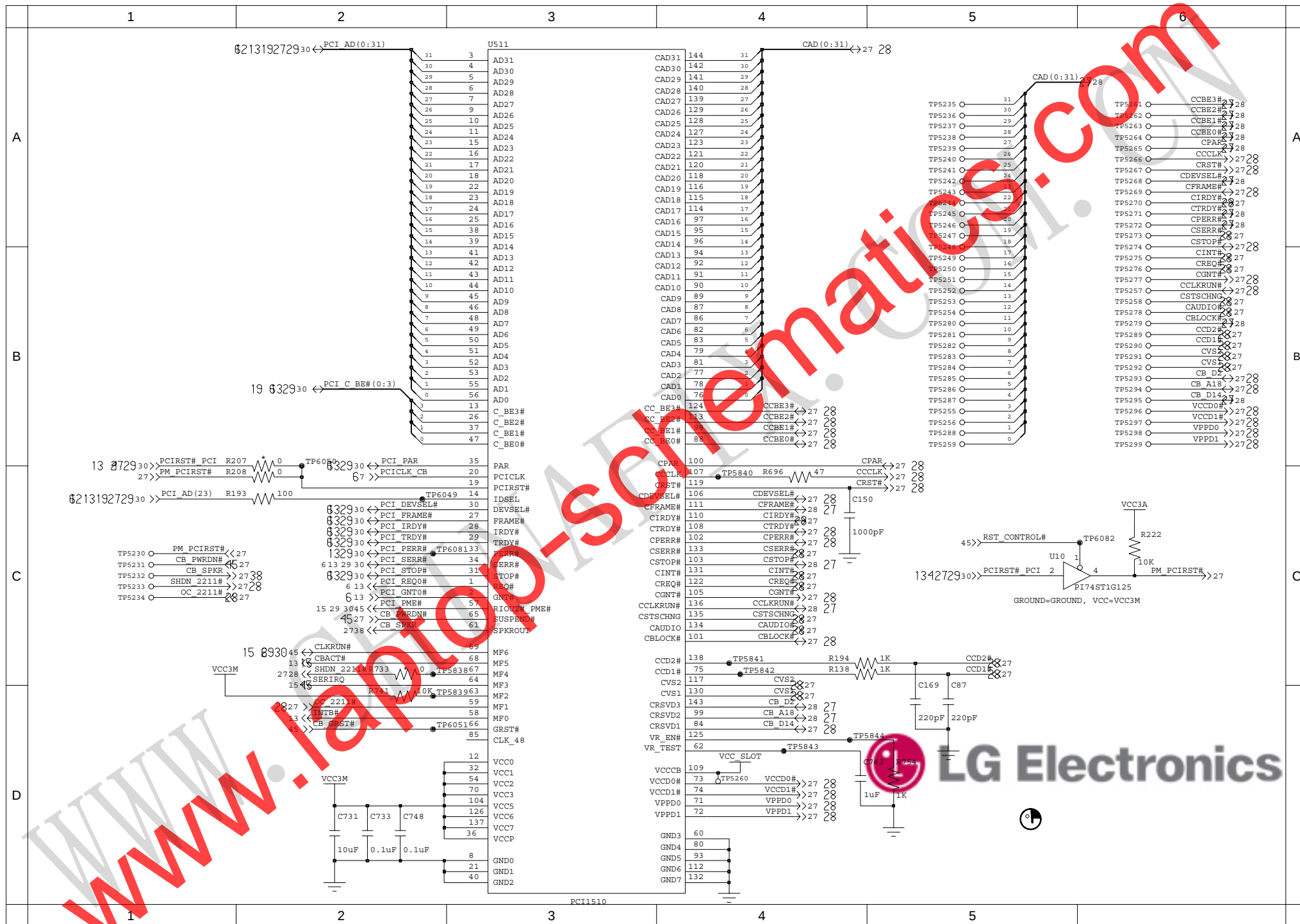


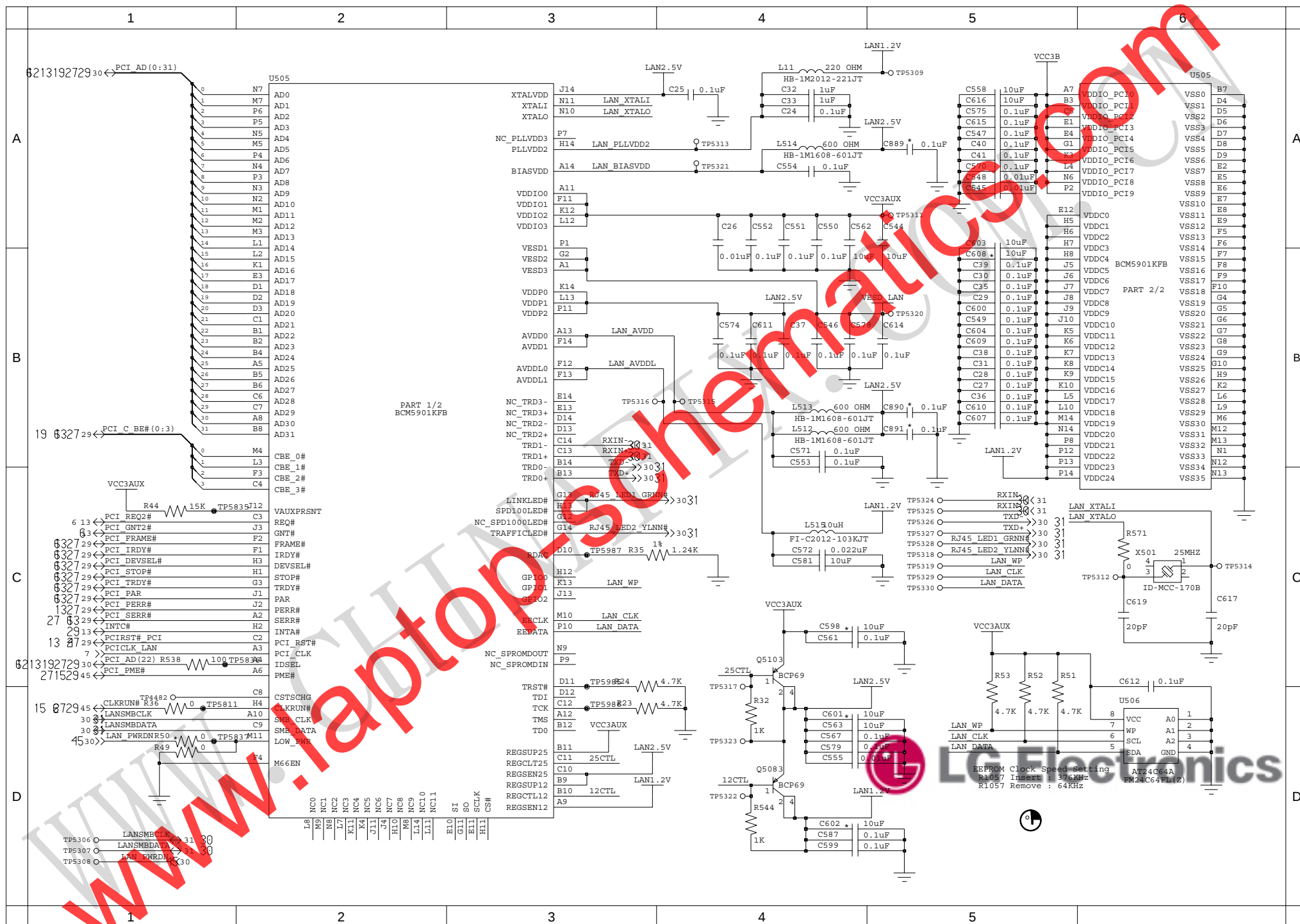


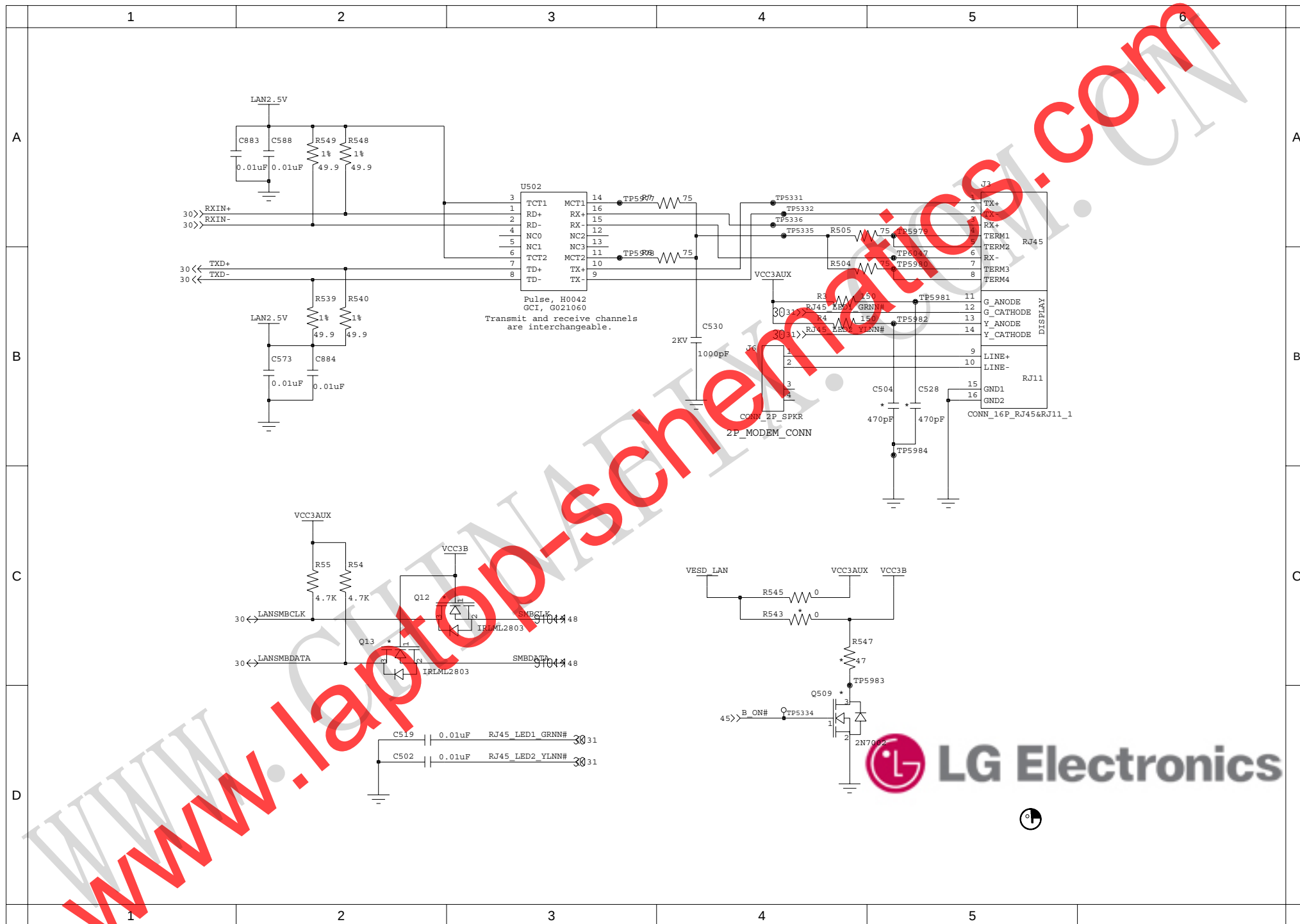


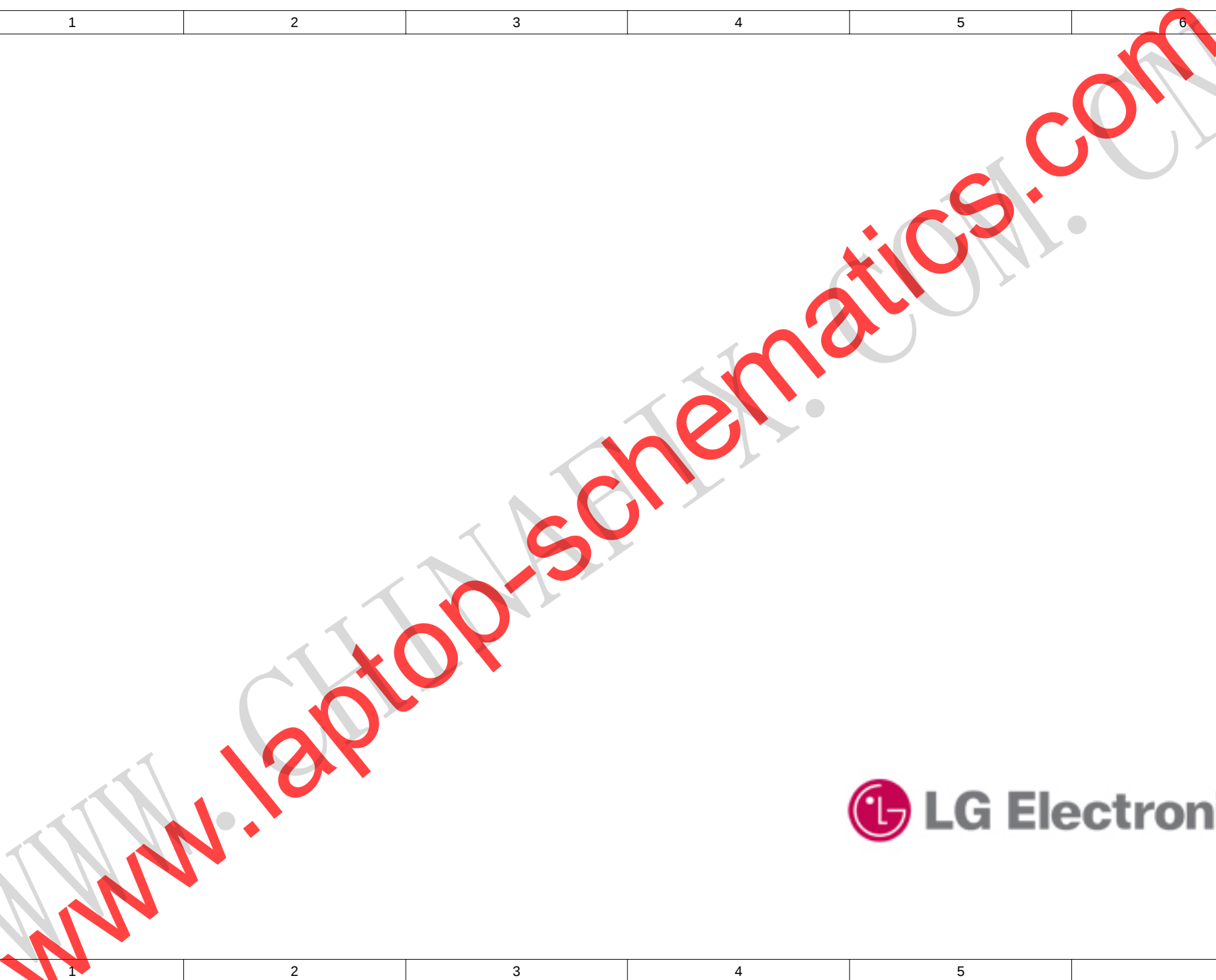


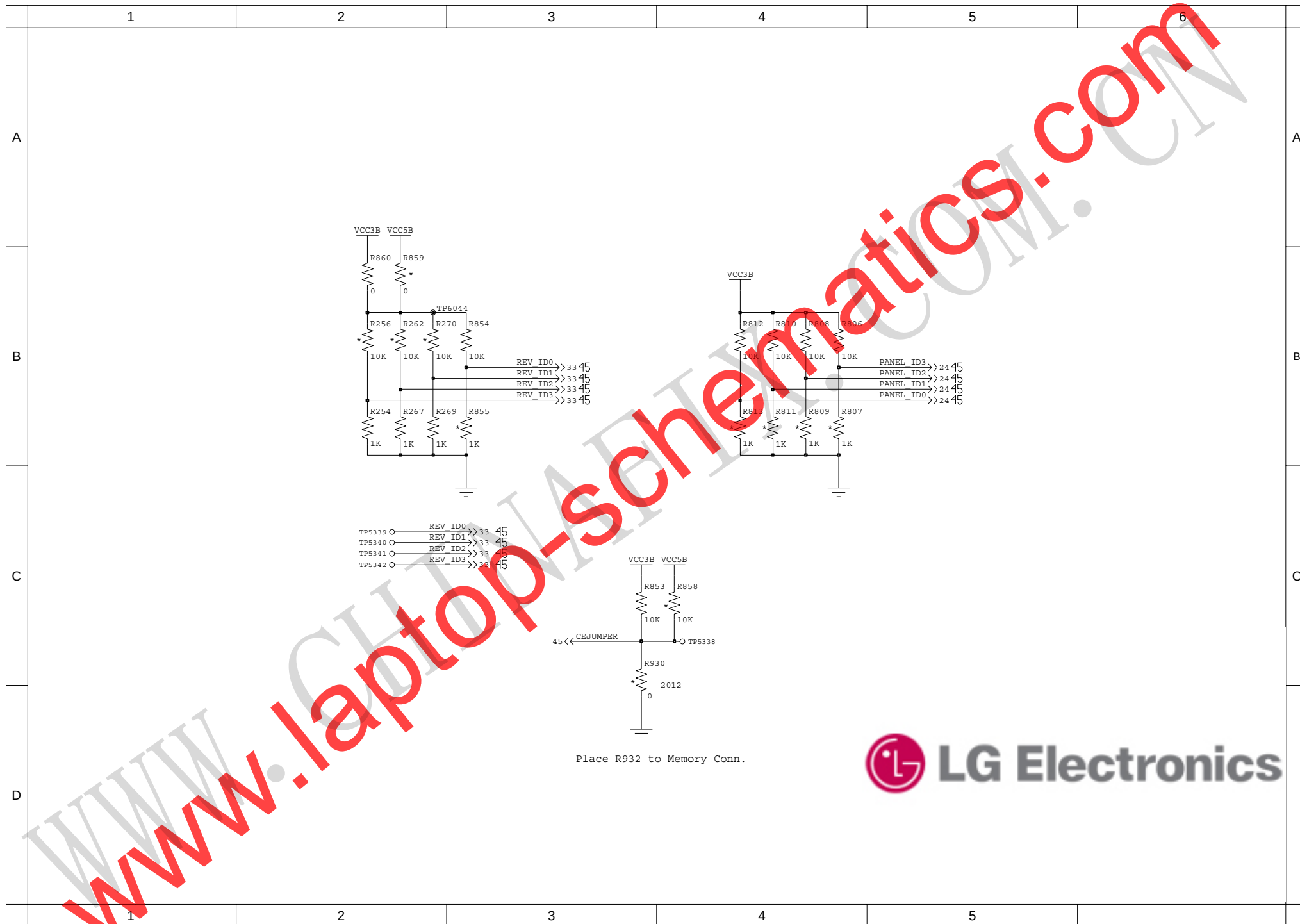


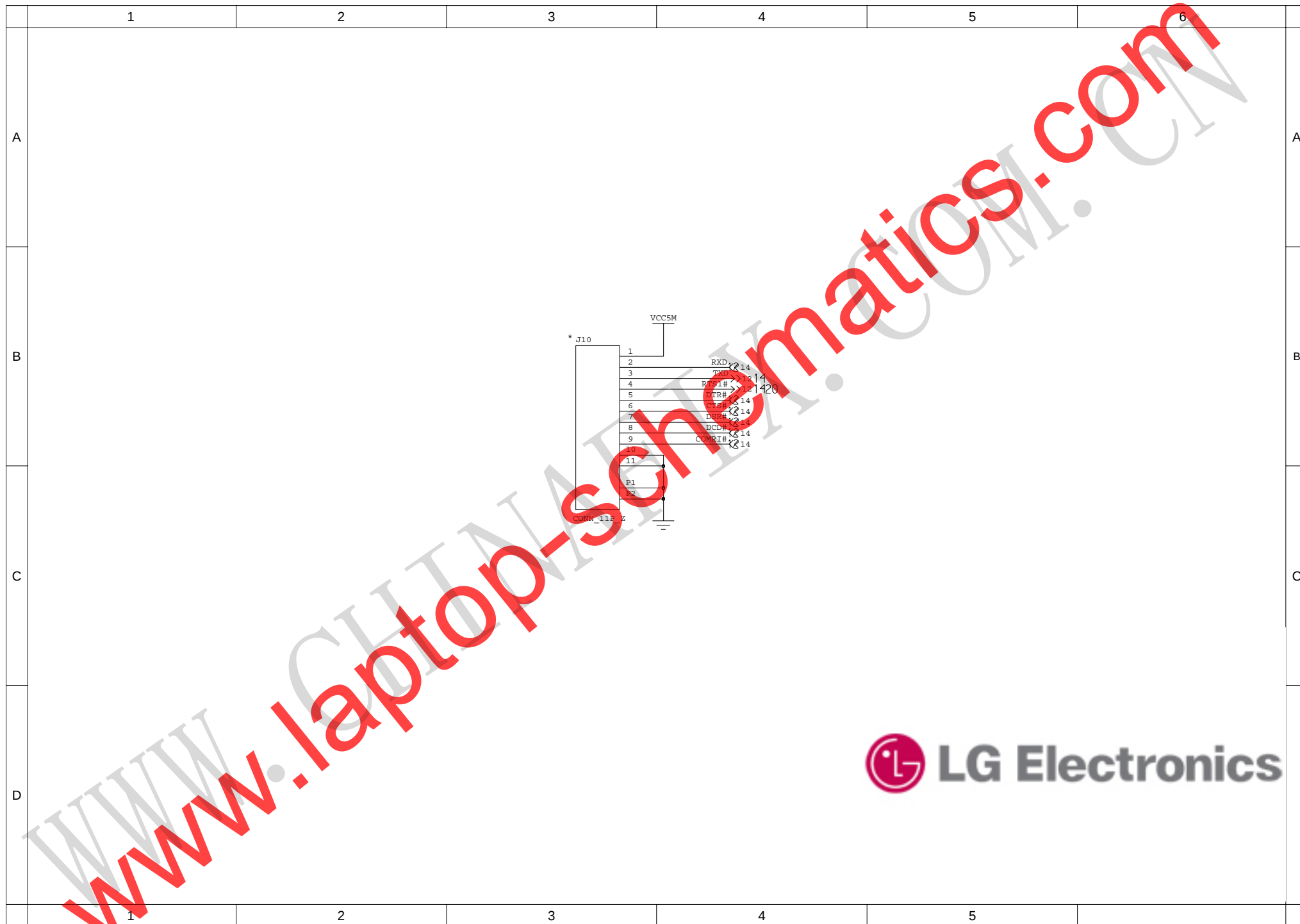


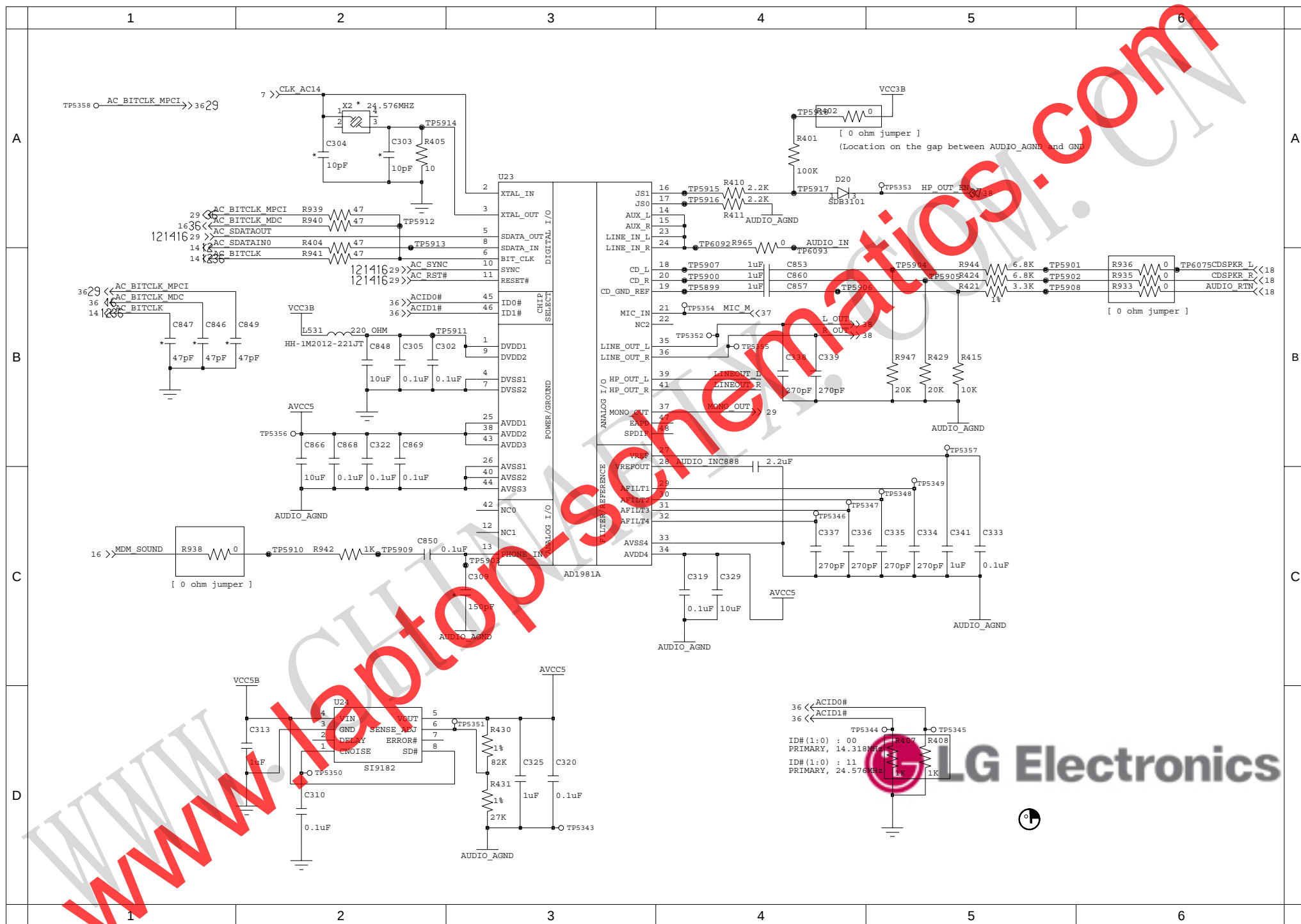


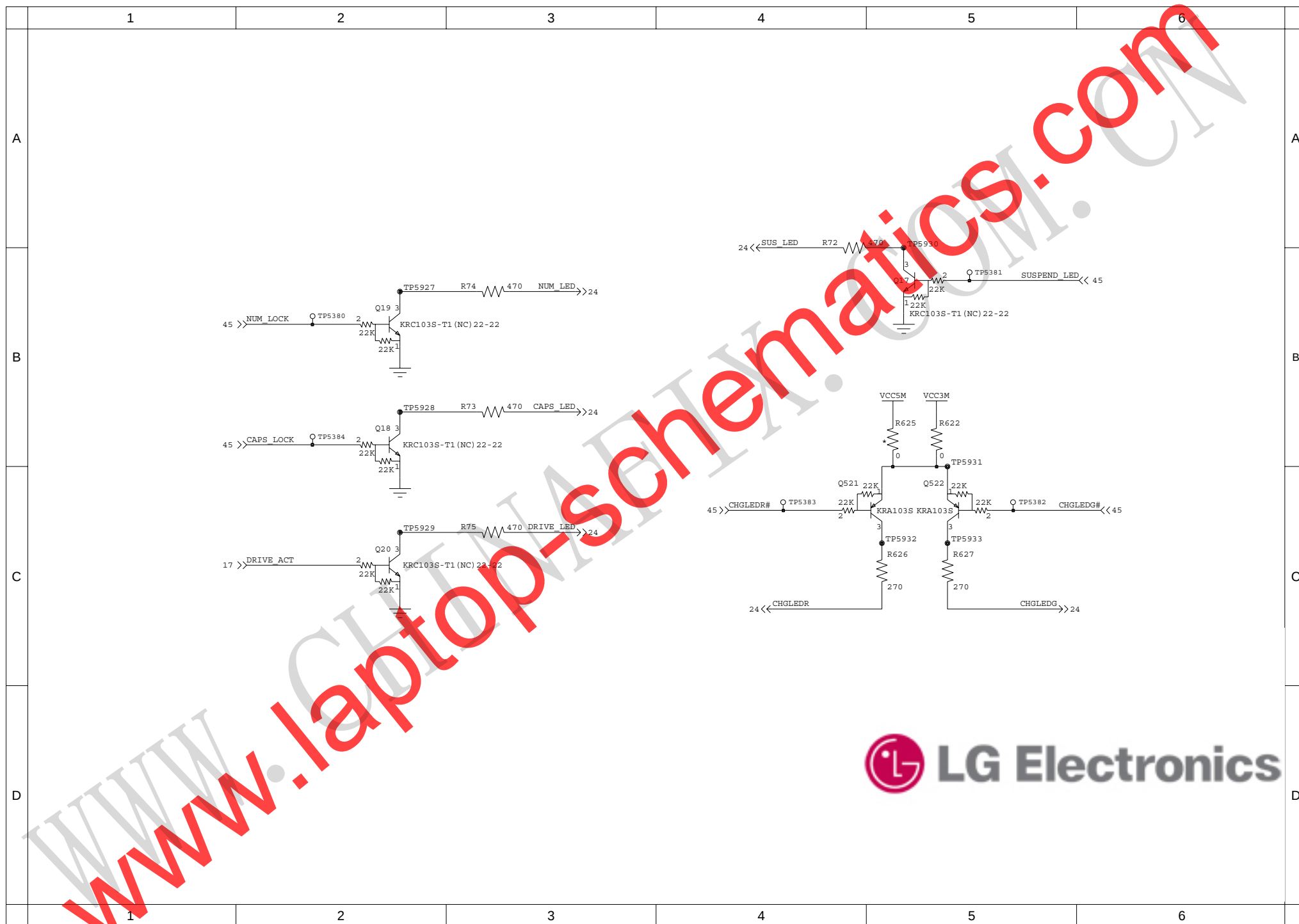


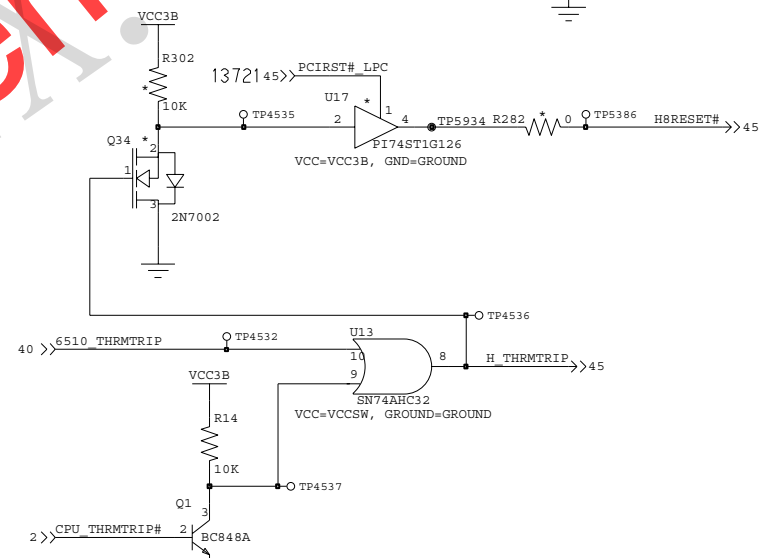
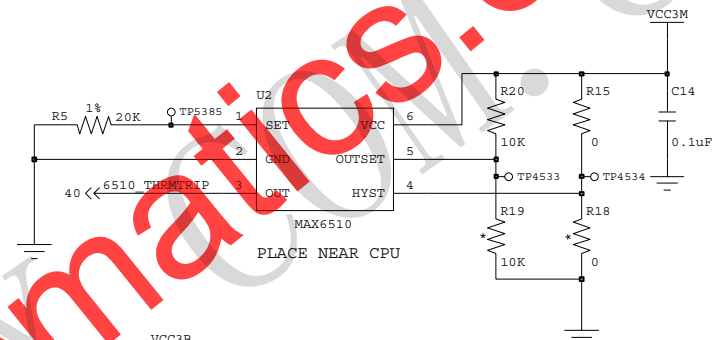
	1	2	3	4	5	6	
A							A
B							B
C							C
D							D
	1	2	3	4	5		

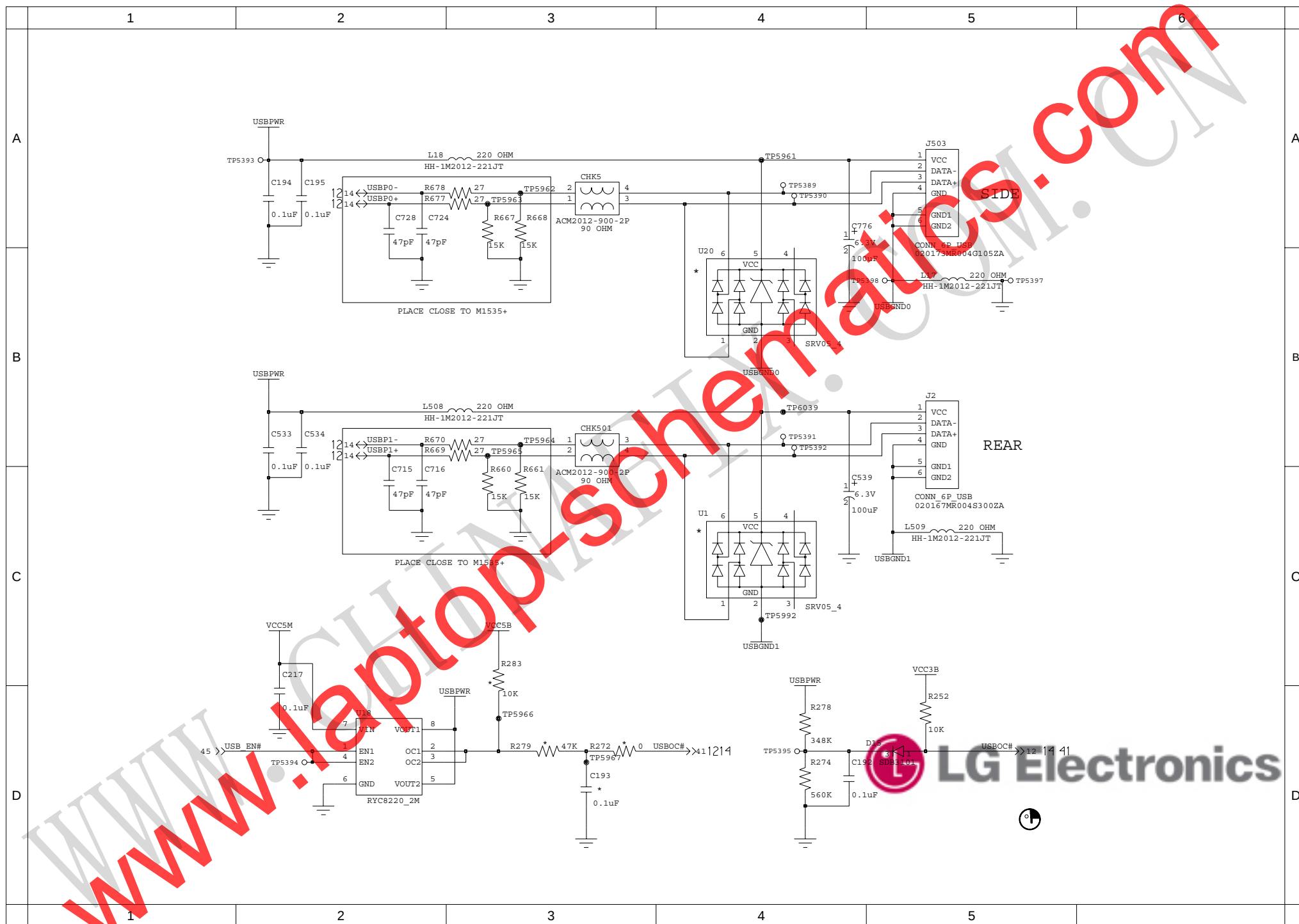


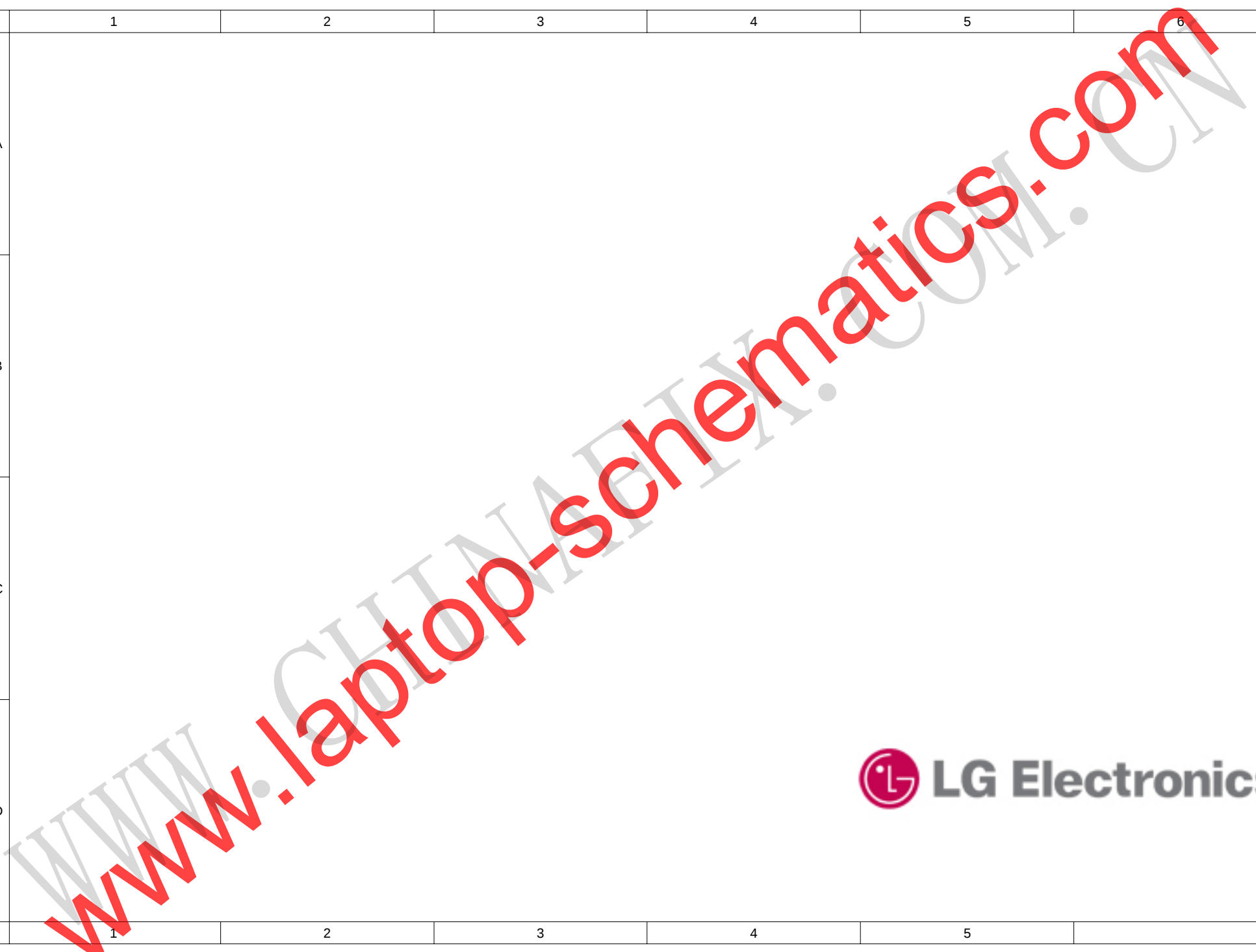


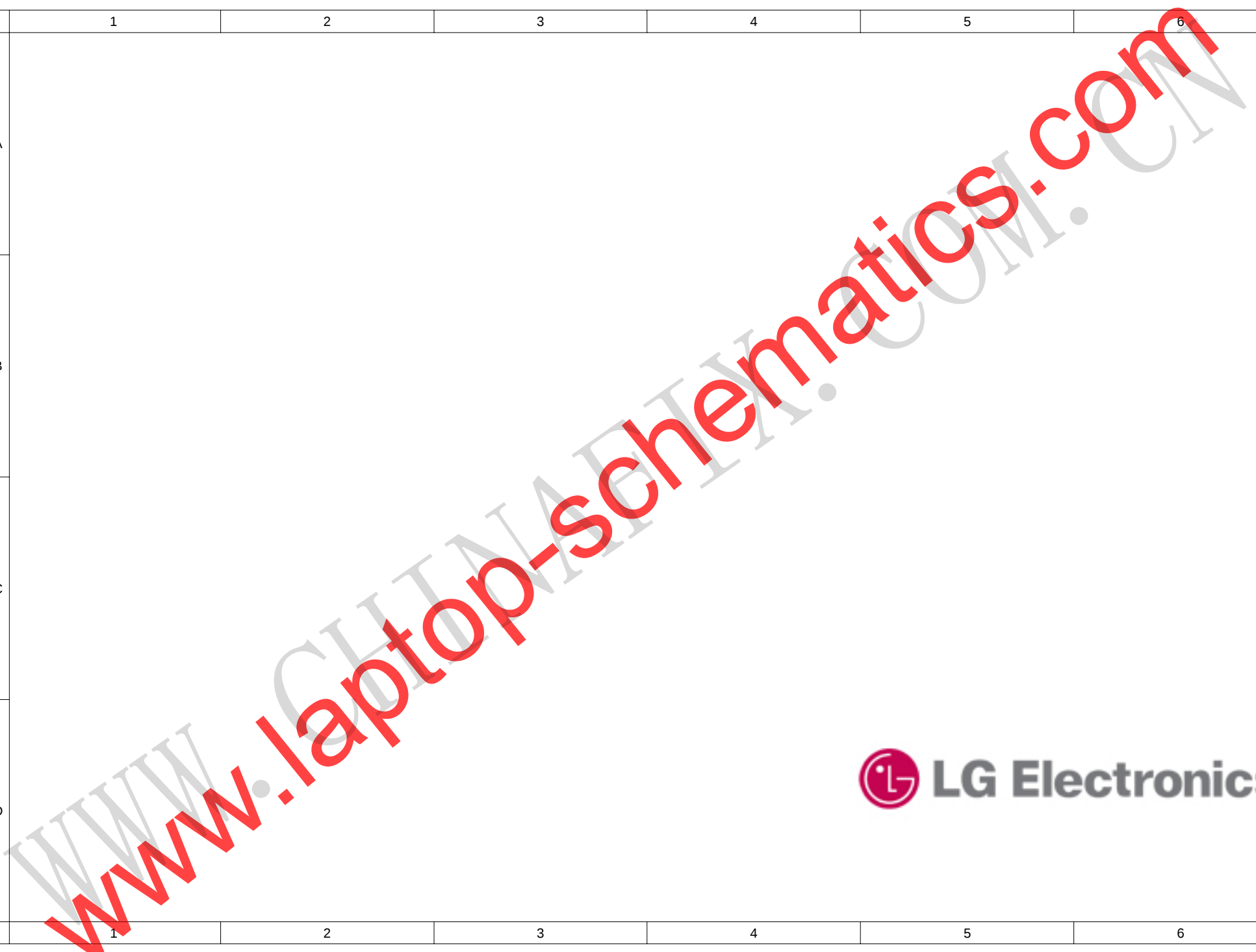


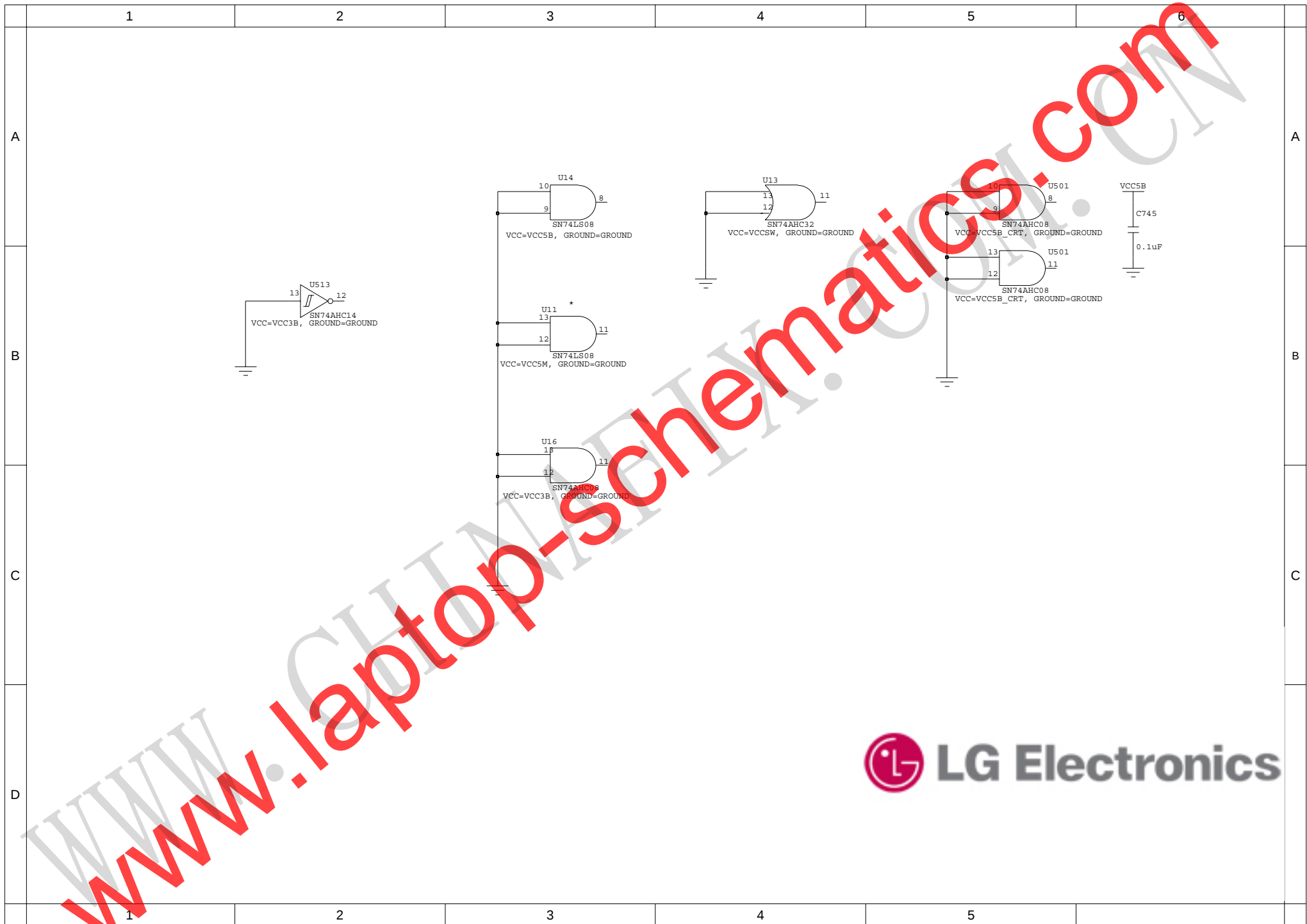


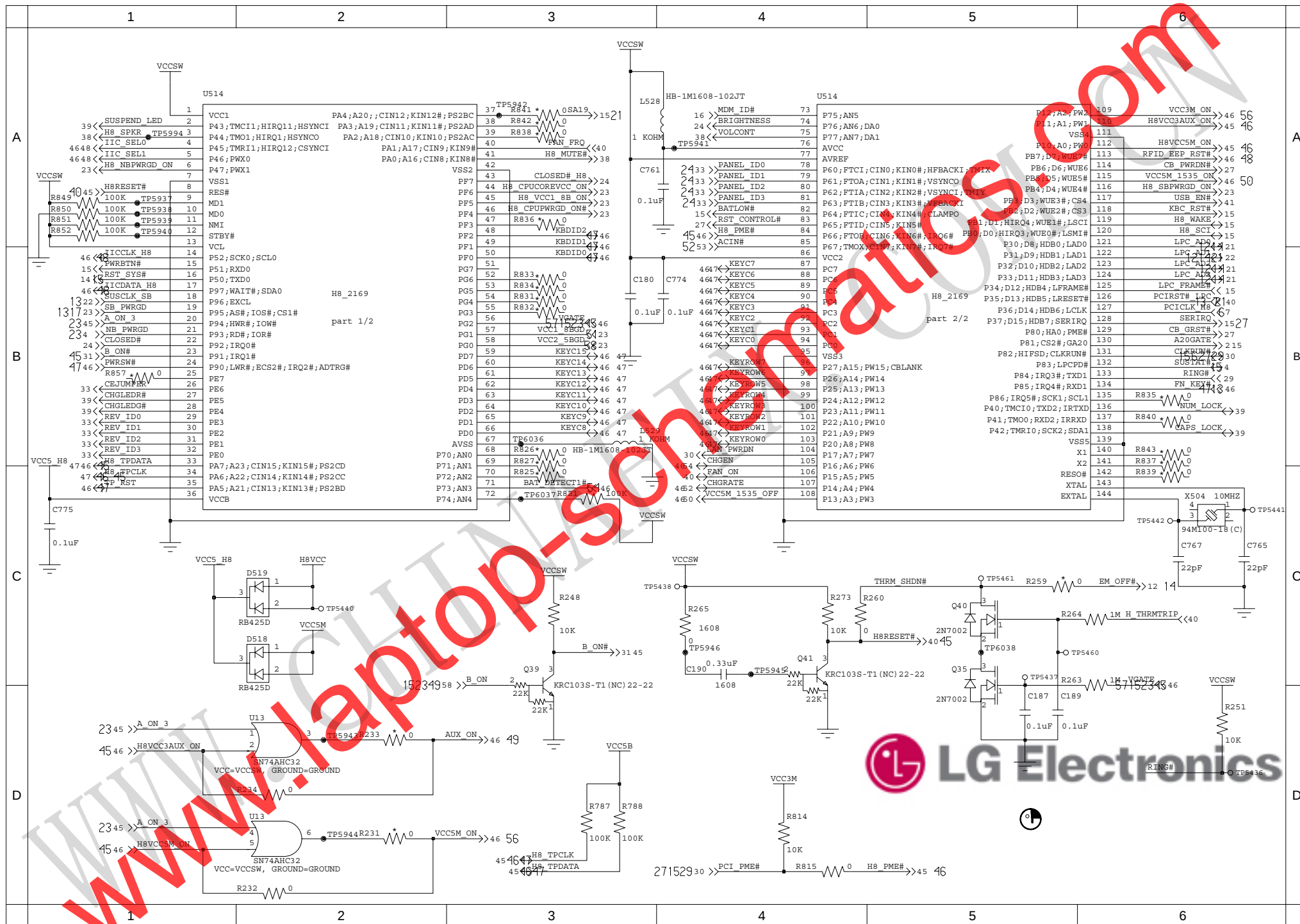


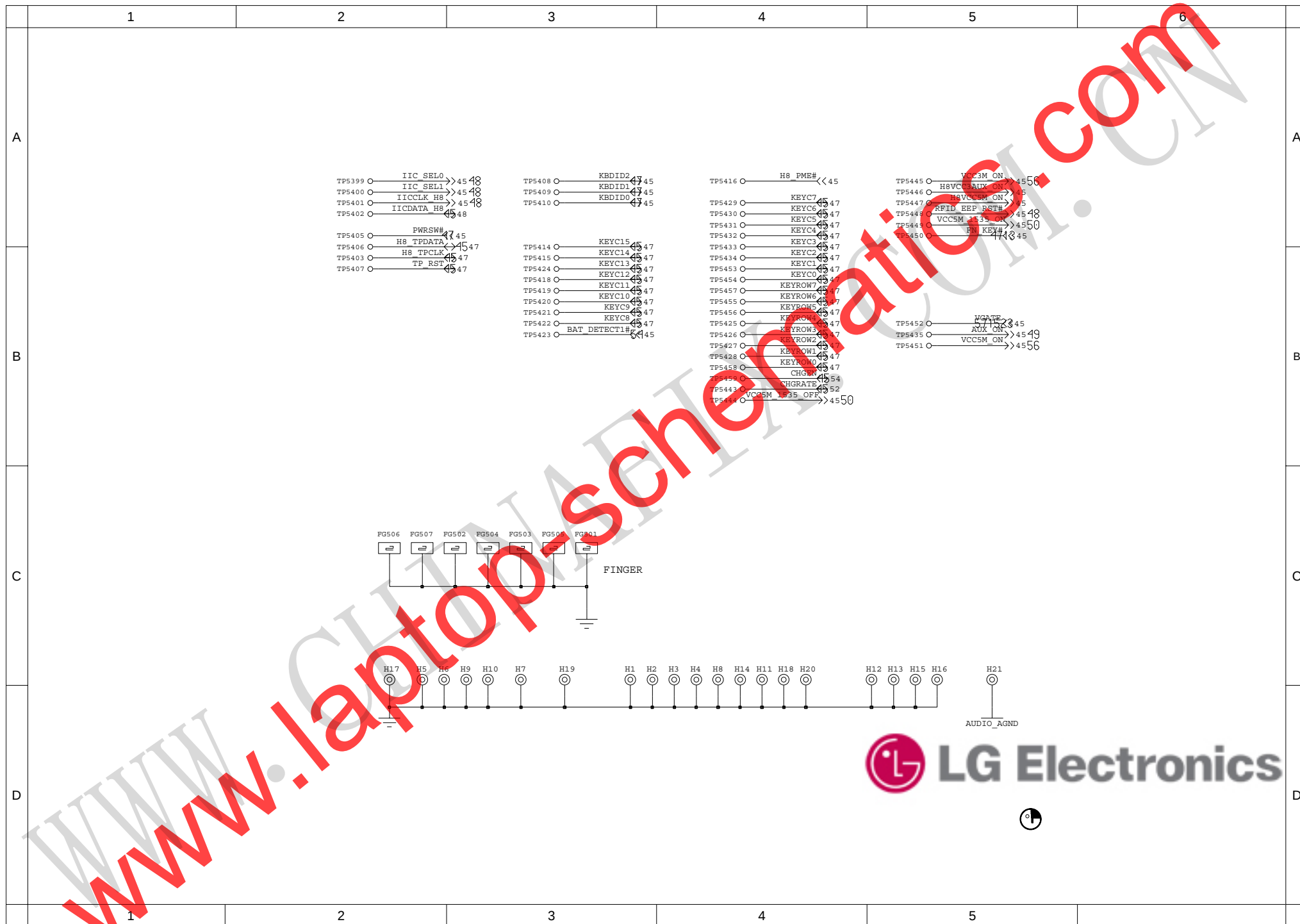


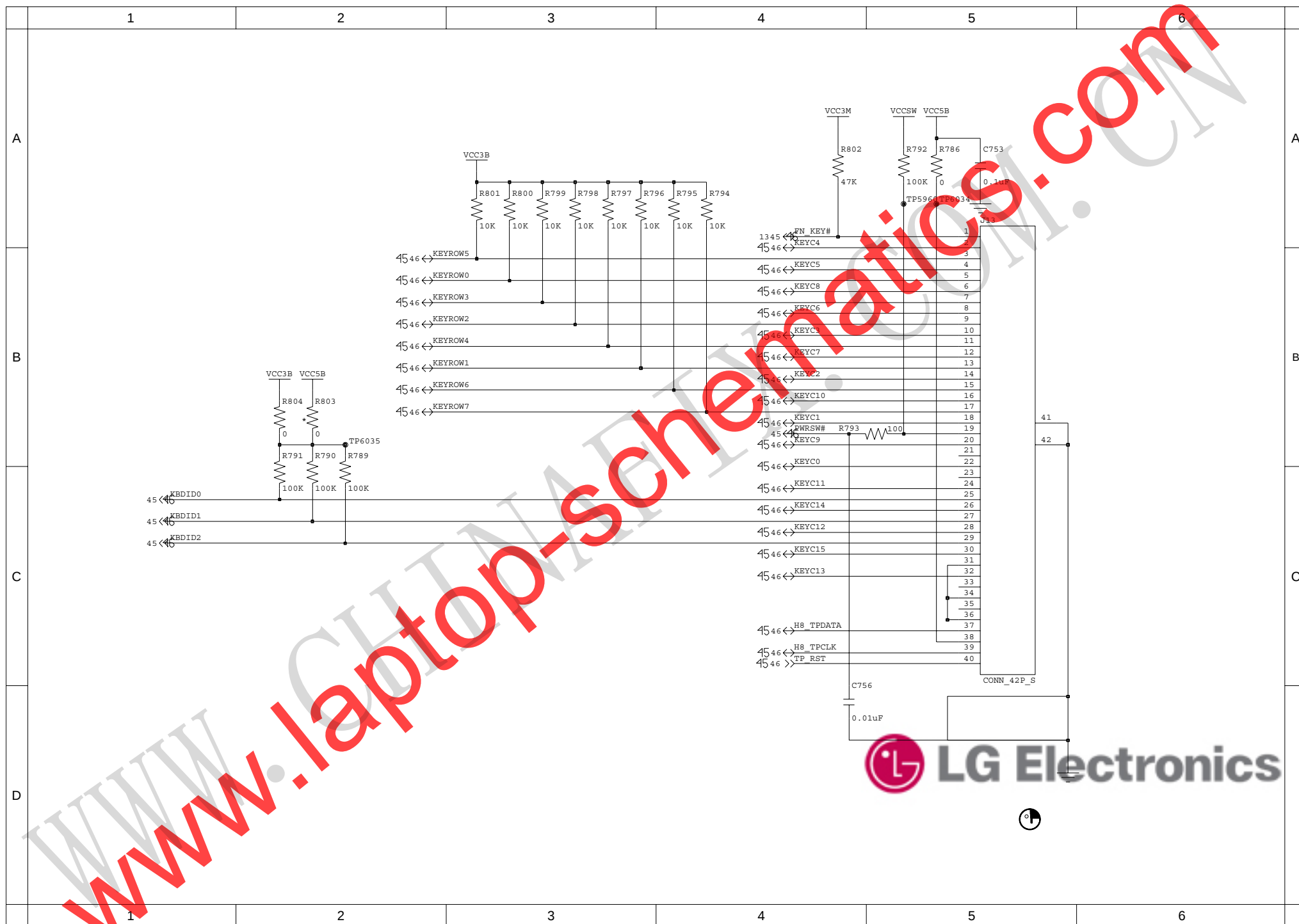
	1	2	3	4	5	6	
A							A
B							B
C							C
D							D
	1	2	3	4	5		

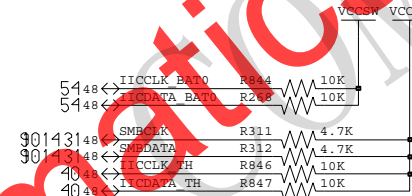
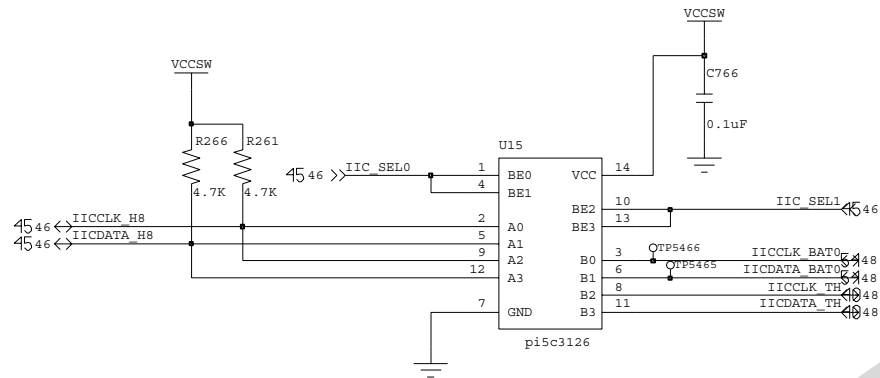
	1	2	3	4	5	6	
A							A
B							B
C							C
D							D
	1	2	3	4	5	6	



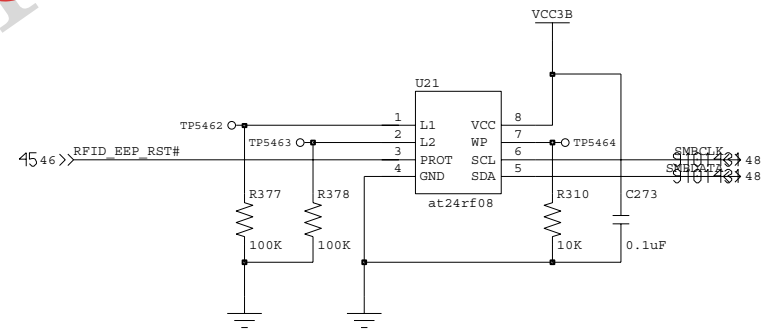


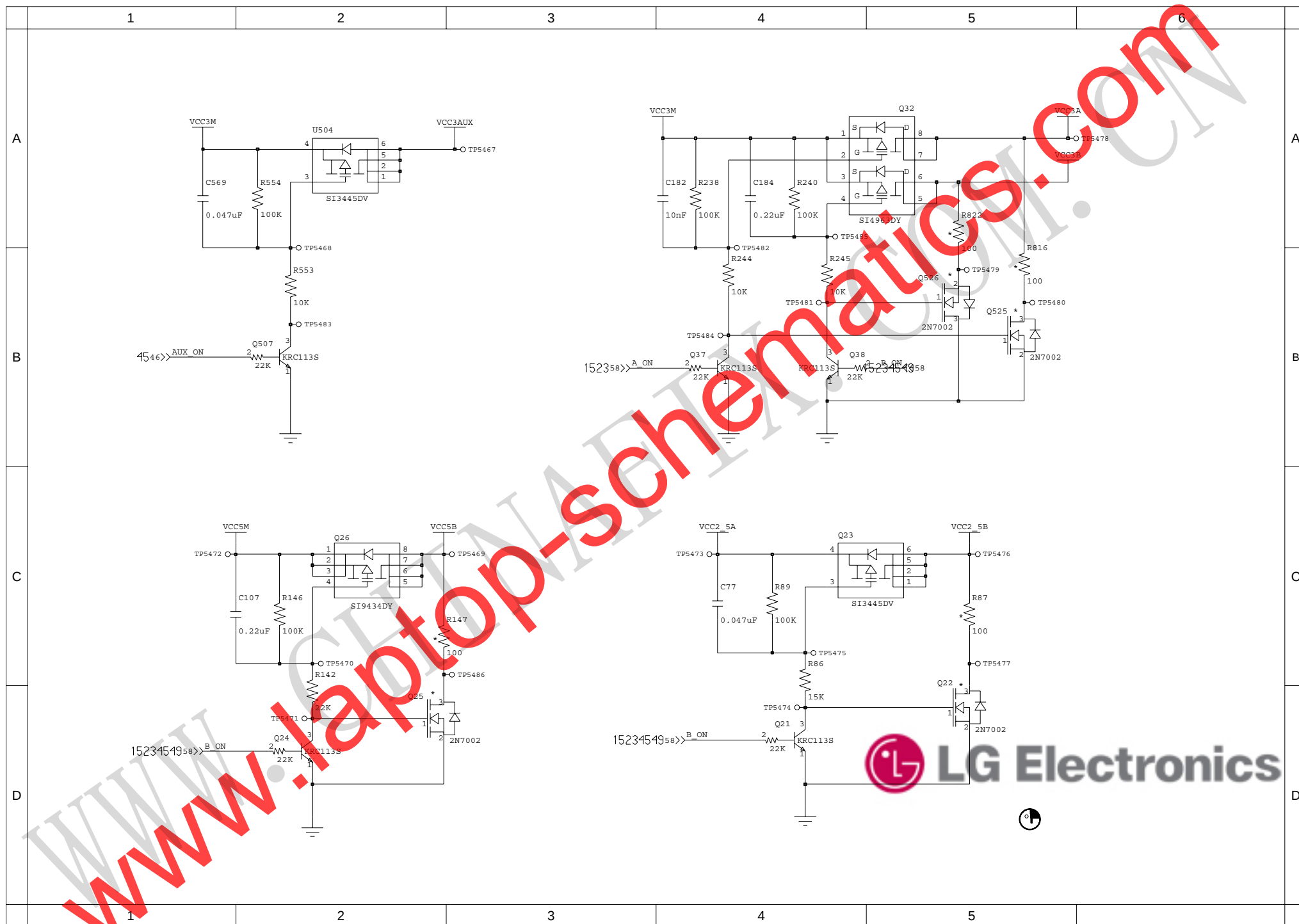


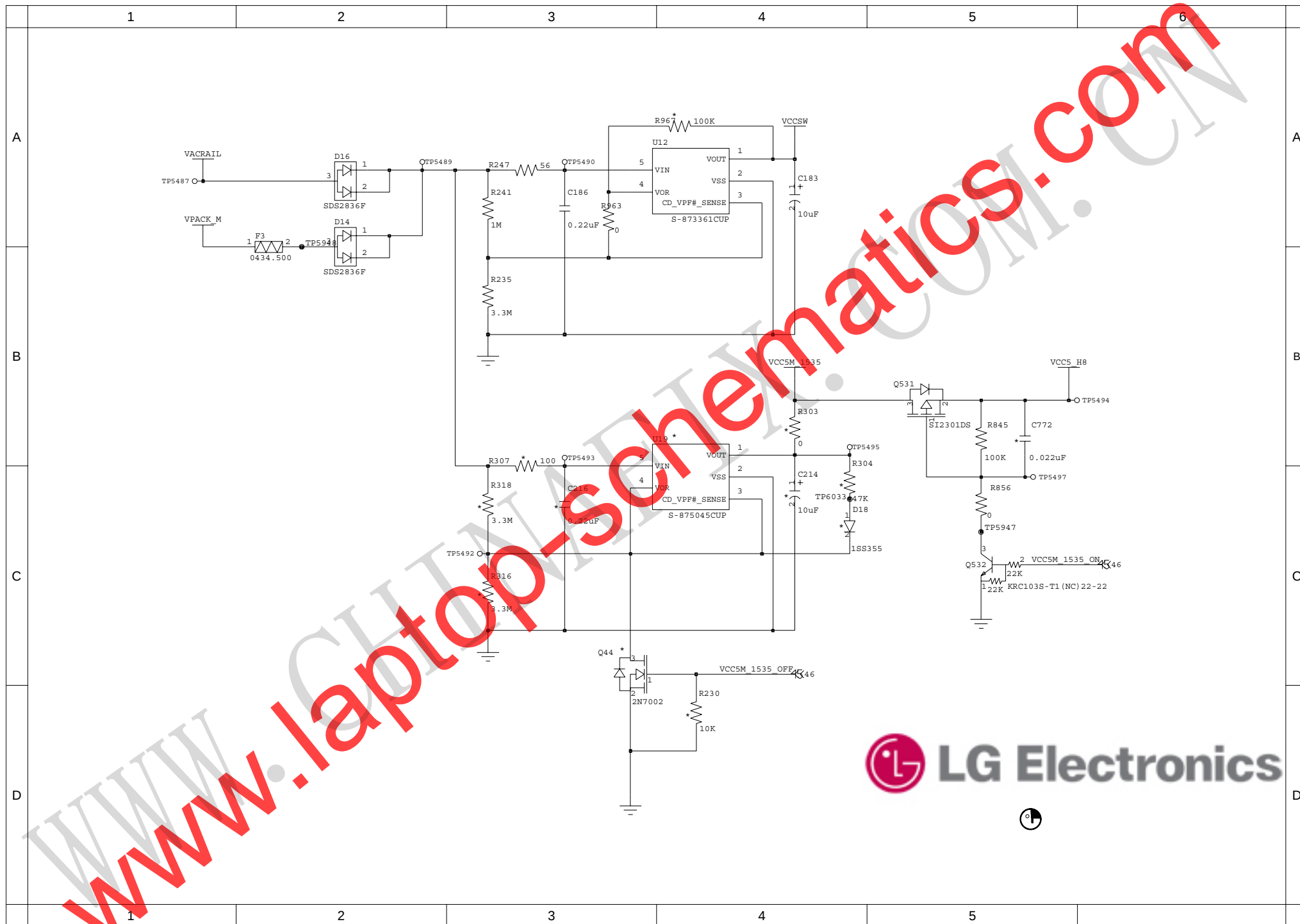


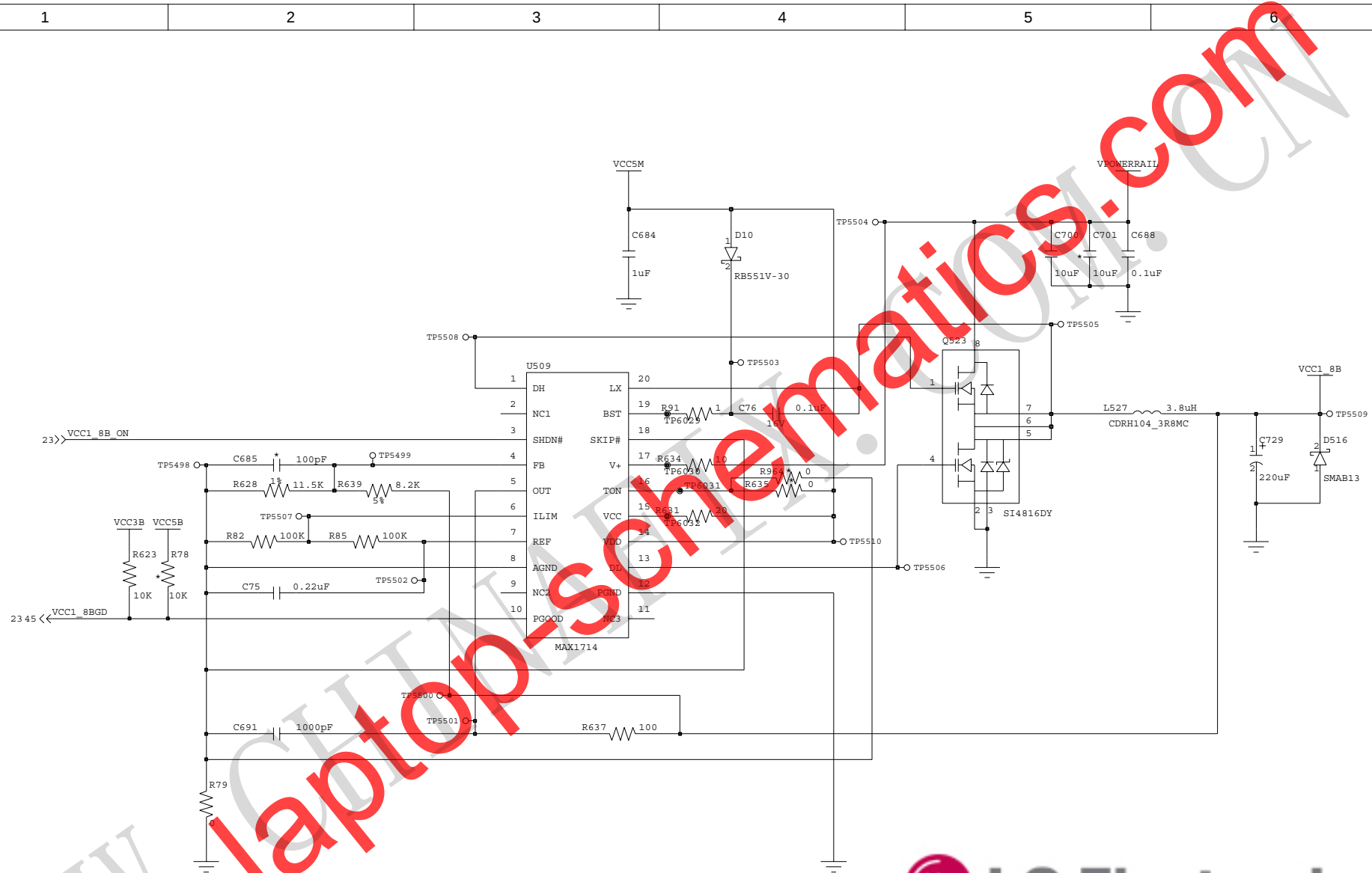


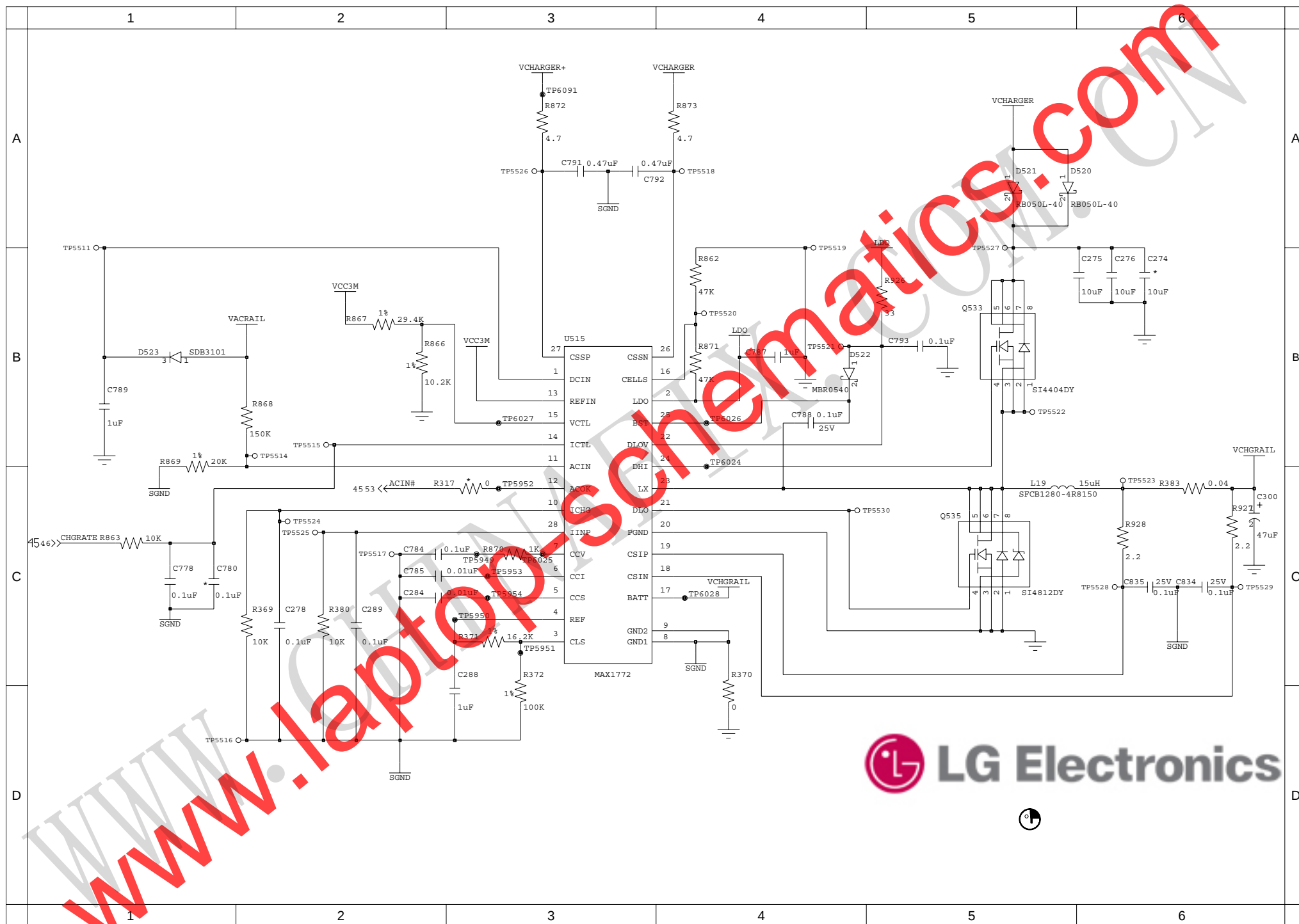
SEL0	SEL1	IICCLK_H8	IICDATA_H8
LOW	LOW	ISOLATE	ISOLATE
HIGH	LOW	IICCLK_BAT0	IICDATA_BAT0
LOW	HIGH	IICCLK_TH	IICDATA_TH

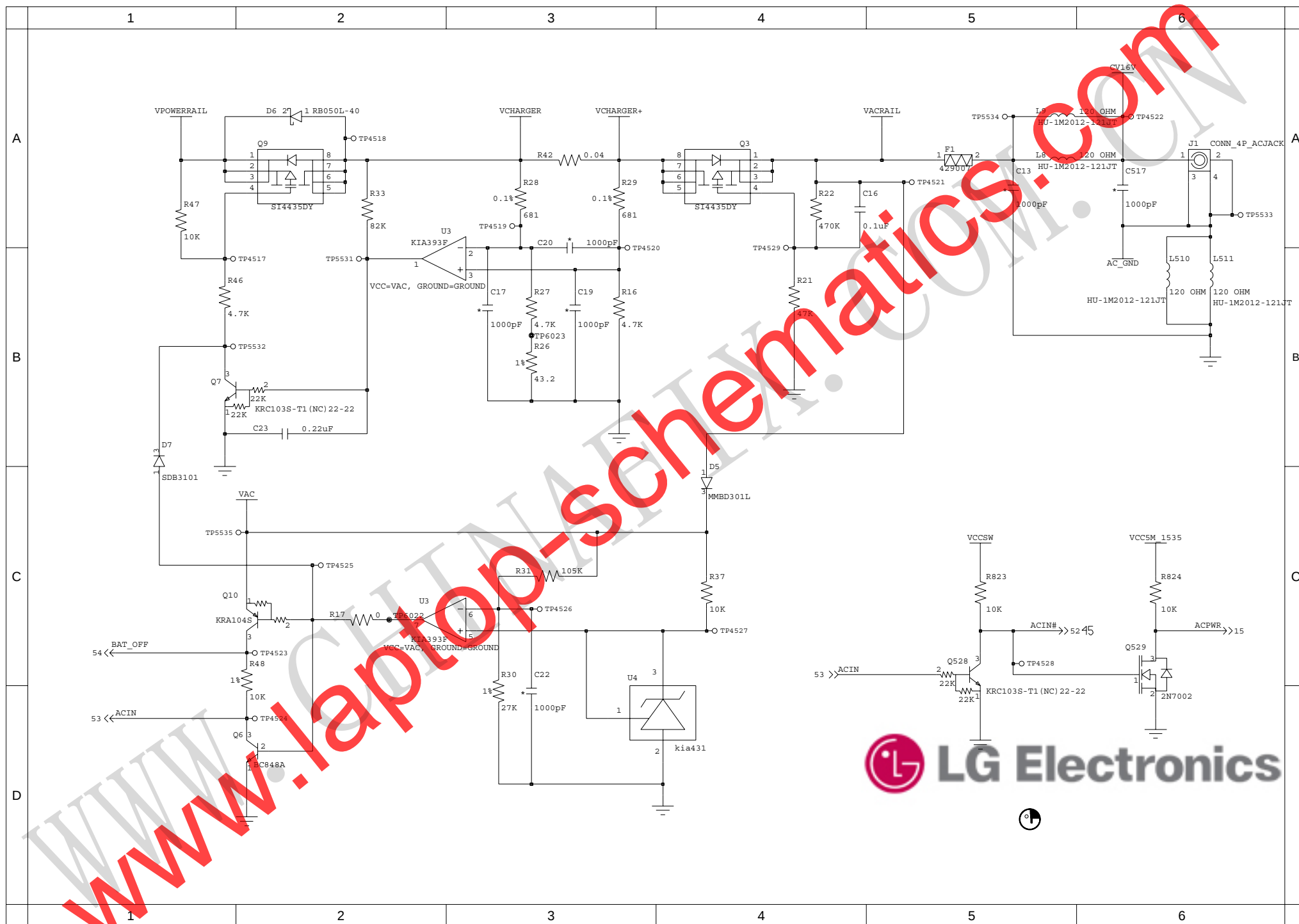


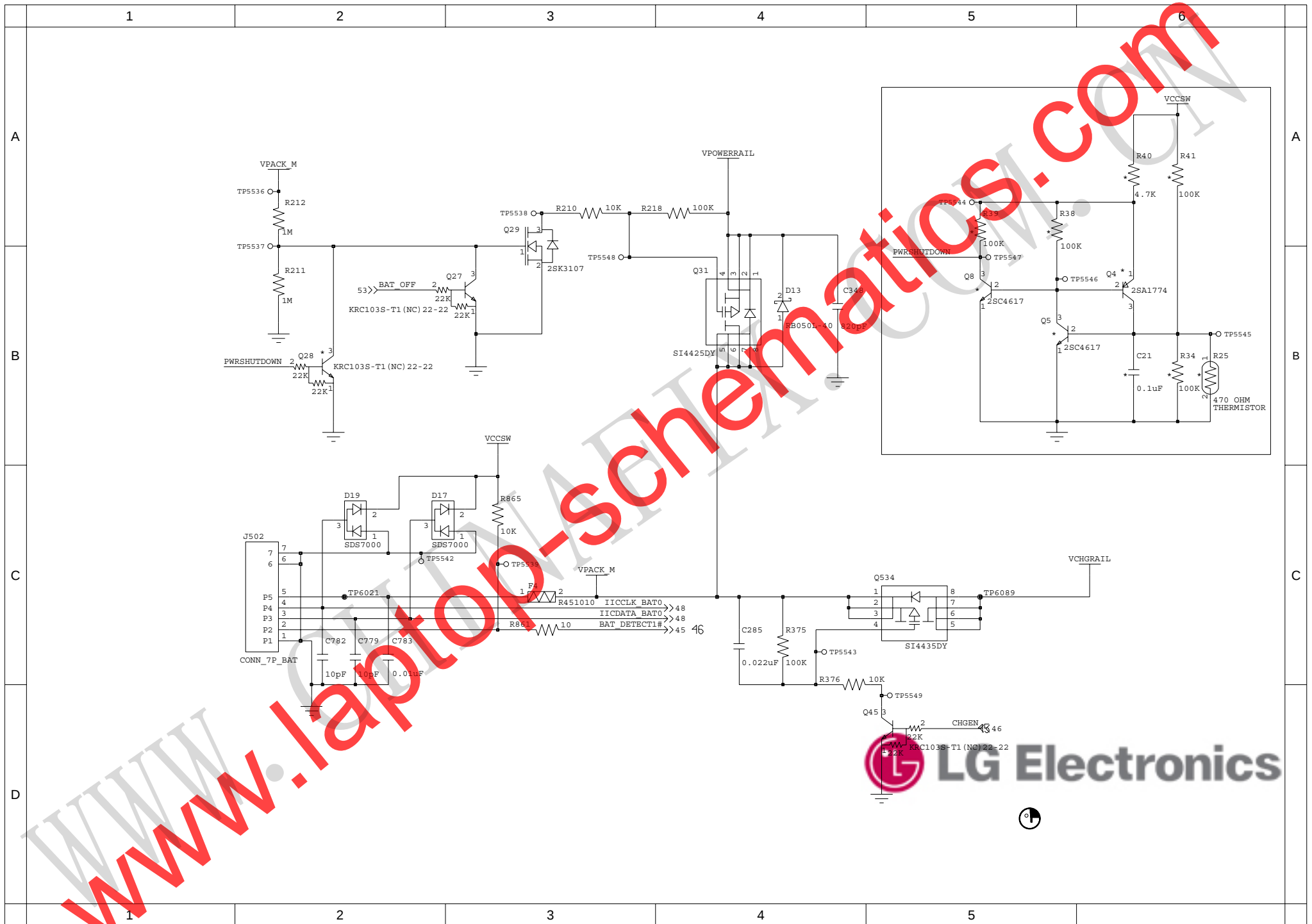


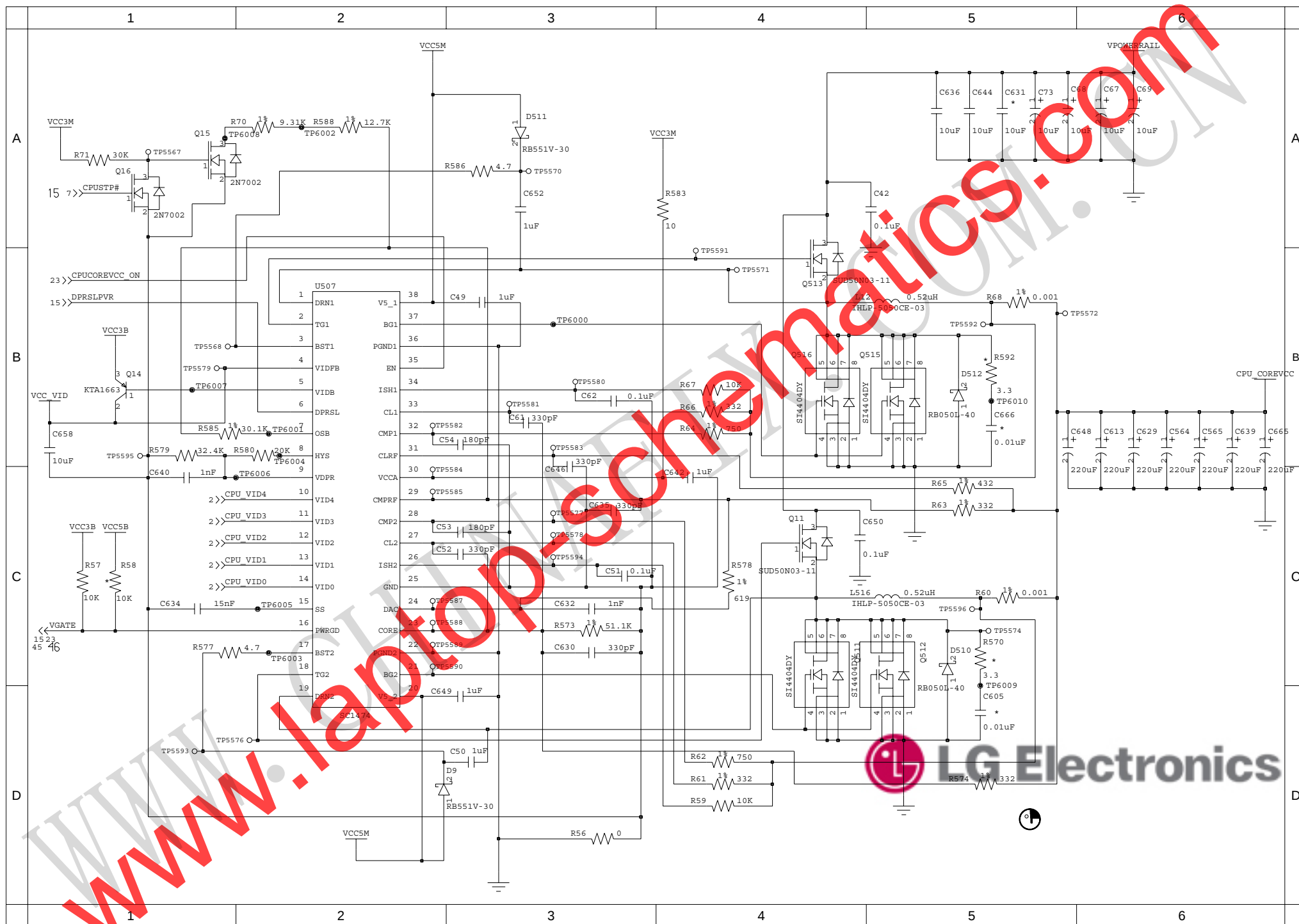


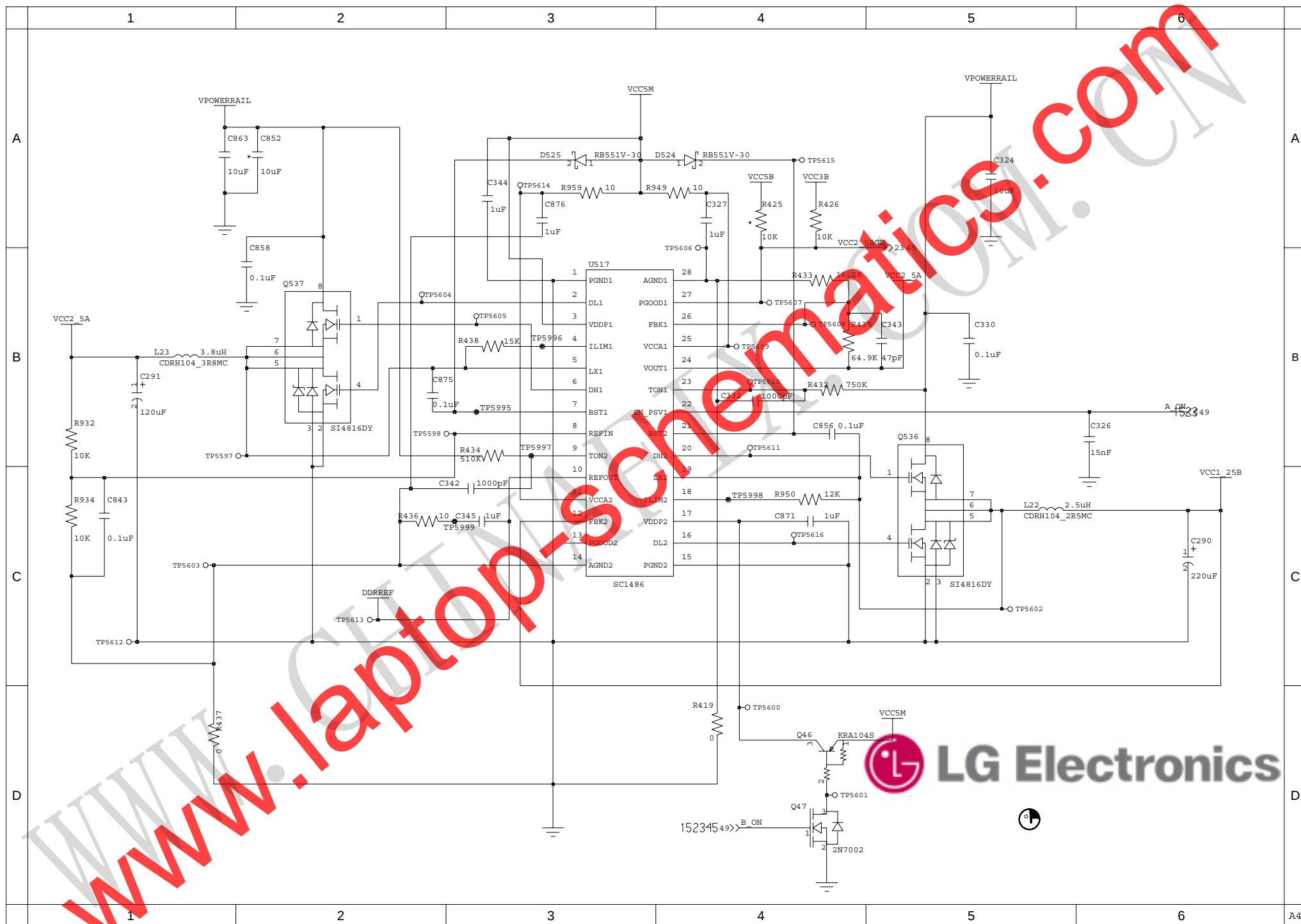


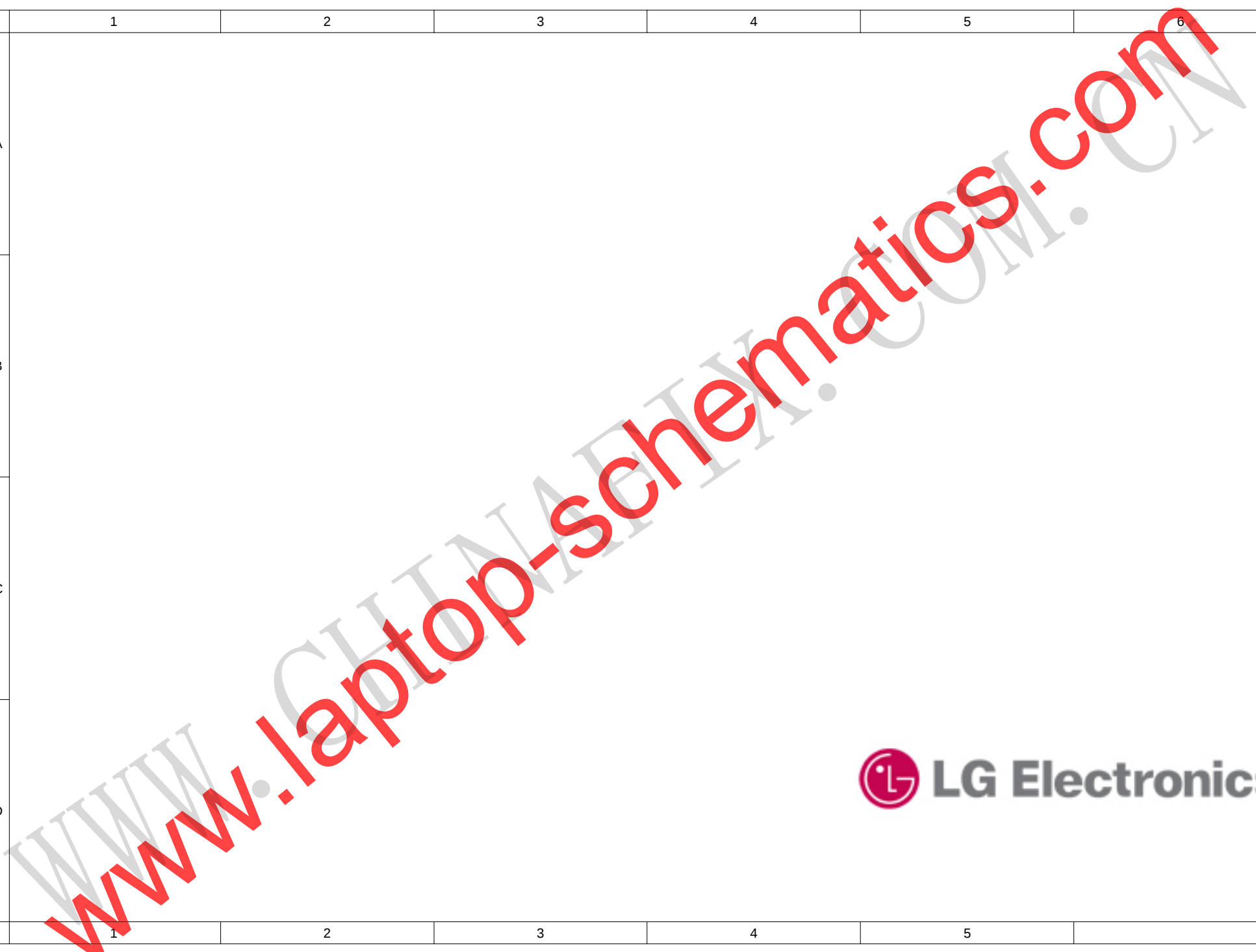










	1	2	3	4	5	6	
A							A
B							B
C							C
D							
	1	2	3	4	5		