PCB STACK UP

LAYER 1 : TOP
LAYER 2 : SGND1
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT

VCC_CORE
MAX8736

VCC1.5
G966

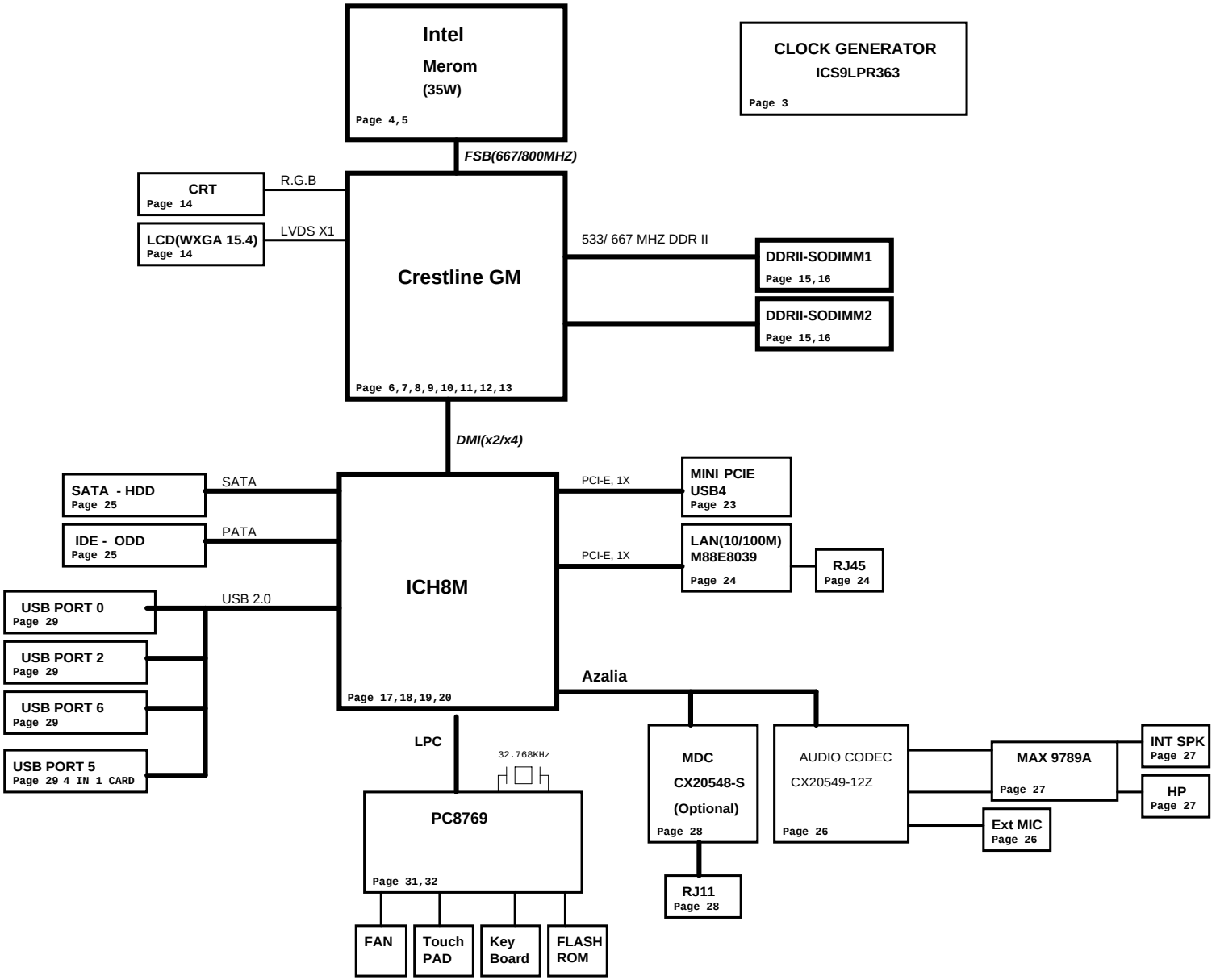
VCC1.05
MAX1933

VCC1.25

1.8VSUS
TPS51116

3VPCU
RVCC3
3VSUS
VCC3
5VPCU
RVCC5
5VSUS
VCC5
MAXIM
MAX8744ETJ+ Page:26

PL3 Block Diagram



PCB P/N:DA0PL3MB6A7

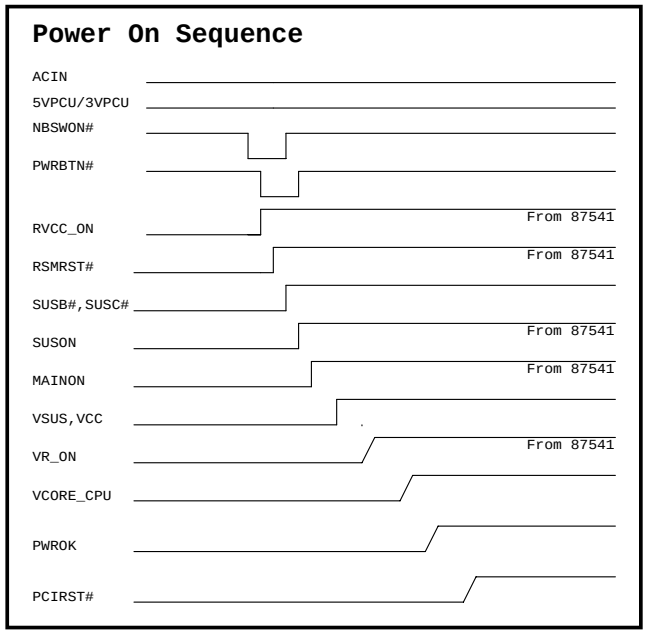
Quanta Computer Inc.
PROJECT : PL3

Size	Document Number	Rev
	Block Diagram	A
Date: Thursday, January 11, 2007	Sheet 1 of 38	

Voltage Rails

Power	Voltage	ON S0~S2	ON S3	ON S4	ON S5	Ctl Signal
9VPCU	9V	V	V	V	V	
5VPCU	5V	V	V	V	V	
3VPCU	3V	V	V	V	V	
RVCC3	3V	V	V	V		RVCC_ON
5VSUS	5V	V	V			SUSON
3VSUS	3V	V	V			SUSON
1.8VSUS	1.8V	V	V			SUSON
VCC5	5V	V				MAINON
VCC3	3V	V				MAINON
VCC1.5	1.5V	V				MAINON
VCC1.25	1.25V	V				MAINON
VCC1.05	1.05V	V				MAINON
SMDDR_VTERM	0.9V	V				MAINON
VCC_CORE	By CPU	V				VR_ON

Power On Sequence



PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 8 : BOT

PCI DEVICES IRQ ROUTING

PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD17	INTA#,INTB#	RICOH832

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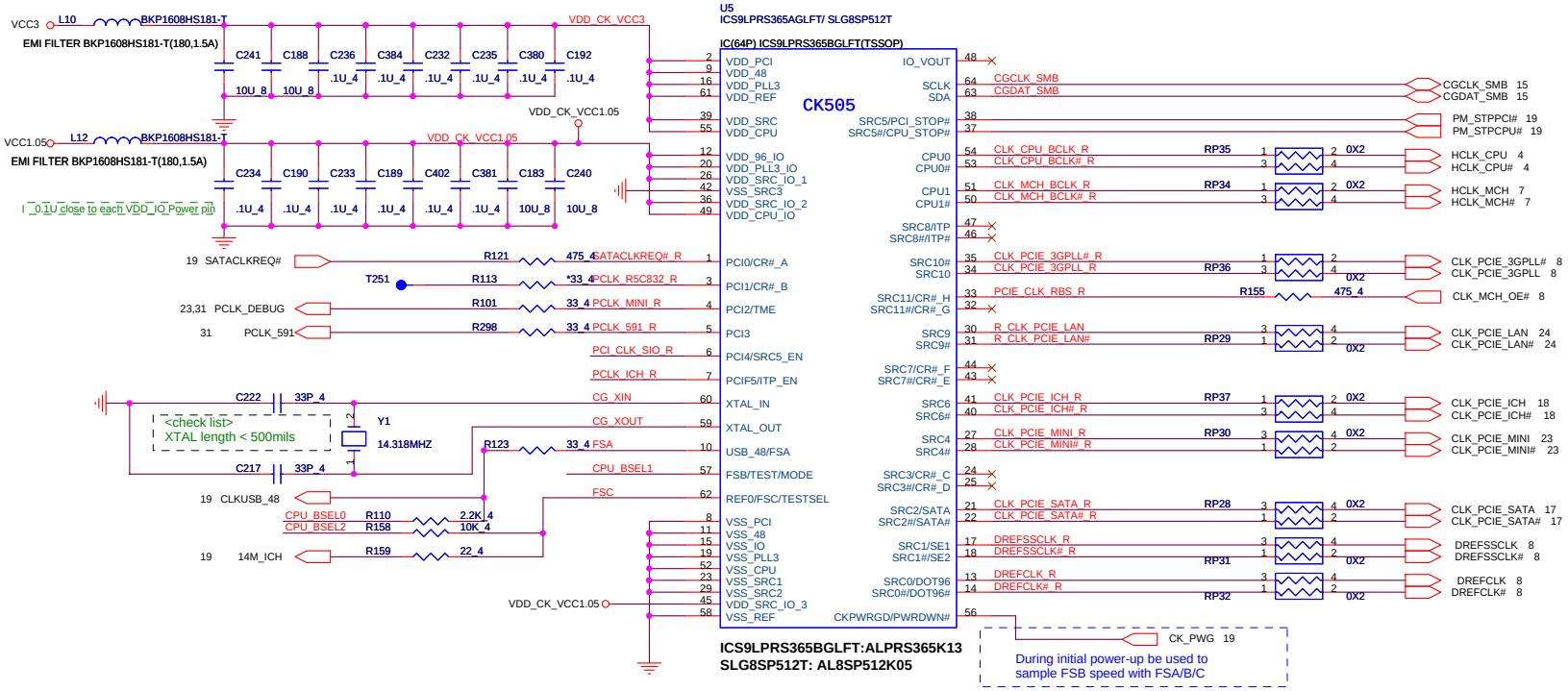
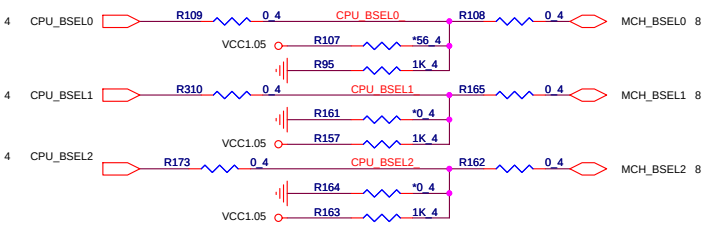
Clock Generator

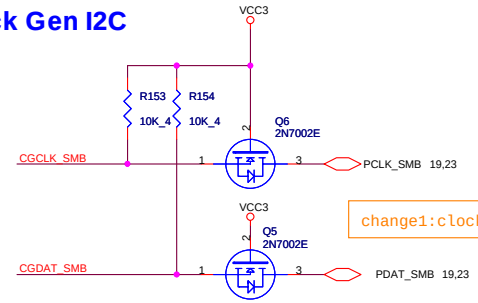




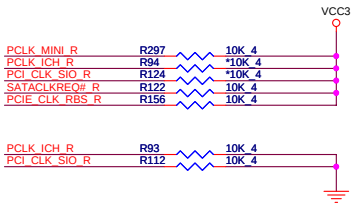
BSEL Frequency Select Table

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz

Clock Gen I2C



change1:clock to data wrong connection b-test



Quanta Computer Inc.
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	Clock Generator	A

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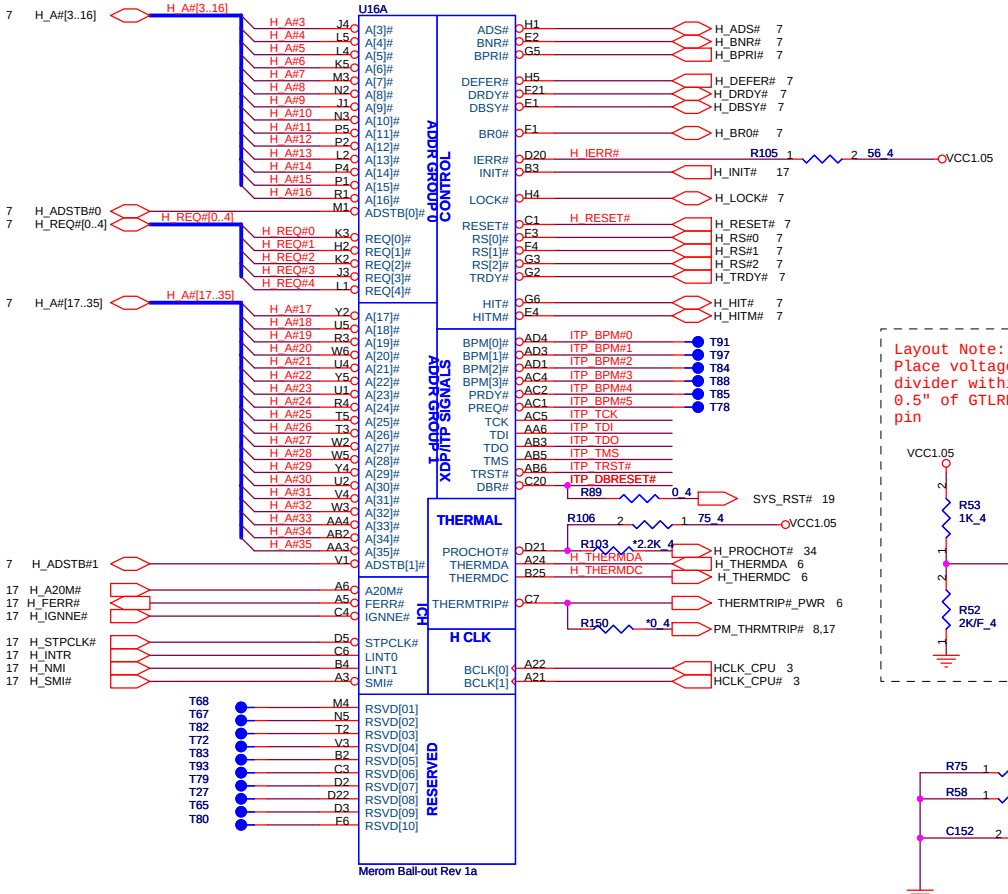
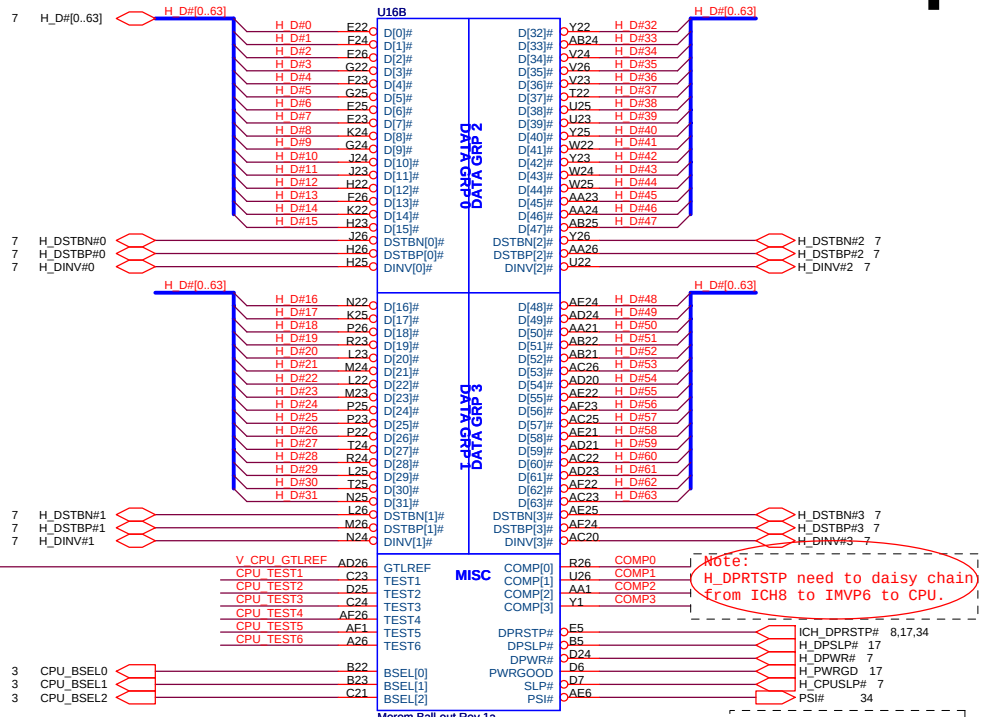


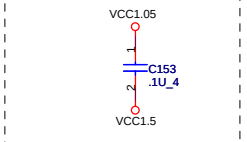


Layout Note:
Place voltage divider within 0.5" of GTLREF pin

VCC1.05
R53 1K_4
R52 2K/F_4

Note:
H_DPRTSTP need to daisy chain from ICH8 to IMVP6 to CPU.

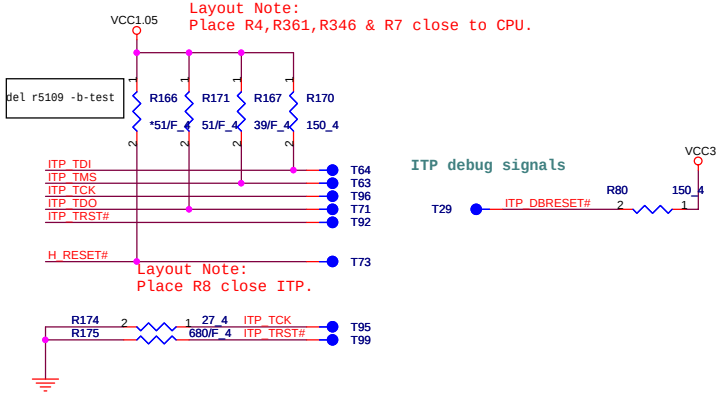
Reserved for EMI.



R75 *1K_4 CPU_TEST1
R58 *1K_4 CPU_TEST2
C152 *.1U_4 CPU_TEST4

T22 CPU_TEST3
T182 CPU_TEST5
T153 CPU_TEST6

Populate ITP700Flex for bringup

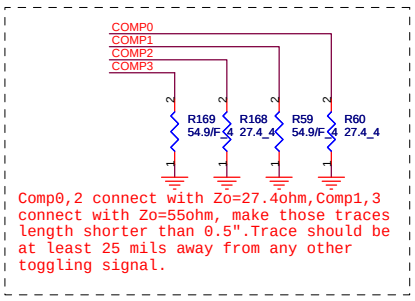


FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0

ITP disable guidelines

Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 2.0" of the ITP
TMS	39 ohm +/- 1%	VTT	Within 2.0" of the ITP
TRST#	500-680ohm +/- 5%	GND	Within 2.0" of the ITP
TCK	27 ohm +/- 1%	GND	Within 2.0" of the ITP
TDO	150 ohm +/- 5%	VTT	Within 2.0" of the ITP

Note: Populate R5, R8, C372 & R430 when ITP connector is populated.



Comp0,2 connect with Zo=27.4ohm,Comp1,3 connect with Zo=55ohm, make those traces length shorter than 0.5".Trace should be at least 25 mils away from any other toggling signal.

Quanta Computer Inc.
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Size	Document Number	Rev
	CPU Host Bus	A
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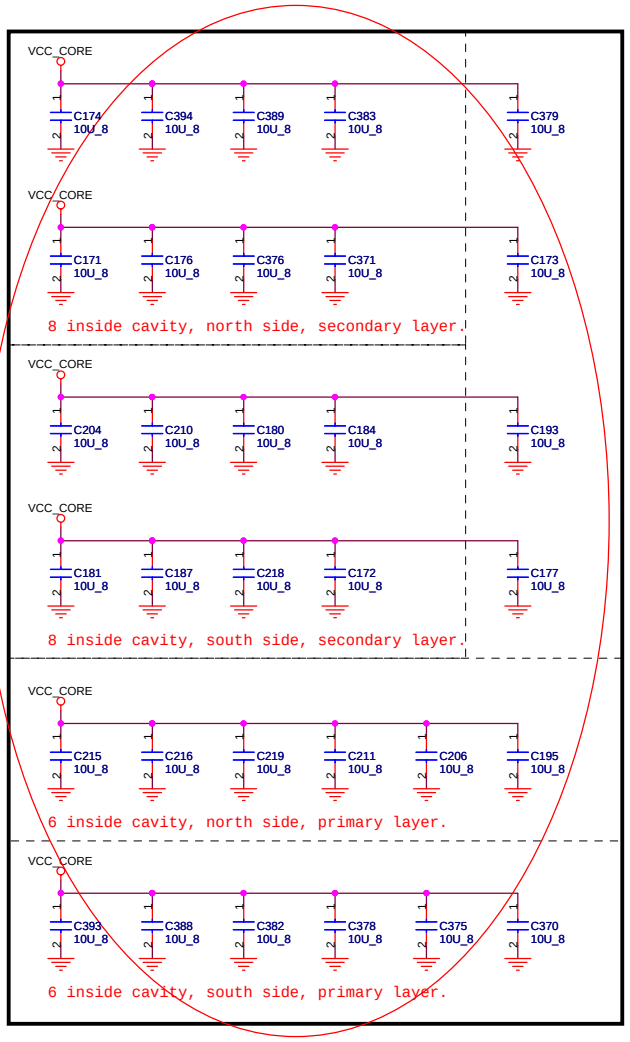
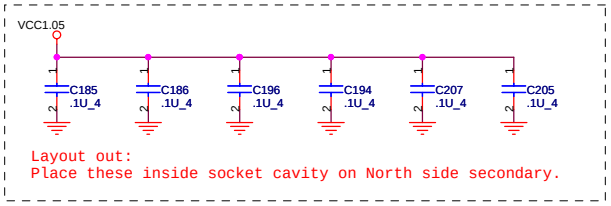
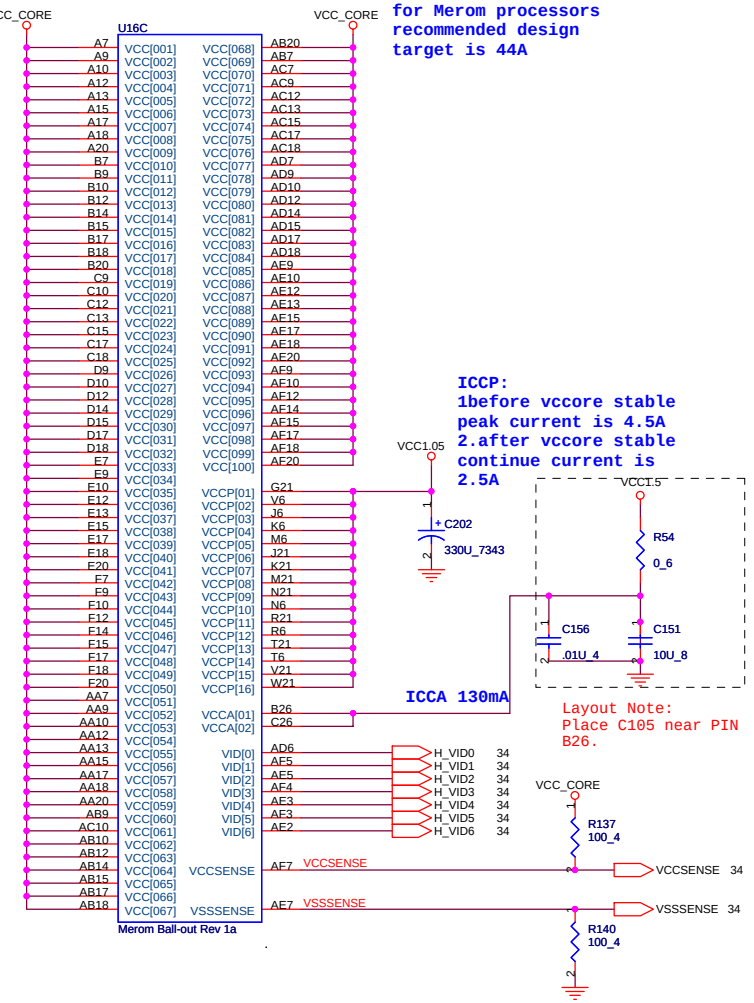


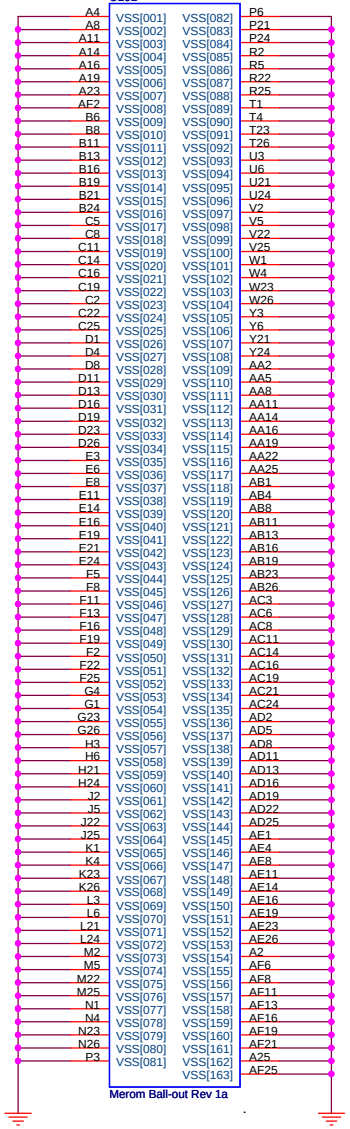


ICCODE:
for Merom processors
recommended design
target is 44A



ICCP:
1before vccore stable
peak current is 4.5A
2.after vccore stable
continue current is
2.5A

Layout Note:
Place C105 near PIN B26.



Quanta Computer Inc.		
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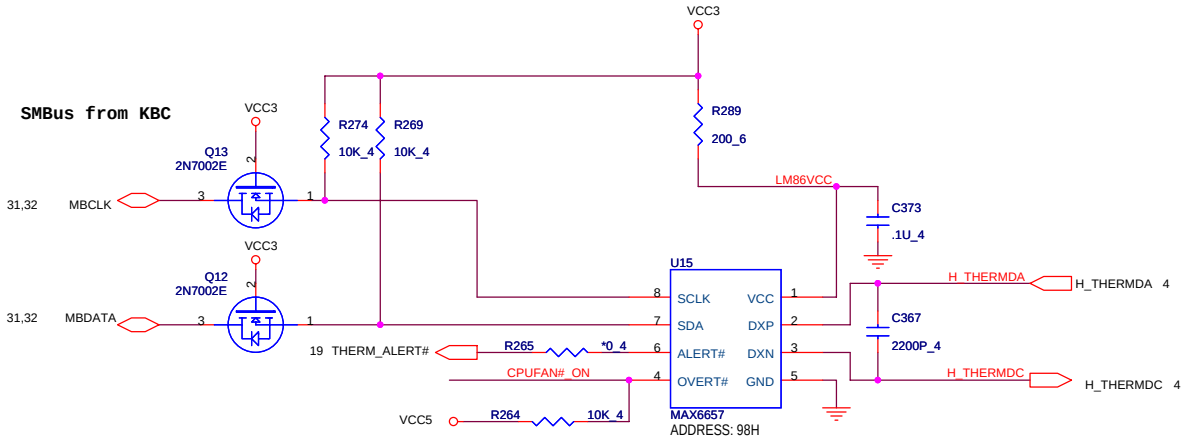
CPU Thermal Sensor

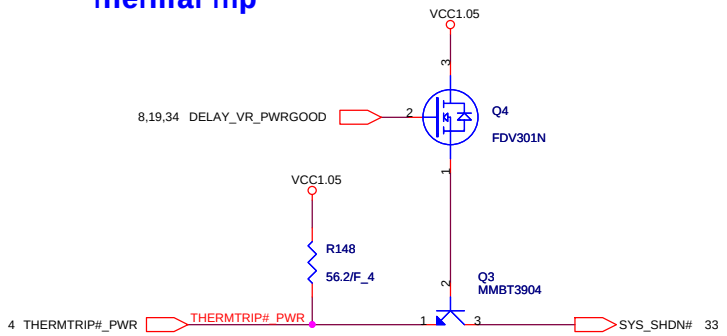
6

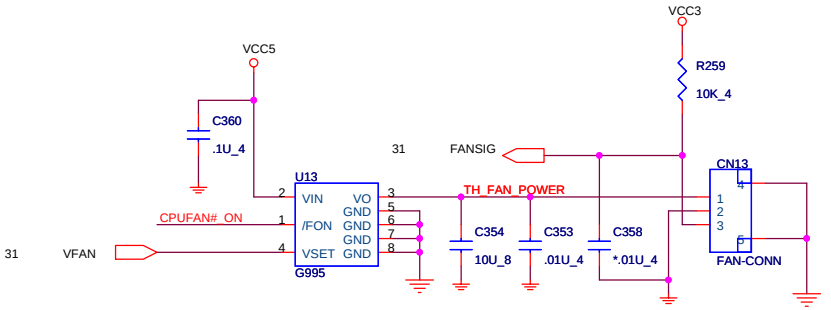


<check list>
Layout Note:Routing 10:10 mils and away from noise source with ground gard

CPU FAN Control

Thermal Trip





FANPWR = 1.6*VSET

<CRB & Design guide>
Layout Note: Thermal trip should connect to ICH8 & GMCH without T-ing (ZS1 default NC)

Quanta Computer Inc.
PROJECT : PL3

Size	Document Number	Rev
	Thermal/FAN Control	A

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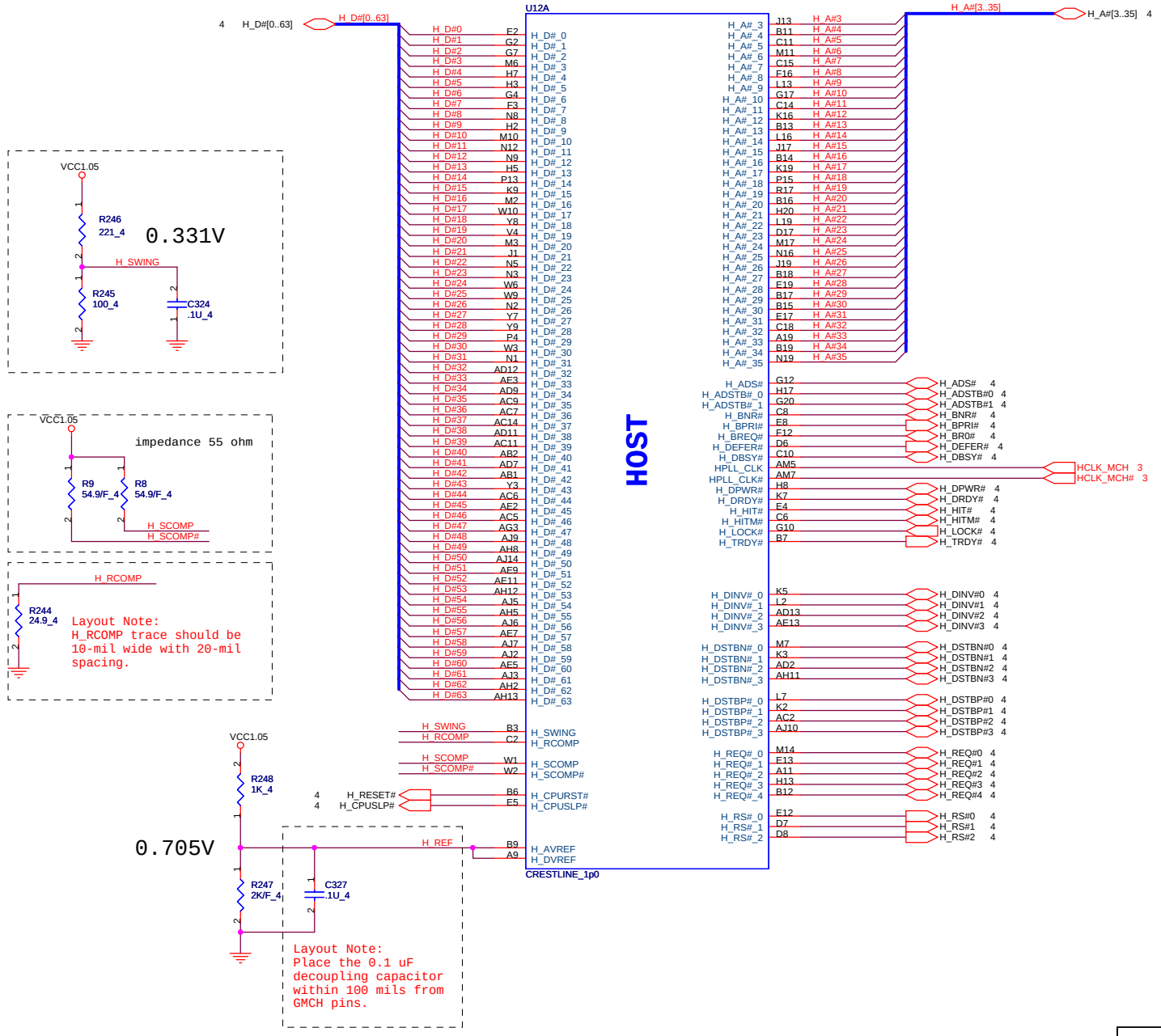

Quanta Computer Inc.		
PROJECT : PL3		
Size	Document Number: GMCH HOST	Rev: A
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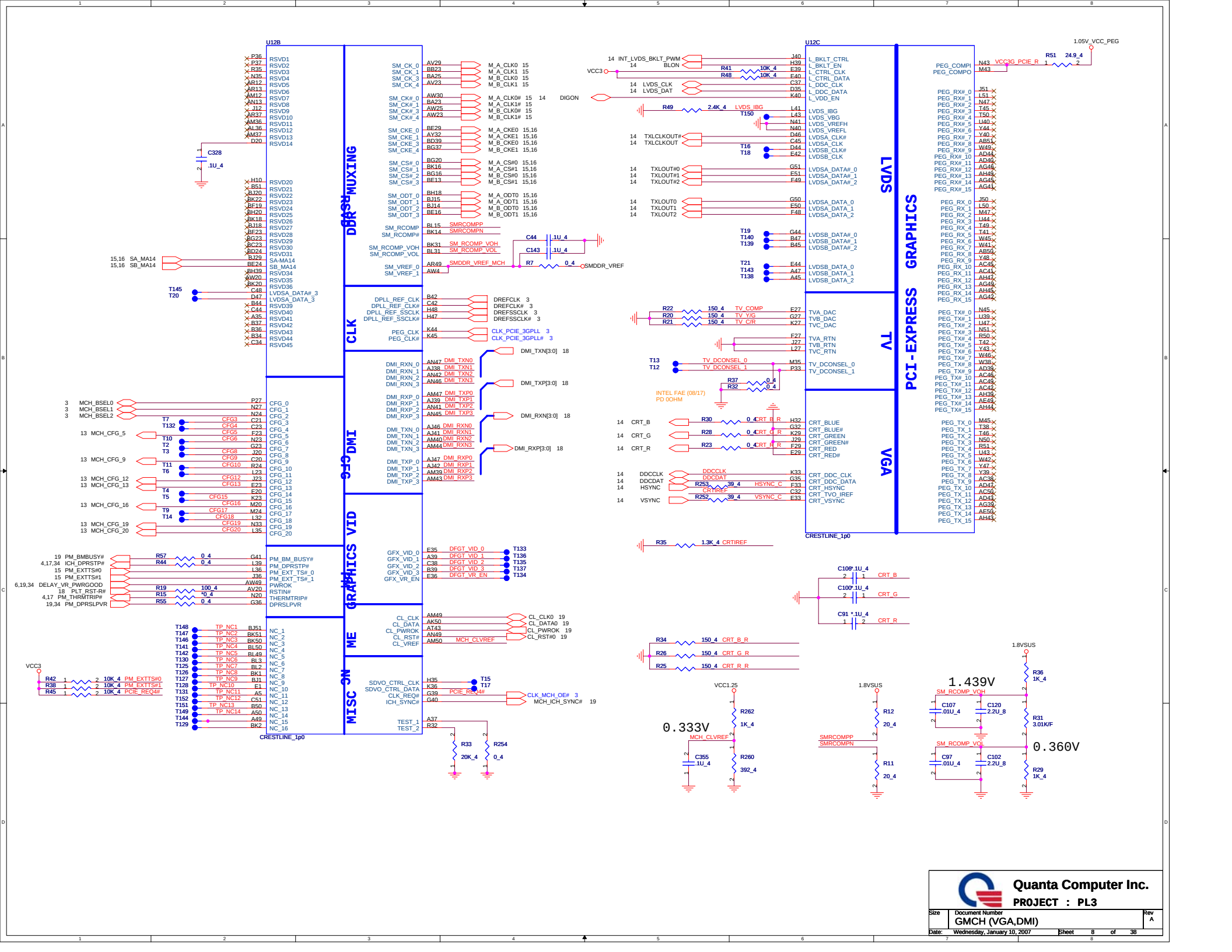
U12B
U12C
DDR MUXING
CLK
DMI
CFG
GRAPHICS VID
MISC
NC
LVDS
TV
VGA
PCI-EXPRESS GRAPHICS
CRESTLINE_1p0
1.05V_VCC_PEG
0.333V
1.439V
0.360V
Quanta Computer Inc.
PROJECT : PL3
Size
Document Number
GMCH (VGA,DMI)
Rev
A
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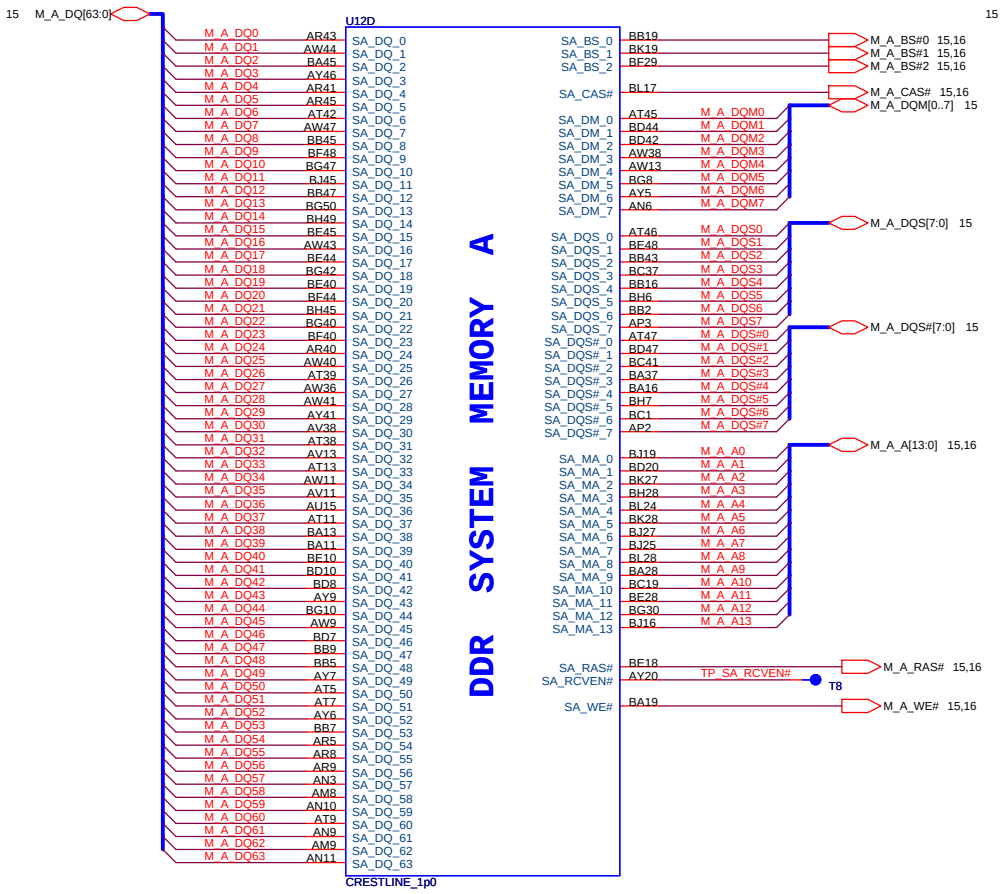

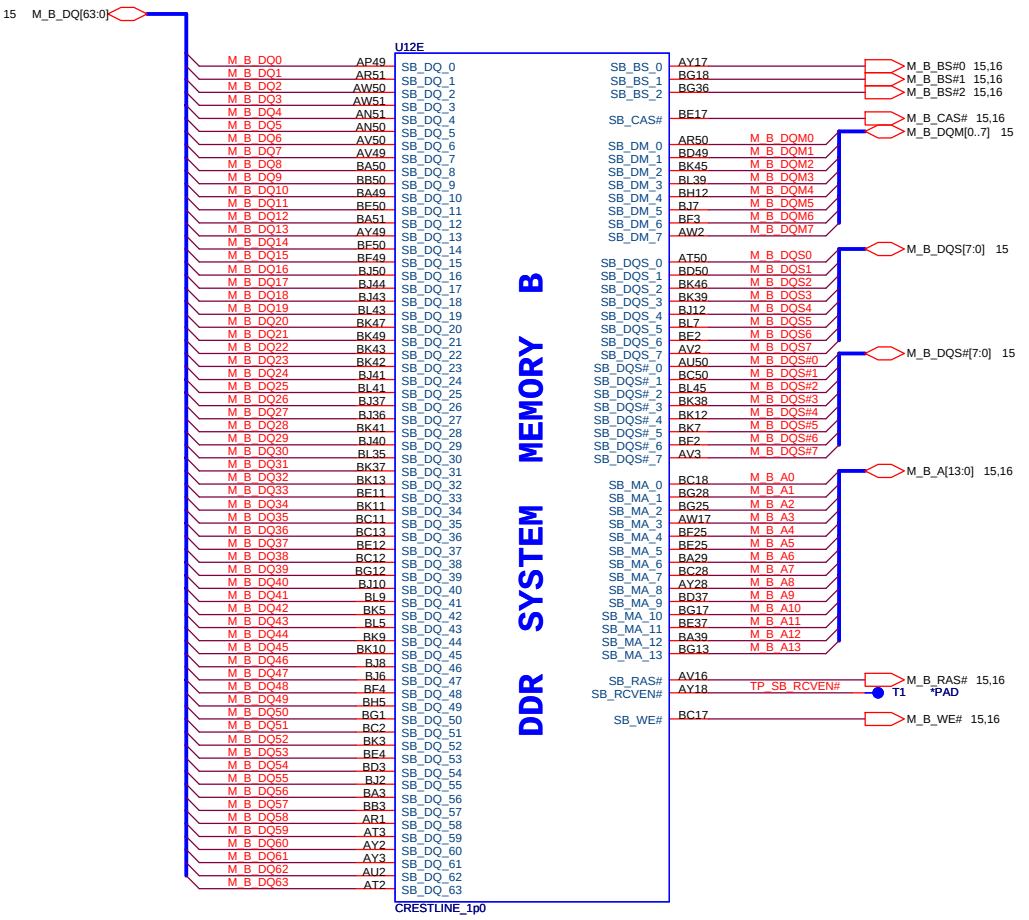

Quanta Computer Inc.

PROJECT : PL3

Size	Document Number	Rev
	GMCH DDR2	A

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U12G

VCC CORE

VCC1.05 — AT35, AT34, AH28, AC32, AC31, AK32, AJ31, AJ28, AH32, AH31, AH29, AF32 — VCC_1 … VCC_12

R30 — VCC_13

IVCCSM MAX: 3.318A

POWER

1.8VSUS — AU32, AU33, AU35, AV33, AW33, AW35, AY35, BA32, BA33, BA35, BB33, BC32, BC33, BC35, BD32, BD35, BE32, BE33, BE35, BF33, BF34, BG32, BG33, BG35, BH32, BH34, BH35, BJ32, BJ33, BJ34, BK32, BK33, BK34, BK35, BL33, AU30 — VCC_SM_1 … VCC_SM_36

VCC SM

VCC1.05 — R20, T14, W13, W14, Y12, AA20, AA23, AA26, AA28, AB21, AB24, AB29, AC20, AC21, AC23, AC24, AC26, AC28, AC29, AD20, AD23, AD24, AD28, AF21, AF26, AA31, AH20, AH21, AH23, AH24, AH26, AD31, AJ20, AN14 — VCC_AXG_1 … VCC_AXG_34

VCC GFX

VCC GFX NCTF

VCC_AXG_NCTF_1 … VCC_AXG_NCTF_83 — T17, T18, T19, T21, T22, T23, T25, U15, U16, U17, U19, U20, U21, U23, U26, V16, V17, V19, V20, V21, V23, V24, Y15, Y16, Y17, Y19, Y20, Y21, Y23, Y24, Y26, Y28, Y29, AA16, AA17, AB16, AB19, AC16, AC17, AC19, AD15, AD16, AD17, AE16, AF19, AH15, AH16, AH17, AH19, AJ16, AJ17, AJ19, AK16, AK19, AL16, AL17, AL19, AL20, AL21, AL23, AM15, AM16, AM19, AM20, AM21, AM23, AP15, AP16, AP17, AP19, AP20, AP21, AP23, AP24, AR20, AR21, AR23, AR24, AR26, V26, V28, V29, Y31

VCC SM LF

VCC_SM_LF1 … VCC_SM_LF7 — AW45, BC39, BE39, BD17, BD4, AW8, AT6 — VCCSM_LF1 … VCCSM_LF7

C51 .1U_4, C49 .1U_4, C38 .22U_6, C46 .22U_6, C125 .47U_6, C130 1U_6, C139 1U_6

CRESTLINE_1p0

VCC3 — R249 10_4 — D11 CH751H-40HPT

Ivcc (External GFX 1.310 A, integrate 1.572 A)

VCC1.05 — C320 220U_7343, C326 22U_8, C108 .22U_6, C134 .22U_6, C118 .1U_4

Layout Note: 370 mils from edge.

Layout Note: Inside GMCH cavity.

VCC1.05 — C317 330U_7343, C319 330U_7343

Ivcc_AXG Graphics core supply current 7.7A

Layout Note: 370 mils from edge.

Layout Note: Inside GMCH cavity for VCC_AXG.

C70 .1U_4, C95 .1U_4, C83 .47U_6, C96 1U_6, C57 10U_8, C60 22U_8

GMCH 1.05V	current(A)	Remark
VCC Core	1.573	(1.3A for external GFX)
VCC_AXG	7.7	for integrated Gfx
VCC_AXD	0.2	
VTT	0.85	FSB VCCP
VCC_PEG	1.2	for PCIEG
VCC_AXM	0.54	for IAMT function
VCCR_RX_DMI	0.25	DMI
SUM	**12.313**	

U12F

VCC NCTF

VCC_NCTF_1 … VCC_NCTF_50 — AB33, AB36, AB37, AC33, AC35, AC36, AD35, AD36, AF33, AF36, AH33, AH35, AH36, AH37, AJ33, AJ35, AK33, AK35, AK36, AK37, AD33, AJ36, AM35, AL33, AL35, AA33, AA35, AA36, AP35, AP36, AR35, AR36, Y32, Y33, Y35, Y36, Y37, T30, T34, T35, U29, U31, U32, U33, U35, U36, V32, V33, V36, V37

VSS NCTF

VSS_NCTF_1 … VSS_NCTF_21 — T27, T37, U24, U28, V31, V35, AA19, AB17, AB35, AD19, AD37, AF17, AF35, AK17, AM17, AM24, AP26, AP28, AR15, AR19, AR28

POWER

VSS SCB

VSS_SCB1 … VSS_SCB6 — A3, B2, C1, BL1, BL51, A51

VCC AXM

VCC1.05 — VCC_AXM_1 … VCC_AXM_7 — AT33, AT31, AK29, AK24, AK23, AJ26, AJ23

VCC AXM NCTF

VCC_AXM_NCTF_1 … VCC_AXM_NCTF_19 — AL24, AL26, AL28, AM26, AM28, AM29, AM31, AM32, AM33, AP29, AP31, AP32, AP33, AL29, AL31, AL32, AR31, AR32, AR33

VCC1.05

Ivcc_AXM Controller supply current 540mA

Layout Note: Inside GMCH cavity.

C124 .1U_4, C115 .1U_4, C117 .1U_4

C135 22U_8, C84 .22U_6, C116 .22U_6

Layout Note: Place close to GMCH edge.

CRESTLINE_1p0

from CH73301M8L9 to CH733LM8812 1/11

1.8VSUS — C119 .1U_4

1.8VSUS — C138 330U_7343, C131 22U_8, C114 22U_8

Layout Note: Place C901 where LVDS and DDR2 taps.

Layout Note: Place on the edge.

Quanta Computer Inc.

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Size	Document Number	Rev
	GMCH VCC,NCTF	A

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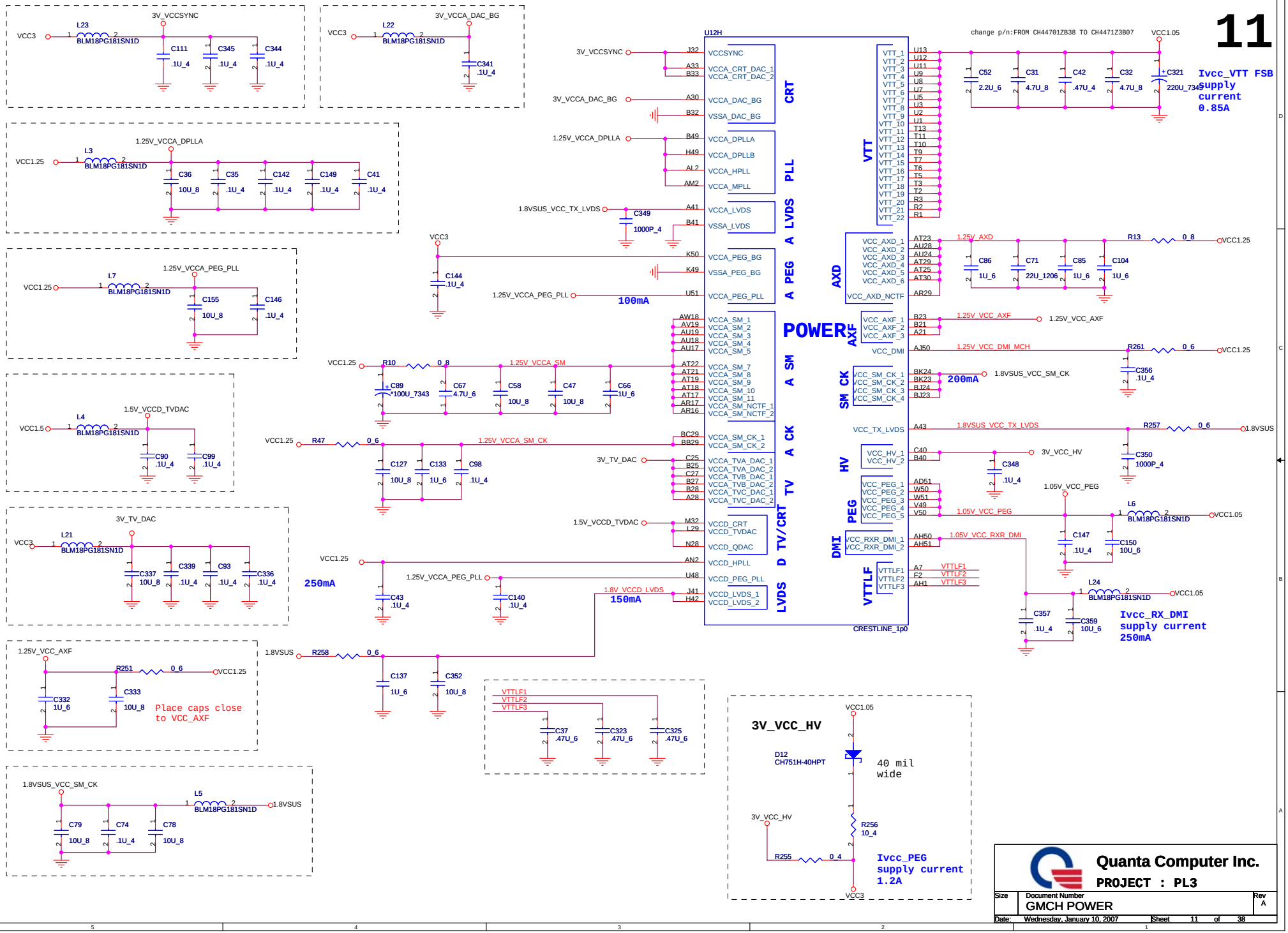
11
3V_VCCSYNC
L23
BLM18PG181SN1D
C111 .1U_4
C345 .1U_4
C344 .1U_4
3V_VCCA_DAC_BG
L22
BLM18PG181SN1D
C341 .1U_4
1.25V_VCCA_DPLLA
L3
BLM18PG181SN1D
C36 10U_8
C35 .1U_4
C142 .1U_4
C149 .1U_4
C41 .1U_4
1.25V_VCCA_PEG_PLL
L7
BLM18PG181SN1D
C155 10U_8
C146 .1U_4
1.5V_VCCD_TVDAC
L4
BLM18PG181SN1D
C90 .1U_4
C99 .1U_4
3V_TV_DAC
L21
BLM18PG181SN1D
C337 10U_8
C339 .1U_4
C93 .1U_4
C336 .1U_4
1.25V_VCC_AXF
R251 0_6
C332 1U_6
C333 10U_8
Place caps close to VCC_AXF
1.8VSUS_VCC_SM_CK
L5
BLM18PG181SN1D
C79 10U_8
C74 .1U_4
C78 10U_8
U12H
CRESTLINE_1p0
CRT
PLL
A LVDS
A PEG
POWER
A SM
A CK
TV
D TV/CRT
LVDS
3V_VCCSYNC
VCCSYNC
VCCA_CRT_DAC_1
VCCA_CRT_DAC_2
3V_VCCA_DAC_BG
VCCA_DAC_BG
VSSA_DAC_BG
1.25V_VCCA_DPLLA
VCCA_DPLLA
VCCA_DPLLB
VCCA_HPLL
VCCA_MPLL
1.8VSUS_VCC_TX_LVDS
C349 1000P_4
VCCA_LVDS
VSSA_LVDS
VCC3
C144 .1U_4
VCCA_PEG_BG
VSSA_PEG_BG
1.25V_VCCA_PEG_PLL
100mA
VCCA_PEG_PLL
VCCA_SM_1
VCCA_SM_2
VCCA_SM_3
VCCA_SM_4
VCCA_SM_5
VCC1.25
R10 0_8
C89 *100U_7343
C67 4.7U_6
C58 10U_8
C47 10U_8
C66 1U_6
1.25V_VCCA_SM
VCCA_SM_7
VCCA_SM_8
VCCA_SM_9
VCCA_SM_10
VCCA_SM_11
VCCA_SM_NCTF_1
VCCA_SM_NCTF_2
R47 0_6
C127 10U_8
C133 1U_6
C98 .1U_4
1.25V_VCCA_SM_CK
VCCA_SM_CK_1
VCCA_SM_CK_2
3V_TV_DAC
VCCA_TVA_DAC_1
VCCA_TVA_DAC_2
VCCA_TVB_DAC_1
VCCA_TVB_DAC_2
VCCA_TVC_DAC_1
VCCA_TVC_DAC_2
1.5V_VCCD_TVDAC
VCCD_CRT
VCCD_TVDAC
VCCD_QDAC
VCCD_HPLL
VCCD_PEG_PLL
VCCD_LVDS_1
VCCD_LVDS_2
VCC1.25
250mA
C43 .1U_4
1.25V_VCCA_PEG_PLL
C140 .1U_4
1.8V_VCCD_LVDS
150mA
1.8VSUS
R258 0_6
C137 1U_6
C352 10U_8
VTTLF1
VTTLF2
VTTLF3
C37 .47U_6
C323 .47U_6
C325 .47U_6
VTT
AXD
AXF
SM CK
HV
PEG
DMI
VTTLF
change p/n:FROM CH44701ZB38 TO CH4471Z3B07
VCC1.05
C52 2.2U_6
C31 4.7U_8
C42 .47U_4
C32 4.7U_8
C321 220U_7343
Ivcc_VTT FSB supply current 0.85A
1.25V_AXD
C86 1U_6
C71 22U_1206
C85 1U_6
C104 1U_6
R13 0_8
1.25V_VCC_AXF
R261 0_6
1.8VSUS_VCC_SM_CK
200mA
1.8VSUS_VCC_TX_LVDS
R257 0_6
3V_VCC_HV
C348 .1U_4
C350 1000P_4
1.05V_VCC_PEG
L6
BLM18PG181SN1D
1.05V_VCC_RXR_DMI
C147 .1U_4
C150 10U_6
L24
BLM18PG181SN1D
C357 .1U_4
C359 10U_6
Ivcc_RX_DMI supply current 250mA
3V_VCC_HV
D12
CH751H-40HPT
40 mil wide
R256 10_4
R255 0_4
Ivcc_PEG supply current 1.2A
Quanta Computer Inc.
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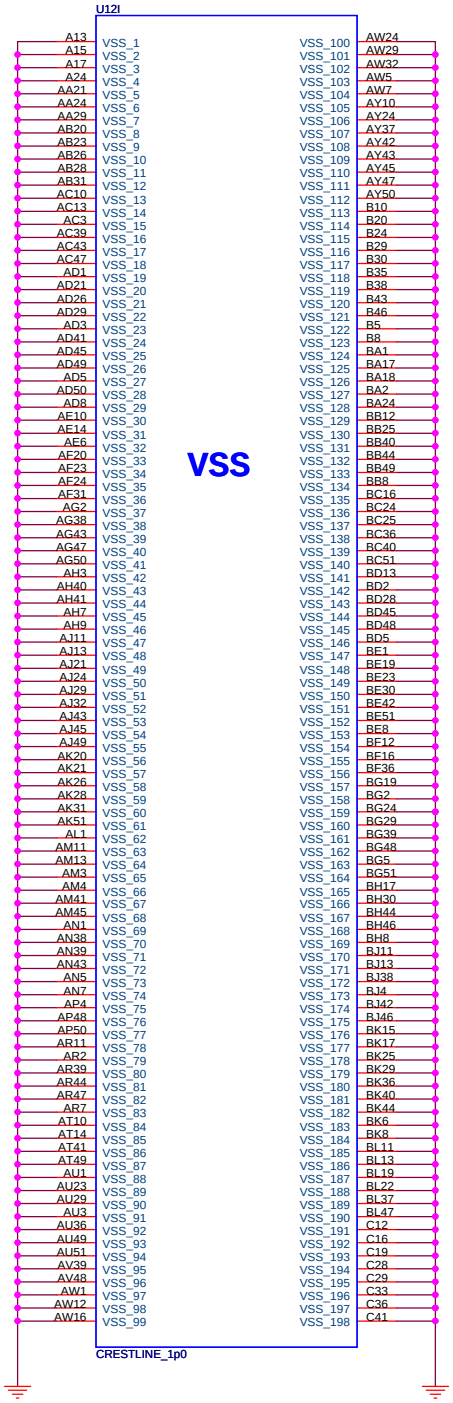

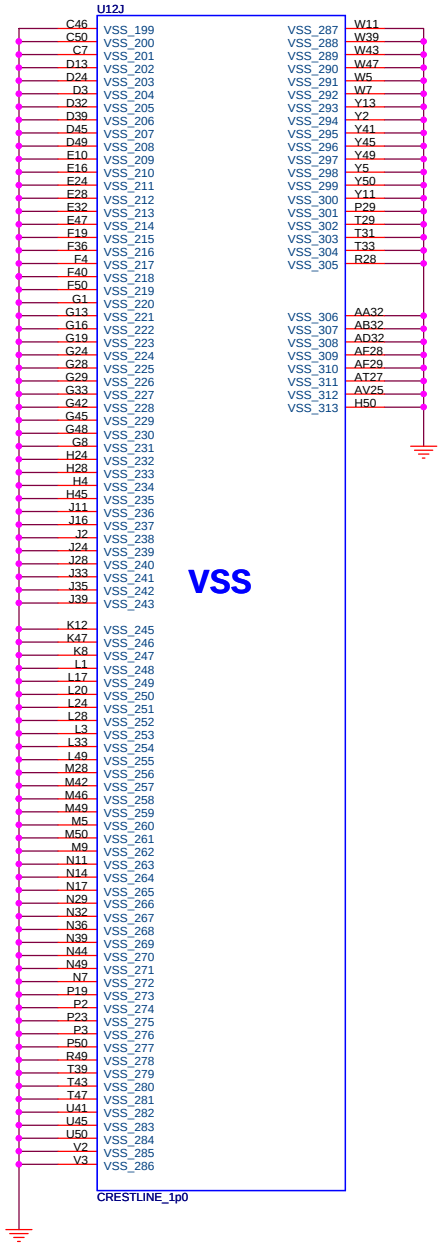

Quanta Computer Inc.

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Strap table

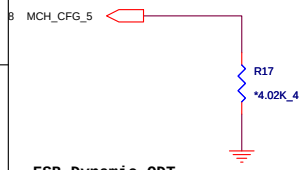
All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal

CFG[17:3] Have internal Pull-up
CFG[18:19] Have internal Pull-down
Any CFG signal strapping option not list below should be left NC Pin

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU(Default)
CFG8	Low power PCI Express	0 = Normal mode 1 = Low Power mode
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIe concurrent	0 = Only SDVO or PCIE x1 is operation(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

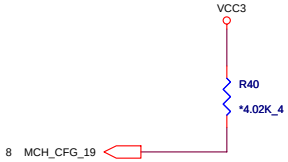
DMI X2 Select

MCH_CFG_5	Low = DMIX2 High = IDMIX4(Default)



DMI Lane Reversal

MCH_CFG_19	Low = Normal operation(Default) High = Reverse Lane



XOR /ALLz /Clock Un-gating

MCH_CFG_12	MCH_CFG_13	Configuration
0	0	Clock gating disable
0	1	XOR Mode Enable
1	0	ALL-z Mode Enable
1	1	Normal operation(Default)

PCI Express Graphics

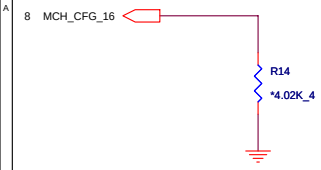
MCH_CFG_9	Low = Reverse Lane High = Normal operation(Default)

SDVO Present

Strap define at External DVI control page

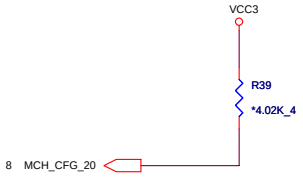
FSB Dynamic ODT

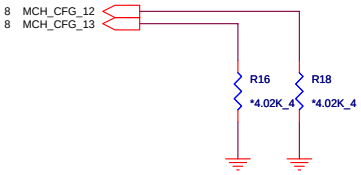
MCH_CFG_16	Low = ODT Disable High = ODT Enable(Default)



SDVO/PCIE Concurrent operation

MCH_CFG_20	Low = Only SDVO or PCIE X1 is operational(Default) High = SDVO andPCIE X1 are operating simultaneously via the PEG port





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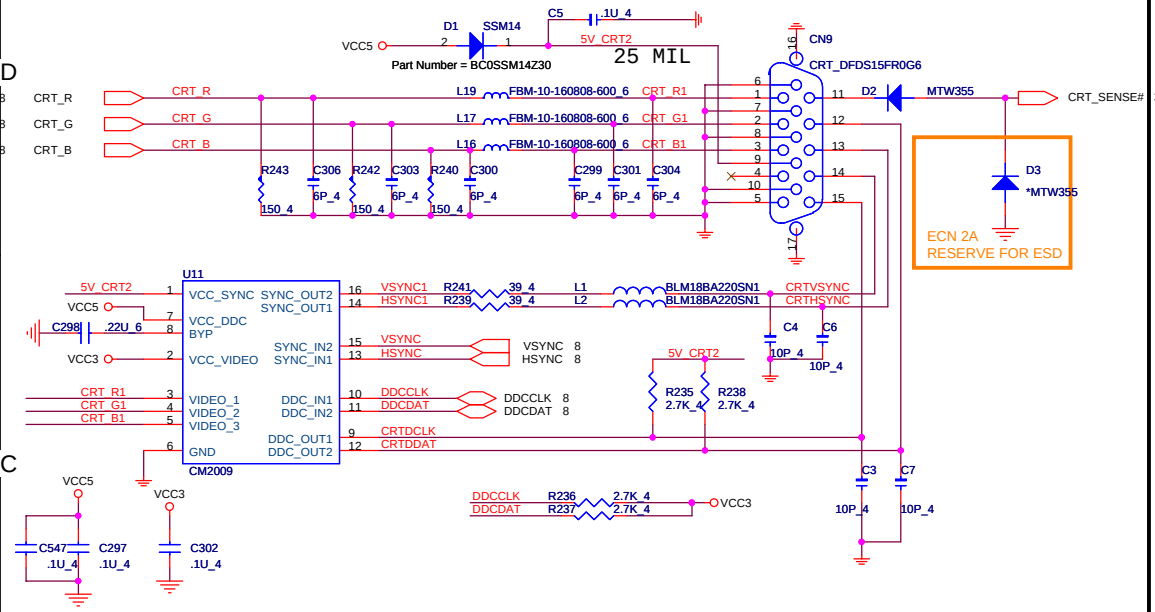
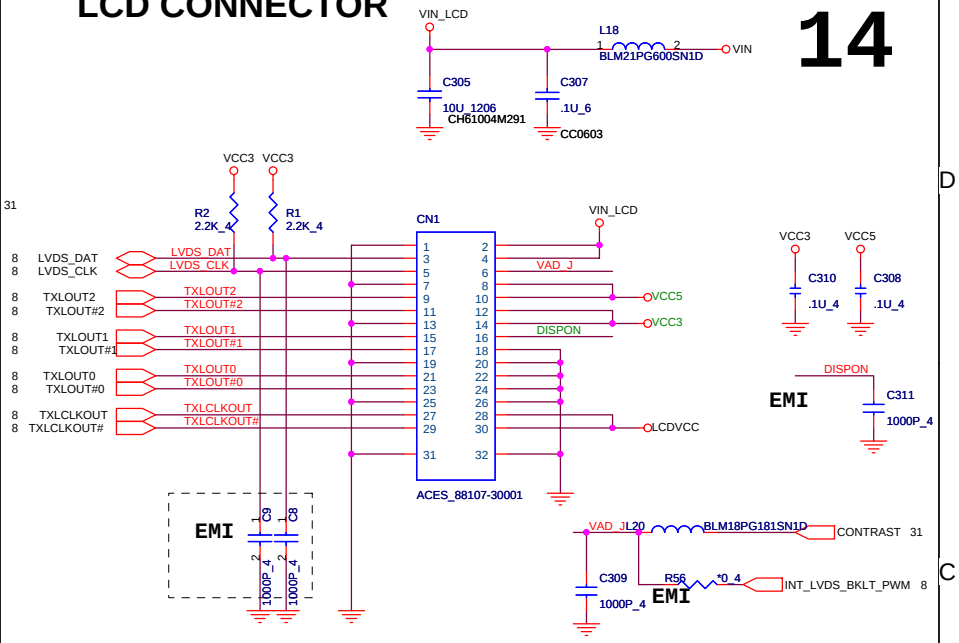
CRT PORT

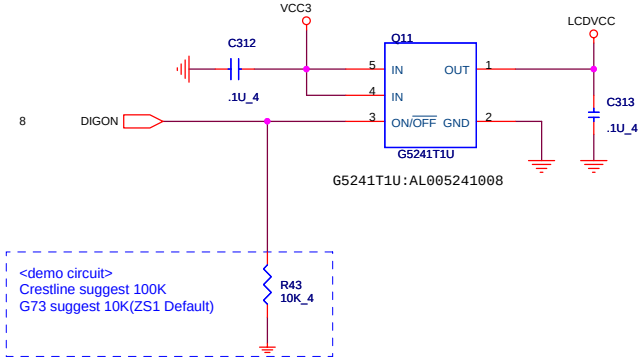


LCD CONNECTOR

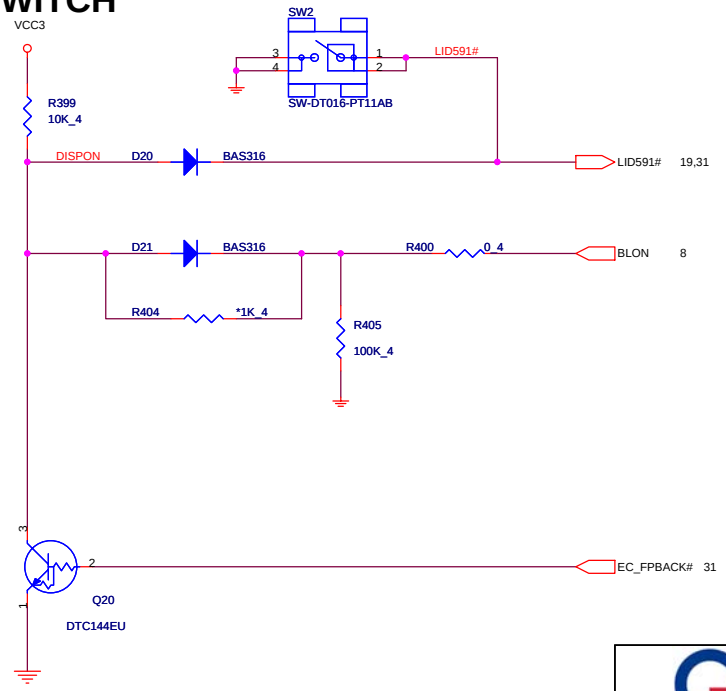


14

PANEL VCC CONTROL



LID SWITCH



Quanta Computer Inc.

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	PANEL LCD CRT	A
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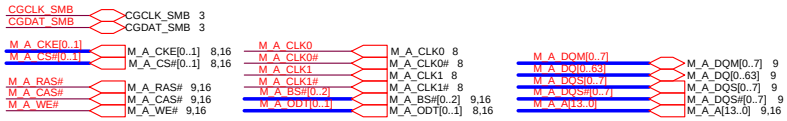
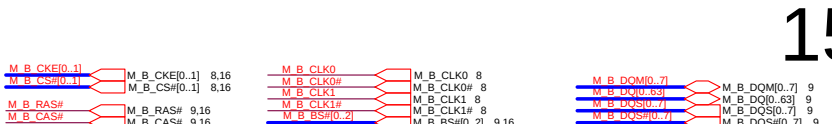
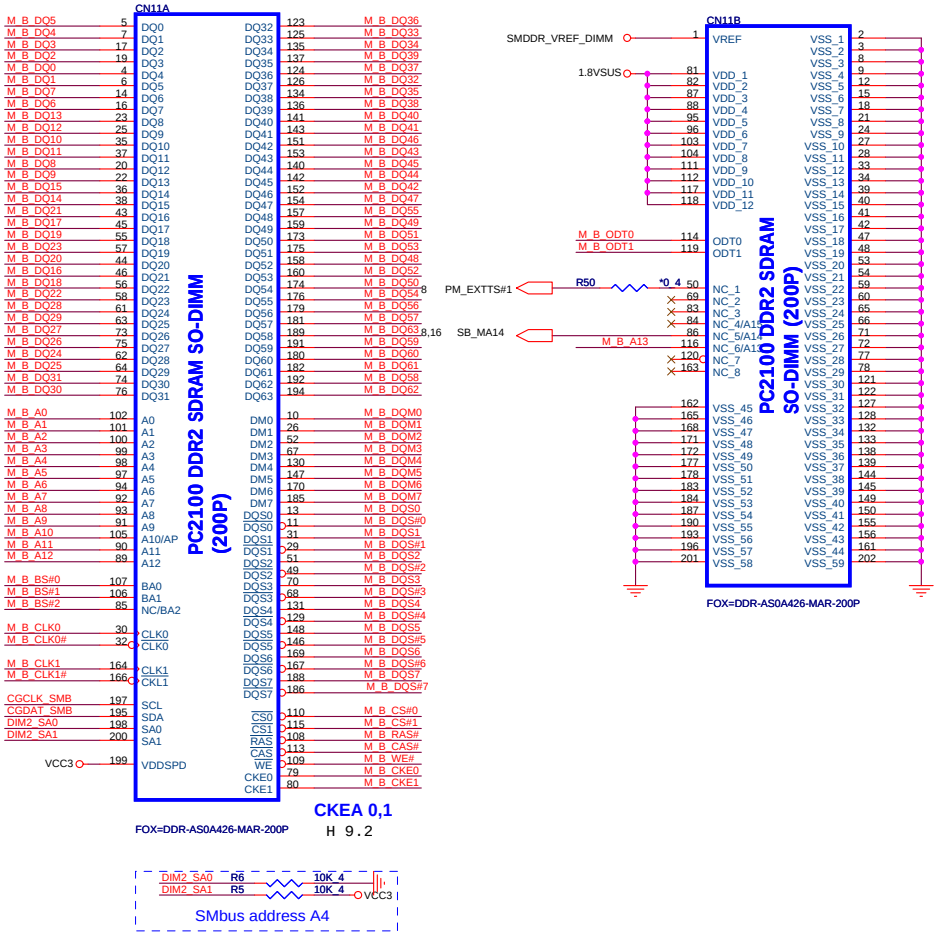
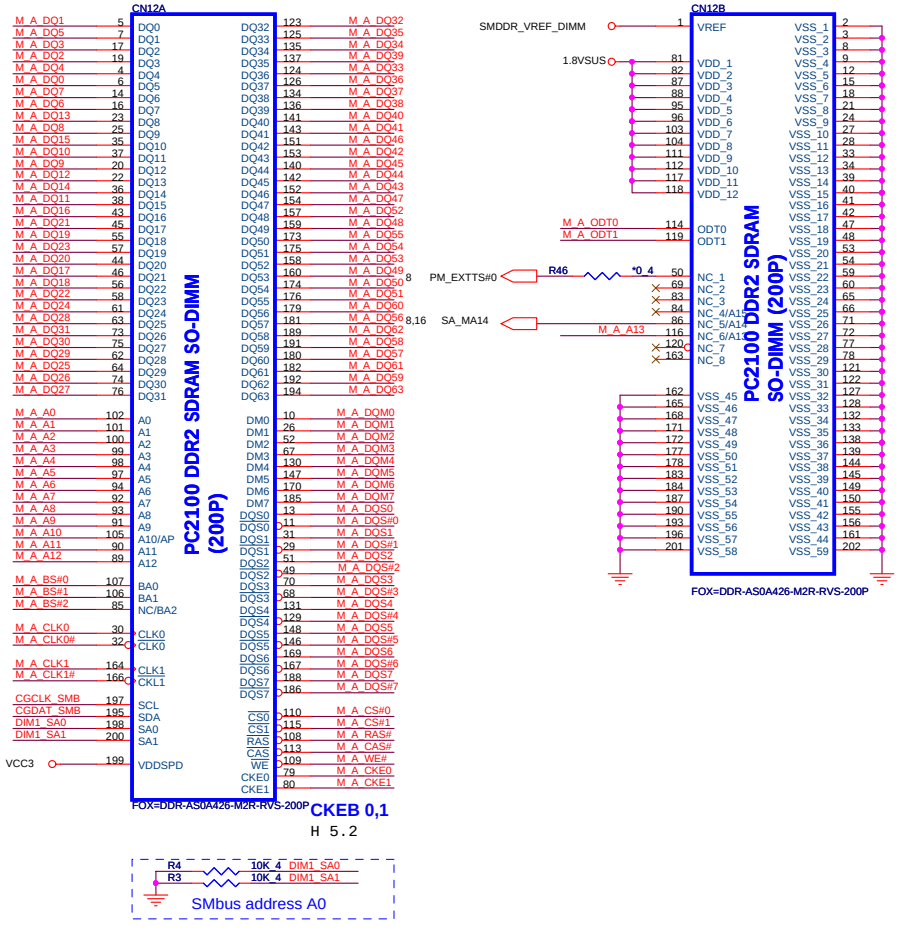
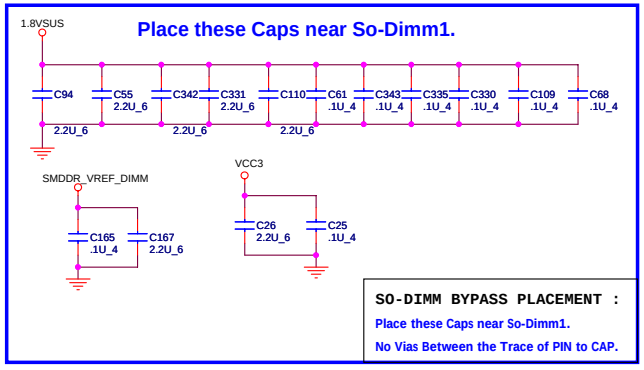
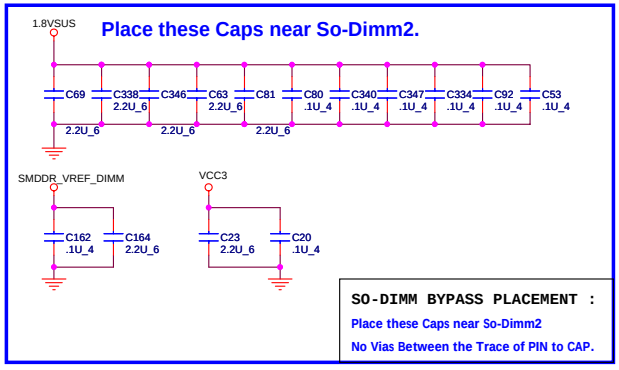




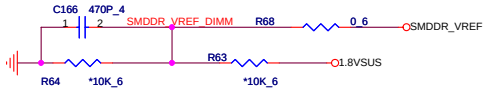








SMDDR_VREF



change2:SMDDR_VREF_DIMM is from SMDDR_VREF;
wrong connection of SMDDR_VTERM and SMDDR_VREF

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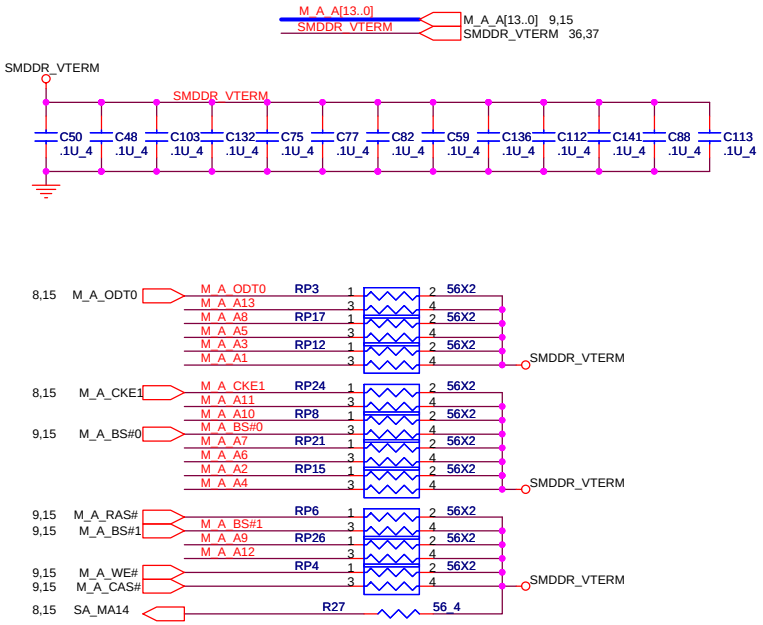
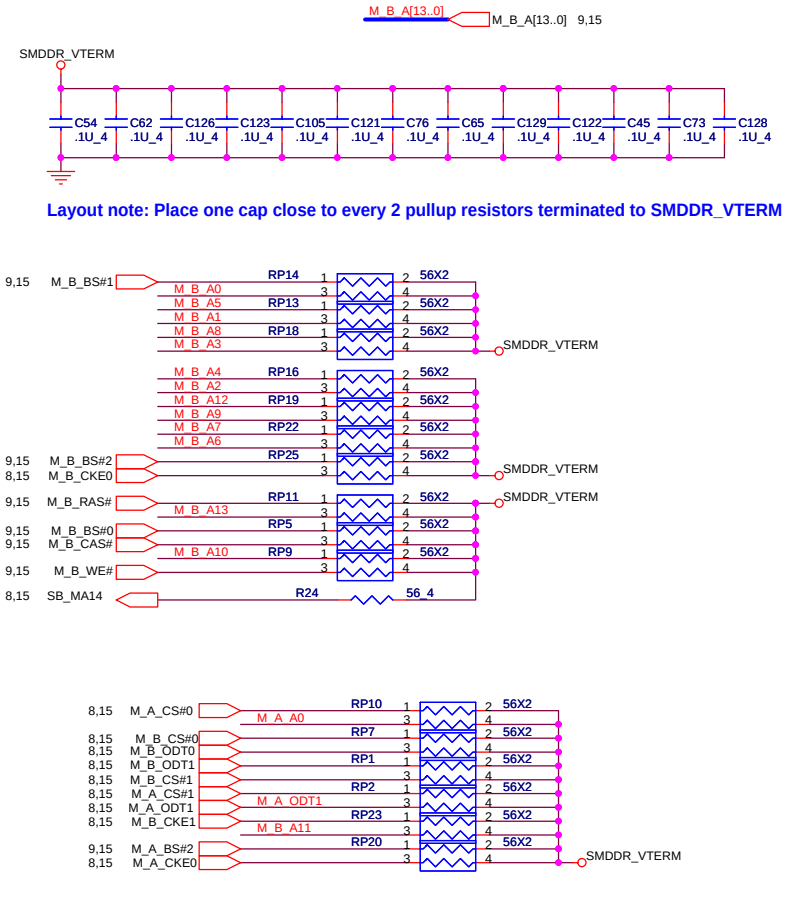
DDRII DUAL CHANNEL A,B.

DDRII A CHANNEL



DDRII B CHANNEL



Quanta Computer Inc.

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	DDR2 RES.ARRAY	A

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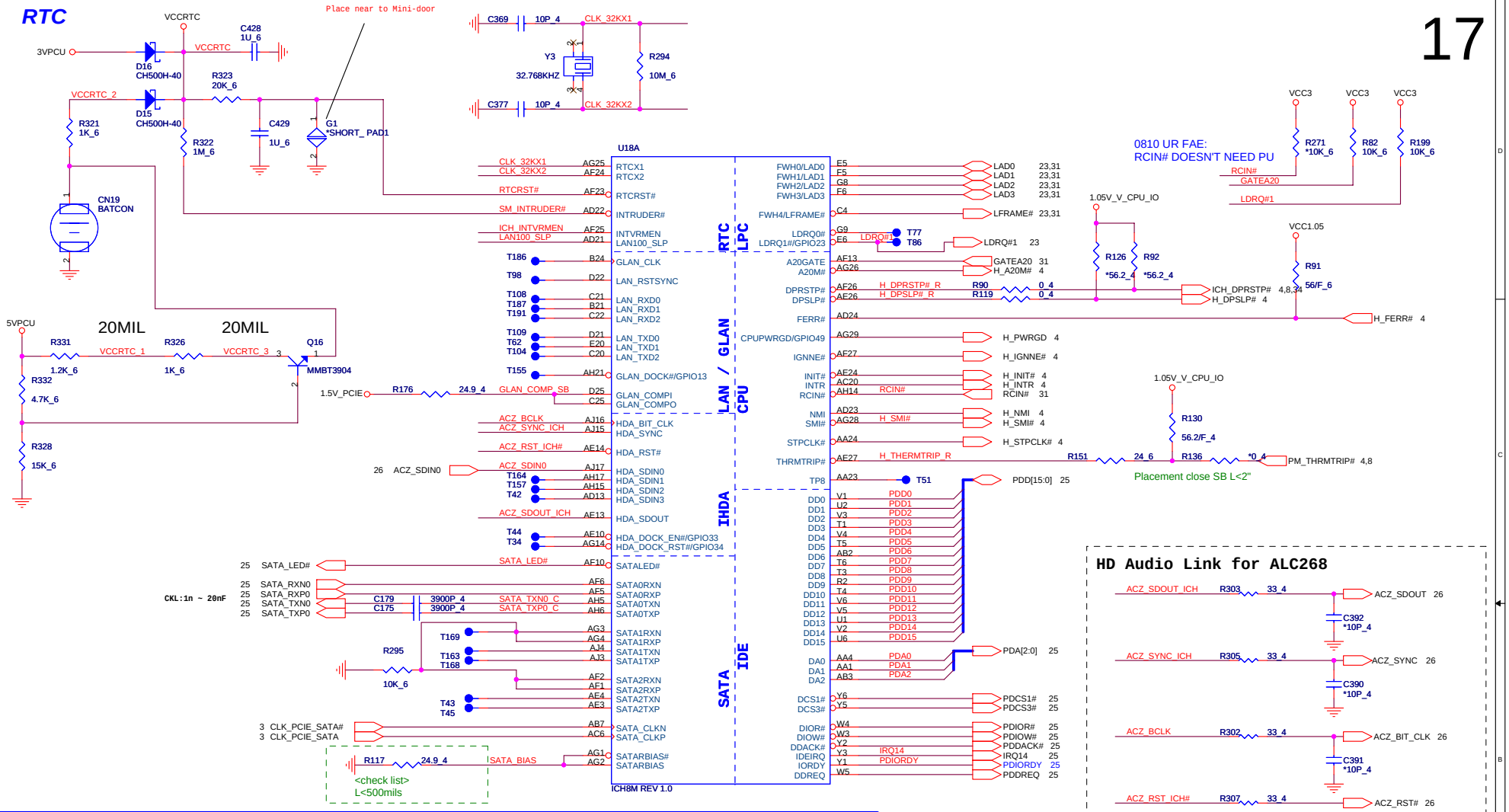
RTC



SB Strap

Internal VR Enable :
VccSus1.05,VccSus1.5,VccCL1.5

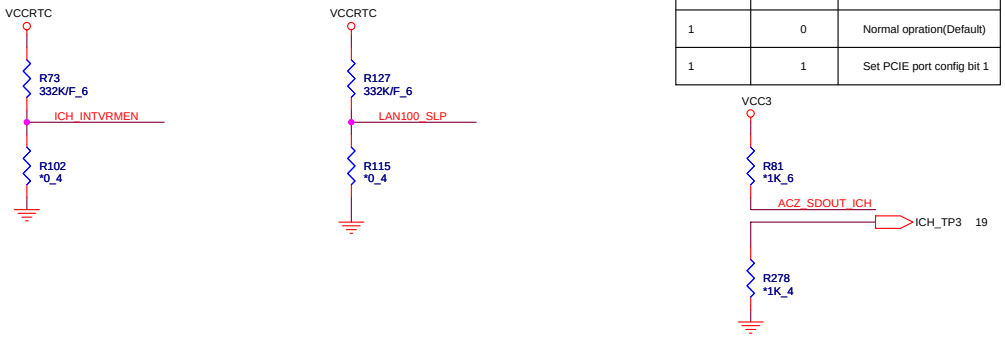
INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)

Internal VR Enable :
VccLAN1.05,VccCL1.05

LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)

XOR Chain Entrance Strap

ICH_RSV0	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1



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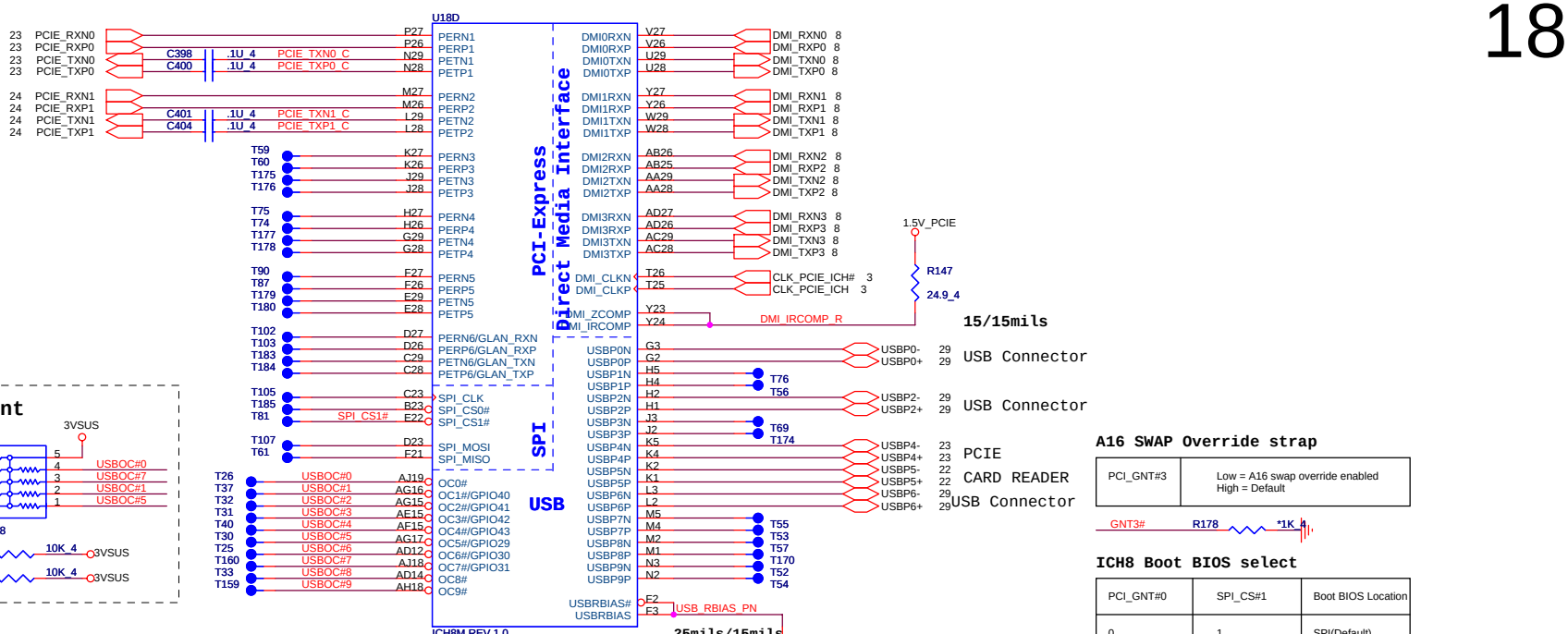
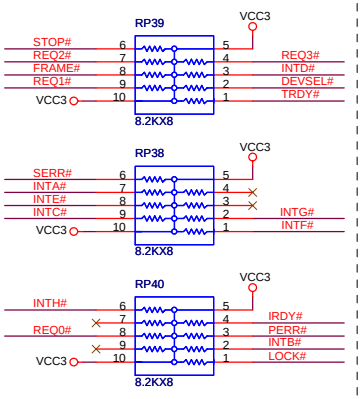
MINI CARD PCI-E

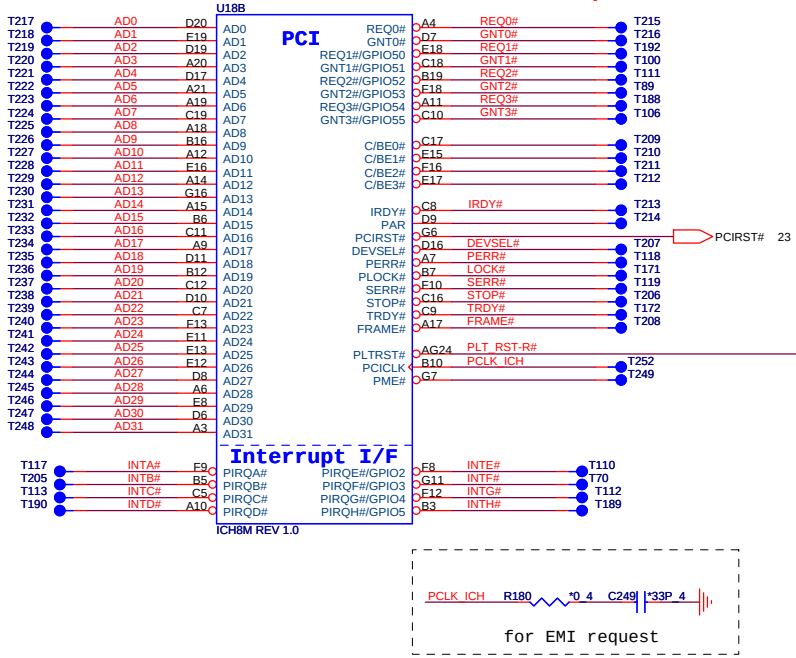
PCIE-LAN



USB OverCurrent

PCI Pull-High





<CRB>
USB_RBIAS_PN<500mils

A16 SWAP Override strap

PCI_GNT#3	Low = A16 swap override enabled High = Default

GNT3# R178 *1K_4

ICH8 Boot BIOS select

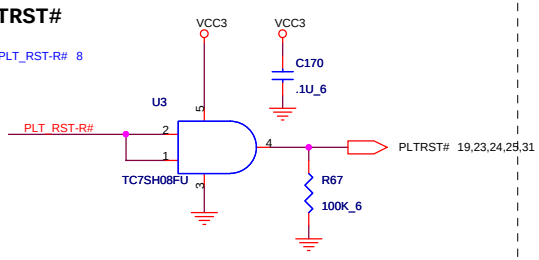
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC

SPI_CS1# R172 *1K_4

GNT0# R177 *1K_4

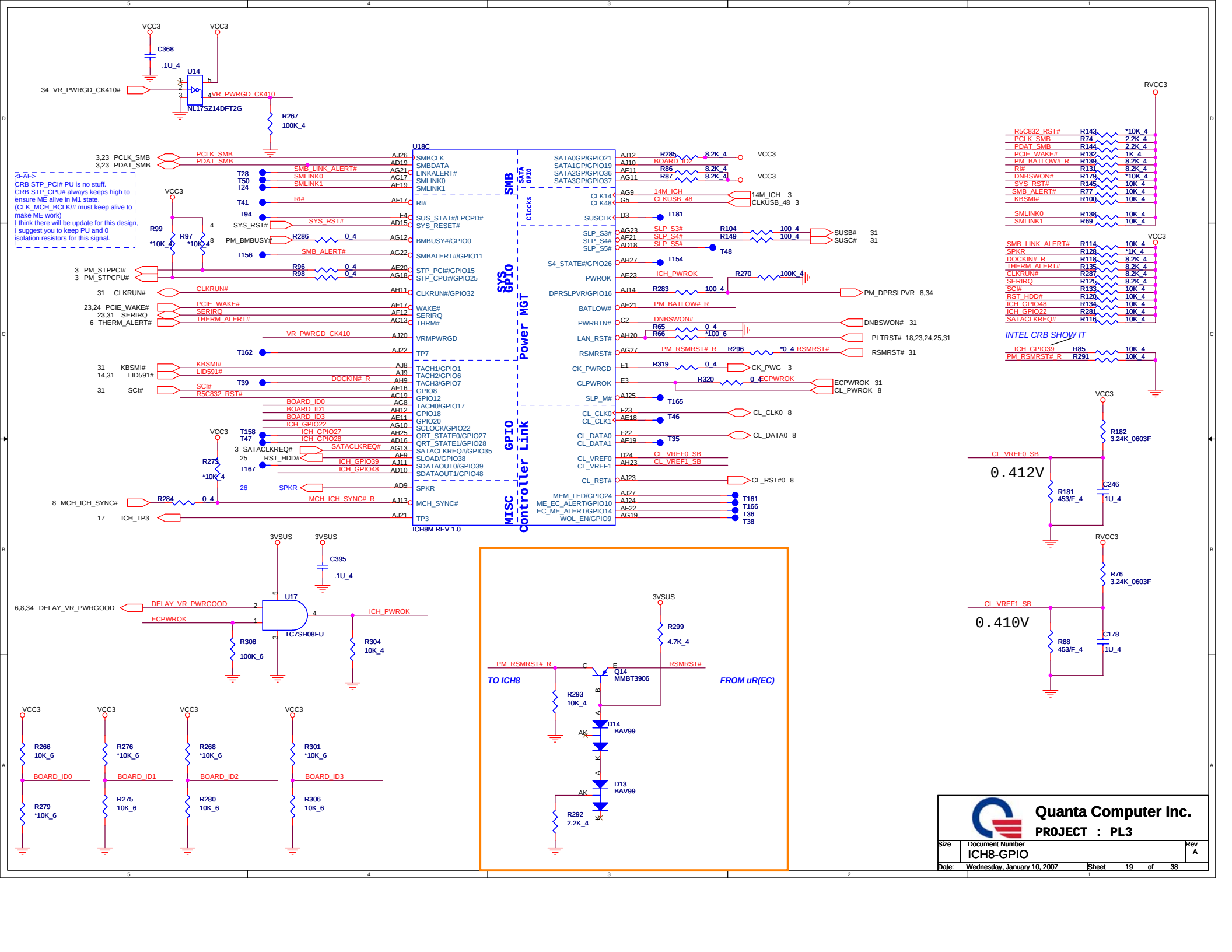
PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD17	INTA#,INTB#	R5C832

PLTRST#



PCLK_ICH R180 *0_4 C249 *33P_4

for EMI request


VCC3
C368
.1U_4
U14
NL17SZ14DFT2G
34 VR_PWRGD_CK410#
VR_PWRGD_CK410
R267
100K_4
U18C
ICH8M REV 1.0
SMB
SATA GPIO
Clocks
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
<FAE>
CRB STP_PCI# PU is no stuff.
CRB STP_CPU# always keeps high to ensure ME alive in M1 state.
(CLK_MCH_BCLK/# must keep alive to make ME work)
I think there will be update for this design, I suggest you to keep PU and 0 isolation resistors for this signal.
3,23 PCLK_SMB
3,23 PDAT_SMB
PCLK_SMB
PDAT_SMB
SMB_LINK_ALERT#
SMLINK0
SMLINK1
RI#
SYS_RST#
PM_BMBUSY#
SMB_ALERT#
R286
R99
R97
*10K_4
R96
R98
3 PM_STPPCI#
3 PM_STPCPU#
31 CLKRUN#
CLKRUN#
23,24 PCIE_WAKE#
23,31 SERIRQ
6 THERM_ALERT#
PCIE_WAKE#
SERIRQ
THERM_ALERT#
VR_PWRGD_CK410
31 KBSMI#
14,31 LID591#
KBSMI#
LID591#
31 SCI#
SCI#
R5C832_RST#
DOCKIN#_R
BOARD_ID0
BOARD_ID1
BOARD_ID2
BOARD_ID3
ICH_GPIO22
ICH_GPIO27
ICH_GPIO28
3 SATACLKREQ#
SATACLKREQ#
25 RST_HDD#
ICH_GPIO39
ICH_GPIO48
R275
26 SPKR
R284
8 MCH_ICH_SYNC#
MCH_ICH_SYNC#_R
17 ICH_TP3
SMBCLK
SMBDATA
LINKALERT#
SMLINK0
SMLINK1
RI#
SUS_STAT#/LPCPD#
SYS_RESET#
BMBUSY#/GPIO0
SMBALERT#/GPIO11
STP_PCI#/GPIO15
STP_CPU#/GPIO25
CLKRUN#/GPIO32
WAKE#
SERIRQ
THRM#
VRMPWRGD
TP7
TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
GPIO8
GPIO12
TACH0/GPIO17
GPIO18
GPIO20
SCLOCK/GPIO22
QRT_STATE0/GPIO27
QRT_STATE1/GPIO28
SATACLKREQ#/GPIO35
SLOAD/GPIO38
SDATAOUT0/GPIO39
SDATAOUT1/GPIO48
SPKR
MCH_SYNC#
TP3
SATA0GP/GPIO21
SATA1GP/GPIO19
SATA2GP/GPIO36
SATA3GP/GPIO37
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
S4_STATE#/GPIO26
PWROK
DPRSLPVR/GPIO16
BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
CK_PWRGD
CLPWROK
SLP_M#
CL_CLK0
CL_CLK1
CL_DATA0
CL_DATA1
CL_VREF0
CL_VREF1
CL_RST#
MEM_LED/GPIO24
ME_EC_ALERT/GPIO10
EC_ME_ALERT/GPIO14
WOL_EN/GPIO9
R285
BOARD_ID2
R86
R87
8.2K_4
14M_ICH
CLKUSB_48
T181
SLP_S3#
SLP_S4#
R104
R149
100_4
SUSB#
SUSC#
T48
T154
ICH_PWROK
R270
100K_4
PM_DPRSLPVR 8,34
PM_BATLOW#_R
DNBSWON#
R65
R66
0_4
*100_6
PLTRST# 18,23,24,25,31
PM_RSMRST#_R
R296
*0_4
RSMRST#
RSMRST# 31
R319
CK_PWG 3
R320
ECPWROK
ECPWROK 31
CL_PWROK 8
T165
CL_CLK0 8
T46
CL_DATA0 8
T35
CL_VREF0_SB
CL_VREF1_SB
CL_RST#0 8
T161
T166
T36
T38
R5C832_RST#
PCLK_SMB
PDAT_SMB
PCIE_WAKE#
PM_BATLOW#_R
RI#
DNBSWON#
SYS_RST#
SMB_ALERT#
KBSMI#
SMLINK0
SMLINK1
SMB_LINK_ALERT#
SPKR
DOCKIN#_R
THERM_ALERT#
CLKRUN#
SERIRQ
SCI#
RST_HDD#
ICH_GPIO48
ICH_GPIO22
SATACLKREQ#
INTEL CRB SHOW IT
ICH_GPIO39
PM_RSMRST#_R
R182
3.24K_0603F
0.412V
R181
453/F_4
C246
.1U_4
R76
3.24K_0603F
0.410V
R88
453/F_4
C178
.1U_4
3VSUS
C395
U17
TC7SH08FU
6,8,34 DELAY_VR_PWRGOOD
DELAY_VR_PWRGOOD
ECPWROK
ICH_PWROK
R308
100K_6
R304
10K_4
R299
4.7K_4
PM_RSMRST#_R
RSMRST#
TO ICH8
FROM uR(EC)
Q14
MMBT3906
R293
10K_4
D14
BAV99
D13
BAV99
R292
2.2K_4
R266
10K_6
R279
*10K_6
R276
*10K_6
R275
10K_6
R268
*10K_6
R280
10K_6
R301
*10K_6
R306
10K_6
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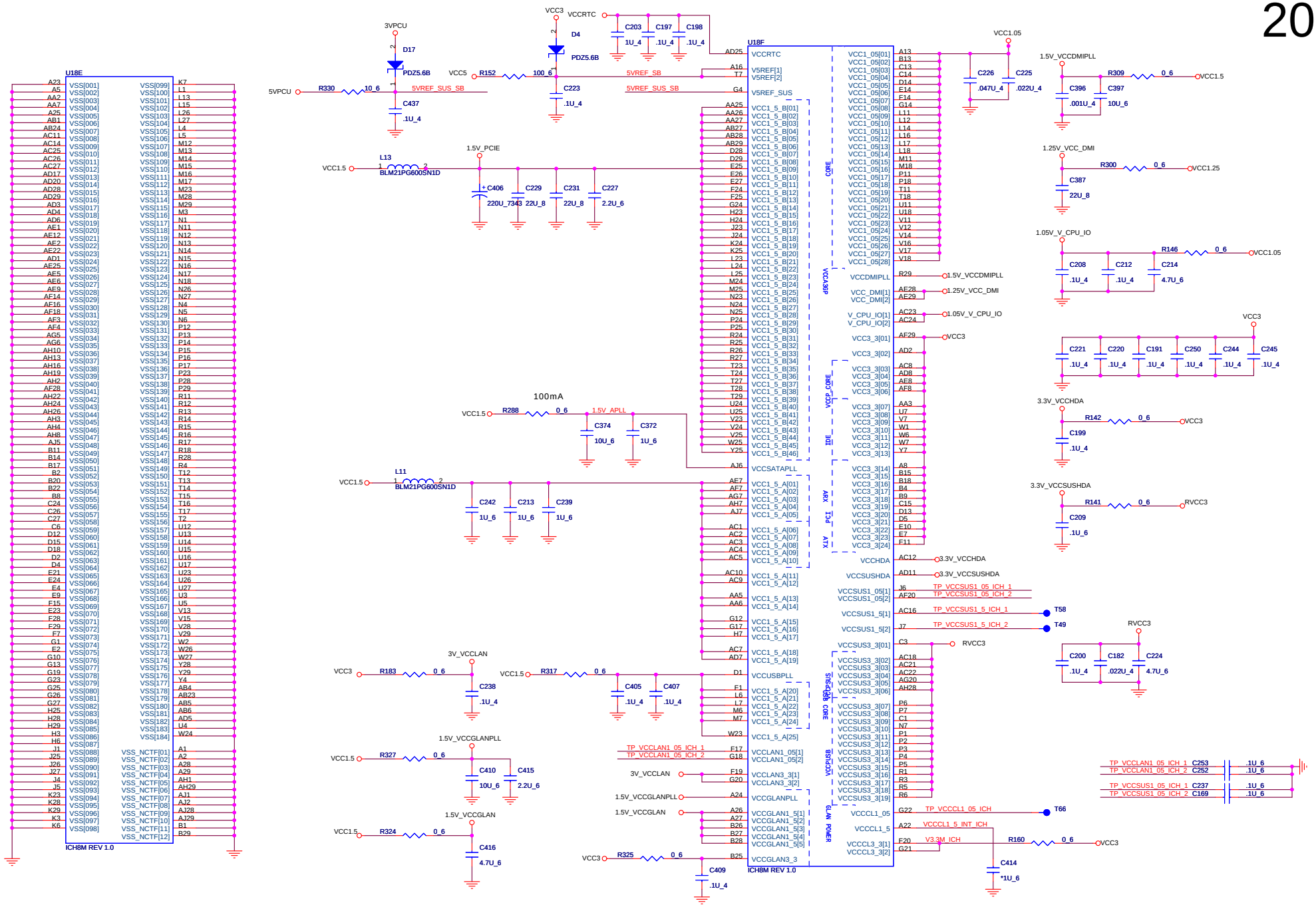

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Quanta Computer Inc.

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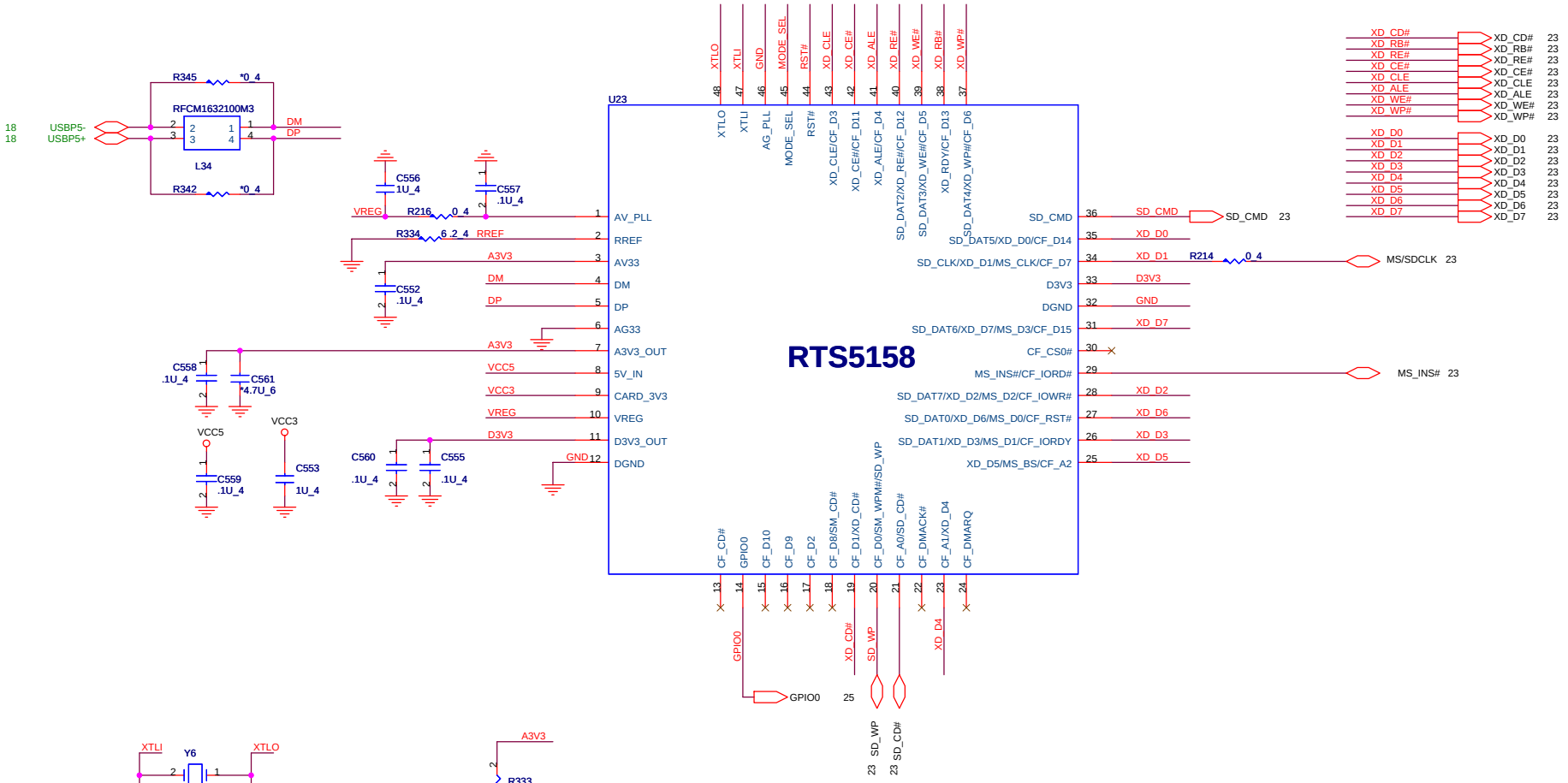

C564 can't be Mounted, reserved for future

Quanta Computer Inc.		
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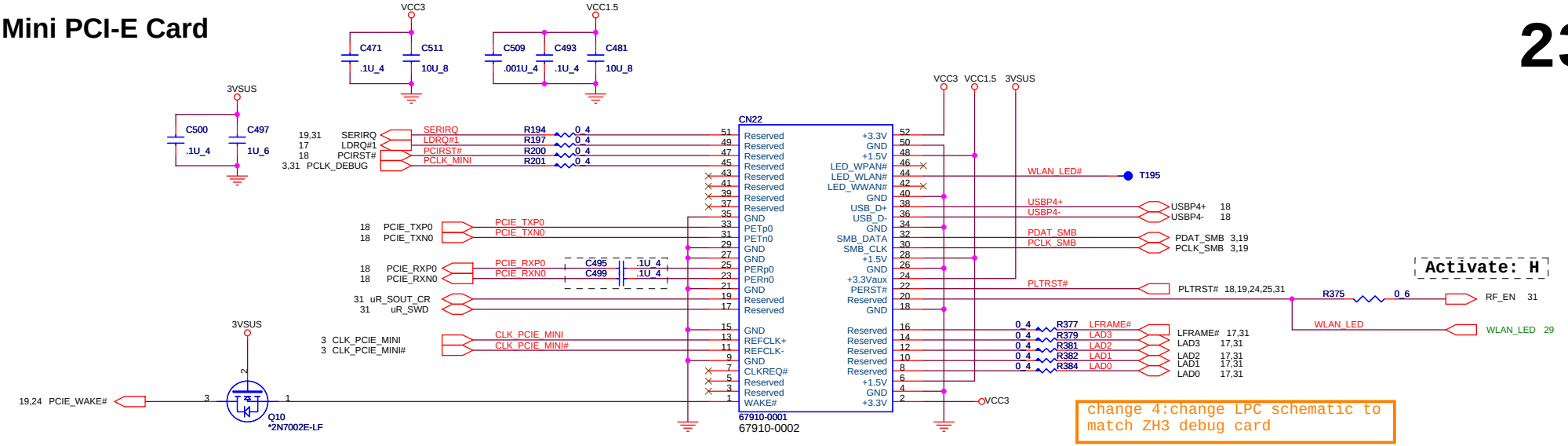
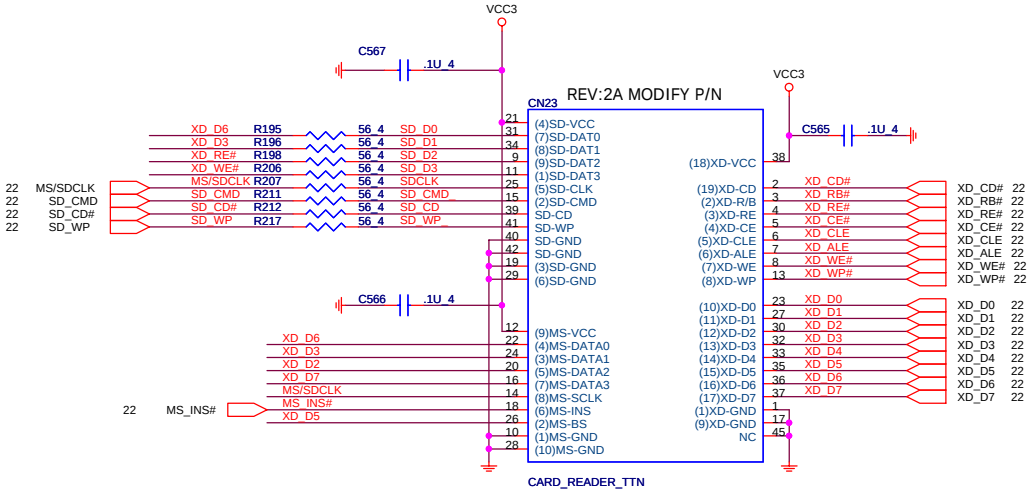
Mini PCI-E Card





	MDIO00	MDIO01
SD/MMC	L	H
MS	H	L
xD	L	L

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	R5C832-4 IN 1/MINI PCIE	A

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change to DB0EW5LAN02 C- TEST_1/11

TW3 final:0.1u

88E8039/88E8055

MARVELL

U22

U10 NS0013LF

U7 24LC08BT-I

CN8 RJ45-C100F8-100B-8P-L

Q19 BCP69T1

Q17 BCP69T1

Y5 25MHz

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	PCIE LAN 10/100M MARVELL 88E8039	A

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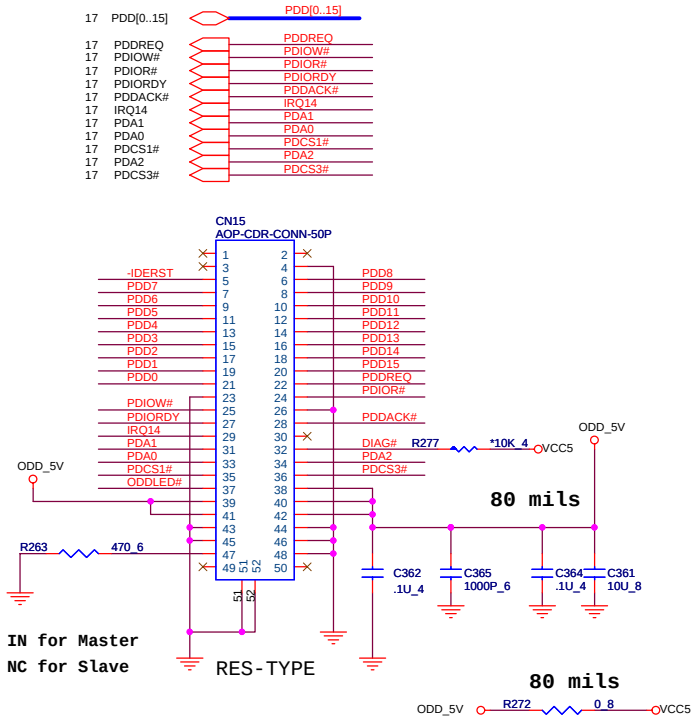
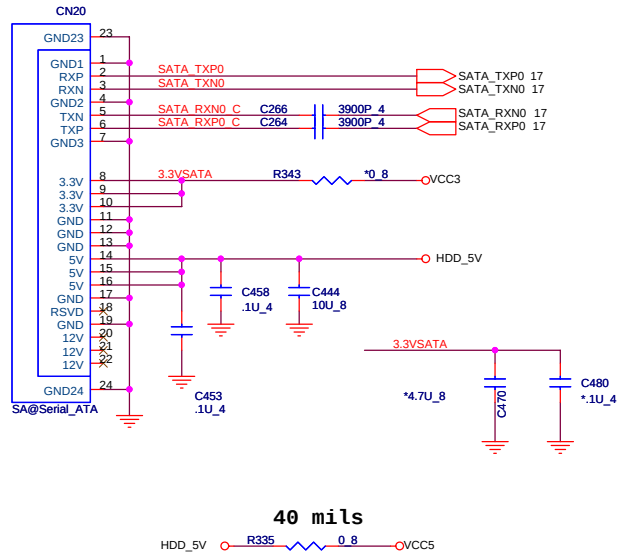
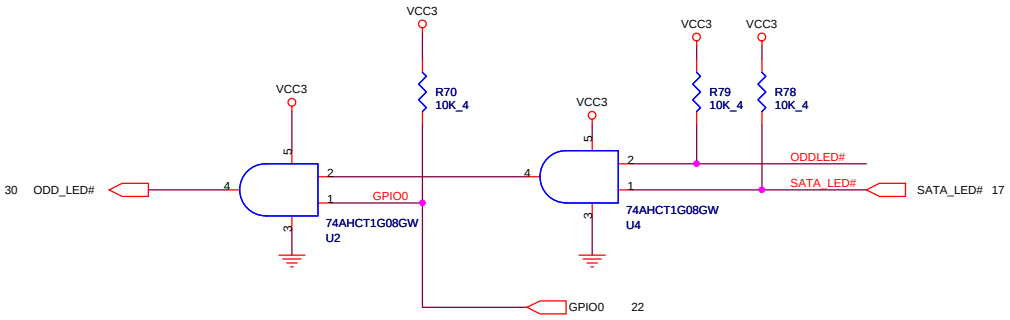
ODD

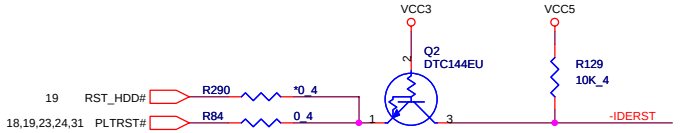


SATA HDD



HDD/ODD/cardreader LED





Quanta Computer Inc.

PROJECT : PL3

Size	Document Number	Rev
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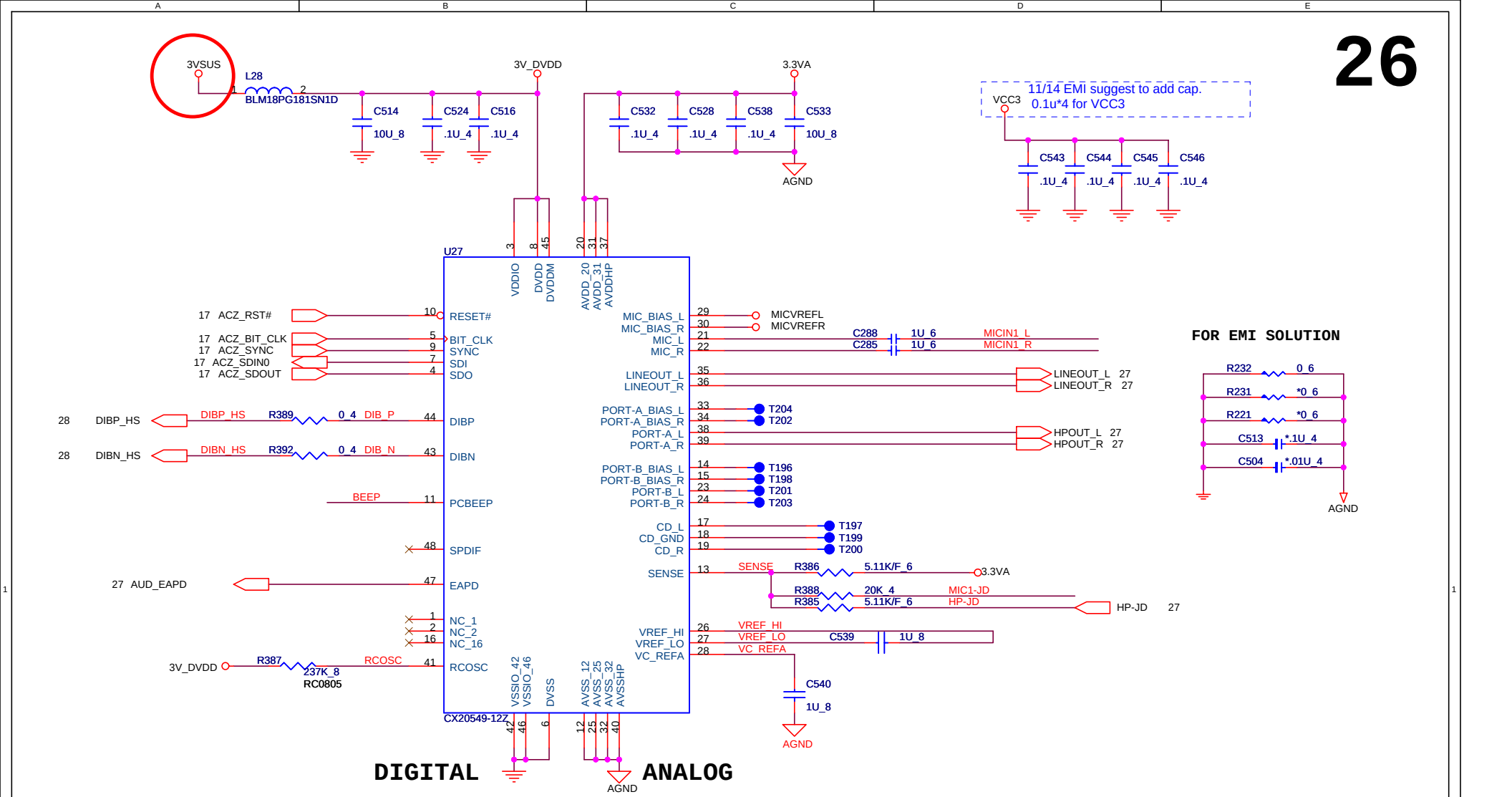
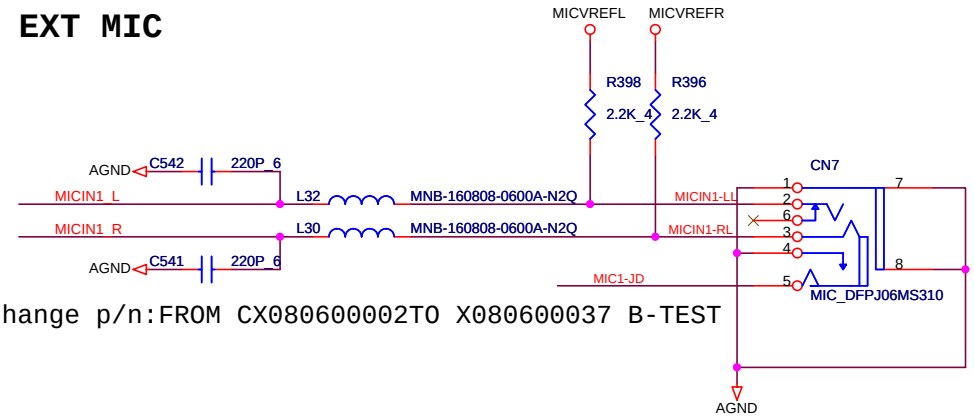
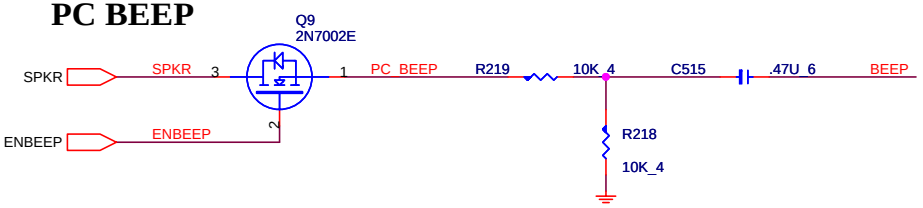


EXT MIC



change p/n:FROM CX080600002TO X080600037 B-TEST

PC BEEP



Quanta Computer Inc.

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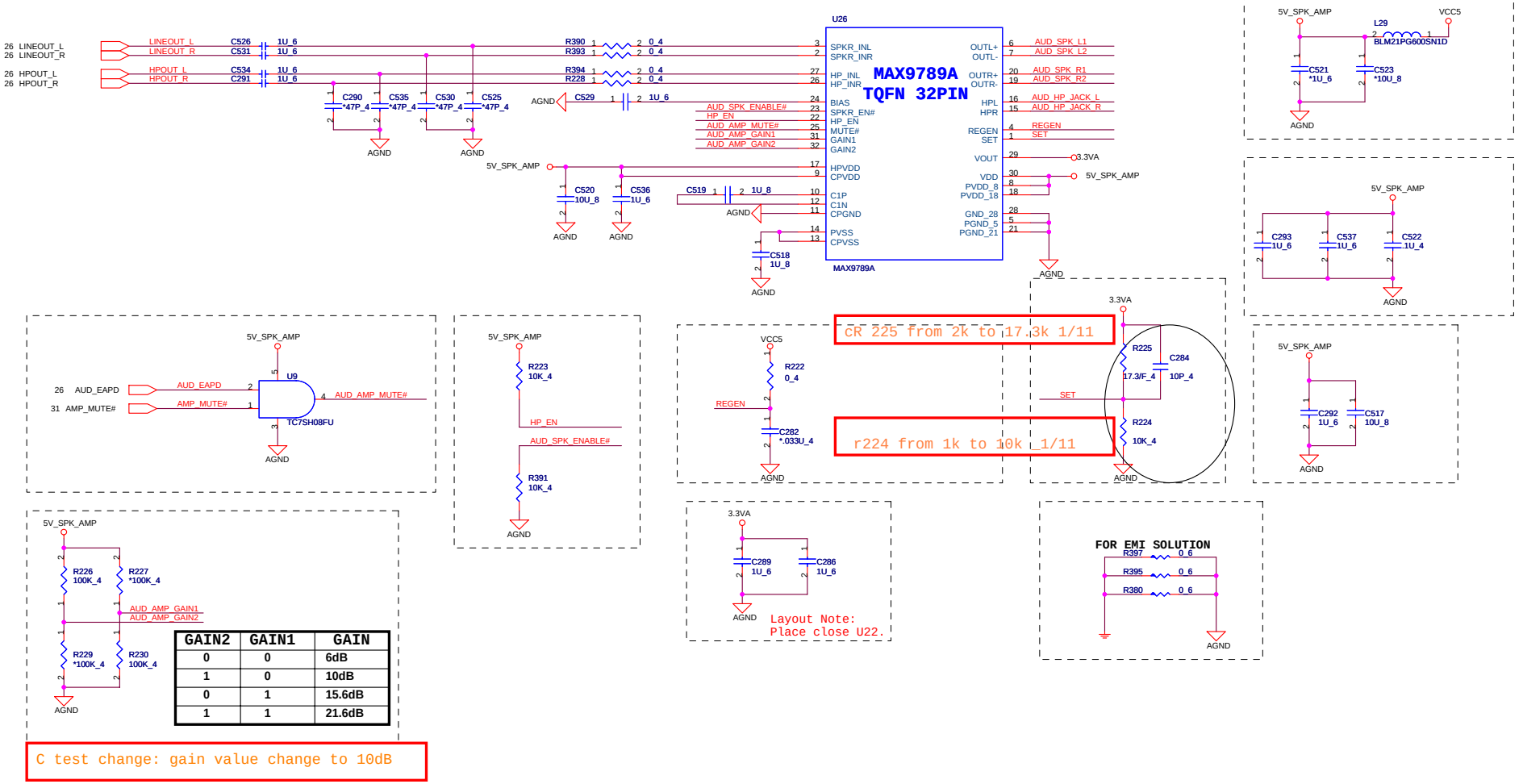
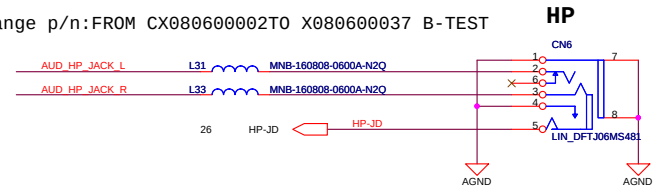
AUDIO AMPLIFIER



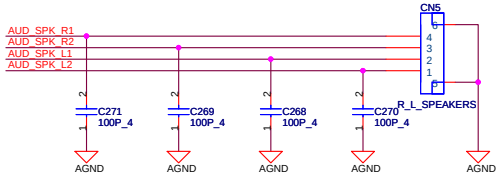
GAIN2	GAIN1	GAIN
0	0	6dB
1	0	10dB
0	1	15.6dB
1	1	21.6dB

Headphone out

change p/n:FROM CX080600002TO X080600037 B-TEST



Int. Stereo Speakers



Quanta Computer Inc.

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	AMP MAX9789A	A

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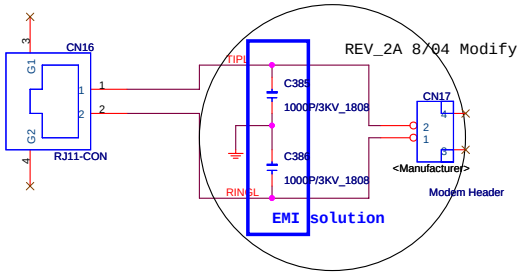
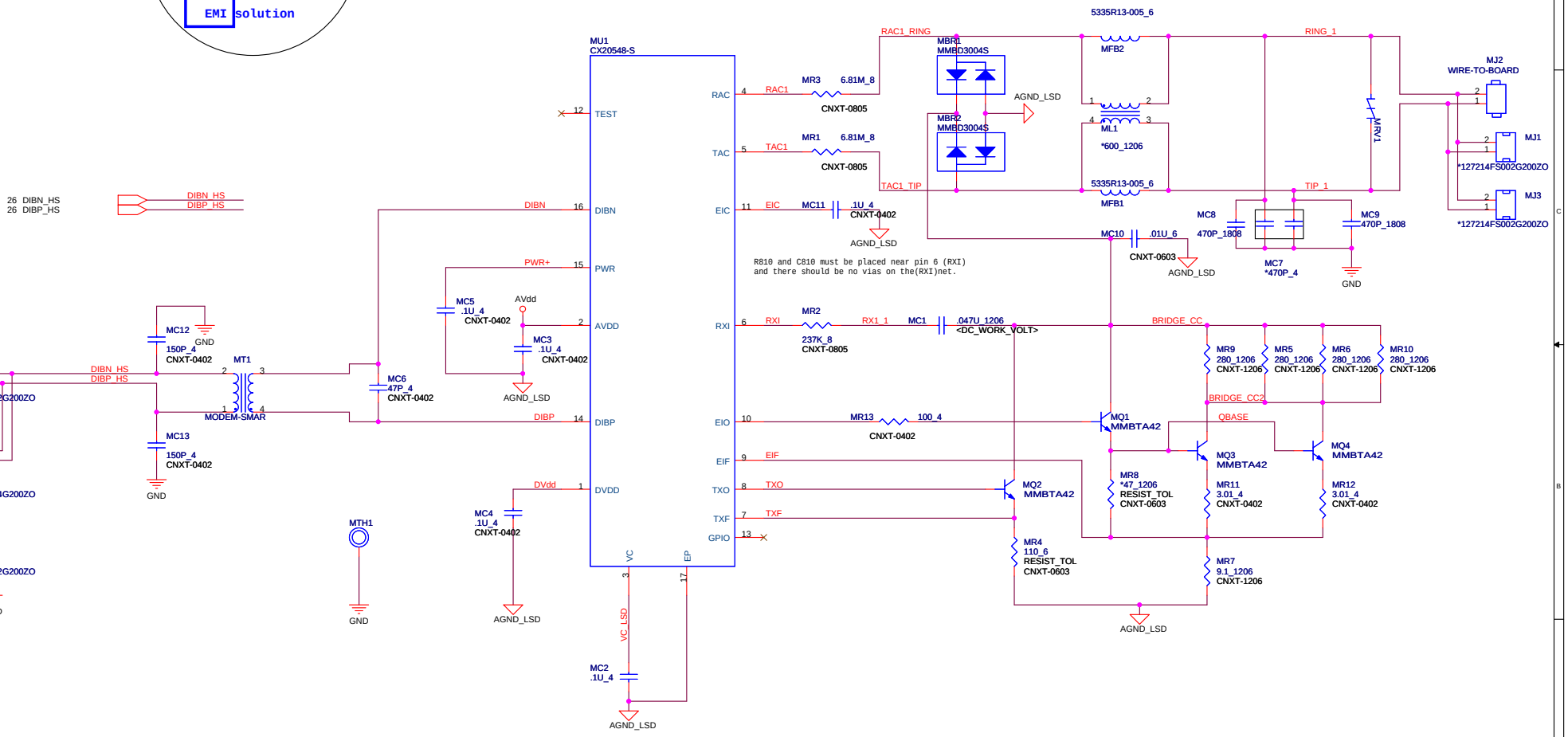


REV_2A 8/04 Modify



Quanta Computer Inc.	
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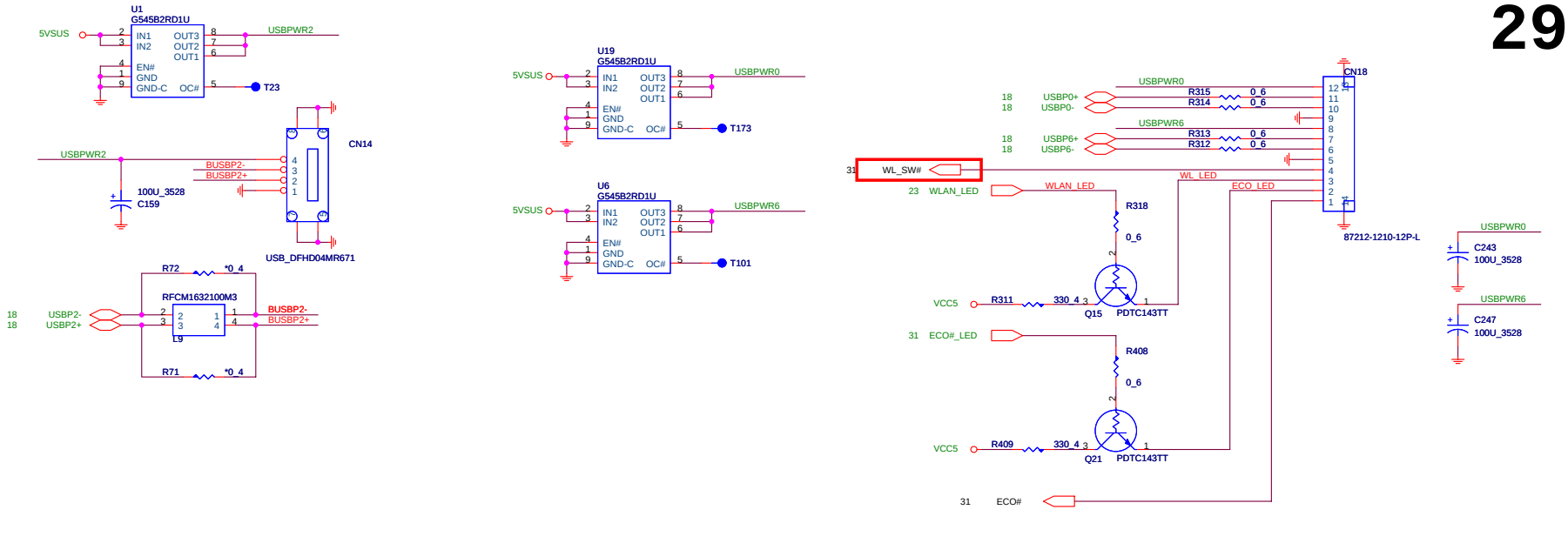
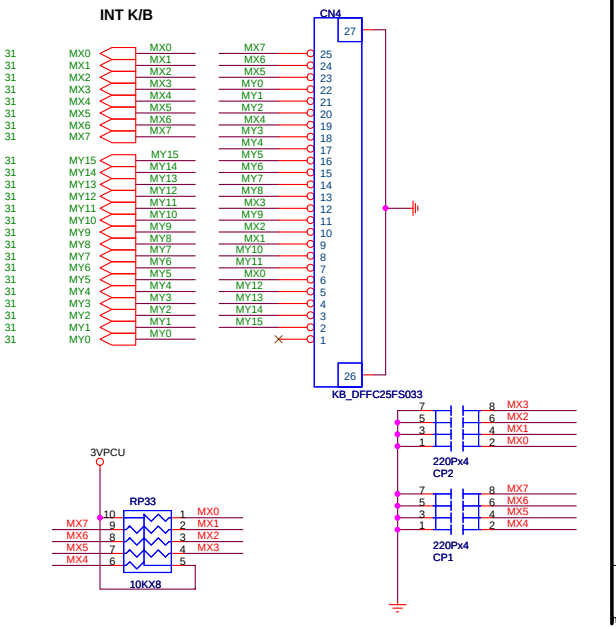
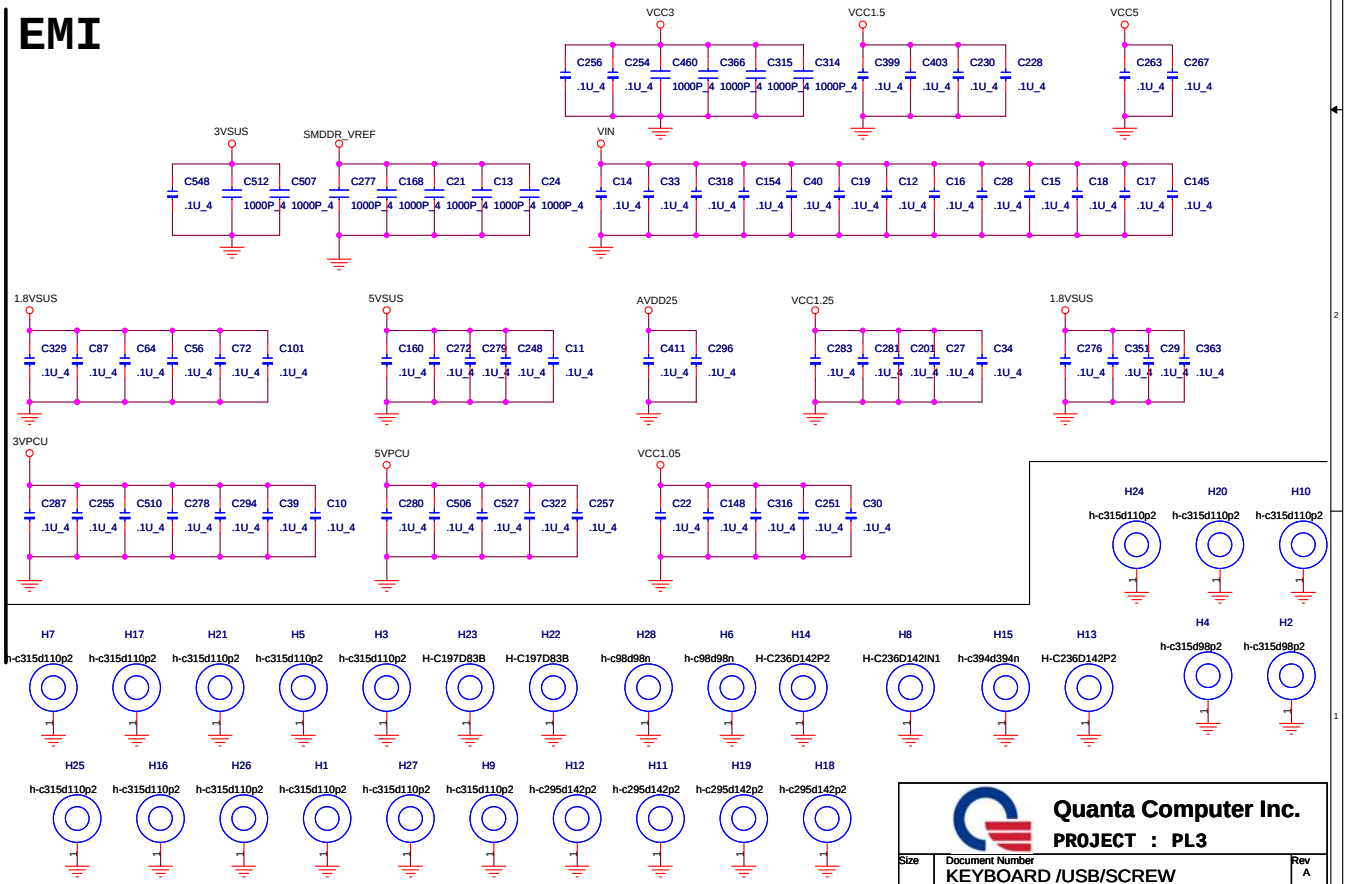
USB



INT KeyBoard



EMI



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	KEYBOARD /USB/SCREW	A

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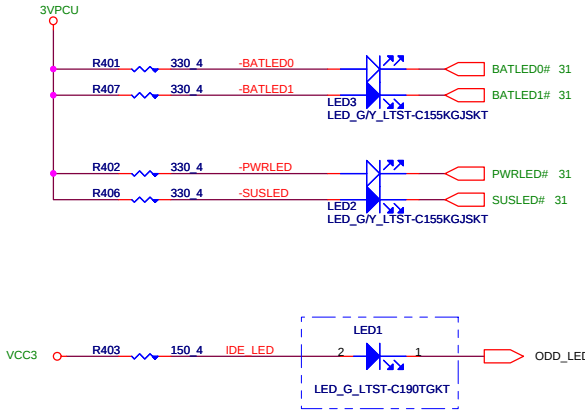
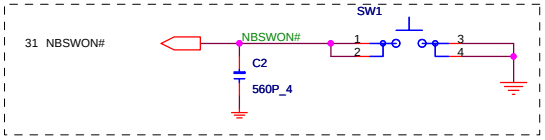
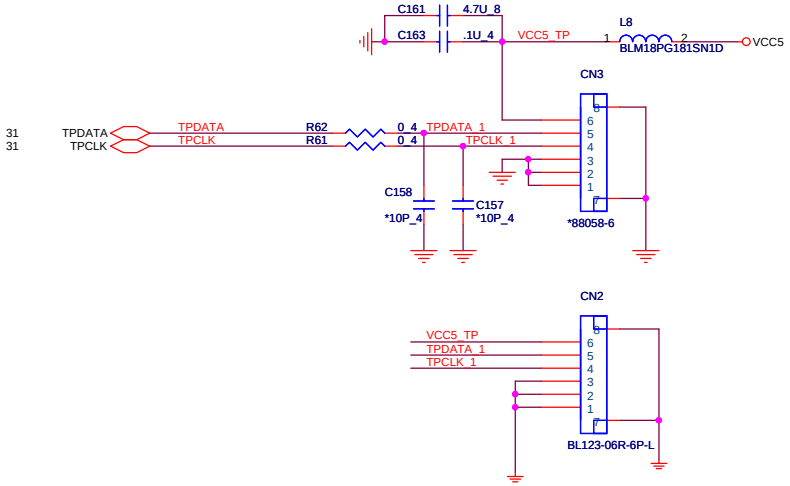
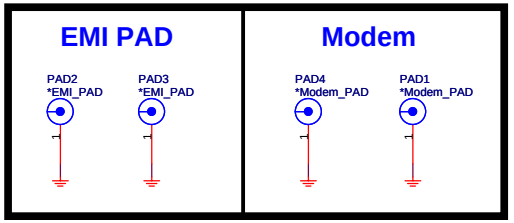






REV_2A 8/03 Add 2'nd source



Quanta Computer Inc.

PROJECT : PL3

Size	Document Number	Rev
	TP/SW	A

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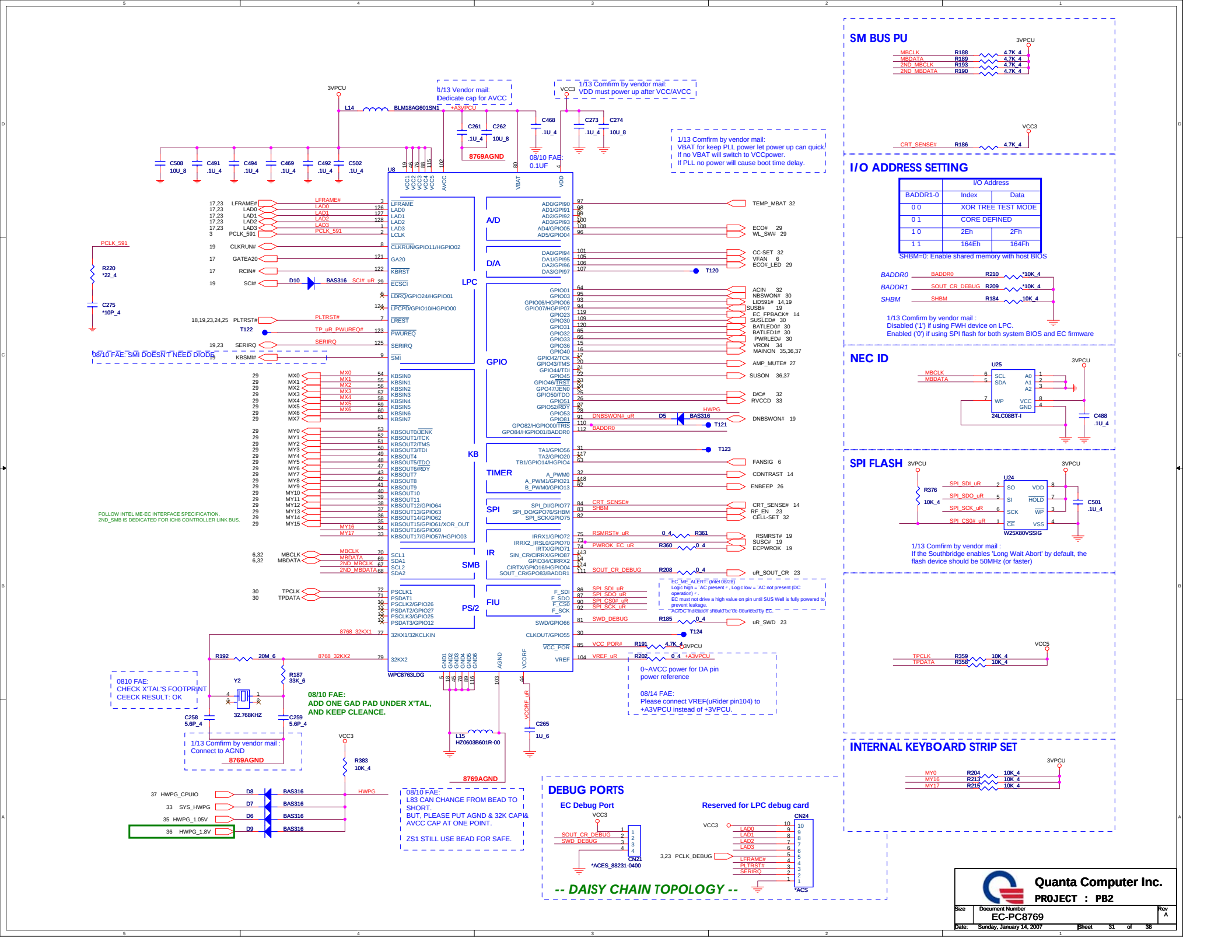
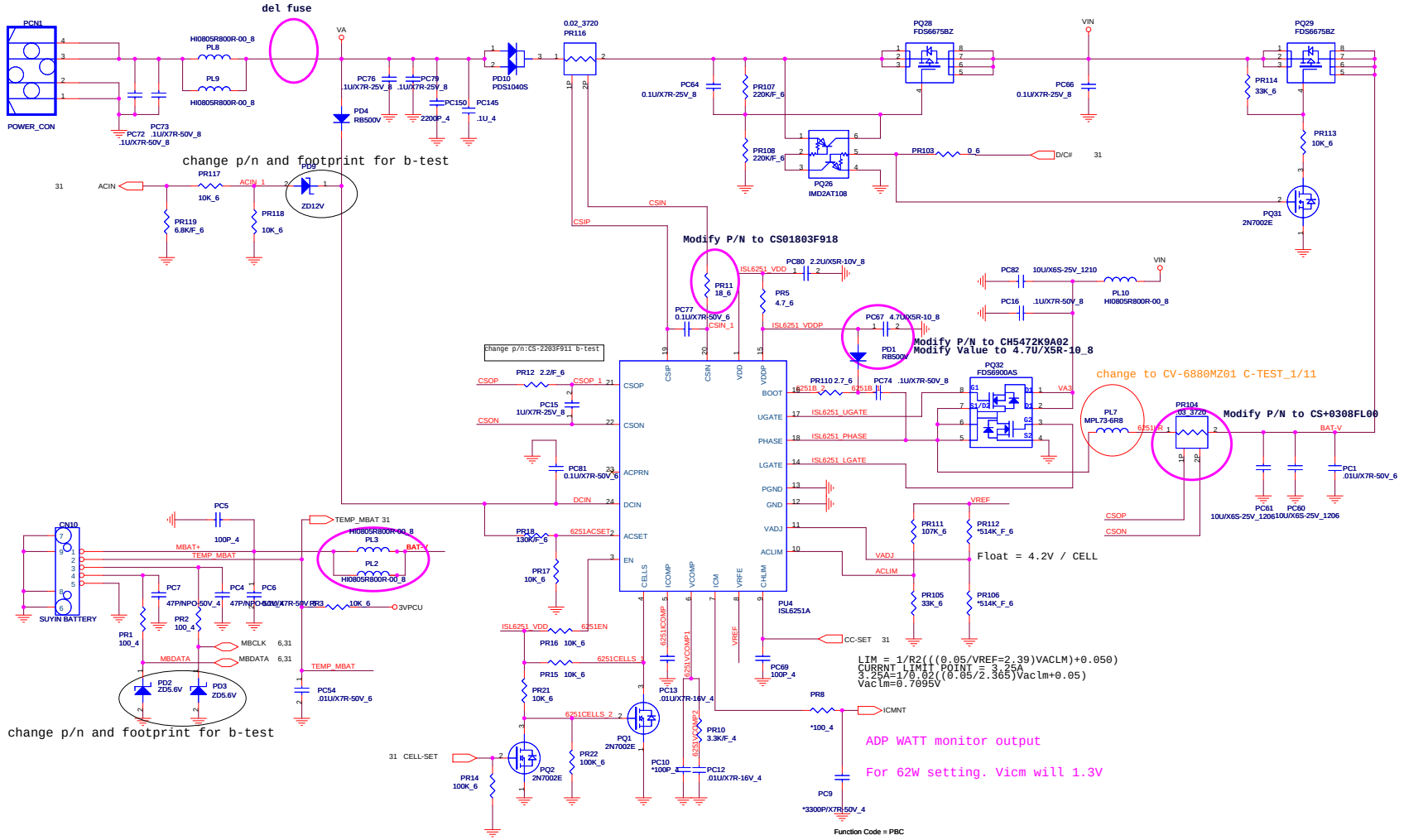
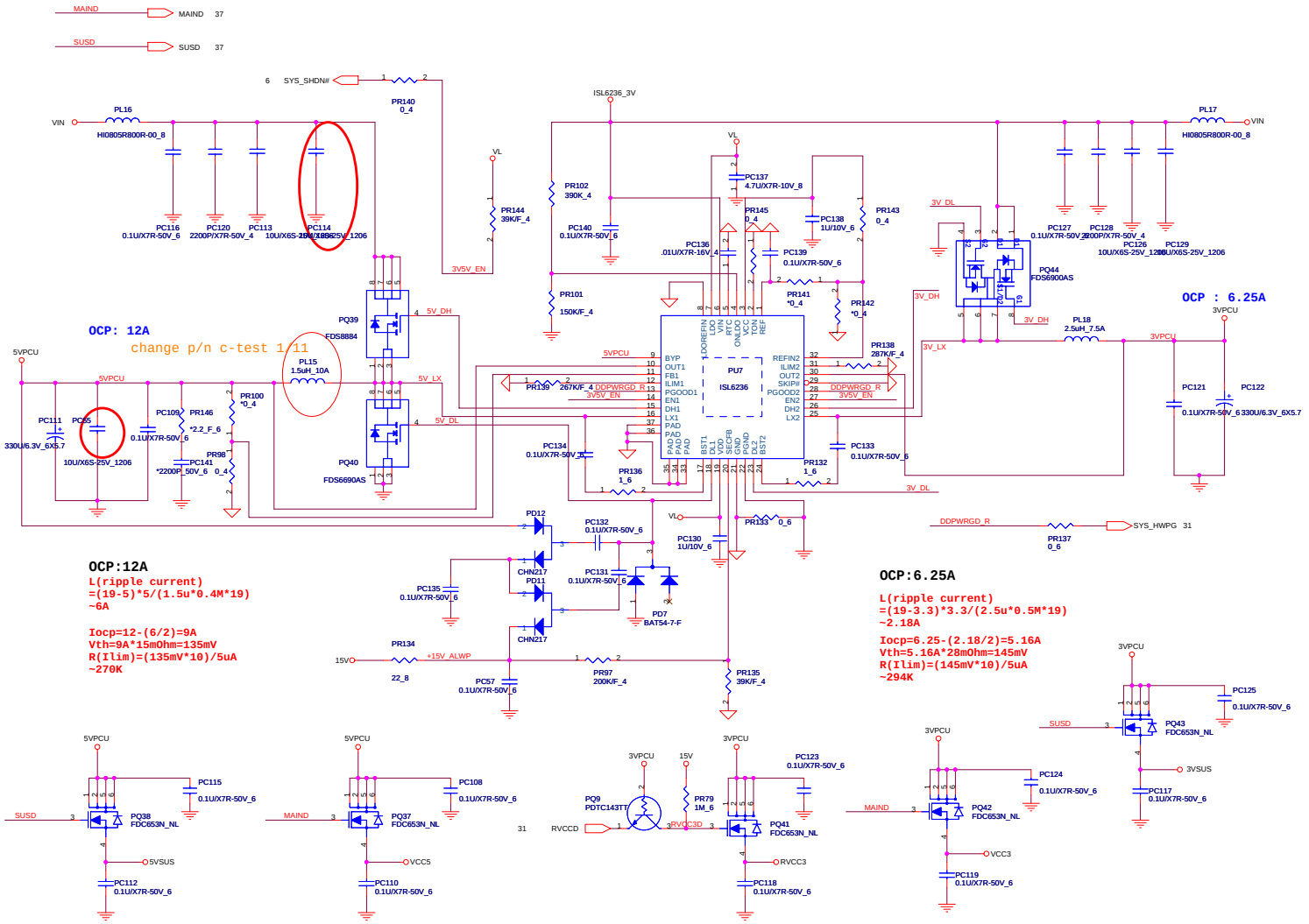

SM BUS PU
3VPCU
MBCLK R188 4.7K_4
MBDATA R189 4.7K_4
2ND_MBCLK R193 4.7K_4
2ND_MBDATA R190 4.7K_4
CRT_SENSE# R186 4.7K_4
VCC3
I/O ADDRESS SETTING
I/O Address
BADDR1-0 | Index | Data
0 0 | XOR TREE TEST MODE
0 1 | CORE DEFINED
1 0 | 2Eh | 2Fh
1 1 | 164Eh | 164Fh
SHBM=0: Enable shared memory with host BIOS
BADDR0 BADDR0 R210 *10K_4
BADDR1 SOUT_CR_DEBUG R209 *10K_4
SHBM SHBM R184 10K_4
1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware
NEC ID
U25
MBCLK
MBDATA
SCL
SDA
A0
A1
A2
WP
VCC
GND
24LC08BT-I
C488 .1U_4
SPI FLASH
R376 10K_4
SPI_SDI_uR
SPI_SDO_uR
SPI_SCK_uR
SPI_CS0#_uR
U24
SO
SI
SCK
CE
VDD
HOLD
WP
VSS
W25X80VSSIG
C501 .1U_4
1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)
TPCLK R359 10K_4
TPDATA R358 10K_4
VCC5
INTERNAL KEYBOARD STRIP SET
MY0 R204 10K_4
MY16 R213 10K_4
MY17 R215 10K_4
1/13 Vendor mail:
Dedicate cap for AVCC
1/13 Comfirm by vendor mail:
VDD must power up after VCC/AVCC
1/13 Comfirm by vendor mail:
VBAT for keep PLL power let power up can quick
If no VBAT will switch to VCCpower.
If PLL no power will cause boot time delay.
08/10 FAE:
0.1UF
L14 BLM18AG601SN1
C508 10U_8
C491 .1U_4
C494 .1U_4
C469 .1U_4
C492 .1U_4
C502 .1U_4
C261 .1U_4
C262 10U_8
8769AGND
C468 .1U_4
C273 .1U_4
C274 10U_8
U8
WPC8763LDG
LFRAME#
LAD0
LAD1
LAD2
LAD3
PCLK_591
CLKRUN#
GA20
KBRST
ECSCI
LDRQ/GPIO24/HGPIO01
LPCPD/GPIO10/HGPIO00
LRESET
PWUREQ
SERIRQ
SMI
LPC
A/D
D/A
GPIO
KB
TIMER
SPI
IR
SMB
PS/2
FIU
TEMP_MBAT 32
ECO# 29
WL_SW# 29
CC-SET 32
VFAN 6
ECO#_LED 29
T120
ACIN 32
NBSWON# 30
LID591# 14,19
SUSB# 19
EC_FPBACK# 14
SUSLED# 30
BATLED0# 30
BATLED1# 30
PWRLED# 30
VRON 34
MAINON 35,36,37
AMP_MUTE# 27
SUSON 36,37
D/C# 32
RVCCD 33
DNBSWON# uR
D5 BAS316
HWPG
DNBSWON# 19
BADDR0
T121
T123
FANSIG 6
CONTRAST 14
ENBEEP 26
CRT_SENSE# 14
SHBM
RF_EN 23
CELL-SET 32
RSMRST# uR
0_4
R361
RSMRST# 19
SUSC# 19
PWROK_EC_uR
R360
ECPWROK 19
SOUT_CR_DEBUG
R208
uR_SOUT_CR 23
SPI_SDI_uR
SPI_SDO_uR
SPI_CS0#_uR
SPI_SCK_uR
SWD_DEBUG
R185
uR_SWD 23
T124
VCC_POR#
R191 4.7K_4
VREF_uR
R202 0_4 +A3VPCU
0~AVCC power for DA pin power reference
08/14 FAE:
Please connect VREF(uRider pin104) to +A3VPCU instead of +3VPCU.
EC_ME_ALERT: (Intel 08/28)
Logic high = 'AC present', Logic low = 'AC not present (DC operation)'.
EC must not drive a high value on pin until SUS Well is fully powered to prevent leakage.
*ACDC indication should be the board by EC.
PCLK_591
R220 *22_4
C275 *10P_4
D10 BAS316
SCI#_uR
PLTRST#
T122
TP_uR_PWUREQ#
SERIRQ
KBSMI#
08/10 FAE: SMI DOESN'T NEED DIODE
FOLLOW INTEL ME-EC INTERFACE SPECIFICATION,
2ND_SMB IS DEDICATED FOR ICH8 CONTROLLER LINK BUS.
MX0
MX1
MX2
MX3
MX4
MX5
MX6
MX7
MY0
MY1
MY2
MY3
MY4
MY5
MY6
MY7
MY8
MY9
MY10
MY11
MY12
MY13
MY14
MY15
MY16
MY17
KBSOUT0/JENK
KBSOUT1/TCK
KBSOUT2/TMS
KBSOUT3/TDI
KBSOUT4
KBSOUT5/TDO
KBSOUT6/RDY
KBSOUT7
KBSOUT8
KBSOUT9
KBSOUT10
KBSOUT11
KBSOUT12/GPIO64
KBSOUT13/GPIO63
KBSOUT14/GPIO62
KBSOUT15/GPIO61/XOR_OUT
KBSOUT16/GPIO60
KBSOUT17/GPIO57/HGPIO03
MBCLK
MBDATA
2ND_MBCLK
2ND_MBDATA
TPCLK
TPDATA
PSCLK1
PSDAT1
PSCLK2/GPIO26
PSDAT2/GPIO27
PSCLK3/GPIO25
PSDAT3/GPIO12
8768_32KX1
32KX1/32CLKIN
32KX2
8768_32KX2
R192 20M_6
R187 33K_6
Y2
32.768KHZ
C258 5.6P_4
C259 5.6P_4
0810 FAE:
CHECK X'TAL'S FOOTPRINT
CEECK RESULT: OK
08/10 FAE:
ADD ONE GAD PAD UNDER X'TAL,
AND KEEP CLEANCE.
1/13 Comfirm by vendor mail :
Connect to AGND
8769AGND
L15 HZ0603B601R-00
C265 1U_6
VCORF_uR
AGND
VCORF
VREF
CLKOUT/GPIO55
VCC_POR
SWD/GPIO66
R383 10K_4
HWPG
D8 BAS316
D7 BAS316
D6 BAS316
D9 BAS316
37 HWPG_CPUIO
33 SYS_HWPG
35 HWPG_1.05V
36 HWPG_1.8V
08/10 FAE:
L83 CAN CHANGE FROM BEAD TO SHORT.
BUT, PLEASE PUT AGND & 32K CAP& AVCC CAP AT ONE POINT.
ZS1 STILL USE BEAD FOR SAFE.
DEBUG PORTS
EC Debug Port
SOUT_CR_DEBUG
SWD_DEBUG
CN21
*ACES_88231-0400
Reserved for LPC debug card
CN24
LAD0
LAD1
LAD2
LAD3
LFRAME#
PLTRST#
SERIRQ
PCLK_DEBUG
*ACS
-- DAISY CHAIN TOPOLOGY --
Quanta Computer Inc.
PROJECT : PB2
Size
Document Number
EC-PC8769
Rev A
Date: Sunday, January 14, 2007
Sheet 31 of 38



Quanta Computer Inc.			
PROJECT : PL3			
Size	Document Number		Rev
	ISL6251		A
Date: Thursday, January 11, 2007		Sheet 32 of 38	



Quanta Computer Inc.		
PROJECT : PL3		
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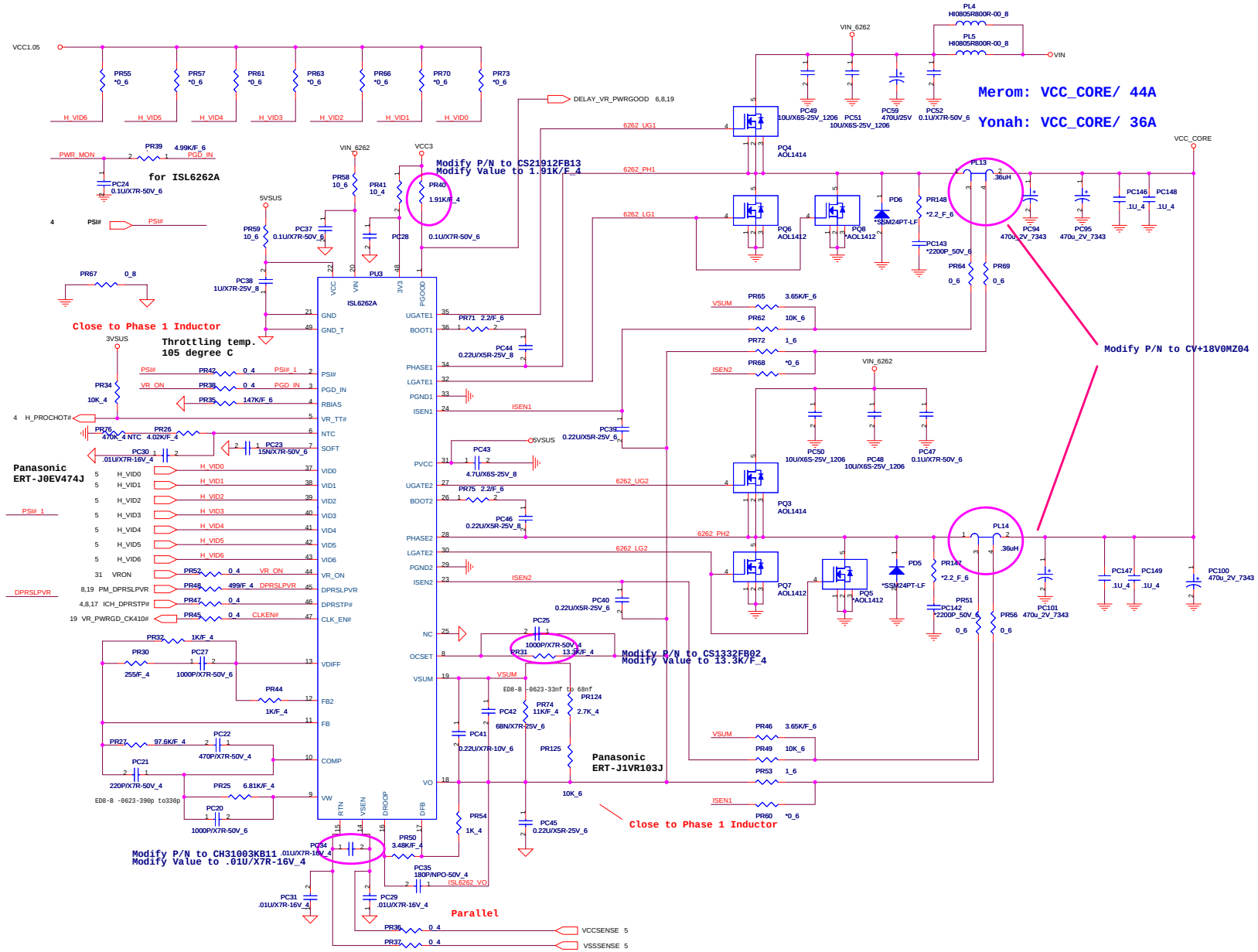
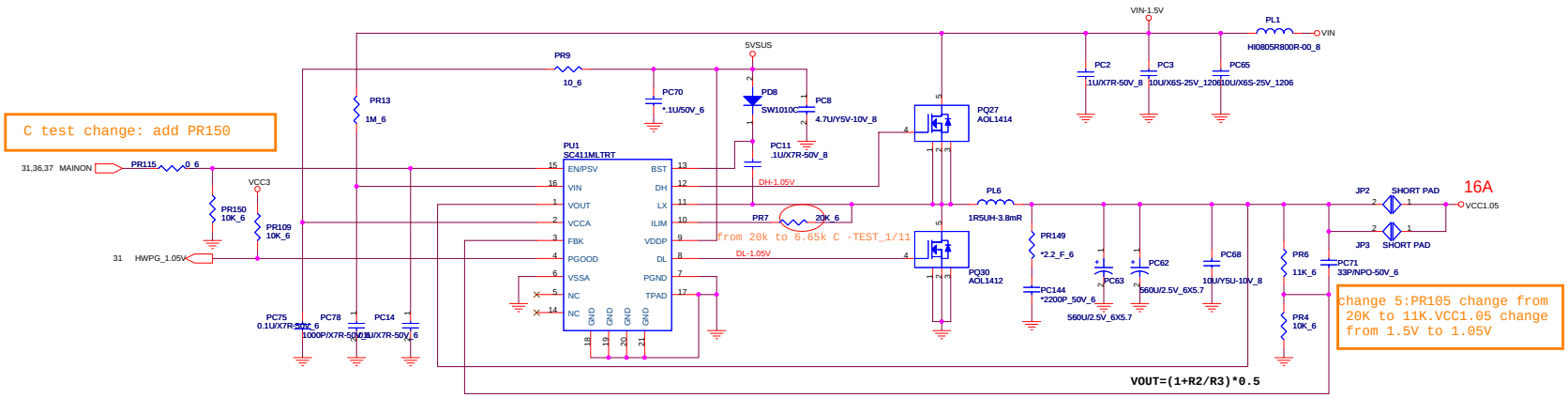

Merom: VCC_CORE/ 44A
Yonah: VCC_CORE/ 36A
for ISL6262A
Modify P/N to CS21912FB13
Modify Value to 1.91K/F_4
Close to Phase 1 Inductor
Throttling temp.
105 degree C
Panasonic
ERT-J0EV474J
Modify P/N to CV+18V0MZ04
Modify P/N to CS1332FB02
Modify Value to 13.3K/F_4
Panasonic
ERT-J1VR103J
Close to Phase 1 Inductor
Modify P/N to CH31003KB11
Modify Value to .01U/X7R-16V_4
Parallel
ISL6262A
Quanta Computer Inc.
PROJECT : PL3
CPU CAORE (6262A)
Wednesday, January 10, 2007



Quanta Computer Inc.		
PROJECT : PL3		
Size	Document Number: VTT 1.05V (SC11)	Rev: A
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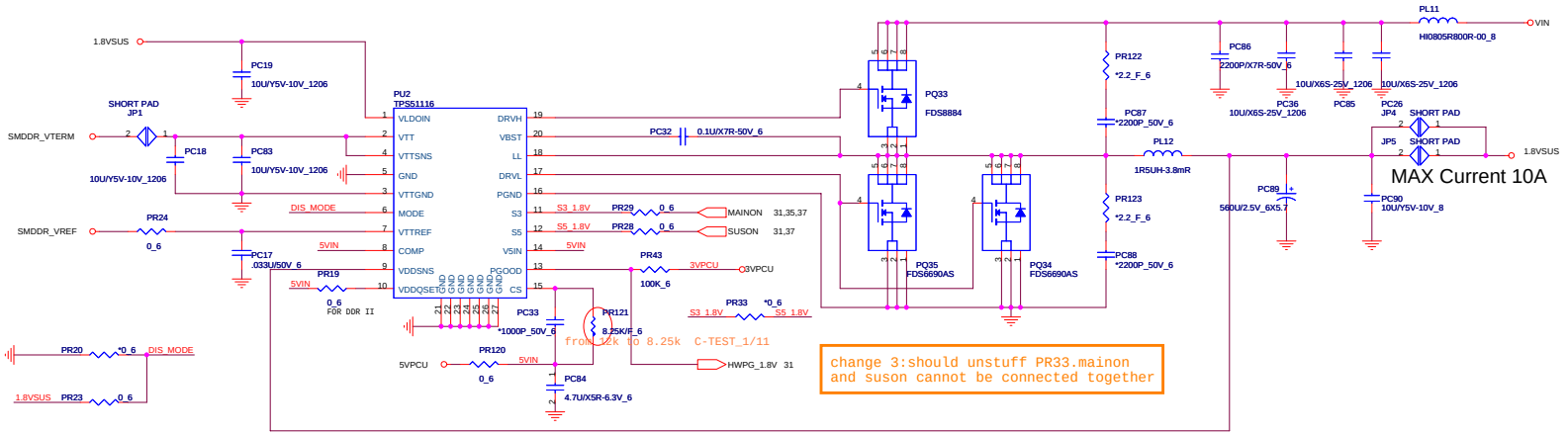

Quanta Computer Inc.		
PROJECT : PL3		
Size	Document Number: DDR2 1.8V(TP1116)	Rev: A
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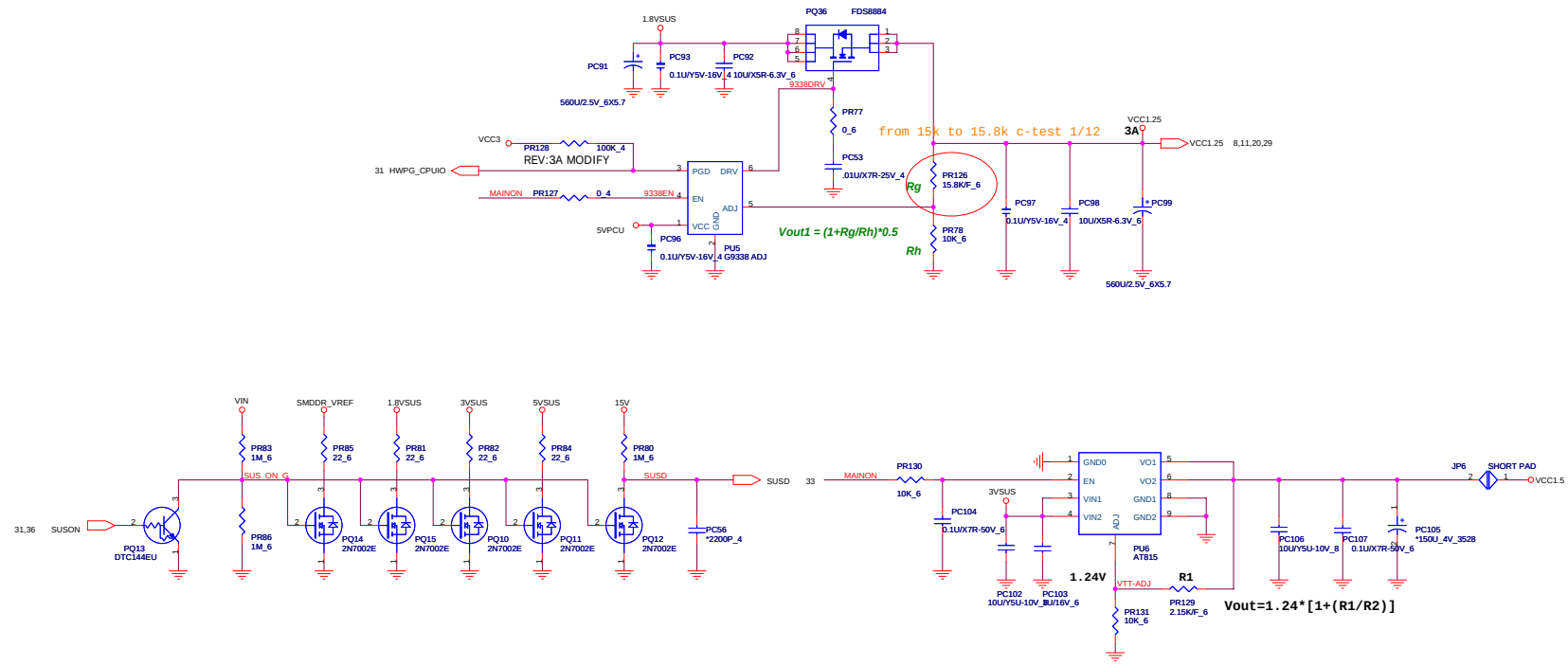

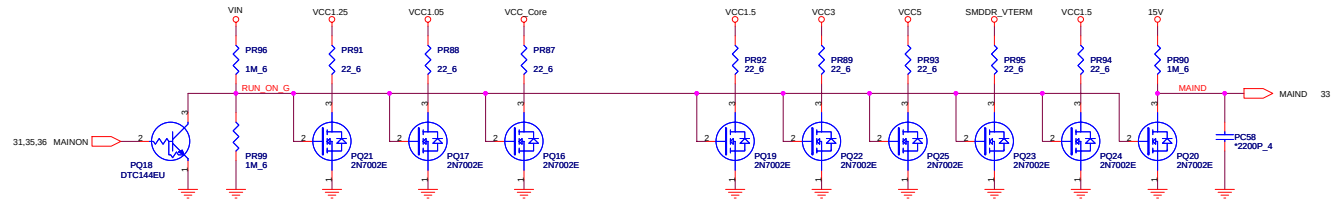

Quanta Computer Inc.

PROJECT : PL3

Size	Document Number	Rev
	DISCHARGE/1.5V/2.5V	A

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change1:SMBUS clock to data wrong connection

change2:change SMDDR_VTERM to SMDDR_VREF_DIMM in page 15
SMDDR_VREF_DIMM is from SMDDR_VREF;
wrong connection of SMDDR_VTERM and SMDDR_VREF

change 3:should unstuff PR114

change 4:change LPC schematic to
match ZH3 debug card

change 5:PR105 change from
20K to 11K.VCC1.05 change
from 1.5V to 1.05V

Title <Title>		
Size A	Document Number <Doc>	Rev <RevCo
Date: Wednesday, January 10, 2007	Sheet 38 of 38	