QL1 BLOCK DIAGRAM

PCB STACK UP
6L HDI

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT

CPU
Penryn SFF ULV DC/SC
Micro-FCBGA956/10W
P4,5

800/1066 MHz FSB

NORTH BRIDGE
Cantiga SFF GS45
PG 6,7,8,9,10,11

DDR2-SODIMM P16
667/800MHZ DDR II

LVDS → LED Panel Connector P17
VGA → CRT Connector P18
TMDS → HDMI Level Shifter P18 → HDMI Connector P18

DMI x 4

SOUTH BRIDGE
ICH9-M SFF
PG 12,13,14,15

SATA0 → 2.5HDD P20
USB → Port 6 → On Board USB0 P20
USB → Port 8 → MINI CARD 1 P21
USB → Port 2 → MINI CARD 2 P21
USB → Port 4 → CCD P17
USB → Port 10 → Bule Tooth P24
USB → Port 0 → USB2 on daughter board P22
USB → Port 1 → USB3 on daughter board P22

PCIE → PCIE1 → MINI CARD 1 Connector P21
PCIE → PCIE4 → MINI CARD 2 Connector P21 → SIM CARD Connector P21
PCIE → PCIE2 → LAN on daughter board P22

IHDA → CODEC + AMP
Realtek
ALC272
P19

MIC/HP/SPDIF → Audio Jacks on daughter board P22
AMP → Speaker → Speaker Connector P19
Digital MIC → LED Panel Connector P17

LPC → EC
ENE KB3926-D2
P23

8x16 → Keyboard Connector P24

SPI → FLASH 2Mbytes P23
PS/2 → TouchPAD Connector P23

CLOCK
CK505 (QFN-64)
P02

FAN & THERMAL
P25

POWER
CPU Core RT8152D P29
VCCP 1.05V RT8209 P27
DDR Power RT8207 P28
SYSTEM 5V/3V RT8206 P26
Charger ISL6251A P30
Discharge P31
1.5V RT9025 P27

NB5

PROJECT : QL1
Quanta Computer Inc.

Size	Document Number	Rev
	Schematic Block Diagram	1A

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02	Front page
03	Clock Generator (SLG8SP513)
04-05	Penryn SFF CULV Processor
06-11	Cantiga North Bridge
12-15	ICH9-M South Bridge
16	DDR2 SO-DIMM
17	LED Panel/CCD
18	CRT / HDMI
19	Azalia ALC272
20	USB/ HDD
21	MINI PCIE(WLAN/WIMAX/3G)
22	LED/B2B conn/ HOLE
23	KB3926/ROM
24	KB/BT/TPD
25	FAN/THERMAL
26	SYSTEM 5V/3V (RT8206)
27	1.05V (RT8209)/1.5V
28	DDR 1.8VSUS(RT8207)
29	VCore(RT8152D)
30	CHARGER (ISL6251A)
31	Discharge/LAN/S5
32	MODIFY LIST

NB5

PROJECT : QL1
Quanta Computer Inc.

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	Front Page	1A

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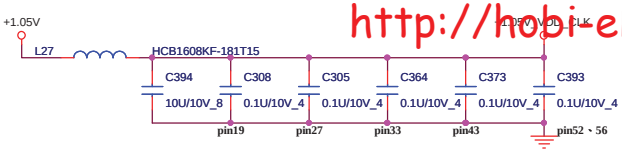
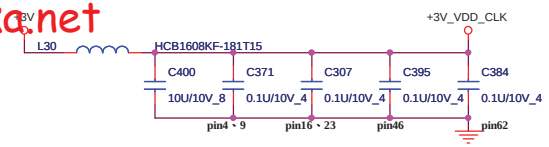
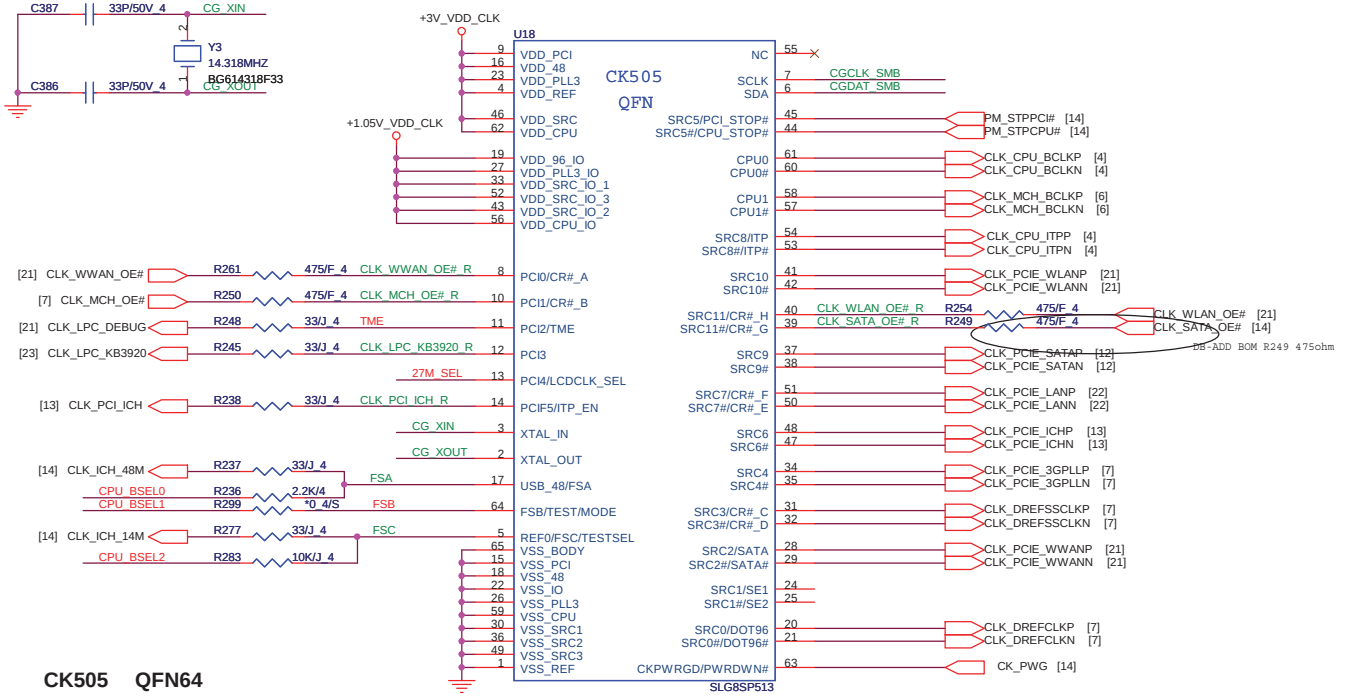
Clock Generator (CLK)



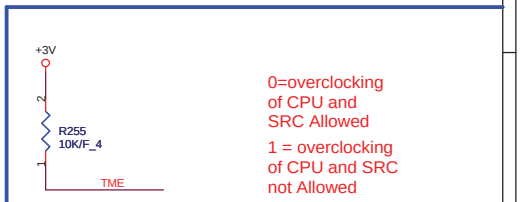


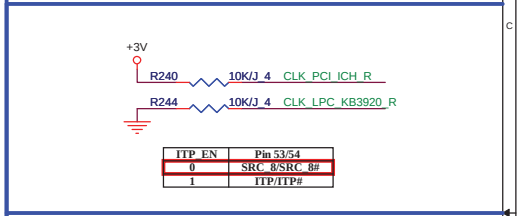


CK505 QFN64

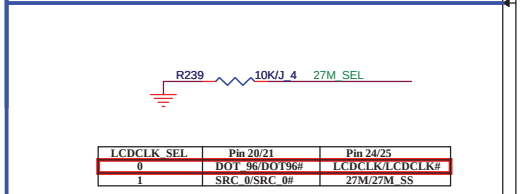
ICS	ICS9LPRS355BKLF	ALPRS355000
Silego	SLG8SP513VTR	AL8SP513000
Realtek	RTM875N-606-VD-GR	AL000875000

Change U18 footprint 8/20





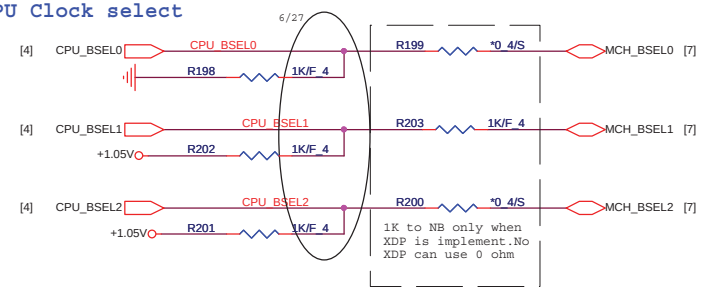
ITP_EN	Pin 53/54
0	SRC_8/SRC_8#
1	ITP/ITP#



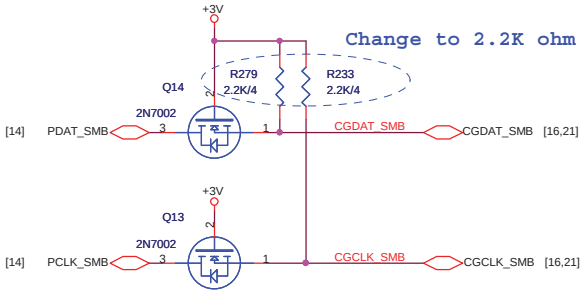
LCDCLK_SEL	Pin 20/21	Pin 24/25
0	DOT_96/DOT96#	LCDCLK/LCDCLK#
1	SRC_0/SRC_0#	27M/27M_SS

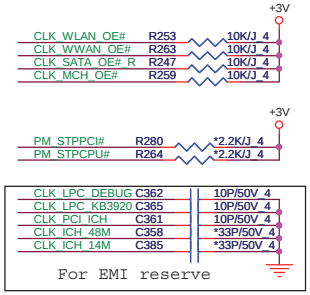
FSC	FSB	FSA	CPU (MHz)	SRC (MHz)	PCI (MHz)	REF (MHz)	DOT96 (MHz)	USB (MHz)
0	0	0	266.6	100.0	33.3	14.318	96.0	48.0
0	0	1	133.3	100.0	33.3	14.318	96.0	48.0
0	1	0	200.0	100.0	33.3	14.318	96.0	48.0
0	1	1	166.6	100.0	33.3	14.318	96.0	48.0
1	0	0	333.3	100.0	33.3	14.318	96.0	48.0
1	0	1	100.0	100.0	33.3	14.318	96.0	48.0
1	1	0	400.0	100.0	33.3	14.318	96.0	48.0
1	1	1	Reserved					

CPU Clock select



Change to 2.2K ohm 8/14





NB5

PROJECT : QL1
Quanta Computer Inc.

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	CLOCK GENERATOR	1A

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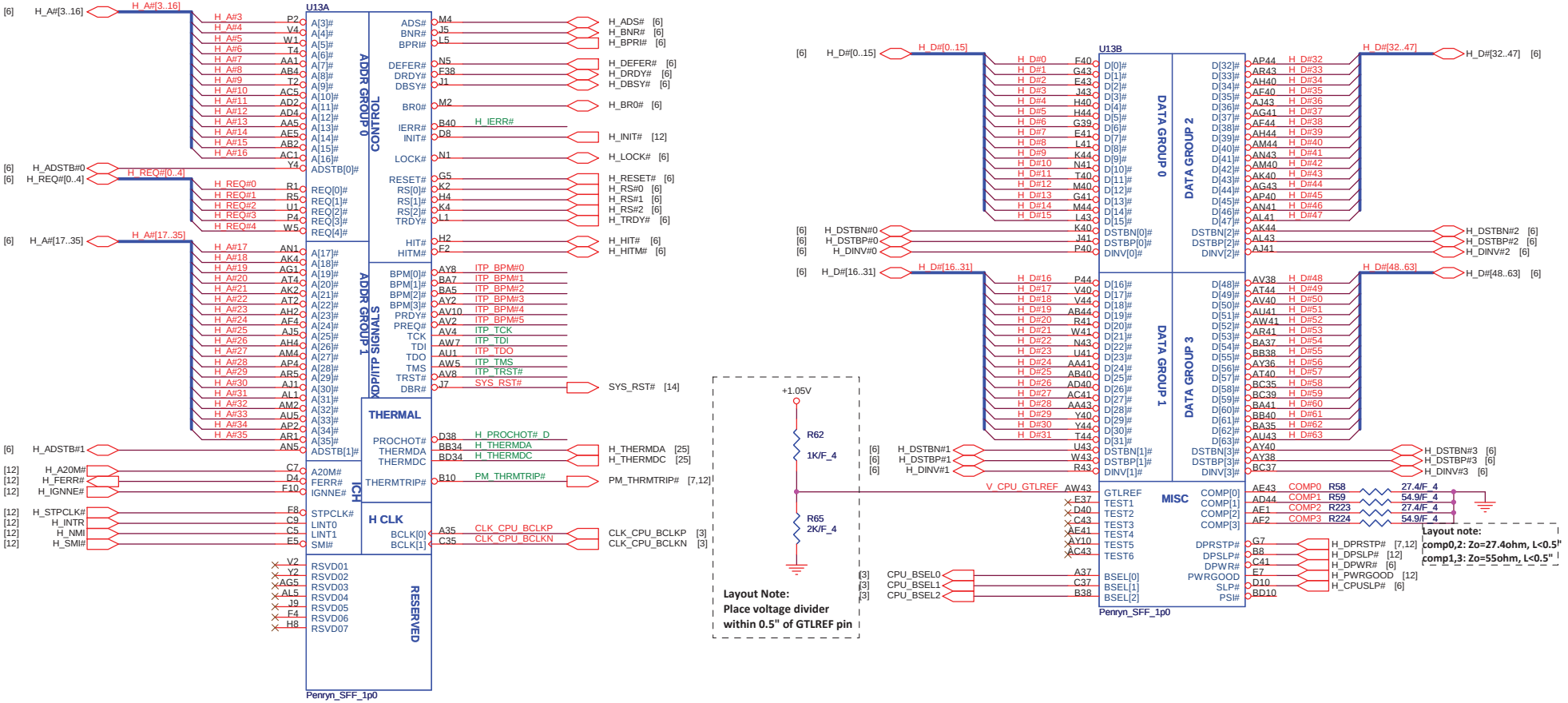
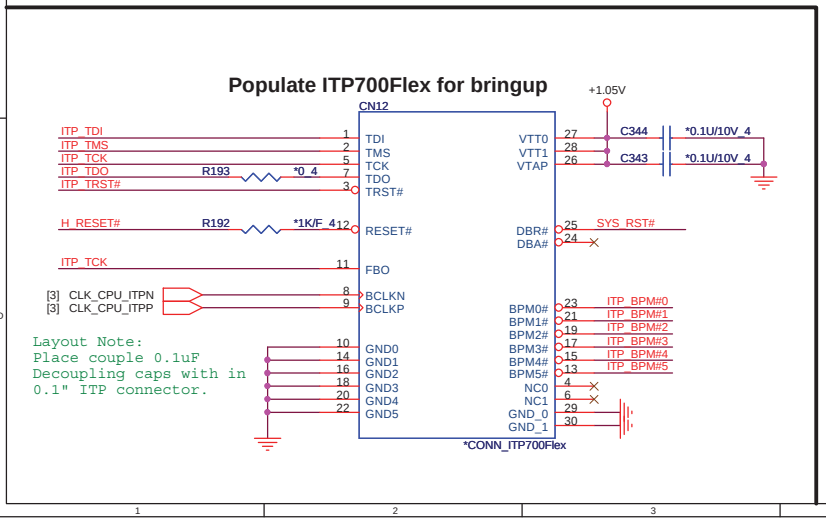
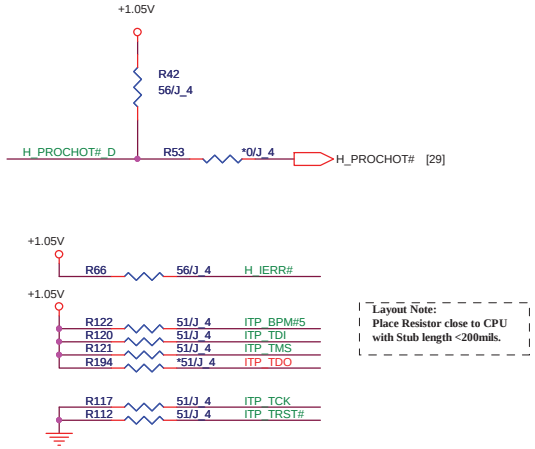
Penryn SFF - Host Bus (CPU)

http://hobi-elektronika.net

04







NB5

PROJECT : QL1
Quanta Computer Inc.

Size	Document Number	Rev
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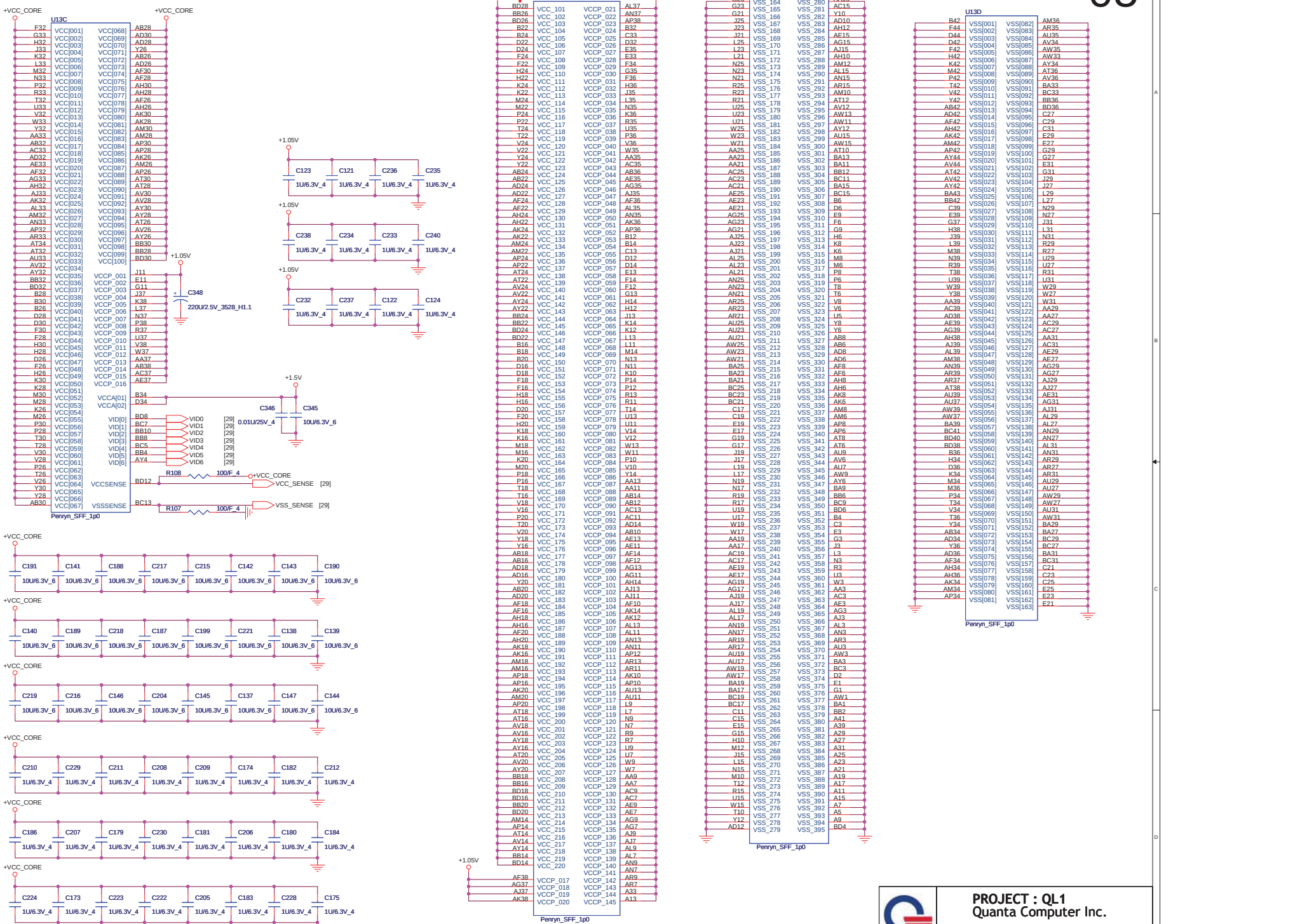
Penryn SFF - Power (CPU)



NB5	PROJECT : QL1 Quanta Computer Inc.
Size	Document Number: Penryn SFF (Power) — Rev 1A
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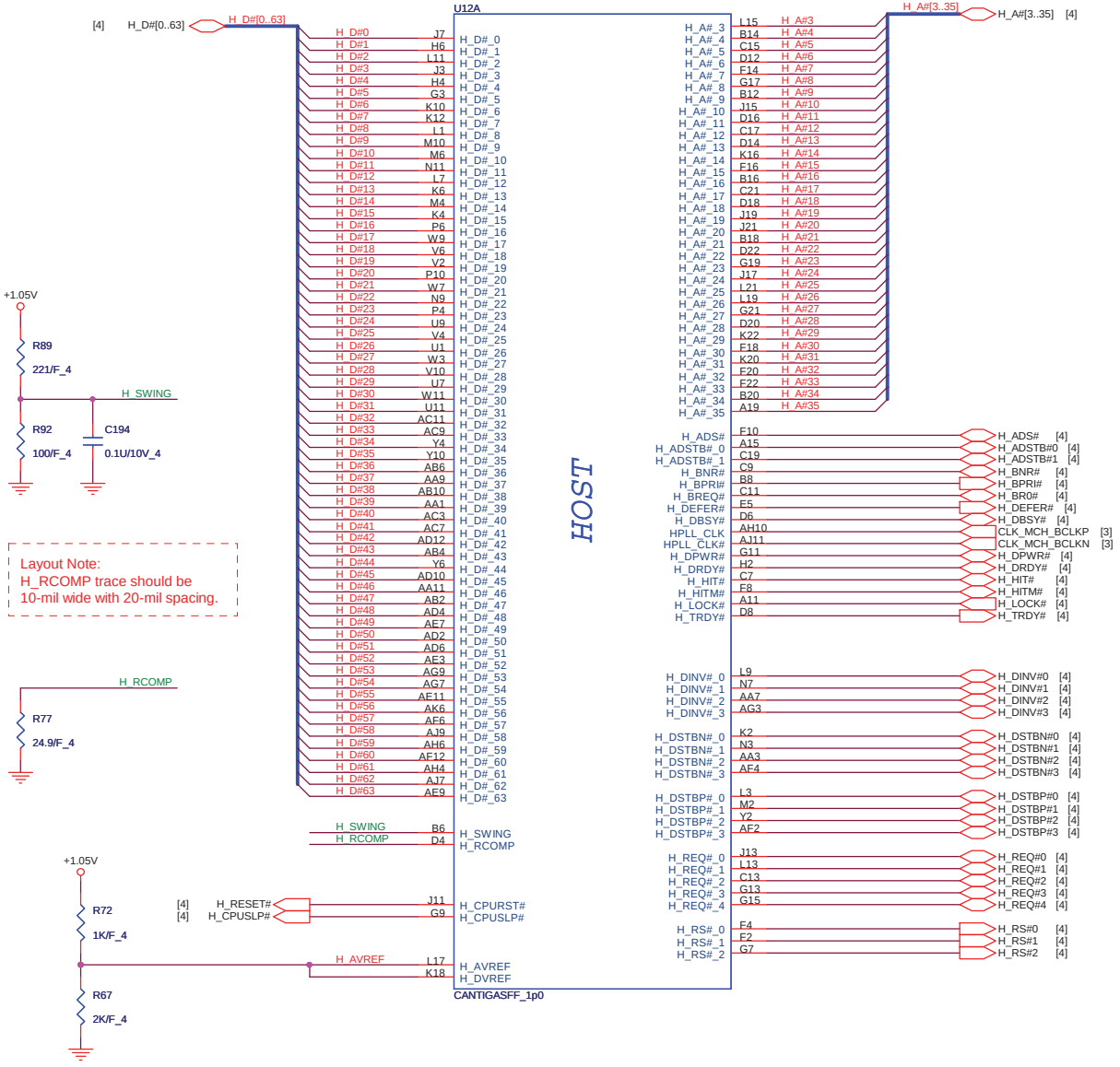

NB5	PROJECT : QL1 Quanta Computer Inc.	
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Cantiga SFF - DMI/VGA (CLG)

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07

Intel GS40/GS45 Strapping Signals and Configuration		
Pin Name	**Strap Description**	**Configuration**
CFG2:0	FSB Frequency	000 = FSB1066 010 = FSB800 011 = FSB667 Other = Reserved
CFG4:3	Reserved	
CFG5	DMI x2 Select	1 = DMI x 4 0 = DMI x2
CFG6	ITPM Host Interface	1 = ITPM disabled 0 = ITPM enabled
CFG7	Intel Management Engine Crypto Strap	1 = Intel Management Engine Crypto TLS cipher suite with confidentiality 0 = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality
CFG8	Reserved	
CFG9	PCIE Graphics Lane	1 = Normal operation : Lane Numbered in Order 0 = Reverse Lanes
CFG10	PCIE Loopback enable	1 = Disabled 0 = Enabled
CFG11	Reserved	
CFG12	ALLZ	1 = Disabled 0 = ALLZ mode enabled
CFG13	XOR	1 = Disabled 0 = XOR mode enabled
CFG14	Reserved	
CFG15	Reserved	
CFG16	FSB Dynamic ODT	1 = Dynamic ODT enabled 0 = Dynamic ODT disabled
CFG17	Reserved	
CFG18	Reserved	
CFG19	DMI Lane Reversal	1 = Reverse Lanes 0 = Normal operation : Lane Numbered in Order
CFG20	Digital DisplayPort (SDVO/DP/iHDMI) Concurrent with PCIE	1 = Digital DisplayPort (SDVO/DP/iHDMI) and PCIE are operating simultaneously via the PEG port 0 = Digital DisplayPort (SDVO/DP/iHDMI) or PCIE are operational
SDVO_CTRLDATA	SDVO Present	1 = SDVO/HDMI/DP interface enabled 0 = No SDVO/HDMI/DP interface disabled
L_DDC_DATA	Local Flat Panel (LFP) Present	1 = LFP Card Present; PCIE disabled 0 = LFP Disable
DDPC_CTRLDATA	Digital Display Present	1 = Digital display (iHDMI/DP) devide present 0 = Digital display (iHDMI/DP) interface absent

- The recommended pull-up resistor value is 4.02 kΩ ±1%
- The recommended pull-down resistor value is 2.21 kΩ ±1%.

U12B

CANTIGASFF_1p0

U12C

CANTIGASFF_1p0

HDMI Port B

Check list note : CL_REF=0.35V

(15mils)

(20mils)

<Checklist ver0.8>
If TSATN# is not used, then it must be terminated with a 56-Ω pull-up resistor to VCCP.

PROJECT : QL1 Quanta Computer Inc.	
NB5	Size: — Document Number: Cantiga SFF (DMI/VGA) — Rev: 1A
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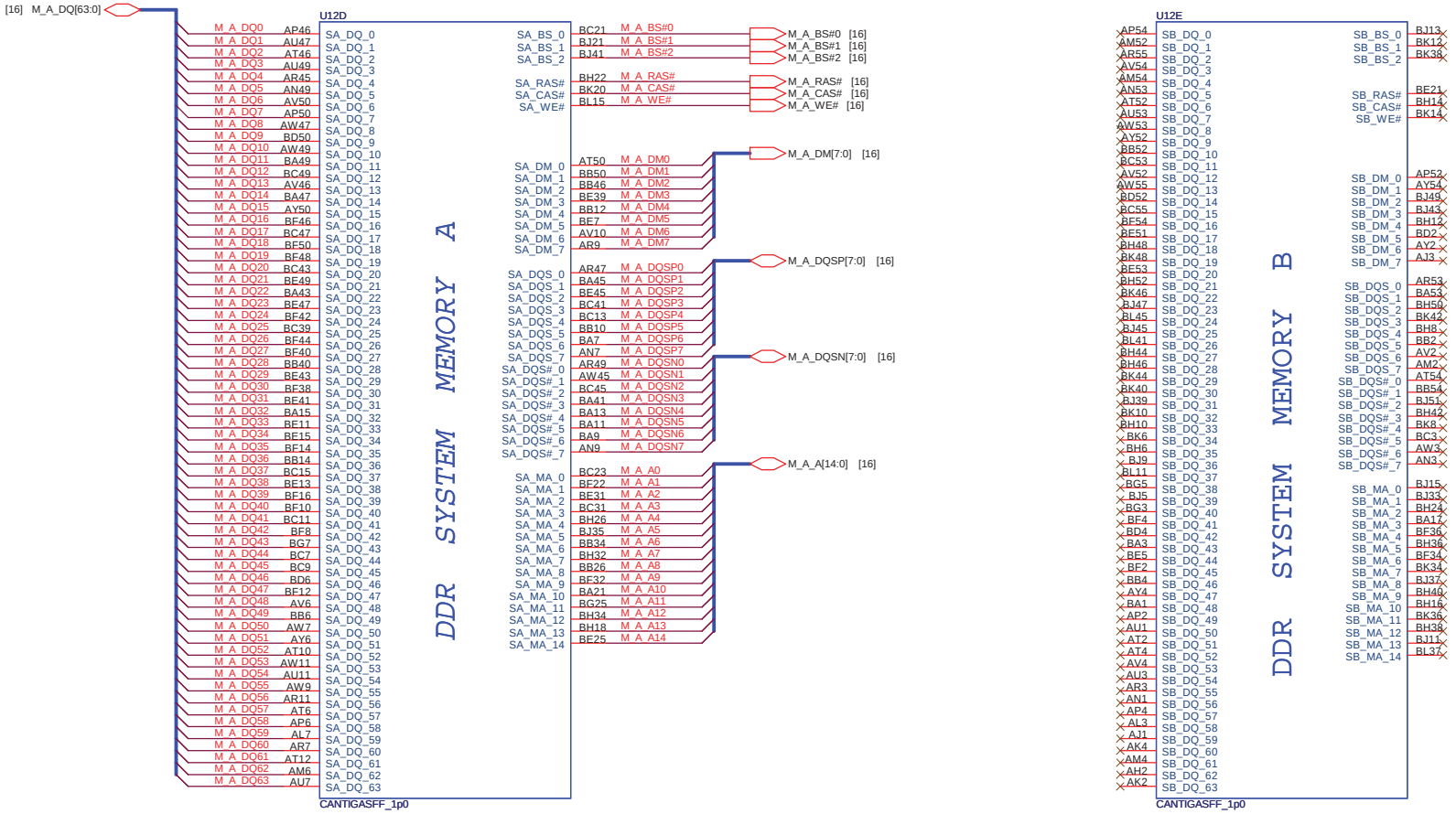

PROJECT :	QL1
	Quanta Computer Inc.
NB5	
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Cantiga SFF - VCC/NCTF (CLG)

Ivcc internal VGA 2.4A
(Shape or 140mils)

DDR2-667 2.6A
DDR2-800 3A
(Shape or 140mils)

UMA 9.6A(GM45)
(Plane or shape)

VCC 2200mA

VCC_SM :3000mA

VCC_AXG 7700mA

U12F

CANTIGASFF_1p0

U12E

CANTIGASFF_1p0

VCC CORE

POWER

VCC NCTF

VCC SM

VCC GFX NCTF

VCC GFX

VCC SM LF

Layout Note:
Inside GMCH cavity.

1. Route VCC_AXG_SENSE and VSS_AXG_SENSE differentially
2. VCC_AXG_SENSE PU to +VGFX_CORE_INT with 10ohm and VSS_AXG_SENSE PD with 10ohm for Intel suggest

PROJECT : QL1 Quanta Computer Inc.		
Size	Document Number Cantiga SFF (VCC/NCTF)	Rev 1A
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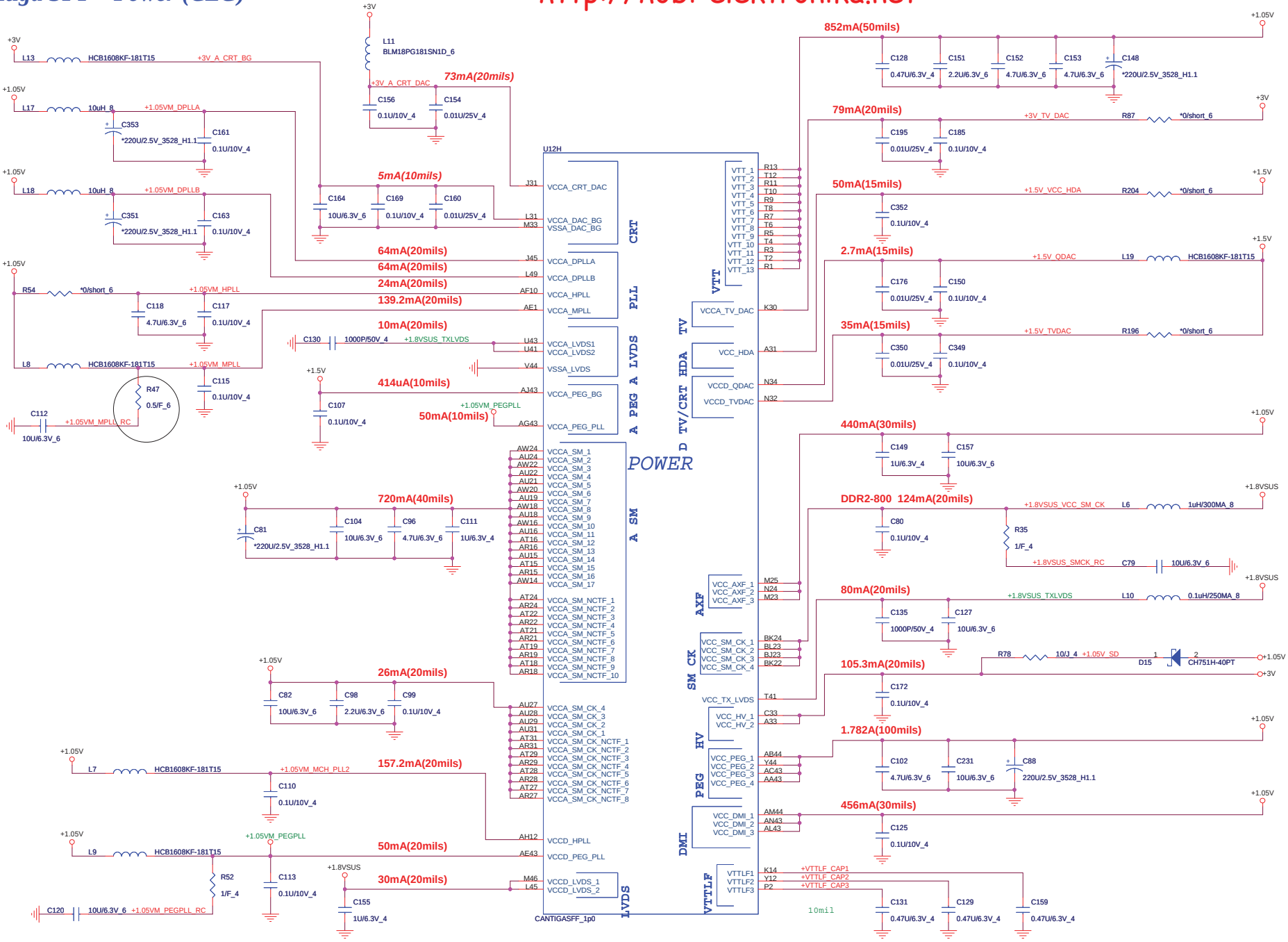
NB5



PROJECT : QL1	Quanta Computer Inc.
NB5	Size: — Document Number: Cantiga SFF (Power) Rev: 1A
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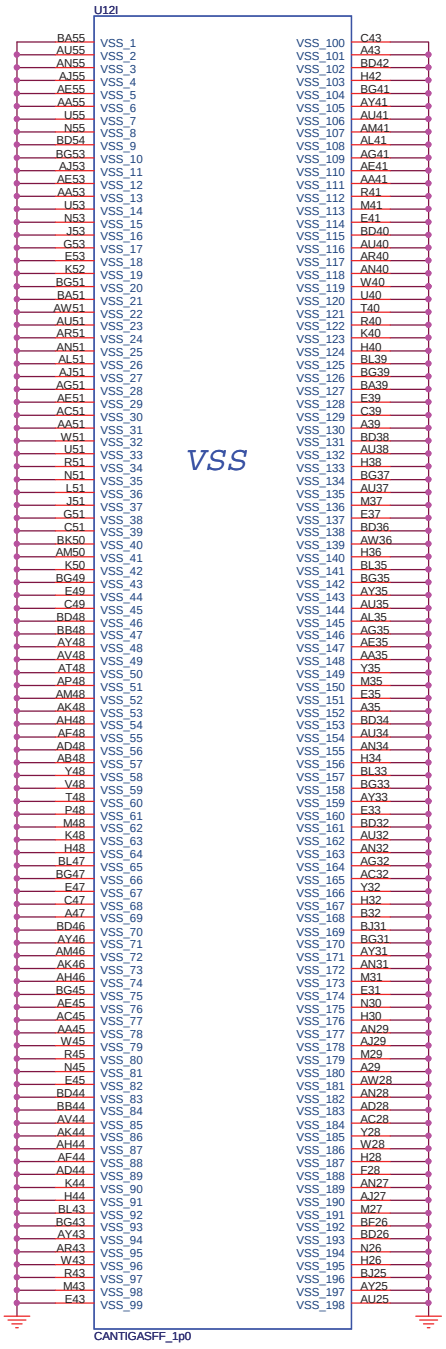

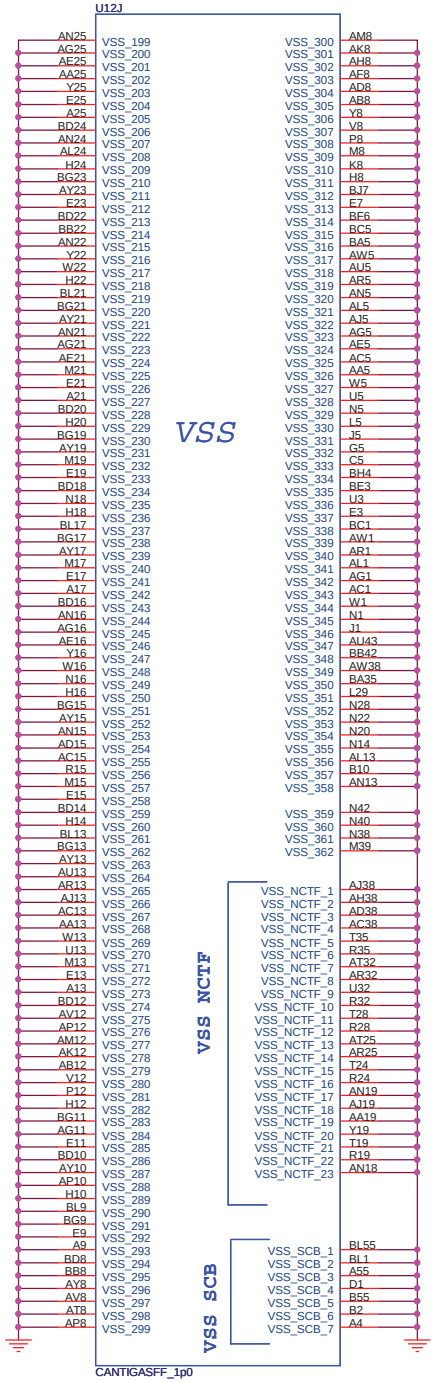

NB5	PROJECT : QL1 Quanta Computer Inc.	
Size	Document Number Cantiga SFF (GND)	Rev 1A
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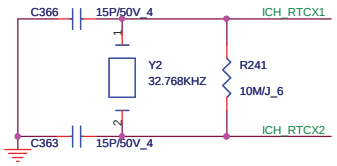
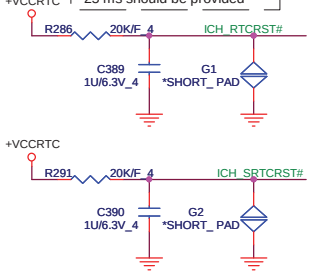
RTC CRYSTAL

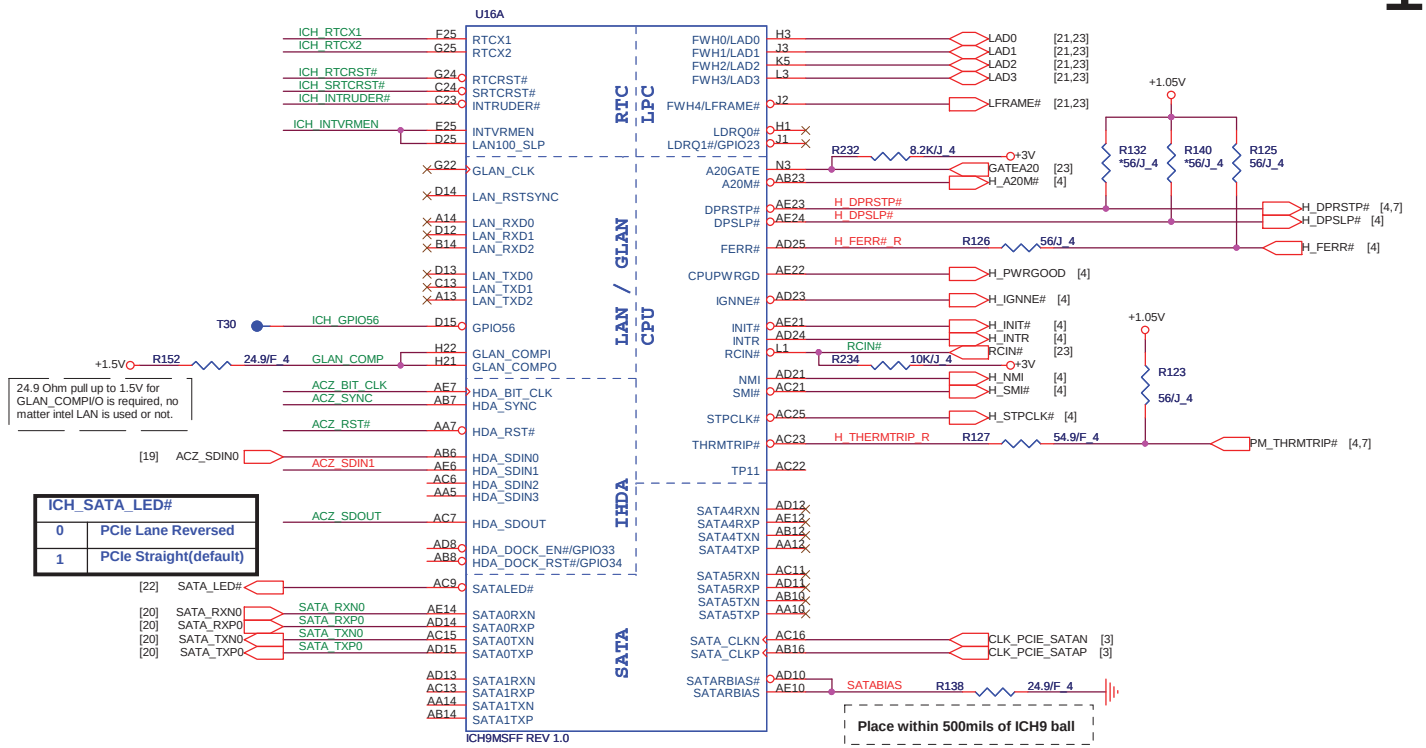


RESET JUMP

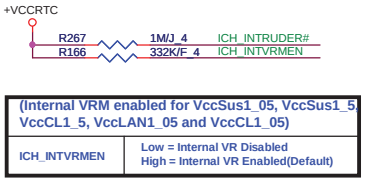
An RC delay circuit with a time delay in the range of 18 ms to 25 ms should be provided



ICH9M SFF (Host/SATA/HDA) (CLG)

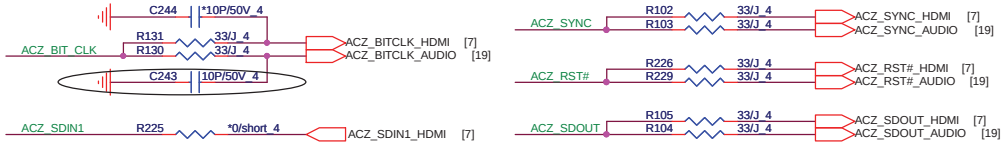


ICH_SATA_LED#	
0	PCIe Lane Reversed
1	PCIe Straight(default)

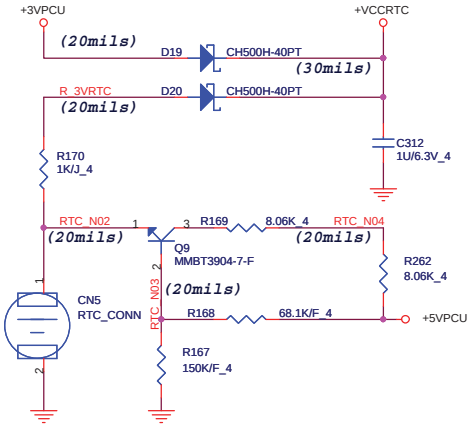


(Internal VRM enabled for VccSus1_05, VccSus1_5, VccCL1_5, VccLAN1_05 and VccCL1_05)	
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)

HD Audio Interface



RTC BATTERY (RTC)



South Bridge Strap Pin (1/3)				
Pin Name	**Strap description**	**Sampled**	**Configuration**	**PU/PD**
HDA_DOCK_EN/ GPIO33	Flash Descriptor Security Override Strap	PWROK	0 = The Flash Descriptor Security will be overridden. 1 = The security measures defined in the Flash Descriptor will be in effect	This strap should only be enabled in manufacturing environments using an external pull-up resistor.
SATALED#	PCI Express Lane Reversal (Lanes 1-4)	PWROK	Internal PU	
	XOR Chain Entrance	PWROK	ICH_TP3 / ACZ_SDOUT / Description 0 / 0 / RSVD 0 / 1 / Enter XOR Chain 1 / 0 / Normal opration(Default) 1 / 1 / Set PCIE port config bit 1	[14] ICH_TP3 — ICH_TP3 — R272 — *1K/J_4
HDA_SDOUT	XOR Chain Entrance /PCI Express* Port Config 1 bit 1(Port 1-4)	PWROK		+3V — R106 — *1K/J_4 — ACZ_SDOUT

NB5

PROJECT : QL1
Quanta Computer Inc.
MV CULV

Size	Document Number	Rev
	ICH9M SFF (Host/SATA/HDA)	1A

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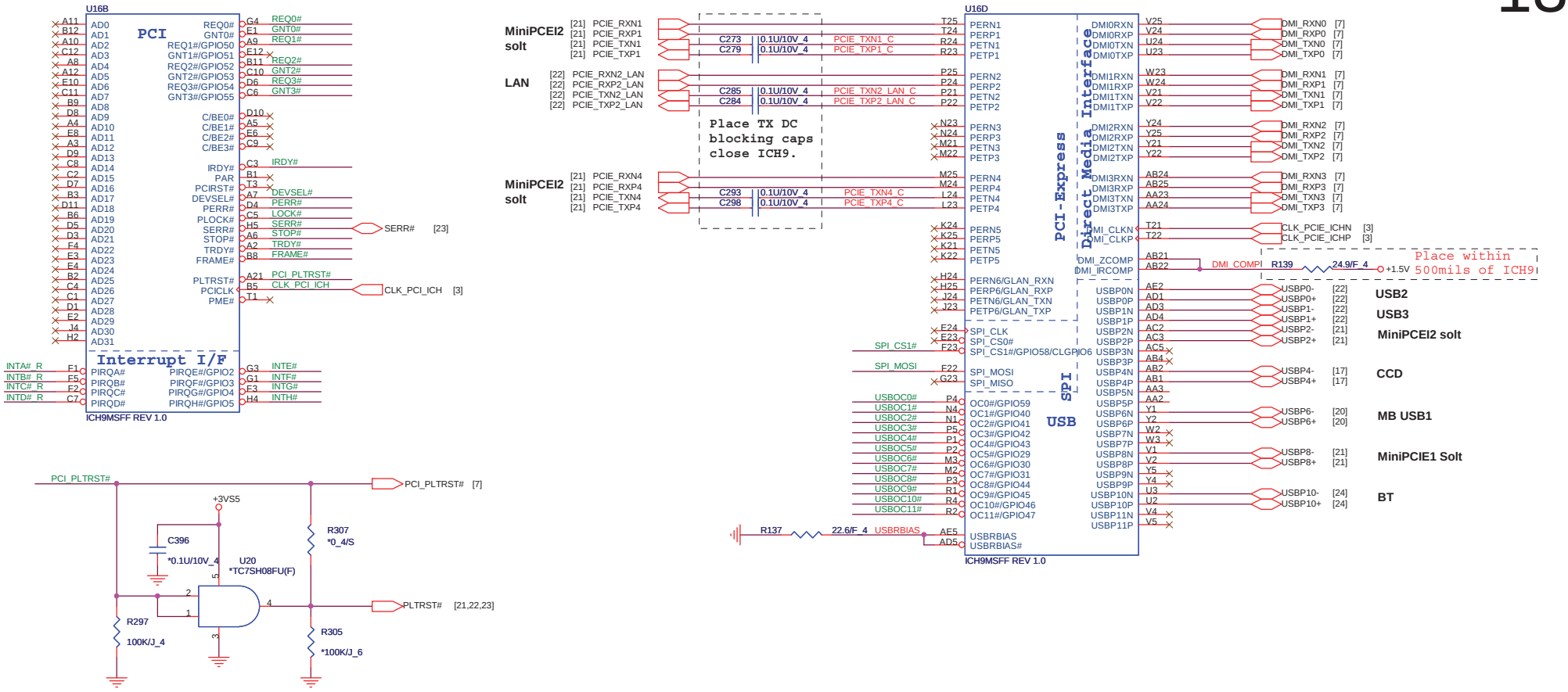
ICH9M SFF - USB/PCIE/DMI (CLG)

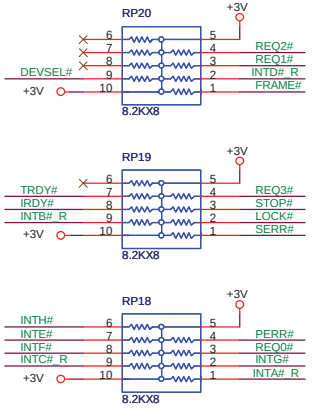


South Bridge Strap Pin (2/3)

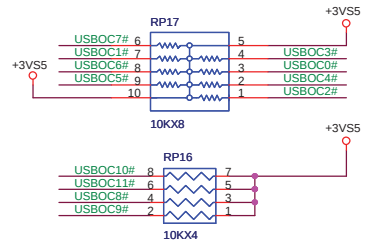
Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0	
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default	GNT2# — T32
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default	GNT3# — T28
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable	SPI_MOSI — T27
GNT0#	Boot BIOS Selection 0	PWROK		GNT0# — T29
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK		SPI_CS1# — T26

PCI_GNT#0	SPI_CS#1	Boot Location
0	1	SPI
1	0	PCI
1	**1**	**LPC(Default)**

PCI PULL-UP



USBOC# PULL-UP



NB5

PROJECT : QL1
Quanta Computer Inc.

Size	Document Number	Rev
	ICH9M SFF (USB/PCIE/DMI)	1A

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ICH9M SFF - PM/GPIO/SMB (CLG)

No Reboot Strap	
SB_BEEP	Low: Default Hi: No reboot

TPM physical presence	
ICH_GPIO57	Low: Default

+3VS5
R273 2.2K/J_4 PCLK_SMB
R274 2.2K/J_4 PDAT_SMB
R269 10K/J_4 ICH_GPIO60
R292 10K/J_4 SMB_CLK_ME
R265 10K/J_4 SMB_DATA_ME
R270 10K/J_4 RI#
R251 10K/J_4 SYS_RST#
R266 10K/J_4 ICH_GPIO11
R289 10K/J_4 PCIE_WAKE#
R258 8.2K/J_4 SWI#
R275 10K/J_4 PM_BATLOW#
R230 10K/J_4 DNBSWON#
R276 10K/J_4 ICH_GPIO12
R163 10K/J_4 ICH_GPIO13
10K/J_4 R268 BT_OFF#

+3V
R231 8.2K/J_4 CLKRUN#
R235 8.2K/J_4 SERIRQ
R207 8.2K/J_4 PM_THRM#
R214 8.2K/J_4 KBSMI#
R206 8.2K/J_4 SC#
R215 8.2K/J_4 ICH_GPIO39
R213 8.2K/J_4 ICH_GPIO48

R210 8.2K/J_4 ICH_GPIO38
R271 10K/J_4 RSMRST#
10K/J_4 R162 ICH_GPIO10
10K/J_4 R165 ICH_GPIO9

U16C

[3] PCLK_SMB — PCLK_SMB C18 SMBCLK
[3] PDAT_SMB — PDAT_SMB C15 SMBDATA
ICH_GPIO60 B21 LINKALERT#/GPIO60/CLGPIO1
SMB_CLK_ME E18 SMLINK0
SMB_DATA_ME A24 SMLINK1
RI# C20 RI#
[4] SYS_RST# — SYS_RST# T5 C25 SUS_STAT#/LPCPD# SYS_RESET#
[7] PM_SYNC# — L2 PMSYNC#/GPIO0
ICH_GPIO11 A23 SMBALERT#/GPIO11
[3] PM_STPPCI# — PM_STPPCI# B15 STP_PCI#/GPIO15
[3] PM_STPCPU# — PM_STPCPU# A20 STP_CPU#/GPIO25
[23] CLKRUN# — CLKRUN# M5 CLKRUN#/GPIO32
[21,22] PCIE_WAKE# — PCIE_WAKE# C21 WAKE#
[23] SERIRQ — SERIRQ L4 SERIRQ
[25] PM_THRM# — AD20 THRM#
VR_PWRGO_CLKEN B24 VRMPWRGD
A19 TP12

SMB
SATA GPIO
Clocks
SYS GPIO
Power MGT
GPIO
Controller Link
MISC

SATA0GP/GPIO21 AE19 BOARD_ID1
SATA1GP/GPIO19 AA18 BOARD_ID0
SATA4GP/GPIO36 AE20 BOARD_ID3
SATA5GP/GPIO37 AA20 BOARD_ID4
CLK14 K1 CLK_ICH_14M — CLK_ICH_14M [3]
CLK48 AB5 CLK_ICH_48M — CLK_ICH_48M [3]
SUSCLK R3 ICH_SUSCLK — T40
SLP_S3# D18 — SUSB# [23]
SLP_S4# B20 — SUSC# [23]
SLP_S5# D16
S4_STATE#/GPIO26 E14
PWROK D23 ICH_PWRGD
DPRSLPVR/GPIO16 M1 DPRSLPVR — DPRSLPVR [7,29]
BATLOW# C16 PM_BATLOW# — PM_BATLOW# [23]
PWRBTN# U4 — DNBSWON# [23]
LAN_RST# D22 PM_LAN_ENABLE_R
RSMRST# D19 — RSMRST# [23]
CK_PWRGD U1 CK_PWG — CK_PWG [3]
CLPWROK T4 ECPWROK
SLP_M# B23

[23] KBSMI# — KBSMI# AE16 GPIO1
[23] SCI# — SCI# AE18 GPIO6
[23] SWI# — AD18 GPIO7
ICH_GPIO12 B25 GPIO8
ICH_GPIO13 C14 GPIO12
BOARD_ID5 D20 GPIO13
[21] WWAN_OFF# — AE17 GPIO17
[17] LCD_BK — K3 GPIO18
BOARD_ID2 AC8 GPIO20
AC19 SCLOCK/GPIO22
[21] RF_EN — D17 GPIO27
[3] CLK_SATA_OE# — CLK_SATA_OE# E20 GPIO28
ICH_GPIO38 M4 SATACLKREQ#/GPIO35
ICH_GPIO39 AB18 SLOAD/GPIO38
ICH_GPIO48 AC18 SDATAOUT0/GPIO39
AB19 SDATAOUT1/GPIO48
AC20 GPIO49
ICH_GPIO57 A16 GPIO57/CLGPIO5

CL_CLK0 C22 — CL_CLK0 [7]
CL_CLK1 A18
CL_DATA0 E22 — CL_DATA0 [7]
CL_DATA1 B18
CL_VREF0 F21 CL_VREF0_SB
CL_VREF1 A17 CL_VREF1_SB
CL_RST0# C17 — ICH_CL_RST0# [7]
CL_RST1# B17
MEM_LED/GPIO24 A22 BT_OFF# — BT_OFF# [24]
GPIO10/SUS_PWR_ACK E16 ICH_GPIO10
GPIO14/AC_PRESENT A15 ICH_GPIO14 — T41
WOL_EN/GPIO9 D21 ICH_GPIO9

[19] SB_BEEP — SB_BEEP K4 SPKR
[7] MCH_ICH_SYNC# — MCH_ICH_SYNC# AB20 MCH_SYNC#
[12] ICH_TP3 — C19 TP3
AB17 TP8
AC17 TP9
AD17 TP10

ICH9MSFF REV 1.0

+3V
R300 1K/F_4
VR_PWRGO_CLKEN
Q15 BS870-7-F
[29] VR_PWRGD_CK410# — 2
R288 100K/F_4

+3V
R161 *1K/F_4 SB_BEEP

+3V
R290 100K/J_4 ICH_GPIO57

+3V
R284 *3.24K/F_6
CL_VREF1_SB
C375 *0.47U/6.3V_4
R278 *453/F_4

+3V
R294 3.24K/F_6
CL_VREF0_SB
C388 0.1U/10V_4
R293 453/F_4

+3V
R216 *10K/J_4 — BOARD_ID0 — R217 10K/J_4
R208 *10K/J_4 — BOARD_ID1 — R209 10K/J_4
R113 *10K/J_4 — BOARD_ID2 — R114 10K/J_4
R129 *10K/J_4 — BOARD_ID3 — R124 10K/J_4
R147 *10K/J_4 — BOARD_ID4 — R148 10K/J_4
R212 *10K/J_4 — BOARD_ID5 — R211 10K/J_4

BOARD ID	ID5	ID4	ID3	ID2	ID1	ID0	NOTE
GS40	0	0	0	0	0	0	
GS45	0	0	0	0	0	1	

+3VSUS
C401 *0.1U/10V_4
[7,29] DELAY_VR_PWRGOOD — DELAY_VR_PWRGOOD
[7,23,25] ECPWROK
U21 *TC7SH08FU(F)
ICH_PWRGD
R304 10K/J_4
R306 *0_4/S

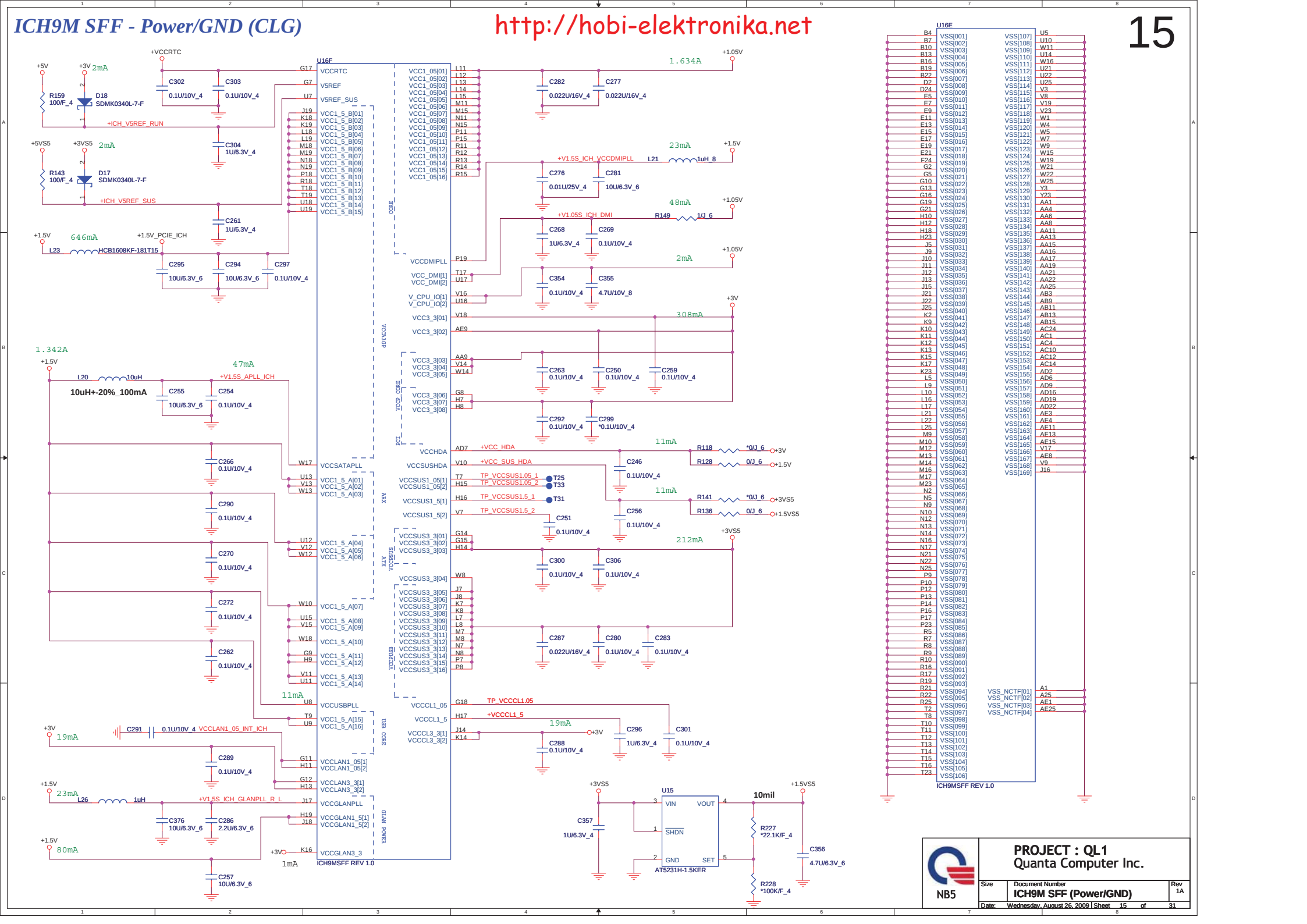
NB5

PROJECT : QL1
Quanta Computer Inc.
MV CULV

Size	Document Number	Rev
	ICH9M SFF (PM/GPIO/SMB)	1A

Date: Wednesday, August 26, 2009 | Sheet 14 of 31

ICH9M SFF - Power/GND (CLG)



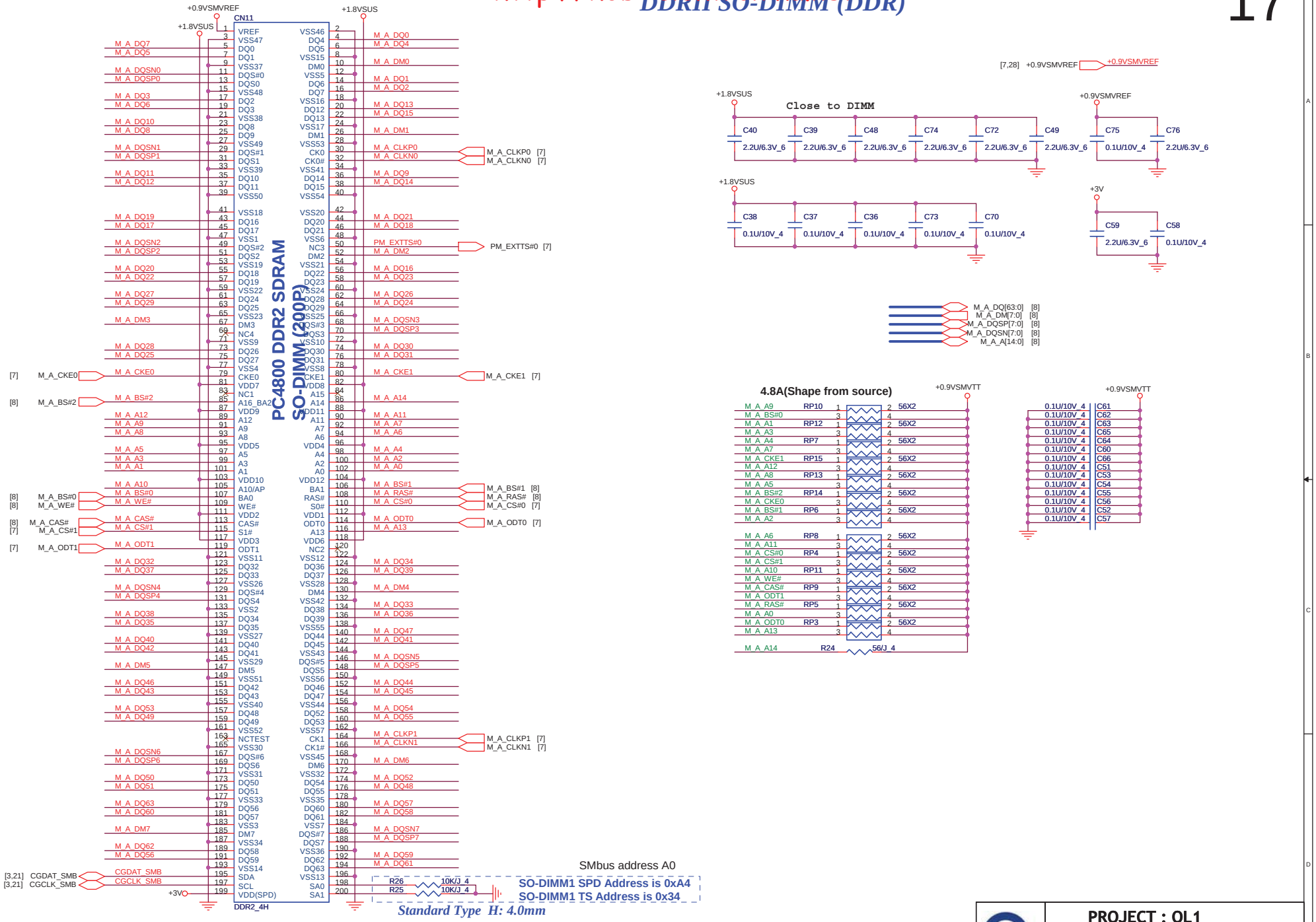
NB5

PROJECT : QL1
Quanta Computer Inc.

Size	Document Number	Rev
	ICH9M SFF (Power/GND)	1A

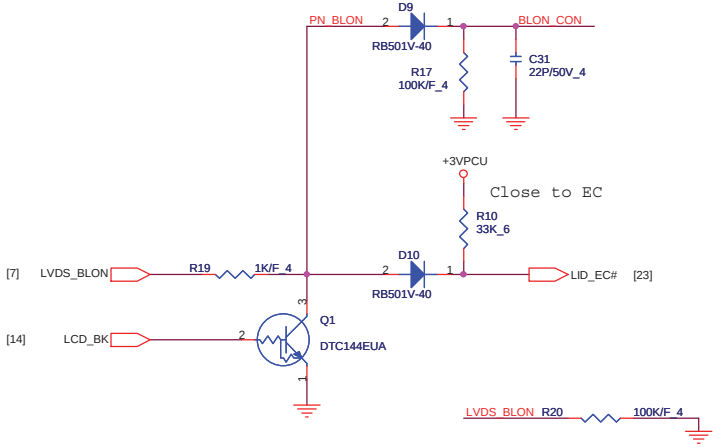
Date: Wednesday, August 26, 2009 | Sheet 15 of 31

DDRII SO-DIMM (DDR)

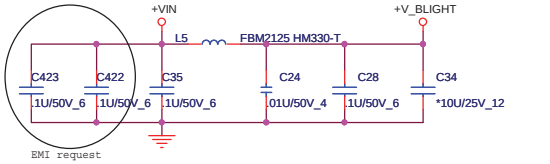


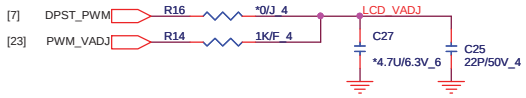
NB5	PROJECT : QL1 Quanta Computer Inc.	
	Size: — Document Number: DDRII SO-DIMM #1	Rev: 1A
	Date: Wednesday, August 26, 2009 Sheet 16 of 31	

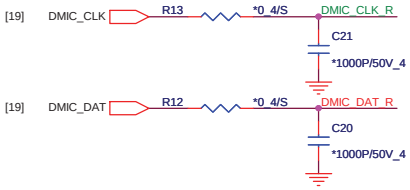
Backlight Control(LDS)

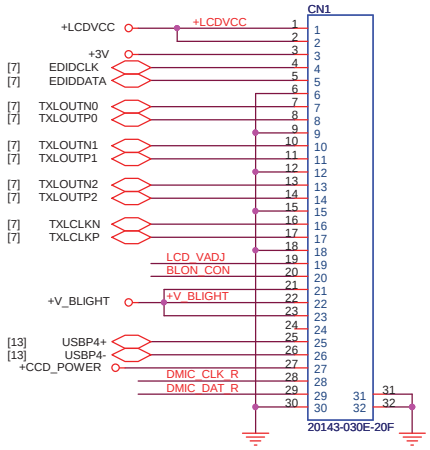


LED Panel(LDS)

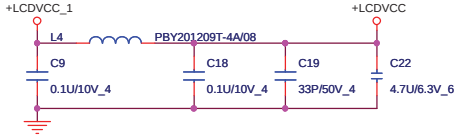


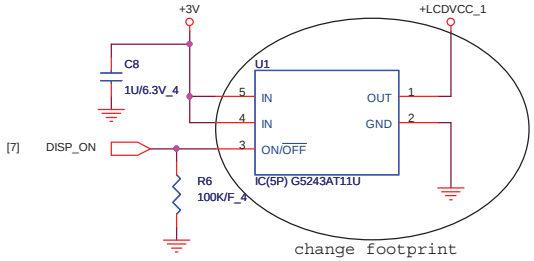




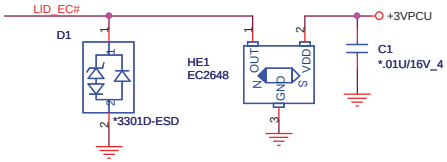


LED Panel POWER SWITCH(LDS)

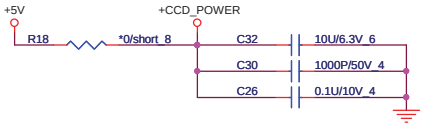




Lid SWITCH(LDS)



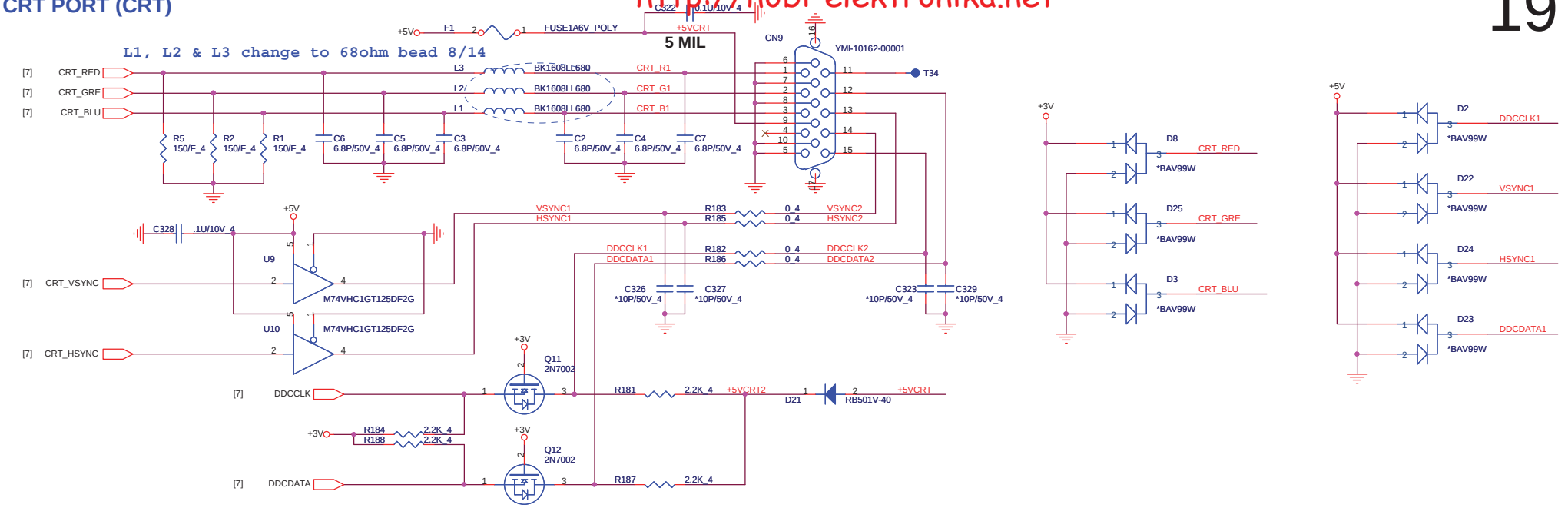
Camera(CCD)



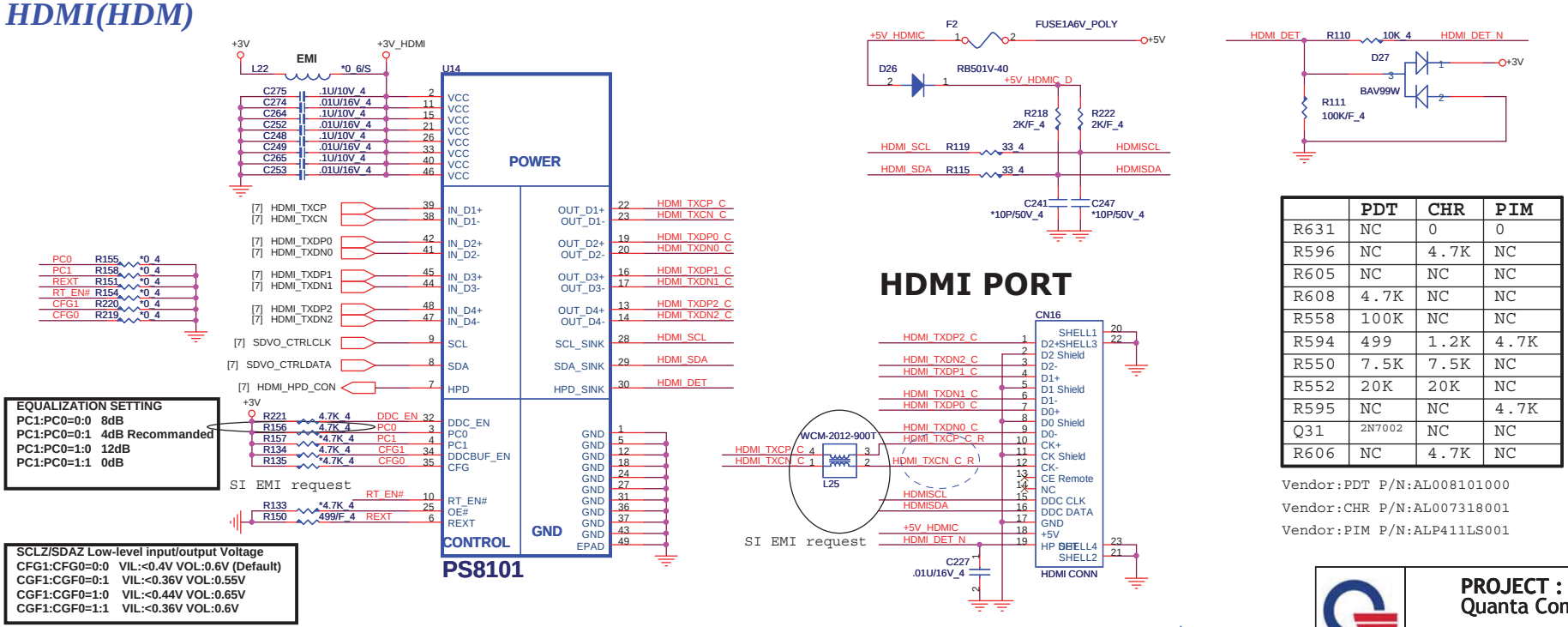
NB5	PROJECT : QL1 Quanta Computer Inc.	
Size	Document Number LED Panel/CCD/HDMI	Rev 1A
Date: Wednesday, August 26, 2009	Sheet 17 of 31	

CRT PORT (CRT)

L1, L2 & L3 change to 68ohm bead 8/14



HDMI(HDM)



HDMI PORT

Change to HDMI_TXCN_C_R & HDMI_TXCP_C_R 8/14

	PDT	CHR	PIM
R631	NC	0	0
R596	NC	4.7K	NC
R605	NC	NC	NC
R608	4.7K	NC	NC
R558	100K	NC	NC
R594	499	1.2K	4.7K
R550	7.5K	7.5K	NC
R552	20K	20K	NC
R595	NC	NC	4.7K
Q31	2N7002	NC	NC
R606	NC	4.7K	NC

Vendor:PDT P/N:AL008101000
Vendor:CHR P/N:AL007318001
Vendor:PIM P/N:ALP411LS001

NB5

PROJECT : QL1
Quanta Computer Inc.

Size	Document Number	Rev
	CRT	1A

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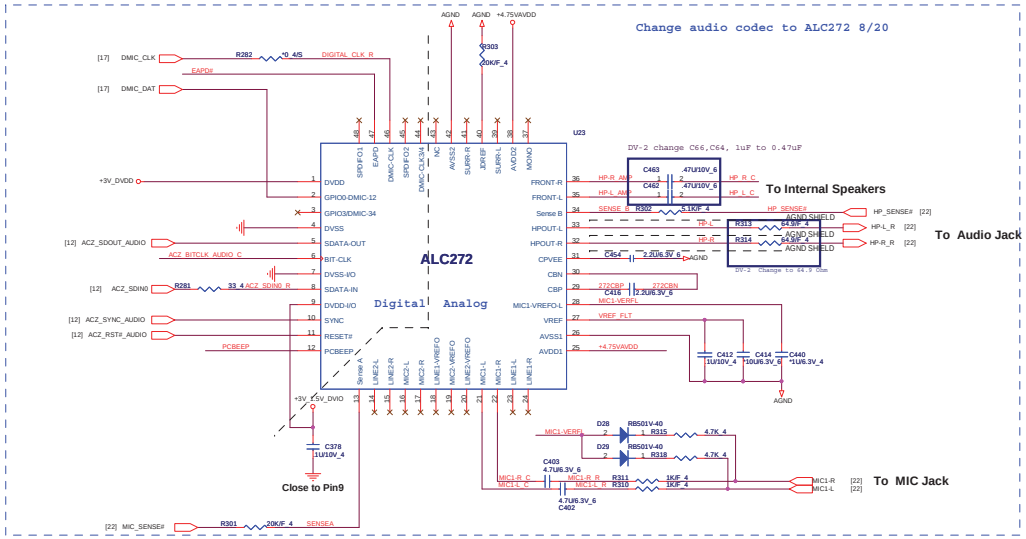
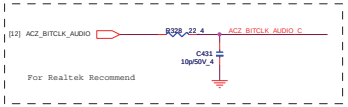
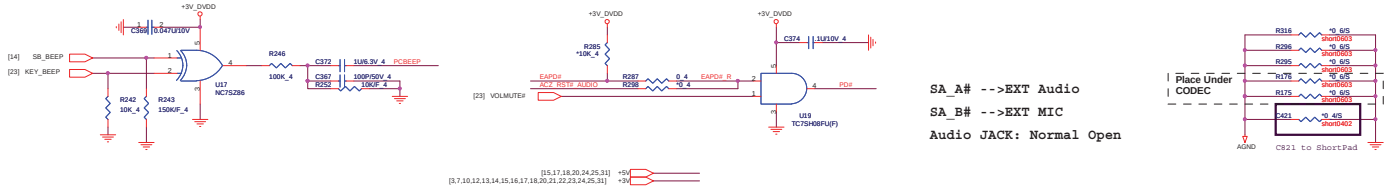
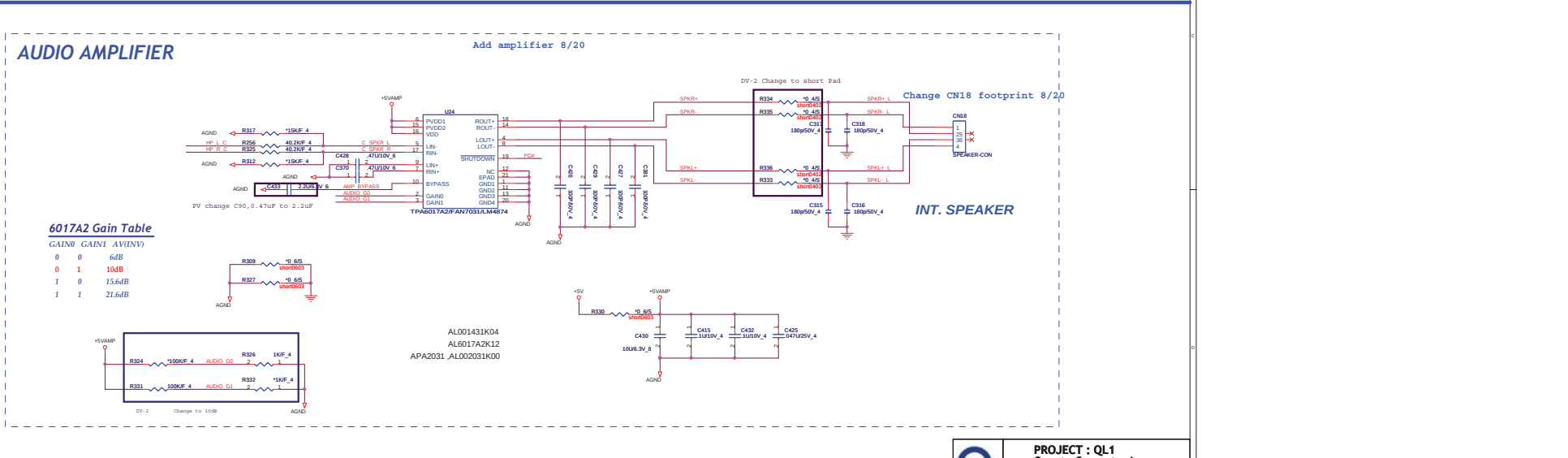


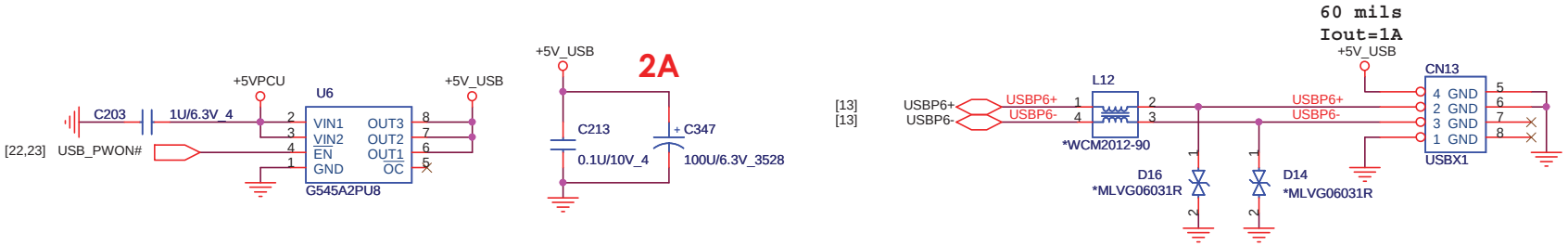


PORT	PLACE TO
MONO_OUT	X
PORT A	AUDIO OUT
PORT B	MIC
PORT C	X
PORT D	Internal Speckers
PORT E	X
PORT F	X
DM	Internal DIGITAL MIC

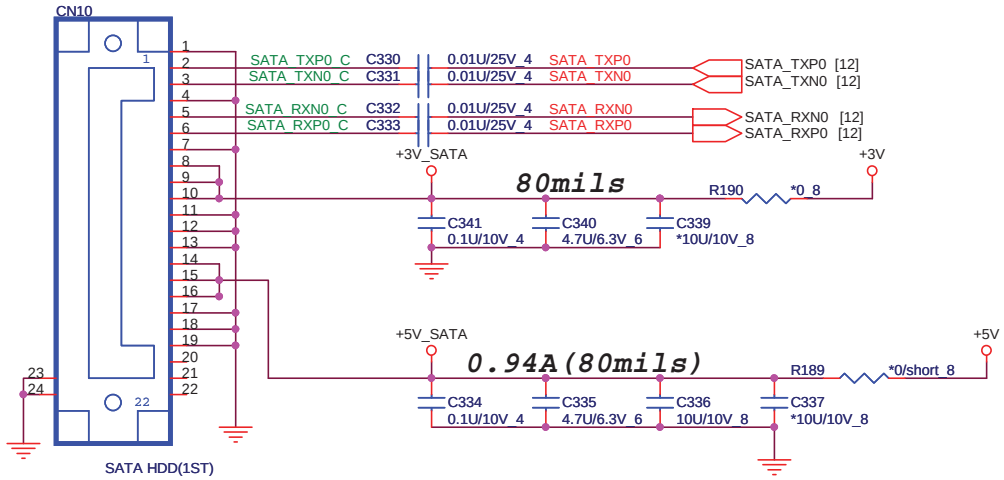




PROJECT : QL1	
Quanta Computer Inc.	
NB5	Size: Document Number: Azalia ALC272/BT CONN Rev: 1A
Date: Wednesday, August 26, 2009	Sheet 19 of 31

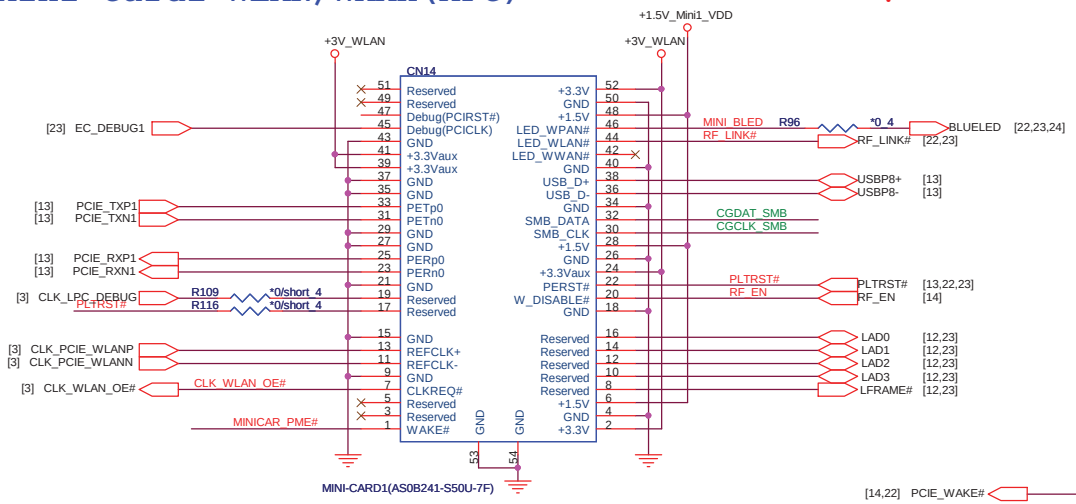


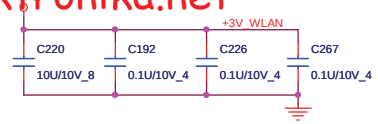
2.5" SATA HDD(HDD)

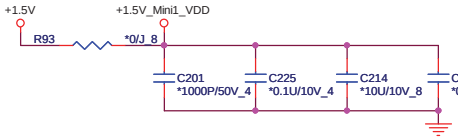


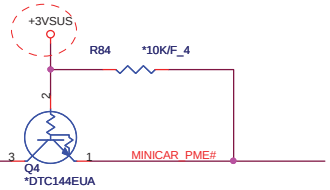
NB5	PROJECT : QL1 Quanta Computer Inc.	
Size	Document Number USB, HDD	Rev 1A
Date: Wednesday, August 26, 2009	Sheet 20 of 31	

Mini Card1-WLAN/WMAX(MPC)

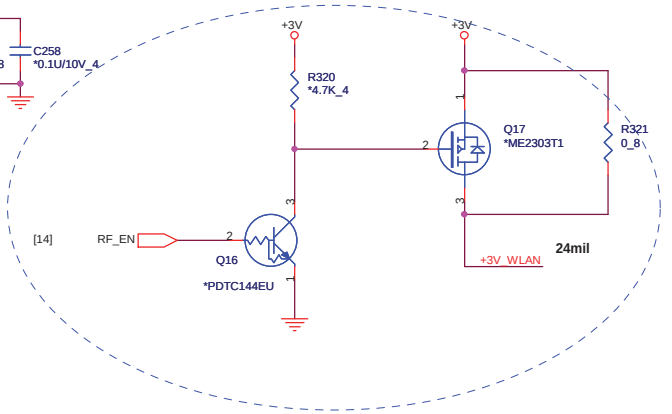






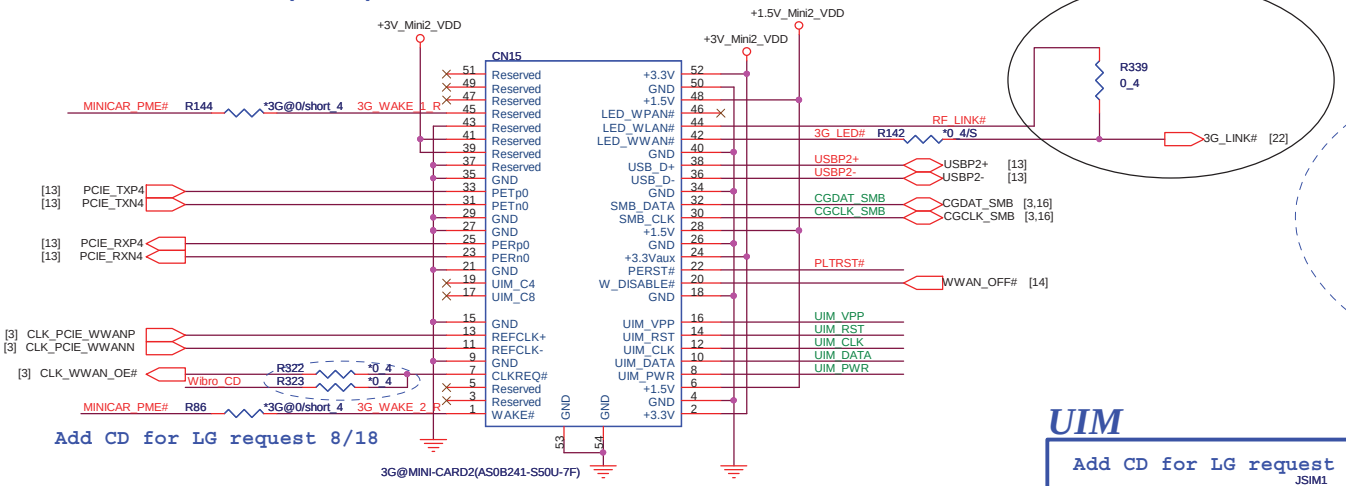


Add power switch circuit 8/12



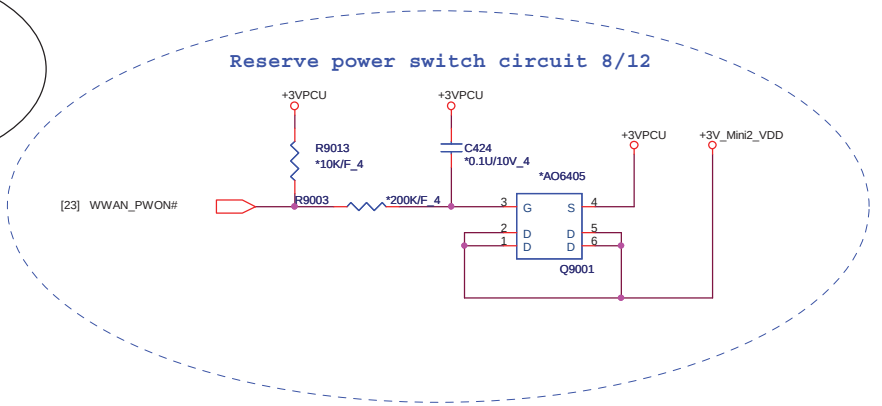
Mini Card2-3G(MNC)

Swap CN14 & CN15 footprint 8/18

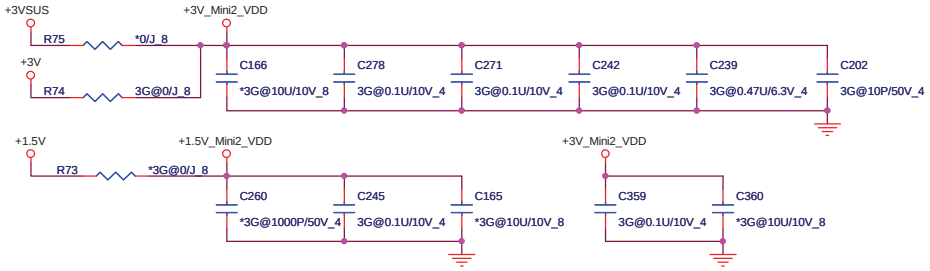


Add CD for LG request 8/18

Reserve power switch circuit 8/12

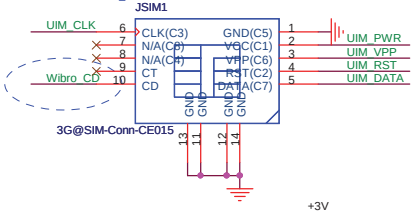


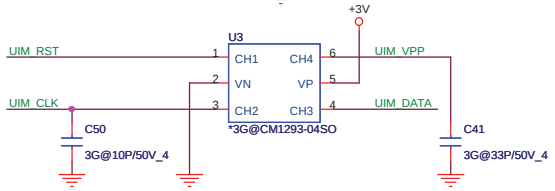
Change CN15 footprint 8/20

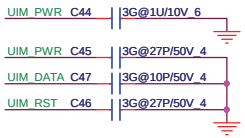


UIM

Add CD for LG request 8/18





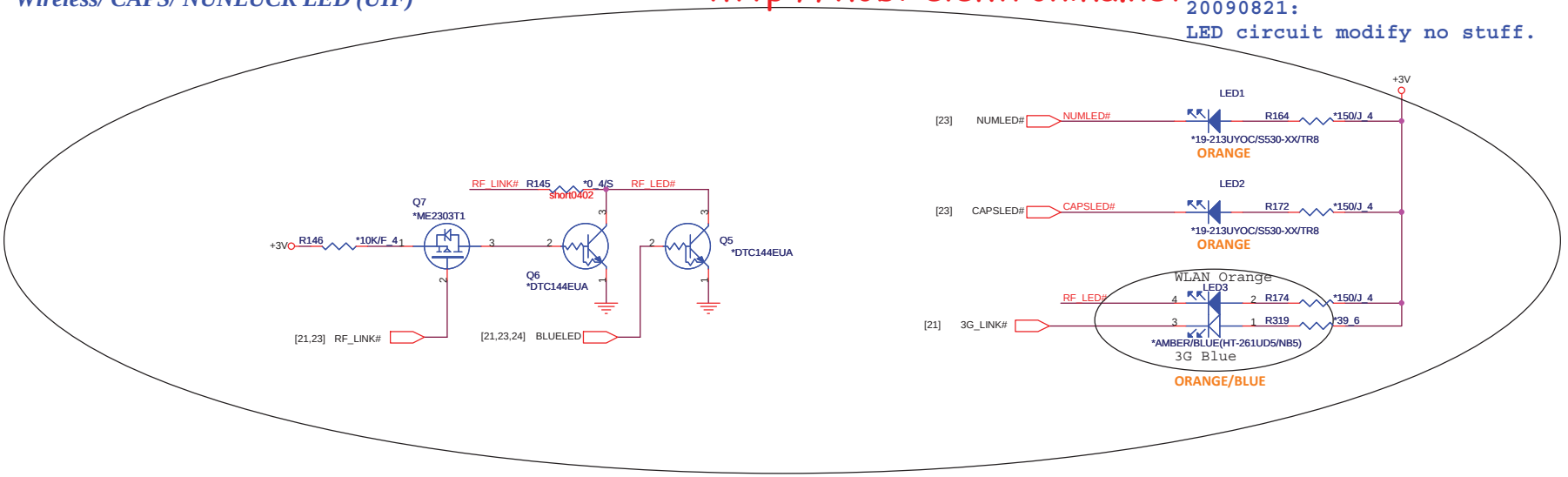


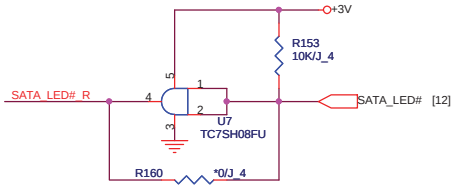
NB5

PROJECT : QL1
Quanta Computer Inc.

Size	Document Number	Rev
	MINI PCIE (WLAN/WMAX/3G)	1A
Date: Wednesday, August 26, 2009	Sheet 21 of 31	

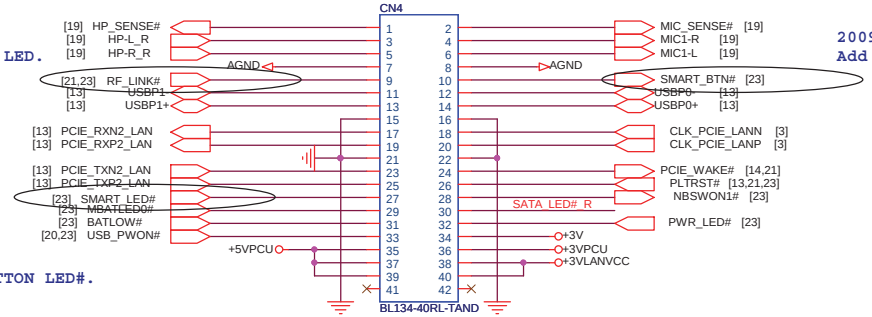
20090821:
LED circuit modify no stuff.





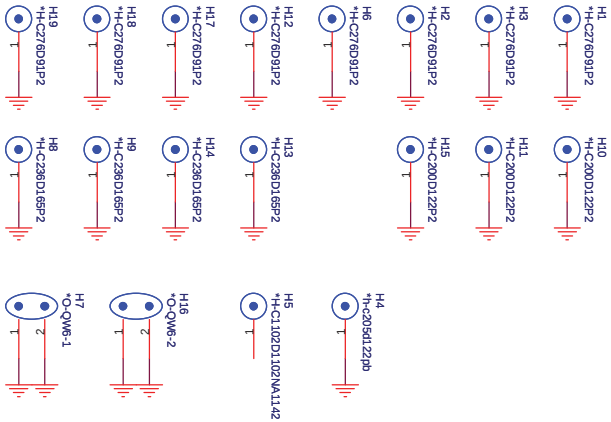
20090824:
Add RF Link# LED.

20090826:
Add SMART BUTTON LED#.

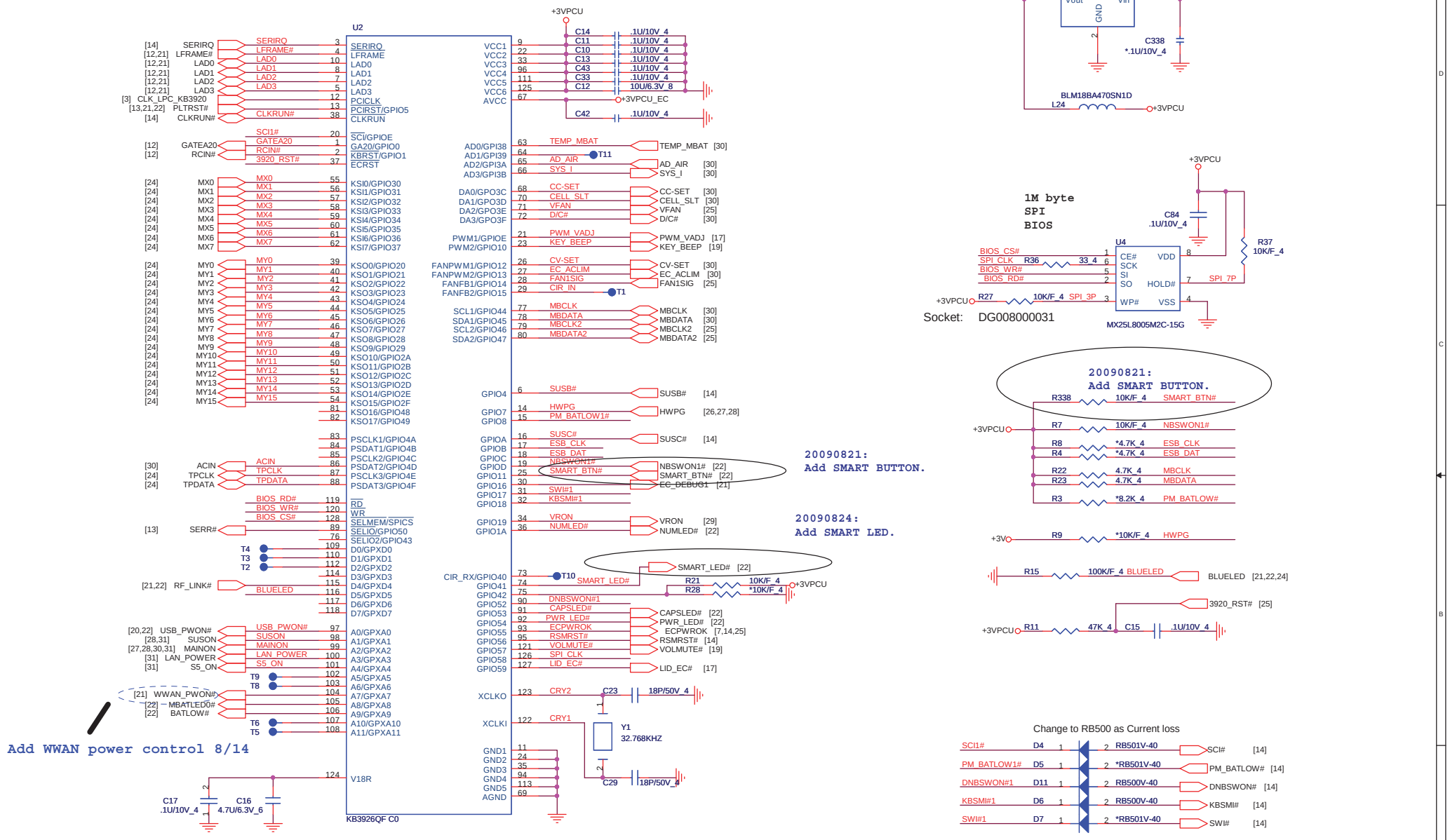


20090821:
Add SMART BUTTON.

HOLE



NB5	PROJECT : QL1 Quanta Computer Inc.	
	Size: — Document Number: LED/ B2B conn/ HOLE	Rev: 1A
	Date: Wednesday, August 26, 2009 | Sheet 22 of 31	



20090821:
Add SMART BUTTON.

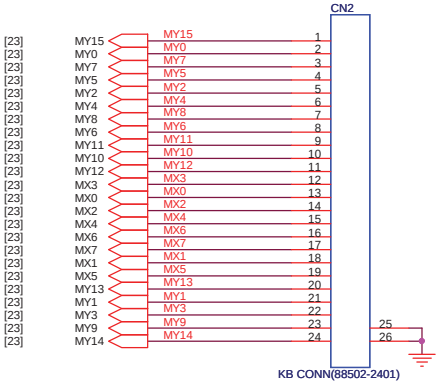
20090824:
Add SMART LED.

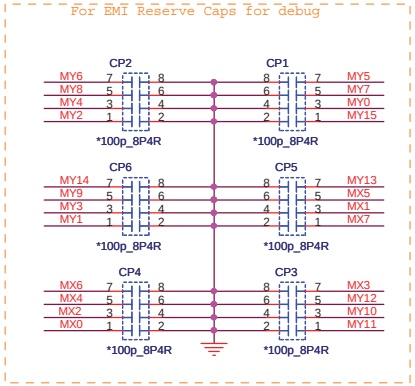
Add WWAN power control 8/14

Change to RB500 as Current loss

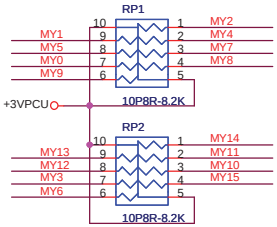
NB5	PROJECT : QL1 Quanta Computer Inc.	
	Size: — Document Number: KB3926/ROM	Rev: 1A
	Date: Wednesday, August 26, 2009	Sheet 23 of 31

Keyboard(KBC)

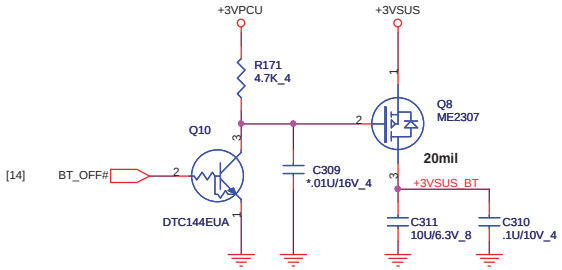


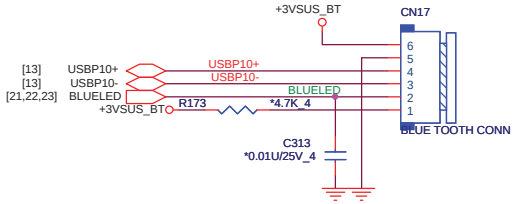


KEYBOARD PULL-UP



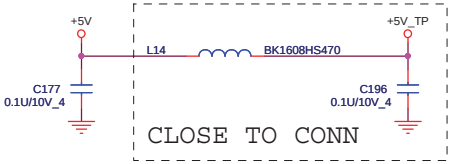
BlueTooth(BTM)

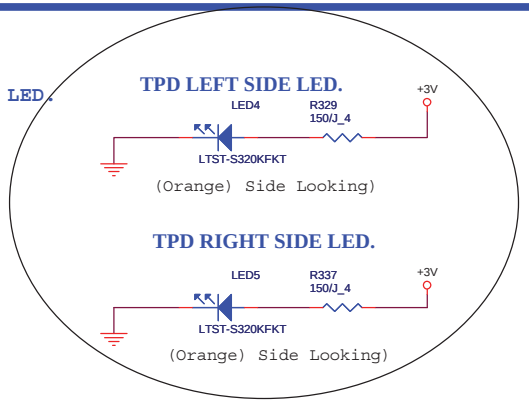


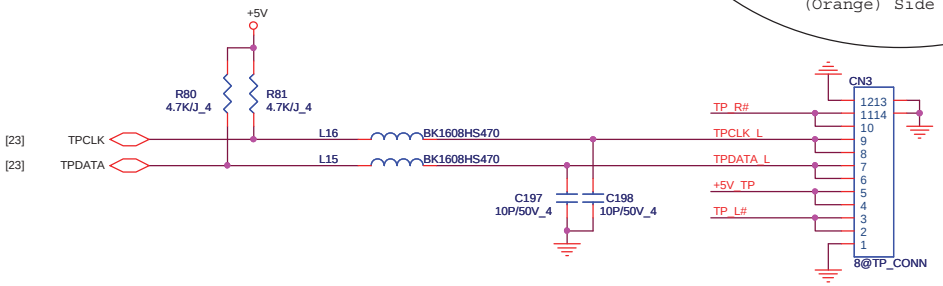


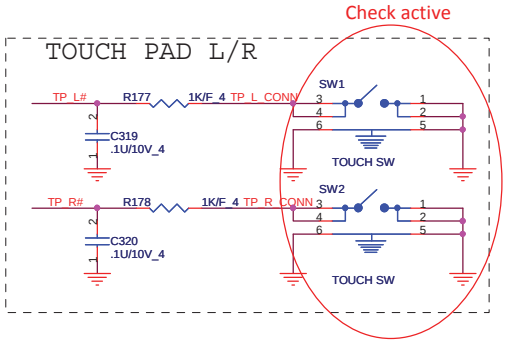
20090821:
Add TPD Right / Left side LED.

Touch Pad D/B (TPD)









NB5

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Quanta Computer Inc.

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	KB/BT/TPD	1A

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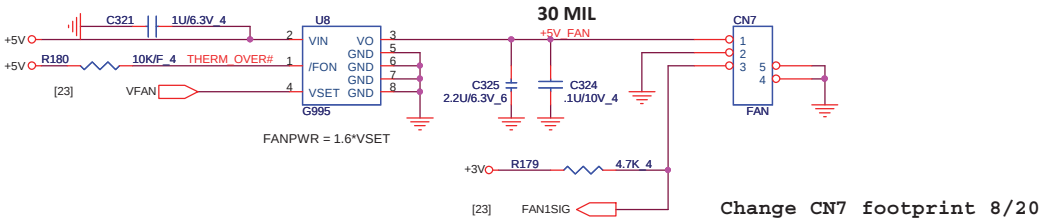
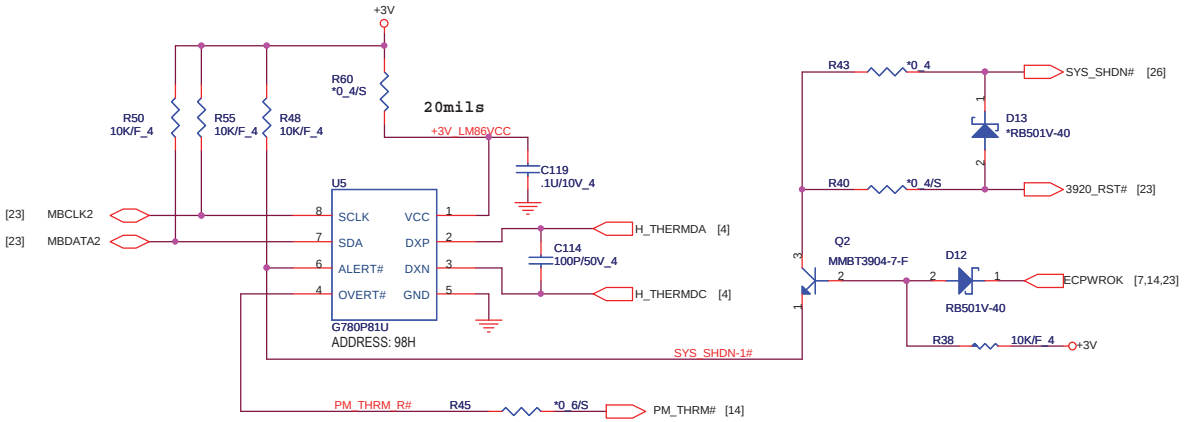
CPU FAN CTRL(THM)



CPU Thermal Monitor(THM)



NB5	PROJECT : QL1 Quanta Computer Inc.	
	Size:	Document Number: FAN/THERMAL — Rev: 1A
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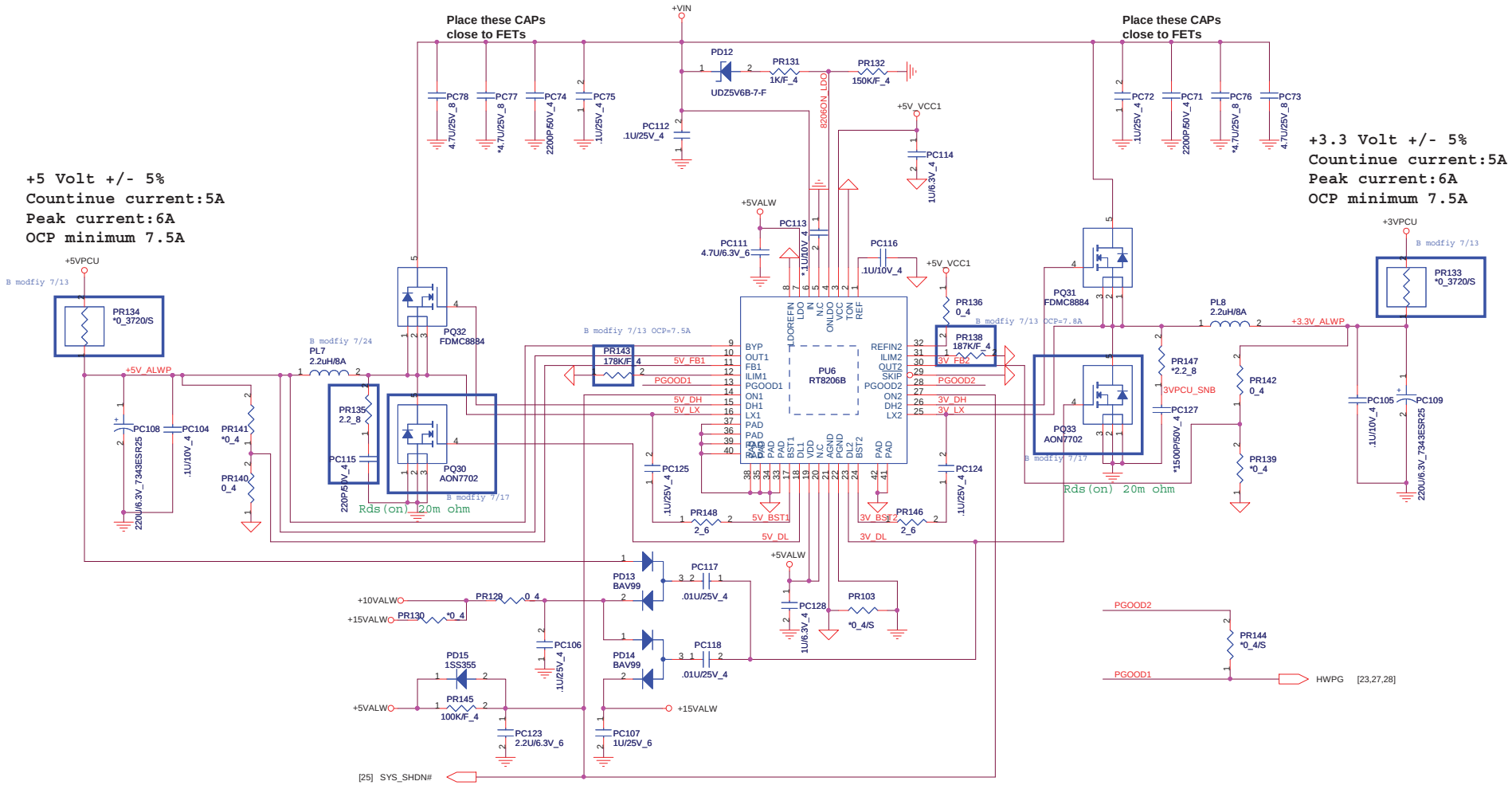

NB5	PROJECT : QL1 Quanta Computer Inc.		
	Size: Custom	Document Number: +5V/+3V (RT8206B)	Rev: 1A
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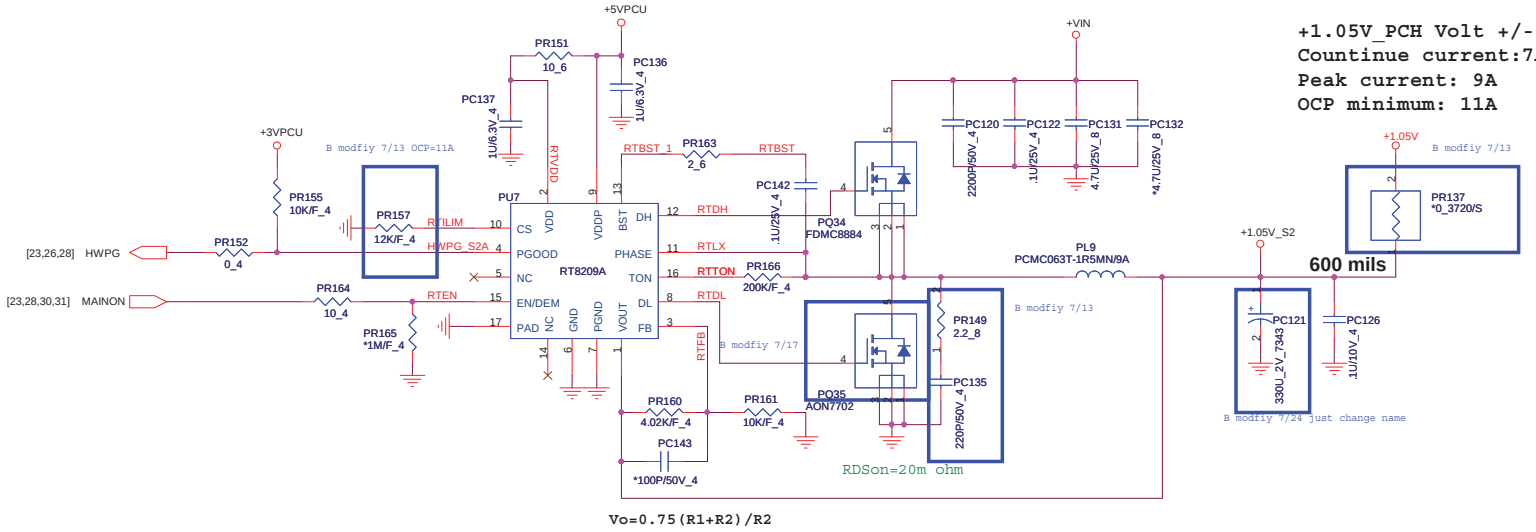
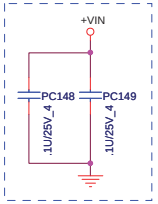
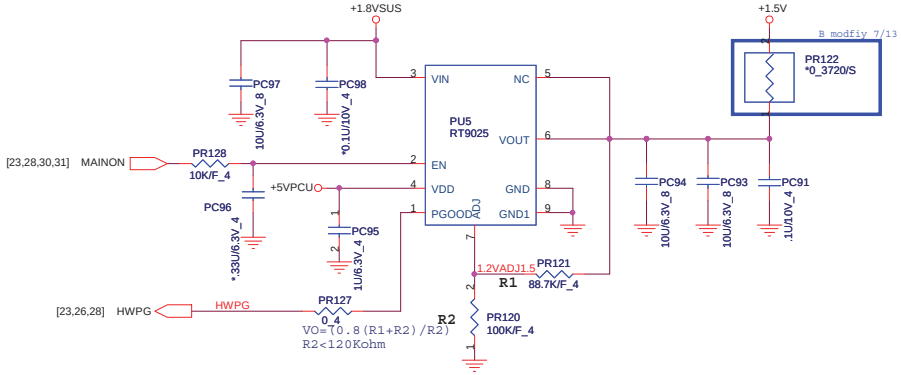


Vo=0.75(R1+R2)/R2

+1.05V_PCH Volt +/- 5%
Countinue current:7A
Peak current: 9A
OCP minimum: 11A



Add two cap for EMI 8/6



VO=T0.8(R1+R2)/R2)
R2<120Kohm

+1.5 Volt +/- 5%
Countinue current:2A
Peak current:3A

NB5	PROJECT : QL1 Quanta Computer Inc.	
Size: Custom	Document Number: +1.1V VTT / PCH	Rev: 1A
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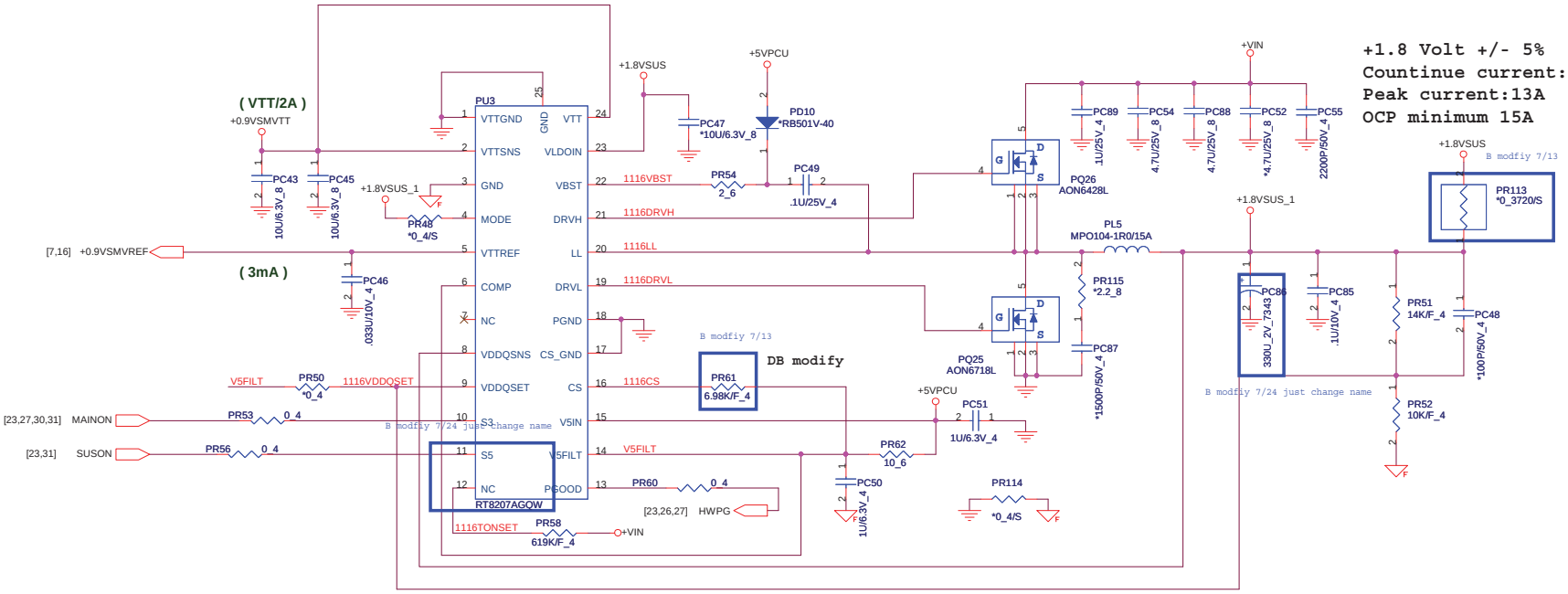

NB5	PROJECT : QL1 Quanta Computer Inc.	
Size: Custom	Document Number: DDR3 (RT8207)	Rev: 1A
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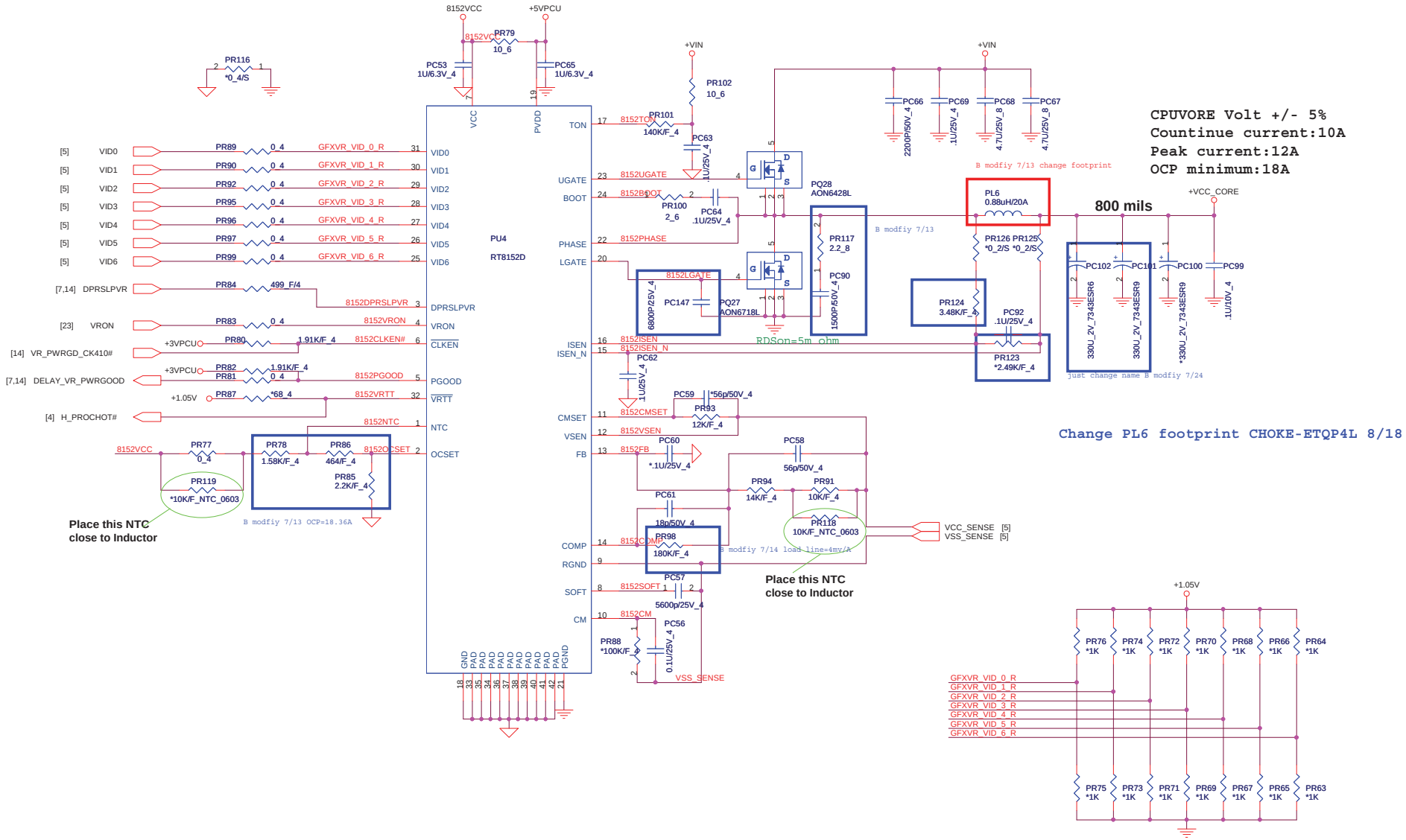

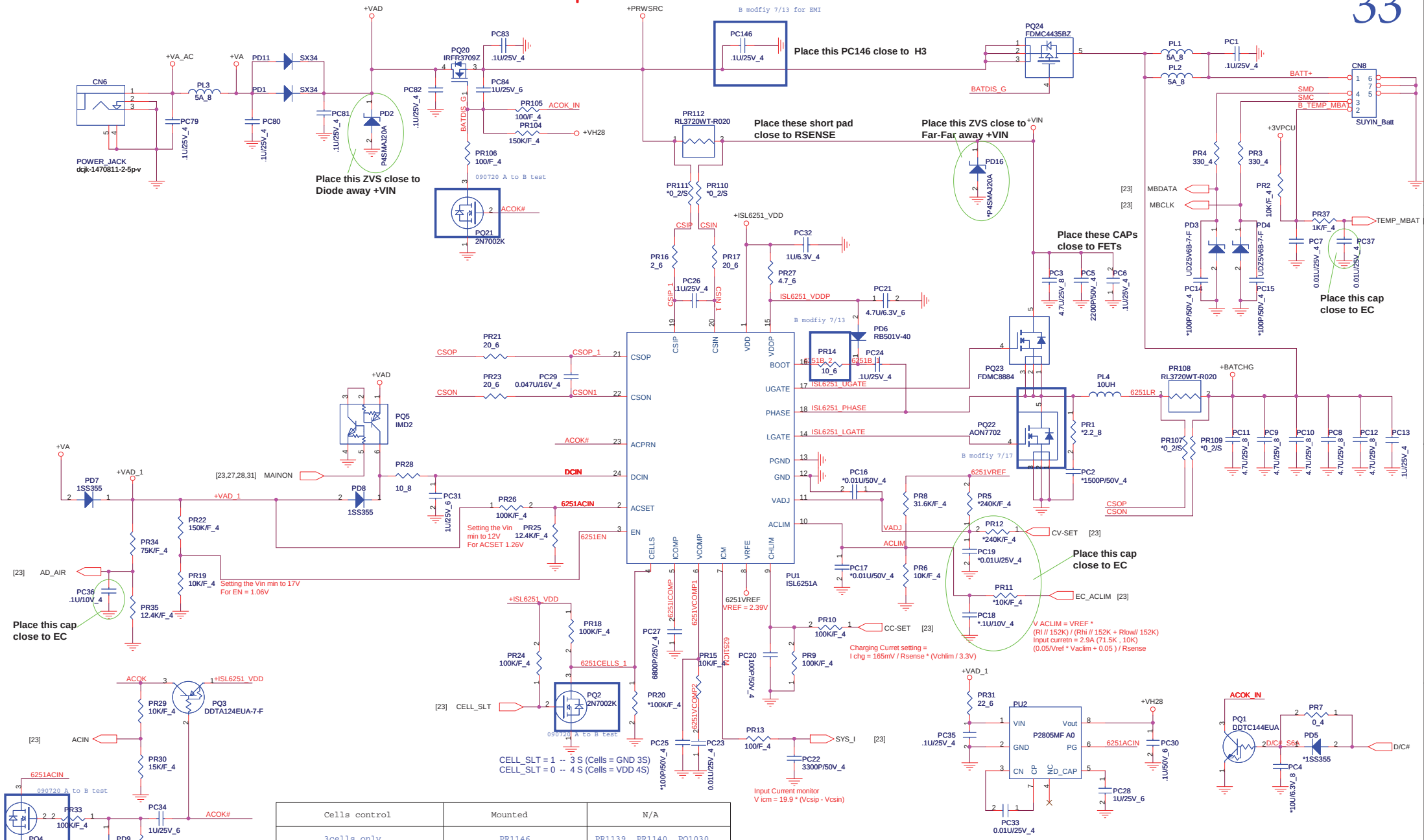

Cells control	Mounted	N/A
3cells only option for 3cells/4cells	PR1146 PR1139, PR1140, PQ1030	PR1139, PR1140, PQ1030 PR1146

NB5

PROJECT : QL1
Quanta Computer Inc.

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Custom	Charger (ISL6251)	1A

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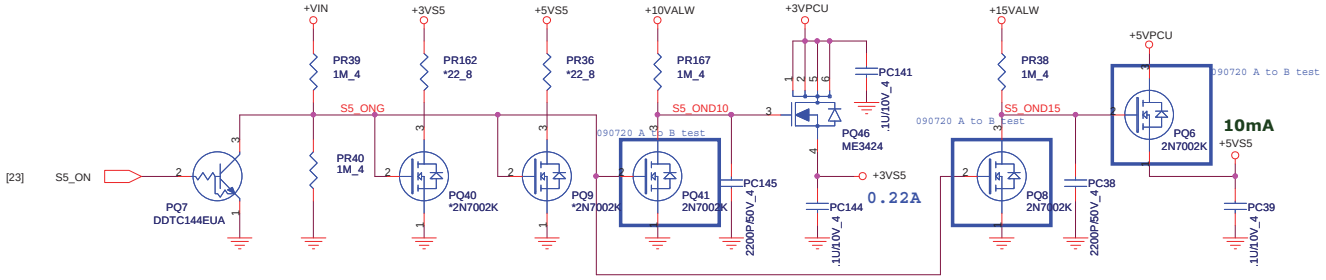

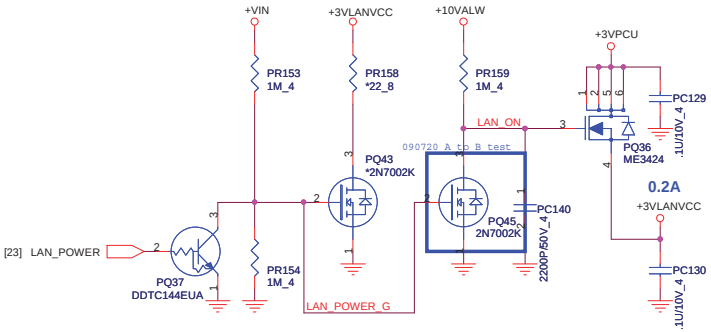

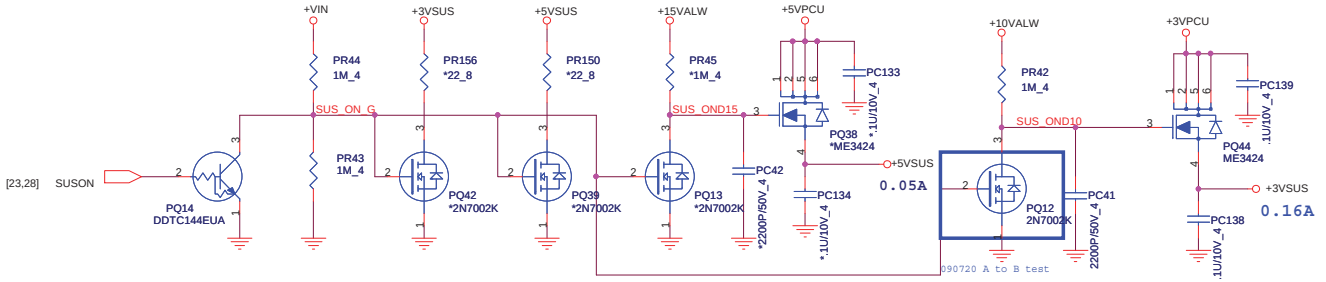

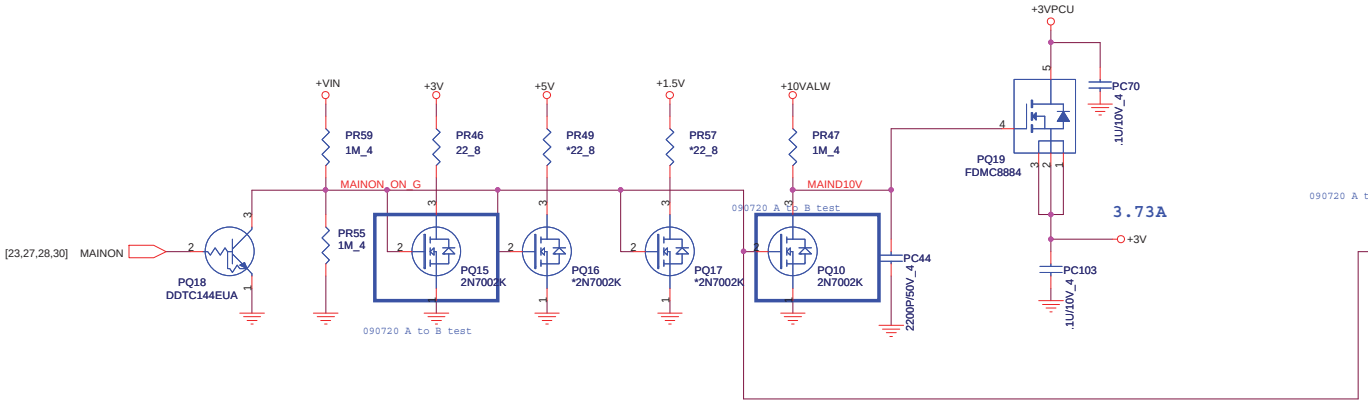

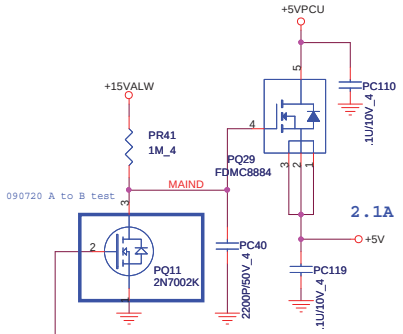

NB5

PROJECT : QL1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Discharge / 1.5V /2.5V	1A

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QW6 DV1 to QL1 DV1 modify list:

Page 3 : 1. ADD BOM R249 475ohm.
2. Change BOM R233,R279 2.2Kohm.
3. Link NET PU_BSEL0,CPU_BSEL1,CPU_BSEL2
4. C361, C362, C365 stuff 10pF for EMI.

Page 12: 1. C243 modify 10pF for EMI.

Page 17: 1. Change U1 footprint 6pin to 5pin.
2. C422, C423 modify for EMI.

Page 18: 1. ADD BOM R156 4.7kohm.
2. Stuff L25 for EMI.
3. L1, L2, L3 modify BK1608LL680 for EMI.

Page 19: 1. Audio CODEC modify to ALC272 + AMP from ALC269 for LG request.

Page 21: 1. Add WLAN module power switch circuit.
2. Add 3G module power switch.
3. Use one 0 ohm for JSIM1 pin 10 (CD) contact with CN15 pin 7 (CLKREQ#) , but not stuff 0 ohm.

Page 22: 1. Change LED Color (ORANGE/BLUE).
2. LED circuit modify no stuff.
3. Add SMART Button & LED & RF LED line for CN4.

Page 23: 1. Add Smart Button line contact with EC.

Page 24: 1. Add TPD Right/ Left side LED.

All page: 81,C88,C89,C148,C167,C348,C351,C353 footprint from Ecap3_5x2_8-3-1_1h change to cc3528-1_1h.

NB5

PROJECT : QL1
Quanta Computer Inc.

Size	Document Number	Rev
B	Modify list	1A

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