INTEL® PENTIUM® II/PENTIUM® III PROCESSOR (SC242) / INTEL 810e CHIPSET

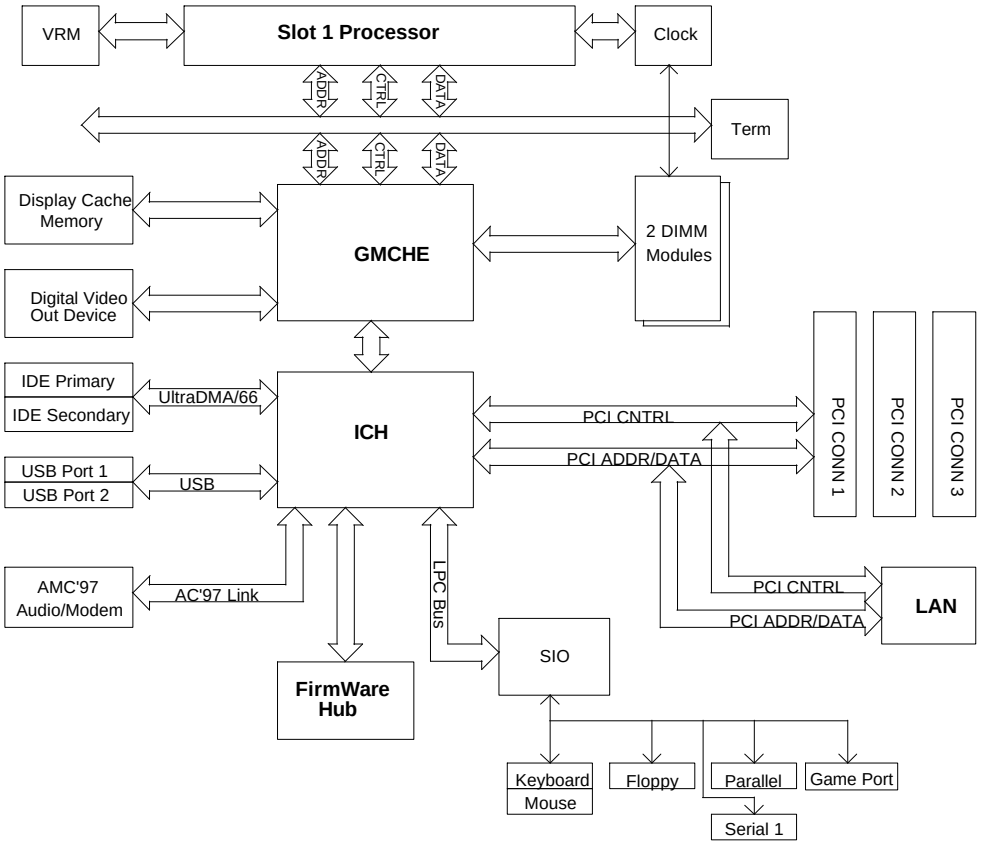
UNIPROCESSOR CUSTOMER REFERENCE SCHEMATICS

REVISION 1.0

** Please note these schematics are subject to change.

Title: Intel® 810e Chipset Customer Reference Board Cover Sheet		REV. 1.0
intel® Platform Components Division 1900 Prairie City Road Folsom, Ca. 95630	Last Revision Date: 6/14/99 Sheet: 1 of 33	

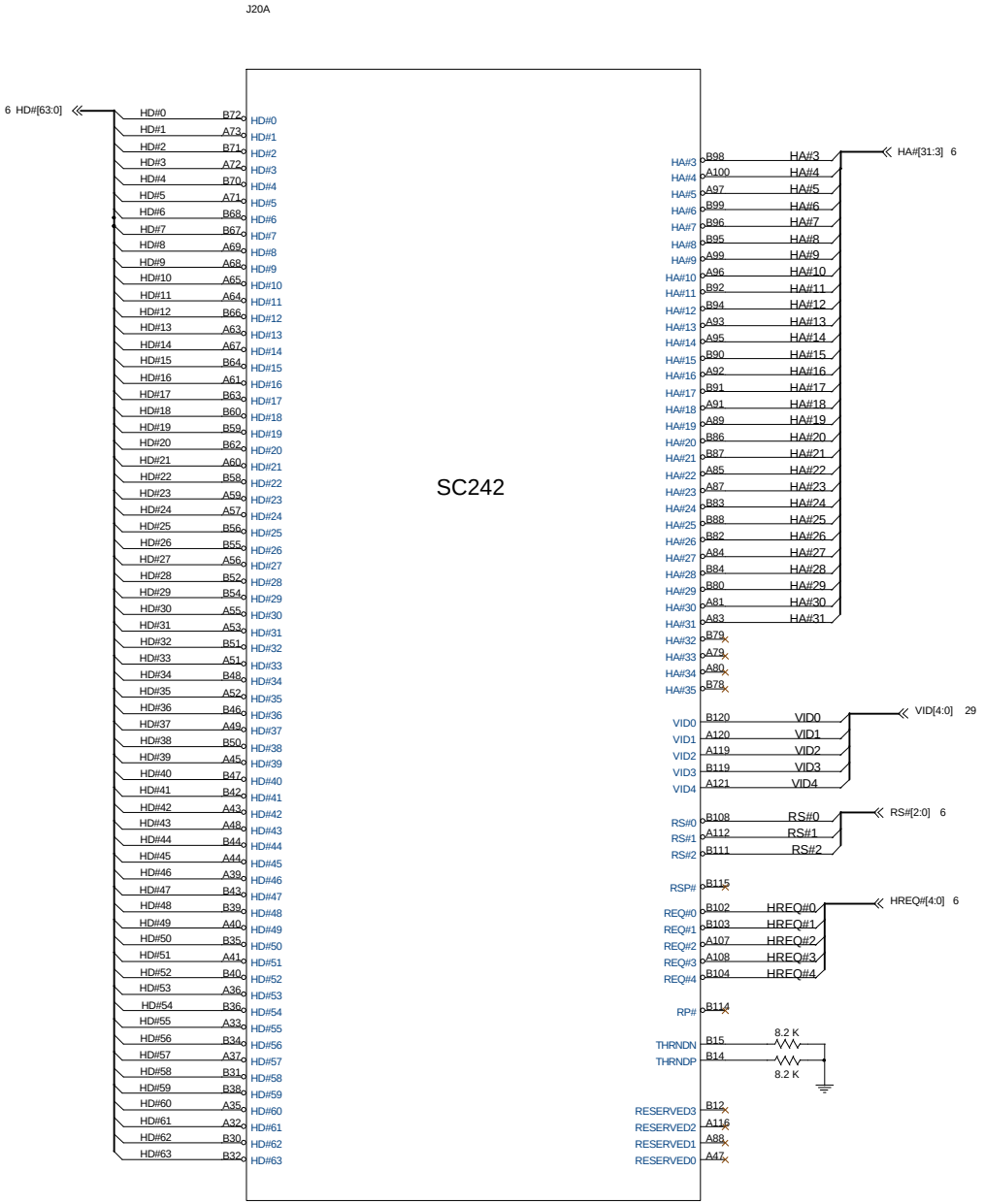
Block Diagram



Title: Intel® 810e Chipset Customer Reference Board Block Diagram		REV. 1.0
intel® Platform Components Division 1900 Prairie City Road Folsom, Ca. 95630	Last Revision Date: 6/14/99 Sheet: 2 of 33	

SC242 CONNECTOR

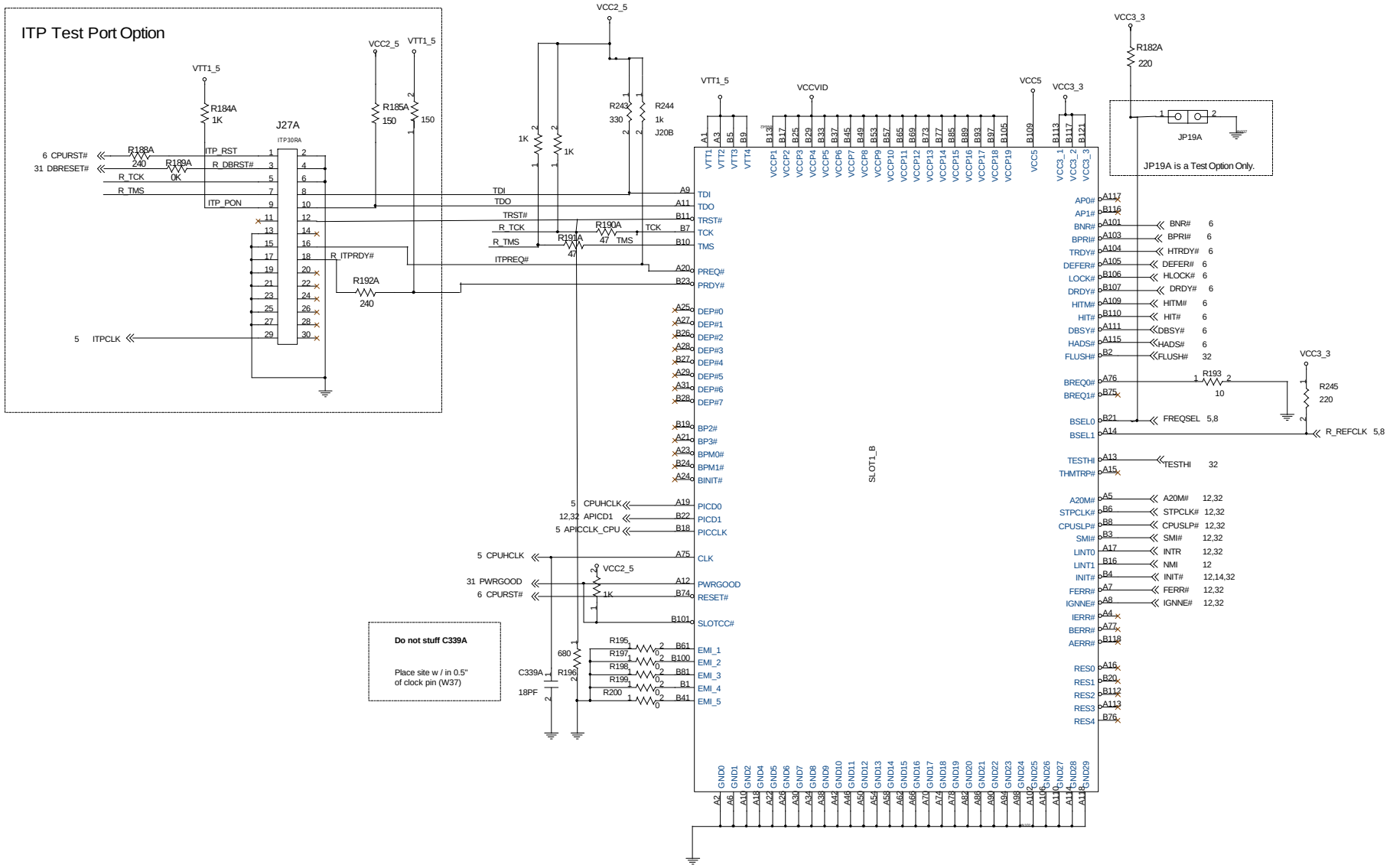
Part 1



Title: Intel® 810e Chipset Customer Reference Board SC242 CONNECTOR: PART1		REV. 1.0
intel® Platform Components Division 1900 Prairie City Road Folsom, Ca. 95630	Last Revision Date: 2/22/99 Sheet: 3 of 33	

SLOT 1

Part 2



Title: Intel® 810e Chipset Customer Reference Board		REV.
SC242 Connector: Part 2		1.0
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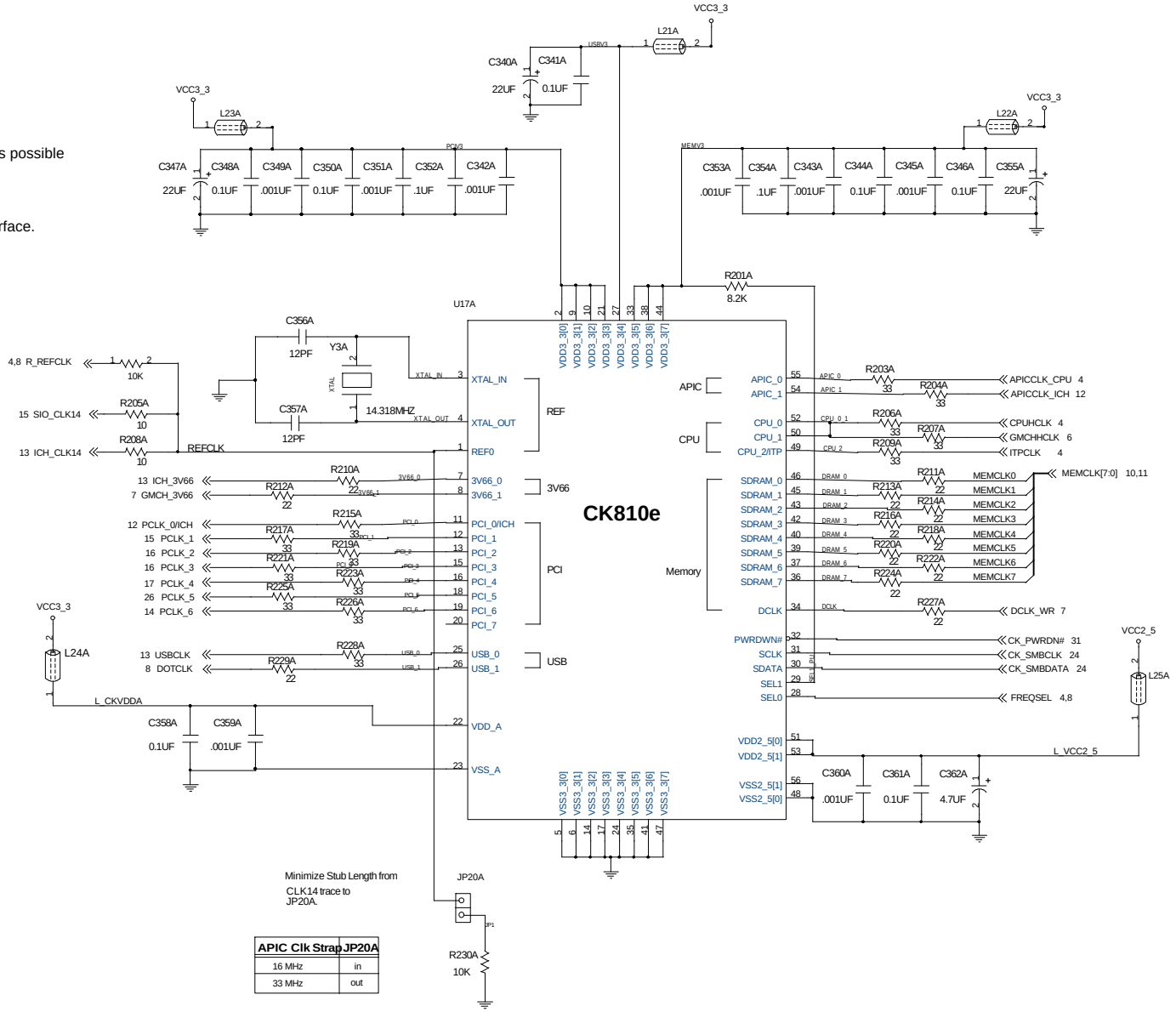
Clock Synthesizer

Notes:

- Place all decoupling caps as close to VCC/GND pins as possible
- PCI_0/ICH pin has to go to the ICH.
  (This clock cannot be turned off through SMBus)
- CPU_ITP pin must go to the ITP. It is the only
  CPU CLK that can be shut off through the SMBUS interface.



APIC Clk Strap	JP20A
16 MHz	in
33 MHz	out

Title: Intel® 810e Chipset Customer Reference Board Clock Synthesizer		REV. 1.0
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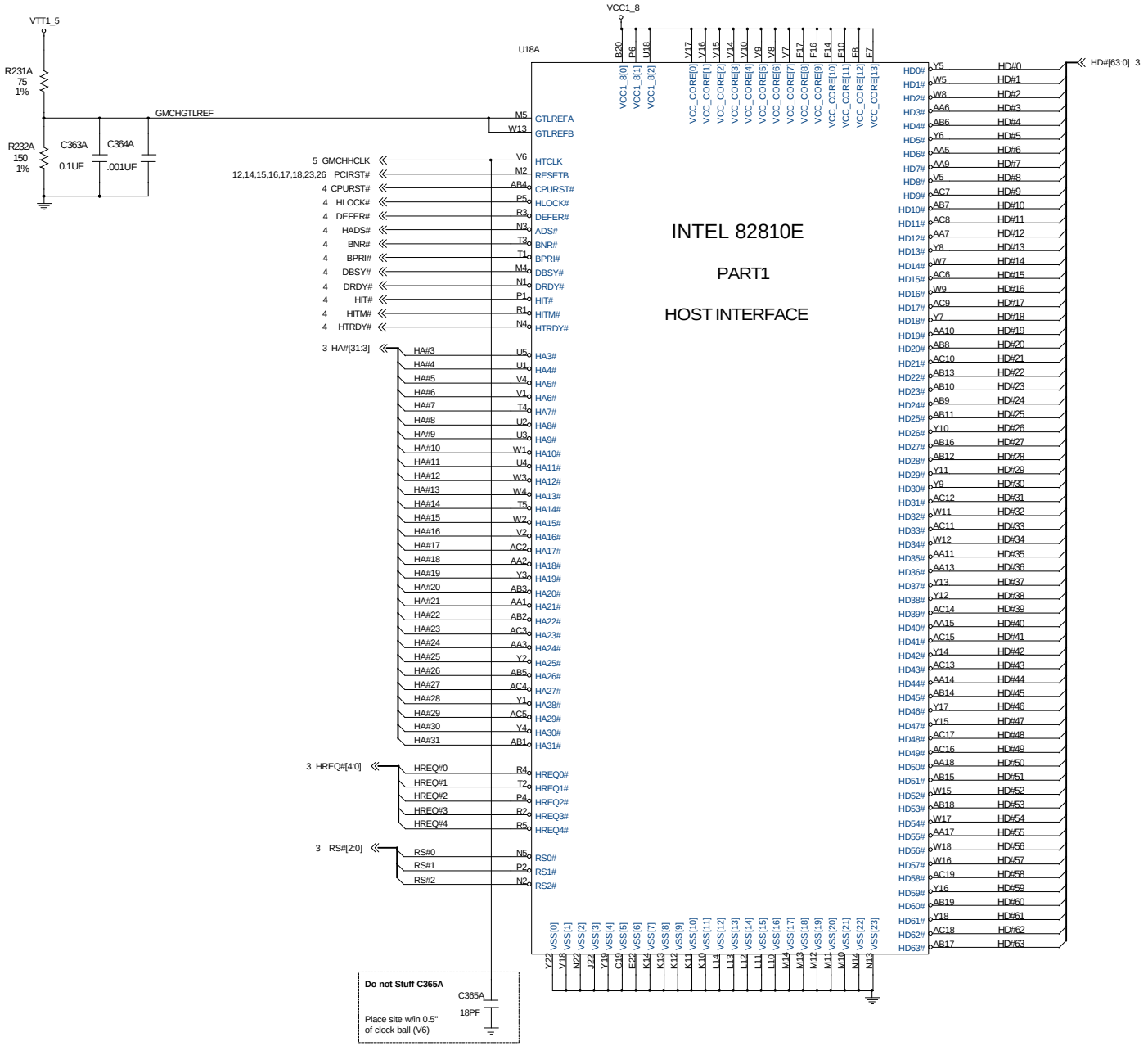
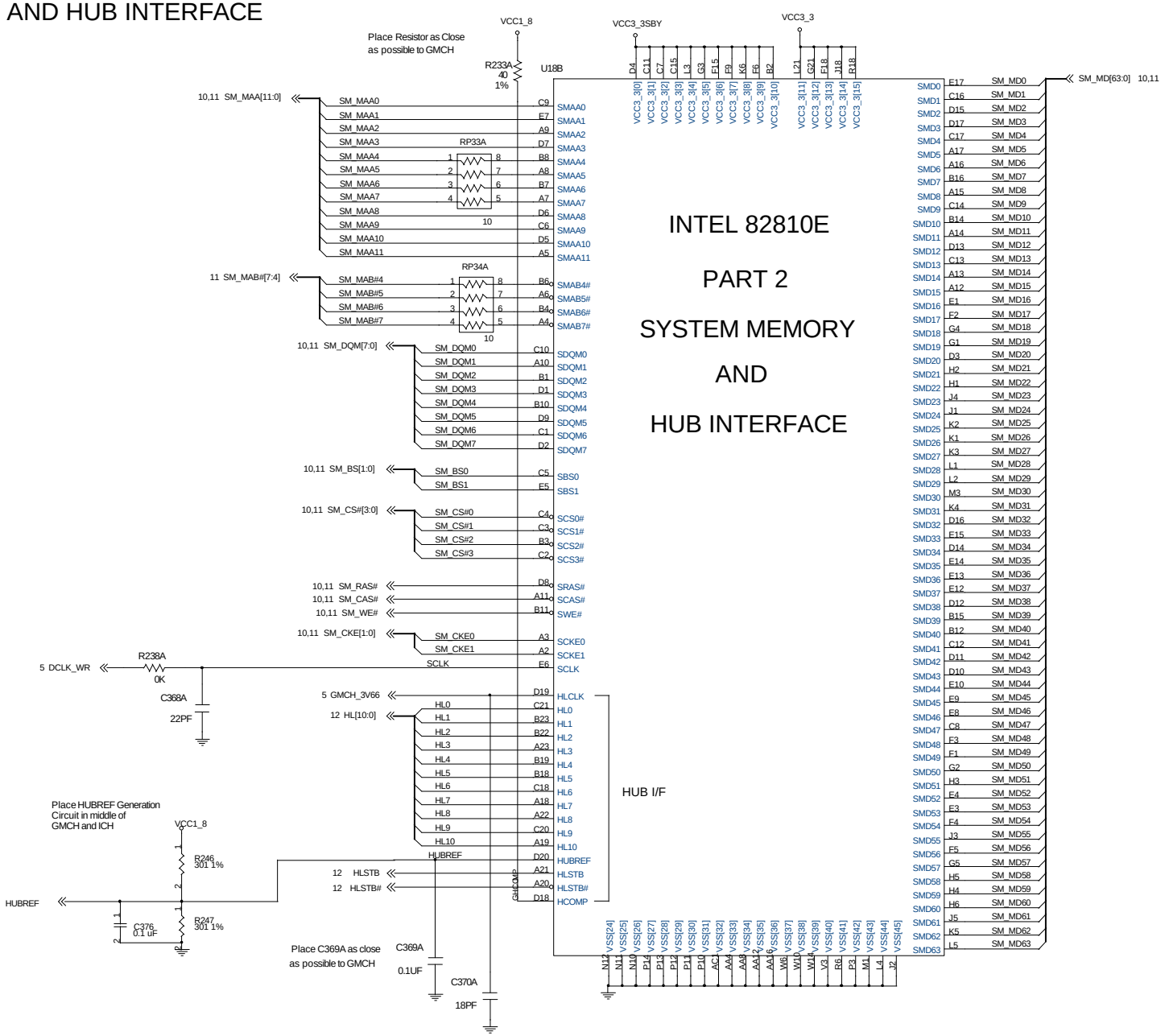
82810E, PART 1: HOST INTERFACE



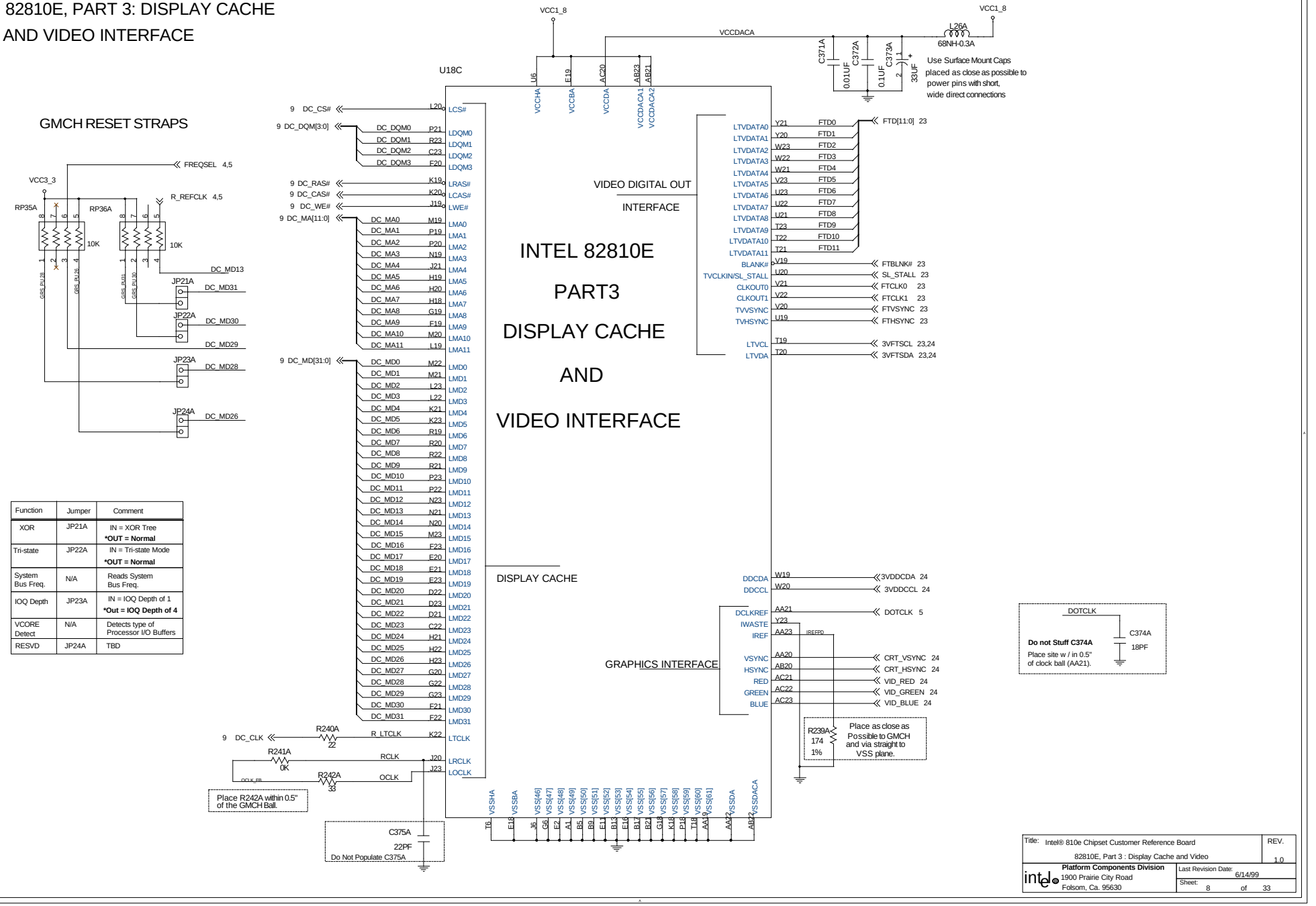
Title: Intel® 810e Chipset Customer Reference Board 82810E, Part 1: Host Interface		REV. 1.0
intel® Platform Components Division 1900 Prairie City Road Folsom, Ca. 95630	Last Revision Date: 6/14/99 Sheet: 6 of 33	

82810E, PART 2: SYSTEM MEMORY AND HUB INTERFACE



Title: Intel® 810e Chipset Customer Reference Board 82810E, Part 2: System Memory and Hub		REV. 1.0
intel® Platform Components Division 1900 Prairie City Road Folsom, Ca. 95630	Last Revision Date: 6/14/99	Sheet: 7 of 33

82810E, PART 3: DISPLAY CACHE AND VIDEO INTERFACE



Function	Jumper	Comment
XOR	JP21A	IN = XOR Tree ***OUT = Normal**
Tri-state	JP22A	IN = Tri-state Mode ***OUT = Normal**
System Bus Freq.	N/A	Reads System Bus Freq.
IOQ Depth	JP23A	IN = IOQ Depth of 1 ***Out = IOQ Depth of 4**
VCORE Detect	N/A	Detects type of Processor I/O Buffers
RESVD	JP24A	TBD

Title: Intel® 810e Chipset Customer Reference Board 82810E, Part 3 : Display Cache and Video		REV. 1.0
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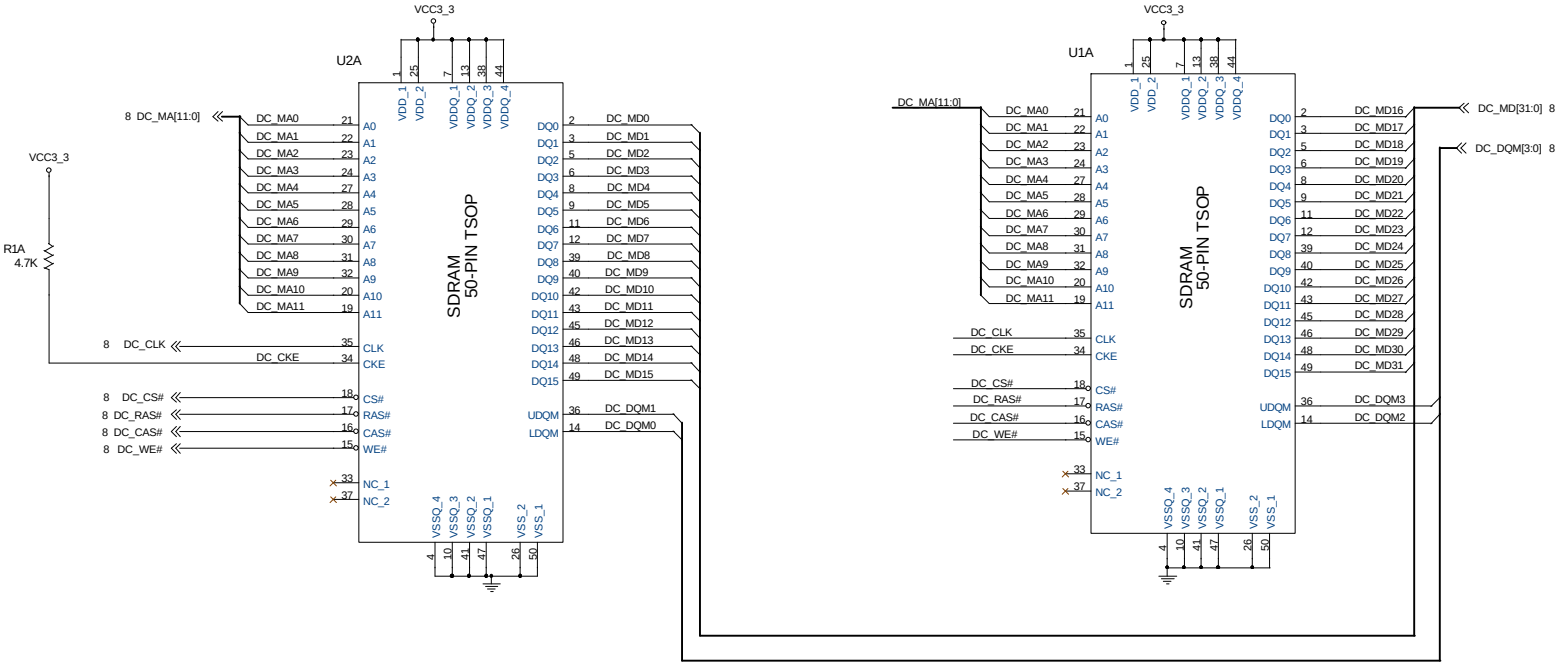
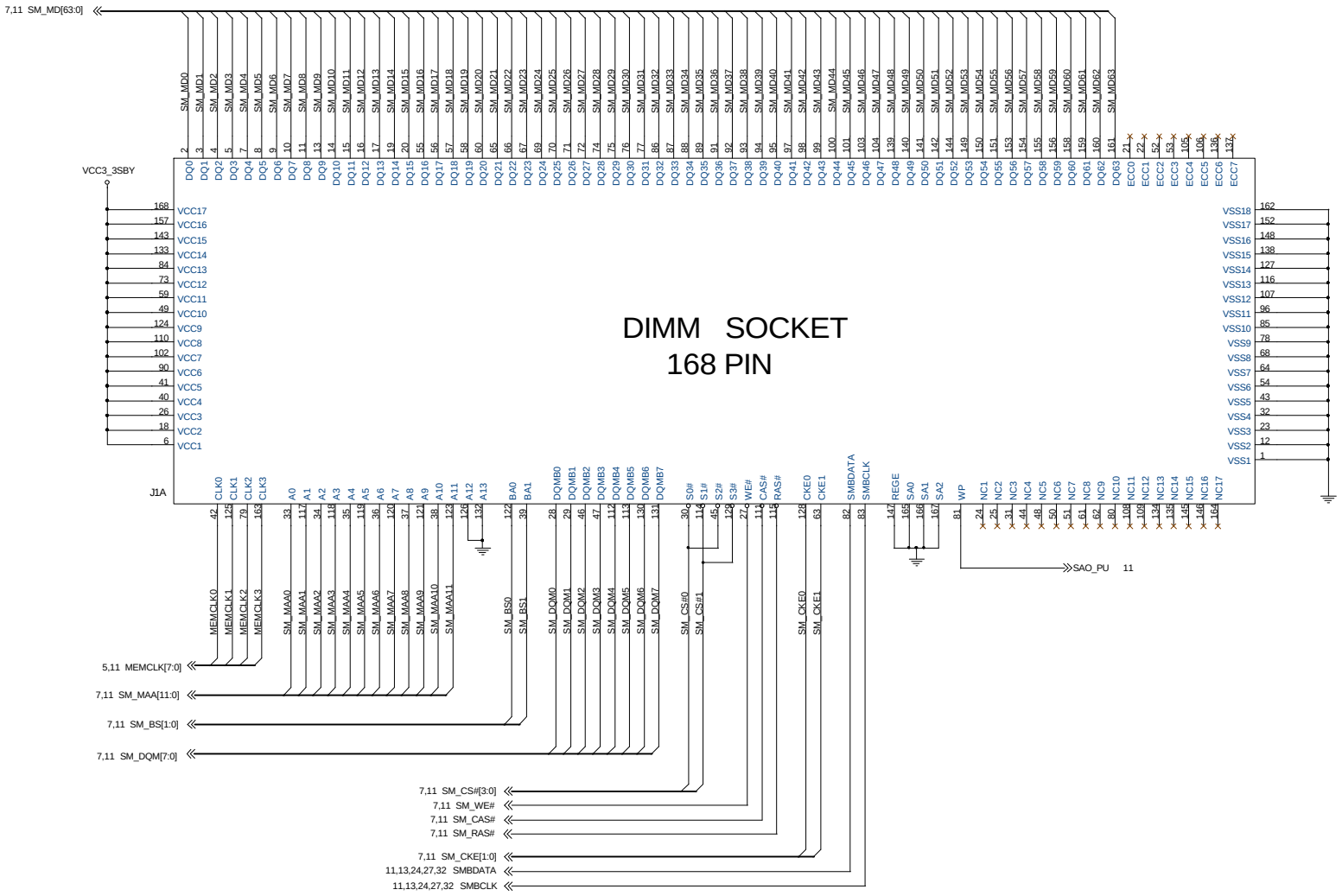
	Sheet: 8 of 33	

4MB Display Cache



Title: Intel® 810e Chipset Customer Reference Board Display Cache		REV. 1.0
intel® Platform Components Division 1900 Prairie City Road Folsom, Ca. 95630	Last Revision Date: 6/14/99 Sheet: 9 of 33	

SYSTEM MEMORY



Title: Intel® 810e Chipset Customer Reference Board		REV. 1.0
System Memory : DIMM0		
intel® Platform Components Division 1900 Prairie City Road Folsom, Ca. 95630	Last Revision Date: 6/14/99	
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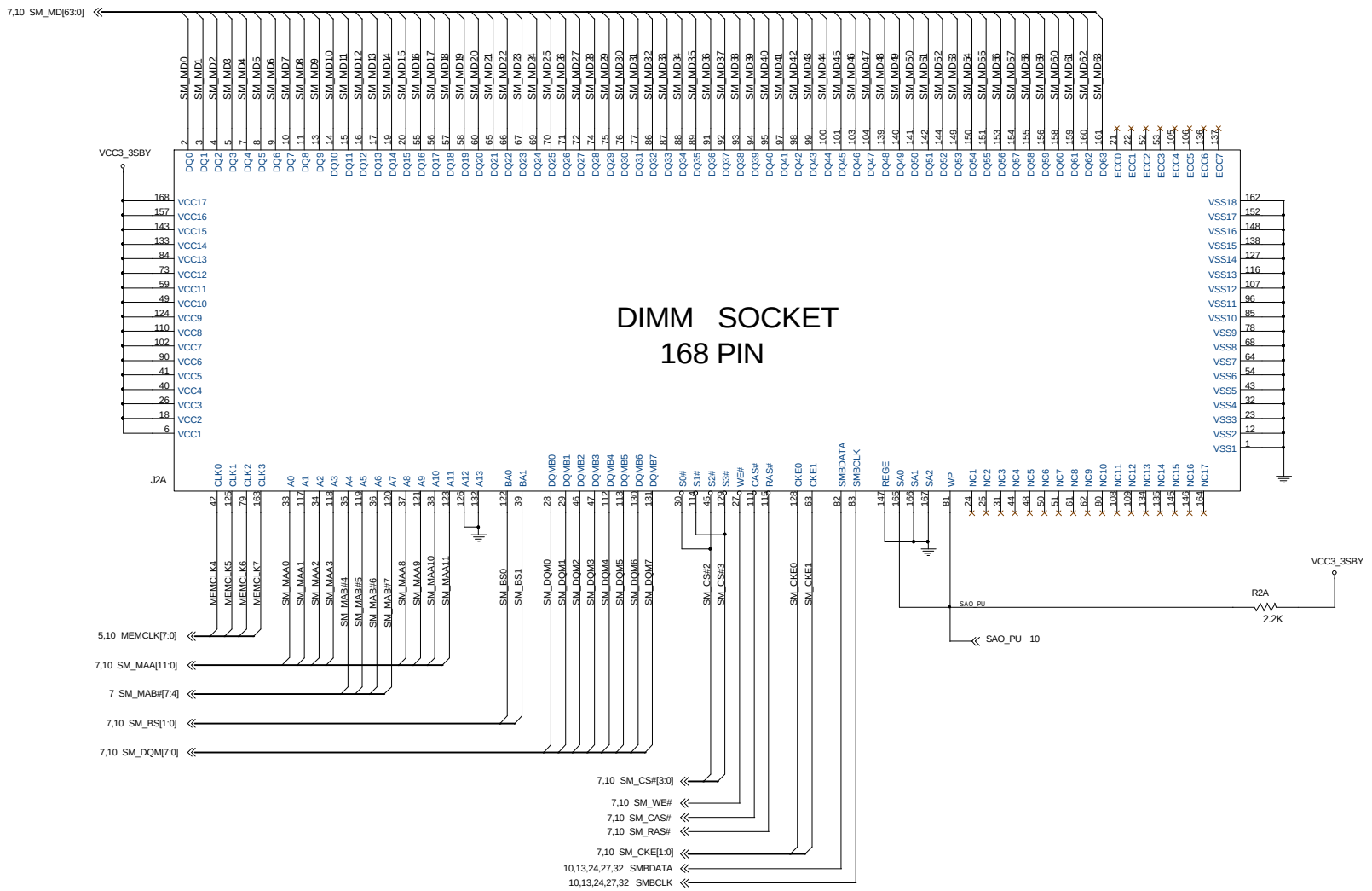
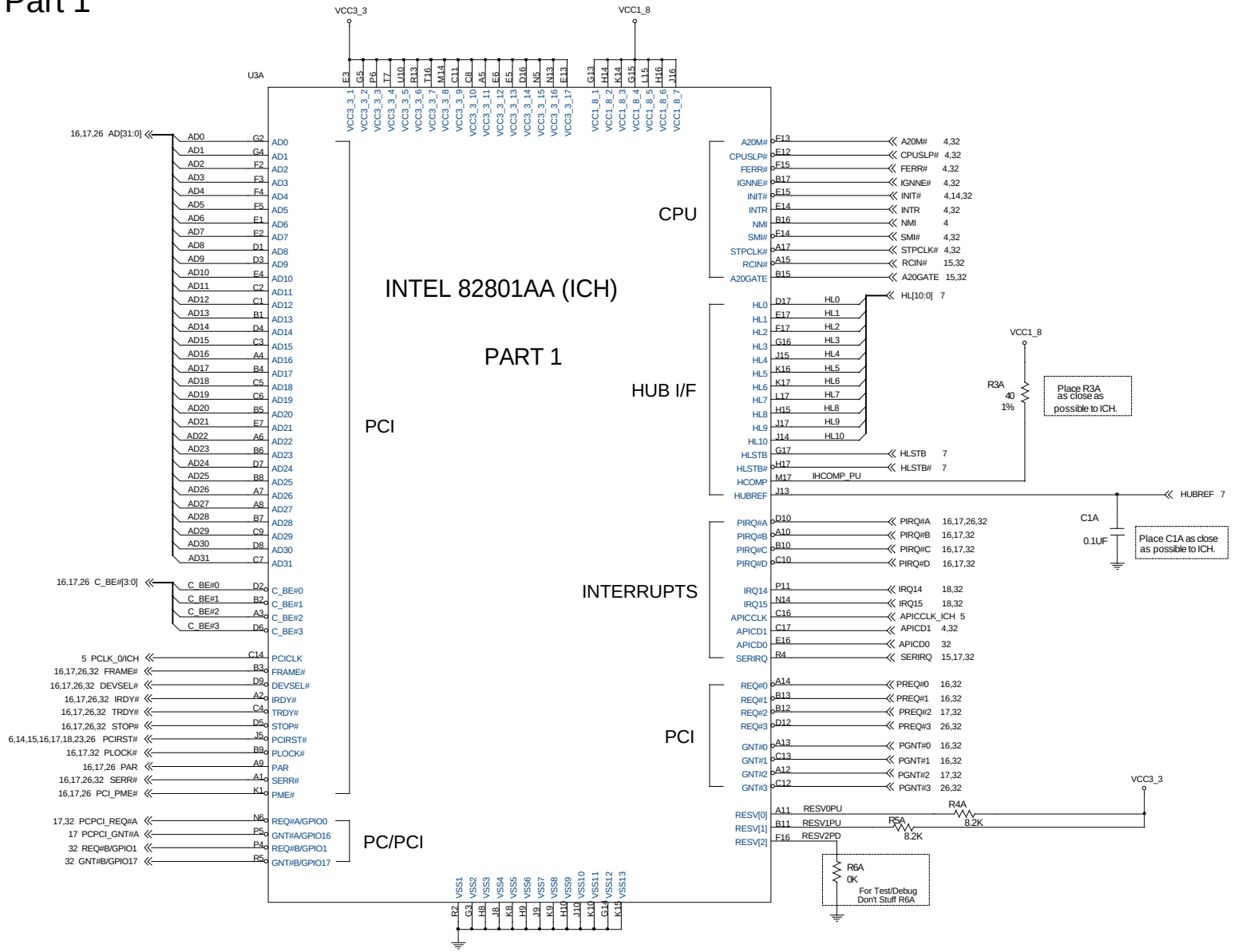
SYSTEM MEMORY



Title: Intel® 810e Chipset Customer Reference Board System Memory : DIMM1		REV. 1.0
intel® Platform Components Division 1900 Prairie City Road Folsom, Ca. 95630	Last Revision Date: 6/14/99 Sheet: 11 of 33	

ICH, Part 1



Title: Intel® 810e Chipset Customer Reference Board ICH, Part 1		REV. 1.0
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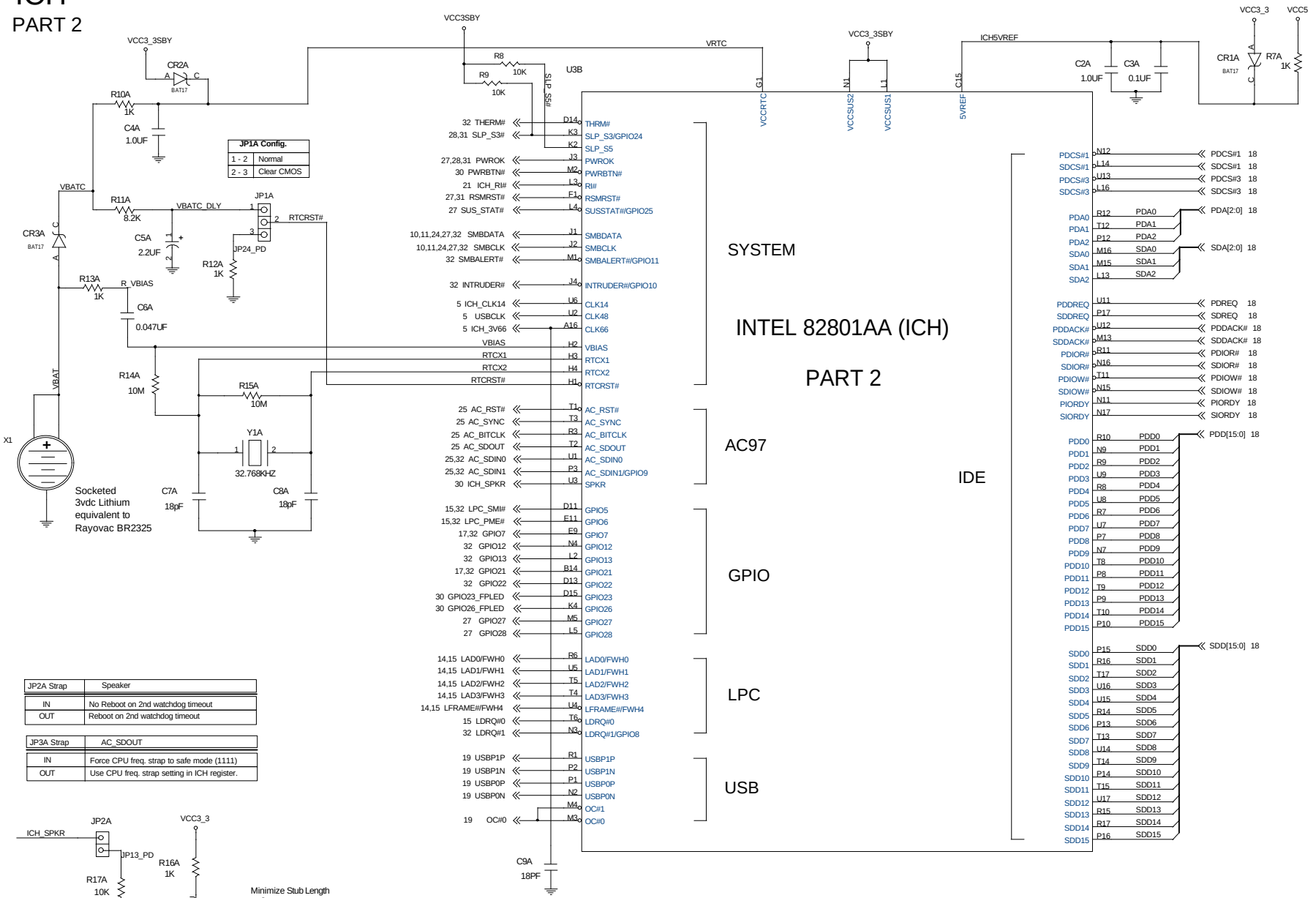
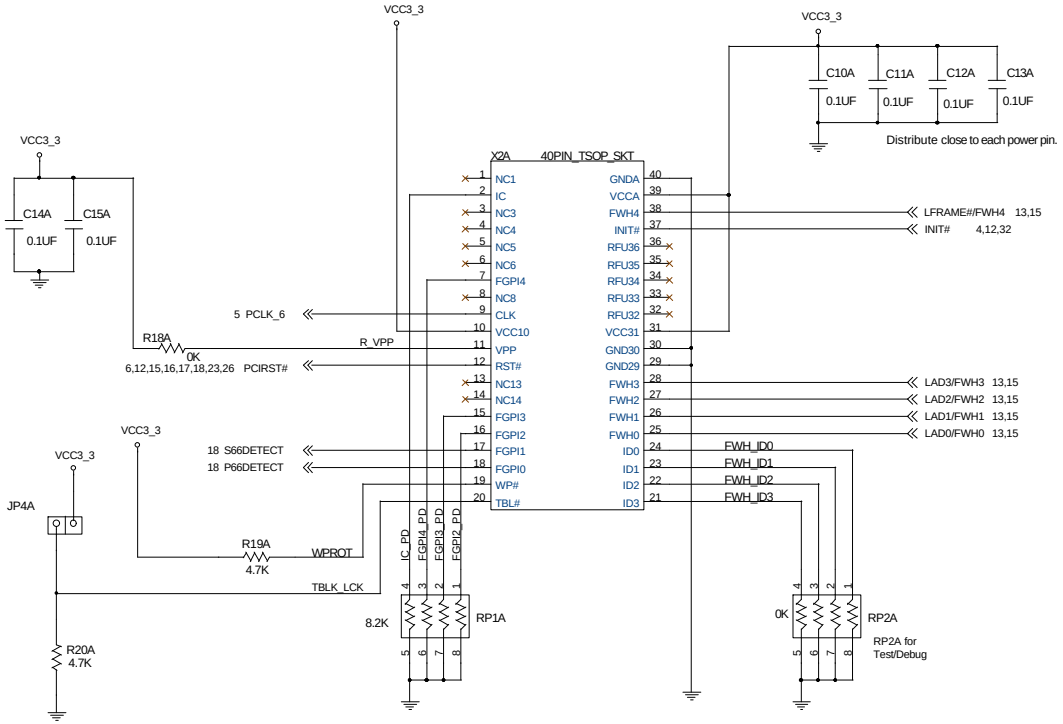
ICH
PART 2



Title: Intel® 810e Chipset Customer Reference Board		REV.
ICH, Part 2		1.0
intel	Platform Components Division 1900 Prairie City Road Folsom, Ca. 95630	Last Revision Date: 6/14/99 Sheet: 13 of 33

FirmWare Hub (FWH) Socket

NOTE: This is a Socketed Implementation



JP4A CONFIG		
IN	Unlocked	
OUT	Locked	Default

Notes:

VPP and WP# are tied to 3.3v
in this configuration Write Protection is register based
with the exception of the Boot Block.

Title: Intel® 810e Chipset Customer Reference Board FIRMWARE HUB (FWH)		REV. 1.0
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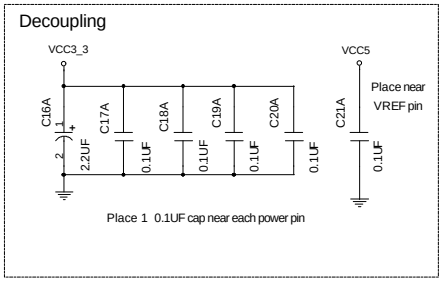
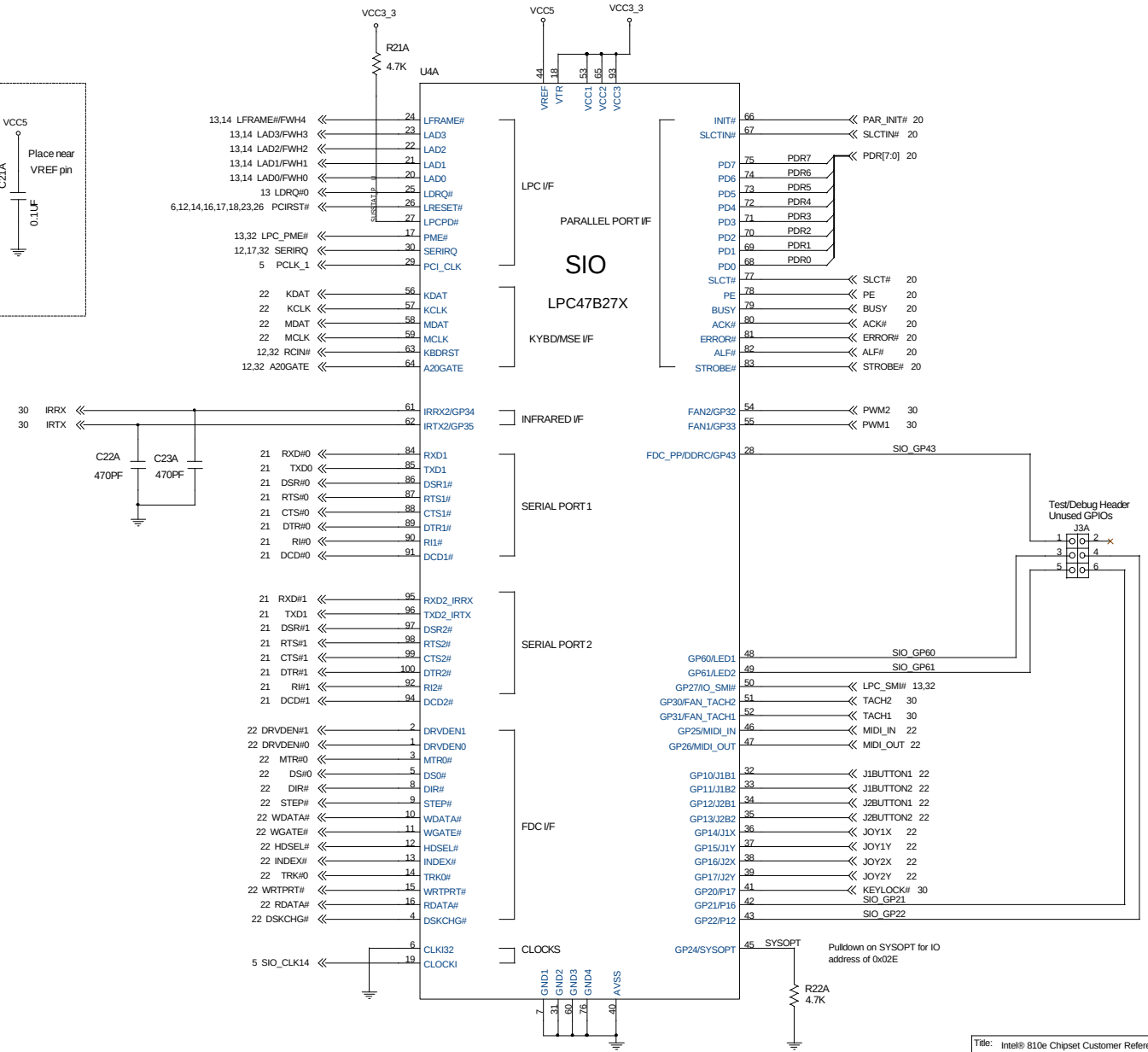
Super I/O





Title:	Intel® 810e Chipset Customer Reference Board
	Super I/O
REV.	1.0
Platform Components Division	1900 Prairie City Road, Folsom, Ca. 95630
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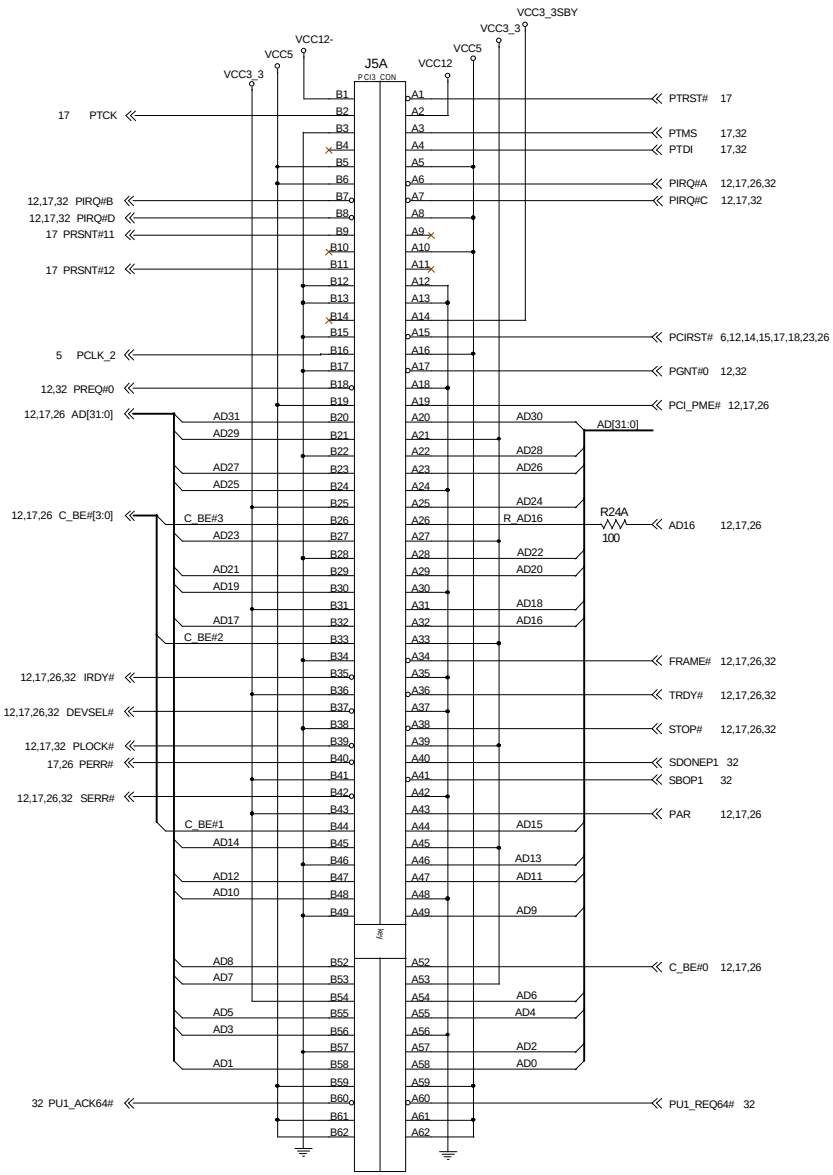
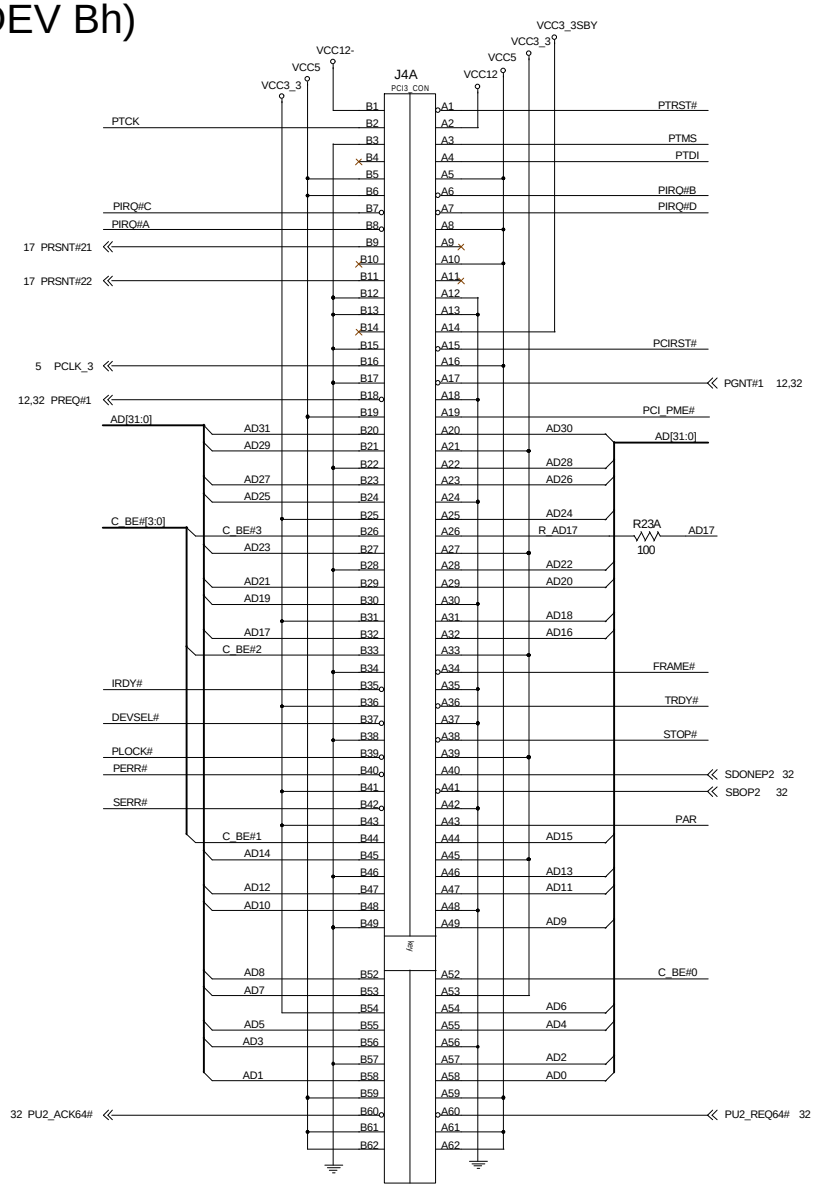
PCI Connector 0 (DEV Ah)



PCI Connector 1 (DEV Bh)



Title: Intel® 810e Chipset Customer Reference Board PCI Connectors 1 and 2		REV. 1.0
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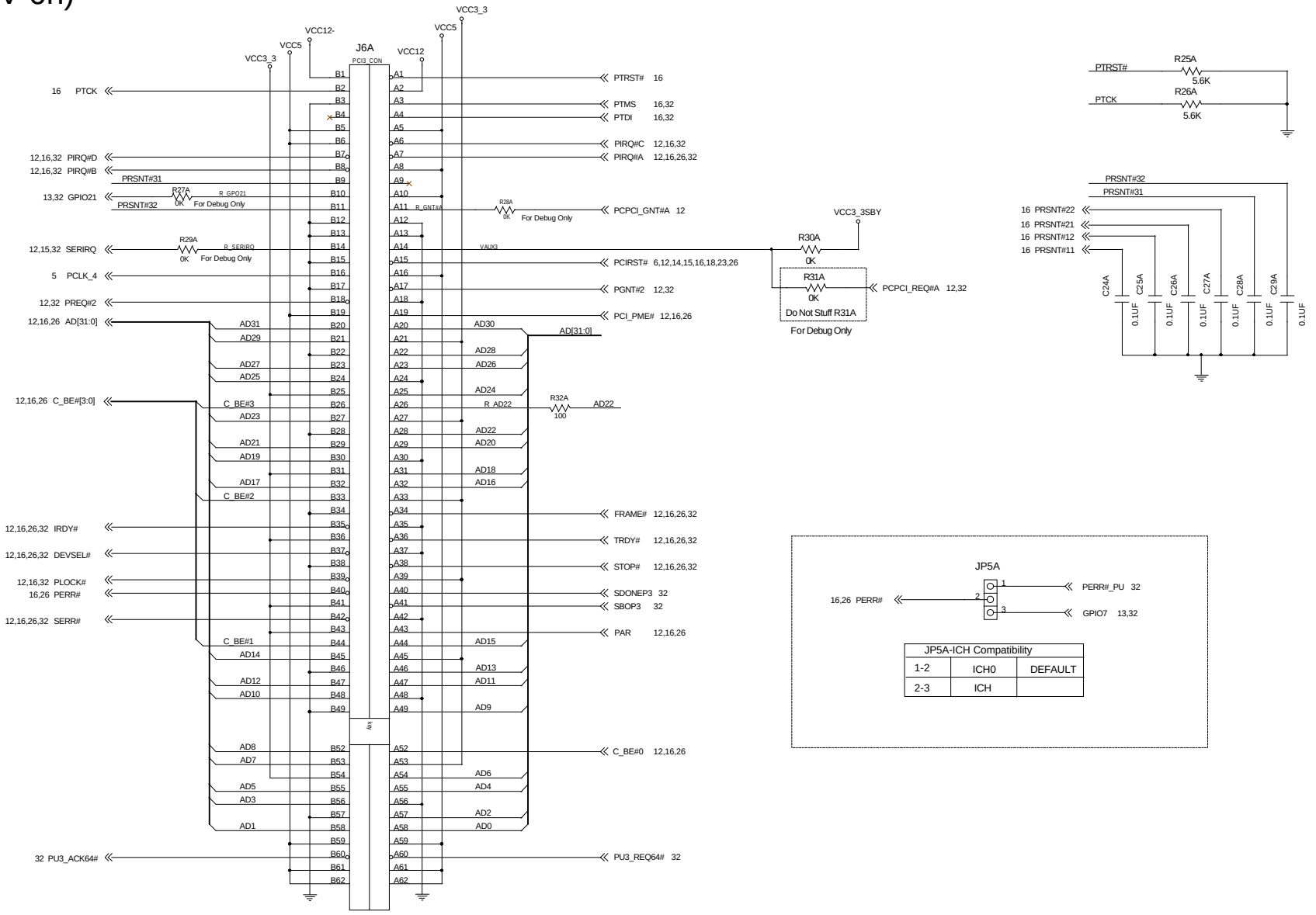
PCI Connector 2 (DEV 6h)

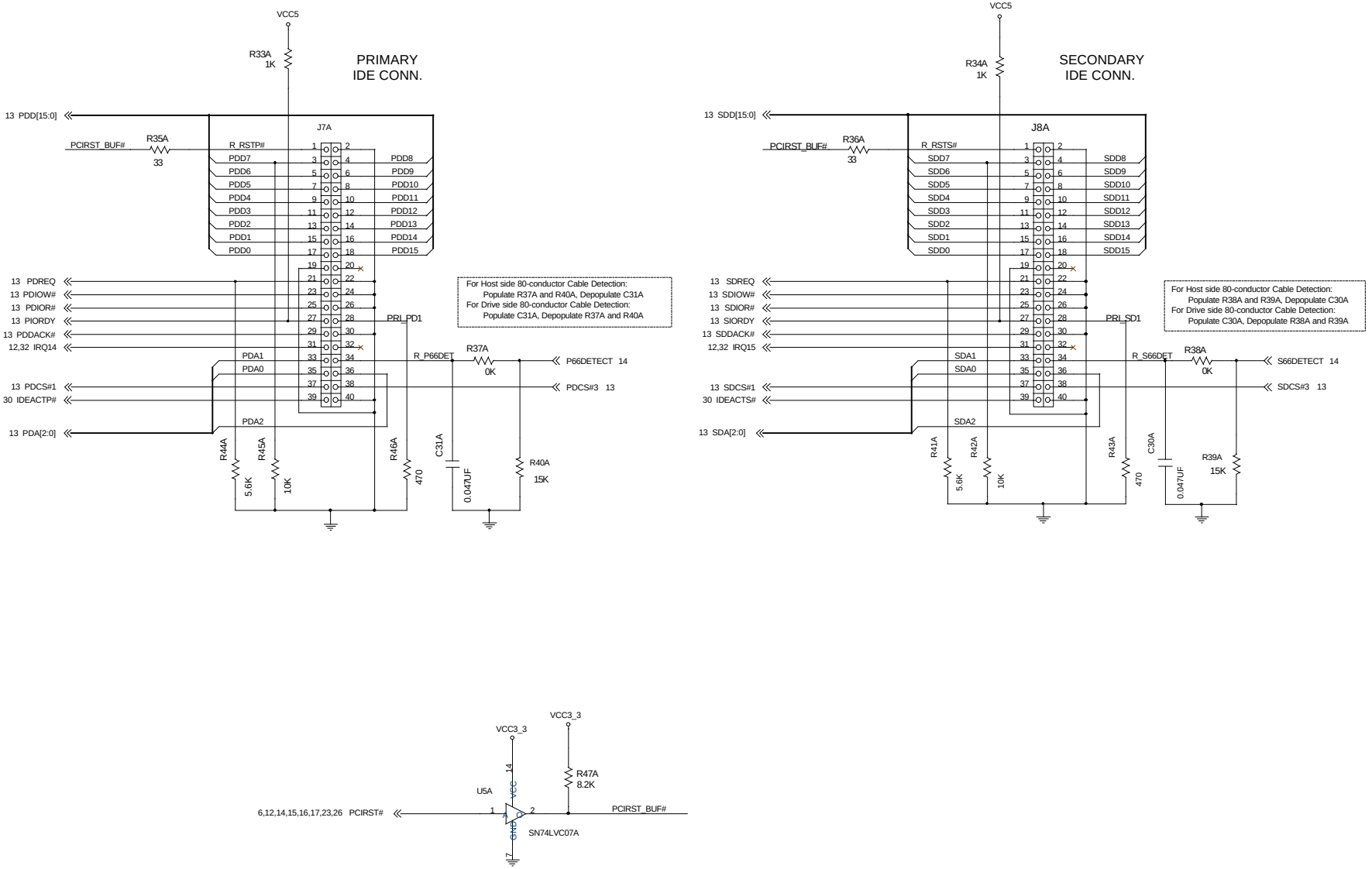
Layout Note: Should be in Slot 0 Position (Outside Edge of Board Furthest from CPU)



JP5A-ICH Compatibility		
1-2	ICH0	DEFAULT
2-3	ICH	

Title: Intel® 810e Chipset Customer Reference Board PCI Connector 2		REV. 1.0
intel® Platform Components Division 1900 Prairie City Road Folsom, Ca. 95630	Last Revision Date: 6/14/99 Sheet: 17 of 33	

ULTRA-ATA66 IDE CONNECTORS



Title: Intel® 810e Chipset Customer Reference Board ULTRAATA/66 IDE CONNECTORS		REV. 1.0
intel® Platform Components Division 1900 Prairie City Road Folsom, Ca. 95630	Last Revision Date: 6/14/99	
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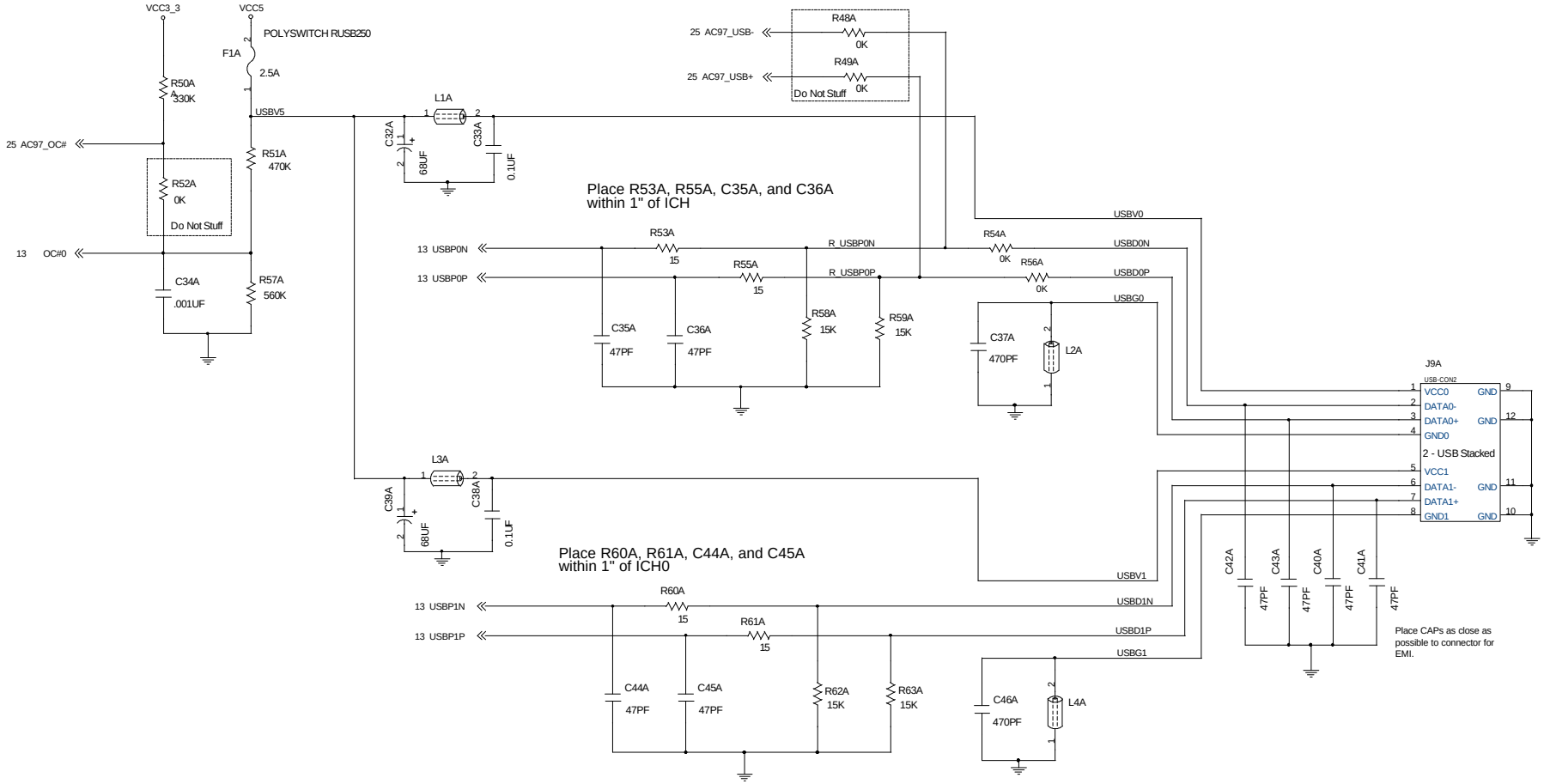
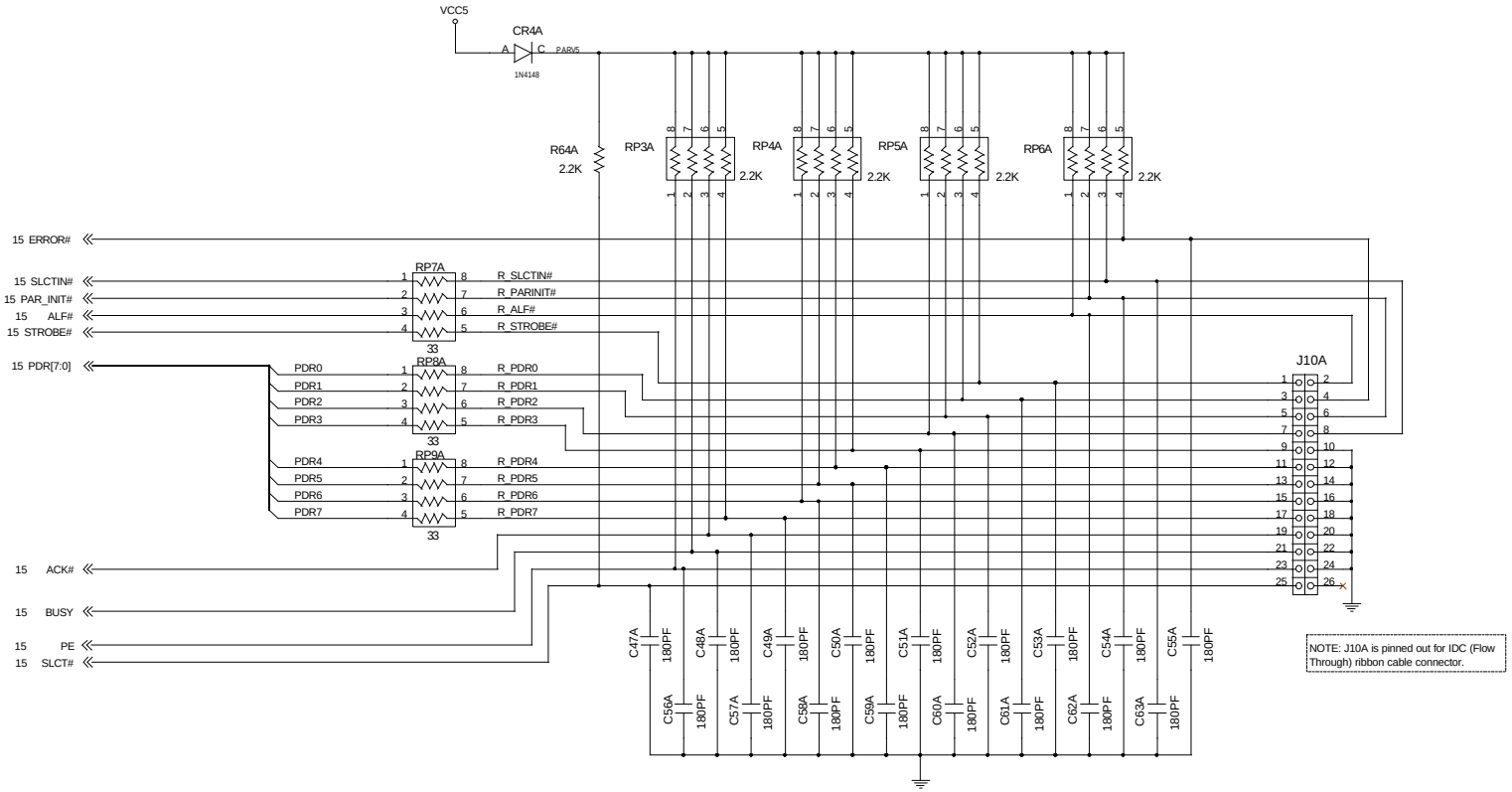
USB Connectors



Title: Intel® 810e Chipset Customer Reference Board USB Connectors	REV. 1.0
intel® Platform Components Division 1900 Prairie City Road Folsom, Ca. 95630	Last Revision Date: 6/14/99 Sheet: 19 of 33

Parallel Port Header



Title: Intel® 810e Chipset Customer Reference Board Parallel Port Header		REV. 1.0
intel® Platform Components Division 1900 Prairie City Road Folsom, Ca. 95630	Last Revision Date: 6/14/99	
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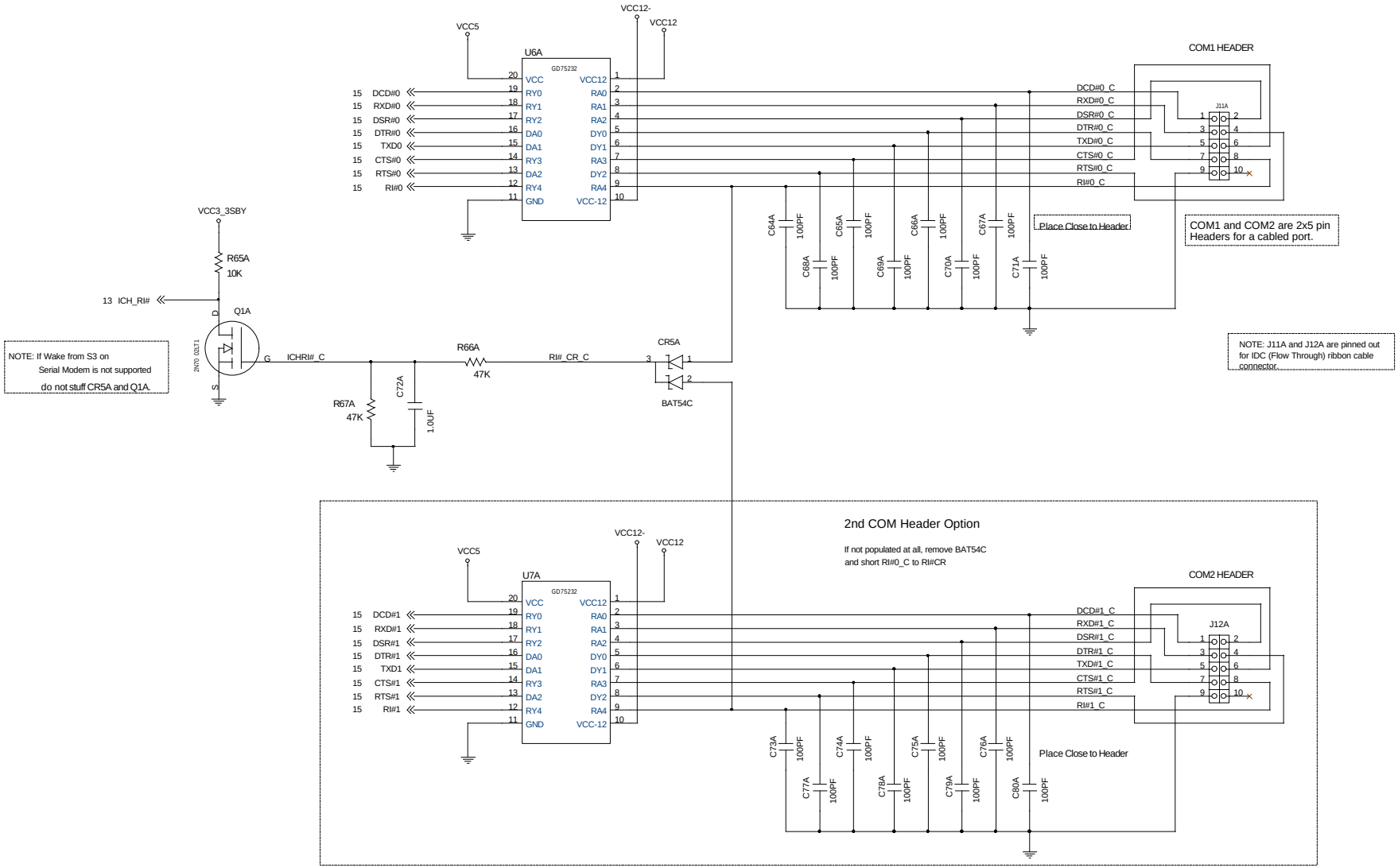
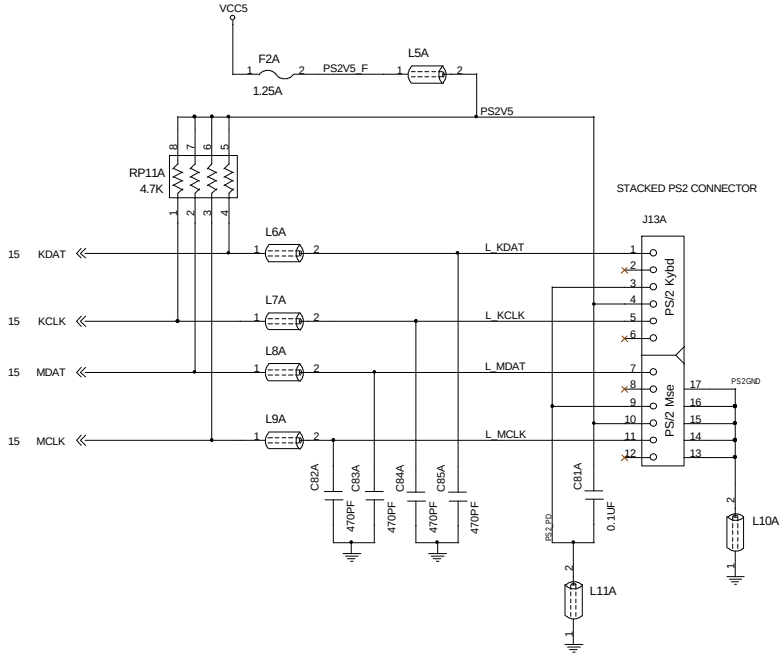
Serial Port/COM Headers

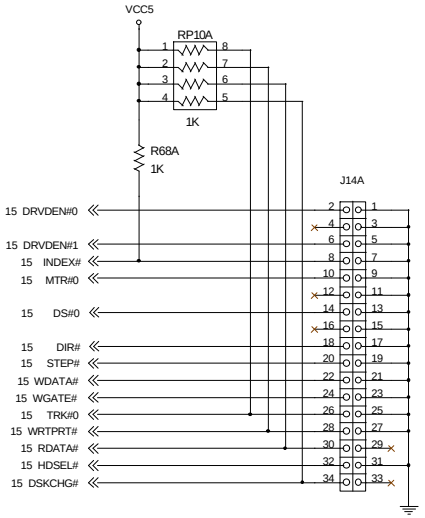


Title: Intel® 810e Chipset Customer Reference Board Serial Port/ COM Headers		REV. 1.0
intel® Platform Components Division 1900 Prairie City Road Folsom, Ca. 95630	Last Revision Date: 6/14/99 Sheet: 21 of 33	

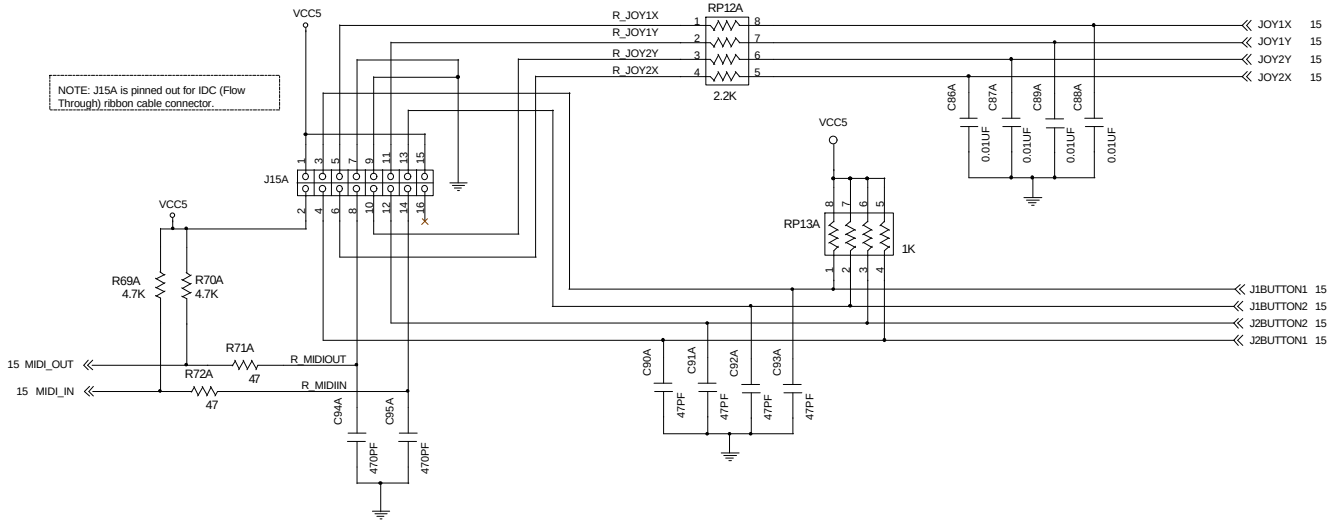
KEYBOARD/MOUSE PORTS



FLOPPY DISK HEADER



GAME PORT HEADER



Title: Intel® 810e Chipset Customer Reference Board KEYBOARD/MOUSE PORTS		REV. 1.0
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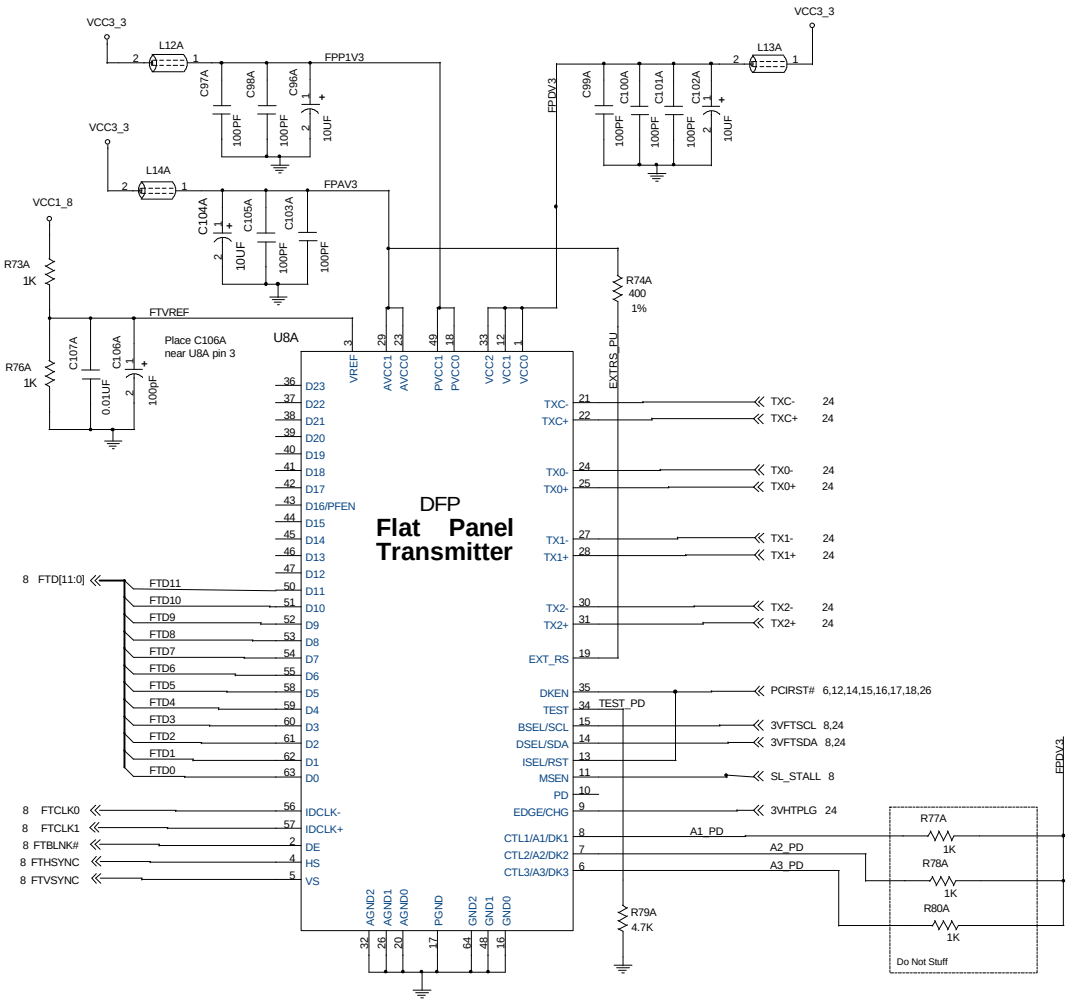
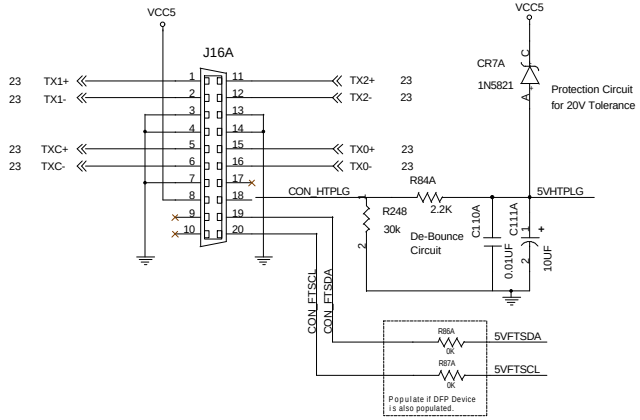
Digital Video Out



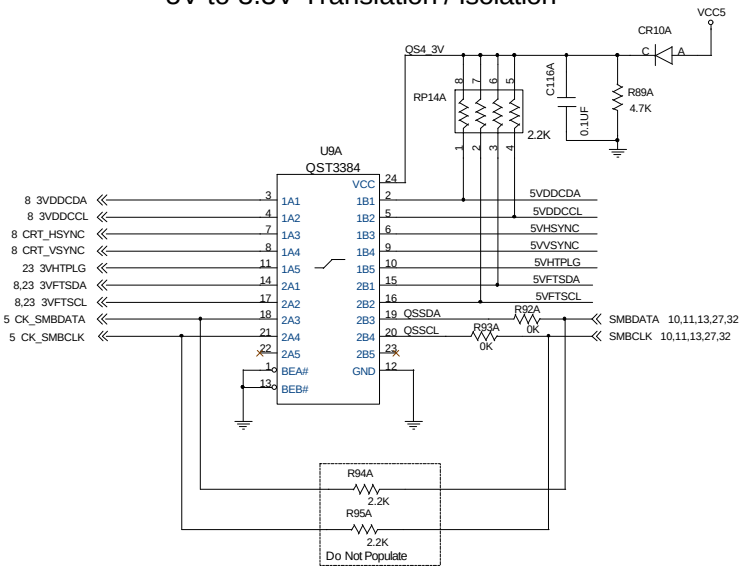
Title: Intel® 810e Chipset Customer Reference Board Digital Video Out		REV. 1.0
intel® Platform Components Division 1900 Prairie City Road Folsom, Ca. 95630	Last Revision Date: 6/14/99 Sheet: 23 of 33	

Video Connectors

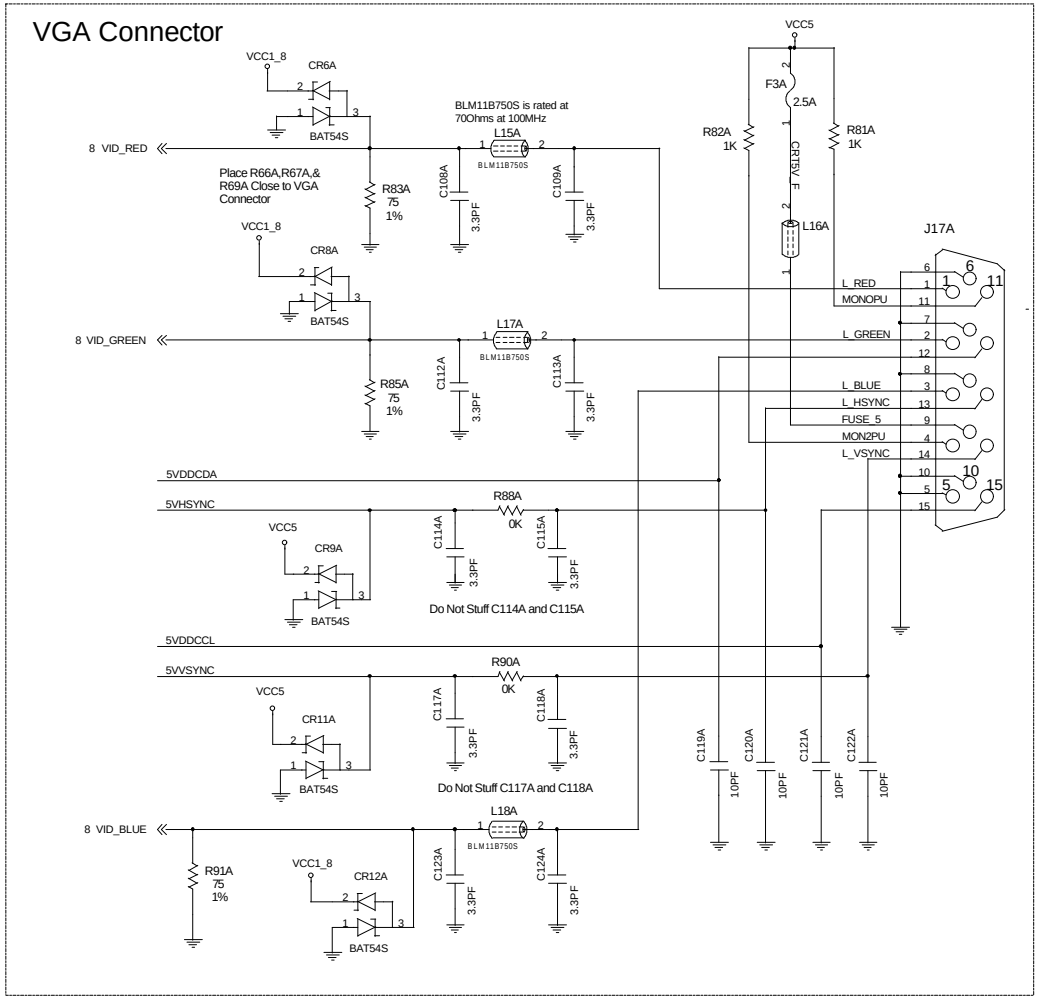
20 Pin Flat Panel Connector



5V to 3.3V Translation / Isolation



VGA Connector



Title: Intel® 810e Chipset Customer Reference Board Video Connectors		REV. 1.0
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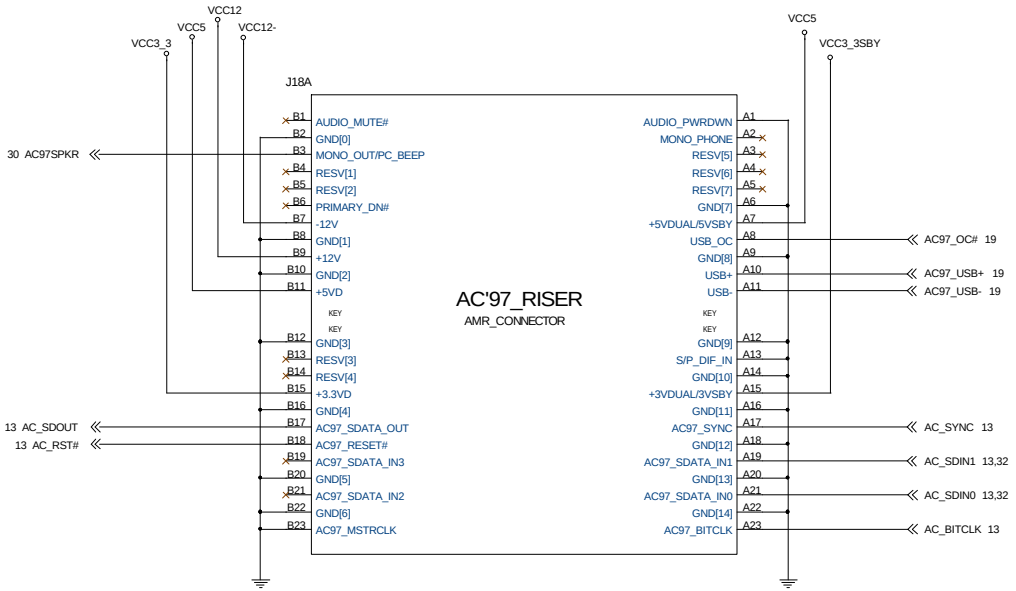
AUDIO/MODEM RISER



Title: Intel® 810e Chipset Customer Reference Board AUDIO/MODEM RISER		REV. 1.0
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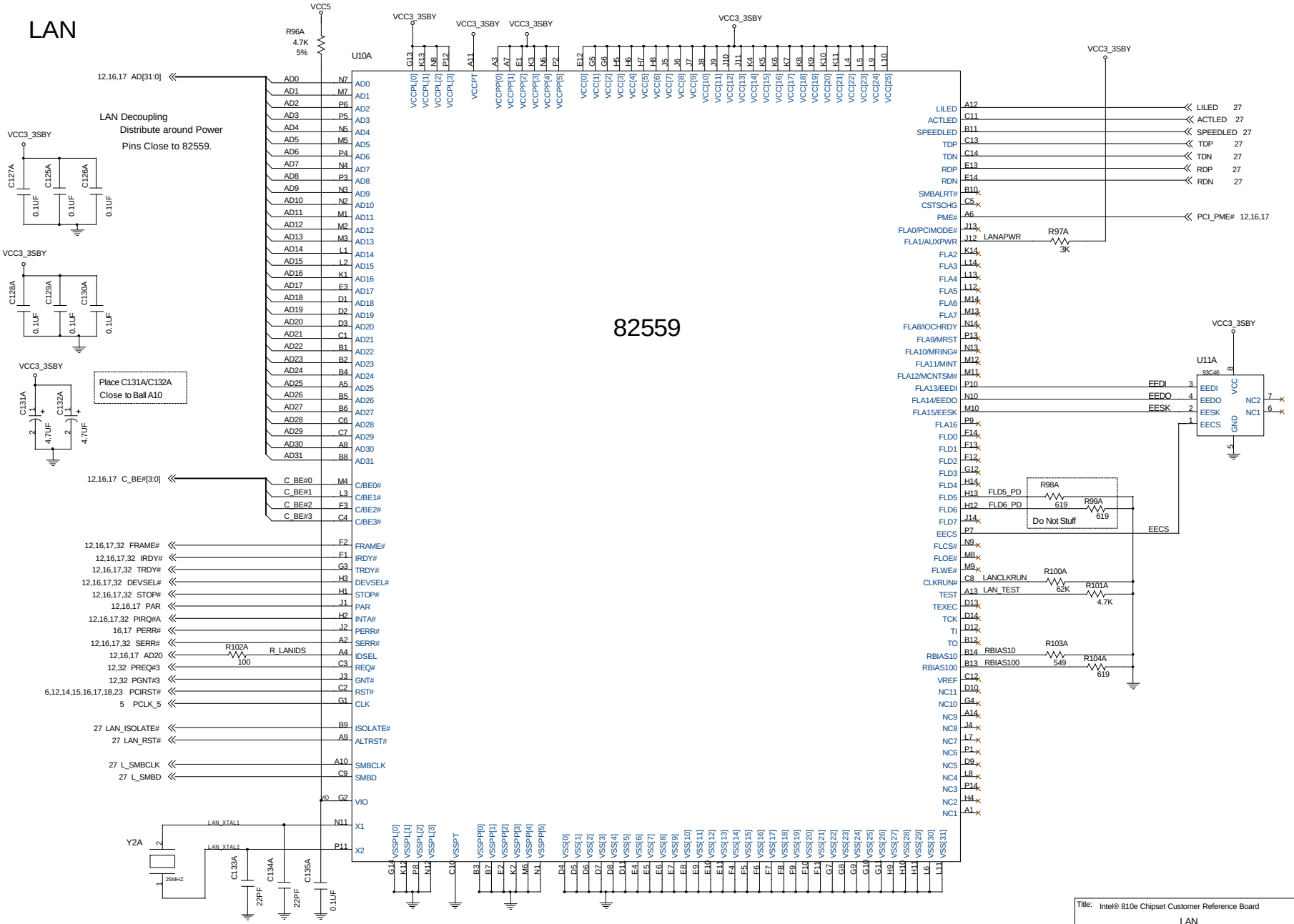
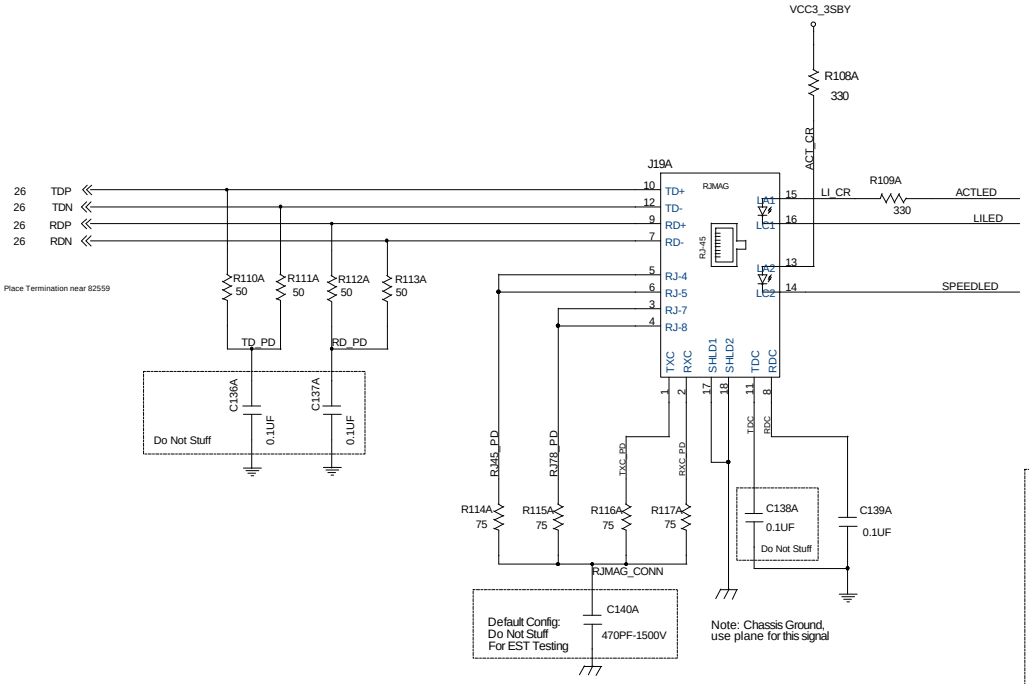
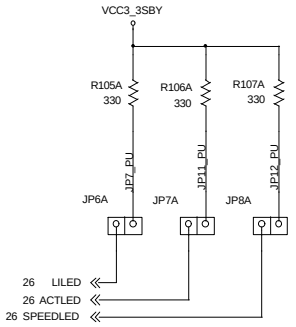
LAN

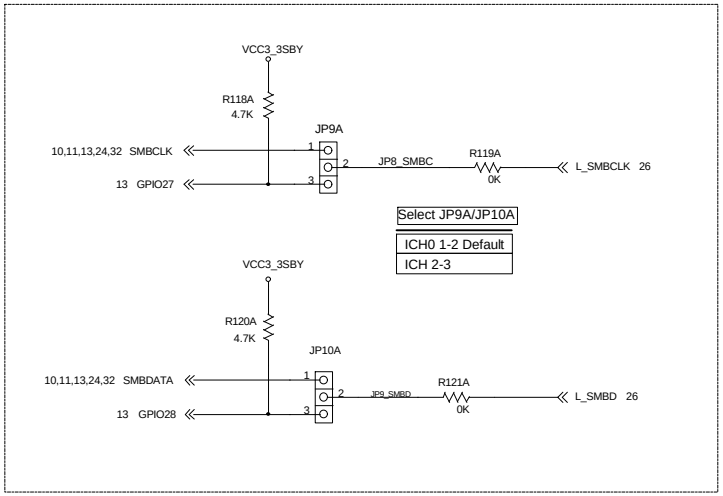


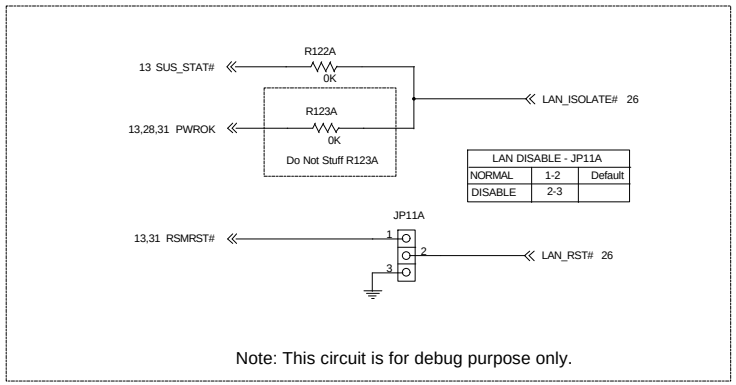
Title: Intel® 810e Chipset Customer Reference Board LAN		REV. 1.0
intel® Platform Components Division 1900 Prairie City Road Folsom, Ca. 95630	Last Revision Date: 6/14/99 Sheet: 26 of 33	

LAN









Title: Intel® 810e Chipset Customer Reference Board LAN		REV. 1.0
intel® Platform Components Division 1900 Prairie City Road Folsom, Ca. 95630	Last Revision Date: 6/14/99	
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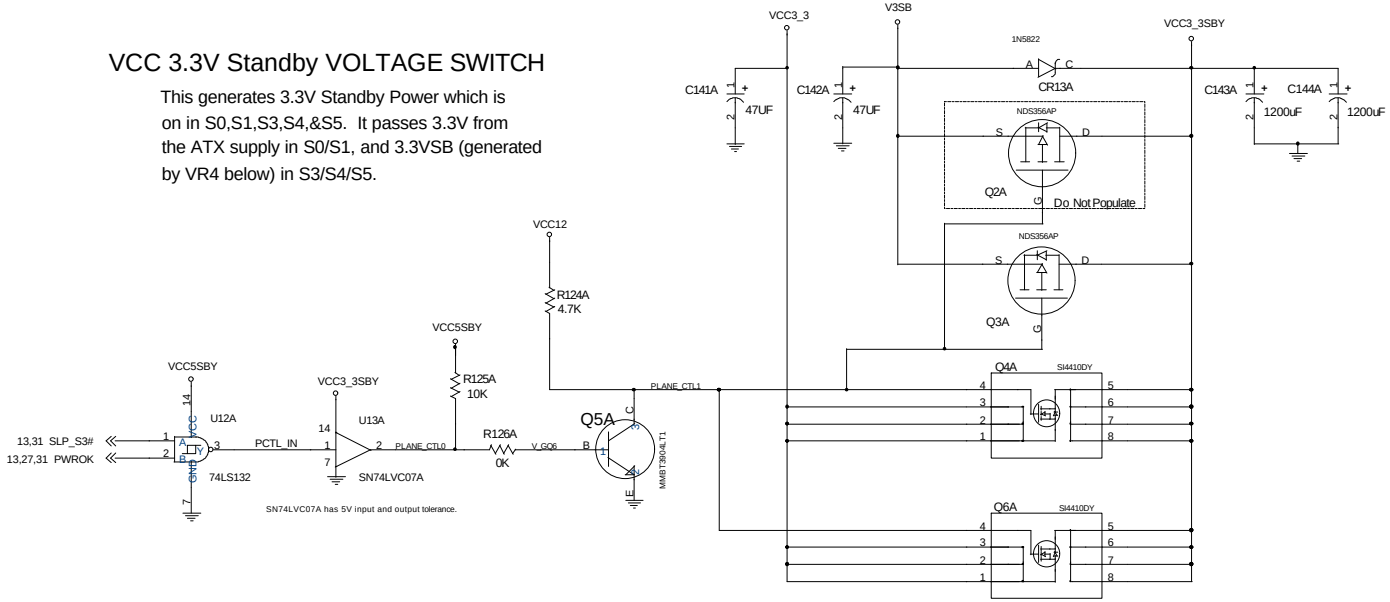
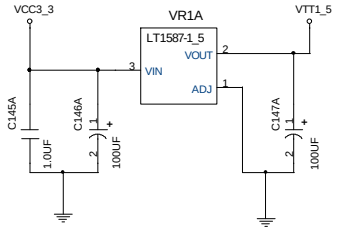
Voltage Regulators

VCC 3.3V Standby VOLTAGE SWITCH

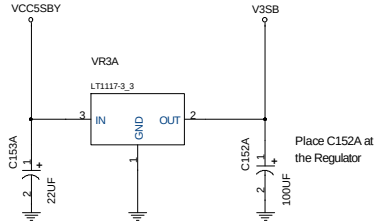
This generates 3.3V Standby Power which is on in S0,S1,S3,S4,&S5. It passes 3.3V from the ATX supply in S0/S1, and 3.3VSB (generated by VR4 below) in S3/S4/S5.



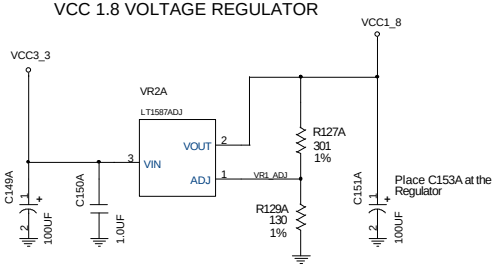
VTT 1.5V VOLTAGE REGULATOR



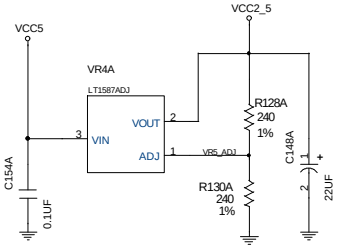
VCC 3.3VSB Regulator



VCC 1.8 VOLTAGE REGULATOR



VCC 2.5 VOLTAGE REGULATOR



Title: Intel® 810e Chipset Customer Reference Board Voltage Regulators		REV. 1.0
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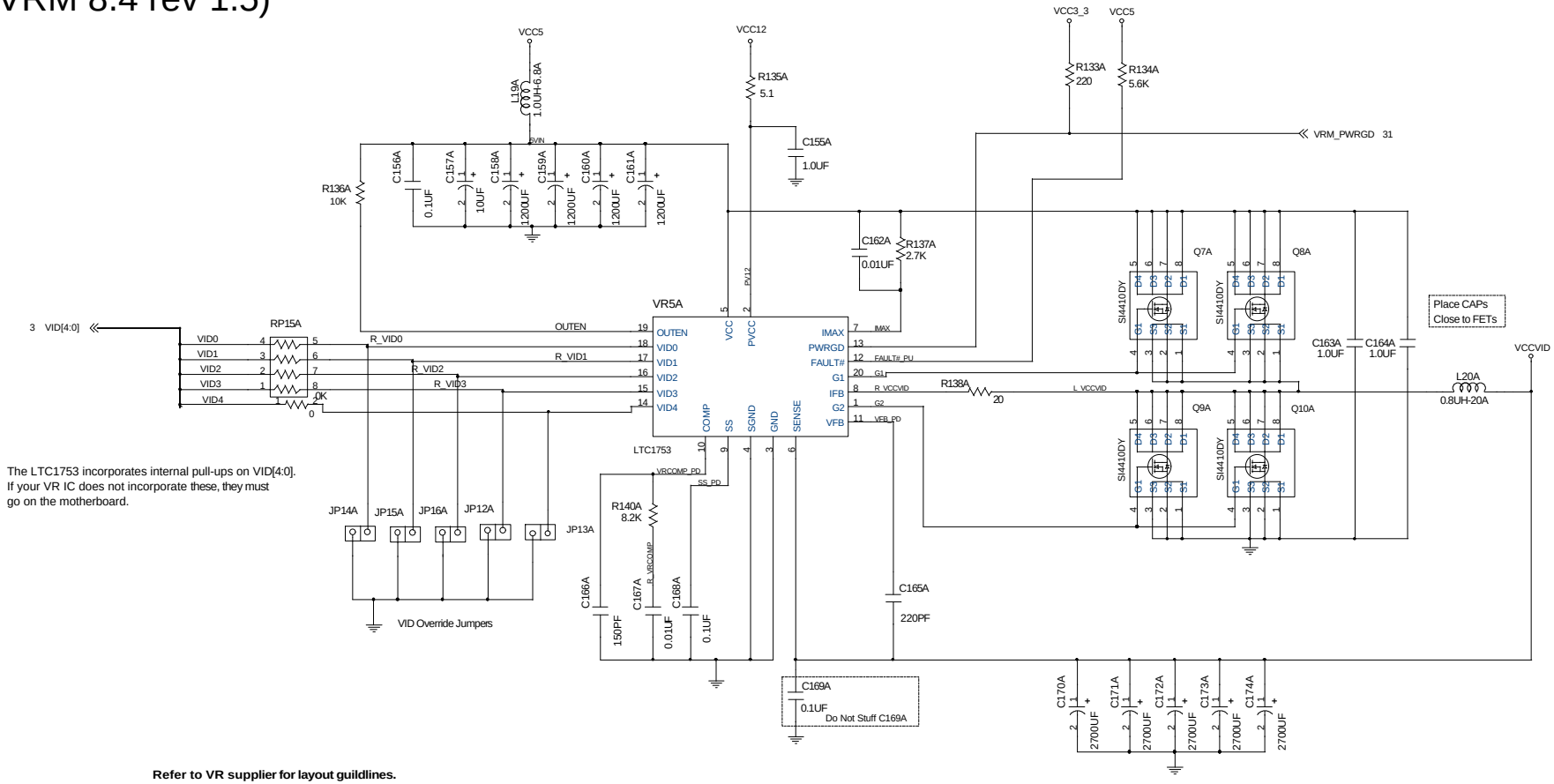
Processor Voltage Regulator (VRM 8.4 rev 1.5)



The LTC1753 incorporates internal pull-ups on VID[4:0]. If your VR IC does not incorporate these, they must go on the motherboard.

Refer to VR supplier for layout guidlines.

Title: Intel® 810e Chipset Customer Reference Board Processor Voltage Regulator (VRM8.4 rev 1.5)		REV. 1.0
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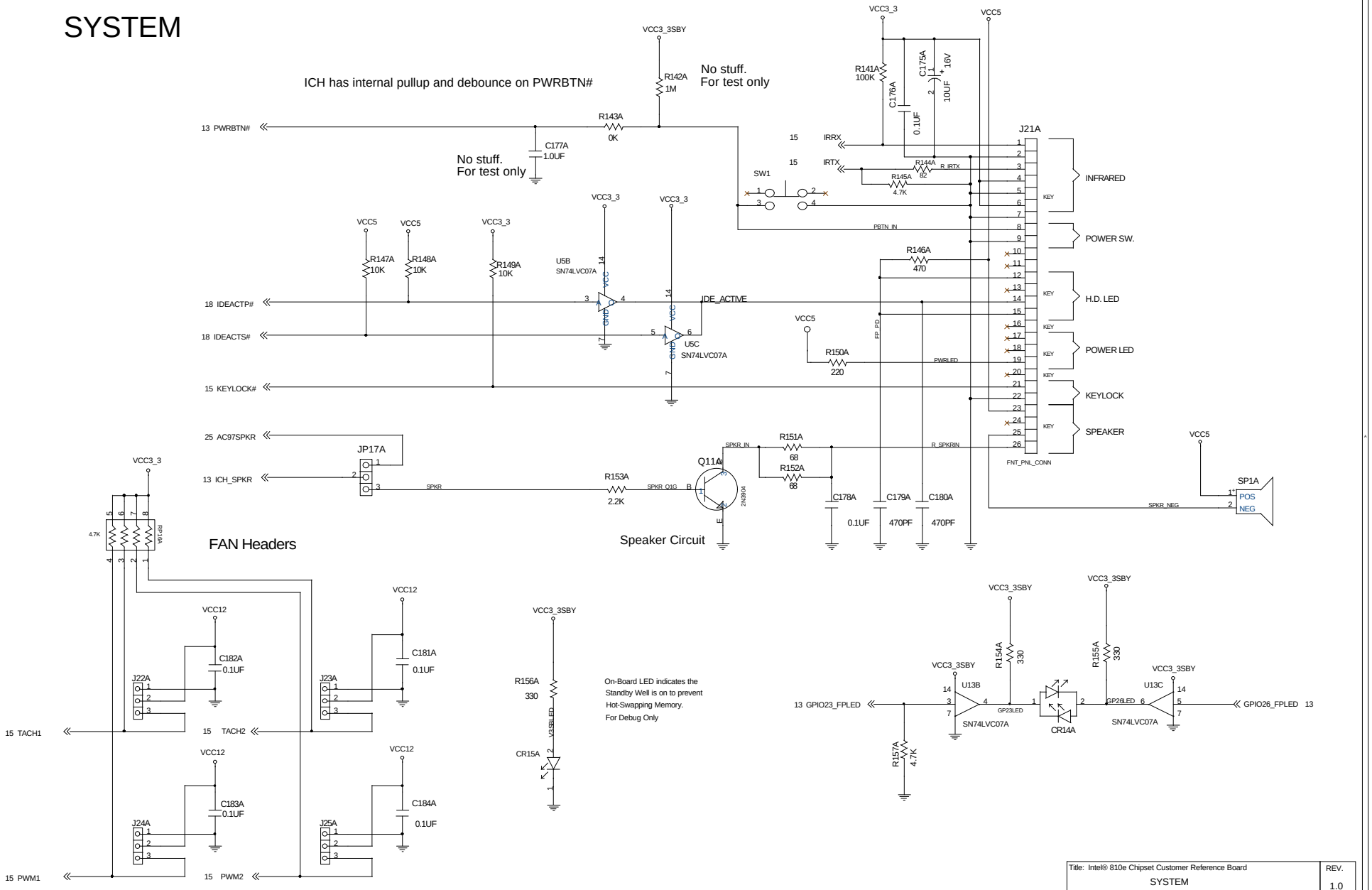
SYSTEM



Title: Intel® 810e Chipset Customer Reference Board SYSTEM		REV. 1.0
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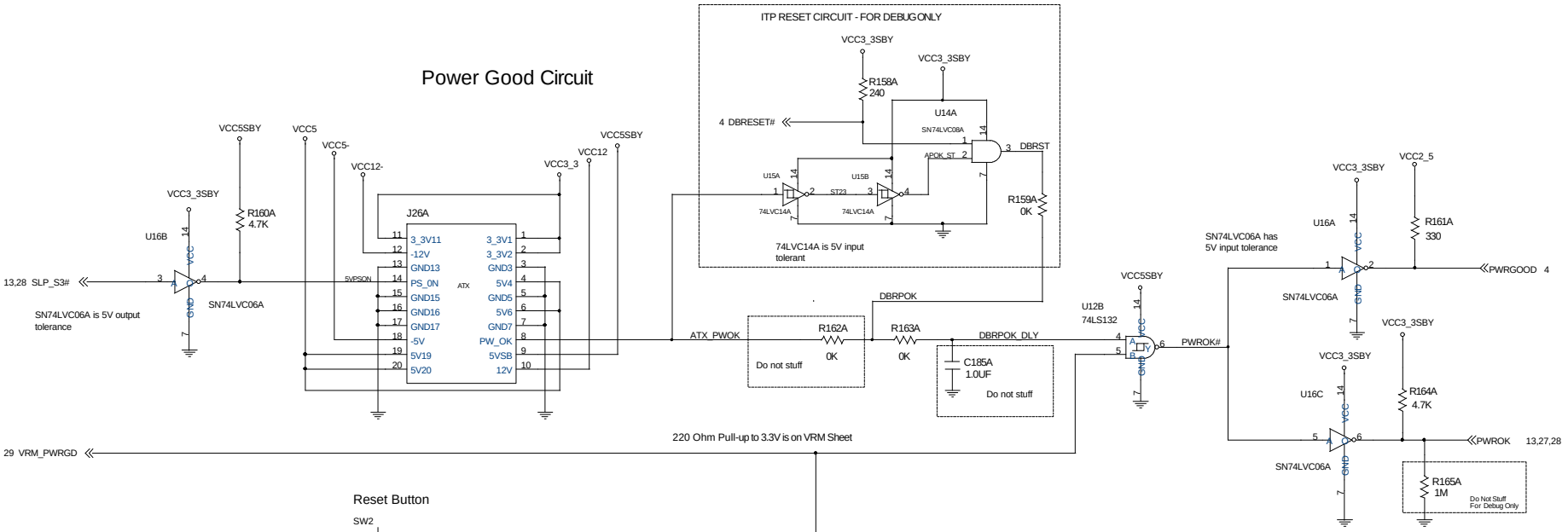
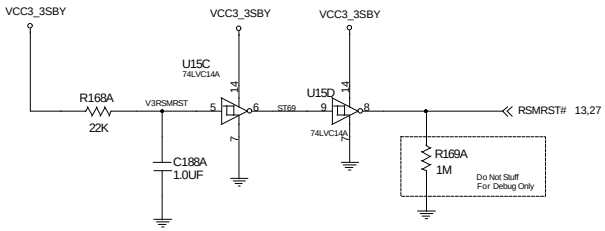
SYSTEM

Power Connector and Reset Control

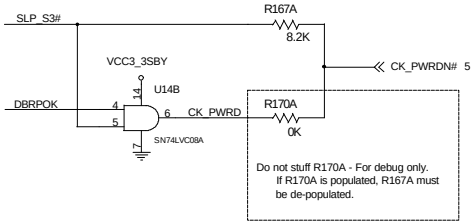


Resume Reset Circuitry

Schmitt Trigger Logic
using a 22msec delay



CLOCK POWERDOWN CONTROL



Title: Intel® 810e Chipset Customer Reference Board System Power Connector and Reset Control		REV. 1.0
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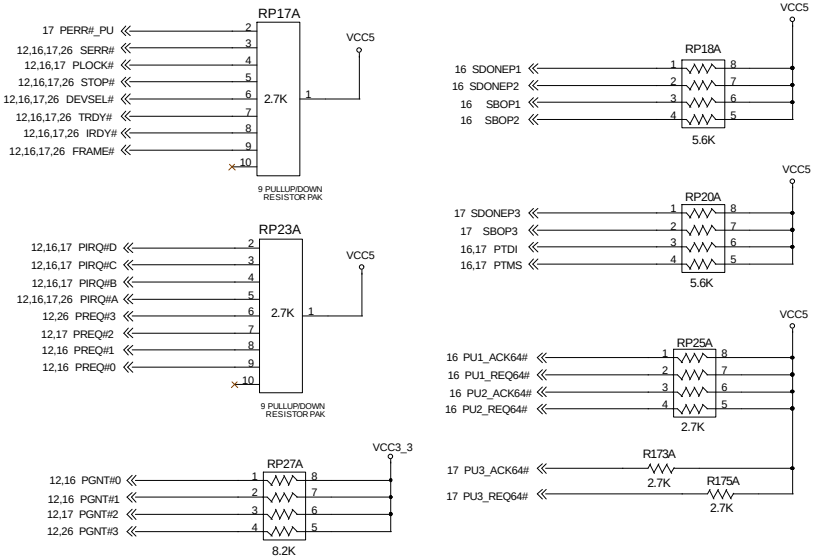
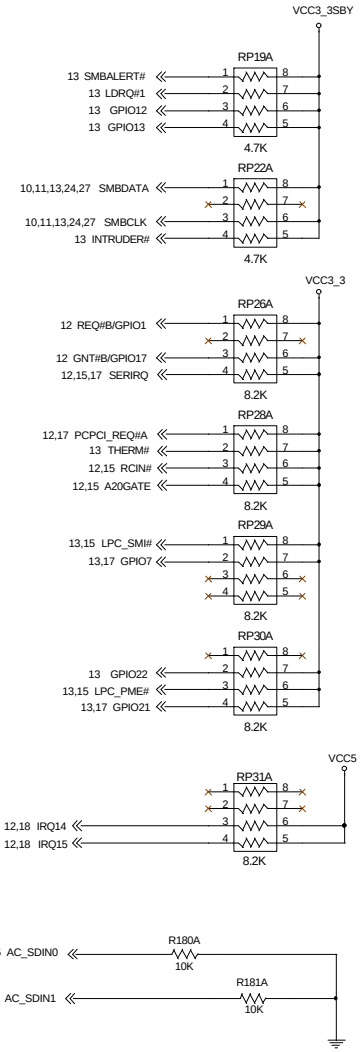
PULL-UP RESISTORS AND UNUSED GATES

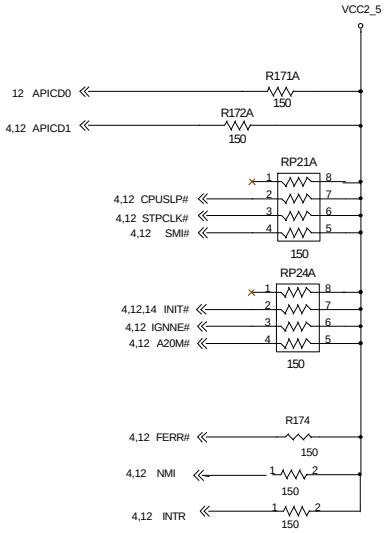
PCI BUS



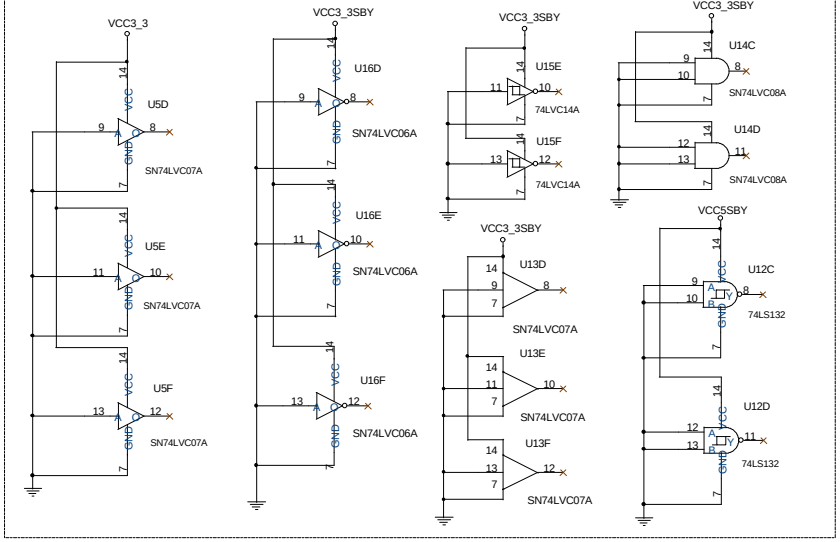
ICH

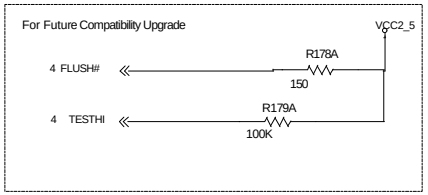


CPU



UNUSED GATES





Title: Intel® 810e Chipset Customer Reference Board PULL-UP RESISTORS AND UNUSED GATES		REV. 1.0
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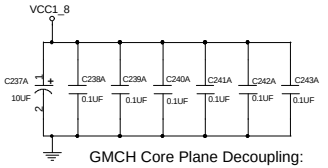
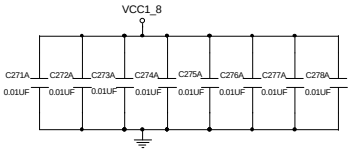
DRAM, CHIPSET, and BULK POWER DECOUPLING

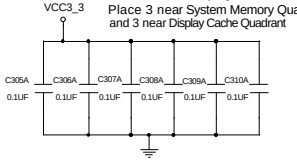
GMCH Decoupling



GMCH Core Plane Decoupling:
Place 1 .1uF/.01uF pair in each corner,
and 2 on opposite sides close to component
if they fit.

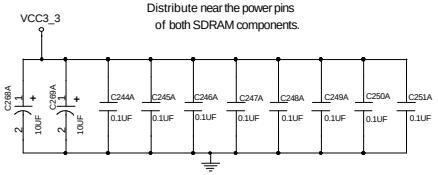


GMCH 3.3V IO Decoupling:
Place 3 near System Memory Quadrant
and 3 near Display Cache Quadrant



Display Cache Decoupling

Distribute near the power pins
of both SDRAM components.

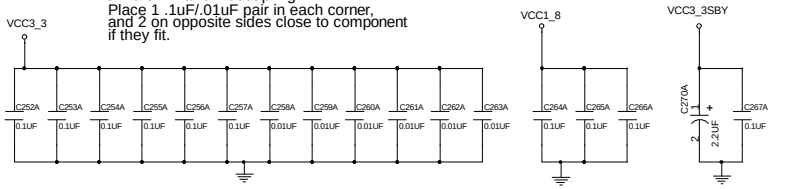


ICH Decoupling

ICH 3.3V Plane Decoupling:
Place 1 .1uF/.01uF pair in each corner,
and 2 on opposite sides close to component
if they fit.

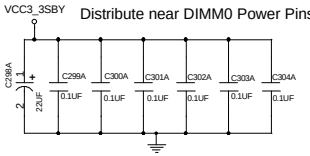
Distribute near the
1.8V power pins of
the ICH.

Distribute near the
VCC3_3SBY power pins of
the ICH.

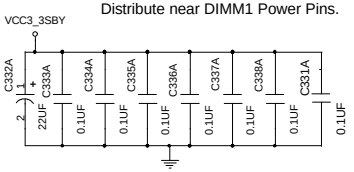


System Memory Decoupling

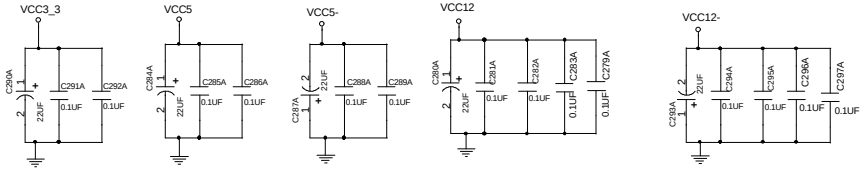
DIMM0 Decoupling:
Distribute near DIMM0 Power Pins.



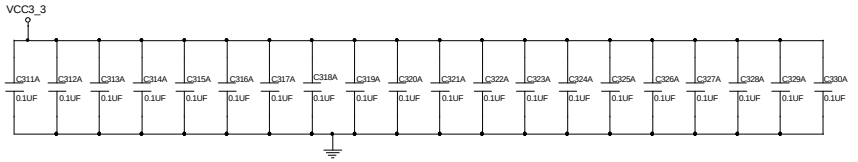
DIMM1 Decoupling:
Distribute near DIMM1 Power Pins.



Bulk Power Decoupling



3 VOLT Decoupling



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