LL6_MV Montevina Block Diagram

01

PCB STACK UP
6L

- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : BOT

POWER

- CPU CORE(ISL6266A) pg36
- VCCP +1.8V AND GMCH 1.05V(RT8204) pg34
- DDR III (TPS51116REGR) 1.5VSUS/SMDDR_VTERM /SMDDR_VREF pg33
- SYSTEM DISCHARGE pg31
- SYSTEM POWER(ISL6237) pg35
- SYSTEM CHARGER(MAX8731A) pg32

CPU
Penryn
478P (uPGA)/35W
pg04~05

CPU THERMAL SENSOR pg05

14.318MHz
CLOCK GEN pg03

CLK_CPU_BCLK, CLK_CPU_BCLK#
CLK_MCH_BCLK, CLK_MCH_BCLK#
DREFCLK, DREFCLK#
DREFSSCLK, DREFSSCLK#

FSB 667/800/1066

NORTH BRIDGE
Cantiga
pg06~10

DDRIII-SODIMM1 pg11 — DDRIII 800/1066 MT/s
DDRIII-SODIMM2 pg12 — DDRIII 800/1066 MT/s

CRT pg18
Dual Link
LCD CONN pg17

DMI LINK

32.768KHz

SOUTH BRIDGE
ICH-9M
pg13~16

- SATA - HDD pg22 — SATA0 300MB
- SATA - CD-ROM pg22 — SATA1 300MB
- E-SATA pg23 — SATA4 300MB

USB2.0
- USB2.0 Ports X4 pg23
- BlueTooth CON. pg26
- Fingerprint CON. pg26
- Camera CON. pg17
- Card Reader RTS5159 pg21

12MHz

PCI-E
- X2 Mini PCI-E Card X 2 (WLAN / WWAN)
  - WLAN (H/S) pg24
  - WWAN (F/S) pg24
- X1 Broadcom 10/100M/1G BCM57780 pg19
  - RJ45 CONN pg19
- X1 Express Card (NEW CARD) pg25

Azalia
Audio Codec IDT 92HD81 pg20

LPC

32.768KHz

EC (ITE) (IT8502E) pg27

Keyboard Touch Pad pg28

- FAN pg29
- SPI EEPROM pg27
- Internal Microphone pg20
- Micphone Jack pg20
- Head-Phone Jack pg20

PROJECT : LL6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Block Diagram	1A

Date: Wednesday, July 15, 2009 Sheet 1 of 36

Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	10V~+19V	18,33,34,35,36,37,38,39	MAIN POWER		S0~S5
+3VRTC	+3.0V~+3.3V	13,16,32	RTC		S0~S5
3VPCU	+3.3V	13,18,22,24,30,32,33,34,36,37	8051 POWER		S0~S5
5VPCU	+5V	30,33,34,35,36,37,38	LCD/CHARGE POWER		S0~S5
+15V	+15V	18,26,33,37	LARGE POWER	5VPCU	S0~S5
LANVCC	+3.3V	22,33	LAN POWER	LAN_ON	
5VSUS	+5V	18,30,33,38	SLP_S5# CTRLD POWER	SUSON	
3VSUS	+3.3V	14,15,27,28,29,32,33,38	SLP_S5# CTRLD POWER	SUSON	
1.8VSUS	+1.8V	10,33,36		SUSON	
1.5VSUS	+1.5V	07,09,10,11,12,33,35	SODIMM POWER CALISTOGA/ICH8 POWER	SUSON	
SMDDR_VREF_DIMM	+0.75V	11,12	SODIMM POWER		
+5V	+5V	16,17,18,19,21,23,24,25,32,33,34	SLP_S3# CTRLD POWER	MAINON	
+3V	+3.3V	03,05,07,10,11,12,13,14,15,16,17,18,19,20,21,22,23,24,25,26,27,28,29,30,31,32,33,34,35,36,37,38	SLP_S3# CTRLD POWER	MAINON	
+1.5V	+1.5V	05,10,13,14,15,16,21,27,28,29,35	CALISTOGA/ICH8 POWER	MAINON	
+1.05V	+1.05V	03,04,05,06,07,09,10,13,16,33,36,38	CPU/CALISTOGA/ICH8 POWER	MAINON	
VCC_CORE	+0.7V~+1.77V	04,05,33,38	CPU CORE POWER	VRON	
LCDVCC	+3.3V	18	LCD Power	INT_DISP_ON	
+5VHDD	+5V	23	HDD Power	MAINON	
MBATV	+10V~+17V	32,34	MAIN BATTERY	D/C#	

PROJECT : LL6

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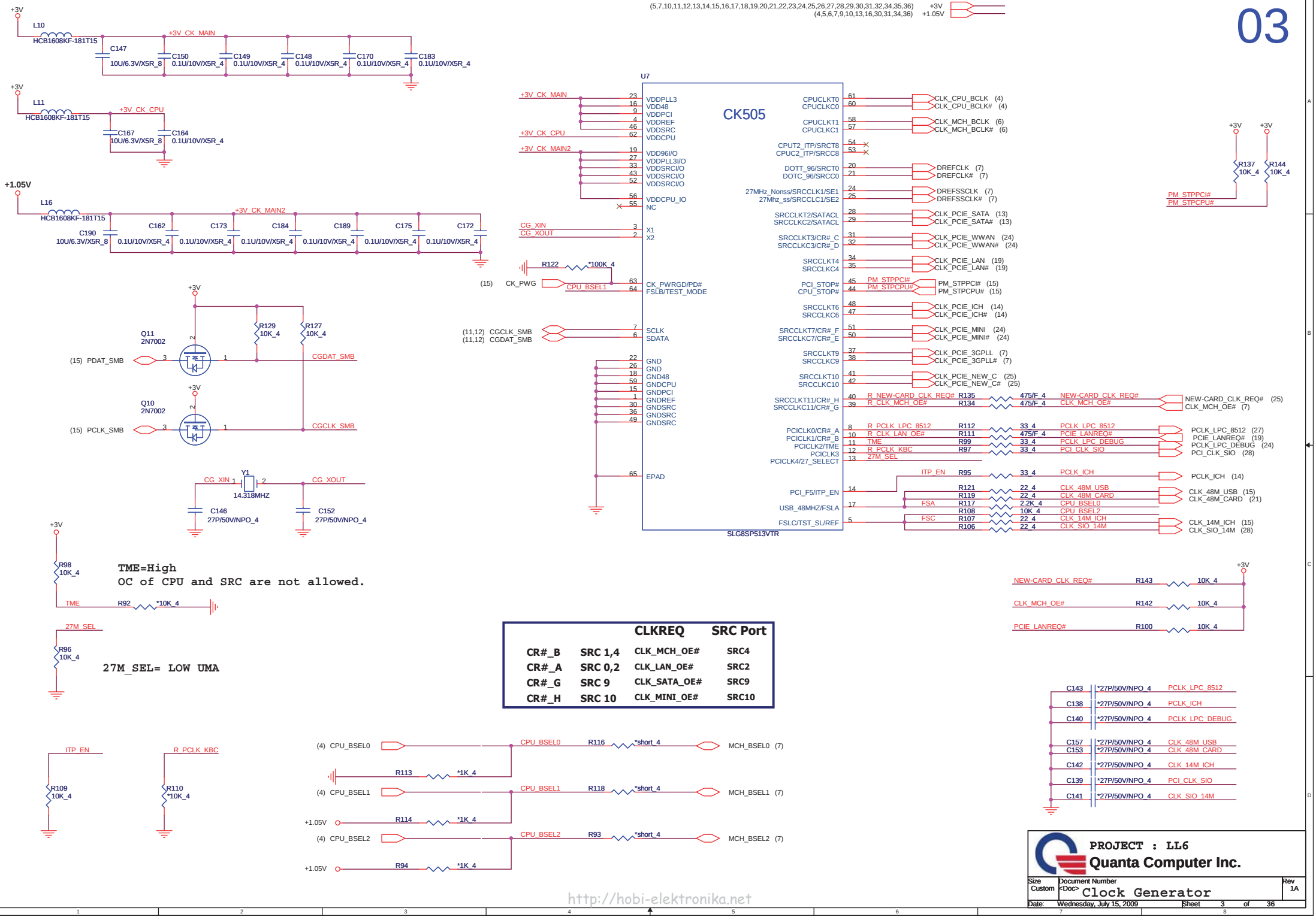
Size	Document Number	Rev
B	FRON TPAGE	1A

Date: Wednesday, July 15, 2009 Sheet 2 of 36



	CLKREQ	SRC Port
CR#_B	SRC 1,4	CLK_MCH_OE# SRC4
CR#_A	SRC 0,2	CLK_LAN_OE# SRC2
CR#_G	SRC 9	CLK_SATA_OE# SRC9
CR#_H	SRC 10	CLK_MINI_OE# SRC10

PROJECT : LL6
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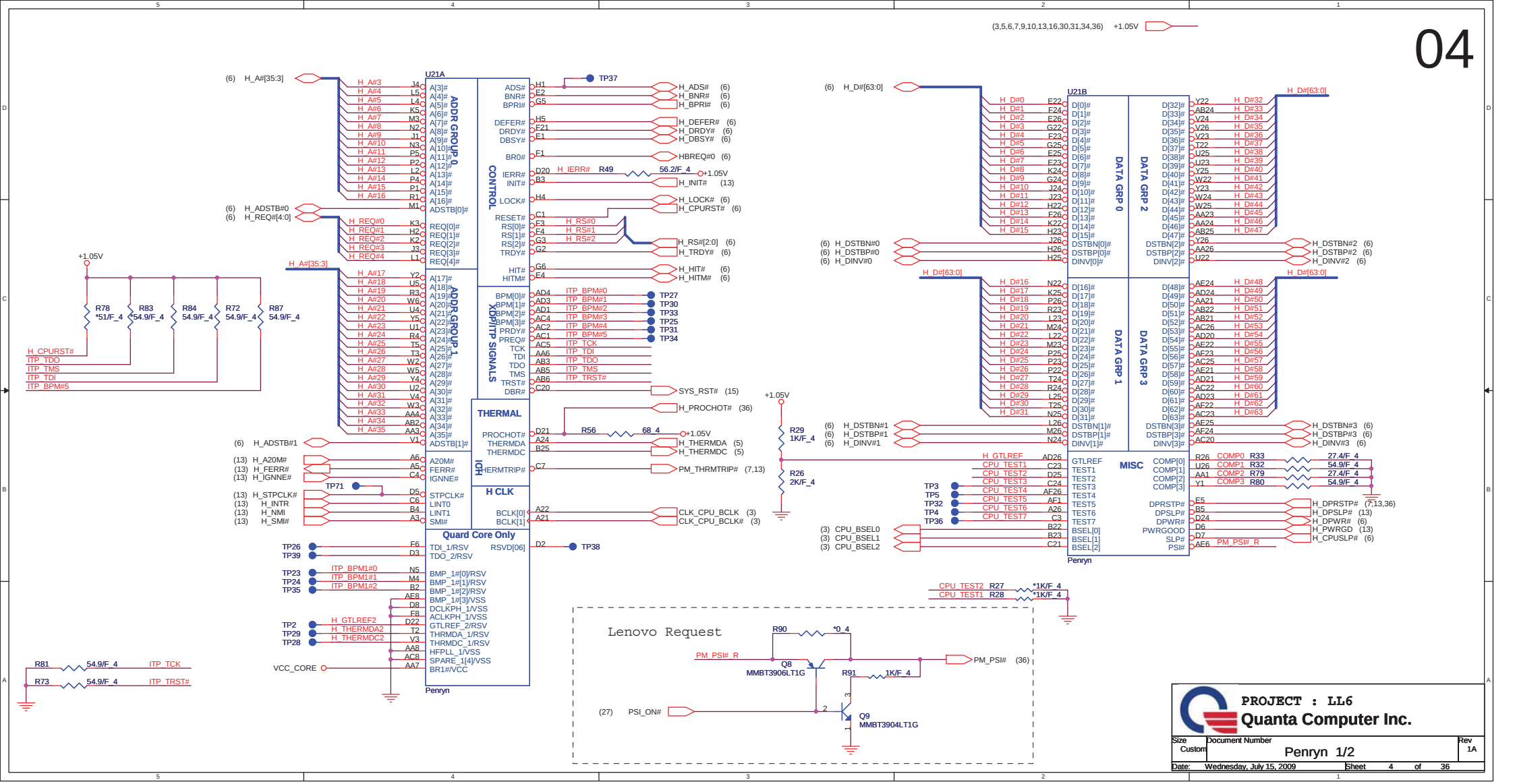
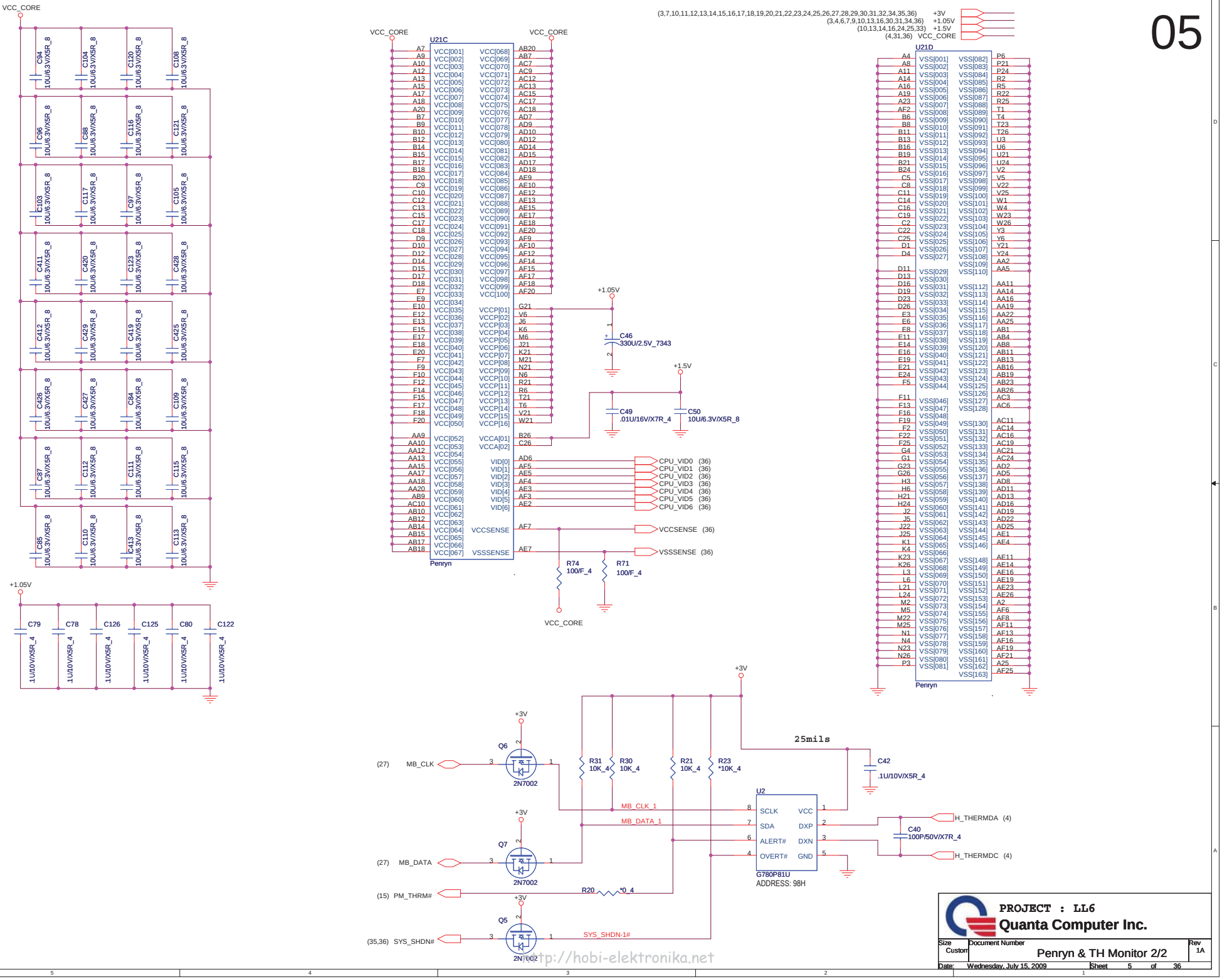
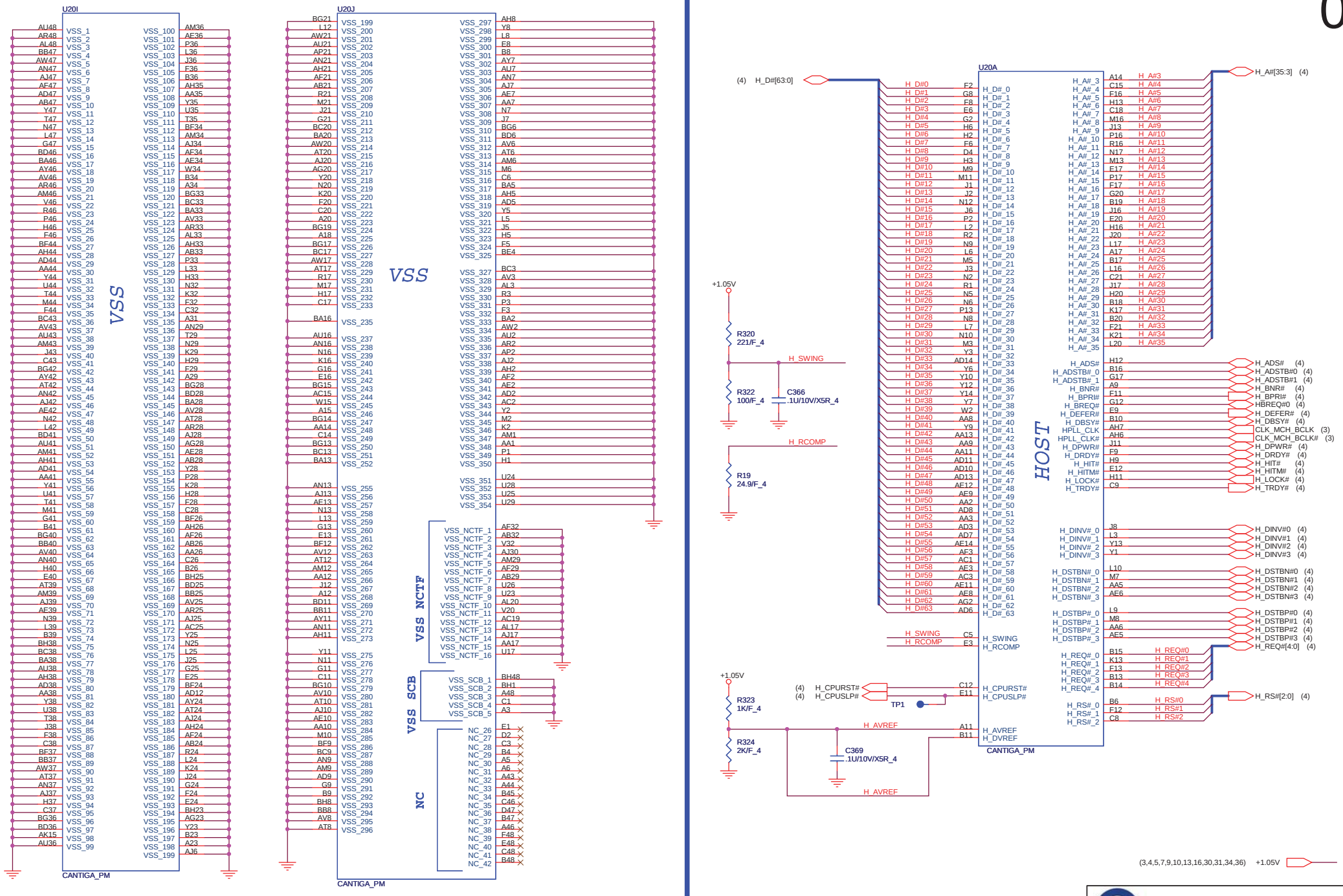
Size	Document Number	Rev
Custom	<Doc> Clock Generator	1A
Date: Wednesday, July 15, 2009	Sheet 3 of 36	


04
U21A
ADDR GROUP_0
ADDR GROUP_1
CONTROL
XDP/ITP SIGNALS
THERMAL
H CLK
Quard Core Only
Penryn
U21B
DATA GRP 0
DATA GRP 2
DATA GRP 1
DATA GRP 3
MISC
Penryn
Lenovo Request
PROJECT : LL6
Quanta Computer Inc.
Penryn 1/2
Size Custom
Document Number
Rev 1A
Date: Wednesday, July 15, 2009
Sheet 4 of 36
http://hobi-elektronika.net





(3,5,10,11,12,13,14,15,16,17,18,19,20,21,22,23,24,25,26,27,28,29,30,31,32,34,35,36) +3V
(9,10,11,12,31,33) 1.5VSUS
(3,4,5,6,9,10,13,16,30,31,34,36) +1.05V

MCH_CFG_5 DMIx2 selection

Low: DMIx2
High: DMIx4 (Default)

MCH_CFG_16 FSB Dynamic ODT

Low: Dynamic ODT disabled
High: Dynamic ODT enabled (Default)

MCH_CFG_9 PCI Express Graphic Lane

Low: Reverse Lane
High: Normal operation(Default)

MCH_CFG_19 DMI Lane Reversal

Low: Normal (Default)
High: Lane Reversed

MCH_CFG_6 iTPM Host Interface

Low: iTPM Host Interface enabled
High: iTPM Host Interface disabled (Default)

MCH_CFG_7 Intel (R) Management Engine Crypto

Low = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality
High = Intel Management Engine Crypto TLS cipher suite with confidentiality (default)

MCH_CFG_10 PCIe Lookback Enable

Low: Enabled
High: Disabled (Default)

MCH_CFG_12/13 XOR/ALLZ/CLOCK Un-gating

MCH_CFG_13	MCH_CFG_12	Configuration
0	0	Reserved
1	0	XOR Mode enabled
0	1	All-Z Mode enabled
1	1	Normal operation (Default)

U20B — CANTIGA_PM

RSVD: RSVD1 M36, RSVD2 N36, RSVD3 R33, RSVD4 T33, RSVD5 AH9, RSVD6 AH10, RSVD7 AH12, RSVD8 AH13, RSVD9 K12, RSVD14 T24, RSVD15 B31, RSVD16 B2, RSVD17 M1, RSVD20 AY21, RSVD22 BG23, RSVD23 BF23, RSVD24 BH18, RSVD25 BF18

ME JTAG: TP16 ME_JTAG_TCK AL34, TP17 ME_JTAG_TDI AK34, TP18 ME_JTAG_TDO AN35, TP20 ME_JTAG_TMS AM35

CFG: (3) MCH_BSEL0 T25, (3) MCH_BSEL1 R25, (3) MCH_BSEL2 P25, CFG_2 P20, CFG_3 P24, CFG_4 C25, CFG_5 N24, CFG_6 M24, CFG_7 E21, CFG_8 C23, CFG_9 C24, CFG_10 N21, CFG_11 P21, CFG_12 T21, CFG_13 R20, CFG_14 M20, CFG_15 L21, CFG_16 H21, CFG_17 P29, CFG_18 R28, CFG_19 T28, CFG_20

MCH_CFG_3 TP6, MCH_CFG_4 TP12 R43 *2.2K_4, MCH_CFG_5 R42 *2.2K_4, MCH_CFG_6 R41 *2.2K_4, MCH_CFG_7 M24, MCH_CFG_8 TP10 R38 *2.2K_4, MCH_CFG_9 R40 *2.2K_4, MCH_CFG_10 C24, MCH_CFG_11 TP9 R37 *2.2K_4, MCH_CFG_12 R36 *2.2K_4, MCH_CFG_13 T21, MCH_CFG_14 TP7, MCH_CFG_15 TP8 R39 *2.2K_4, MCH_CFG_16 L21, MCH_CFG_17 TP11, MCH_CFG_18 TP15 R52 *2.2K_4, MCH_CFG_19 R53 *2.2K_4, MCH_CFG_20 +3V

PM: (15) PM_SYNC# R29, (4,13,36) H_DPRSTP# B7, (11,12) PM_EXTTS#0 N33, PM_EXTTS#1 P32, (15,36) DELAY_VR_PWRGOOD AT40, (14) PLT_RST-R# R22 100/F_4 RST_IN# MCH AT11, (4,13) PM_THRMTRIP# R35 *0_4 T20, (15,36) DPRSLPVR R32

PM_SYNC# B7, PM_DPRSTP# N33, PM_EXT_TS#_0 P32, PM_EXT_TS#_1 AT40, PWROK AT11, RSTIN# T20, THERMTRIP# R32

NC: BG48 NC_1, BF48 NC_2, BD48 NC_3, BC48 NC_4, BH47 NC_5, BG47 NC_6, BE47 NC_7, BH46 NC_8, BF46 NC_9, BG45 NC_10, BH44 NC_11, BH43 NC_12, BH6 NC_13, BH5 NC_14, BG4 NC_15, BH3 NC_16, BF3 NC_17, BH2 NC_18, BG2 NC_19, BE2 NC_20, BG1 NC_21, BF1 NC_22, BD1 NC_23, BC1 NC_24, F1 NC_25, A47 NC_26

R63 10K_4 PM_EXTTS#0, R61 10K_4 PM_EXTTS#1

DDR CLK/CONTROL/COMPENSATION:

SA_CK_0 AP24 M_A_CLK0 (11), SA_CK_1 AT21 M_A_CLK1 (11), SB_CK_0 AY24 M_B_CLK0 (12), SB_CK_1 AU20 M_B_CLK1 (12)
SA_CK#_0 AR24 M_A_CLK0# (11), SA_CK#_1 AR21 M_A_CLK1# (11), SB_CK#_0 AU24 M_B_CLK0# (12), SB_CK#_1 AV20 M_B_CLK1# (12)
SA_CKE_0 BC28 M_A_CKE0 (11), SA_CKE_1 AY28 M_A_CKE1 (11), SB_CKE_0 AY36 M_B_CKE0 (12), SB_CKE_1 BB36 M_B_CKE1 (12)
SA_CS#_0 BA17 M_A_CS#0 (11), SA_CS#_1 AY16 M_A_CS#1 (11), SB_CS#_0 AV16 M_B_CS#0 (12), SB_CS#_1 AR13 M_B_CS#1 (12)
SA_ODT_0 BD17 M_A_ODT0 (11), SA_ODT_1 AY17 M_A_ODT1 (11), SB_ODT_0 BF15 M_B_ODT0 (12), SB_ODT_1 AY13 M_B_ODT1 (12)
SM_RCOMP SM_RCOMP# BG22 SM_RCOMP R330 80.6/F_4, BH21 SM_RCOMP# R329 80.6/F_4
SM_RCOMP_VOH BF28 SM_RCOMP_VOH, SM_RCOMP_VOL BH28 SM_RCOMP_VOL
SM_VREF AV42 SMDDR_VREF, SM_PWROK AR36 SM_PWROK, SM_REXT BF17 SM_REXT, SM_DRAMRST# BC36 DDR3_DRAMRST# (11,12)
1.5VSUS: R69 15K/F_4 DDR3_PWG (33), R67 18.7K/F_4, R34 499/F_4

CLK:
DPLL_REF_CLK B38 DREFCLK (3), DPLL_REF_CLK# A38 DREFCLK# (3), DPLL_REF_SSCLK E41 DREFSSCLK (3), DPLL_REF_SSCLK# F41 DREFSSCLK# (3)
PEG_CLK F43 CLK_PCIE_3GPLL (3), PEG_CLK# E43 CLK_PCIE_3GPLL# (3)

DMI:
DMI_RXN_0 AE41 DMI_TXN0, DMI_RXN_1 AE37 DMI_TXN1, DMI_RXN_2 AE47 DMI_TXN2, DMI_RXN_3 AH39 DMI_TXN3 — DMI_TXN[3:0] (14)
DMI_RXP_0 AE40 DMI_TXP0, DMI_RXP_1 AE38 DMI_TXP1, DMI_RXP_2 AE48 DMI_TXP2, DMI_RXP_3 AH40 DMI_TXP3 — DMI_TXP[3:0] (14)
DMI_TXN_0 AE35 DMI_RXN0, DMI_TXN_1 AE43 DMI_RXN1, DMI_TXN_2 AE46 DMI_RXN2, DMI_TXN_3 AH42 DMI_RXN3 — DMI_RXN[3:0] (14)
DMI_TXP_0 AD35 DMI_RXP0, DMI_TXP_1 AE44 DMI_RXP1, DMI_TXP_2 AF46 DMI_RXP2, DMI_TXP_3 AH43 DMI_RXP3 — DMI_RXP[3:0] (14)

GRAPHICS VID:
GFX_VID_0 B33 GFXVR_VID_0 TP68, GFX_VID_1 B32 GFXVR_VID_1 TP67, GFX_VID_2 G33 GFXVR_VID_2 TP22, GFX_VID_3 E33 GFXVR_VID_3 TP21, GFX_VID_4 E33 GFXVR_VID_4 TP19
GFX_VR_EN C34 GFXVR_EN TP69

ME:
CL_CLK AH37, CL_DATA AH36, CL_PWROK AN36, CL_RST# AJ35, CL_VREF AH34
CL_CLK0 (15), CL_DATA0 (15), ECPWROK (15,27), CL_RST#0 (15)
MCH_CLVREF — 0.35 V
+1.05V: R65 1K/F_4, R66 499/F_4, C92 1U/10V/X5R_4

MISC:
DDPC_CTRLCLK N28 DDPC_CTRLCLK TP14, DDPC_CTRLDATA M28 DDPC_CTRLDATA TP13, SDVO_CTRLCLK G36, SDVO_CTRLDATA E36, CLKREQ# K36, ICH_SYNC# H36 — CLK_MCH_OE# (3), MCH_ICH_SYNC# (15)
TSATN# B12 MCH_TSATN R325 56.2/F_4 +1.05V

HDA:
HDA_BCLK B28, HDA_RST# B30, HDA_SDI B29, HDA_SDO C28, HDA_SYNC A28

U20C — CANTIGA_PM

LVDS:
L_BKLT_CTRL L32, L_BKLT_EN G32, L_CTRL_CLK M32, L_CTRL_DATA M33, L_DDC_CLK K33, L_DDC_DATA J33, L_VDD_EN M29
(17) INT_DPST_PWM, (17) INT_LVDS_BLON — R59 10K/F_4 +3V, R60 10K/F_4
(17) LCD_DDCCLK, (17) LCD_DDCDAT, (17) INT_DISP_ON
LVDS_IBG C44 — R70 2.37K/F_4 LVDS_IBG, LVDS_VBG B43 — TP70
LVDS_VBG B43, LVDS_VREFH E37, LVDS_VREFL E38, LVDSA_CLK# C41, LVDSA_CLK C40, LVDSB_CLK# B37, LVDSB_CLK A37
(17) LA_CLK# — LA_CLK#, (17) LA_CLK — LA_CLK
LVDSA_DATA#_0 H47, LVDSA_DATA#_1 E46, LVDSA_DATA#_2 G40, LVDSA_DATA#_3 A40 — (17) LA_DATAN0 LA_DATAN0, (17) LA_DATAN1 LA_DATAN1, (17) LA_DATAN2 LA_DATAN2
LVDSA_DATA_0 H48, LVDSA_DATA_1 D45, LVDSA_DATA_2 F40, LVDSA_DATA_3 B40 — (17) LA_DATAP0 LA_DATAP0, (17) LA_DATAP1 LA_DATAP1, (17) LA_DATAP2 LA_DATAP2
LVDSB_DATA#_0 A41, LVDSB_DATA#_1 H38, LVDSB_DATA#_2 G37, LVDSB_DATA#_3 J37
LVDSB_DATA_0 B42, LVDSB_DATA_1 G38, LVDSB_DATA_2 F37, LVDSB_DATA_3 K37

TV:
TVA_DAC F25 — R44 75/F_4 TV_COMP1, R45 75/F_4 TV_Y/G1, R46 75/F_4 TV_C/R1
TVB_DAC H25, TVC_DAC K25, TV_RTN H24
TV_DCONSEL_0 C31 — TV_DCONSEL0, TV_DCONSEL_1 E32 — TV_DCONSEL1

VGA:
CRT_BLUE E28 — (18) INT_CRT_BLU — R47 150/F_4
CRT_GREEN G28 — (18) INT_CRT_GRN — R50 150/F_4
CRT_RED J28 — (18) INT_CRT_RED — R48 150/F_4
CRT_IRTN G29
CRT_DDC_CLK H32 — (18) INT_CRT_DDCCLK
CRT_DDC_DATA J32 — (18) INT_CRT_DDCDAT
CRT_HSYNC J29 — R55 33_4 HSYNC_INT — (18) INT_HSYNC
CRT_TVO_IREF F29 — R54 1.02K/F_4 CRTIREF
CRT_VSYNC L29 — R51 33_4 VSYNC_INT — (18) INT_VSYNC

PCI-EXPRESS GRAPHICS:
PEG_COMPI T37, PEG_COMPO T36 — PEG_COMP R64 49.9/F_4 +1.05V
PEG_RX#_0 H44, PEG_RX#_1 J46, PEG_RX#_2 L44, PEG_RX#_3 L40, PEG_RX#_4 N41, PEG_RX#_5 P48, PEG_RX#_6 N44, PEG_RX#_7 T43, PEG_RX#_8 U43, PEG_RX#_9 Y43, PEG_RX#_10 Y48, PEG_RX#_11 Y36, PEG_RX#_12 AA43, PEG_RX#_13 AD37, PEG_RX#_14 AC47, PEG_RX#_15 AD39
PEG_RX_0 H43, PEG_RX_1 J44, PEG_RX_2 L43, PEG_RX_3 L41, PEG_RX_4 N40, PEG_RX_5 P47, PEG_RX_6 N43, PEG_RX_7 T42, PEG_RX_8 U42, PEG_RX_9 Y42, PEG_RX_10 W41, PEG_RX_11 Y37, PEG_RX_12 AA42, PEG_RX_13 AD38, PEG_RX_14 AC46, PEG_RX_15 AD46
PEG_TX#_0 J41, PEG_TX#_1 M46, PEG_TX#_2 M47, PEG_TX#_3 M40, PEG_TX#_4 M42, PEG_TX#_5 R48, PEG_TX#_6 N38, PEG_TX#_7 T40, PEG_TX#_8 U37, PEG_TX#_9 U40, PEG_TX#_10 Y40, PEG_TX#_11 AA46, PEG_TX#_12 AA37, PEG_TX#_13 AA40, PEG_TX#_14 AD43, PEG_TX#_15 AC45
PEG_TX_0 J42, PEG_TX_1 L46, PEG_TX_2 M48, PEG_TX_3 M39, PEG_TX_4 M43, PEG_TX_5 R47, PEG_TX_6 N37, PEG_TX_7 T39, PEG_TX_8 U36, PEG_TX_9 U38, PEG_TX_10 Y39, PEG_TX_11 Y46, PEG_TX_12 AA36, PEG_TX_13 AA39, PEG_TX_14 AD42, PEG_TX_15 AD45

1.5VSUS: R333 1K/F_4
SM_RCOMP_VOH — C403 .01U/16V/X7R_4, C400 2.2U/6.3V/X5R_6 — R332 3.01K/F_4
SM_RCOMP_VOL — C395 .01U/16V/X7R_4, C394 2.2U/6.3V/X5R_6 — R331 1K/F_4

1.5VSUS: R339 *1K/F_4
SMDDR_VREF — C435 .1U/10V/X5R_4, C436 470P/50V/X7R_4 — R338 *1K/F_4 — SMDDR_VREF (11,33)

PROJECT : LL6
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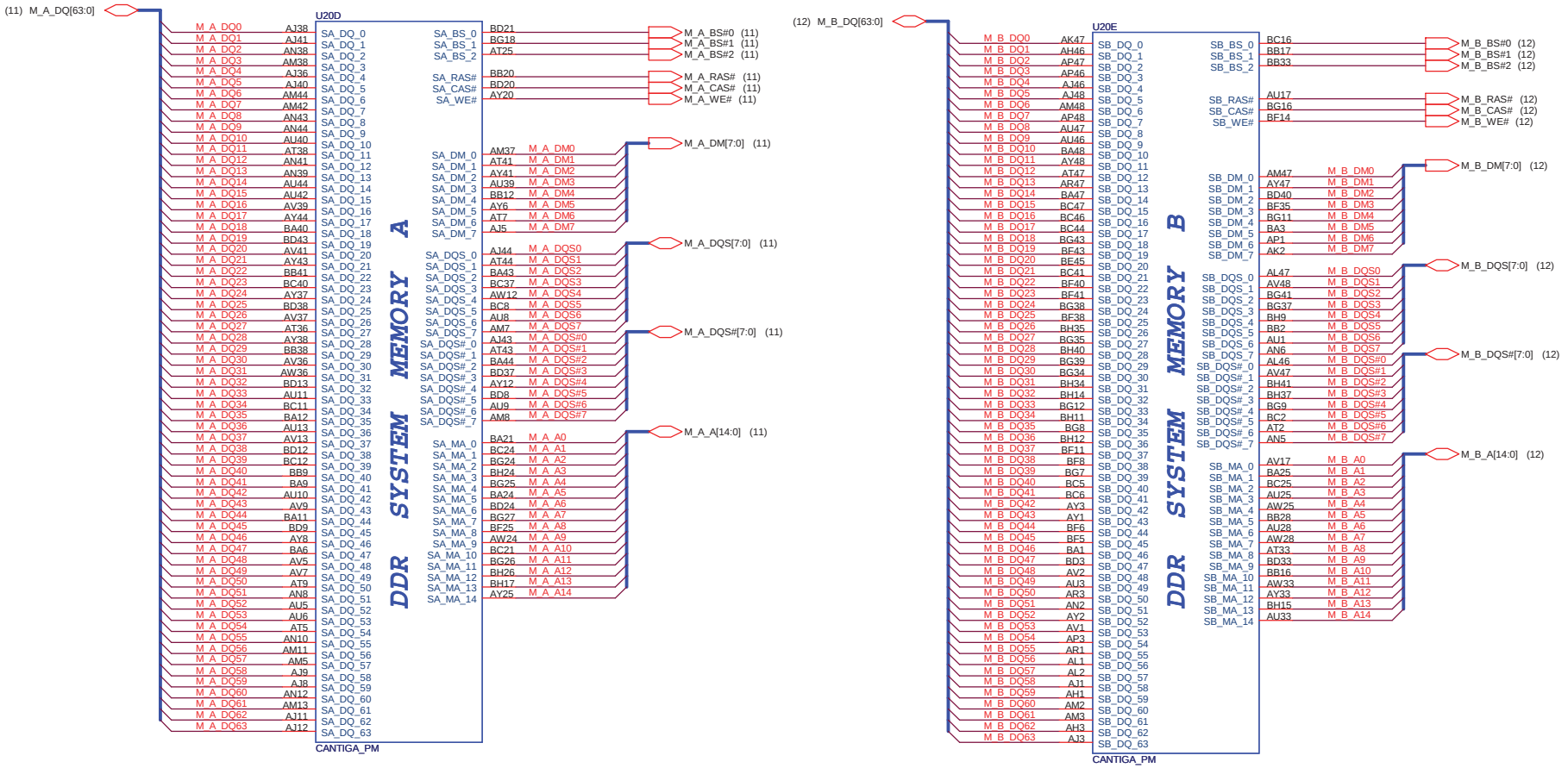
Size: Custom | Document Number: Cantiga DMI/DISP 2/5 | Rev: 1A
Date: Wednesday, July 15, 2009 | Sheet 7 of 36



PROJECT : LL6
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Size	Document Number	Rev
Custom	Cantiga DDR3 3/5	1A
Date: Wednesday, July 15, 2009	Sheet 8 of 36	

(7,10,11,12,31,33) 1.5VSUS
(3,4,5,6,7,10,13,16,30,31,34,36) +1.05V

1.5VSUS

U20G

1067M--4140mA
800M--3162.5mA

VCC_SM_1 AP33
VCC_SM_2 AN33
VCC_SM_3 BH32
VCC_SM_4 BG32
VCC_SM_5 BF32
VCC_SM_6 BD32
VCC_SM_7 BC32
VCC_SM_8 BB32
VCC_SM_9 BA32
VCC_SM_10 AY32
VCC_SM_11 AW32
VCC_SM_12 AV32
VCC_SM_13 AU32
VCC_SM_14 AT32
VCC_SM_15 AR32
VCC_SM_16 AP32
VCC_SM_17 AN32
VCC_SM_18 BH31
VCC_SM_19 BG31
VCC_SM_20 BF31
VCC_SM_21 BG30
VCC_SM_22 BH29
VCC_SM_23 BG29
VCC_SM_24 BF29
VCC_SM_25 BD29
VCC_SM_26 BC29
VCC_SM_27 BB29
VCC_SM_28 BA29
VCC_SM_29 AY29
VCC_SM_30 AW29
VCC_SM_31 AV29
VCC_SM_32 AU29
VCC_SM_33 AT29
VCC_SM_34 AR29
VCC_SM_35 AP29

VCC_SM_36/NC BA36
VCC_SM_37/NC BB24
VCC_SM_38/NC BD16
VCC_SM_39/NC BB21
VCC_SM_40/NC AW16
VCC_SM_41/NC AW13
VCC_SM_42/NC AT13

C91 *.1U/10V/X5R_4
C67 *.1U/10V/X5R_4
C53 *.1U/10V/X5R_4
C60 *.1U/10V/X5R_4
C52 *.1U/10V/X5R_4
C48 *.1U/10V/X5R_4
C43 *.1U/10V/X5R_4

VCC SM POWER

+1.05V

VCC_AXG_1 Y26
VCC_AXG_2 AE25
VCC_AXG_3 AB25
VCC_AXG_4 AA25
VCC_AXG_5 AE24
VCC_AXG_6 AC24
VCC_AXG_7 AA24
VCC_AXG_8 Y24
VCC_AXG_9 AE23
VCC_AXG_10 AC23
VCC_AXG_11 AB23
VCC_AXG_12 AA23
VCC_AXG_13 AJ21
VCC_AXG_14 AG21
VCC_AXG_15 AE21
VCC_AXG_16 AC21
VCC_AXG_17 AA21
VCC_AXG_18 Y21
VCC_AXG_19 AH20
VCC_AXG_20 AF20
VCC_AXG_21 AE20
VCC_AXG_22 AC20
VCC_AXG_23 AB20
VCC_AXG_24 AA20
VCC_AXG_25 T17
VCC_AXG_26 T16
VCC_AXG_27 AM15
VCC_AXG_28 AL15
VCC_AXG_29 AE15
VCC_AXG_30 AJ15
VCC_AXG_31 AH15
VCC_AXG_32 AG15
VCC_AXG_33 AF15
VCC_AXG_34 AB15
VCC_AXG_35 AA15
VCC_AXG_36 Y15
VCC_AXG_37 V15
VCC_AXG_38 U15
VCC_AXG_39 AN14
VCC_AXG_40 AM14
VCC_AXG_41 U14
VCC_AXG_42 T14

8700mA

VCC GFX

+1.05V

R24 10_4
R25 10_4

VCC_AXG_SENSE AJ14
VSS_AXG_SENSE AH14

VCC_AXG_SENSE
VSS_AXG_SENSE

VCC_SM_LF1 AV44 +VCCSM_LF1
VCC_SM_LF2 BA37 +VCCSM_LF2
VCC_SM_LF3 AM40 +VCCSM_LF3
VCC_SM_LF4 AV21 +VCCSM_LF4
VCC_SM_LF5 AY5 +VCCSM_LF5
VCC_SM_LF6 AM10 +VCCSM_LF6
VCC_SM_LF7 BB13 +VCCSM_LF7

VCC SM LF

.1U/10V/X5R_4 C47
.1U/10V/X5R_4 C41
.33U/6.3V/X5R_4 C38
.33U/6.3V/X5R_4 C62
.47U/6.3V/X5R_4 C106
1U/6.3V/X5R_4 C95
1U/6.3V/X5R_4 C100

VCC_AXG_NCTF_1 W28
VCC_AXG_NCTF_2 V28
VCC_AXG_NCTF_3 W26
VCC_AXG_NCTF_4 V26
VCC_AXG_NCTF_5 W25
VCC_AXG_NCTF_6 V25
VCC_AXG_NCTF_7 W24
VCC_AXG_NCTF_8 V24
VCC_AXG_NCTF_9 W23
VCC_AXG_NCTF_10 V23
VCC_AXG_NCTF_11 AM21
VCC_AXG_NCTF_12 AL21
VCC_AXG_NCTF_13 AK21
VCC_AXG_NCTF_14 W21
VCC_AXG_NCTF_15 V21
VCC_AXG_NCTF_16 U21
VCC_AXG_NCTF_17 AM20
VCC_AXG_NCTF_18 AK20
VCC_AXG_NCTF_19 W20
VCC_AXG_NCTF_20 U20
VCC_AXG_NCTF_21 AM19
VCC_AXG_NCTF_22 AL19
VCC_AXG_NCTF_23 AK19
VCC_AXG_NCTF_24 AJ19
VCC_AXG_NCTF_25 AH19
VCC_AXG_NCTF_26 AG19
VCC_AXG_NCTF_27 AF19
VCC_AXG_NCTF_28 AE19
VCC_AXG_NCTF_29 AB19
VCC_AXG_NCTF_30 AA19
VCC_AXG_NCTF_31 Y19
VCC_AXG_NCTF_32 W19
VCC_AXG_NCTF_33 V19
VCC_AXG_NCTF_34 U19
VCC_AXG_NCTF_35 AM17
VCC_AXG_NCTF_36 AK17
VCC_AXG_NCTF_37 AH17
VCC_AXG_NCTF_38 AG17
VCC_AXG_NCTF_39 AF17
VCC_AXG_NCTF_40 AE17
VCC_AXG_NCTF_41 AC17
VCC_AXG_NCTF_42 AB17
VCC_AXG_NCTF_43 Y17
VCC_AXG_NCTF_44 W17
VCC_AXG_NCTF_45 V17
VCC_AXG_NCTF_46 AM16
VCC_AXG_NCTF_47 AL16
VCC_AXG_NCTF_48 AK16
VCC_AXG_NCTF_49 AJ16
VCC_AXG_NCTF_50 AH16
VCC_AXG_NCTF_51 AG16
VCC_AXG_NCTF_52 AF16
VCC_AXG_NCTF_53 AE16
VCC_AXG_NCTF_54 AC16
VCC_AXG_NCTF_55 AB16
VCC_AXG_NCTF_56 AA16
VCC_AXG_NCTF_57 Y16
VCC_AXG_NCTF_58 W16
VCC_AXG_NCTF_59 V16
VCC_AXG_NCTF_60 U16

VCC GFX NCTF POWER

Ivcc_axg=6326.84mA

CANTIGA_PM

+1.05V

Ivcc=1930.4+508.12=2438.52mA

10U/6.3V/X5R_8 C56
10U/6.3V/X5R_8 C37
33U/6.3V/X5R_4 C99
33U/6.3V/X5R_4 C61
.1U/10V/X5R_4 C68

1.5VSUS

.1U/10V/X5R_4 C408
10U/6.3V/X5R_6 C416
10U/6.3V/X5R_6 C417
10U/6.3V/X5R_6 C418
10U/6.3V/X5R_6 C415

+1.05V

390U/2.5V_6X5.8ESR10 C361
.47U/6.3V/X5R_4 C74
1U/6.3V/X5R_4 C73
10U/6.3V/X5R_8 C86
10U/6.3V/X5R_8 C69
10U/6.3V/X5R_8 C63
.1U/10V/X5R_4 C64
1U/10V/X5R_4 C72

U20F

AG34 VCC_1
AC34 VCC_2
AB34 VCC_3
AA34 VCC_4
Y34 VCC_5
V34 VCC_6
U34 VCC_7
AM33 VCC_8
AK33 VCC_9
AJ33 VCC_10
AG33 VCC_11
AF33 VCC_12

AE33 VCC_13
AC33 VCC_14
AA33 VCC_15
Y33 VCC_16
W33 VCC_17
V33 VCC_18
U33 VCC_19
AH28 VCC_20
AF28 VCC_21
AC28 VCC_22
AA28 VCC_23
AJ26 VCC_24
AG26 VCC_25
AE26 VCC_26
AC26 VCC_27
AH25 VCC_28
AG25 VCC_29
AF25 VCC_30
AG24 VCC_31
AJ23 VCC_32
AH23 VCC_33
AF23 VCC_34

T32 VCC_35

VCC CORE POWER

+1.05V

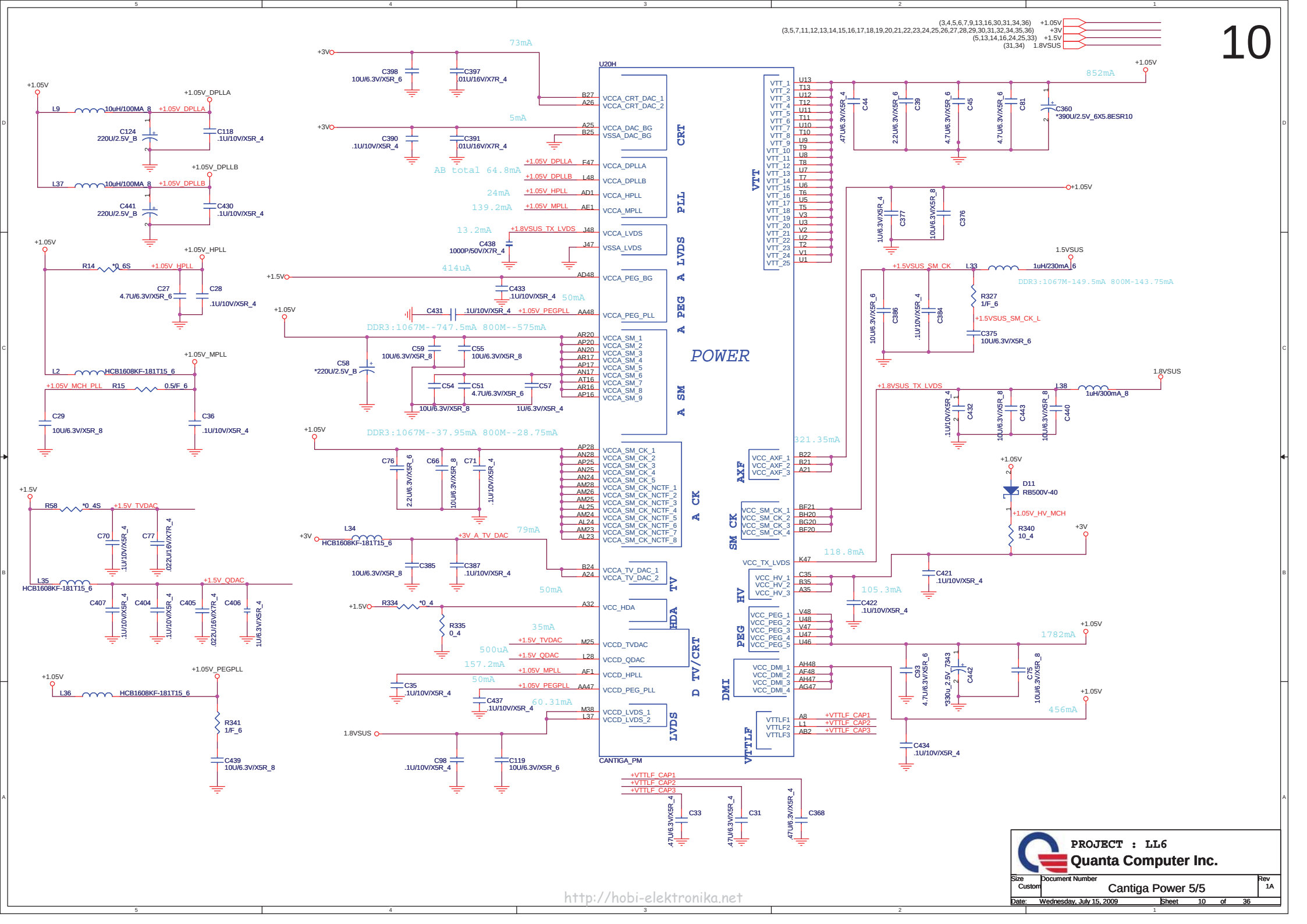
VCC_NCTF_1 AM32
VCC_NCTF_2 AL32
VCC_NCTF_3 AK32
VCC_NCTF_4 AJ32
VCC_NCTF_5 AH32
VCC_NCTF_6 AG32
VCC_NCTF_7 AE32
VCC_NCTF_8 AC32
VCC_NCTF_9 AA32
VCC_NCTF_10 Y32
VCC_NCTF_11 W32
VCC_NCTF_12 U32
VCC_NCTF_13 AM30
VCC_NCTF_14 AL30
VCC_NCTF_15 AK30
VCC_NCTF_16 AH30
VCC_NCTF_17 AG30
VCC_NCTF_18 AF30
VCC_NCTF_19 AE30
VCC_NCTF_20 AC30
VCC_NCTF_21 AB30
VCC_NCTF_22 AA30
VCC_NCTF_23 Y30
VCC_NCTF_24 W30
VCC_NCTF_25 V30
VCC_NCTF_26 U30
VCC_NCTF_27 AL29
VCC_NCTF_28 AK29
VCC_NCTF_29 AJ29
VCC_NCTF_30 AH29
VCC_NCTF_31 AG29
VCC_NCTF_32 AF29
VCC_NCTF_33 AC29
VCC_NCTF_34 AA29
VCC_NCTF_35 Y29
VCC_NCTF_36 W29
VCC_NCTF_37 V29
VCC_NCTF_38 AL28
VCC_NCTF_39 AK28
VCC_NCTF_40 AL26
VCC_NCTF_41 AK26
VCC_NCTF_42 AK25
VCC_NCTF_43 AK24
VCC_NCTF_44 AK23

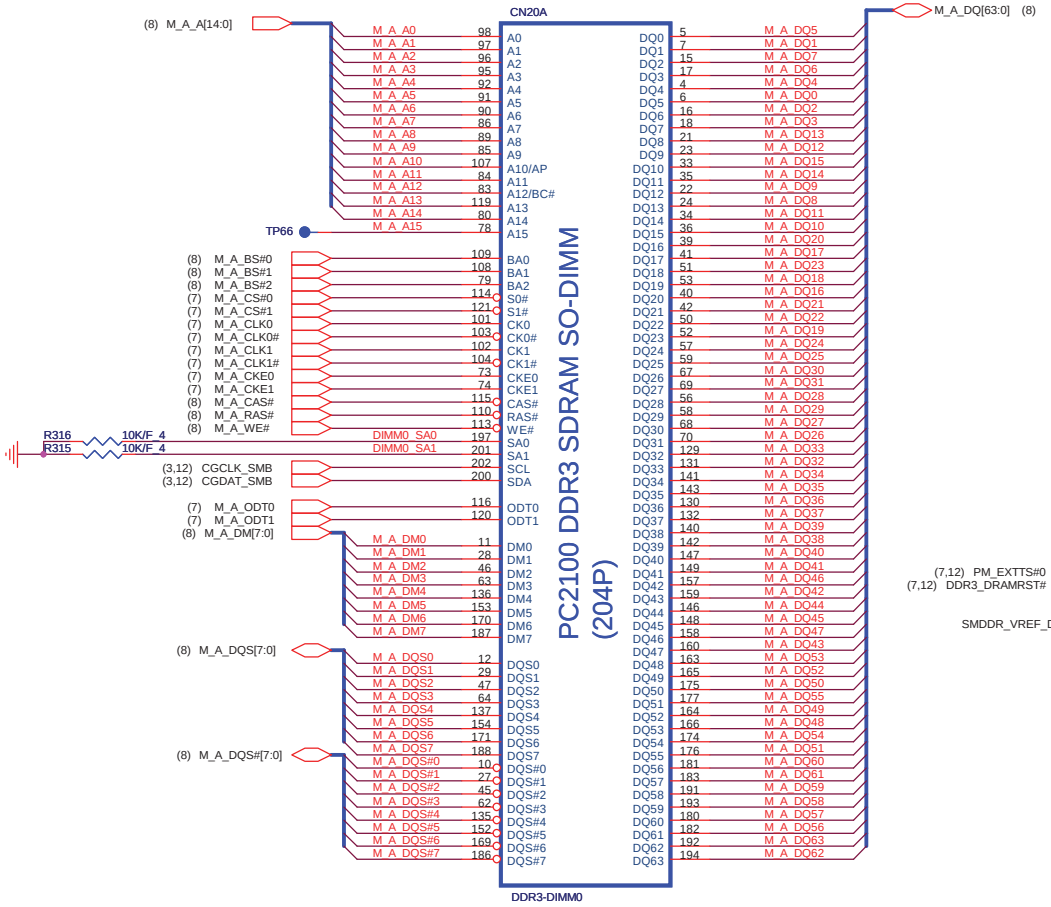
VCC NCTF

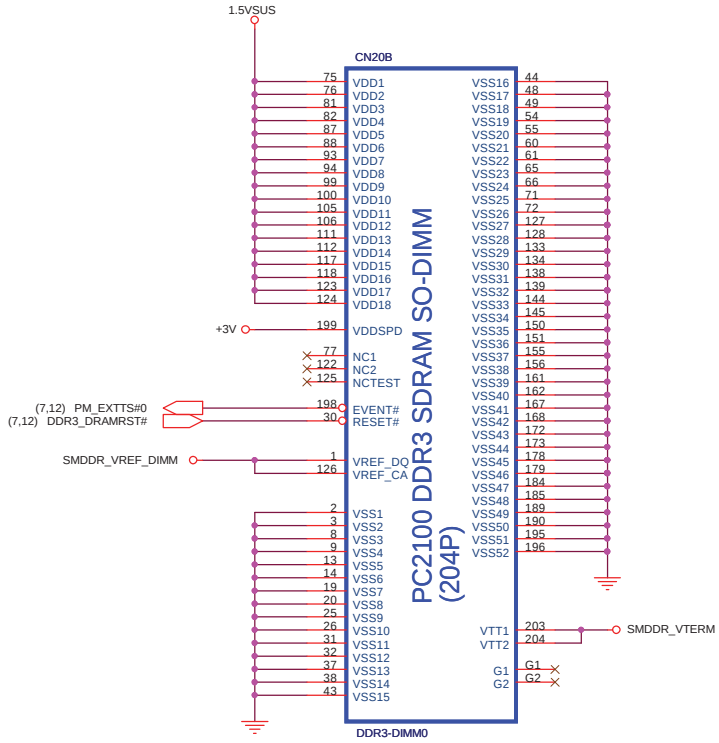
CANTIGA_PM

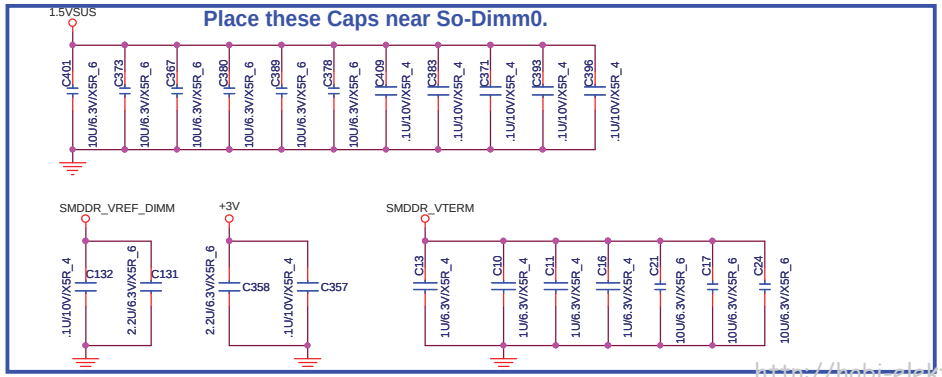
PROJECT : LL6
Quanta Computer Inc.

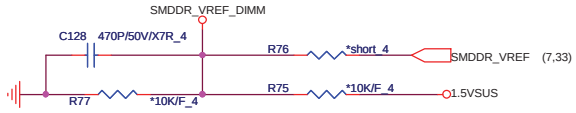
Size	Document Number	Rev
Custom	Cantiga Vcc 4/5	1A
Date: Wednesday, July 15, 2009	Sheet 9 of 36	


U20H
CANTIGA_PM
POWER
CRT
PLL
LVDS
A PEG
A SM
A CK
AXF
SM CK
HV
PEG
DMI
VTT
VTTLF
TV
HDA
D TV/CRT
A LVDS
(3,4,5,6,7,9,13,16,30,31,34,36) +1.05V
(3,5,7,11,12,13,14,15,16,17,18,19,20,21,22,23,24,25,26,27,28,29,30,31,32,34,35,36) +3V
(5,13,14,16,24,25,33) +1.5V
(31,34) 1.8VSUS
73mA
5mA
AB total 64.8mA
24mA
139.2mA
13.2mA
414uA
50mA
DDR3:1067M--747.5mA 800M--575mA
DDR3:1067M--37.95mA 800M--28.75mA
79mA
35mA
500uA
157.2mA
50mA
60.31mA
321.35mA
118.8mA
105.3mA
852mA
DDR3:1067M-149.5mA 800M-143.75mA
1782mA
456mA
http://hobi-elektronika.net
PROJECT : LL6
Quanta Computer Inc.
Size Custom
Document Number Cantiga Power 5/5
Rev 1A
Date: Wednesday, July 15, 2009
Sheet 10 of 36







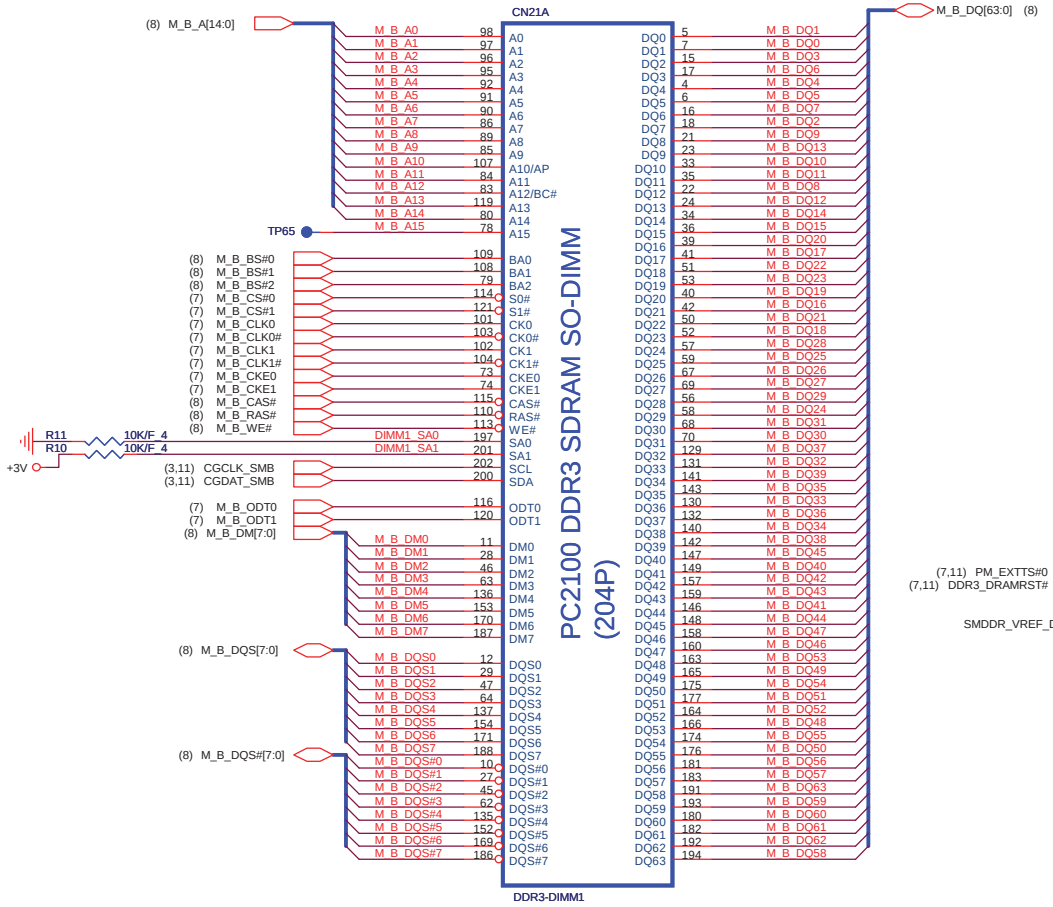


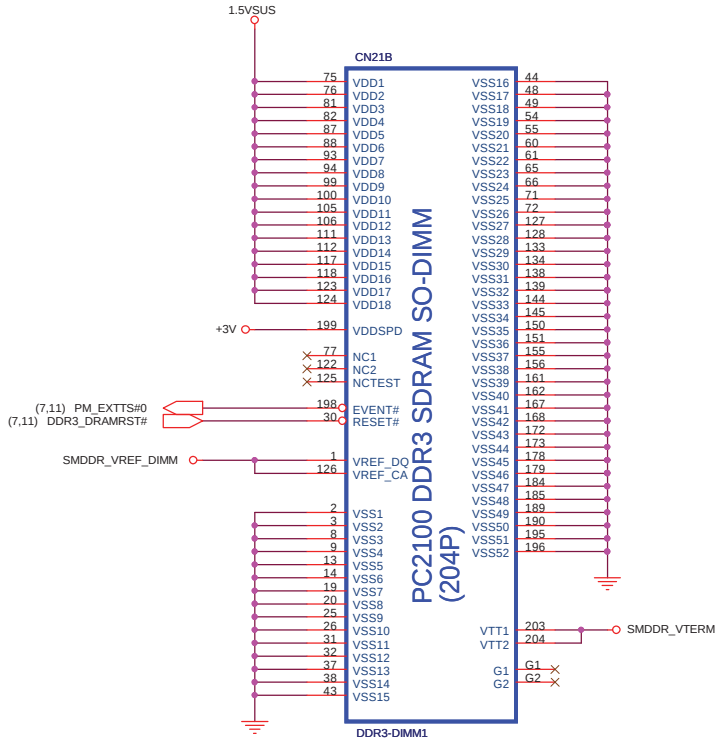
PROJECT : LL6

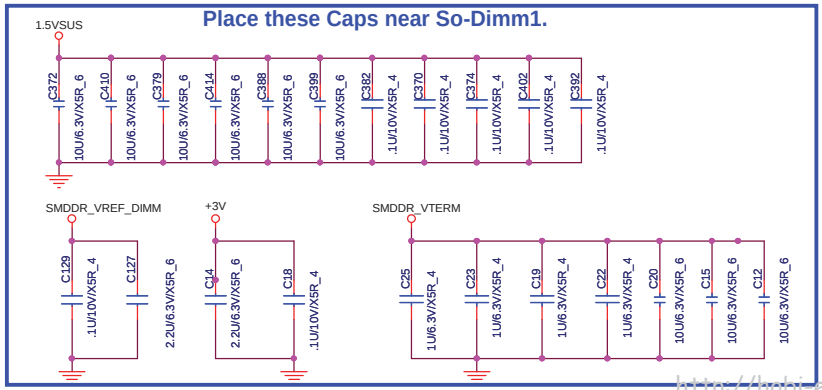
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM-0(H=5.2)	1A

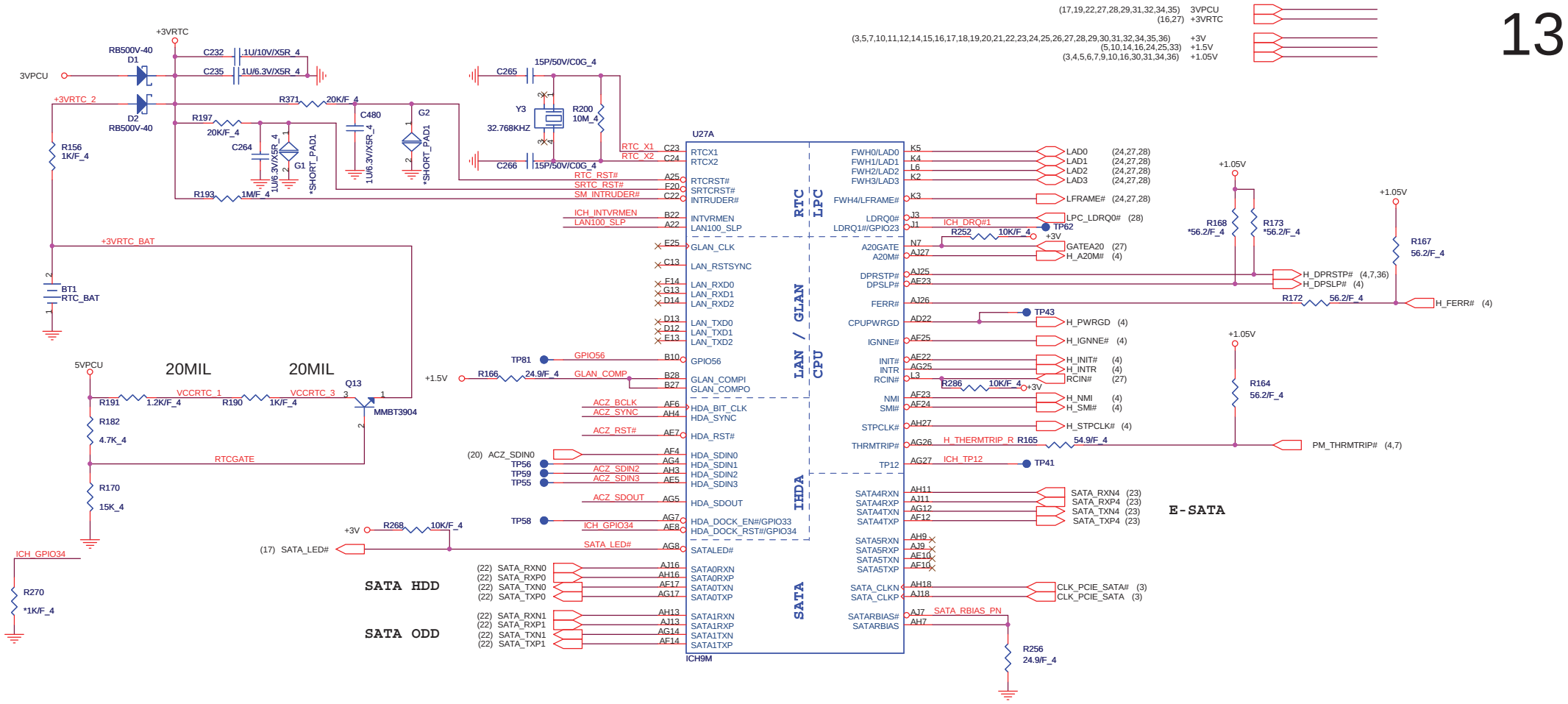
Date: Wednesday, July 15, 2009 Sheet 11 of 36







PROJECT : LL6		
Quanta Computer Inc.		
Size: Custom	Document Number: DDR3 DIMM-1(H=9.2)	Rev: 1A
Date: Wednesday, July 15, 2009	Sheet 12 of 36	



SB Strap

ICH9-M Internal VR Enable strap (Internal VR for Vccsus1_05,VccSus1_5 and VccCL1_5)

INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)

ICH9-M LAN100_SLP Strap (Internal VR for VccLAN1_05 and VccCL1.05)

LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)

XOR Chain Entrance Strap

ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1

ICH9 Boot BIOS select

STRAP	PCI_GNT0#	SPI_CS#1
SPI	0	1
PCI	1	0
LPC	1	1

(default)

No Reboot Strap	
ACZ_SPKR	Low: Default Hi: No reboot

A16 swap override strap	
PCI_GNT#3	Low = A16 swap override enabled Hi = Default

TPM physical presence	
ICH_GPIO57	Low: Default

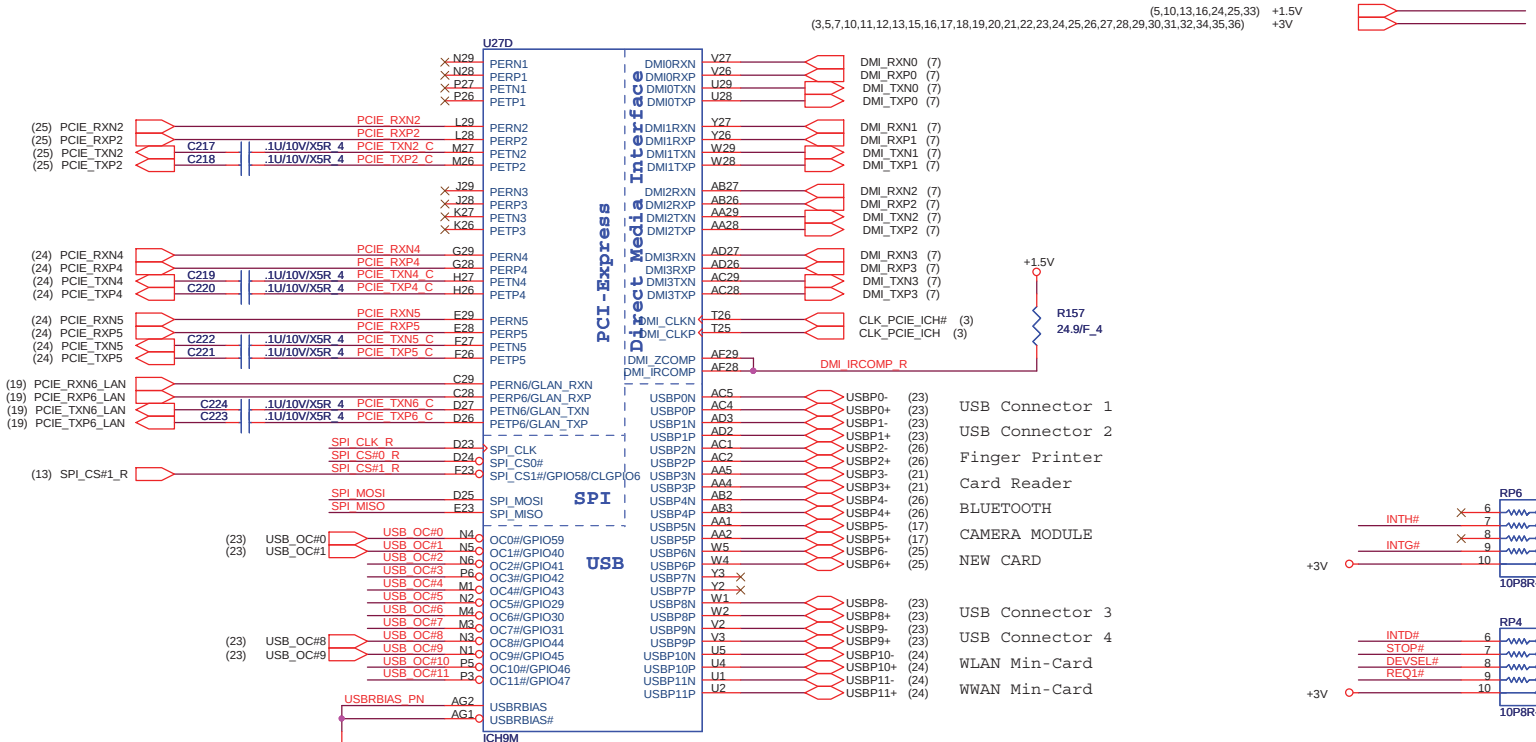
Project	PROJECT : LL6	
Quanta Computer Inc.		
Size: Custom	Document Number: ICH9-M Host 1/4	Rev: 1A
Date: Wednesday, July 15, 2009	Sheet 13 of 36	

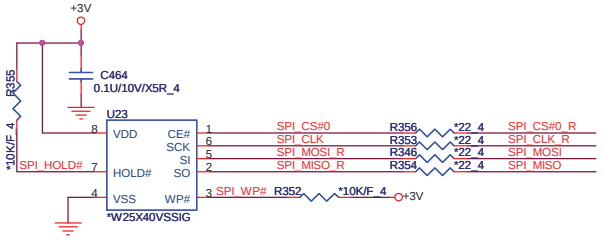
Express Card(NEW CARD)

MINI CARD PCI-E(WLAN)

MINI CARD PCI-E(WWAN)

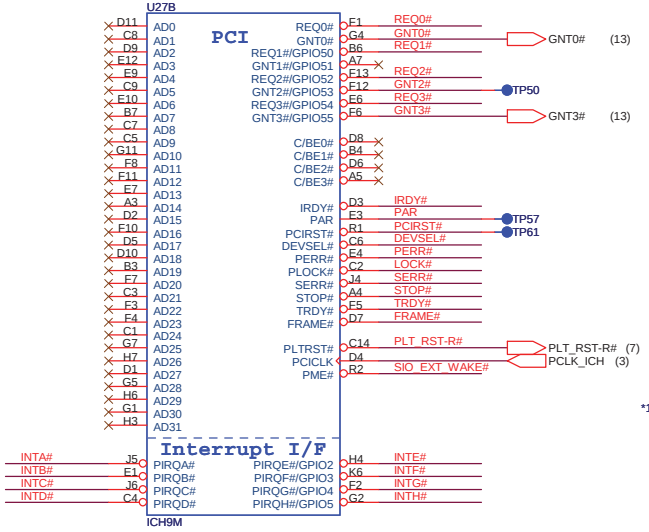
PCIE-LAN

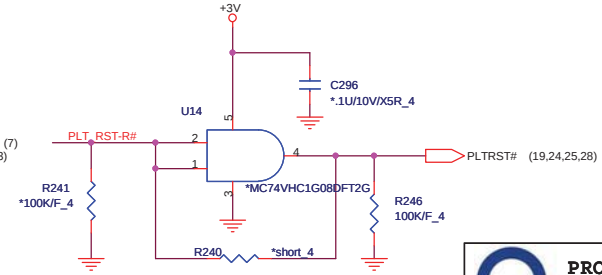


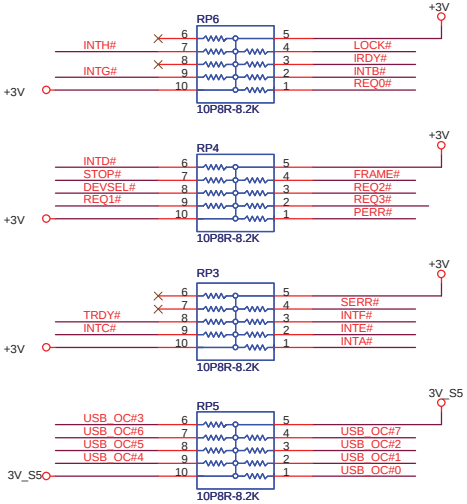


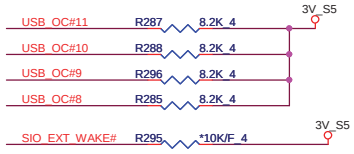
512K byte SPI ROM

For HDCP only









PROJECT : LL6

Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH9-M PCIE 2/4	1A
Date: Wednesday, July 15, 2009	Sheet 14 of 36	

(3,5,7,10,11,12,13,14,16,17,18,19,20,21,22,23,24,25,26,27,28,29,30,31,32,34,35,36) +3V
(13,14,16,31) 3V_S5

U27C

(3) PCLK_SMB — G16 SMBCLK
(3) PDAT_SMB — A13 SMBDATA
SMB_LINK_ALERT# — E17 LINKALERT#/GPIO60/CLGPIO4
SMB_CLK_ME — C17 SMLINK0
SMB_DATA_ME — B18 SMLINK1
SMB

(28) PM_RI# — F19 RI#
(28) LPC_PD# — R4 SUS_STAT#/LPCPD#
(4) SYS_RST# — G19 SYS_RESET#
(7) PM_SYNC# — M6 PMSYNC#/GPIO0
SMB_ALERT# — A17 SMBALERT#/GPIO11
(3) PM_STPPCI# — A14 STP_PCI#
(3) PM_STPCPU# — E19 STP_CPU#
(27,28) CLKRUN# — L4 CLKRUN#
(19,24,25) PCIE_WAKE# — E20 WAKE#
(27,28) SERIRQ — M5 SERIRQ
(5) PM_THRM# — AJ23 THRM#
VR_PWRGO_CLKEN — D21 VRMPWRGD
TP79 — ICH_TP11 — A20 TP11
TP76 — JCD385_INT — AG19 GPIO1
(27) KBSMI# — AH21 GPIO6
(27) SCI# — AG21 GPIO7
TP77 — SWI# — A21 GPIO8
T25 — LAN_PHYPC — C12 GPIO12
TP44 — ENERGY_DEC — C21 GPIO13
BOARD_ID0 — AE18 GPIO17
TP60 — SIM_CARD_DET — K1 GPIO18
(17) LCD_BK_OFF — AF8 GPIO20
BOARD_ID3 — AJ22 SCLOCK/GPIO22
(24) WWAN_OFF# — A9 GPIO27
(24) WLAN_OFF# — D19 GPIO28
TP64 — ICH_GPIO35 — L1 SATACLKREQ#/GPIO35
(17) CCD_OFF# — AE19 SLOAD/GPIO38
TP78 — ICH_GPIO39 — AG22 SDATAOUT0/GPIO39
TP75 — ICH_GPIO48 — AF21 SDATAOUT1/GPIO48
TP42 — ICH_GPIO49 — AH24 GPIO49
(13) ICH_GPIO57 — A8 GPIO57/CLGPIO5
(13,20) ACZ_SPKR — M7 SPKR
(7) MCH_ICH_SYNC# — AJ24 MCH_SYNC#
(13) ICH_TP3 — B21 TP3
TP73 — ICH_TP8 — AH20 TP8
TP74 — ICH_TP9 — AJ20 TP9
TP72 — ICH_TP10 — AJ21 TP10
ICH9M

SYS GPIO / Power MGT / GPIO / Controller Link / MISC

SATA0GP/GPIO21 — AH23 — BOARD_ID2
SATA1GP/GPIO19 — AF19 — BOARD_ID1
SATA4GP/GPIO36 — AE21 — BOARD_ID4
SATA5GP/GPIO37 — AD20 — BOARD_ID5
CLK14 — H1 — CLK_14M_ICH (3)
CLK48 — AF3 — CLK_48M_USB (3)
SUSCLK — P1 — SUSCLK — TP63
SLP_S3# — C16 — SUSB# (27)
SLP_S4# — E16 — SUSC# (27)
SLP_S5# — G17 — SLP_S5# — TP47
S4_STATE#/GPIO26 — C10 — S4_STATE# — TP51
PWROK — G20 — PM_ICH_PWROK
DPRSLPVR/GPIO16 — M2 — DPRSLPVR (7,36)
BATLOW# — B13 — PM_BATLOW#
PWRBTN# — R3 — DNBSWON# (27)
LAN_RST# — D20 — ICH_LAN_RST#
RSMRST# — D22 — RSMRST# — RSMRST# (27)
CK_PWRGD — R5 — CK_PWG (3)
CLPWROK — R6 — ECPWROK
SLP_M# — B16 — ICH_SLP_M# — TP80
CL_CLK0 — F24 — CL_CLK0 (7)
CL_CLK1 — B19 — CL_CLK1 — TP45
CL_DATA0 — F22 — CL_DATA0 (7)
CL_DATA1 — C19 — CL_DATA1 — TP46
CL_VREF0 — C25 — CL_VREF0_ICH
CL_VREF1 — A19 — CL_VREF1_ICH
CL_RST0# — F21 — CL_RST#0 (7)
CL_RST1# — D18 — CL_RST#1 — TP49
MEM_LED/GPIO24 — A16 — BT_OFF# (26)
GPIO10/SUS_PWR_ACK — C18 — SUS_PWR_ACK
GPIO14/AC_PRESENT — C11 — AC_PRESENT_R
WOL_EN/GPIO9 — C20 — ICH_WOL_EN — TP54
R199 10K/F_4

3V_S5
R393 *3.24K/F_4
0.405V
R394 *453/F_4
C497 *.1U/10V/X5R_4
+3V
R184 3.24K/F_4
R174 453/F_4
C247 .1U/10V/X5R_4

Notice: GPIO20 signal should not be pulled high for functional strap(internal pull down 20k).

Notice: GPIO49 is also a strap pin(internal pull up 20k). Don't pull-down.

+3V
R251 1K/F_4
VR_PWRGO_CLKEN
Q15
(36) VR_PWRGD_CK410#
2N7002
R205 100K/F_4

+3V
3V_S5
C273 .1U/10V/X5R_4
R237 *2K/F_4
U12
(7,36) DELAY_VR_PWRGOOD
(7,27) ECPWROK
MC74VHC1G08DFT2G
PM_ICH_PWROK
R213 10K/F_4
R218 *0_4

Board ID

Board ID For Function	ID3 GPIO22	ID2 GPIO21	ID1 GPIO19	ID0 GPIO17
Default	0	0	0	0
	0	0	0	1
	0	0	1	0
	0	0	1	1
	0	1	0	0
	0	1	0	1
	0	1	1	0
	0	1	1	1
	1	0	0	0
	1	0	0	1
	1	0	1	0
	1	0	1	1
	1	1	0	0
	1	1	0	1
	1	1	1	0
	1	1	1	1

+3V
R185 *10K/F_4 BOARD_ID0 R186 10K/F_4
R204 *10K/F_4 BOARD_ID1 R208 10K/F_4
R188 *10K/F_4 BOARD_ID2 R189 10K/F_4
R177 *10K/F_4 BOARD_ID3 R178 10K/F_4
R194 *10K/F_4 BOARD_ID4 R195 10K/F_4
R201 *10K/F_4 BOARD_ID5 R202 10K/F_4

Board ID For Model	ID5 GPIO37	ID4 GPIO36
	0	0
	0	1
	1	0
	1	1

3V_S5
SWI# R384 10K/F_4
PM_RI# R219 10K/F_4
SMB_CLK_ME R230 10K/F_4
SMB_DATA_ME R397 10K/F_4
DNBSWON# R294 10K/F_4
PCLK_SMB R233 2.2K_4
PDAT_SMB R234 2.2K_4
SMB_ALERT# R396 10K/F_4
PCIE_WAKE# R211 10K/F_4
PM_BATLOW# R399 8.2K_4
SMB_LINK_ALERT# R222 10K/F_4
SYS_RST# R215 10K/F_4
SUS_PWR_ACK R229 10K/F_4

+3V
ICH_TP3 R387 *10K/F_4
PM_THRM# R183 8.2K_4
SERIRQ R253 10K/F_4
CLKRUN# R255 8.2K_4
KBSMI# R192 10K/F_4
SCI# R209 10K/F_4
ICH_GPIO35 R297 10K/F_4
SIM_CARD_DET R298 10K/F_4
ICH_GPIO39 R217 10K/F_4

RSMRST# R198 10K/F_4
JCD385_INT R216 10K/F_4

PROJECT : LL6
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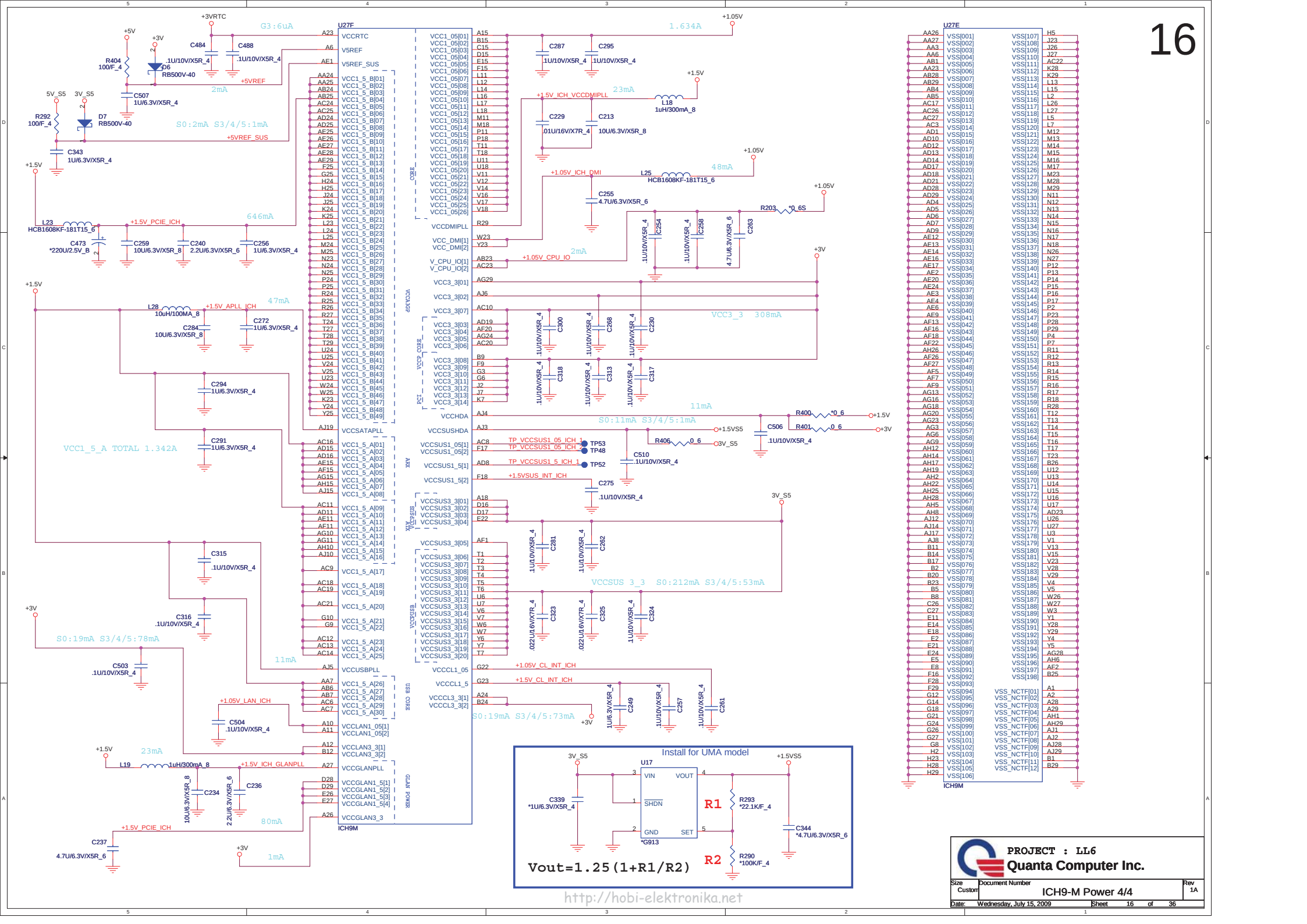
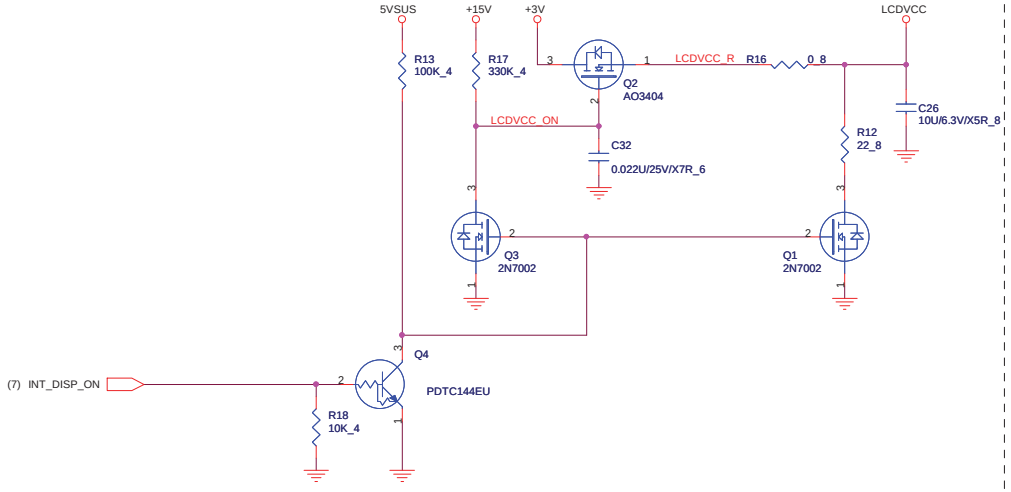
Size	Document Number	Rev
Custom	ICH9-M GPIO 3/4	1A

Date: Wednesday, July 15, 2009 Sheet 15 of 36

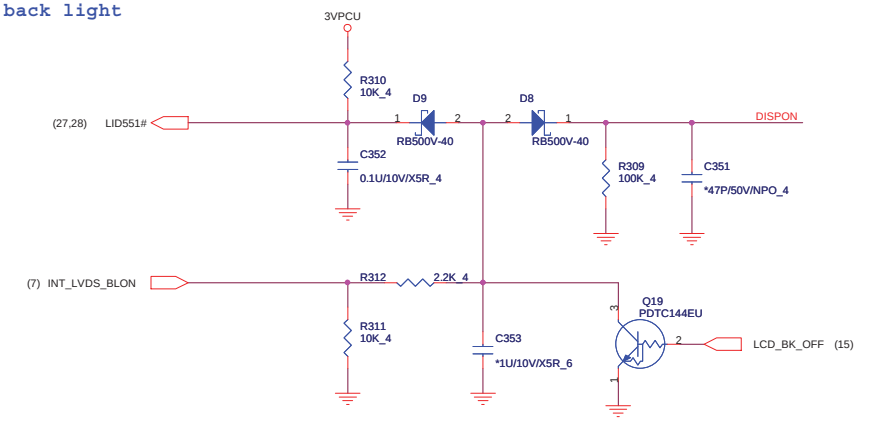

U27F
ICH9M
U27E
ICH9M
+3VRTC
G3:6uA
+5V
+3V
R404
100/F_4
D6
RB500V-40
.1U/10V/X5R_4
C484
C488
.1U/10V/X5R_4
+5VREF
2mA
5V_S5
3V_S5
C507
1U/6.3V/X5R_4
R292
100/F_4
D7
RB500V-40
S0:2mA S3/4/5:1mA
+5VREF_SUS
C343
1U/6.3V/X5R_4
+1.5V
L23
HCB1608KF-181T15_6
+1.5V_PCIE_ICH
646mA
C473
*220U/2.5V_B
C259
10U/6.3V/X5R_8
C240
2.2U/6.3V/X5R_6
C256
1U/6.3V/X5R_4
L28
10uH/100MA_8
+1.5V_APLL_ICH
47mA
C284
10U/6.3V/X5R_8
C272
1U/6.3V/X5R_4
C294
1U/6.3V/X5R_4
C291
1U/6.3V/X5R_4
VCC1_5_A TOTAL 1.342A
C315
.1U/10V/X5R_4
C316
.1U/10V/X5R_4
S0:19mA S3/4/5:78mA
C503
.1U/10V/X5R_4
11mA
+1.05V_LAN_ICH
C504
.1U/10V/X5R_4
+1.5V
23mA
L19
1uH/300mA_8
+1.5V_ICH_GLANPLL
C234
10U/6.3V/X5R_8
C236
2.2U/6.3V/X5R_6
80mA
+1.5V_PCIE_ICH
C237
4.7U/6.3V/X5R_6
+3V
1mA
+1.05V
1.634A
C287
1U/10V/X5R_4
C295
1U/10V/X5R_4
+1.5V_ICH_VCCDMIPLL
23mA
L18
1uH/300mA_8
C229
.01U/16V/X7R_4
C213
10U/6.3V/X5R_8
+1.05V_ICH_DMI
48mA
L25
HCB1608KF-181T15_6
C255
4.7U/6.3V/X5R_6
R203
*0_6S
+1.05V_CPU_IO
2mA
C254
.1U/10V/X5R_4
C258
.1U/10V/X5R_4
C263
4.7U/6.3V/X5R_6
VCC3_3 308mA
C300
C268
C230
C318
C313
C317
11mA
S0:11mA S3/4/5:1mA
R400
*0_6
R401
0_6
+1.5V
+3V
+1.5VS5
R406
0_6
3V_S5
C506
.1U/10V/X5R_4
TP_VCCSUS1_05_ICH_1
TP_VCCSUS1_05_ICH_2
TP_VCCSUS1_5_ICH_1
TP53
TP48
TP52
C510
.1U/10V/X5R_4
+1.5VSUS_INT_ICH
C275
.1U/10V/X5R_4
3V_S5
C281
C262
VCCSUS 3_3 S0:212mA S3/4/5:53mA
C323
C325
C324
+1.05V_CL_INT_ICH
+1.5V_CL_INT_ICH
S0:19mA S3/4/5:73mA
+3V
C249
C257
C261
Install for UMA model
U17
VIN
VOUT
SHDN
GND
SET
*G913
3V_S5
+1.5VS5
C339
*1U/6.3V/X5R_4
R1
R293
*22.1K/F_4
R2
R290
*100K/F_4
C344
*4.7U/6.3V/X5R_6
Vout=1.25(1+R1/R2)
http://hobi-elektronika.net
PROJECT : LL6
Quanta Computer Inc.
Size Custom
Document Number
ICH9-M Power 4/4
Rev 1A
Date: Wednesday, July 15, 2009
Sheet 16 of 36

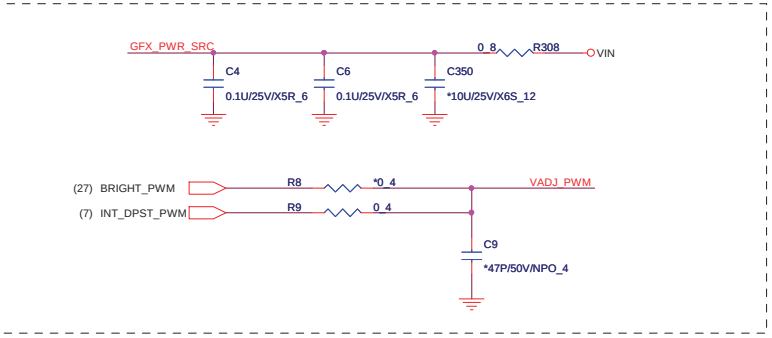
LCD panel control & connector

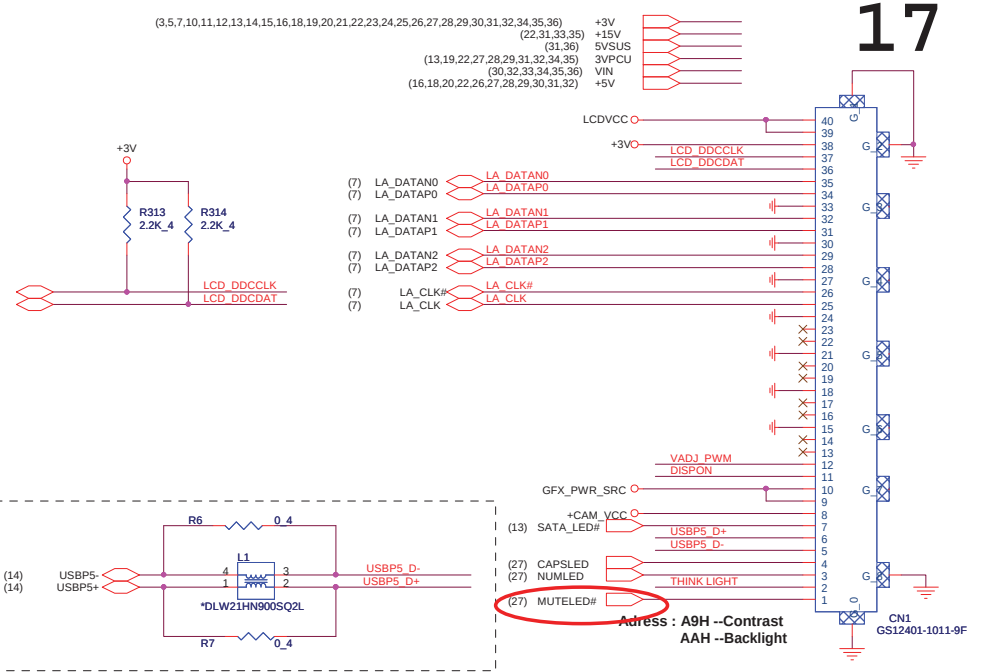
LCDVCC



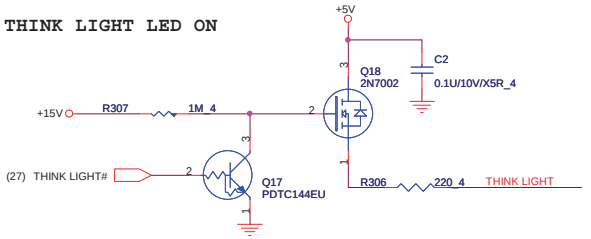
back light



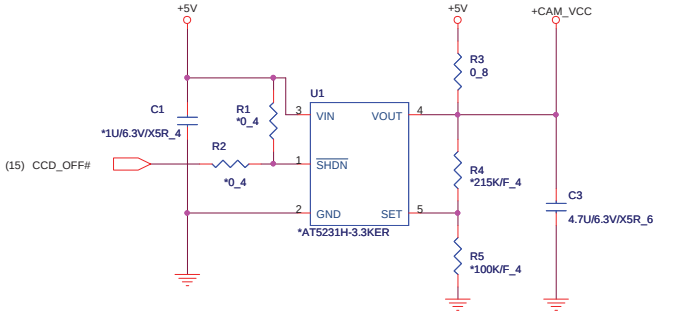




THINK LIGHT LED ON



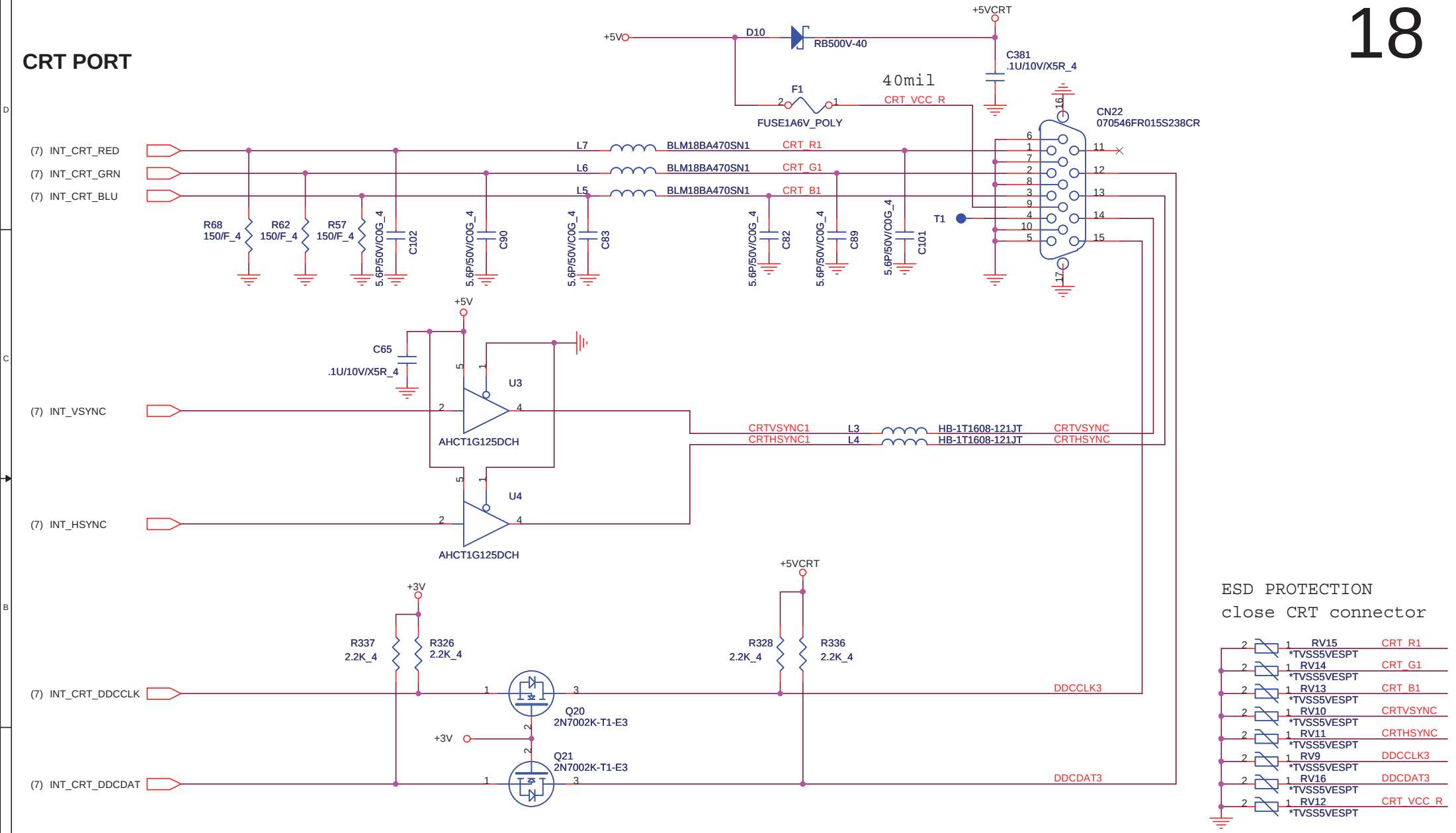
CAMERA VCC Control



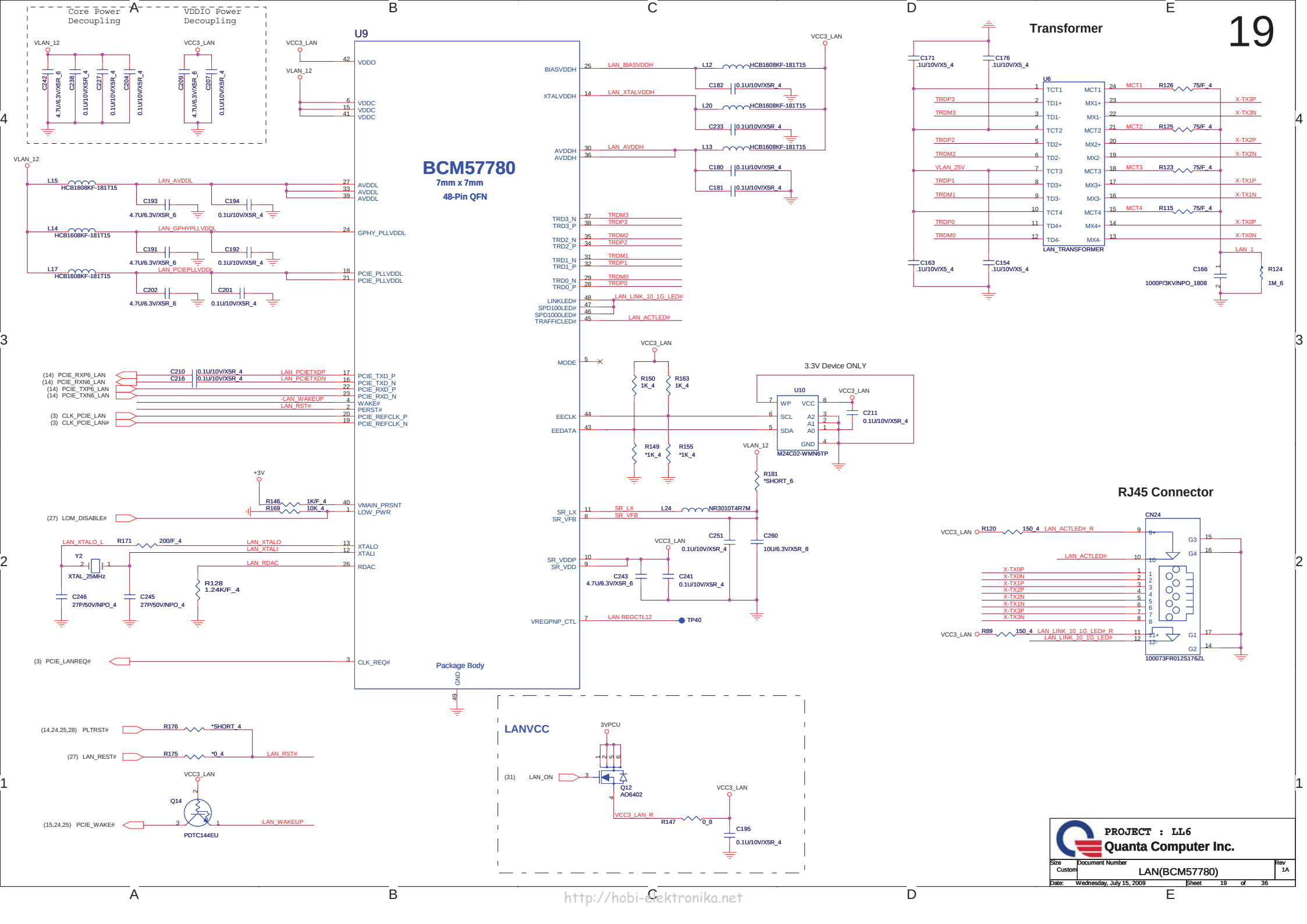
PROJECT : LL6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD/LID/CCD CON	1A
Date: Wednesday, July 15, 2009	Sheet 17 of 36	

CRT PORT



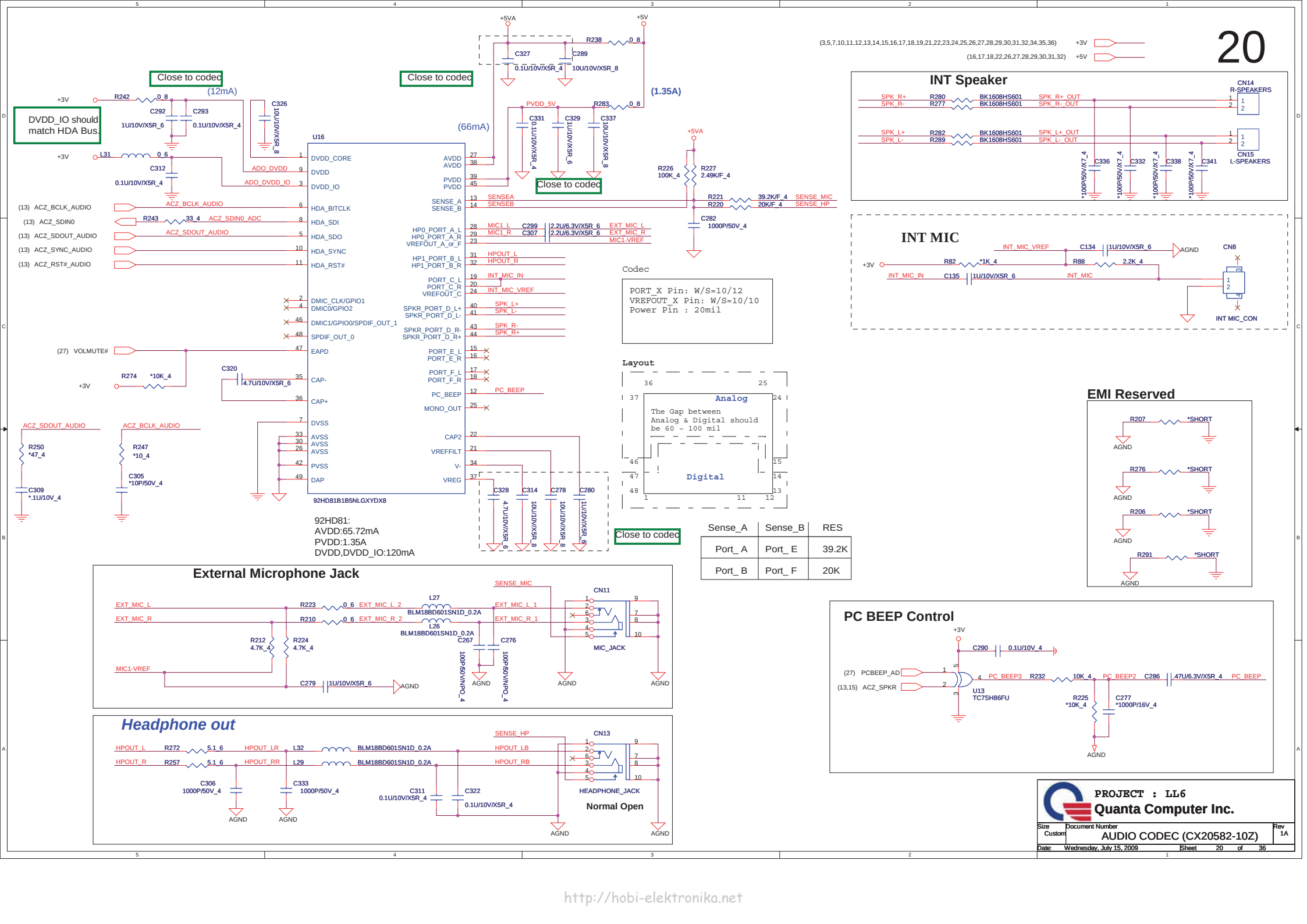
PROJECT : LL6		
Quanta Computer Inc.		
Size: Custom	Document Number: CRT_CON	Rev: 1A
Date: Wednesday, July 15, 2009	Sheet 18 of 36	



PROJECT : LL6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LAN(BCM57780)	1A

Date: Wednesday, July 15, 2009 Sheet 19 of 36



+3V (3,5,7,10,11,12,13,14,15,16,17,18,19,20,22,23,24,25,26,27,28,29,30,31,32,34,35,36)

RTS5159-GR

Realtek RTS5159

For external 12Mhz clock input
pin13 floating
For external 48Mhz clock input
pin13 pull high

Close to Pin9

Vreg out 1.8V from Internal 3.3VLDO

Note:

For RTS5159

	SD/MMC	MS	XD
SP0			
SP1			XD_CD#
SP2	SD_WP		
SP3	SD_CD#		
SP4	SD_DAT1		XD_D4
SP5		MS_BS	XD_D5
SP6		MS_D1	XD_D3
SP7	SD_DAT0	MS_D0	XD_D6
SP8	SD_DAT7	MS_D2	XD_D2
SP9		MS_INS#	
SP10	SD_DAT6	MS_D3	XD_D7
SP11	SD_CLK	MS_SCLK	XD_D1
SP12	SD_DAT5		XD_D0
SP13	SD_DAT4		XD_WP#
SP14			XD_R/B#
SP15	SD_DAT3		XD_WE#
SP16	SD_DAT2		XD_RE#
SP17			XD_ALE
SP18			XD_CE#
SP19			XD_CLE

SP7 R360 0_4 MS_DATA0_SD_DAT0
R359 0_4 XD-D6
SP6 R361 0_4 MS_DATA1
R362 0_4 XD-D3
SP16 R347 0_4 SD_DAT2
R351 0_4 XD-RE#
SP5 R364 0_4 MS_BS
R363 0_4 XD-D5
SP15 R348 0_4 SD_DAT3
R349 0_4 XD_WE
SP11 R162 0_4 SD_CLK_MS_CLK
R161 0_4 XD-D1
SP10 R158 0_4 MS_DATA3
R159 0_4 XD-D7
SP4 R367 0_4 XD-D4
R368 0_4 SD_DAT1

5 IN1 CARD READER
XD,MMC/SD,MS/MSP

CN12

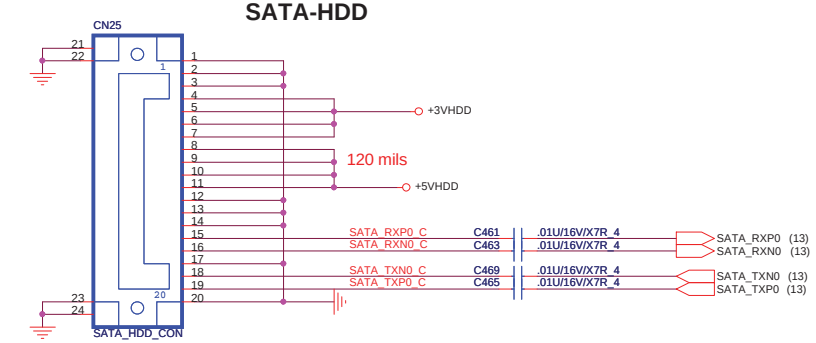
144-1300302600-42p

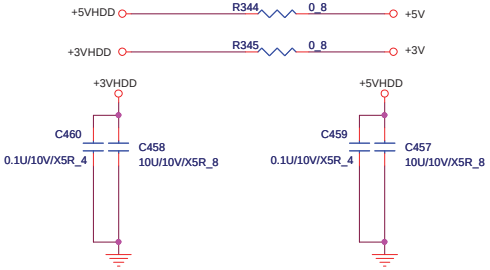
CLOSE CONN 18Pin

PROJECT : LL6
Quanta Computer Inc.

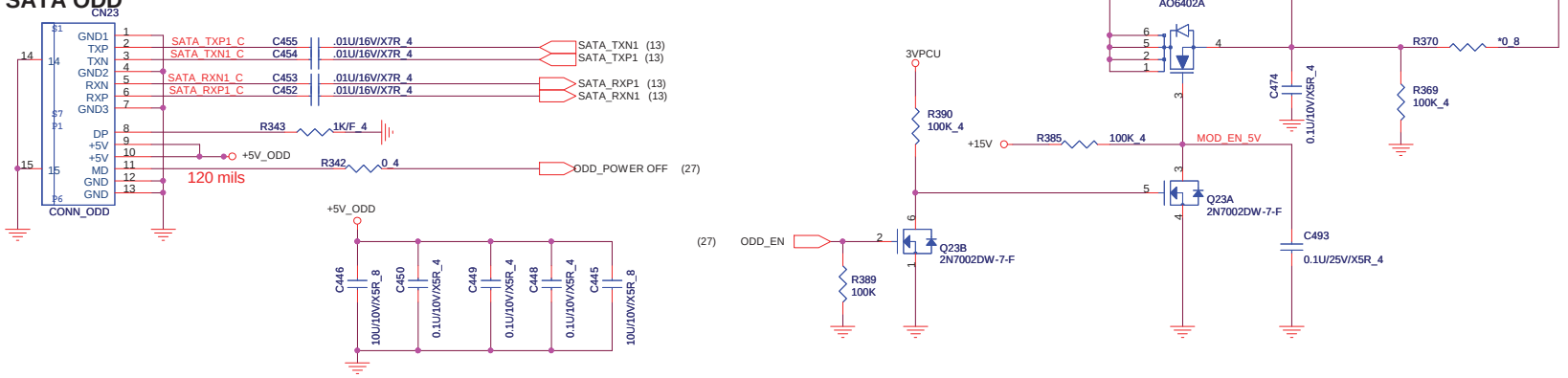
Size	Document Number	Rev
Custom	Card Reader (RTS5159)	1A
Date: Wednesday, July 15, 2009	Sheet 21 of 36	

SATA-HDD





SATA ODD

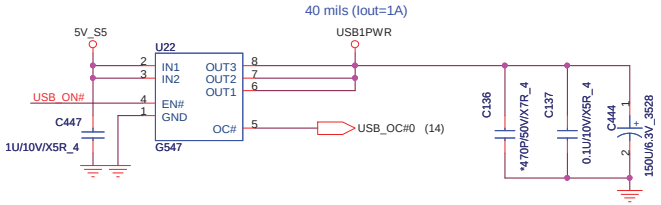


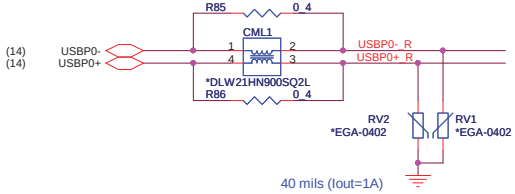
PROJECT : LL6

Quanta Computer Inc.

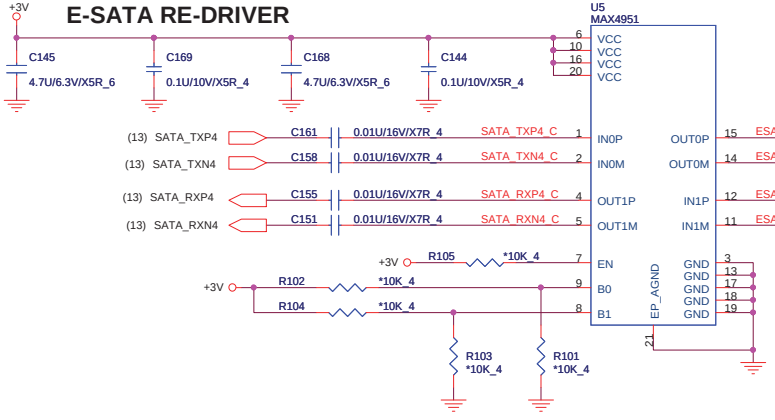
Size	Document Number	Rev
Custom	SATA HDD/ ODD/ eSATA/USB	1A
Date: Wednesday, July 15, 2009	Sheet 22 of 36	

USB 1

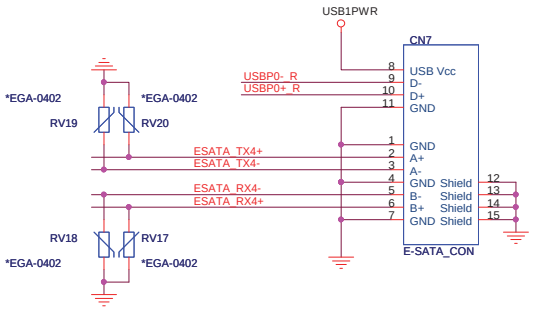




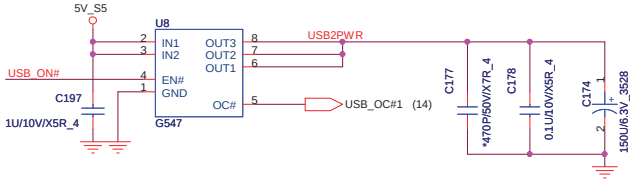
E-SATA RE-DRIVER

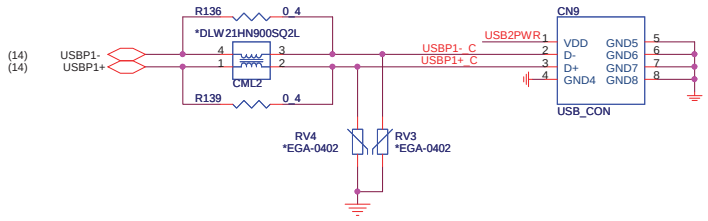


EN	B0	B1	FUNCTION
0	X	X	Standby
1	0	0	Standard SATA Output
1	1	0	Ch 0 Boost Output
1	0	1	Ch 1 Boost Output
1	1	1	Ch 0,1 Boost Output

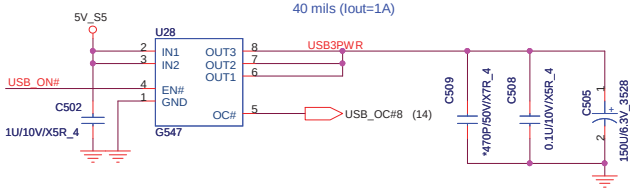


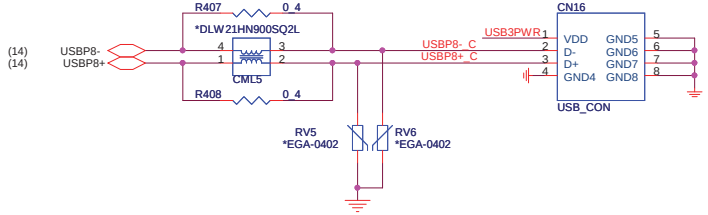
USB 2



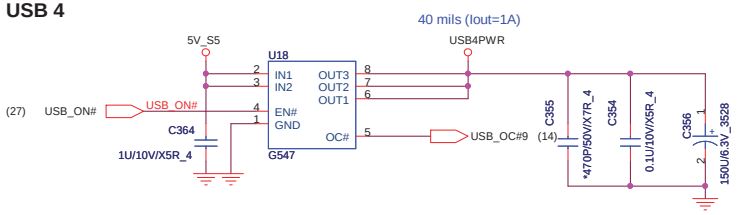


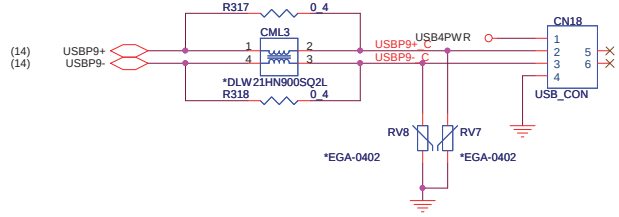
USB 3





USB 4





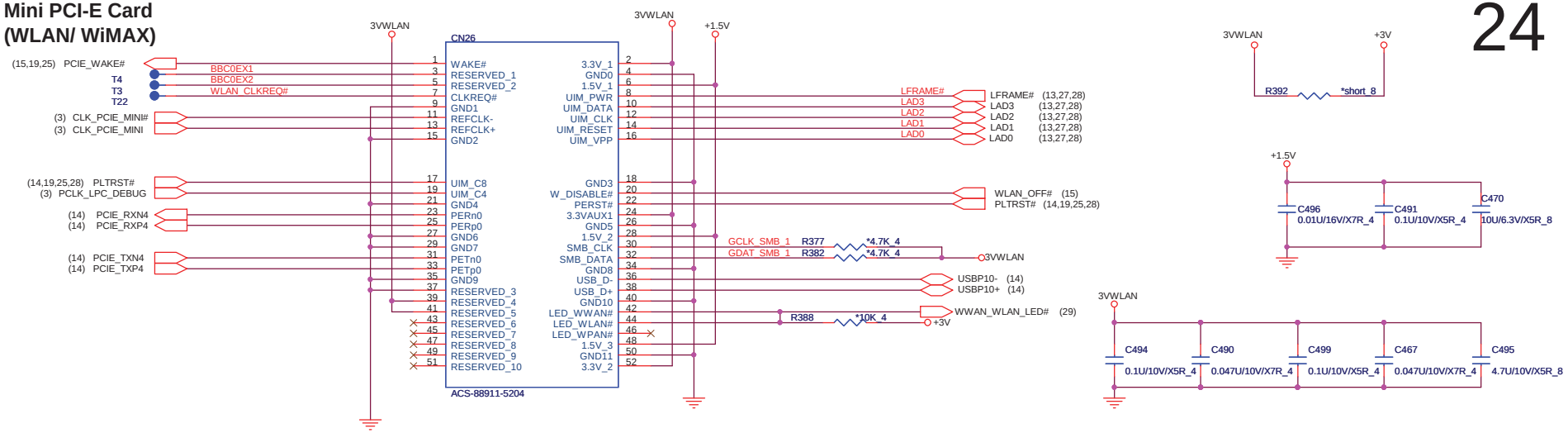
PROJECT : LL6

Quanta Computer Inc.

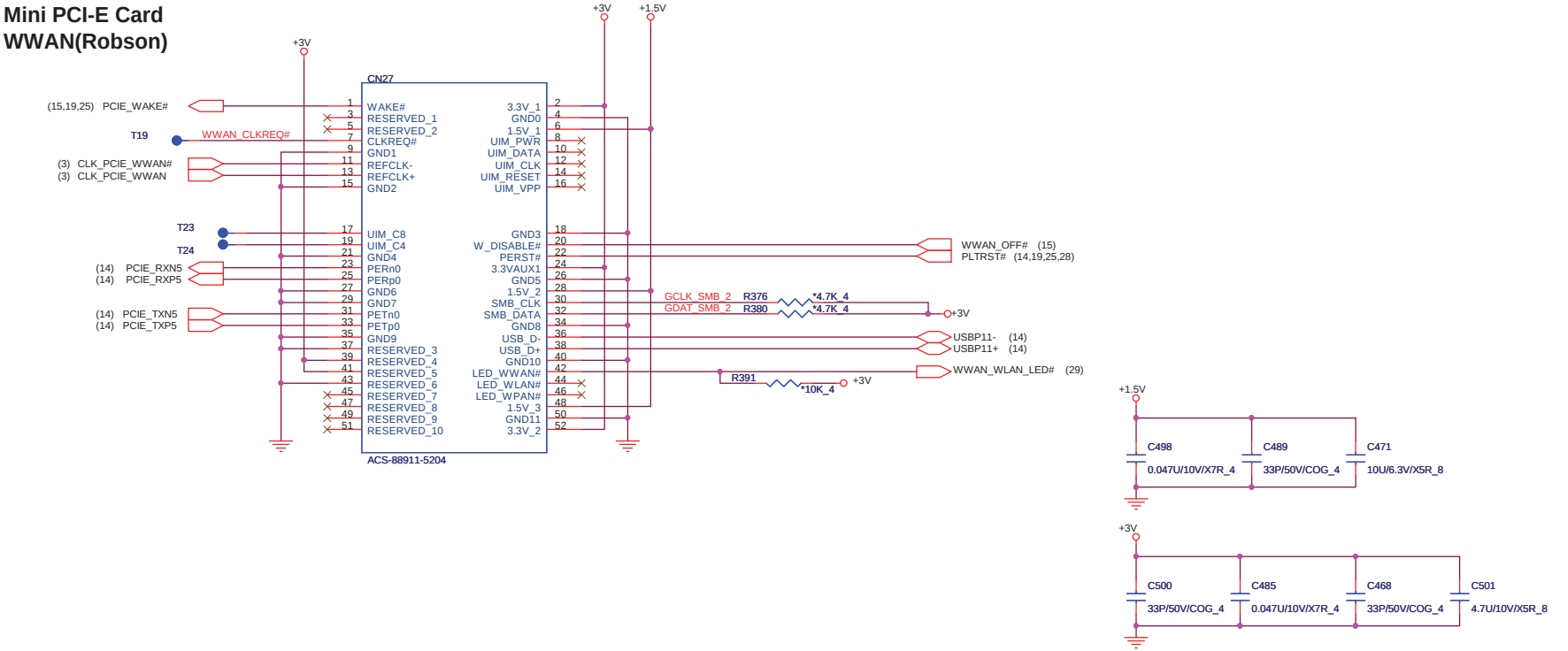
Size	Document Number	Rev
Custom	USB X4/eSATA PORT	1A

Date: Wednesday, July 15, 2009 Sheet 23 of 36

Mini PCI-E Card (WLAN/ WiMAX)



Mini PCI-E Card WWAN(Robson)



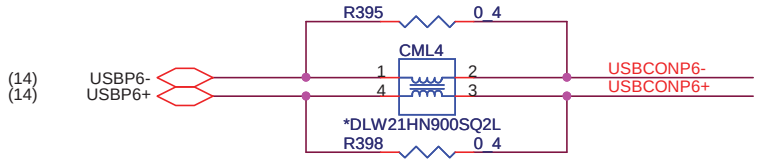
PROJECT : LL6

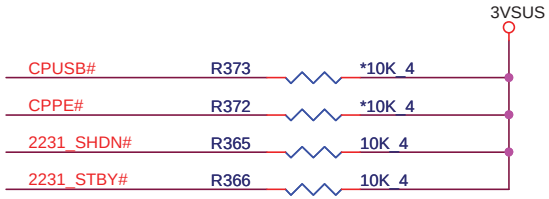
Quanta Computer Inc.

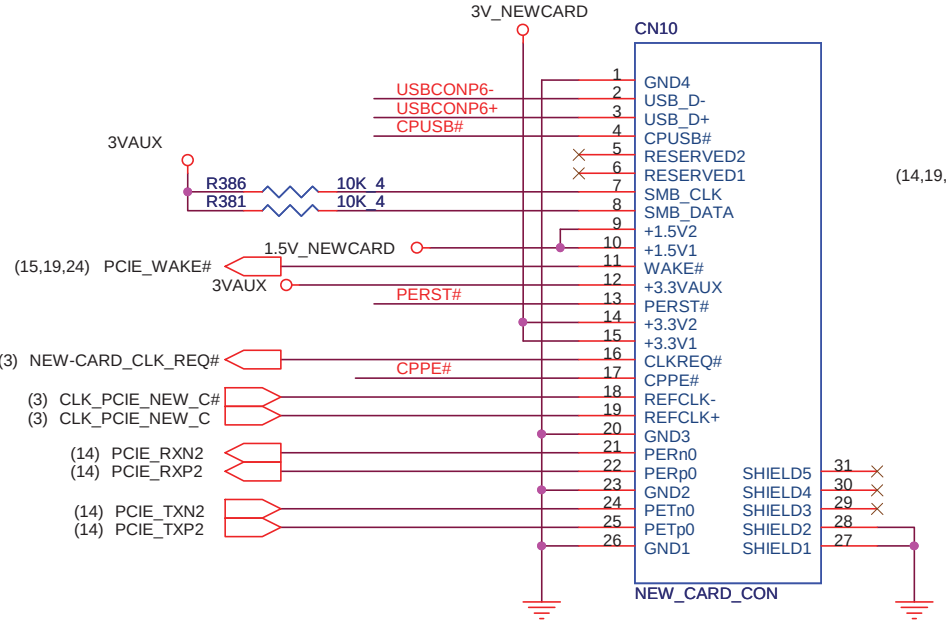
Size	Document Number	Rev
Custom	WLAN & WWAN Slot	1A
Date: Wednesday, July 15, 2009	Sheet 24 of 36	

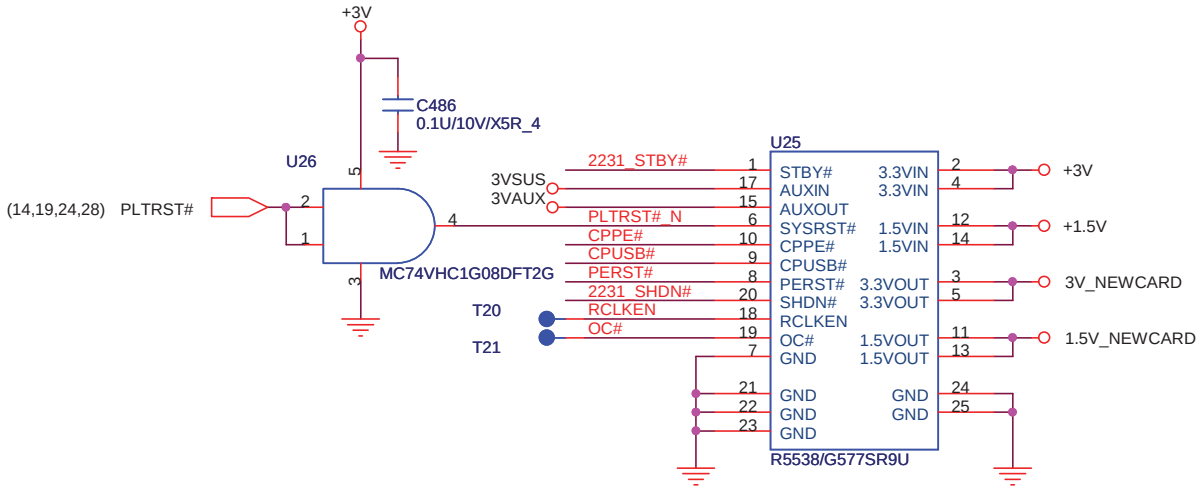
PCI Express Card

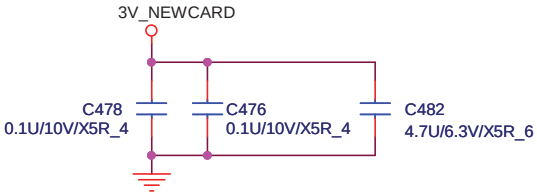
25

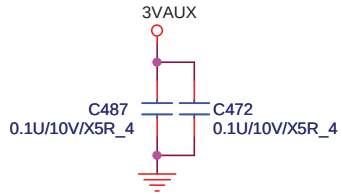


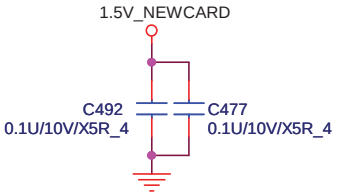












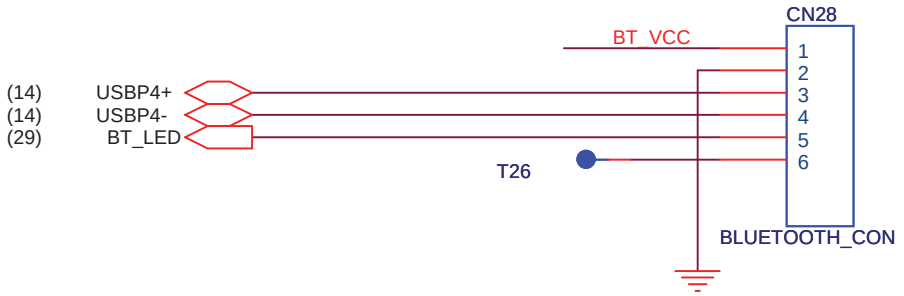
PROJECT : LL6

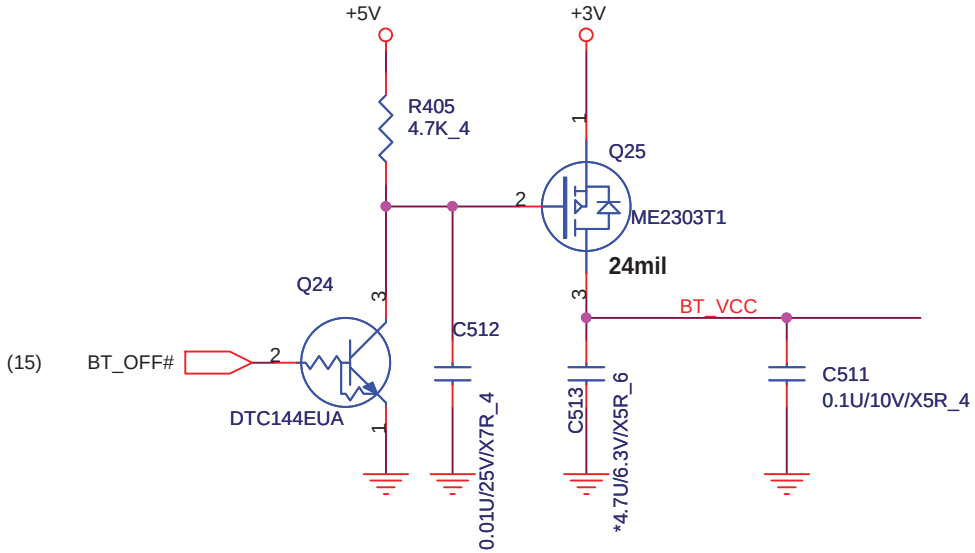
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCI Express Card	1A

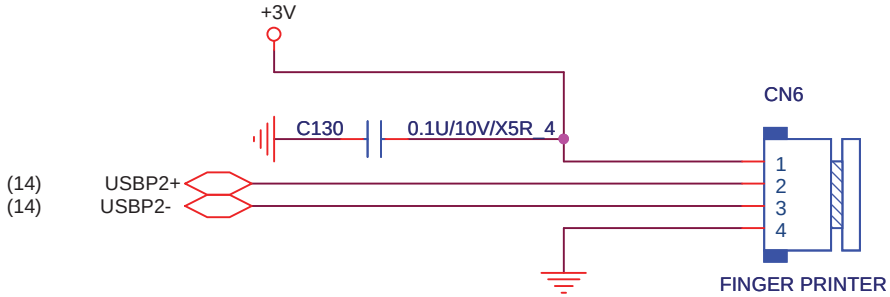
Date: Wednesday, July 15, 2009 Sheet 25 of 36

BLUETOOTH





FINGER PRINTER



PROJECT : LL6		
Quanta Computer Inc.		
Size: Custom	Document Number: Buletooth / FP Conn	Rev: 1A
Date: Wednesday, July 15, 2009	Sheet 26 of 36	

IT8502E

(For PLL Power)

GM/PM Board ID

POWER SWITCH/ NOVO BUTTON

RF ON/OFF SWITCH

16Mbit (2M Byte), SPI

SST AKE28FP0K07
MX AKE37FP0Z13

U15 MX25L1605A

Layout Note:
Place all capacitors close to IT8512.

Layout Note:
net "3VPCU" and "RTC_VCC" minimum trace width 12mils.

Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.

Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.

TMKBC Function	
High	Enable
Low	Disable

R609	FLASH TYPE SELECT
High	LPC/FWH FLASH ROM
Low	SPI FLASH ROM (Default)

GPIO
LPC
CIR
SM BUS
PS/2
PWM
WAKE UP
UART
FLASH
KBMX
A/D D/A
CLOCK

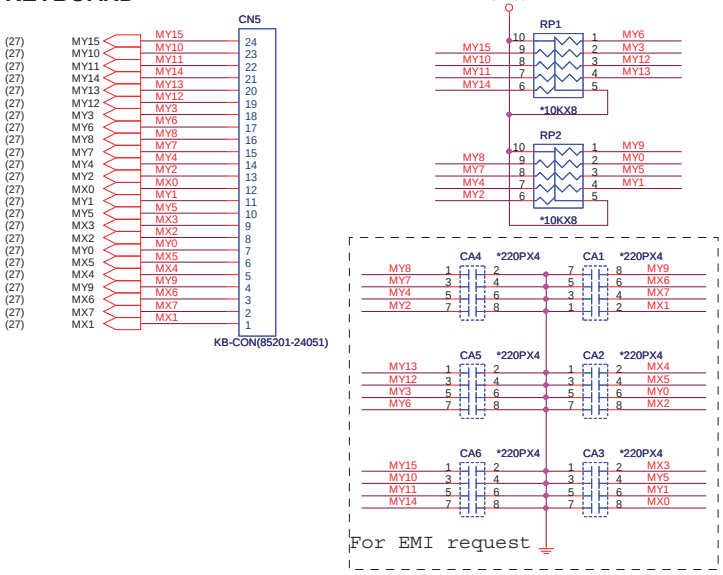
U11 IT8502E

PROJECT : LL6
Quanta Computer Inc.

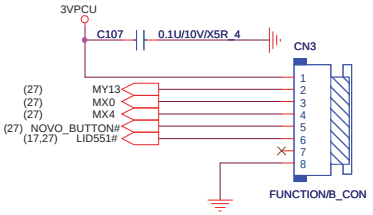
Size	Document Number	Rev
Custom	KBC IT8502E	1A

Date: Wednesday, July 15, 2009 Sheet 27 of 36

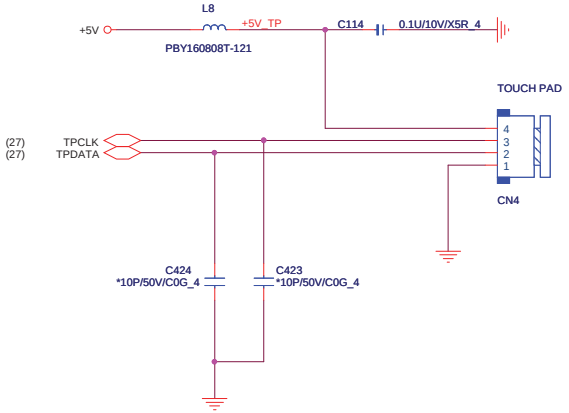
KEYBOARD



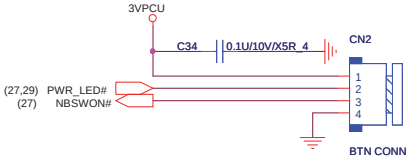
FUNCTION BUTTON BOARD



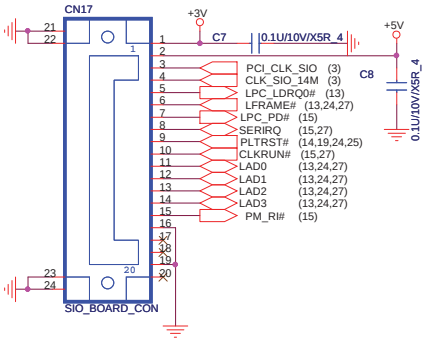
TOUCH PAD



POWER BUTTON BOARD



SIO BOARD

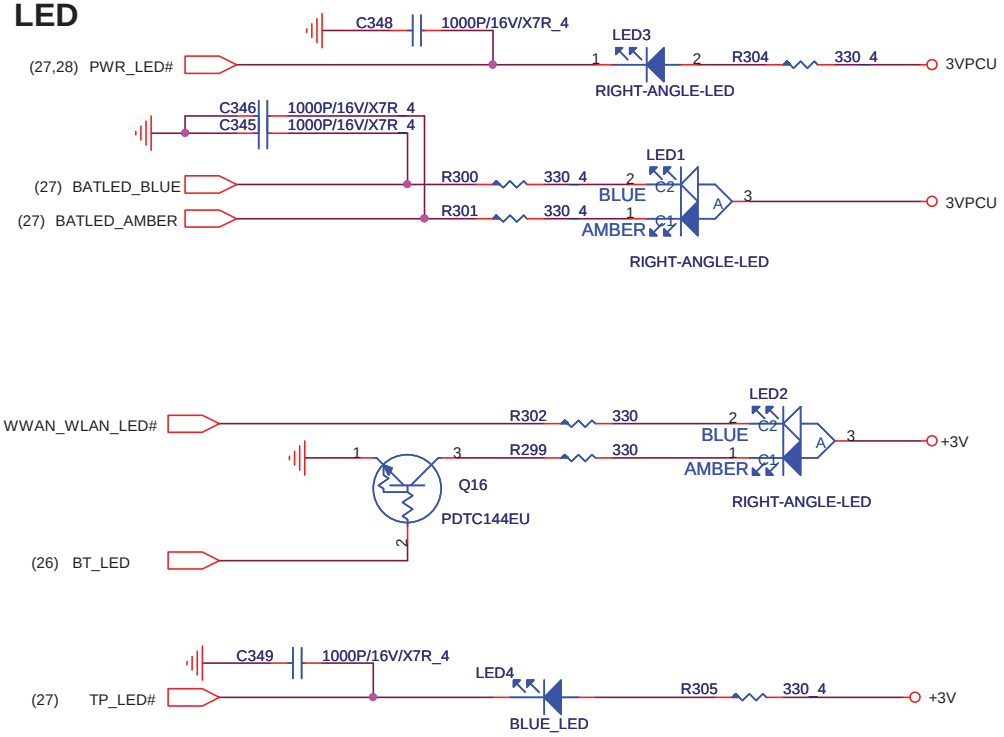


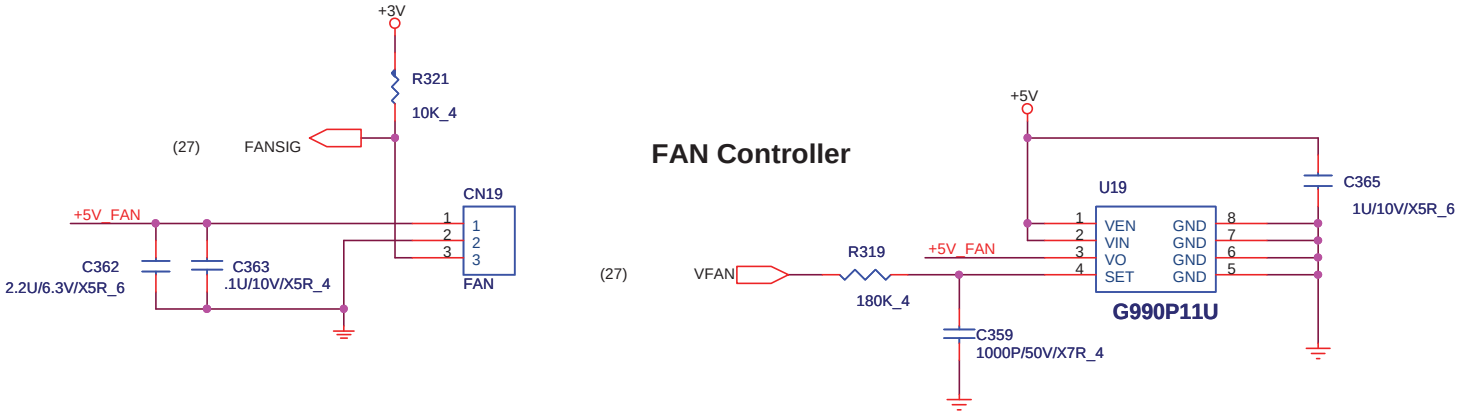
PROJECT : LL6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KB/TP/PW-B/FN-B	1A

Date: Wednesday, July 15, 2009 Sheet 28 of 36

LED





PROJECT : LL6		
Quanta Computer Inc.		
Size: Custom	Document Number: LED/FAN	Rev: 1A
Date: Wednesday, July 15, 2009	Sheet 29 of 36	

Hole for CPU support

HOLE7 *H-C142D142N
HOLE6 *H-C142D142N
HOLE8 *H-C142D142N
HOLE9 *H-C142D142N

North Bridge nut

HOLE4 H-C166D126P2NS
HOLE11 H-C166D126P2NS

HOLE17 *H-C276D106P2
HOLE18 *H-C276D106P2
HOLE19 *H-C276D106P2
HOLE5 *H-C276D106P2
HOLE1 *H-C276D106P2
HOLE3 *H-C276D106P2
HOLE10 *H-C276D106P2

HOLE12 *H-C315D220P2
HOLE13 *H-C315D220P2
HOLE15 *O-K46-1
HOLE14 *H-O551X354D394X197P2
HOLE2 *H-C87D87N
HOLE16 *H-C87D87N

WWAN nut

HOLE21 H-TC177BC79D79PT
HOLE23 H-TC177BC79D79PT

WLAN nut

HOLE20 H-TC236BC157D157PT
HOLE22 H-TC236BC157D157PT

For EMI

VIN
C30 *0.1u/25V/X5R_4
C456 *0.1u/25V/X5R_4
C334 *0.1u/25V/X5R_4
C514 *0.1u/25V/X5R_4
C451 *0.1u/25V/X5R_4
C5 *0.1u/25V/X5R_4

+5V_ODD
C179 *0.1U/10V/X5R_4

+1.05V
C133 *0.1U/10V/X5R_4

+3V
C244 *0.1U/10V/X5R_4

+5V
C308 *0.1U/10V/X5R_4
C319 *0.1U/10V/X5R_4
C335 *0.1U/10V/X5R_4
C250 *0.1U/10V/X5R_4

5V_S5
C288 *0.1U/10V/X5R_4

5V_S5
C342 *0.1U/10V/X5R_4

VIN
C196 *1000P/50V/X7R_4
C203 *1000P/50V/X7R_4
+5V_ODD

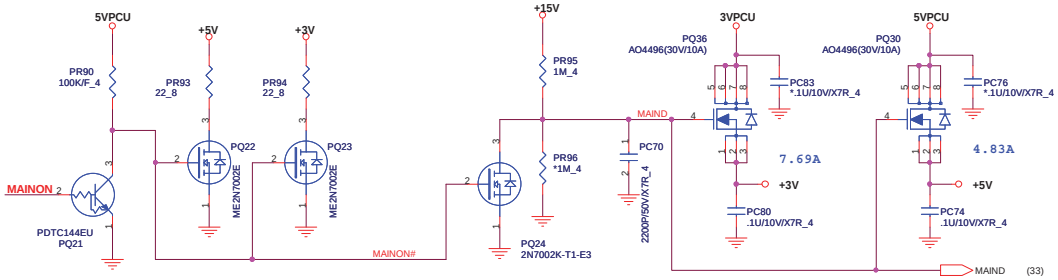
VIN
C475 *1000P/50V/X7R_4
+3V

PROJECT : LL6
Quanta Computer Inc.

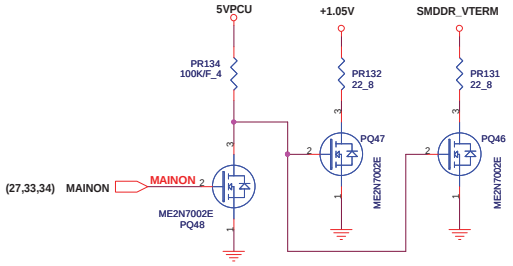
Size	Document Number	Rev
A	KB/TP/FAN/SCREW HOLE	1A
Date: Wednesday, July 15, 2009	Sheet 30 of 36	

DISCHARGE

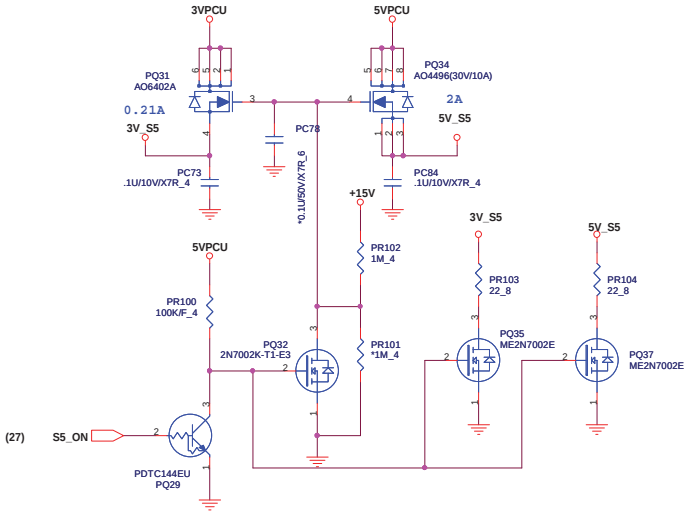
+3V, +5V



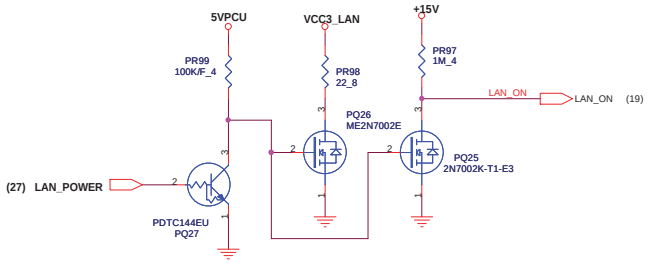
+1.05V, SMDDR_VTERM



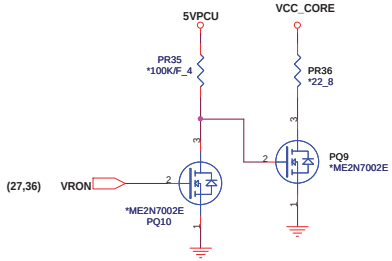
3V_S5, 5V_S5



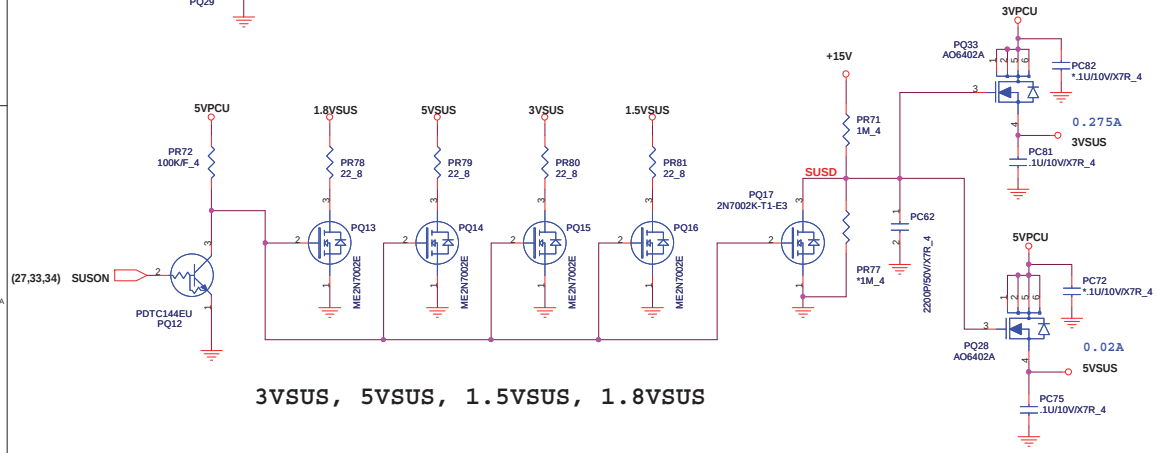
LANVCC



VCC_CORE



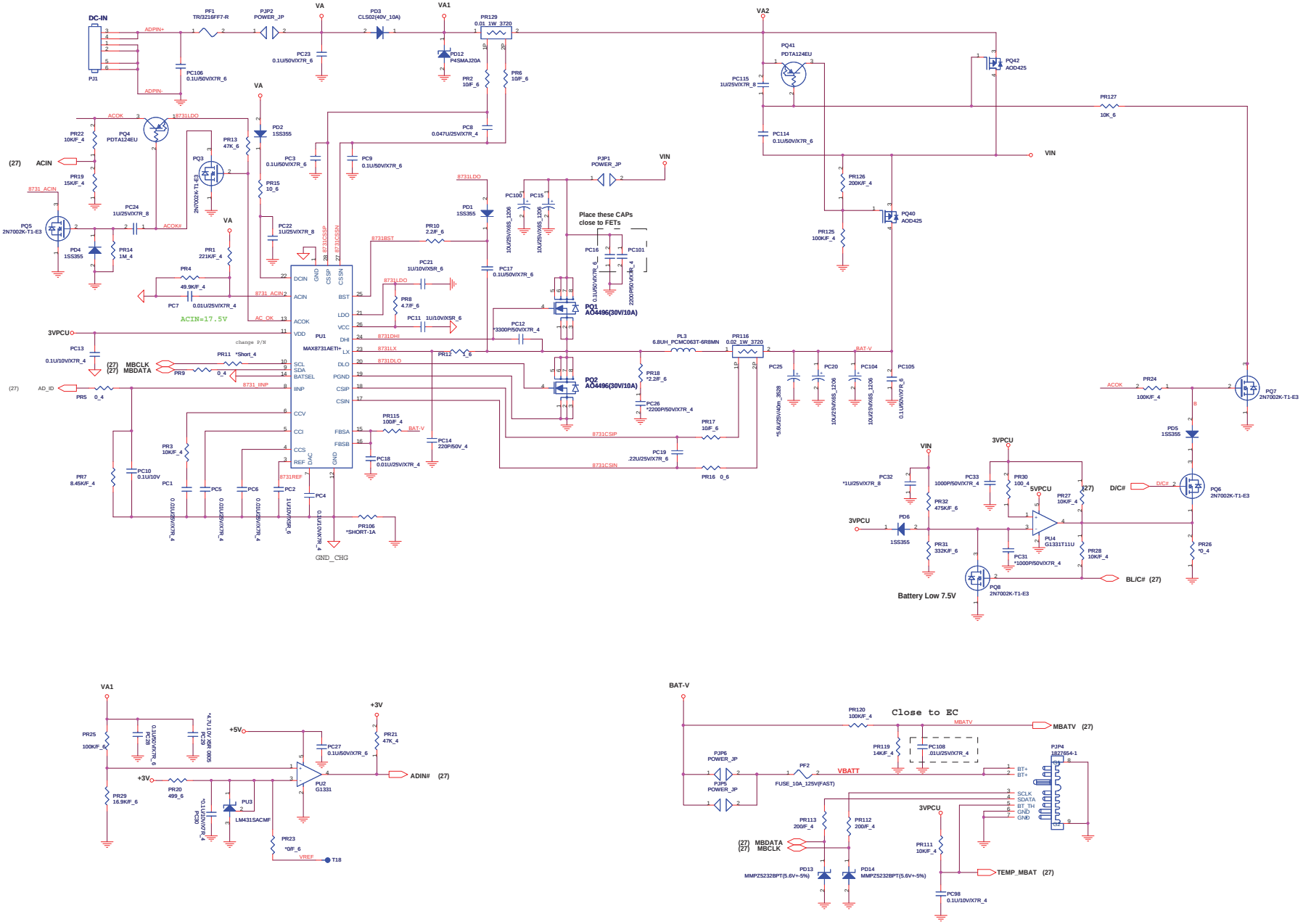
3VSUS, 5VSUS, 1.5VSUS, 1.8VSUS



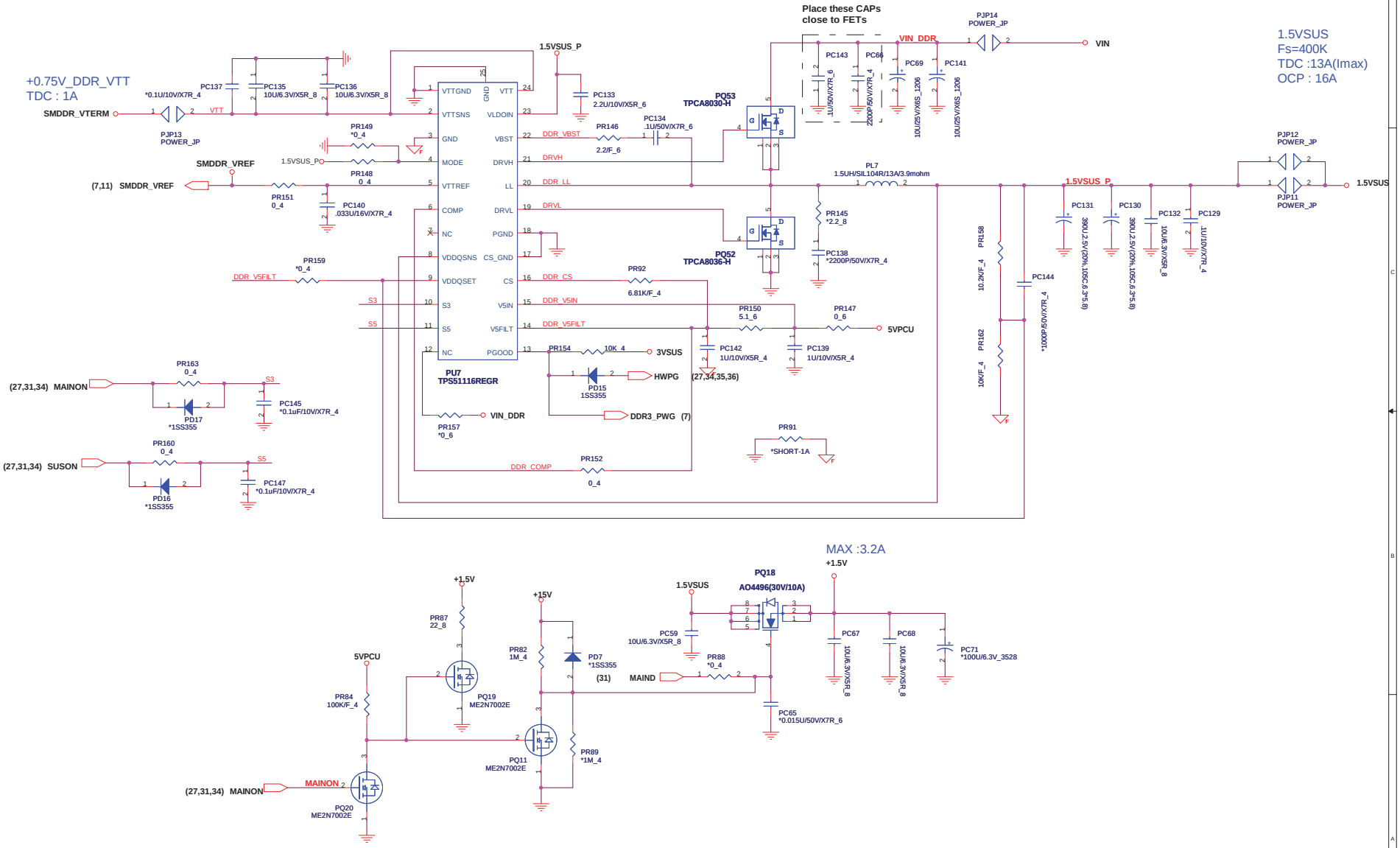
PROJECT : LL6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Discharge	2A

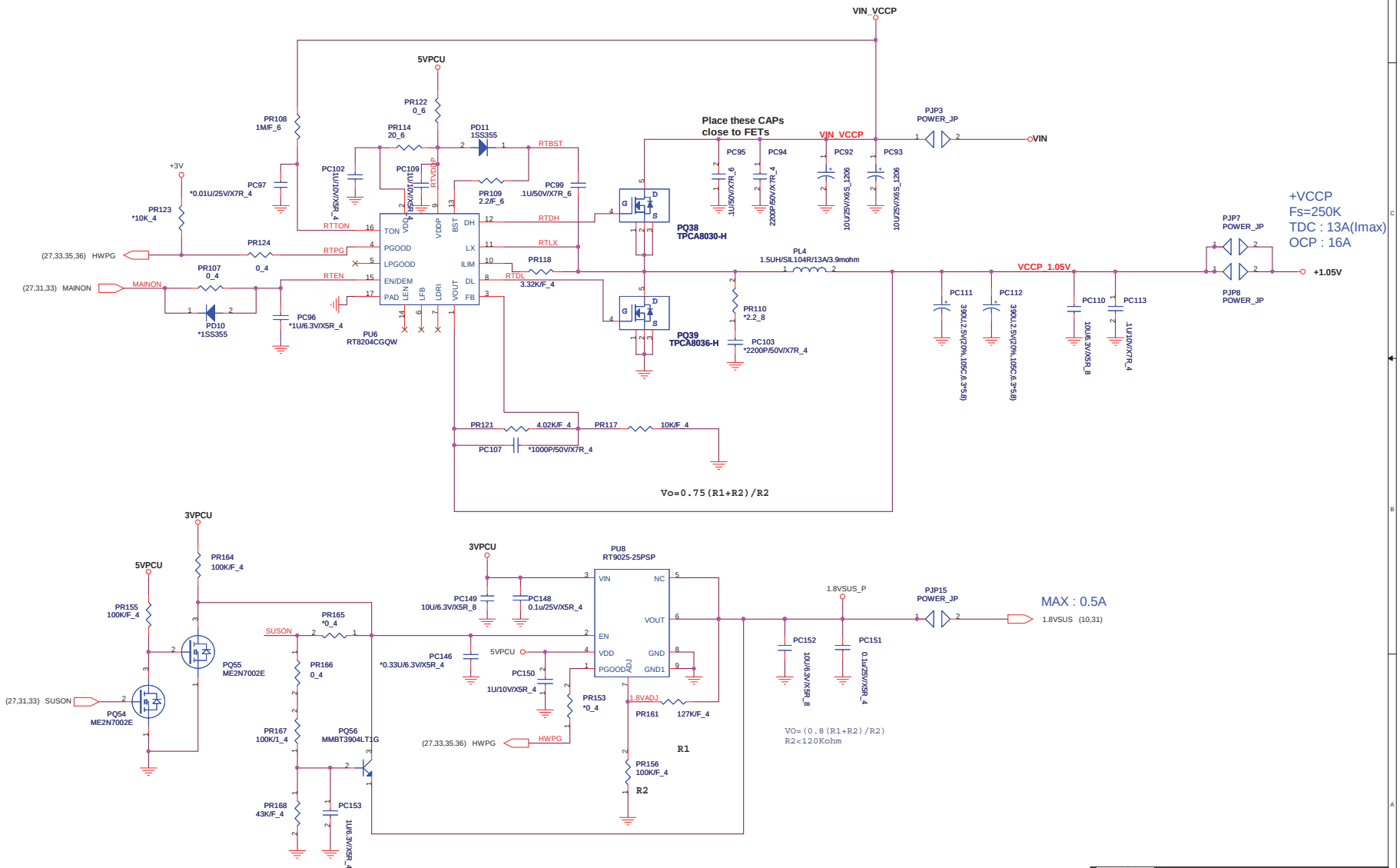
Date: Wednesday, July 15, 2009 Sheet 31 of 36



PROJECT : LL6			
Quanta Computer Inc.			
Size: Custom	Document Number: Charger (MAX8731A)		Rev: 2A
Date: Wednesday, July 15, 2009	Sheet 32 of 36		



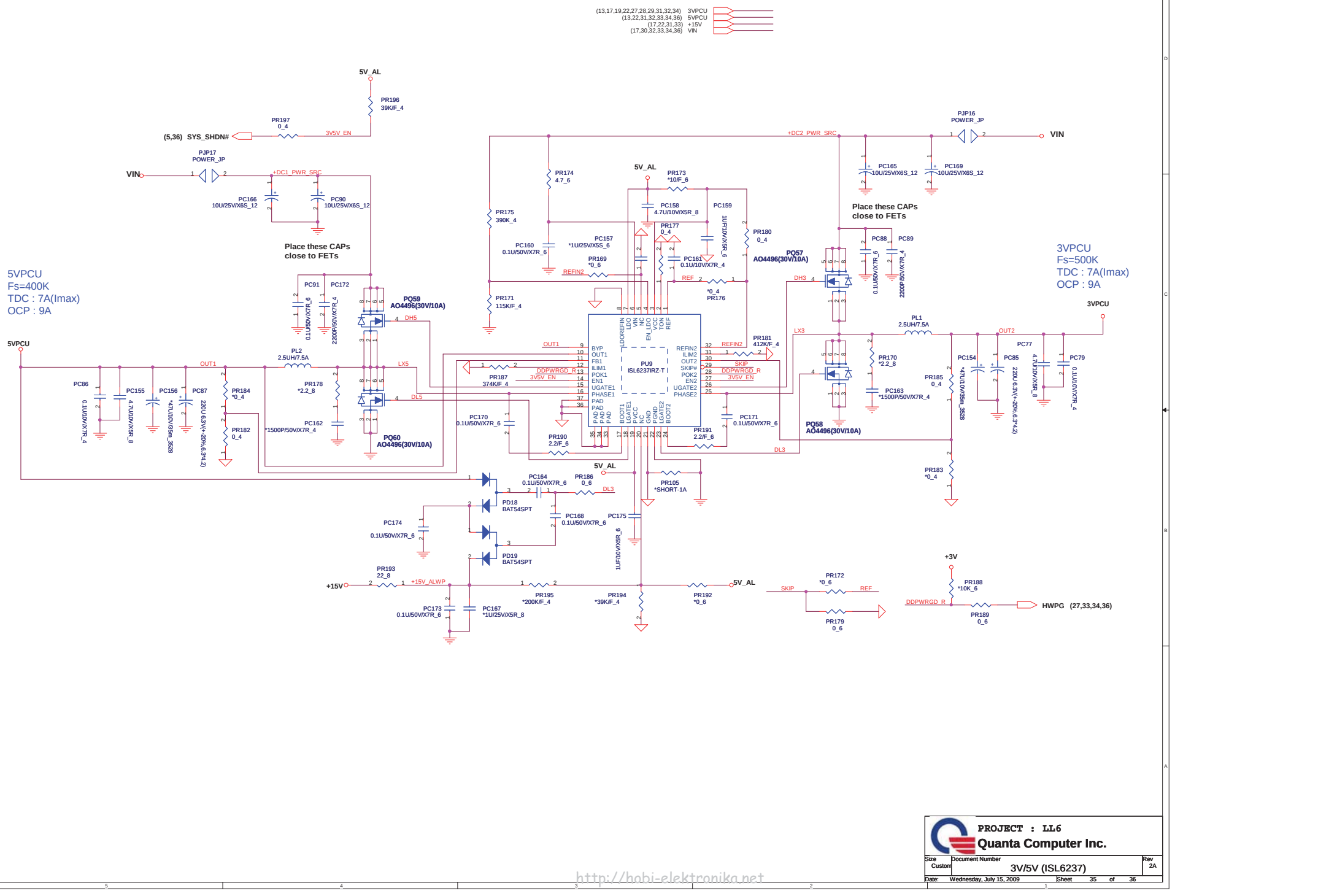
PROJECT : LL6			
Quanta Computer Inc.			
Size: Custom	Document Number: DDR3 (TPS51116REGR)		Rev: 2A
Date: Wednesday, July 15, 2009	Sheet 33 of 36		



PROJECT : LL6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	1.0V / 1.5V (RT8204)	2A

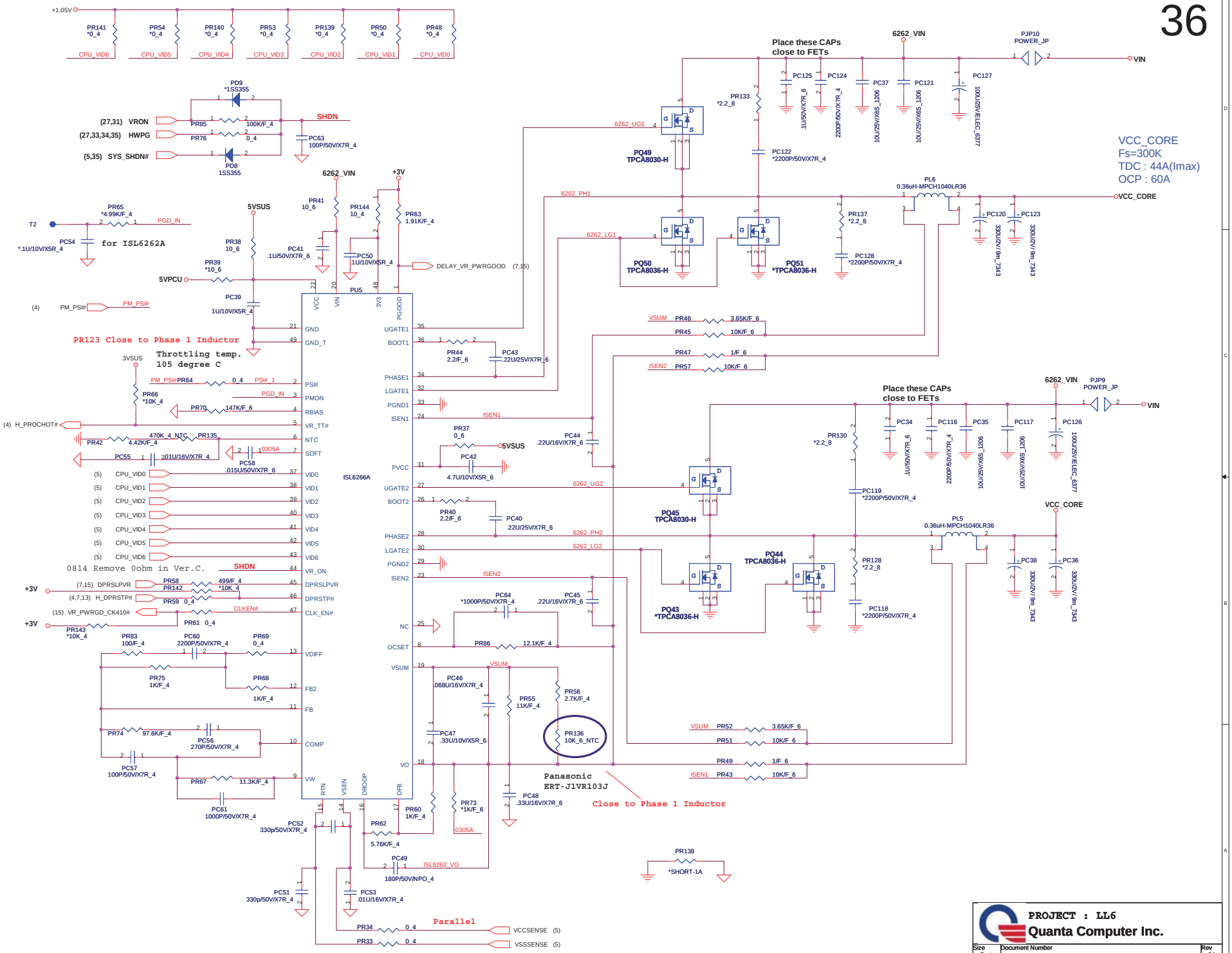
Date: Wednesday, July 15, 2009 Sheet 34 of 36



PROJECT : LL6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	3V/5V (ISL6237)	2A

Date: Wednesday, July 15, 2009 Sheet 35 of 36



PROJECT : LL6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CPU (ISL6266A)	2A

Date: Wednesday, July 15, 2009 Sheet 36 of 36