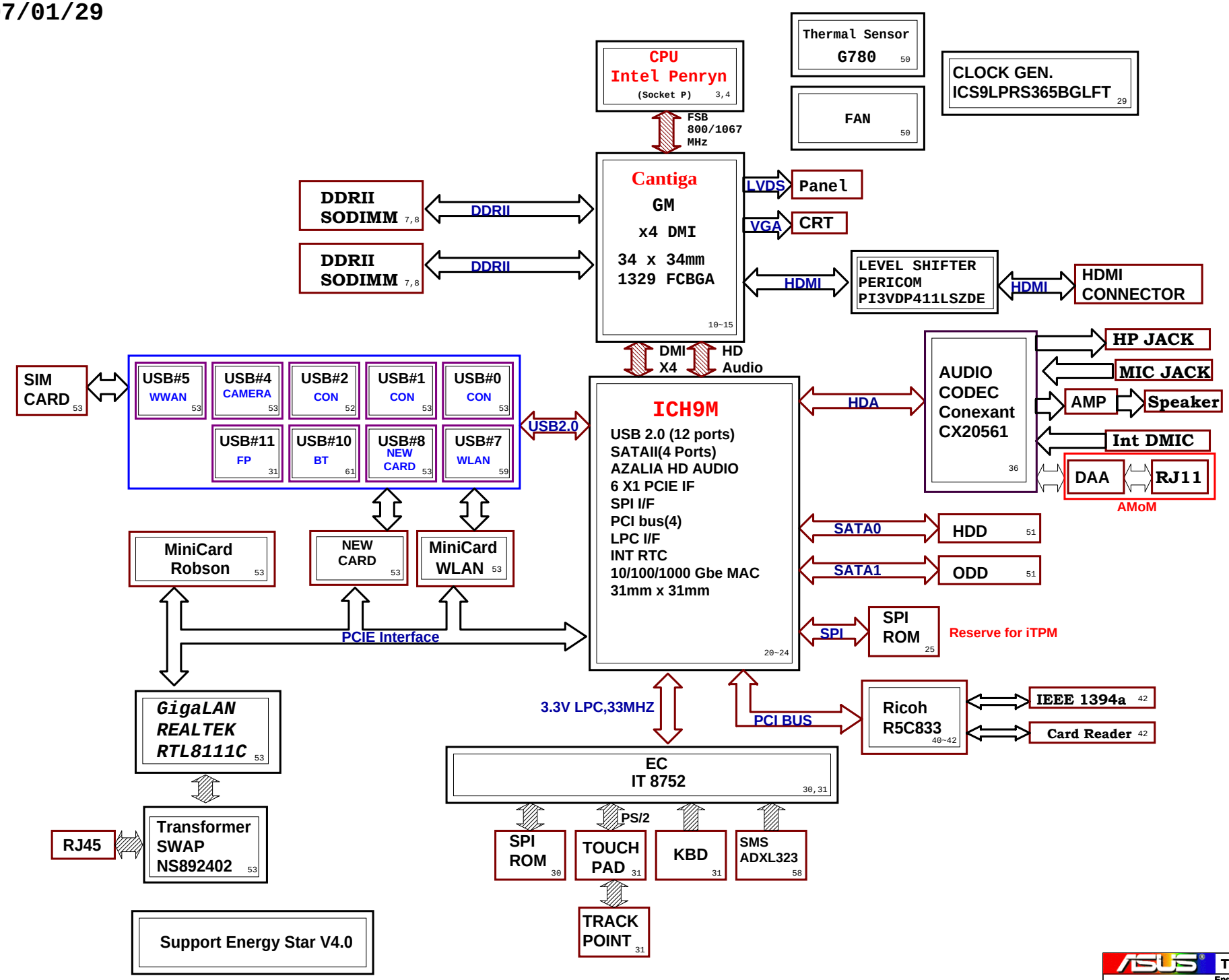
B3 NOTE 13" UMA Block Diagram
2007/01/29



Title : Block Diagram
Engineer: Peter Lo
Size C | Project Name Rocky30 | Rev 1.0
Date: Tuesday, January 29, 2008 | Sheet 1 of 94

Rocky30 Schematic Index

Page	System page Ref.
01	Block Diagram
02	Schematic Information
03-05	CPU-Penryn
07-09	DDR3 SO-DIMM
10-15	Cantiga
20-24	ICH9M
25	SPI ROM
29	CLK-ICS9LPR365
30-31	EC_IT8752
32	POWER-ON SEQUENCE
33	*
34	*
35	*
36	AUD_CODEC CX20561
37	AUDIO_AMP-G1431F2U & HP
38	MICROPHONE & LINE-IN-R01
39	*
40	CARDBUS R5C833(PCI I/F)
41	CARDBUS R5C833(1394 & SD)
42	IEEE1394A & CardReader
43	*
44	Debug
45	CRT
46	LVDS & INVERTER CONNECTOR
48	HDMI
50	THER SENSOR & FAN
51	HDD & CDROM
52	USB Port
53	IO Board
54	*
56	LED&PWRSW
57	DISCHARGE
58	SMS
59	MINI CARD-WLAN
60	DC-IN & BATTERY CONN
61	Blue Tooth
62	*
65	MDC NUT & Hinksink NUT
66	*
69	POWER_ON SEQUENCE
70-75	*
79	History
80	POWER_VCORE
81	POWER_SYSTEM
82	POWER_I/O_1.8VS
83	POWER_I/O_DDR_VCCP
84	PWR_-****
85	PWR_VGA(Empty)
86	PWR_-****
87	PWR-SHUTDOWN#(Empty)
88	PWR_CHARGER
89	TFT-LCD DRIVE(Empty)
90	PWR_DETECT
91	PWR_LOAD SWITCH
92	PWR_PROTECT
93	PWR_SIGNAL
94	PWR_FLOWCHART

ICH9-M GPIO	Use As	Signal Name	Power
GPIO 00	GPI	PM_SYNC#	+3VS
GPIO 01	GPI	-	+3VS
GPIO [2:5]	GPI	PCI_INT[E:H]#	+3VS
GPIO 06	GPI		+3VS
GPIO 07	GPI		+3VS
GPIO 08	GPI	EXT_SMI#	+3VSUS
GPIO 09	Native	UWB_ON	+3VSUS
GPIO 10	GPI	-	+3VSUS
GPIO 11	Native	EXT_SCI#	+3VSUS
GPIO 12	GPO	-	+3VSUS
GPIO 13	GPI	CB_SD#	+3VSUS
GPIO 14	GPI	RTLAN_DSM#	+3VSUS
GPIO 15	Native	-	+3VSUS
GPIO 16	Native	PM_DPRSLPVR	+3VS
GPIO 17	GPI	WLAN_LED	+3VS
GPIO 18	GPO		+3VS
GPIO 19	GPI	-	+3VS
GPIO 20	GPO	-	+3VS
GPIO 21	GPI	-	+3VS
GPIO 22	GPI	BT_DET#	+3VS
GPIO 23	Native	-	+3VS
GPIO 24	GPO	WLAN_ON	+3VSUS
GPIO 25	Native	-	+3VSUS
GPIO 26	Native	-	+3VSUS
GPIO 27	GPO	BT_ON	+3VSUS
GPIO 28	GPO	-	+3VSUS
GPIO 29	Native	USB_OC5#	+3VSUS
GPIO 30	Native	USB_OC6#	+3VSUS
GPIO 31	Native	USB_OC7#	+3VSUS
GPIO 32	GPO	-	+3VS
GPIO 33	GPO	-	+3VS
GPIO 34	GPO	-	+3VS
GPIO 35	GPO	CLK_SATA_REQ#	+3VS
GPIO 36	GPI	GPIO36	+3VS
GPIO 37	GPI	PCB_ID0	+3VS
GPIO 38	GPI	PCB_ID1	+3VS
GPIO 39	GPI	PCB_ID2	+3VS
GPIO 40	Native	USB_OC1#	+3VSUS
GPIO 41	Native	USB_OC2#	+3VSUS
GPIO 42	Native	USB_OC3#	+3VSUS
GPIO 43	Native	USB_OC4#	+3VSUS
GPIO 44	Native	USB_OC8#	N/A
GPIO 45	Native	USB_OC9#	N/A
GPIO 46	Native	USB_OC10#	N/A
GPIO 47	Native	USB_OC11#	N/A
GPIO 48	GPI	-	+3VS
GPIO 49	GPO	HDCP_EEPROM_PROTECT#	**+3VS**
GPIO 50	Native	PCI_REQ#1	+3VS
GPIO 51	Native	-	+3VS
GPIO 52	Native	PCI_REQ#2	+3VS
GPIO 53	Native	-	+3VS
GPIO 54	Native	PCI_REQ#3	+3VS
GPIO 55	Native	-	+3VS
GPIO 56	GPI	-	+3VSUS
GPIO 57	GPI	-	+3VSUS
GPIO 58	GPI	-	+3VSUS
GPIO 59	Native	USB_OC0#	+3VSUS
GPIO 60	Native	RTLAN_DSM_EN	+3VSUS

EC GPIO	Use As	Signal Name	Power
GPA0	GPO	PWR_LED#	
GPA1	GPO	CHG_LED#	
GPA2	GPO	BATSEL_3S#	
GPA3	-	NOVO_CARE_LED#	
GPA4	GPO	LCD_BL_PWM	
GPA5	GPO	FAN_PWM	
GPA6	GPO	-	
GPA7	GPO	-	
GPB0	GPO	CHG_EN#	
GPB1	GPO	PRECHG	
GPB2	GPI	-	
GPB3	ALT	SMB0_CLK	
GPB4	ALT	SMB0_DAT	
GPB5	OD	A20GATE	
GPB6	OD	RCIN#	
GPB7	GPO	PM_RSMRST#	
GPC0	GPI	-	
GPC1	ALT	SMB1_CLK	
GPC2	ALT	SMB1_DAT	
GPC3	GPO	PM_PWRBTN#	
GPC4	ALT	AC_IN_OC#	
GPC5	GPO	OP_SD#	
GPC6	ALT	BAT1_IN_OC#	
GPC7	GPO	RFON_SW#	
GPD0	GPI	PWRLIMIT#	
GPD1	ALT	PM_SUSC#	
GPD2	ALT	BUF_PLT_RST#	
GPD3	OD	EXT_SCI#	
GPD4	OD	EXT_SMI#	
GPD5	GPO	LCD_BACKOFF#	
GPD6	ALT	FAN0_TACH	
GPD7	GPI	-	
GPE0	GPO	VSUS_ON	
GPE1	GPO	SUSC_EC#	
GPE2	GPO	SUSB_EC#	
GPE3	GPO	CPU_VRON	
GPE4	ALT	PWR_SW#	
GPE5	ALT	-	
GPE6	GPI	LID_SW#	
GPE7	GPO	MEDIA_KEY#	
GPF0	GPI	-	
GPF1	GPI	NOVO_CARE#	
GPF2	ALT	TP1_CLK	
GPF3	ALT	TP1_DAT	
GPF4	ALT	TP_CLK	
GPF5	ALT	TP_DAT	
GPF6	GPO	THRO_CPU	
GPF7	GPO	SUSPEND_LED#	
GPG0	GPI	PM_THERM#_EC	
GPG1	ALT	PM_SUSB#	
GPG2	GPO	BAT1_CNT2#	
-	-	-	
-	-	-	

EC GPIO	Use As	Signal Name	Power
-	-	-	
GPG6	GPO	-	
-	-	-	
GPH0	OD	PM_CLKRUN#	
GPH1	ALT	3G_ON#	
GPH2	ALT	LOGO_LED#	
GPH3	GPO	BAT_LEARN	
GPH4	GPO	-	
GPH5	GPO	NUM_LED#	
GPH6	GPO	CAP_LED#	
-	-	-	
GPI0	GPI	NV_OVERT#	
GPI1	GPI	SUS_PWRGD	
GPI2	GPI	ALL_SYSTEM_PWRGD	
GPI3	GPI	VRM_PWRGD	
GPI4	GPI	XOUT	
GPI5	GPI	YOUT	
GPI6	GPI	-	
GPI7	GPI	-	
GPJ0	GPO	EC_CLK_EN	
GPJ1	GPO	PM_PWROK	
GPJ2	GPI	-	
GPJ3	-	-	
GPJ4	GPO	BL_DA	
GPJ5	GPO	-	
GPK0	GPI	-	
GPK1	GPI	-	
GPK2	GPI	-	
GPK3	GPI	-	
GPK4	GPI	-	
GPK5	GPI	-	
GPL0	GPI	APS_PWR_CNT#	
GPL1	GPI	APS_ST#	
GPL2	GPO	USB_PWR_EN#	
GPL3	GPO	-	
GPL4	GPO	-	
GPL5	GPO	AC_ID	
GPL6	GPO	AC_65W	
GPL7	GPO	CHG_LOW_LED#	
GPK6	GPO	-	
GPK7	GPI	-	

ASUS

Title : Schematic Information

Engineer: Peter Lo

Size	Project Name	Rev
Custom	Rocky30	1.0

Date: Tuesday, January 15, 2008 Sheet 2 of 94

10 H_D#[63:0] H_D#[63:0]

10 H_A#[35:3] H_A#[35:3]

10 H_REQ#[4:0] H_REQ#[4:0]

Reserved for the S3 reboot issue

U0301A

ADDR GROUP 0

ADDR GROUP 1

CONTROL

XDP/ITP SIGNALS

THERMAL

H CLK

RESERVED

SOCKET478BR

Place Series Resistor on H_CPURST# Without Stub

Comp0,2 connect with Zo=27.4 ohm, make trace length shorter than 0.5". Comp 1,3 connect with Z0=55 ohm, make trace length shorter than 0.5".

Zo=55 ohm, 0.5" max for GTLREF

U0301B

DATA GRP 0

DATA GRP 2

DATA GRP 1

DATA GRP 3

MISC

SOCKET478BR

BCLK	FSB	BSEL2	BSEL1	BSEL0
166	667	L	H	H
200	800	L	H	L
266	1067	L	L	L

Place R0304 & R0306 for XDP function

Default Strapping When Not Used

+VCCP_CPU

XDP_BPM#1 R0301 54.9Ohm 1% @

H_PREQ# R0302 54.9Ohm 1%

H_TDI R0303 54.9Ohm 1%

H_TDO R0304 54.9Ohm 1% @

H_TMS R0305 54.9Ohm 1%

H_DBR# R0306 1KOhm 1% @ +3VS

H_TCK R0307 54.9Ohm 1%

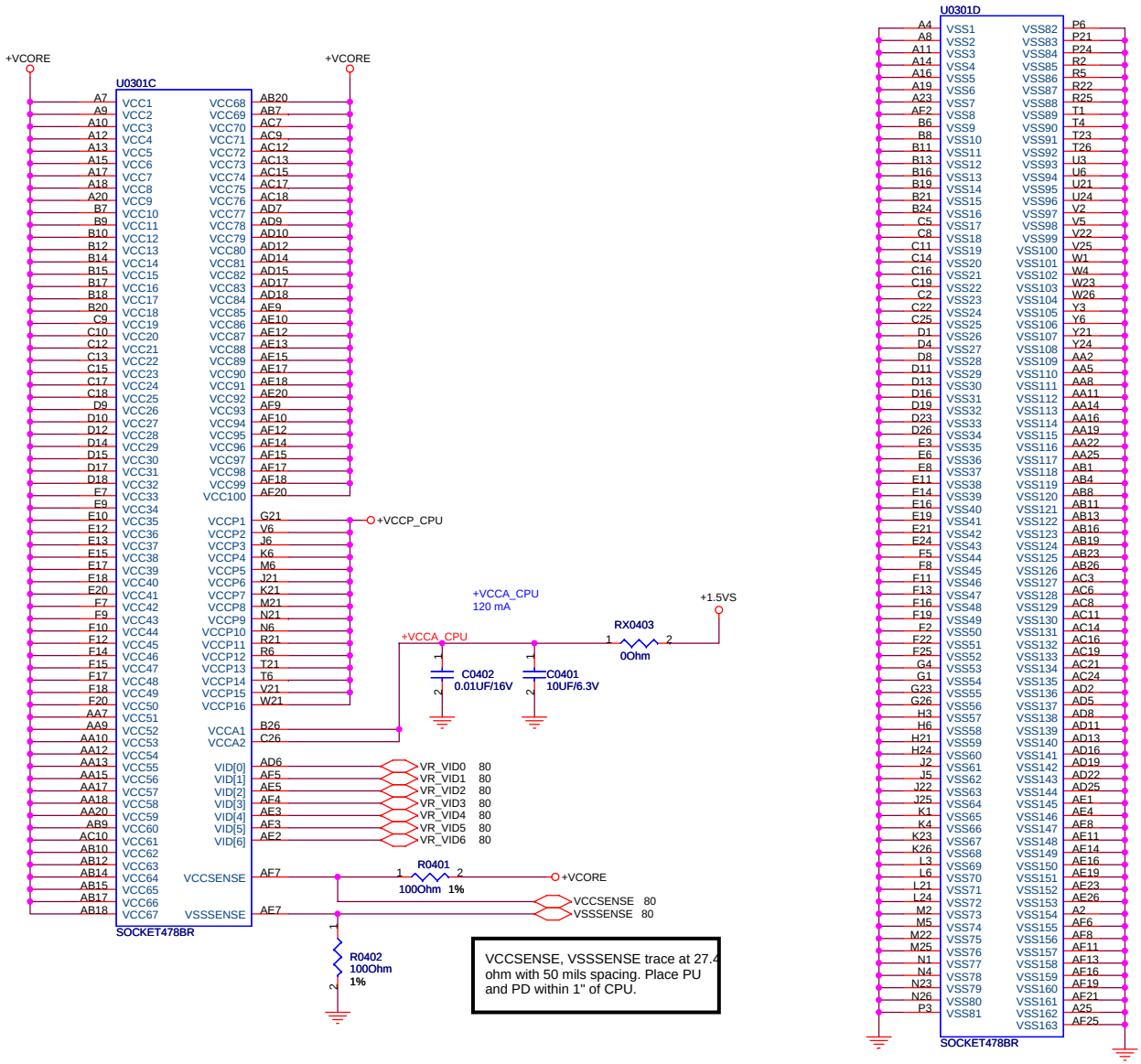
H_TRST# R0308 54.9Ohm 1%

Title : Penryn CPU (1)

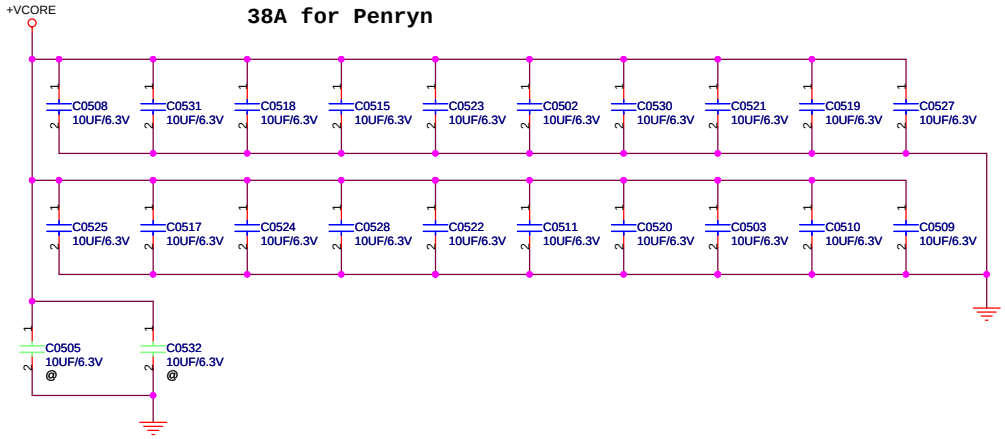
Engineer: Peter Lo

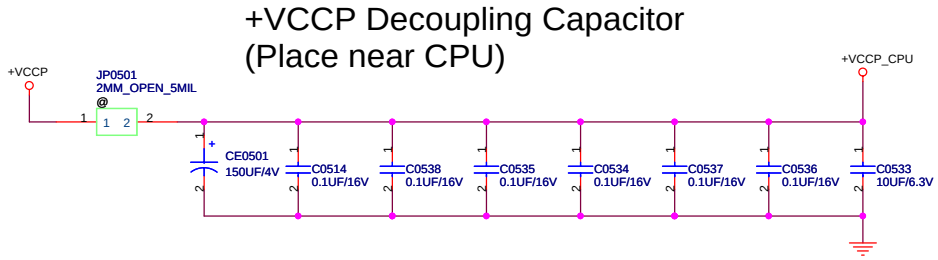
Size: Custom | Project Name: Rocky30 | Rev: 1.0

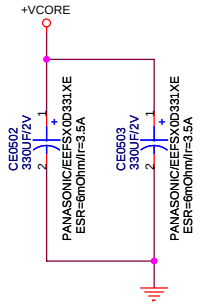
Date: Monday, February 04, 2008 | Sheet 3 of 94

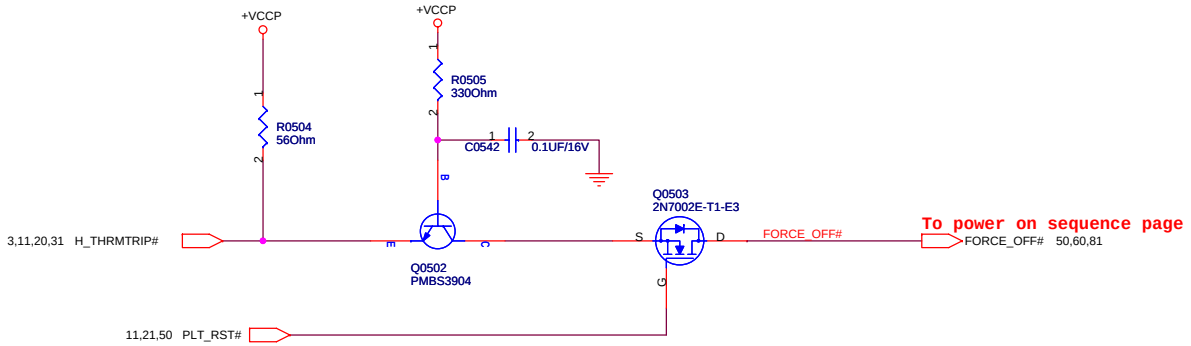


Title : Penryn CPU (2)		
Engineer: Peter Lo		
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 4 of 94	





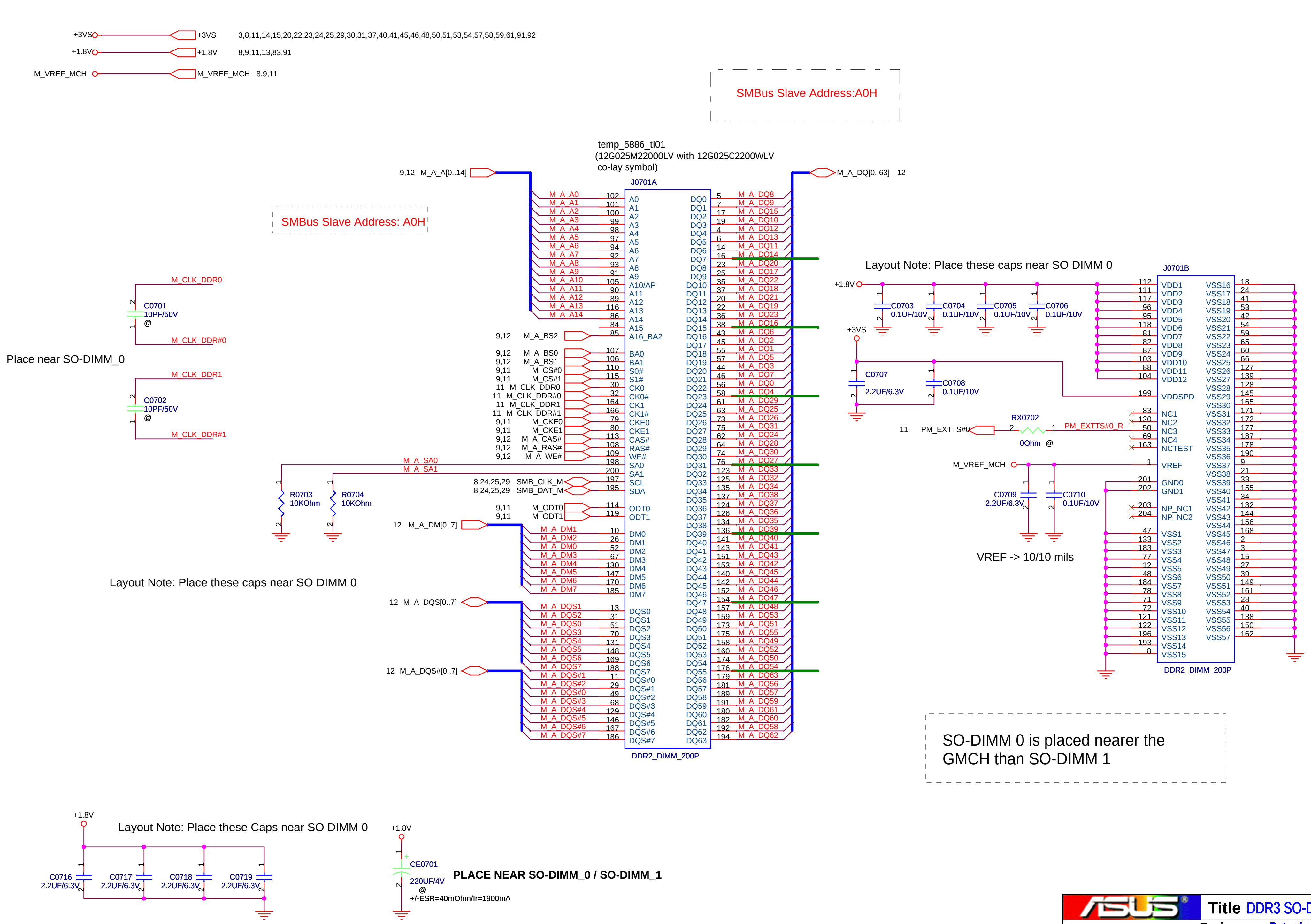




Thermal Trip signal(From CPU to ICH-9M and sequence)

Title : CPU CAPS		
Engineer: Peter Lo		
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 5 of 94	

Title :		
Engineer: *Peter Lo*		
Size: A	Project Name: **Rocky30**	Rev: 1.0
Date: Thursday, October 18, 2007	Sheet 6 of 94	


+3VS 3,8,11,14,15,20,22,23,24,25,29,30,31,37,40,41,45,46,48,50,51,53,54,57,58,59,61,91,92
+1.8V 8,9,11,13,83,91
M_VREF_MCH 8,9,11
SMBus Slave Address:A0H
SMBus Slave Address: A0H
temp_5886_tl01
(12G025M22000LV with 12G025C2200WLV
co-lay symbol)
J0701A
9,12 M_A_A[0..14]
M_A_DQ[0..63] 12
M_A_A0 102 A0; M_A_A1 101 A1; M_A_A2 100 A2; M_A_A3 99 A3; M_A_A4 98 A4; M_A_A5 97 A5; M_A_A6 94 A6; M_A_A7 92 A7; M_A_A8 93 A8; M_A_A9 91 A9; M_A_A10 105 A10/AP; M_A_A11 90 A11; M_A_A12 89 A12; M_A_A13 116 A13; M_A_A14 86 A14; 84 A15
9,12 M_A_BS2 85 A16_BA2
9,12 M_A_BS0 107 BA0; 9,12 M_A_BS1 106 BA1; 9,11 M_CS#0 110 S0#; 9,11 M_CS#1 115 S1#
11 M_CLK_DDR0 30 CK0; 11 M_CLK_DDR#0 32 CK0#; 11 M_CLK_DDR1 164 CK1; 11 M_CLK_DDR#1 166 CK1#
9,11 M_CKE0 79 CKE0; 9,11 M_CKE1 80 CKE1; 9,12 M_A_CAS# 113 CAS#; 9,12 M_A_RAS# 108 RAS#; 9,12 M_A_WE# 109 WE#
M_A_SA0 198 SA0; M_A_SA1 200 SA1
8,24,25,29 SMB_CLK_M 197 SCL; 8,24,25,29 SMB_DAT_M 195 SDA
9,11 M_ODT0 114 ODT0; 9,11 M_ODT1 119 ODT1
12 M_A_DM[0..7]
M_A_DM1 10 DM0; M_A_DM2 26 DM1; M_A_DM0 52 DM2; M_A_DM3 67 DM3; M_A_DM4 130 DM4; M_A_DM5 147 DM5; M_A_DM6 170 DM6; M_A_DM7 185 DM7
12 M_A_DQS[0..7]
M_A_DQS1 13 DQS0; M_A_DQS2 31 DQS1; M_A_DQS0 51 DQS2; M_A_DQS3 70 DQS3; M_A_DQS4 131 DQS4; M_A_DQS5 148 DQS5; M_A_DQS6 169 DQS6; M_A_DQS7 188 DQS7
12 M_A_DQS#[0..7]
M_A_DQS#1 11 DQS#0; M_A_DQS#2 29 DQS#1; M_A_DQS#0 49 DQS#2; M_A_DQS#3 68 DQS#3; M_A_DQS#4 129 DQS#4; M_A_DQS#5 146 DQS#5; M_A_DQS#6 167 DQS#6; M_A_DQS#7 186 DQS#7
DQ0 5 M_A_DQ8; DQ1 7 M_A_DQ9; DQ2 17 M_A_DQ15; DQ3 19 M_A_DQ10; DQ4 4 M_A_DQ12; DQ5 6 M_A_DQ13; DQ6 14 M_A_DQ11; DQ7 16 M_A_DQ14
DQ8 23 M_A_DQ20; DQ9 25 M_A_DQ17; DQ10 35 M_A_DQ22; DQ11 37 M_A_DQ18; DQ12 20 M_A_DQ21; DQ13 22 M_A_DQ19; DQ14 36 M_A_DQ23; DQ15 38 M_A_DQ16
DQ16 43 M_A_DQ6; DQ17 45 M_A_DQ2; DQ18 55 M_A_DQ1; DQ19 57 M_A_DQ5; DQ20 44 M_A_DQ3; DQ21 46 M_A_DQ7; DQ22 56 M_A_DQ0; DQ23 58 M_A_DQ4
DQ24 61 M_A_DQ29; DQ25 63 M_A_DQ25; DQ26 73 M_A_DQ26; DQ27 75 M_A_DQ31; DQ28 62 M_A_DQ24; DQ29 64 M_A_DQ28; DQ30 74 M_A_DQ30; DQ31 76 M_A_DQ27
DQ32 123 M_A_DQ33; DQ33 125 M_A_DQ32; DQ34 135 M_A_DQ34; DQ35 137 M_A_DQ38; DQ36 124 M_A_DQ37; DQ37 126 M_A_DQ36; DQ38 134 M_A_DQ35; DQ39 136 M_A_DQ39
DQ40 141 M_A_DQ40; DQ41 143 M_A_DQ41; DQ42 151 M_A_DQ43; DQ43 153 M_A_DQ42; DQ44 140 M_A_DQ45; DQ45 142 M_A_DQ44; DQ46 152 M_A_DQ46; DQ47 154 M_A_DQ47
DQ48 157 M_A_DQ48; DQ49 159 M_A_DQ53; DQ50 173 M_A_DQ51; DQ51 175 M_A_DQ55; DQ52 158 M_A_DQ49; DQ53 160 M_A_DQ52; DQ54 174 M_A_DQ50; DQ55 176 M_A_DQ54
DQ56 179 M_A_DQ63; DQ57 181 M_A_DQ56; DQ58 189 M_A_DQ57; DQ59 191 M_A_DQ59; DQ60 180 M_A_DQ61; DQ61 182 M_A_DQ60; DQ62 192 M_A_DQ58; DQ63 194 M_A_DQ62
DDR2_DIMM_200P
M_CLK_DDR0
C0701 10PF/50V @
M_CLK_DDR#0
Place near SO-DIMM_0
M_CLK_DDR1
C0702 10PF/50V @
M_CLK_DDR#1
R0703 10KOhm
R0704 10KOhm
Layout Note: Place these caps near SO DIMM 0
Layout Note: Place these caps near SO DIMM 0
+1.8V
C0703 0.1UF/10V
C0704 0.1UF/10V
C0705 0.1UF/10V
C0706 0.1UF/10V
+3VS
C0707 2.2UF/6.3V
C0708 0.1UF/10V
J0701B
112 VDD1; 111 VDD2; 117 VDD3; 96 VDD4; 95 VDD5; 118 VDD6; 81 VDD7; 82 VDD8; 87 VDD9; 103 VDD10; 88 VDD11; 104 VDD12
199 VDDSPD
83 NC1; 120 NC2; 50 NC3; 69 NC4; 163 NCTEST
11 PM_EXTTS#0
RX0702 0Ohm @
PM_EXTTS#0_R
M_VREF_MCH 1 VREF
C0709 2.2UF/6.3V
C0710 0.1UF/10V
201 GND0; 202 GND1
203 NP_NC1; 204 NP_NC2
47 VSS1; 133 VSS2; 183 VSS3; 77 VSS4; 12 VSS5; 48 VSS6; 184 VSS7; 78 VSS8; 71 VSS9; 72 VSS10; 121 VSS11; 122 VSS12; 196 VSS13; 193 VSS14; 8 VSS15
VSS16 18; VSS17 24; VSS18 41; VSS19 53; VSS20 42; VSS21 54; VSS22 59; VSS23 65; VSS24 60; VSS25 66; VSS26 127; VSS27 139; VSS28 128; VSS29 145; VSS30 165; VSS31 171; VSS32 172; VSS33 177; VSS34 187; VSS35 178; VSS36 190; VSS37 9; VSS38 21; VSS39 33; VSS40 155; VSS41 34; VSS42 132; VSS43 144; VSS44 156; VSS45 168; VSS46 2; VSS47 3; VSS48 15; VSS49 27; VSS50 39; VSS51 149; VSS52 161; VSS53 28; VSS54 40; VSS55 138; VSS56 150; VSS57 162
DDR2_DIMM_200P
VREF -> 10/10 mils
SO-DIMM 0 is placed nearer the
GMCH than SO-DIMM 1
+1.8V
Layout Note: Place these Caps near SO DIMM 0
C0716 2.2UF/6.3V
C0717 2.2UF/6.3V
C0718 2.2UF/6.3V
C0719 2.2UF/6.3V
+1.8V
CE0701 220UF/4V @
+/-ESR=40mOhm/Ir=1900mA
PLACE NEAR SO-DIMM_0 / SO-DIMM_1

Title DDR3 SO-DIMM_0

Engineer: Peter Lo

Size	Project Name	Rev
Custom	Rocky30	1.0

Date: Monday, February 04, 2008 Sheet 7 of 94

+3VS → +3VS 3,7,11,14,15,20,22,23,24,25,29,30,31,37,40,41,45,46,48,50,51,53,54,57,58,59,61,91,92

+1.8V → +1.8V 7,9,11,13,83,91

M_VREF_MCH → M_VREF_MCH 7,9,11

temp_5886_tl02
(12G025032005LV with 12G025022004LV
CO-LAY symbol)

9,12 M_B_A[0..14]

M_B_DQ[0..63] 12

SMBus Slave Address:A4H

J0801A

M_B_A0 M_B_A1 M_B_A2 M_B_A3 M_B_A4 M_B_A5 M_B_A6 M_B_A7 M_B_A8 M_B_A9 M_B_A10 M_B_A11 M_B_A12 M_B_A13 M_B_A14

9,12 M_B_BS2

9,12 M_B_BS0
9,12 M_B_BS1
9,11 M_CS#2
9,11 M_CS#3
11 M_CLK_DDR2
11 M_CLK_DDR#2
11 M_CLK_DDR3
11 M_CLK_DDR#3
9,11 M_CKE2
9,11 M_CKE3
9,12 M_B_CAS#
9,12 M_B_RAS#
9,12 M_B_WE#

M_B_SA0
R0804 10KOhm M_B_SA1
+3VS
R0803 10KOhm
7,24,25,29 SMB_CLK_M
7,24,25,29 SMB_DAT_M

9,11 M_ODT2
9,11 M_ODT3

12 M_B_DM[0..7]
M_B_DM0 M_B_DM1 M_B_DM3 M_B_DM2 M_B_DM5 M_B_DM4 M_B_DM6 M_B_DM7

12 M_B_DQS[0..7]
M_B_DQS0 M_B_DQS1 M_B_DQS3 M_B_DQS2 M_B_DQS5 M_B_DQS4 M_B_DQS6 M_B_DQS7

12 M_B_DQS#[0..7]
M_B_DQS#0 M_B_DQS#1 M_B_DQS#3 M_B_DQS#2 M_B_DQS#5 M_B_DQS#4 M_B_DQS#6 M_B_DQS#7

A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12 A13 A14 A15 A16_BA2
BA0 BA1 S0# S1# CK0 CK0# CK1 CK1# CKE0 CKE1 CAS# RAS# WE# SA0 SA1 SCL SDA
ODT0 ODT1
DM0 DM1 DM2 DM3 DM4 DM5 DM6 DM7
DQS0 DQS1 DQS2 DQS3 DQS4 DQS5 DQS6 DQS7
DQS#0 DQS#1 DQS#2 DQS#3 DQS#4 DQS#5 DQS#6 DQS#7
DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15 DQ16 DQ17 DQ18 DQ19 DQ20 DQ21 DQ22 DQ23 DQ24 DQ25 DQ26 DQ27 DQ28 DQ29 DQ30 DQ31 DQ32 DQ33 DQ34 DQ35 DQ36 DQ37 DQ38 DQ39 DQ40 DQ41 DQ42 DQ43 DQ44 DQ45 DQ46 DQ47 DQ48 DQ49 DQ50 DQ51 DQ52 DQ53 DQ54 DQ55 DQ56 DQ57 DQ58 DQ59 DQ60 DQ61 DQ62 DQ63

M_B_DQ0 M_B_DQ5 M_B_DQ4 M_B_DQ1 M_B_DQ7 M_B_DQ0 M_B_DQ6 M_B_DQ3 M_B_DQ2 M_B_DQ9 M_B_DQ8 M_B_DQ15 M_B_DQ14 M_B_DQ13 M_B_DQ12 M_B_DQ10 M_B_DQ11 M_B_DQ24 M_B_DQ25 M_B_DQ26 M_B_DQ27 M_B_DQ28 M_B_DQ29 M_B_DQ30 M_B_DQ31 M_B_DQ22 M_B_DQ23 M_B_DQ21 M_B_DQ19 M_B_DQ16 M_B_DQ18 M_B_DQ17 M_B_DQ20 M_B_DQ44 M_B_DQ41 M_B_DQ43 M_B_DQ46 M_B_DQ40 M_B_DQ45 M_B_DQ42 M_B_DQ47 M_B_DQ36 M_B_DQ33 M_B_DQ38 M_B_DQ35 M_B_DQ32 M_B_DQ34 M_B_DQ39 M_B_DQ37 M_B_DQ48 M_B_DQ53 M_B_DQ55 M_B_DQ49 M_B_DQ52 M_B_DQ54 M_B_DQ50 M_B_DQ51 M_B_DQ61 M_B_DQ60 M_B_DQ63 M_B_DQ57 M_B_DQ56 M_B_DQ59 M_B_DQ58 M_B_DQ62

DDR2_DIMM_200P

Place near SO-DIMM_1

M_CLK_DDR3 — C0801 10PF/50V @ — M_CLK_DDR#3

M_CLK_DDR2 — C0802 10PF/50V @ — M_CLK_DDR#2

+1.8V

Layout Note: Place these Caps near the SO-DIMM_1

C0816 2.2UF/6.3V C0817 2.2UF/6.3V C0818 2.2UF/6.3V C0819 2.2UF/6.3V

+1.8V

Layout Note: Place these Caps near SO DIMM 1

C0807 0.1UF/10V C0808 0.1UF/10V C0809 0.1UF/10V C0810 0.1UF/10V

+3VS

C0811 2.2UF/6.3V C0812 0.1UF/10V

11 PM_EXTTS#1

RX0802 @ 0Ohm

PM_EXTTS#1_R

M_VREF_MCH

C0821 2.2UF/6.3V C0820 0.1UF/10V

Layout Note: Place these Caps near SO DIMM 1

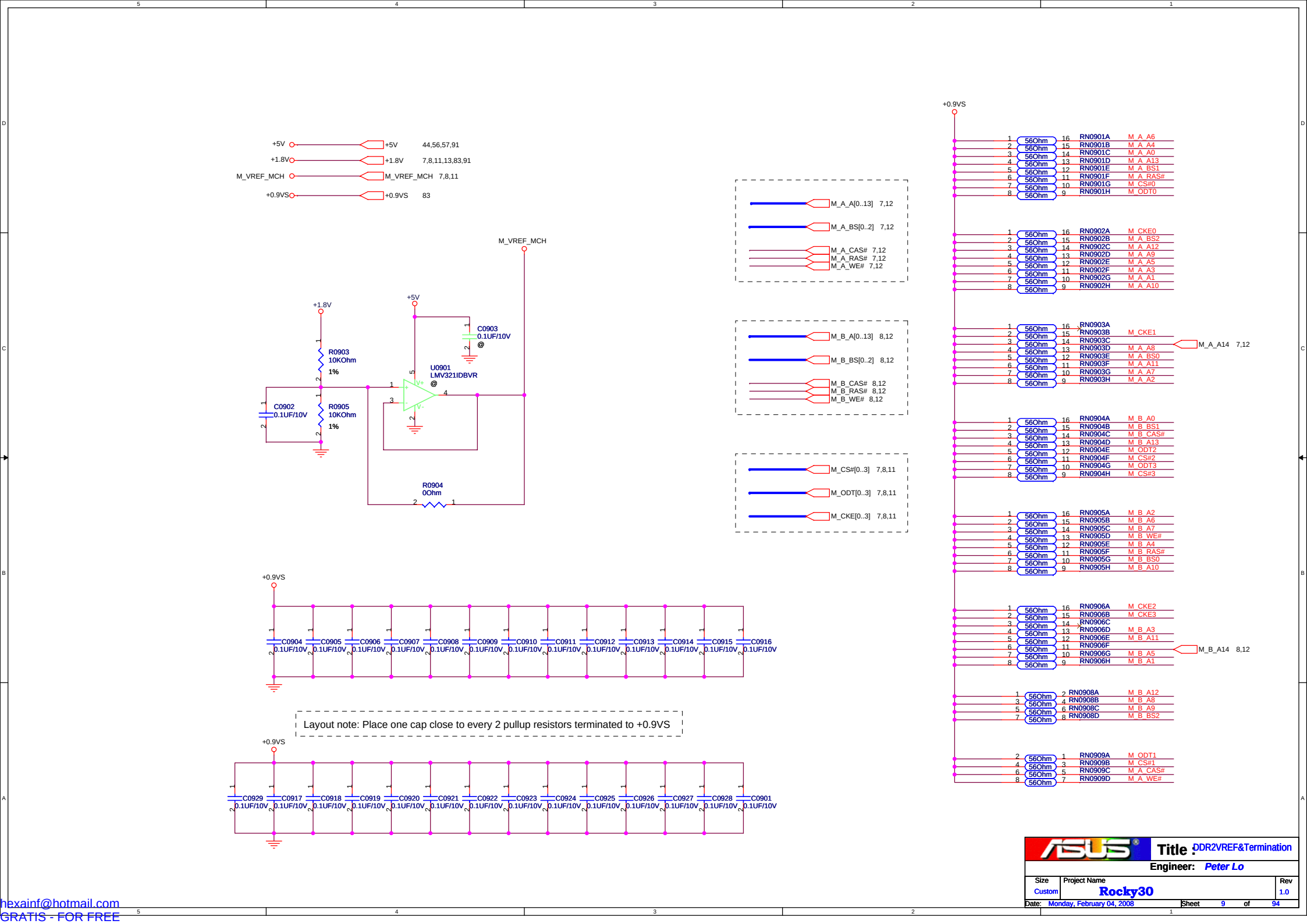
VREF -> 10/10 mils

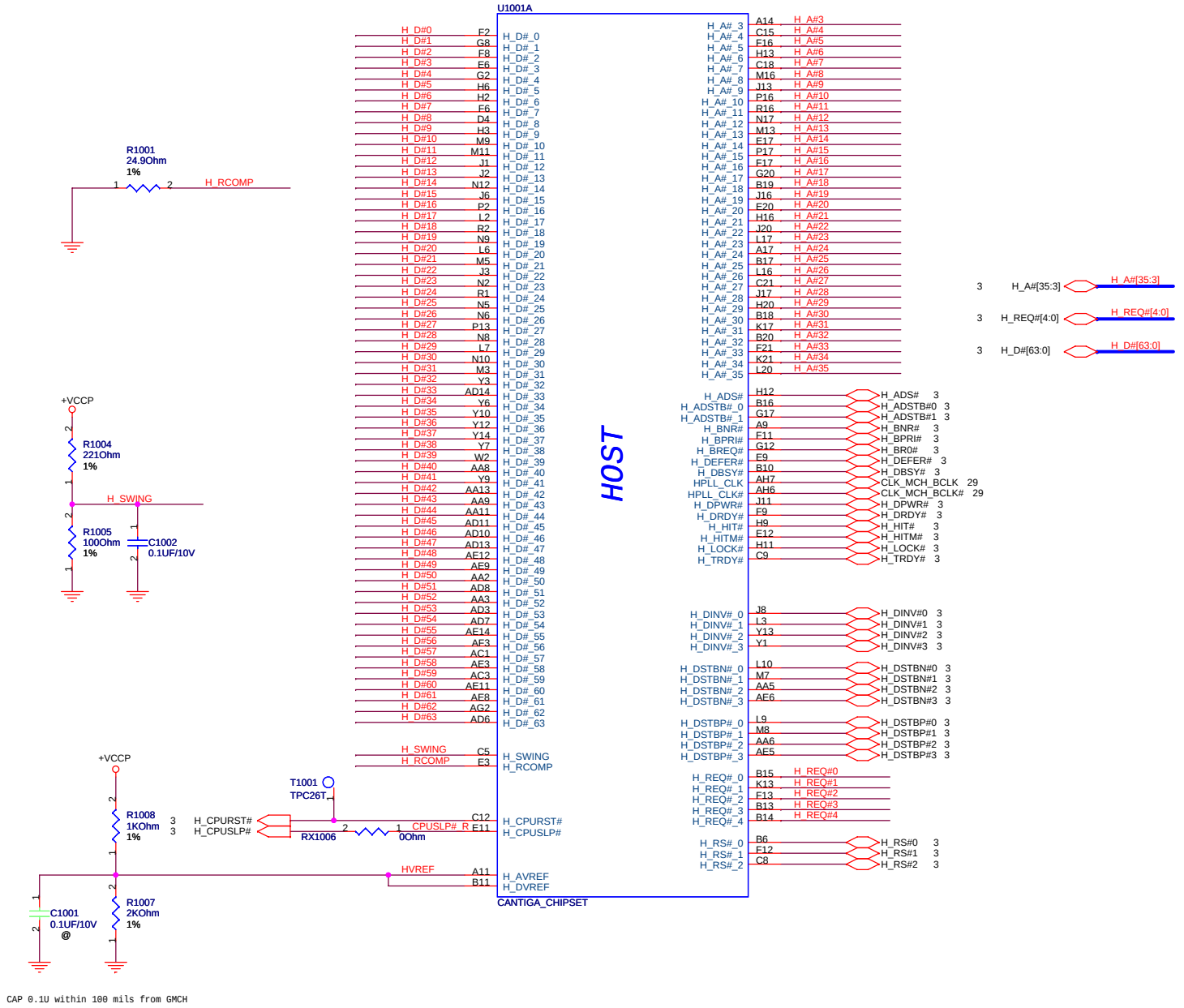
J0801B

VDD1 VDD2 VDD3 VDD4 VDD5 VDD6 VDD7 VDD8 VDD9 VDD10 VDD11 VDD12 VDDSPD NC1 NC2 NC3 NC4 NCTEST VREF GND0 GND1 NP_NC1 NP_NC2 VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 VSS8 VSS9 VSS10 VSS11 VSS12 VSS13 VSS14 VSS15 VSS16 VSS17 VSS18 VSS19 VSS20 VSS21 VSS22 VSS23 VSS24 VSS25 VSS26 VSS27 VSS28 VSS29 VSS30 VSS31 VSS32 VSS33 VSS34 VSS35 VSS36 VSS37 VSS38 VSS39 VSS40 VSS41 VSS42 VSS43 VSS44 VSS45 VSS46 VSS47 VSS48 VSS49 VSS50 VSS51 VSS52 VSS53 VSS54 VSS55 VSS56 VSS57

DDR2_DIMM_200P

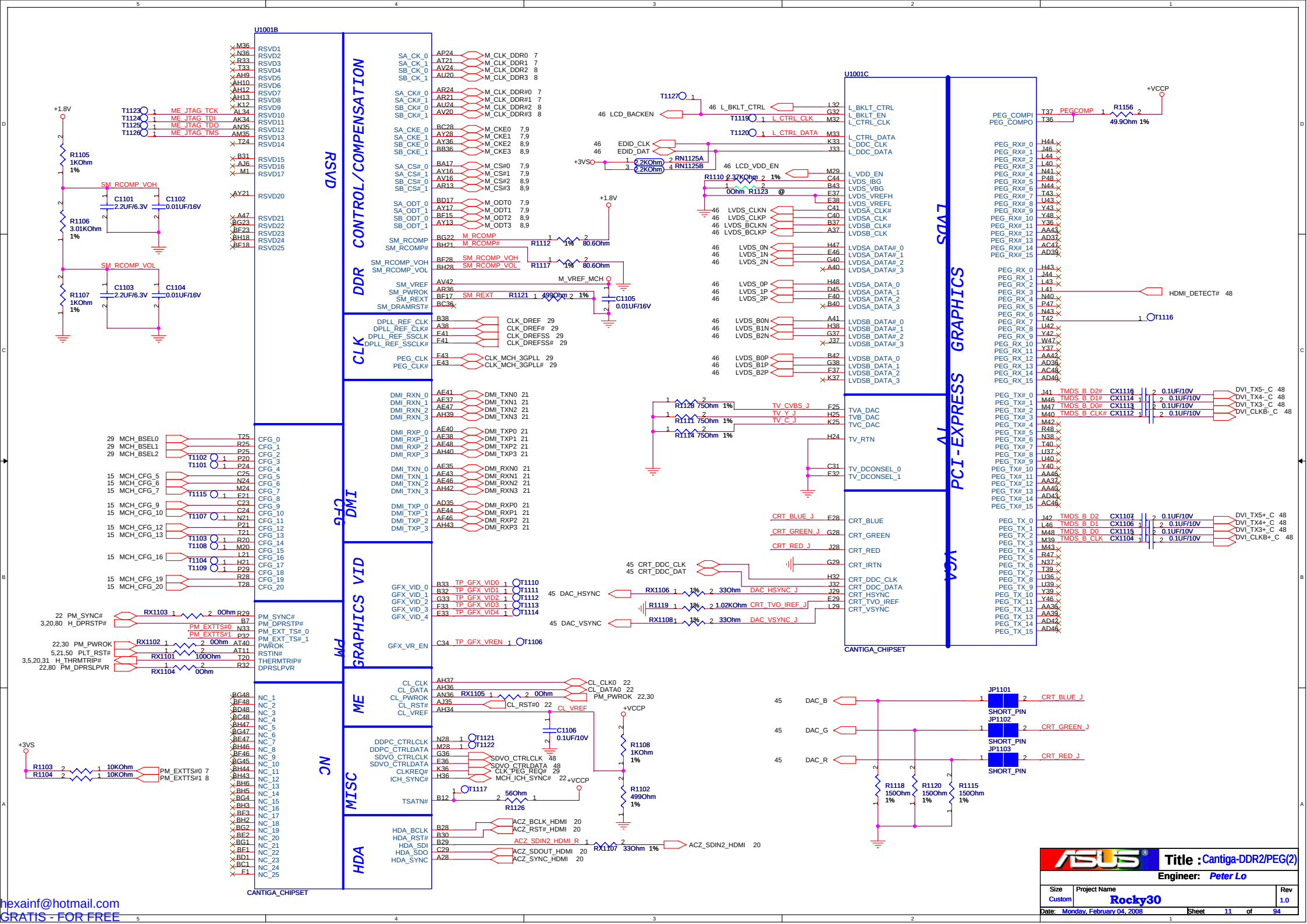
Title : DDR3 SO-DIMM_1		
Engineer: Peter Lo		
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 8 of 94	

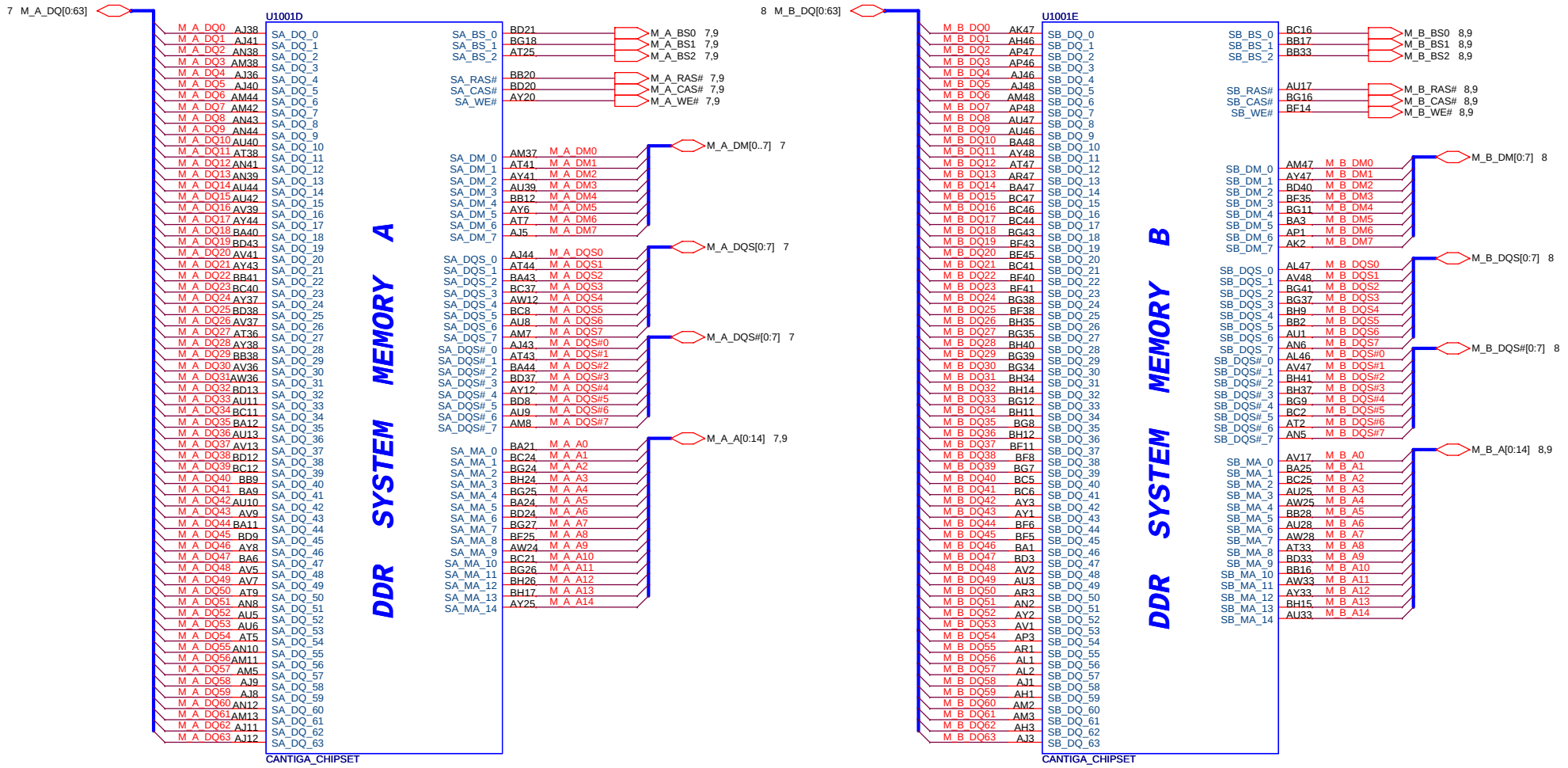




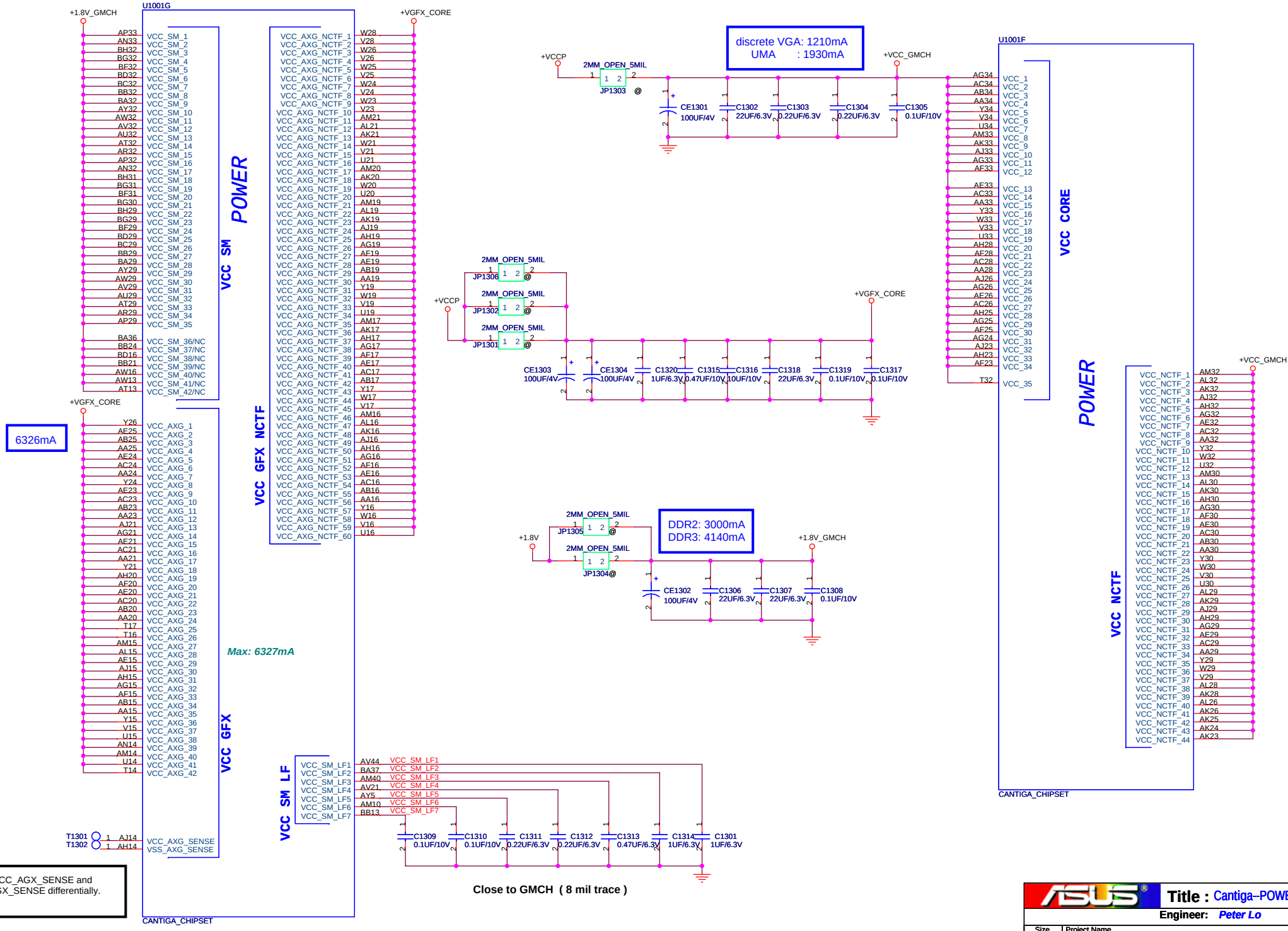
CAP 0.1U within 100 mils from GMCH

Title :	Cantiga -- CPU (1)
Engineer:	Peter Lo
Size	Custom
Project Name	Rocky30
Rev	1.0
Date:	Monday, February 04, 2008
Sheet	10 of 94

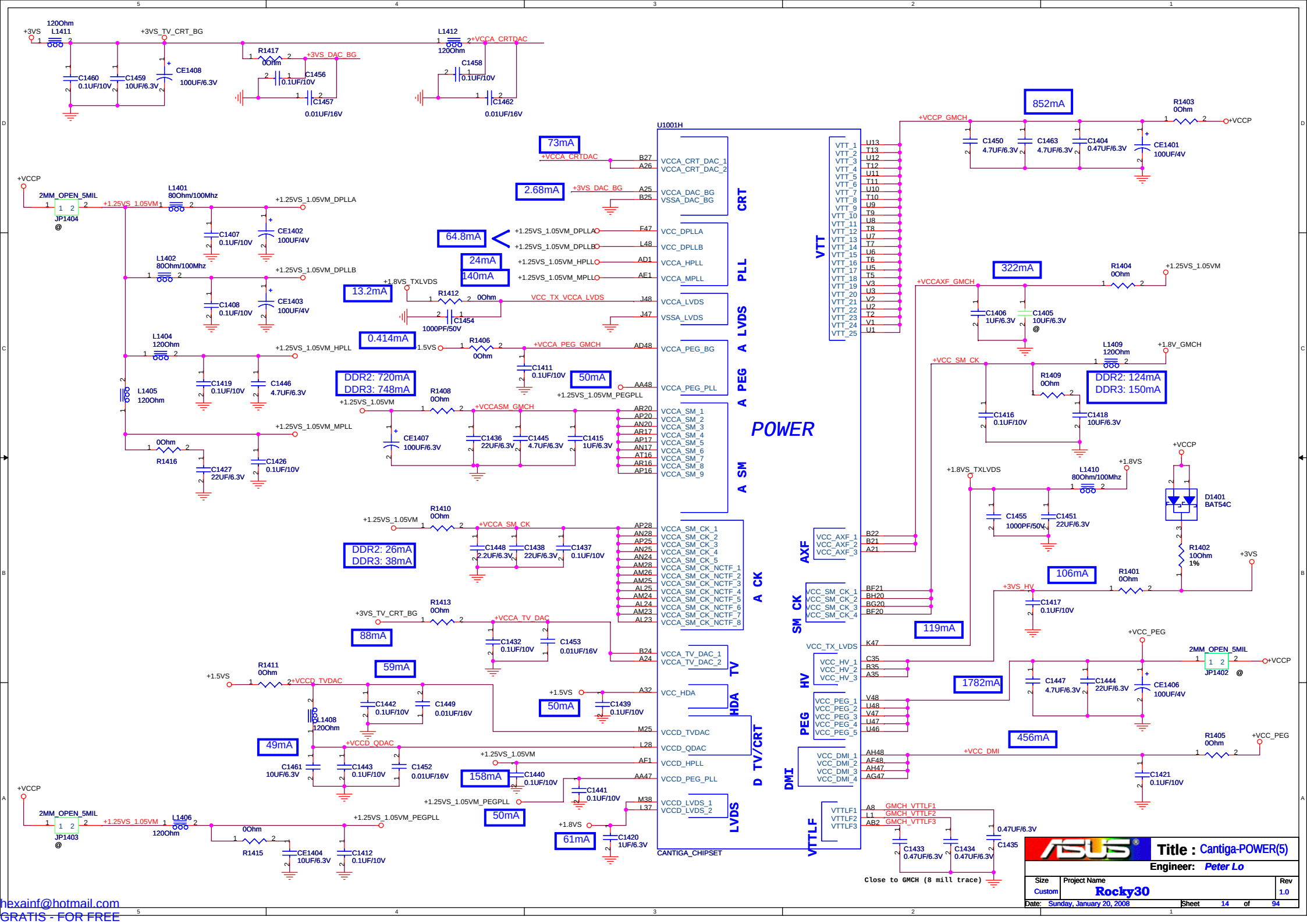

U1001B
RSVD
DDR CONTROL/COMPENSATION
CLK
DMI
CFG
GRAPHICS VID
PWR MGT
ME
MISC
HDA
NC
CANTIGA_CHIPSET
U1001C
PCI-EXPRESS GRAPHICS
LVDS
TV
VGA
CANTIGA_CHIPSET
Title : Cantiga-DDR2/PEG(2)
Engineer: Peter Lo
Project Name
Rocky30
Rev
1.0
Date: Monday, February 04, 2008
Sheet 11 of 94
hexainf@hotmail.com
GRATIS - FOR FREE

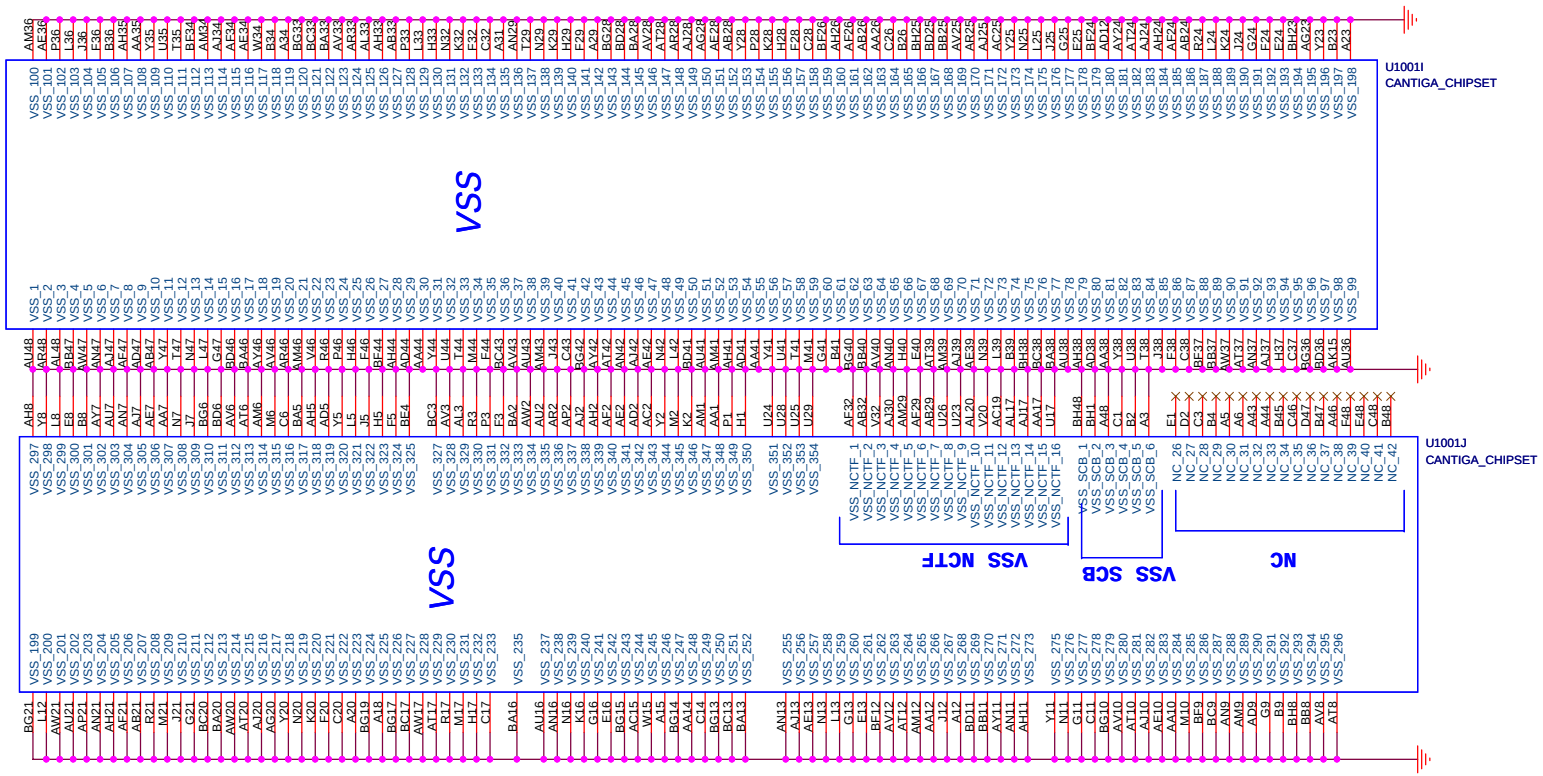


Title : Cantiga--DDR2 (3)		
Engineer: Peter Lo		
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 12 of 94	



Title : Cantiga--POWER (4)		
Engineer: Peter Lo		
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Sunday, January 20, 2008	Sheet 13 of 94	





11 MCH_CFG_5 — R1509 2.21KOhm @ 1%

CFG5 : DMI STRAP
HIGH = DMI X 4 (Default)
LOW = DMI X 2

11 MCH_CFG_6 — R1514 2.21KOhm @ 1%

CFG6 : Integrated TPM Host Interface
HIGH = iTPM disable (Default)
LOW = iTPM enable

11 MCH_CFG_7 — R1511 2.21KOhm @ 1%

CFG7 : Intel ME Crypto Strap Transport Layer Security cipher suite
HIGH = With confidentiality (Default)
LOW = Without confidentiality

11 MCH_CFG_9 — R1512 2.21KOhm @ 1%

CFG9 : PCIE GRAPHIC LANE
LOW = Reverse Lanes
HIGH = Normal Operation (Default)

11 MCH_CFG_16 — R1507 2.21KOhm @ 1%

CFG16 : FSB Dynamic ODT
HIGH = Ensable (Default)
LOW = Disable

11 MCH_CFG_10 — R1508 2.21KOhm @ 1%

CFG10 : PCIe Loopback
HIGH = Disable (Default)
LOW = Enable

11 MCH_CFG_12 — R1513 2.21KOhm @ 1%

11 MCH_CFG_13 — R1510 2.21KOhm @ 1%

CFG [13:12] : XOR/ALL-Z
00 = Reserved
01= XOR Mode Enabled
10= All-Z Mode Enabled
11= Normal Operation (Default)

+3VS — R1503 4.02KOhm @ 1% — 11 MCH_CFG_19

CFG19 : DMI Lane Reversal
LOW = NORMAL (default)
HIGH = Reverse Lanes

+3VS — R1506 4.02KOhm @ 1% — 11 MCH_CFG_20

CFG20 : SDVO/PCIE CONCURRENT MODE
LOW = ONLY SDVO or PCIE is Operational (Default)
HIGH = SDVO and PCIE are operating simultaneously via the PEG port

Title : Cantiga-GND		
Engineer: Peter Lo		
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 15 of 94	

Title :	***
Engineer:	Peter Lo
Size: B	Project Name: Rocky30
Rev: 1.0	
Date: Thursday, October 18, 2007	Sheet 16 of 94

Title :	***
Engineer:	Peter Lo
Size: B	Project Name: Rocky30
Rev:	1.0
Date:	Thursday, October 18, 2007
Sheet	17 of 94

Title : ***

Engineer: *Peter Lo*

Size	Project Name	Rev
B	Rocky30	1.0

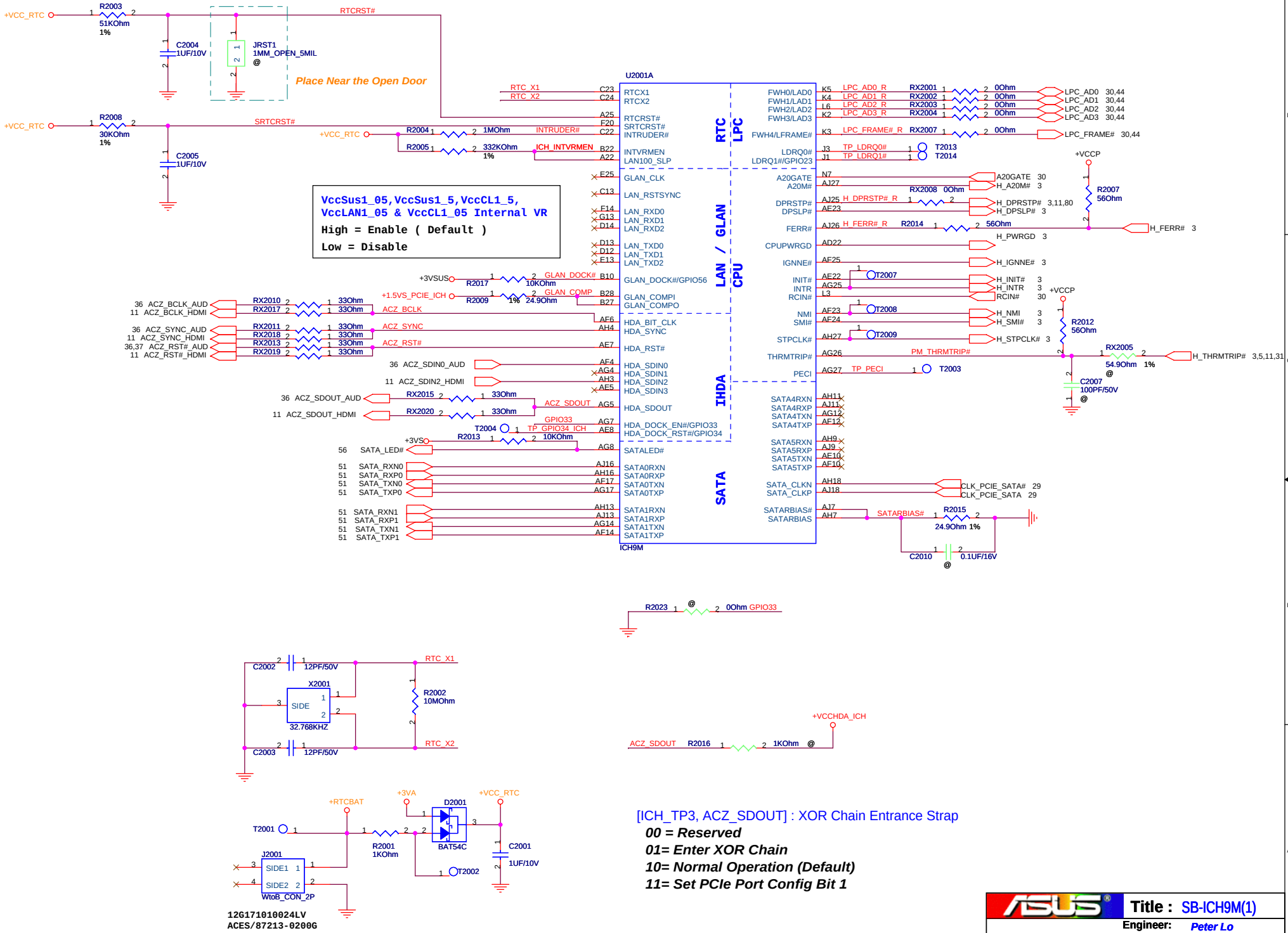
Date: Thursday, October 18, 2007 Sheet 18 of 94

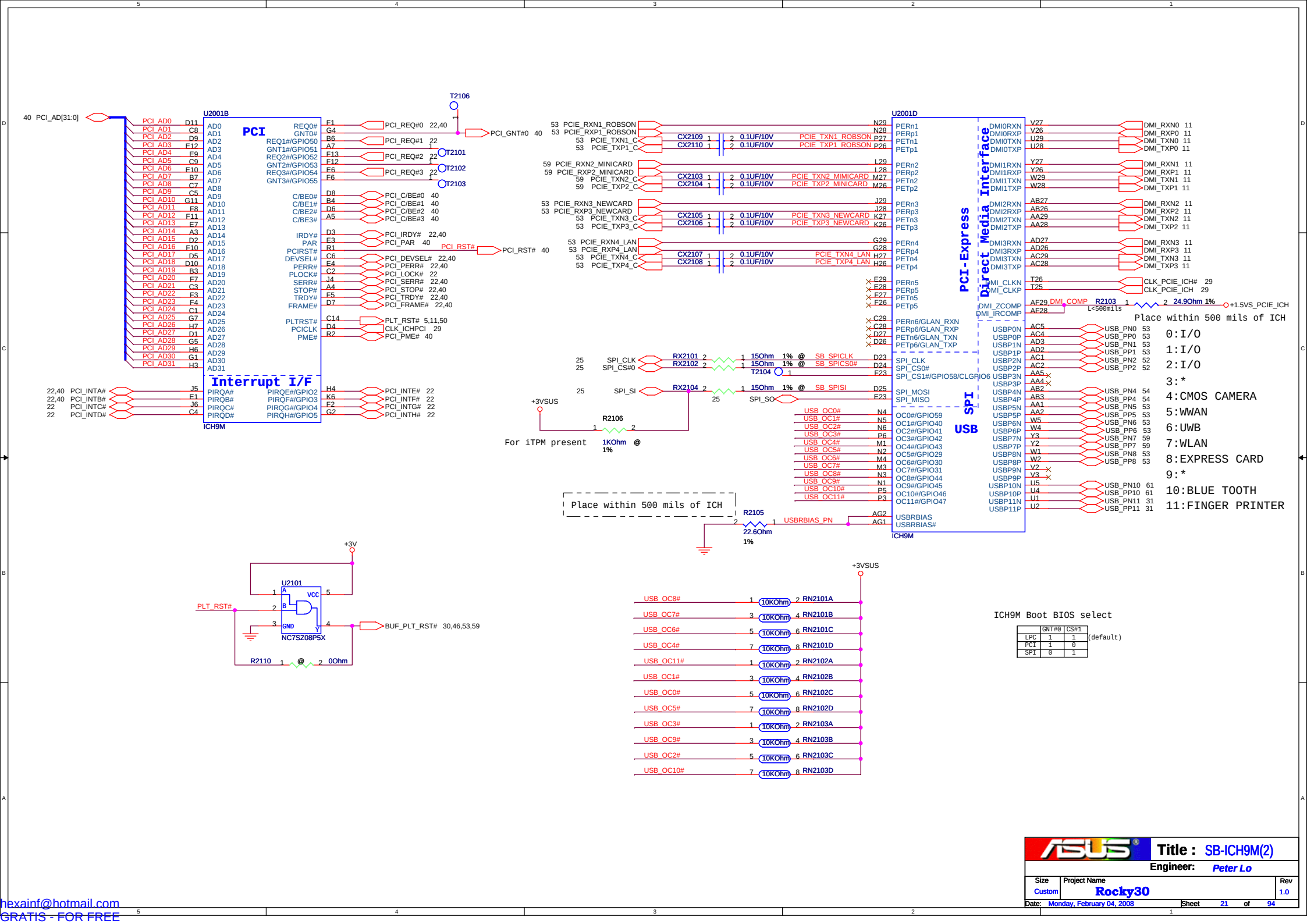
Title : ***

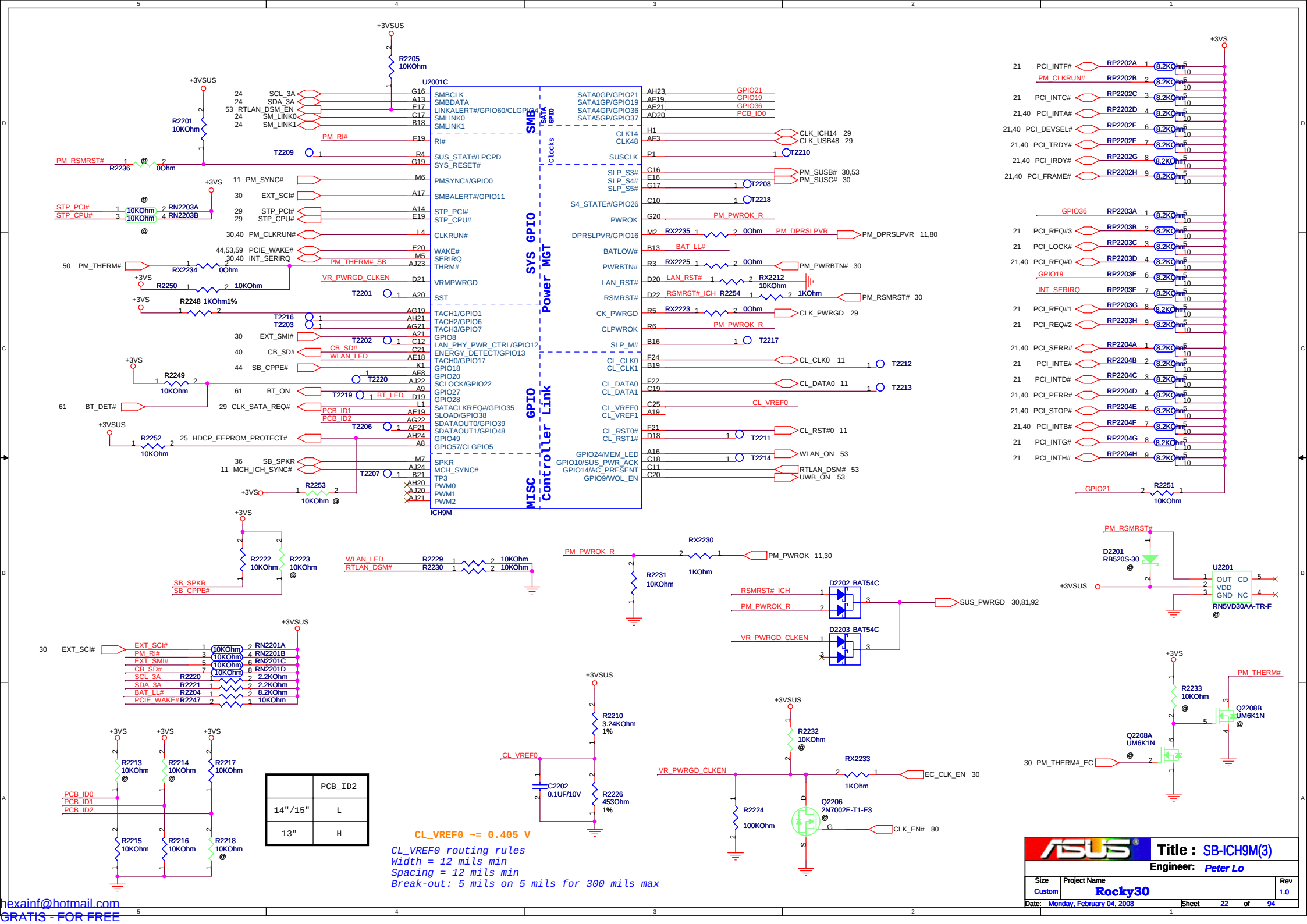
Engineer: *Peter Lo*

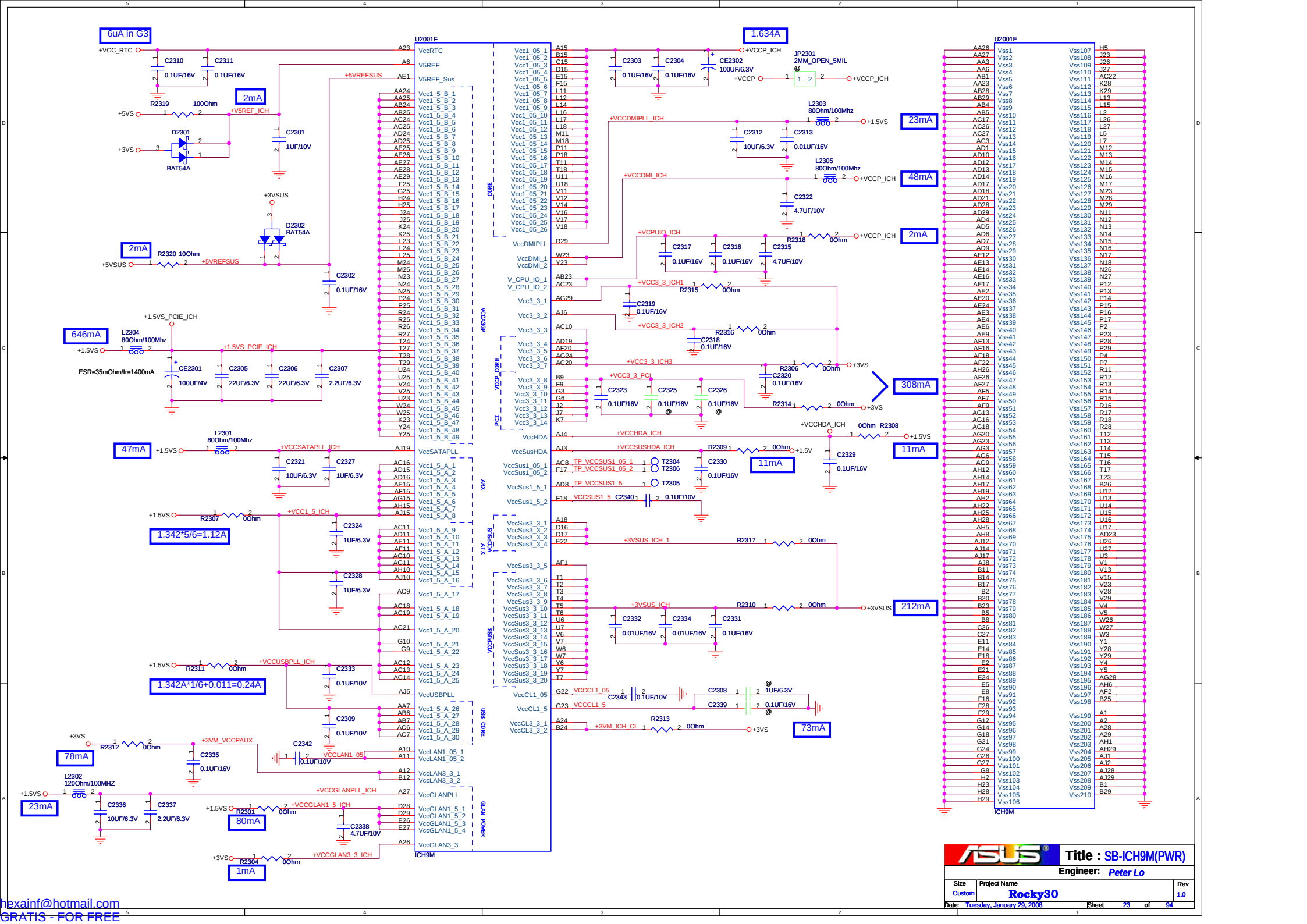
Size	Project Name	Rev
B	Rocky30	1.0

Date: Thursday, October 18, 2007 Sheet 19 of 94

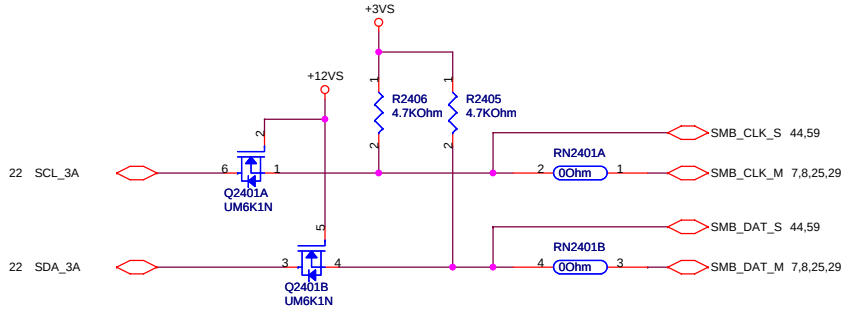








ICH9-M



ICH9M

NEWCARD,WLAN

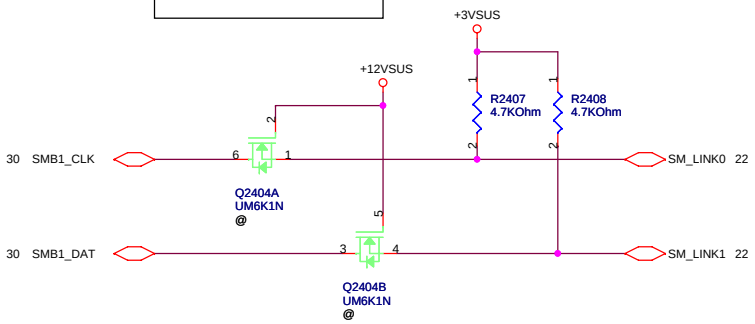
CLOCK GEN
SO-DIMM0 , SO-DIMM1

NEWCARD,WLAN

CLOCK GEN
SO-DIMM0 , SO-DIMM1

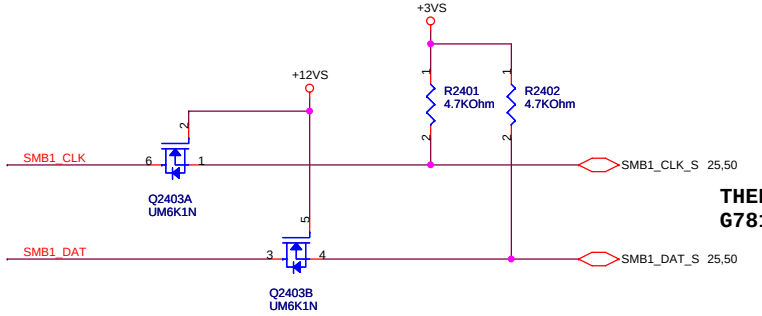
EC

Don't support iAMT
Remove ME-EC SMBus.



EC

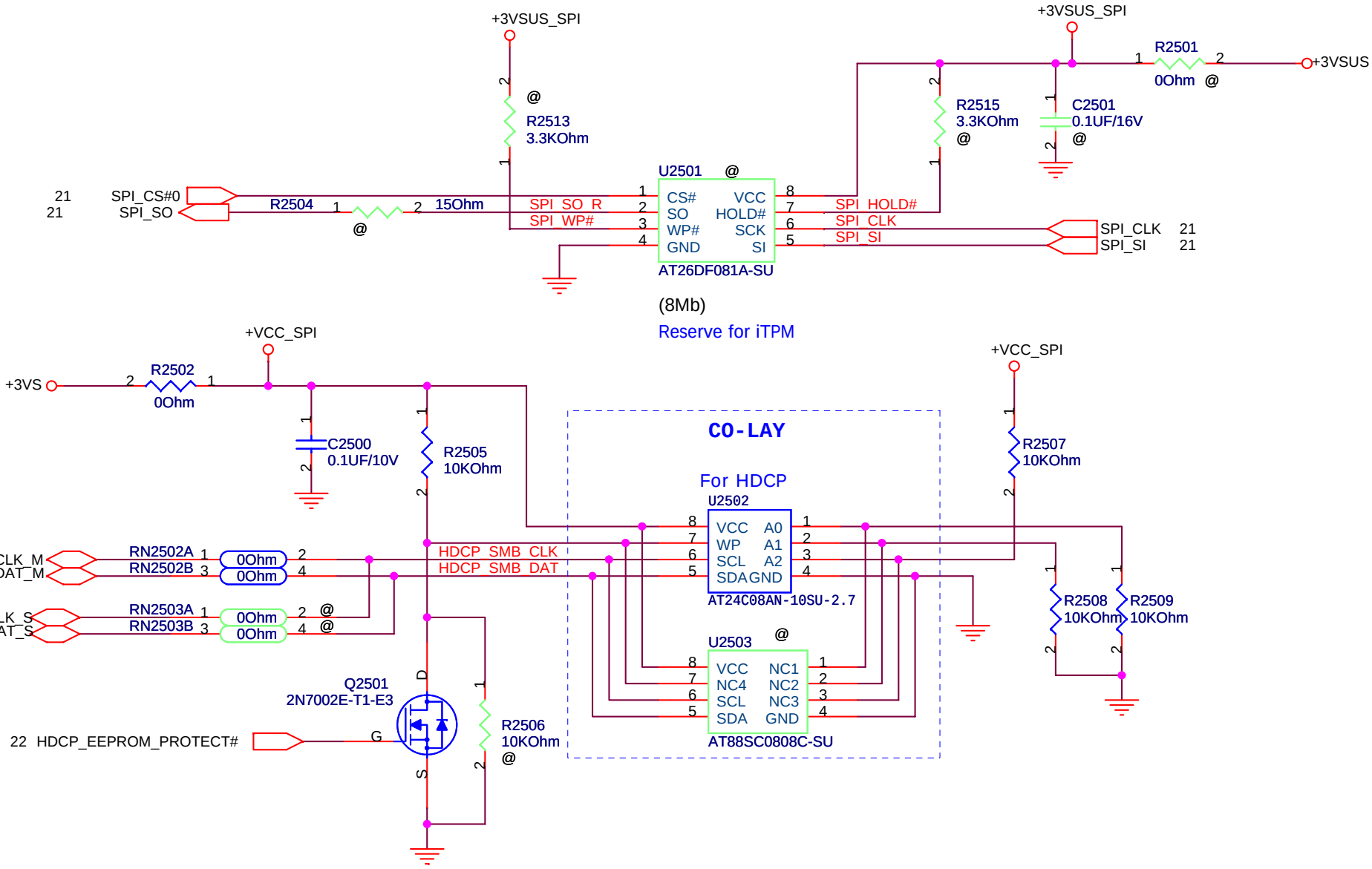
SB



EC

THERMAL IC
G781,G781-1

Title : ICH9M-Other		
Engineer: Peter Lo		
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 24 of 94	



U2502-AT24C08A :
Stuff : R2506 ; U2502 ; R2507 ; R2508 ; R2509
Nostuff : R2505

U2503-AT88SC0808C :
Stuff : U2503
Nostuff : R2505 ; R2506 ; R2507 ; R2508 ; R2509

ASUS	Title : SPI ROM	
	Engineer: Peter Lo	
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 25 of 94	

Title :	
Engineer:	Peter Lo
Size: A	Project Name: Rocky30
Rev:	1.0
Date:	Thursday, October 18, 2007
Sheet	26 of 94

Title :	
Engineer:	Peter Lo
Size: A	Project Name: Rocky30
Rev:	1.0
Date:	Thursday, October 18, 2007
Sheet	27 of 94

Title :	
Engineer:	Peter Lo
Size: A	Project Name: Rocky30
Rev:	1.0
Date:	Thursday, October 18, 2007
Sheet	28 of 94

+VCCP → +VCCP 5,10,11,13,14,20,23,80,82

+3VS → +3VS 3,7,8,11,14,15,20,22,23,24,25,30,31,37,40,41,45,46,48,50,51,53,54,57,58,59,61,91,92

U2901

ICS9LPRS365BGLFT

C2917,C2918,C2919 near CLK Gen.

CR#_A	0 = SRC 0 1 = SRC 2 SATA
CR#_B	0 = SRC 1 1 = SRC 4 MCH
CR#_C	0 = SRC 0 1 = SRC 2
CR#_D	0 = SRC 1 1 = SRC 4
CR#_E	SRC 6 WLAN
CR#_F	SRC 8 LAN
CR#_G	SRC 9 New Card
CR#_H	SRC 10 Robson

Latched Input Select

0 = SRC 8
1 = CPU_ITP CLK

Decide pin 46,47

ITP_EN — R2909 10KOhm

27_Select =0,
pin#13/14=DOT96;
pin#17/18=LCD_SST;

Decide pin 13/14,17/18

27_Select =1,
pin#13/14=SRC0;
pin#17/18=27MHz non-spread SE clock;

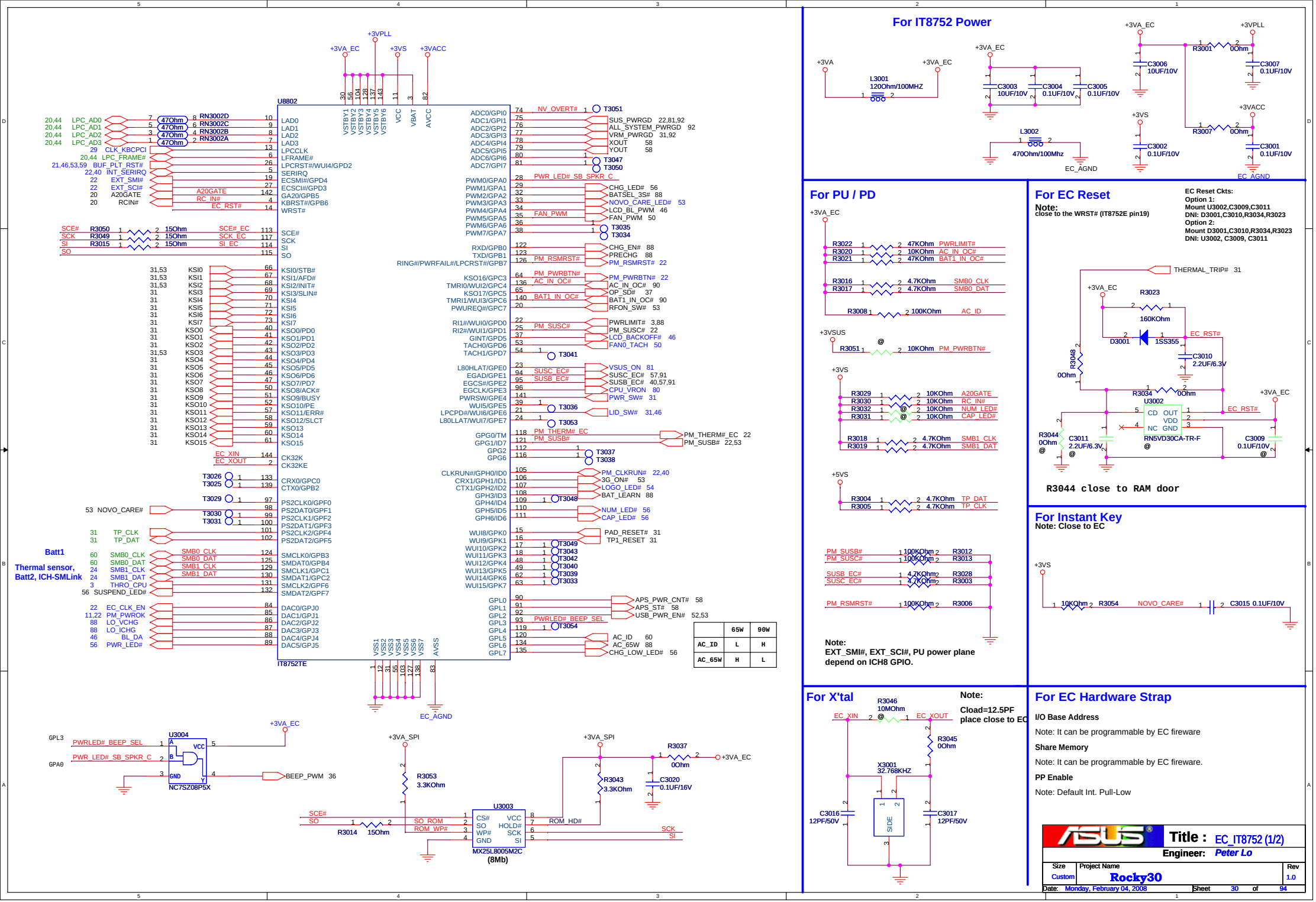
27_SEL — R2915 10KOhm @ — R2913 10KOhm

For GM/GL, need to PD for 96MHz output.
For PM, need to PU for 27MHz output.

BCLK	FSB	FSLC BSEL2	FSLB BSEL1	FSLA BSEL0
166	667	0	1	1
200	800	0	1	0
266	1066	0	0	0

C2921, C2922, C2923, C2924, C2925, C2926,
C2927, C2928, C2929, C2930 near CLK Gen.

Title :	ICS9LPR365
Engineer:	Peter Lo
Size	Custom
Project Name	Rocky30
Rev	1.0
Date:	Monday, February 04, 2008
Sheet	29 of 94



For IT8752 Power

For PU / PD

Note:
EXT_SMI#, EXT_SCI#, PU power plane depend on ICH8 GPIO.

For EC Reset

Note:
close to the WRST# (IT8752E pin19)

EC Reset Ckts:
Option 1:
Mount U3002,C3009,C3011
DNI: D3001,C3010,R3034,R3023
Option 2:
Mount D3001,C3010,R3034,R3023
DNI: U3002, C3009, C3011

R3044 close to RAM door

For Instant Key

Note: Close to EC

For X'tal

Note:
Cload=12.5PF
place close to EC

For EC Hardware Strap

I/O Base Address

Note: It can be programmable by EC fireware

Share Memory

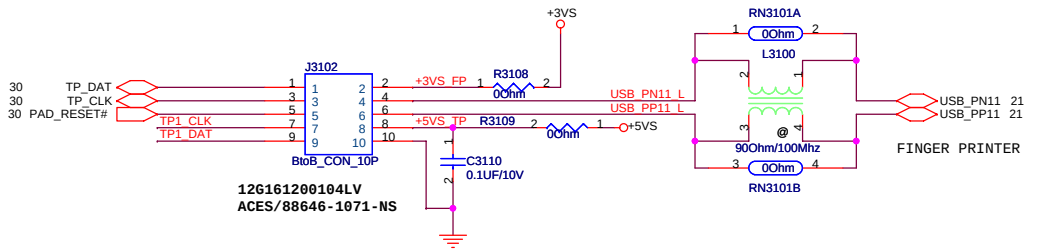
Note: It can be programmable by EC fireware.

PP Enable

Note: Default Int. Pull-Low

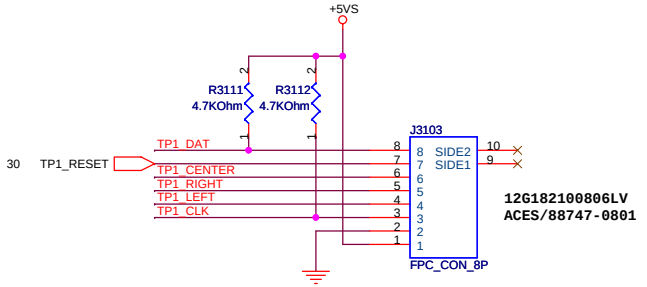
Title :	EC_IT8752 (1/2)		
Engineer:	Peter Lo		
Size	Project Name		Rev
Custom	Rocky30		1.0
Date:	Monday, February 04, 2008	Sheet 30 of 94	

TOUCH PAD CONN

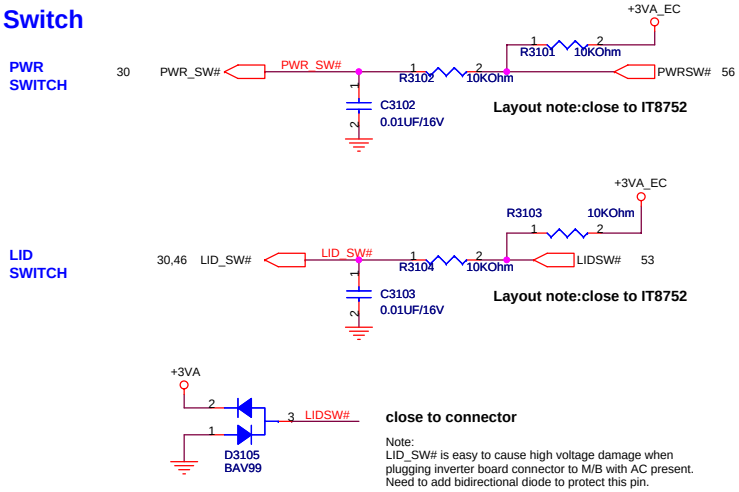


TP : Touch Pad
TP1: Track Point

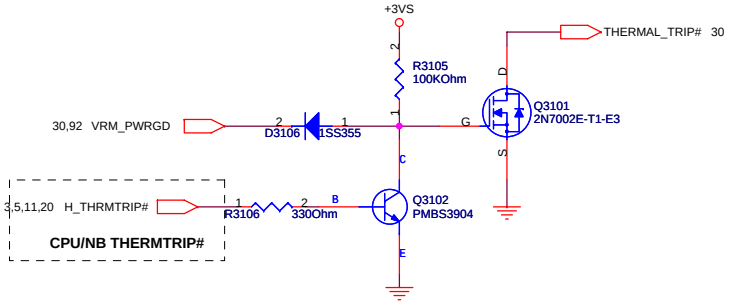
TRACK POINT CONN



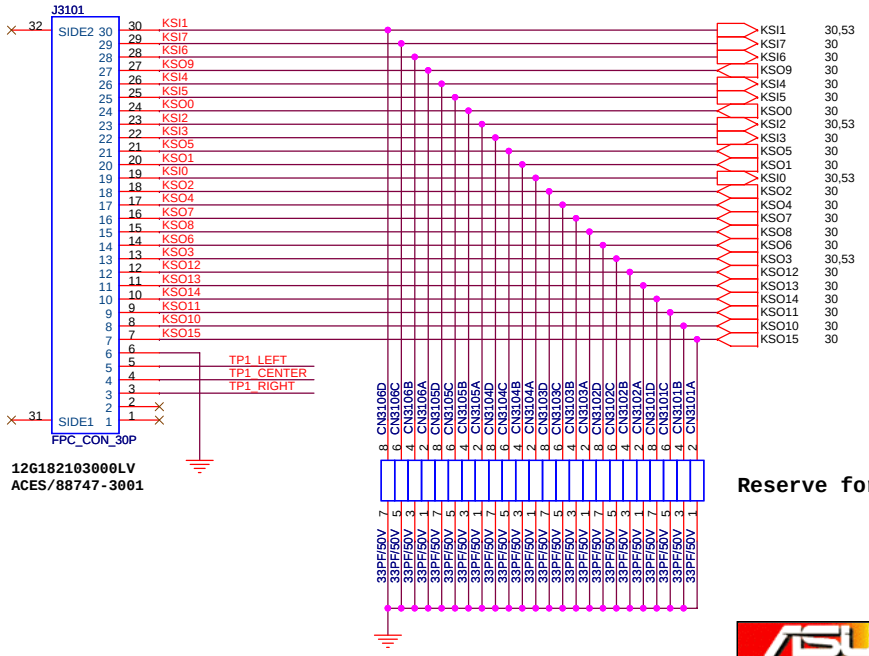
For Switch



For Thermal Control Method



Keyboard Connector

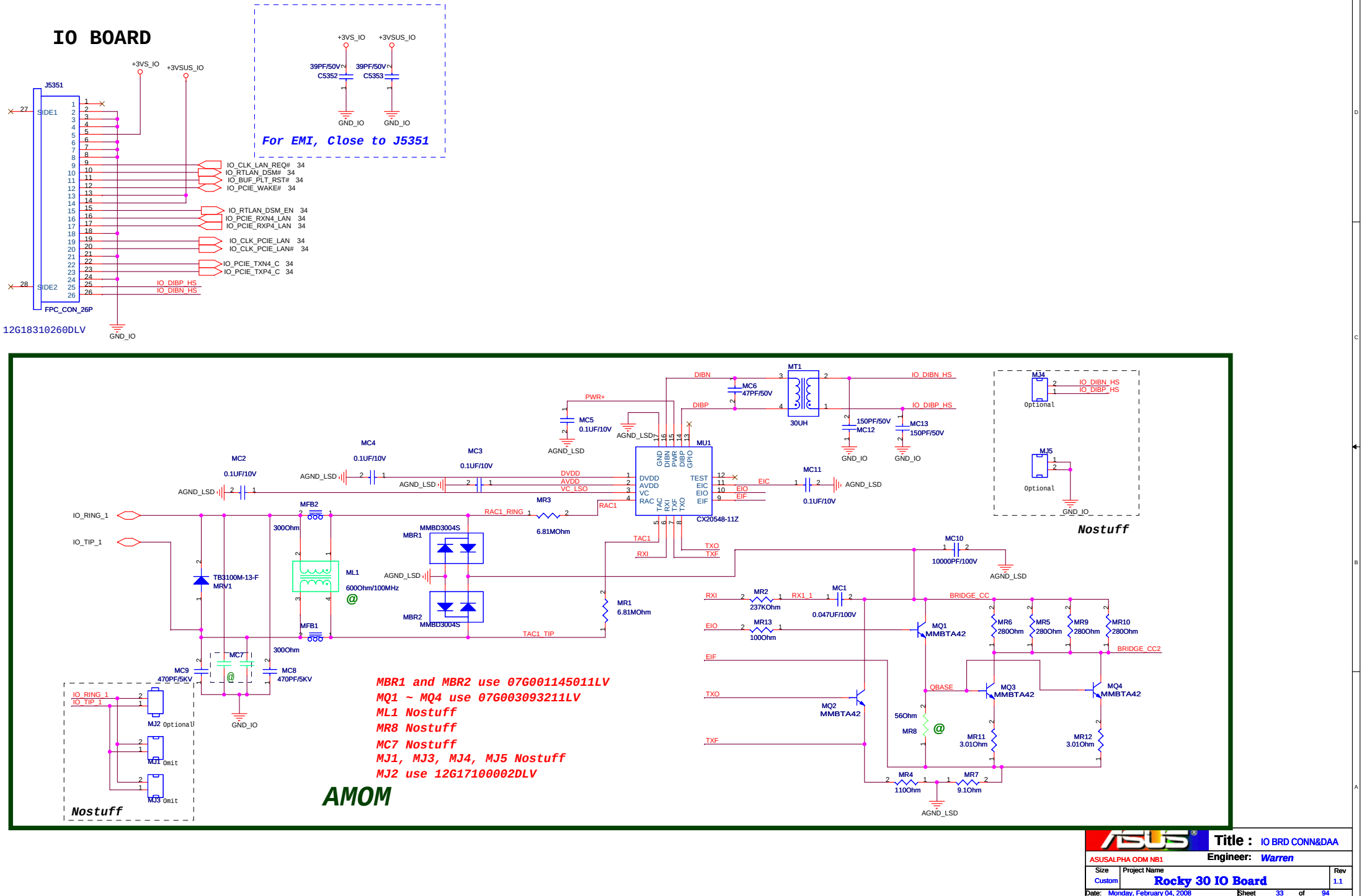


Reserve for WWAN

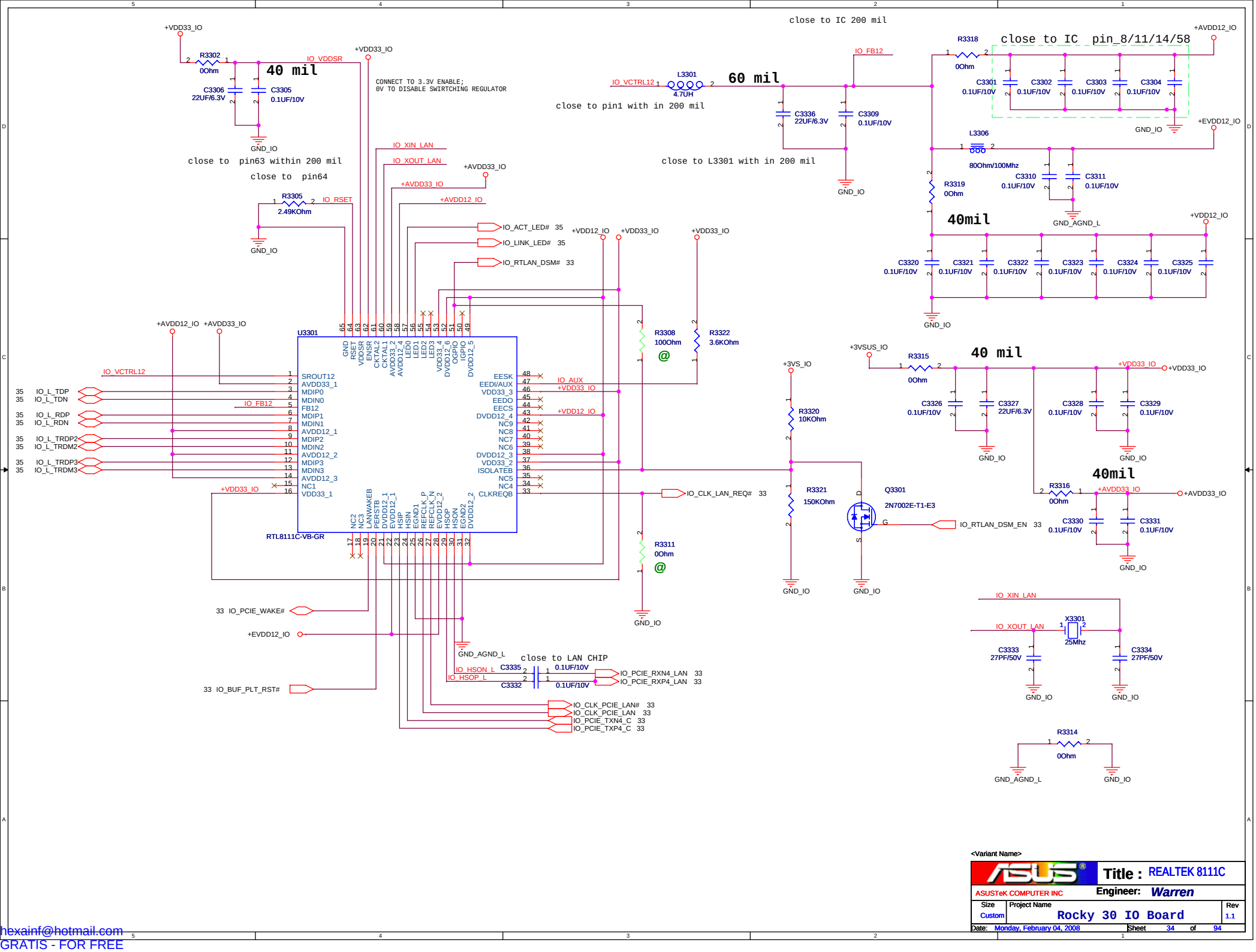
Title : EC_IT8752 (2/2)		
Engineer: Peter Lo		
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 31 of 94	

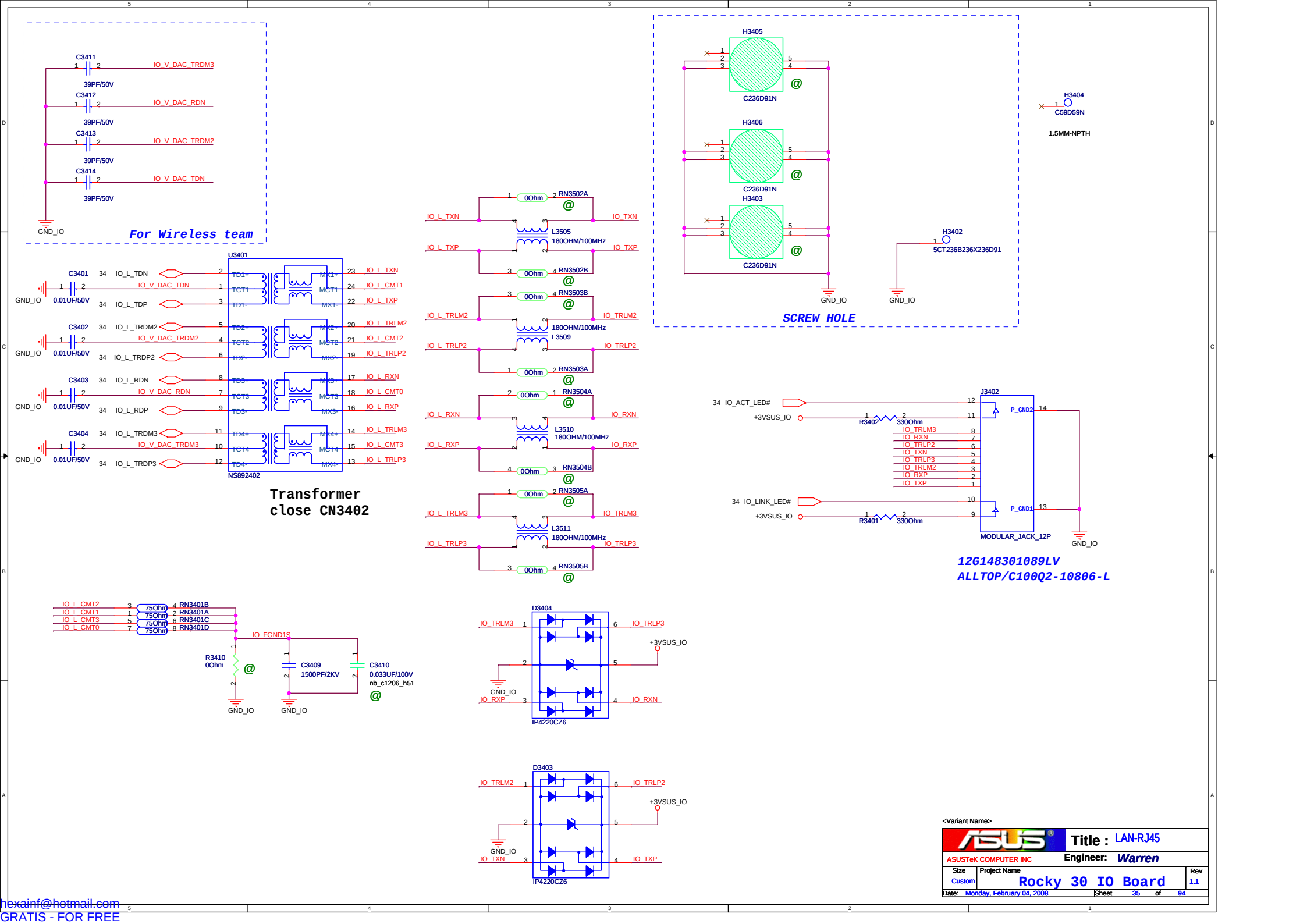
Title :	*
Engineer:	Peter Lo
Size: Custom	Project Name: Rocky30
Rev:	1.0
Date: Sunday, January 20, 2008	Sheet 32 of 94

IO BOARD



ASUSALPHA ODM NB1	Title : IO BRD CONN&DAA	
	Engineer: Warren	
Size: Custom	Project Name: Rocky 30 IO Board	Rev: 1.1
Date: Monday, February 04, 2008	Sheet 33 of 94	





<Variant Name>

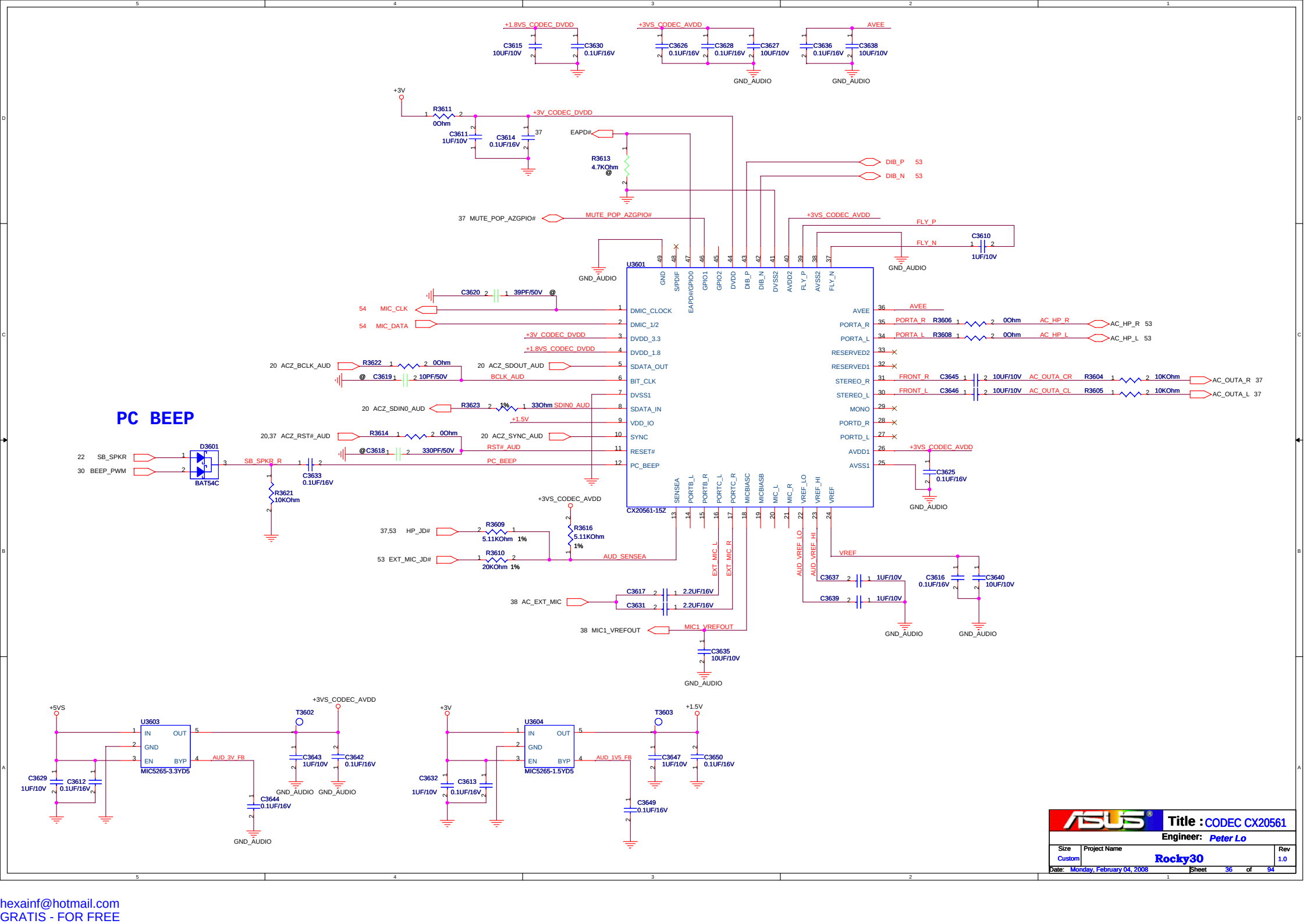
ASUSTeK COMPUTER INC

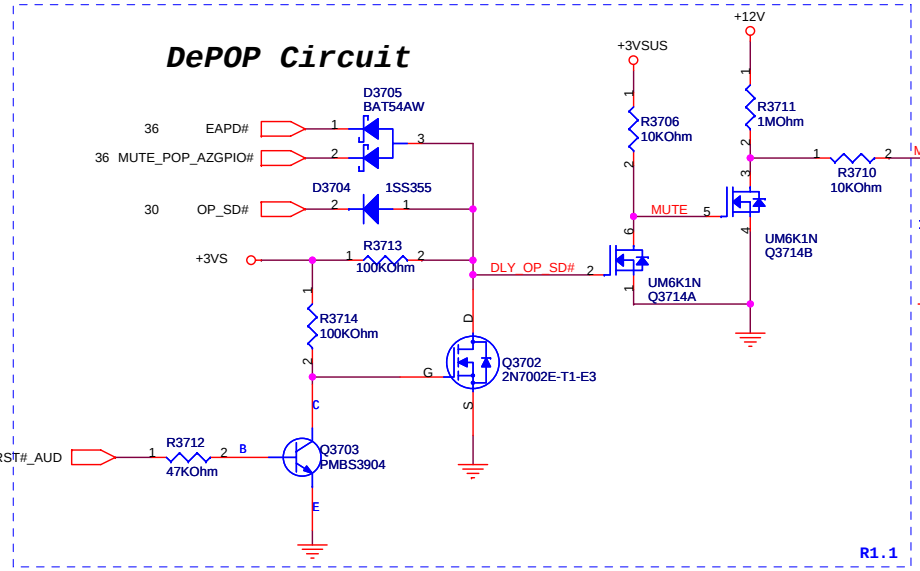
Title : LAN-RJ45

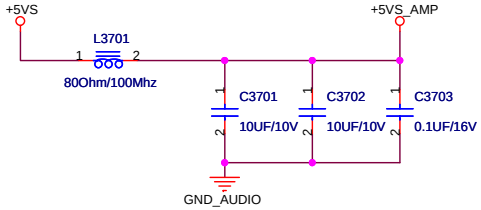
Engineer: Warren

Size	Project Name	Rev
Custom	Rocky 30 IO Board	1.1

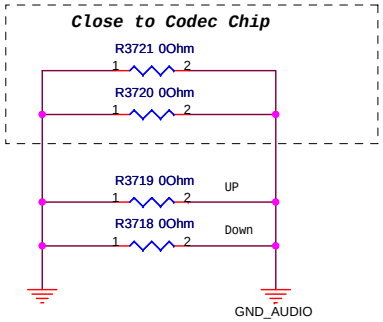
Date: Monday, February 04, 2008 Sheet 35 of 94





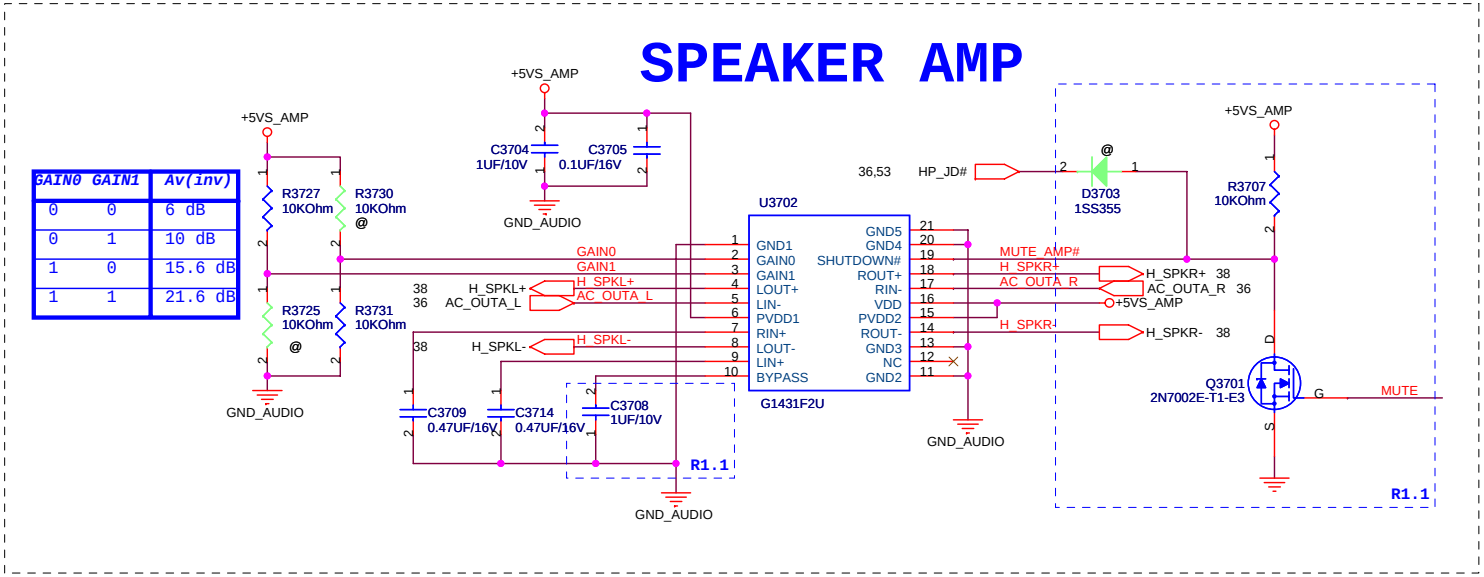


JACK GND



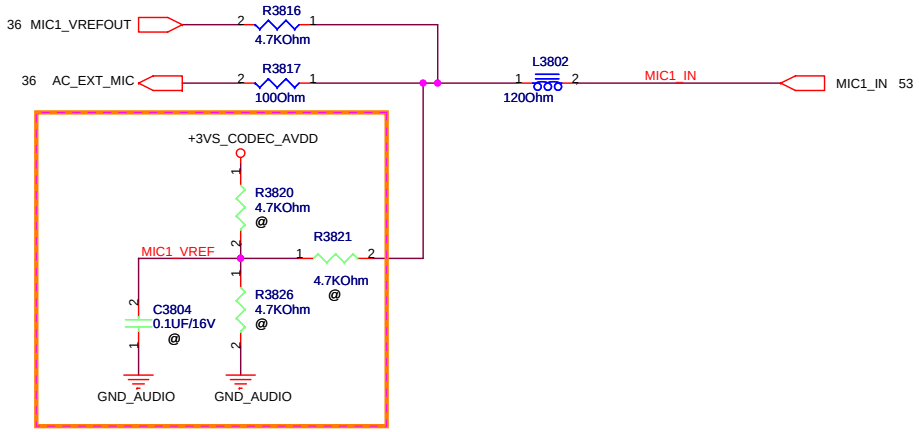
SPEAKER AMP

GAIN0	GAIN1	Av(inv)
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB



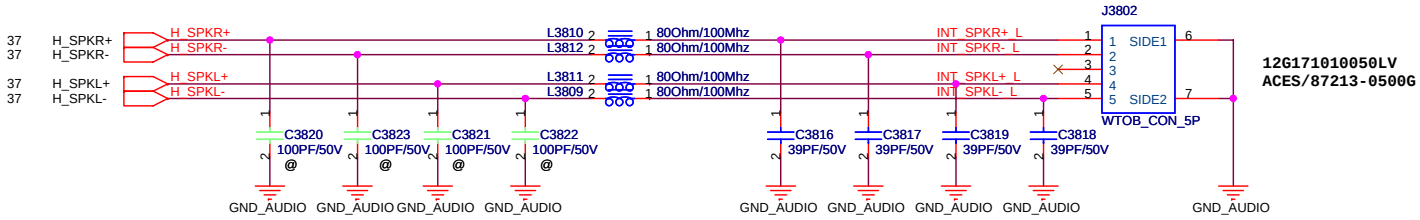
ASUS	Title : AUDIO AMP	
	Engineer: Peter Lo	
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 37 of 94	

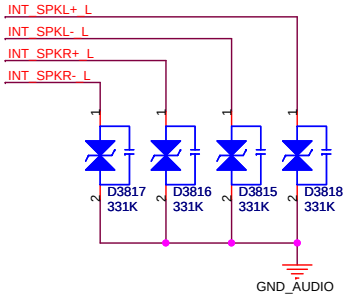
EXT MICROPHONE



Reserved the external MIC bias(T filter).

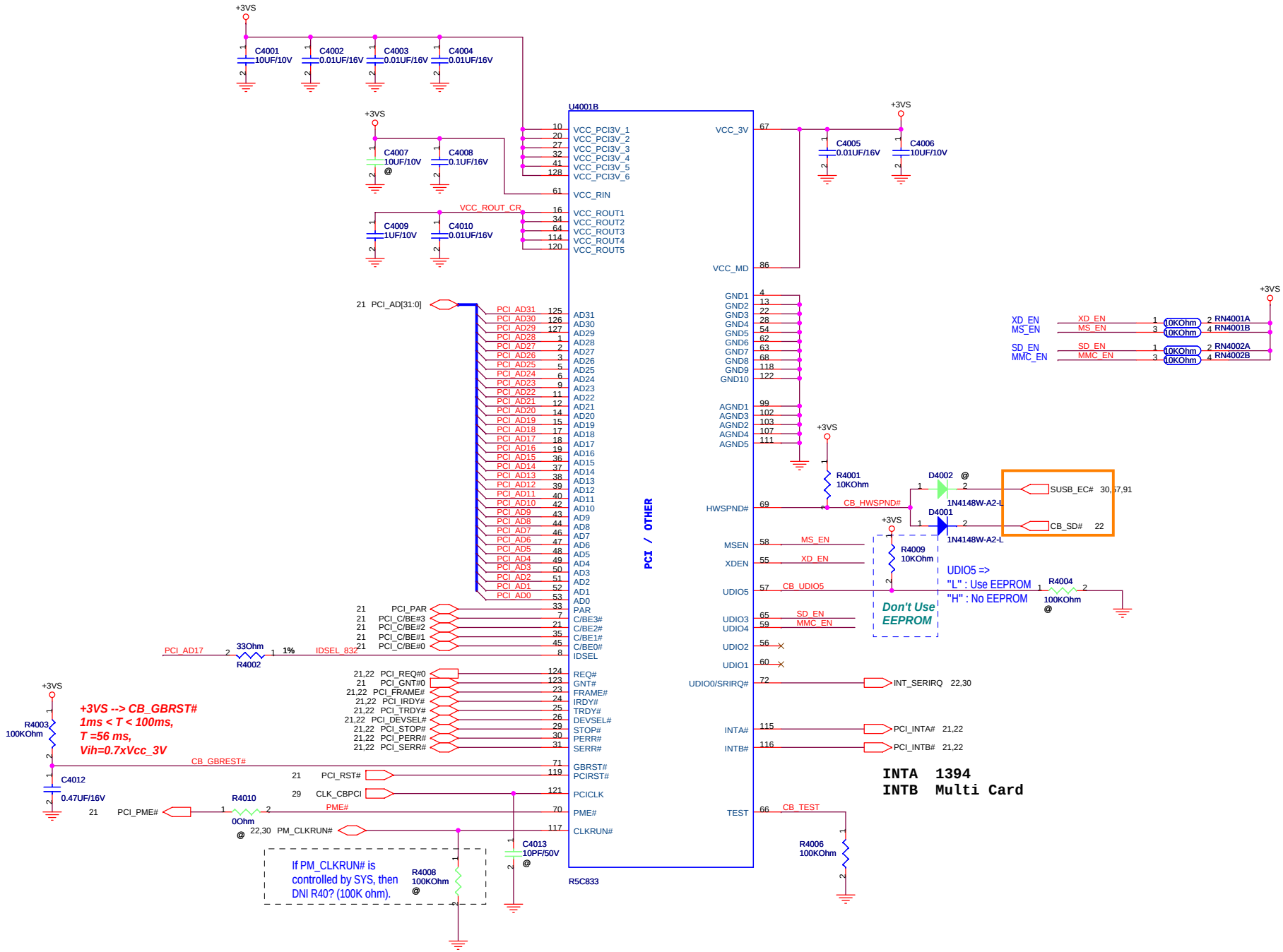
SPEAKER CONNECTOR



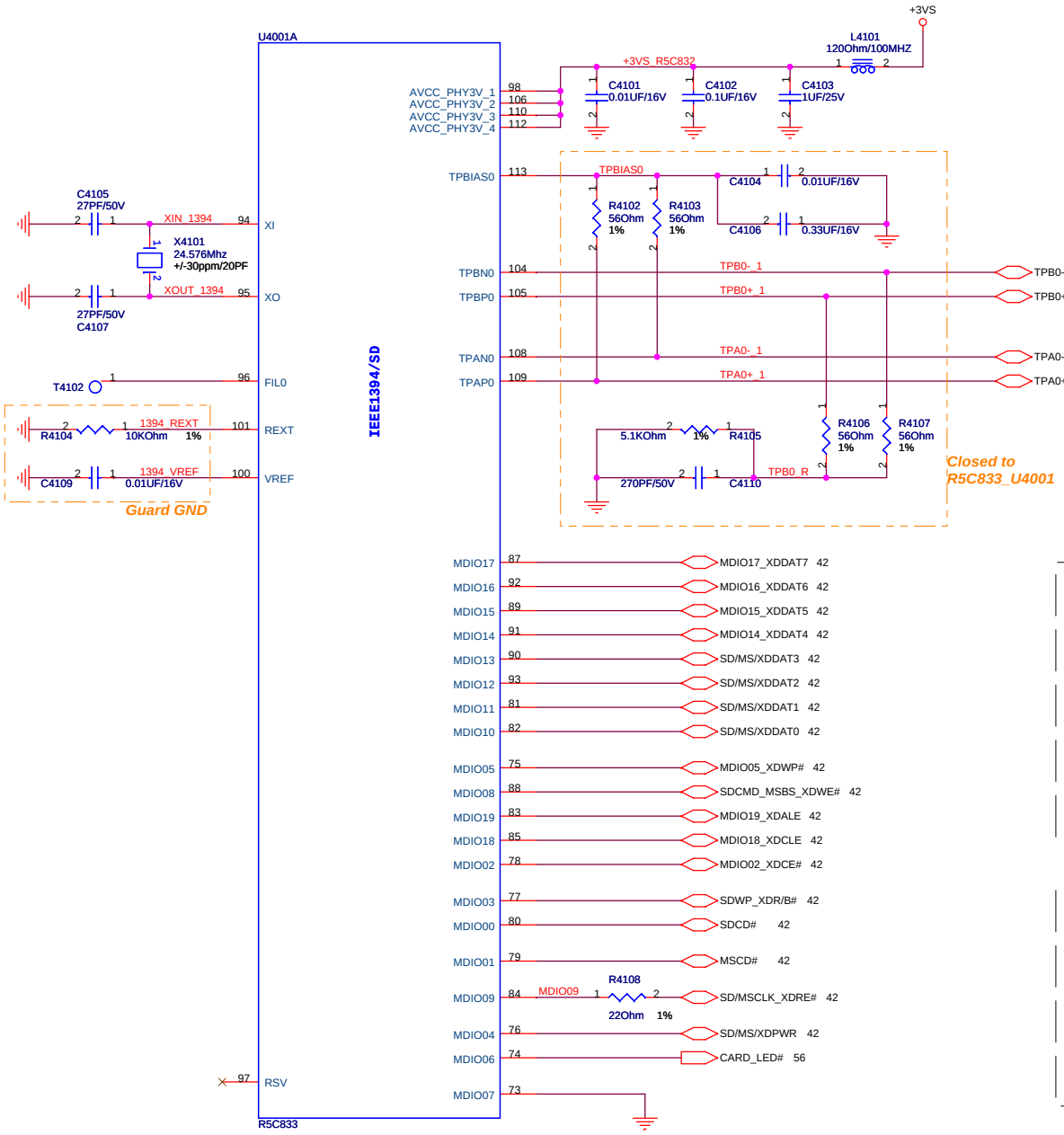


Title : MIC&LINEIN		
Engineer: Peter Lo		
Size: B	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 38 of 94	

Title :	***
Engineer:	Peter Lo
Size: Custom	Project Name: Rocky30
Rev:	1.0
Date: Thursday, October 18, 2007	Sheet 39 of 94



Title : CARDBUS R5C833 (1)		
Engineer: Peter Lo		
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 40 of 94	




```
MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO03--> SD Write Protect
MDIO04--> SD Card Power0 Control/
          MS Power Control
MDIO08--> SD Command/MS Bus State
MDIO09--> SD Clock/MS Clock
MDIO10--> SD Data 0/MS Data 0
MDIO11--> SD Data 1/MS Data 1
MDIO12--> SD Data 2/MS Data 2
MDIO13--> SD Data 3/MS Data 3
```

```
MDIO02--> xDCE#
MDIO05--> SD Power Control 1 / xDWP
MDIO06--> xD/MS/SD LED Control
MDIO14--> xD Data
MDIO15--> xD Data
MDIO16--> xD Data
MDIO17--> xD Data
MDIO18--> xD CLE
MDIO19--> xD ALE
```

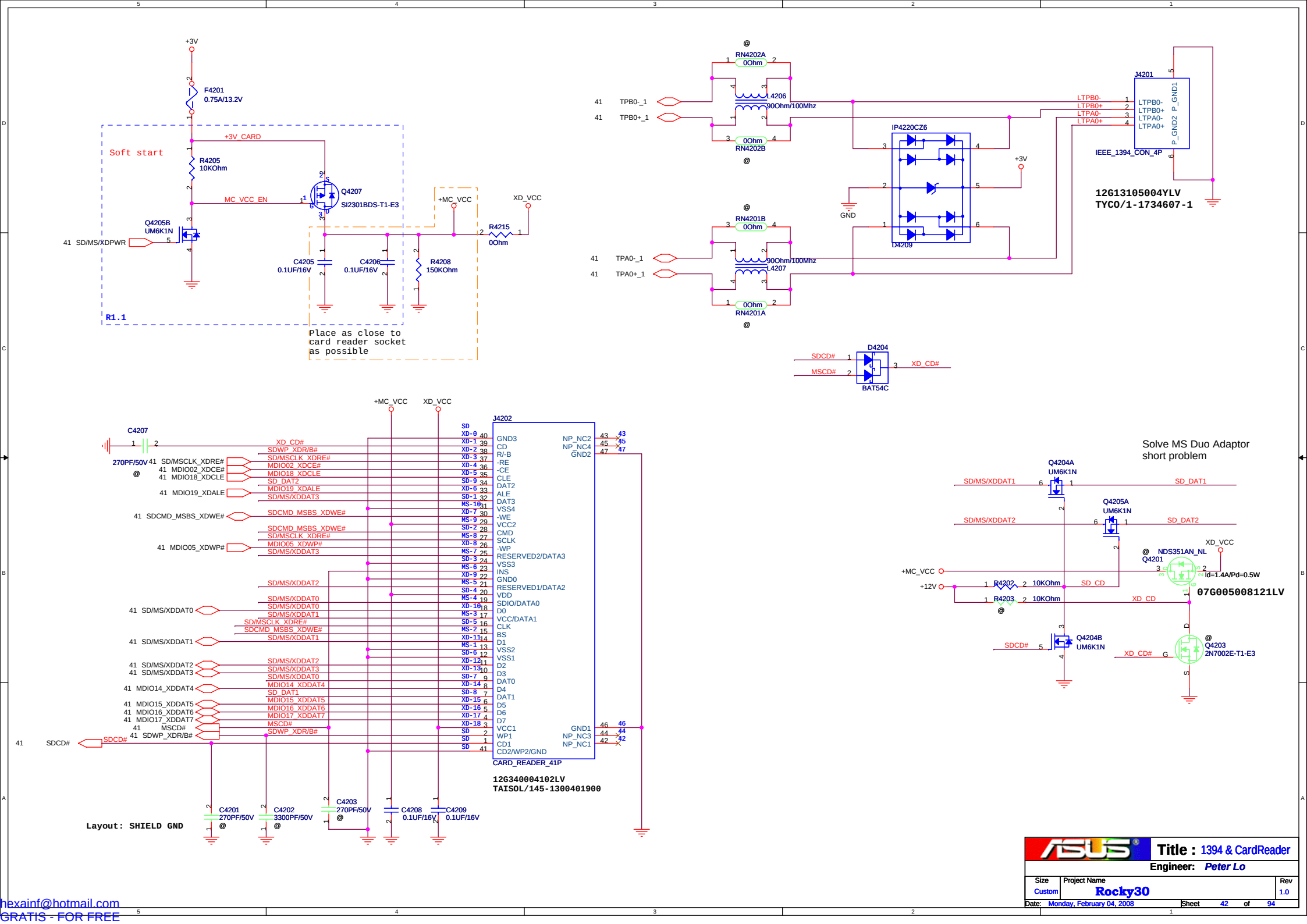
ASUS

Title : CARDBUS R5C833 (2)

Engineer: Peter Lo

Size	Project Name	Rev
Custom	Rocky30	1.0

Date: Monday, February 04, 2008 Sheet 41 of 94



Title : 1394 & CardReader

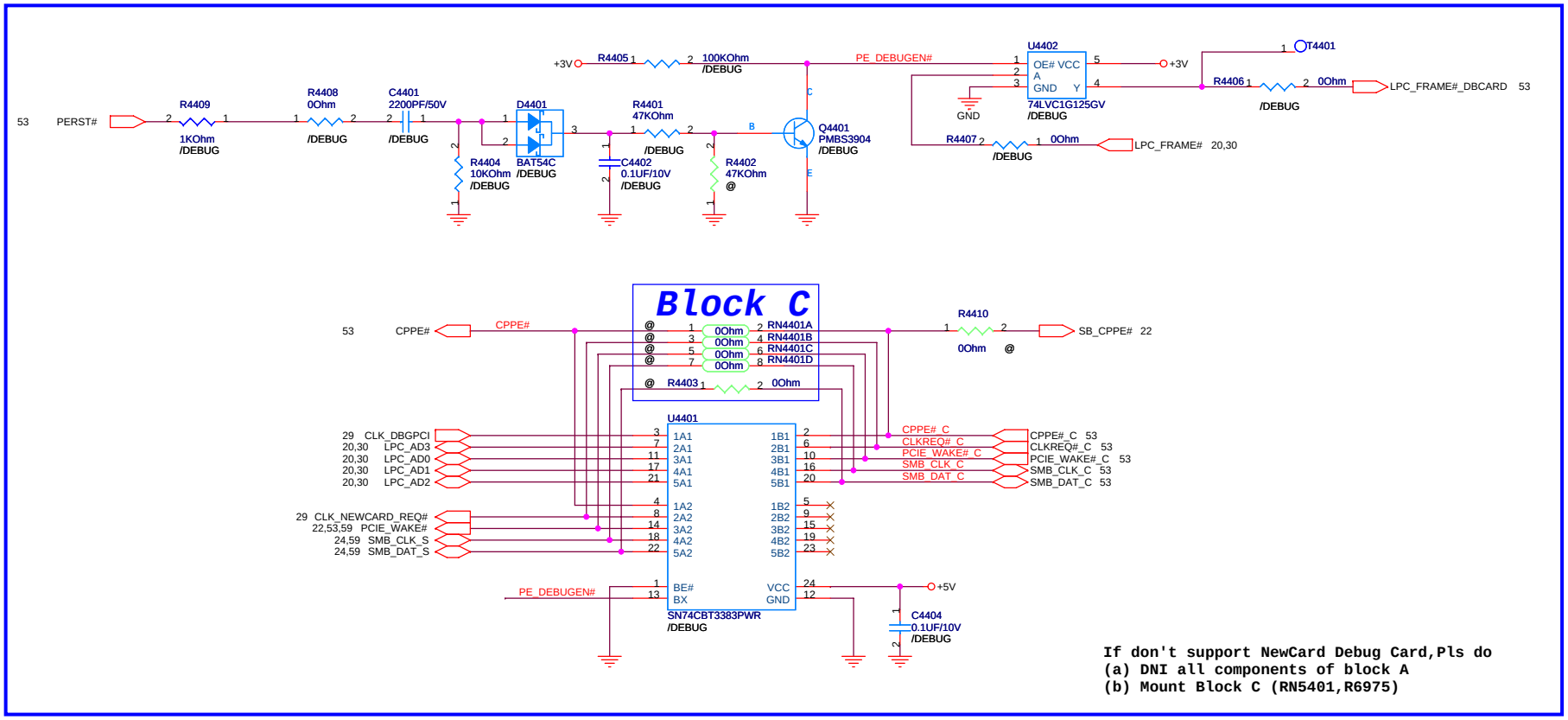
Engineer: Peter Lo

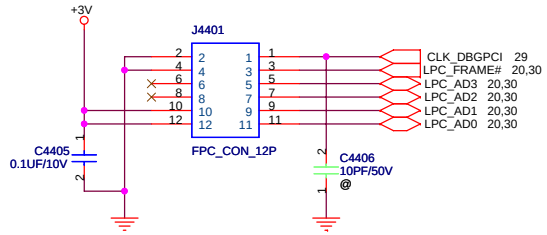
Size	Project Name	Rev
Custom	Rocky30	1.0

Date: Monday, February 04, 2008 Sheet 42 of 94

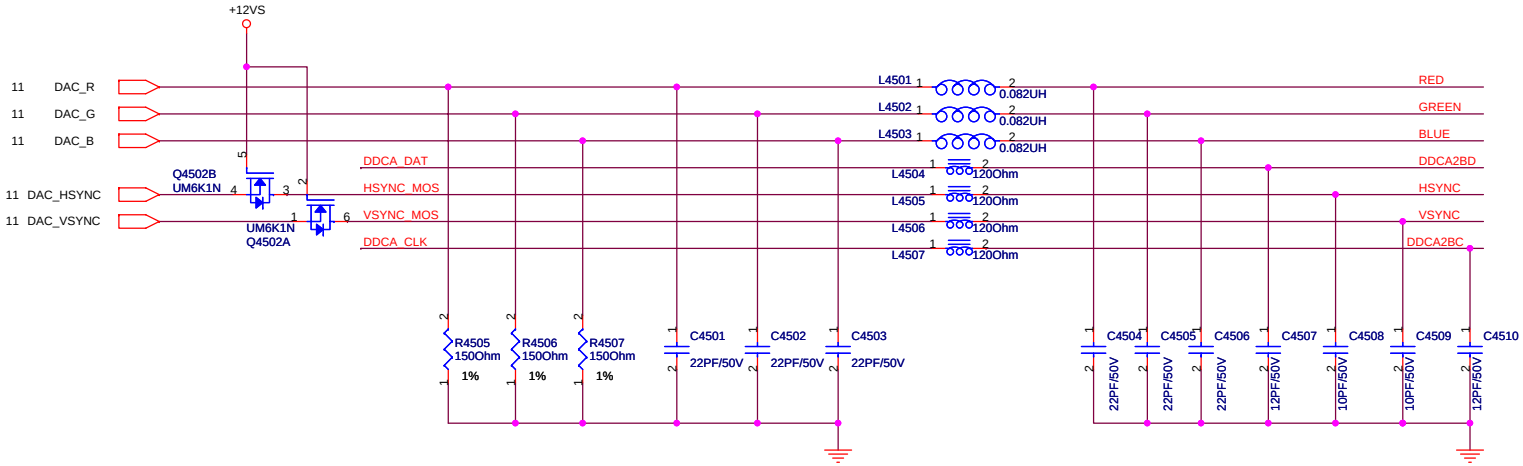
Title :	****
Engineer:	*Peter Lo*
Size: Custom	Project Name: **Rocky30**
Rev: 1.0	
Date: Thursday, October 18, 2007	Sheet 43 of 94

Block A

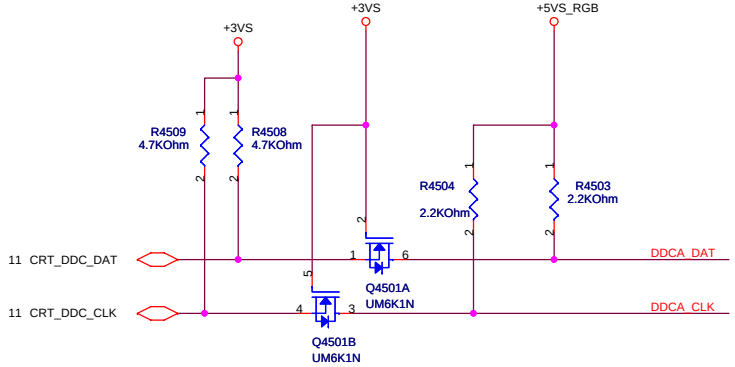


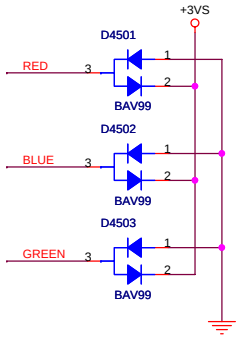


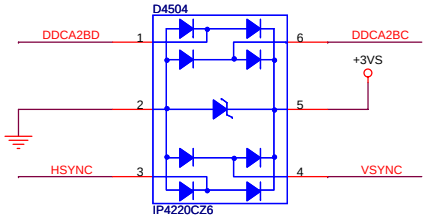
Title : DEBUG		
Engineer: Peter Lo		
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 44 of 94	

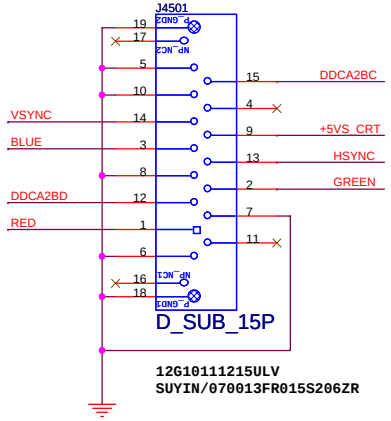


PLACE ESD Diodes near VGA port





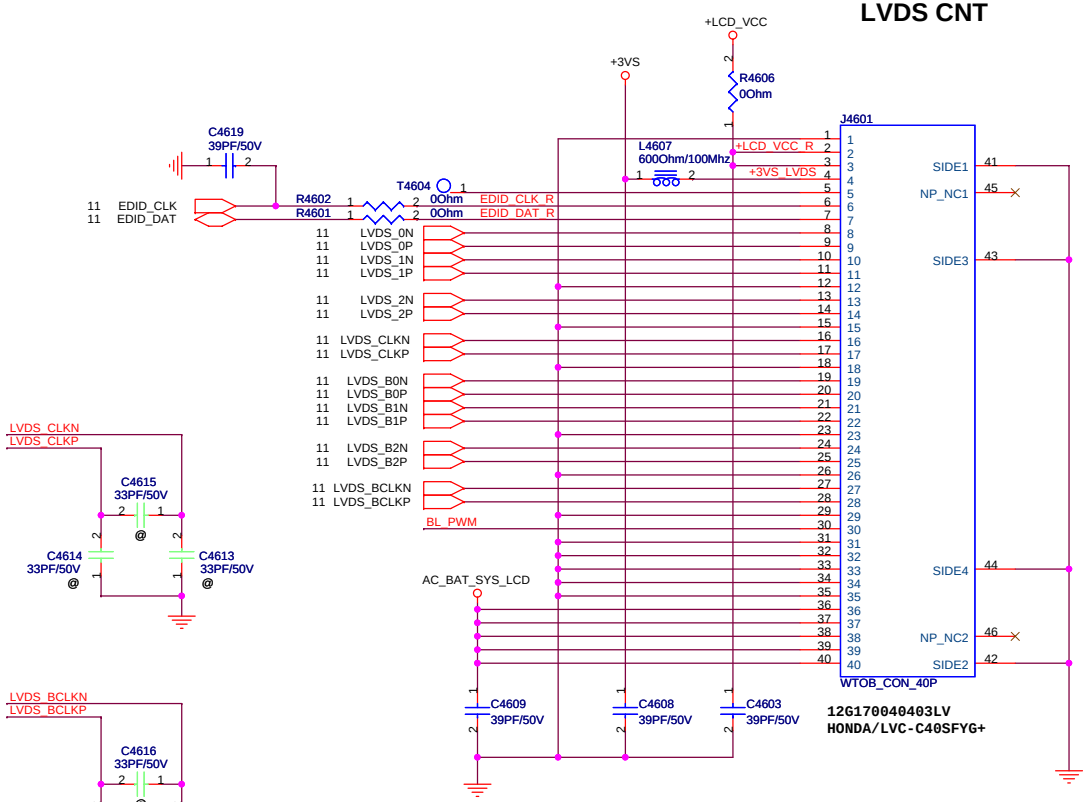




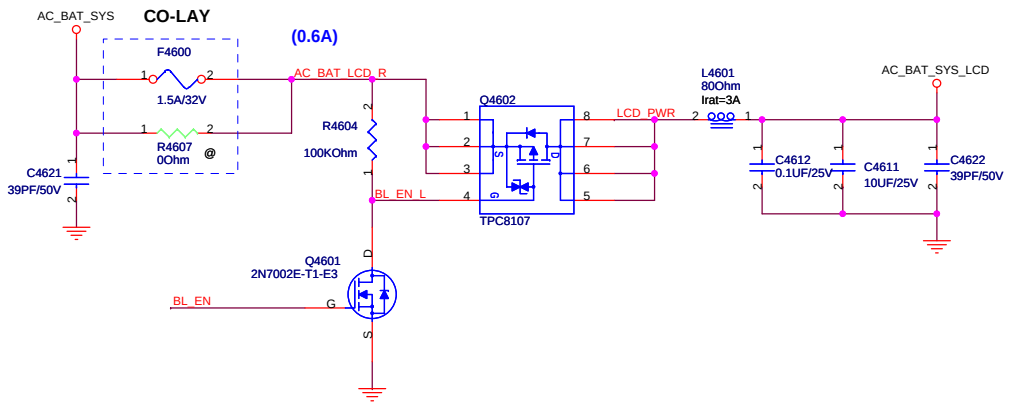
12G10111215ULV
SUYIN/070013FR015S206ZR

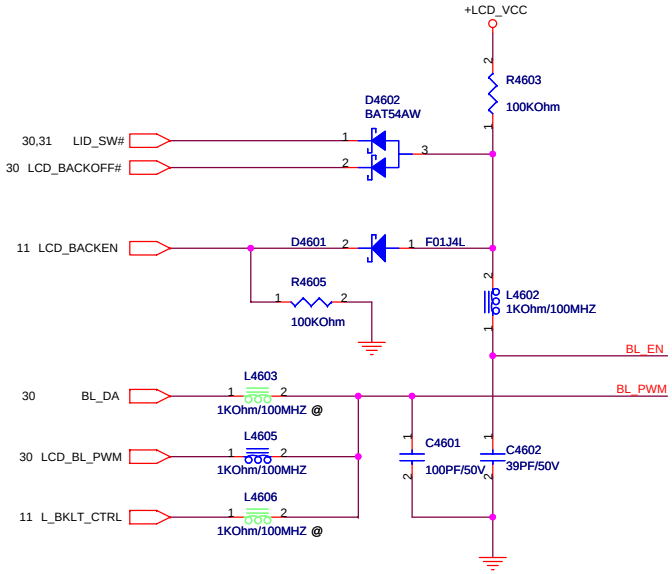
Title : CRT		
Engineer: Peter Lo		
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 45 of 94	

LVDS CNT

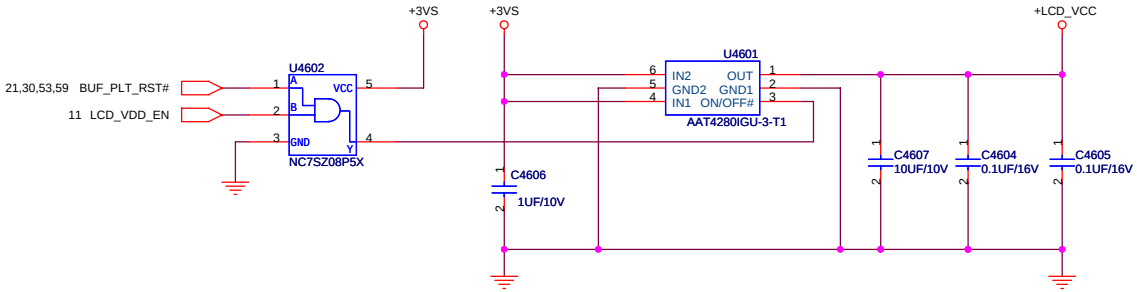


12G170040403LV
HONDA/LVC-C40SFYG+



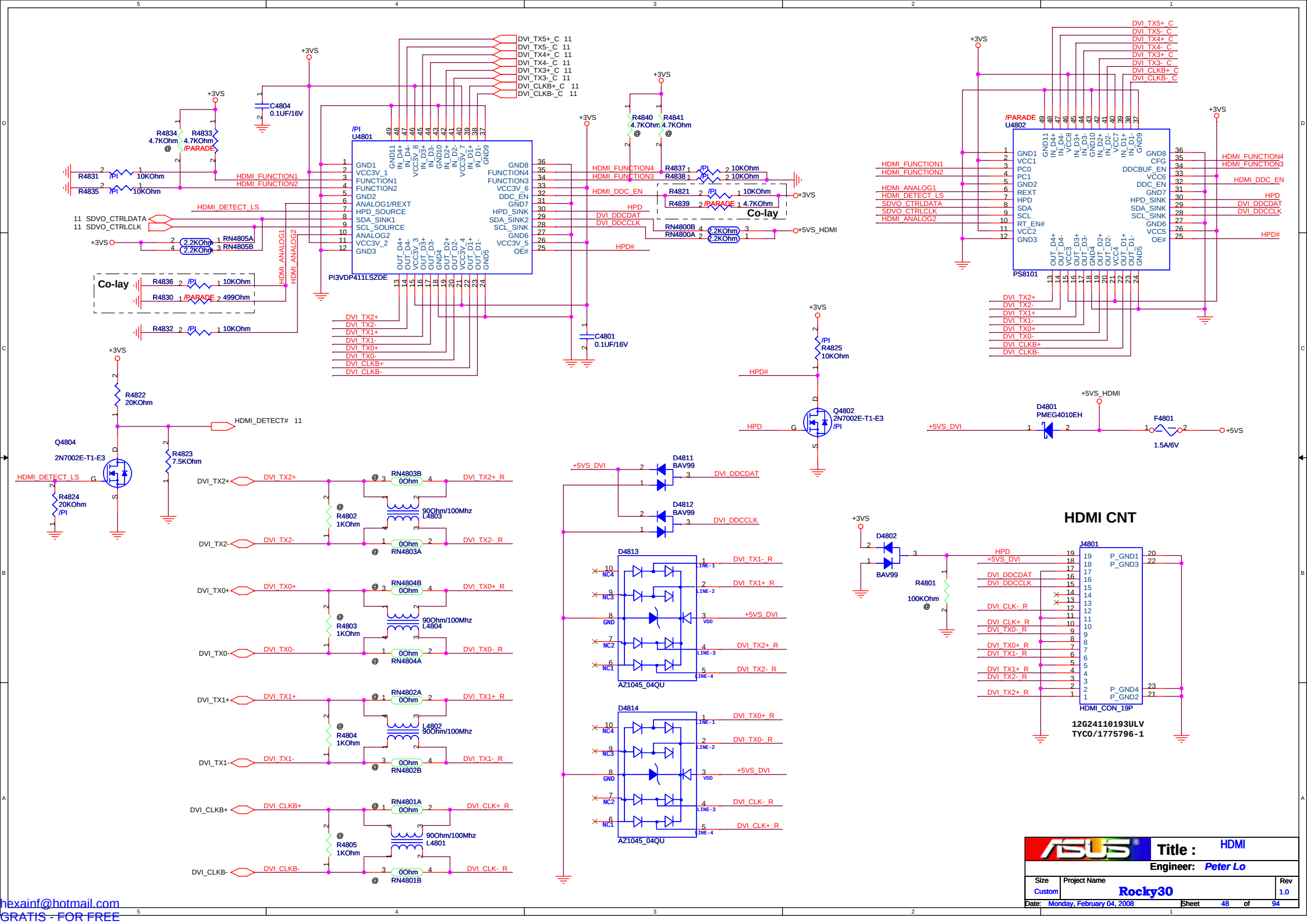


Power Switch for LCD Power



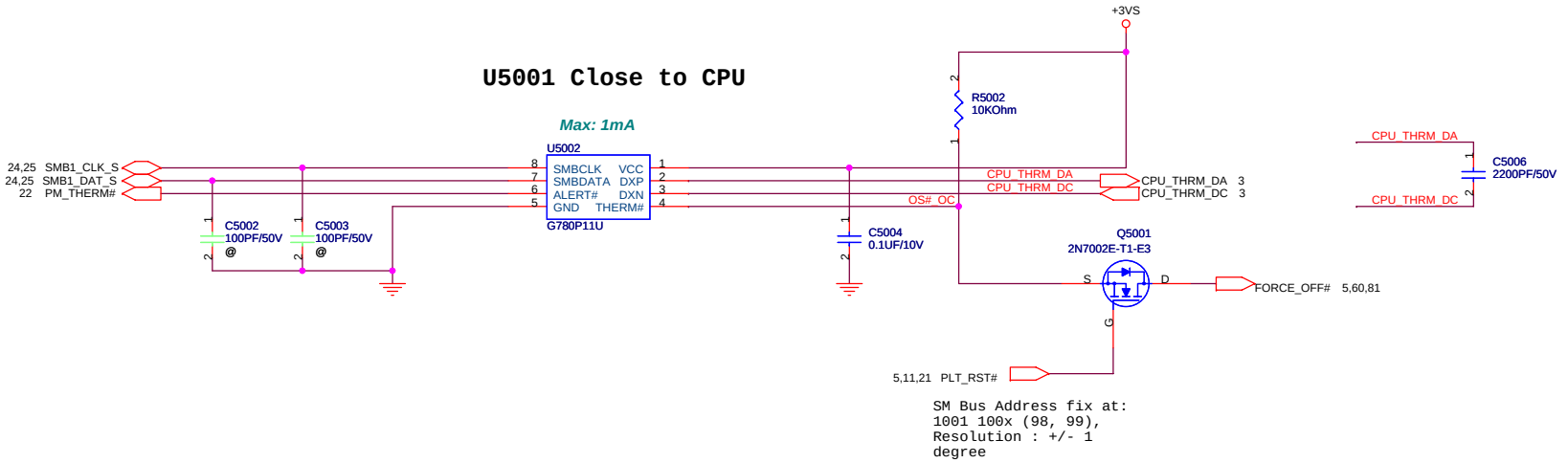
ASUS	Title : LVDS & Inverter CON	
	Engineer: Peter Lo	
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 46 of 94	

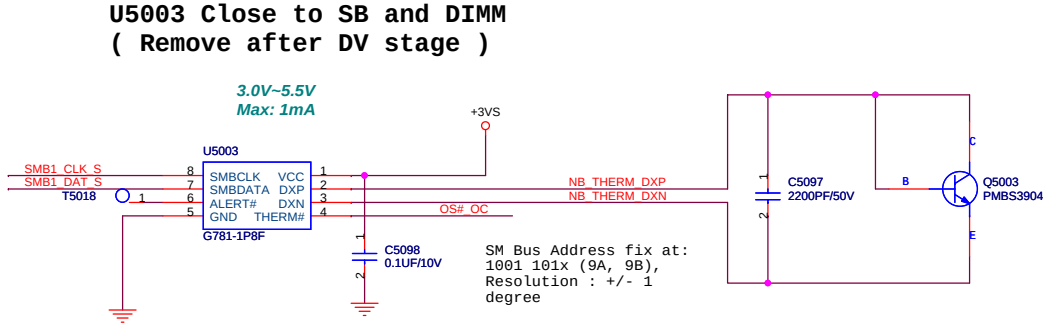
Title :	***	
Engineer:	Peter Lo	
Size: C	Project Name: Rocky30	Rev: 1.0
Date: Thursday, October 18, 2007	Sheet 47 of 94	

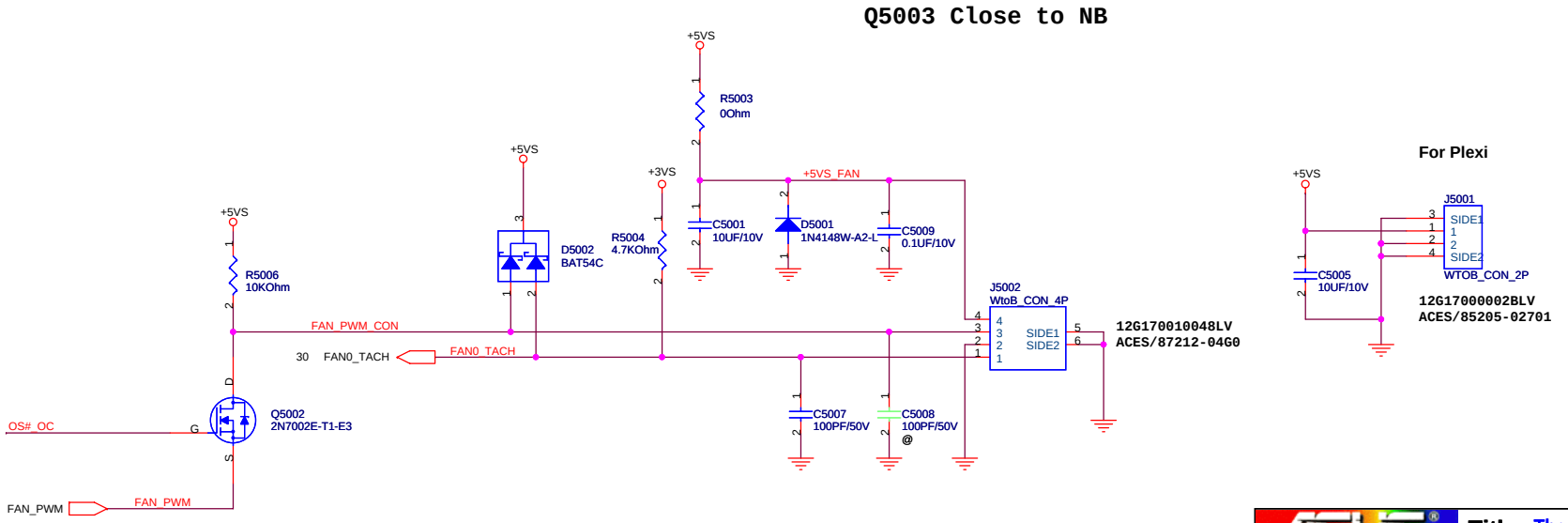


Title :		
Engineer: *Peter Lo*		
Size: A	Project Name: **Rocky30**	Rev: 1.0
Date: Thursday, October 18, 2007	Sheet 49 of 94	

Thermal Sensor

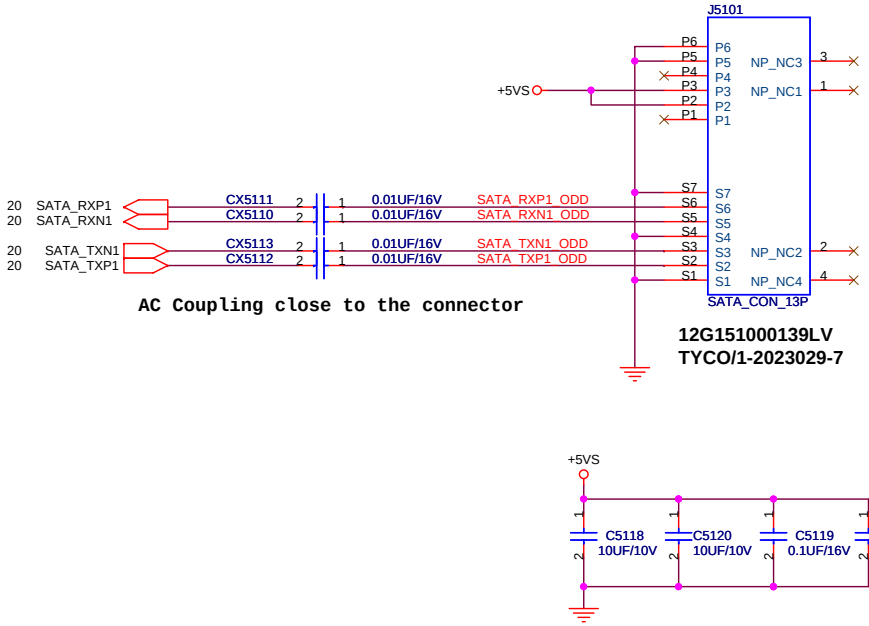






ASUS	Title : Thermal & Fan	
	Engineer: Peter Lo	
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 50 of 94	

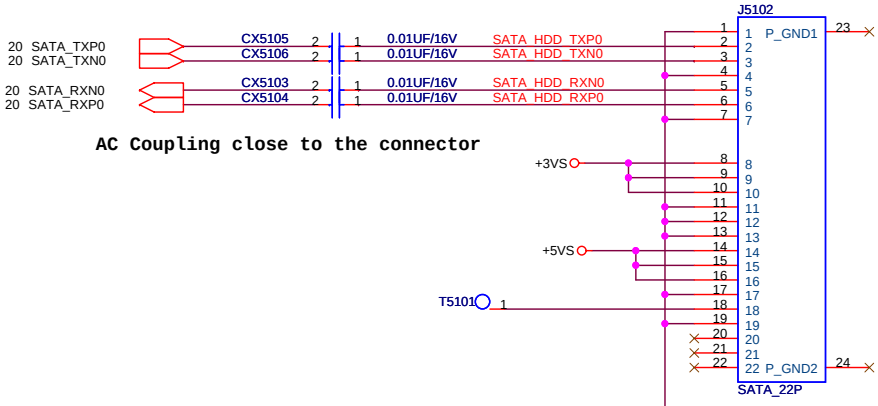
ODD CON



AC Coupling close to the connector

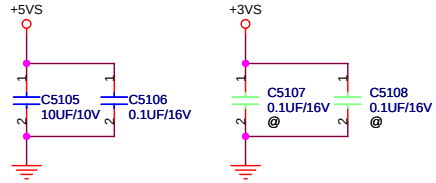
12G151000139LV
TYCO/1-2023029-7

SATA HDD CON

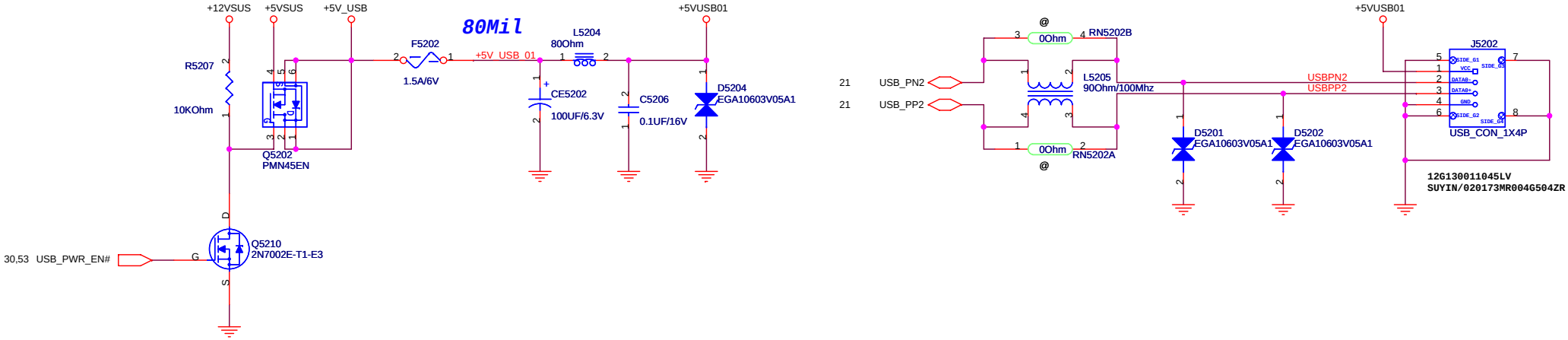


AC Coupling close to the connector

12G15111022PLV
TYCO/1735544-1

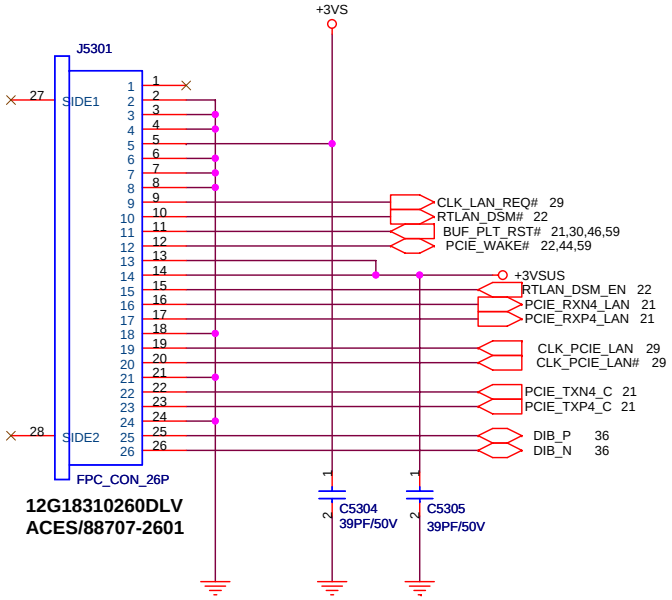


Title : Sata HDD & Swap Bay		
Engineer: *Peter Lo*		
Size: B	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 51 of 94	



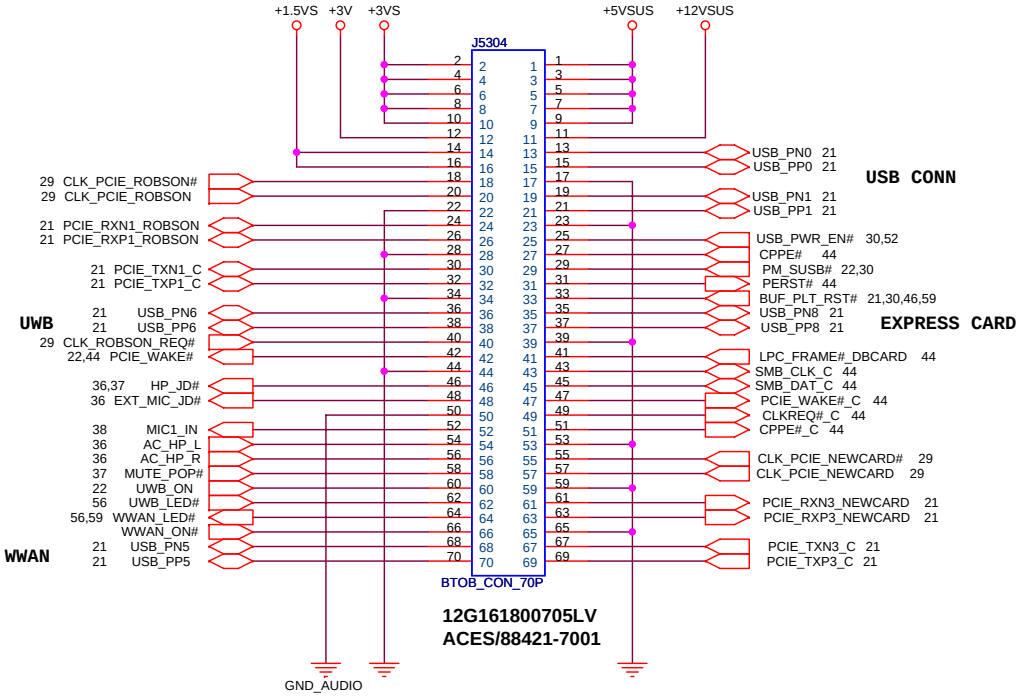
Title : USB CONN		
Engineer: Peter Lo		
Size: B	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 52 of 94	

IO BOARD



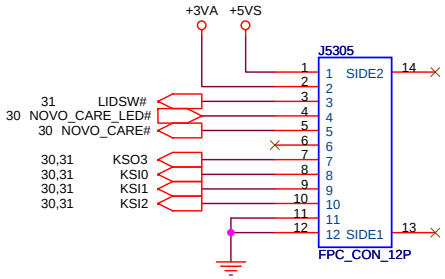
12G18310260DLV
ACES/88707-2601

SMALL BOARD

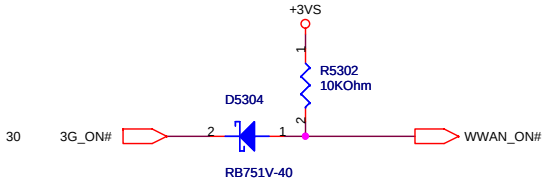


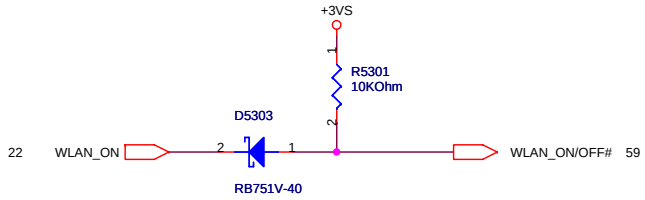
12G161800705LV
ACES/88421-7001

For Media Control Board

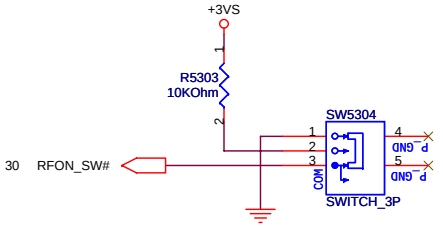


12G18310120BLV
ACES/88278-1200L



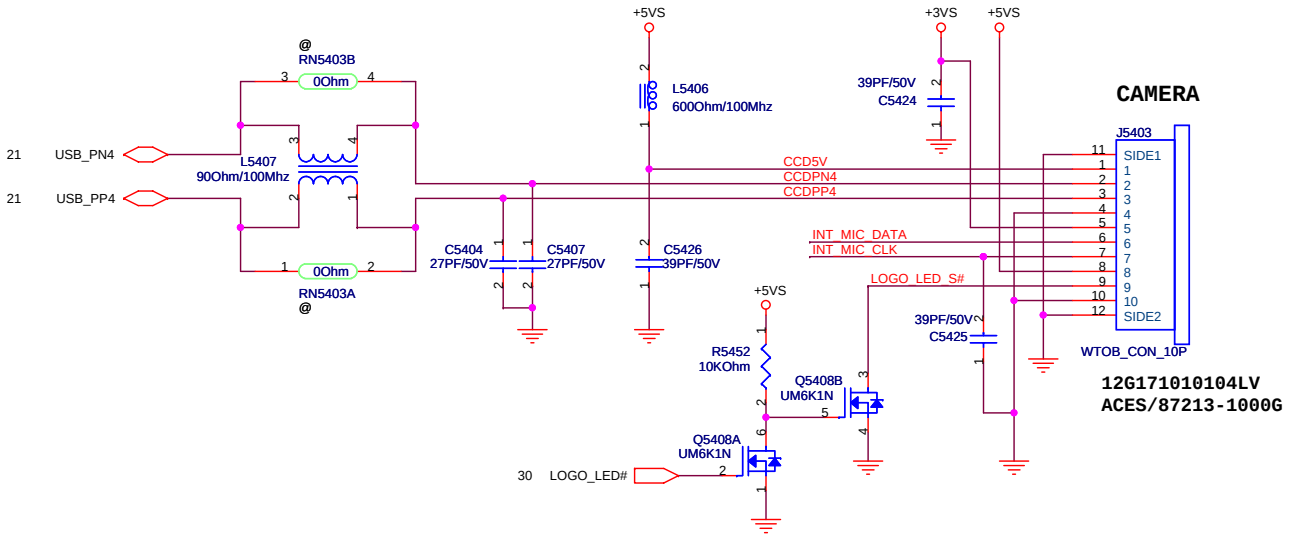


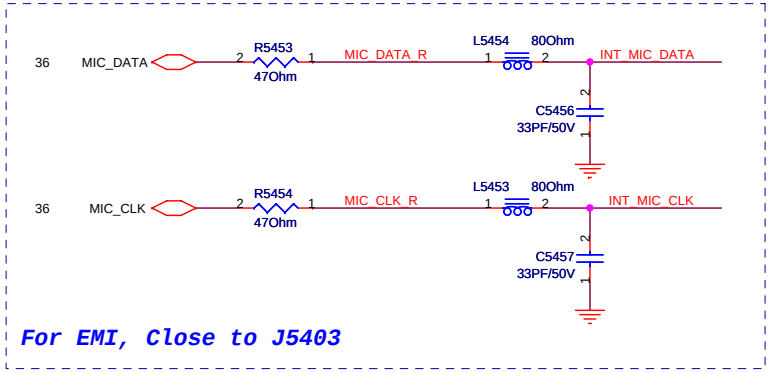
Wireless Switch



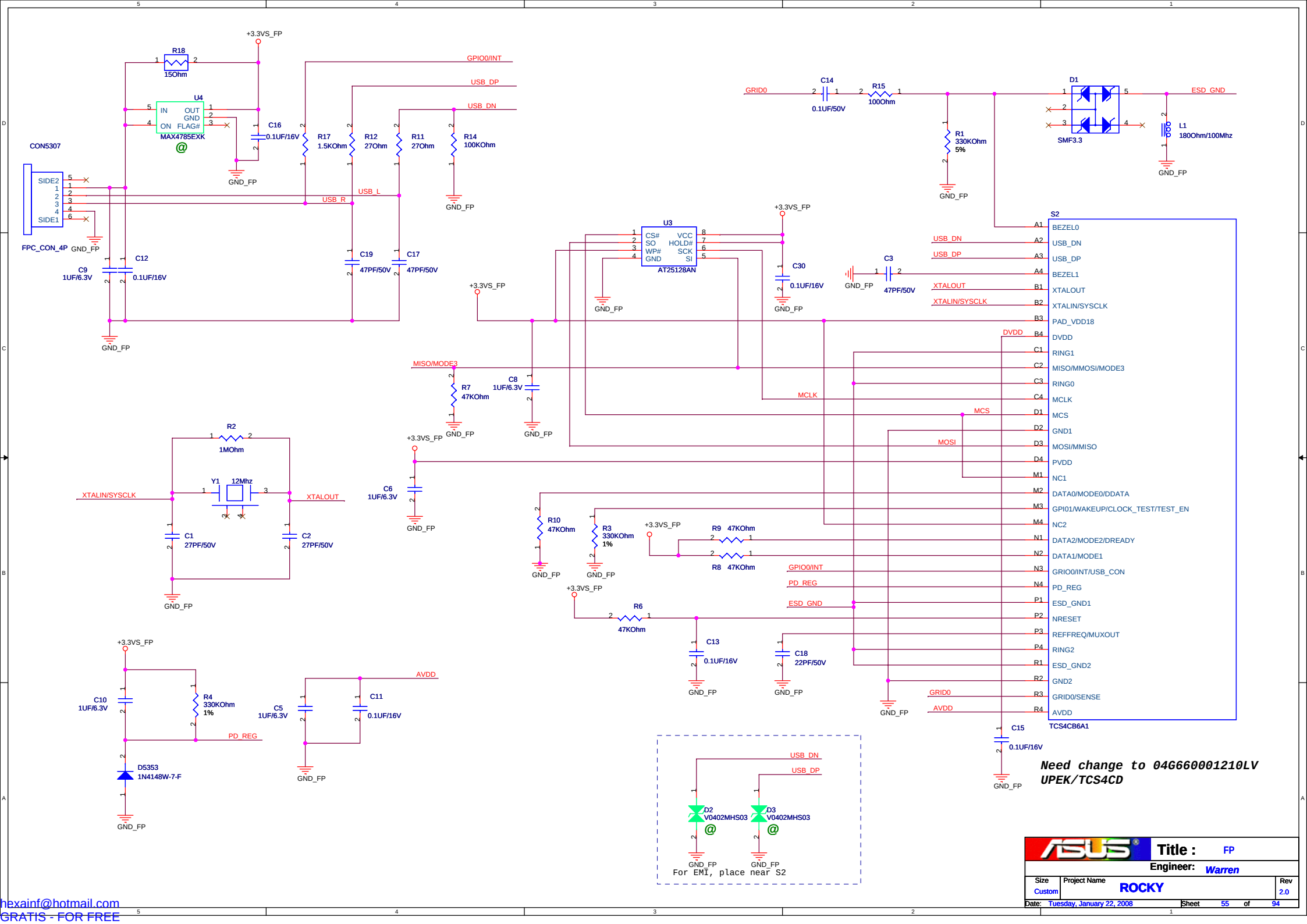
12G091070031LV
ALPS/SSSS710603

Title : IO BOARD		
Engineer: Peter Lo		
Size: B	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 53 of 94	

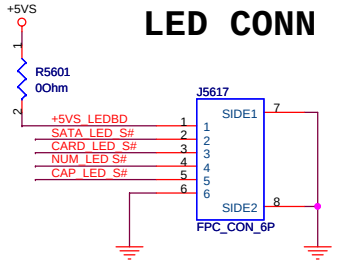




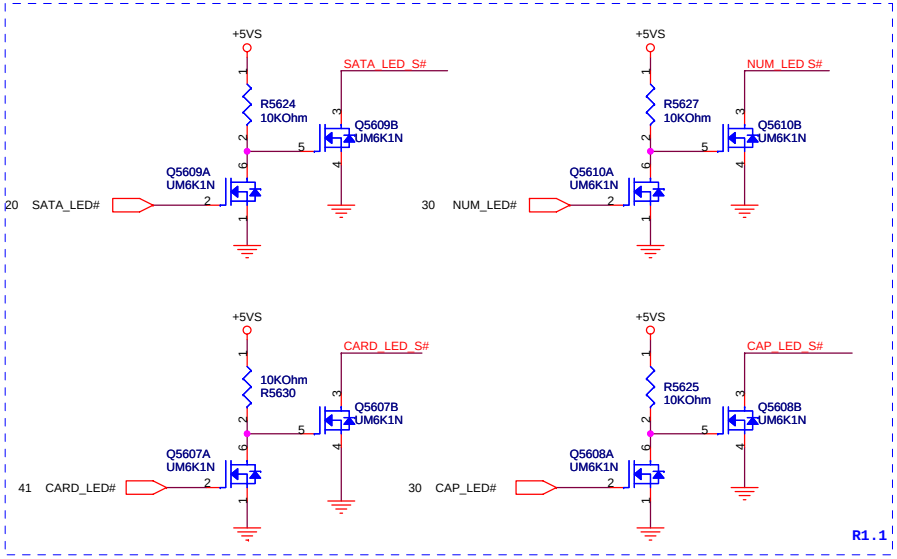
Title : CAMERA		
Engineer: *Peter Lo*		
Size: B	Project Name: **Rocky30**	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 54 of 94	

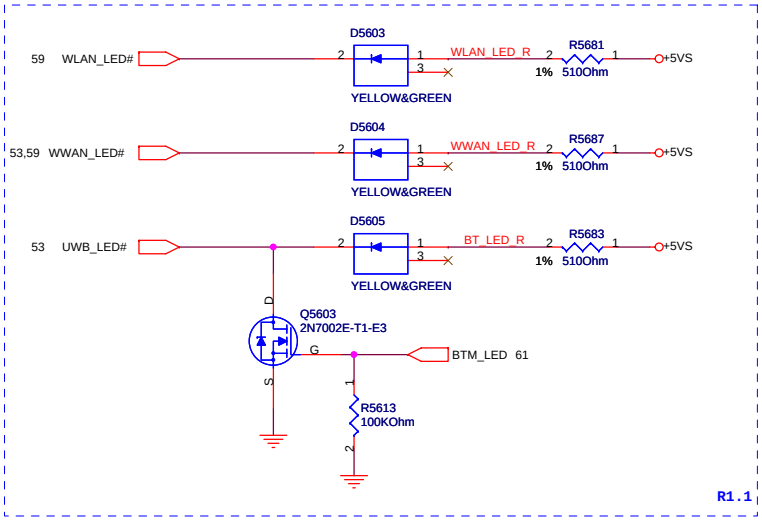


LED CONN

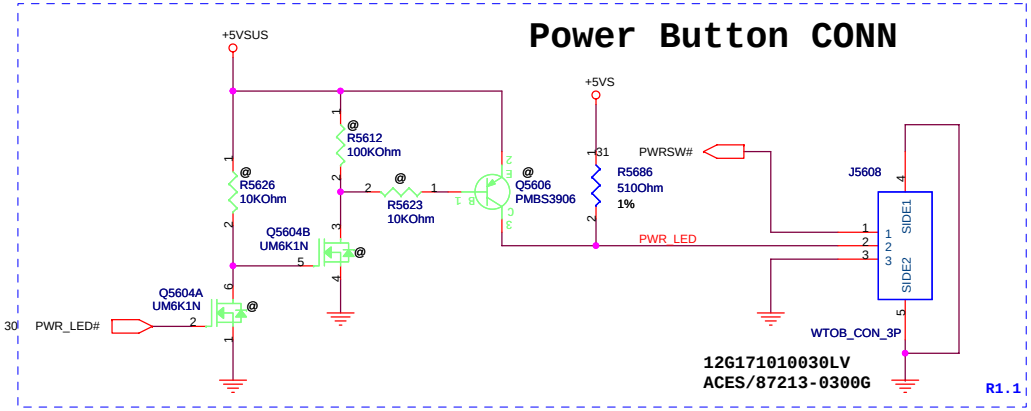


12G183100603LV
ACES/88278-06001

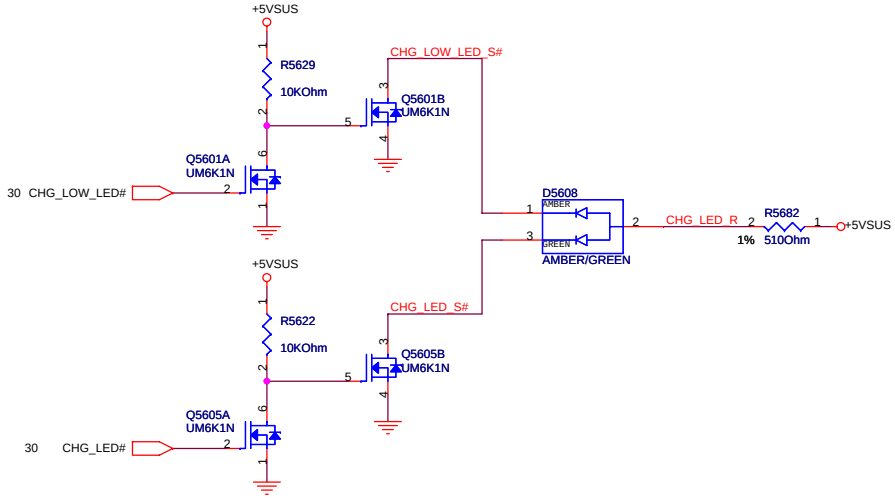


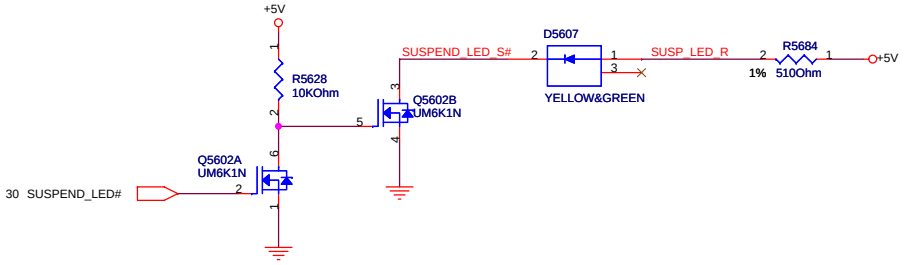


Power Button CONN

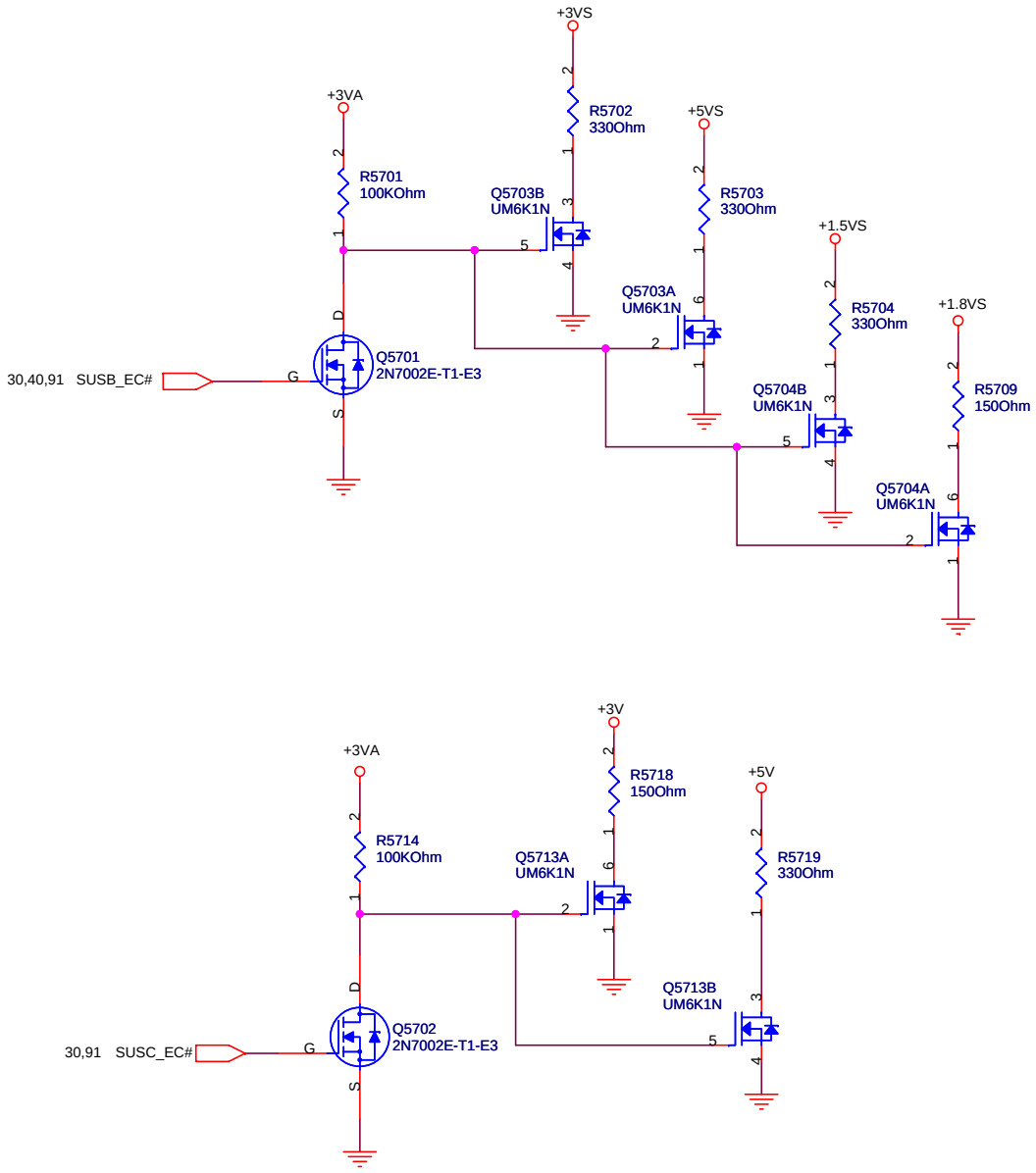


12G171010030LV
ACES/87213-0300G
R1.1

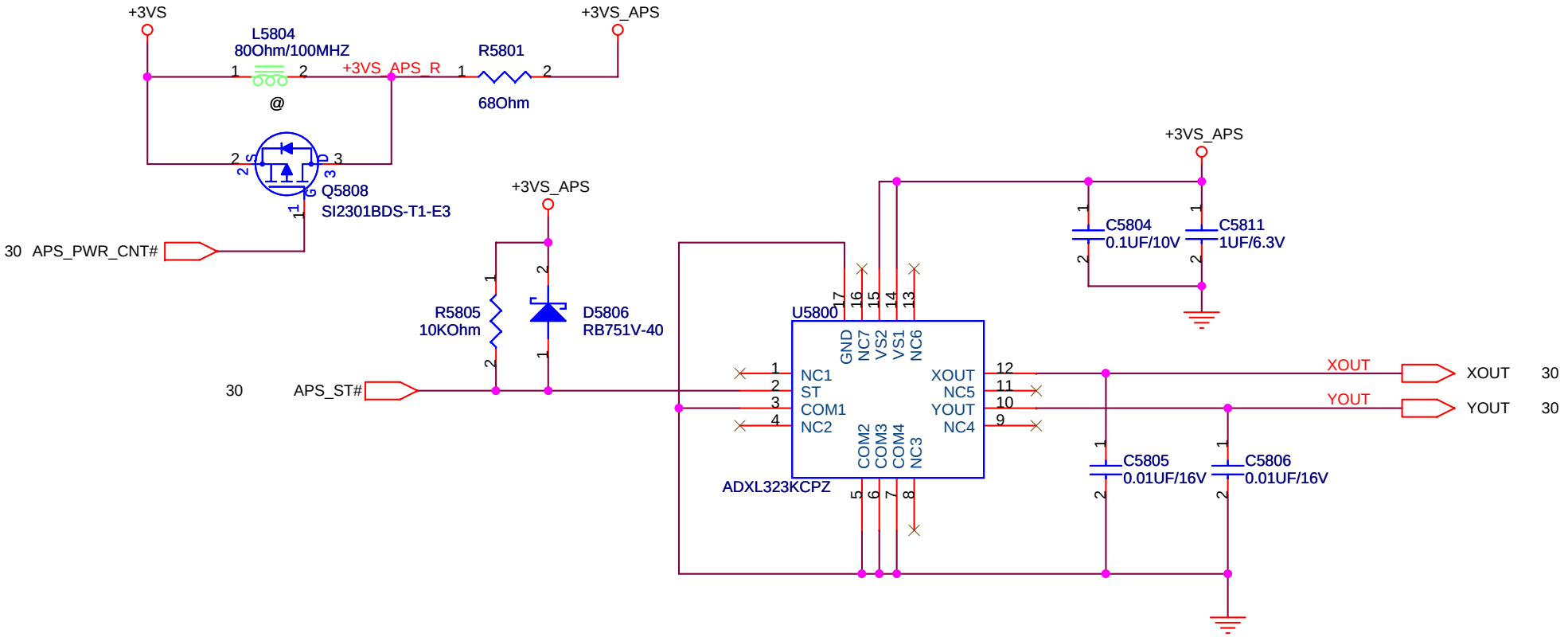




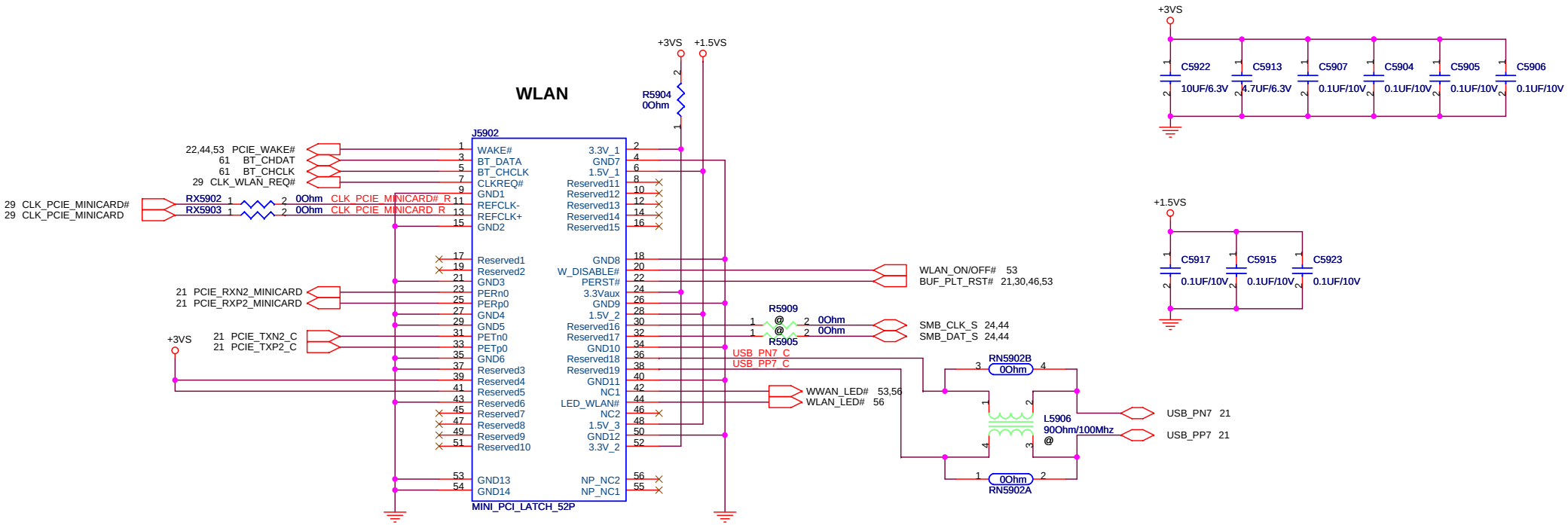
Title : LED/SW		
Engineer: Peter Lo		
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 56 of 94	



Title : DISCHARGE		
Engineer: Peter Lo		
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 57 of 94	

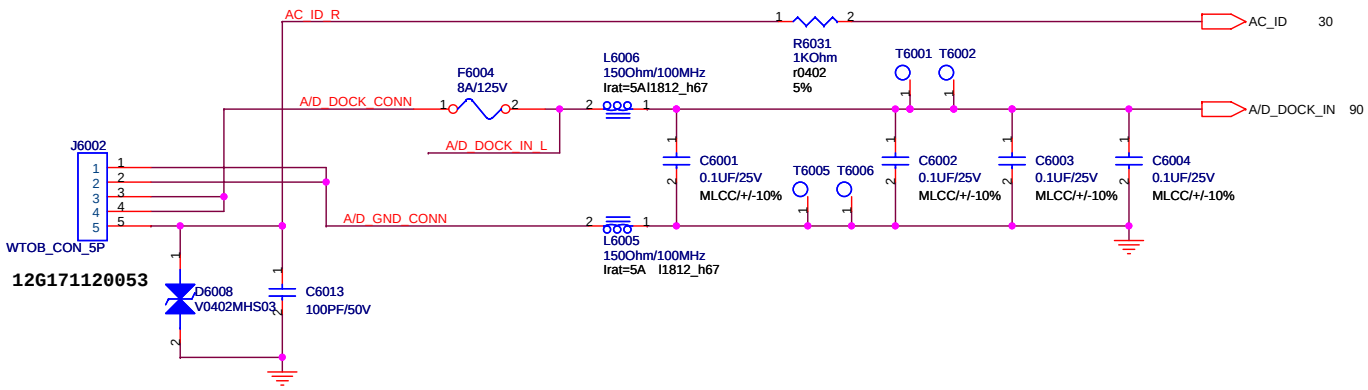


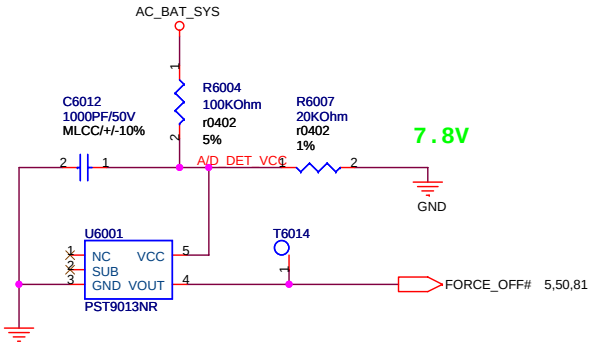
Title : SMS		
Engineer: *Peter Lo*		
Size: A	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 58 of 94	



Title :	Mini Card	
Engineer:	*Peter Lo*	
Size: B	Project Name: **Rocky30**	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 59 of 94	

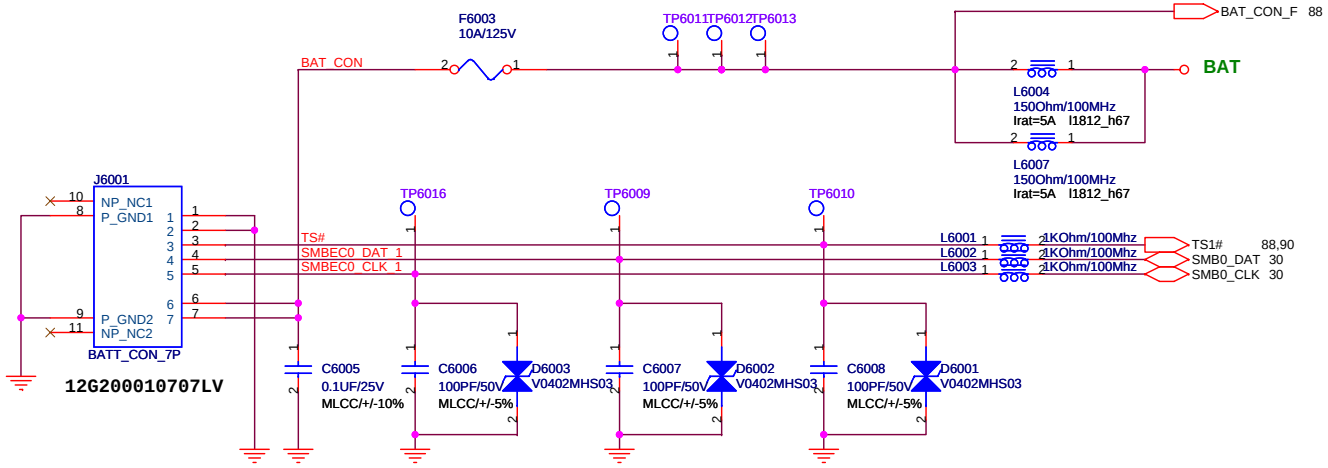
DC IN CONN





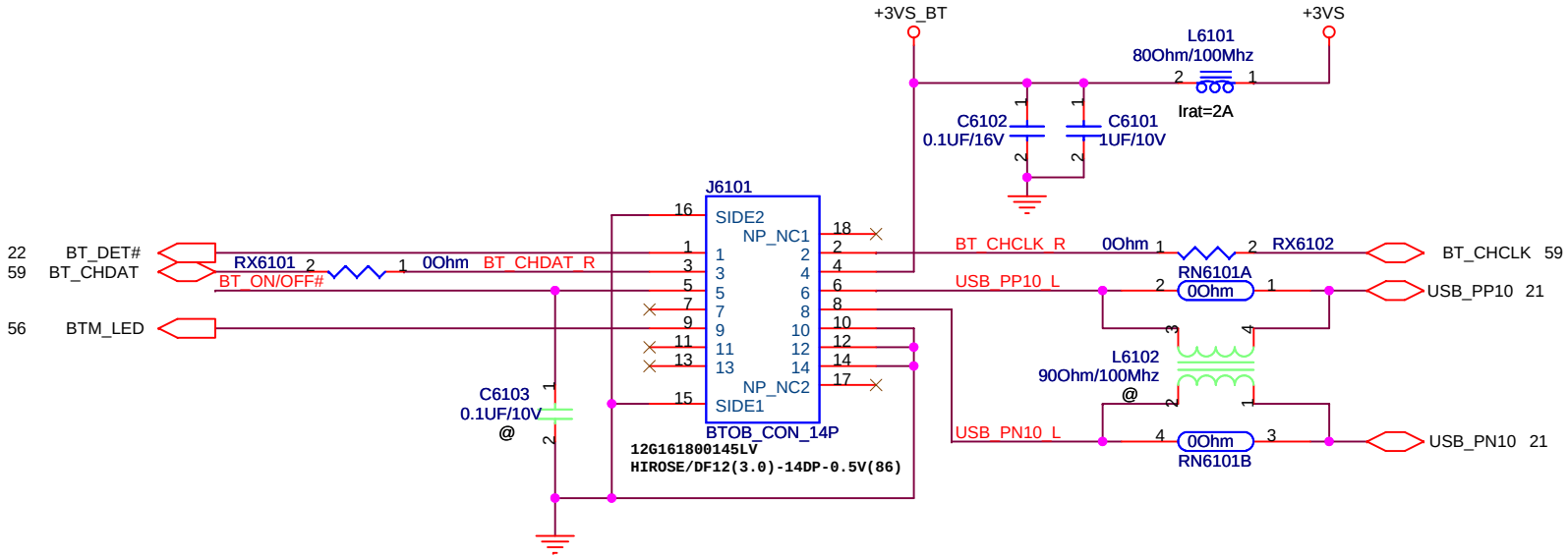
Without Battery & Pull out Adapter

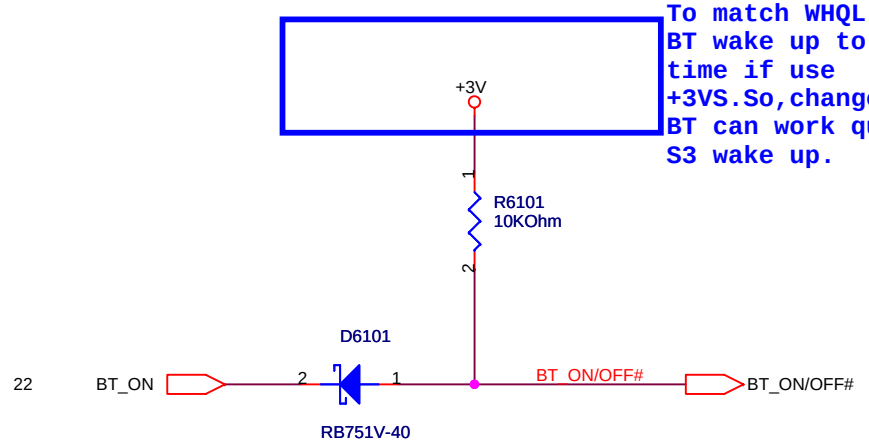
Battery CONN



ASUS	Title : DC Jack & Battery CONN	
	Engineer: Kevin Chang	
Size: Custom	Project Name: Rocky 30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 60 of 94	

Blue Tooth





To match WHQL test.Due to BT wake up to spend much time if use +3VS.So,change to +3V,let BT can work quickly when S3 wake up.

From GPIO27 ICH9

Title : BlueTooth			
Engineer: Peter Lo			
Size: A4	Project Name: Rocky30		Rev: 1.0
Date: Monday, February 04, 2008		Sheet 61 of 94	

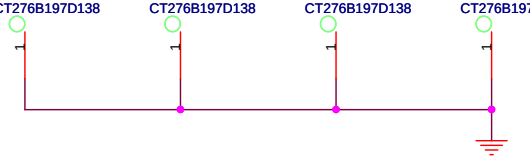
Title :	***
Engineer:	*Peter Lo*
Size: A4	Project Name: **Rocky30**
Rev: 1.0	
Date: Thursday, October 18, 2007	Sheet 62 of 94

Title :	***
Engineer:	Peter Lo
Size: A4	Project Name: Rocky30
Rev: 1.0	
Date: Thursday, October 18, 2007	Sheet 63 of 94

Title :	
Engineer:	Peter Lo
Size: A	Project Name: Rocky30
Rev:	1.0
Date:	Thursday, October 18, 2007
Sheet	64 of 94

CPU

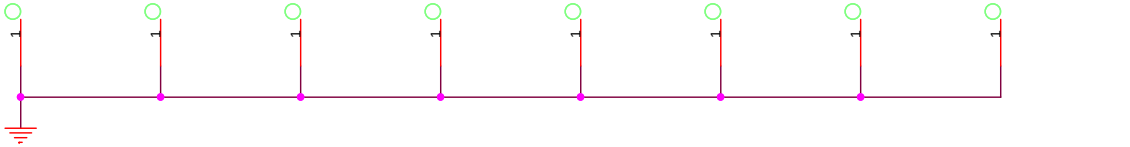
@ H6513 CT276B197D138
@ H6514 CT276B197D138
@ H6515 CT276B197D138
@ H6516 CT276B197D138



CT276B197D138

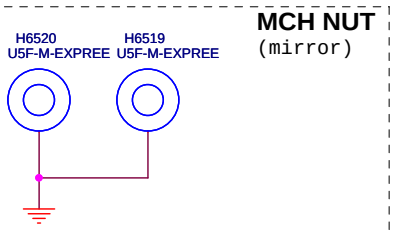
TOP 5CT236B236X236D91 PTH

@ H6508 5CT236B236X236D91
@ H6517 5CT236B236X236D91
@ H6509 5CT236B236X236D91
@ H6510 5CT236B236X236D91
@ H6511 5CT236B236X236D91
@ H6512 5CT236B236X236D91
@ H6506 5CT236B236X236D91
@ H6518 5CT236B236X236D91



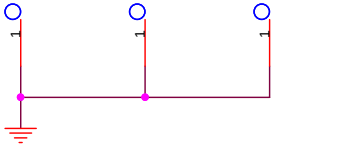
MCH NUT (mirror)

H6520 U5F-M-EXPREE
H6519 U5F-M-EXPREE



CR236X236D91 PTH

@ H6507 CR236X236D91
@ H6529 CR236X236D91
@ H6504 CR236X236D91



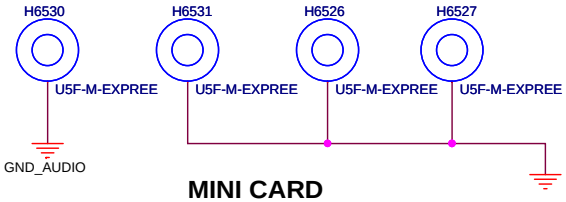
BOT 5CT236B236X236D91 PTH

@ H6528 5CT236B236X236D91

MINI CARD

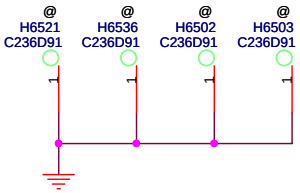
H6530 U5F-M-EXPREE
H6531 U5F-M-EXPREE
H6526 U5F-M-EXPREE
H6527 U5F-M-EXPREE

GND_AUDIO



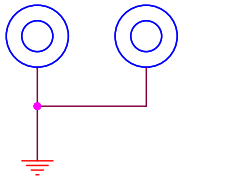
C236D91 PTH

@ H6521 C236D91
@ H6536 C236D91
@ H6502 C236D91
@ H6503 C236D91



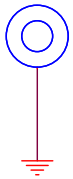
For Fan Stand Off
C236B189D150 PTH (mirror)

H6524 U5F-M-EXPREE
H6525 U5F-M-EXPREE



For KB Stand Off
C236B189D150 PTH

H6533 U5F-M-EXPREE



@ H6534 SMD169X169

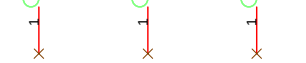
For BT StandOff

H6546 ROCKY50-1A

TOOLING HOLE

For ICT

@ H6522 C103D103N
@ H6523 C103D103N
@ H6532 C103D103N

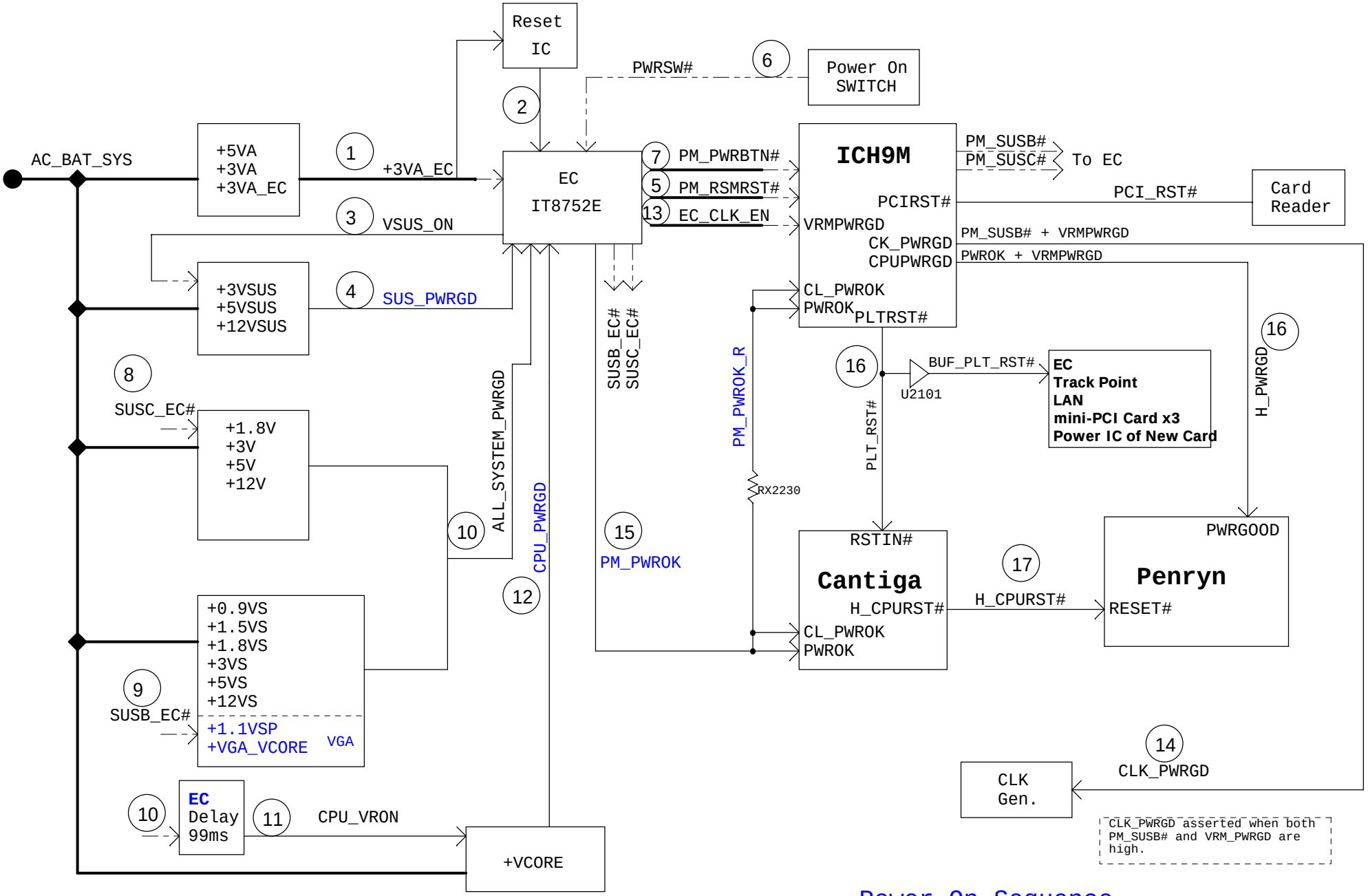


Title: MDC NUT & Hinksink NUT		
Engineer: Peter Lo		
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Tuesday, January 22, 2008	Sheet 65 of 94	

Title :	***
Engineer:	*Peter Lo*
Size: Custom	Project Name: **Rocky30**
Rev: 1.0	
Date: Thursday, October 18, 2007	Sheet 66 of 94

Title : ***		
Engineer: Peter Lo		
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Thursday, October 18, 2007	Sheet 67 of 94	

Title :	***
Engineer:	Peter Lo
Size: Custom	Project Name: Rocky30
Rev:	1.0
Date: Thursday, October 18, 2007	Sheet 68 of 94



Power On Sequence

1 → 17

ASUS	Title : Power Sequence	
	Engineer: Peter Lo	
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Monday, November 05, 2007	Sheet 69 of 94	

Title : ***

Engineer: Peter Lo

Size	Project Name	Rev
B	Rocky30	1.0

Date: Thursday, October 18, 2007 Sheet 70 of 94

Title : ***

Engineer: *Peter Lo*

Size	Project Name	Rev
B	Rocky30	1.0

Date: Thursday, October 18, 2007 Sheet 71 of 94

Title :	***
Engineer:	Peter Lo
Size: B	Project Name: Rocky30
Rev: 1.0	
Date: Thursday, October 18, 2007	Sheet 72 of 94

Title :	***
Engineer:	Peter Lo
Size: B	Project Name: Rocky30
Rev:	1.0
Date:	Thursday, October 18, 2007
Sheet	73 of 94

Title :	***
Engineer:	Peter Lo
Size: B	Project Name: Rocky30
Rev:	1.0
Date:	Thursday, October 18, 2007
Sheet	74 of 94

Title :	***
Engineer:	Peter Lo
Size: B	Project Name: Rocky30
Rev:	1.0
Date:	Thursday, October 18, 2007
Sheet	75 of 94

Title : ***

Engineer: *Peter Lo*

Size	Project Name	Rev
B	Rocky30	1.0

Date: Thursday, October 18, 2007 Sheet 76 of 94

Title :	***
Engineer:	Peter Lo
Size: B	Project Name: Rocky30
Rev: 1.0	
Date: Thursday, October 18, 2007	Sheet 77 of 94

Title : ***

Engineer: *Peter Lo*

Size	Project Name	Rev
B	Rocky30	1.0

Date: Thursday, October 18, 2007 Sheet 78 of 94

Title :	
Engineer:	Peter Lo
Size: A	Project Name: Rocky30
Rev:	1.0
Date:	Thursday, October 18, 2007
Sheet	79 of 94

IMVP6 CPU VCORE REGULATOR

3.3V level logic level: DPRSLPVR, SHDN#
1.05V level logic: VID, PSI#, DPRSTP#
POUT=(VCSN2-VGNDS)x(CSP1-CNS1+CSP2-CSN2)/16.67mV

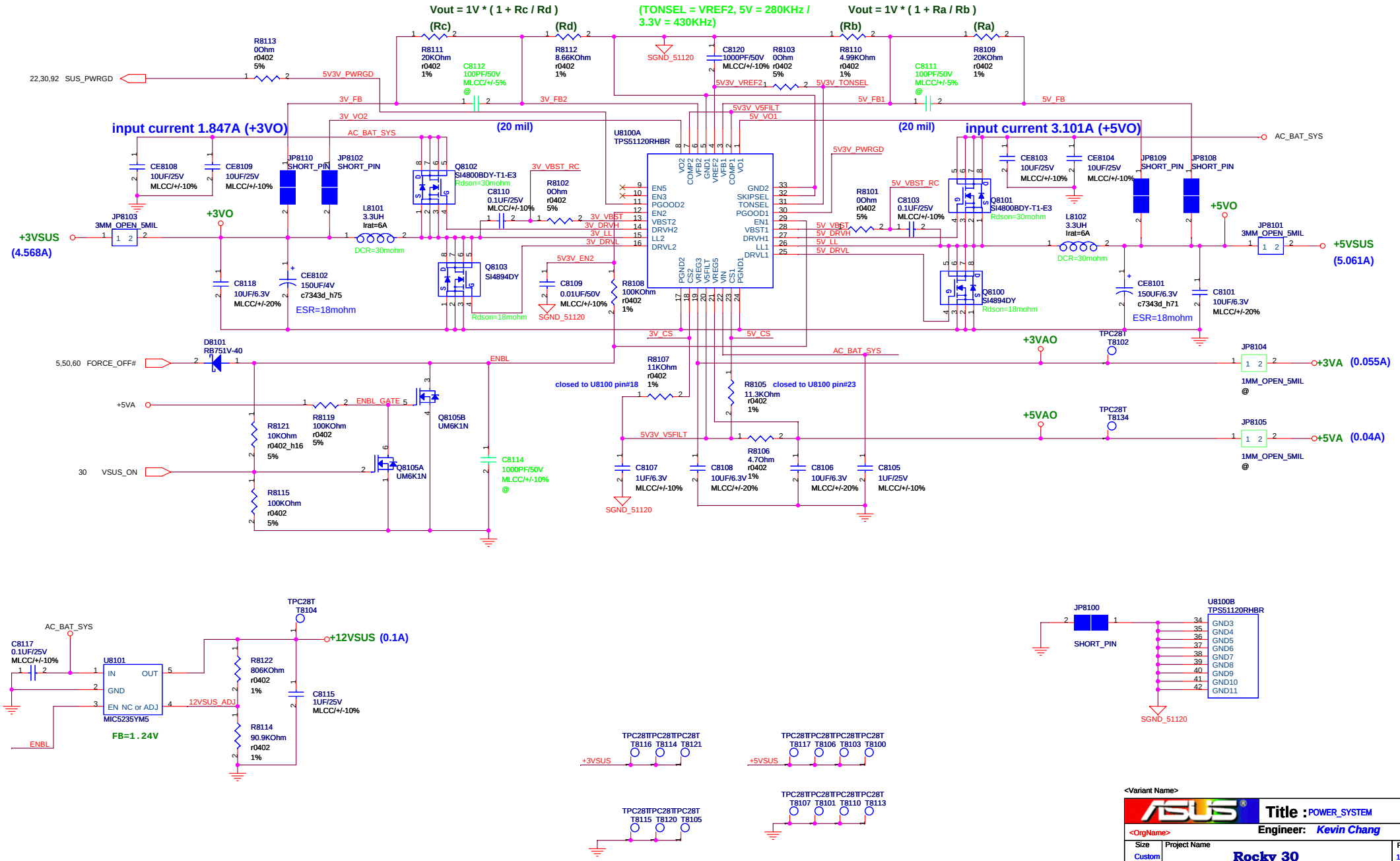
FSW=297.8kHz
Slewrate=12.5mV/us
VPS=-2.1mV/A

Max input ripple: 5.59A

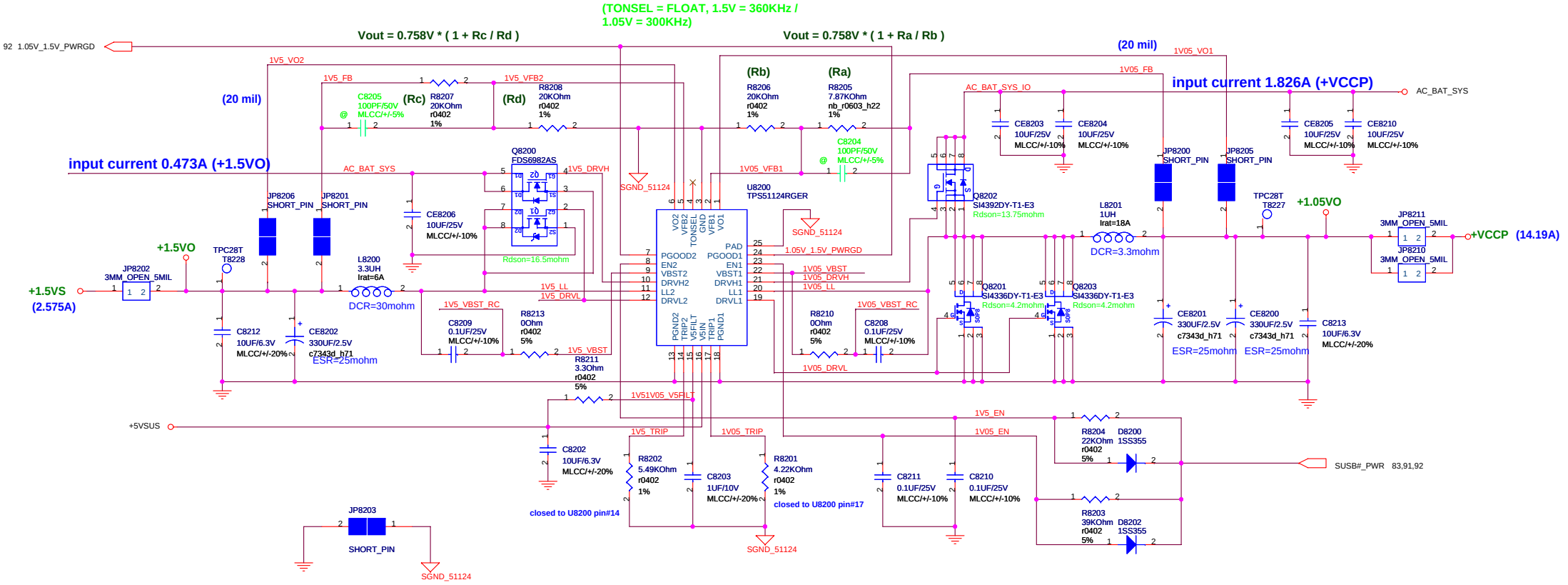
Max input ripple: 5.59A

Title :	POWER_VCORE
<OrgName>	Engineer: Kevin Chang
Size: Custom	Project Name: Rocky 30
Rev	1.0
Date: Monday, February 04, 2008	Sheet 80 of 94

+5V / +3.3V POWER SUPPLY



+1.5VS / +VCCP POWER SUPPLY



<Variant Name>

ASUS

Title : POWER_I/O_1.5VS & 1.05VS

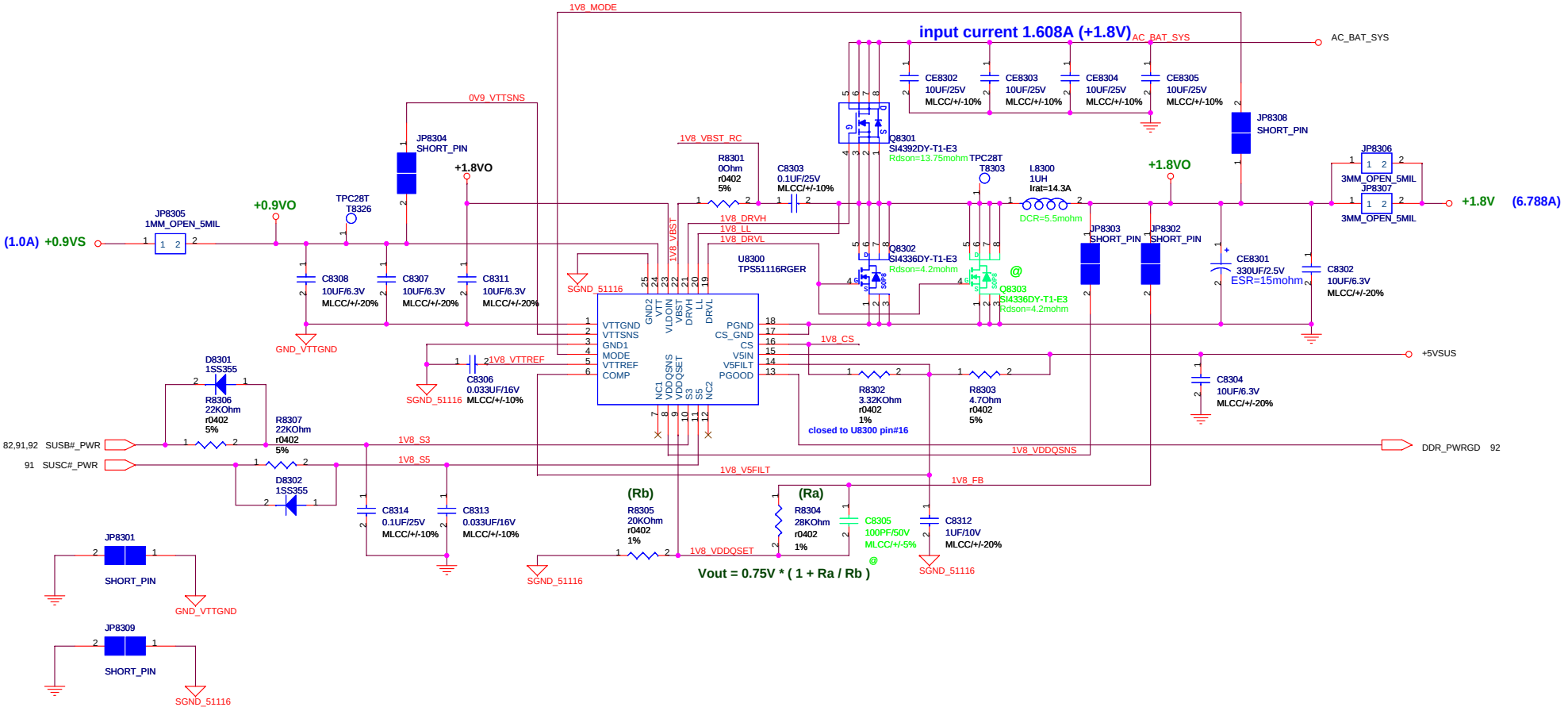
<OrgName>

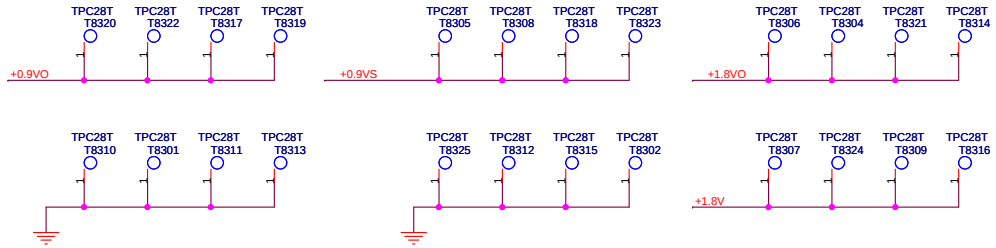
Engineer: Kevin Chang

Size	Project Name	Rev
Custom	Rocky 30	1.0

Date: Monday, February 04, 2008 Sheet 82 of 94

+1.8V / +0.9VS POWER SUPPLY





<Variant Name>

Title :	POWER_I/O_DDR & VTT
<OrgName>	Engineer: Kevin Chang
Size: Custom	Project Name: Rocky 30
Rev	1.0
Date: Monday, February 04, 2008	Sheet 83 of 94

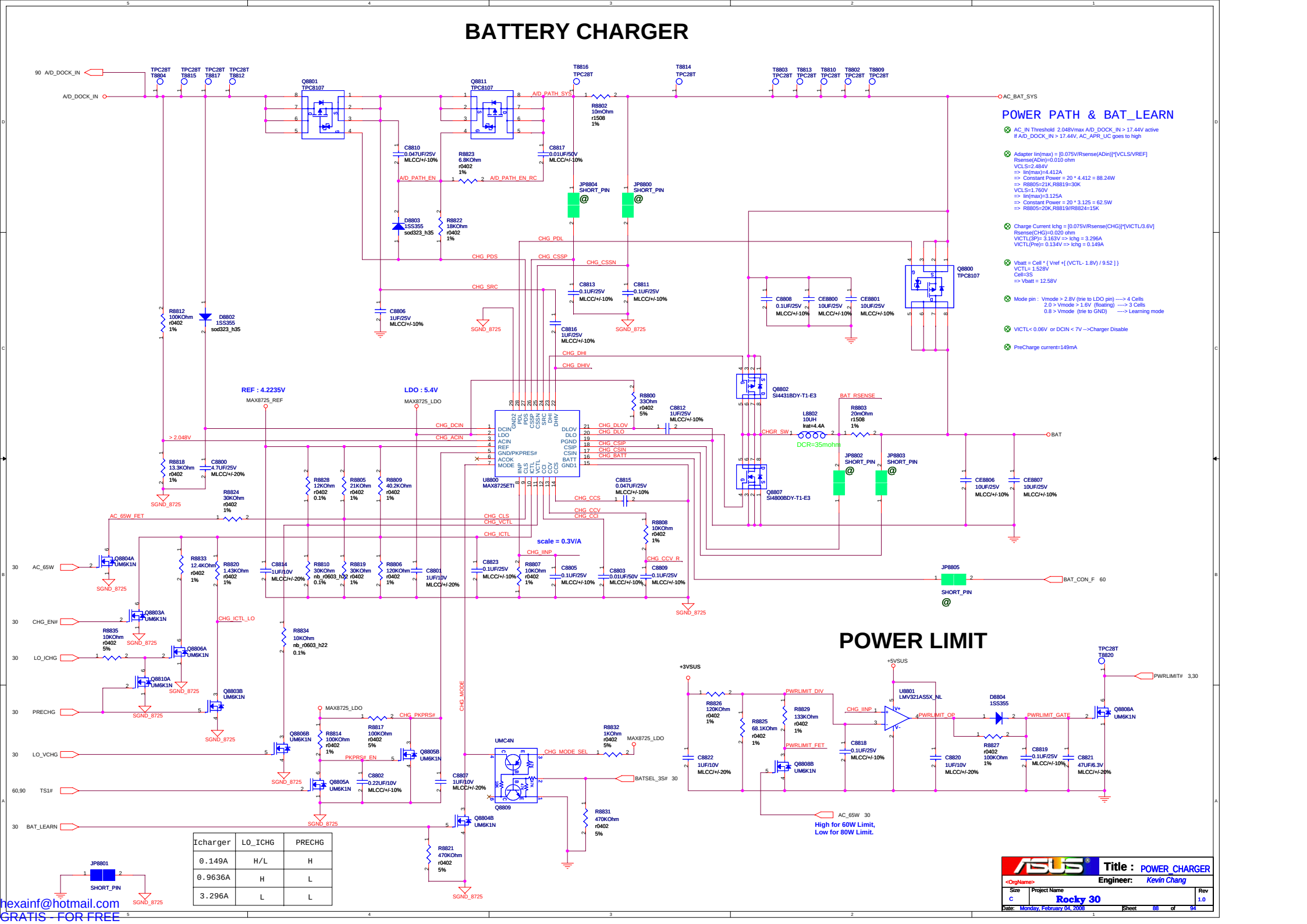
Title : PWR_-****		
Engineer: <OrgName>		
Size: A4	Project Name: Rocky30	Rev: 1.0
Date: Saturday, January 26, 2008	Sheet 84 of 94	

Title :		
Engineer: Kevin Chang		
<OrgName>		
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Friday, January 11, 2008	Sheet 85 of 94	

Title :	PWR_-****	
<OrgName>	Engineer:	Kevin Chang
Size: A4	Project Name: Rocky30	Rev: 1.0
Date: Friday, January 11, 2008	Sheet 86 of 94	

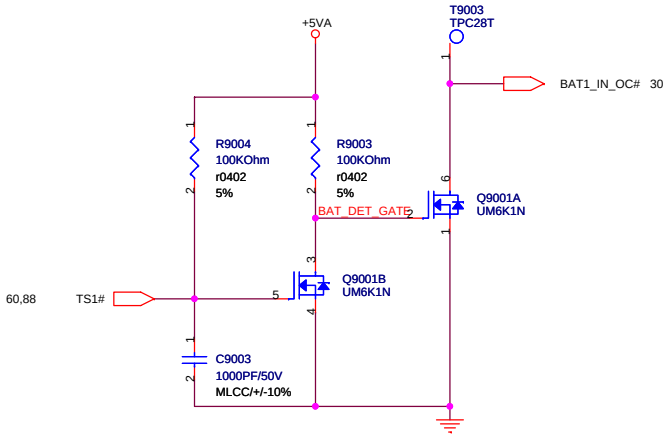
Title :	POWER_SHUTDOWN#	
Engineer:	<OrgName>	
Size: A4	Project Name: Rocky30	Rev: 1.0
Date: Saturday, January 26, 2008	Sheet 87 of 94	

BATTERY CHARGER

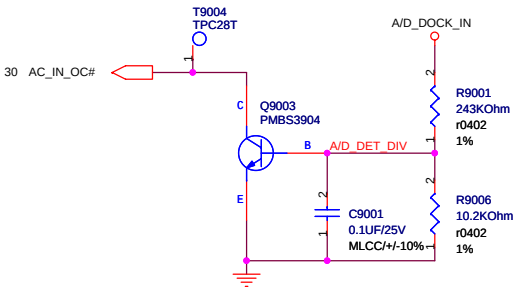


Title :	TFT-LCD DRIVE	
<OrgName>	Engineer:	
Size: A4	Project Name: Rocky30	Rev: 1.0
Date: Friday, January 11, 2008	Sheet 89 of 94	

BATTERY IN DETECT

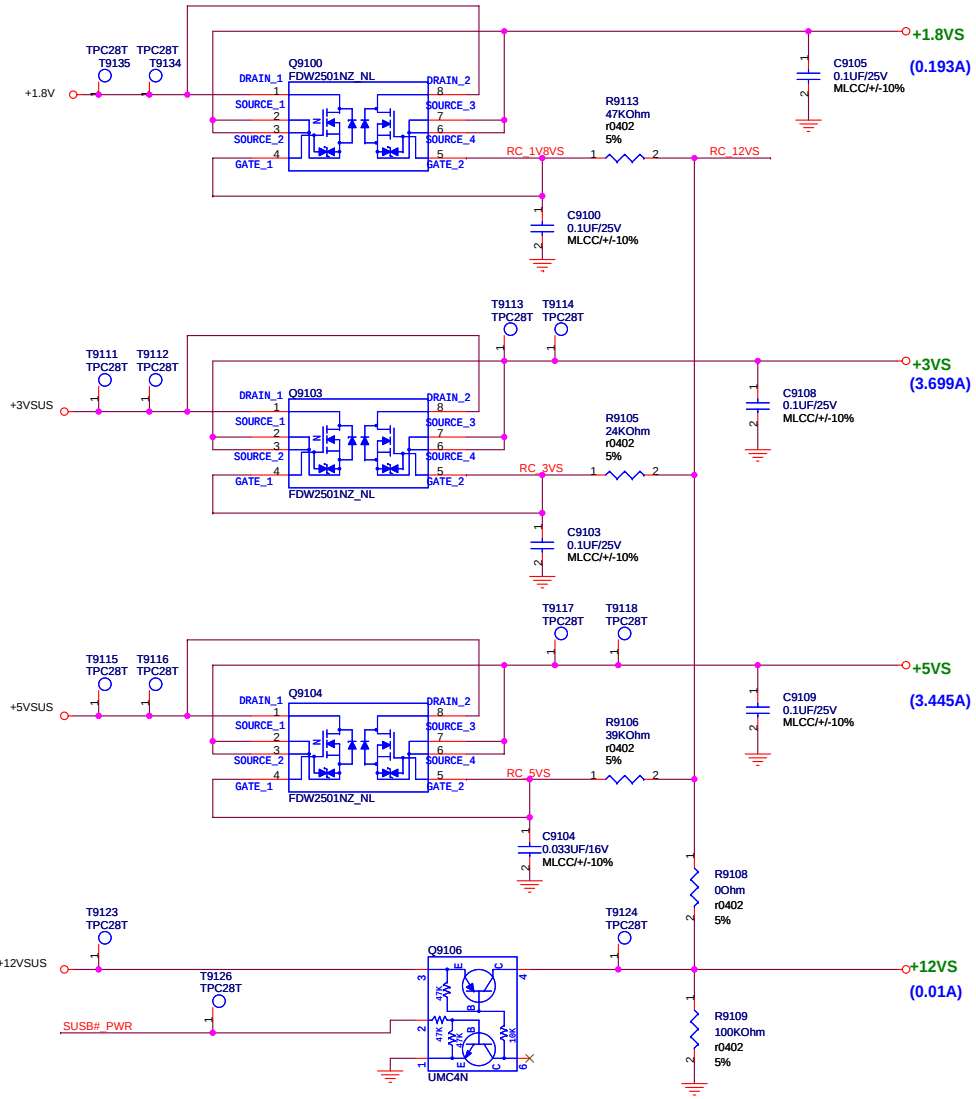


ADAPTER IN DETECT

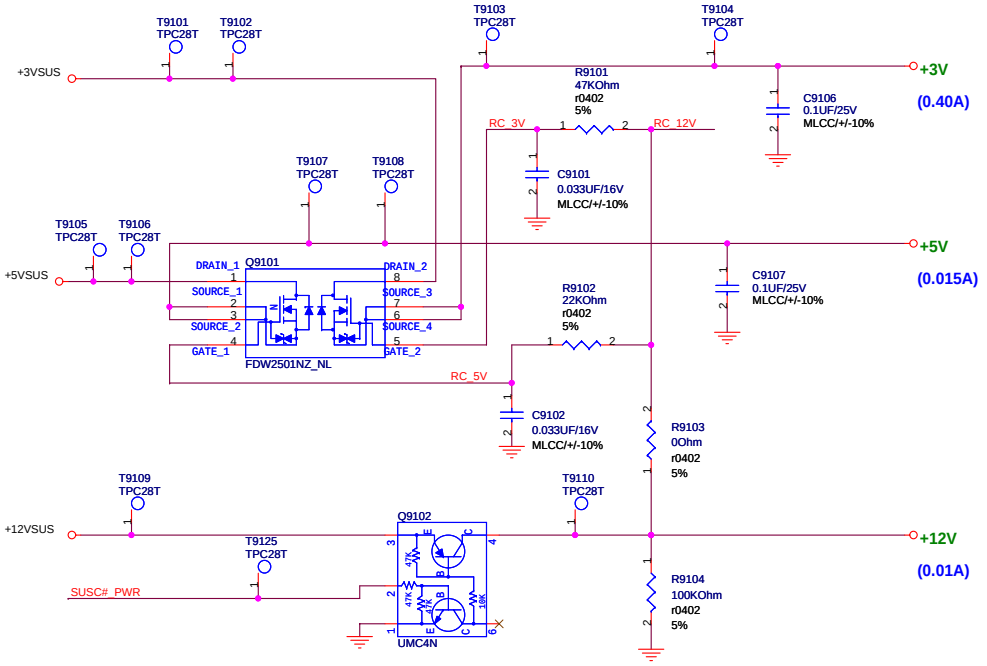


ASUS	Title : POWER_DETECT	
<OrgName>	Engineer: Kevin Chang	
Size: A3	Project Name: Rocky 30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 90 of 94	

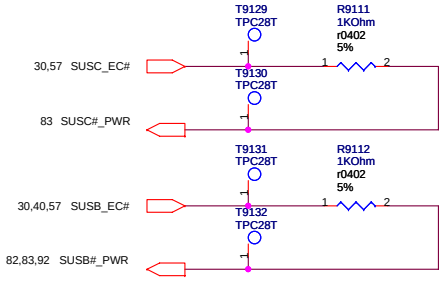
SUSB#_PWR Load SW



SUSC#_PWR Load SW

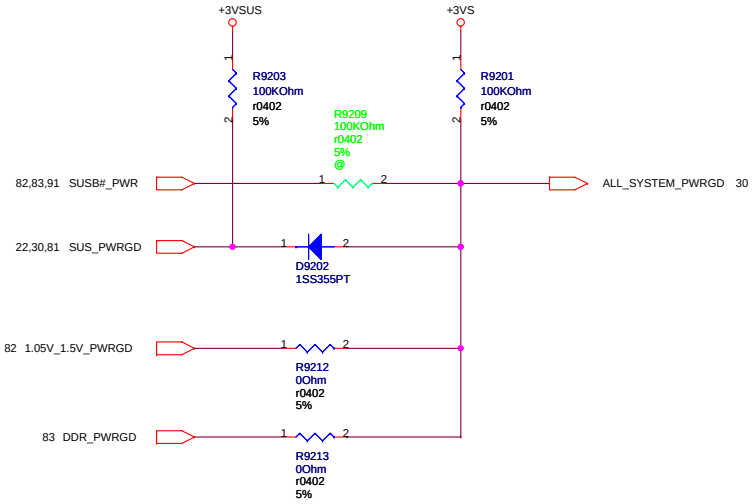


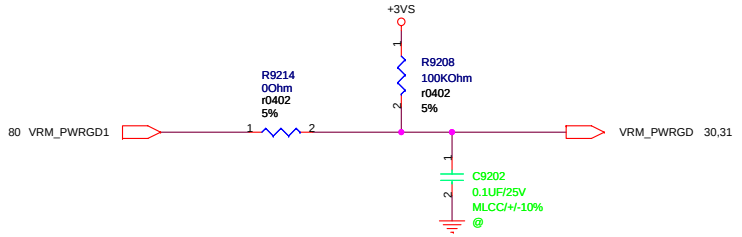
Enable Signal



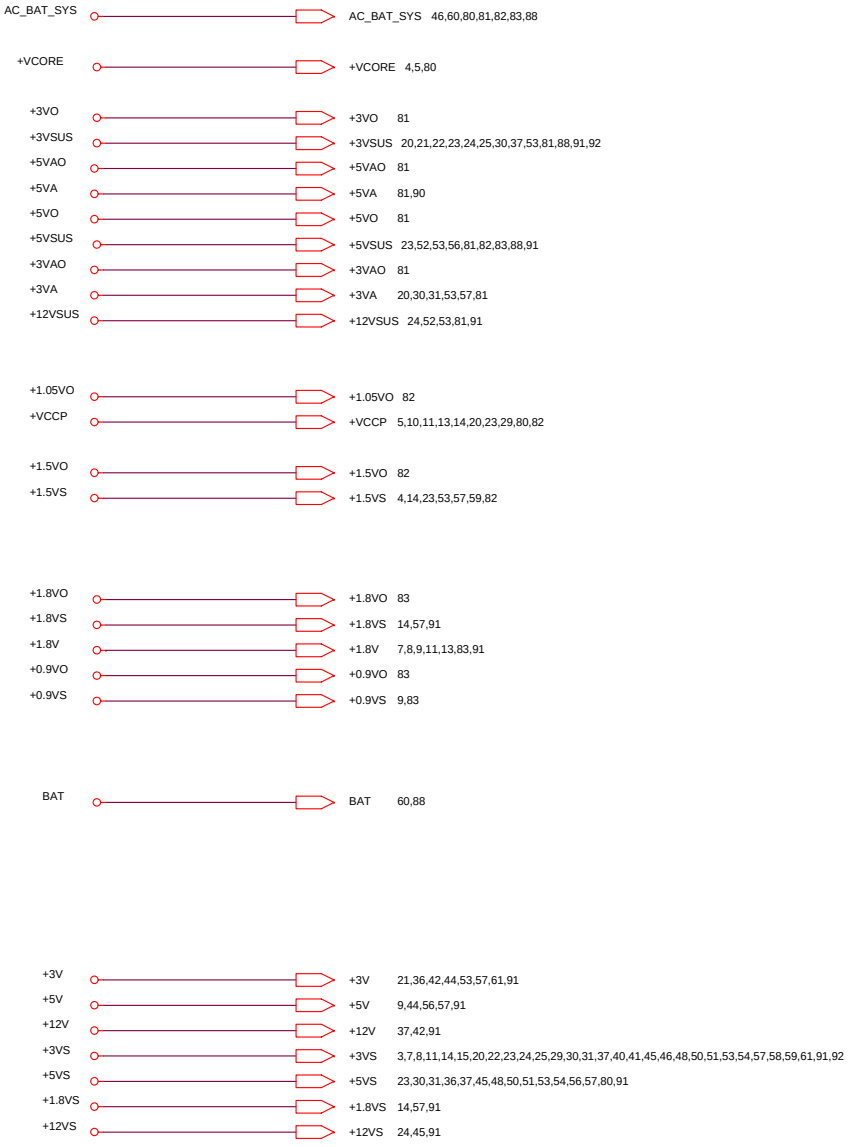
ASUS	Title : POWER_LOAD SWITCH	
<OrgName>	Engineer: Kevin Chang	
Size: Custom	Project Name: Rocky 30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 91 of 94	

POWER GOOD DETECTER

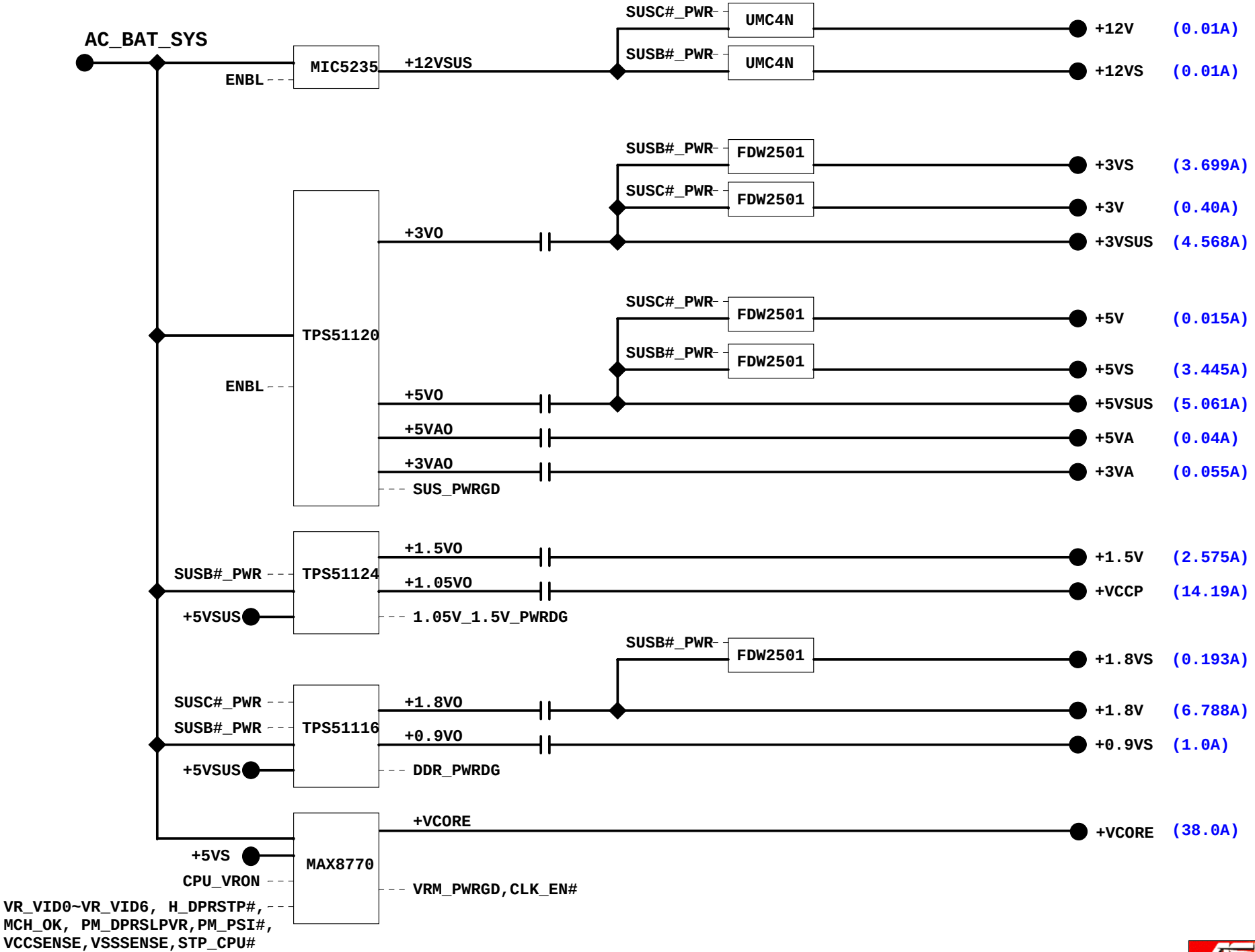




Title : POWER_PROTECT		
Engineer: Kevin Chang		
<OrgName>		
Size: Custom	Project Name: Rocky 30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 92 of 94	



ASUS	Title :	POWER_SIGNAL
<OrgName>	Engineer:	Kevin Chang
Size: Custom	Project Name: Rocky 30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 93 of 94	



ASUS	Title :	POWER_FLOWCHART	
<OrgName>	Engineer:	Kevin Chang	
Size: Custom	Project Name: Rocky 30		Rev: 1.0
Date: Saturday, January 26, 2008	Sheet 94 of 94		