

Compal Confidential

PAWGC/D Schematics Document

AMD APU Ontario-FT1 + FCH Hudson-M1 + GPU Roberson XT

2010-11-10

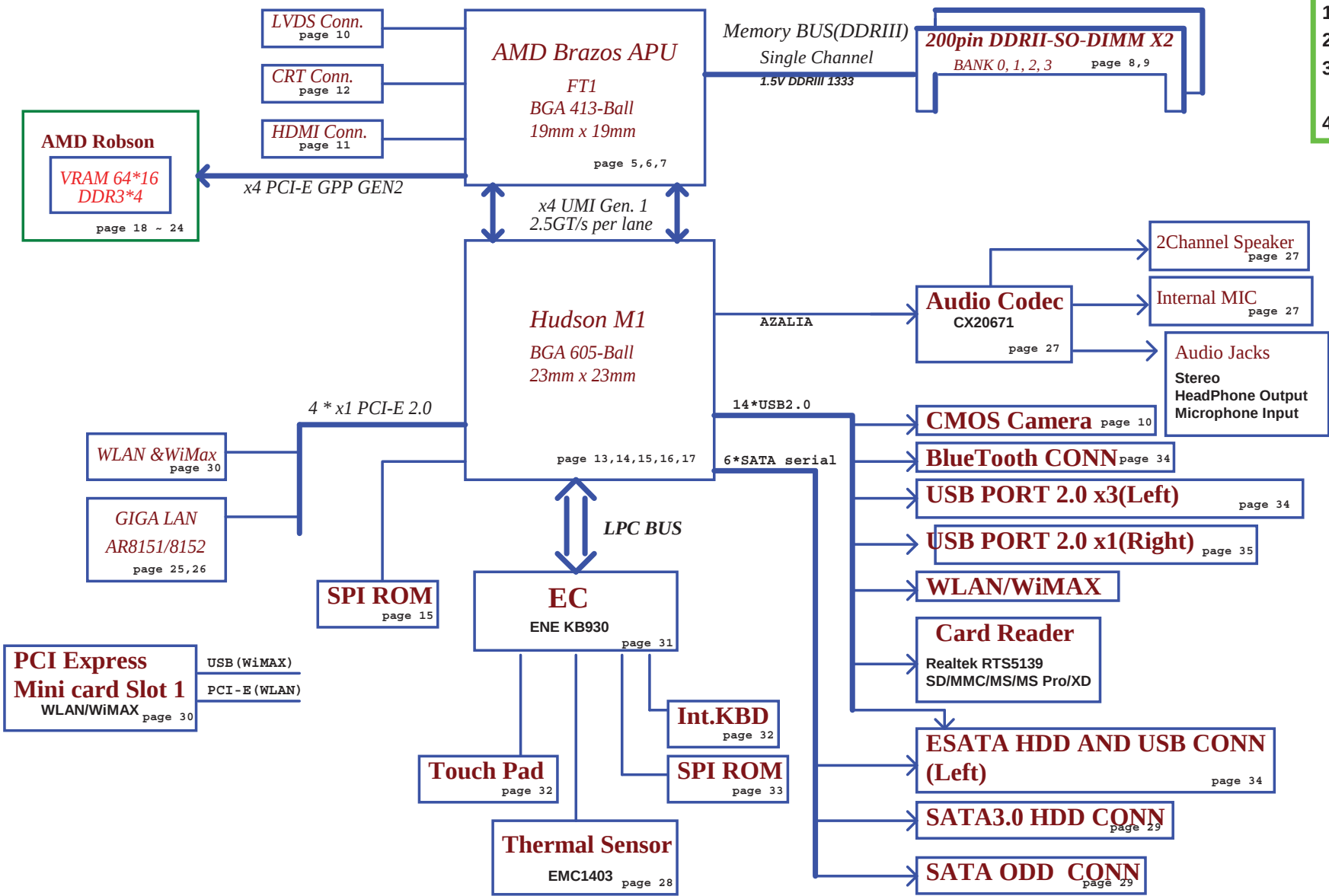
REV:1.0

CIT RD Only

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- For PAWGC
- 1. POWER BOARD
 - 2. Card Reader BOARD

- For PAWGD
- 1. POWER BOARD
 - 2. Card reader BOARD
 - 3. 4*LED+SW(3pin)
+SW(4pin) BOARD
 - 4. ODD BOARD



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+APU_CORE	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+APU_CORE_NB	1.0V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDRIII	ON	ON	OFF
+0.75VS	0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VS	1.0V switched power rail for NB VDDC & VGA	ON	OFF	OFF
+1.1VS	1.1VS switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON(WOL)	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
+1.1VALW	1.1V always on power rail	ON	ON	ON*

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address			EC SM Bus2 address		
Device	Address	HEX	Device	Address	HEX
Smart Battery	0001-011xb	15H	EMC1412-2 (dGPU)	1111-100xb	F8H
			EMC1403-2(DDR,WLAN)	1001-101xb	9AH
			SB-TSI	1001-100xb	98H

SM Bus Controller 0 (FCH_SMB1 ~ FCH_SMB4, SMB_ALERT#)

Device	Address	HEX
APU SIC/SID (FCH_SMB3)		
H_THERMTRIP# (FCH_ALERT#)		

SM Bus Controller 1 (FCH_SMB0)

Device	Address	HEX
DDR DIMM1 (FCH_SMB0)	1001-000xb	90
DDR DIMM2 (FCH_SMB0)	1001-001xb	92
WLAN (FCH_SMB0)		

FCH Hudson-M1 USB Port List	
USB1.1	
Port0	NC
Port1	NC
USB2.0	
Port0	Left USB1
Port1	USB Camera
Port2	Left (Combo)
Port3	Left USB2
Port4	Right USB
Port5	BT
Port6	CardReader
Port7	Mini-PCIE
Port8	NC
Port9	NC
Port10	NC
Port11	NC
Port12	NC
Port13	NC

Brazos PCIE Port List		
APU	PCIE0	GPU PCIE x4
	PCIE1	
	PCIE2	
	PCIE3	
FCH	PCIE0	LAN
	PCIE1	WLAN
	PCIE2	NC
	PCIE3	NC

FCH Hudson-M1 SATA Port List	
SATA0	HDD
SATA1	ODD
SATA2	eSATA
SATA3	NC
SATA4	NC
SATA5	NC

BOM Structure

UMA@ : UMA only
PX@ : DIS muxluss
- PX3@ : PX3.0 only
- BACO@ : Baco only

GIGA@ : AR8151
8152@ : AR8152
CMOS@ : USB camera
HDMI@ : HDMI function
nonHDMI@ : w/o HDMI function
ESATA@: eSATA function
BT@ : BT function
ME@ : ME components
X76@, H1G@, H512@, S1G@, S512@ : VRAM
45@ : 45 Level
HWM@ : hardware monitor function
nonHWM@: w/o hardware monitor function

Power-Up/Down Sequence

1. All the ASIC supplies must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred.

2. VDDR3 should ramp-up before or simultaneously with VDDC.

3. For LVDS, DPx_VDD10 should ramp-up before DPx_VDD18 and the PCIe Reference clock should begin before DPx_VDD18. For power-down, DPx_VDD18 should ramp-down before DPx_VDD10.

4. The external pull-ups on the DDC/AUX signals (if applicable) should ramp-up before or after both VDDC and VDD_CT have ramped up.

5. VDDC and VDD_CT should not ramp-up simultaneously. (e.g., VDDC should reach 90% before VDD_CT starts to ramp-up (or vice versa).)

VDDR3(3.3VGS)

PCIE_VDDC(1.0V)

VDDR1(1.5VGS)

VDDC/VDDCI(1.12V)

VDD_CT(1.8V)

PERSTb

REFCLK

Straps Reset

Straps Valid

Global ASIC Reset

Note: Do not drive any IOs before VDDR3 is ramped up.

T4+16clock

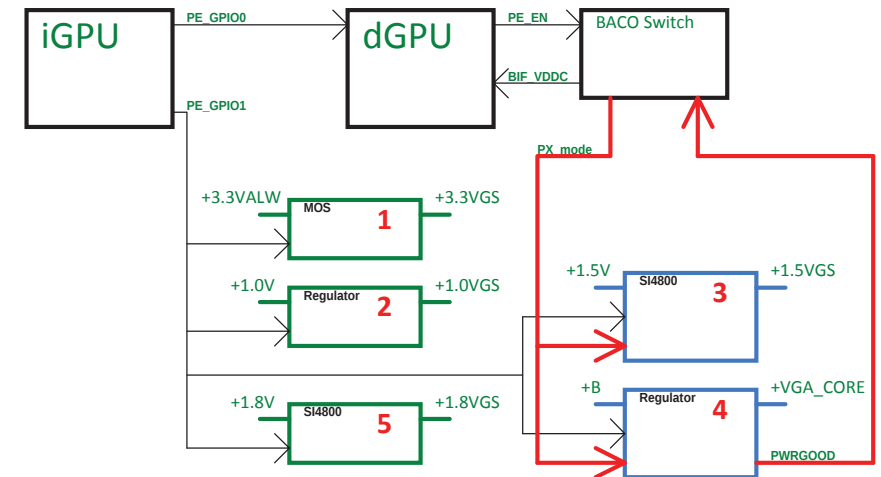
Without BACO option :

PE_GPIO0 : Low -> Reset dGPU ; High -> Normal operation
PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON

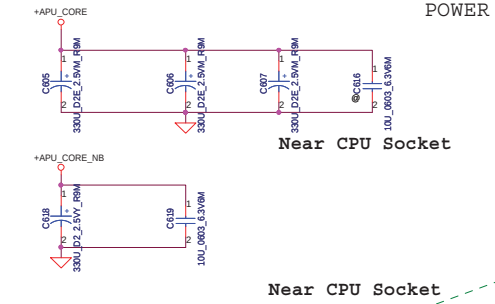
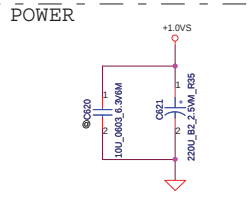
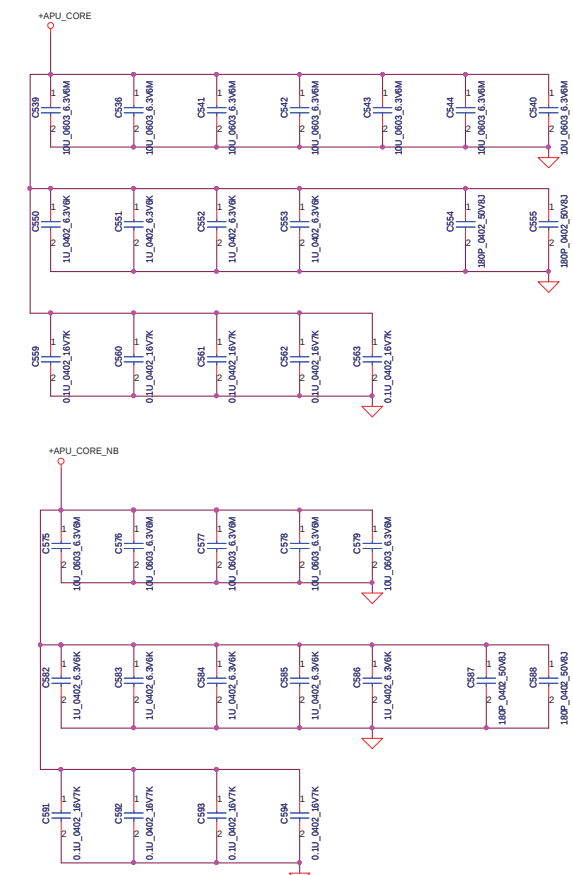
BACO option :

PE_GPIO0 : High -> Normal operation (dGPU is not reset on BACO mode)
PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON (always High)

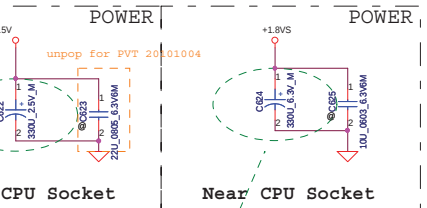
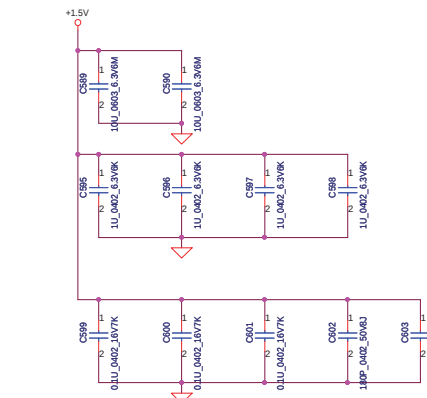
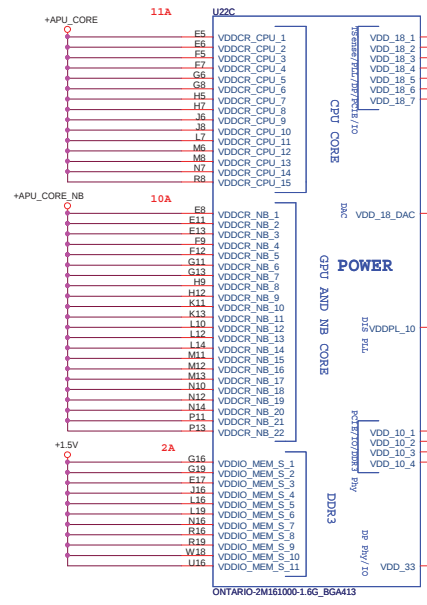
dGPU Power Pins	Voltage	PX 3.0	BACO Mode	Max current
PCIE_PVDD, PCIE_VDDR, TSVDD, VDDR4, VDD_CT, DPE_PVDD, DP[F:E]_VDD18, DP[D:A]_PVDD, DP[D:A]_VDD18, AVDD, VDD1DI, A2VDDQ, VDD2DI, DPLL_PVDD, MPV18, and SPV18	1.8V	OFF	ON	1679mA
DP[F:E]_VDD10, DP[D:A]_VDD10, DPLL_VDDC, and SPV10	1.0V	OFF	ON	575mA
PCIE_VDDC	1.0V	OFF	ON	2A
VDDR3 , and A2VDD	3.3V	OFF	ON	190mA
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode)	Same as VDDC	OFF	ON Same as PCIE_VDDC	70mA
VDDR1	1.5V	OFF	OFF	2.8A
VDDC/VDDCI	1.12V	OFF	OFF	12.9A



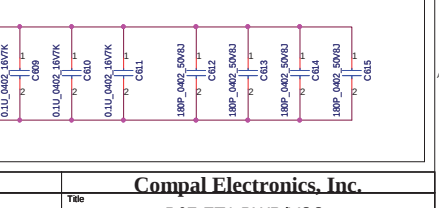
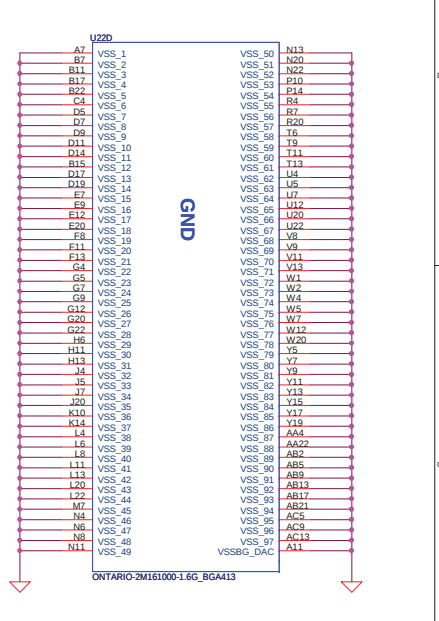
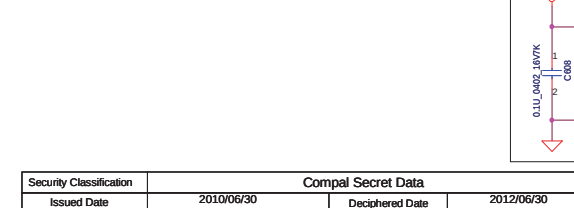
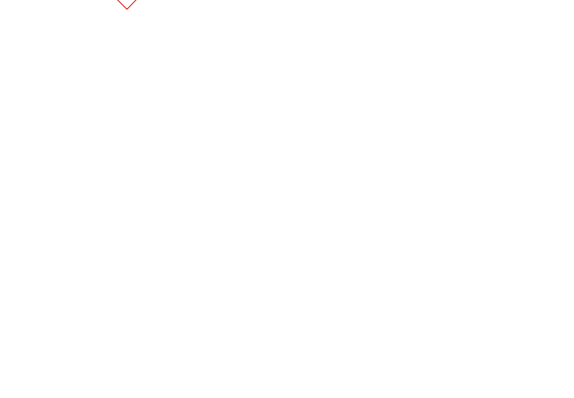
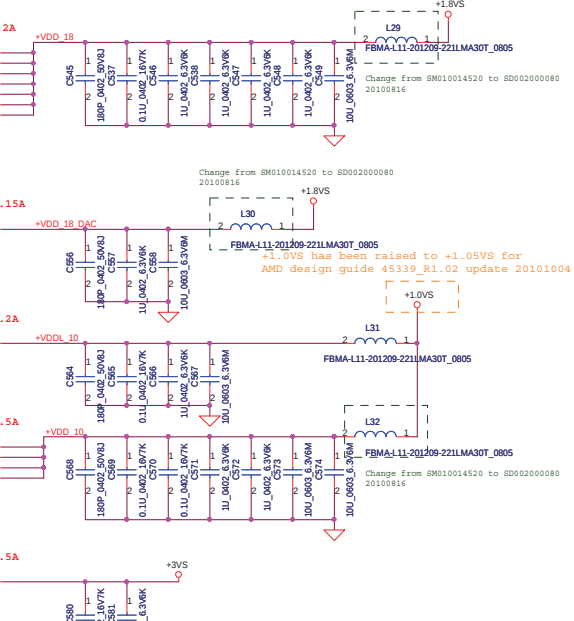
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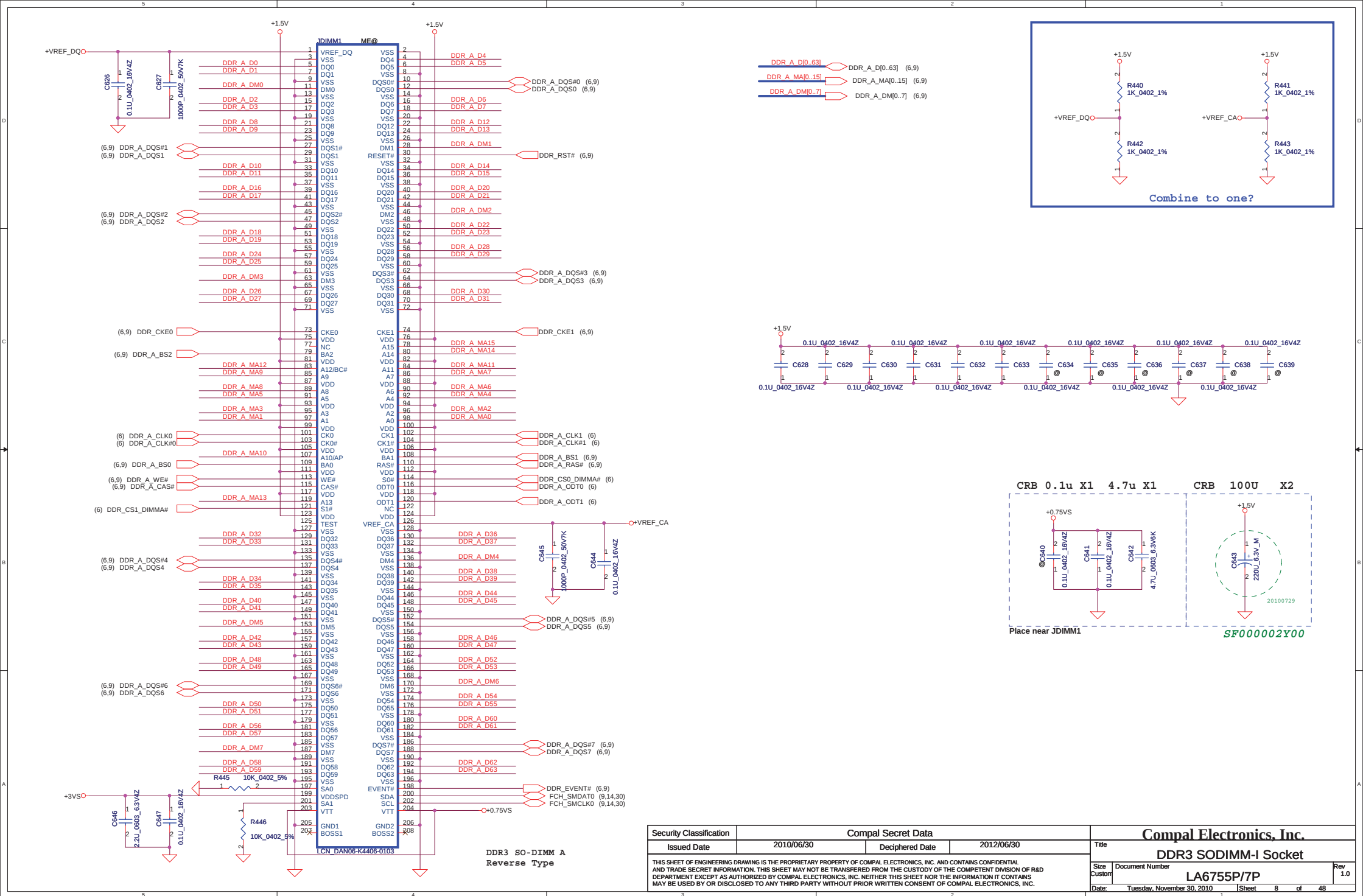
(330uF 6.3V 4.2L_ESR17m)*1=(SF000002Z00)

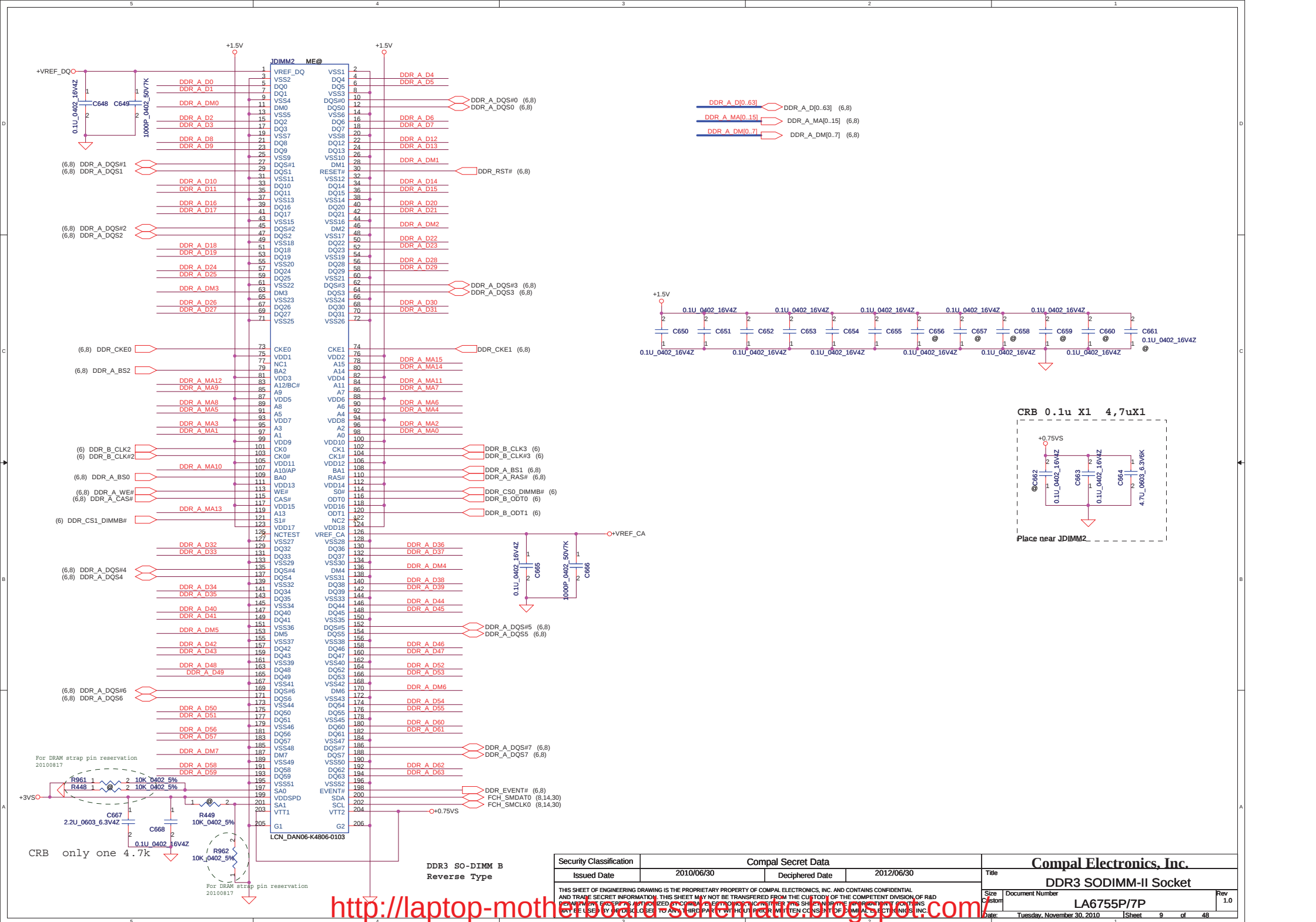


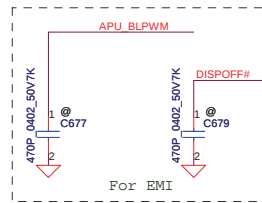
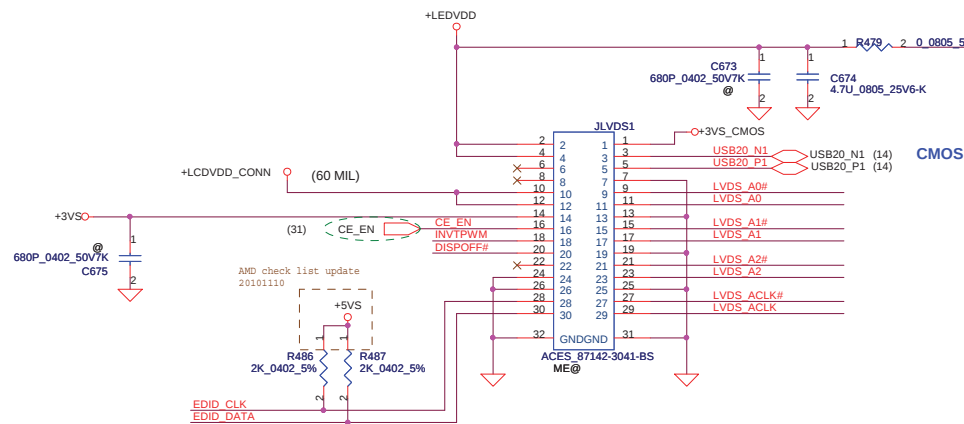
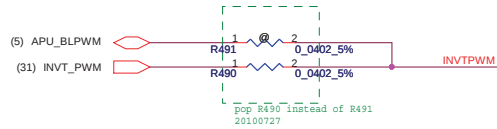
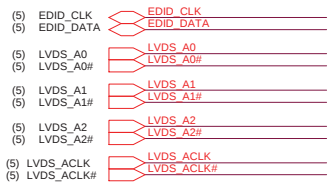
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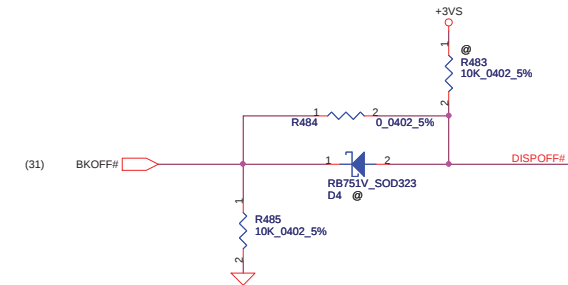
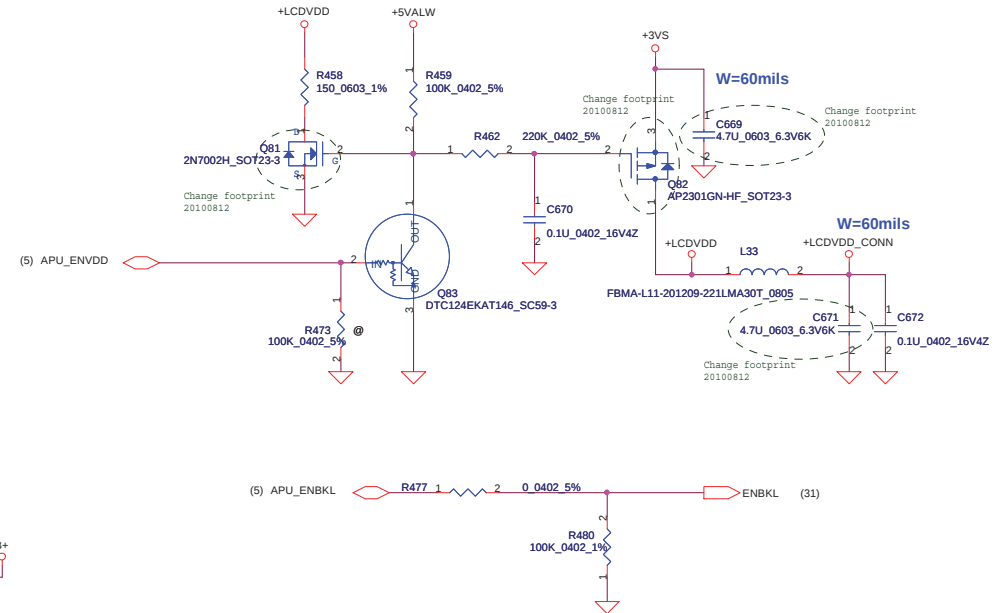
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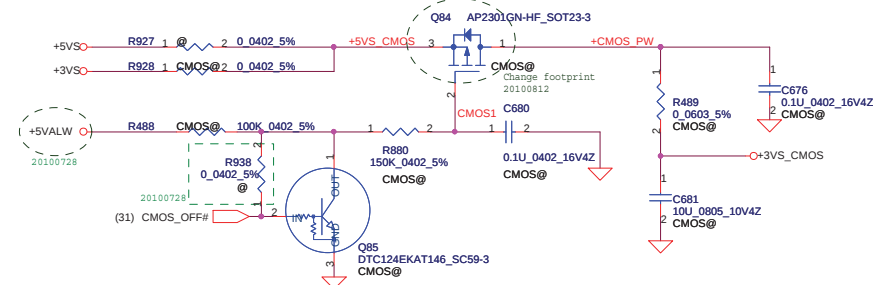




LCD POWER CIRCUIT

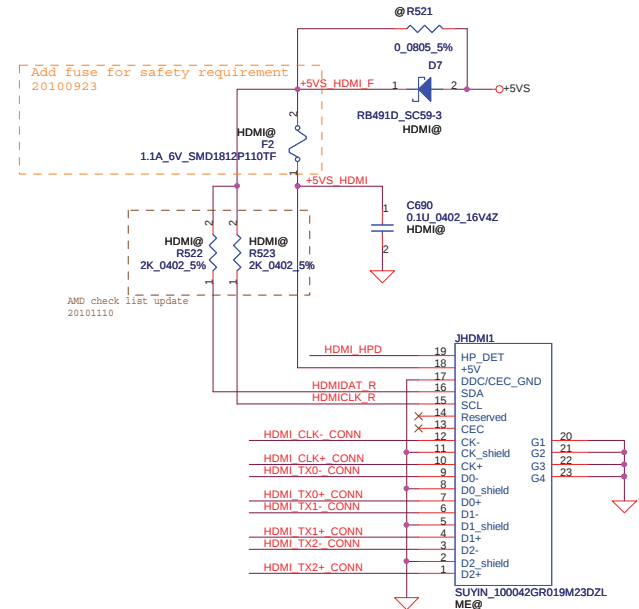
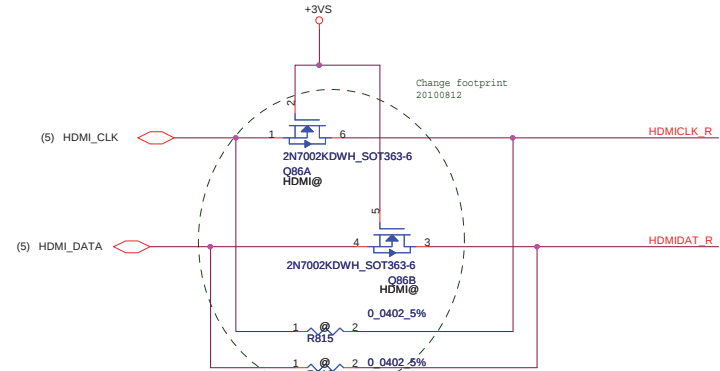
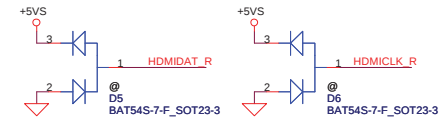
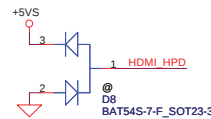
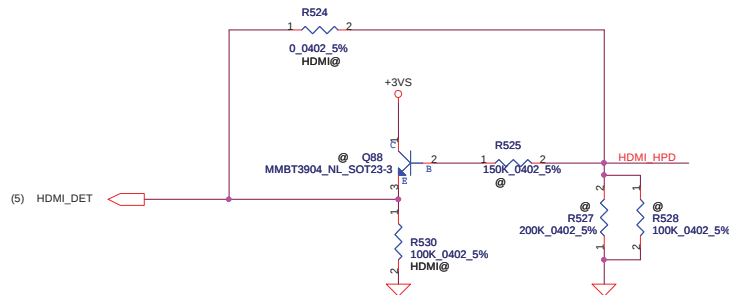
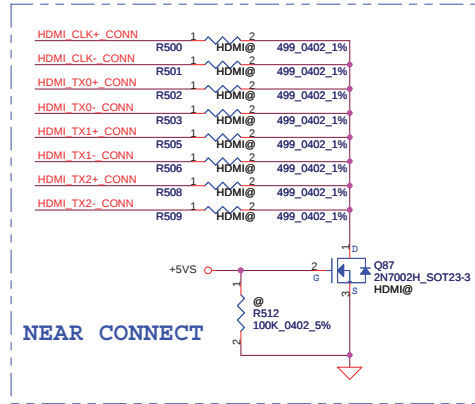
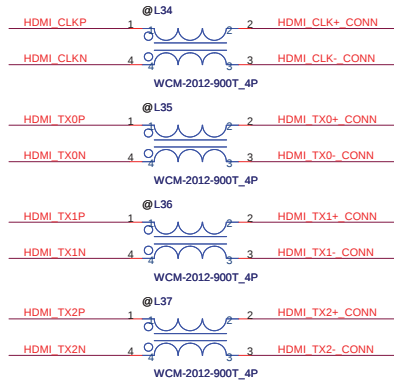


CMOS Camera



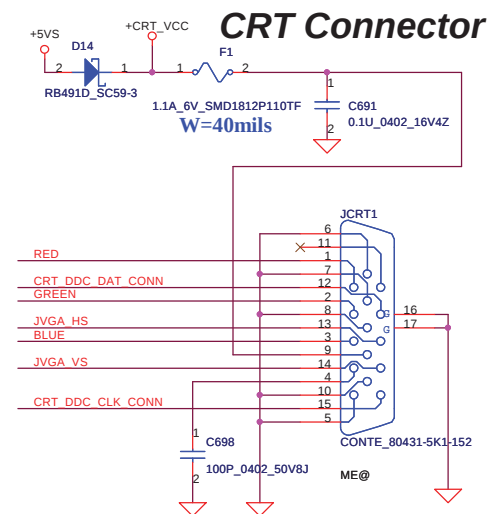
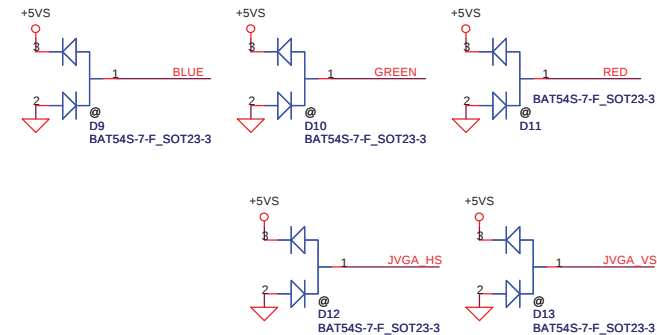
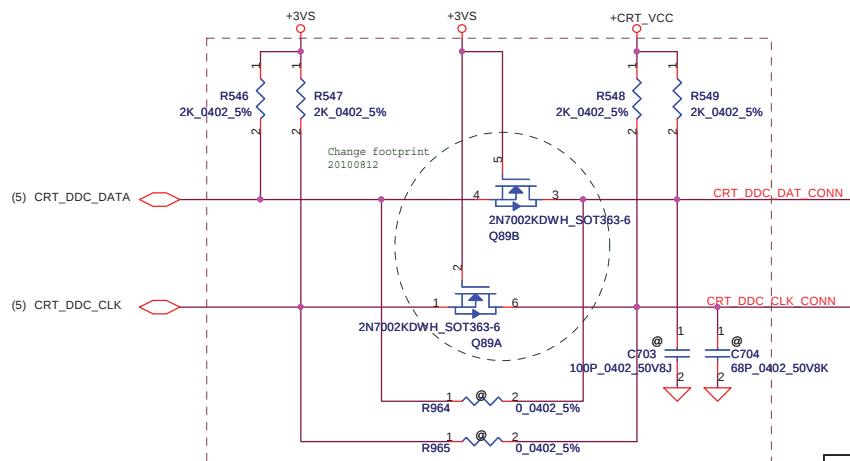
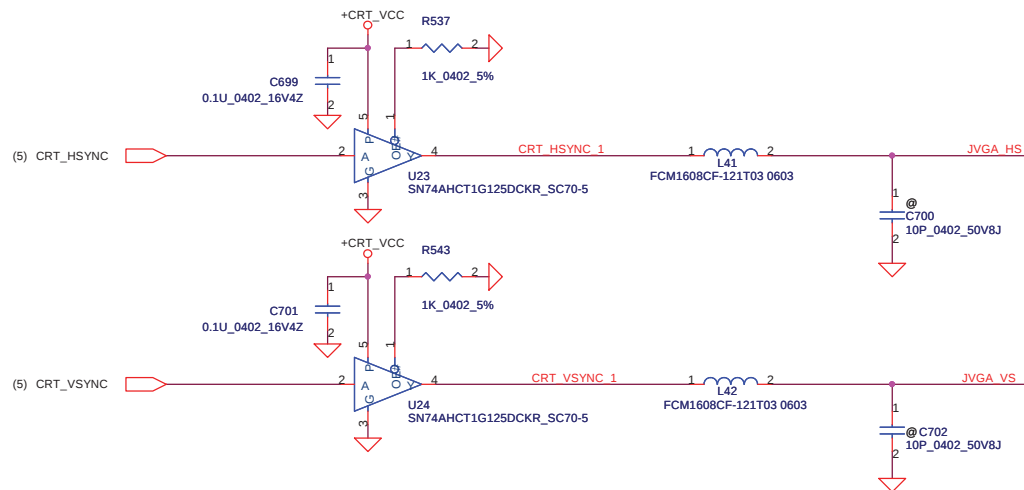
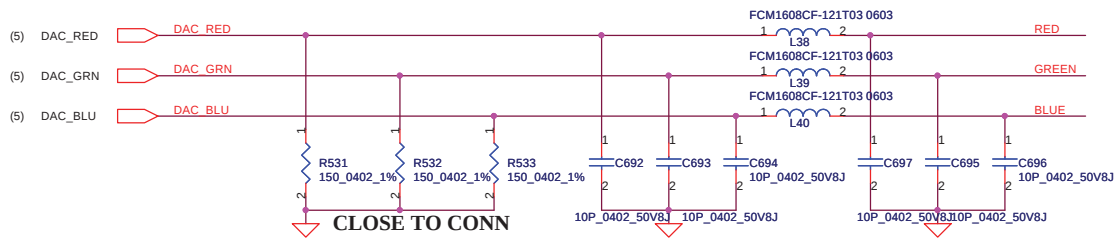
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(5) HDMI_CLKP	R513	1	HDMI@	2	0_0402_5%	HDMI_CLK+ CONN
(5) HDMI_CLKN	R514	1	HDMI@	2	0_0402_5%	HDMI_CLK- CONN
(5) HDMI_TX0P	R515	1	HDMI@	2	0_0402_5%	HDMI_TX0+ CONN
(5) HDMI_TX0N	R516	1	HDMI@	2	0_0402_5%	HDMI_TX0- CONN
(5) HDMI_TX1P	R517	1	HDMI@	2	0_0402_5%	HDMI_TX1+ CONN
(5) HDMI_TX1N	R518	1	HDMI@	2	0_0402_5%	HDMI_TX1- CONN
(5) HDMI_TX2P	R519	1	HDMI@	2	0_0402_5%	HDMI_TX2+ CONN
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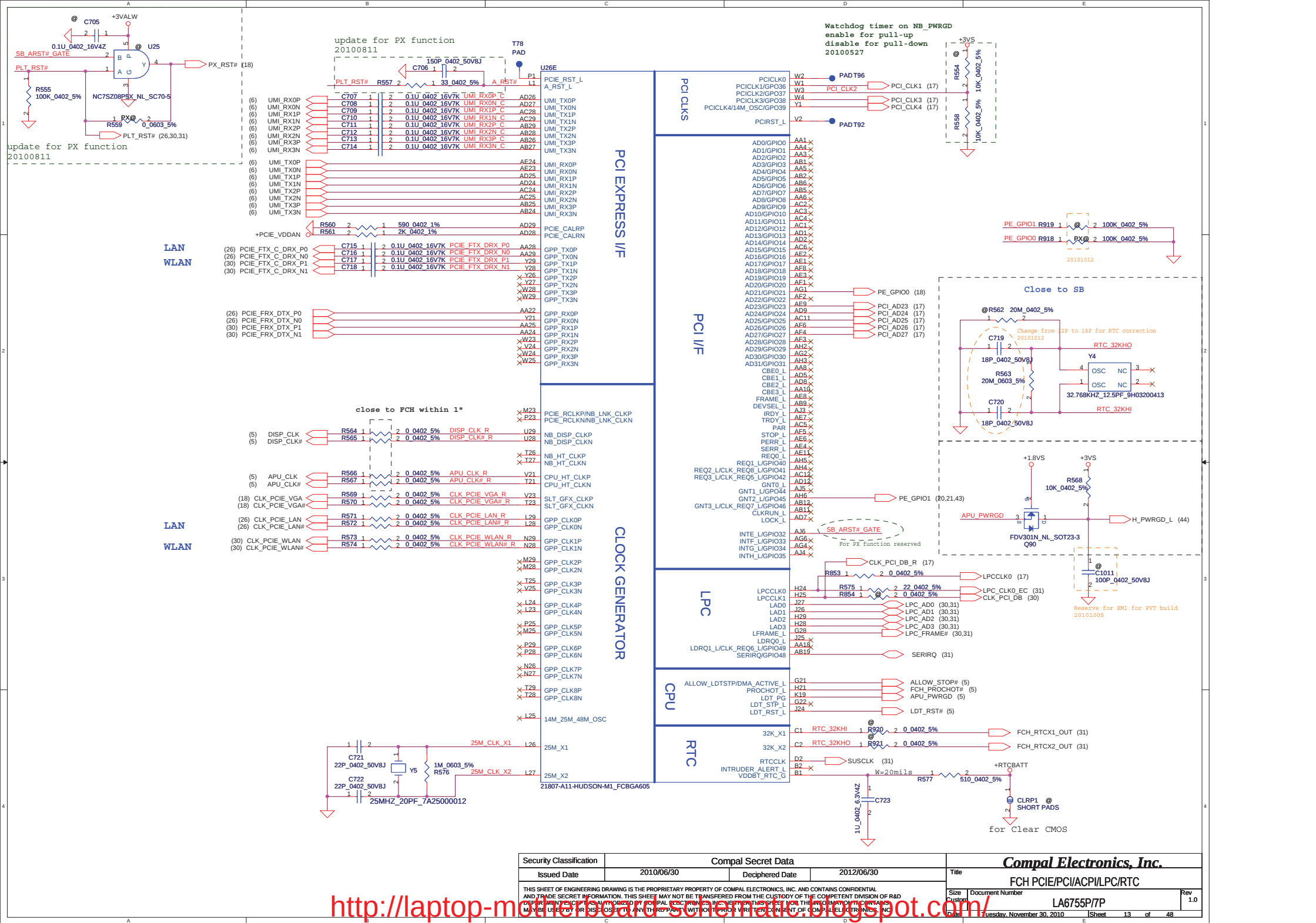
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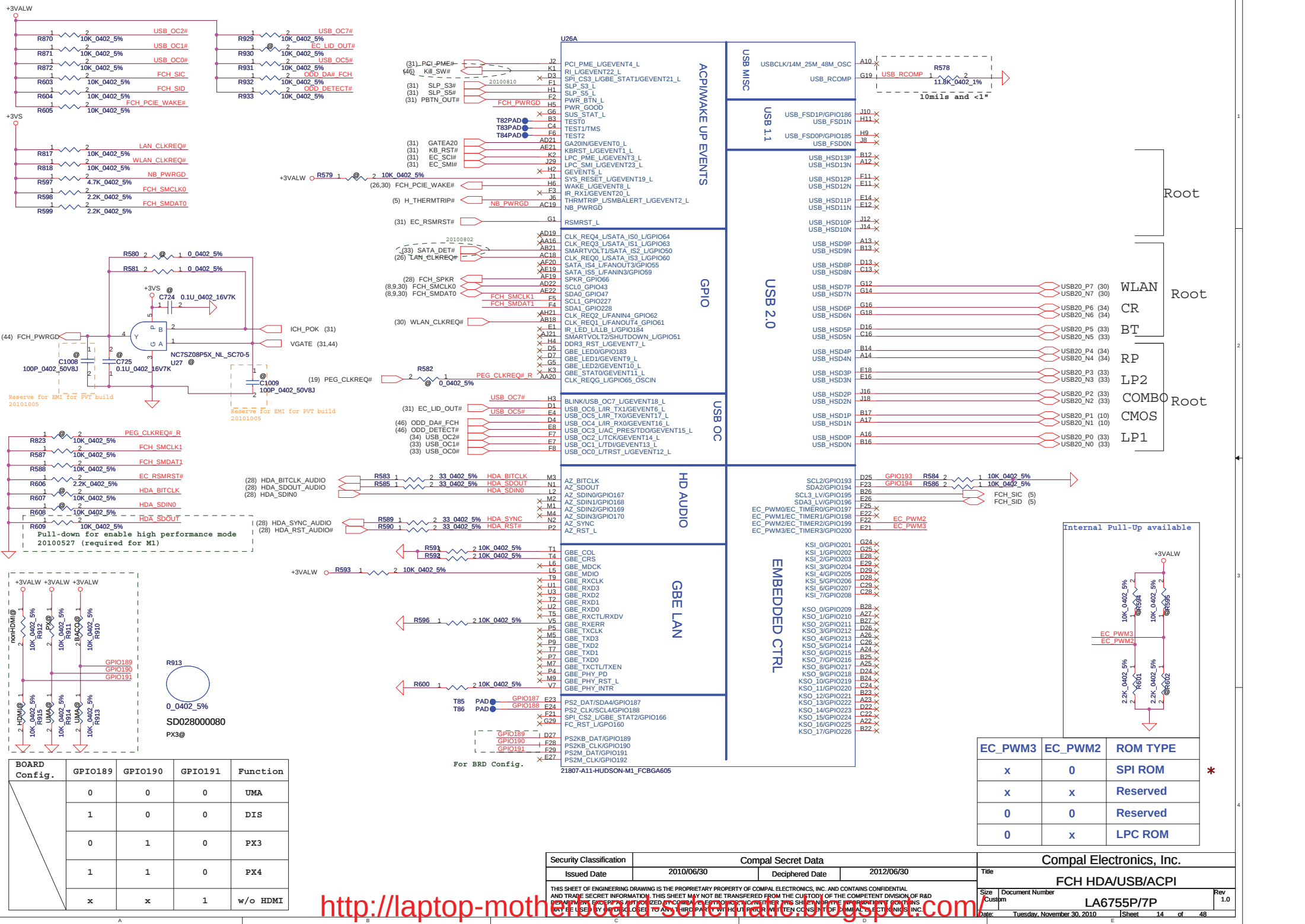
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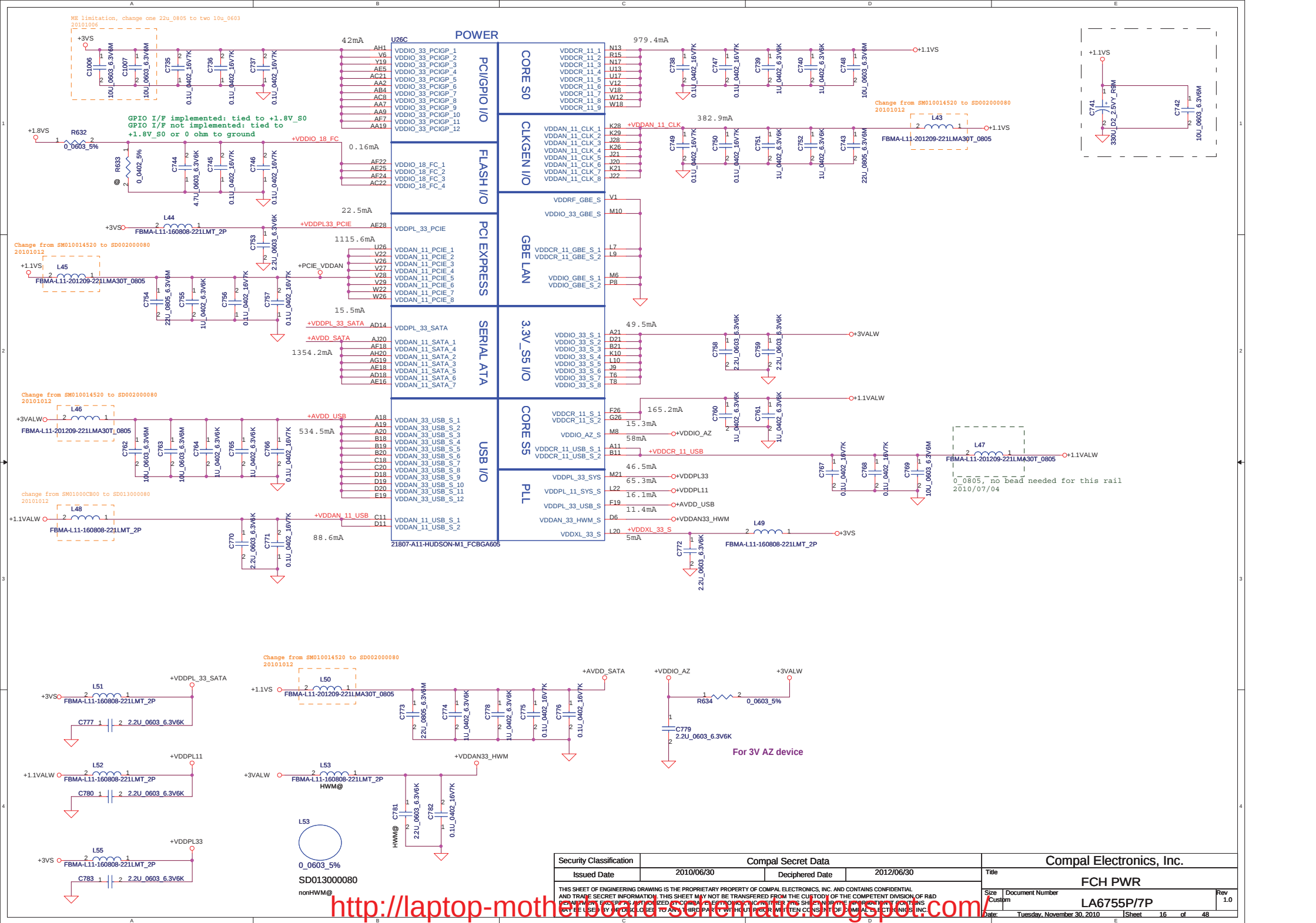


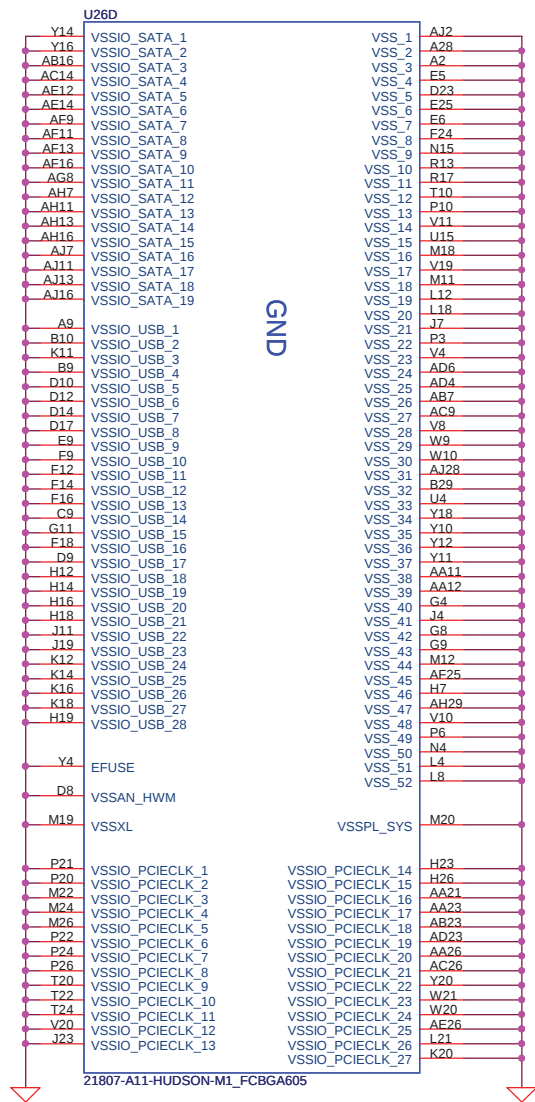
BOARD Config.	GPIO189	GPIO190	GPIO191	Function
	0	0	0	UMA
	1	0	0	DIS
	0	1	0	PX3
	1	1	0	PX4
	x	x	1	w/o HDMI

EC_PWM3	EC_PWM2	ROM TYPE
x	0	SPI ROM
x	x	Reserved
0	0	Reserved
0	x	LPC ROM

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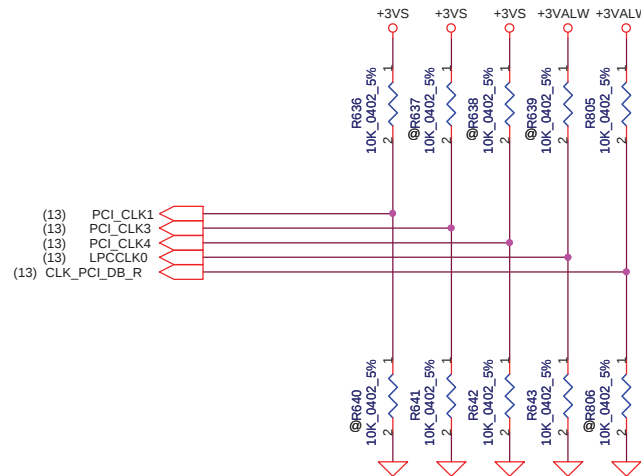




REQUIRED STRAPS

Check Internal PU/PD

	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	CLK_PCI_DB				
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAP	Reserved	internal EC ENABLE	Internal CLKGEN Mode DEFAULT				
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	CLKGEN Mode Internal DEFAULT	internal EC DISABLE DEFAULT	External CLKGEN Mode				



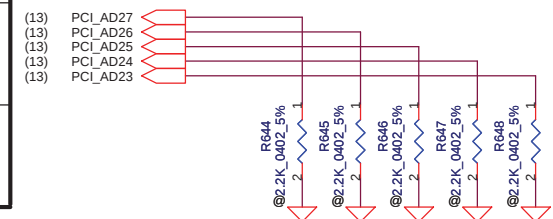
DEBUG STRAPS

FCH M1 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

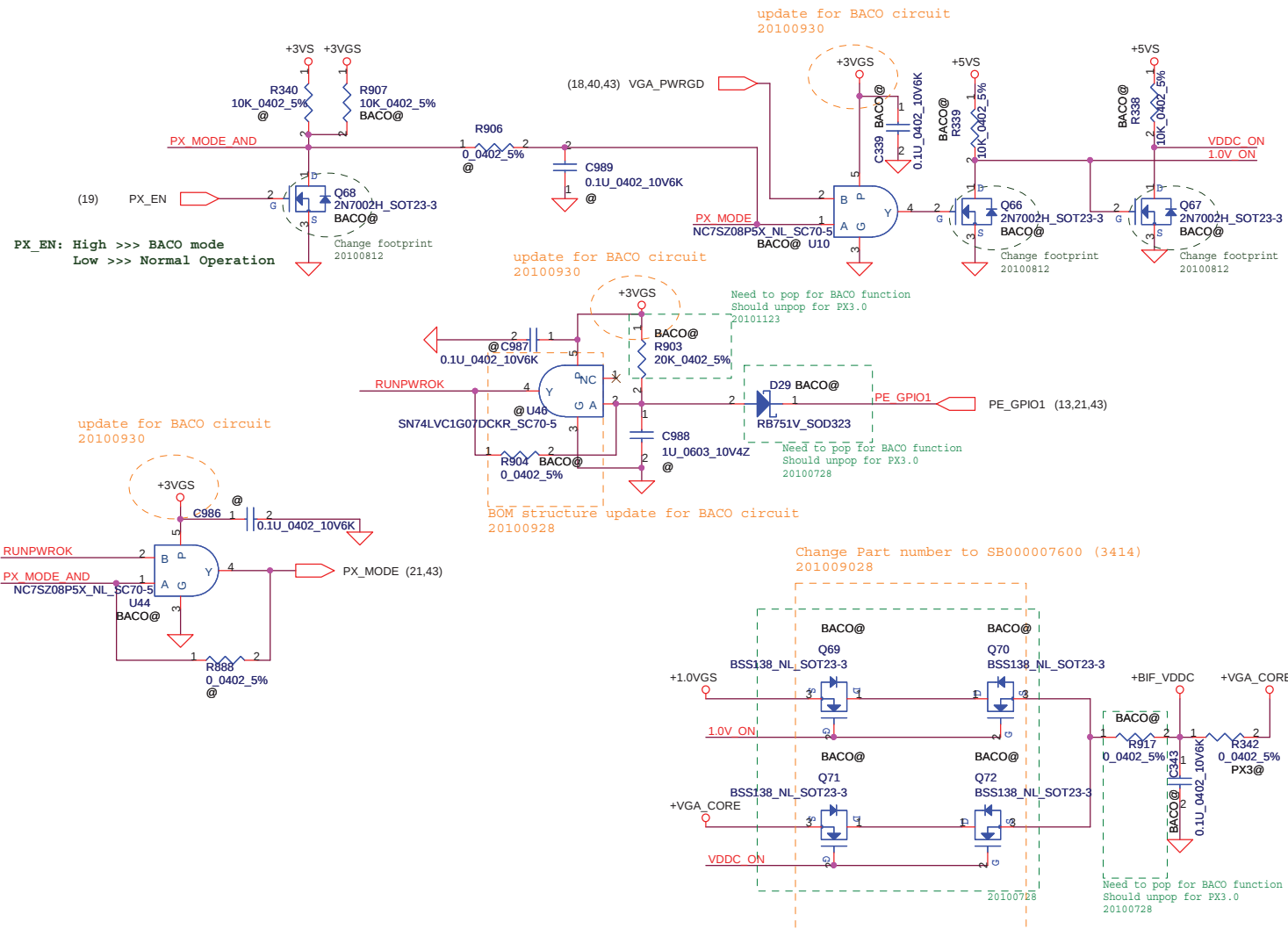
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23 Enable ROM Straps
PULL HIGH	USE internal PLL generated PLL CLK DEFAULT	ILA AUTORUN Disabled DEFAULT	Selects FC PLL DEFAULT	Disable I2C ROM DEFAULT	Required Setting DEFAULT
PULL LOW	BYPASS PCI PLL	ILA AUTORUN Enabled	FC PLL bypassed	Getting Value from I2C EPROM	Reserved

Check AD29,AD28 strap function

check default

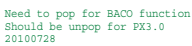


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		Size B	Document Number							Rev 1.0
		LA6755P/7P								
		Date:		Tuesday, November 30, 2010			Sheet 17		of 48	



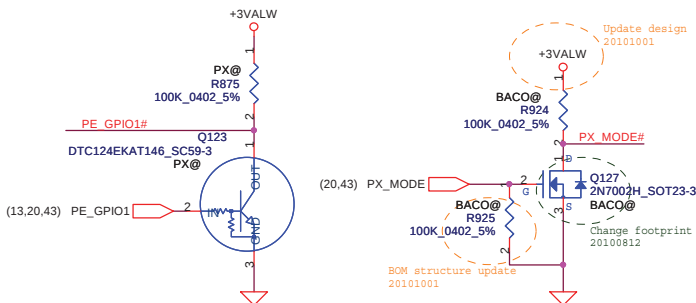
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/06/30	Deciphered Date	2012/06/30	Title	
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				Size B	Document Number
				LA6755P/7P	
				Date:	Tuesday, November 30, 2010
				Sheet	20 of 48
				Rev	1.0

For VGA power sequence
20100816

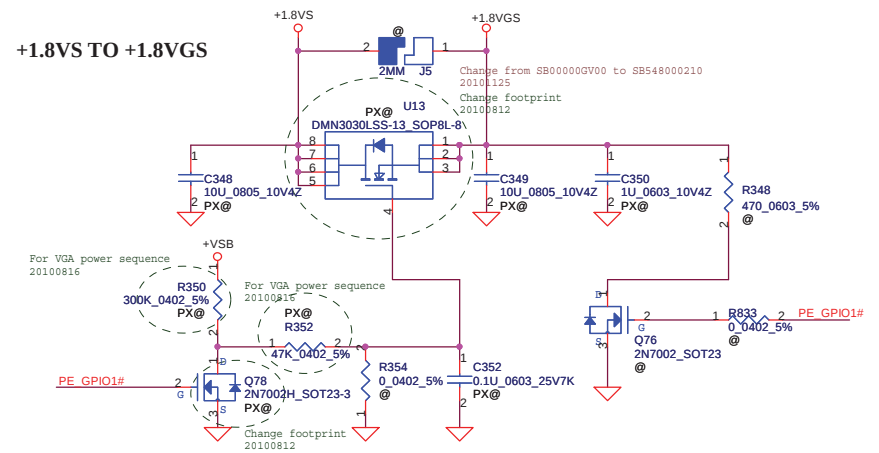


PX_MODE# 1 R829 2
0_0402_5%
BACO@

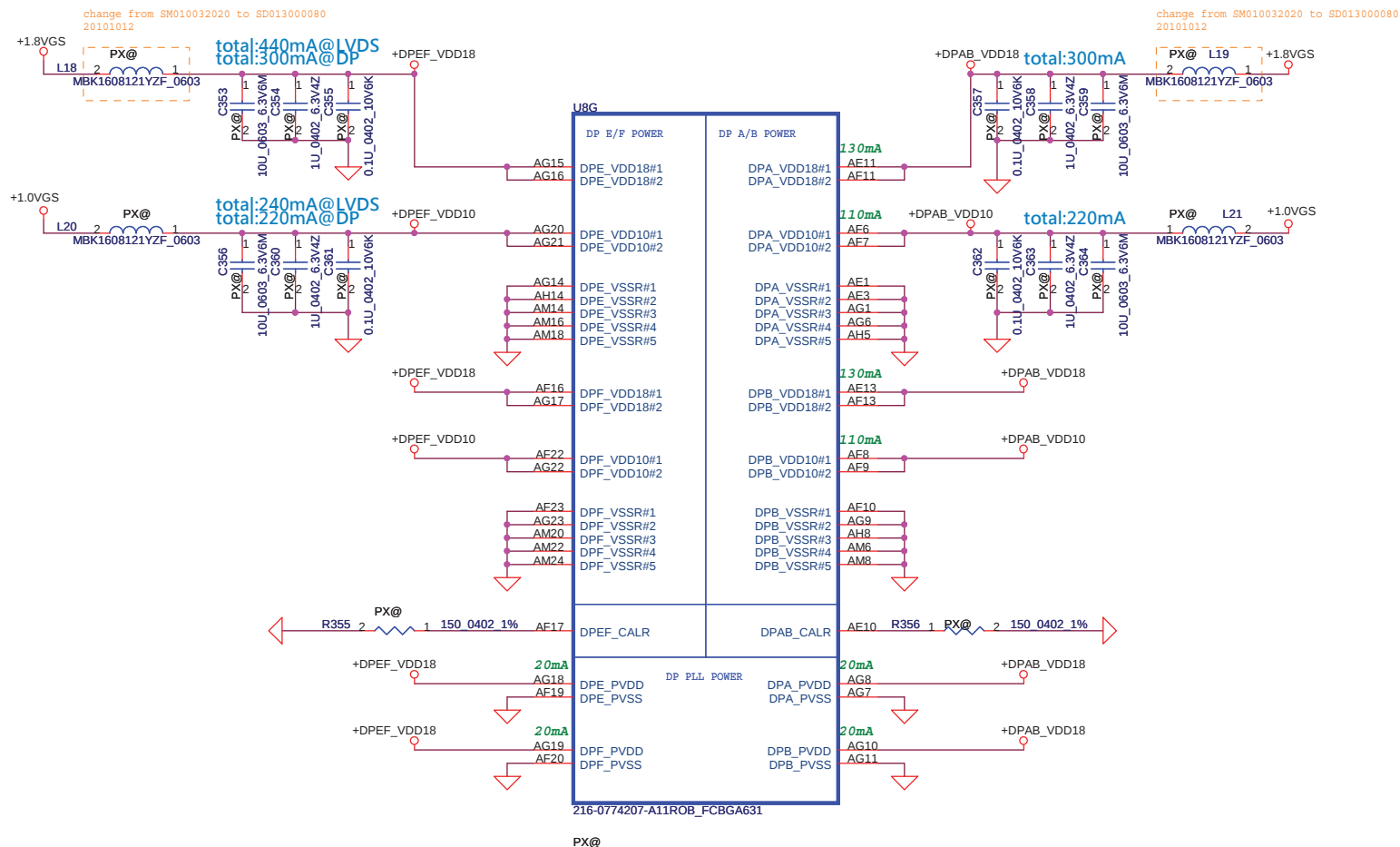
PE_GPIO1# 1 R830 2
0_0402_5%
PX3@



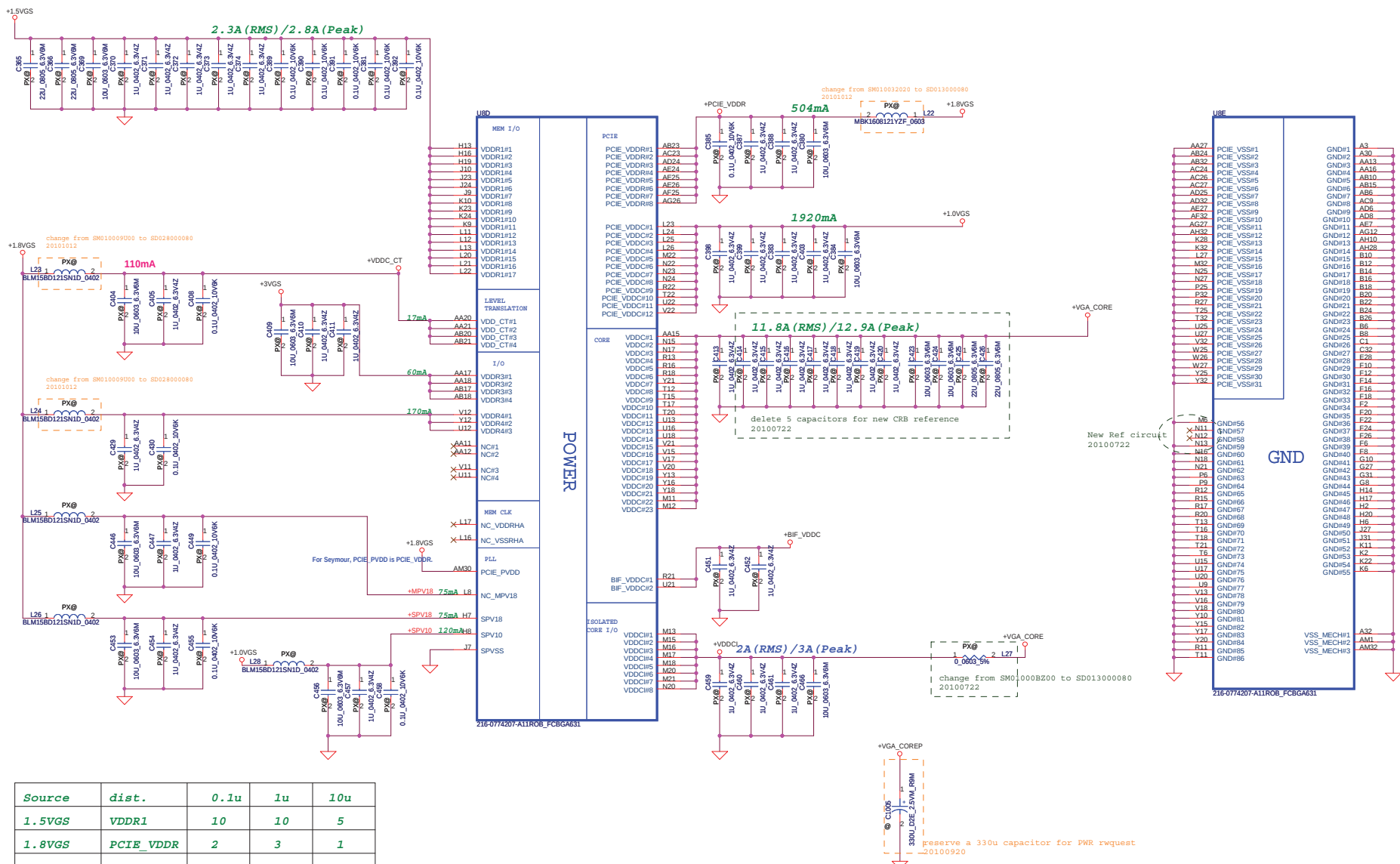
For VGA power sequence
20100816
R839
20K_0402_5%
PX@
PX@
For VGA PWR sequence



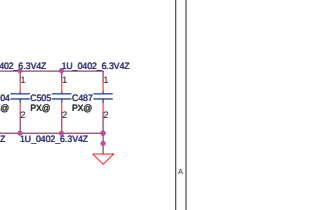
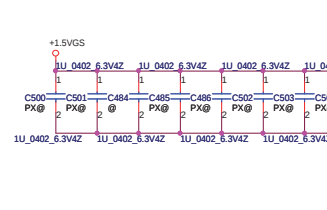
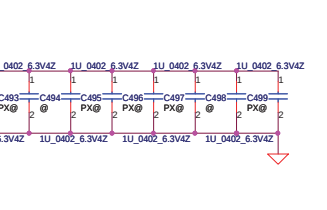
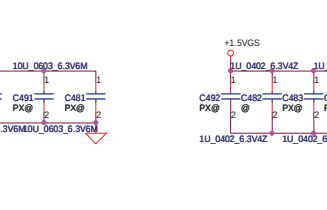
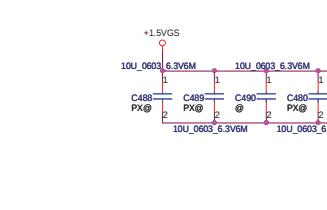
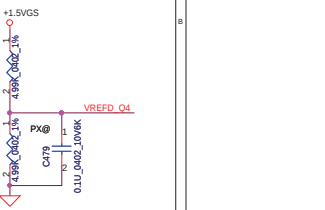
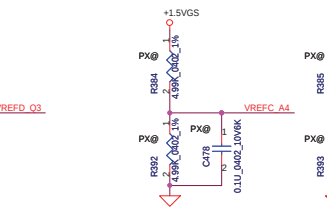
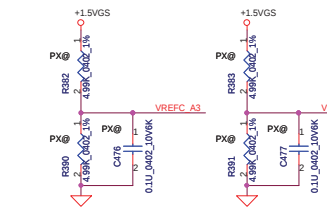
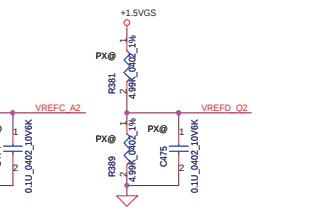
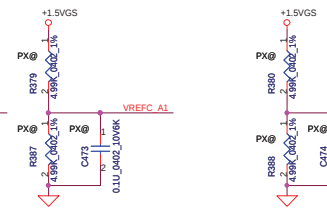
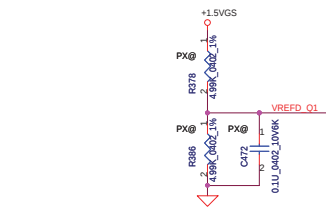
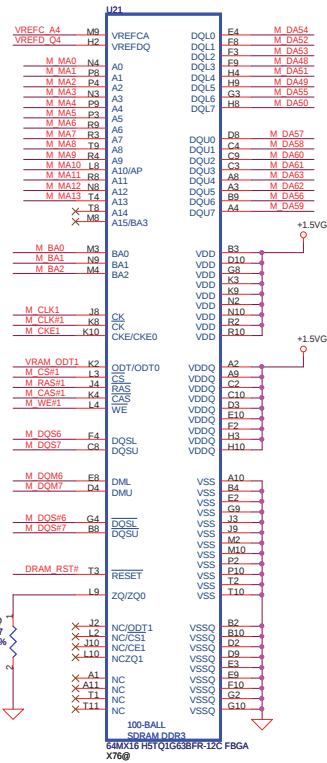
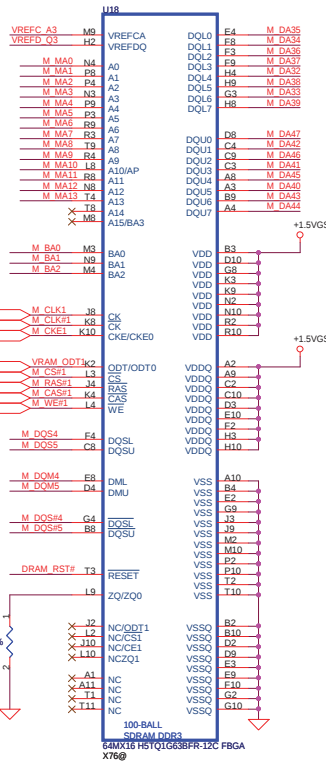
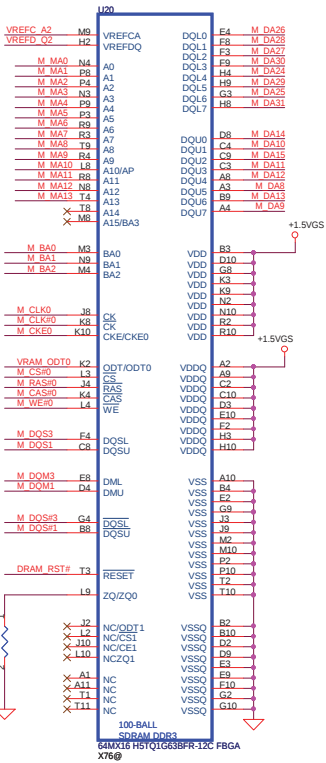
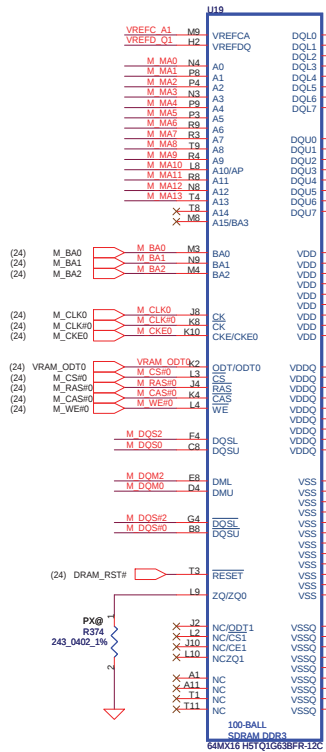
1 2 3



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Size B	Document Number	LA6755P/7P		Rev	1.0
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- (24) M_DA[63..0] M_DA[63..0]
 (24) M_MA[13..0] M_MA[13..0]
 (24) M_DQM[7..0] M_DQM[7..0]
 (24) M_DQS[7..0] M_DQS[7..0]
 (24) M_DQS[7..0] M_DQS[7..0]

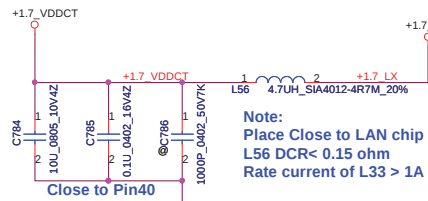
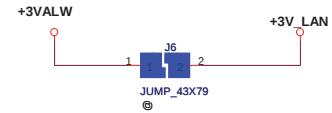


VRAM P/N :
 Hynix : SA000041S10 (S IC D3 64MX16 H5TQ1G63BFR-11C FBGA C38!)
 Samsung : SA000041T10 (S IC D3 64MX16 K4W1G1646E-HC11 FBGA C38!)
 update VRAM PN 0619 update

<http://laptop-motherboard.com/>

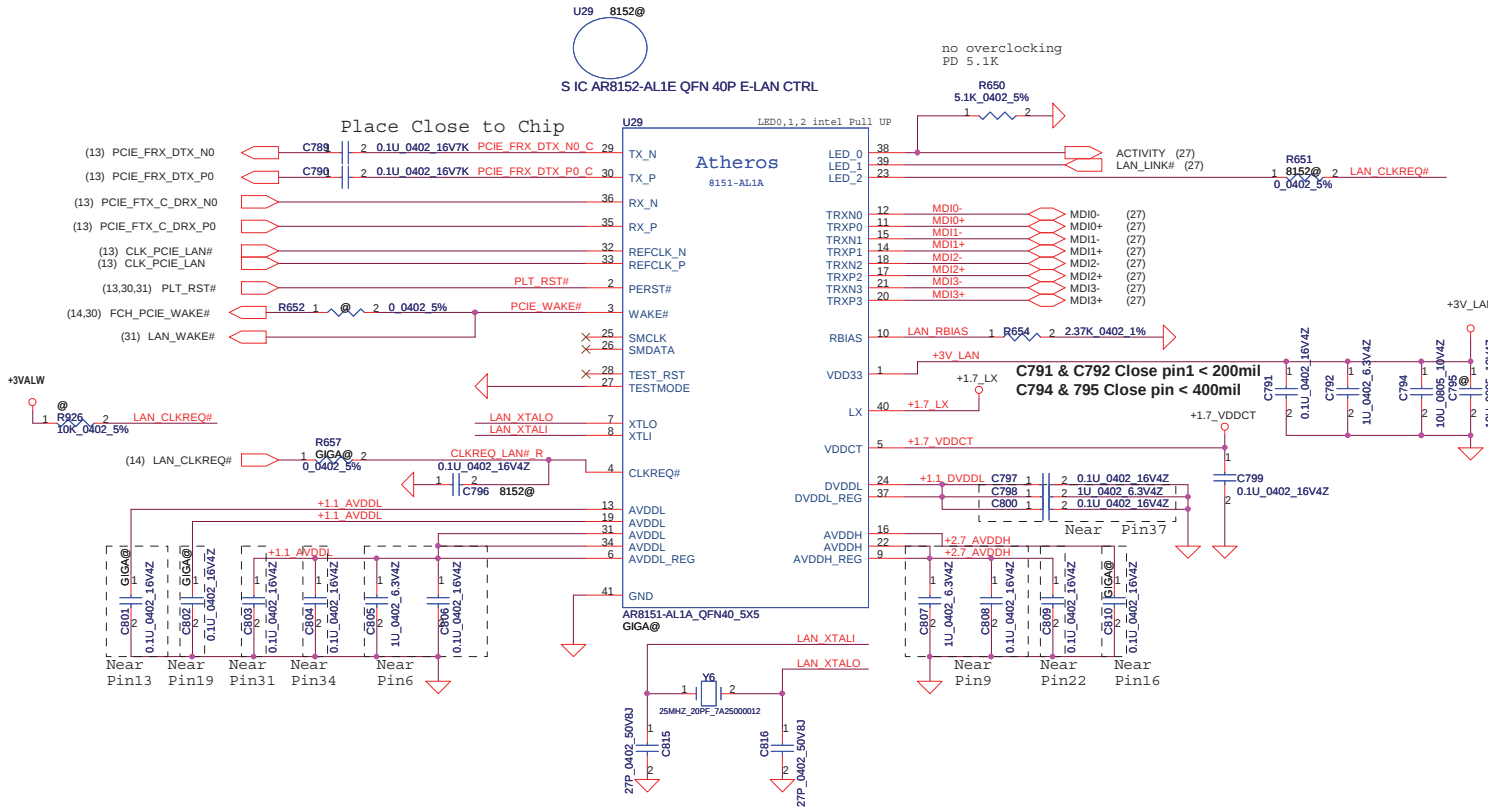
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		Deciphered Date		Title	
2010/06/30		2012/06/30		RobsonXT-S3 VRAM	
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Size	Document Number				Rev
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Atheros request can't disable LAN power

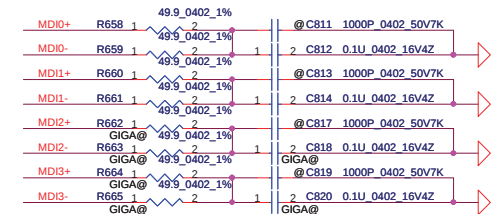


Power On strapping

Pin	Description	Chip Default
LED0	H:Over Clock Enable L:Over Clock Disable *	H
LED2	H:SWR Switch mode regulator Select *	--
	AR8152, Pin23 is CLKREQ	



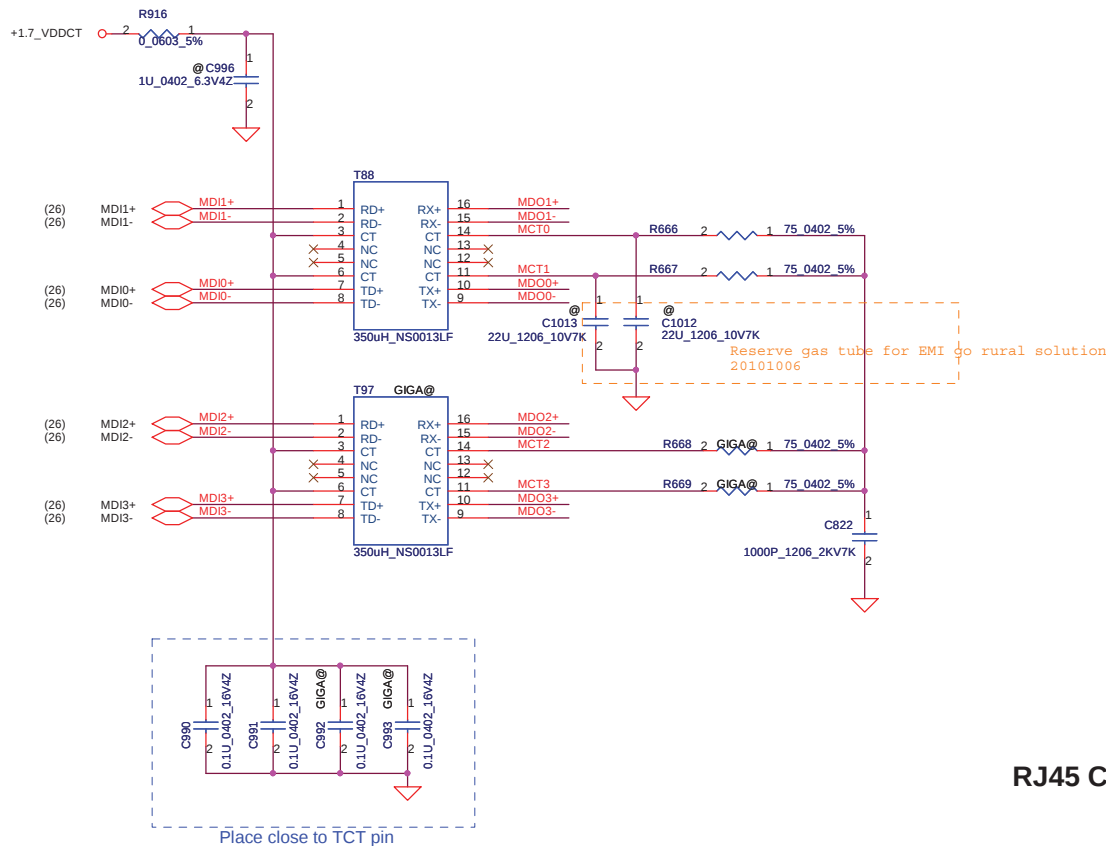
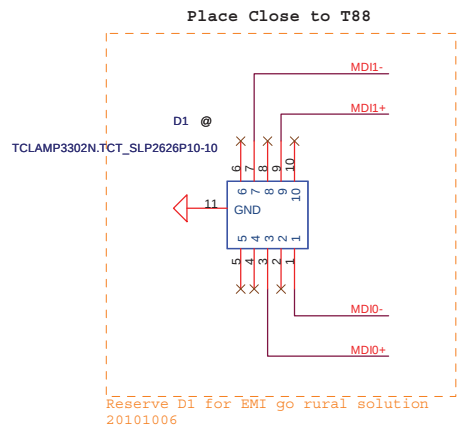
Place Close to LAN chip



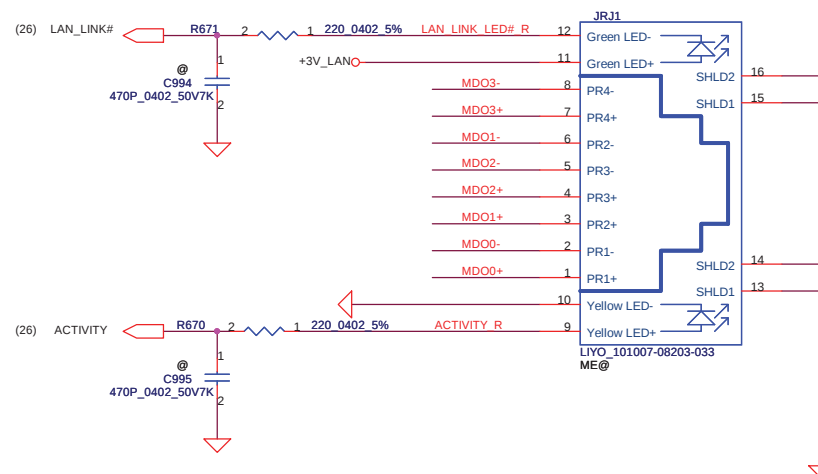
8152 no mount MDI3+,MDI3-,MDI2-,MDI2+ resistor and cap

	Pin4	Configure		Pin23	Configure
		R657	C796		R651
AR8152	VDDCT_REG		*	CLKREQn	*
AR8151	CLKREQn	*		LED [2]	

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				Date: Tuesday, November 30, 2010	Sheet 26 of 48



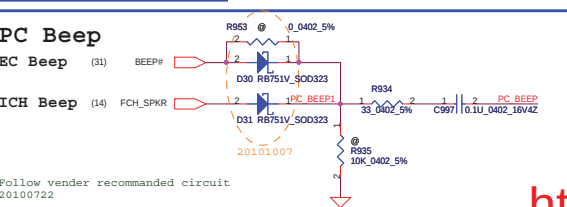
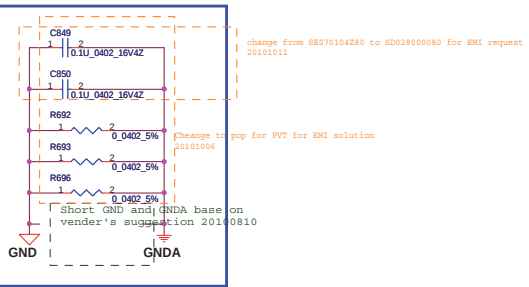
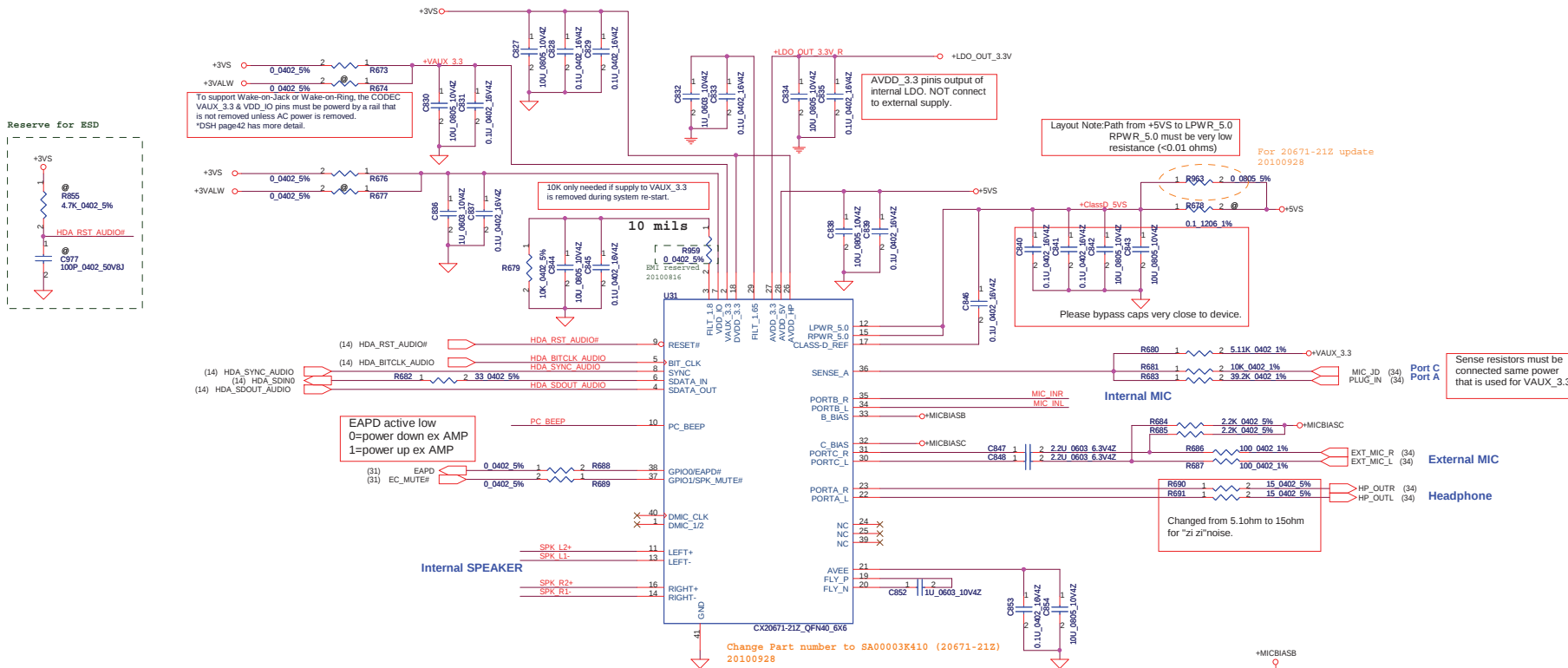
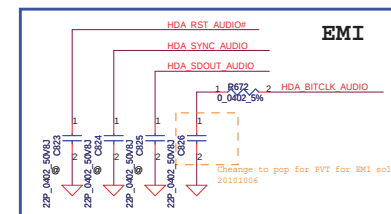
RJ45 Conn.



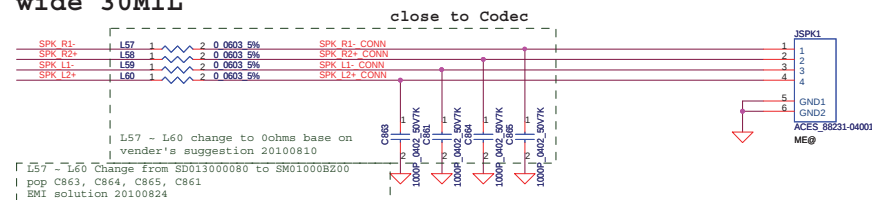
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Issued Date				2010/06/30		Deciphered Date		2012/06/30		Title	
										LAN Transformer	
										LA6755P/7P	
										Rev 1.0	
										Date: Tuesday, November 30, 2010	
										Sheet 27 of 48	

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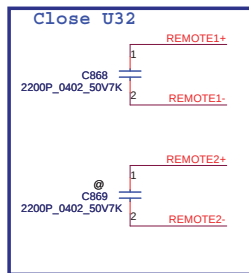
CX20671
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).



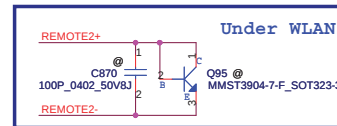
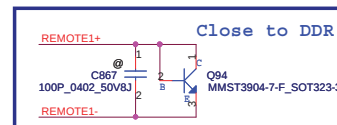
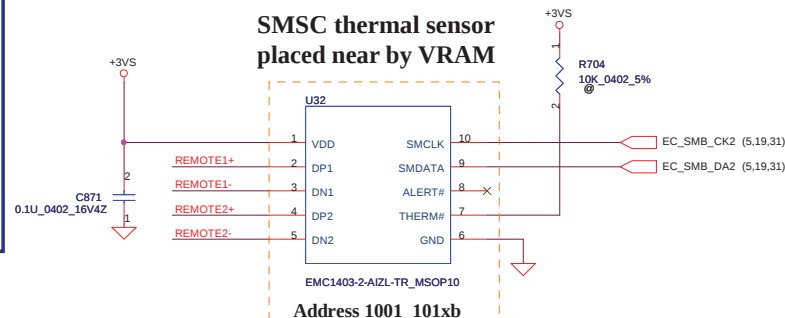
wide 30MIL



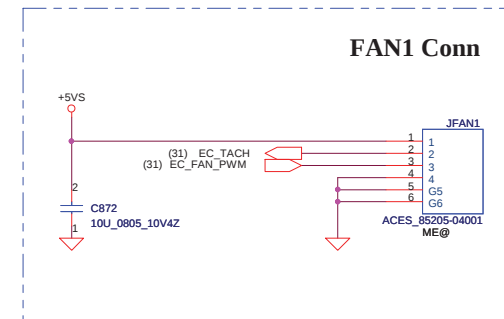
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LA6755P/7P				Size C	Document Number
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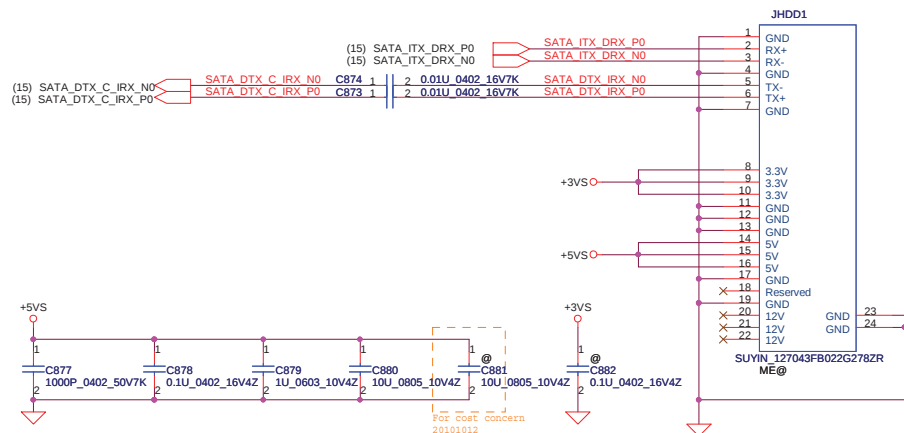
SMSC thermal sensor placed near by VRAM



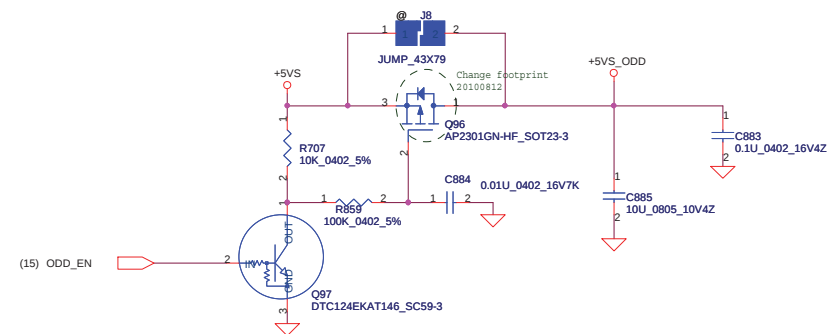
REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"



SATA HDD Conn.

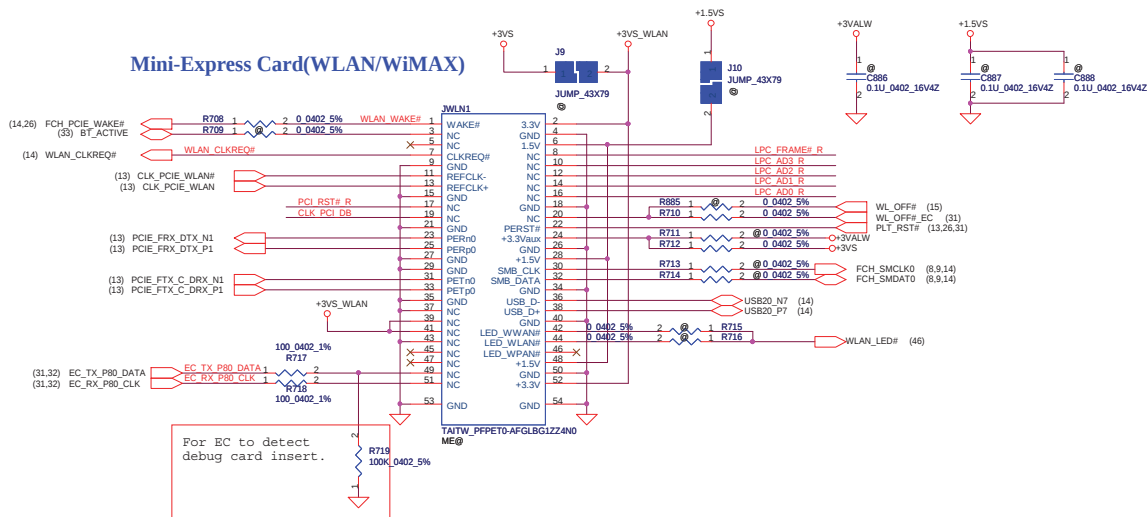


ODD Power Control



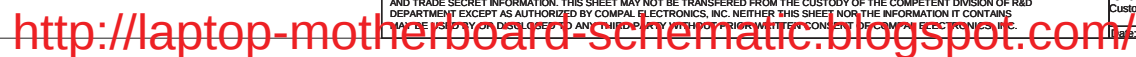
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				LA6755P/7P	
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Mini-Express Card for WLAN/WiMAX(Half)

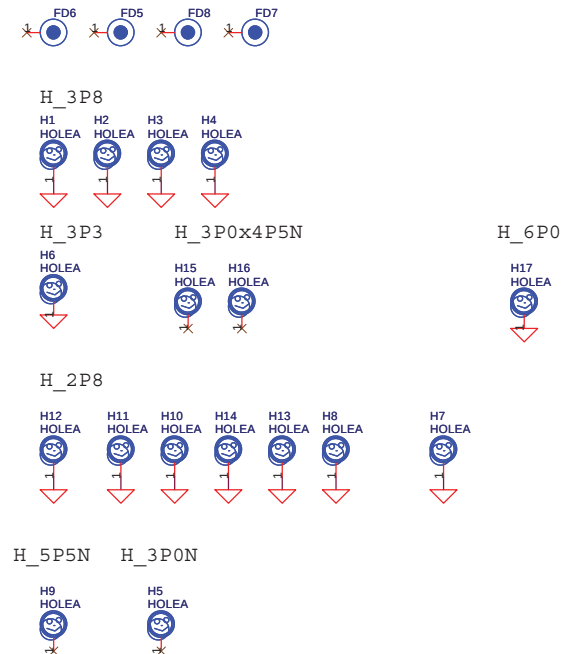
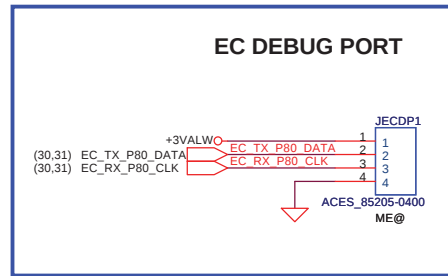
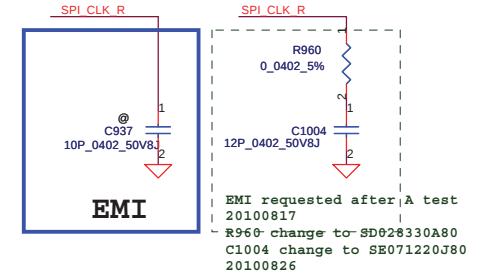
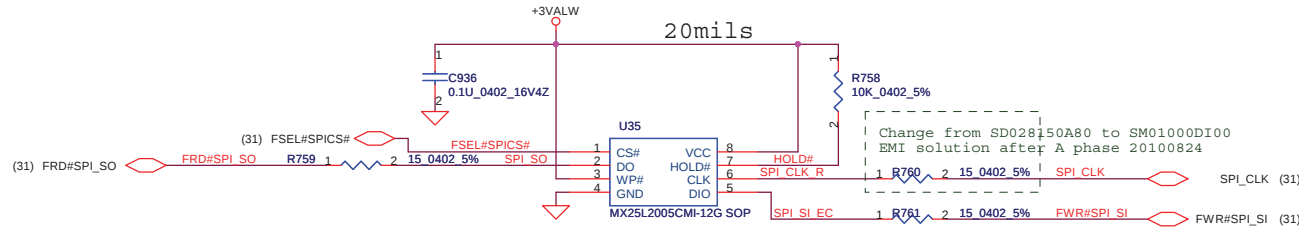


Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

LPC_FRAME# R	R720	1	0.0402 5%	LPC_FRAME#	LPC_FRAME# (13,31)
LPC_AD3 R	R721	1	0.0402 5%	LPC_AD3	LPC_AD3 (13,31)
LPC_AD2 R	R722	1	0.0402 5%	LPC_AD2	LPC_AD2 (13,31)
LPC_AD1 R	R723	1	0.0402 5%	LPC_AD1	LPC_AD1 (13,31)
LPC_AD0 R	R724	1	0.0402 5%	LPC_AD0	LPC_AD0 (13,31)
PCI_RST# R	R725	1	0.0402 5%	PLT_RST#	PLT_RST# (13,26,31)
CLK_PCIE_DB				CLK_PCIE_DB	CLK_PCIE_DB (13)

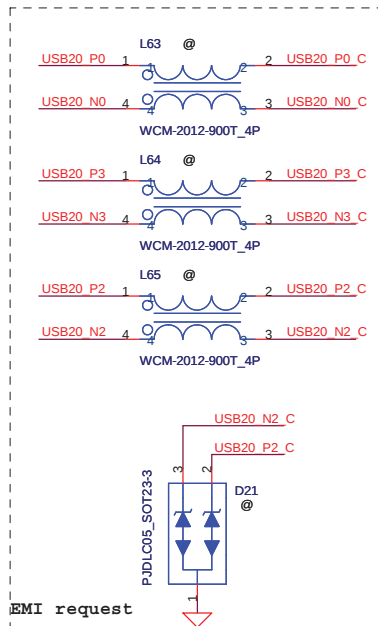
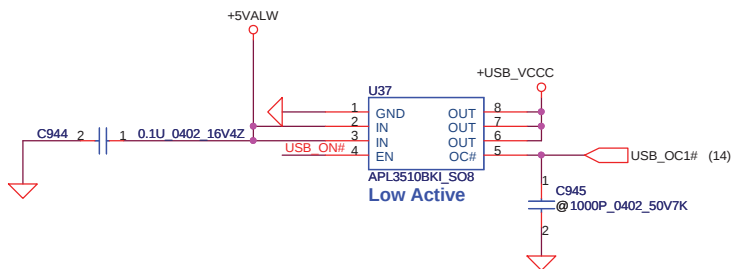
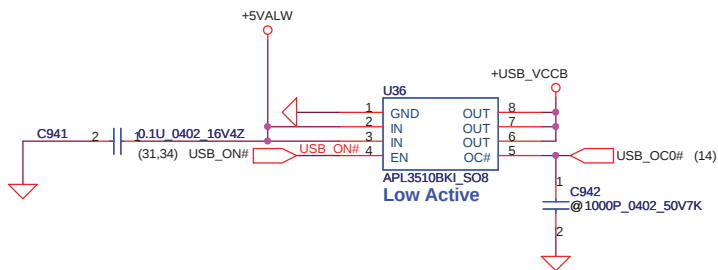


FOR EC 128KB SPI ROM
(150mil PACKAGE)
SA00003FL10
SA00003JD00



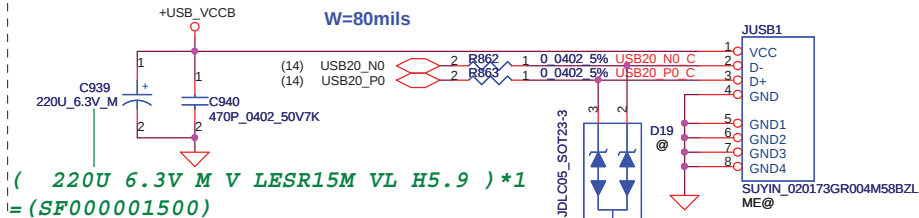
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Size	3	Document Number	LA6755P/7P	Rev	1.0
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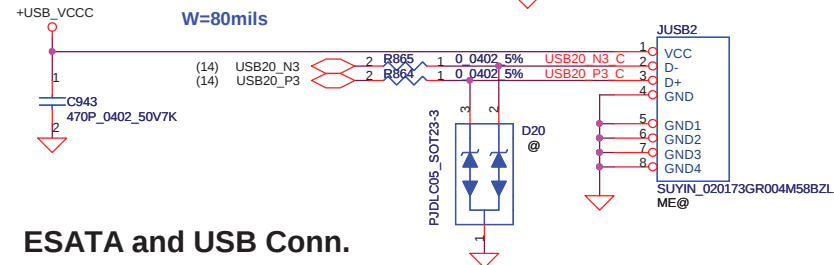


(220U 6.3V M 6.3X4.2) *1=(SF000002Y00)

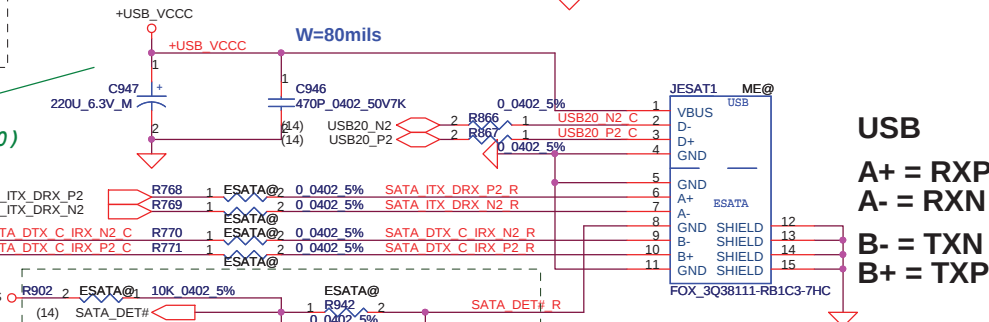
Left USB Conn.



Left USB Conn.

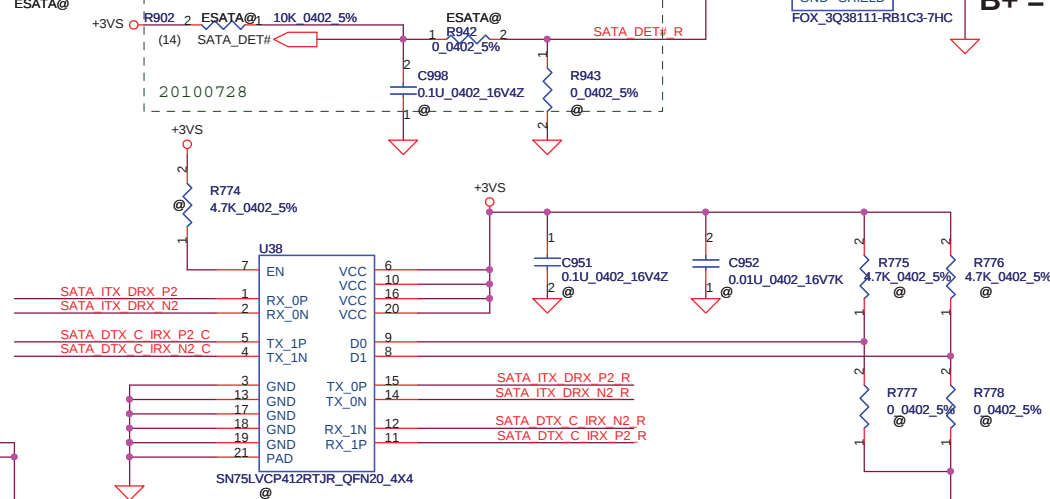
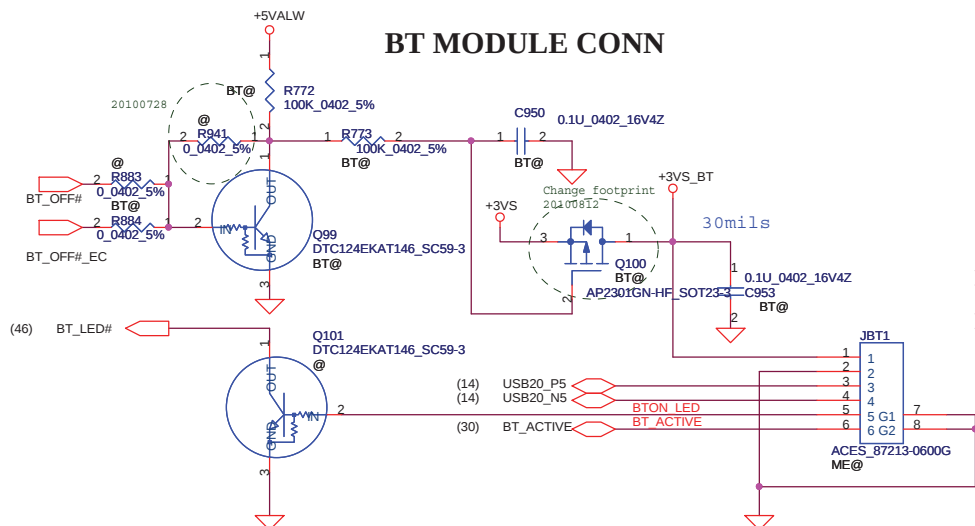


ESATA and USB Conn.



USB
A+ = RXP
A- = RXN
B- = TXN
B+ = TXP

BT MODULE CONN



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				Size	Document Number	Rev
				LA6755P/7P		1.0
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Bottom Side



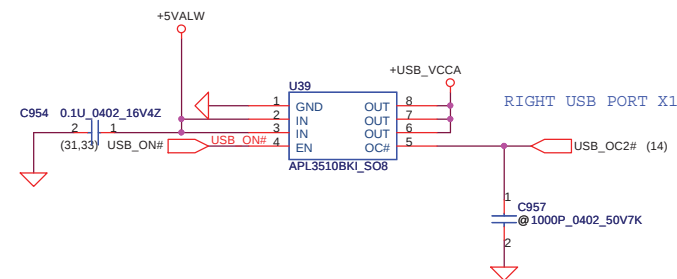
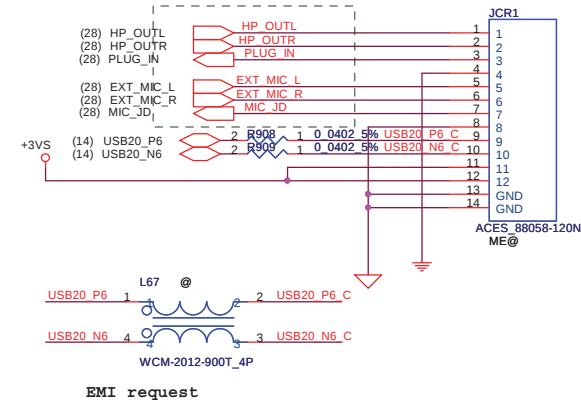
(31) NUM_LED#

(31) CAPS_LED#

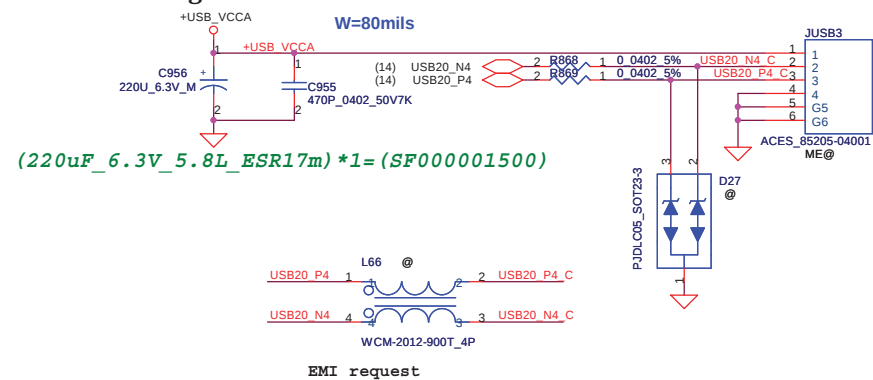
(31,46) PWR_LED#



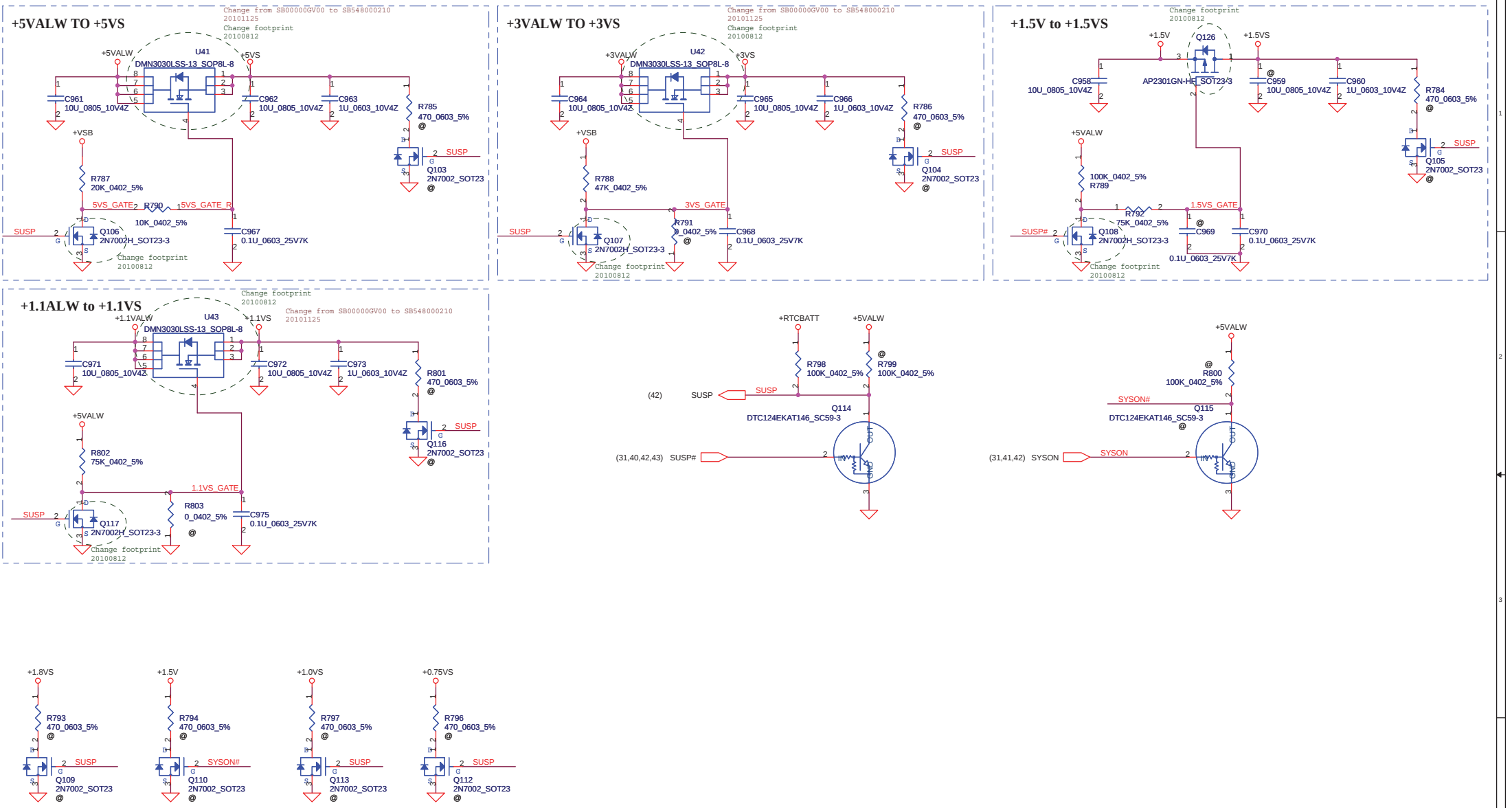
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Pin swap
20100810
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W=80mils

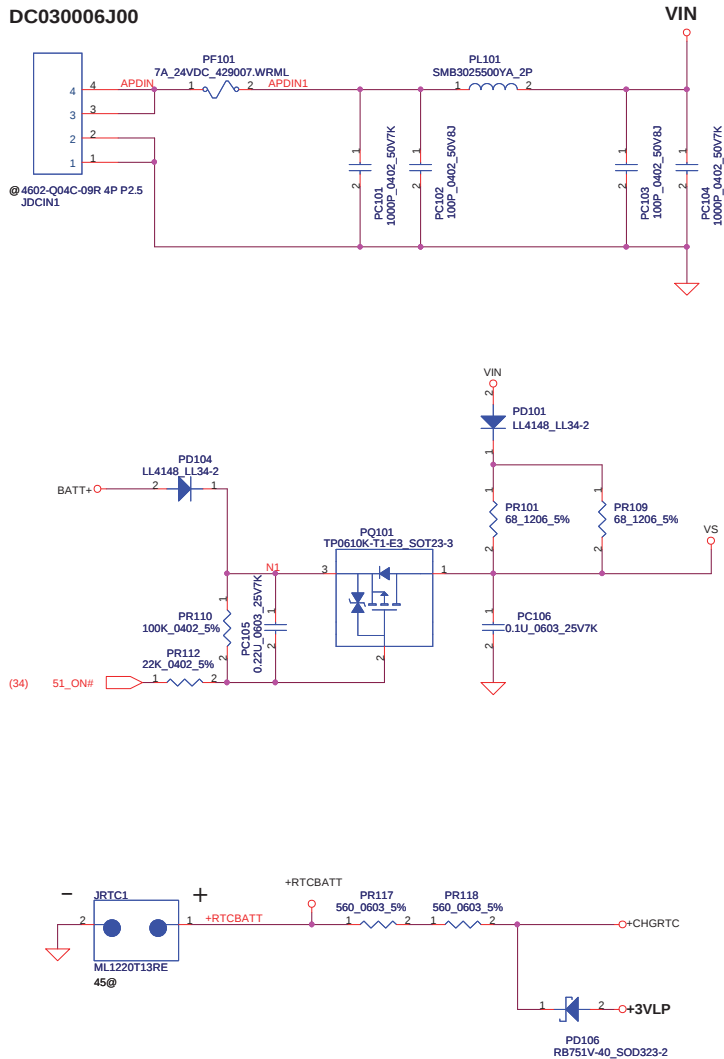


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				Size Custom	Document Number	Rev 1.6
				LA6755P/7P		
Date: Tuesday, November 30, 2010				Sheet: 34 of 48		

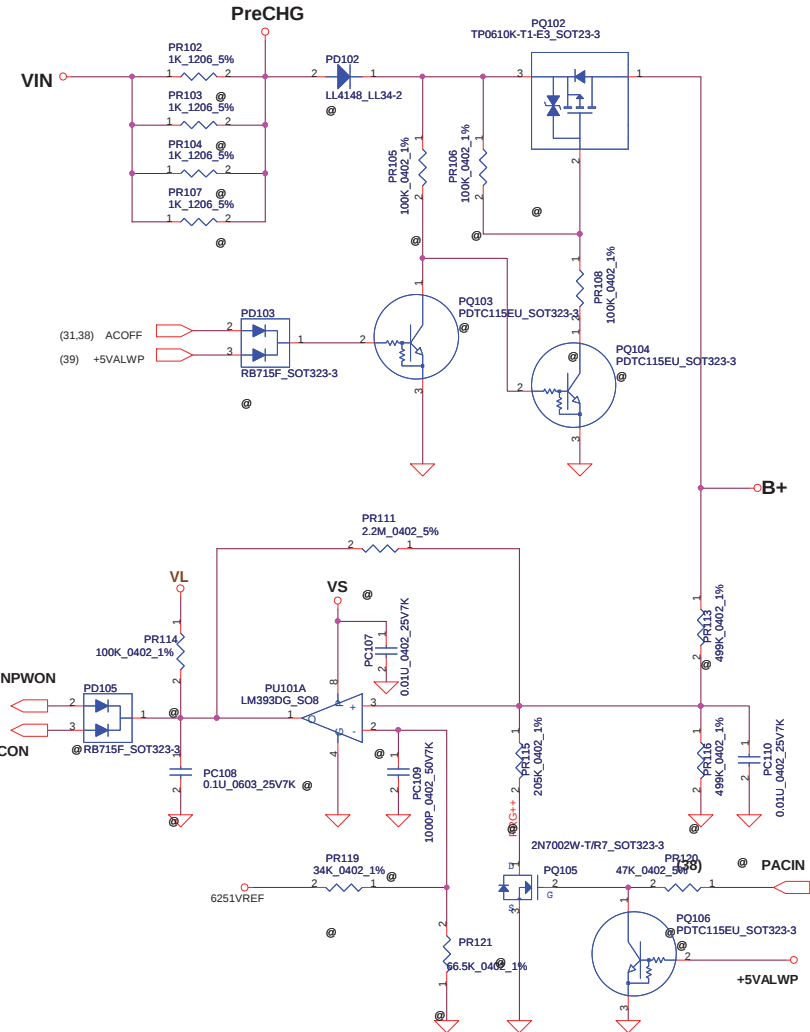


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				Size	Document Number	Rev
				Customer	LA6755P/7P	1.0
Date:		Tuesday, November 30, 2010		Sheet	35	of 48

DC030006J00



Precharge detector
15.97V/14.84V FOR
ADAPTOR



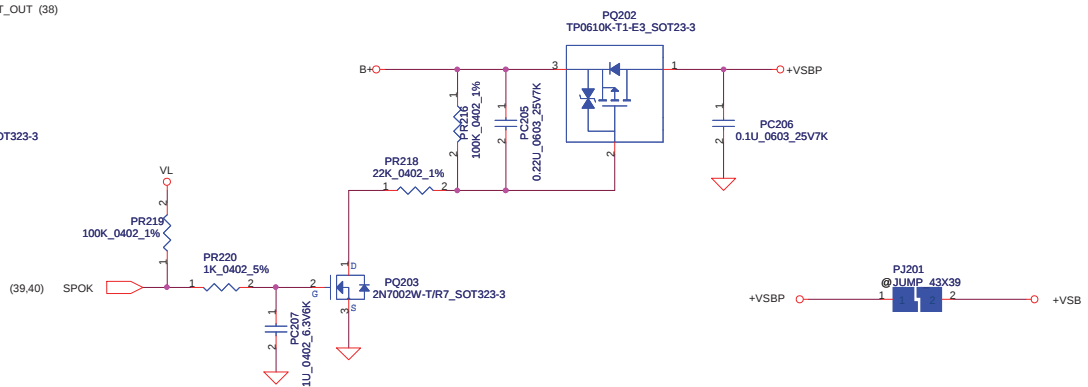
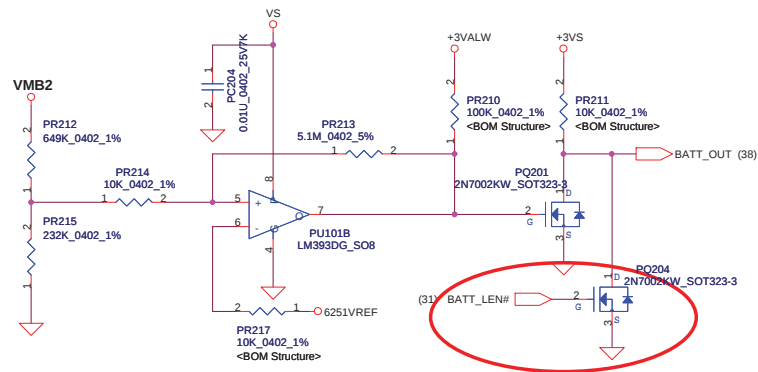
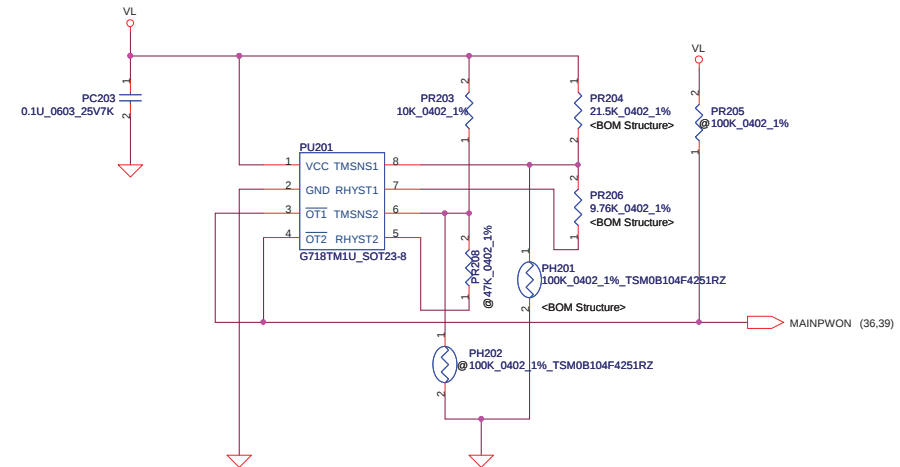
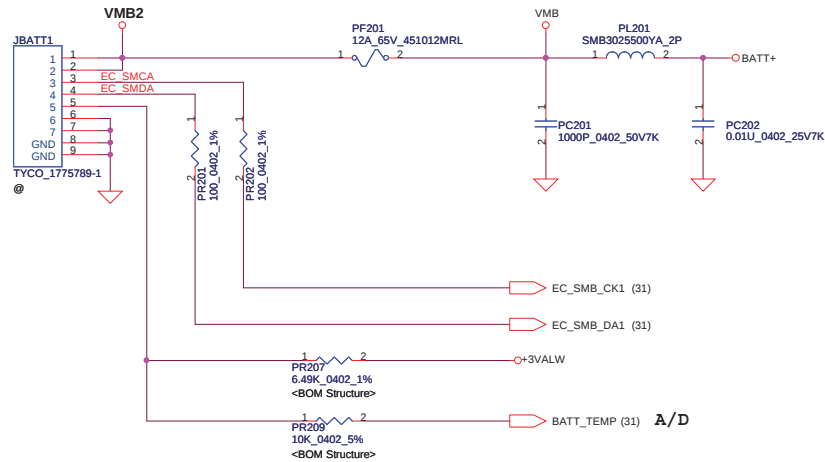
ACIN

Precharge detector			
Min.	typ.	Max.	
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V

BATT ONLY

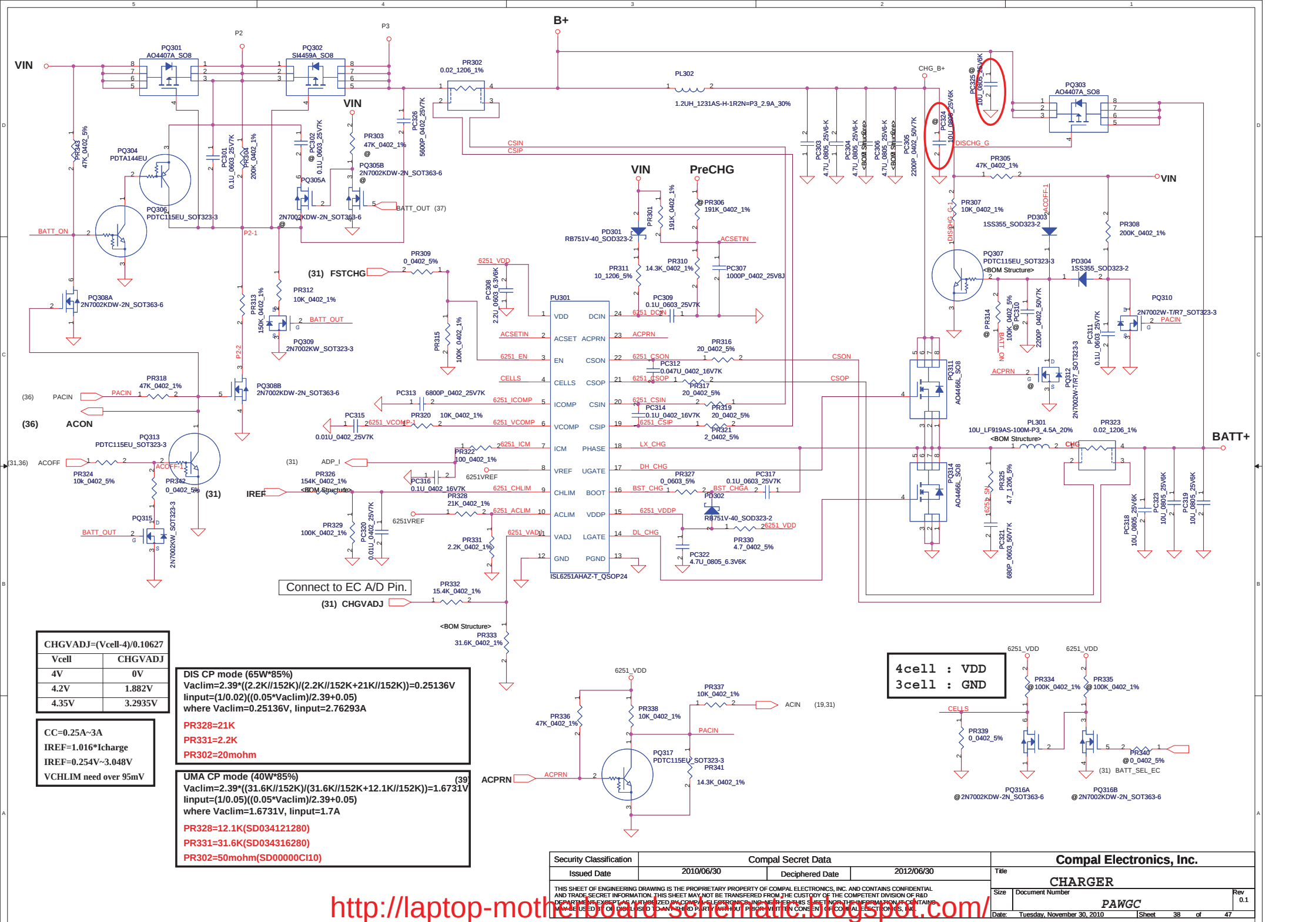
Precharge detector			
Min.	typ.	Max.	
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V

PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C

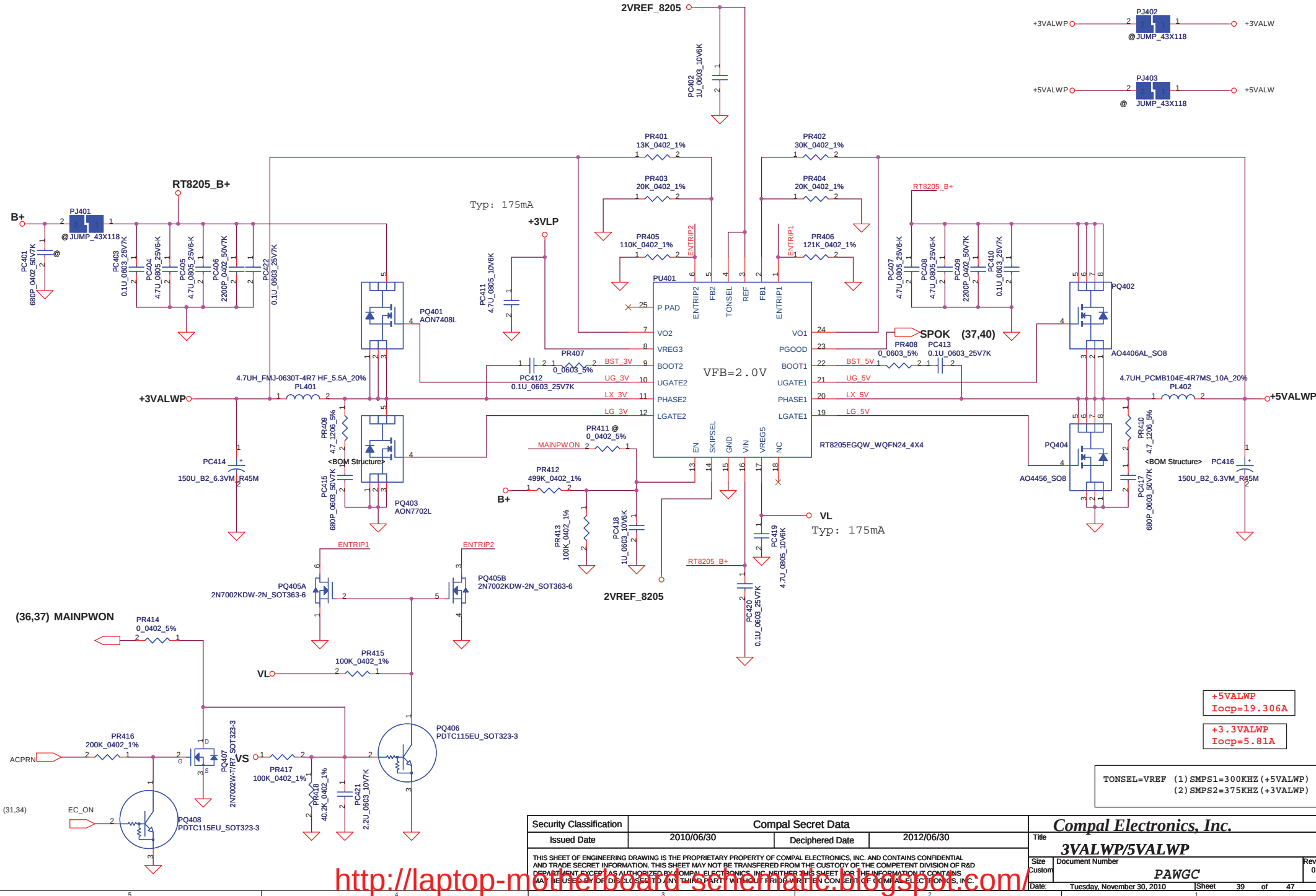


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Customer	Sheet	37	of	47	

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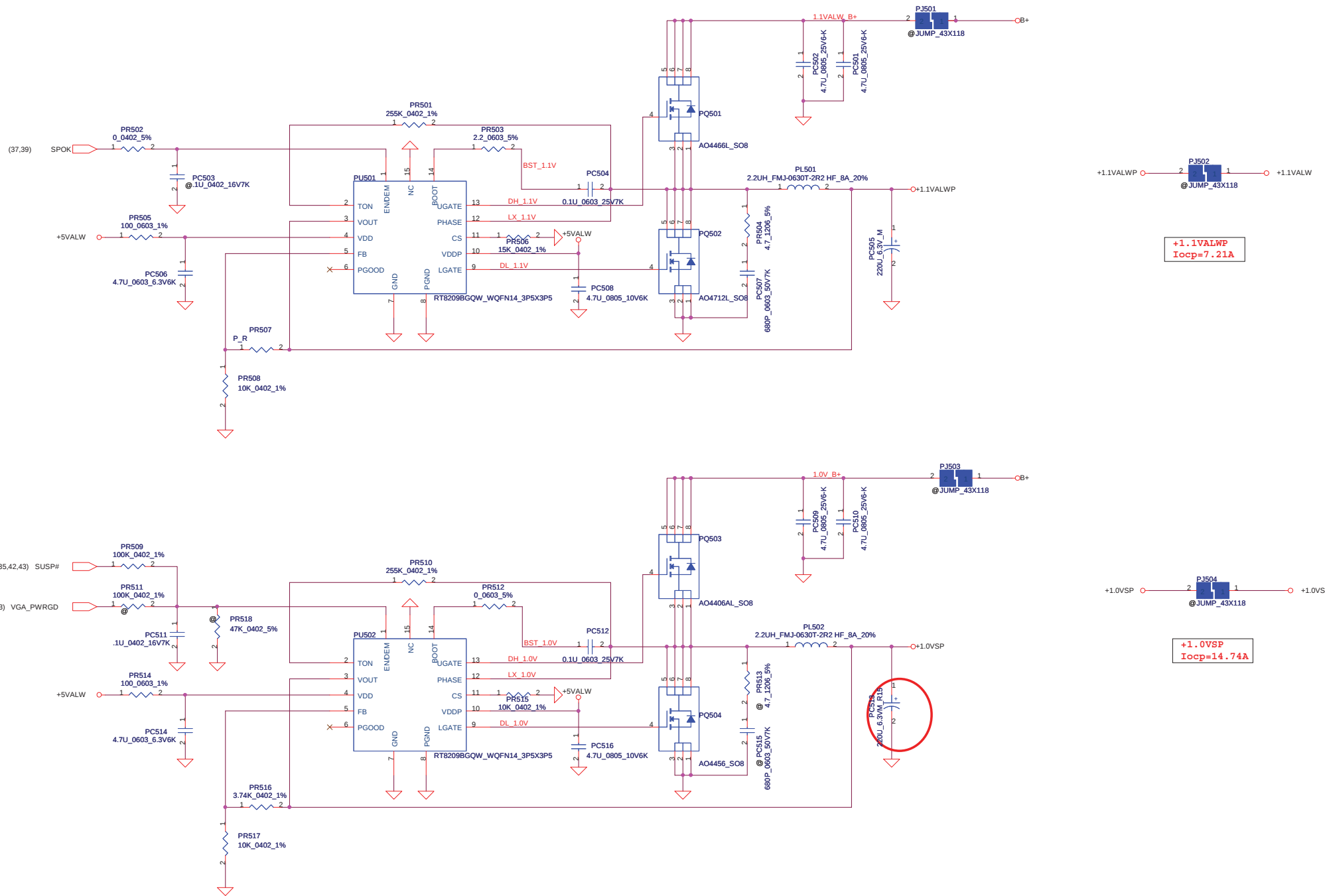


Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO

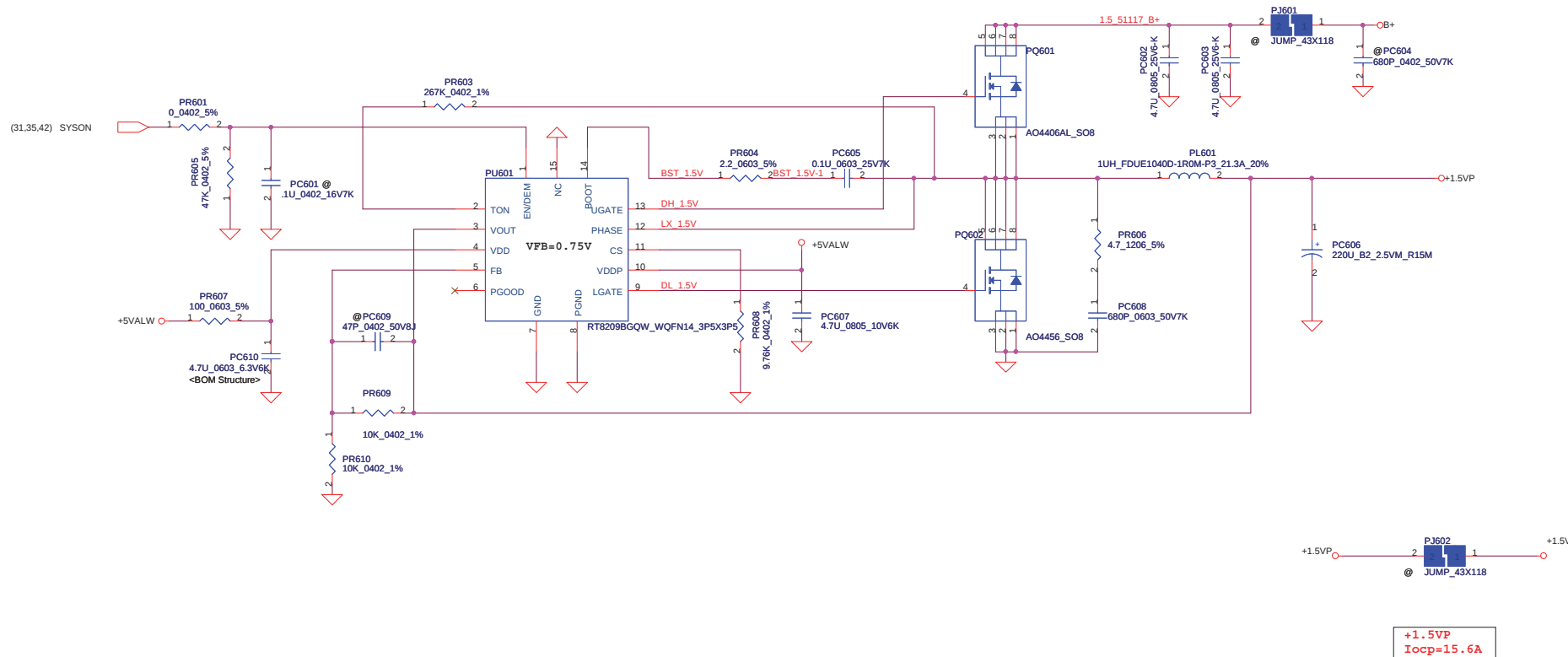


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				Date	Tuesday, November 30, 2010
				Sheet	39 of 47
				Rev	0.1

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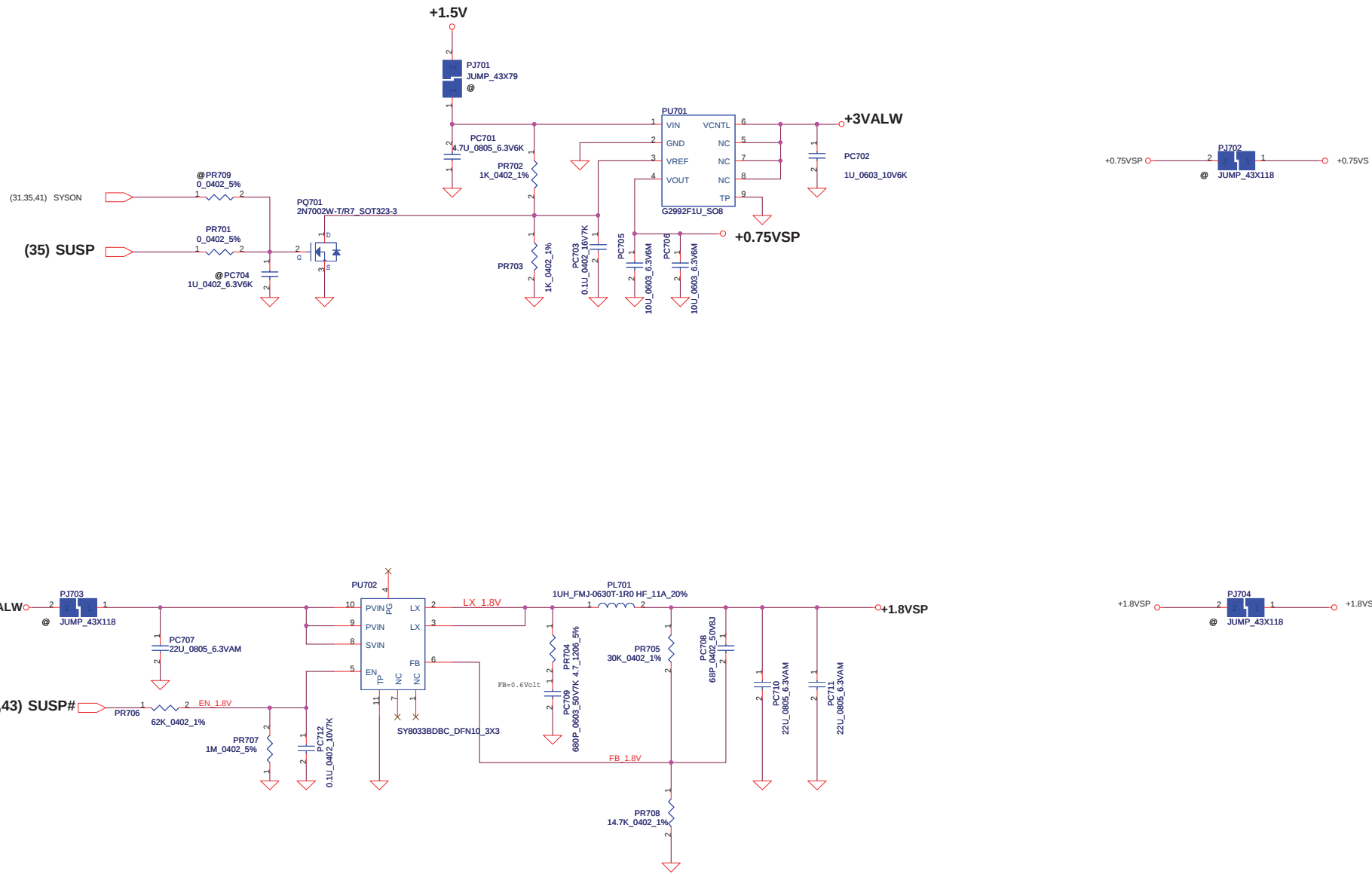


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Size		Document Number		Rev	
Date		Tuesday, November 30, 2010		PAWGC	
Sheet		40		of	
47					

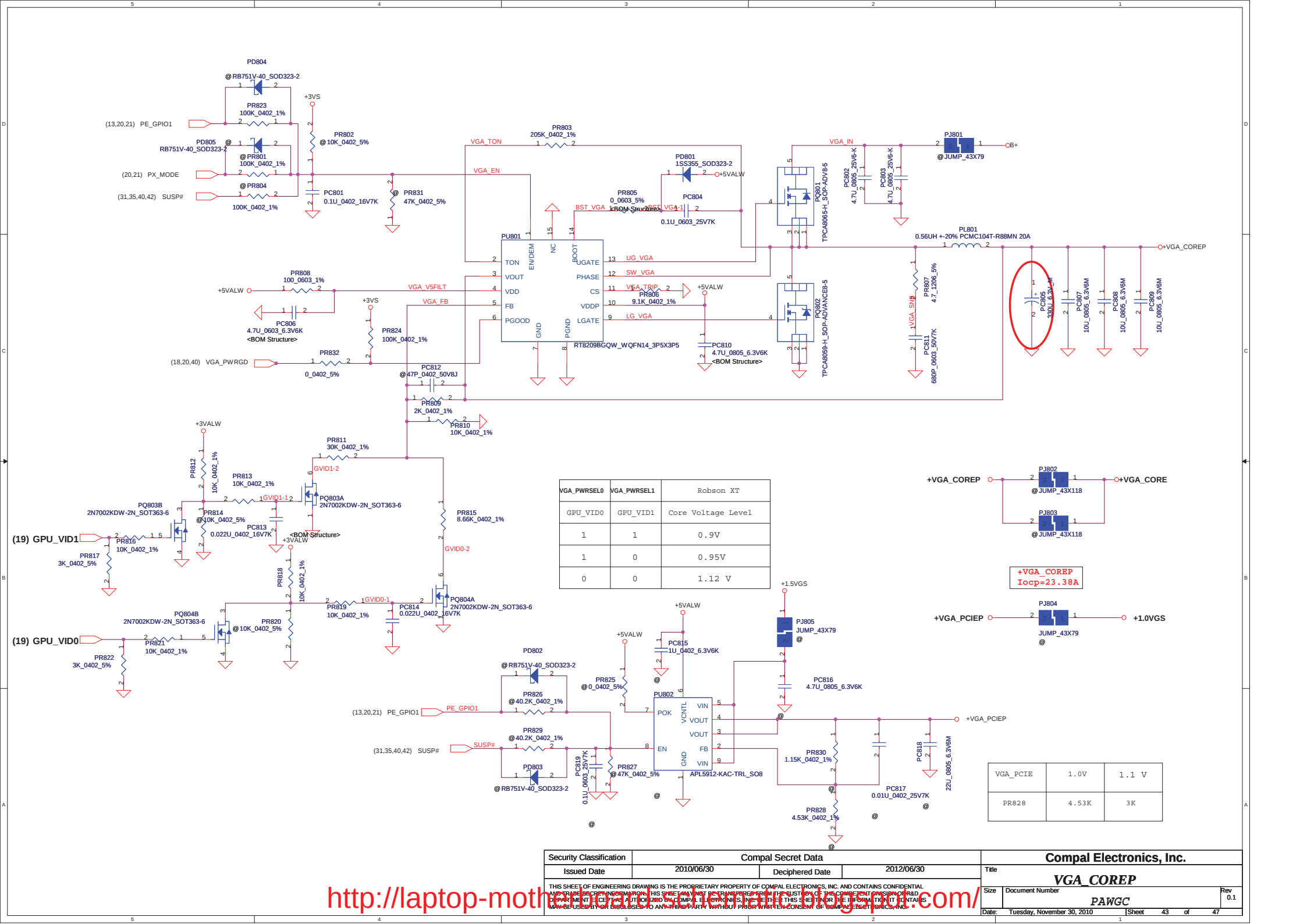


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				Sheet	41 of 47

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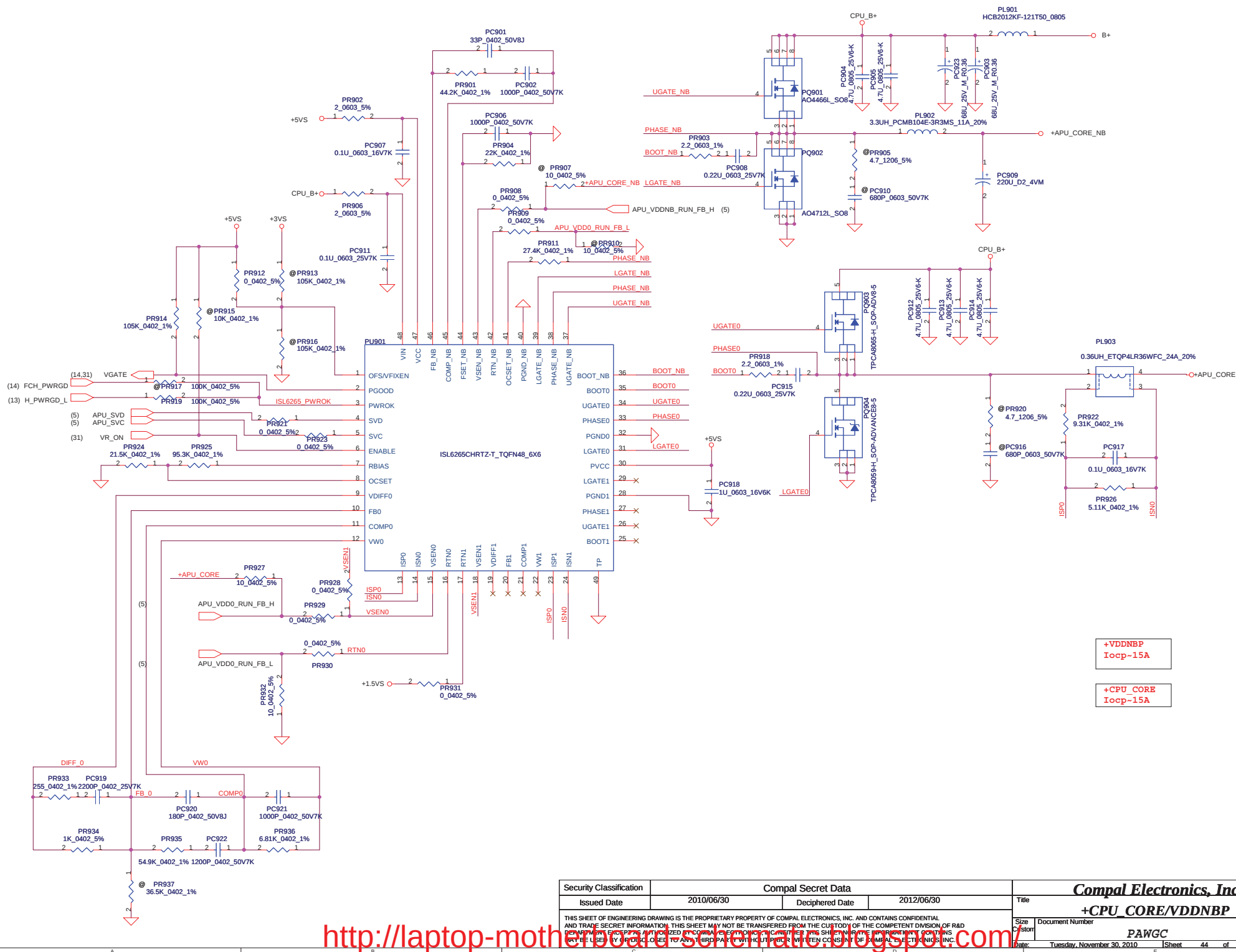


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VGA_PWSEL0	VGA_PWSEL1	Robson XT
GPU_VID0	GPU_VID1	Core Voltage Level
1	1	0.9V
1	0	0.95V
0	0	1.12 V

VGA_PCIE	1.0V	1.1 V
PR828	4.53K	3K



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				Size			
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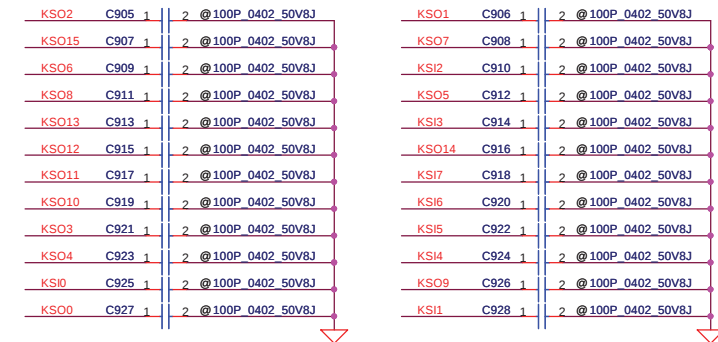
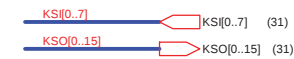
Size Document Number
Custom 1A-6755D/7P
Page 1 of 1
Date 10/20/2000 10:00 AM
User 10/20/2000 10:00 AM
Page 1 of 1

<i>Page #</i>	<i>Title</i>	<i>Date</i>	<i>Request Owner</i>	<i>Issue Description</i>	<i>Solution Description</i>
	power sequence	2010/07/30	HW		PR701 change to 0 ohm and PC704 non mount.
	Add PU802 for AMD's request	2010/09/21	AMD		
	Add PL302,PC324 and PC325 for EMC Solution.	2010/10/04	EMC		change PJ301 to PL302.
	Add PC422 for EMC Solution.	2010/10/06	EMC		
	Add PQ204 for EM6.0 battery learning function.	2010/11/12	PWR		

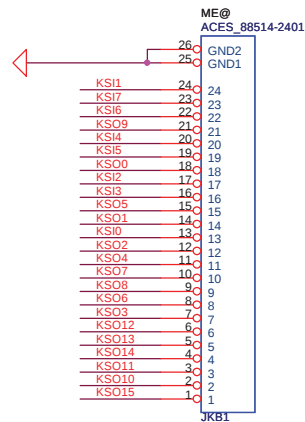
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				Rev 0.1	

(Use Rev. 10-2010) 15 pages 05 of 47

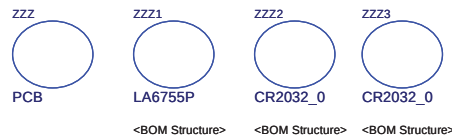
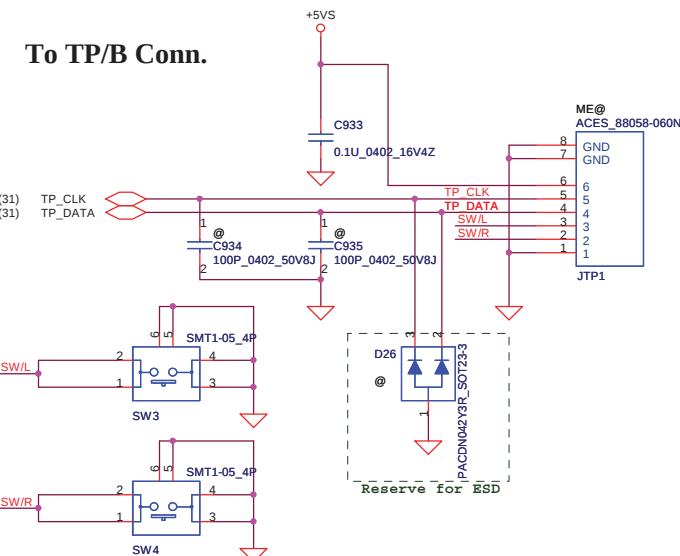
INT_KBD Conn.



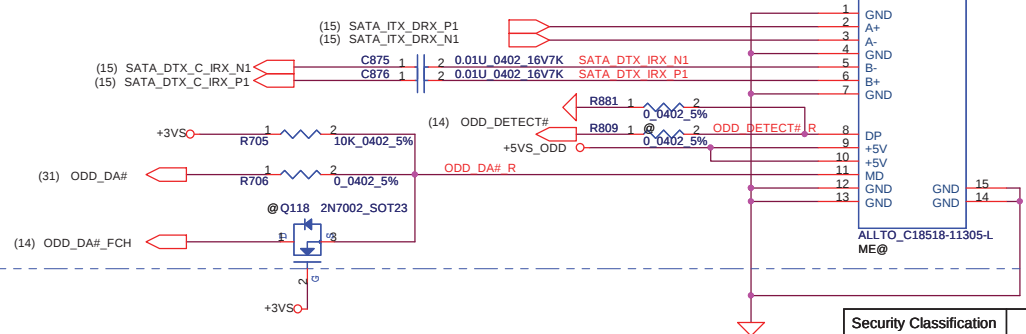
CONN PIN define need double check



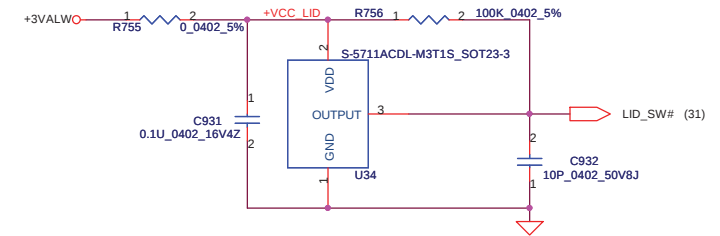
To TP/B Conn.



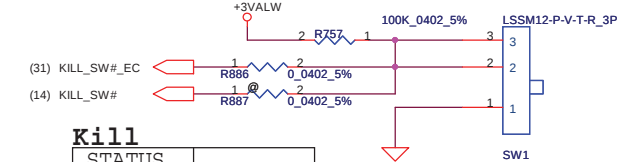
SATA ODD Conn.



Lid Switch



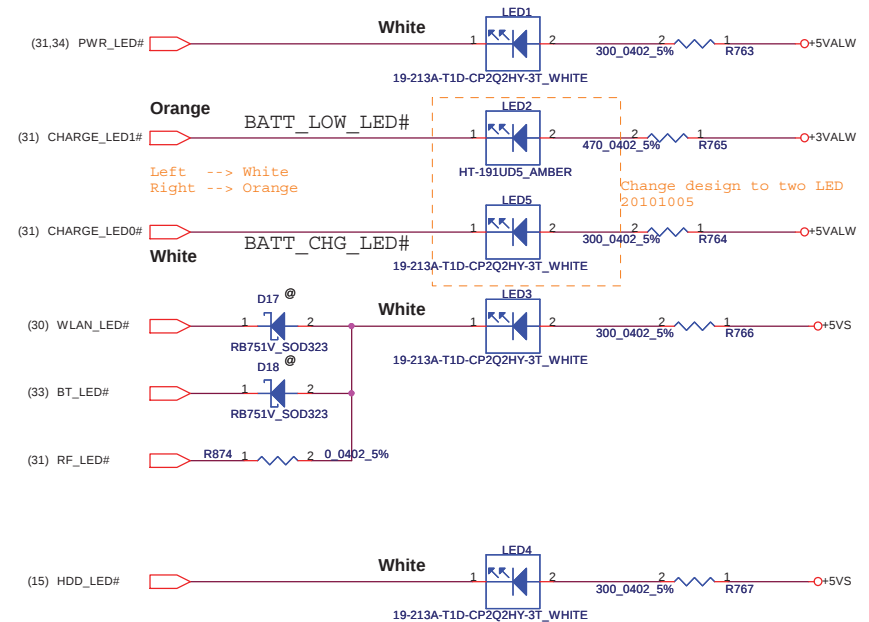
Kill Switch



Kill

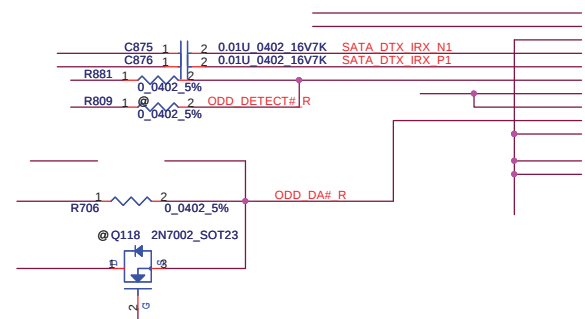
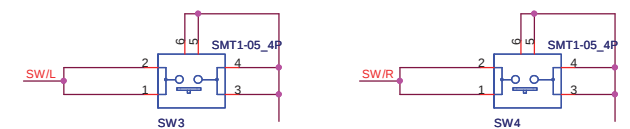
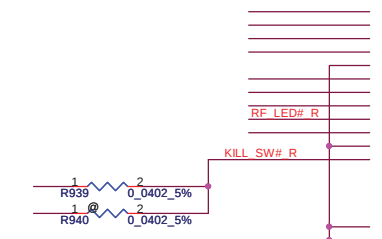
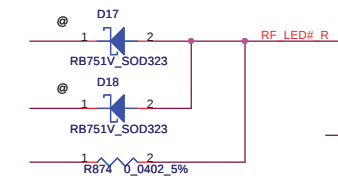
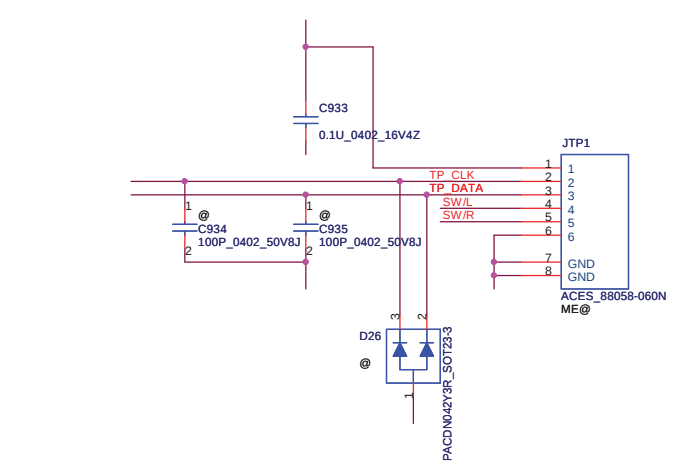
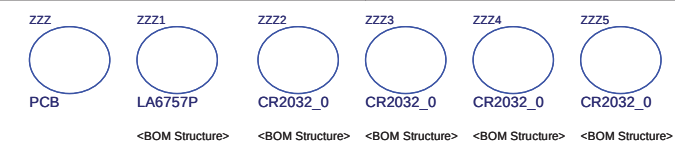
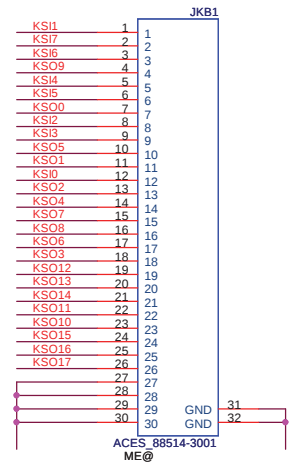
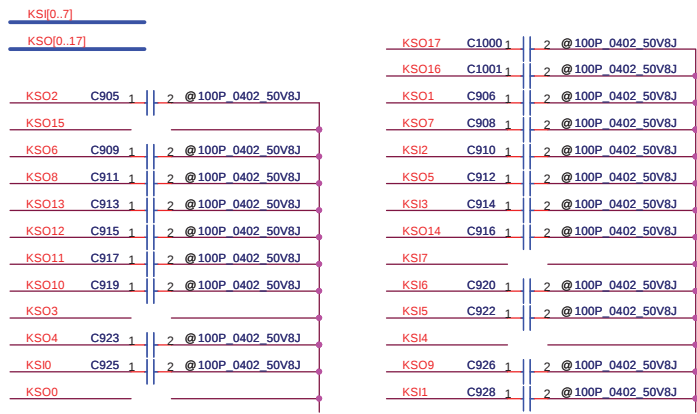
STATUS	
1, 2 (LOW)	OFF
2, 3 (HI)	ON

LED



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PHASE	PAGE	Modification list	PURPOSE
0.2	P08	C643 change to OS-CON type	For cost down purpose
0.2	P10	pop R490, unpop R491	LVDS PWM controls by EC
0.2	P10	Add CE_EN @ JLVDS1.16 and U33.98	For color engine function
0.2	P10	R488 pull-up to +5VALW	For C38 module design
0.2	P10	Add R938	For CMOS cost down purpose
0.2	P12	JCRT1 change foot-print from DC060003000 to DC060004800	Foot-print is wrong
0.2	P14	SATA_DET# change from U26.AE19 to U26.AB21	For corresponding SATA port assigned
0.2	P16	Delete R635	Our codec consumes +3V
0.2	P18	Add R936	For VGA_PWRGD reservation
0.2	P20	Q69 ~ Q72 change to N-MOS	Follow BACO suggestion SCH
0.2	P21	R840 pull-up change to +5VALW and R857 change to 20K ohms	For +3VGS sequence design
0.2	P21	Delete Q122, Add U47, C999, R944	For +1.0VGS DC power design
0.2	P23	L27 change to 0 ohms	For new reference circuit
0.2	P23	Delete GND connection of U8.N11 and U8.N12	For new reference circuit
0.2	P21	R344 change to 20K ohms	Prevent Q74 damage
0.2	P28	J7 foot-print update	Base on DFX request
0.2	P28	Add net CLK_PCF_DE_R and unpop R854	For EMI concern
0.2	P28	Modify PC_Beep circuit	Base on vender suggestion
0.2	P23	Delete C421, C422, C431, C432, C433	For new reference circuit
0.2	P31	R734 pull-high change to +5VALW	For USB ports ACIN leakage
0.2	P31	Add BATT_SEL_EC at U33.103	For Battery selection reservation
0.2	P33	Add R941	For further cost down purpose
0.2	P33	Add R942, R943, C998	For SATA_DET# function design
0.2	P28	Delete C851, C855	For useless AGND bridge
0.2	P34	Change JP7 to JPWRB1 and JP8 to JCR1	For standard naming
0.2	P34	Del U45, R890 ~ R899, J12, CHR_ON# (U33.70)	Deleting USB charge function
0.2	P35	Delete C974	Deleting unnecessary part for +1.1VS
0.2	P19	Add R945, R946	For HDMI Audio strap
0.2	P13	Delete T79, T80	For layout space needed for SATA calibration
0.2	P28	Add R947, R948	For EMI solution reservation base on vender suggetion
0.2	P28	Delete C857, R694	To delete redundant part base on vender suggestion
0.2	P28	L57 ~ L60 change to 0_0603_5%	Base on vender suggestion
0.2	P28	R672 change to 0ohm and location to be series on HDA_BITCLK_AUDIO	For EMI solution reservation base on vender suggetion
0.2	P14	Kill_SW# change from U26.G24 to U26.K1	Kill_SW# function needs event pin
0.2	P31	Add R949, C1002	Requirement of implementing SUSCLK
0.2	P28	Add R950 @ +3VS, R951 @ +LDO_OUT_3.3V, R952 @ +5VS	For customer request (PWR consumption)
0.2	P28	Add R953	For PC Beep circuit
0.2	P29	Add R954, R955	For customer request (PWR consumption)
0.2	P13	Add C1003, U48, R956, R957	For PX_GPU_RST# function
	P18	Delete R556, R841, R889, D28	
0.2	P05	Add R958	For enabling HDMI function
0.2	P28	Add R959	For EMI reservation
0.2	P32	Add R960 and C1004	For EMI reservation
0.2	P09	Add R961 and R962	For DDR SO-DIMMB strap pin reservation
0.2	P05	Delete T74, T75	For layout limitation
0.3	P29 P46	change +5V_ODD to +5VS_ODD	For better net name
0.3	P32	R760 change to 100ohm bead and R761 change back to 15ohm resistor	For correct EMI solution
0.3	P21	U47 change to SB00000GV00 footprint	For correct symbol
0.3	P05	R958 change to HDMI@ and R422 change to nonHDMI@	For SKU without HDMI function
0.3	P21	Add PX_MODE off page	For design correction

Change footprint : For cost down purpose to change parts
20100812

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0.2	P35	Delete C974	Deleting unnecessary part for +1.IVS
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0.2	P28	Delete C857, R694	To delete redundant part base on vender suggestion
0.2	P28	L57 ~ L60 change to 0_0603_5%	Base on vender suggestion
0.2	P28	R672 change to 0ohm and location to be series on HDA_BITCLK_AUDIO	For EMI solution reservation base on vender suggetion
0.2	P14	Kill_SW# change from U26.G24 to U26.K1	Kill_SW# function needs event pin
0.2	P31	Add R949, C1002	Requirement of implementing SUSCLK
0.2	P28	Add R950 @ +3VS, R951 @ +LDO_OUT_3.3V, R952 @ +5VS	For customer request (PWR consumption)
0.2	P28	Add R953	For PC Beep circuit
0.2	P29	Add R954, R955	For customer request (PWR consumption)
0.2	P13	Add C1003, U48, R956, R957	For PX_GPU_RST# function
0.2	P18	Delete R556, R841, R889, D28	
0.2	P05	Add R958	For enabling HDMI function
0.2	P28	Add R959	For EMI reservation
0.2	P32	Add R960 and C1004	For EMI reservation
0.2	P09	Add R961 and R962	For DDR SO-DIMMB strap pin reservation
0.2	P05	Delete T74, T75	For layout limitation
15 only part			
0.2	P46	Add C1000, C1001	For 15" 30pin KB connector

Change footprint
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PHASE	PAGE	Modification list	PURPOSE
0.3	P14	R603 and R604 change to pop	For SM Bus pull-high
0.3	P23	Reserve C1005	For PWR team request reserving a 330u capacitor
0.3	P33	C939 change to 5.9H OS-con	For cost saving
0.3	P33	R902 and R942 change to unpop	For eSATA function deletion
0.3	P29	U32 change PN to SA000046C00	For main source PN concern
0.3	P05	Delete JHDT1	For layout limitation
0.3	P11	Add F2 and change SM-BUS pull high net name to +5VS_HDMI_F	For safety team requirement
0.3	P21	change J3 footprint	For larger jumper footprint
0.3	P21	R856 change from 20K to 39K	For VGA power sequence
0.3	P11	Add net name +5VS_HDMI_F	For power trace indecation
0.3	P20	Change Q69 ~ Q72 PN	For design correction
0.3	P28	Add R963	For 20671-21Z update
0.3	P28	Change U31 PN to SA00003K410	For 20671-21Z PN
0.3	P20	U10.5, U46.5, and U44.5 change from +3VS to +3VGS	For BACO circuit update
0.3	P28	Delete R951	For unnecessary part deletion
0.3	P07	C623 change to unpop	Base on AMD checklist
0.3	P16	Delete C734, add C1006, C1007	For ME concern
0.3	P21	R924 cahgne pull-up from +3VS to +3VALW	For BACO design correction
0.3	P21	R925 change to pop	For BACO design correction
0.3	P14	Reserve C1008 at FCH_PWRGD	For EMI request
0.3	P14	Reserve C1009 at VGATE	For EMI request
0.3	P31	Reserve C1010 at VR_ON	For EMI request
0.3	P13	Reserve C1011 at H_PWRGD_L	For EMI request
0.3	P28	pop C849, C850, R692, R693, R696, C826	For EMI request
0.3	P27	Add C1012, C1013	For EMI request (gas discharge tube)
0.3	P27	Add D1	For EMI request (ESD diode)
0.3	P28	update R672 location	For EMI request (RC to GND for codec BIT_CLK)
0.3	P07	Delete C617	For EMI solution space needed
0.3	P28	Pop D30, D31, unpop R953	For FCH PC-beep function
0.3	P31	R751 and R752 change from 4.7K ohm to 2.2K ohm	For PWR team request
0.3	P13	C719, C720 change from 22P to 18P	For RTC design
14" only	part		
0.3	P46	Change one dual-diode LED2 to two single diode LED2 and LED5	For design change
1.0	P5	unpop R415	AMD checklist update
1.0	P10	R486, R487 change pull-high to +5VS	AMD checklist update
1.0	P11	R522, R523 change from 2.2K to 2K	AMD checklist update
1.0	P12	reserve R964, R965, change R546 ~ R549 from 4.7K to 2K	AMD checklist update
1.0	P31	BATT_LEN# added to U33.38	PWR team request
1.0	P20	Delete R341	For design update
1.0	P21	Delete R837, R832, R836	For design update
1.0	P28	Delete R947, R948, R950, R952	For design update
1.0	P29	Delete R955, R954, R810	For design update
1.0	P30	unpop C887, C888	For design update
1.0	P25	unpop C494, C484, C498, C482, C490	For design update

Change footprint
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