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Compal Confidential

Schematics Document
P4 uFCBGA/uFCPGA Northwood with SIS Core Logic

2001-5-30

REV:1.0A

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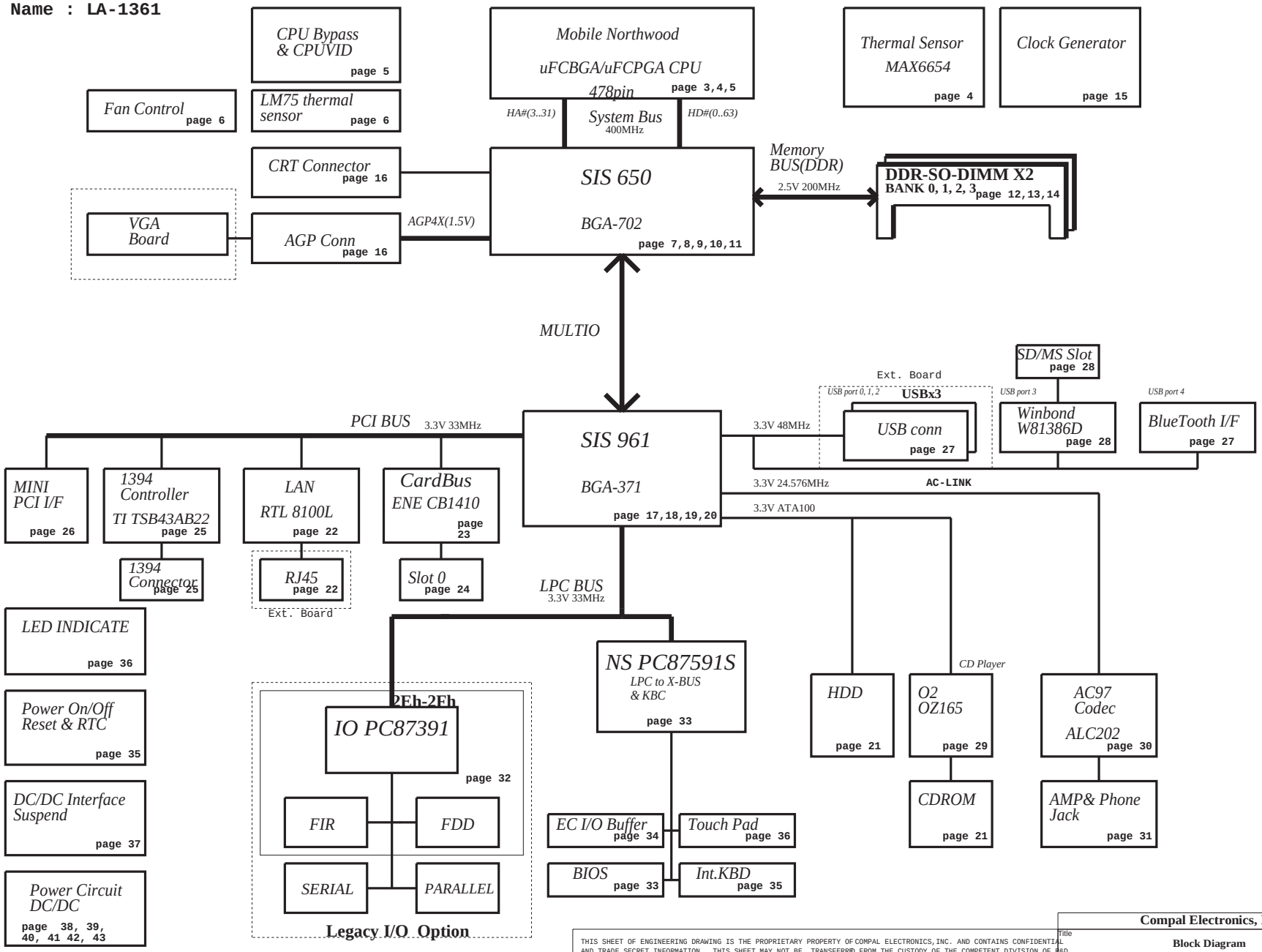
Block Diagram

Model Name :CT10

File Name : LA-1361



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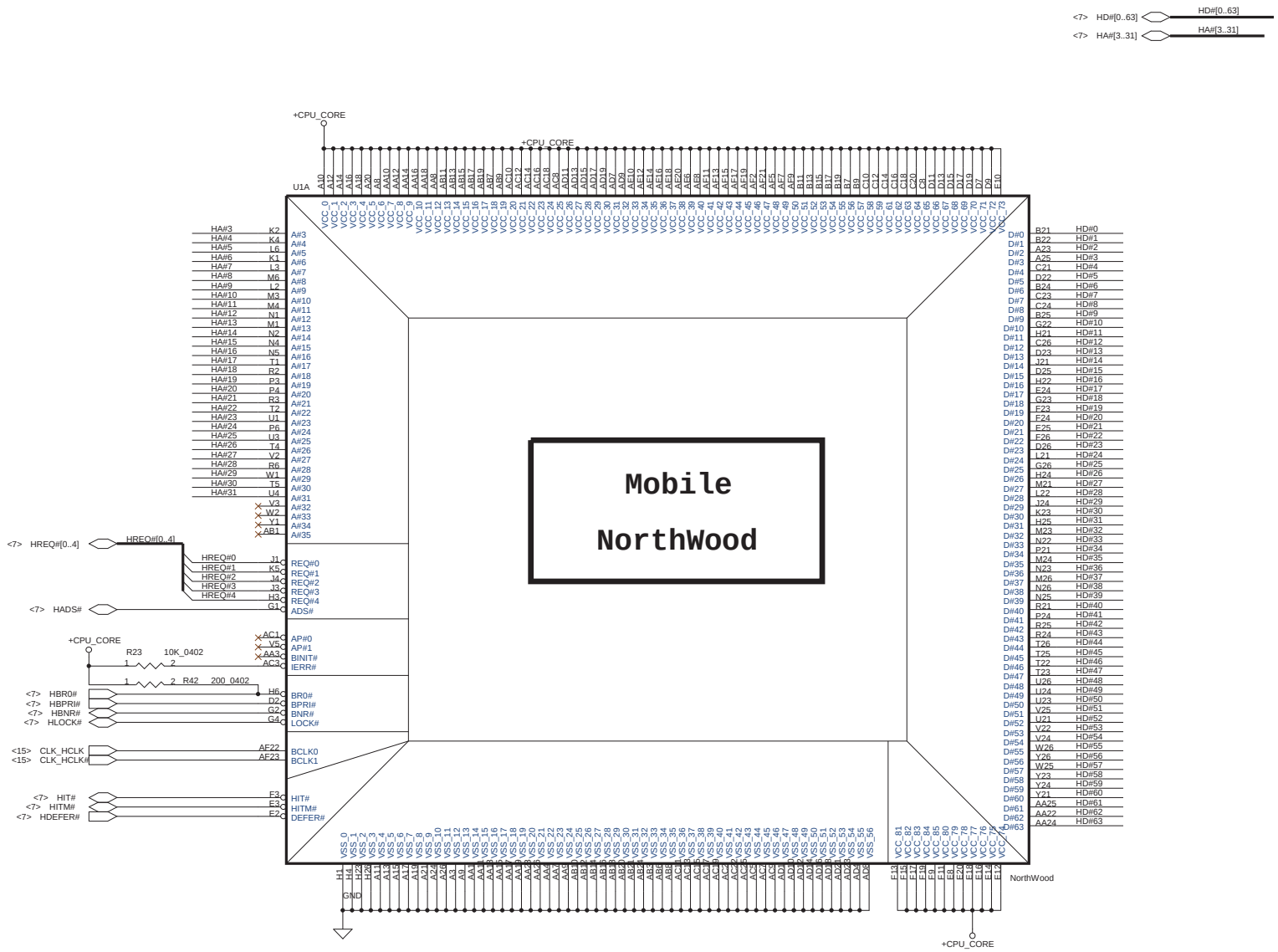

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Title	Mobile Northwood uFCPGA
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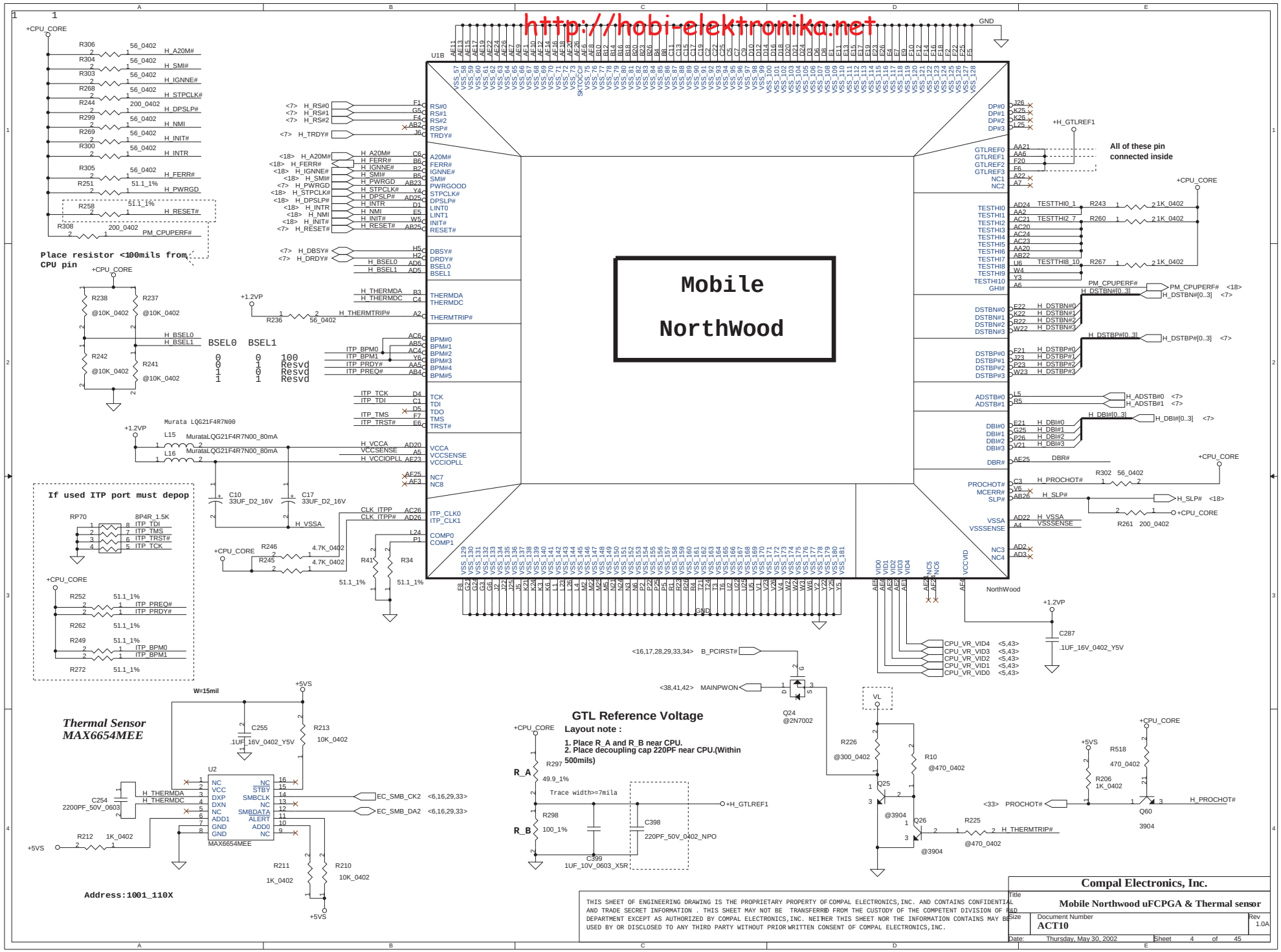

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Title: Mobile Northwood uFCPGA & Thermal sensor

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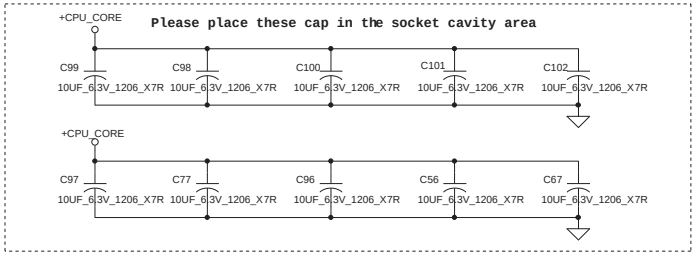
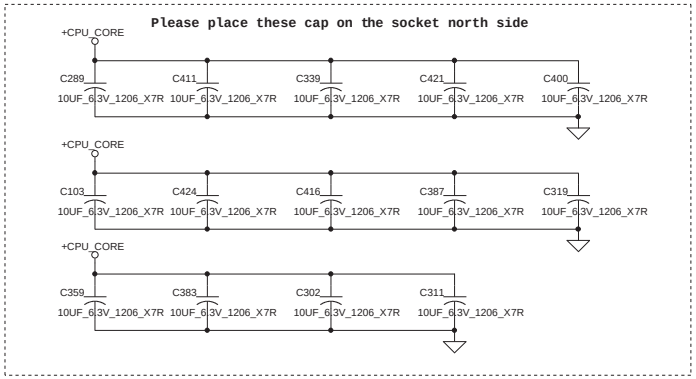
Layout note :

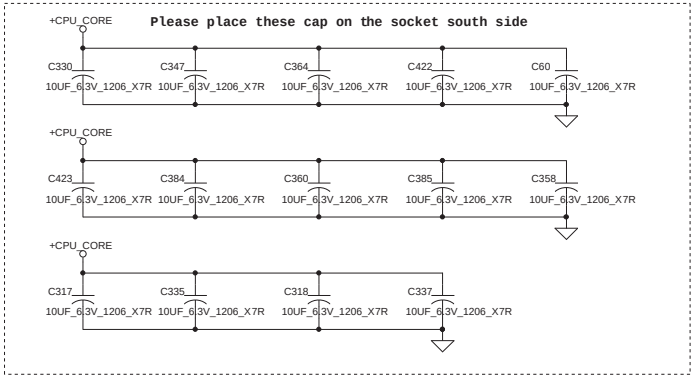
Place close to CPU, Use 2~3 vias per PAD.
Place .22uF caps underneath balls on solder side.
Place 10uF caps on the peripheral near balls.
Use 2~3 vias per PAD.

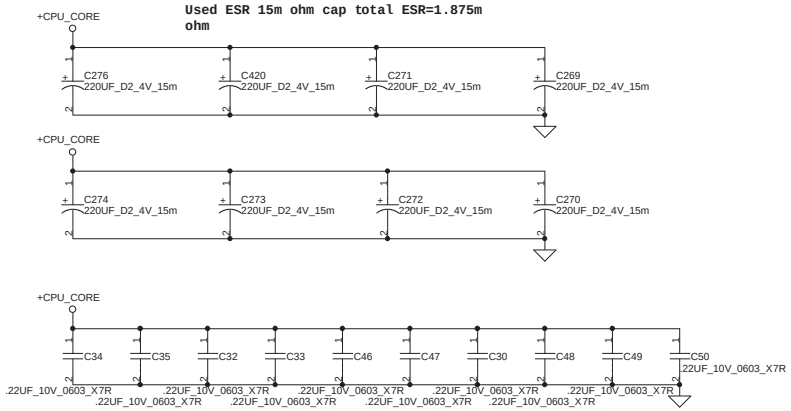
Layout note :

Place close to CPU power and ground pin as possible (<1inch)

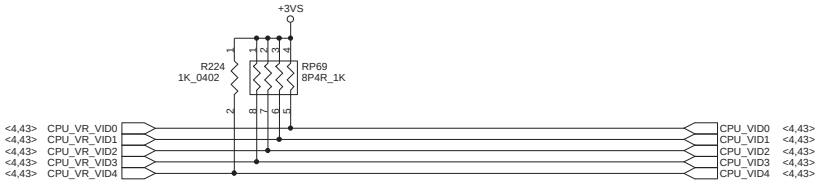




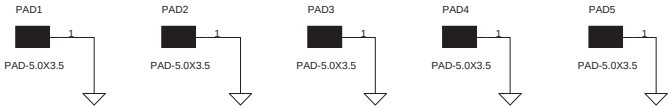




CPU Voltage ID



EMI Clip PAD for CPU



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Compal Electronics, Inc.			
Title	CPU Bypass & CPU VID		
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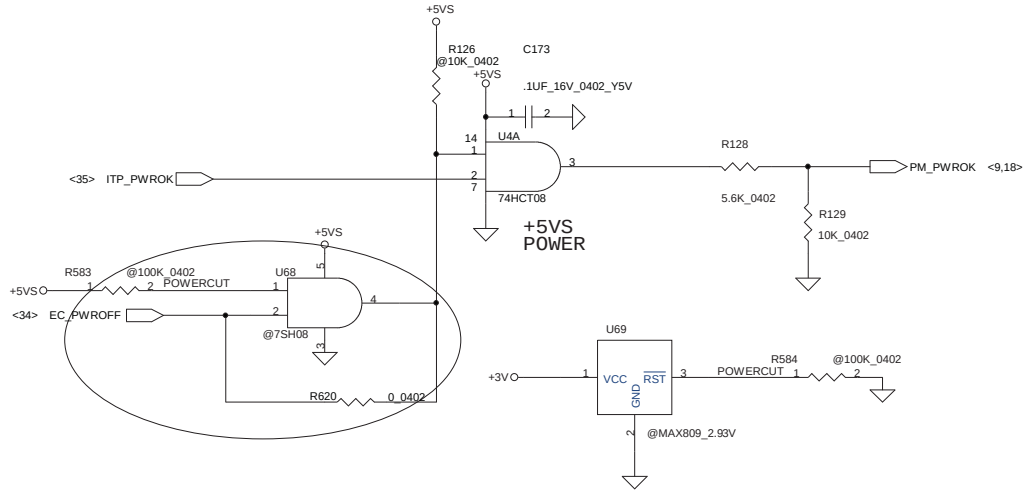
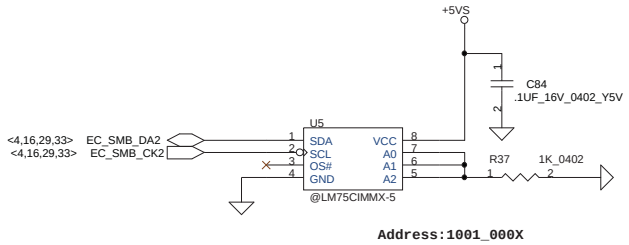
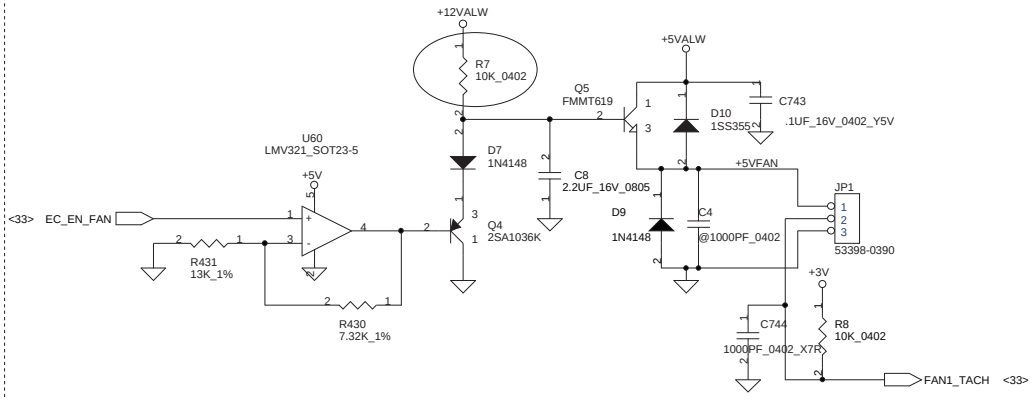




Dectect PCB Thermal

Fan1 Control circuit



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COMPAL Electronics,Inc	
Title	LM75 Thermal sensor & Fan control
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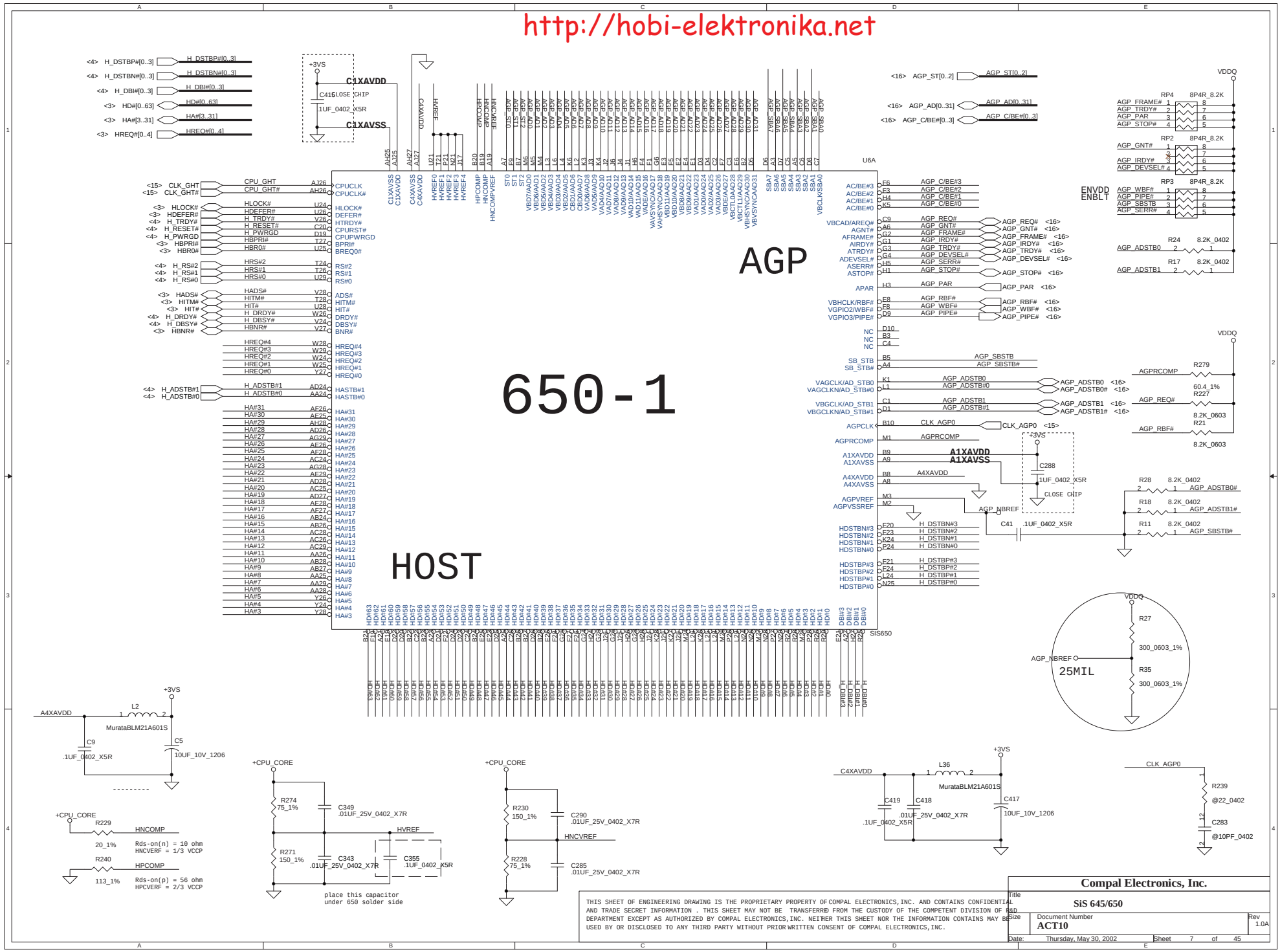

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Compal Electronics, Inc.	
Title	SiS 645/650
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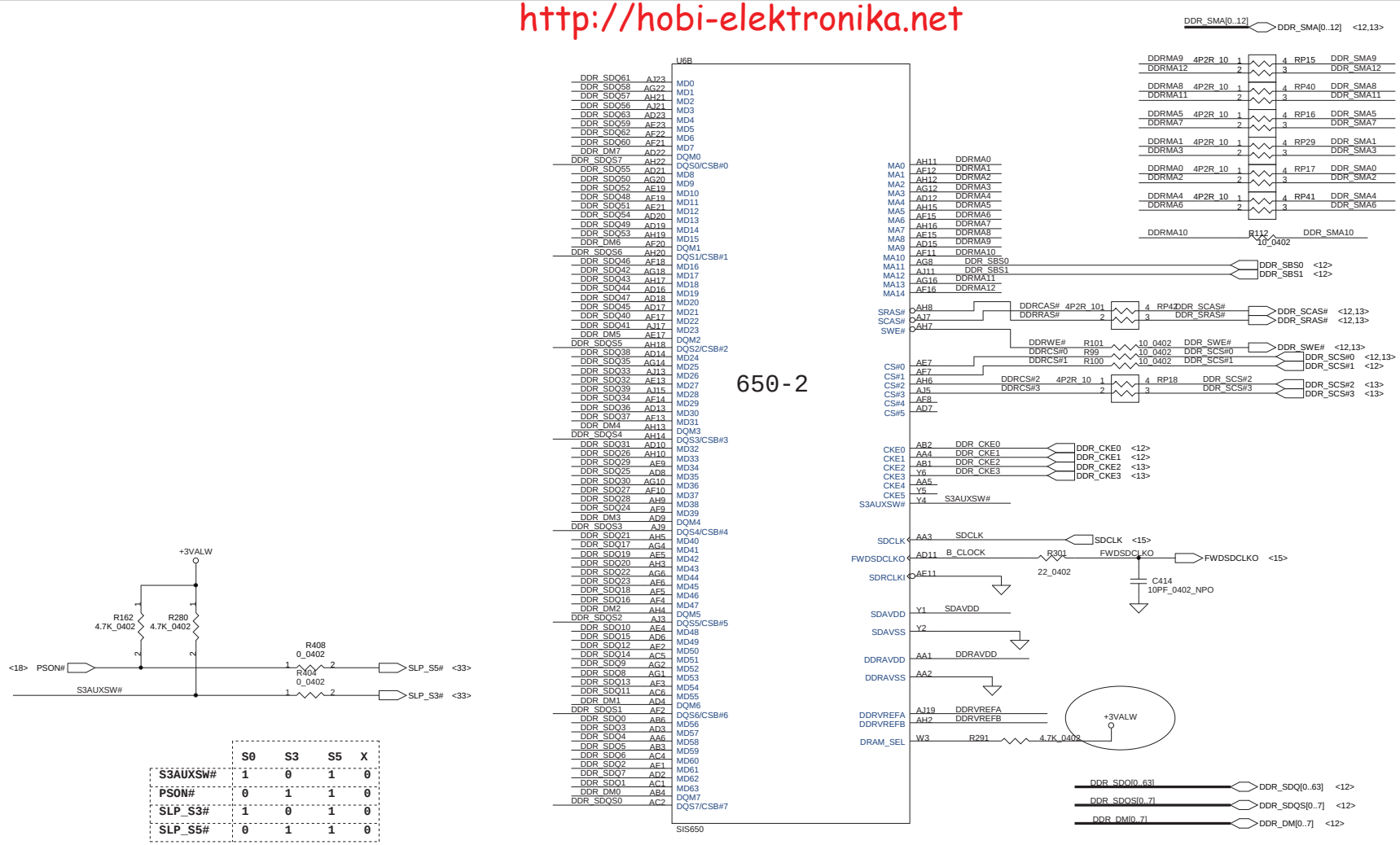
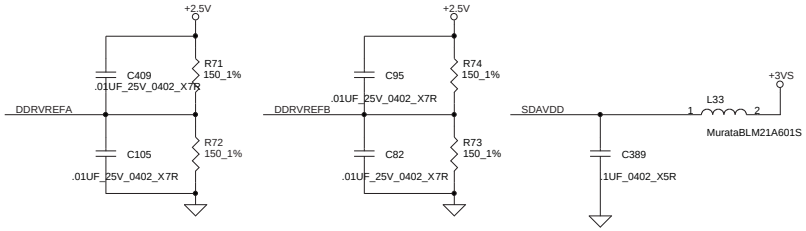
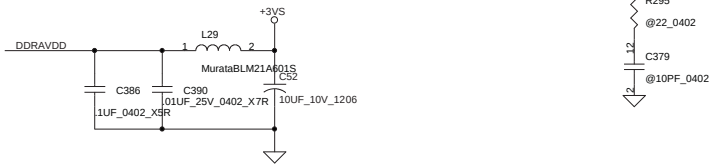


	S0	S3	S5	X
S3AUXSW#	1	0	1	0
PSON#	0	1	1	0
SLP_S3#	1	0	1	0
SLP_S5#	0	1	1	0





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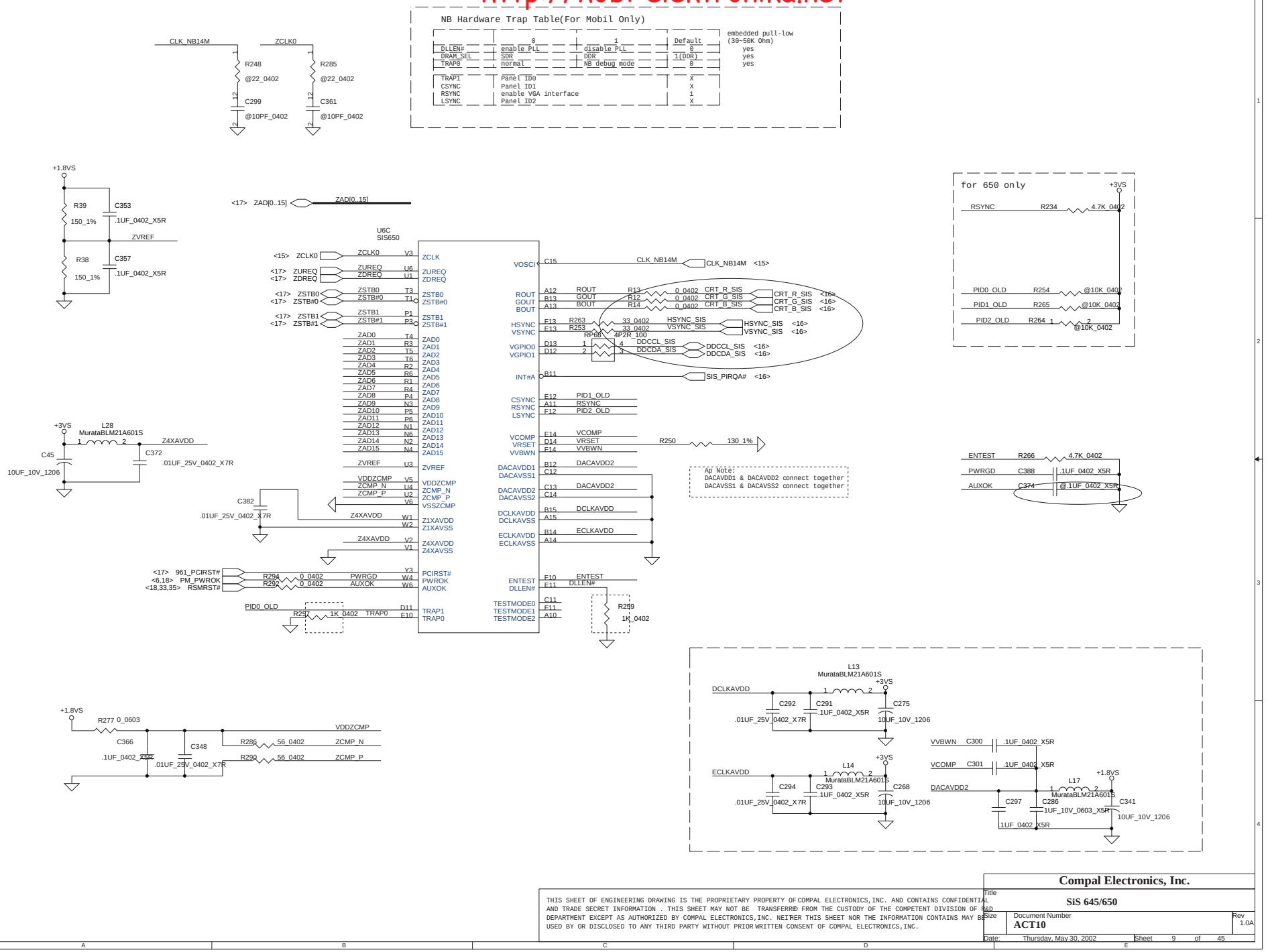

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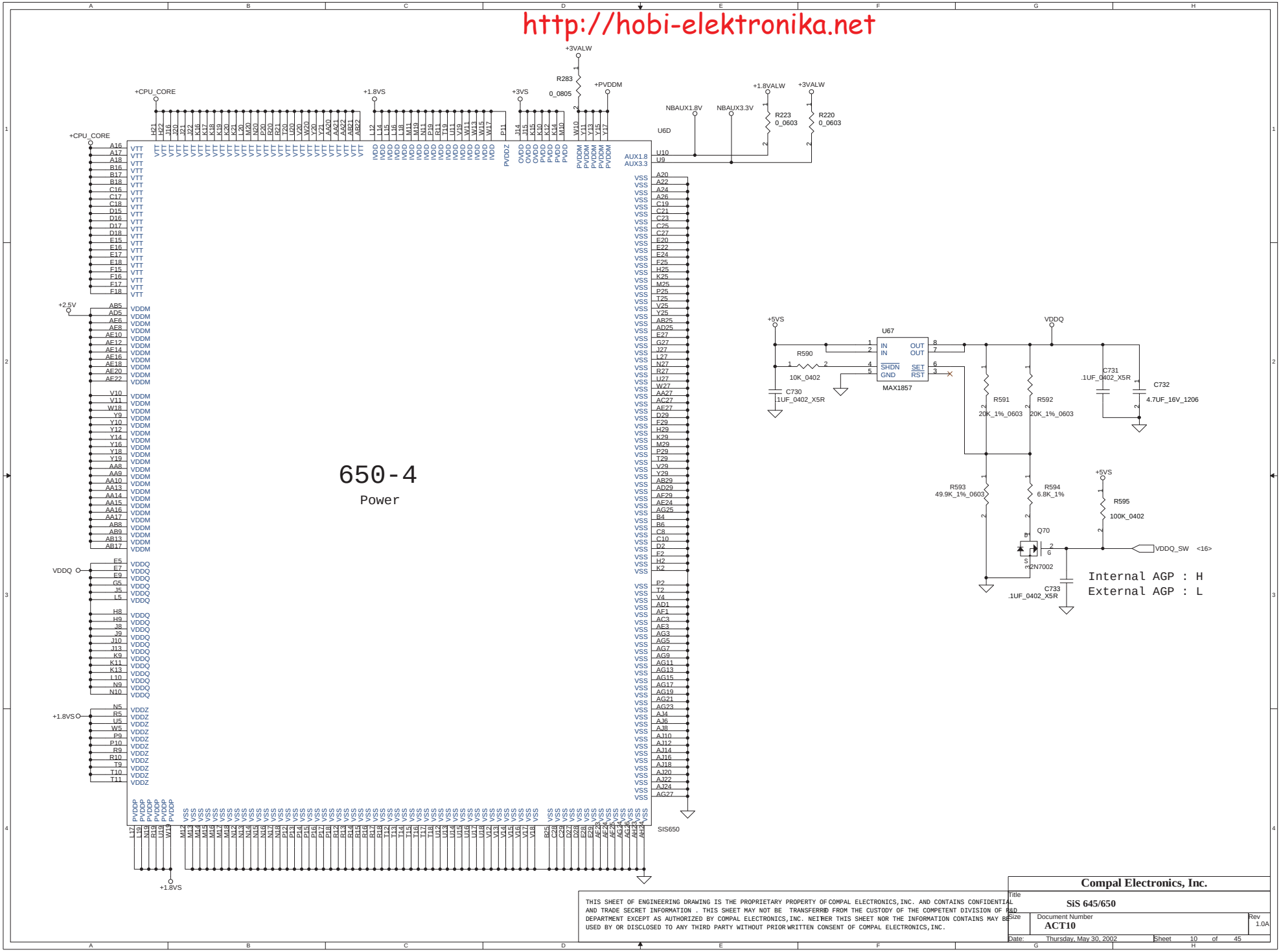

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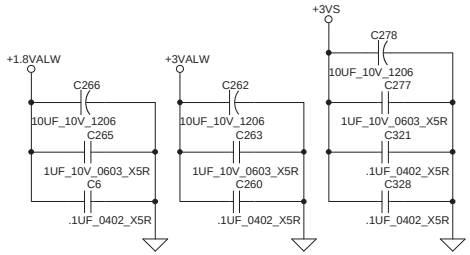
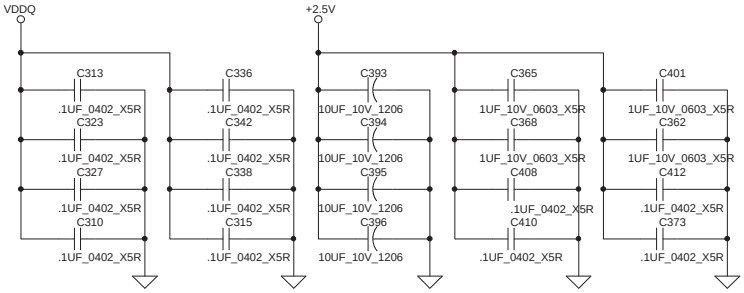
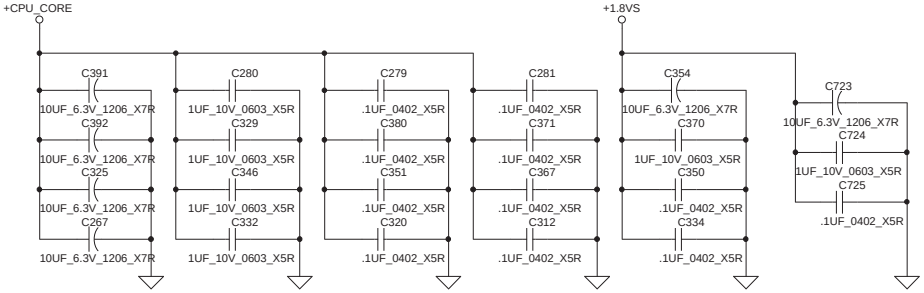
Layout note : Processor system bus

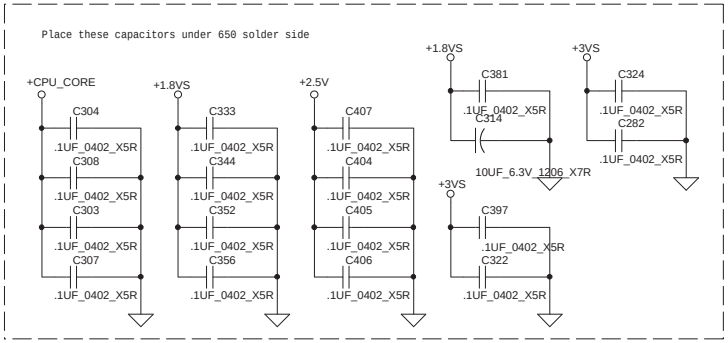
Distribute as close as possible
to Processor Quadrant.(between VTTFSB and VSS pin)

CHECK SiS 650 CAP.
IT NEED HOW MANY ESR









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Compal Electronics, Inc.			
Title	SiS 645/650 Decoupling		
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DDR SWAP NOW, SO DATA NOT CORRECT

Layout note

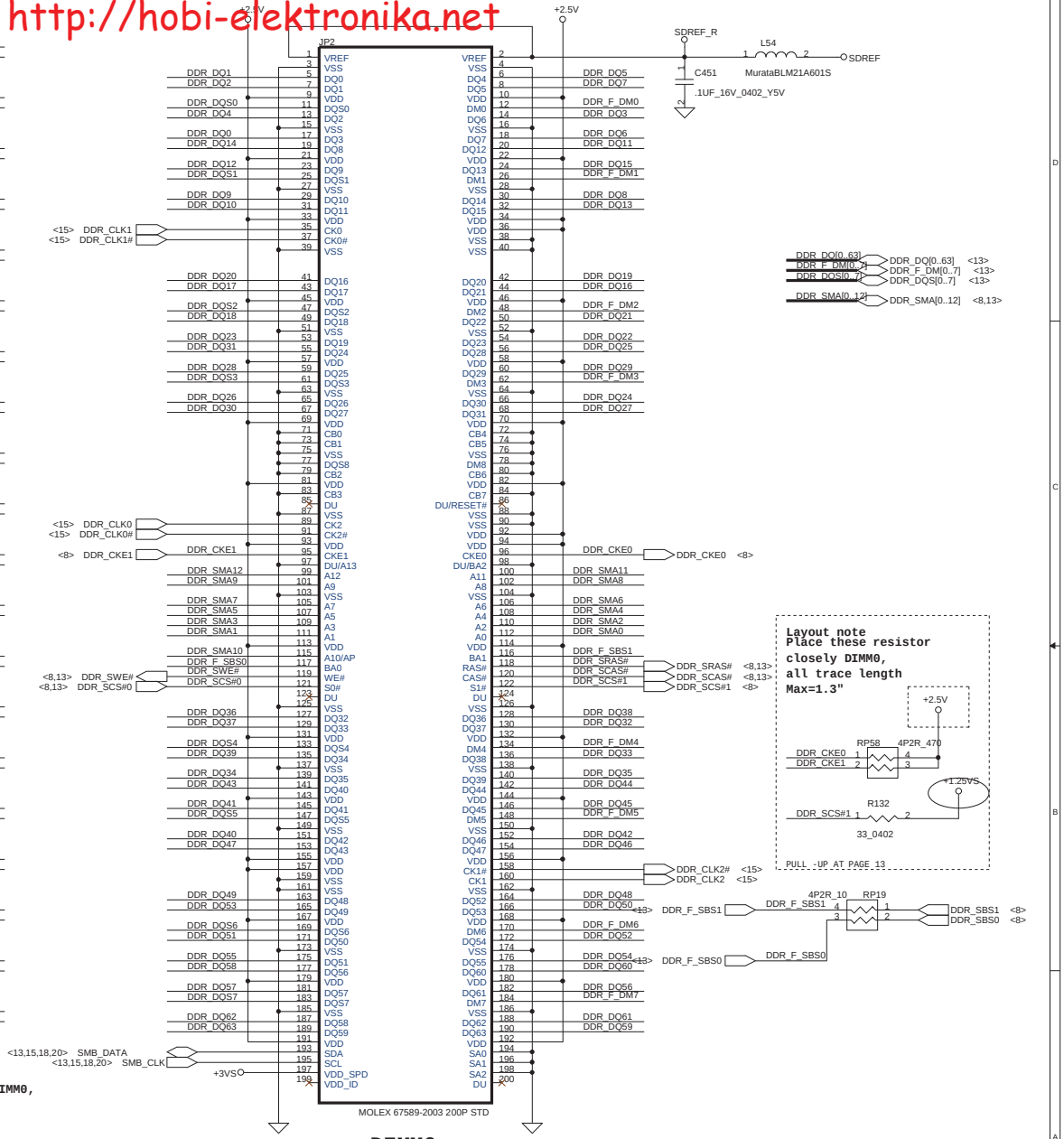
Place these resistor closely DIMM0, all trace length<750mil

Resistor	Pin 1	Pin 2	Pin 3	Pin 4
RP5 4P2R_10	DDR_SDQ1	DDR_SDQ5	DDR_DQ1	DDR_DQ5
RP30 4P2R_10	DDR_SDQ2	DDR_SDQ7	DDR_DQ2	DDR_DQ7
RP6 4P2R_10	DDR_DM0	DDR_SDQS0	DDR_F_DM0	DDR_DQS0
RP31 4P2R_10	DDR_SDQ4	DDR_SDQ3	DDR_DQ4	DDR_DQ3
RP7 4P2R_10	DDR_SDQ0	DDR_SDQ6	DDR_DQ0	DDR_DQ6
RP32 4P2R_10	DDR_SDQ14	DDR_SDQ11	DDR_DQ14	DDR_DQ11
RP8 4P2R_10	DDR_SDQ12	DDR_SDQ15	DDR_DQ12	DDR_DQ15
RP33 4P2R_10	DDR_DM1	DDR_SDQS1	DDR_F_DM1	DDR_DQS1
RP9 4P2R_10	DDR_SDQ9	DDR_SDQ8	DDR_DQ9	DDR_DQ8
RP34 4P2R_10	DDR_SDQ10	DDR_SDQ13	DDR_DQ10	DDR_DQ13
RP10 4P2R_10	DDR_SDQ20	DDR_SDQ19	DDR_DQ20	DDR_DQ19
RP35 4P2R_10	DDR_SDQ17	DDR_SDQ16	DDR_DQ17	DDR_DQ16
RP11 4P2R_10	DDR_SDQS2	DDR_DM2	DDR_DQS2	DDR_F_DM2
RP36 4P2R_10	DDR_SDQ18	DDR_SDQ21	DDR_DQ18	DDR_DQ21
RP12 4P2R_10	DDR_SDQ23	DDR_SDQ22	DDR_DQ23	DDR_DQ22
RP37 4P2R_10	DDR_SDQ31	DDR_SDQ25	DDR_DQ31	DDR_DQ25
RP13 4P2R_10	DDR_SDQ28	DDR_SDQ29	DDR_DQ28	DDR_DQ29
RP38 4P2R_10	DDR_SDQS3	DDR_DM3	DDR_DQS3	DDR_F_DM3
RP14 4P2R_10	DDR_SDQ26	DDR_SDQ24	DDR_DQ26	DDR_DQ24
RP39 4P2R_10	DDR_SDQ30	DDR_SDQ27	DDR_DQ30	DDR_DQ27
RP43 4P2R_10	DDR_SDQ36	DDR_SDQ38	DDR_DQ36	DDR_DQ38
RP20 4P2R_10	DDR_SDQ37	DDR_SDQ32	DDR_DQ37	DDR_DQ32
RP44 4P2R_10	DDR_SDQS4	DDR_DM4	DDR_DQS4	DDR_F_DM4
RP21 4P2R_10	DDR_SDQ39	DDR_SDQ33	DDR_DQ39	DDR_DQ33
RP45 4P2R_10	DDR_SDQ34	DDR_SDQ35	DDR_DQ34	DDR_DQ35
RP22 4P2R_10	DDR_SDQ43	DDR_SDQ44	DDR_DQ43	DDR_DQ44
RP46 4P2R_10	DDR_SDQ41	DDR_SDQ45	DDR_DQ41	DDR_DQ45
RP23 4P2R_10	DDR_DM5	DDR_SDQS5	DDR_F_DM5	DDR_DQS5
RP47 4P2R_10	DDR_SDQ40	DDR_SDQ42	DDR_DQ40	DDR_DQ42
RP24 4P2R_10	DDR_SDQ47	DDR_SDQ46	DDR_DQ47	DDR_DQ46
RP48 4P2R_10	DDR_SDQ49	DDR_SDQ48	DDR_DQ49	DDR_DQ48
RP25 4P2R_10	DDR_SDQ53	DDR_SDQ50	DDR_DQ53	DDR_DQ50
RP49 4P2R_10	DDR_SDQS6	DDR_DM6	DDR_DQS6	DDR_F_DM6
RP26 4P2R_10	DDR_SDQ51	DDR_SDQ52	DDR_DQ51	DDR_DQ52
RP50 4P2R_10	DDR_SDQ55	DDR_SDQ54	DDR_DQ55	DDR_DQ54
RP27 4P2R_10	DDR_SDQ58	DDR_SDQ60	DDR_DQ58	DDR_DQ60
RP51 4P2R_10	DDR_SDQ57	DDR_SDQ56	DDR_DQ57	DDR_DQ56
RP28 4P2R_10	DDR_DM7	DDR_SDQS7	DDR_F_DM7	DDR_DQS7
RP52 4P2R_10	DDR_SDQ62	DDR_SDQ61	DDR_DQ62	DDR_DQ61
RP71 4P2R_10	DDR_SDQ63	DDR_SDQ59	DDR_DQ63	DDR_DQ59

Layout note

Place these resistor closely DIMM0, all trace length<=750mil

<8> DDR_SDQ[0..63] — DDR_SDQ[0..63]
<8> DDR_DM[0..7] — DDR_DM[0..7]
<8> DDR_SDQS[0..7] — DDR_SDQS[0..7]



DIMM0

top side

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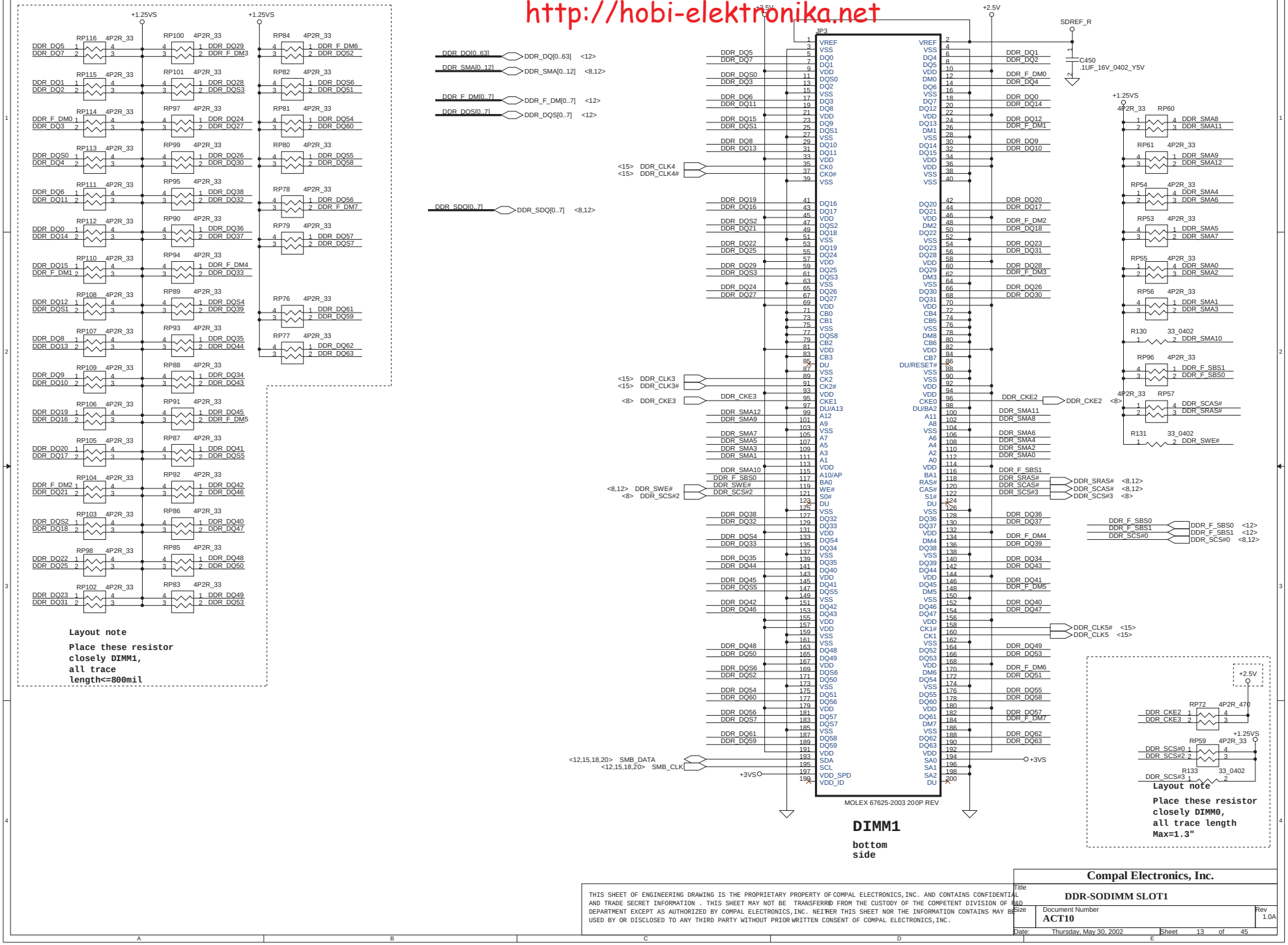

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Compal Electronics, Inc.	
Title	DDR-SODIMM SLOT1
Size	Document Number ACT10 — Rev 1.0A
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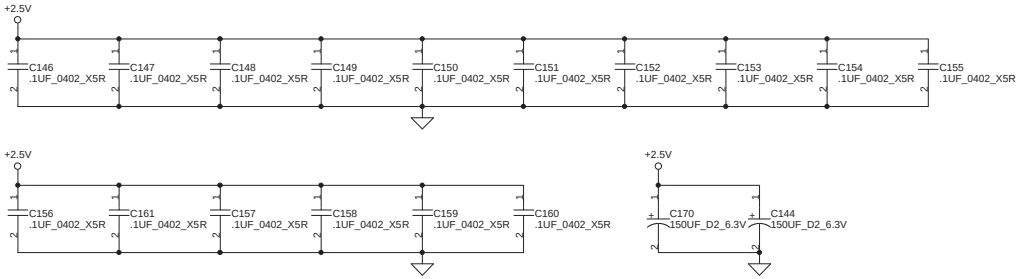
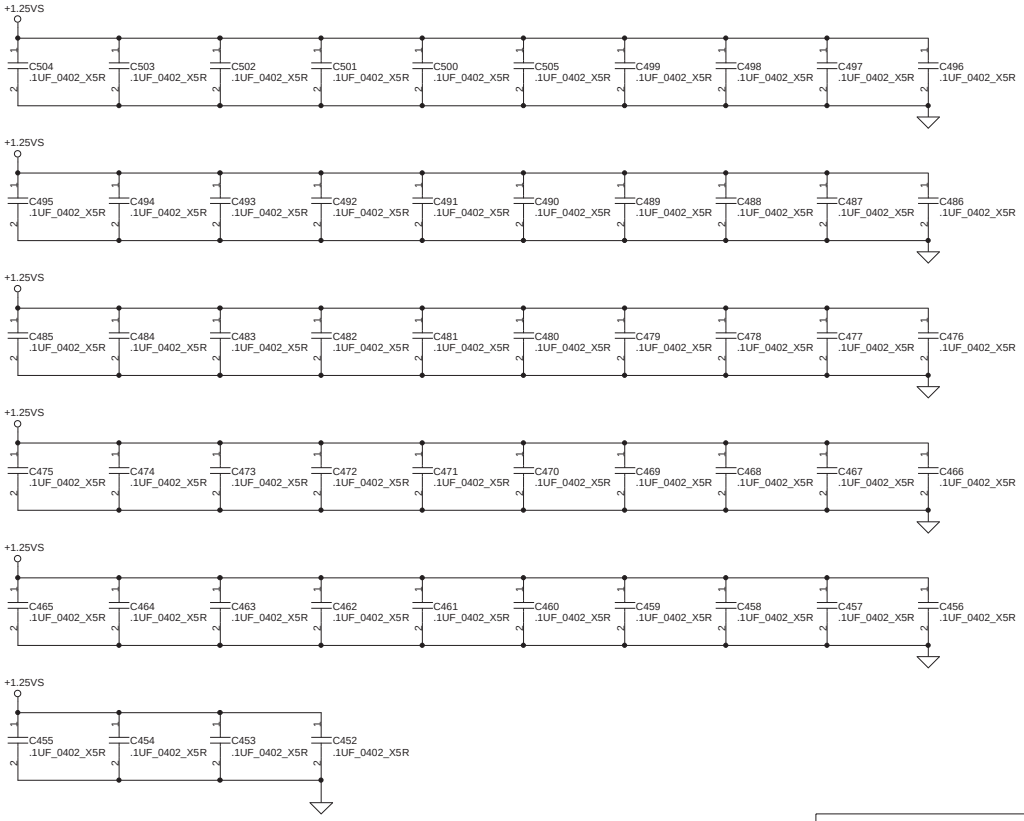
Layout note :

Distribute as close as possible to DDR-SODIMM.



Layout note :

Place one cap close to every 2 pull up resistors termination to +1.25V



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Compal Electronics, Inc.

Title	DDR SODIMM Decoupling	
Size	Document Number ACT10	Rev 1.0A
Date: Thursday, May 30, 2002	Sheet 14 of 45	

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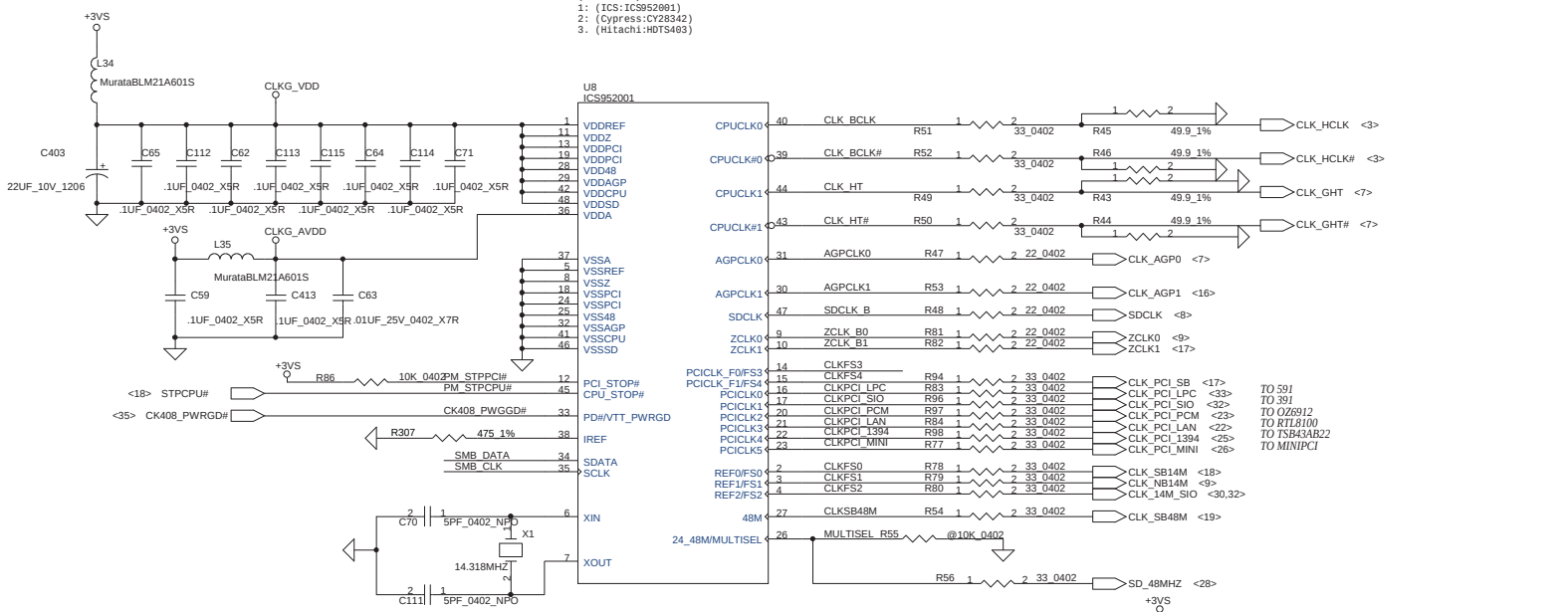
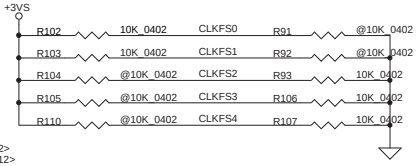
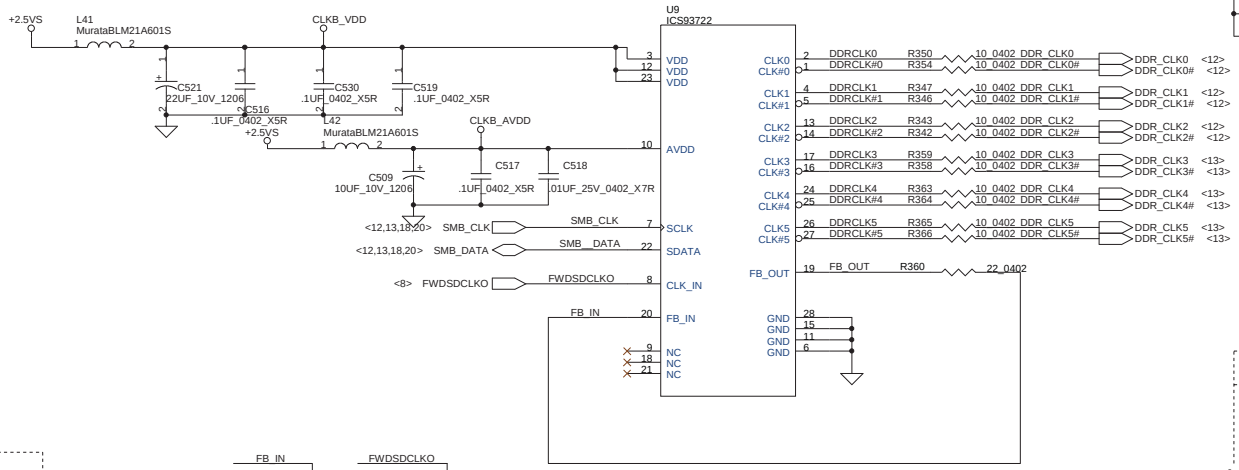
Main Clock Generator

(3 OPTIONS)
1: (ICS:ICS952001)
2: (Cypress:CY28342)
3. (Hitachi:HDTS403)

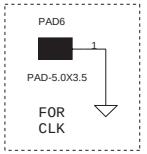


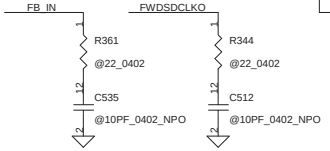
ICS suggestion 14.318MHz > 36pF, C273, C274 4pF





FS4	FS3	FS2	FS1	FS0	CPU	DDR	ZCLK	AGP	PCI
1	1	0	0	0	100.0	133.0	80.0	66.7	33.3
1	1	0	0	1	100.0	100.0	80.0	66.7	33.3
0	0	1	1	1	100.0	133.3	80.0	66.7	33.3
* 0	0	0	1	1	100.0	133.3	66.7	66.7	33.3





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Compal Electronics, Inc.	
Title	Clock Generator
Size	Document Number: ACT10 — Rev 1.0A
Date: Thursday, May 30, 2002	Sheet 15 of 45

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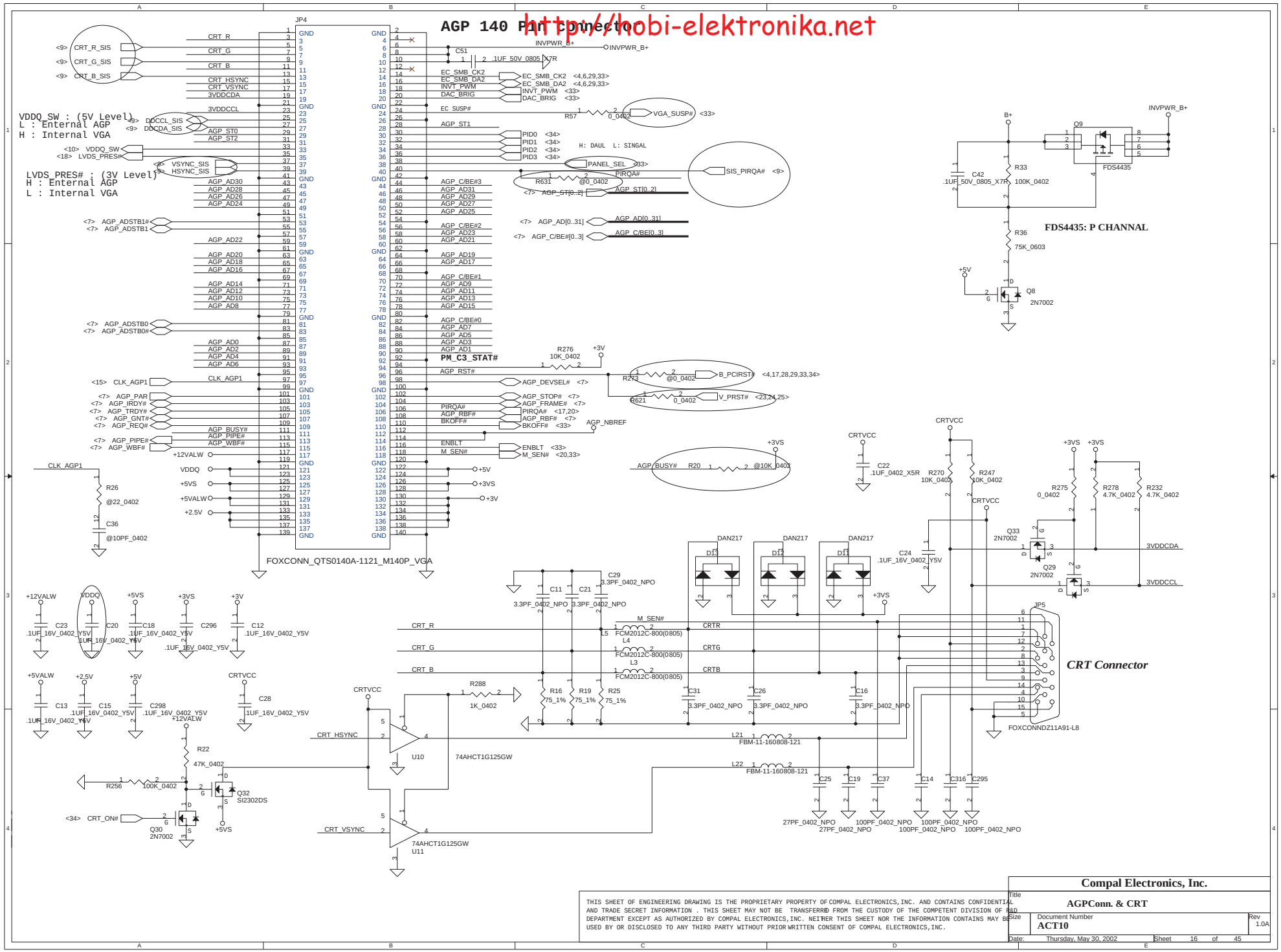
AGP 140 Pin Connector



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Compal Electronics, Inc.	
Title	AGPConn. & CRT
Size	Document Number: ACT10 — Rev 1.0A
Date: Thursday, May 30, 2002	Sheet 16 of 45

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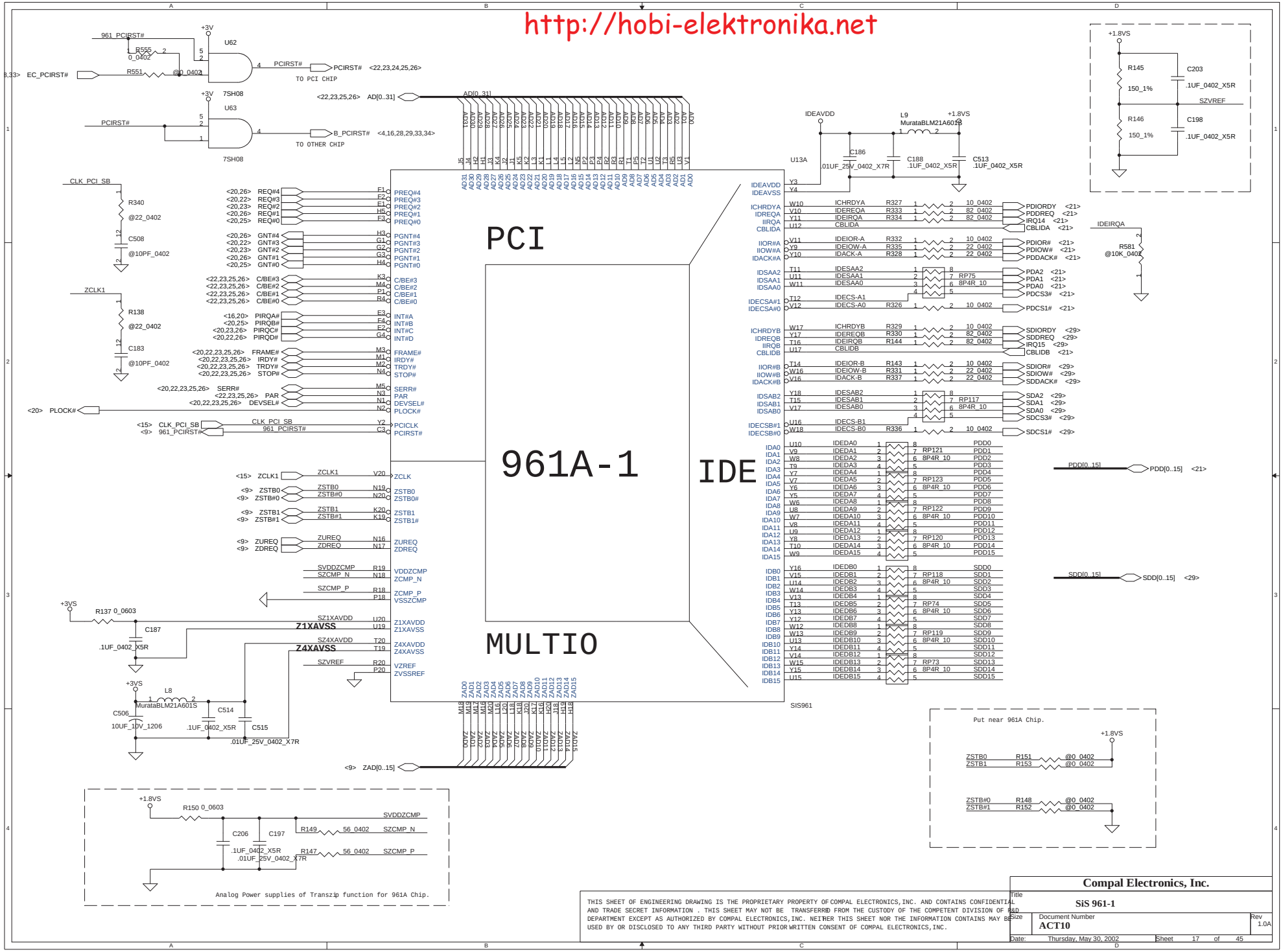

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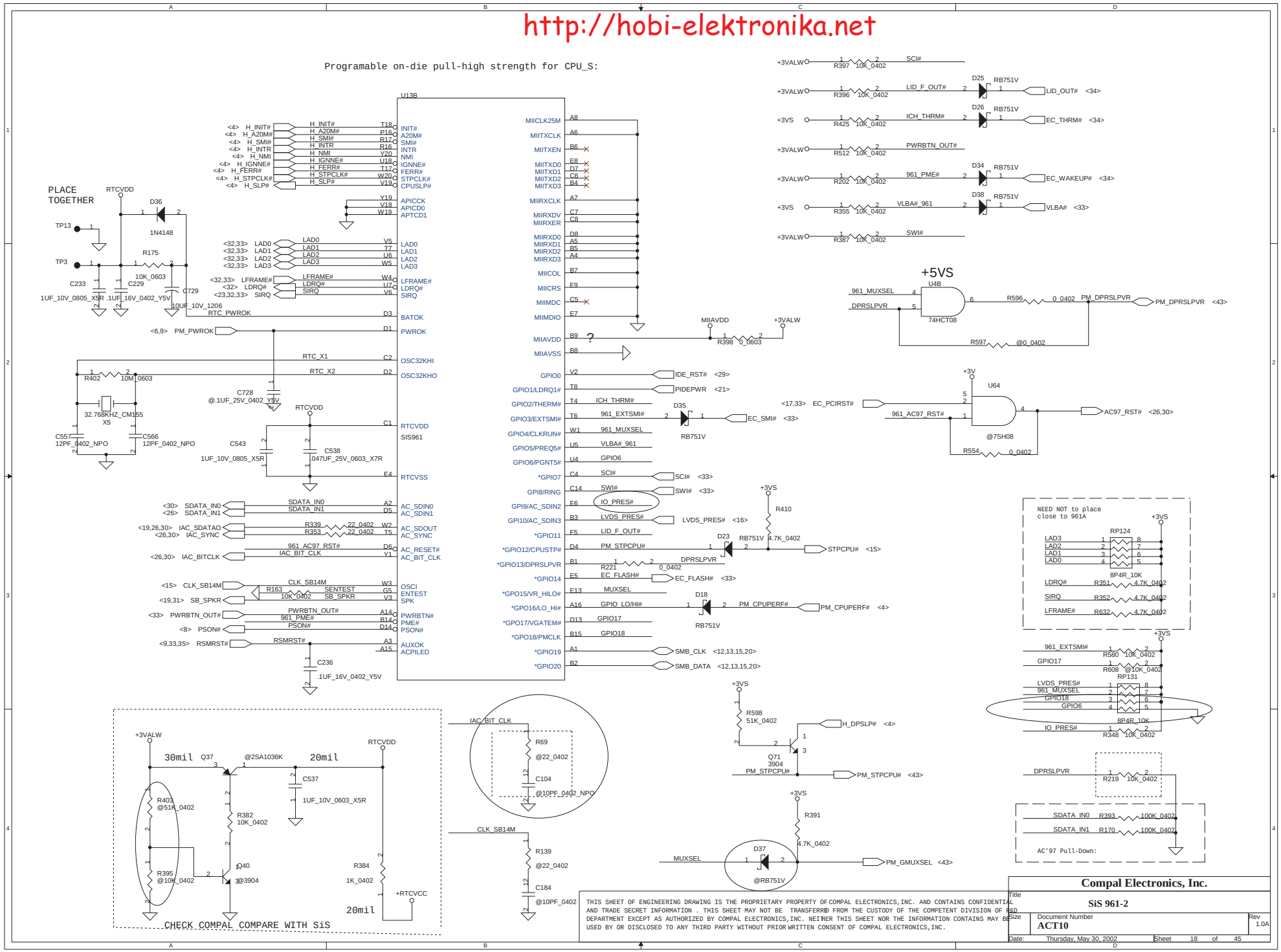

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Compal Electronics, Inc.

Title: SiS 961-2		
Size	Document Number: ACT10	Rev: 1.0A
Date: Thursday, May 30, 2002	Sheet 18 of 45	

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FOR 961 USB PIN DEFINITION

Control 0 : port 0 UV0+ B18 UV0- C18 OC0# G20
Control 0 : port 1 UV1+ E14 UV1- D15 OC1# J16
Control 0 : port 2 UV2+ E16 UV2- E15 OC2# H17
HW TRIP PULL LOW 1K SOUTH BIRDGE DEBUG MODE

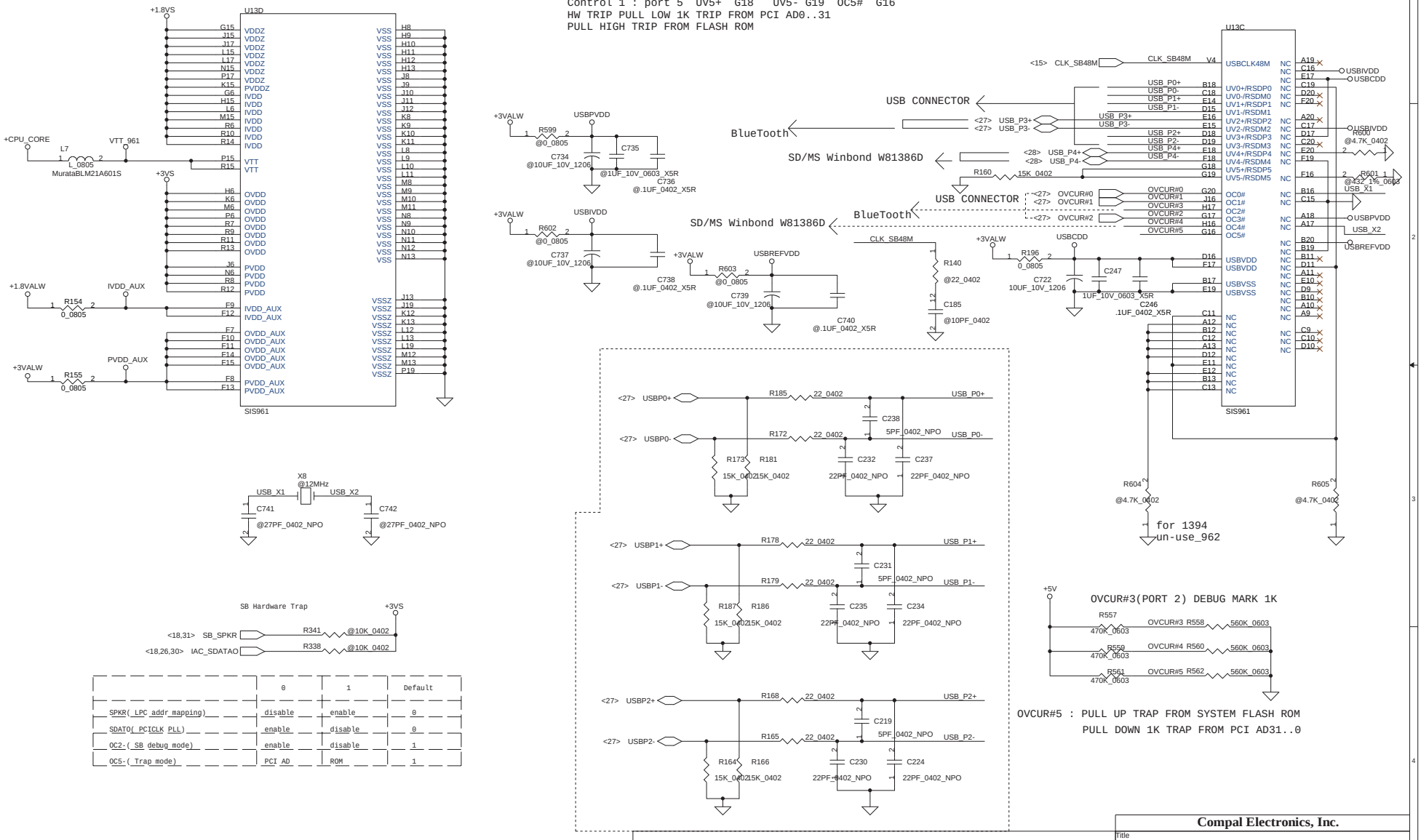
Control 1 : port 3 UV3+ D18 UV3- D19 OC3# G17
Control 1 : port 4 UV4+ E18 UV4- F18 OC4# H16
Control 1 : port 5 UV5+ G18 UV5- G19 OC5# G16
HW TRIP PULL LOW 1K TRIP FROM PCI AD0..31
PULL HIGH TRIP FROM FLASH ROM

FOR 962 USB PIN DEFINITION

Control 0 : port 0 UV0+ B18 UV0- C18 OC0# G20
Control 0 : port 3 UV3+ E18 UV3- F18 OC3# H16

Control 1 : port 1 UV1+ D18 UV1- D19 OC1# G17
Control 1 : port 4 UV4+ E16 UV4- E15 OC4# H17

Control 2 : port 2 UV2+ E14 UV2- D15 OC2# J16
Control 2 : port 5 UV5+ G18 UV5- G19 OC5# G16



OVCUR#5 : PULL UP TRAP FROM SYSTEM FLASH ROM
PULL DOWN 1K TRAP FROM PCI AD31..0

	0	1	Default
SPKR(LPC addr mapping)	disable	enable	0
SDATO(PCICLK PLL)	enable	disable	0
OC2-(SB debug mode)	enable	disable	1
OC5-(Trap mode)	PCI AD	ROM	1

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Compal Electronics, Inc.

Title: SiS 961(3) USB

Size: Document Number: ACT10 Rev: 1.0A

Date: Thursday, May 30, 2002 Sheet 19 of 45

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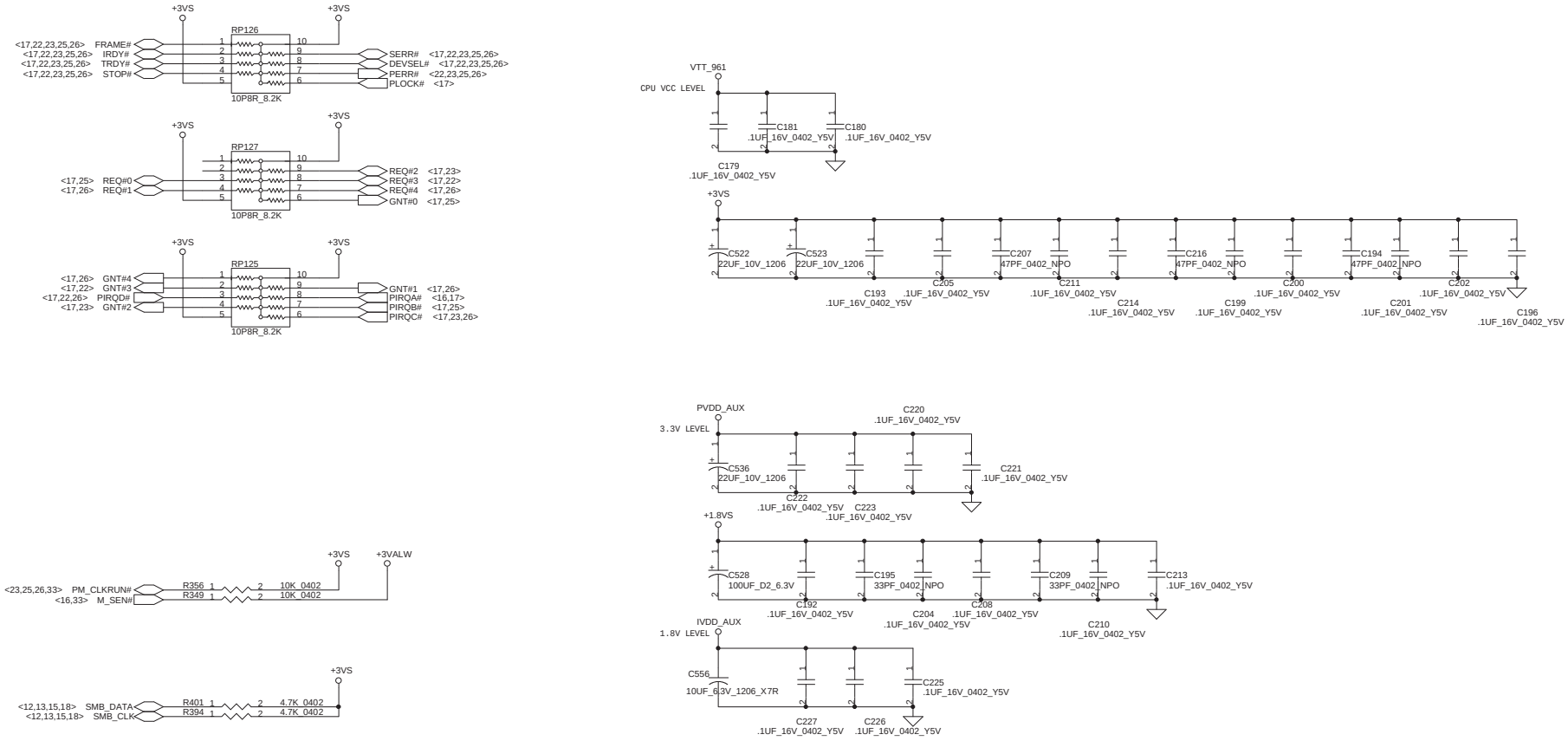

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Compal Electronics, Inc.	
Title	SiS961 Decoupling & Pull-Up
Size	Document Number: ACT10 — Rev 1.0A
Date: Thursday, May 30, 2002	Sheet 20 of 45

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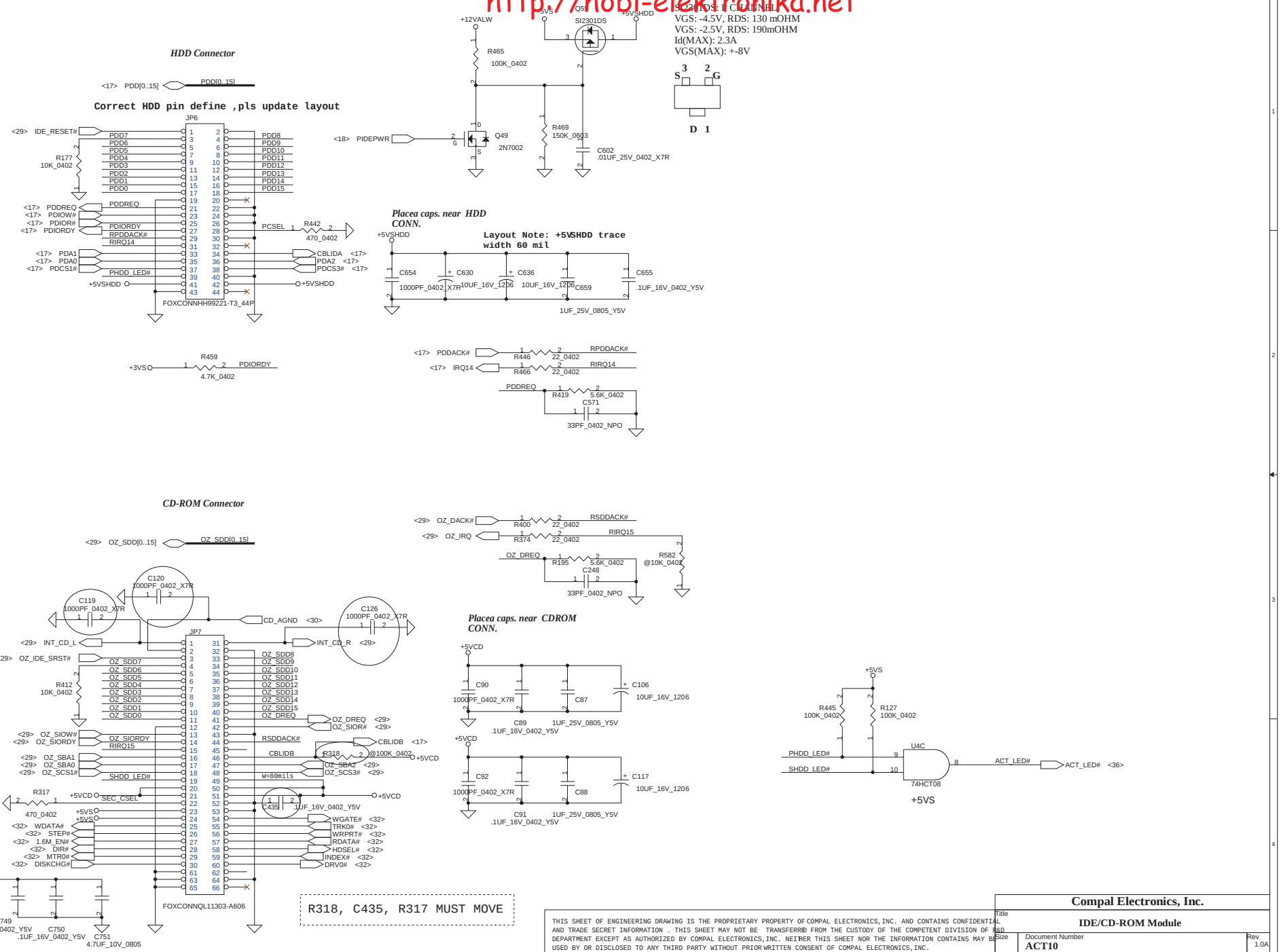

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Compal Electronics, Inc.	
Title	IDE/CD-ROM Module
Size	
Document Number	ACT10
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Date: Thursday, May 30, 2002	Sheet 21 of 45

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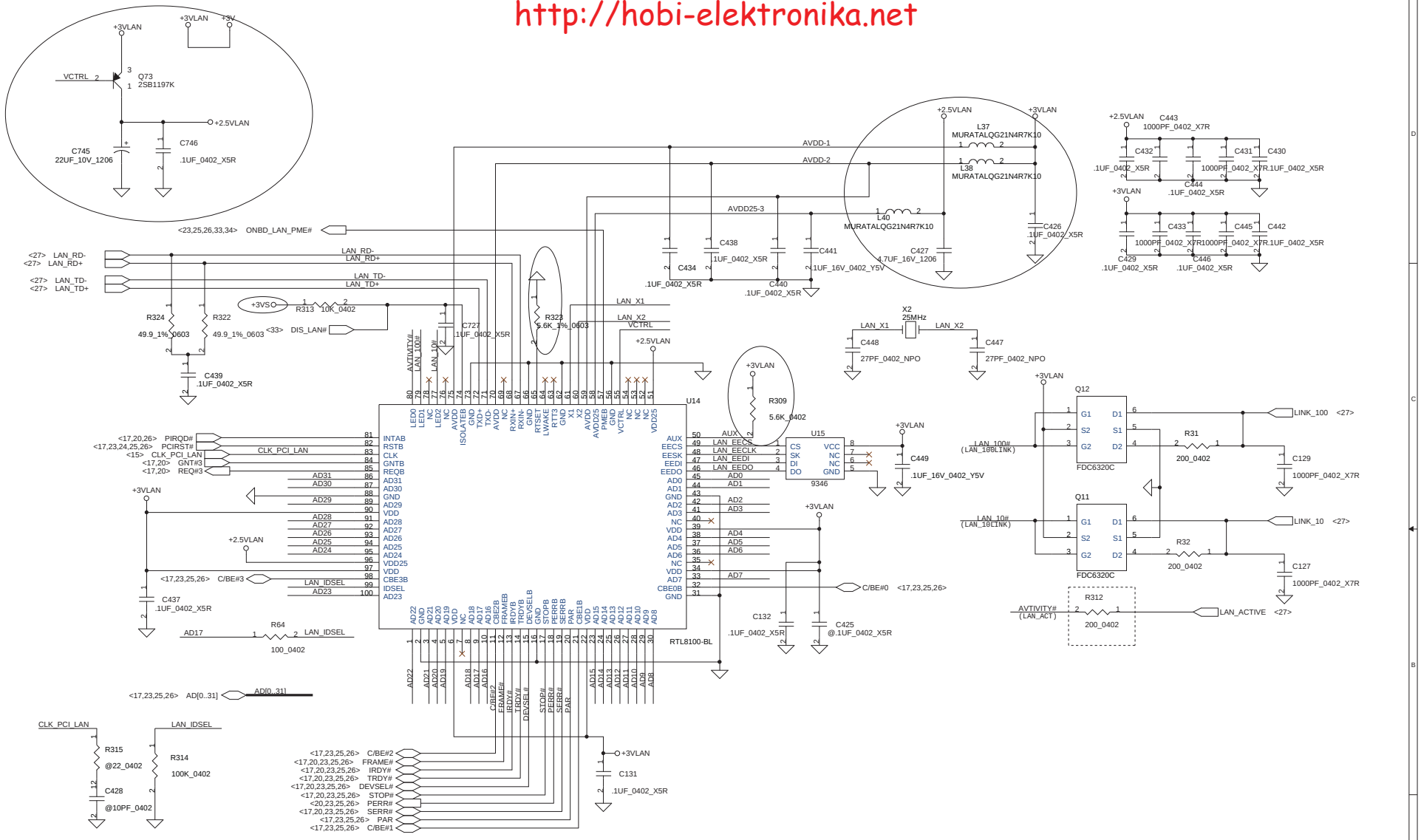

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Compal Electronics, Inc.

Title	Realtek RTL8100BL	
Size	Document Number ACT10	Rev 1.0A
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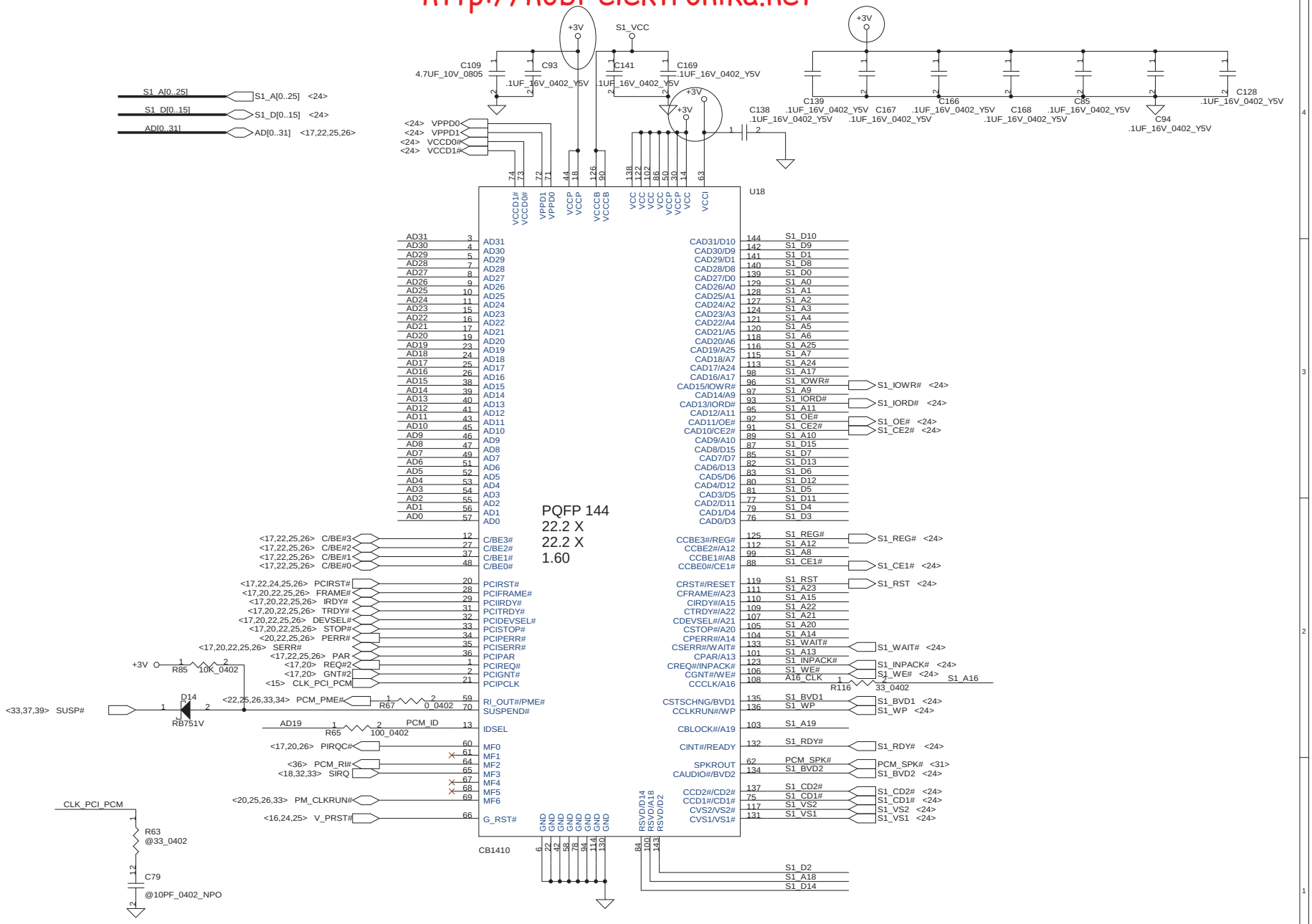

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Compal Electronics, Ltd.

Title	PCMCIA controller ENE CB1410
Size	Document Number: ACT10 — Rev 1.0A
Date:	Thursday, May 30, 2002
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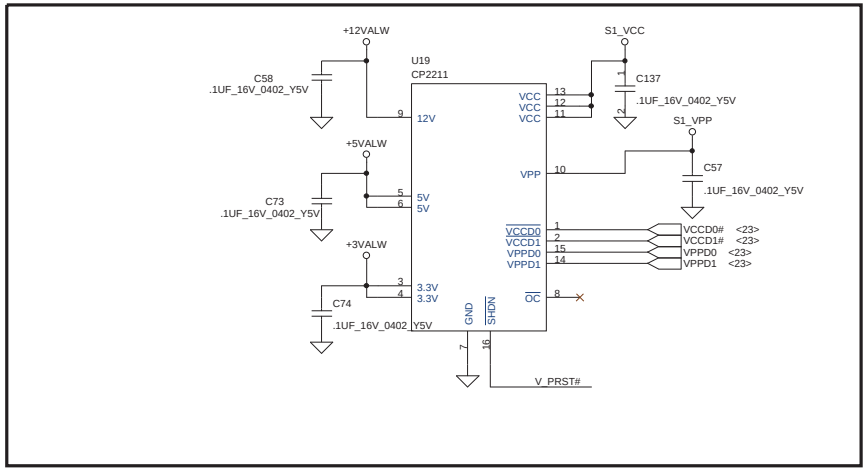
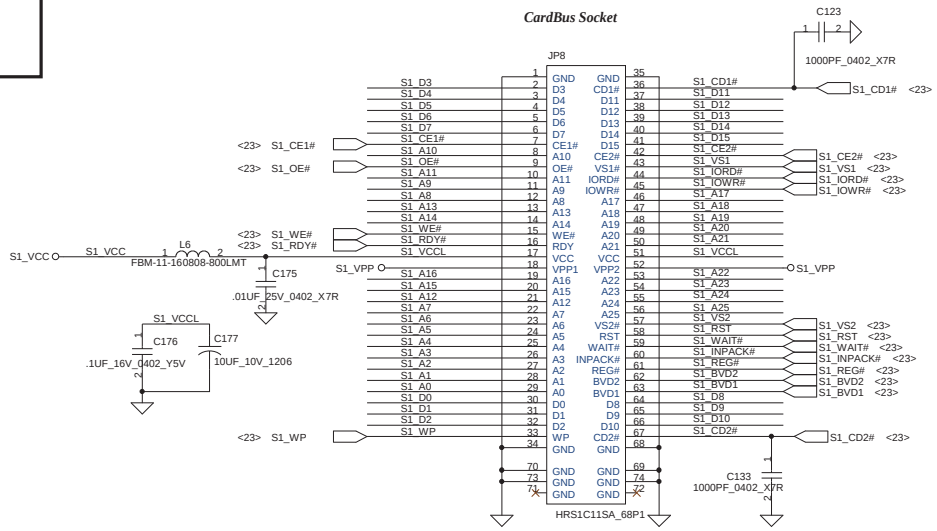
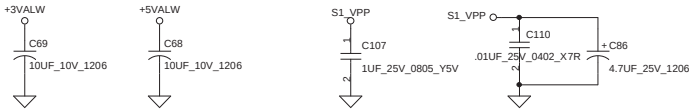
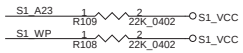
PCMCIA Power Controller

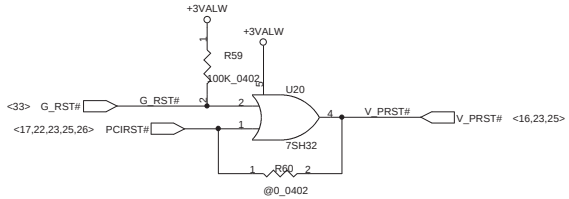


CardBus Socket









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Compal Electronics, Inc.	
Title	CardBus Socket
Size	Document Number: ACT10 — Rev 1.0A
Date: Thursday, May 30, 2002	Sheet 24 of 45

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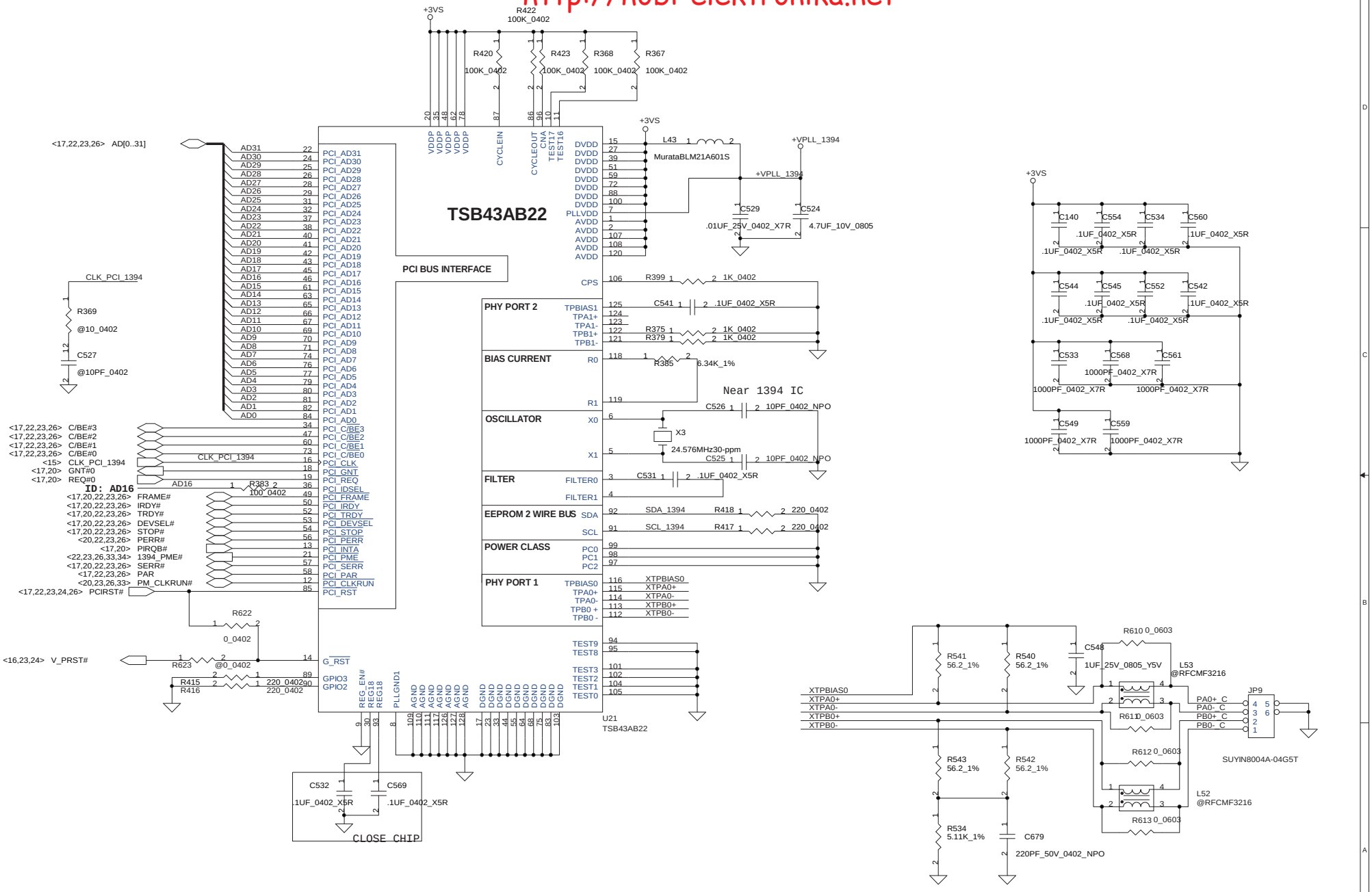

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Compal Electronics, Ltd.

Title: IEEE-1394 Controller (TSB43AB22)

Size: Custom | Document Number: ACT10 | Rev: 1.0A

Date: Thursday, May 30, 2002 | Sheet 25 of 45

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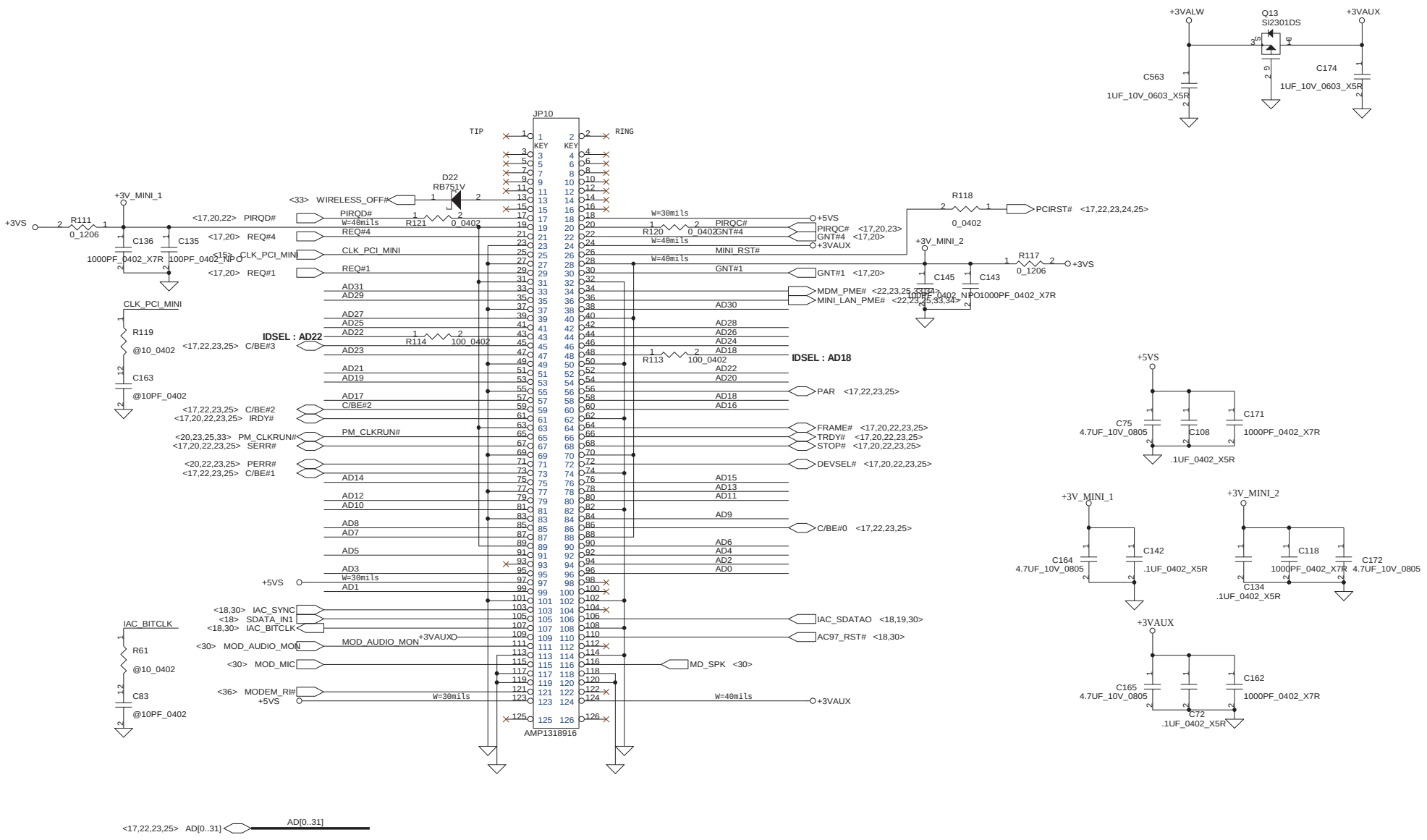

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Compal Electronics, Ltd.

Title	Mini PCI Slot		
Size Custom	Document Number ACT10		Rev 1.0A
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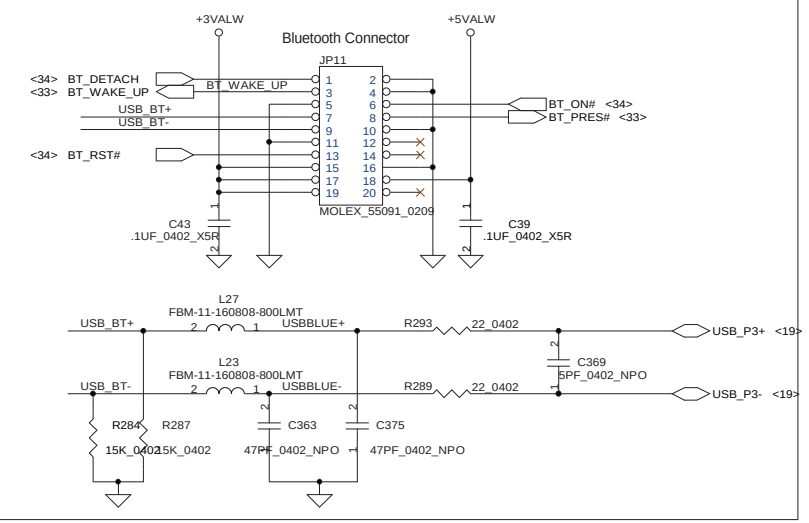
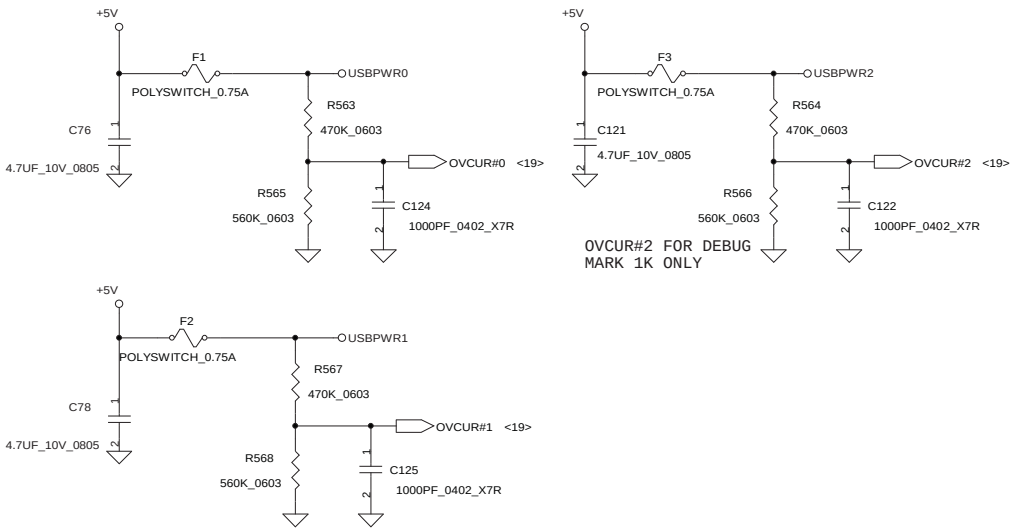
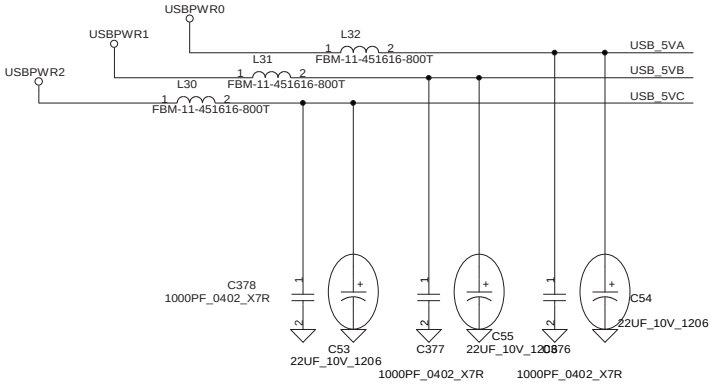
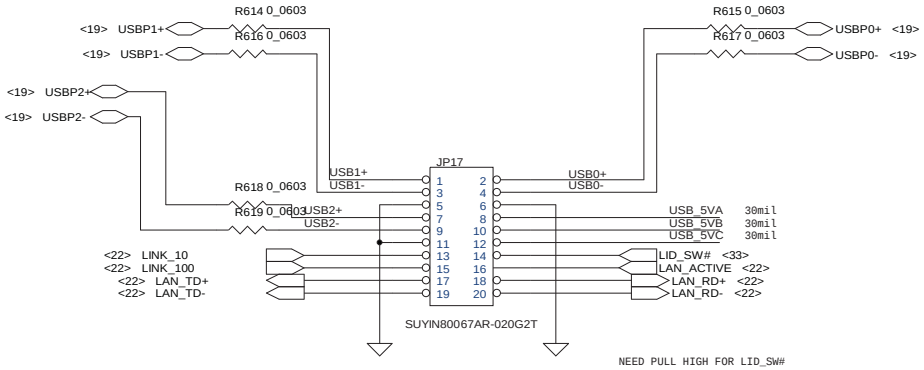
BlueTooth Interface









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Compal Electronics, Ltd.			
Title: USB & BlueTooth Connector			
Size: Custom	Document Number: ACT10		Rev: 1.0A
Date: Thursday, May 30, 2002	Sheet 27 of 45		

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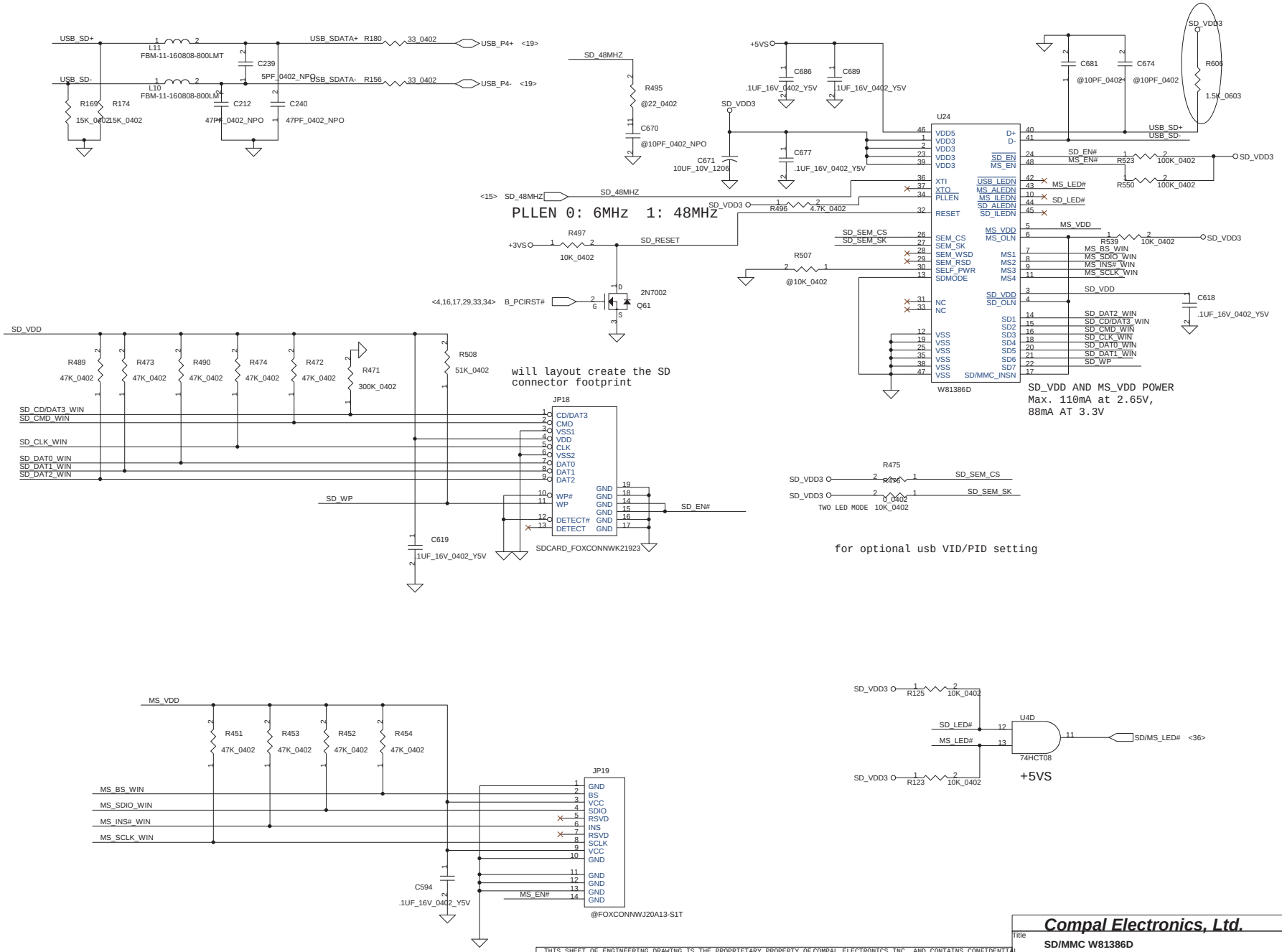

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Compal Electronics, Ltd.

Title	SD/MMC W81386D	
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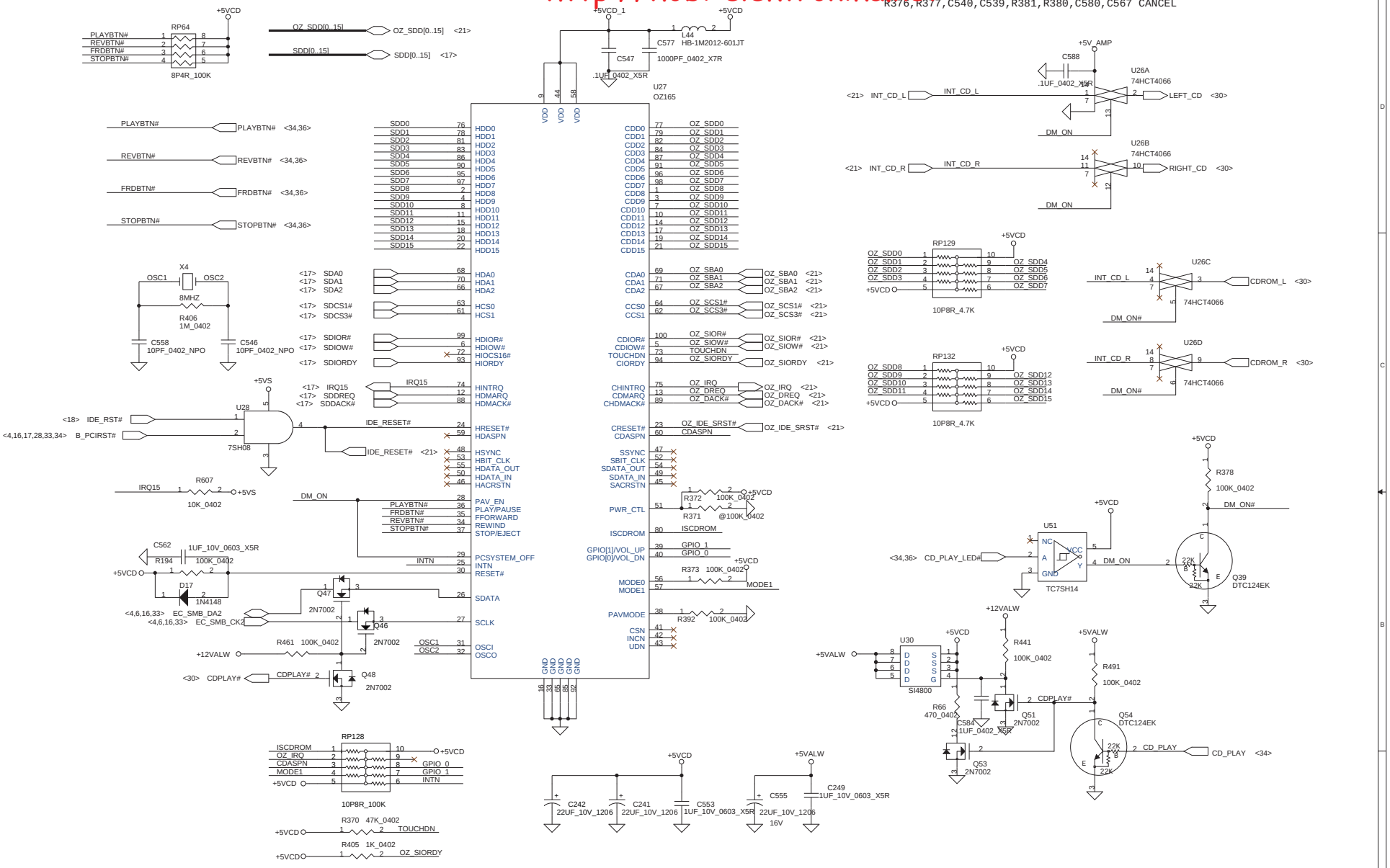
R376,R377,C540,C539,R381,R380,C580,C567 CANCEL



Compal Electronics, Ltd.		
Title: Direct CD Play OZ165		
Size: Custom	Document Number: ACT10	Rev: 1.0A
Date: Thursday, May 30, 2002	Sheet 29 of 45	

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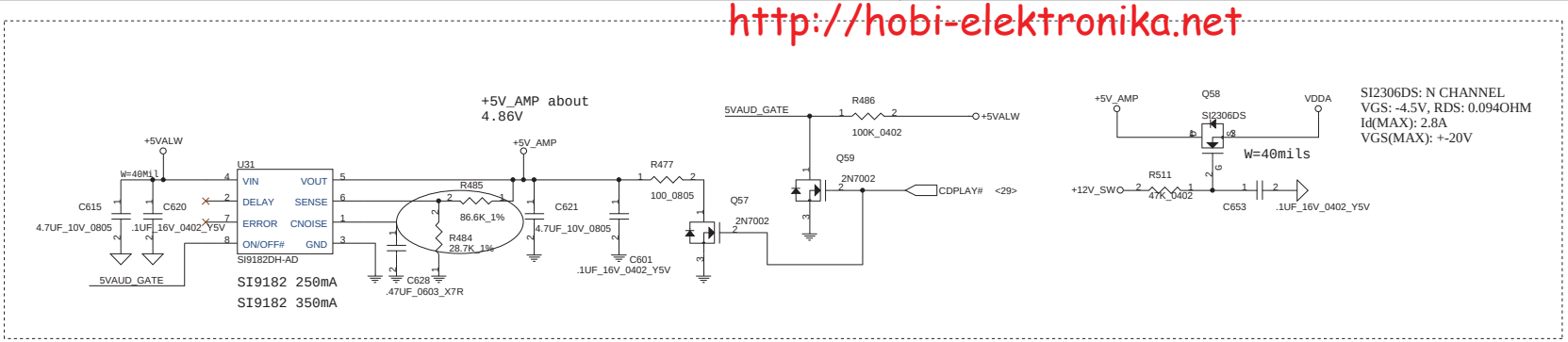

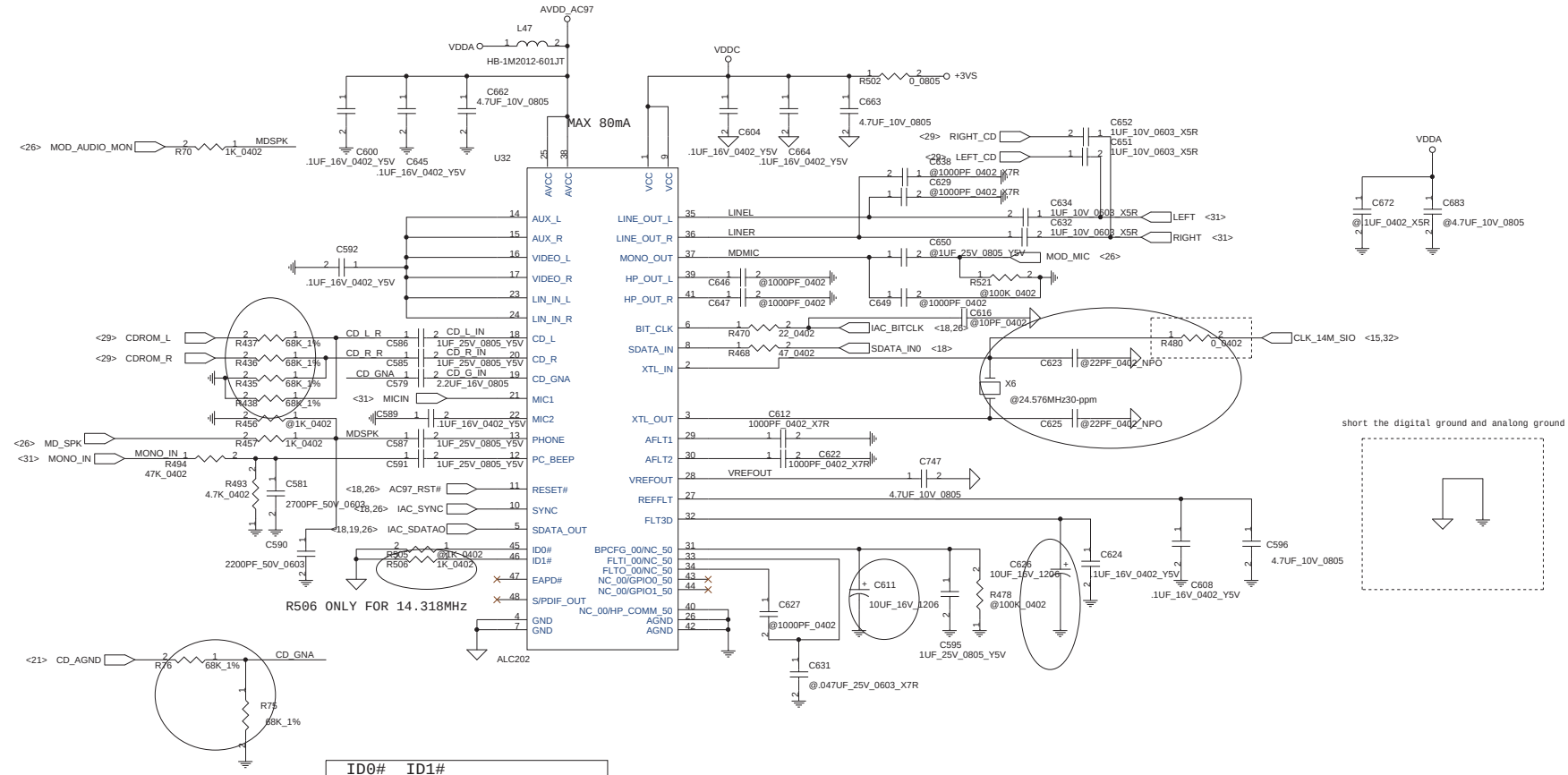

ID0#	ID1#	
1	1	14.318 OPEN
1	0	27MHZ
0	1	48MHZ
0	0	24.576MHZ

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Compal Electronics, Inc.

Title: **AC97 CODEC**

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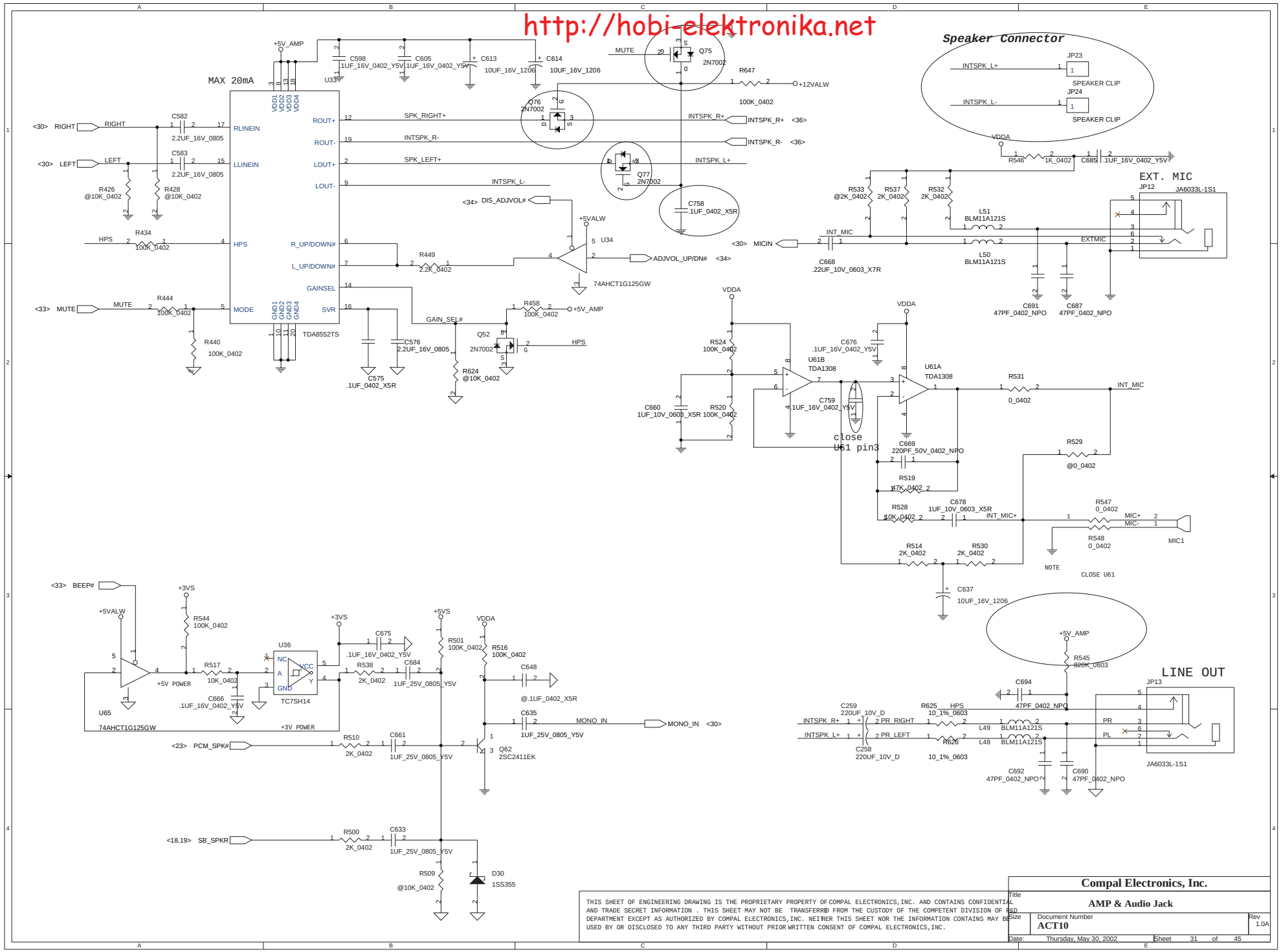

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Compal Electronics, Inc.	
Title	AMP & Audio Jack
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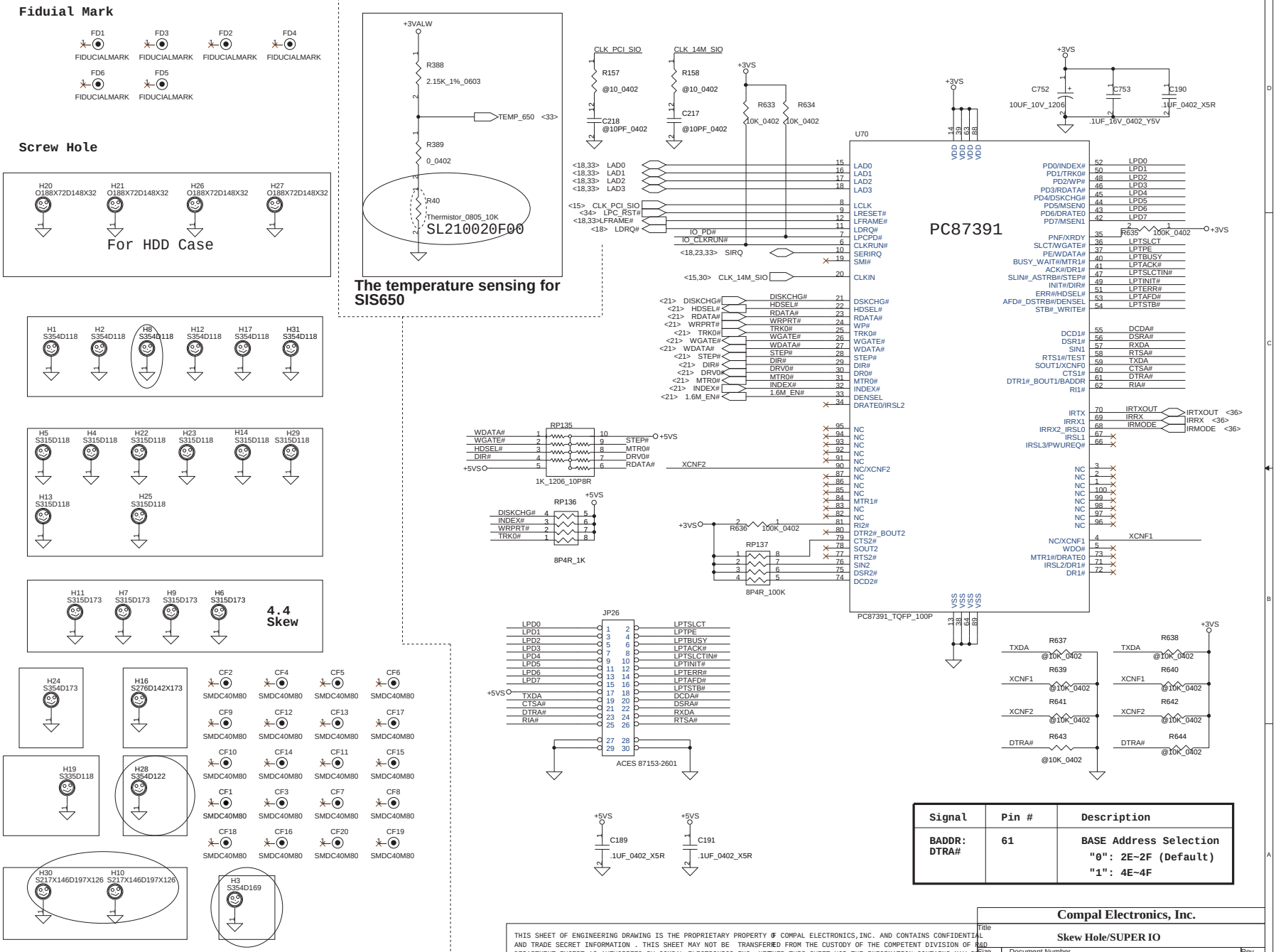

Signal	Pin #	Description
BADDR: DTRA#	61	BASE Address Selection "0": 2E~2F (Default) "1": 4E~4F

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Compal Electronics, Inc.

Title: Skew Hole/SUPER IO

Size: | Document Number: ACT10 | Rev: 1.0A

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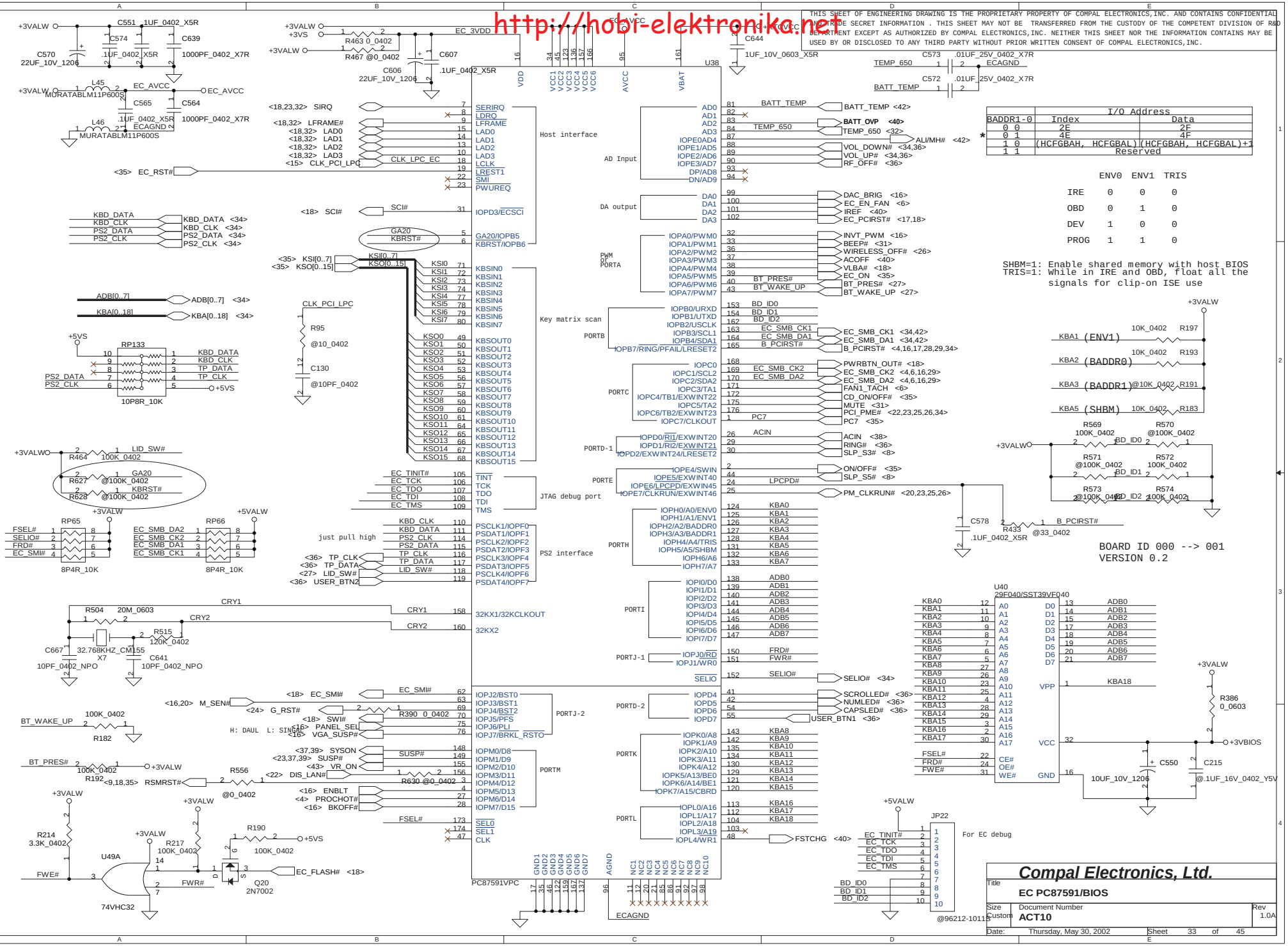

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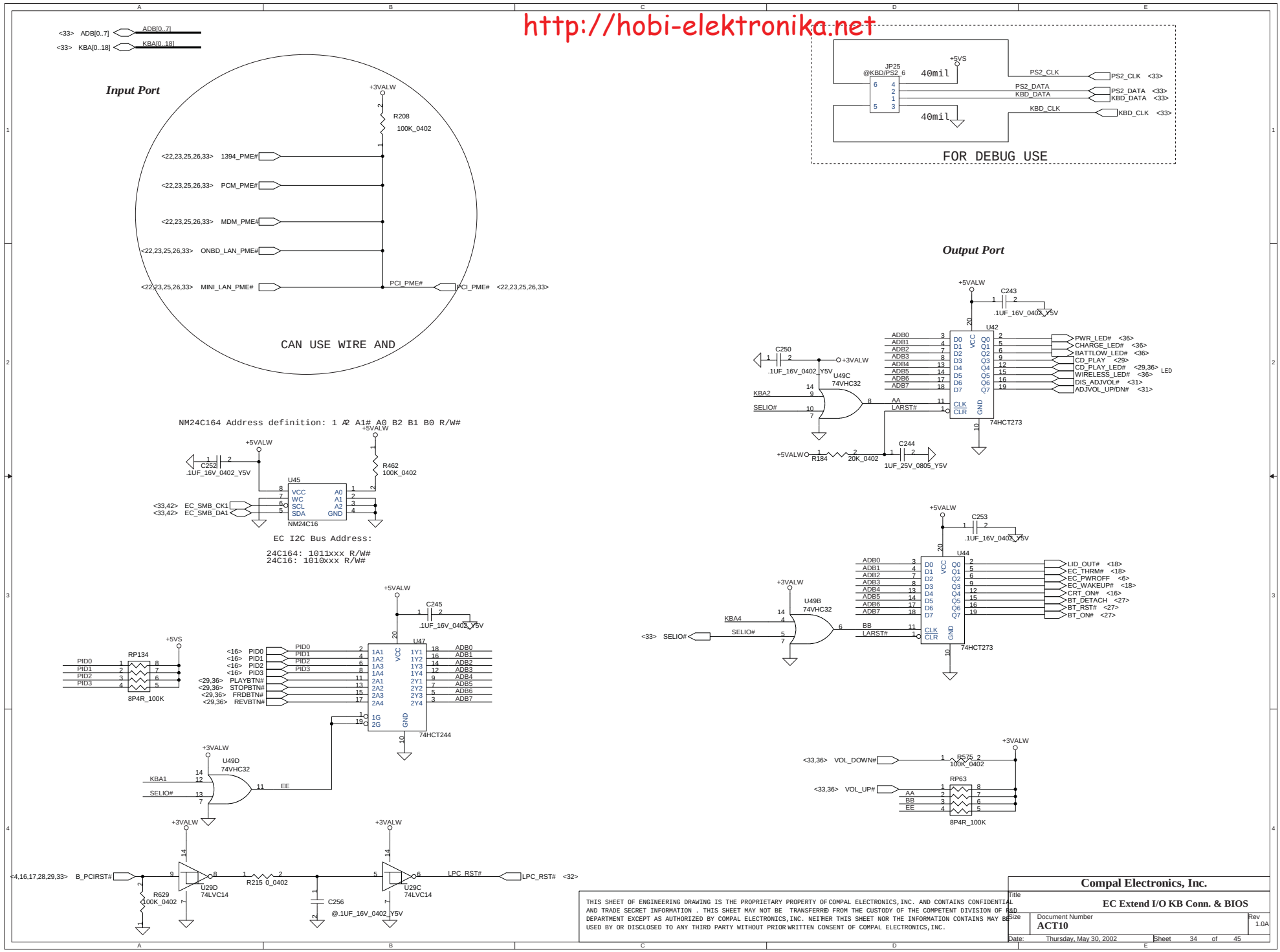

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Compal Electronics, Inc.	
Title	EC Extend I/O KB Conn. & BIOS
Size	
Document Number	ACT10
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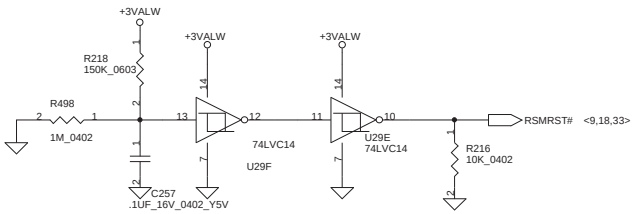
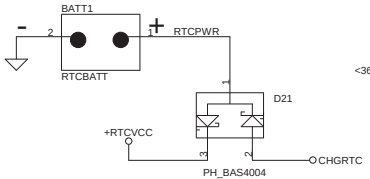
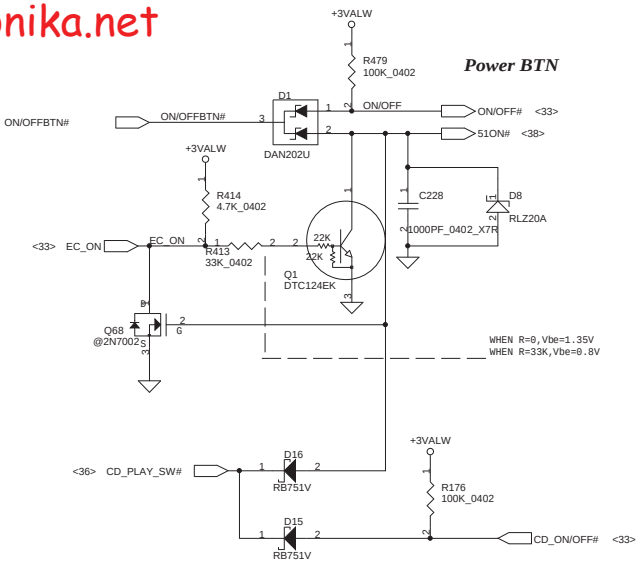
Power ON Circuit

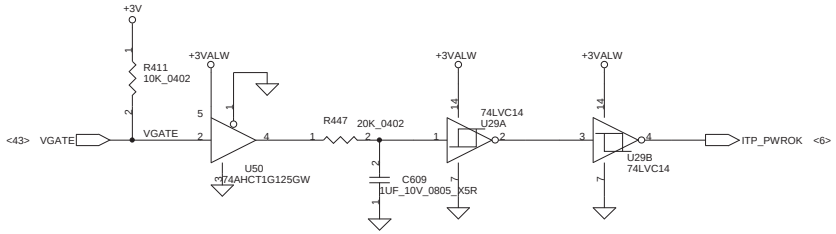


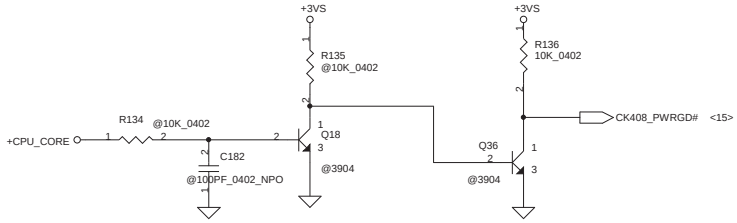
RTC Battery

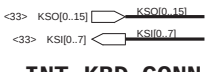


Power BTN

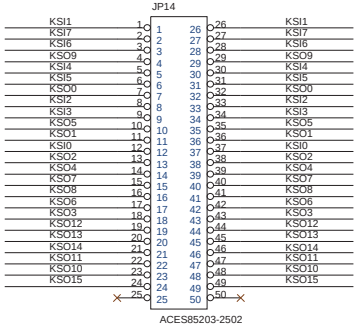


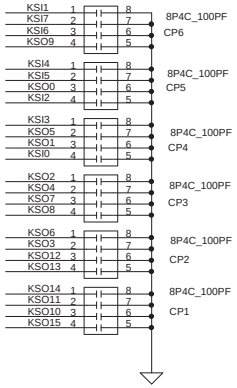


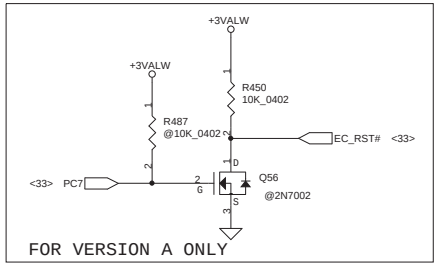




INT_KBD CONN.







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Compal Electronics, Inc.	
Title	Power OK/Reset/RTC battery/Lid Switch/Int. KB
Size	Document Number: ACT10 — Rev 1.0A
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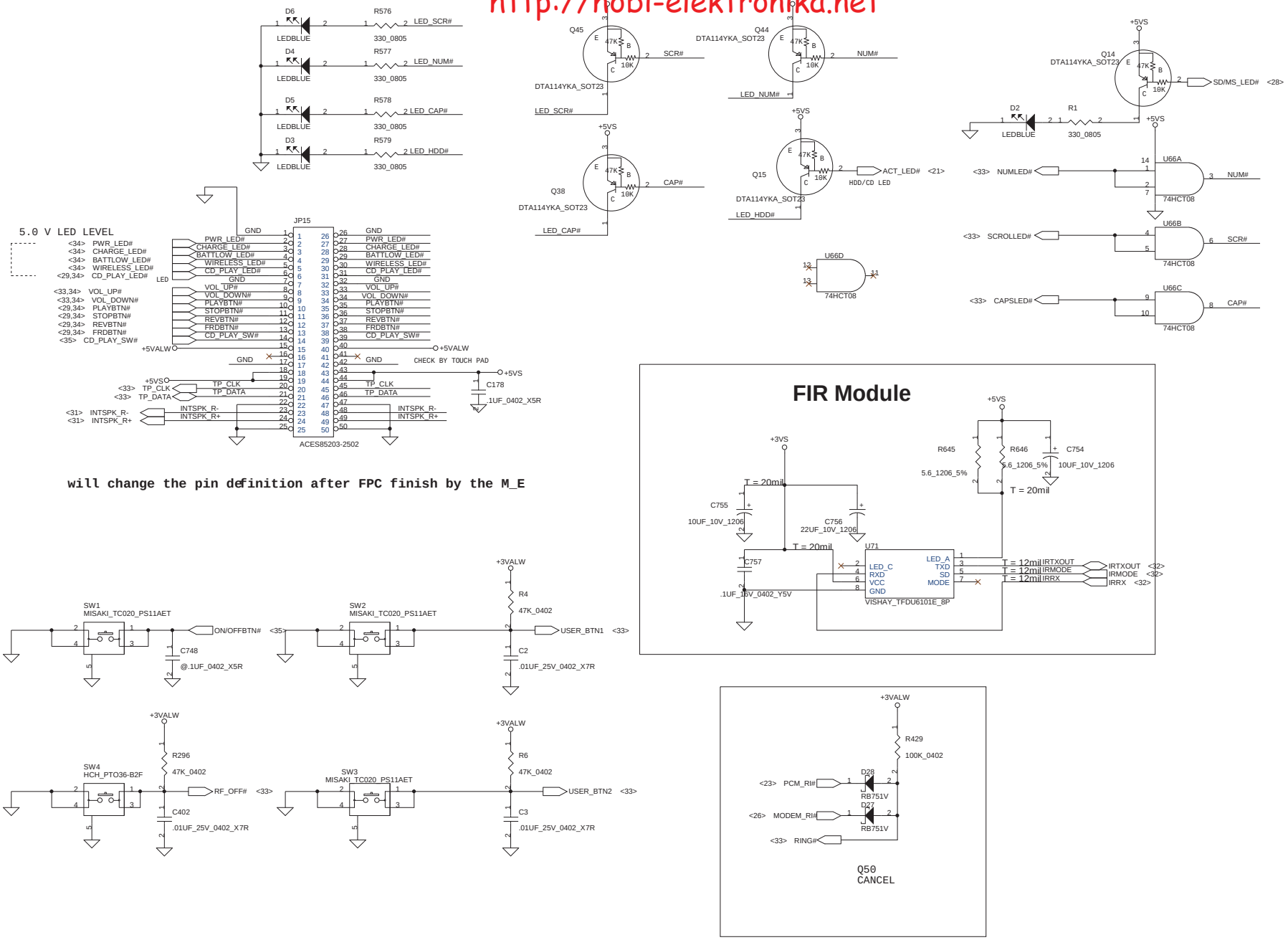

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Compal Electronics, Ltd.

Title	SW/LED/RI#/IR/CD BUTTOM
Size Custom	Document Number ACT10
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Date: Thursday, May 30, 2002	Sheet 36 of 45

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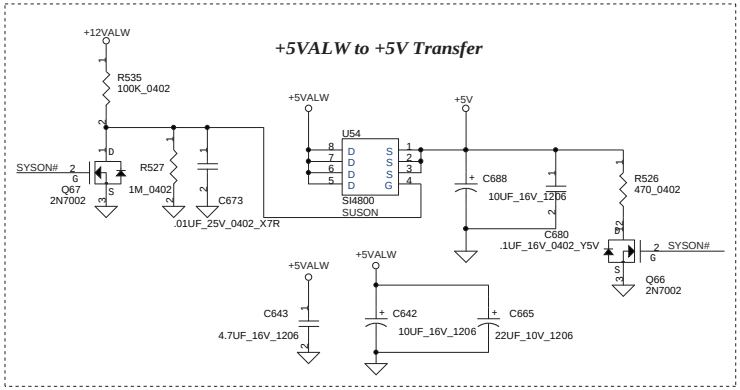
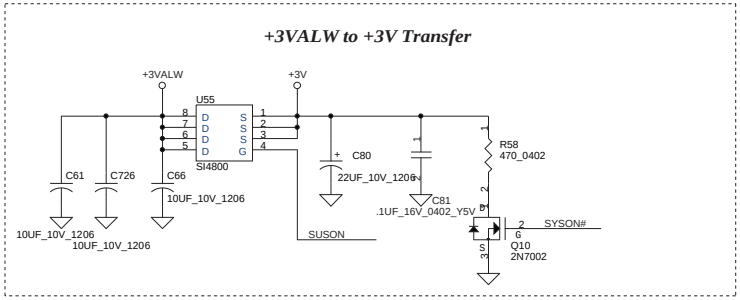
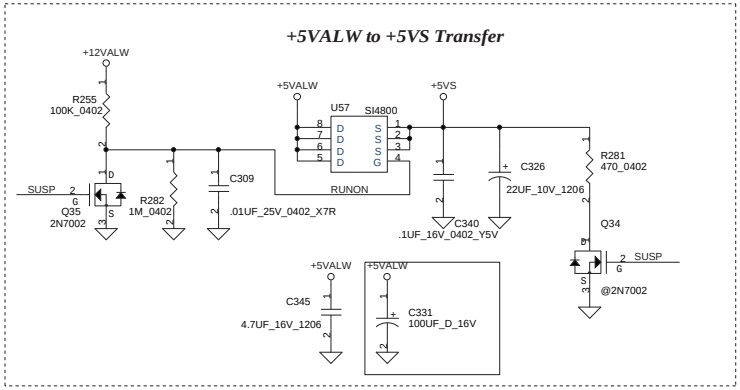
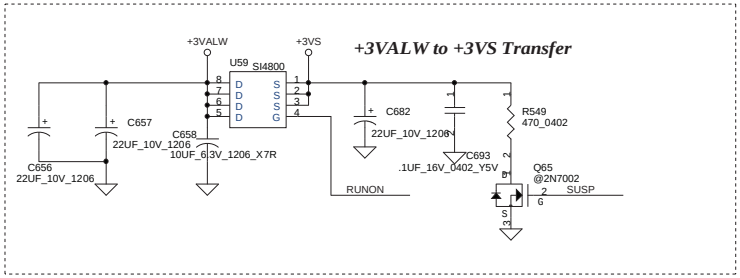
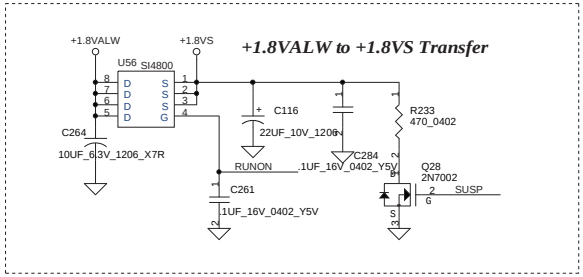


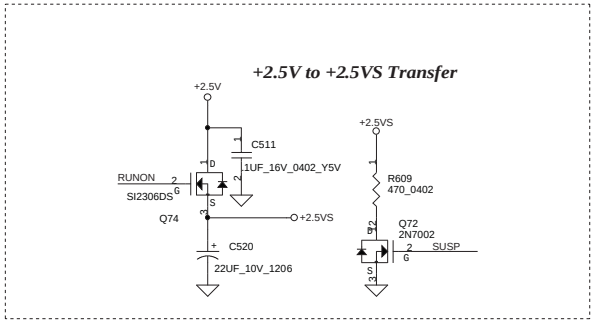


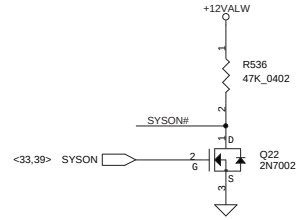


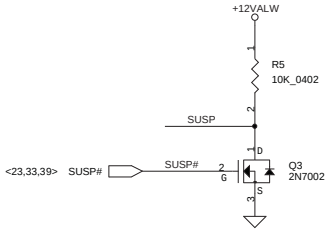


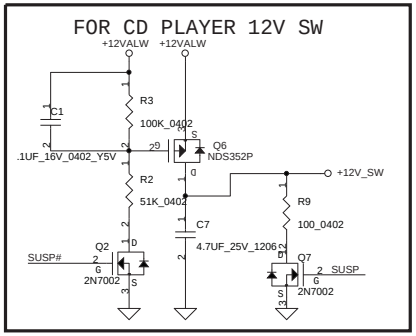
1.8VALW/+1.5VS Power direct provide











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Compal Electronics, Inc.	
Title	DC/DC Circuit Interface
Size	
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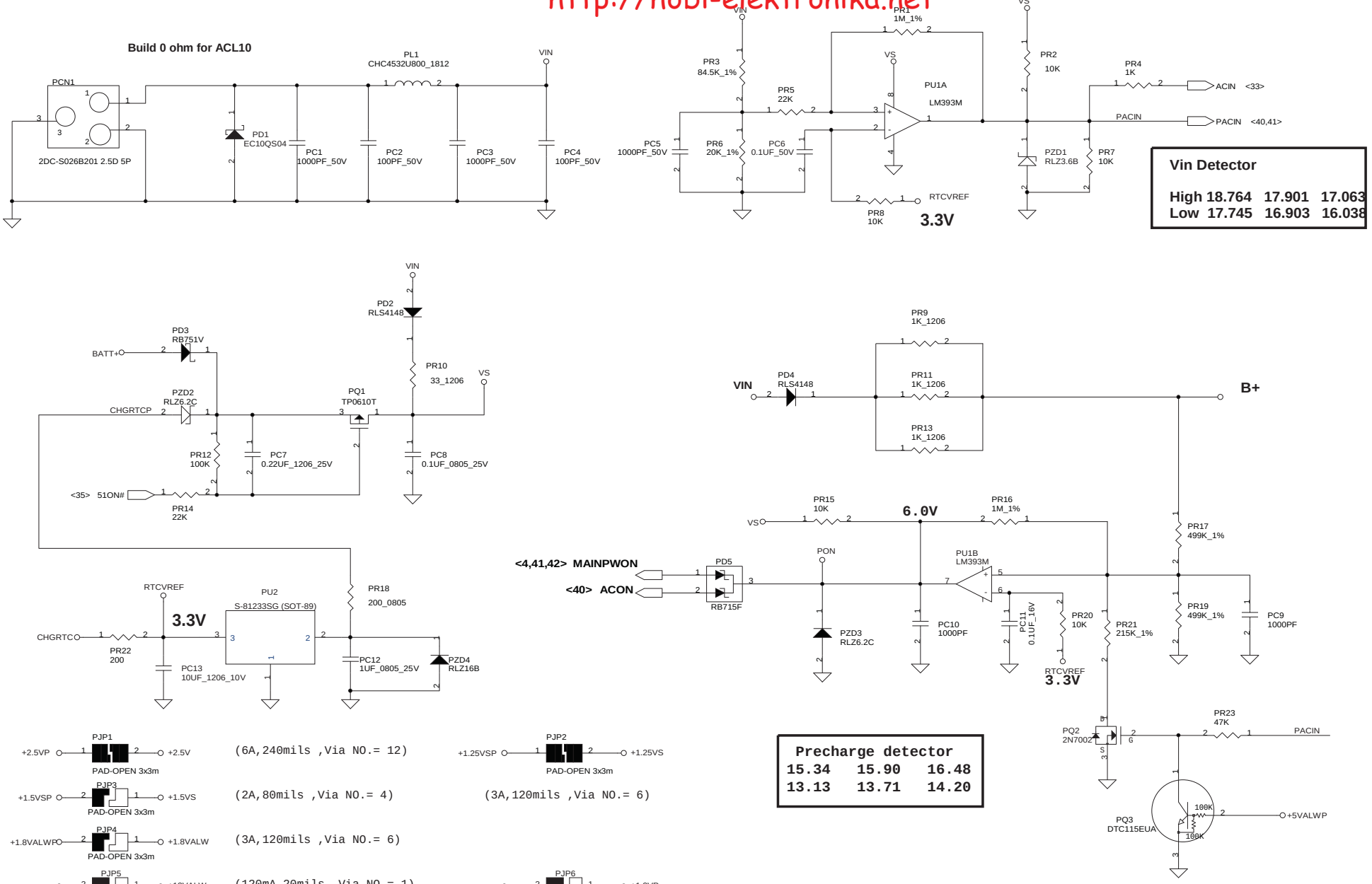

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COMPAL ELECTRONICS, INC			
Title: DCIN & DETECTOR			
Size: B	Document Number: ACT10		Rev: 1.0A
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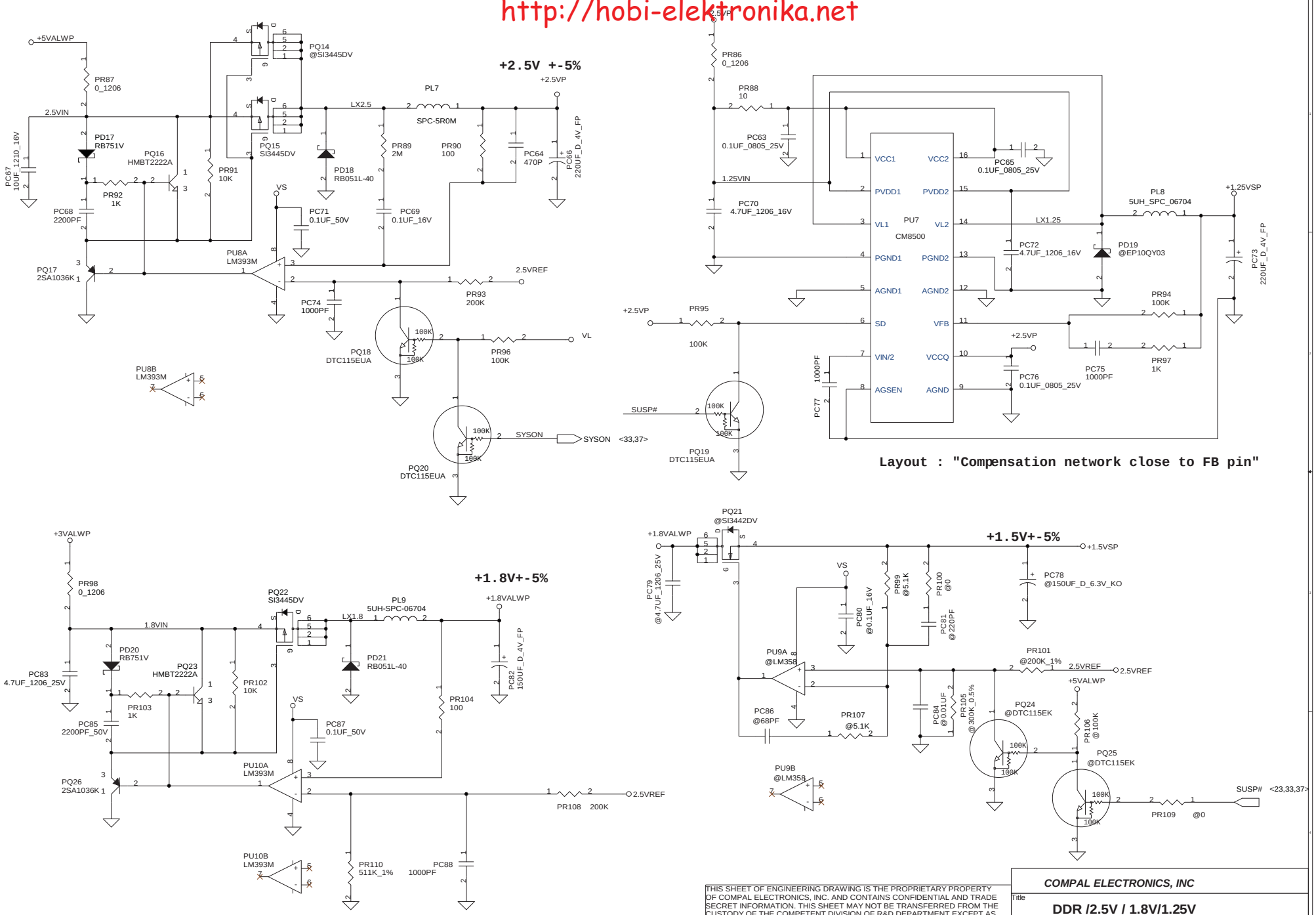

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COMPAL ELECTRONICS, INC	
Title	DDR /2.5V / 1.8V/1.25V
Size B	Document Number ACT10
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Date: Thursday, May 30, 2002	Sheet 39 of 45

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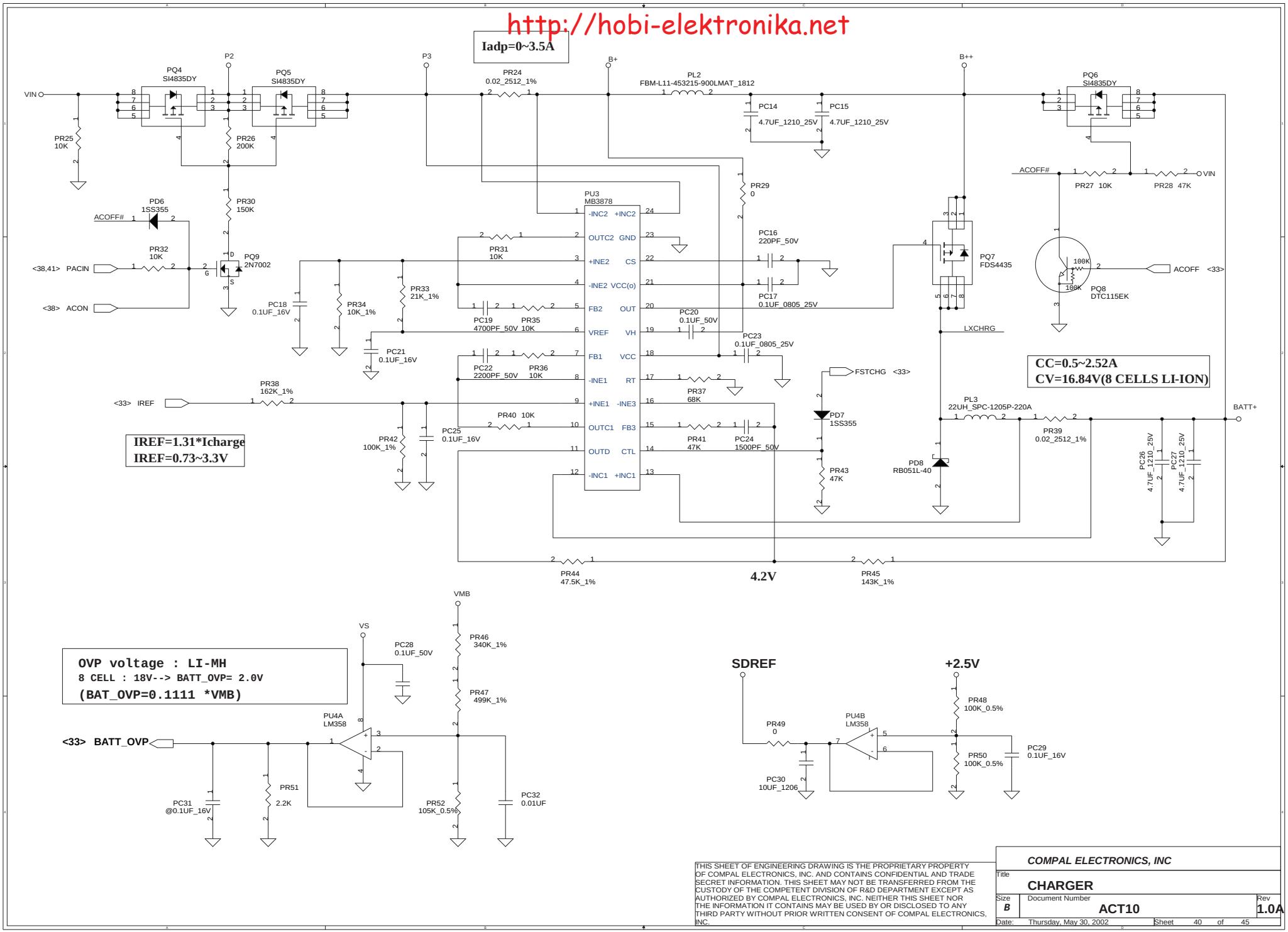

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COMPAL ELECTRONICS, INC		
Title: CHARGER		
Size: B	Document Number: ACT10	Rev: 1.0A
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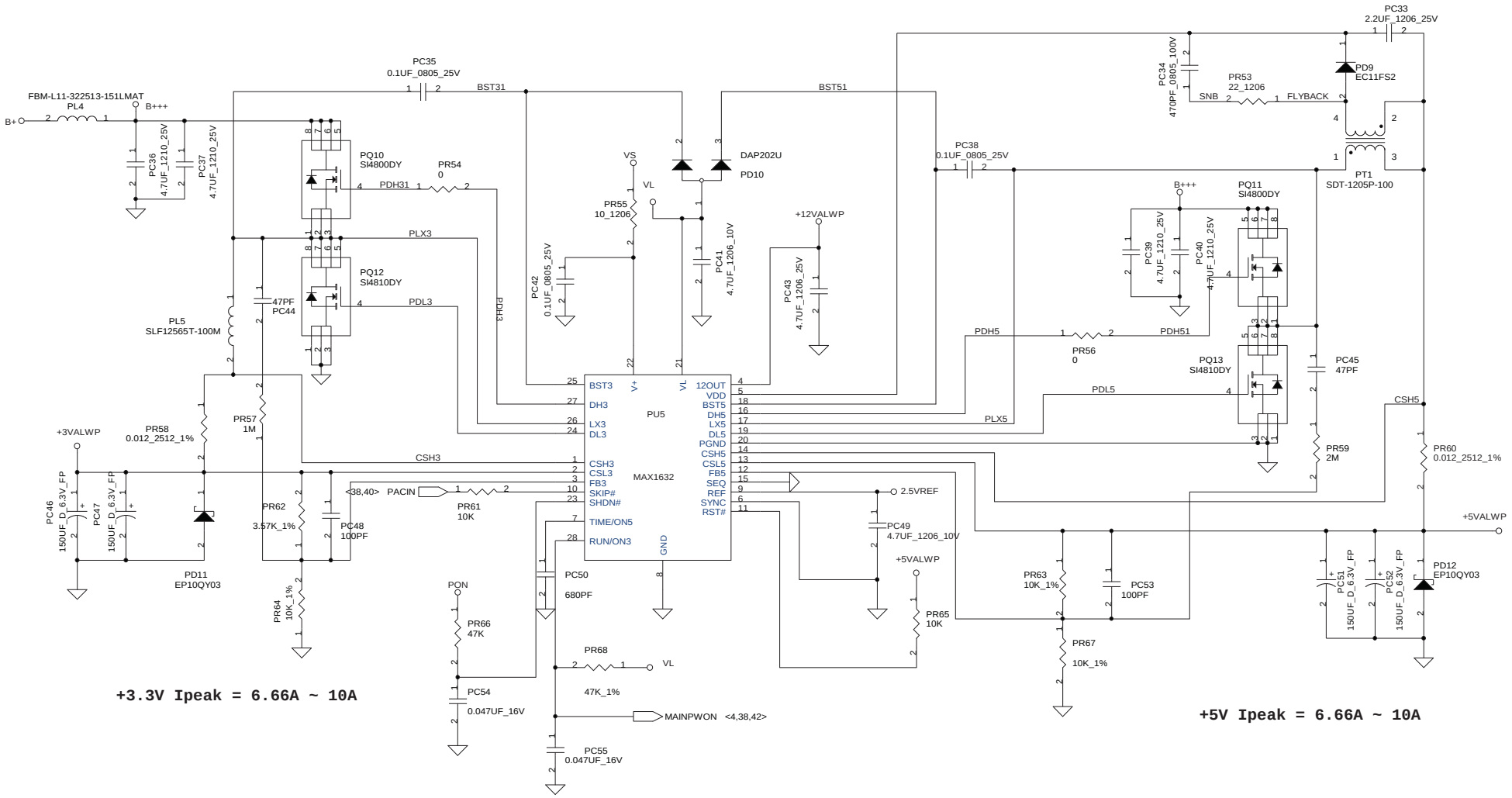

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COMPAL ELECTRONICS, INC		
Title: 5V/3.3V/12V		
Size: B	Document Number: ACT10	Rev: 1.0A
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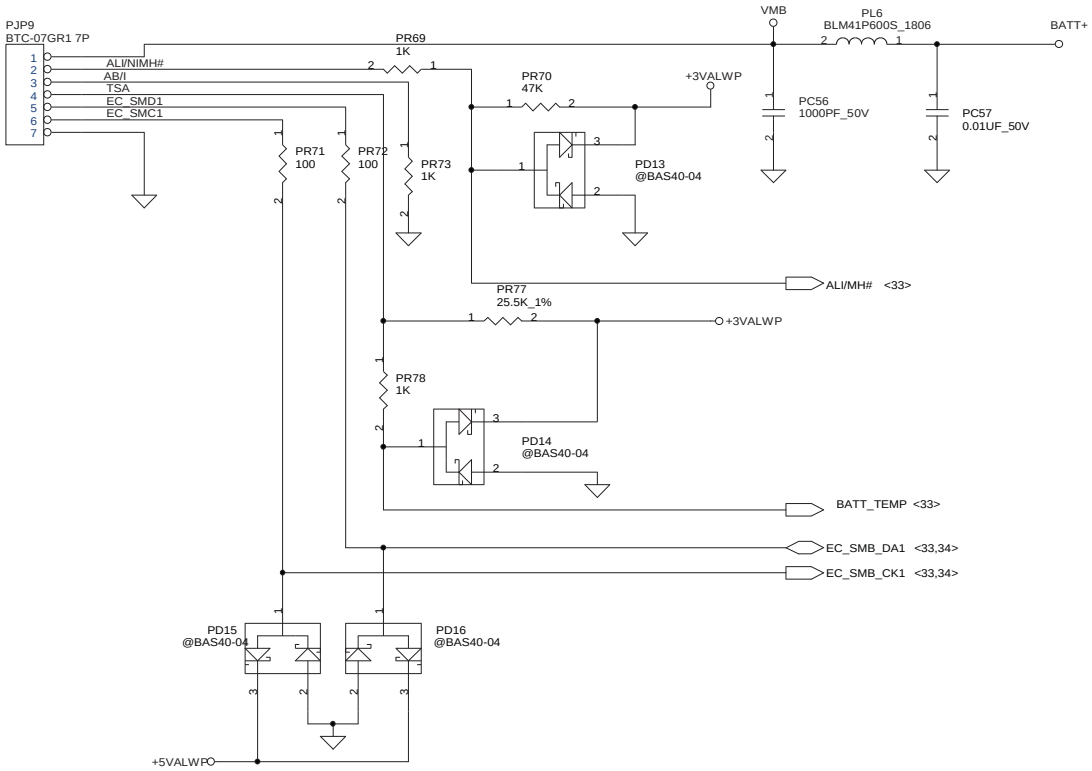
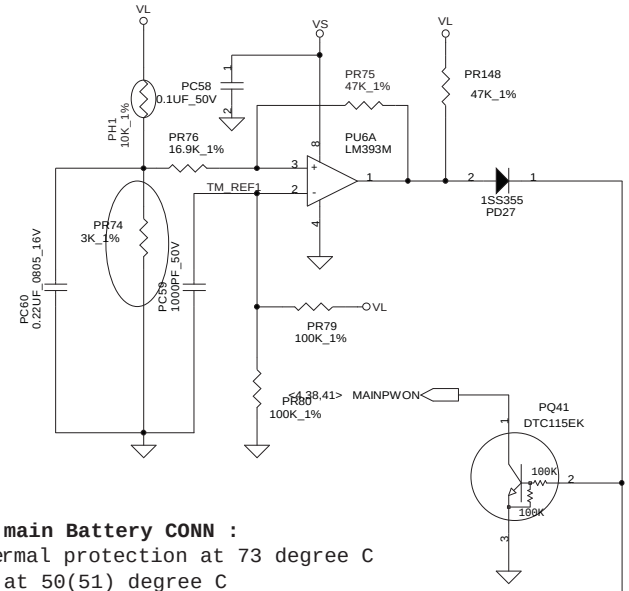
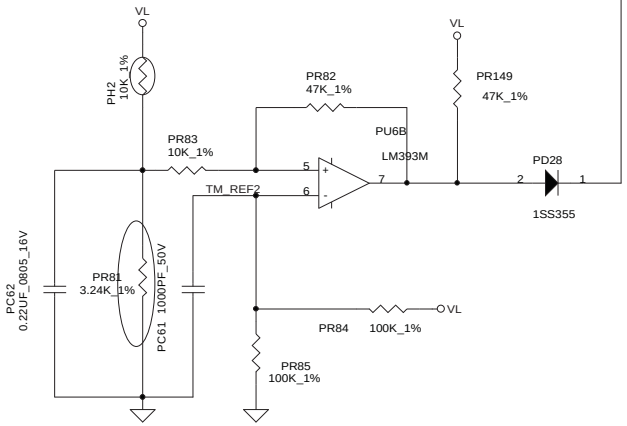


PH1 under CPU botten side :
CPU thermal protection at 87 degree C
Recovery at 48 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 73 degree C
Recovery at 50(51) degree C



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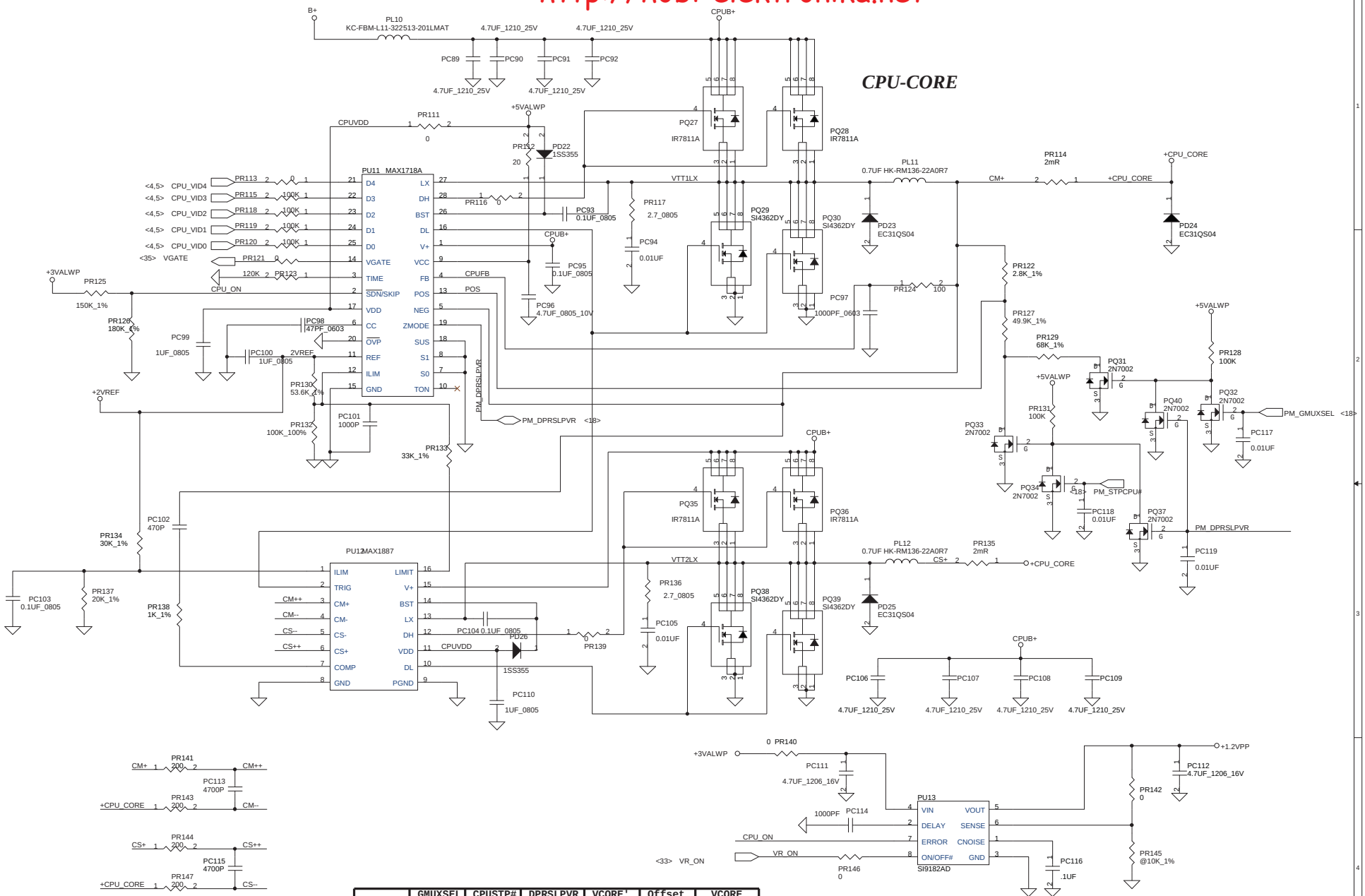

	GMUSEL	CPUSTP#	DPRSLPVR	VCORE'	Offset	VCORE
PM	1	1	0	1.30V	0%	1.30V
PM D-S	1	0	0		4.62%	1.239V
BM	0	1	0	1.20V	2.0%	1.176V
BM D-S	0	0	0		4.62%	1.144V
Deeper	X	0	1	1.0V	0%	1.0V

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AGP Multiplexed Channel B List **Power Managment table**

AGP D0 : VBD7
AGP D1 : VBD6
AGP D2 : VBD5
AGP D3 : VBD4
AGP D4 : VBD3
AGP D5 : VBD2
AGP D6 : VBD1
AGP D7 : VBD0
AGP D19 : VBD11
AGP D20 : VBD10
AGP D21 : VBD8
AGP D22 : VBD9
AGP D27 : VBDE
AGP D28 : VBCTL0
AGP D29 : VBCTL1
AGP D30 : VBHSYNC
AGP D31 : VBVSYNC
AGP AREQ# : VBCD
AGP RBF# : VBHCLK
AGP SBA0 : VBCLK
AGP STB1 : VBGCLK
AGP STB1# : VBGCLK#

AGP D24 : VAD0
AGP D23 : VAD1
AGP D25 : VAD2
AGP D26 : VAD3
AGP D10 : VAD4
AGP D9 : VAD5
AGP D8 : VAD6
AGP D11 : VAD7
AGP D12 : VAD8
AGP D13 : VAD9
AGP D14 : VAD10
AGP D15 : VAD11
AGP D16 : VADE
AGP D18 : VAHSYNC
AGP D17 : VAVSYNC
AGP STB0 : VAGCLK
AGP STB0# : VAGCLK#

State \ Signal	+3VALW +5VALW +1.8VALW +12VALW	+3V +5V +2.5V	+3VS +5VS +1.8VS +1.5VS +1.2VP +CPU_CORE +1.25VS
S0	ON	ON	ON
S1	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

IDSEL :
1394 : AD16
LAN : AD17
CARDBUS : AD19
MINI_PCI : AD18, AD22

PCI MASTER :
1394 : REQ0#, GNT0#
MINI-PCI(Wireless Lan) : REQ1#, GNT1#
CARDBUS : REQ2#, GNT2#
LAN : REQ3#, GNT3#
MINI-PCI : REQ4#, GNT4#

PCI IRQ ROUTING :
VGA : INTA#
1394 : INTB#
CARDBUS/MINI-PCI : INTC#
LAN/MINI-PCI : INTD#

History List

Item	Description	Page	Note	Date
1	Layout Ver. 0.0		Power not Include	01/11/22
2	Layout Ver. 0.0 add power		Power Include	01/11/23
3	Add Part Number			01/12/25
4	Change some parts suggest from SiS		Add Jumpper	01/1/3

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