REV: 3B

MODEL	REV	CHANGE LIST
NT2 M/B	3A	PAGE2: BOM Change R66,R68,R76 from 10K to 0ohm. PAGE11: Reserve VGARST signal to GPIO pin and detect VGA power control pin. PAGE13: BOM change_VGA PCIE_TESTIN need pull low.(ADD R542=10K,DEL R548=10K) PAGE13: ADD 4.7K on TV-OUT select pin. PAGE13: BOM Del U48,R547,R135,R131,R123,C83,C82,C139,L20,R124,R129,R127 , ADD R563,R571,R564 FOR disable spread spectrum. PAGE14: Change Q64 circuit for VGA_1.5V leakage. PAGE14: ADD two Caps for VGACore Voltage quality.. PAGE15: STRAP PIN GPIO4 FOR A23 VER FUNCTION (called Reversed_Lanes) NEED PULL-UP. PAGE21: Change 6-in-1 connect vendor and reserve one B-T-B connect. PAGE21: ADD resister 1K for Write Protect isssue,Chnage XD CD signal circuit (diode,resister). PAGE22: Change Bluetooth Power from 3V to 3VSUS for supsend issue. PAGE24: Change MIC circuit. PAGE24: ADD resisters and change CON for MODEM EMI issue, ADD two screw hole for M/E. PAGE25: Change Headphone detect circuit for noise issue with CableDock. PAGE25: Change MIC circuit of MIC_BIAS. PAGE27: Cable Dock pin 59,60 NET CHANGE from AGND to GND. PAGE27: DEL Q38 for change Dock-in circuit. PAGE27: Reserve MINI_PCI 3VAUX and -MINIPME to 3VPCU. PAGE28: Change HDD connect type from SMT to DIP for reduce SMT issue (BOM need to update). PAGE28: ADD FAN CAP 220U FOR FAN FG. PAGE29: BOM change_fine-tune LED driving current. (R678,R677=>300ohm; R425,R482,R31,R359,R316,R112,R540=>130ohm) PAGE30: BOM change_fine-tune LED driving current.(R102,R99=>130ohm) PAGE36: BOM DEL PQ64 AND Change 1.8V circuit for TV-OUT quality. PAGE37: BOM DEL PR232 for enhance VGACORE power. PAGE37: Change VGACORE setting to support 1.15V for M22 chip.
	3B	PAGE04: Change Thermal IC pin "-ALT","-OVT" define. PAGE04: Add reserve CPUHOT CONTROL from PC551. PAGE11: Change "-WAKE" signal pull-up value from 10K to 5.1K for Express Card. PAGE13: Add one circuit base on refer-122 ATI schematic change the -PERST may momentarily act as an output when during power up. PAGE19: TV-OUT signals add protect Diode. PAGE19: L65,L62,L60 FROM 10R Change to CX8LL680001and C668,C670,C671 add 10P for EMI. PAGE20: Change 7411 CLKRUN (MFUNC6) to plll-low. PAGE25: Change DOCK_OK resister value for fix sound break. PAGE26: Change resister value for Express Card modify. PAGE27: Change CableDock power to BEAD for fix DOCK5V. PAGE27: Add one resister for wake up from RF device. PAGE28: Change FAN circuit for enhance Fan control performance. PAGE30: ADD reserve one resister(100K) for CIR_IN signal pull up. PAGE30: ADD one resister(10K) of "SWID1" for system change Thermal pin define ID. PAGE31: Change CN23(DC Jack) footprint. PAGE33: Del PR206,PR209(reserve system power measure before) PAGE35: PR6,PR14,PR25,PR37 add 2.2B and PC4,PC11,PC17,PC29 1000P for EMI. PAGE36: Del PR220,PR238(reserve system power measure before) PAGE37: Del PR226(reserve system power measure before) PAGE38: Del PR234(reserve system power measure before)

Page	NT2 M/B BOARD FM	NT2 M/B BOARD TO
1	2B	
2	3A	
3	1A	
4	2A	3B
5	1A	
6	1A	
7	2A	
8	1A	
9	1A	
10	1A	
11	3A	3B
12	2A	
13	3A	3B
14	3A	
15	3A	
16	2A	
17	1A	
18	1A	
19	2B	3B
20	1A	3B
21	3A	
22	3A	
23	2B	
24	3A	
25	3A	3B
26	2B	3B
27	3A	3B
28	3A	3B
29	3A	
30	3A	3B
31	2B	3B
32	2A	
33	2A	3B
34	2A	
35	2A	3B
36	3A	3B
37	3A	3B
38	2A	3B

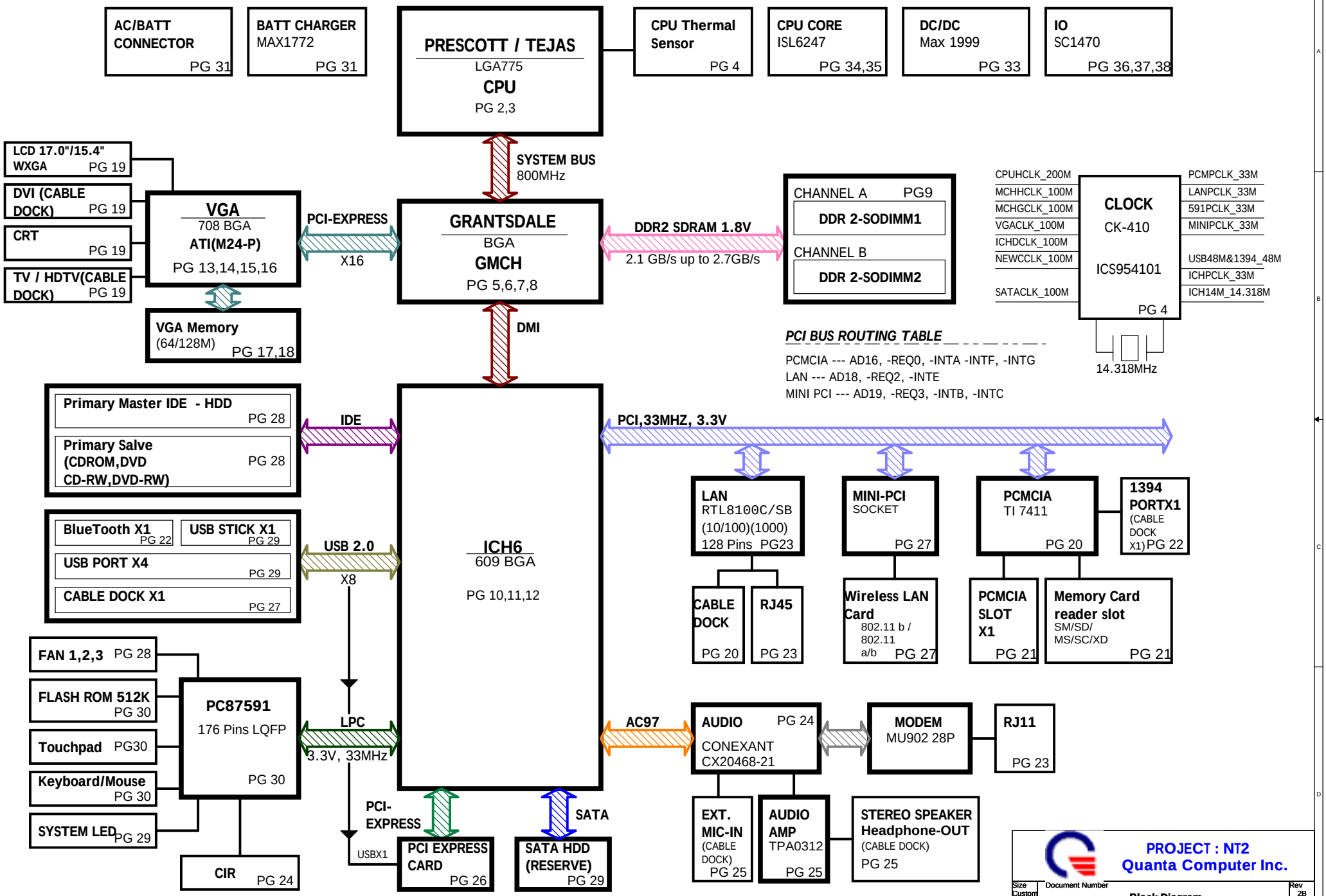
Quanta Computer Inc.	PROJECT:NT2	PCBA NO.		DOC. NO: 204
	APPROVED BY :Tom Wang	CHECK BY:Carey Chen	DRAWING BY:Johnny O	DATE :08/09/2004 SHEET 1

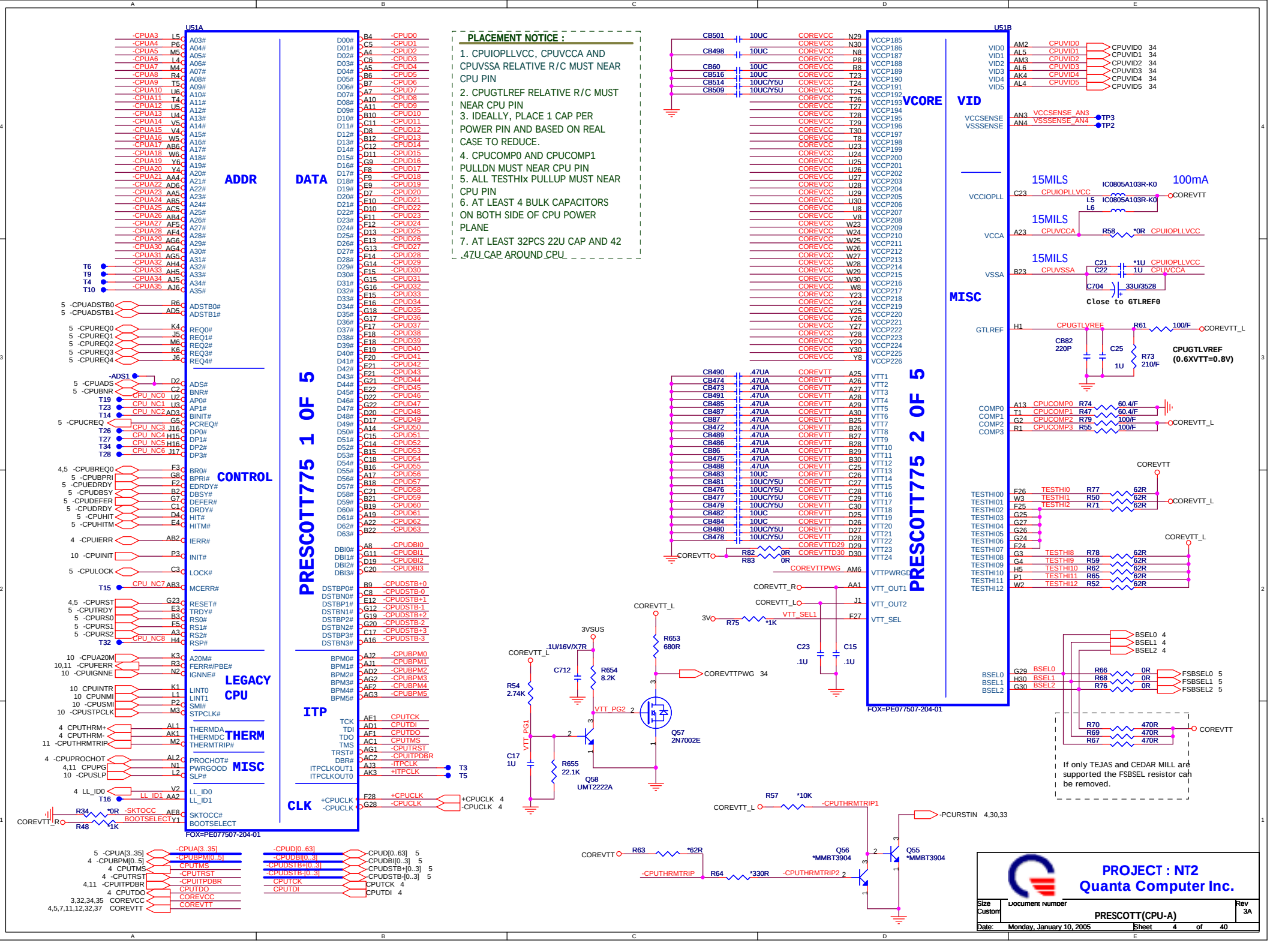
MODEL	REV	CHANGE LIST
NT2 M/B	1A	FIRST RELEASE
	2A	PAGE1: Change COREVTT power good circuit for CORE VCC Sequence. PAGE4,11: Add CPU PROCHOT CIRCUT (Throttle) at battery only. PAGE7: Because system 2.5V will change to 1.8V for support 1.8V VRAM so reserve one LED for support GMCH 2.5V voltage. PAGE11: Add one system ID for NT2B, and assign GPO19 pin to support CPU PROCHOT (Throttle) function. PAGE13: Add M24 GPIO14 to support TV_OUT select forTampa2, and reserve strap pin for VGA Memory tyep setting. PAGE14: Add LDO for VGA2.5 when system 2.5V change to 1.8V for suppport 1.8V VRAM. PAGE14: Reserve LDO of VGA1.5V for tune VGA power sequence. PAGE15: Add VGA BIOS "-ROMCS" control pin for support VRAM 256MB and reserve Memory type strip pin. PAGE16: Add Flash ROM for VGA BIOS. PAGE19: Modify DIODE Pin Deffine for BAV99 Part. PAGE21: Add pull up resister for XD "-CE" singnal. PAGE23: Reserve another LAN TRANSFORM FOR 10/100 and reserver one resister for LAN1.2V source and pull up resister for GIGA LAN transform terminal pin. PAGE24: Del CIR on board circuit and reserve CN37 for NT2B. PAGE24: Add resister to lower Cable Dock MIC signal and add more EMI PAD reserve. PAGE25: Modify Headphone CIRCUIT FOR CABLE DOCK. PAGE26: Change PCI EXPRESS Card power circuit - use TI TPS2331; and add CAP of Power plane bridge for EMI reserve. PAGE27: Cable Dock pin define change for match NP2 pin define and add one pin for TV-OUT select. PAGE27: Reserve always turn on the cable dock power circuit and change VA power to VAD. PAGE29: Add two connect for LED board and reserve two LED for NT2B. PAGE30: Add pull-up resister for Touch PAD power control and DIODE on "-SWI"&"-RUNSCI" for leakage, and reserve schottky diode and resister for VCC voltage undershoot issue. PAGE31: Add PD32 prevent power VAD with PWR_SRC leakage. PAGE31: Change PR146 and PR72 to 100K because PWM frequence change to 200Hz. PAGE32: Add 1.8V,VGACORE,VGA1.2V voltage discharge circuit. PAGE33: Add PR210 to fix MAX1999. PAGE34: Change PR180 to 0ohm and delete PC36 for COREVTTPWG signal delay time. PAGE34: Add PR203 NTC 4.7K to control cpu load line. PAGE36: Change 1.8VSUS and 1.5V power circuit of use MAX1845 for enhance transform efficiency. PAGE37: Change VGACORE of use LMV321 for enhance transform efficiency.
	2B	PAGE1: R655 BOM Change from 2.2K to 22.1K fix Q58 can't turn on issue. PAGE11: Add one cap for RTCVCC and place mechanic open area. PAGE13: BOM del C64,C90,C78 for same use TV-OUT filter. PAGE14: Reserve resister for use one VGA 2.5V LDO. PAGE19: Modify TV-OUT circuit and default use HDTV filiter. PAGE21: Reserve one circuit of Card power control for TI recommand. PAGE22: Change CN13 connect type for system ASS'Y. PAGE22: Reserve CAP for EMI solution on "DCOEX1" &"DCOEX2". PAGE23: Modify LAN transform pin8 need connect to "-LANPHY_MDI0". PAGE24: Add Hole for mechanic, and DEL CN37 for NT2B. PAGE25: BOM change AMP form TPA0212 to TPA0312. PAGE26: Modify PCI EXPRESS signal TX and RX change, and TPS2231 and CN22 footprint modify. PAGE26: New Card power switch reserve another source RICOH R5535. PAGE27: Modify Cable Dock TV-OUT circuit. PAGE27: BOM Modify R401 and Q44 DEL.R688 1K ADD for always turn on 5VDOCK and 5VAMP_PR power. PAGE28: CN36 Change type. PAGE29: Change CN38 from 5Pin to 8Pin for NT2B system and CN10 change type. PAGE30: CN14 change from 10pin to 12pin for NT2B system. PAGE31: ADD one circuit for disable charger IC working while system battery only.

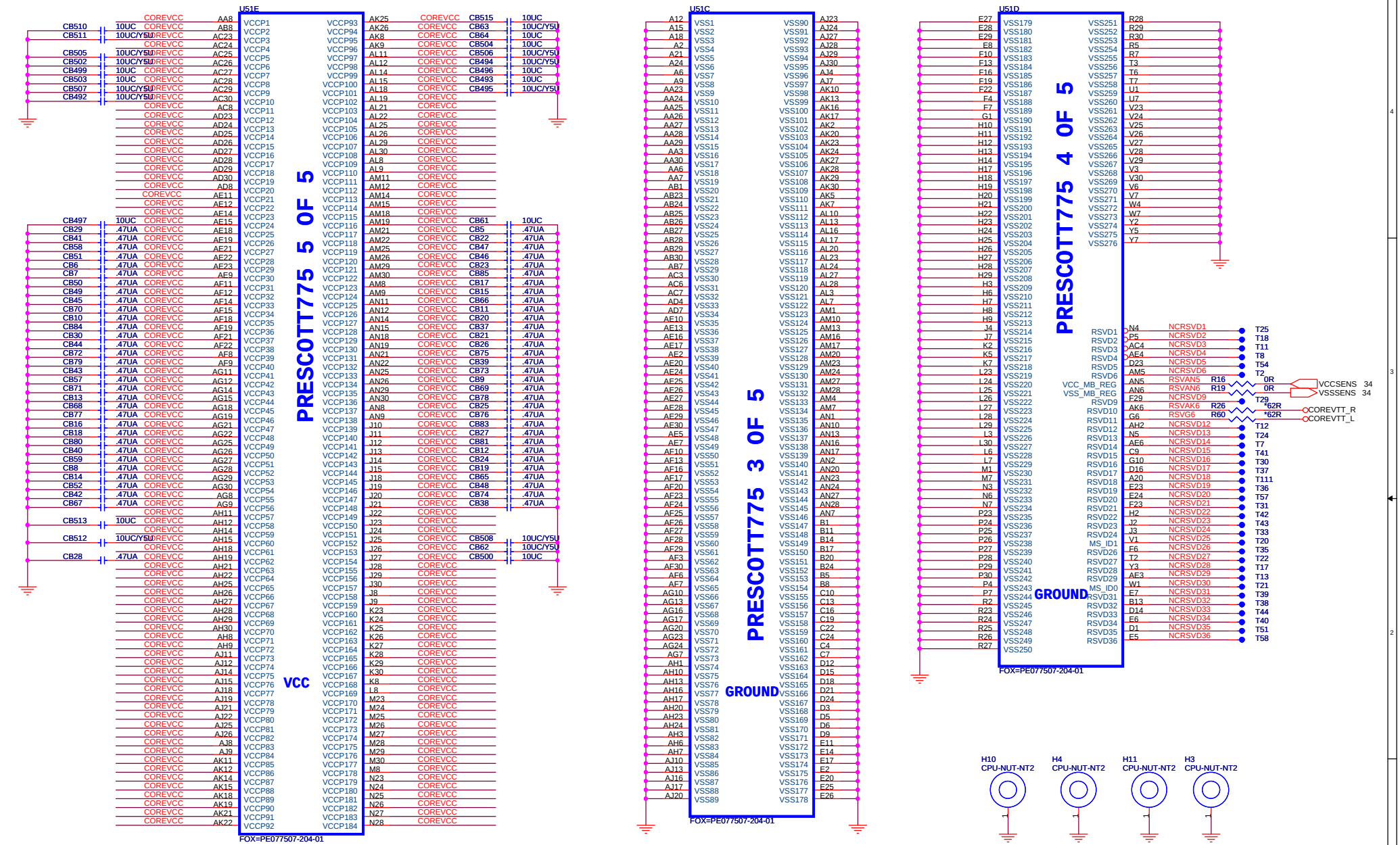
Page	NT2 M/B BOARD FM	NT2 M/B BOARD TO
1	2B	
2	3A	
3	1A	
4	2A	3B
5	1A	
6	1A	
7	2A	
8	1A	
9	1A	
10	1A	
11	3A	3B
12	2A	
13	3A	3B
14	3A	
15	2A	
16	2A	
17	1A	
18	1A	
19	2B	3B
20	1A	3B
21	3A	
22	3A	
23	2B	
24	3A	
25	3A	3B
26	2B	3B
27	3A	3B
28	3A	3B
29	3A	
30	3A	3B
31	2B	3B
32	2A	
33	2A	3B
34	2A	
35	2A	3B
36	3A	3B
37	3A	3B
38	2A	3B

Quanta Computer Inc.	PROJECT:NT2	PCBA NO.	REV: 3B	DOC. NO: 204
	APPROVED BY :Tom Wang	CHECK BY:Carey Chen	DRAWING BY:Johnny O	DATE :08/09/2004 SHEET 1

NT2 - Block Diagram



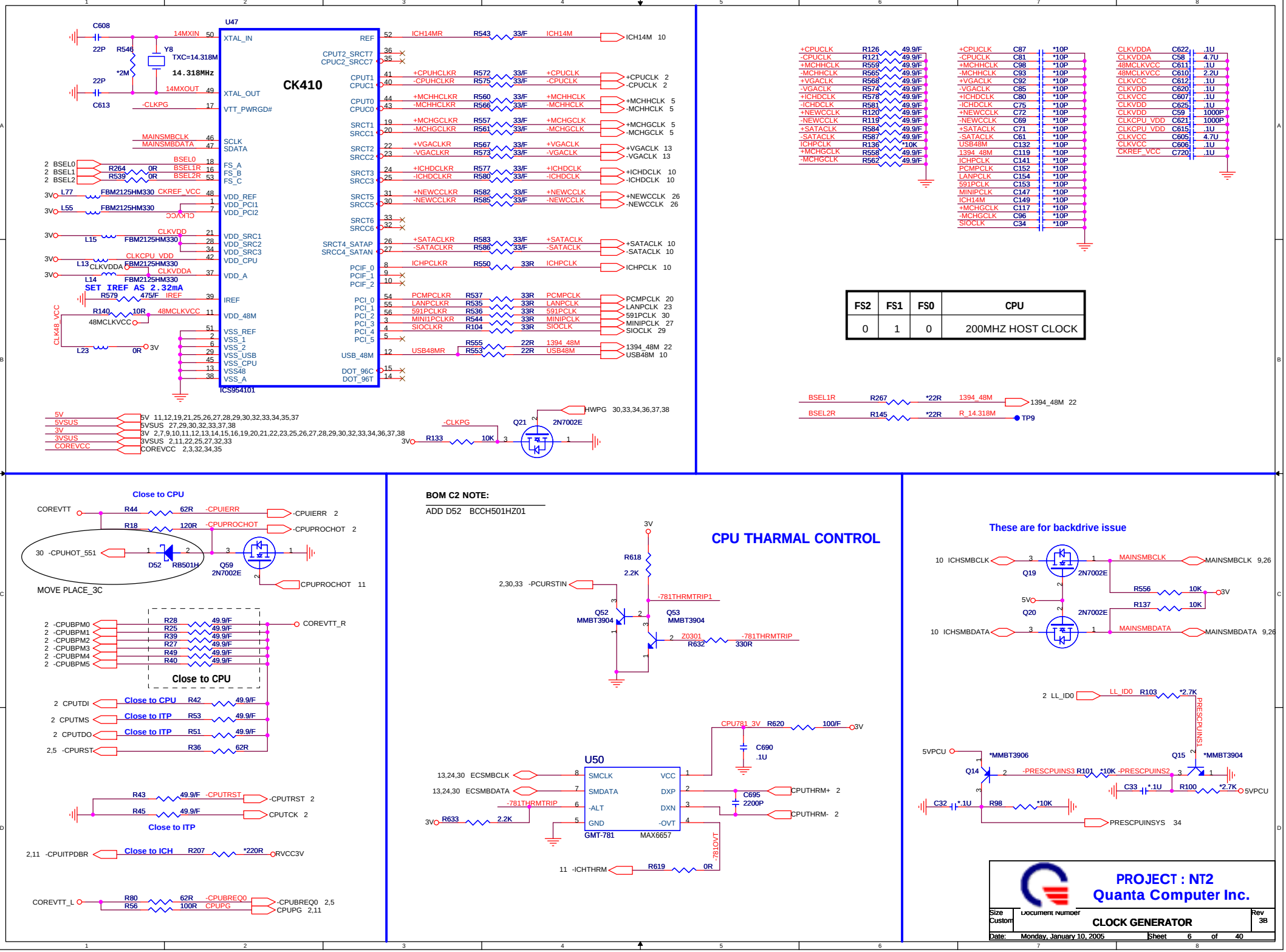

U51A
PRESCOTT775 1 OF 5
ADDR
DATA
CONTROL
LEGACY CPU
THERM
MISC
ITP
CLK
FOX=PE077507-204-01
PLACEMENT NOTICE :
1. CPUIOPLLVCC, CPUVCCA AND CPUVSSA RELATIVE R/C MUST NEAR CPU PIN
2. CPUGTLREF RELATIVE R/C MUST NEAR CPU PIN
3. IDEALLY, PLACE 1 CAP PER POWER PIN AND BASED ON REAL CASE TO REDUCE.
4. CPUCOMP0 AND CPUCOMP1 PULLDN MUST NEAR CPU PIN
5. ALL TESTHIx PULLUP MUST NEAR CPU PIN
6. AT LEAST 4 BULK CAPACITORS ON BOTH SIDE OF CPU POWER PLANE
7. AT LEAST 32PCS 22U CAP AND 42 .47U CAP AROUND CPU
U51B
PRESCOTT775 2 OF 5
VCORE
VID
MISC
FOX=PE077507-204-01
15MILS
100mA
IC0805A103R-K0
COREVTT
CPUIOPLLVCC
CPUVCCA
CPUVSSA
Close to GTLREF0
CPUGTLVREF
(0.6XVTT=0.8V)
COREVTT_L
If only TEJAS and CEDAR MILL are supported the FSBSEL resistor can be removed.
PROJECT : NT2
Quanta Computer Inc.
Size Custom
Document Number
PRESCOTT(CPU-A)
Rev 3A
Date: Monday, January 10, 2005
Sheet 4 of 40



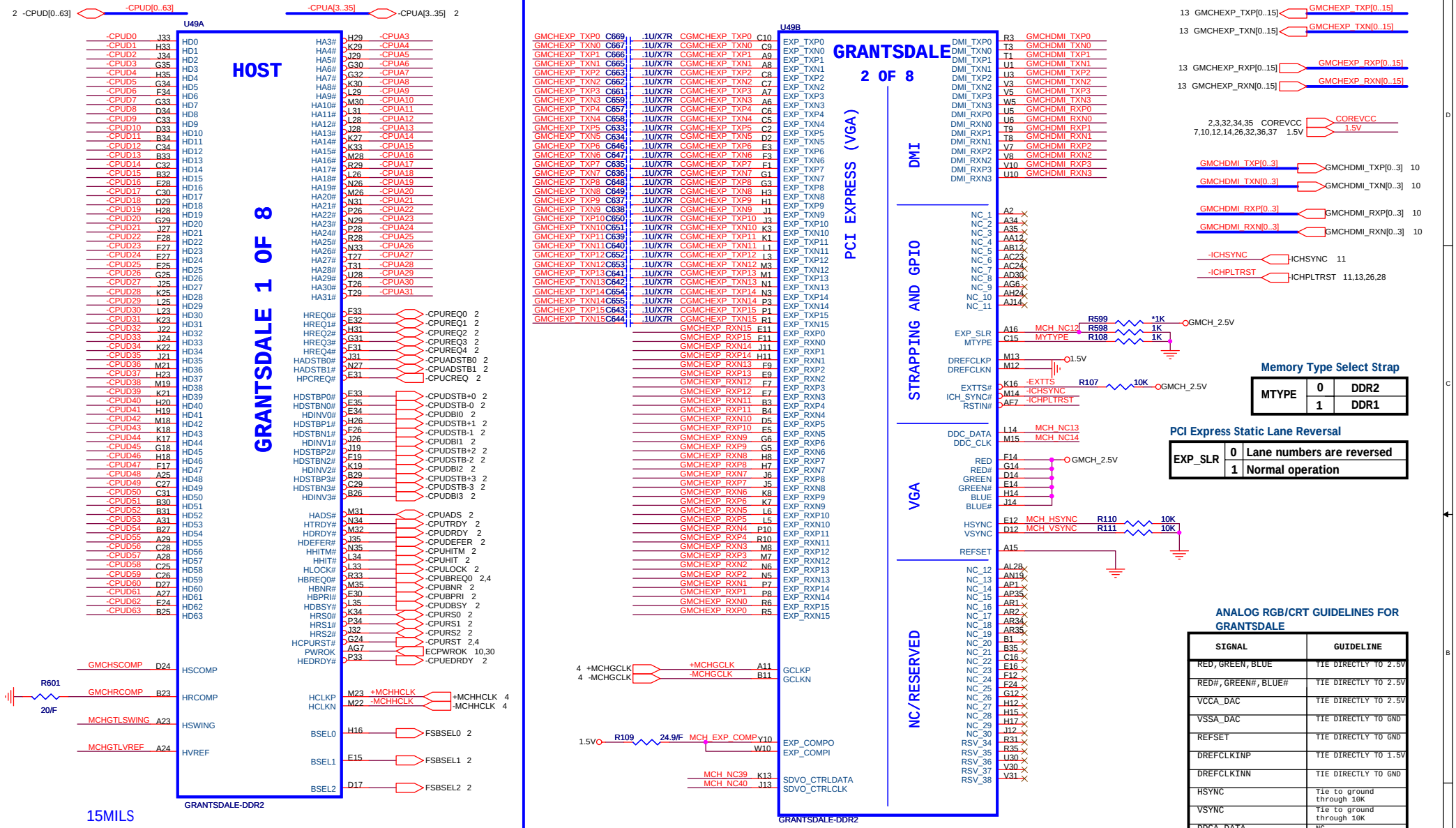
PROJECT : NT2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PRESCOTT(POWER/GND)	1A

Date: Monday, January 10, 2005 Sheet 5 of 40



FS2	FS1	FS0	CPU
0	1	0	200MHZ HOST CLOCK


U49A
HOST
GRANTSDALE 1 OF 8
GRANTSDALE-DDR2
U49B
GRANTSDALE
2 OF 8
PCI EXPRESS (VGA)
DMI
STRAPPING AND GPIO
VGA
NC/RESERVED
GRANTSDALE-DDR2
R601
20/F
15MILS
R604 301/F COREVTT
R603 102/F
C675 .01U/X7R
MCHGTLSWING
GMCHSWING = 1/4 * GMCHVTT
15MILS
R605 49.9/F COREVTT
R606 100/F
C677 .1U
C678 220P
MCHGTLVREF
GMCHVREF = 0.67 * COREVTT=0.8V
COREVTT R607 60.4/F GMCHSCOMP
C679 2.2P
R109 24.9/F MCH_EXP_COMP
Memory Type Select Strap
MTYPE 0 DDR2
1 DDR1
PCI Express Static Lane Reversal
EXP_SLR 0 Lane numbers are reversed
1 Normal operation
ANALOG RGB/CRT GUIDELINES FOR GRANTSDALE
SIGNAL GUIDELINE
RED,GREEN,BLUE TIE DIRECTLY TO 2.5V
RED#,GREEN#,BLUE# TIE DIRECTLY TO 2.5V
VCCA_DAC TIE DIRECTLY TO 2.5V
VSSA_DAC TIE DIRECTLY TO GND
REFSET TIE DIRECTLY TO GND
DREFCLKINP TIE DIRECTLY TO 1.5V
DREFCLKINN TIE DIRECTLY TO GND
HSYNC Tie to ground through 10K
VSYNC Tie to ground through 10K
DDCA_DATA NC
DDCA_CLK NC
DDCA_DATA NC
DDCA_CLK NC
D_REFSCKINP TIE DIRECTLY TO 1.5V
D_REFSCKINN TIE DIRECTLY TO GND
PLACEMENT NOTICE :
1. GMCHSWING, GMCHVREF, GMCHHLSWING, GMCHHLVREF RELATIVE R/C MUST NEAR GMCH PIN
2. GMCHRCOMP AND AGPRCOMP RELATIVE R/C MUST NEAR GMCH PIN
3. GMCHRCOMP AND AGPRCOMP RELATIVE R/C MUST NEAR GMCH PIN
4. GMCHREFSET R/C MUST NEAR GMCH PIN
5. GMCHHLRCOMP R/C MUST NEAR GMCH PIN
6. GMCHBSEL0 AND GMCHBSEL1 MUST NEAR GMCH PIN
7. -AGPRST R/C MUST NEAR GMCH PIN
PROJECT : NT2
Quanta Computer Inc.
Size Custom
Document Number
GMCH(Processor System Bus)
Rev 1A
Date: Monday, January 10, 2005
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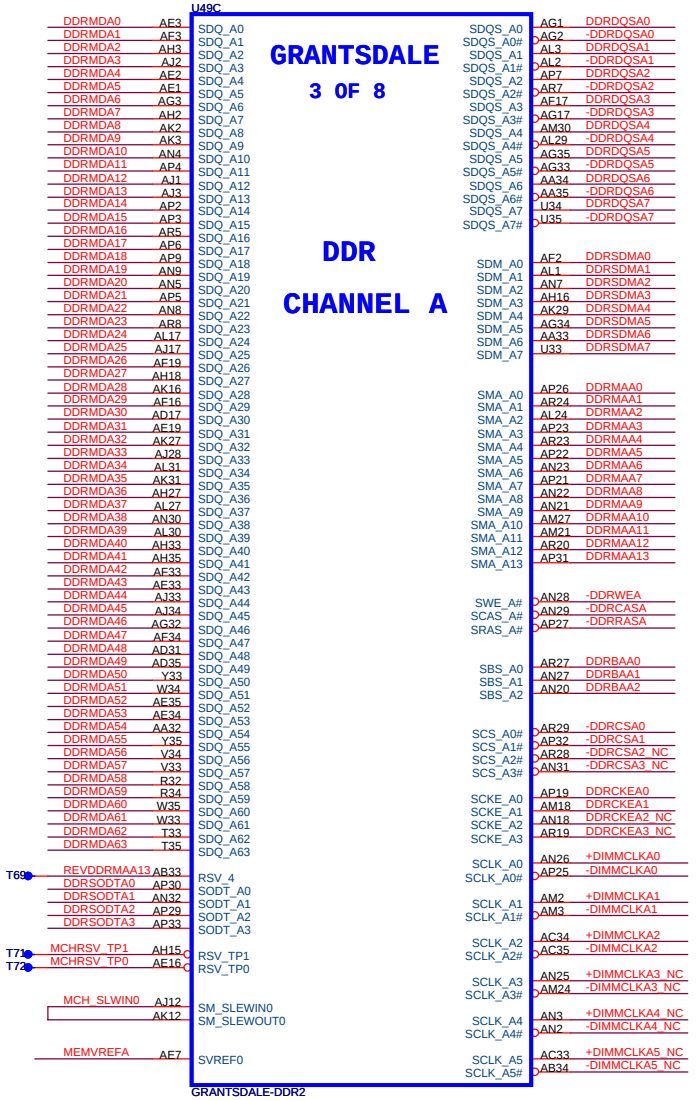
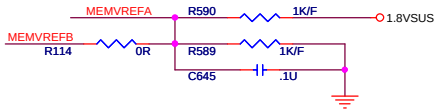
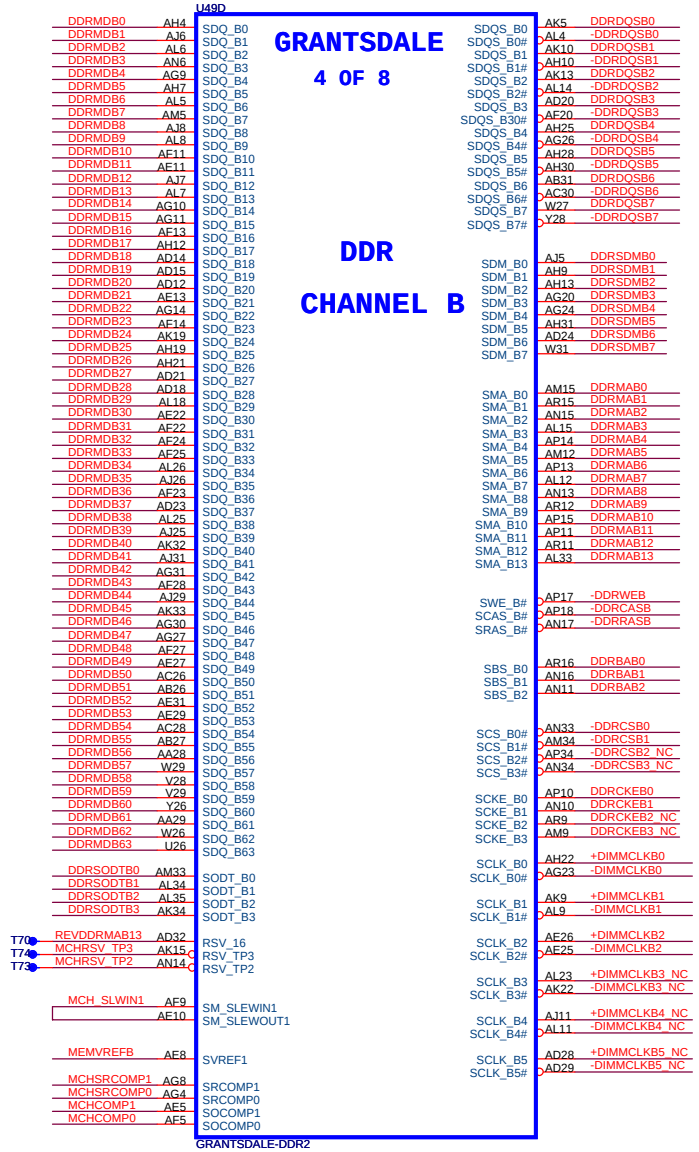
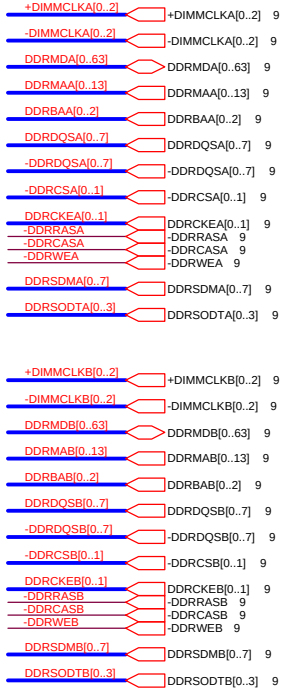
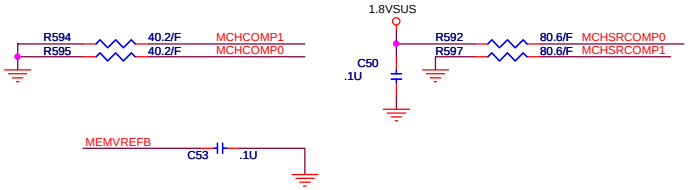




1. MEMVREFA AND MEMVREFB RELATIVE R/C MUST NEAT GMCH PIN



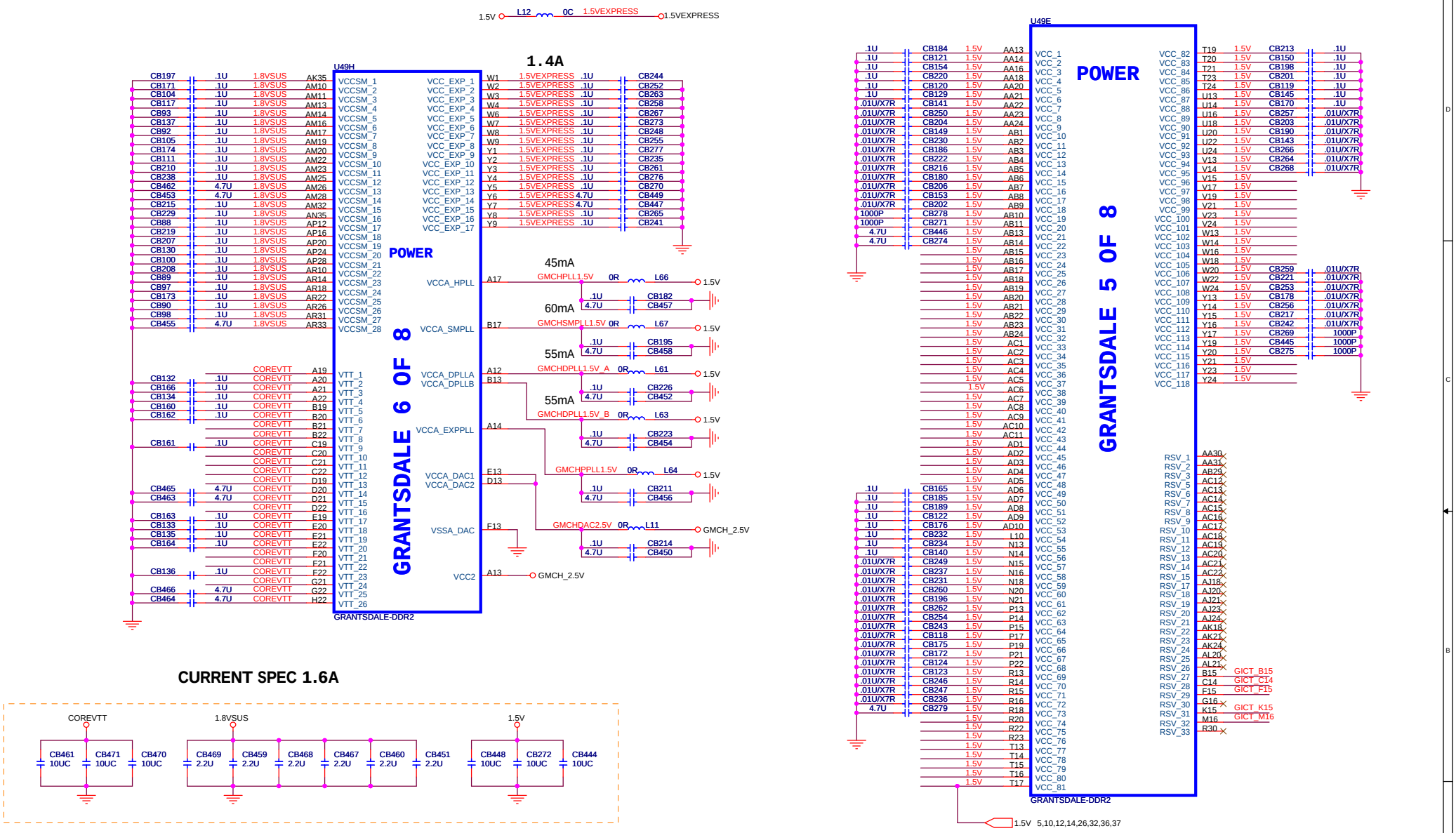




PROJECT : NT2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	GMCH DDR2 CHANNEL A	1A

Date: Monday, January 10, 2005 Sheet 8 of 40



PLACEMENT NOTICE :

1. IDEALLY, PLACE 1 CAP PER POWER PIN AND BASED ON REAL CASE TO REDUCE.
2. GMCHFSB1.5V RELATIVE R/C MUST NEAR GMCH PIN
3. GMCHDACPLL1.5V RELATIVE R/C MUST NEAR GMCH PIN

PROJECT : NT2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	GMCH(POWER/GND)	2A

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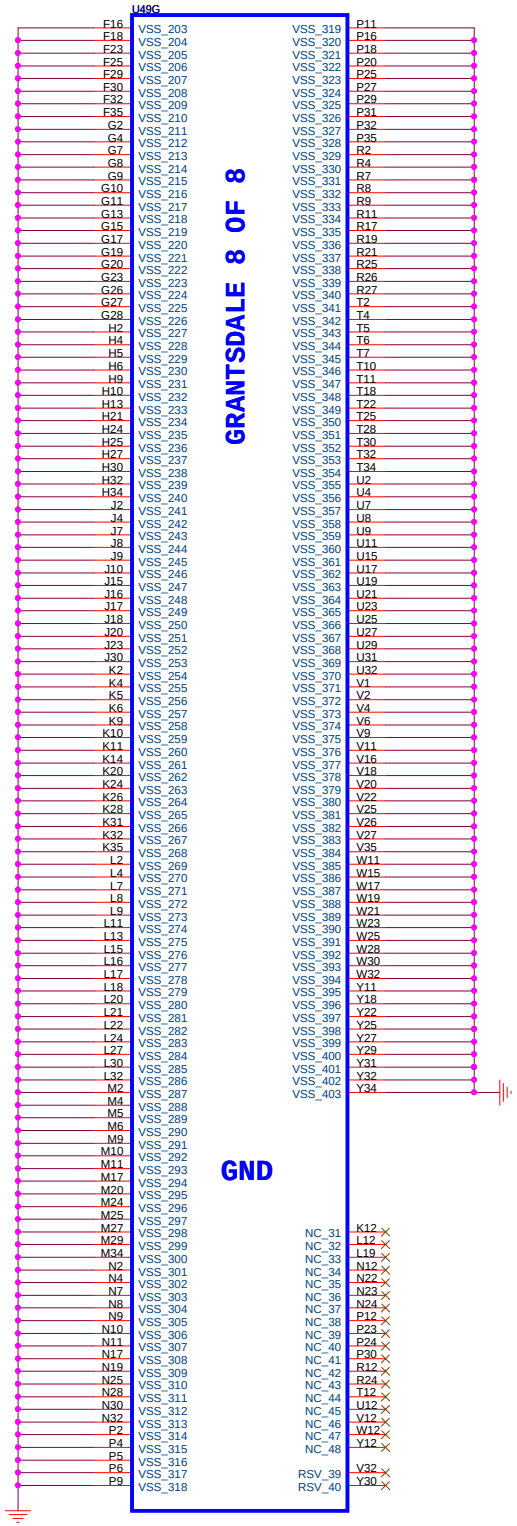

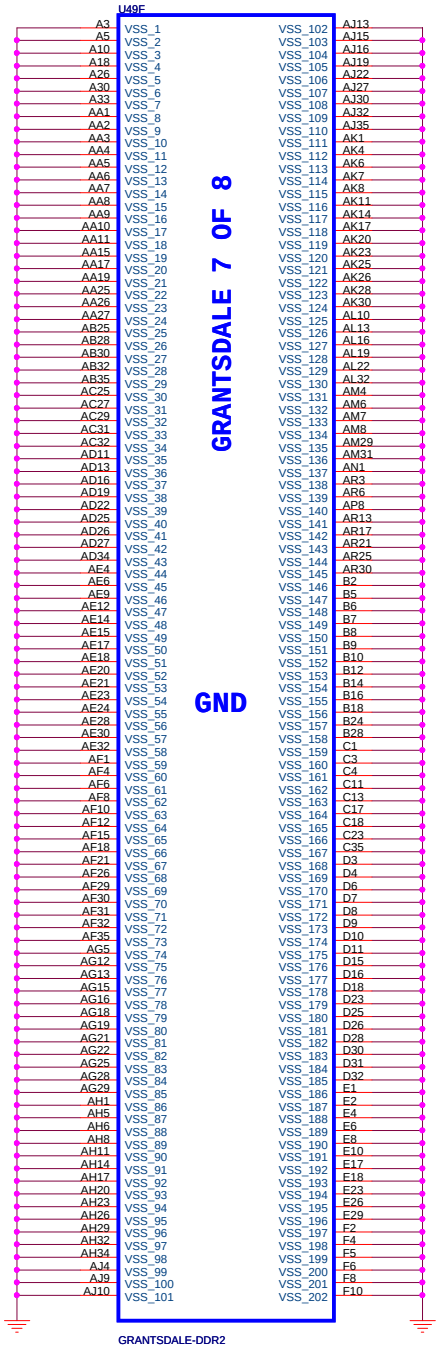

PROJECT : NT2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	GMCH(POWER/GND)-2	1A

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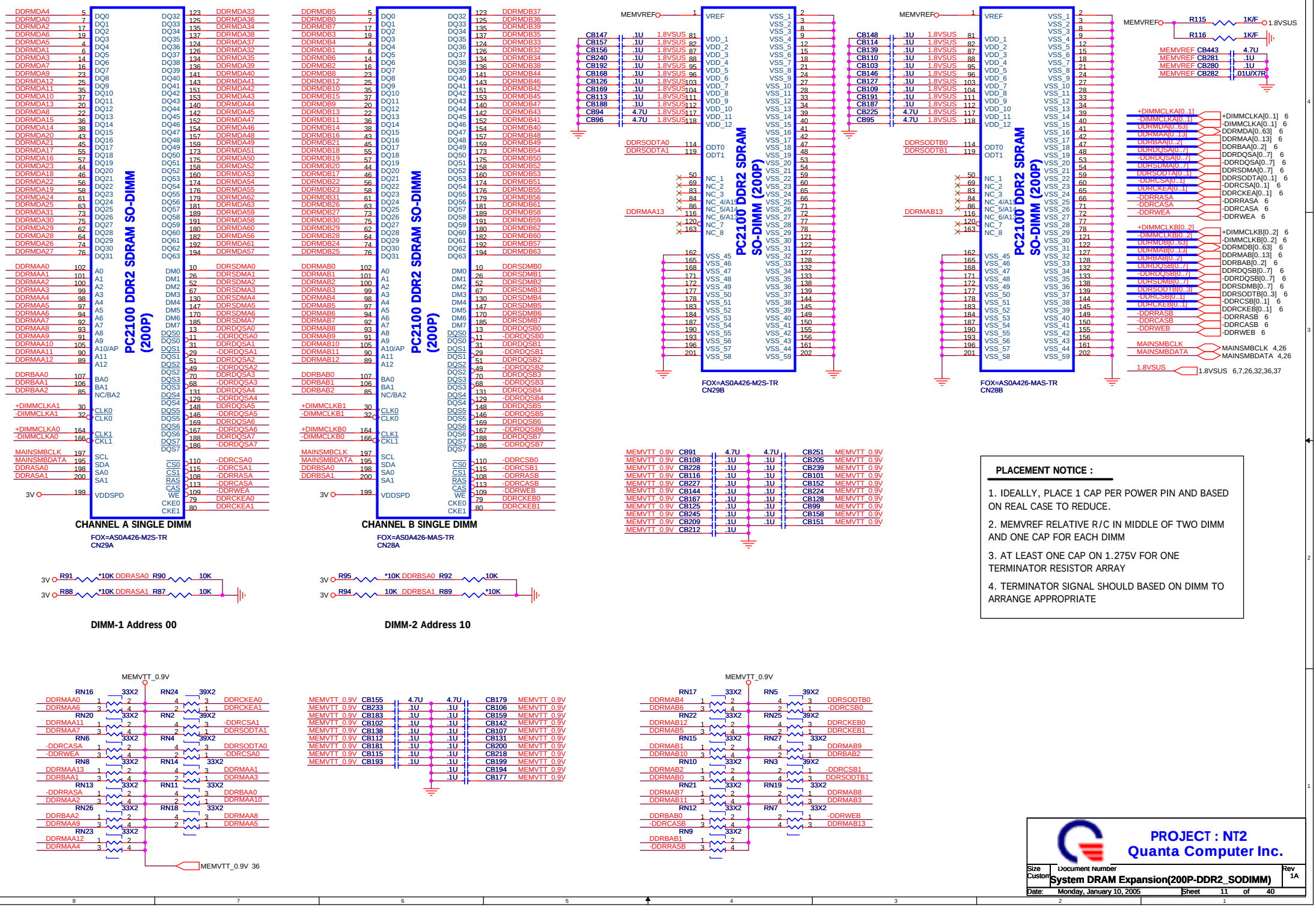
PC2100 DDR2 SDRAM SO-DIMM (200P)
CHANNEL A SINGLE DIMM
FOX=AS0A426-M2S-TR
CN29A
CHANNEL B SINGLE DIMM
FOX=AS0A426-MAS-TR
CN28A
PC2100 DDR2 SDRAM SO-DIMM (200P)
FOX=AS0A426-M2S-TR
CN29B
FOX=AS0A426-MAS-TR
CN28B
DIMM-1 Address 00
DIMM-2 Address 10
PLACEMENT NOTICE :
1. IDEALLY, PLACE 1 CAP PER POWER PIN AND BASED ON REAL CASE TO REDUCE.
2. MEMVREF RELATIVE R/C IN MIDDLE OF TWO DIMM AND ONE CAP FOR EACH DIMM
3. AT LEAST ONE CAP ON 1.275V FOR ONE TERMINATOR RESISTOR ARRAY
4. TERMINATOR SIGNAL SHOULD BASED ON DIMM TO ARRANGE APPROPRIATE
PROJECT : NT2
Quanta Computer Inc.
Size Custom
Document Number
System DRAM Expansion(200P-DDR2_SODIMM)
Rev 1A
Date: Monday, January 10, 2005
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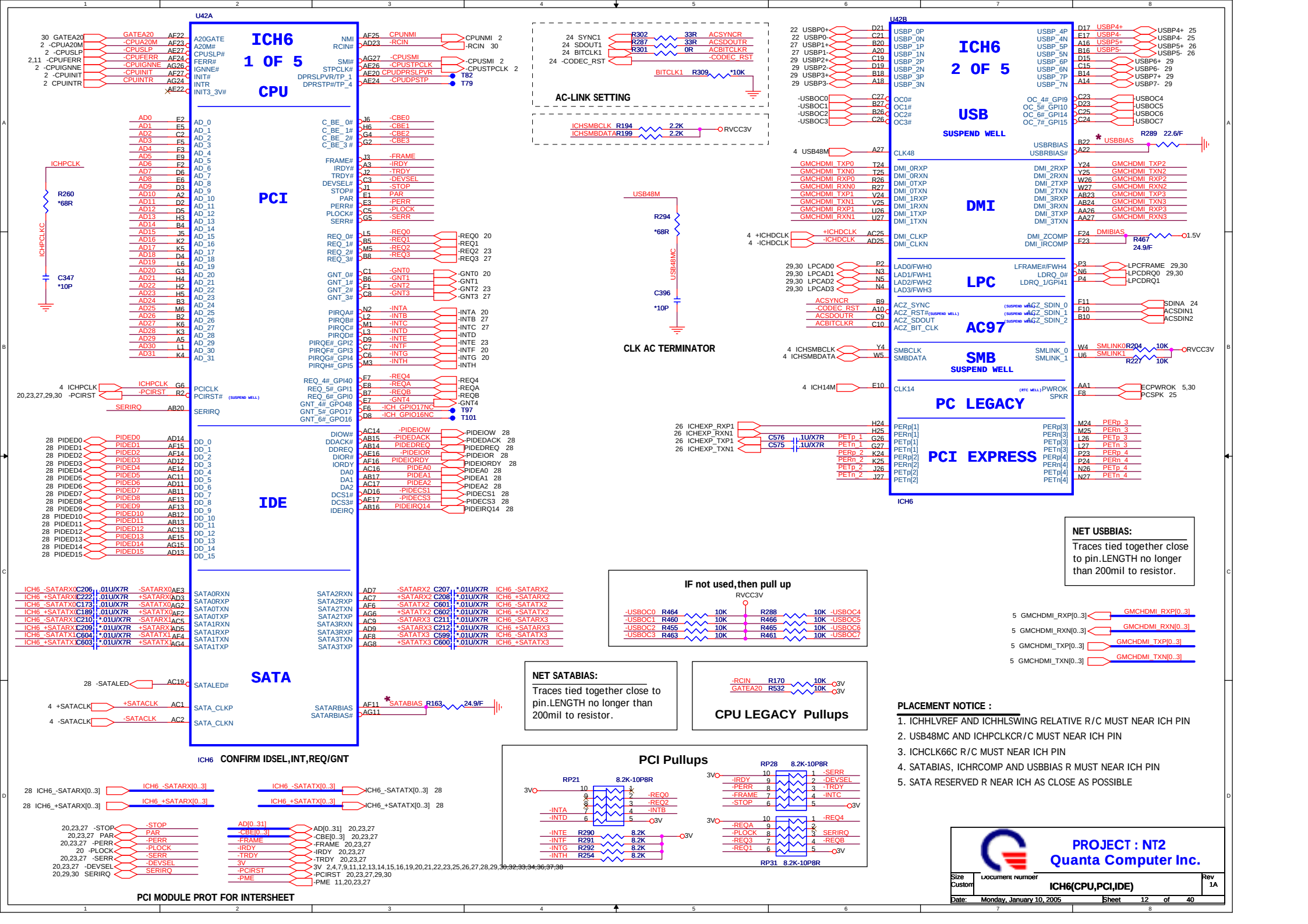
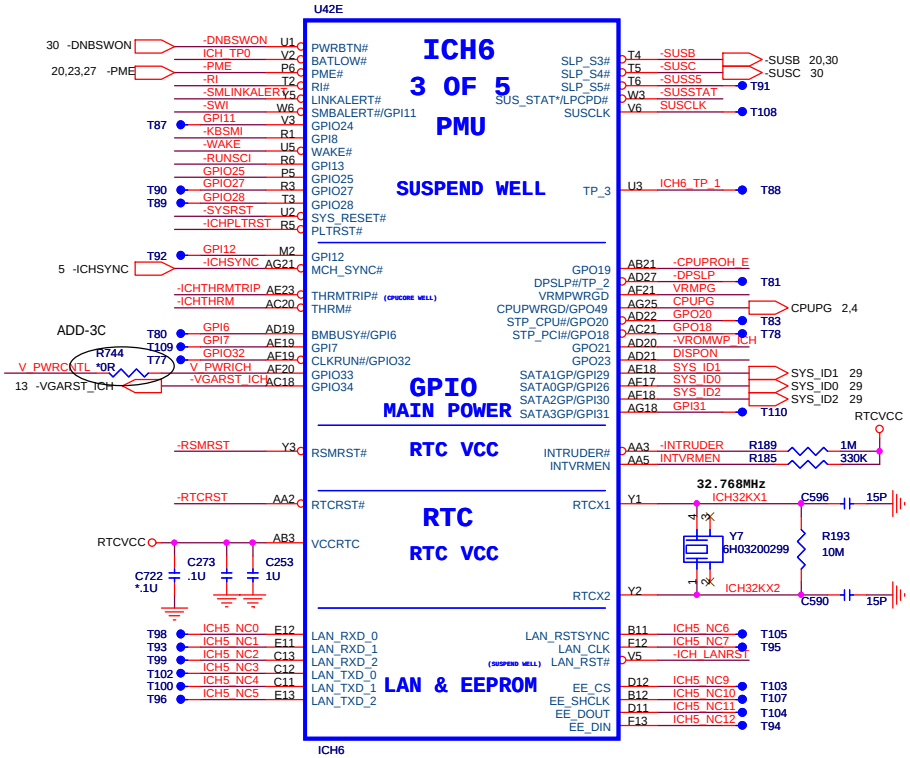

U42A
ICH6
1 OF 5
CPU
PCI
IDE
SATA
U42B
ICH6
2 OF 5
USB
SUSPEND WELL
DMI
LPC
AC97
SMB
SUSPEND WELL
PC LEGACY
PCI EXPRESS
ICH6
AC-LINK SETTING
CLK AC TERMINATOR
NET USBBIAS:
Traces tied together close to pin.LENGTH no longer than 200mil to resistor.
IF not used,then pull up
RVCC3V
NET SATABIAS:
Traces tied together close to pin.LENGTH no longer than 200mil to resistor.
CPU LEGACY Pullups
PCI Pullups
RP21 8.2K-10P8R
RP28 8.2K-10P8R
RP31 8.2K-10P8R
ICH6 CONFIRM IDSEL,INT,REQ/GNT
PCI MODULE PROT FOR INTERSHEET
PLACEMENT NOTICE :
1. ICHHLVREF AND ICHHLSWING RELATIVE R/C MUST NEAR ICH PIN
2. USB48MC AND ICHPCLKCR/C MUST NEAR ICH PIN
3. ICHCLK66C R/C MUST NEAR ICH PIN
4. SATABIAS, ICHRCOMP AND USBBIAS R MUST NEAR ICH PIN
5. SATA RESERVED R NEAR ICH AS CLOSE AS POSSIBLE
PROJECT : NT2
Quanta Computer Inc.
Size Custom
Document Number
ICH6(CPU,PCI,IDE)
Rev 1A
Date: Monday, January 10, 2005
Sheet 12 of 40

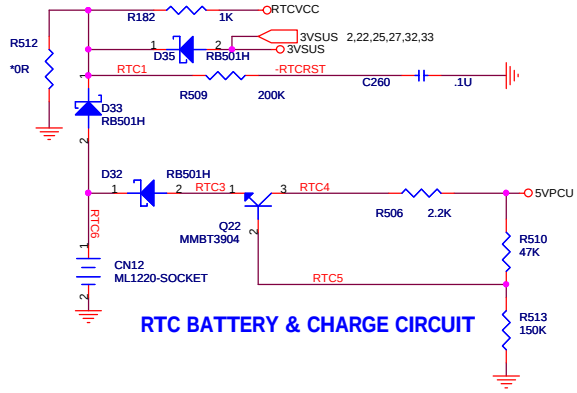
GPIO PIN DEFINE

GPI6		
GPI7		PULL UP
GPI8	-KBSMI	PULL UP
GPI11	-SWI	PULL UP
GPI12		PULL UP
GPI13	-RUNSCI	PULL UP
GPI26	SYS_ID0	PULL UP
GPI29	SYS_ID1	PULL LO
GPI30		PULL UP
GPI31		PULL UP
GPO18		SET OUTPUT
GPO19		SET OUTPUT
GPO20		SET OUTPUT
GPO21		SET OUTPUT
GPO23	DISPON	SET OUTPUT
GPIO24		SET OUTPUT
GPO49	CPUPG	SET OUTPUT
GPIO25		SET OUTPUT
GPIO27		SET OUTPUT
GPIO28		SET OUTPUT
GPIO32		SET OUTPUT
GPIO33		SET OUTPUT
GPIO34		SET OUTPUT

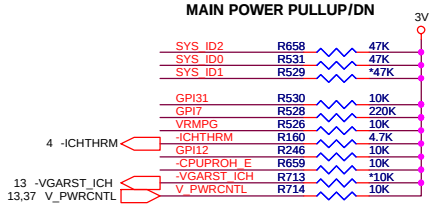
Functional Straps

GNT[6]#/ GPO[16]	**Top-Block Swap Override**
	Pull-Low : "top-block swap" mode
LINKALERT#	**Reserved**
	Requires an external pull-up resistor.
SPKR	**No Reboot**
	Pull-up : "No Reboot" mode
INTVRMEN	**Integrated VccSus1.5 VRM enable/disable**
	Pull-up : Enable integrated VccSus1.5V VRM
GPIO[25]	**Integrated Vcc2.5 VRM enable/disable**
	Pull-Low : Enable inegrated Vcc2.5 VRM
EE_CS	**Reserved**
	iternal pull-down & should not be pull-high
GNT[5]#/ GPO[17]	**Boot BIOS Desination Selection**
	This functionality for debug/testing only
EE_DOUT	**Reserved**
	iternal pull-up & should not be pull-low
ACZ_SDOUT	**XOR chain Entrance / PCI Express port config bit1**
	Pull-low : allows entrance to XOR Chain testing
ACZ_SYNC	**PCI Express Port Config bit 0**
	This signal has a weak internal pull-down
TP[1]	iternal pull-down & should not be pull-high
STATLED#	iternal pull-up & should not be pull-low
REQ[4:1]	**XOR Chain Selection / See Chapter 8**
TP[3]	**XOR Chain Entrance / See Chapter 8** This signal should not be Pull-low unless using XOR Chain testing

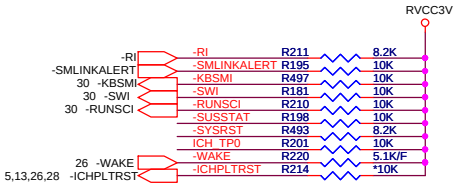




MAIN POWER PULLUP/DN



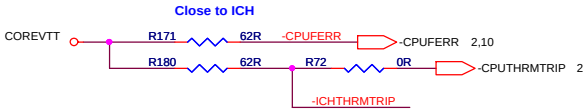
SUSPEND WELL PULLUP

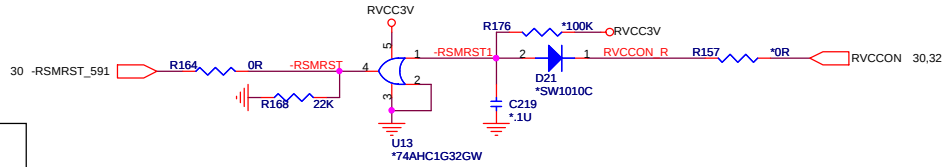


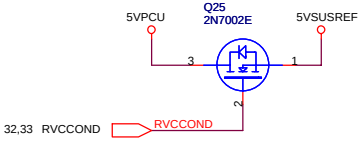
ASSUME S5 SUPPORT

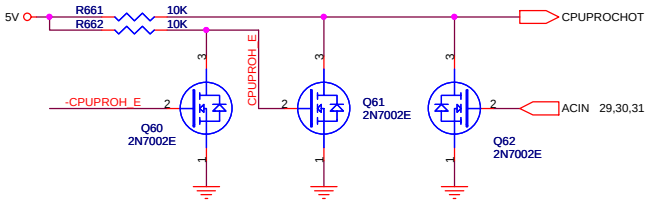
BOM Note-3C

ADD R744 CS00003J900









DESIGN CHECK LIST :

1. CLASSIFY THE POWER PLANE FOR PMU AND GPIO PIN
2. CLASSIFY GPI AND GPO PIN
3. COMMON PIN FOR PMU INPUT: -PME, BATLOW, -RI, -WAKESCI, RUNSCI, KBSMI AND -DNBSWON
4. USUALLY USED GPIO PIN : DISPON, CRTSENSE, SPKOFF
5. USUALLY USED CLK CONTRL PIN : -CPUSTP, -PCISTP, -SUSA AND -SUSSTAT
6. AGP PMU PIN : -AGPBUSY AND -STPAGP
7. CHECK -PCIRST BUFFERAND PWROK SIGNAL
8. CHECK -RSMRST CIRCUI

PLACEMENT NOTICE :

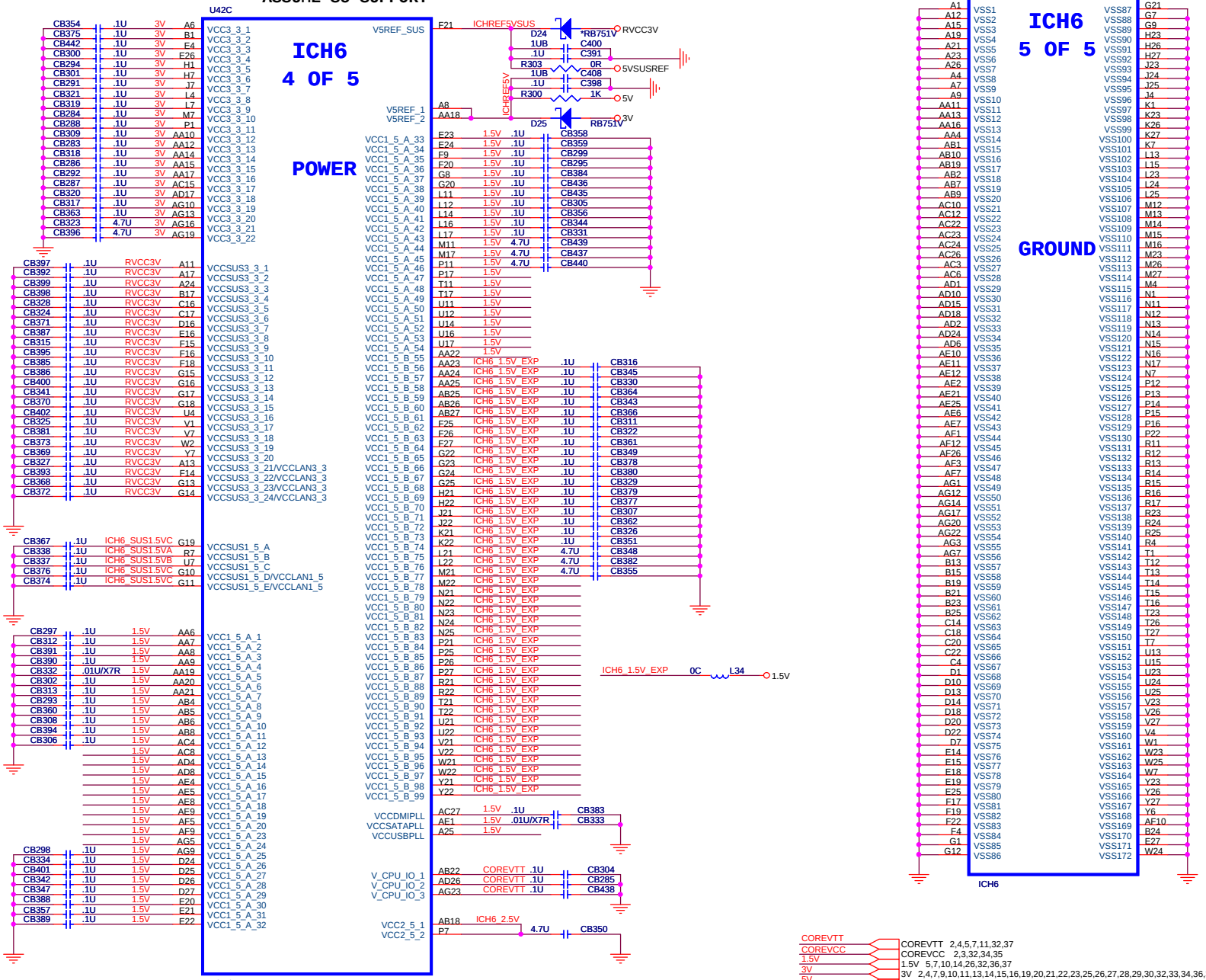
1. ONE BYPASS CAP FOR EACH ICH PIN IF POSSIBLE
2. RTC XTAL MUST NEAR ICH
3. PUT RTC BAT CIRCUIT AS A GROUP
4. REF5VSUS AND REF5V R/C/D NEAR ICH PIN

PROJECT : NT2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH6(GPIO/MISC)	3A

Date: Monday, January 10, 2005 Sheet 13 of 40

ASSUME S5 SUPPORT



COREVTT	COREVTT 2,4,5,7,11,32,37
COREVCC	COREVCC 2,3,32,34,35
1.5V	1.5V 5,7,10,14,26,32,36,37
3V	3V 2,4,7,9,10,11,13,14,15,16,19,20,21,22,23,25,26,27,28,29,30,32,33,34,36,37,38
5V	5V 4,11,19,21,25,26,27,28,29,30,32,33,34,35,37
RVCC1.5V	RVCC1.5V
3VSUS	3VSUS 2,11,22,25,27,32,33
5VSUS	5VSUS 27,29,30,32,33,37,38
RVCC3V	RVCC3V 4,10,11,26,30,32,33

DEFINE AS S5 SUPPORT INITIALLY.

PROJECT : NT2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH6(POWER/GND)	2A

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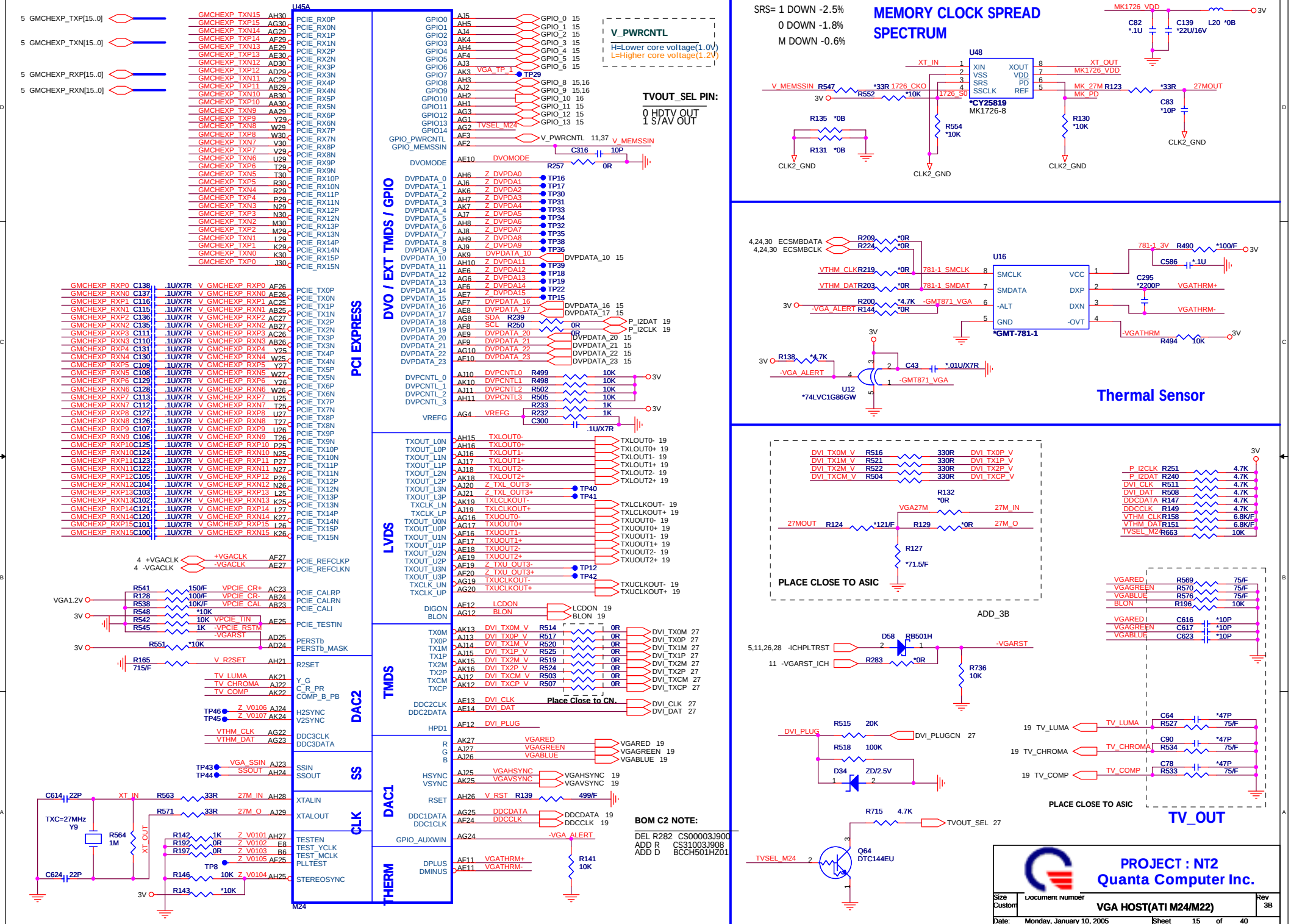
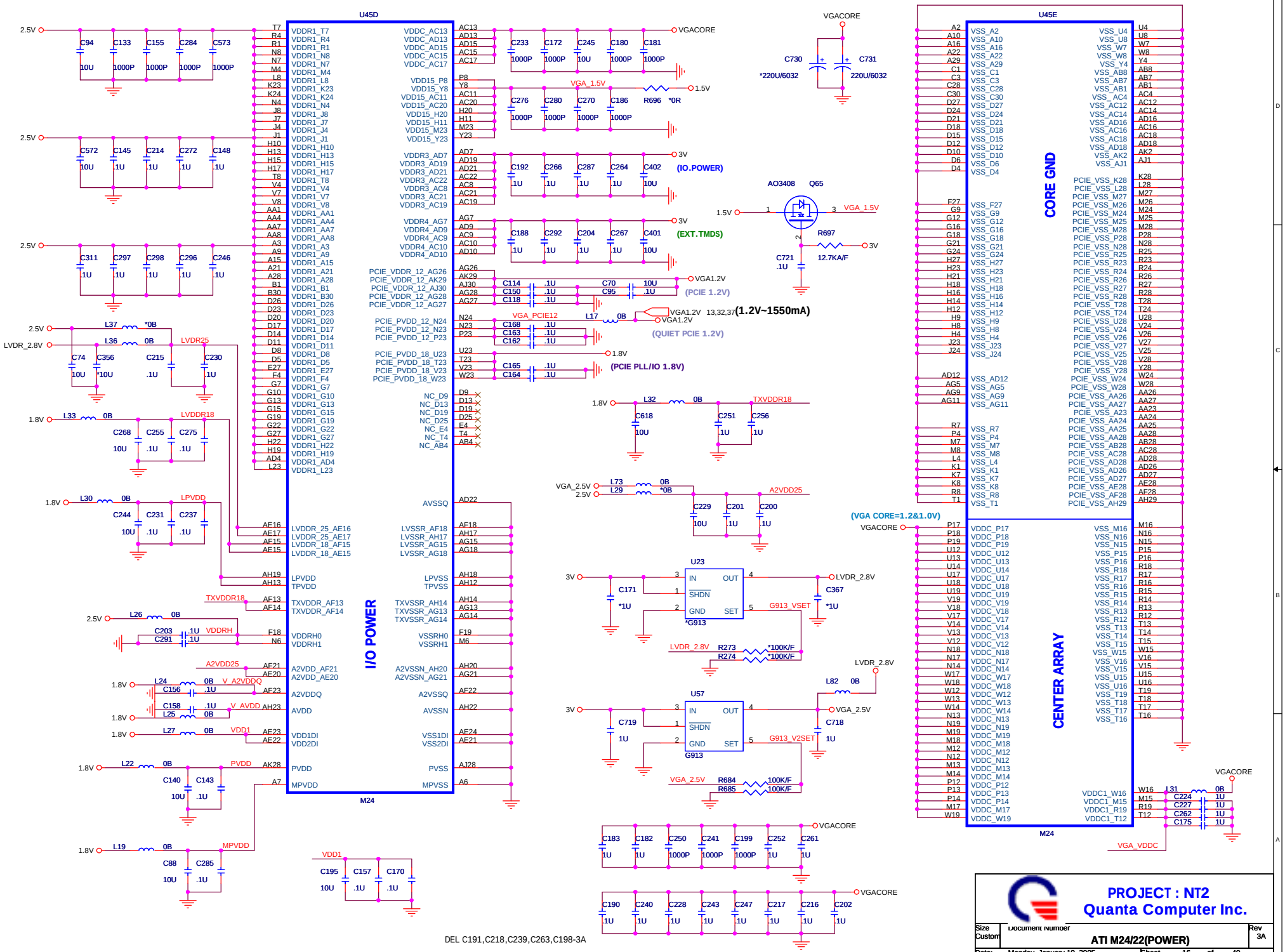
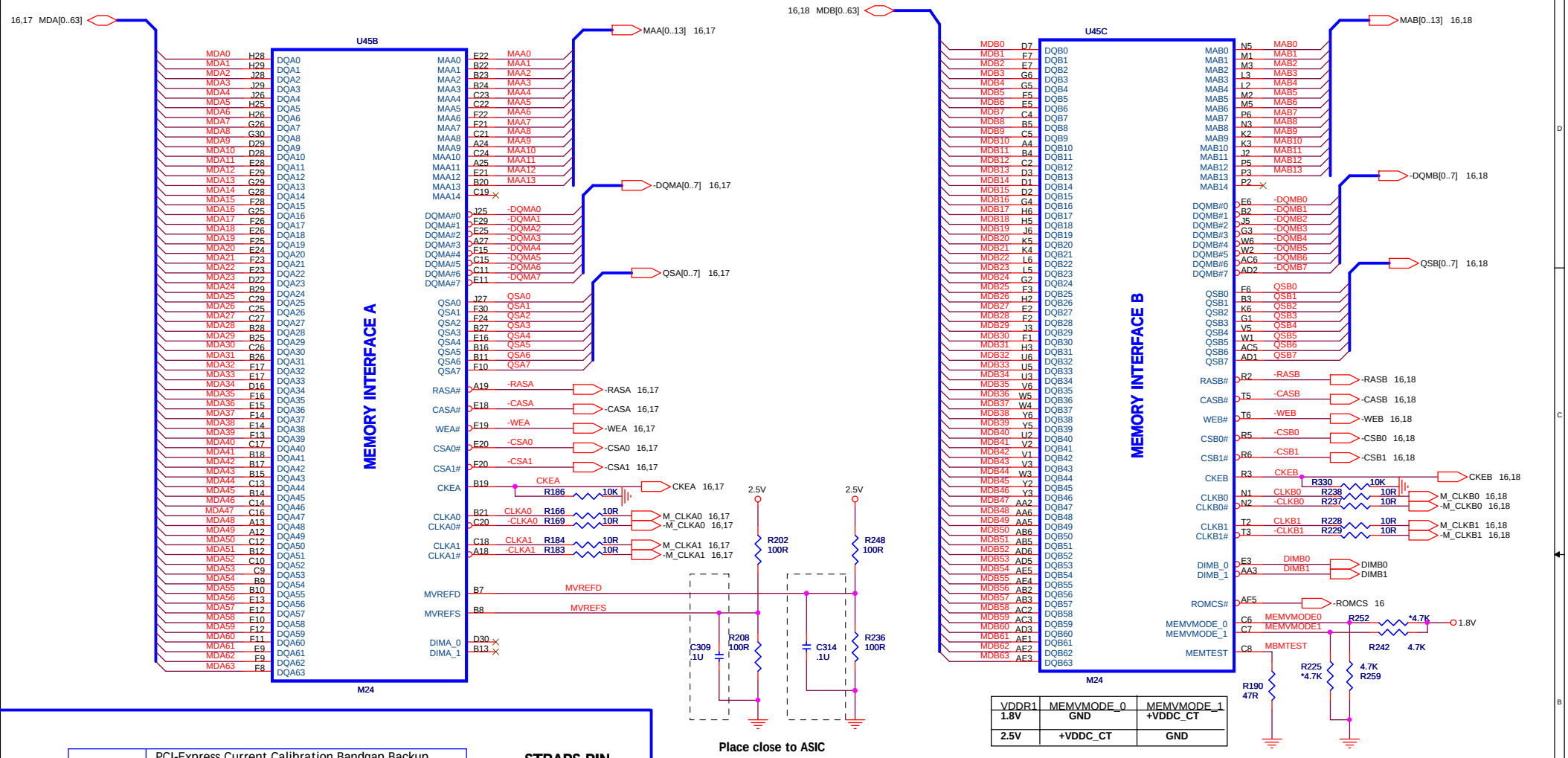

U45A
PCI EXPRESS
DVO / EXT TMDS / GPIO
LVDS
TMDS
DAC2
SS
CLK
DAC1
THERM
M24
V_PWRCNTL
H=Lower core voltage(1.0V)
L=Higher core voltage(1.2V)
TVOUT_SEL PIN:
0 HDTV OUT
1 S/AV OUT
BOM C2 NOTE:
DEL R282 CS00003J900
ADD R CS31003J908
ADD D BCCH501HZ01
SRS= 1 DOWN -2.5%
0 DOWN -1.8%
M DOWN -0.6%
MEMORY CLOCK SPREAD SPECTRUM
U48
*CY25819
MK1726-8
U16
*GMT-781-1
U12
*74LVC1G86GW
Thermal Sensor
PLACE CLOSE TO ASIC
ADD_3B
Place Close to CN.
Q64
DTC144EU
TV_OUT
PROJECT : NT2
Quanta Computer Inc.
VGA HOST(ATI M24/M22)
Size Custom
Document Number
Rev 3B
Date: Monday, January 10, 2005
Sheet 15 of 40


U45D
I/O POWER
M24
U45E
CORE GND
CENTER ARRAY
M24
U23
U57
VGACORE
1.5V
3V
(IO.POWER)
(EXT.TMDS)
VGA1.2V
(PCIE 1.2V)
(QUIET PCIE 1.2V)
1.8V
(PCIE PLL/IO 1.8V)
AO3408 Q65
R697
12.7KA/F
(1.2V~1550mA)
(VGA CORE=1.2&1.0V)
LVDR_2.8V
VGA_2.5V
VGA_VDDC
DEL C191,C218,C239,C263,C198-3A
PROJECT : NT2
Quanta Computer Inc.
Size Custom
Document Number
ATI M24/22(POWER)
Rev 3A
Date: Monday, January 10, 2005
Sheet 16 of 40

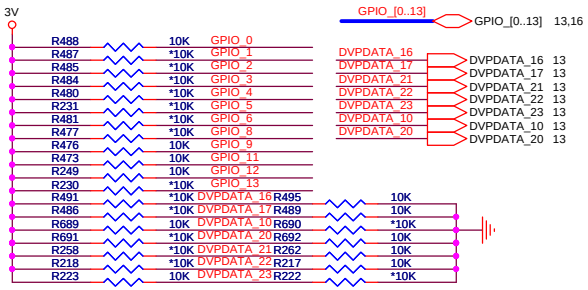


VDDR1	MEMVMODE_0	MEMVMODE_1
1.8V	GND	+VDDC_CT
2.5V	+VDDC_CT	GND

STRAPS PIN

GPIO_0	PCI-Express Current Calibration Bandgap Backup
	0: use reference voltage from Bandgap
	1: use reference voltage from resistor divider
GPIO_1	PCI-Express PLL Calibration force enable
	0: Disable PLL force calibration
	1: Enable PLL force calibration
GPIO_(3,2)	**00: PCI Express 1.0 mode**
	01: RESERVED
	10: PCI Express 1.0 mode
	11: RESERVED
GPIO_4	Pin strap called Reversed_Lanes
	0: Non-reversed
	1:Reversed PCIe layouts
GPIO_5	Bypass PCI-Express PLL
GPIO_6	PCI-Express transmitter current compensation
	0: Normal
	1: Inject extra current for output buffer switching

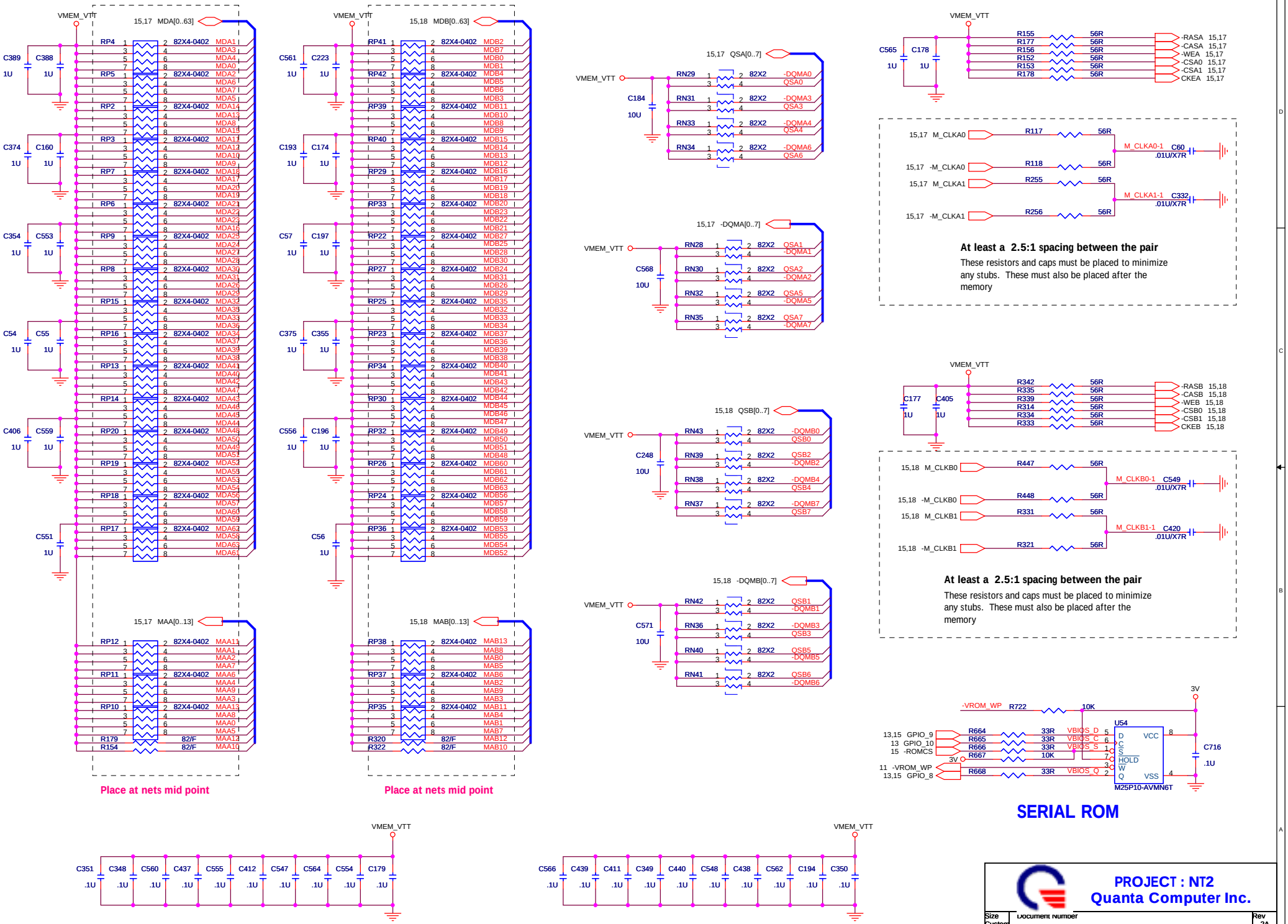
GPIO_8	Strap to set the debug muxes to bting out DEBUG signals even if registers are inaccessible
GPIO(9,13:11)	ROMIDCFG
INT P/D	0x0x: No ROM, CHG_ID=0 0x1x: No Rom, CHG_ID=1 **1011 - Serial M25P10 ROM (ST), chip IDis from ROM** 1100 - Serial M25P05 ROM (ST), chip IDis from ROM
DVPDATA_10, 20,21~23	DATA23 Vendor; DATA22 Voltage; DATA21 CS; DATA20 MEM SIZE; DATA10 MEM TYPE
MEM TYPE	X X X X 0 4MX32 X X X X 1 8MX32 X X X 0 X 128M(M22), 256M(M24) X X X 1 X 64M(M22),128M(M24) X X 0 X X CS x1 X X 1 X X CS x2 X 0 X X X 1.8V X 1 X X X 2.5V 0 X X X X Hynix 1 X X X X Samsung M24-256M 10001 M24-128M 01010 M22-64M 01010

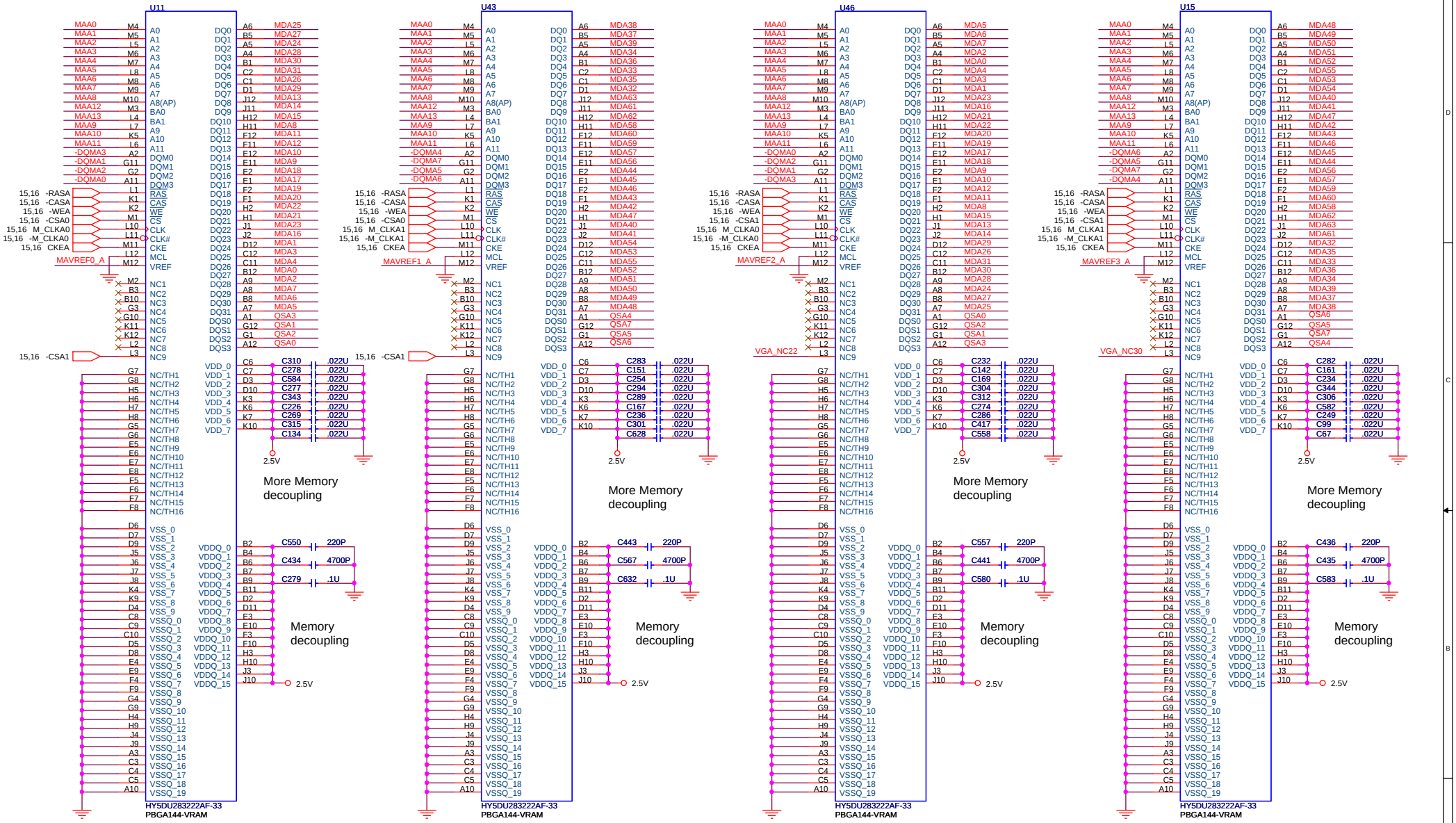


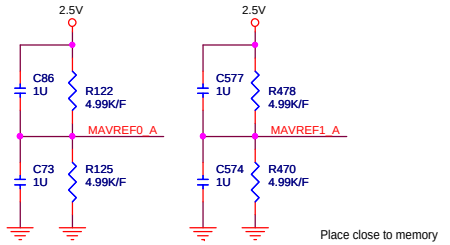
PROJECT : NT2
Quanta Computer Inc.

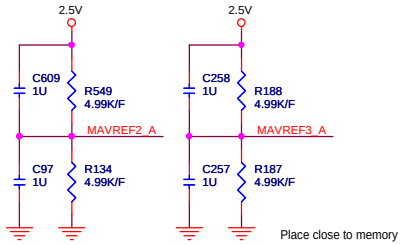
Size	Document Number	Rev
Custom	ATI M24/22 MEM/STRAPS PIN	3A

Date: Monday, January 10, 2005 Sheet 17 of 40


VMEM_VTT
15,17 MDA[0..63]
15,18 MDB[0..63]
15,17 MAA[0..13]
15,18 MAB[0..13]
82X4-0402
82/F
Place at nets mid point
Place at nets mid point
15,17 QSA[0..7]
15,17 -DQMA[0..7]
15,18 QSB[0..7]
15,18 -DQMB[0..7]
82X2
-RASA 15,17
-CASA 15,17
-WEA 15,17
-CSA0 15,17
-CSA1 15,17
CKEA 15,17
15,17 M_CLKA0
15,17 -M_CLKA0
15,17 M_CLKA1
15,17 -M_CLKA1
M_CLKA0-1 C60 .01U/X7R
M_CLKA1-1 C332 .01U/X7R
At least a 2.5:1 spacing between the pair
These resistors and caps must be placed to minimize any stubs. These must also be placed after the memory
-RASB 15,18
-CASB 15,18
-WEB 15,18
-CSB0 15,18
-CSB1 15,18
CKEB 15,18
15,18 M_CLKB0
15,18 -M_CLKB0
15,18 M_CLKB1
15,18 -M_CLKB1
M_CLKB0-1 C549 .01U/X7R
M_CLKB1-1 C420 .01U/X7R
At least a 2.5:1 spacing between the pair
These resistors and caps must be placed to minimize any stubs. These must also be placed after the memory
3V
-VROM_WP R722 10K
13,15 GPIO_9
13 GPIO_10
15 -ROMCS
11 -VROM_WP
13,15 GPIO_8
VBIOS_D
VBIOS_C
VBIOS_S
VBIOS_Q
U54
VCC
HOLD
VSS
M25P10-AVMN6T
C716 .1U
SERIAL ROM
PROJECT : NT2
Quanta Computer Inc.
Size Custom
Document Number
MEM TERMINATION & VGA ROM
Rev 2A
Date: Monday, January 10, 2005
Sheet 18 of 40







VGA DDR MEMORY A

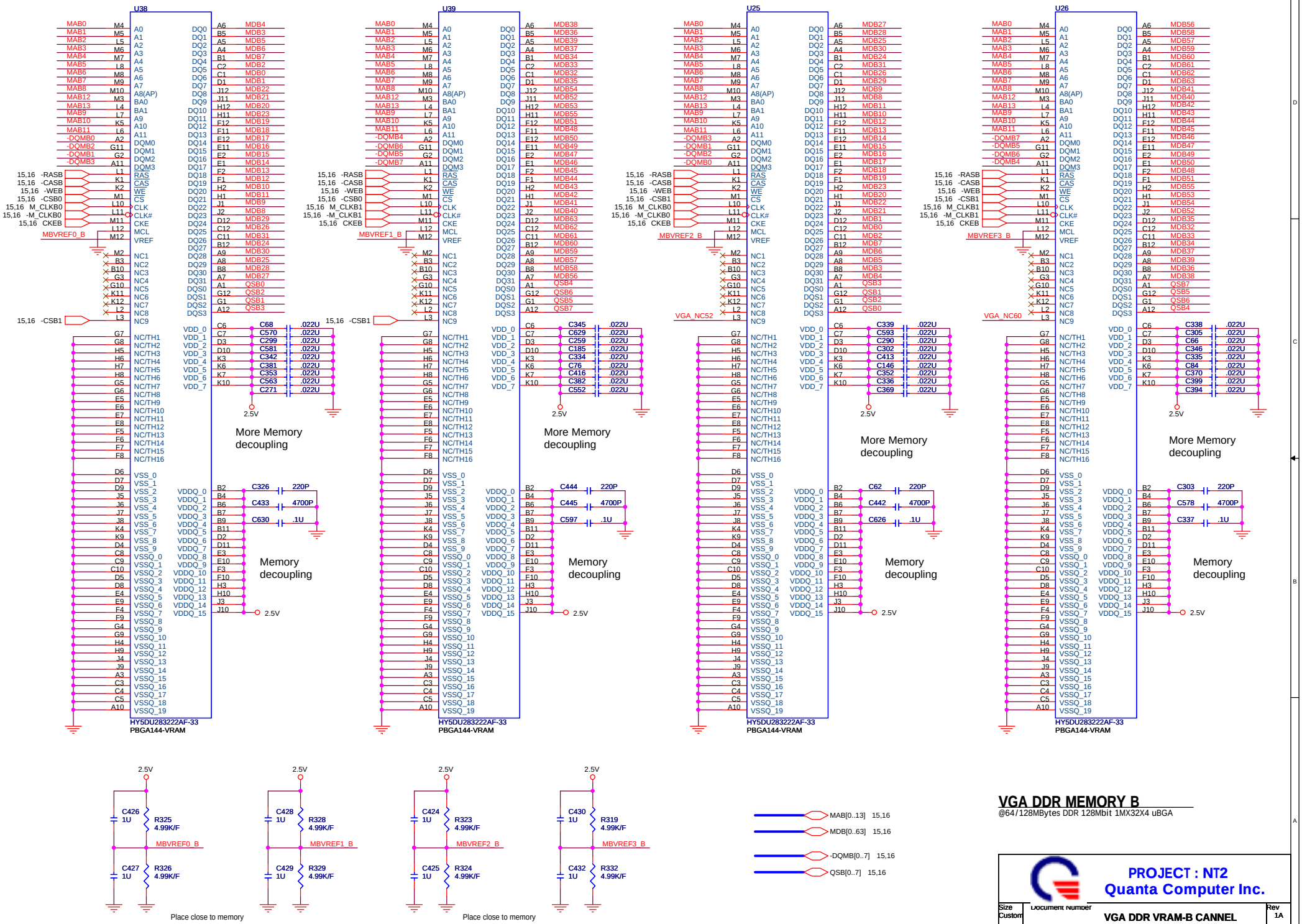
@64/128MBytes DDR 128Mbit 1MX32X4 uBGA

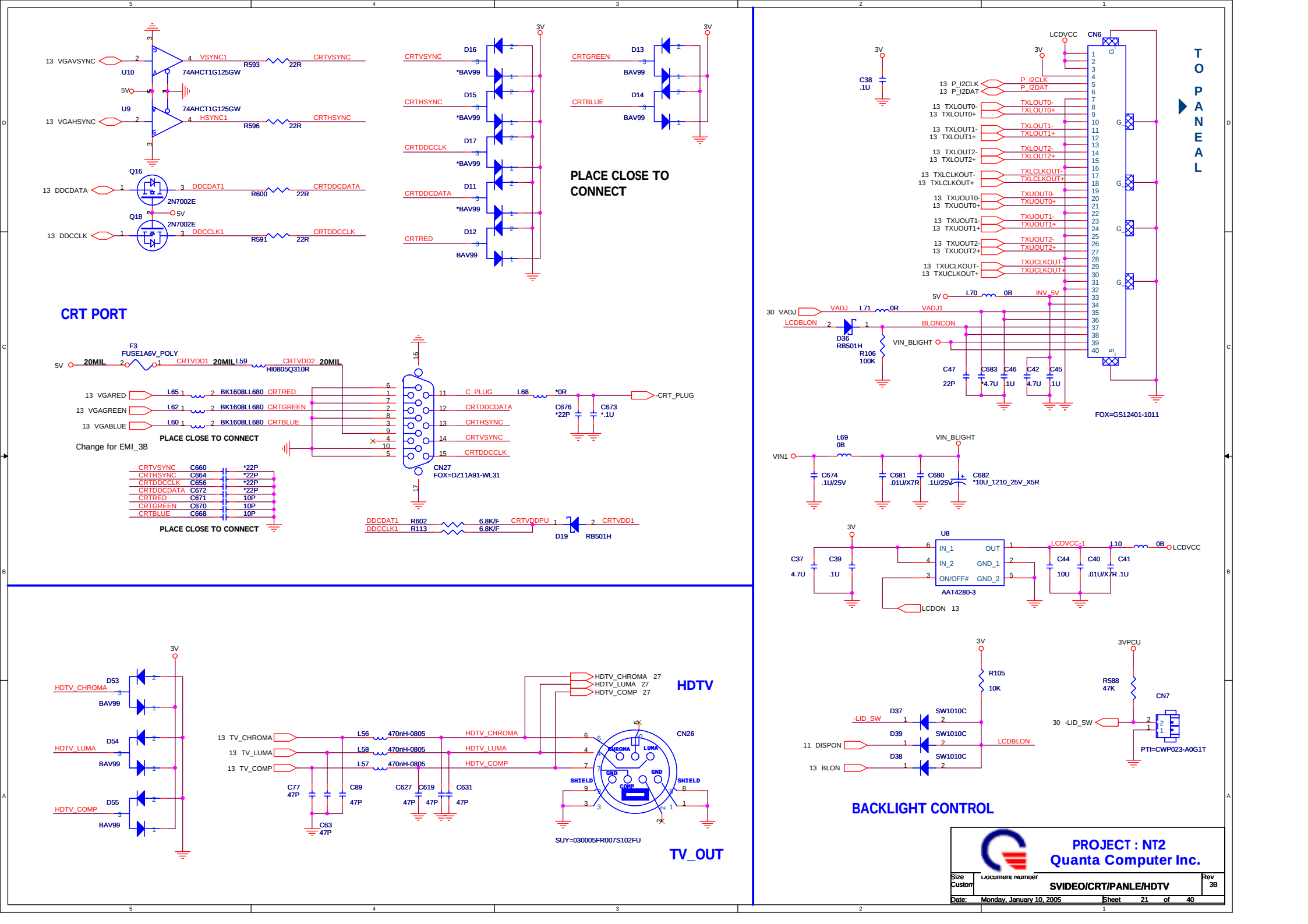
MAA[0..13] 15,16
MDA[0..63] 15,16
-DQMA[0..7] 15,16
QSA[0..7] 15,16

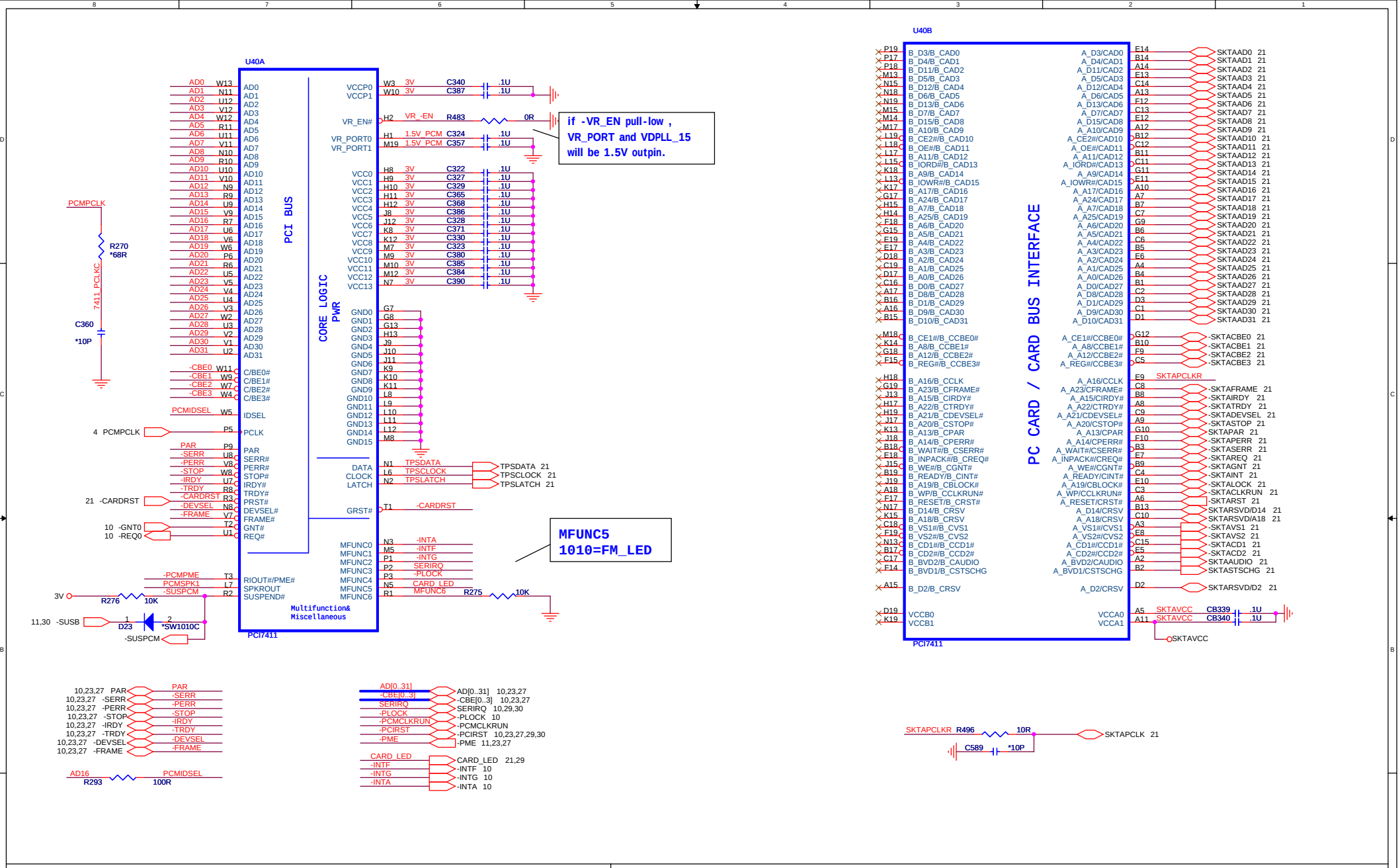
PROJECT : NT2
Quanta Computer Inc.

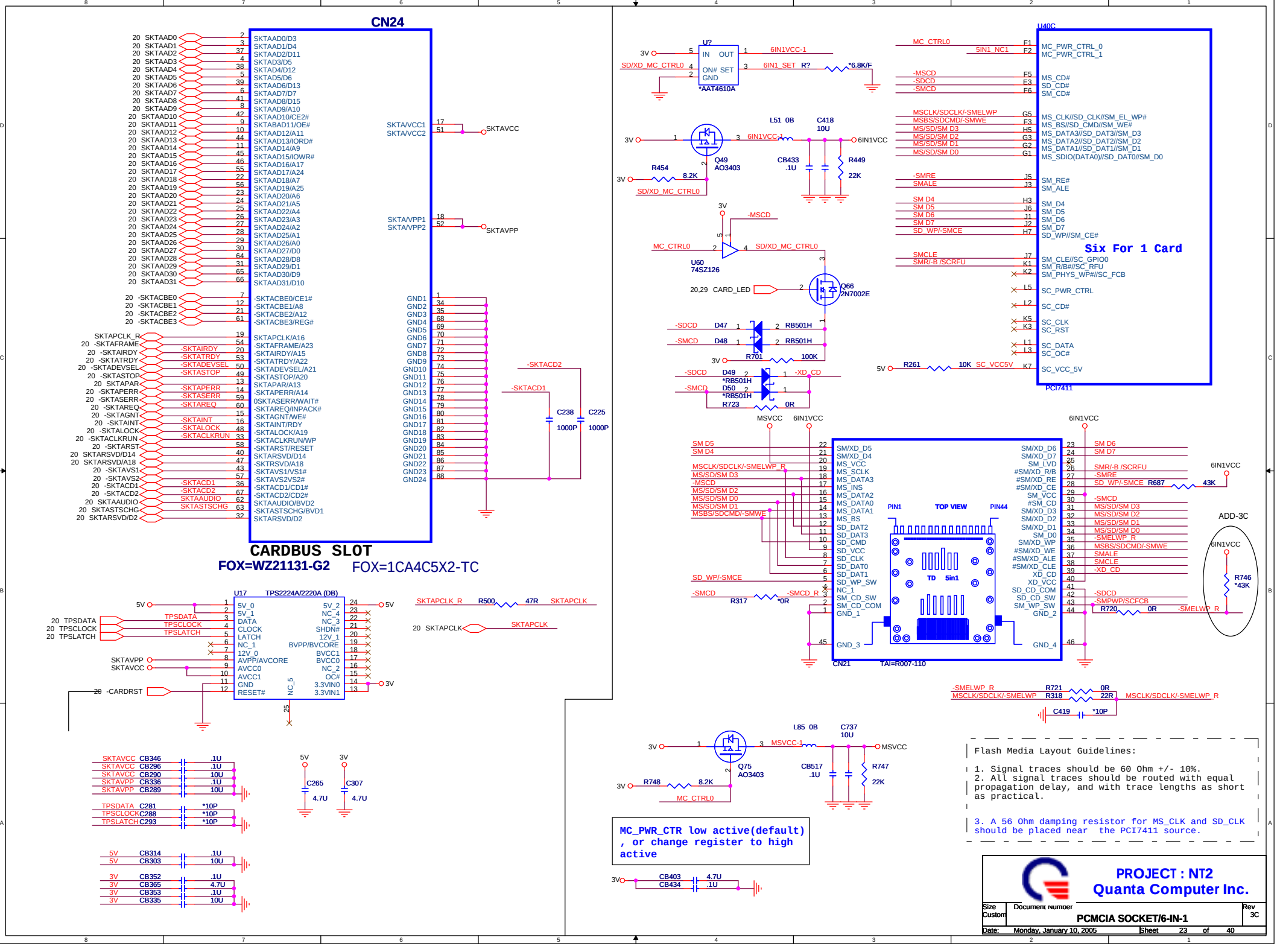
Size	Document Number	Rev
Custom	VGA DDR VRAM-A CANNEL	1A

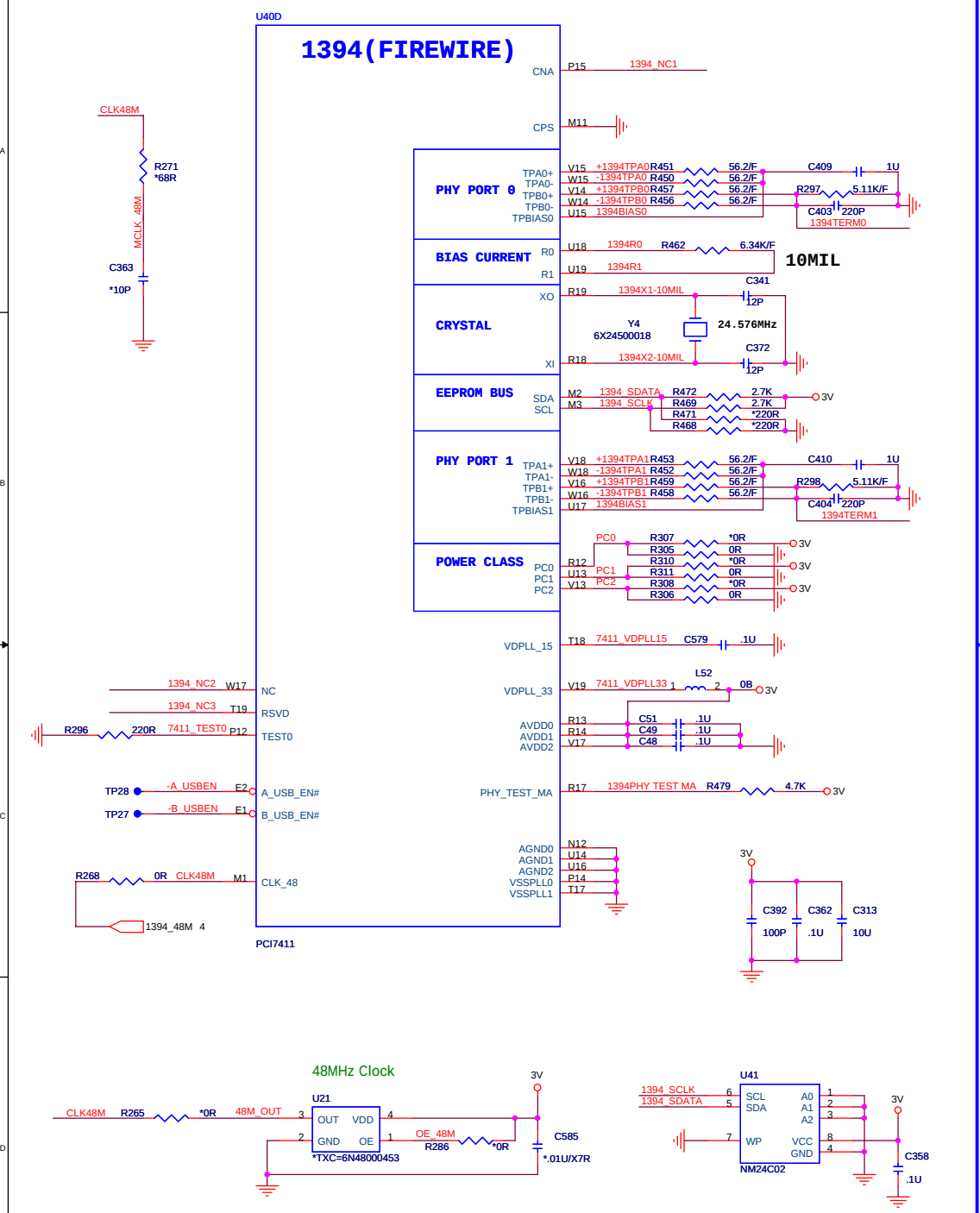
Date: Monday, January 10, 2005 Sheet 19 of 40

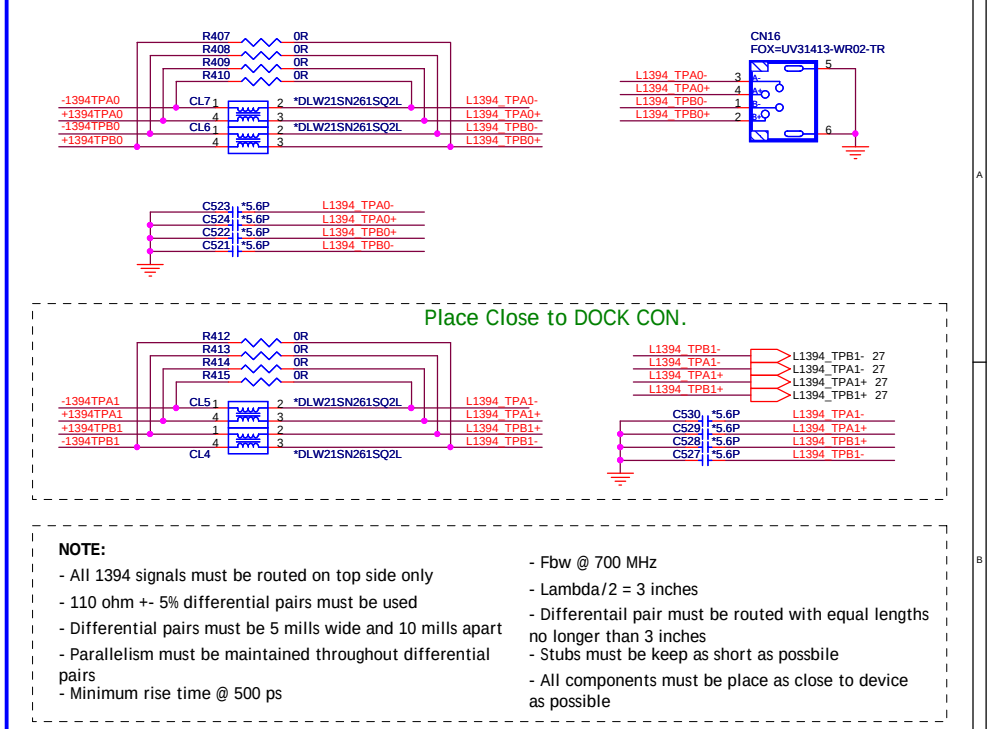

U38
U39
U25
U26
HY5DU283222AF-33
PBGA144-VRAM
More Memory decoupling
Memory decoupling
2.5V
MBVREF0_B
MBVREF1_B
MBVREF2_B
MBVREF3_B
VGA_NC52
VGA_NC60
15,16 -RASB
15,16 -CASB
15,16 -WEB
15,16 -CSB0
15,16 -CSB1
15,16 M_CLKB0
15,16 M_CLKB1
15,16 -M_CLKB0
15,16 CKEB
15,16 -CSB1
C426 1U
R325 4.99K/F
C427 1U
R326 4.99K/F
C428 1U
R328 4.99K/F
C429 1U
R329 4.99K/F
C424 1U
R323 4.99K/F
C425 1U
R324 4.99K/F
C430 1U
R319 4.99K/F
C432 1U
R332 4.99K/F
Place close to memory
MAB[0..13] 15,16
MDB[0..63] 15,16
-DQMB[0..7] 15,16
QSB[0..7] 15,16
VGA DDR MEMORY B
@64/128MBytes DDR 128Mbit 1MX32X4 uBGA
PROJECT : NT2
Quanta Computer Inc.
Size Custom
Document Number
VGA DDR VRAM-B CANNEL
Rev 1A
Date: Monday, January 10, 2005
Sheet 20 of 40


CRT PORT
13 VGAVSYNC
U10
74AHCT1G125GW
VSYNC1
R593
22R
CRTVSYNC
U9
74AHCT1G125GW
13 VGAHSYNC
HSYNC1
R596
22R
CRTHSYNC
Q16
13 DDCDATA
2N7002E
DDCDAT1
R600
22R
CRTDDCDATA
Q18
2N7002E
13 DDCCLK
DDCCLK1
R591
22R
CRTDDCCLK
D16
CRTVSYNC
*BAV99
D15
CRTHSYNC
*BAV99
D17
CRTDDCCLK
*BAV99
D11
CRTDDCDATA
*BAV99
D12
CRTRED
BAV99
D13
CRTGREEN
BAV99
D14
CRTBLUE
BAV99
PLACE CLOSE TO CONNECT
F3
FUSE1A6V_POLY
20MIL
CRTVDD1
L59
HI0805Q310R
CRTVDD2
L65
BK1608LL680
CRTRED
L62
CRTGREEN
L60
CRTBLUE
13 VGARED
13 VGAGREEN
13 VGABLUE
PLACE CLOSE TO CONNECT
Change for EMI_3B
CN27
FOX=DZ11A91-WL31
C_PLUG
L68
*0R
C676
*22P
C673
*.1U
CRT_PLUG
CRTVSYNC C660 *22P
CRTHSYNC C664 *22P
CRTDDCCLK C656 *22P
CRTDDCDATA C672 *22P
CRTRED C671 10P
CRTGREEN C670 10P
CRTBLUE C668 10P
PLACE CLOSE TO CONNECT
DDCDAT1 R602 6.8K/F
DDCCLK1 R113 6.8K/F
CRTVDDPU
D19
RB501H
CRTVDD1
TO PANEL
LCDVCC
CN6
C38
.1U
13 P_I2CLK
13 P_I2DAT
13 TXLOUT0-
13 TXLOUT0+
13 TXLOUT1-
13 TXLOUT1+
13 TXLOUT2-
13 TXLOUT2+
13 TXLCLKOUT-
13 TXLCLKOUT+
13 TXUOUT0-
13 TXUOUT0+
13 TXUOUT1-
13 TXUOUT1+
13 TXUOUT2-
13 TXUOUT2+
13 TXUCLKOUT-
13 TXUCLKOUT+
L70
0B
INV_5V
30 VADJ
VADJ
L71
0R
VADJ1
LCDBLON
BLONCON
D36
RB501H
R106
100K
VIN_BLIGHT
C47
22P
C683
*4.7U
C46
.1U
C42
4.7U
C45
.1U
FOX=GS12401-1011
L69
0B
VIN1
C674
.1U/25V
C681
.01U/X7R
C680
.1U/25V
C682
*10U_1210_25V_X5R
U8
IN_1
OUT
IN_2
GND_1
ON/OFF#
GND_2
AAT4280-3
C37
4.7U
C39
.1U
LCDVCC-1
L10
0B
LCDVCC
C44
10U
C40
.01U/X7R
C41
.1U
LCDON 13
R105
10K
D37
SW1010C
-LID_SW
D39
SW1010C
11 DISPON
LCDBLON
D38
SW1010C
13 BLON
R588
47K
CN7
30 -LID_SW
PTI=CWP023-A0G1T
BACKLIGHT CONTROL
HDTV
D53
HDTV_CHROMA
BAV99
D54
HDTV_LUMA
BAV99
D55
HDTV_COMP
BAV99
13 TV_CHROMA
13 TV_LUMA
13 TV_COMP
L56
470nH-0805
L58
470nH-0805
L57
470nH-0805
HDTV_CHROMA
HDTV_LUMA
HDTV_COMP
C77
47P
C89
47P
C63
47P
C627
47P
C619
47P
C631
47P
HDTV_CHROMA 27
HDTV_LUMA 27
HDTV_COMP 27
CN26
CHROMA
LUMA
GND
COMP
SHIELD
SUY=030005FR007S102FU
TV_OUT
PROJECT : NT2
Quanta Computer Inc.
Size Custom
Document Number
SVIDEO/CRT/PANLE/HDTV
Rev 3B
Date: Monday, January 10, 2005
Sheet 21 of 40


U40A
PCI BUS
CORE LOGIC
PWR
PCI7411
Multifunction&
Miscellaneous
if -VR_EN pull-low ,
VR_PORT and VDPLL_15
will be 1.5V outpin.
MFUNC5
1010=FM_LED
U40B
PC CARD / CARD BUS INTERFACE
PCI7411
PCMPCLK
R270
*68R
7411 PCLKC
C360
*10P
R276
10K
D23
*SW1010C
-SUSPCM
-SUSB
R293
100R
R275
10K
R483
0R
C324
C357
C322
C327
C329
C365
C368
C386
C328
C371
C330
C323
C380
C385
C384
C390
C340
C387
TPSDATA
TPSCLOCK
TPSLATCH
-CARDRST
-INTA
-INTF
-INTG
SERIRQ
-PLOCK
CARD_LED
MFUNC6
SKTAVCC
CB339
CB340
SKTAPCLK
R496
10R
C589
*10P
AD[0..31]
-CBE[0..3]
-PCMCLKRUN
-PCIRST
-PME
PAR
-SERR
-PERR
-STOP
-IRDY
-TRDY
-DEVSEL
-FRAME
AD16
PCMIDSEL
-PCIRST
R285
0R
-CARDRST
R284
*0R
-PCMPME
Q27
DTC144EU
R295
10K
PCMSPK1
D31
SW1010C
PCMSPK
R475
*10K
R474
10K
PROJECT : NT2
Quanta Computer Inc.
Size
Custom
Document Number
PCMCIA T7411
Rev
3B
Date: Monday, January 10, 2005
Sheet 22 of 40

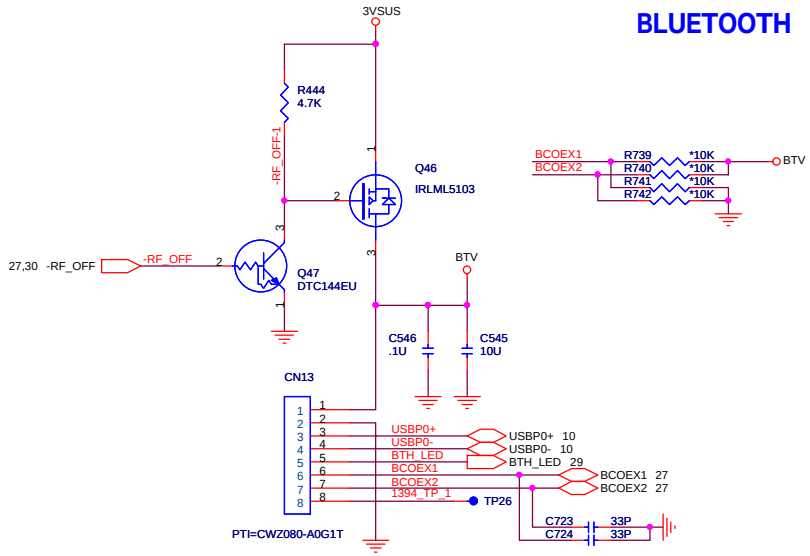

CN24
CARDBUS SLOT
FOX=WZ21131-G2
FOX=1CA4C5X2-TC
U40C
Six For 1 Card
PCI7411
U2
*AAT4610A
Q49
AO3403
U60
74SZ126
Q66
2N7002E
CN21
TAI=R007-110
TOP VIEW
TD 5in1
ADD-3C
U17
TPS2224A/2220A (DB)
Q75
AO3403
MC_PWR_CTR low active(default) , or change register to high active
Flash Media Layout Guidelines:
1. Signal traces should be 60 Ohm +/- 10%.
2. All signal traces should be routed with equal propagation delay, and with trace lengths as short as practical.
3. A 56 Ohm damping resistor for MS_CLK and SD_CLK should be placed near the PCI7411 source.
PROJECT : NT2
Quanta Computer Inc.
Size Custom
Document Number
PCMCIA SOCKET/6-IN-1
Rev 3C
Date: Monday, January 10, 2005
Sheet 23 of 40





NOTE:

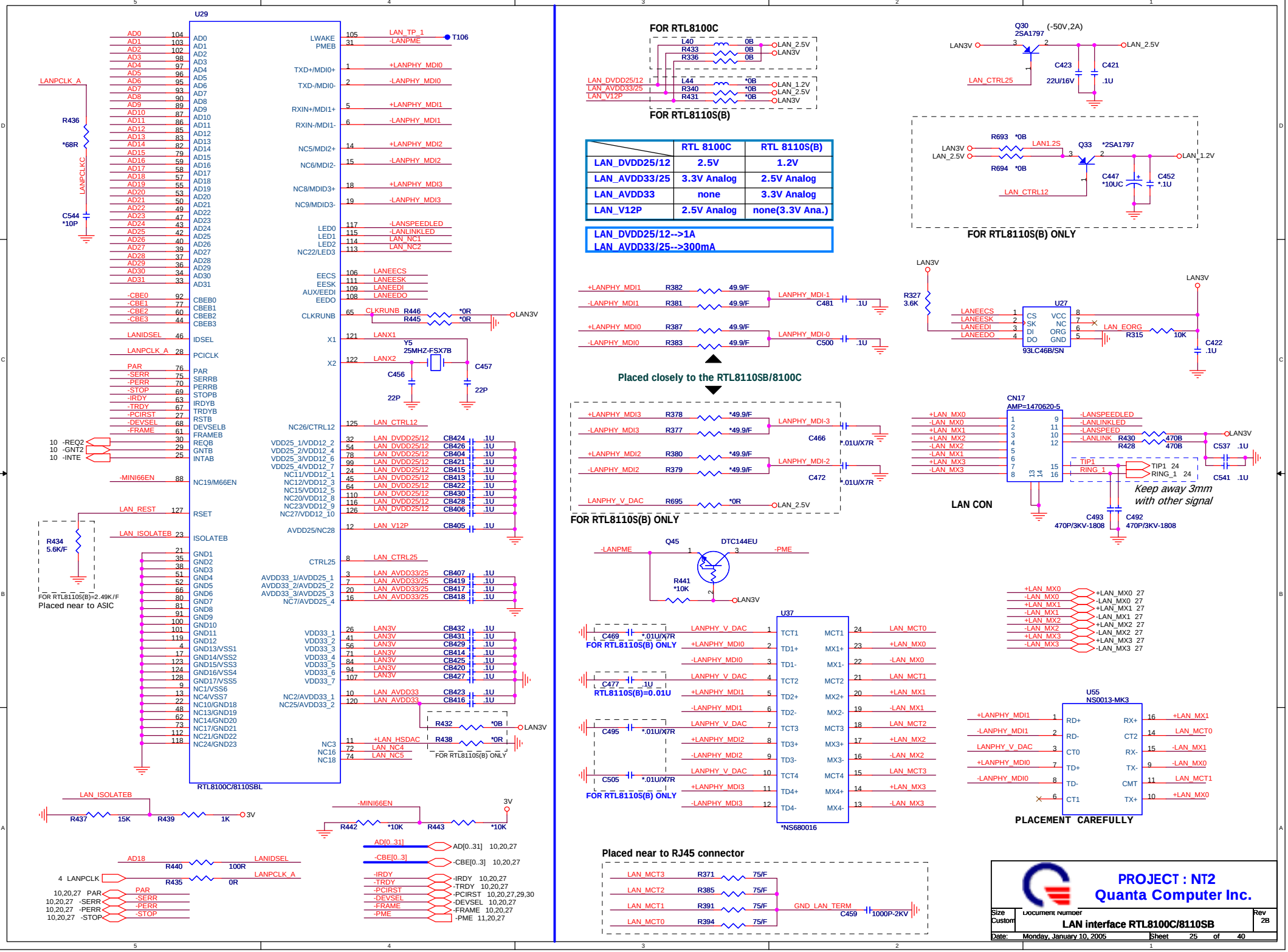
- All 1394 signals must be routed on top side only
- 110 ohm +- 5% differential pairs must be used
- Differential pairs must be 5 mills wide and 10 mills apart
- Parallelism must be maintained throughout differential pairs
- Minimum rise time @ 500 ps
- Fbw @ 700 MHz
- Lambda/2 = 3 inches
- Differentail pair must be routed with equal lengths no longer than 3 inches
- Stubs must be keep as short as possbile
- All components must be place as close to device as possible



PROJECT : NT2
Quanta Computer Inc.

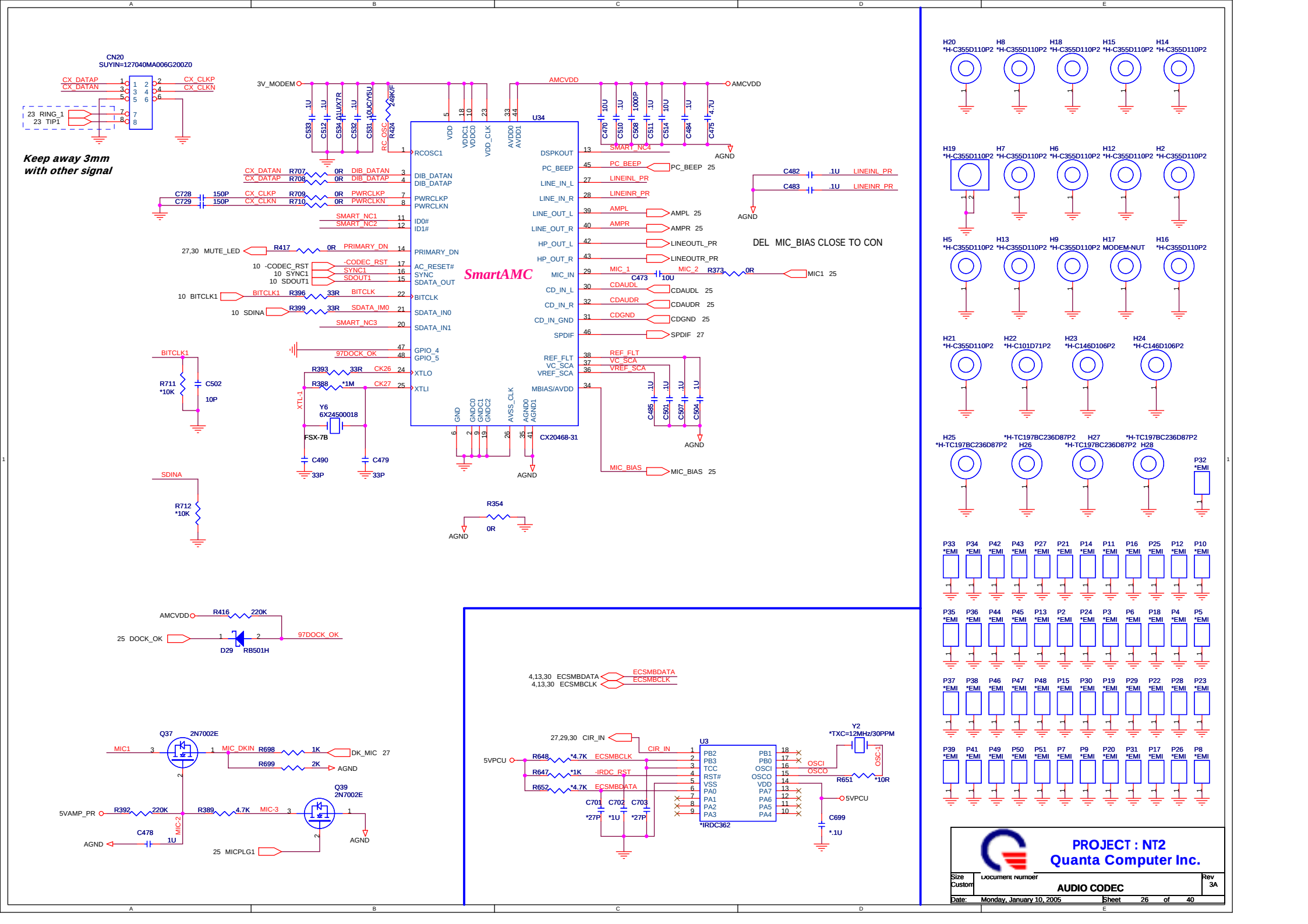
Size	Document Number	Rev
Custom	1394 CONTROL/BLUETOOTH	3A

Date: Monday, January 10, 2005 Sheet 24 of 40

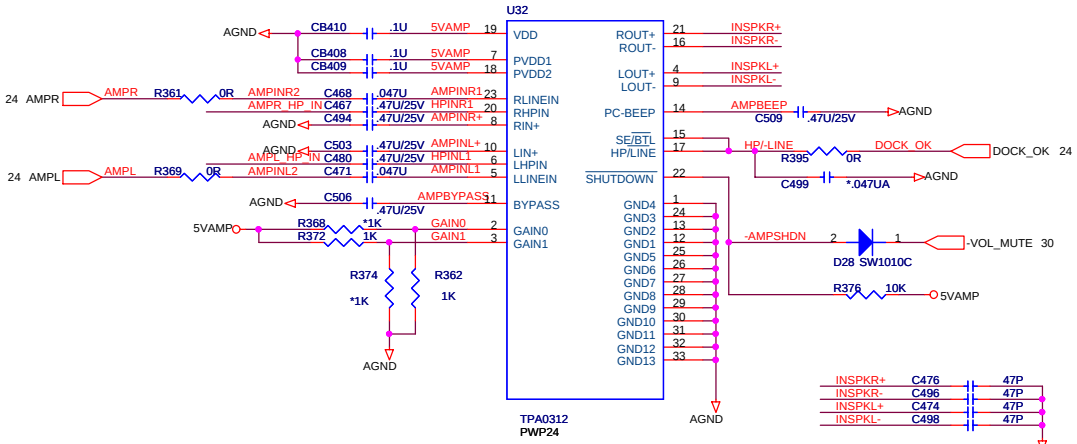


	RTL 8100C	RTL 8110S(B)
LAN_DVDD25/12	2.5V	1.2V
LAN_AVDD33/25	3.3V Analog	2.5V Analog
LAN_AVDD33	none	3.3V Analog
LAN_V12P	2.5V Analog	none(3.3V Ana.)

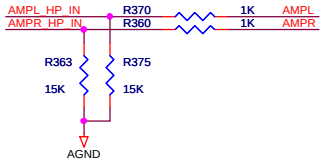
LAN_DVDD25/12-->1A
LAN_AVDD33/25-->300mA


CN20
SUYIN=127040MA006G200Z0
CX_DATAP
CX_DATAN
CX_CLKP
CX_CLKN
23 RING_1
23 TIP1
Keep away 3mm
with other signal
3V_MODEM
AMCVDD
U34
SmartAMC
CX20468-31
RCOSC1
DIB_DATAN
DIB_DATAP
PWRCLKP
PWRCLKN
ID0#
ID1#
PRIMARY_DN
AC_RESET#
SYNC
SDATA_OUT
BITCLK
SDATA_IN0
SDATA_IN1
GPIO_4
GPIO_5
XTLO
XTLI
DSPKOUT
PC_BEEP
LINE_IN_L
LINE_IN_R
LINE_OUT_L
LINE_OUT_R
HP_OUT_L
HP_OUT_R
MIC_IN
CD_IN_L
CD_IN_R
CD_IN_GND
SPDIF
REF_FLT
VC_SCA
VREF_SCA
MBIAS/AVDD
MIC_BIAS
SMART_NC4
LINEINL_PR
LINEINR_PR
AMPL
AMPR
LINEOUTL_PR
LINEOUTR_PR
MIC_1
MIC_2
CDAUDL
CDAUDR
CDGND
SMART_NC1
SMART_NC2
SMART_NC3
97DOCK_OK
CK26
CK27
BITCLK1
SDINA
Y6
6X24500018
FSX-7B
AGND
DEL MIC_BIAS CLOSE TO CON
MUTE_LED
DOCK_OK
D29
RB501H
ECSMBDATA
ECSMBCLK
CIR_IN
5VPCU
U3
*IRDC362
Y2
*TXC=12MHz/30PPM
OSCI
OSCO
Q37
2N7002E
MIC1
MIC_DKIN
DK_MIC
5VAMP_PR
MIC-3
MIC-2
MICPLG1
Q39
2N7002E
PROJECT : NT2
Quanta Computer Inc.
Size
Custom
Document Number
AUDIO CODEC
Rev
3A
Date: Monday, January 10, 2005
Sheet 26 of 40

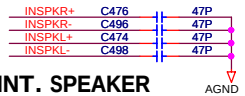
AUDIO AMPLIFIER

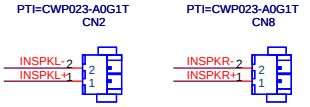


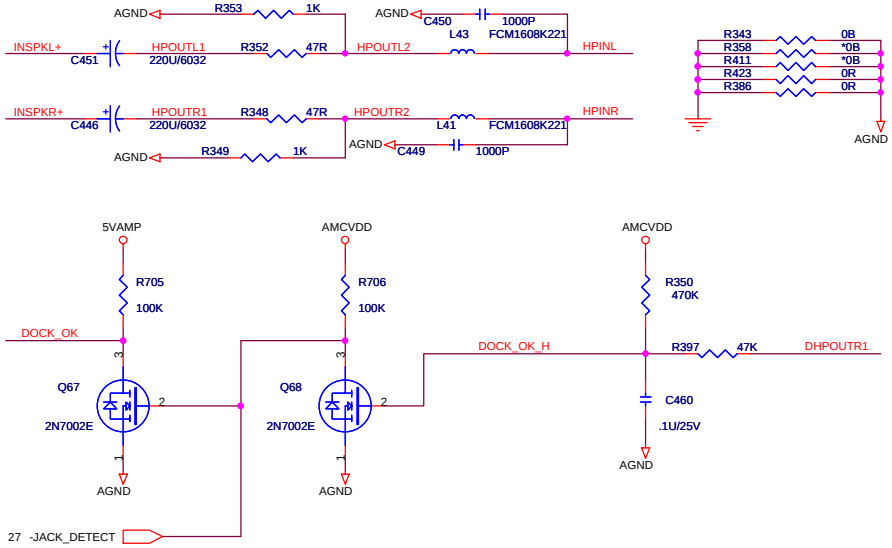
GAIN0	GAIN1	Av
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



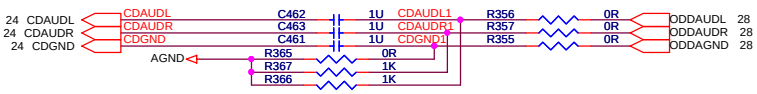
INT. SPEAKER



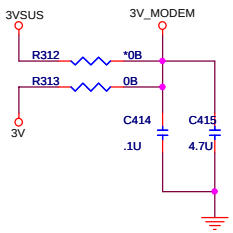


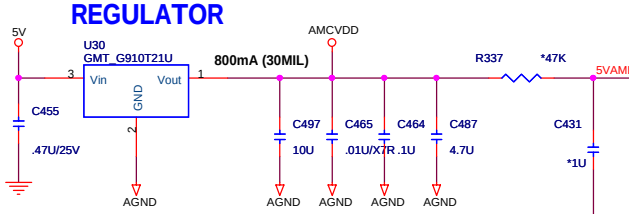


CD/PHONE INPUT & MONOOUT

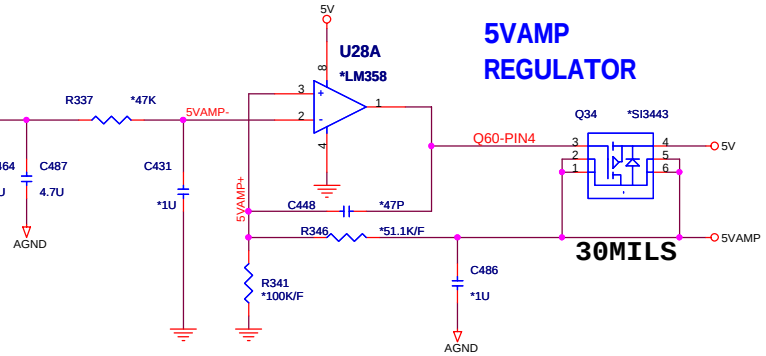


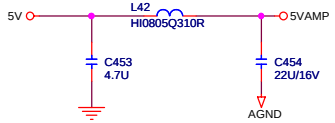
3VAUD REGULATOR



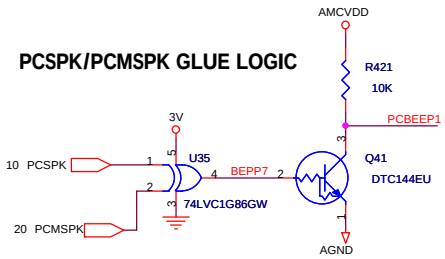


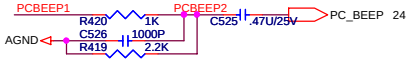
5VAMP REGULATOR

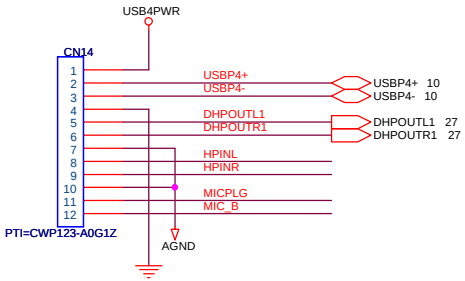




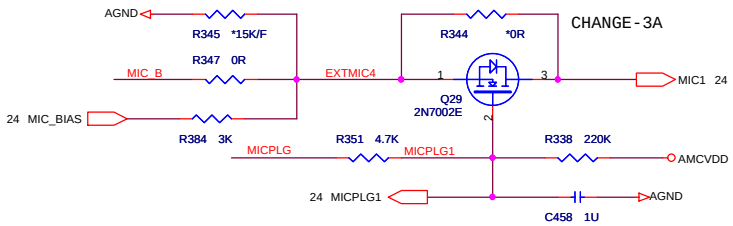
PCSPK/PCMSPK GLUE LOGIC







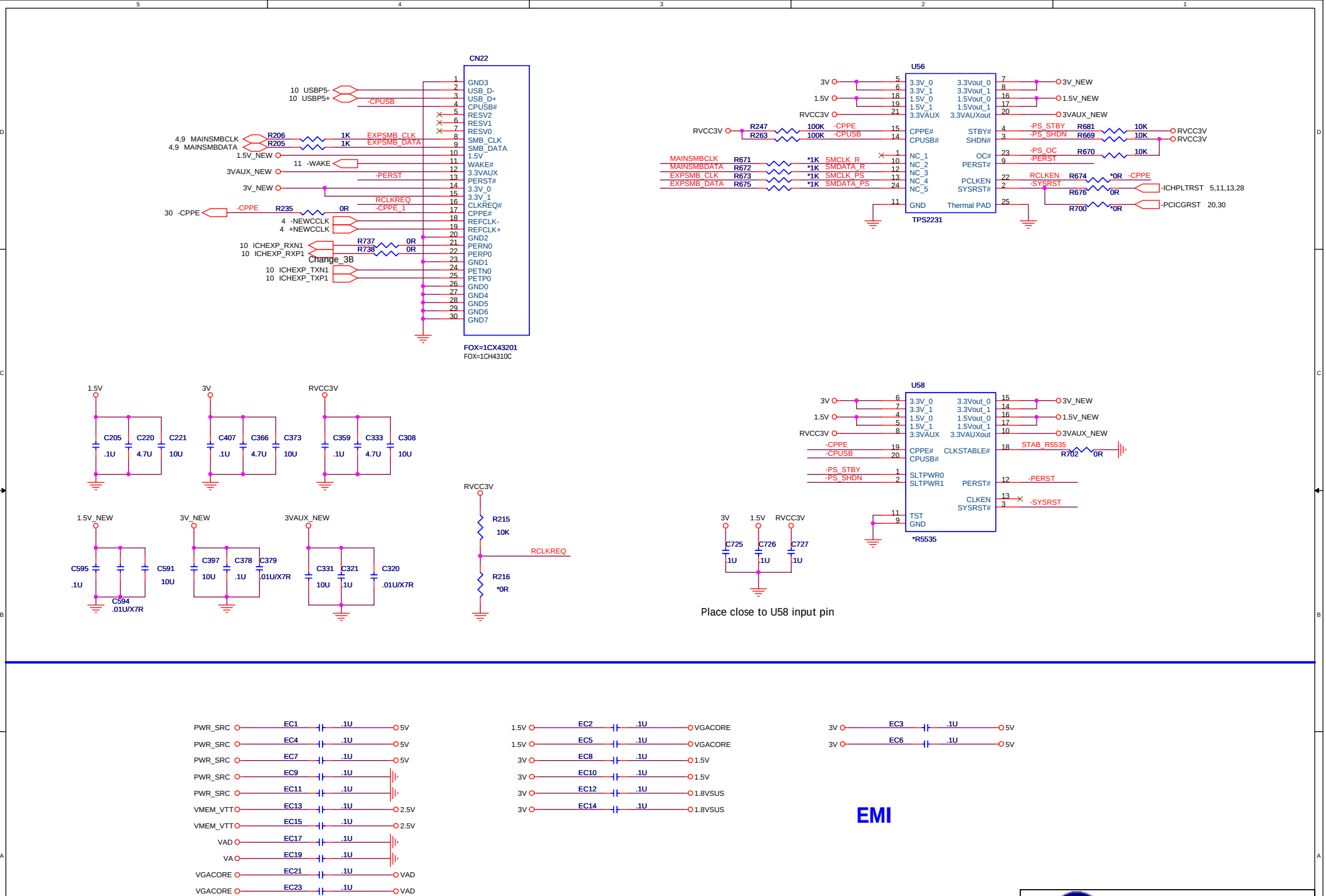
EXT MIC

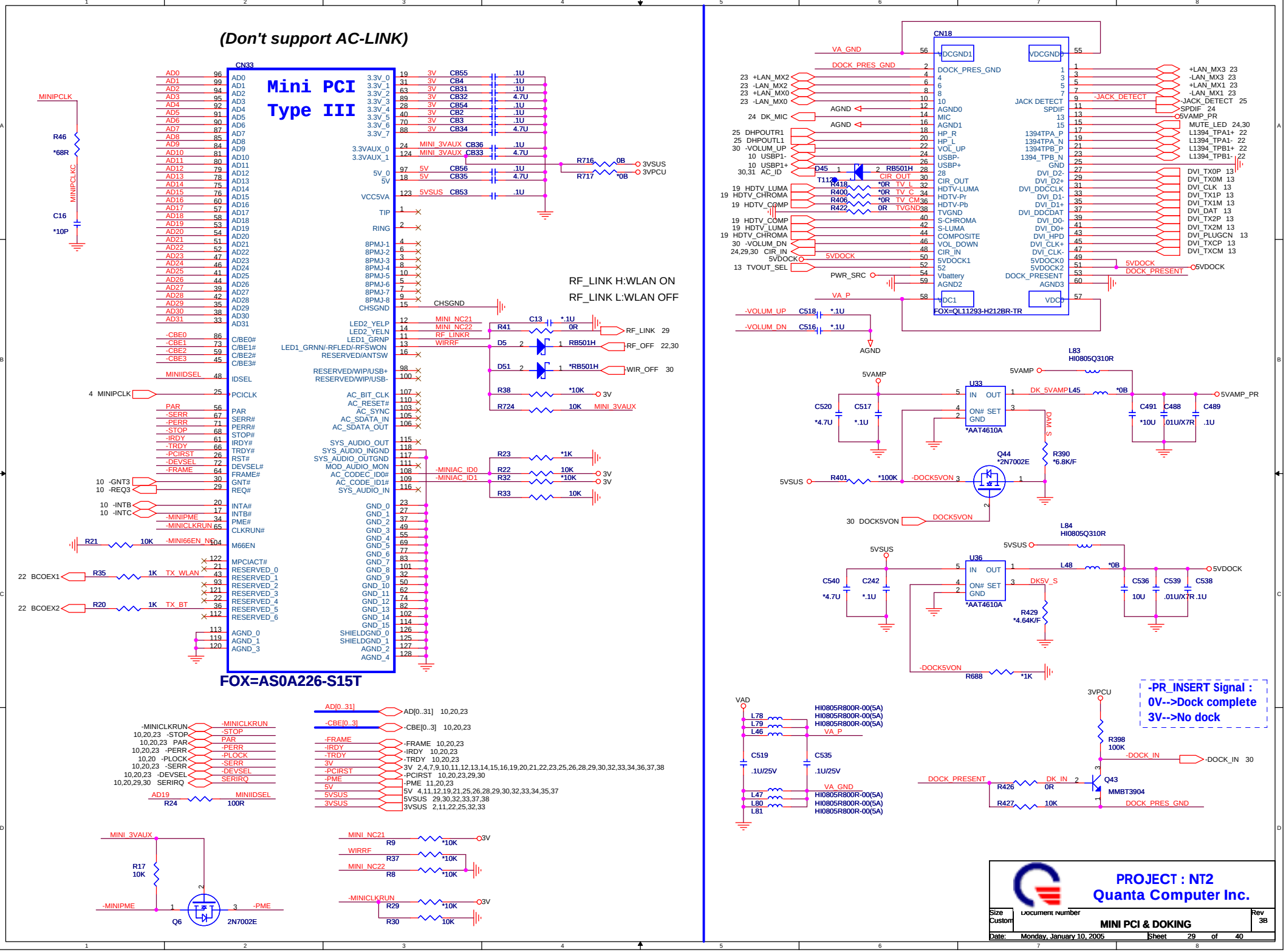


PROJECT : NT2
Quanta Computer Inc.

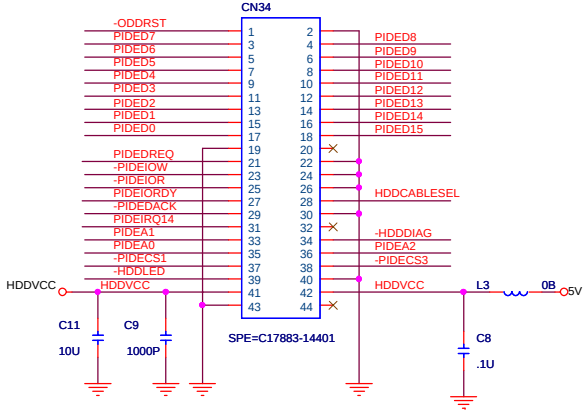
Size	Document Number	Rev
Custom	AUDIO AMP, HEADPHONE&SPEAKER	3B

Date: Monday, January 10, 2005 Sheet 27 of 40

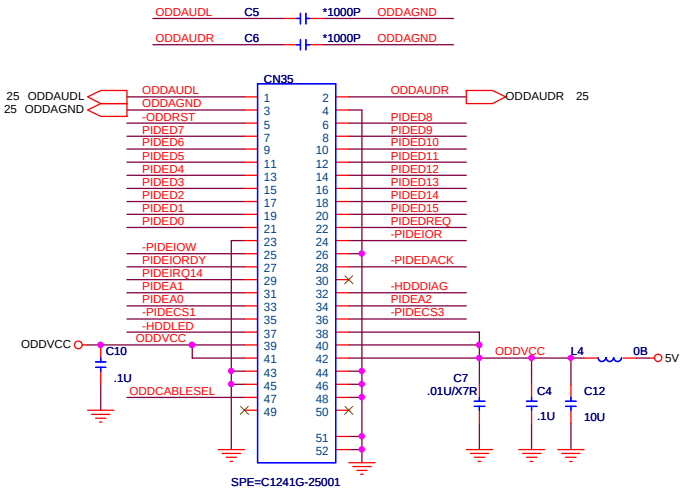

CN22
GND3
USB_D-
USB_D+
CPUSB#
RESV2
RESV1
RESV0
SMB_CLK
SMB_DATA
1.5V
WAKE#
3.3VAUX
PERST#
3.3V_0
3.3V_1
CLKREQ#
CPPE#
REFCLK-
REFCLK+
GND2
PERN0
PERP0
GND1
PETN0
PETP0
GND0
GND4
GND5
GND6
GND7
10 USBP5-
10 USBP5+
-CPUSB
4,9 MAINSMBCLK
4,9 MAINSMBDATA
R206 1K EXPSMB_CLK
R205 1K EXPSMB_DATA
1.5V_NEW
11 -WAKE
3VAUX_NEW
-PERST
3V_NEW
RCLKREQ
-CPPE_1
30 -CPPE
-CPPE R235 0R
4 -NEWCCLK
4 +NEWCCLK
10 ICHEXP_RXN1
10 ICHEXP_RXP1
R737 0R
R738 0R
Change_3B
10 ICHEXP_TXN1
10 ICHEXP_TXP1
FOX=1CX43201
FOX=1CH4310C
U56
3V
1.5V
RVCC3V
3.3V_0
3.3V_1
1.5V_0
1.5V_1
3.3VAUX
3.3Vout_0
3.3Vout_1
1.5Vout_0
1.5Vout_1
3.3VAUXout
3V_NEW
1.5V_NEW
3VAUX_NEW
R247 100K -CPPE
R263 100K -CPUSB
CPPE#
CPUSB#
STBY#
SHDN#
-PS_STBY R681 10K
-PS_SHDN R669 10K
RVCC3V
RVCC3V
-PS_OC R670 10K
-PERST
OC#
PERST#
MAINSMBCLK R671 *1K SMCLK_R
MAINSMBDATA R672 *1K SMDATA_R
EXPSMB_CLK R673 *1K SMCLK_PS
EXPSMB_DATA R675 *1K SMDATA_PS
NC_1
NC_2
NC_3
NC_4
NC_5
RCLKEN R674 *0R -CPPE
-SYSRST
R676 0R
-ICHPLTRST 5,11,13,28
R700 *0R
-PCICGRST 20,30
PCLKEN
SYSRST#
GND
Thermal PAD
TPS2231
1.5V
3V
RVCC3V
C205 .1U
C220 4.7U
C221 10U
C407 .1U
C366 4.7U
C373 10U
C359 .1U
C333 4.7U
C308 10U
1.5V_NEW
3V_NEW
3VAUX_NEW
C595 .1U
C591 10U
C594 .01U/X7R
C397 10U
C378 .1U
C379 .01U/X7R
C331 10U
C321 .1U
C320 .01U/X7R
RVCC3V
R215 10K
RCLKREQ
R216 *0R
U58
3V
1.5V
RVCC3V
3.3V_0
3.3V_1
1.5V_0
1.5V_1
3.3VAUX
3.3Vout_0
3.3Vout_1
1.5Vout_0
1.5Vout_1
3.3VAUXout
3V_NEW
1.5V_NEW
3VAUX_NEW
-CPPE
-CPUSB
CPPE#
CPUSB#
CLKSTABLE#
STAB_R5535
R702 0R
-PS_STBY
-PS_SHDN
SLTPWR0
SLTPWR1
PERST#
-PERST
CLKEN
SYSRST#
-SYSRST
TST
GND
*R5535
3V 1.5V RVCC3V
C725 .1U
C726 .1U
C727 .1U
Place close to U58 input pin
PWR_SRC EC1 .1U 5V
PWR_SRC EC4 .1U 5V
PWR_SRC EC7 .1U 5V
PWR_SRC EC9 .1U
PWR_SRC EC11 .1U
VMEM_VTT EC13 .1U 2.5V
VMEM_VTT EC15 .1U 2.5V
VAD EC17 .1U
VA EC19 .1U
VGACORE EC21 .1U VAD
VGACORE EC23 .1U VAD
1.5V EC2 .1U VGACORE
1.5V EC5 .1U VGACORE
3V EC8 .1U 1.5V
3V EC10 .1U 1.5V
3V EC12 .1U 1.8VSUS
3V EC14 .1U 1.8VSUS
3V EC3 .1U 5V
3V EC6 .1U 5V
EMI
PROJECT : NT2
Quanta Computer Inc.
Size Custom
Document Number
NEW CARD
Rev 3B
Date: Monday, January 10, 2005
Sheet 28 of 40

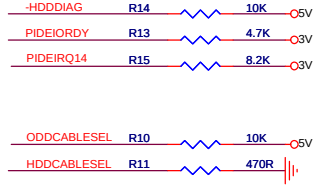

(Don't support AC-LINK)
Mini PCI
Type III
CN33
FOX=AS0A226-S15T
RF_LINK H:WLAN ON
RF_LINK L:WLAN OFF
CN18
FOX=QL11293-H212BR-TR
-PR_INSERT Signal :
0V-->Dock complete
3V-->No dock
PROJECT : NT2
Quanta Computer Inc.
MINI PCI & DOKING
Size Custom
Document Number
Rev 3B
Date: Monday, January 10, 2005
Sheet 29 of 40

HDD CONNECTOR

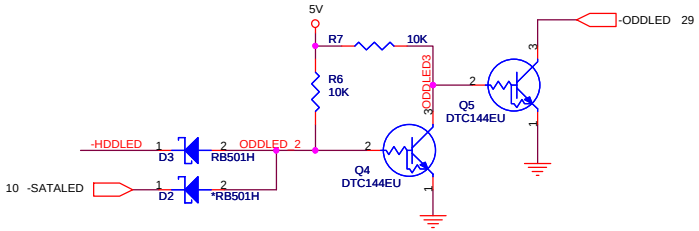


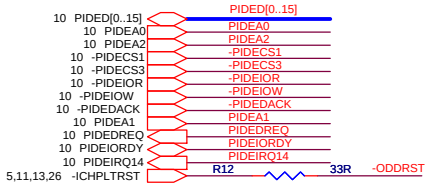
ODD CONNECTOR





CABLESEL: H=SLAVE L=MASTER

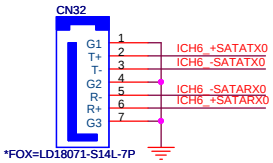


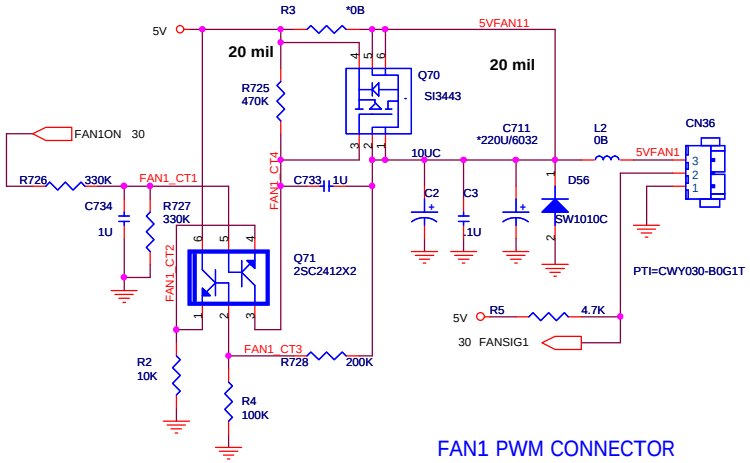


PLACEMENT NOTICE :

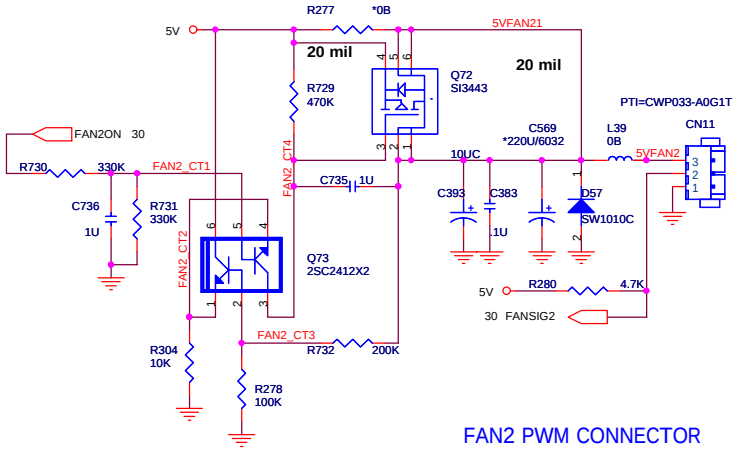
1. PUT THE BYPASS CAP AND INDUCTOR NEAR THE HDD AND ODD CONNECTOR
2. ALL DAMPING RESISTORS SHOULD NEAR ODD AND HDD CONNECOTR RESPECTIVELY
3. ALL PULLUP AND PULLDN SHOULD NEAR THE CONNECTOR
4. ALL IDE TRACE SHOULD KEEP 5:15 ID POSSIBLE AND 5:10 IS MINIMUM REQUIREMENT

SATA HDD CONNECTOR

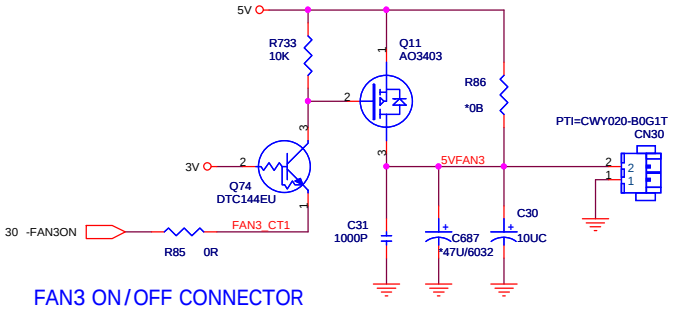




FAN1 PWM CONNECTOR



FAN2 PWM CONNECTOR



FAN3 ON/OFF CONNECTOR

PROJECT : NT2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDD/CD-ROM/FAN	3B

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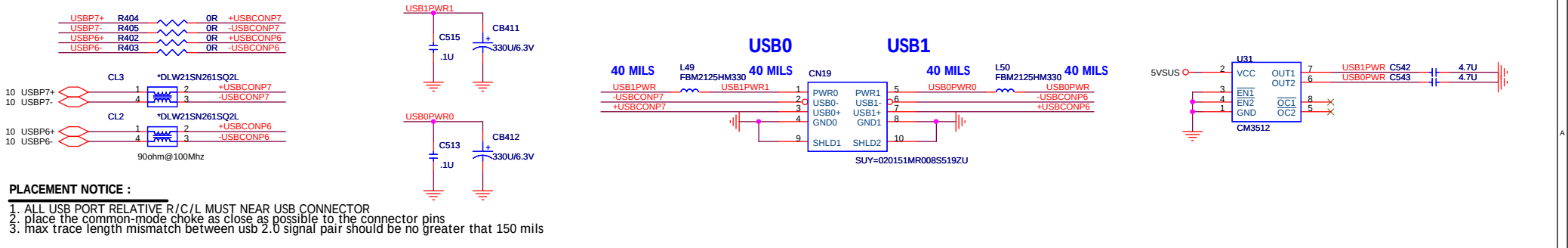

PLACEMENT NOTICE :

1. ALL USB PORT RELATIVE R/C/L MUST NEAR USB CONNECTOR
2. place the common-mode choke as close as possible to the connector pins
3. max trace length mismatch between usb 2.0 signal pair should be no greater that 150 mils

PROJECT : NT2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	USB PORT/LED	3C

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KBC-NS87591L

PIN	NS PC87591		ENE KB3910	
11	NC		TEST_TP	High: Clock Test Mode. Low: 32KHz clock in normal running. (Recommend)
12	NC		DPLL_TP	High: Test mode, set KSO [0:15] and KSO16 to become internal output. Low : Normal operation. (Recommend)
105	TINT#		ISP_TP	High: Normal operation. (Recommend) Low: Enable ISP mode.
124	ENV0	Internal pull-down to GND. Set the Enviroment to OBD which is used for debugging the PC87591 firmware while it is mounted on its final production board.	A0	
125	ENV1	External pull-up to 3VPCU by 10k. Set the Enviroment to OBD which is used for debugging the PC87591 firmware while it is mounted on its final production board.	XIOP_TP	High: Enable the internal pull-up resistor on XIOCS [F:0] pins. Low: Disable the internal pull-up resistor on XIOCS [F:0] pins.
126	BADDR0	Internal pull-down to GND. To set Super I/O configuration Base Address.	A2	
127	BADDR1	Internal pull-down to GND. To set Super I/O configuration Base Address.	A3	
128	TRIS	Internal pull-down to GND. Normal operation.	DMRP_TP	High: Disable Memory Remapping Process. (Recommend) Low : Enable Memory Remapping Process.
131	SHBM	External pull-up to 3VPCU by 10k. Enable shared memory with host BIOS.	EMWB_TP	High: Enable Memory while Boot. (Recommand for shared BIOS application) Low: Disable Memory while Boot.

-LDRQ(pin 8) internal is no use

CHANGE FOOTPRINT-2B

Reserve for 97551

Should have a 0.1uF capacitor close to every GND-VCC pair + one larger cap on the supply.

EEPROM

VOLUME DOWN	/ MX5-MY15
VOLUME UP	/ MX4-MY15
TOUCH PAD	/ MX1-MY15
MUTE	/ MX0-MY15

PC97551VPC

Pin 103 internal is "A19",Can't use to GPIO

Pin 24 if no pull-high, will can't reboot.

(FOR KB3910)

ADD-3C

BIOS ROM

ROM CHIP P/N:AKE34ZAPK01

I/O Address

BADDR1-0	Index	Data
0 0	2E	2F
0 1	4E	4F
1 0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+1
1 1	Reserved	

KEYBOARD PULL-UP

PTI=AF1263-A2G1Z

TOUCH PAD

RESERVE: POWER BUTTON

BOM Note-3C

DEL Q13,Q40,Q12 BA001440Z87
DEL R99,R102 CS11303J905
ADD Q13,Q12,Q40 BAN70020Z13
ADD R745 CS31003J908

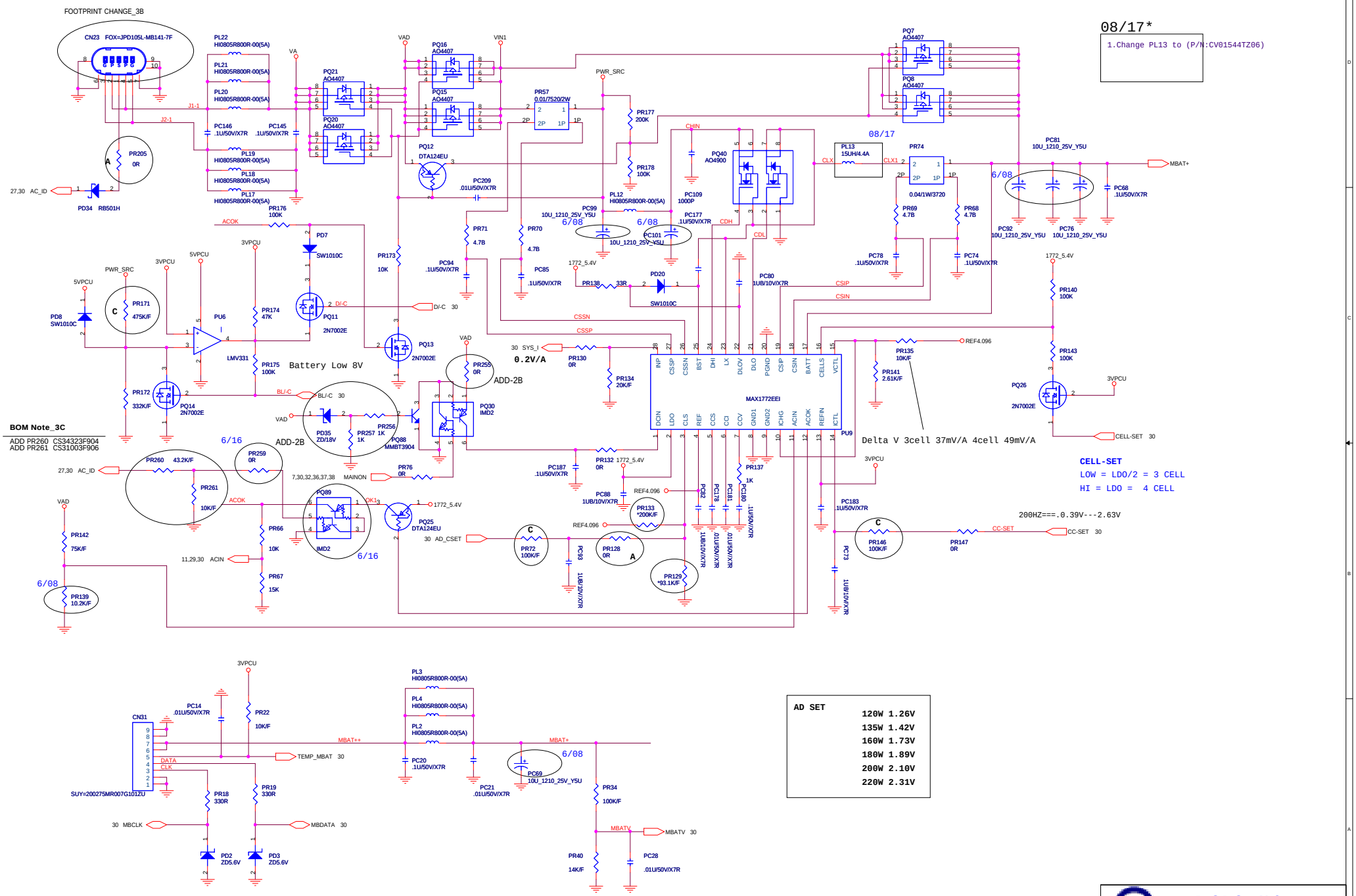
PTI=AF712L-A2G1T

PROJECT : NT2
Quanta Computer Inc.

Size	Document Number	Rev
C	KBC PCU-87591	3C

Date: Monday, January 10, 2005 Sheet 32 of 40

BATTERY CHARGER



08/17*

1.Change PL13 to (P/N:CV01544TZ06)

BOM Note_3C

ADD PR260 CS34323F904
ADD PR261 CS31003F906

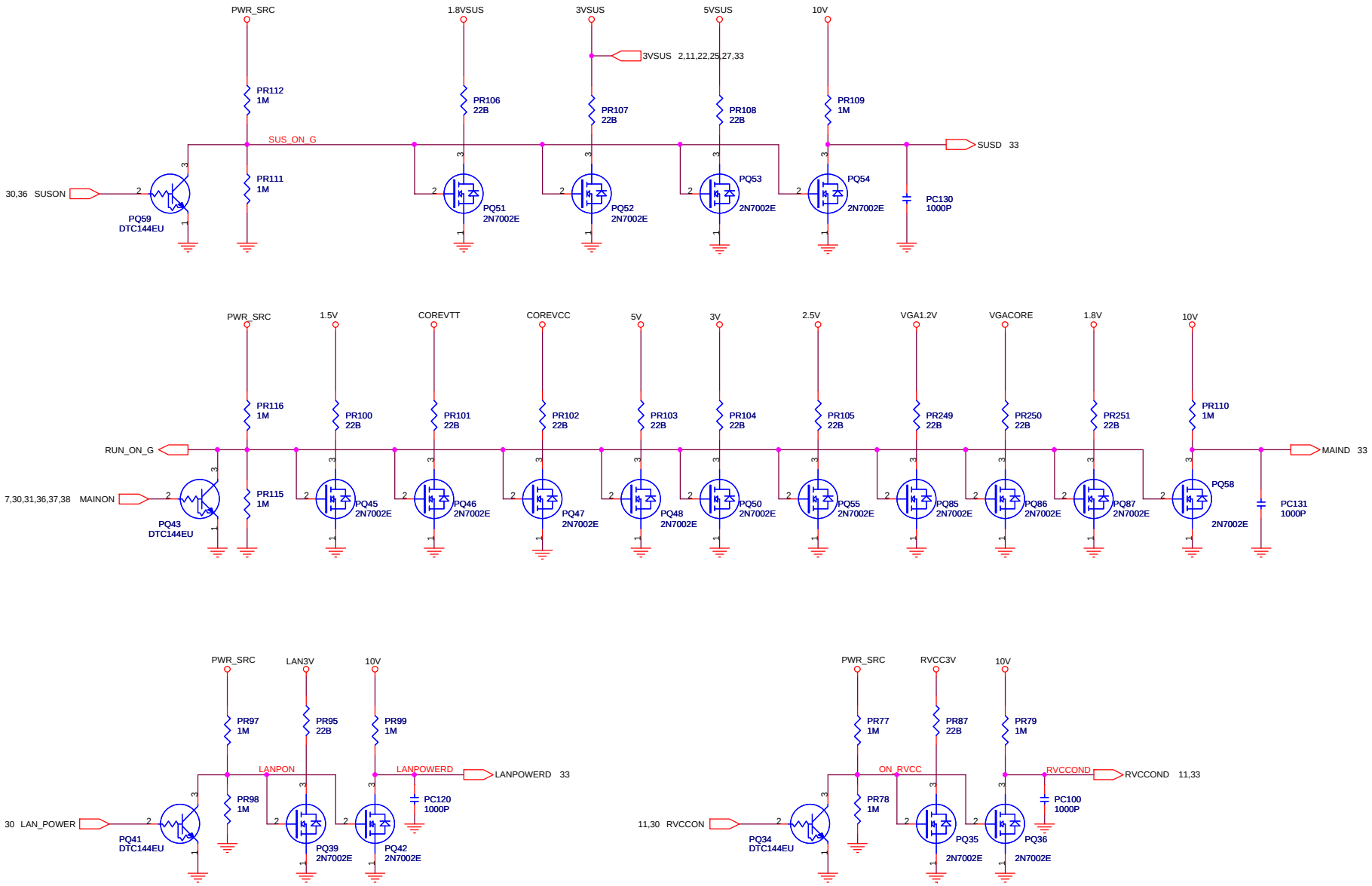
AD SET

120W	1.26V
135W	1.42V
160W	1.73V
180W	1.89V
200W	2.10V
220W	2.31V

PROJECT : NT2
Quanta Computer Inc.

Size	Document Number	Rev
C	BATTERY CHARGER 1772	3B

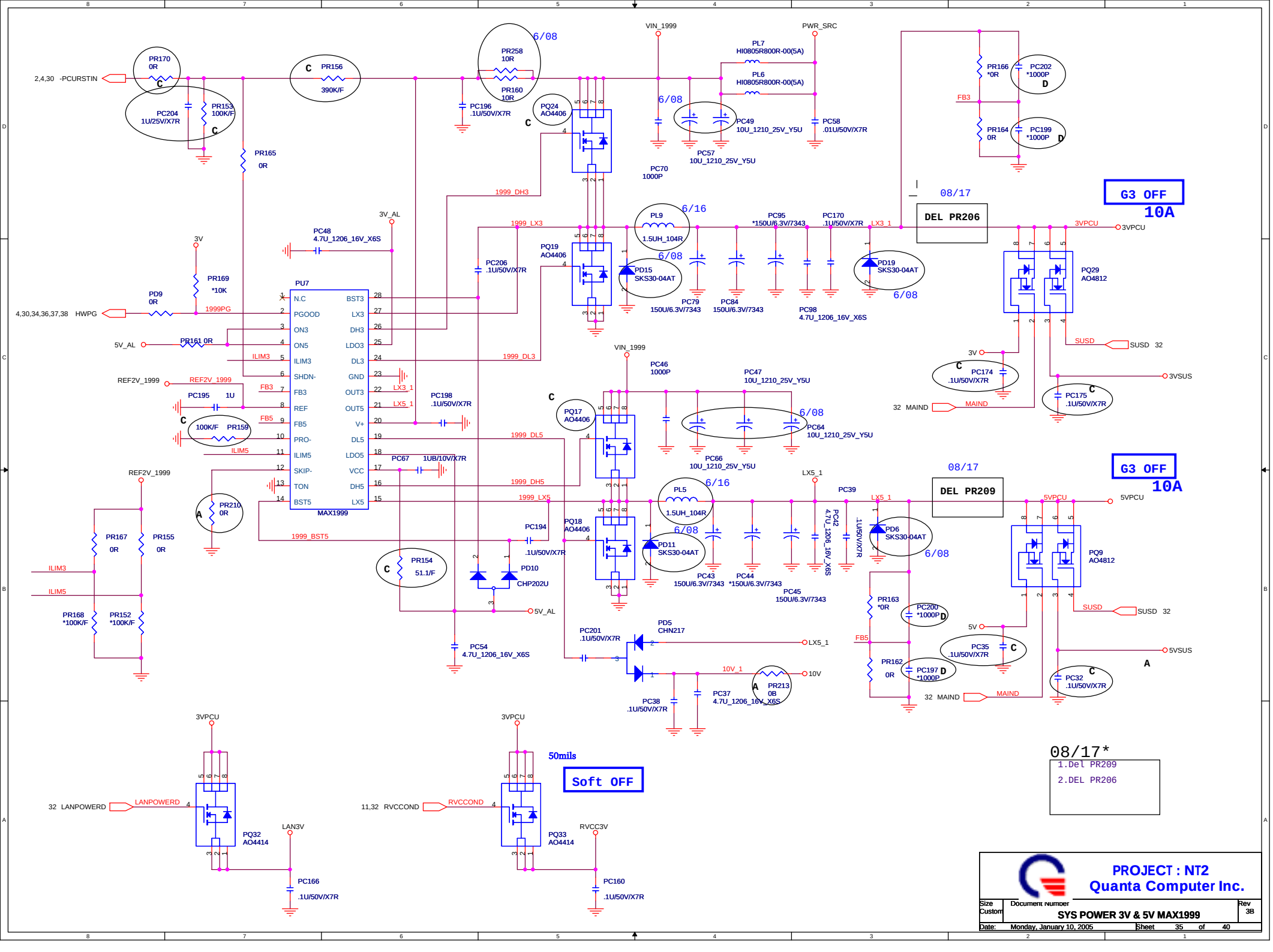
Date: Monday, January 10, 2005 Sheet 33 of 40

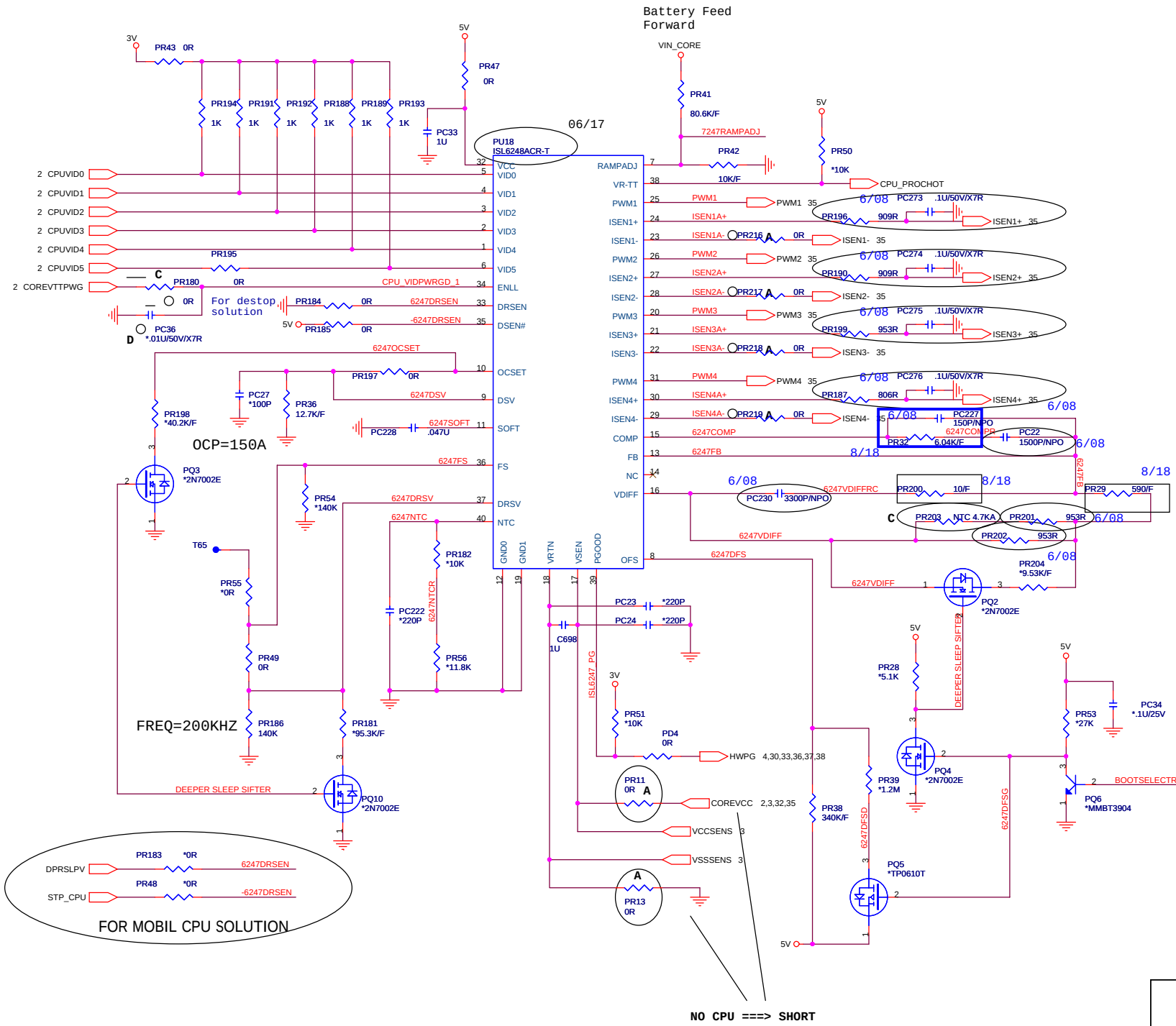


PROJECT : NT2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DISCHARGE CIRCUIT	2A

Date: Monday, January 10, 2005 Sheet 34 of 40


2,4,30 -PCURSTIN
PR170 0R
PC204 1U/25V/X7R
PR153 100K/F
PR156 390K/F
PR165 0R
PR258 10R
PR160 10R
PC196 .1U/50V/X7R
PQ24 AO4406
VIN_1999
PWR_SRC
PL7 HI0805R800R-00(5A)
PL6 HI0805R800R-00(5A)
PC49 10U_1210_25V_Y5U
PC57 10U_1210_25V_Y5U
PC58 .01U/50V/X7R
PC70 1000P
PR166 *0R
PC202 *1000P
PR164 0R
PC199 *1000P
FB3
G3 OFF
10A
08/17
DEL PR206
3VPCU
1999_DH3
1999_LX3
PL9 1.5UH_104R
PC95 *150U/6.3V/7343
PC170 .1U/50V/X7R
LX3_1
PD15 SKS30-04AT
PD19 SKS30-04AT
PC79 150U/6.3V/7343
PC84 150U/6.3V/7343
PC98 4.7U_1206_16V_X6S
PQ29 AO4812
SUSD
SUSD 32
3VSUS
PC174 .1U/50V/X7R
PC175 .1U/50V/X7R
32 MAIND
MAIND
PC48 4.7U_1206_16V_X6S
3V_AL
3V
PR169 *10K
PD9 0R
4,30,34,36,37,38 HWPG
1999PG
PU7
N.C
PGOOD
ON3
ON5
ILIM3
SHDN-
FB3
REF
FB5
PRO-
ILIM5
SKIP-
TON
BST5
BST3
LX3
DH3
LDO3
DL3
GND
OUT3
OUT5
V+
DL5
LDO5
VCC
DH5
LX5
MAX1999
5V_AL
PR161 0R
REF2V_1999
PC195 1U
100K/F PR159
PC206 .1U/50V/X7R
PC198 .1U/50V/X7R
LX3_1
LX5_1
1999_DL3
1999_DL5
1999_DH5
1999_LX5
1999_BST5
PC67 1UB/10V/X7R
PR210 0R
PR167 0R
PR155 0R
PR168 *100K/F
PR152 *100K/F
PR154 51.1/F
PC194 .1U/50V/X7R
PD10 CHP202U
PC54 4.7U_1206_16V_X6S
PQ17 AO4406
PC46 1000P
PC47 10U_1210_25V_Y5U
PC64 10U_1210_25V_Y5U
PC66 10U_1210_25V_Y5U
PQ18 AO4406
PL5 1.5UH_104R
PD11 SKS30-04AT
PC43 150U/6.3V/7343
PC44 *150U/6.3V/7343
PC45 150U/6.3V/7343
PC42 4.7U_1206_16V_X6S
PC39 .1U/50V/X7R
PD6 SKS30-04AT
PC201 .1U/50V/X7R
PD5 CHN217
10V_1
10V
PR213 0B
PC38 .1U/50V/X7R
PC37 4.7U_1206_16V_X6S
08/17
DEL PR209
5VPCU
5VSUS
PQ9 AO4812
PR163 *0R
PC200 *1000P
PR162 0R
PC197 *1000P
PC35 .1U/50V/X7R
PC32 .1U/50V/X7R
5V
32 LANPOWERD
LANPOWERD
PQ32 AO4414
LAN3V
PC166 .1U/50V/X7R
11,32 RVCCOND
RVCCOND
PQ33 AO4414
RVCC3V
PC160 .1U/50V/X7R
50mils
Soft OFF
08/17*
1.Del PR209
2.DEL PR206
PROJECT : NT2
Quanta Computer Inc.
Size Custom
Document Number
SYS POWER 3V & 5V MAX1999
Rev 3B
Date: Monday, January 10, 2005
Sheet 35 of 40



08/18*

1. Change PR29 to 590ohm (P/N:CS15903F906)
2. Change PR32 to 12.7Kohm (P/N:CS31273F905)
3. Change PR200 to 10ohm (P/N:CS01003F901)

Northwood : Rdroop=2.26K
Vdroop=40.2uA*2.26K=91mV
Prescott : Rdroop=2.26K//16.2K=1.98K
Vdroop=49uA*1.98K=97mV

2V/ROFS=VOFS/RFB
Prescott : ROFS=PR14//PR79=265K
2V/265K=VOFS/1.98K;VOFS=15mV
Northwood : ROFS=340K
2V/340K=VOFS/2.26K;VOFS=13mV

Prescott:	Northood:
HFM=1.325V/80A	HFM=1.55V/66A
LFM=1.15V/32A	LFM=1.20V/34A
DRSM=0.8V/6A	DRSM=1.0V/6A
Vos=1.7%	Vos=1.7%
Load line=1.3mV/A	Load line=1.5mV/A
Vdroop=80A*1.3mV=104mV	Vdroop=66A*1.5mV=99mV

PROJECT : NT2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	VCORE-1(ISL6248)	3B

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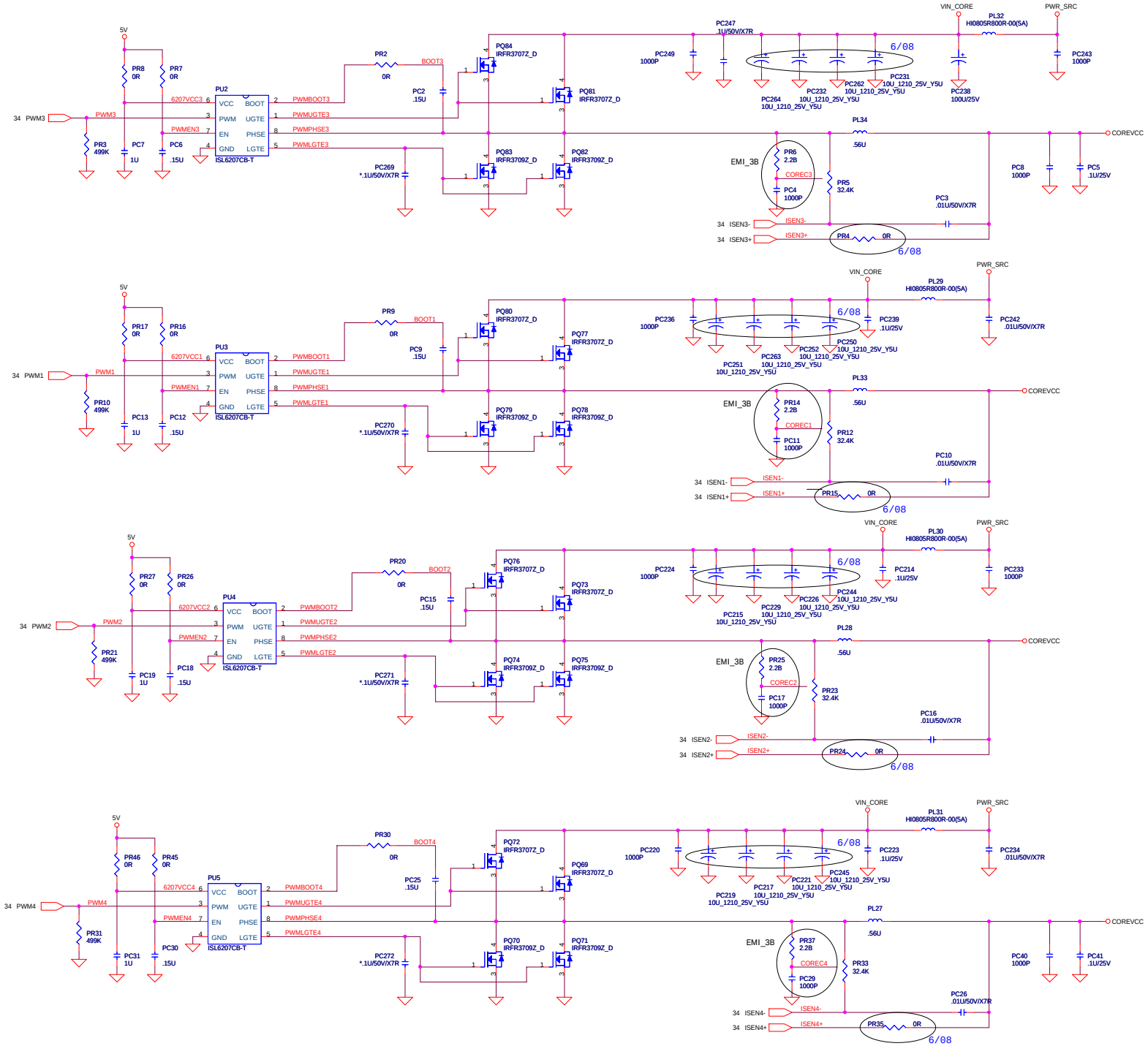

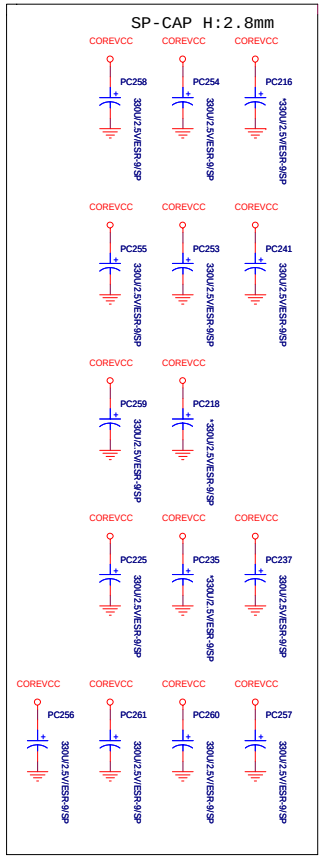

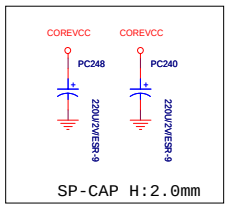

NT2 BOM C2 NOTE:
ADD PR6,PR14,PR25,PR37 CS-2203JA07
ADD PC4,PC11,PC17,PC29 CH21006K917

PROJECT : NT2
Quanta Computer Inc.

Size	Document Number	Rev
C	COREVCC (Power train)	2A

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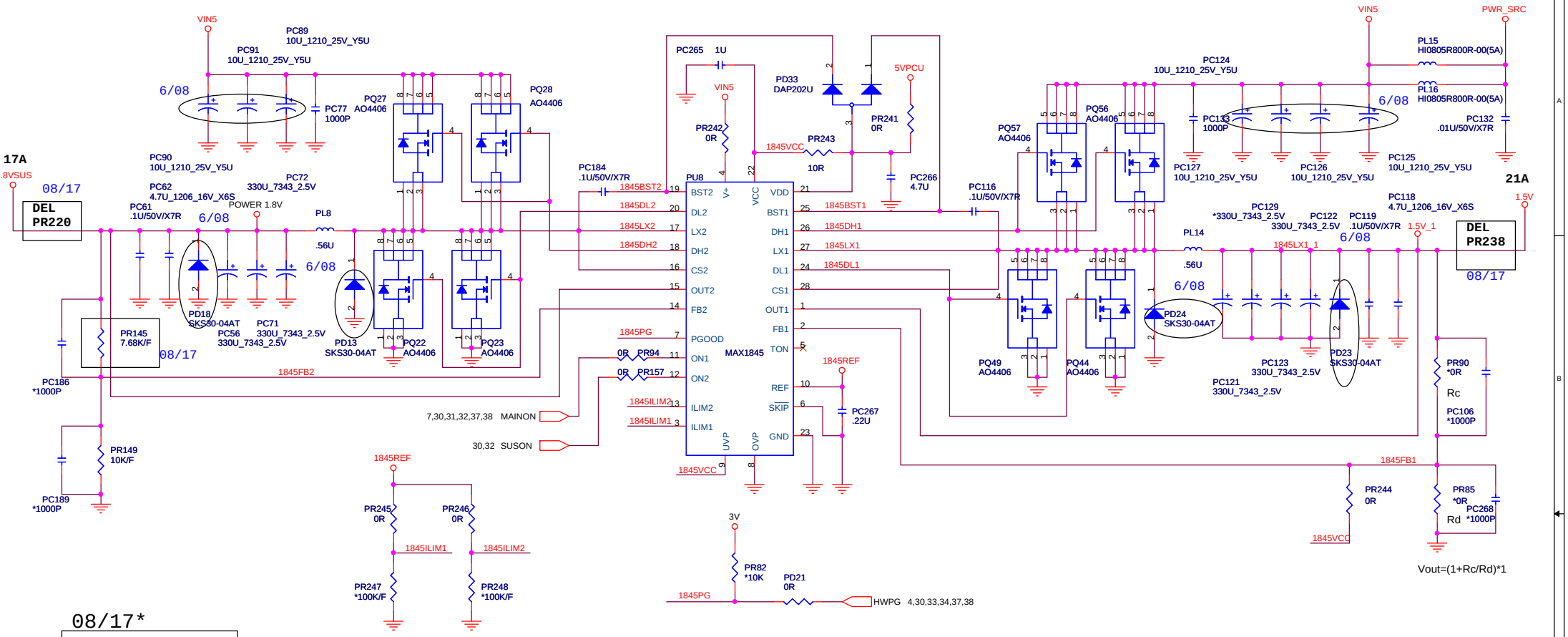
MAX1845

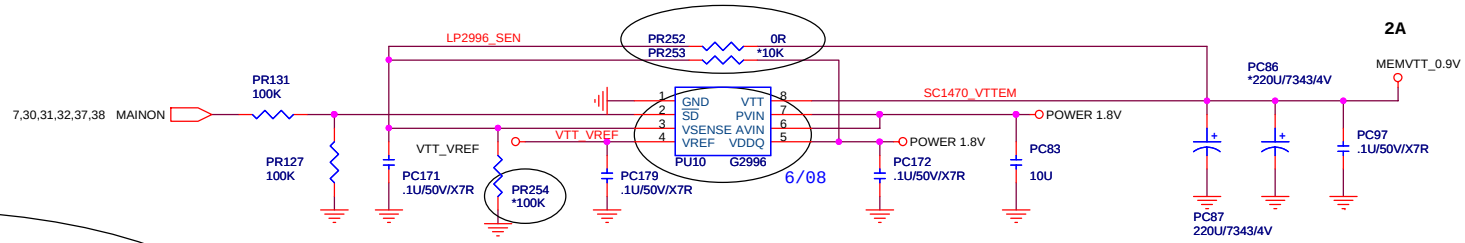


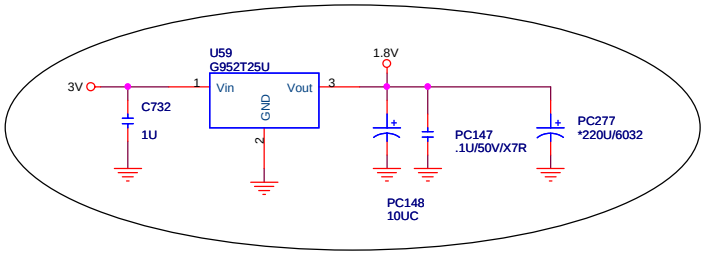
08/17*

1.Change PR145 to 7.68K

2.Del PR220

3.DEL PR238



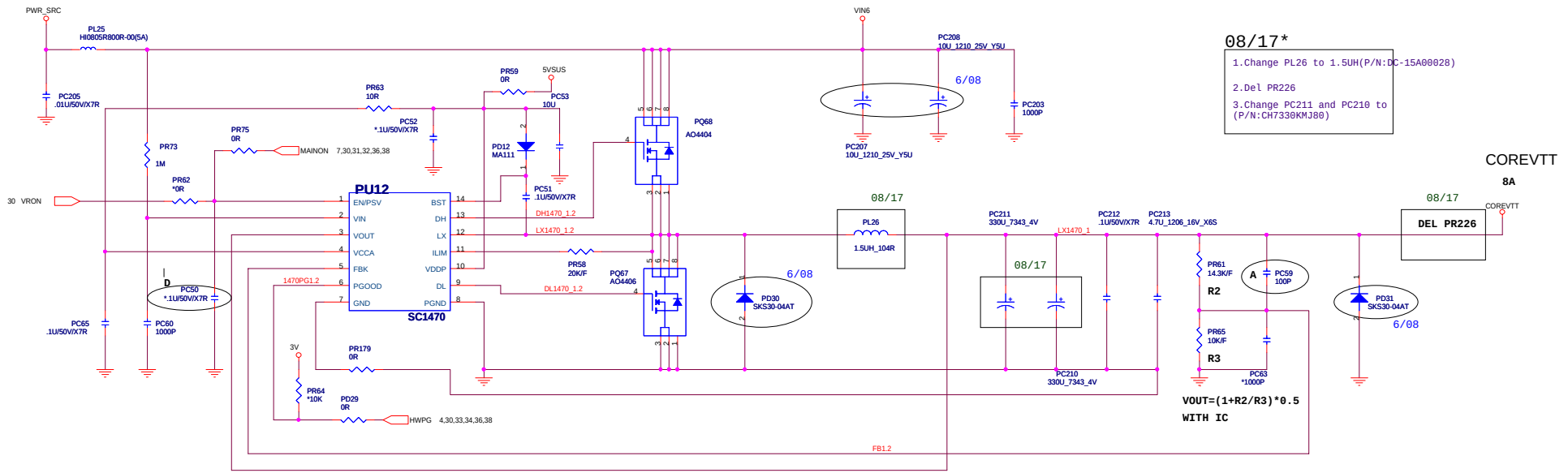


DEL PQ64 AND CHANGE -3A

PROJECT : NT2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SYSTEM POWER 1.5V	3B

Date: Monday, January 10, 2005 Sheet 38 of 40

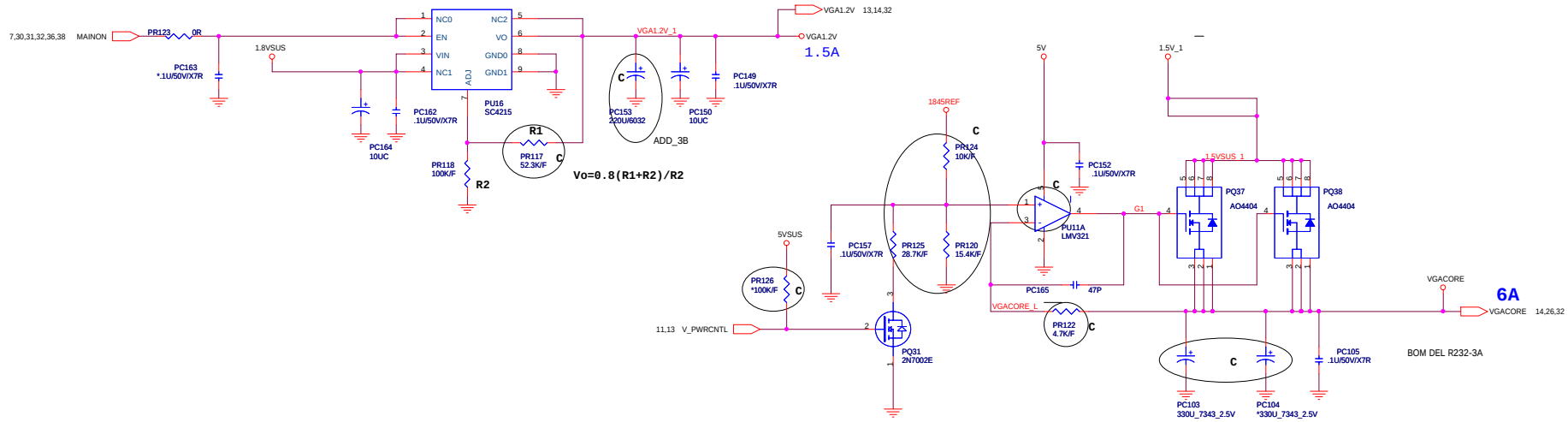


08/17*

1.Change PL26 to 1.5UH(P/N:DC-15A00028)

2.Del PR226

3.Change PC211 and PC210 to (P/N:CH7330KMJ80)



M24 VGACORECTL	
LO	1.2V
HI	1.0V

M22 VGACORECTL	
LO	1.15V
HI	1.0V

BOM C2 NOTE:

ADD PC153 CH72201M7T2 220u TAN

PROJECT : NT2
Quanta Computer Inc.

Size C	Document Number	Rev 3B
	VGA POWER / SC1470 1.2VSUS	

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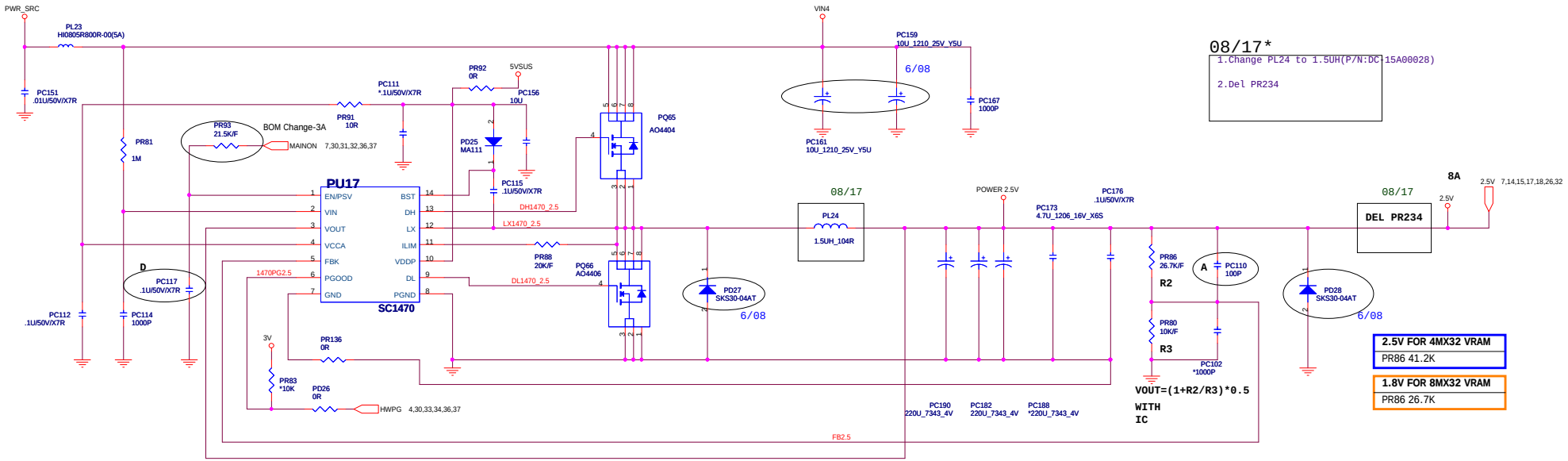

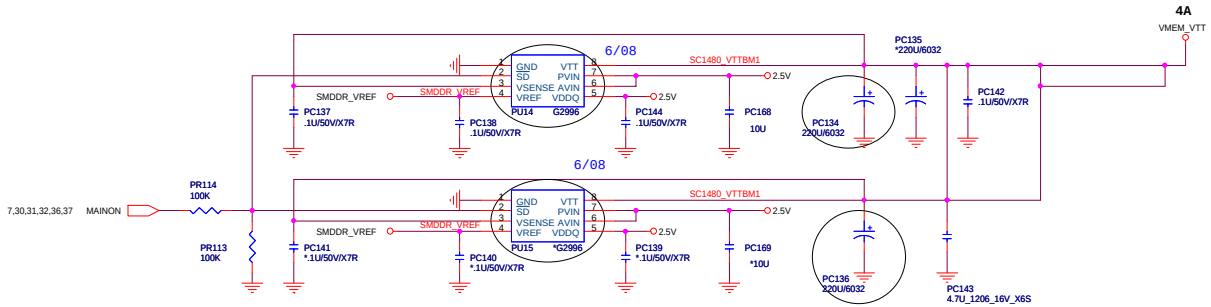

BOM C2 NOTE:

DEL PC134,PC136 CH7222KMJ82
ADD PC134,PC136 CH72201M7T2

PROJECT : NT2
Quanta Computer Inc.

Size	Document Number	Rev
C	SYSTEM POWER 2.5V & MEM_VTT	3B

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