R13 INTEL UMA/DISCRETE SYSTEM DIAGRAM 01

+3V/+5V S5 PG.31
+1.05V_VTT PG.32
CPU Core PG.33~34
DDR3 PG.35
VCCSA PG.36
Charge PG.37
+VGACORE PG.39

SODIMM1 Max. 4GB PG.12 — DDR3 Channel A
SODIMM2 Max. 4GB PG.13 — DDR3 Channel B

INTEL Sandy
37.5mm X 37.5mm
989pin PGA
TDP 35W
PG.2~5

PCI-E x8

AMD Seymour
23mm X 23mm
TDP 15W
PG.14~18

DDR3 800MHz
VRAM 64Mx16x4,64bit PG.19

HDMI PG.21
CRT PG.22
LVDS PG.20

FDI DMI

HDD PG.23 — SATA0
ODD PG.23 — SATA1

INTEL PCH
COUGAR POINT
PG.6~11

DP Port B
CRT
LVDS

PCI-E x 1 — LANE1 / LANE0
LAN RTL8165EH 10/100 PG.27
WLAN BT COMBO PG.30 — USB 2.0 PORT10

USB2.0 Ports X3 PG.26 — USB 2.0 PORT0,1,8
Webcam PG.20 — PORT4
BT Softbreeze PG.26 — PORT13

PCI-E x 1 — LANE2
Card Reader RTS5219 PG.24

KBC EnE KB3930QF A1 PG.29 — LPC
KB
TP
ROM
FAN

AUDIO CODEC
IDT 92HD80Bx
PG.25

Speaker PG.25
HP/MIC PG.26
Analog MIC PG.25

Stackup
TOP
GND
IN1
IN2
VCC
BOT

PROJECT : R13
Quanta Computer Inc.
NB5
Size: Custom | Document Number: SNB 1/4 (PCIE &DMI&FDI) | Rev: 3A
Date: Saturday, September 18, 2010 | Sheet 2 of 39

Sandy Bridge Processor (DMI,PEG,FDI)

Sandy Bridge Processor (CLK,MISC,JTAG)

02

U15A

DMI_TXN0 B27 DMI_RX#[0]
DMI_TXN1 B25 DMI_RX#[1]
DMI_TXN2 A25 DMI_RX#[2]
DMI_TXN3 B24 DMI_RX#[3]
DMI_TXP0 B28 DMI_RX[0]
DMI_TXP1 B26 DMI_RX[1]
DMI_TXP2 A24 DMI_RX[2]
DMI_TXP3 B23 DMI_RX[3]
DMI_RXN0 G21 DMI_TX#[0]
DMI_RXN1 E22 DMI_TX#[1]
DMI_RXN2 F21 DMI_TX#[2]
DMI_RXN3 D21 DMI_TX#[3]
DMI_RXP0 G22 DMI_TX[0]
DMI_RXP1 D22 DMI_TX[1]
DMI_RXP2 F20 DMI_TX[2]
DMI_RXP3 C21 DMI_TX[3]

DMI

FDI_TXN0 A21 FDI0_TX#[0]
FDI_TXN1 H19 FDI0_TX#[1]
FDI_TXN2 E19 FDI0_TX#[2]
FDI_TXN3 F18 FDI0_TX#[3]
FDI_TXN4 B21 FDI1_TX#[0]
FDI_TXN5 C20 FDI1_TX#[1]
FDI_TXN6 D18 FDI1_TX#[2]
FDI_TXN7 E17 FDI1_TX#[3]
FDI_TXP0 A22 FDI0_TX[0]
FDI_TXP1 G19 FDI0_TX[1]
FDI_TXP2 E20 FDI0_TX[2]
FDI_TXP3 G18 FDI0_TX[3]
FDI_TXP4 B20 FDI1_TX[0]
FDI_TXP5 C19 FDI1_TX[1]
FDI_TXP6 D19 FDI1_TX[2]
FDI_TXP7 F17 FDI1_TX[3]
FDI_FSYNC0 J18 FDI0_FSYNC
FDI_FSYNC1 J17 FDI1_FSYNC
FDI_INT H20 FDI_INT
FDI_LSYNC0 J19 FDI0_LSYNC
FDI_LSYNC1 H17 FDI1_LSYNC

Intel(R) FDI

eDP_COMP A18 eDP_COMPIO
INT_eDP_HPD_Q A17 eDP_ICOMPO
B16 eDP_HPD
C15 eDP_AUX
D15 eDP_AUX#
C17 eDP_TX[0]
F16 eDP_TX[1]
C16 eDP_TX[2]
G15 eDP_TX[3]
C18 eDP_TX#[0]
E16 eDP_TX#[1]
D16 eDP_TX#[2]
F15 eDP_TX#[3]

eDP

Sandy Bridge_rPGA_Rev0p61
rpga989-47989-socket
DGG^9000005
IC SOCKET RPGA 989P(P1.0,M/H3.0)

eDP_COMP connect to PIN A18 W:4mils/S:15mils/L: 500mils.
eDP_COMP connect to PIN A17 W:12mils/S:15mils/L: 500mils.

PCI EXPRESS* - GRAPHICS

PEG_ICOMPI J22 PEG_COMP
PEG_ICOMPO J21
PEG_RCOMPO H22

PEG_COMP connect to PIN H22&J22 W:4mils/S:15mils/L: 500mils.
PEG_COMP connect to PIN J21 W:12mils/S:15mils/L: 500mils.

PEG_RX#[0..7] 14
K33 PEG_RX#0
M35 PEG_RX#1
L34 PEG_RX#2
J35 PEG_RX#3
J32 PEG_RX#4
H34 PEG_RX#5
H31 PEG_RX#6
G33 PEG_RX#7

PEG_RX[0..7] 14
J33 PEG_RX0
L35 PEG_RX1
K34 PEG_RX2
H35 PEG_RX3
H32 PEG_RX4
G34 PEG_RX5
G31 PEG_RX6
F33 PEG_RX7

M29 C_PEG_TX#0
M32 C_PEG_TX#1
M31 C_PEG_TX#2
L32 C_PEG_TX#3
L29 C_PEG_TX#4
K31 C_PEG_TX#5
K28 C_PEG_TX#6
J30 C_PEG_TX#7

M28 C_PEG_TX0
M33 C_PEG_TX1
M30 C_PEG_TX2
L31 C_PEG_TX3
L28 C_PEG_TX4
K30 C_PEG_TX5
K27 C_PEG_TX6
J29 C_PEG_TX7

U15B

SNB_IVB# N.A at SNB EDS #27637 0.7v1

7 H_SNB_IVB# C26 SNB_IVB#
TP4 SKTOCC# AN34 SKTOCC#

MISC

TP2 TP_CATERR# AL33 CATERR#

Placement close to EC.

29 EC_PECI R386 43_4 H_PECI AN33 PECI
29,33 H_PROCHOT# R146 56.2/F_4 H_PROCHOT#_R AL32 PROCHOT#
9,29 PM_THRMTRIP# R148 0_4 PM_THRMTRIP#_R AN32 THERMTRIP#

THERMAL

6 PM_SYNC R377 0_4 PM_SYNC_R AM34 PM_SYNC
9 H_PWRGOOD R378 0_4 H_PWRGOOD_R AP33 UNCOREPWRGOOD
R384 10K_4
PM_DRAM_PWRGD_R V8 SM_DRAMPWROK
CPU_PLTRST#_R AR33 RESET#

PWR MANAGEMENT

9/15 SI for H/W.

CPU RESET#

8,14,24,27,29,30 PLTRST#
U18 GND OUT IN NC VCC *74LVC1G07GW
+1.05V_VTT R404 *75/F_4
CPU_PLTRST# R400 *43_4
+3VS5 C560 0.1U/10V_4
R401 750/F_4
R402 1.5K/F_4

SM_DRAMPWROK Processor Input.

Sandy Bridge_rPGA_Rev0p61
rpga989-47989-socket
DGG^9000005
IC SOCKET RPGA 989P(P1.0,M/H3.0)

BCLK A28 CLK_CPU_BCLKP 8
BCLK# A27 CLK_CPU_BCLKN 8
DPLL_REF_SSCLK A16 CLK_DPLL_SSCLKP
DPLL_REF_SSCLK# A15 CLK_DPLL_SSCLKN

CLOCKS

SM_DRAMRST# R8 CPU_DRAMRST#
SM_RCOMP[0] AK1 SM_RCOMP_0 R143 140/F_4
SM_RCOMP[1] A5 SM_RCOMP_1 R318 26.1/F_4
SM_RCOMP[2] A4 SM_RCOMP_2 R316 200/F_4

DDR3 MISC

SM_RCOMP[0] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[1] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[2] W:15mils/S:20mils/L: 500mils,

PRDY# AP29 XDP_PRDY#
PREQ# AP27 XDP_PREQ#
TCK AR26 XDP_TCLK
TMS AR27 XDP_TMS
TRST# AP30 XDP_TRST#
TDI AR28 XDP_TDI_R
TDO AP26 XDP_TDO
DBR# AL35 XDP_DBRST#
BPM#[0] AT28 XDP_BPM0
BPM#[1] AR29 XDP_BPM1
BPM#[2] AR30 XDP_BPM2
BPM#[3] AT30 XDP_BPM3
BPM#[4] AP32 XDP_BPM4
BPM#[5] AR31 XDP_BPM5
BPM#[6] AT31 XDP_BPM6
BPM#[7] AR32 XDP_BPM7

CPU XDP
TP12 TP11 TP8 TP10 TP13 TP39 TP7 TP40 TP41 TP43 TP42 TP5 TP45 TP44 TP46

R375 *1K_4 +3V
XDP_DBRST# 6

JTAG & BPM

DDR3 DRAM RESET

+1.5VSUS R311 1K_4 R313 *0_4
12,13 DDR3_DRAMRST# R312 1K_4
CPU_DRAMRST#
CPU_DRAMRST#_R
8 DRAMRST_CNTRL_PCH R315 0_4
Q24 2N7002
R314 4.99K/F_4
C442 0.047U/10V_4

+3VS5 R49 10K_4 PM_DRAM_PWRGD_PU
U2 NC VCC IN GND OUT *74LVC1G07GW
C27 0.1U/10V_4
+1.5V_CPU
R40 200/F_4
PM_DRAM_PWRGD_C R42 130/F_4 PM_DRAM_PWRGD_R
R37 *39_4
R48 *0_4
PM_DRAM_PWRGD 6
R47 0_4 PM_DRAM_PWRGD_R
Q3 *2N7002
MAIN_ONG 4,38
R43 *3K/F_4

+1.05V_VTT 4,6,7,8,10,29,32,33
+1.5V_CPU 4
+3VS5 6,7,8,9,10,22,26,31,32,38,39
+3V 6,7,8,9,10,12,13,14,17,20,21,22,23,24,25,27,28,29,30,33,38,39

FDI disable (DIS only stuff)

DEL

FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (DG V0.5 Ch2.2.9).

PEG x16 disable (UMA only remove)

14 PEG_TX[0..7]

C_PEG_TX0	C483	0.1U/10V_4	PEG_TX0
C_PEG_TX1	C489	0.1U/10V_4	PEG_TX1
C_PEG_TX2	C492	0.1U/10V_4	PEG_TX2
C_PEG_TX3	C498	0.1U/10V_4	PEG_TX3
C_PEG_TX4	C501	0.1U/10V_4	PEG_TX4
C_PEG_TX5	C504	0.1U/10V_4	PEG_TX5
C_PEG_TX6	C508	0.1U/10V_4	PEG_TX6
C_PEG_TX7	C512	0.1U/10V_4	PEG_TX7

14 PEG_TX#[0..7]

C_PEG_TX#0	C488	0.1U/10V_4	PEG_TX#0
C_PEG_TX#1	C490	0.1U/10V_4	PEG_TX#1
C_PEG_TX#2	C496	0.1U/10V_4	PEG_TX#2
C_PEG_TX#3	C500	0.1U/10V_4	PEG_TX#3
C_PEG_TX#4	C503	0.1U/10V_4	PEG_TX#4
C_PEG_TX#5	C507	0.1U/10V_4	PEG_TX#5
C_PEG_TX#6	C511	0.1U/10V_4	PEG_TX#6
C_PEG_TX#7	C517	0.1U/10V_4	PEG_TX#7

0.22uF AC coupling Caps for PCIE GEN1/2/3

0.22uF AC coupling Caps for PCIE GEN1/2/3

Embedded Display PLL Clock

Ra

3/26 DB change
Part reference.

CLK_DPLL_SSCLKP CLK_DPLL_SSCLKP 8
CLK_DPLL_SSCLKN CLK_DPLL_SSCLKN 8

DEL

	Ra	Rb	Rc
DIS	NC	Stuff	Stuff
SG/UMA	Stuff	NC	NC

DP & PEG Compensation

+1.05V_VTT R67 10K_4 INT_eDP_HPD_Q
+1.05V_VTT R319 24.9/F_4 eDP_COMP

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

+1.05V_VTT R85 24.9/F_4 PEG_COMP

PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms PEG_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

Processor pull-up (CPU)

+1.05V_VTT

H_PROCHOT#	R145	62_4
XDP_TDO	R155	51_4
XDP_TMS	R159	51_4
XDP_TDI_R	R403	51_4
XDP_PREQ#	R158	*51_4
XDP_TCLK	R156	51_4
XDP_TRST#	R163	51_4

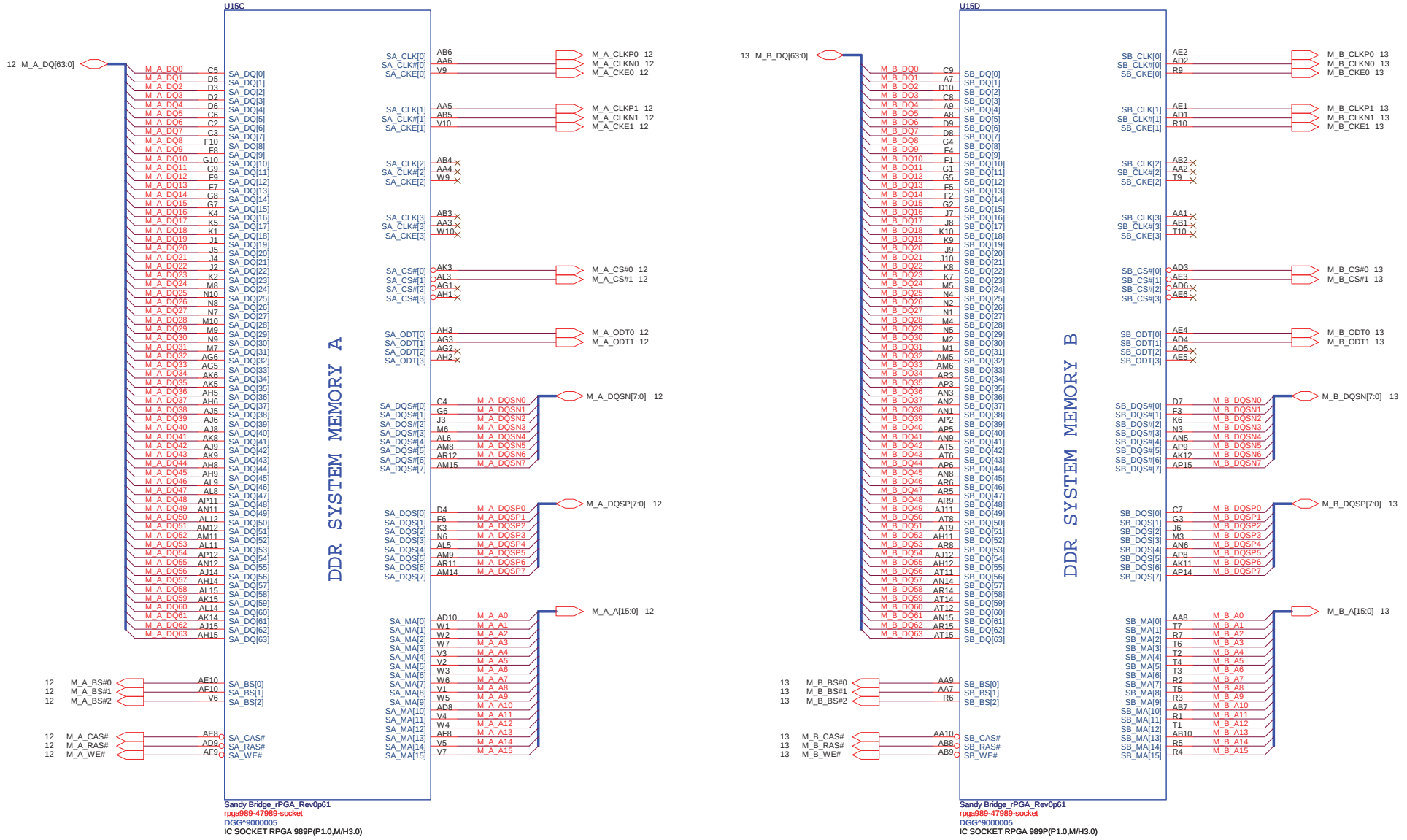
NB5

PROJECT : R13
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SNB 1/4 (PCIE&DMI&FDI)	3A

Date: Saturday, September 18, 2010 Sheet 2 of 39

Sandy Bridge Processor (DDR3)



NB5

PROJECT : R13
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SNB 2/4 (DDR3 I/F)	1A

Date: Saturday, September 18, 2010 | Sheet 3 of 39

Sandy Bridge Processor (POWER)

Sandy Bridge Processor (GRAPHIC POWER)

04

CORE SUPPLY

SNB: 55A

+VCC_CORE

U15F

C493 22U/6.3VS_8
C521 10U/6.3VS_6
C516 22U/6.3VS_8
C42 22U/6.3VS_8
C36 22U/6.3VS_8
C174 22U/6.3VS_8
C509 22U/6.3VS_8
C172 22U/6.3VS_8
C263 22U/6.3VS_8
C300 22U/6.3VS_8
C39 22U/6.3VS_8
C502 22U/6.3VS_8
C177 22U/6.3VS_8
C527 *10U/6.3V_6S
C33 22U/6.3VS_8
C151 22U/6.3VS_8
C286 22U/6.3VS_8
C283 22U/6.3VS_8
C237 22U/6.3VS_8
C242 22U/6.3VS_8
C163 22U/6.3VS_8
C535 *22U/6.3VS_8
C220 *22U/6.3VS_8
C447 22U/6.3VS_8
C173 22U/6.3VS_8
C515 10U/6.3VS_6
C270 22U/6.3VS_8
C450 22U/6.3VS_8
C451 22U/6.3VS_8
C542 *10U/6.3V_6S

22uF_8 x8 Socket TOP cavity
22uF_8 x10 Socket BOT cavity
22uF_8 x8 Socket TOP edge
470uF_7343 x4

3/26 DB change 10U FP to 0805.

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71 VCC72 VCC73 VCC74 VCC75 VCC76 VCC77 VCC78 VCC79 VCC80 VCC81 VCC82 VCC83 VCC84 VCC85 VCC86 VCC87 VCC88 VCC89 VCC90 VCC91 VCC92 VCC93 VCC94 VCC95 VCC96 VCC97 VCC98 VCC99 VCC100

PEG AND DDR

SNB: 8.5A

+1.05V_VTT

VCCIO1 VCCIO2 VCCIO3 VCCIO4 VCCIO5 VCCIO6 VCCIO7 VCCIO8 VCCIO9 VCCIO10 VCCIO11 VCCIO12 VCCIO13 VCCIO14 VCCIO15 VCCIO16 VCCIO17 VCCIO18 VCCIO19 VCCIO20 VCCIO21 VCCIO22 VCCIO23 VCCIO24 VCCIO25 VCCIO26 VCCIO27 VCCIO28 VCCIO29 VCCIO30 VCCIO31 VCCIO32 VCCIO33 VCCIO34 VCCIO35 VCCIO36 VCCIO37 VCCIO38 VCCIO39 VCCIO40

C145 22U/6.3VS_8
C147 22U/6.3VS_8
C482 22U/6.3VS_8
C260 22U/6.3VS_8
C180 22U/6.3VS_8
C166 22U/6.3VS_8
C146 *22U/6.3VS_8
C215 22U/6.3VS_8
C526 22U/6.3VS_8
C532 *22U/6.3VS_8
C200 *22U/6.3VS_8
C61 *22U/6.3VS_8
C491 22U/6.3VS_8
C66 *22U/6.3VS_8
5/14 modify
C282 *22U/6.3VS_8
C167 *22U/6.3VS_8
C506 22U/6.3VS_8
C236 *22U/6.3VS_8
C513 *22U/6.3VS_8
C499 22U/6.3VS_8
C158 22U/6.3VS_8

22uF_8 x7 Socket TOP cavity
22uF_8 x5 Socket BOT cavity
22uF_8 x2 Socket TOP cavity (no stuff)
22uF_8 x5 Socket BOT cavity (no stuff)
330uF_7343 x2

J23

+1.05V_VTT_40 R86 *0_4/S +1.05V_VTT

SVID

VIDALERT# AJ29 H_CPU_SVIDALRT#
VIDSCLK AJ30 H_CPU_SVIDCLK
VIDSOUT AJ28 H_CPU_SVIDDAT

SENSE LINES

VCC_SENSE AJ35
VSS_SENSE AJ34

R136 100_4 +VCC_CORE
VCC_SENSE 33
VSS_SENSE 33
R139 100_4

VCCIO_SENSE B10
VSSIO_SENSE A10
VSSP_SENSE
VCCP_SENSE 32
VSSP_SENSE 32

Trace Route to Power IC area.

+VCC_CORE 22,34
+VCC_GFX 34
+VCCSA 36
+1.05V_VTT 2,6,7,8,10,29,32,33
+1.5V_CPU 2
+1.5V_CPU 2
+1.5VSUS 2,10,12,13,22,35,39

Sandy Bridge_rPGA_Rev0p61
rpga989-47989-socket
DGG^9000005
IC SOCKET RPGA 989P(P1.0,M/H3.0)

GRAPHICS

22uF_8 x2 Socket TOP cavity
22uF_8 x2 Socket BOT cavity
22uF_8 x4 Socket TOP edge
22uF_8 x4 Socket BOT edge
470uF_7343 x2

+VCC_GFX SNB: 21.5A

C529 22U/6.3V_8
C264 22U/6.3V_8
C285 22U/6.3V_8
C299 22U/6.3V_8
C284 22U/6.3V_8
C530 22U/6.3V_8
C301 22U/6.3V_8
C238 22U/6.3V_8
C528 22U/6.3V_8
C239 22U/6.3V_8
C265 22U/6.3V_8
C531 22U/6.3V_8

DEL

	DIS	SG/UMA
Ra	Stuff	NC

U15G

VAXG1 VAXG2 VAXG3 VAXG4 VAXG5 VAXG6 VAXG7 VAXG8 VAXG9 VAXG10 VAXG11 VAXG12 VAXG13 VAXG14 VAXG15 VAXG16 VAXG17 VAXG18 VAXG19 VAXG20 VAXG21 VAXG22 VAXG23 VAXG24 VAXG25 VAXG26 VAXG27 VAXG28 VAXG29 VAXG30 VAXG31 VAXG32 VAXG33 VAXG34 VAXG35 VAXG36 VAXG37 VAXG38 VAXG39 VAXG40 VAXG41 VAXG42 VAXG43 VAXG44 VAXG45 VAXG46 VAXG47 VAXG48 VAXG49 VAXG50 VAXG51 VAXG52 VAXG53 VAXG54

1.8V RAIL

SNB: 1.5A

+1.8V

VCCPLL1 B6
VCCPLL2 A6
VCCPLL3 A2

C449 10U/6.3V_8
C441 1U/6.3V_4
C443 1U/6.3V_4
C440 330U/2V_7343

330uF x1, 10uF_8 x1, 1uF_4 x2 Socket BOT edge.

Sandy Bridge_rPGA_Rev0p61
rpga989-47989-socket
DGG^9000005
IC SOCKET RPGA 989P(P1.0,M/H3.0)

SENSE LINES

VAXG_SENSE AK35
VSSAXG_SENSE AK34

R140 100_4 +VCC_GFX
VCC_AXG_SENSE 33
VSS_AXG_SENSE 33
R142 100_4

VREF

SM_VREF AL1

+VDDR_REF_CPU

CAD Note: +VDDR_REF_CPU should have 10 mil trace width

R28 *0_8 DDR_VTTREF 12,13,35
R31 100K_4
Q2 2N7002
MAIND MAIND 38

DDR3 -1.5V RAILS

VDDQ1 AF7
VDDQ2 AF4
VDDQ3 AF1
VDDQ4 AC7
VDDQ5 AC4
VDDQ6 AC1
VDDQ7 Y7
VDDQ8 Y4
VDDQ9 Y1
VDDQ10 U7
VDDQ11 U4
VDDQ12 U1
VDDQ13 P7
VDDQ14 P4
VDDQ15 P1

SNB: 5A +1.5V_CPU

C297 10U/6.3V_6
C214 10U/6.3V_8
C289 10U/6.3V_6
C268 10U/6.3V_6

4/27: layout modify

9/10 SI for H/W.

C190 10U/6.3V_6
C305 10U/6.3V_6
C576 *330U_2.5V_5.0x5.9_ESR10m

330uF x1, 10uF_8 x6 Socket BOT edge.

SA RAIL

SNB: 6A +VCCSA

VCCSA1 M27
VCCSA2 M26
VCCSA3 J26
VCCSA4 J25
VCCSA5 J24
VCCSA6 H26
VCCSA7 H25
VCCSA8 H25

C485 10U/6.3V_8
C448 10U/6.3V_8
C484 10U/6.3V_8
C445 *10U/6.3V_8

330uF x1, 10uF_8 x1 Socket BOT edge, 10uF_8 x2 Socket BOT cavity.

MISC

VCCSA_SENSE H23
VCCUSA_SENSE_R R82 0_4 VCCUSA_SENSE 36

FC_C22 C22
VCCSA_VID1 C24
H_FC_C22 R77 10K_4 VCCSA_SEL 36

R81 10K_4

5/11: Add for intel CRB

+1.5V_CPU R310 *0_8/S +1.5V

40mile routing

Layout note: need routing together and ALERT need between CLK and DATA.

SVID CLK

Place PU resistor close to VR

R309 *54.9/F_4 +1.05V_VTT
H_CPU_SVIDCLK VR_SVID_CLK 33

SVID DATA

+1.05V_VTT +1.05V_VTT

Place PU resistor close to CPU
R137 130/F_4
H_CPU_SVIDDAT

R308 *130/F_4
Place PU resistor close to VR

VR_SVID_DATA 33

SVID ALERT

Place PU resistor close to CPU

+1.05V_VTT R26 75/F_4
H_CPU_SVIDALRT# R25 43_4 VR_SVID_ALERT# 33

CPU VDDQ

+1.5VSUS +1.5V_CPU +1.5VSUS

Q36 AON7410
R185 220_8
MAIND
C438 *470P/50V_4
Q16 2N7002
MAIN_ONG 2,38

C455 0.1U/10V_4
C452 0.1U/10V_4
C554 0.1U/10V_4
C558 0.1U/10V_4

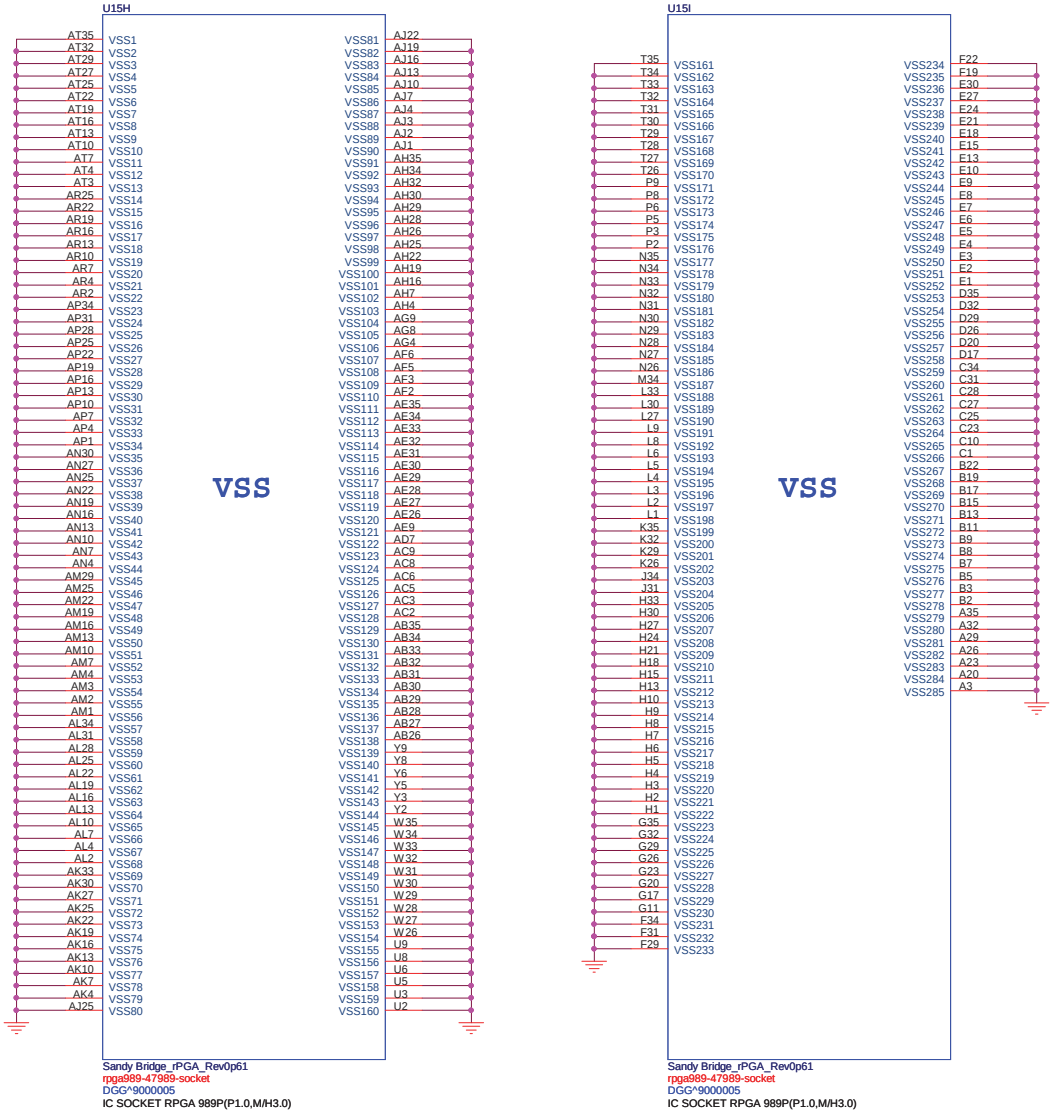
3/26 DB add for Intel. Placement close to CPU.

PROJECT : R13
Quanta Computer Inc.

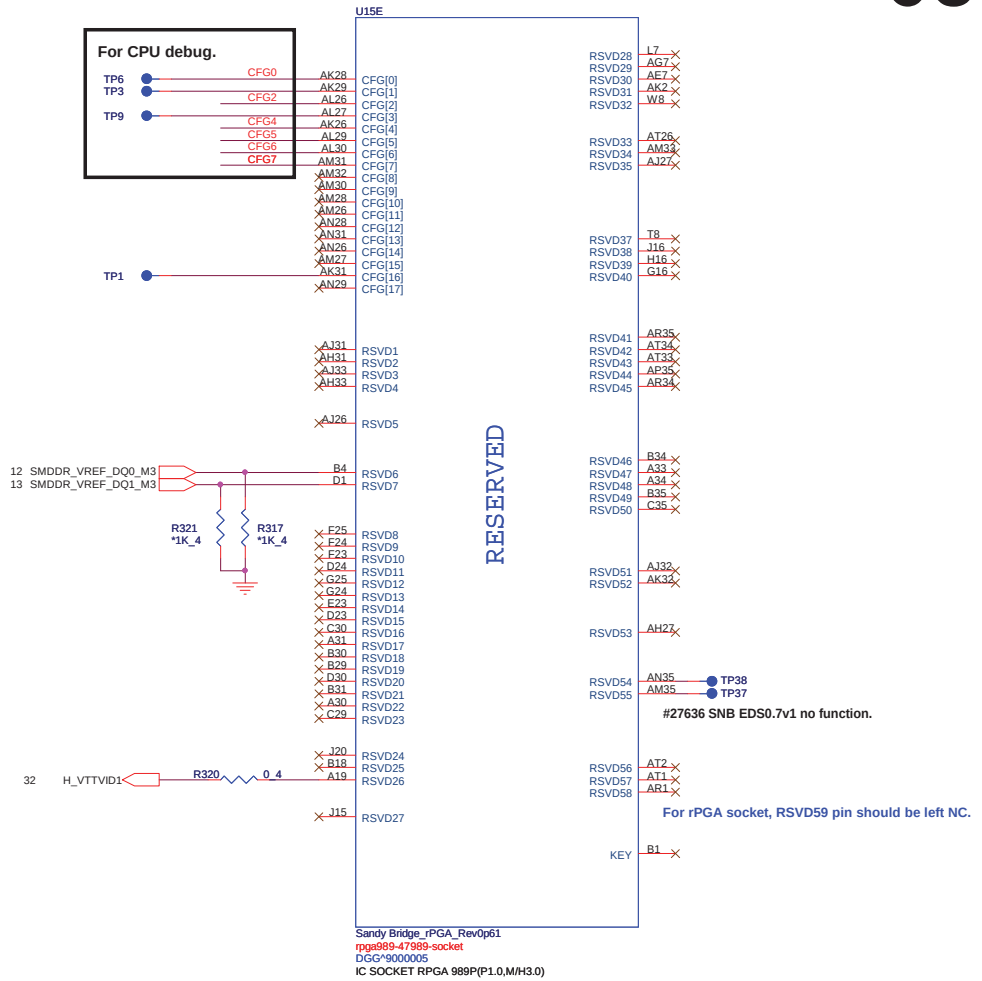
NB5

Size	Document Number	Rev
Custom	SNB 3/4 (POWER)	1A
Date: Saturday, September 18, 2010	Sheet 4 of 39	

Sandy Bridge Processor (GND)



Sandy Bridge Processor (RESERVED, CFG)



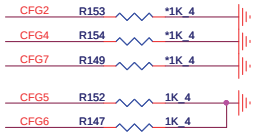
Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



NB5

PROJECT : R13
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SNB 4/4 (GND)	1A

Date: Saturday, September 18, 2010 | Sheet 5 of 39

Cougar Point (DMI,FDI,PM)

Cougar Point (LVDS,DDI)

06

U24C

U24D

DMI

FDI

System Power Management

LVDS

Digital Display Interface

CRT

INT. HDMI

9/10 SI for H/W.

PD Res place close to PCH

PCH to Res routeing 50 ohm Impedance.

Res to connector filter routeing 37.5ohm Impedance.

9/3 SI for H/W.

Reserve for R13 power on sequence

CougarPoint_Rev_0p7

fcbga989-intel-cougarpoint

AJ0QMZQ0T00

IC CTRL(989P)COUGARPOINT QMVY TOP B/S

+1.05V_VTT 2,4,7,8,10,29,32,33

+3V_RTC 7,10

+3V_DSW

+3VPCU 7,20,28,29,31,37

+3VS5 2,7,8,9,10,22,26,31,32,38,39

+3V 2,7,8,9,10,12,13,14,17,20,21,22,23,24,25,27,28,29,30,33,38,39

+5V 7,10,17,21,22,23,25,28,30,38

PCH Pull-high/low(CLG)

INT HDMI disable (DIS only remove)

INT HDMI Detect Function

System PWR_OK(CLG)

On Die DSW VR Enable

High = Enable (Default)

Low = Disable

DPWROK FOR DSW

9/10 SI for EE

Remove DSW power rail

PROJECT : R13

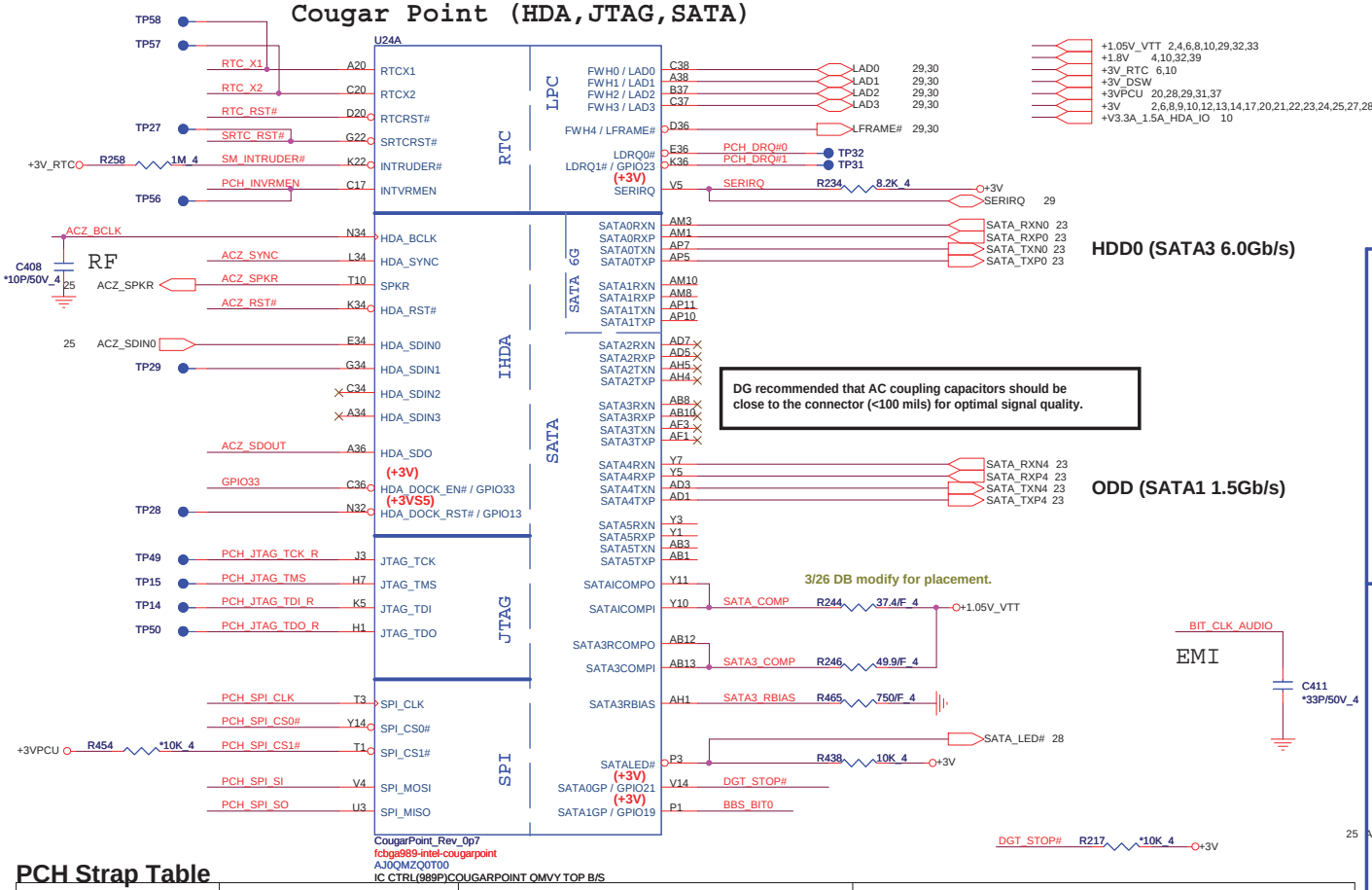
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	PCH 1/6 (DMI/FDI/VIDEO)	1A

Date: Saturday, September 18, 2010 Sheet 6 of 39

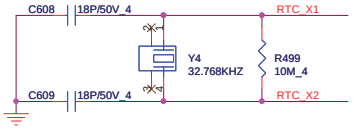
Cougar Point (HDA,JTAG,SATA)



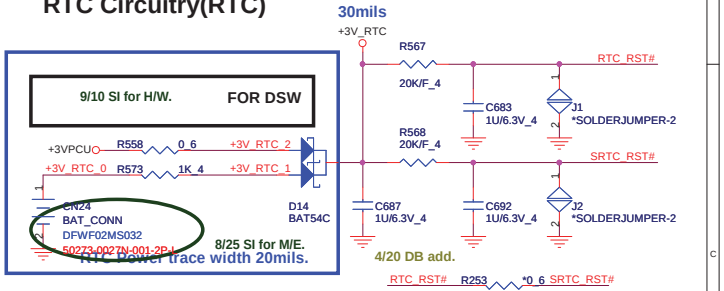
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR (Different from Calpella)	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	ACZ_SPKR R435 *1K_4 +3V
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	+3V R522 *1K_4 R521 10K_4 PCI_GNT3# 8
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	PCH_INVRMEN R497 330K_4 +3V_RTC
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	GPIO33 R509 1K_4 GPIO33_E 29
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# 1, GNT0# 1 → Boot Location SPI	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#
GPIO19 (Different from Calpella)	Boot BIOS Selection 0 [bit-0]	PWROK	GNT1# 1, GNT0# 0 → Boot Location LPC	R455 *1K_4 BBS_BIT0 R523 *1K_4 BBS_BIT1 8
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	+1.8V R468 *1K_4 NV_ALE 8
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm	+1.8V R470 2.2K_4 R469 4.7K_4 NV_CLE 8 H_SNB_IVB# 2 N.A at CPT EDS 0.7
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3VS5 R278 1K_4 ACZ_SYNC
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	ACZ_SDOUT R510 *1K_4 +V3.3A_1.5A_HDA_IO
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	R483 *1K_4 ICC_EN# 9
GPIO28 (Different from Calpella)	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R447 *1K_4 PLL_ODVR_EN 9
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	PCH_SPI_SI R198 1K_4 +3V

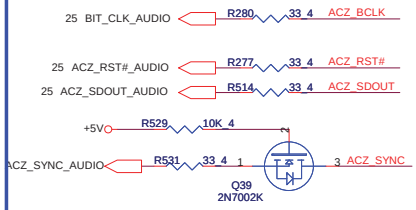
RTC Clock 32.768KHz



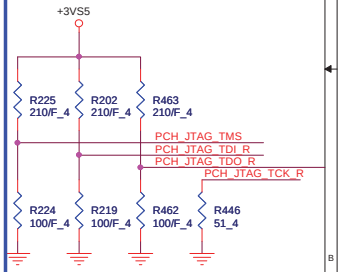
RTC Circuitry(RTC)



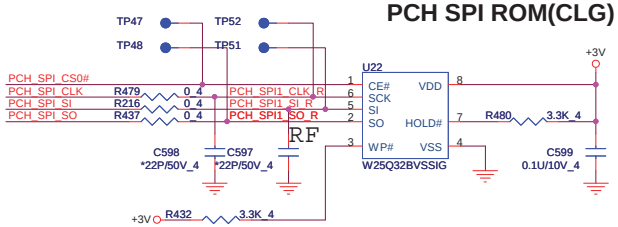
HDA Bus(CLG)



PCH JTAG Debug(CLG)



PCH SPI ROM(CLG)



Vender	Size	P/N
EON	4MB	AKE39FN0Q00 (EN25F32-100HIP)
Winbond	4MB	AKE391P0N00 (W25Q32BVSSIG)
Socket		DG008000031

PROJECT : R13
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	PCH 2/6 (SATA/HDA/SPI)	1A

Date: Saturday, September 18, 2010 | Sheet 7 of 39

Cougar Point-M (PCI,USB,NVRAM)

Cougar Point-M (PCI-E,SMBUS,CLK)

08

PCI/USBOC# Pull-up(CLG)

MPC Switch Control

MPC_PWR_CTRL#	Low = MPC ON High = MPC OFF (Default)

9/3 SI for H/W.

U24E

RSVD

NVRAM

PCI

USB

Left_USB

Left_USB 2

Webcam

Right_USB

WLAN

Blue tooth

CougarPoint_Rev_0p7
fcbga989-intel-cougarpoint
AJ0QMZQ0T00
IC CTRL(989P)COUGARPOINT QMVY TOP B/S

U24B

PCI-E*

SMBUS

Controller Link

CLOCKS

FLEX CLOCKS

WLAN

LAN

Cardreader

EMI

change 25M to small size RF

9/8 SI for TXC

Remove Ra, Rb for UMA &
SG. 27MHz support DIS only.

PLTRST#(CLG)

SMBus/Pull-up(CLG)

CLK_REQ/Strap Pin(CLG)

PEG Clock detect (SG only)

PCIE Clock

3/26 DB change Part reference.

Remove for UMA only.

SMBus/Pull-up(CLG)

PROJECT : R13
Quanta Computer Inc.

NB5

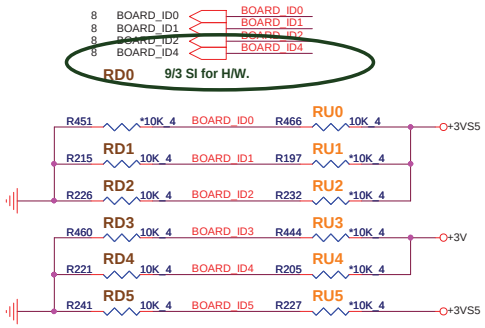
Size	Document Number	Rev
Custom	PCH 3/6 (PCIE/USB/CLK)	3A

Date: Saturday, September 18, 2010 | Sheet 8 of 39

Cougar Point (GPIO,VSS_NCTF,RSVD)

BOARD ID SETTING

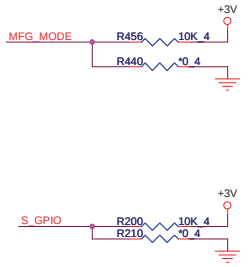
Model	BOARD_ID5	BOARD_ID4	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0
R13 UMA	0	0	0	0	0	0
R13 DIS	0	0	0	0	0	1
	0	0	0	0	0	0
	0	0	0	0	0	0
	0	0	0	0	0	0



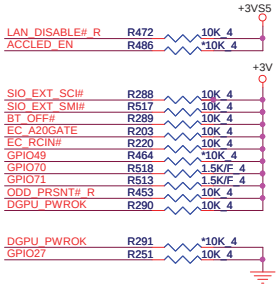
Clock Gen Power OK (CLG)

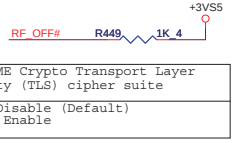
09

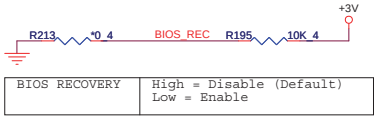
MFG-TEST

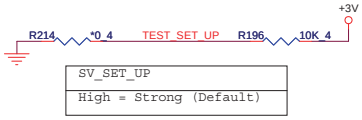


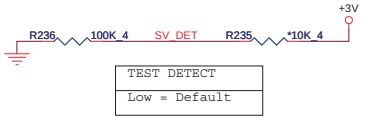
GPIO Pull-up/Pull-down(CLG)

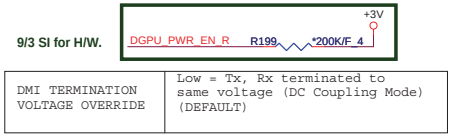


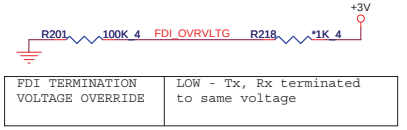




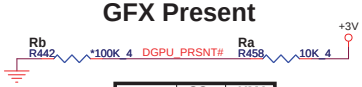








GFX Present



	SG	UMA
Stuff	Ra	Rb
NC	Rb	Ra

PROJECT : R13
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	PCH 4/6 (GPIO/MISC)	1A

Date: Saturday, September 18, 2010 Sheet 9 of 39

Cougar Point-M (POWER)

COUGAR POINT (POWER)

U24J

Clock and Miscellaneous | USB | PCI/GPIO/LPC | SATA | MISC | CPU | RTC | HDA

U24G

CRT | VCC CORE | LVDS | HVCMOS | VCCIO | DMI | NAND / SPI | FDI

CougarPoint_Rev_0p7
fcbga989-intel-cougarpoint
AJ0QMZQ0T00
IC CTRL(989P)COUGARPOINT QMVY TOP B/S

9/10 SI for H/W.

9/15 SI for EE

UMA Only, If have power noise issue then stuff it.

U29 G910T21U

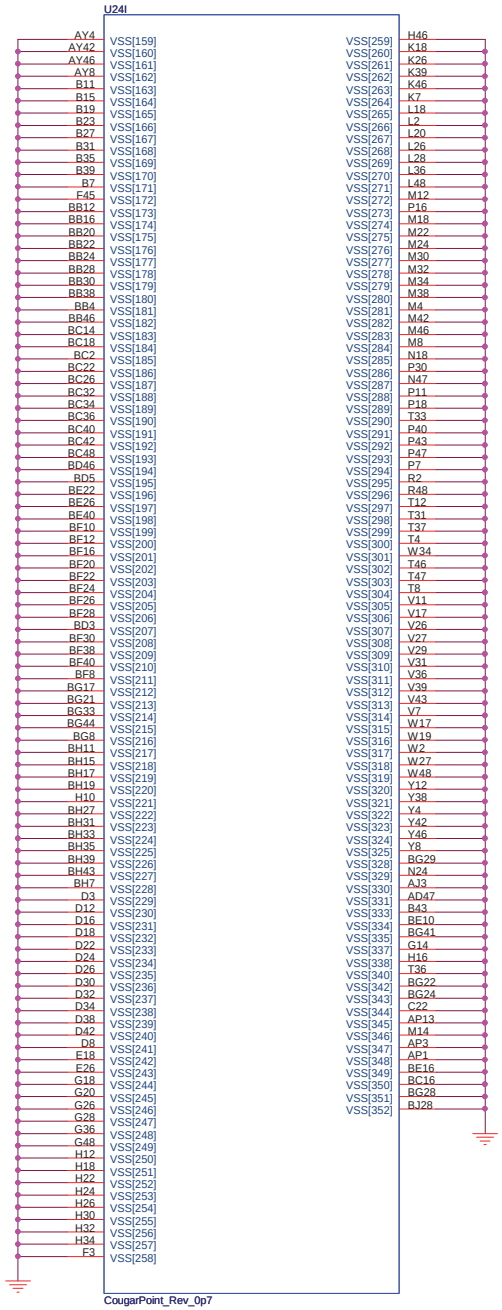
9/15 SI for EE

+1.05V_VTT 2,4,6,7,8,29,32,33
+1.5VSUS 2,4,12,13,22,35,39
+1.8V 4,7,32,39

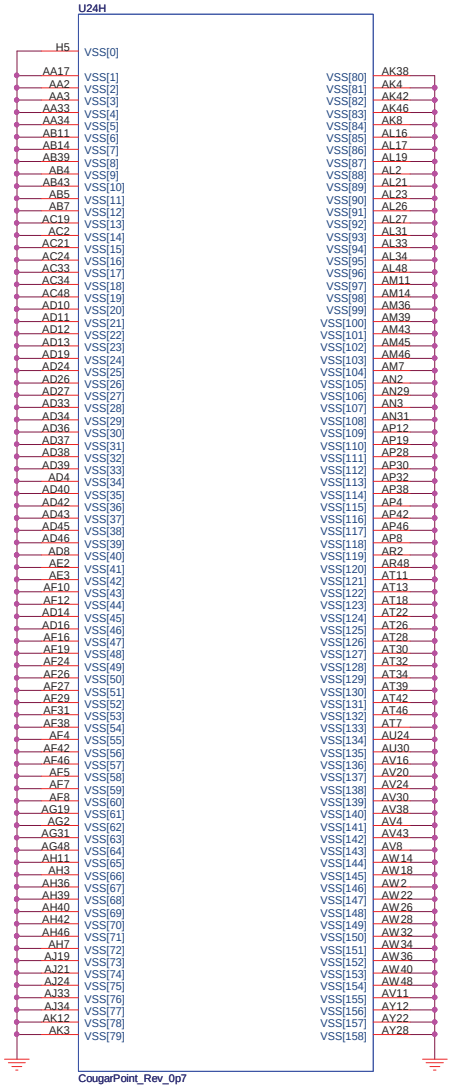
+3V_RTC 6,7
+3V_DSW
+3VS5 2,6,7,8,9,22,26,31,32,38,39
+3V 2,6,7,8,9,12,13,14,17,20,21,22,23,24,25,27,28,29,30,33,38,39
+5VS5 20,26,31,32,33,34,35,36,38,39
+5V 6,7,17,21,22,23,25,28,30,38

PROJECT : R13
Quanta Computer Inc.
NB5
Size: Custom | Document Number: PCH 5/6 (POWER) | Rev: 3A
Date: Saturday, September 18, 2010 | Sheet 10 of 39

IBEX PEAK-M (GND)



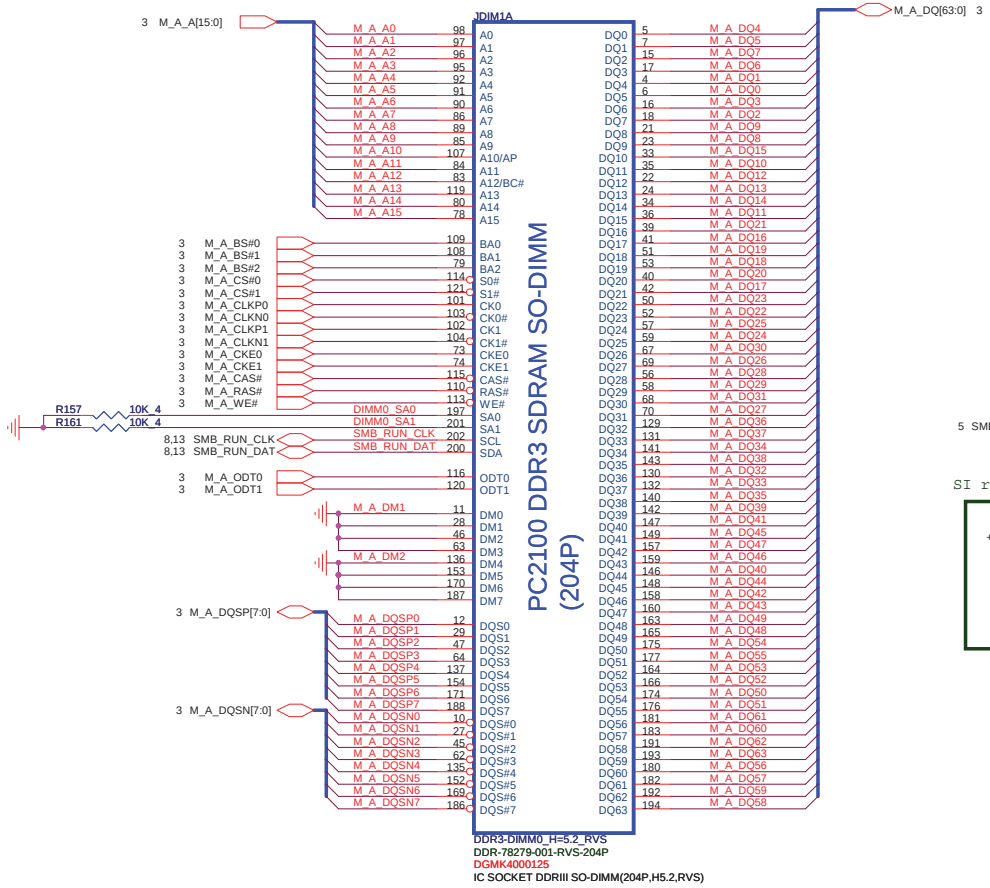
IBEX PEAK-M (GND)

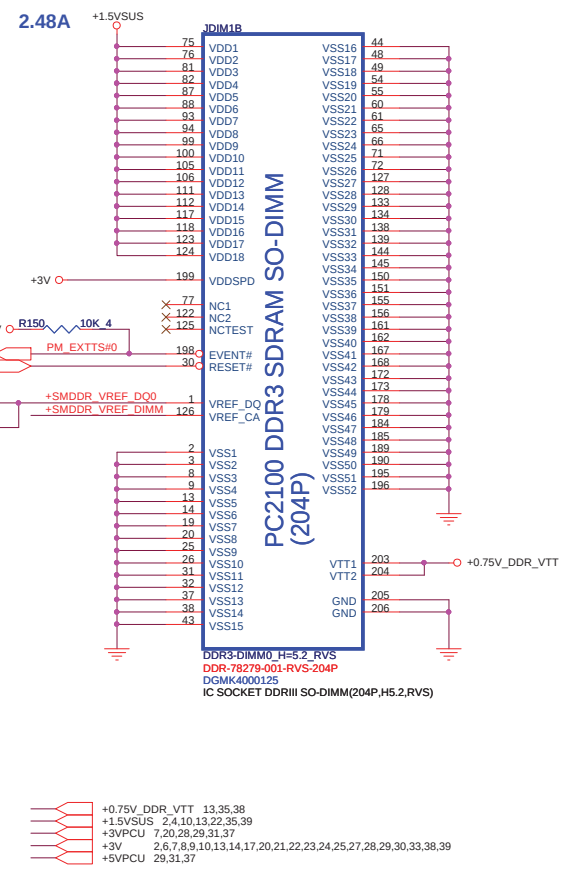


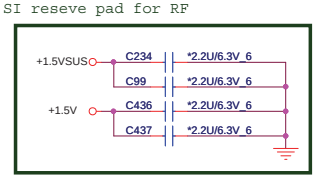
NB5

PROJECT : R13
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 6/6 (GND)	1A
Date: Saturday, September 18, 2010	Sheet 11 of 39	



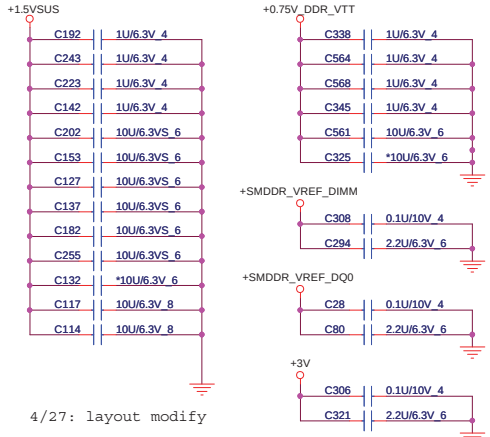




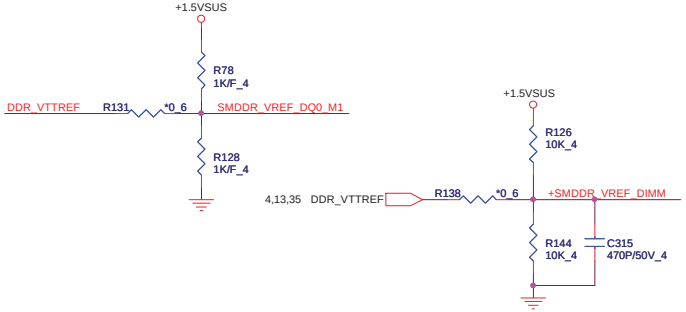
VREF DQ0 M2 Solution

del M2 solution

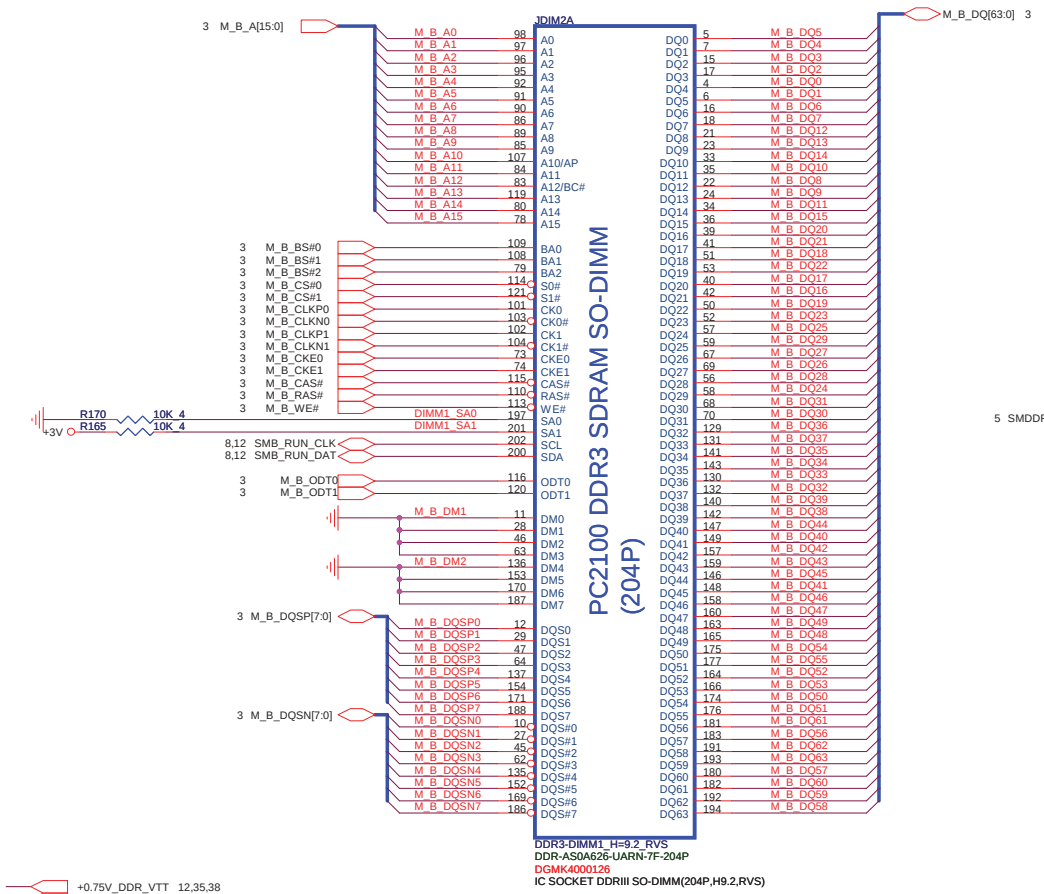
Place these Caps near So-Dimm0.

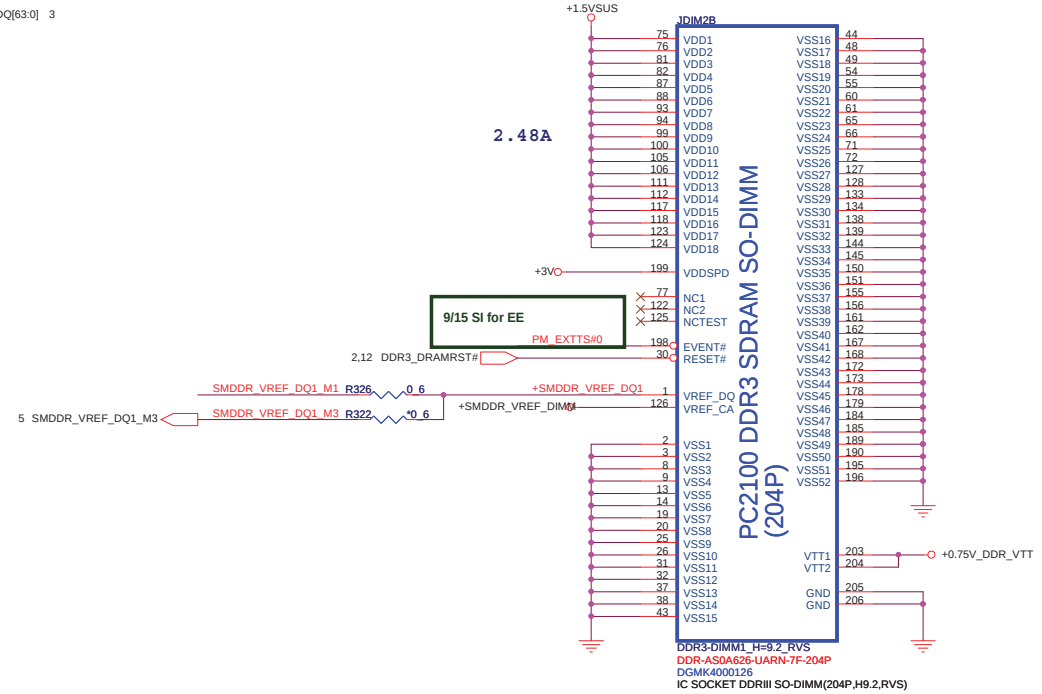


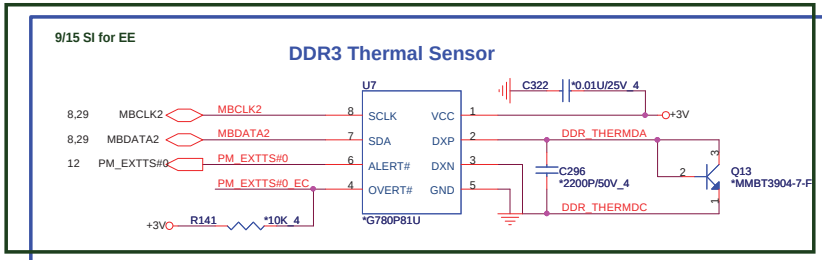
VREF DQ0 M1 Solution



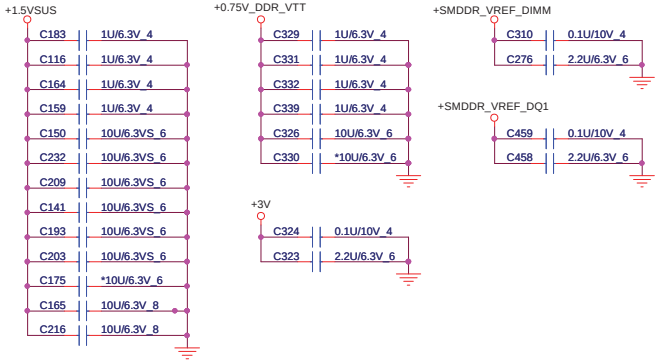
PROJECT : R13	Quanta Computer Inc.
NB5	Size: Custom; Document Number: DDR3 DIMM0-RVS (5.2H); Rev: 1A
Date: Saturday, September 18, 2010	Sheet 12 of 39

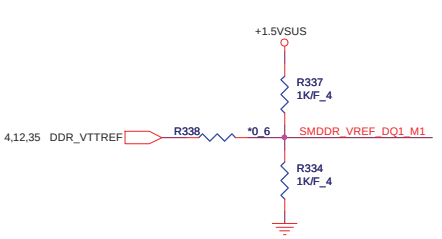






del M2 solution



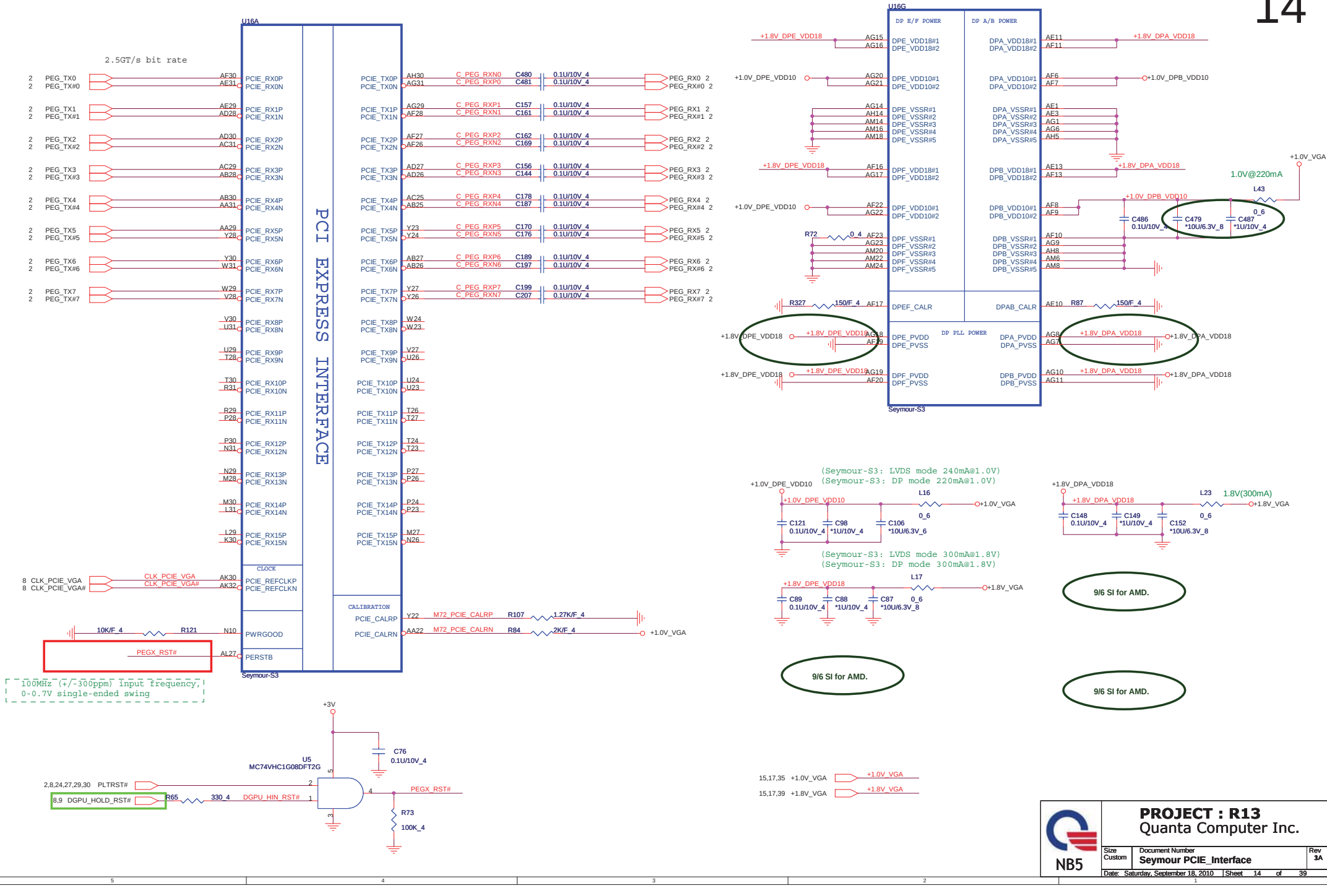


NB5

PROJECT : R13
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM1-RVS (9.2H)	1A

Date: Saturday, September 18, 2010 Sheet 13 of 39



NB5	PROJECT : R13 Quanta Computer Inc.	
Size: Custom	Document Number: Seymour PCIE_Interface	Rev: 1A
Date: Saturday, September 18, 2010	Sheet 14 of 39	

MEM_ID[3:0]	Vendor	Type	Vendor P/N
0000	Samsung- E die	64*16-800MHZ	K4W1G1646E-HC12
0001	Hynix- Vega die	64*16-800MHZ	H5TQ1G63DFR-12C
0010	Hynix- Vega die	128*16-800MHZ	H5TQ2G63BFR-12C
0011	Samsung- C die	128*16-800MHZ	K4W2G1646C-HC12
0100	Micron	128*16-800MHZ	MT41J128M16HA-125:D
0101	Reserved		
0110	Hynix- Vega die	64*16-900MHZ	H5TQ1G63DFR-11C
0111	Samsung- B die	64*16-900MHZ	K4W1G1646E-HC11
1000	Samsung- G die	64*16-900MHZ	K4W1G1646G-BC11
1001	Reserved		
1010	Hynix- Vega die	128*16-900MHZ	H5TQ2G63BFR-11C
1011	Samsung- C die	128*16-900MHZ	K4W2G1646C-HC11
1100	Reserved		
1101	Reserved		
1110	Reserved		
1111	Reserved		

GPIO15 GPIO20

Seymour	PWRCNTL0	PWRCNTL1	V-CORE
L	0	0	0.9V
M	0	1	1V
H	1	0	1.1V (Default)
TBD	1	1	NA

Access to SCL and SDA is mandatory on BACO designs for debug purposes

GPIO22(ROMCS#) PD without external VBIOS ROM

If no contact this pin to LVDS need pull low

Seymour uninstall Ra to meet AF24 N/C

DAC2 is NC on Seymour

Reserve for DB debug only

Reserve for DB debug only

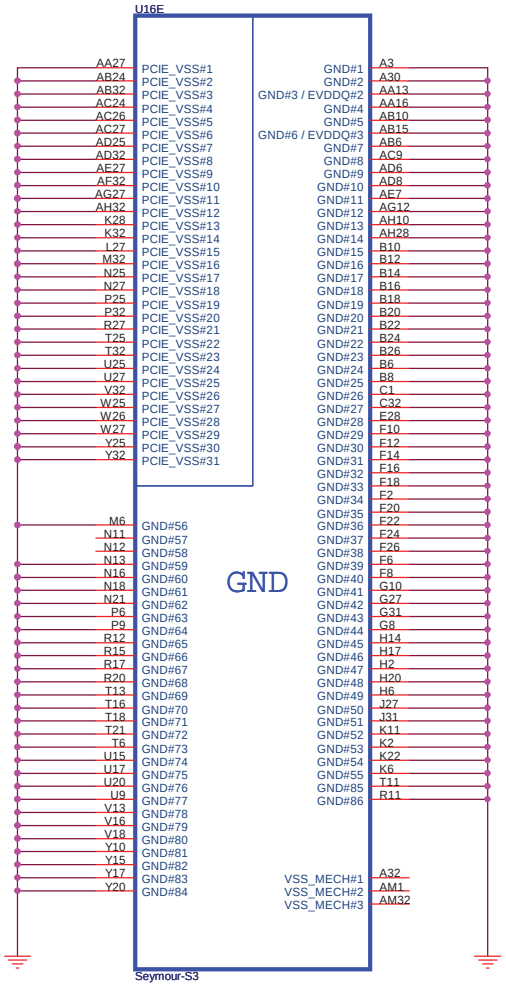
Seymour-S3--NC ROBSON--install

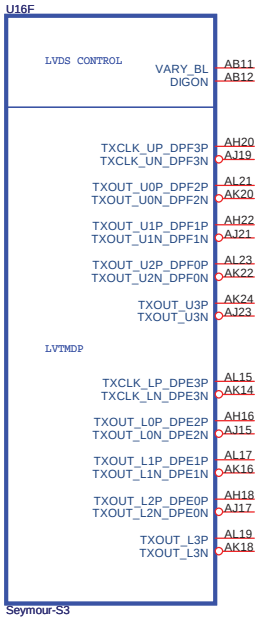
For Int Clk 27Mhz

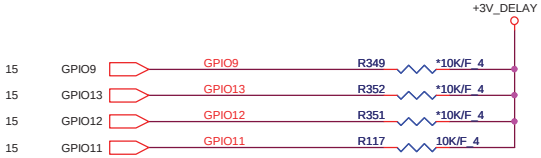
9/3 SI for H/W.

Robson-- Install Seymour- NC BACO mode -- install

PROJECT : R13
Quanta Computer Inc.
NB5
Size: Custom | Document Number: Seymour Main | Rev: 3A
Date: Saturday, September 18, 2010 | Sheet 15 of 39







CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	**Transmitter Power Savings Enable** 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	**PCI Express Transmitter De-emphasis Enable** 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

AMD RESERVED CONFIGURATION STRAPS

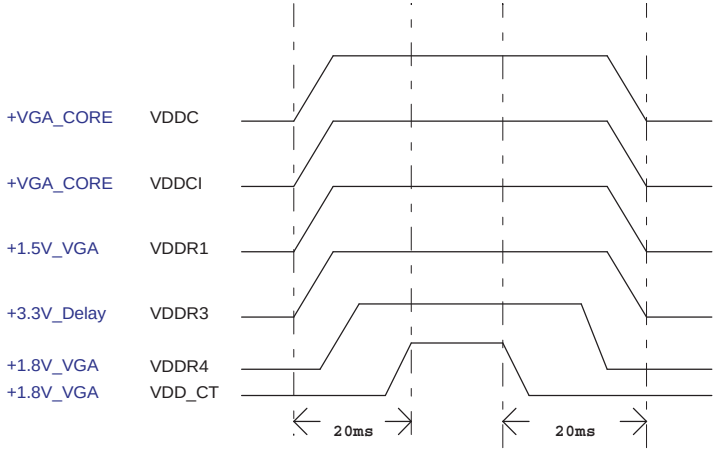
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO21_BB_EN

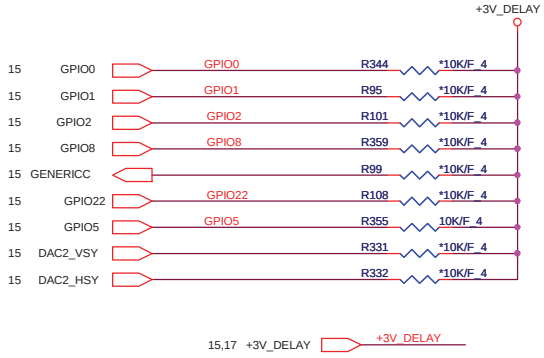
Power Up/Down Sequence



Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.



NB5

PROJECT : R13
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Seymour GND / LVDS/ Straps	3A

Date: Saturday, September 18, 2010 Sheet 16 of 39

6,7,10,21,22,23,25,28,30,38 +5V
2,6,7,8,9,10,12,13,14,20,21,22,23,24,25,27,28,29,30,33,38,39 +3V
14,15,35 +1.0V_VGA
39 +3V_VGA
39 +VGA_CORE

+5V
+3V
+1.0V_VGA
+3V_VGA
+VGA_CORE

PCIE_VDDR--PCI-E I/O power. 1.8 V ± 5%

U16D

MEM I/O
VDDR1#1 VDDR1#2 VDDR1#3 VDDR1#4 VDDR1#5 VDDR1#6 VDDR1#7 VDDR1#8 VDDR1#9 VDDR1#10 VDDR1#11 VDDR1#12 VDDR1#13 VDDR1#14 VDDR1#15 VDDR1#16 VDDR1#17

LEVEL TRANSLATION
VDD_CT#1 VDD_CT#2 VDD_CT#3 VDD_CT#4

I/O
VDDR3#1 VDDR3#2 VDDR3#3 VDDR3#4

VDDR4#1 / VDDR5
VDDR4#2
VDDR4#3 / VDDR5

NC#1 / VDDR4
DVCLK / VDDR4

NC#3 / VDDR5
NC / VDDR5

MEM CLK
VDDRHA
VSSRHA

PLL
PCIE_PVDD
MPV18
SPV18
SPV10
SPVSS

BACK BIAS
BBP#1
BBP#2

Seymour-S3

PCIE
PCIE_VDDR#1 PCIE_VDDR#2 PCIE_VDDR#3 PCIE_VDDR#4 PCIE_VDDR#5 PCIE_VDDR#6 PCIE_VDDR#7 PCIE_VDDR#8

PCIE_VDDC#1 PCIE_VDDC#2 PCIE_VDDC#3 PCIE_VDDC#4 PCIE_VDDC#5 PCIE_VDDC#6 PCIE_VDDC#7 PCIE_VDDC#8 PCIE_VDDC#9 PCIE_VDDC#10 PCIE_VDDC#11 PCIE_VDDC#12

CORE
POWER
VDDC#1 VDDC#2 VDDC#3 VDDC#4 VDDC#5 VDDC#6 VDDC#7 VDDC#8 VDDC#9 VDDC#10 VDDC#11 VDDC#12 VDDC#13 VDDC#14 VDDC#15 VDDC#16 VDDC#17 VDDC#18 VDDC#20 VDDC#21 VDDC#22
VDDC#23 /BIF_VDDC
VDDC#19/BIF_VDDC

ISOLATED CORE I/O
VDDCI#1 VDDCI#2 VDDCI#3 VDDCI#4 VDDCI#5 VDDCI#6 VDDCI#7 VDDCI#8

+1.5V_VGA

1.5V (DDR3, MVDDQ = 1.5V@2.0A)

C580 1U/10V_4 C259 1U/10V_4 C290 1U/10V_4 C277 1U/10V_4 C293 1U/10V_4
C278 10U/6.3VS_6 C295 10U/6.3VS_6 C275 10U/6.3VS_6

1.8V(110mA VDD_CT)

+1.8V_VGA L15 PBY160808T-121Y-N(120,2.5A) +1.8V_VDD_CT

C104 10U/6.3VS_6 C115 1U/10V_4 C196 1U/10V_4 C124 1U/10V_4 C205 0.1U/10V_4

Gated 3.3V
60mA by
VDDC

+3V_VGA L18 0_6 +3V_DELAY

C188 1U/10V_4 C198 1U/10V_4 C185 1U/10V_4 C103 10U/6.3VS_6

VDD_R3 --IO power for
3.3 V pins (e.g.
GPIO's). 3.3 V ± 5%

1.8V(75mA MPV18)
BLM18PG471SN1D(470,1000MA)
+1.8V_VGA L29 MPV18
C302 1U/10V_4 C304 0.1U/10V_4

1.8V(90mA SPV18)
+1.8V_VGA L28 PBY160808T-121Y-N(120,2.5A) SPV18
C291 1U/10V_4 C292 0.1U/10V_4

+VDDR4
+1.8V_VGA L24 PBY160808T-121Y-N(120,2.5A) +VDDR4
1.8V(170mA VDDR4)
C168 10U/6.3VS_6 C171 1U/10V_4 C208 0.1U/10V_4 T11

1.0V_VGA(100mA SPV10)
BLM18PG471SN1D(470,1000MA)
+1.0V_VGA L46 +1.0V_VGA_SPV10
C537 10U/6.3VS_6 C279 0.1U/10V_4 C543 1U/10V_4

+1.8V_PCIE_VDDR

1.8V(500mA)
PBY160808T-221Y-N(220,2A)
L19
+1.8V_PCIE_VDDR +1.8V_VGA
C191 0.1U/10V_4 C125 0.1U/10V_4 C131 1U/10V_4 C109 1U/10V_4 C108 1U/10V_4 C179 1U/10V_4 C110 1U/10V_4 C139 10U/6.3VS_6

+1.0V_VGA
+1.0V_PCIE_VDDC
1.0V(2.0A)
L26 0_8
+1.0V_PCIE_VDDC
C245 1U/10V_4 C235 1U/10V_4 C241 1U/10V_4 C221 1U/10V_4 C271 1U/10V_4 C273 1U/10V_4 C257 1U/10V_4 C231 10U/6.3VS_6

VDDC+VDDCI
0.85~1.1V(15A peak)(Ripple < 87.2mV)
+VGA_CORE
C250 1U/10V_4 C247 1U/10V_4 C249 1U/10V_4 C246 1U/10V_4 C228 1U/10V_4 C212 1U/10V_4 C211 1U/10V_4 C460 10U/6.3VS_6
C230 1U/10V_4 C225 2.2U/6.3V_4 C233 1U/10V_4 C258 10U/6.3V_8 C224 1U/10V_4 C204 1U/10V_4 C206 1U/10V_4
C201 1U/10V_4 C217 2.2U/6.3V_4 C210 1U/10V_4 C186 1U/10V_4 C118 1U/10V_4 C195 1U/10V_4
C70 10U/6.3VS_6 C68 10U/6.3VS_6 C119 10U/6.3VS_6 C462 10U/6.3VS_6 C461 10U/6.3VS_6 C71 10U/6.3VS_6

Note1.
BIF_VDDC R114 *0_4 +VGA_CORE
Ra

0.95V~1.1V(2A VDDCI)
+VDDCI L25 0_8 +VGA_CORE
C267 1U/10V_4 C253 1U/10V_4 C248 1U/10V_4 C218 10U/6.3VS_6 C219 10U/6.3VS_6 C262 10U/6.3VS_6

39 PX_MODE1
Q45
PX_EN 2N7002
9/9 SI for AMD
PX_MODE R783 *0_4 PX_MODE1

Support BACO Mode

+3V R372 *10K_4
39 PX_MODE R369 0_4
18 PX_EN
Q33 2N7002
R376 5.1K/F_4
9/9 SI for AMD
6,29 EC_PWROK

+3V R366 100K/F_4
Q28 2N7002
Q31 2N7002
8,9,29,35,39 DGPU_PWROK

+3V C534 0.1U/10V_4
PX_MODE
U17 TC7SH08FU
BACO_EN

+5V R383 1K_4
+5V R380 1K_4
PX_EN##
PX_EN#
Q30 2N7002
Q32 2N7002

+1.0V_VGA
Q15 AO3416
Q27 AO3416
PX_EN#
Q14 AO3416
Q29 AO3416
+VGA_CORE
PX_EN##
BIF_VDDC
C287 22U/6.3VS_8
C251 10U/6.3V_6
C266 10U/6.3V_6
C229 2.2U/6.3V_4
C213 2.2U/6.3V_4

Note1. 1. No BACO Support :BIF_VDDC shorts with VDDC (Install Ra)

2. BACO Support: Refer to the BACO reference schematics/Application note for detail about BIF_VDDC Rail if BACO is supported (Uninstall Ra)

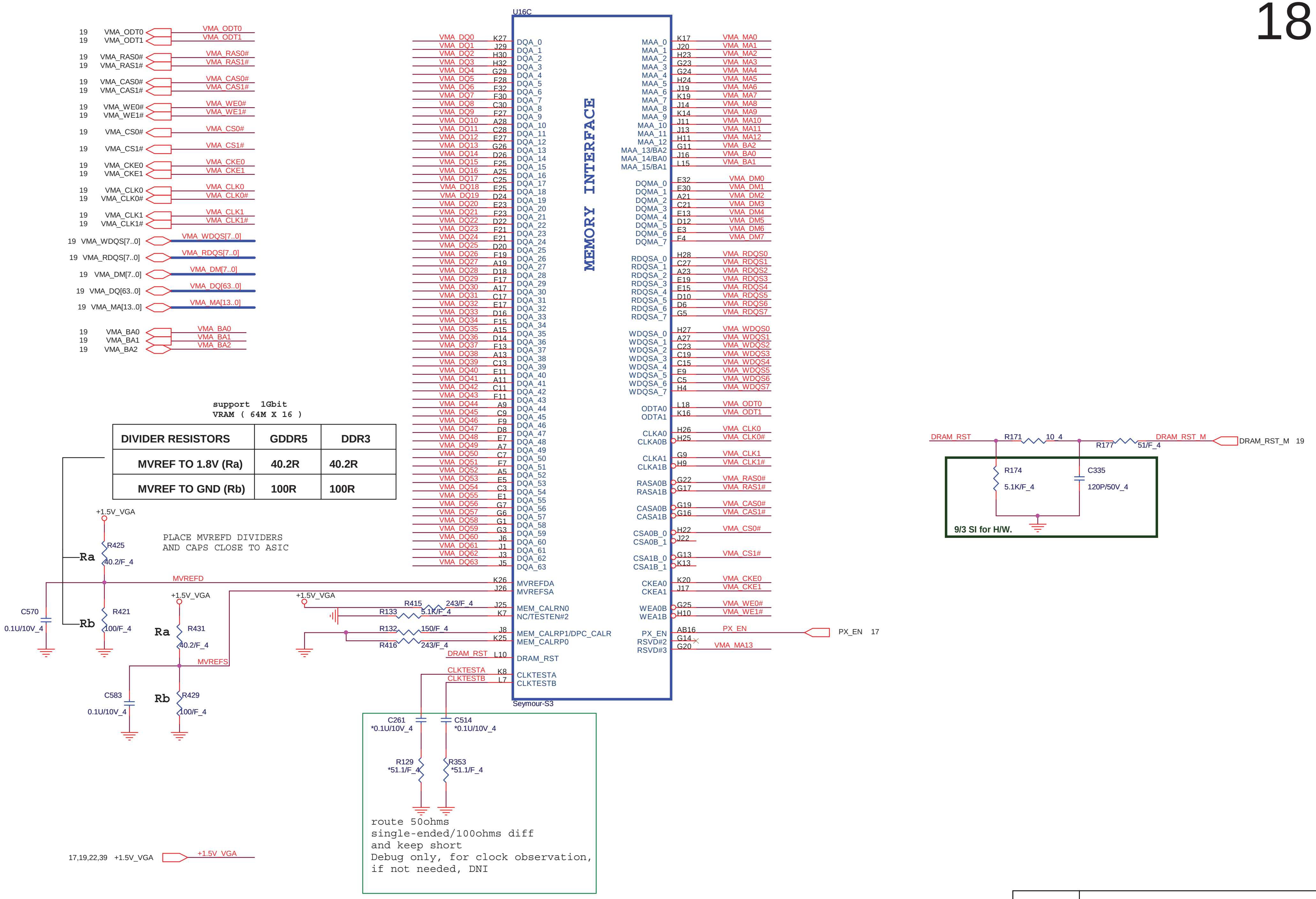
PX_EN = 0, for Normal Operation
PX_EN = 1, for BACO MODE

NB5

PROJECT : R13
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Seymour_Power_and_NC	3A

Date: Saturday, September 18, 2010 | Sheet 17 of 39


U16C
MEMORY INTERFACE
Seymour-S3
19 VMA_ODT0
19 VMA_ODT1
19 VMA_RAS0#
19 VMA_RAS1#
19 VMA_CAS0#
19 VMA_CAS1#
19 VMA_WE0#
19 VMA_WE1#
19 VMA_CS0#
19 VMA_CS1#
19 VMA_CKE0
19 VMA_CKE1
19 VMA_CLK0
19 VMA_CLK0#
19 VMA_CLK1
19 VMA_CLK1#
19 VMA_WDQS[7..0]
19 VMA_RDQS[7..0]
19 VMA_DM[7..0]
19 VMA_DQ[63..0]
19 VMA_MA[13..0]
19 VMA_BA0
19 VMA_BA1
19 VMA_BA2
VMA_DQ0 … VMA_DQ63 → DQA_0 … DQA_63
MAA_0 … MAA_12, MAA_13/BA2, MAA_14/BA0, MAA_15/BA1
DQMA_0 … DQMA_7
RDQSA_0 … RDQSA_7
WDQSA_0 … WDQSA_7
ODTA0 ODTA1
CLKA0 CLKA0B CLKA1 CLKA1B
RASA0B RASA1B CASA0B CASA1B
CSA0B_0 CSA0B_1 CSA1B_0 CSA1B_1
CKEA0 CKEA1 WEA0B WEA1B
PX_EN RSVD#2 RSVD#3
MVREFDA MVREFSA
MEM_CALRN0 NC/TESTEN#2
MEM_CALRP1/DPC_CALR MEM_CALRP0
DRAM_RST
CLKTESTA CLKTESTB
+1.5V_VGA
R425 40.2/F_4
R421 100/F_4
C570 0.1U/10V_4
MVREFD
R431 40.2/F_4
R429 100/F_4
C583 0.1U/10V_4
MVREFS
Ra
Rb
R415 243/F_4
R133 5.1K/F_4
R132 150/F_4
R416 243/F_4
C261 *0.1U/10V_4
C514 *0.1U/10V_4
R129 *51.1/F_4
R353 *51.1/F_4
PX_EN 17
VMA_MA13
DRAM_RST
R171 10_4
R177 51/F_4
DRAM_RST_M
DRAM_RST_M 19
R174 5.1K/F_4
C335 120P/50V_4
9/3 SI for H/W.
17,19,22,39 +1.5V_VGA

support 1Gbit
VRAM (64M X 16)

DIVIDER RESISTORS	GDDR5	DDR3
MVREF TO 1.8V (Ra)	40.2R	40.2R
MVREF TO GND (Rb)	100R	100R

PLACE MVREFD DIVIDERS
AND CAPS CLOSE TO ASIC

route 50ohms
single-ended/100ohms diff
and keep short
Debug only, for clock observation,
if not needed, DNI

PROJECT : R13
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	Seymour/MEM_Interface	3A

Date: Saturday, September 18, 2010 Sheet 18 of 39

512MB DDR3

18 VMA_MA[13..0]
18 VMA_DM[7..0]
VMA_MA[13..0]
18 VMA_DQ[63..0]
18 VMA_WDQS[7..0]
18 VMA_RDQS[7..0]

U10 / U19 / U9 / U20 — K4W1G1646E-HC12
100-BALL SDRAM DDR3

+1.5V_VGA

Should be 243 Ohms +-1%
R187 243/F_4
R414 243/F_4
R166 243/F_4
R413 243/F_4

R428 4.99K/F_4
R424 4.99K/F_4
C573 0.1U/10V_4
VREFC_VMA1
R160 4.99K/F_4
R162 4.99K/F_4
C328 0.1U/10V_4
VREFD_VMA1

R418 4.99K/F_4
R426 4.99K/F_4
C574 0.1U/10V_4
VREFC_VMA2
R180 4.99K/F_4
R176 4.99K/F_4
C342 0.1U/10V_4
VREFD_VMA2

R183 4.99K/F_4
R179 4.99K/F_4
C348 0.1U/10V_4
VREFC_VMA3
R175 4.99K/F_4
R178 4.99K/F_4
C340 0.1U/10V_4
VREFD_VMA3

R417 4.99K/F_4
R419 4.99K/F_4
C566 0.1U/10V_4
VREFC_VMA4
R410 4.99K/F_4
R412 4.99K/F_4
C562 0.1U/10V_4
VREFD_VMA4

VMA_CLK0
R182 56.2/F_4
VMA_CLK0_COMM
C357 0.01U/16V_4
R184 56.2/F_4
VMA_CLK0#
VMA_CLK1
R167 56.2/F_4
VMA_CLK1_COMM
C333 0.01U/16V_4
R172 56.2/F_4
VMA_CLK1#
7,18,22,39 +1.5V_VGA

C565 C362 C361 C360 C359 C567 C569 C349 1U/6.3V_4
C571 C572 C577 C350 C354 C347 C581 C579 1U/6.3V_4
C586 C582 C356 C358 10U/6.3VS_6
C555 C551 C575 C316 C578 C320 C548 C546 0.1U/10V_4
C319 C585 C587 C317 C351 C318 C337 C343 0.1U/10V_4

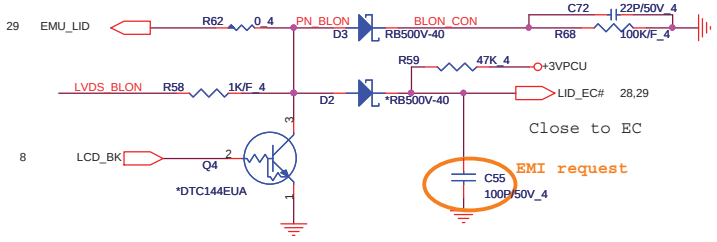
	QCI PN
SAMSUNG	AKD5LGGT502
HYNIX	AKD5LZGTW00

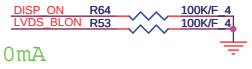
NB5

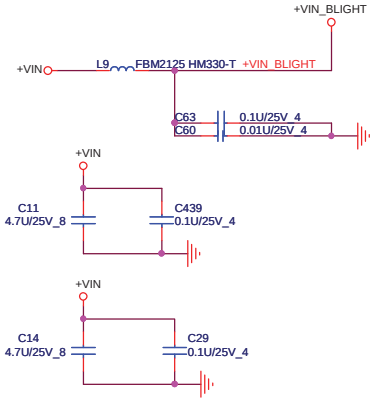
PROJECT : R13
Quanta Computer Inc.

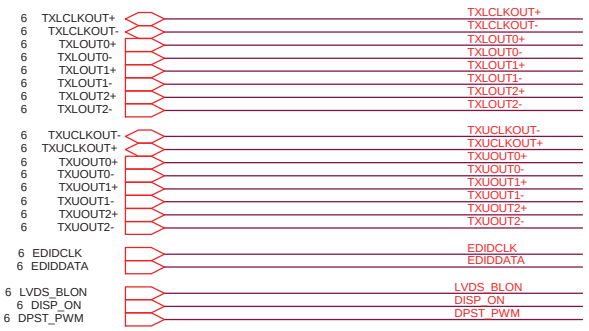
Size: Custom | Document Number: Seymour VRAM(DDR3 BGA96) | Rev: 3A
Date: Saturday, September 18, 2010 | Sheet 19 of 39

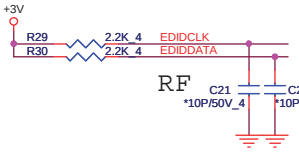
LID Switch



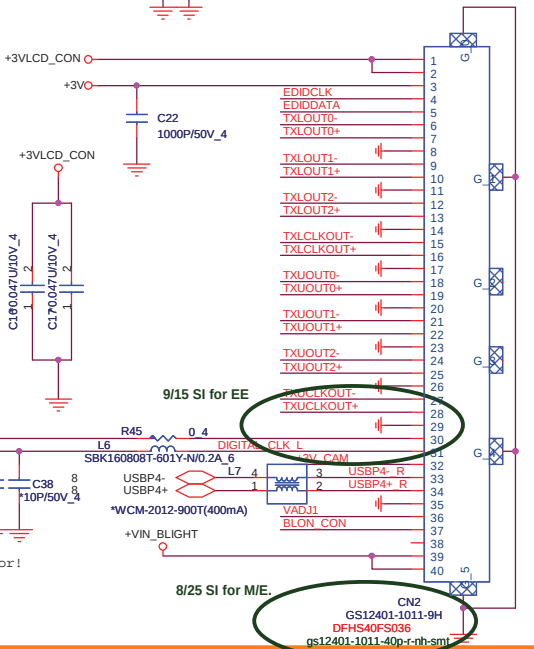


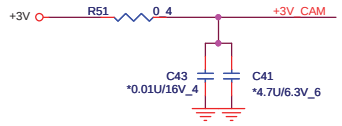






RF SI change to AX type

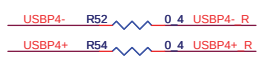


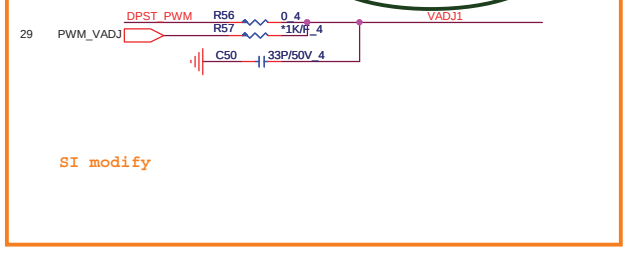


EMI

Please note that 2011 camera is +3V a We do not need to use 5V -> 3.95V regulator!

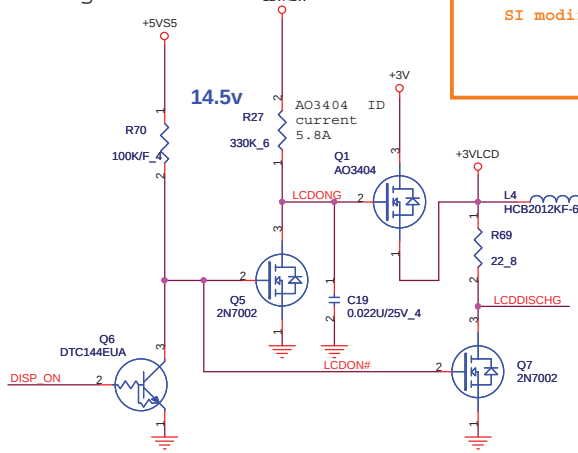
follow L7 location





SI modify

change to +5VS5



1A

NB5

PROJECT : R13
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN/LID/CAM	3A

Date: Saturday, September 18, 2010 | Sheet 20 of 39

close to HDMI conn

6	IN_CLK#	IN_CLK#	C280	0.1U/10V_4	C_TXC_HDMI-
6	IN_CLK	IN_CLK	C288	0.1U/10V_4	C_TXC_HDMI+
6	IN_D0#	IN_D0#	C307	0.1U/10V_4	C_TX0_HDMI-
6	IN_D0	IN_D0	C309	0.1U/10V_4	C_TX0_HDMI+
6	IN_D1#	IN_D1#	C298	0.1U/10V_4	C_TX1_HDMI-
6	IN_D1	IN_D1	C303	0.1U/10V_4	C_TX1_HDMI+
6	IN_D2#	IN_D2#	C313	0.1U/10V_4	C_TX2_HDMI-
6	IN_D2	IN_D2	C314	0.1U/10V_4	C_TX2_HDMI+

6 SDVO_CLK — SDVO_CLK — HDMI_SCL_R
6 SDVO_DATA — SDVO_DATA — HDMI_SDA_R

6 HDMI_HPD_CON — HDMI_HPD_CON — HDMI_HPD_3V

+3V
C518 *0.1U/10V_4
C222 *0.1U/10V_4

DISCRETE HDMI I2C SELECT
Close to HDMI Connector

+3V
R363 2.2K_4
HDMI_SCL_R — HDMI_SCLK
Q26 2N7002
R110 2.2K_4
HDMI_SDA_R — HDMI_SDATA
Q12 2N7002

SI add

+3V +5V
R783 0_4
R781 0_4
Q35 2N7002K
R392 100K_4
C31 0.1U/10V_4

R387	680_4	C_TX2_HDMI+	
R385	680_4	C_TX2_HDMI-	
R374	680_4	C_TX1_HDMI+	
R373	680_4	C_TX1_HDMI-	
R382	680_4	C_TX0_HDMI+	
R379	680_4	C_TX0_HDMI-	
R367	680_4	C_TXC_HDMI+	
R365	680_4	C_TXC_HDMI-	

+3V
Q25 MMBT3904-7-F
HDMI_DET_R
R347 200K/F_4
HDMI_HPD
HDMI_HPD_3V
R342 10K/F_4
R350 200K/F_4

C_TXC_HDMI+ R786 *100/F_4 C_TXC_HDMI-

L32 *WCM2012-90
L30 *WCM2012-90
L31 *WCM2012-90
L27 *WCM2012-90

C_TX2_HDMI+	C_TX2_HDMI+	1
C_TX2_HDMI-	C_TX2_HDMI-	3
C_TX1_HDMI+	C_TX1_HDMI+	4
C_TX1_HDMI-	C_TX1_HDMI-	6
C_TX0_HDMI+	C_TX0_HDMI+	7
C_TX0_HDMI-	C_TX0_HDMI-	9
C_TXC_HDMI+	C_TXC_HDMI+	10
C_TXC_HDMI-	C_TXC_HDMI-	12

CN18
D2+ D2- D1+ D1- D0+ D0- CK+ CK-
SHELL1 SHELL2 D2 Shield D1 Shield D0 Shield CK Shield GND
20 21 2 5 8 11 17

EMI

HDMI_SCLK — DDC CLK CE Remote — 15
HDMI_SDATA — DDC DATA NC — 16 13 14
1A +5V_HDMIC
FUSE1A6V_POLY F1
+5V — +5V — 18
C3 *0.1U/10V_4
HDMI_HPD — HDMI_HPD_L — HP DET — 19
0_6 L45
C510 220P/50V_4
HDMI CONN DFHD19MR054 hdmi-100042mr019s172zl-19p-v

reserved for EMI
C274 *10P/50V_4
HDMI_SDATA
C254 *10P/50V_4
HDMI_SCLK

+5V_HDMIC
D4 CH501H-40PT
+5V_HDMIC1
R354 2.2K_4
R120 2.2K_4
HDMI_SCLK
HDMI_SDATA

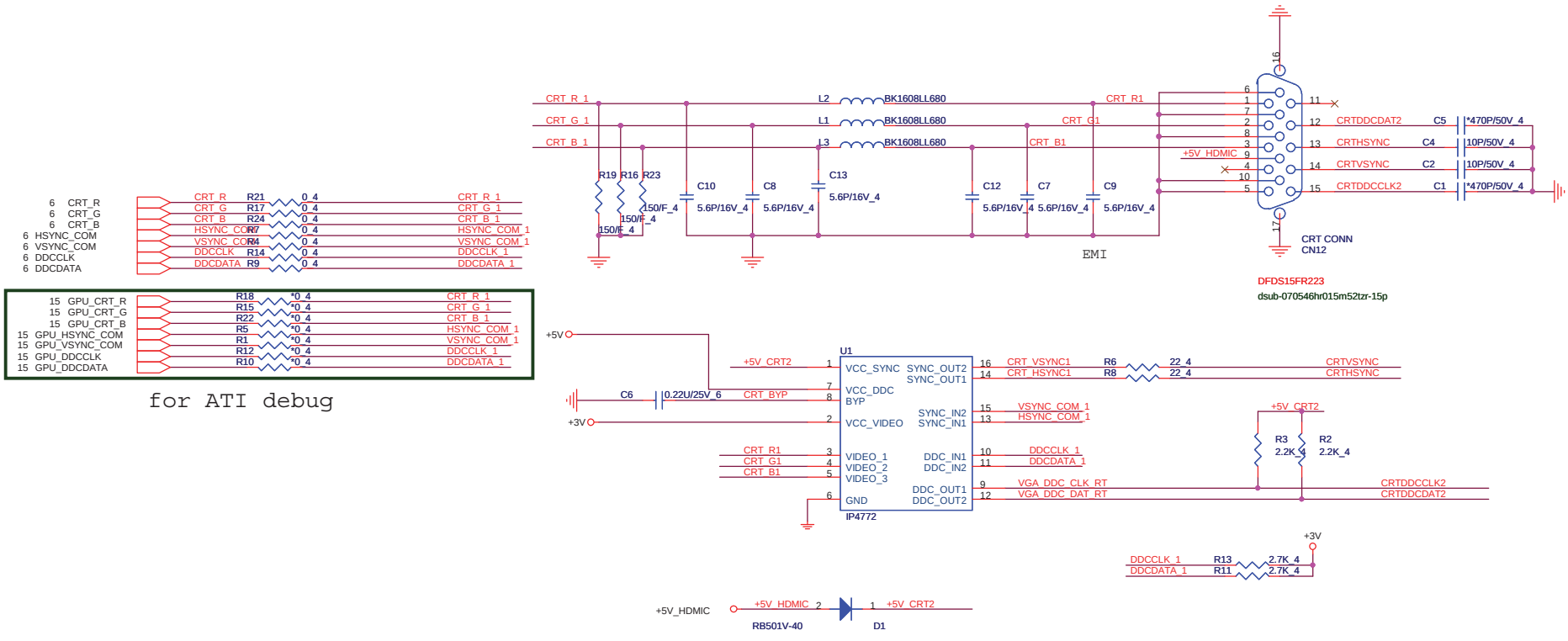
NB5

PROJECT : R13
Quanta Computer Inc.

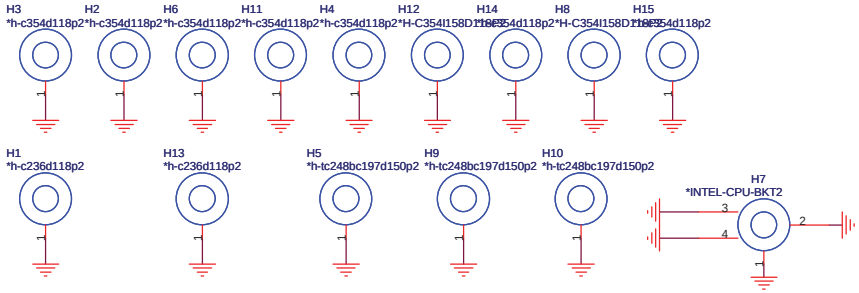
Size	Document Number	Rev
Custom	HDMI CONN	3A

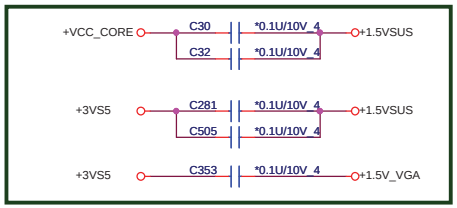
Date: Saturday, September 18, 2010 Sheet 21 of 39

CRT PORT



HOLE





RF solution

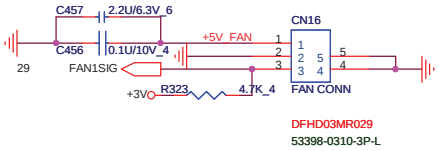
NB5

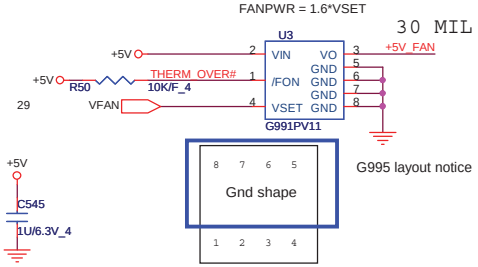
PROJECT : R13
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CRT,Hole	3A

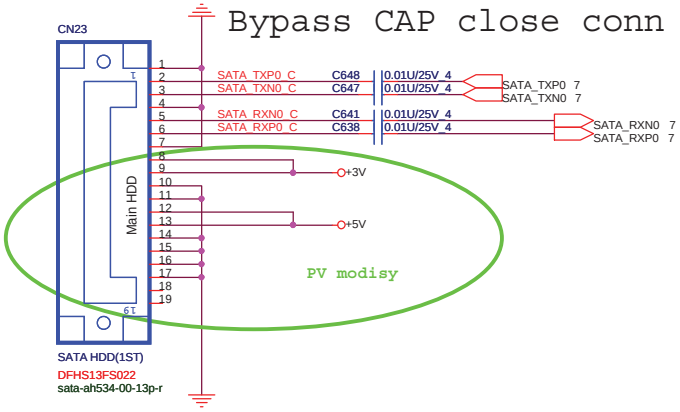
Date: Saturday, September 18, 2010 | Sheet 22 of 39

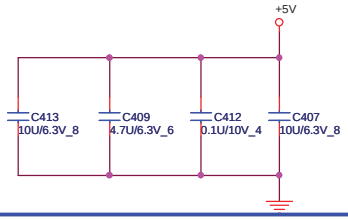
CPU FAN



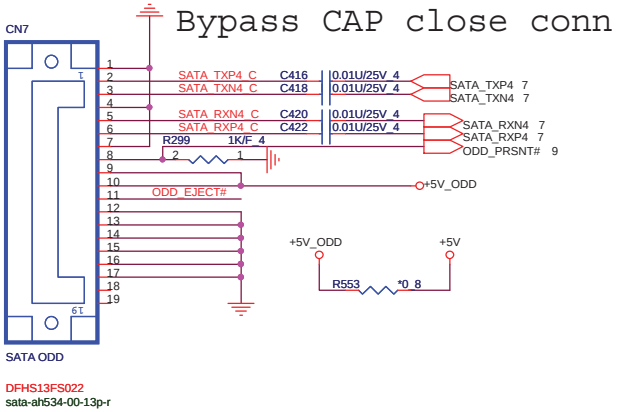


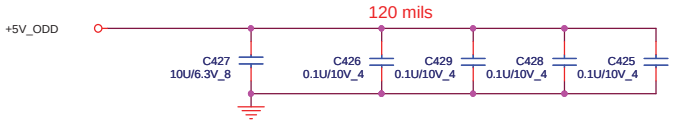
SATA HDD CONNECTOR



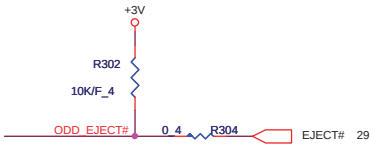


SATA ODD CONNECTOR

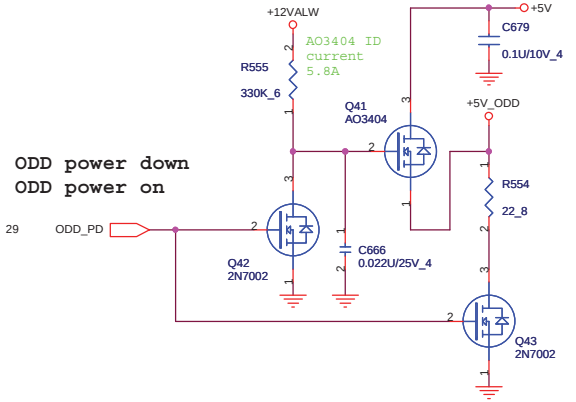




follow INTEL DG change eject PU to +3V.



High : ODD power down
Low : ODD power on

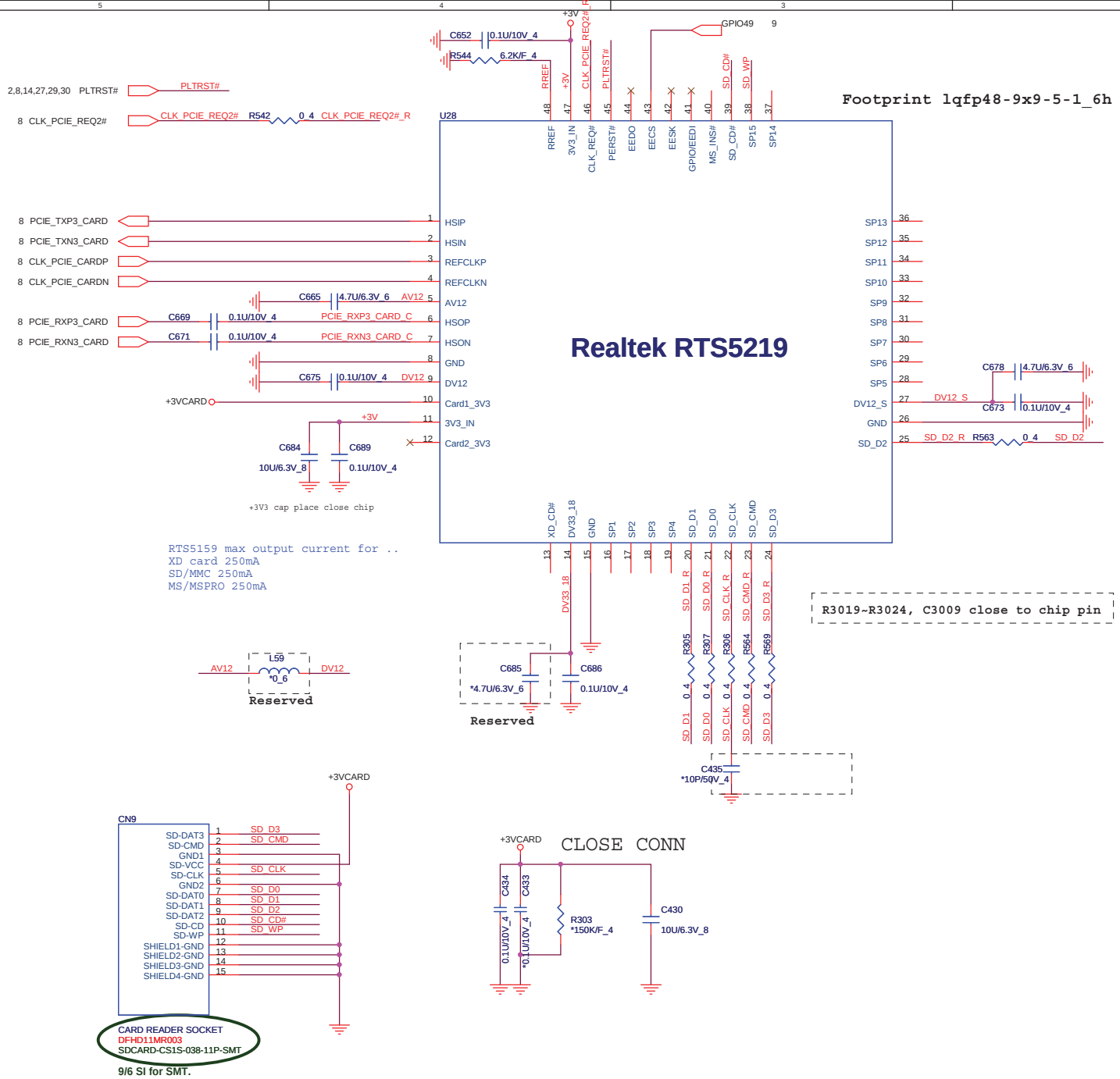


NB5

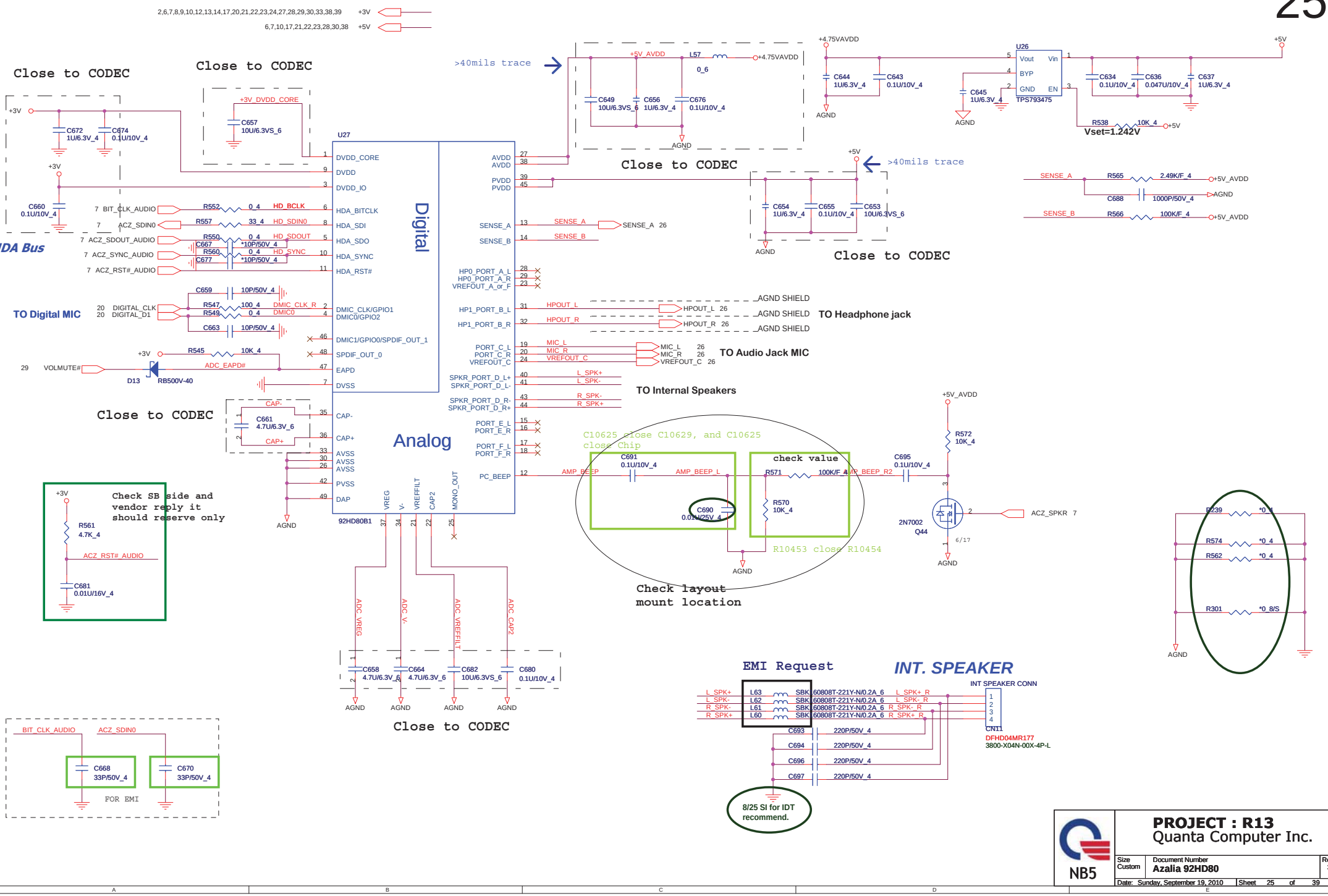
PROJECT : R13
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDD/ODD/FAN	3A

Date: Saturday, September 18, 2010 | Sheet 23 of 39



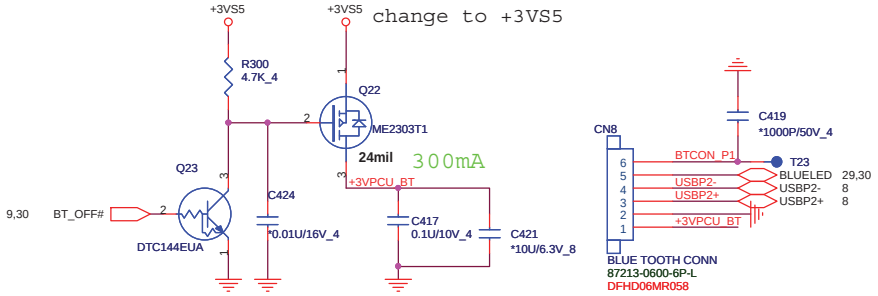
NB5	PROJECT : R13 Quanta Computer Inc.	
Size: Custom	Document Number: RTS5219 & CR SOCKET &HOLE	Rev: 3A
Date: Saturday, September 18, 2010	Sheet 24 of 39	



BLUETOOTH

300mA

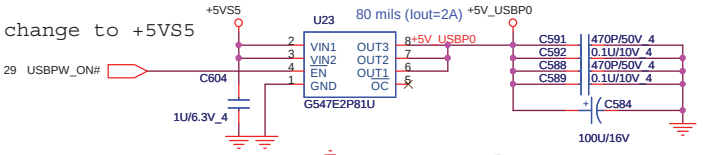
change to +3VS5



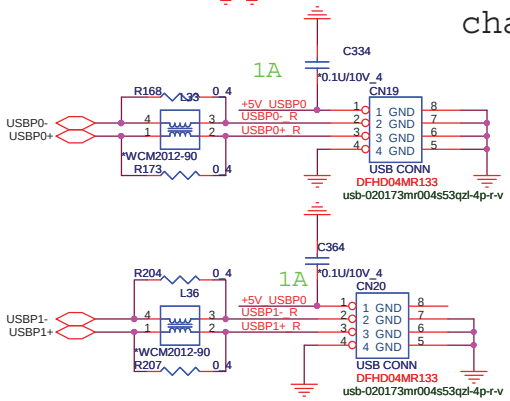
LEFT SIDE USBX2

change to AL000547005

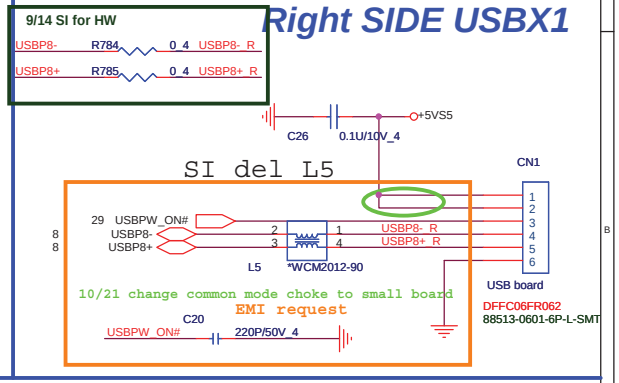
2A 2A



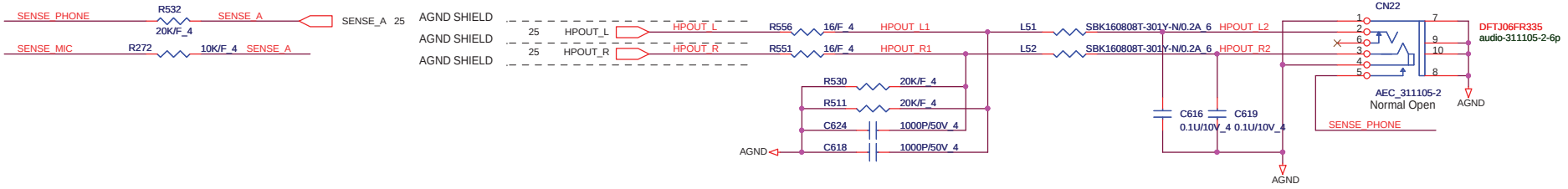
change to ELEC CAP



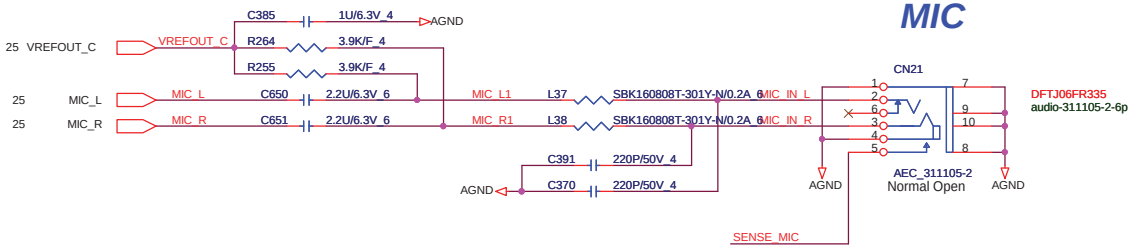
Right SIDE USBX1



Line out



MIC

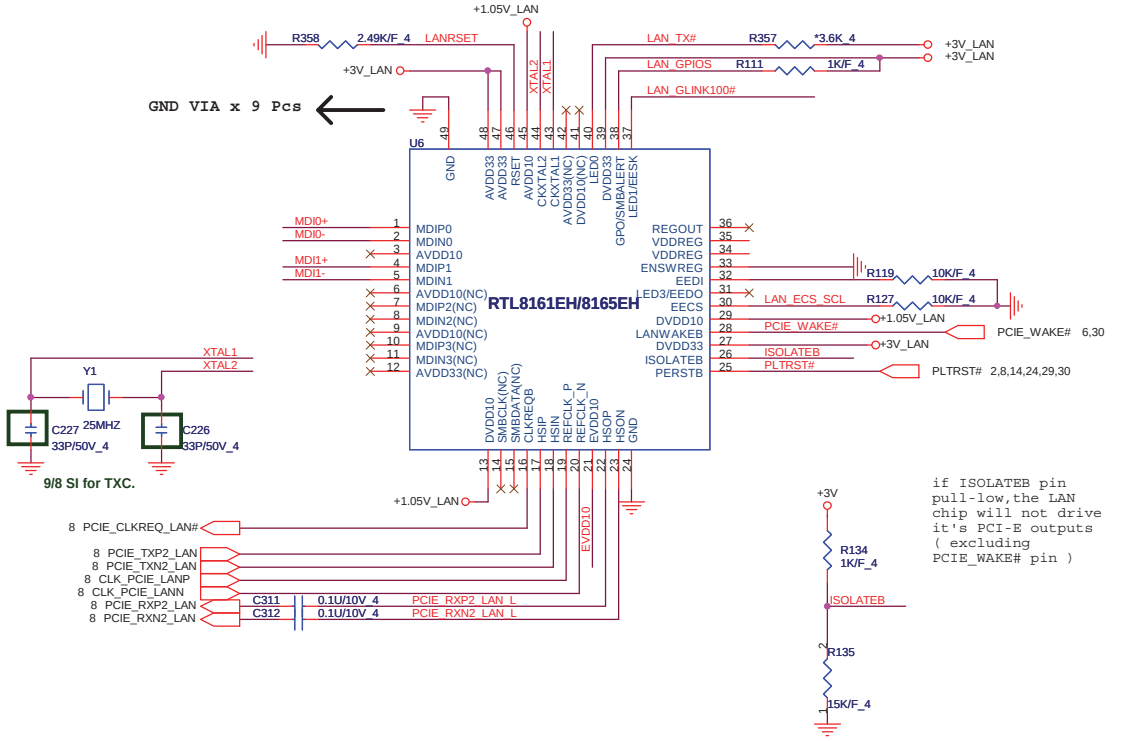


NB5

PROJECT : R13
Quanta Computer Inc.

Size	Document Number	Rev
Custom	USB/BT/Audio JacK	3A

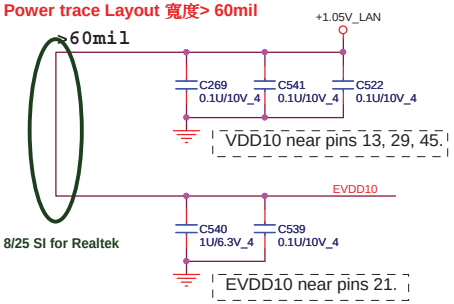
Date: Saturday, September 18, 2010 | Sheet 26 of 39



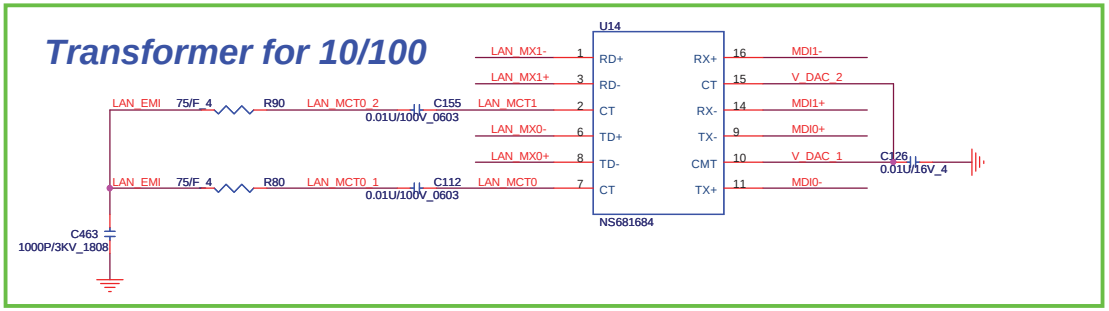
if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

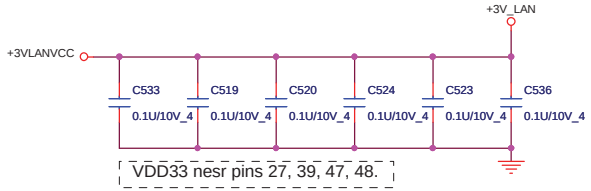
IND SMD 4.7UH +-20% 680MA(CBC2518T4R7M) CV-4707MZ00

Power trace Layout 寬度> 60mil

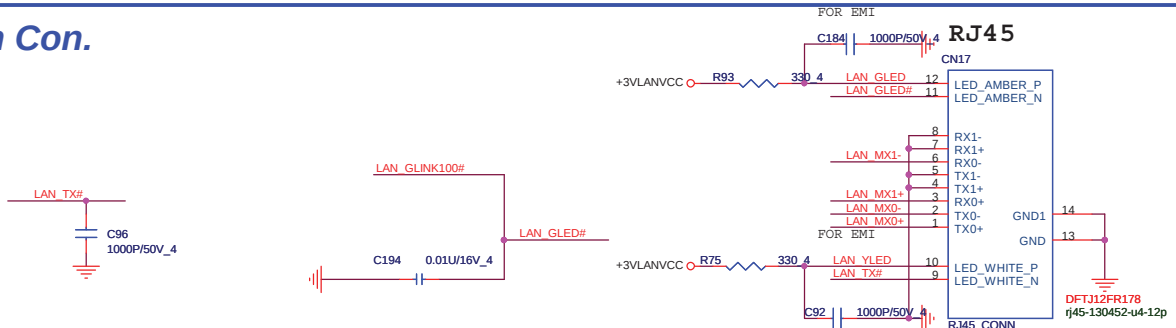


Transformer for 10/100





Lan Con.



38 +3VLANVCC
2,6,7,8,9,10,12,13,14,17,20,21,22,23,24,25,28,29,30,33,38,39 +3V

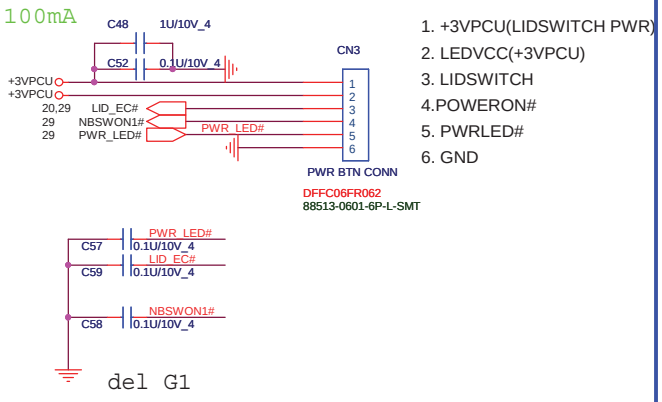
NB5

PROJECT : R13
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTL8165EH	3A

Date: Saturday, September 18, 2010 | Sheet 27 of 39

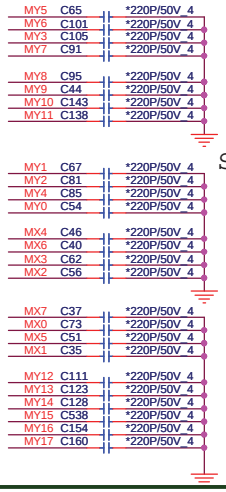
POWER BOTTON CONNECT



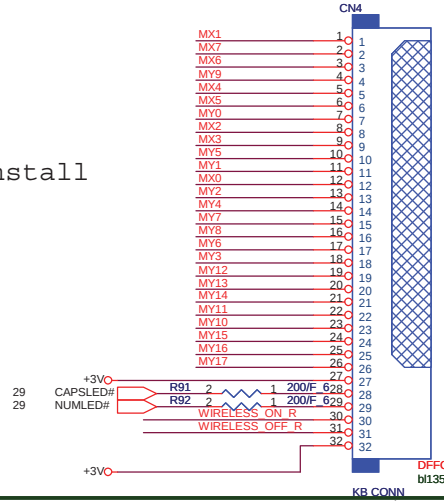
1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH
4.POWERON#
5. PWRLED#
6. GND

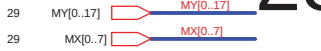
del G1

KEYBOARD Con.

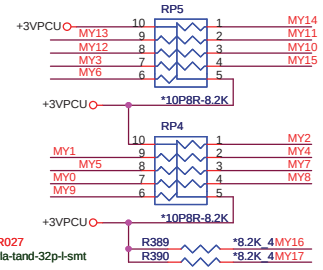


SI un-install



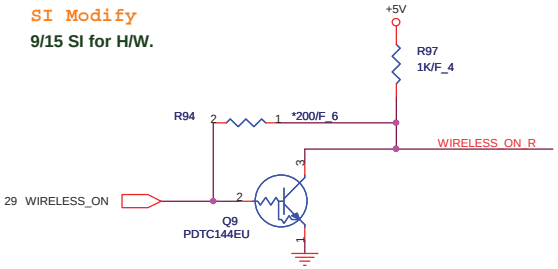


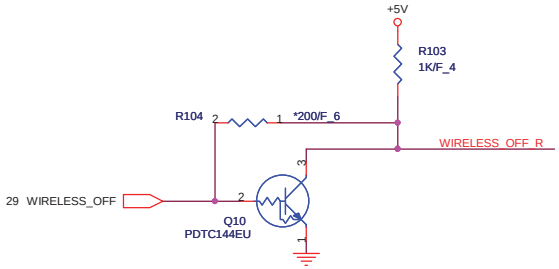
KEYBOARD PULL-UP



EC KB3930 has included K/B pull-up resistor and function

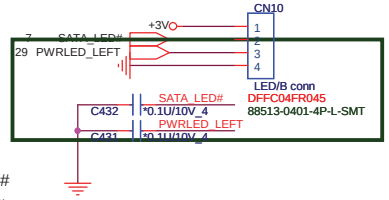
SI Modify
9/15 SI for H/W.



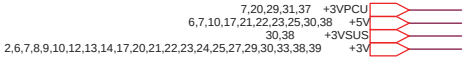


LED Con.

9/6 SI for H/W.

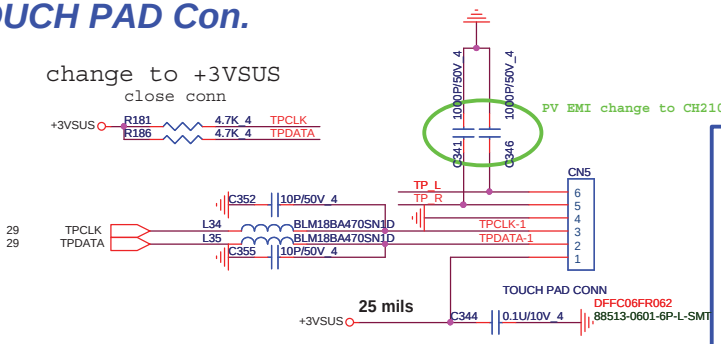


1. +3V
2. SATA_LED#
3. PWR_LED#
4.GND

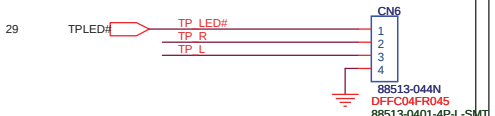


TOUCH PAD Con.

change to +3VSUS
close conn



To TOUCH PAD SW board



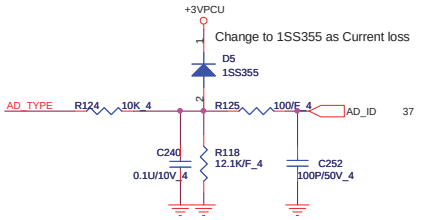
NB5

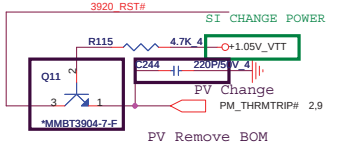
PROJECT : R13
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LED/KB/SW/TP	3A

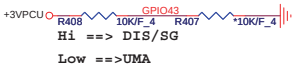
Date: Saturday, September 18, 2010 | Sheet 28 of 39

adapter Type check



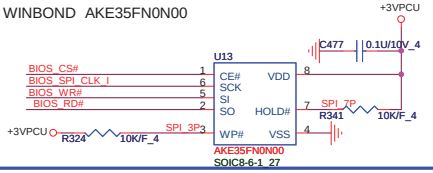


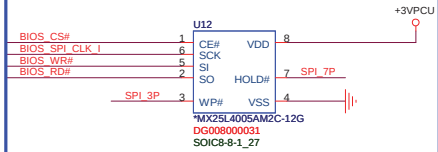
adapter select for EC



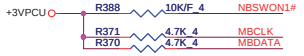
512K byte SPI EC ROM

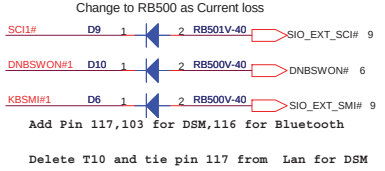
Socket: DG008000031
EON AKE35FN0Q00
WINBOND AKE35FN0N00

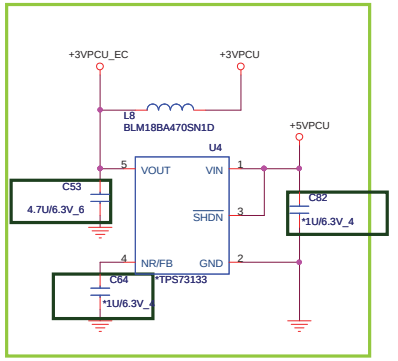


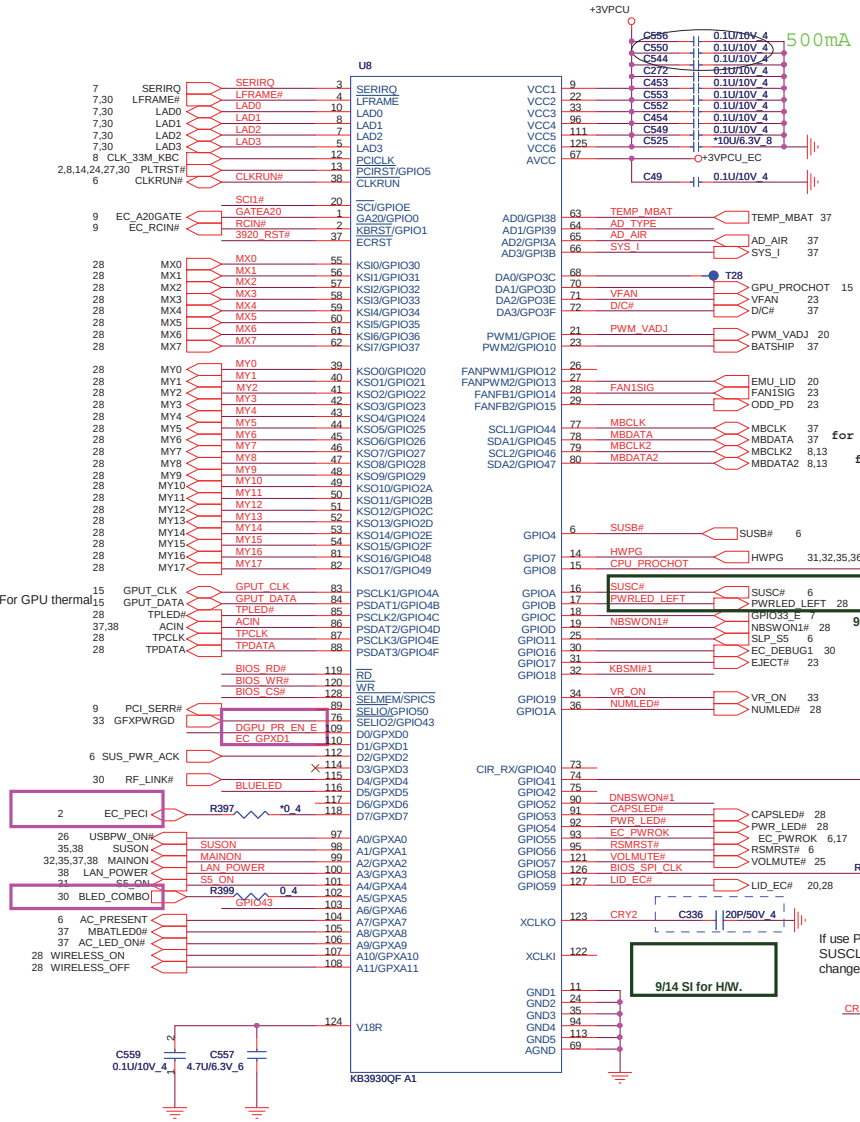


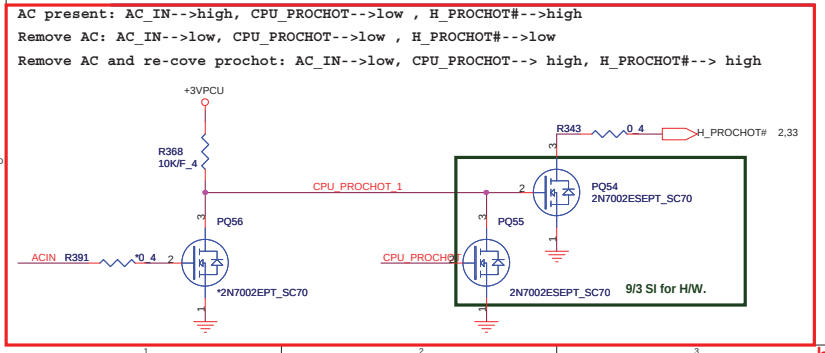
128K byte SPI EC ROM

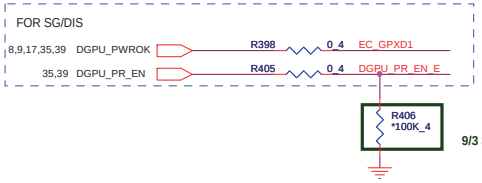


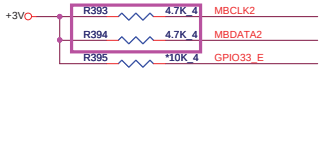


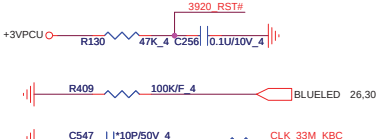












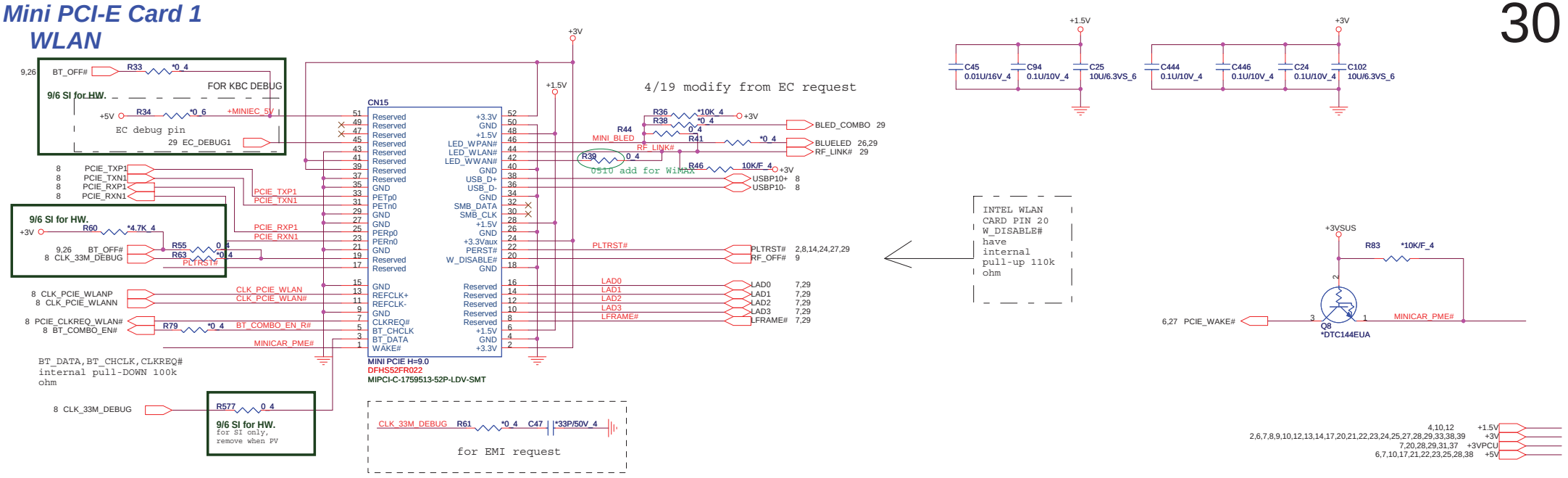
2,4,6,7,8,10,32,33 +1.05V_VTT
2,6,7,8,9,10,12,13,14,17,20,21,22,23,24,25,27,28,30,33,38,39 +3V
7,20,28,31,37 +3VPCU
31,37 +5VPCU

PROJECT : R13
Quanta Computer Inc.

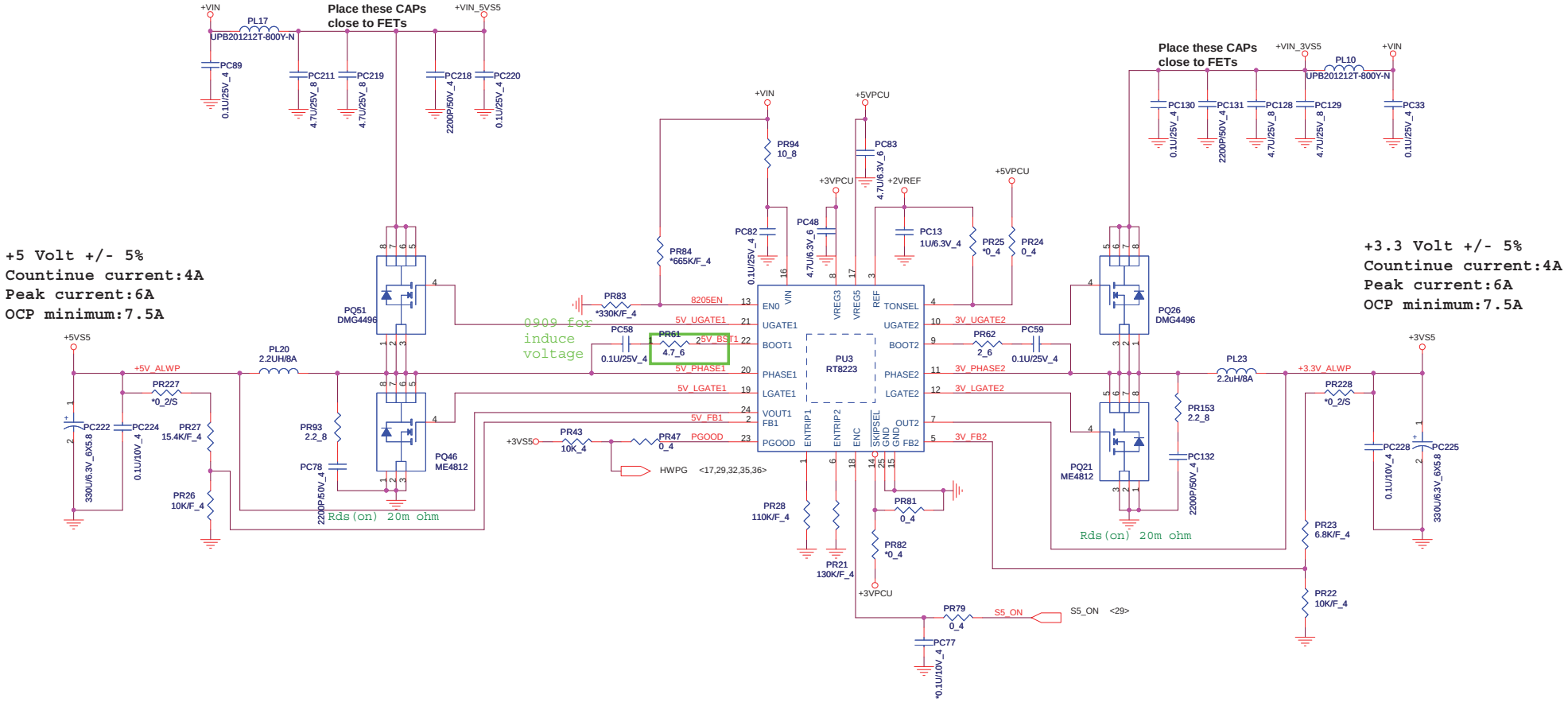
Size	Document Number	Rev
Custom	EC (KB3926)/ROM	3A
Date: Saturday, September 18, 2010	Sheet 29 of 39	

NB5

Mini PCI-E Card 1
WLAN



NB5	PROJECT : R13 Quanta Computer Inc.		
Size Custom	Document Number MINI PCIE CONN X1		Rev 1A
Date: Saturday, September 18, 2010	Sheet 30 of 39		

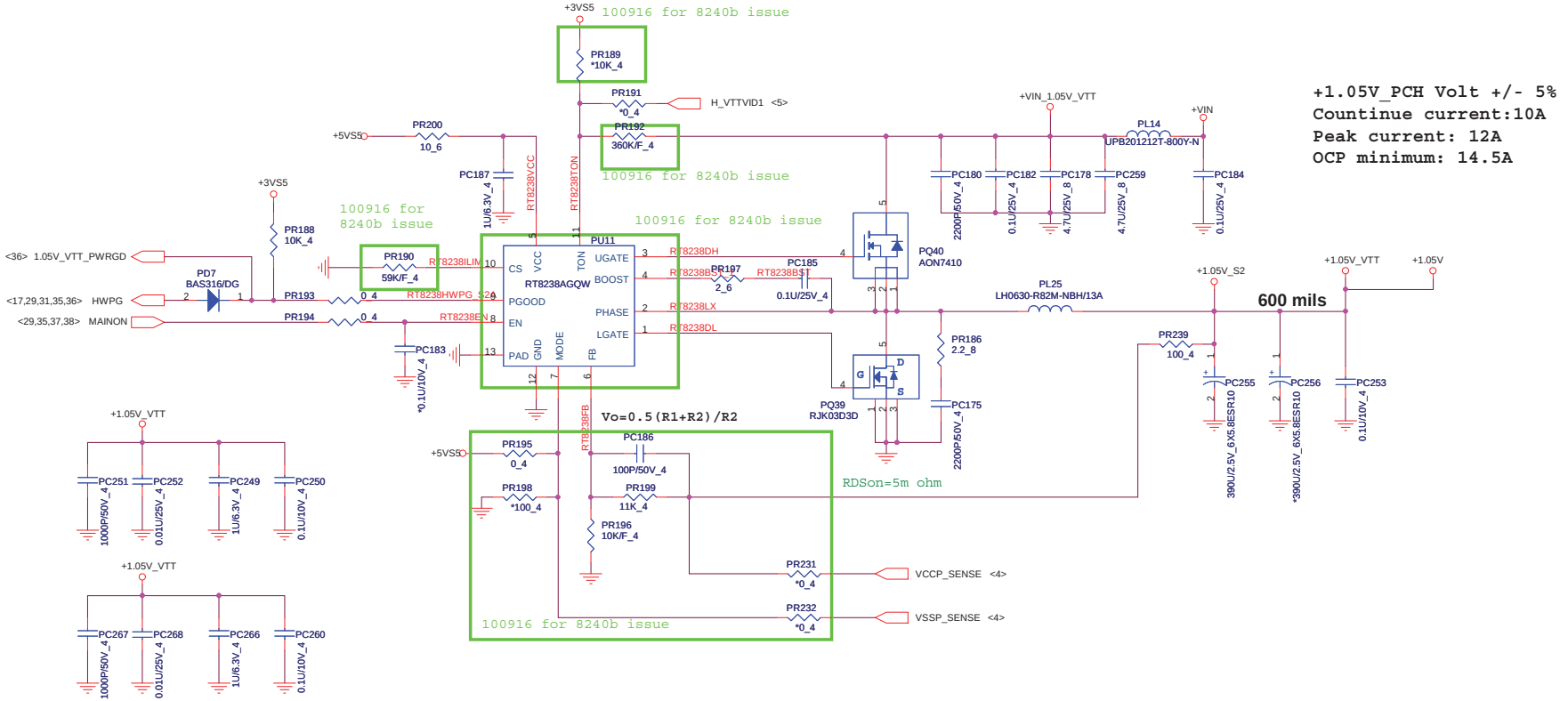


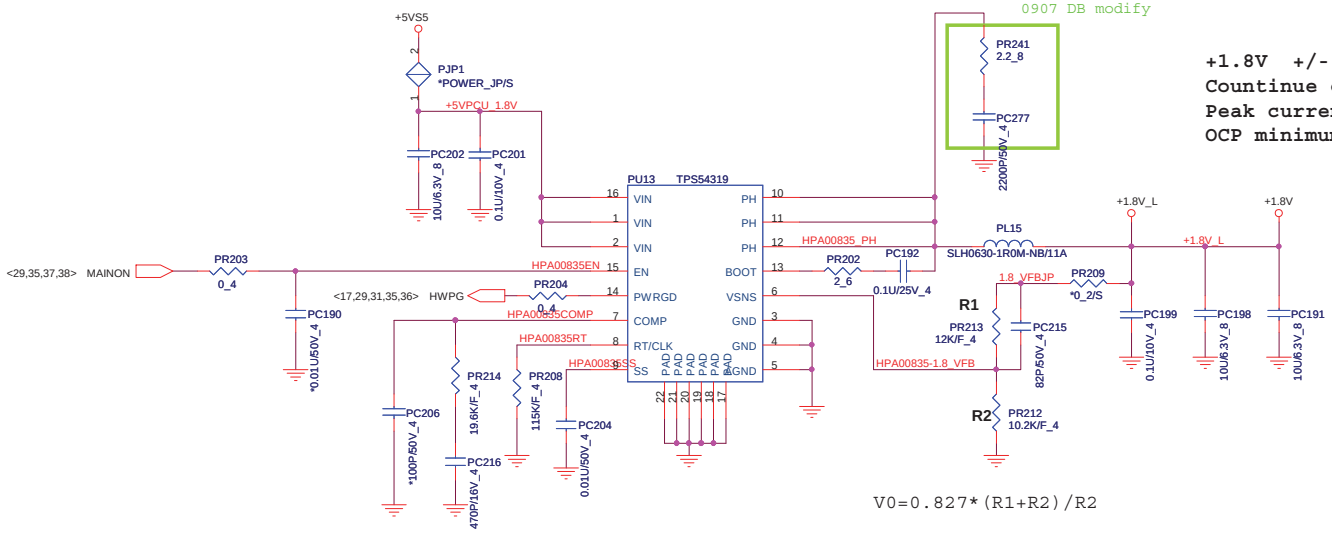
PROJECT : R13
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+5V/+3V (RT8206B)	1A

NB5

Date: Saturday, September 18, 2010 | Sheet 31 of 39





NB5	PROJECT : R13 Quanta Computer Inc.	
Size: Custom	Document Number: +1.1V VTT / PCH	Rev: 1A
Date: Saturday, September 18, 2010	Sheet 32 of 39	

1.Alert trace routing between data and clock trace
2.Refer to ground
3.Keep out 20 mils

0909 DB MODIFY

0826 cancel for layout

B~4350

PUT COLSE TO VCORE Phase 1 Inductor

20100913 for LOAD LINE

SV 35W CPU
VID1=1.05V
IccMax=54A
R_LL=1.9m ohm
OCP~60A

PUT COLSE TO VCORE HOT SPOT

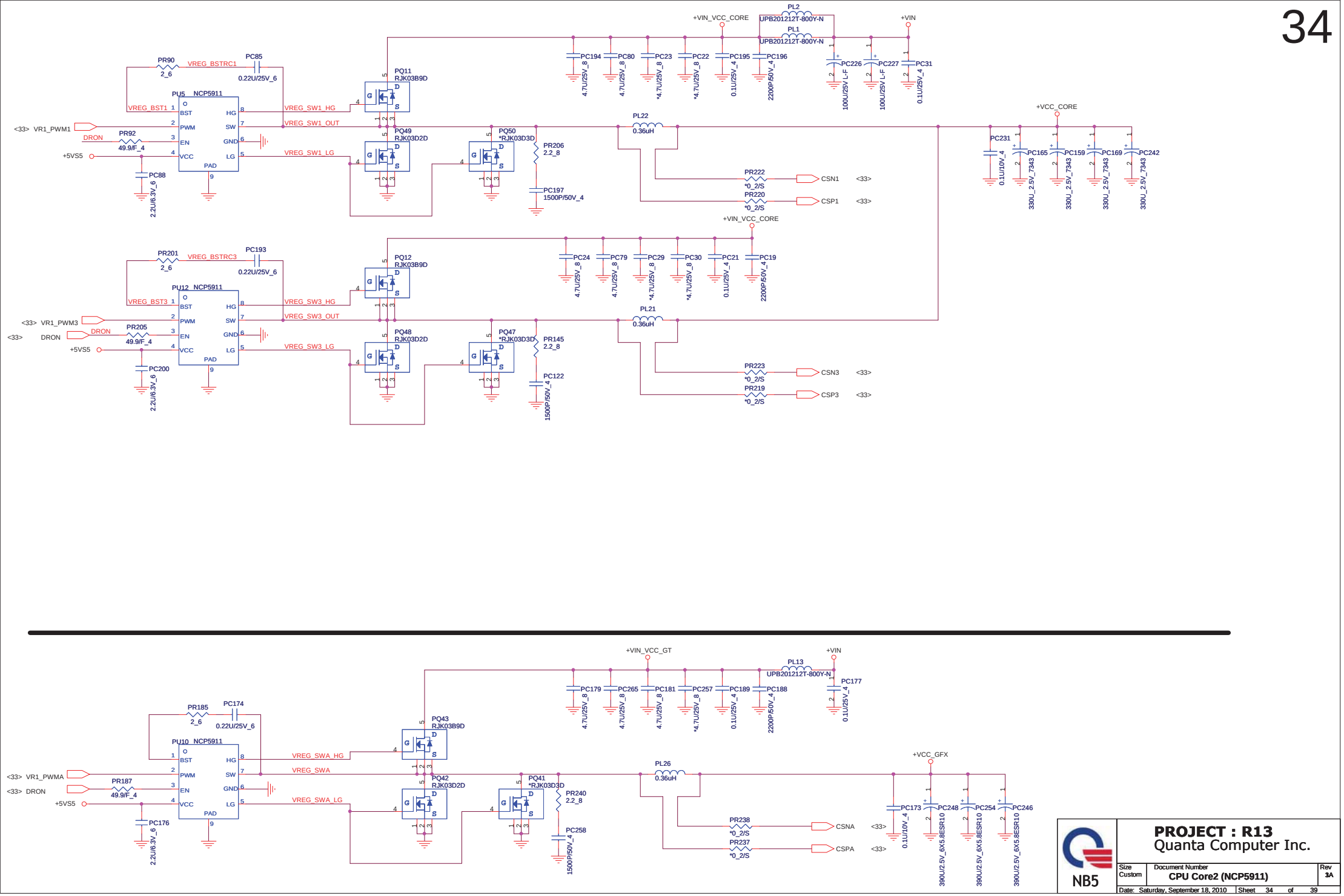
PUT COLSE TO V_GT HOT SPOT

0907 DB MODIFY

20100913 for LOAD LIINE

PUT COLSE TO V_GT Inductor

PROJECT : R13	Quanta Computer Inc.
NB5	Size: Custom; Document Number: CPU Core1 (NCP6131S); Rev: 1A
Date: Saturday, September 18, 2010	Sheet 33 of 39

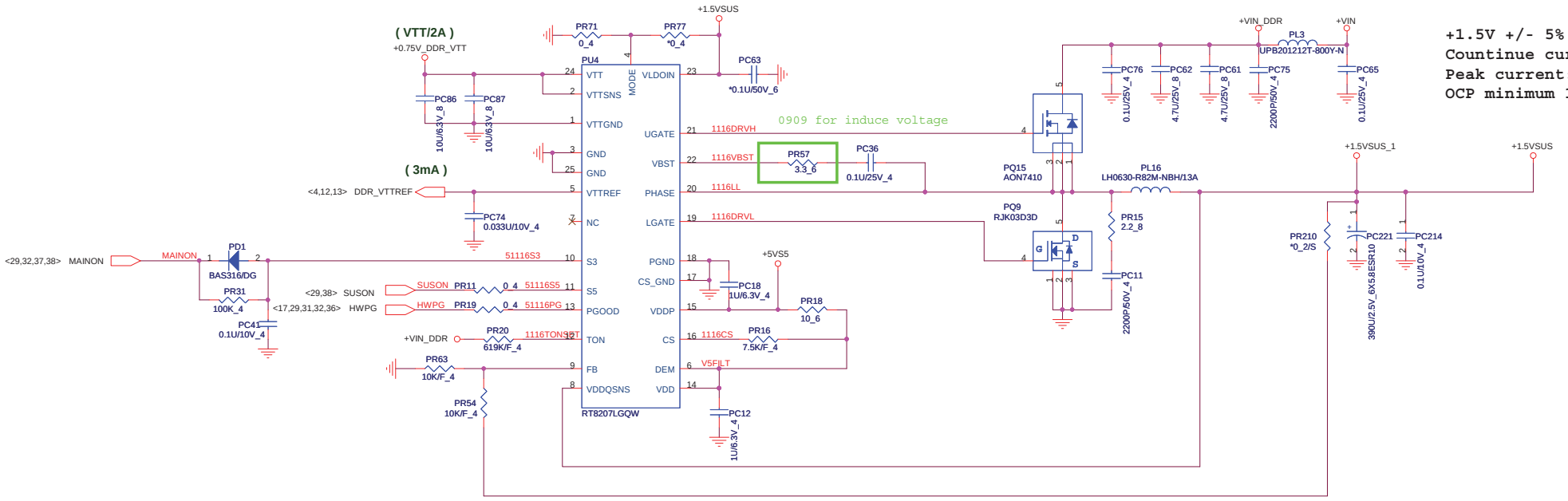


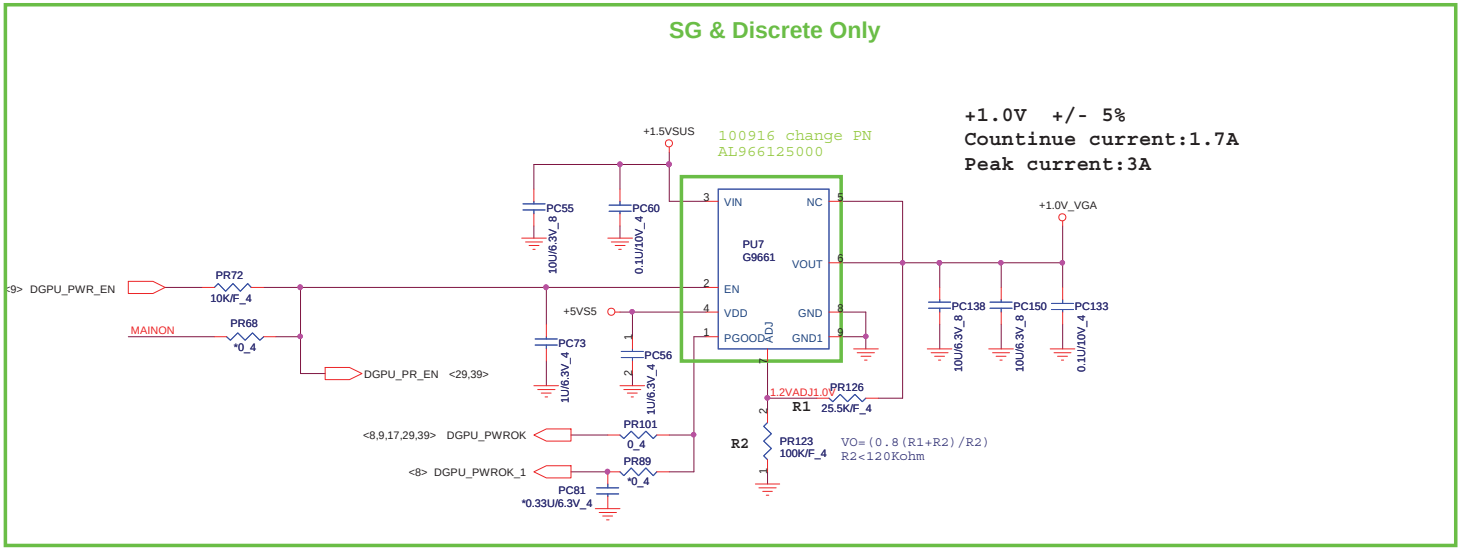
PROJECT : R13
Quanta Computer Inc.

NB5

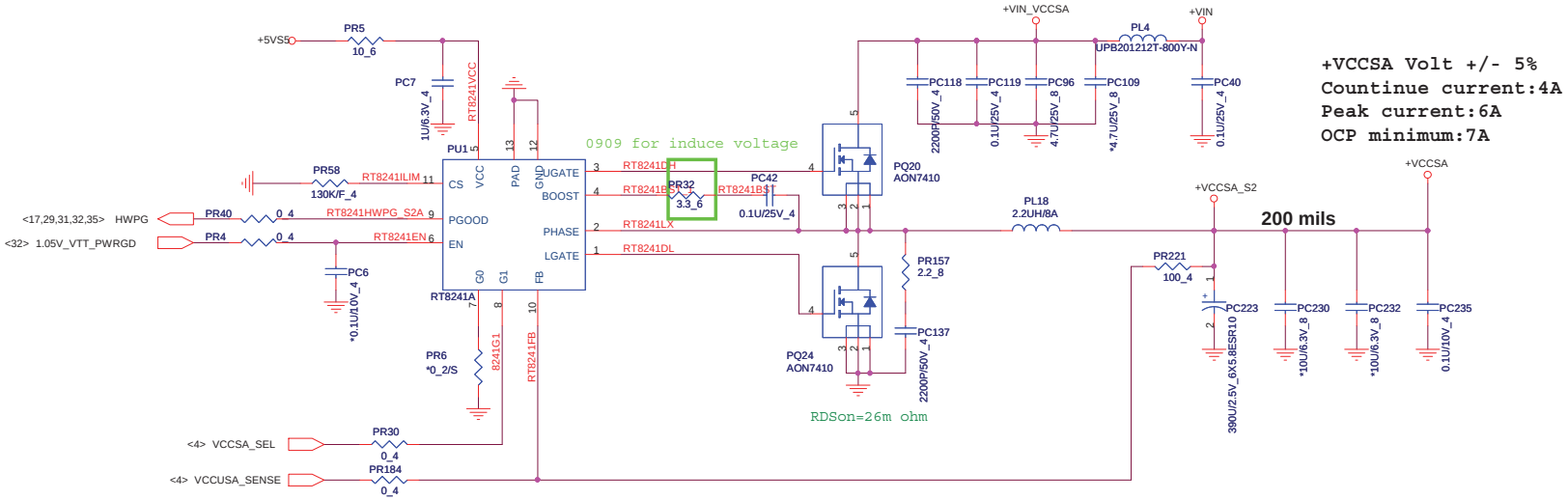
Size	Document Number	Rev
Custom	CPU Core2 (NCP5911)	1A

Date: Saturday, September 18, 2010 | Sheet 34 of 39

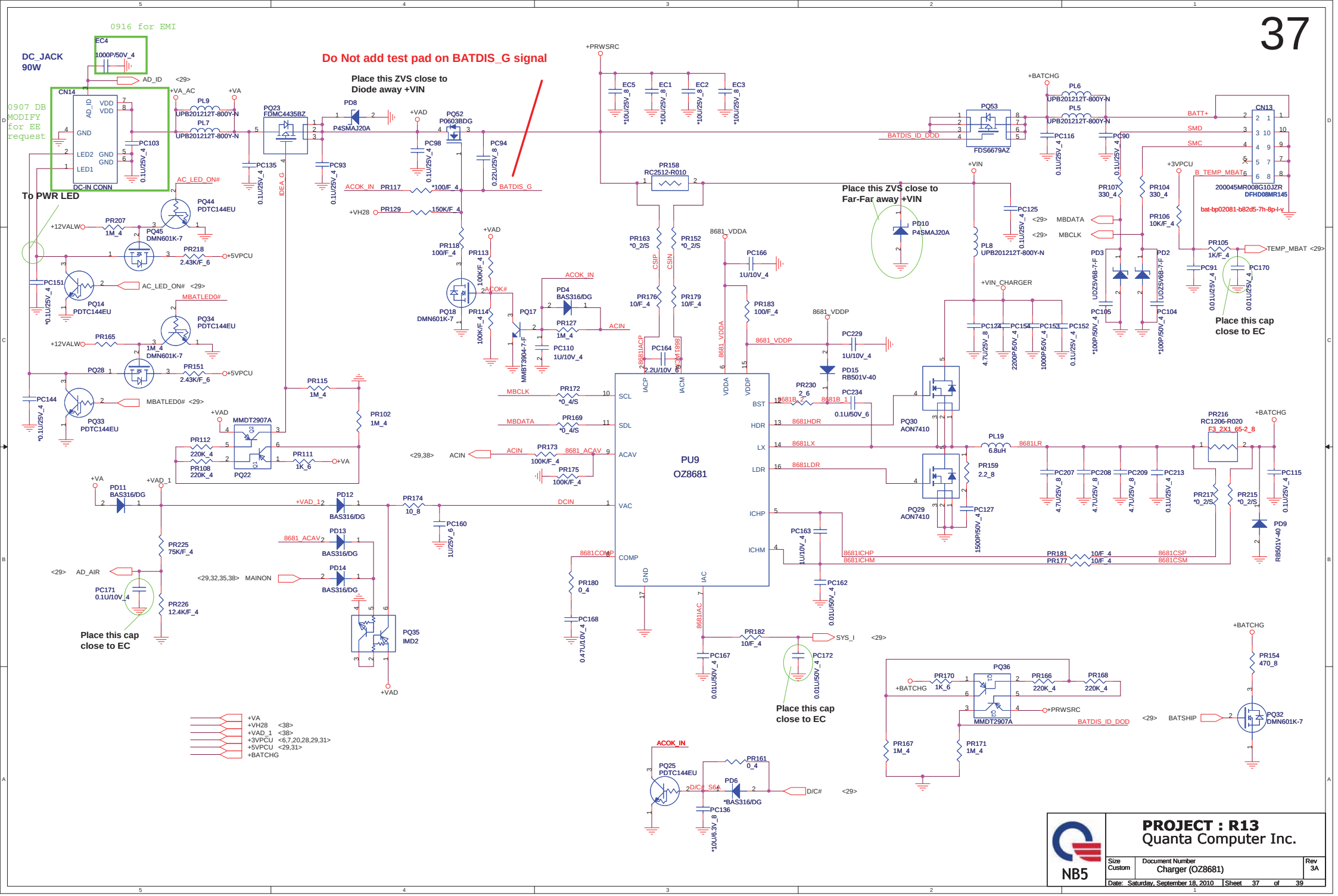


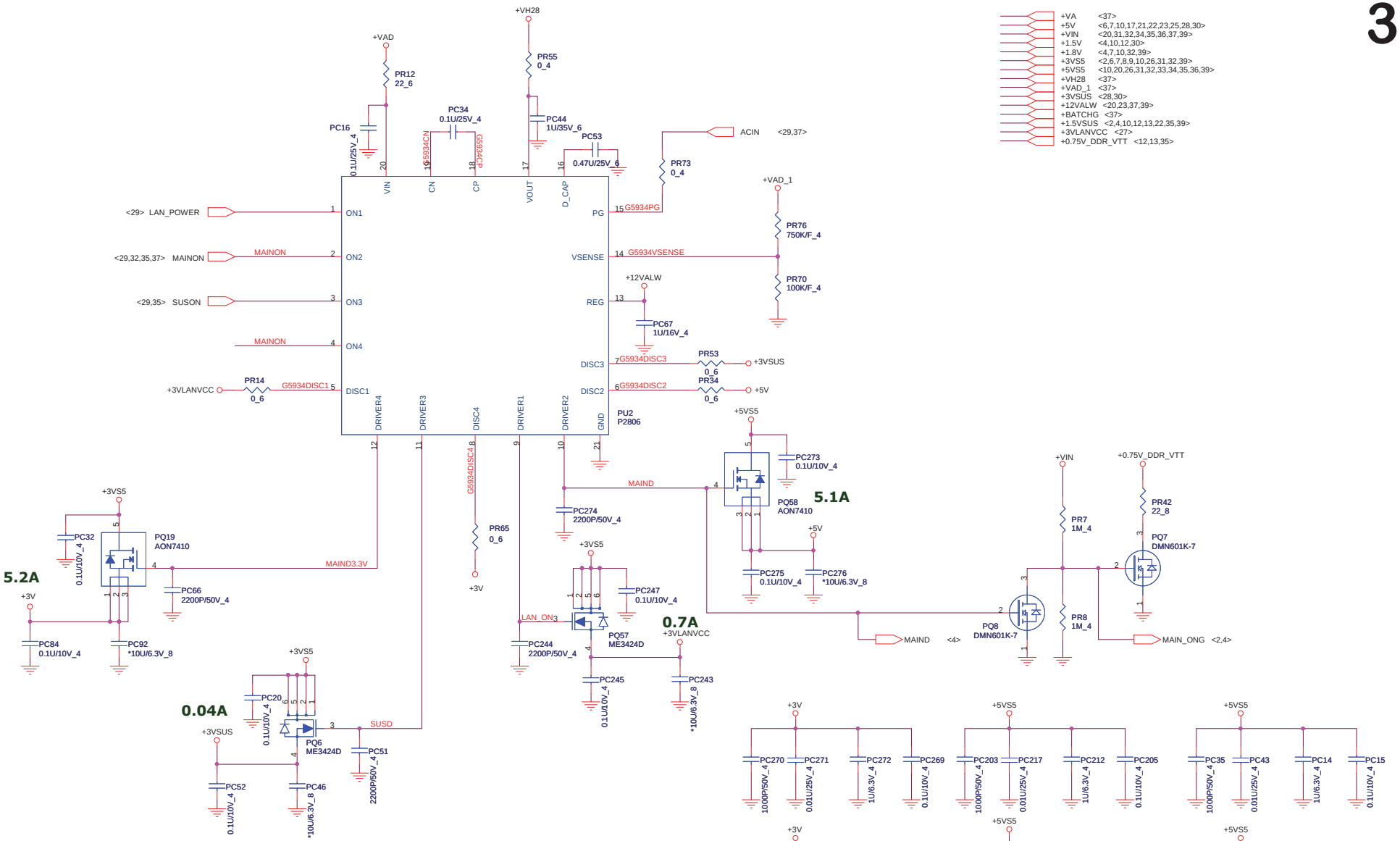


NB5	**PROJECT : R13** Quanta Computer Inc.	
Size: Custom	Document Number: DDR3 (RT8207)	Rev: 1A
Date: Saturday, September 18, 2010	Sheet 35 of 39	



NB5	**PROJECT : R13** Quanta Computer Inc.	
Size: Custom	Document Number: +1.1V VTT / PCH	Rev: 3A
Date: Saturday, September 18, 2010	Sheet 36 of 39	





NB5

PROJECT : R13
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Dis-charge IC (G5934)	3A

Date: Saturday, September 18, 2010 | Sheet 38 of 39

VGA Core

+VGACORE +/- 5%
Countinue current:10A
Peak current:14A
OCP minimum 16A

0915 for EE BACO
0914 cost down
0910 for EE BACO mode request
0910 for AMD default
0909 for AMD default
100916 for EE power plane modify
100916 BACO function
0915 for EE BACO mode request

600 mils

RDSon=5m ohm

Vo=0.75(R1+R2)/R2

Park-LP	PWRCNTL0	PWRCNTL1	V-CORE
L	0	0	0.9V
M	0	1	1V
H	1	0	1.1V(defult)
TBD	1	1	NA

1.5A
0.06A
(5A)

NB5	PROJECT : R13 Quanta Computer Inc.	
Size: Custom	Document Number: +VGACORE (RT8208/1.8V)	Rev: 3A
Date: Saturday, September 18, 2010	Sheet 39 of 39	