RTS5210

POWER

- AC/BATT CONNECTOR
- BATT CHARGER
- CPU CORE
- 5V/ 3.3VSTBY
- 1.5V/ 0.75_VTT_DDR
- 1.1VS
- 1.05VS
- 1.8VS LDO
- 2.5VS LDO
- 1.1VSTBY_SB LDO
- DGPU VCORE
- SUS/ RUN PWR Switch

Page 39 ~ 47

EMI/ Moat CAP Page 48

History Page 49, 50

DDR3-SODIMM Page 5 — DDR III 1066/ 1333MHZ

DDR3-SODIMM Page 6 — DDR III 1066/1333MHZ

Dual/ Single Core CPU
AMD
Danube
Dual:35W Page 2, 3, 4

1066 MHz HT

VRAM Page 22, 23

64MX16
HYNIX: HPMH-14-00D0000040G
SAMSUNG: HPMH-14-00D0000042G
128MX16:
Hynix: HPMH-14-00D0000039G
Samsung: HPMH-14-00D0000043G

DGPU with Muxless
ATI
Seymour/ Whistler
15.6"/17.3" Muxless Hybrid:
Seymour 64bit 15W + DDR3 x4
Whistler 128bit 25W + DDR3 x8
M2 package 29 x 29 FCBGA962
Seymour XT:
HPMH-10-0020000049G
Whistler Pro:
HPMH-10-0020000050G
Page 15, 16, 17, 18, 19, 20, 21

Side-Port 128M Page 9

PCIE 8X

North Bridge
ATI
RS880M
HPMH-10-0010000096G
Page 7, 8, 9, 10

HDMI — **HDMI Conn** Page 25

CRT — **D-sub Conn** Page 26

Cable/ 2ch LVDS — **LVDS + Touch**
LVDS 15"/17": 2 ch HD+ 1600x900
2 ch FHD 1920x1080
Page 24

USB2.0 x 1

Page 27

HDD Conn 2nd for 17.3" only — Cable

HDD Conn — Cable — SATA 3: 6Gbps

ODD Conn Zero Power ODD Intel: Saving 100 ~ 160mW — Cable — SATA 2: 3Gbps

PCI-E x 1 — **Cardreader** Realtek RTS5209 Page 31 — **BToB Conn** — 17.3": daughter Board — **2 in 1 Slot** 1) SD/SDHC/SDXC 2) MMC

PCI-E x 1 — **USB3.0 TI TUSB7320** Page 33 — USB2.0/ 3.0 — USB2.0 — **USB2.0/3.0 cnn** Wake Up; **USB2.0/3.0 cnn** Wake Up — Page 34

PCI-E

A-link (PCIE x 4)

PCI-E x 1 / USB2.0 x 1 — **WLAN Half MINI-CARD** Page 30

Int. CLK

South Bridge
AMD
SB820M
HPMH-10-0010000106G
Page 11, 12, 13, 14

USB2.0 — USB2.0 x 2 — **Conn** — Cable
- **USB Conn** Wake Up
- **USB Conn** Wake Up
- **Standby LED** White blink
- **HDD LED** Dual LED White: Normal , Amber: Park

15.6"/17.3" x2 daughter board

WebCam Conn White LED: Enable — Sensor OVT 9726 Dual DMic Page 28 — Cable

Fingerprint Validaty Module VFM5131 Dual LED x1: White normal, Amber not reconized Page 28 — Cable

SATA

USB2.0

SPI BIOS — SPI

G SENSOR ST Micro HP3DC Page 27

RTC Cell Conn — Cable

25M **32.768K** Crystal

PCI-E x 1 — **Realtek Gb LAN** RTL8111E-VB-GR W/ASPM Page 32 — No cable: NIC auto disabled. — **Magnetic** — **RJ45** LED White x1 for connectivity, Amber x1 for activity

15.6"/17.3" daughter board — Cable embeded — **TouchPad LED daughter board** — Conn

Dual LED White: AC in Amber: Charging — **Charge LED**

SPI 512KB 25

Crystal Free **32.768K**

SIO
ITE
ITE8518
Page 29

LPC

HDA

Module board — **HP Logo LED Module** — Conn — Cable embeded

Lid Switch Page 28

Thermal Page 30

FAN Conn Page 30 — Cable embeded

Cable — **Keyboard Conn** Page 29

KB with:
White LEDx1: Cap lock
Amber LEDx1:Mute
White/Amber dual LEDx1: wireless
NumLock LED x1: 17" only

Cable — **Touchpad Conn** Page 28

Amber LED x1:
Amber: T/P off
On/Off by tapping LED

Conn — **PWR Button / White LEDx1** Blink White: Standby — **Quick Web Button / LED x1**

15.6"/17.3" daughter board

AUDIO CODEC
IDT
92HD80TA
Page 35, 36, 37

LDO TPS793475DBVR

SPK AMP TPA3113D2 — **Internal Speaker Conn x4 speakers**

Correct should be: TI TPA2012 — **Internal DMic Conn To Webcam**

Microphone x1

HP AMP TPA6130A2 — **Headphone Microphone Combo Conn x2**

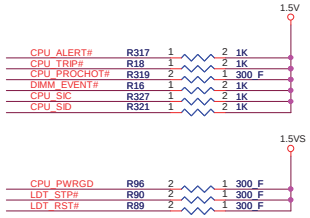
Woofer AMP TPA3111D1 — **WOOFER CONN** for 17.3" only

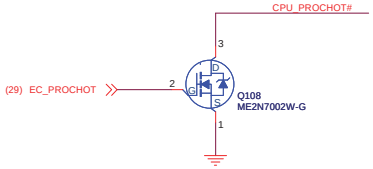
FLEX Computing

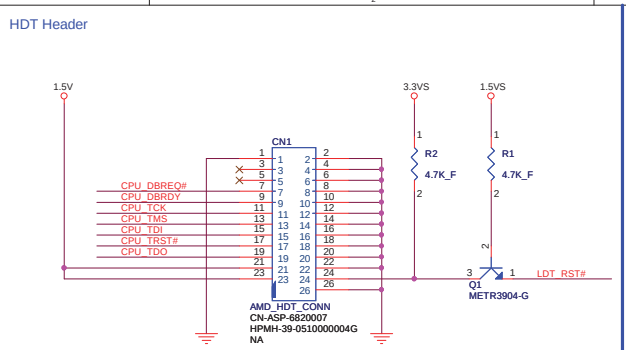
Project Name : H510UA1	Title : Block Diagram	
Size :	Document Number : HPMH-40GAB6300-D	Rev : D
Date: Thursday, December 30, 2010	Sheet : 1 of 51	

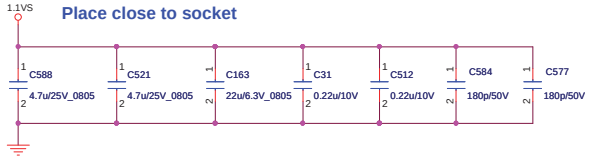
AMD Debug Termination

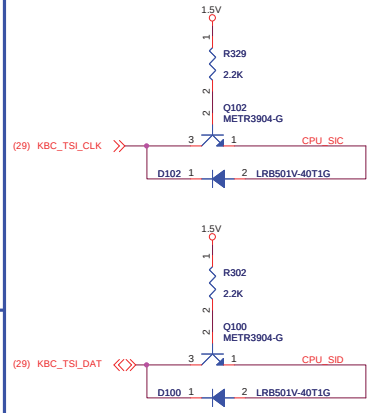
Signal Name	Type	Connection	Termination	Voltage
TEST6 TEST7 TEST8		Remain unconnected	-	
TEST9	I	Tie to VSS	-	VSS
TEST10		S1g2: Leave unconnected S1g3: Pulled up to VLDT (0603 DNI)		
TEST12		Test point access required for scan function. Connection to scan header preferred but not required.	1 K Ω to VSS No pop	VSS
TEST14 TEST15 TEST16 TEST17		Test point access required, header is preferred	-	-
TEST18,		Test point access required for scan function. Connection to scan header preferred but not required.	1 K Ω to VSS No pop	VSS
TEST19			1 K Ω to VSS No pop	VSS
TEST20			300 Ω[6]	VSS
TEST21			300 Ω[6]	VSS
TEST22			1 K Ω to VSS No pop	VSS
TEST23			300 Ω[6]	VSS
TEST24	I	Test point access required for scan function. Connection to scan header preferred but not required.	300 Ω[6]	VSS
TEST25_H			510 Ω[6]	VSS
TEST25_L			510 Ω[6]	VDDIO
TEST27 TEST28_H TEST28_L TEST29_H TEST29_L		Need test point on board	-	-

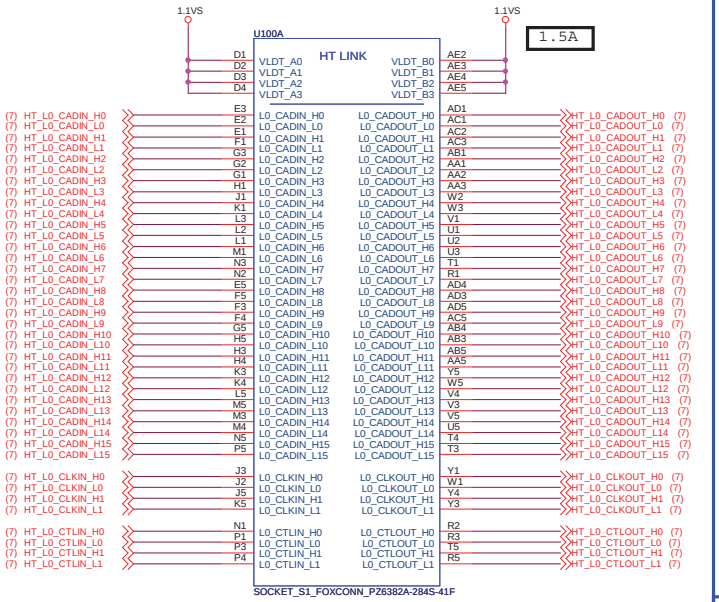


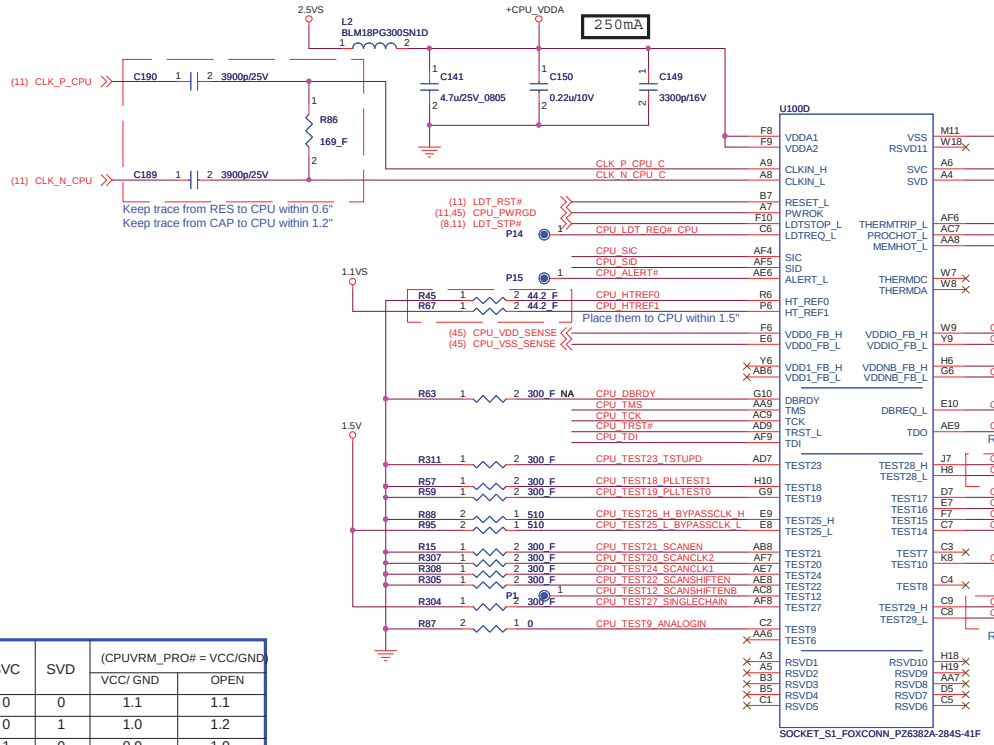












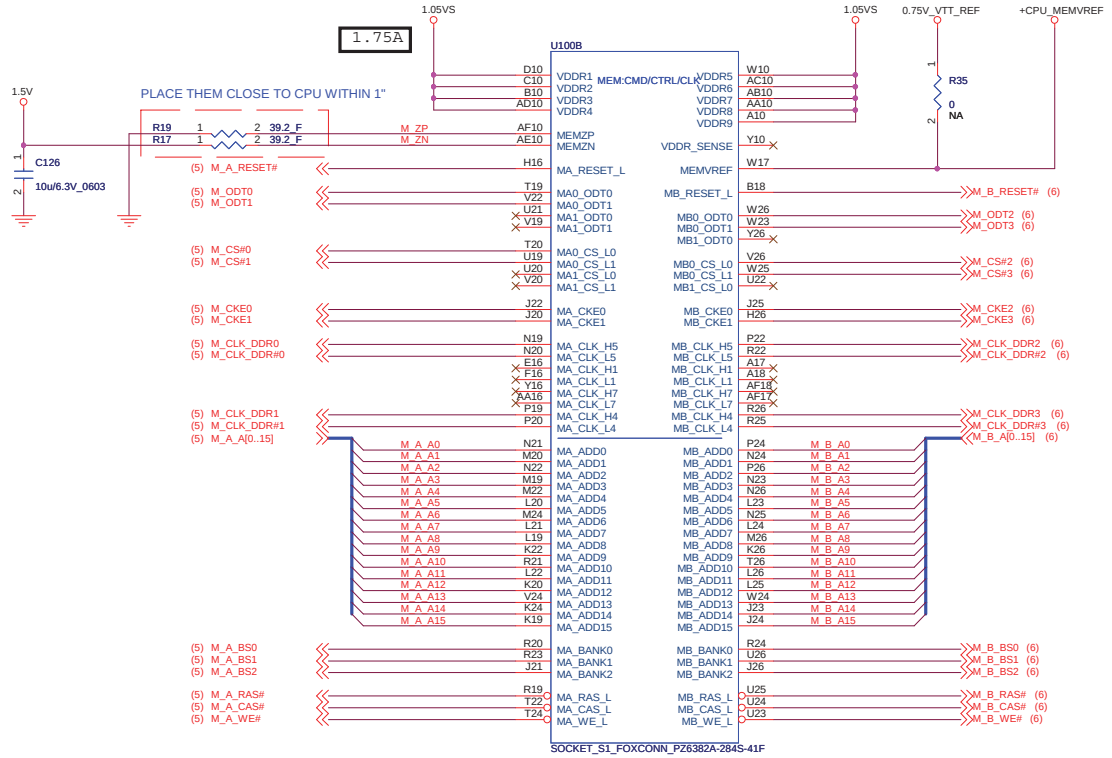
SVC	SVD	(CPUVRM_PRO# = VCC/GND)	
		VCC/ GND	OPEN
0	0	1.1	1.1
0	1	1.0	1.2
1	0	0.9	1.0
1	1	0.8	0.8

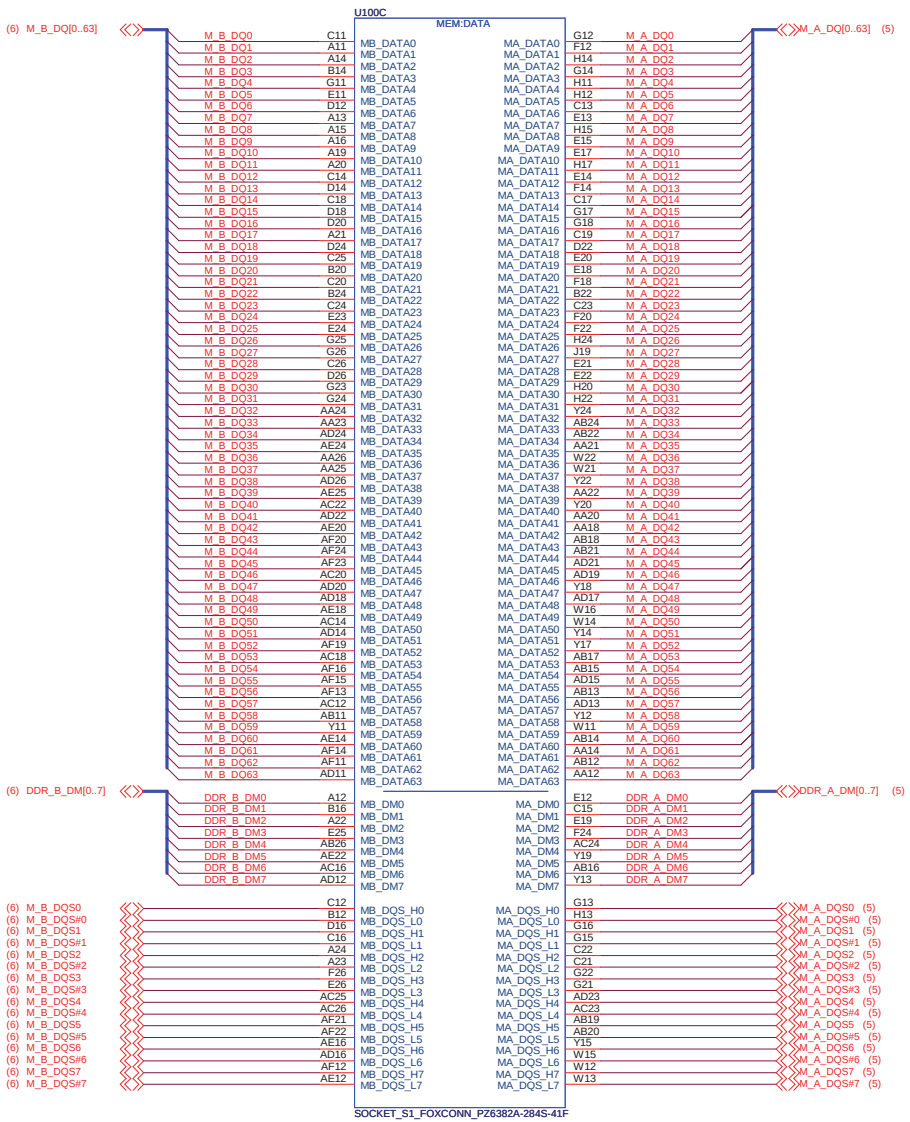
CPU HT/ MISC

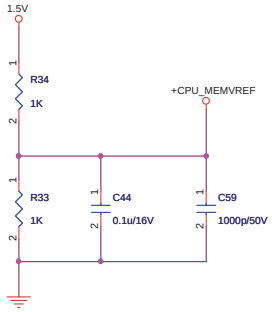
FLEX Computing

Project Name : H510UA1	Title : CPU - HT/ MISC I/F	
Size :	Document Number : HPMH-40GAB6300-D	Rev : D
Date: Thursday, December 30, 2010	Sheet : 2 of 51	

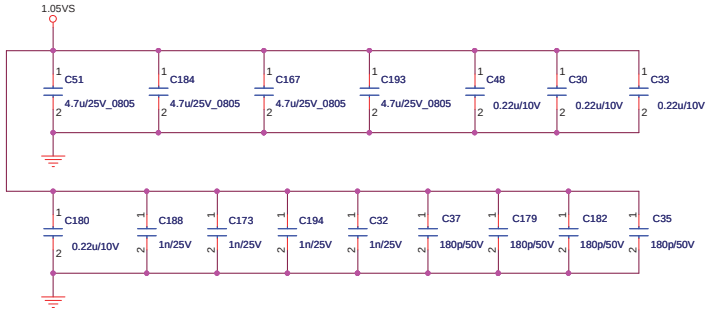
CPU Memory





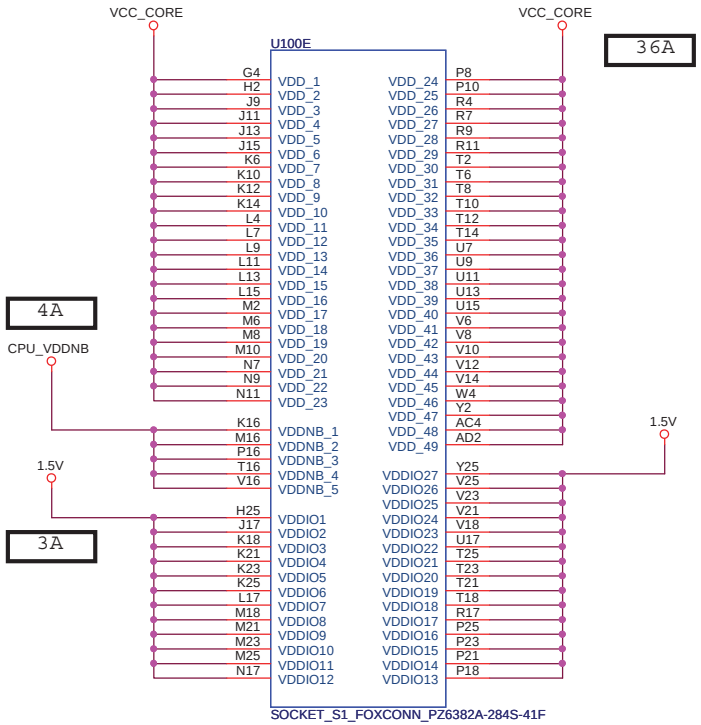


Place close to socket

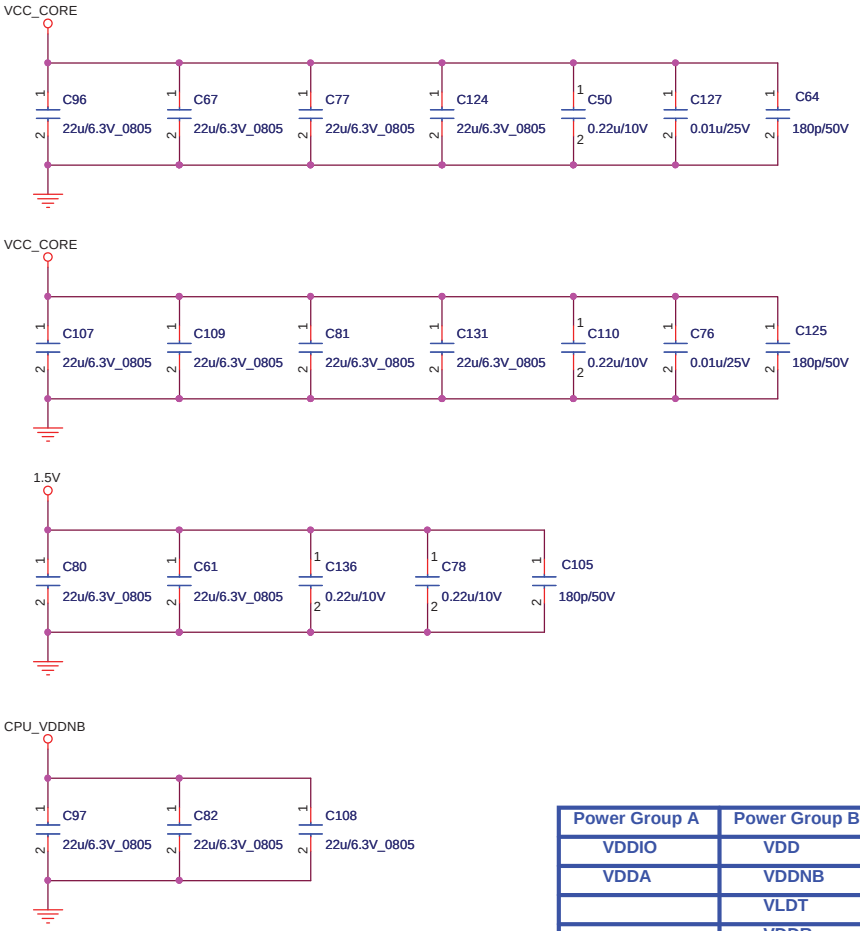


Project Name : H510UA1	Title : CPU - MEM I/F
Size :	Document Number : HPMH-40GAB6300-D — Rev : D
Date: Thursday, December 30, 2010	Sheet : 3 of 51

CPU PWR

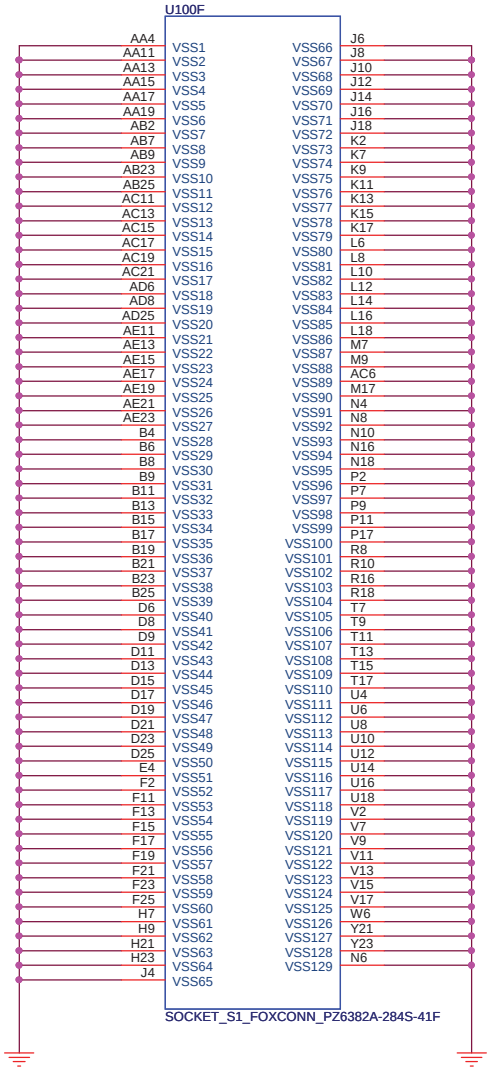


BOTTOM SIDE DECOUPLING

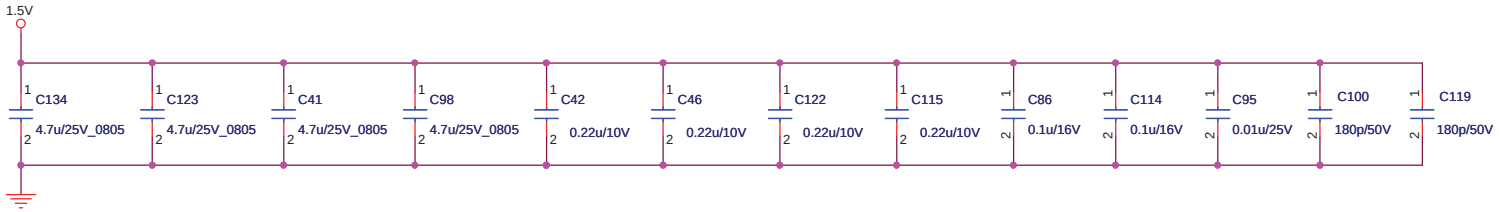


Power Group A	Power Group B
VDDIO	VDD
VDDA	VDDNB
	VLDT
	VDDR

CPU GND



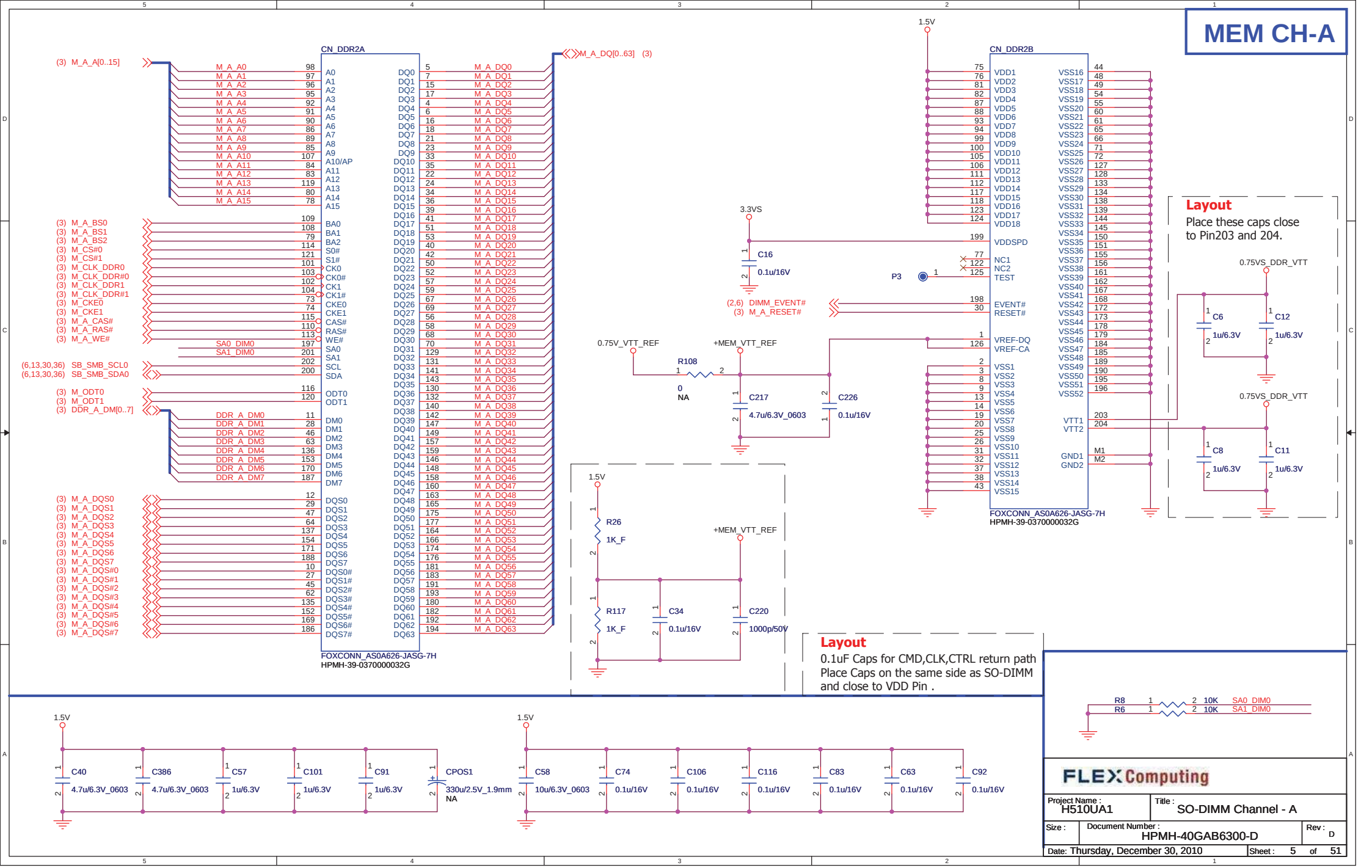
DECOUPLING BETWEEN PROCESSOR AND DIMMs
PLACE CLOSE TO PROCESSOR AS POSSIBLE



FLEXComputing

Project Name : H510UA1	Title : CPU - PWR/ GND	
Size :	Document Number : HPMH-40GAB6300-D	Rev : D
Date: Thursday, December 30, 2010	Sheet : 4 of 51	

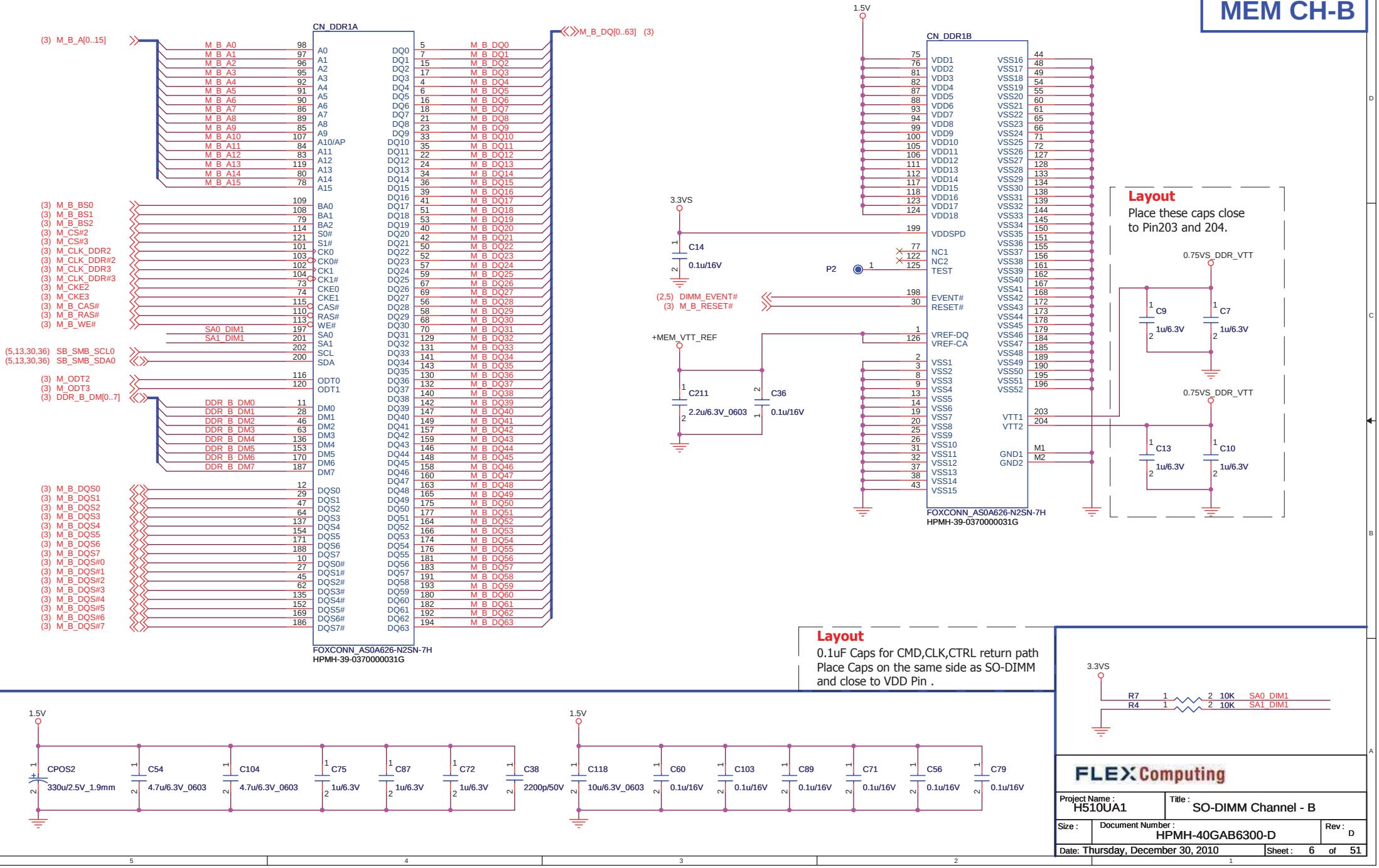
MEM CH-A



FLEXComputing

Project Name : H510UA1	Title : SO-DIMM Channel - A	
Size :	Document Number : HPMH-40GAB6300-D	Rev : D
Date: Thursday, December 30, 2010	Sheet : 5 of 51	

MEM CH-B

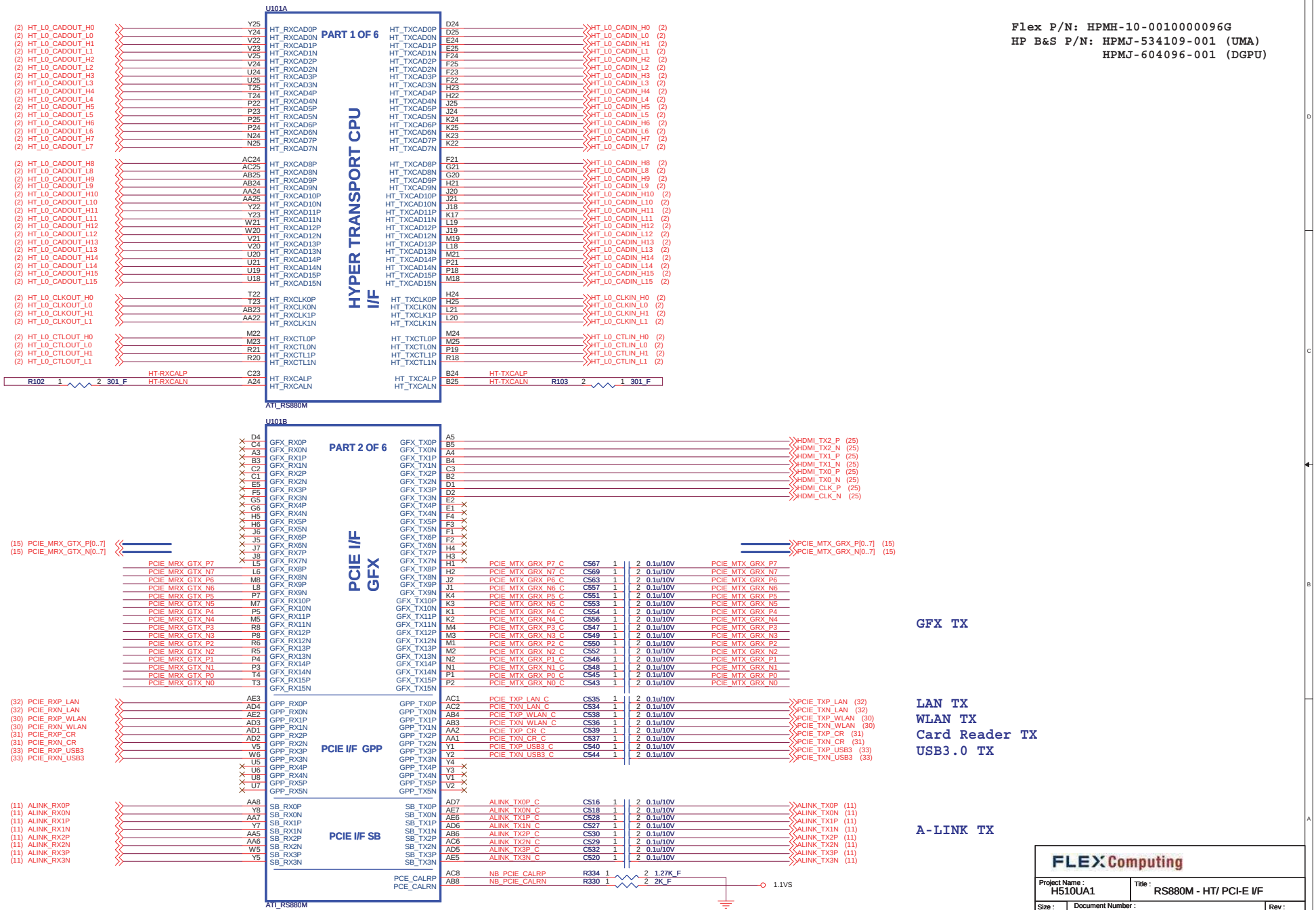


FLEXComputing

Project Name : H510UA1	Title : SO-DIMM Channel - B
Size :	Document Number : HPMH-40GAB6300-D — Rev : D
Date: Thursday, December 30, 2010	Sheet : 6 of 51

NB HT/ PCIE

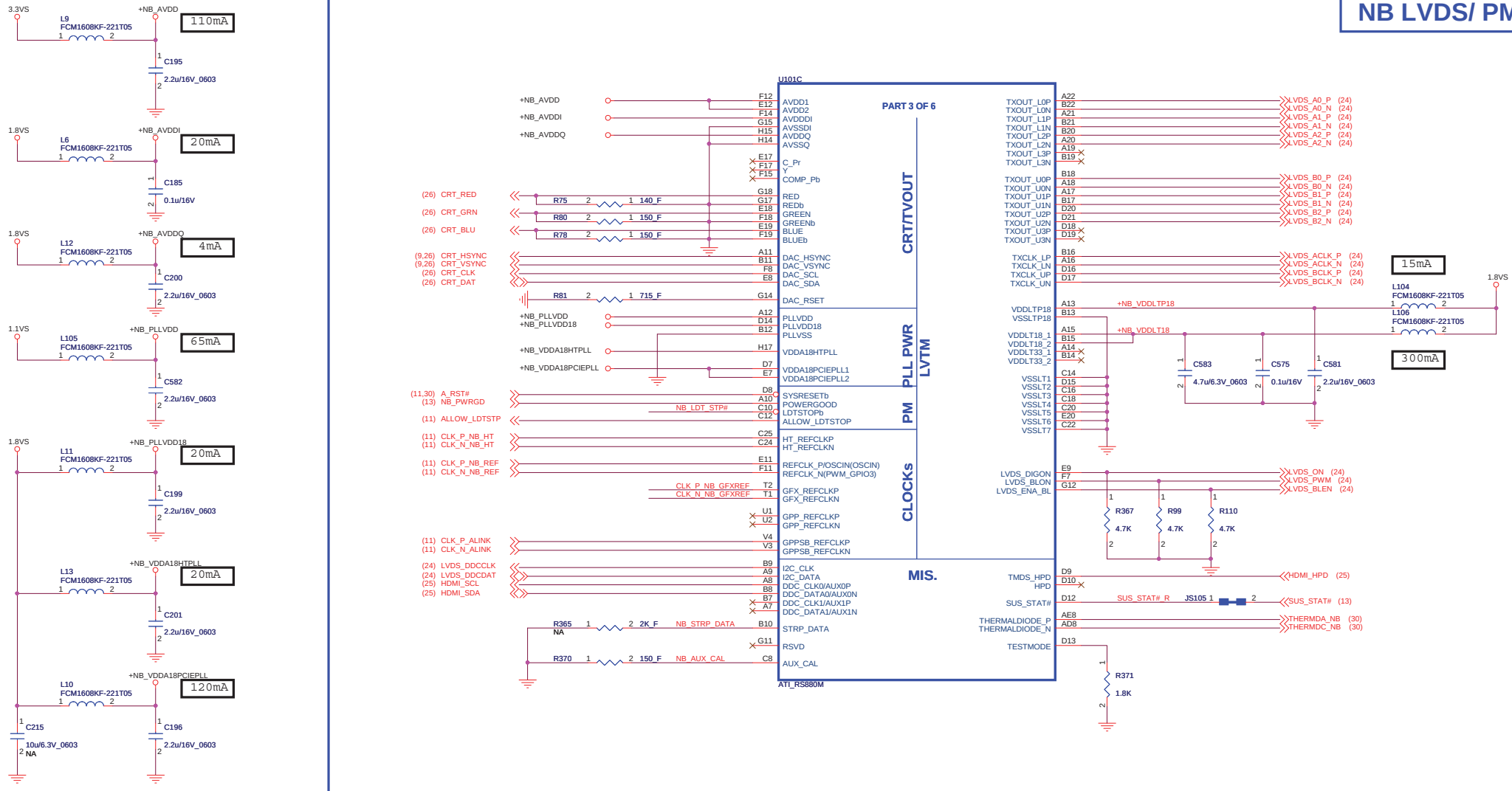
Flex P/N: HPMH-10-0010000096G
HP B&S P/N: HPMJ-534109-001 (UMA)
HPMJ-604096-001 (DGPU)

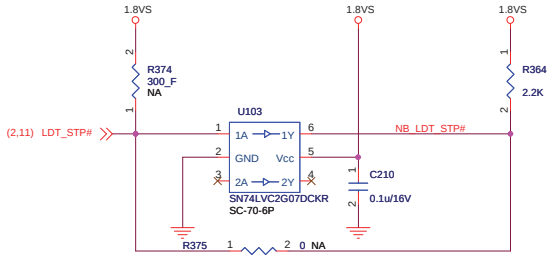


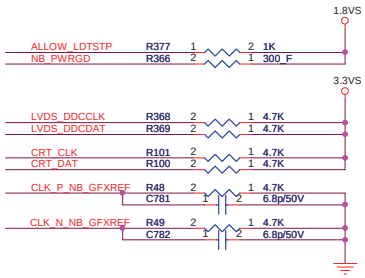
FLEX Computing

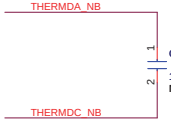
Project Name : H510UA1	Title : RS880M - HT/ PCI-E I/F	
Size :	Document Number : HPMH-40GAB6300-D	Rev : D
Date: Thursday, December 30, 2010	Sheet : 7 of 51	

NB LVDS/ PM





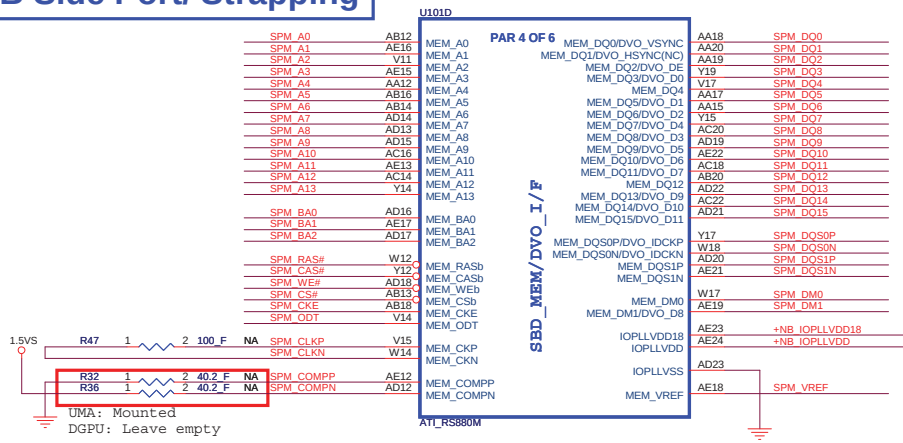


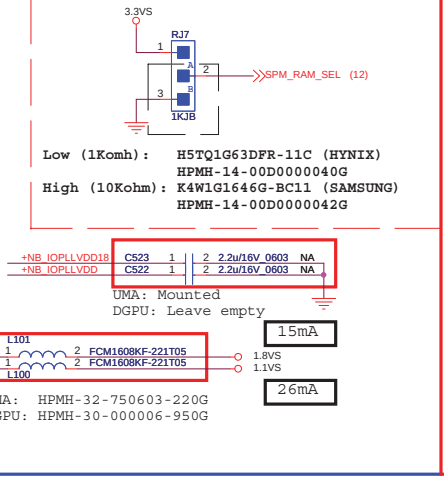


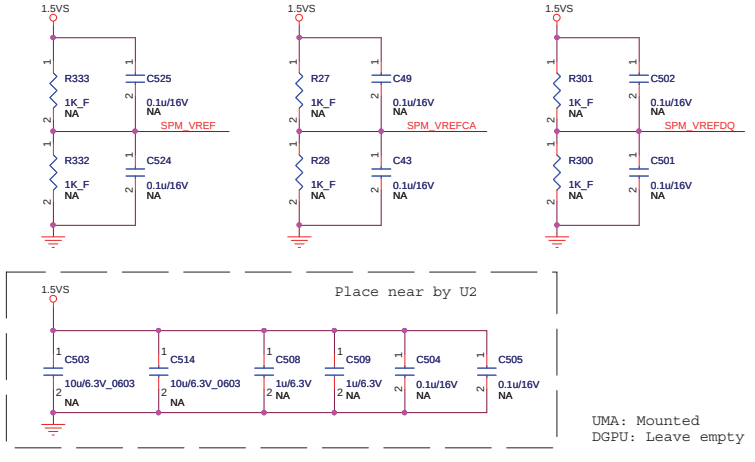
FLEX Computing

Project Name : H510UA1	Title : RS880M - LVDS/ PM I/F
Size :	Document Number : HPMH-40GAB6300-D
Rev : D	
Date: Thursday, December 30, 2010	Sheet : 8 of 51

NB Side Port/ Strapping

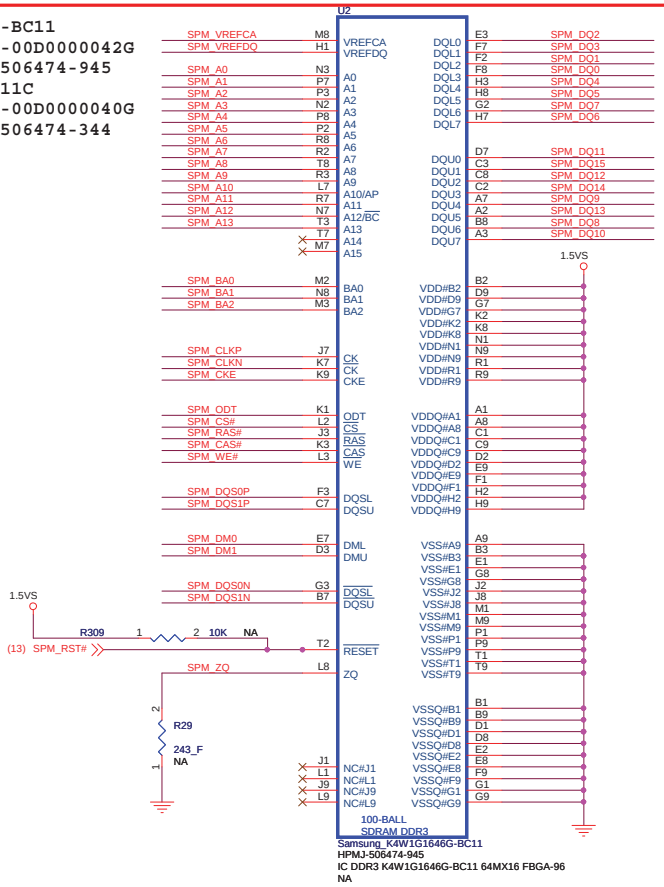






Samsung/ K4W1G1646G-BC11
Flex P/N: HPMH-14-00D0000042G
HP B&S P/N: HPMJ-506474-945
Hynix/ H5TQ1G63DFR-11C
Flex P/N: HPMH-14-00D0000040G
HP B&S P/N: HPMJ-506474-344

UMA: Mounted
DGPU: Leave empty

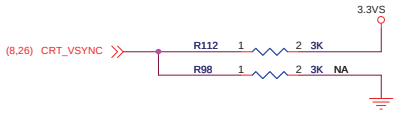


RS880M H/W STRAPS

The strap values are latched into internal registers after the assertion of the POWERGOOD signal to the RS880M

STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.
DAC_VSYNC (RS880.Pin B11)
1 = Disable (default)
0 = Ensable

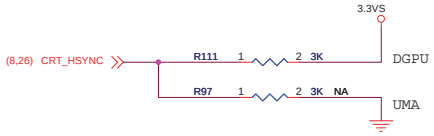


DFT_GPIO1: LOAD_EEPROM_STRAPS

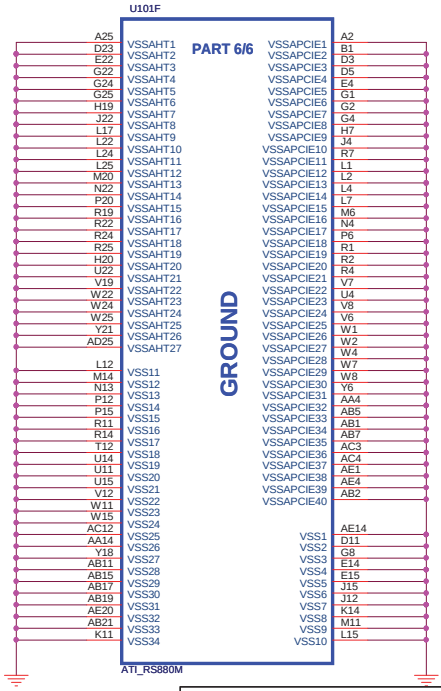
Selects Loading of STRAPS from EPROM.
SUS_STAT# (RS880.Pin D12)
1 = Bypass the loading of EEPROM straps and use Hardware Default Values
0 = I2C Master can load strap values from EEPROM if connected, or use default values if not connected

RS880: Enable Side Port Memory

Selects if Memory SIDE PORT is available or not
DAC_HSYNC (RS880.Pin A11)
1 : Disable (default)
0 : Enable
Register Readback of strap:
NB_CLKCFG:CLK_TOP_SPARE_D[1]



NB GND

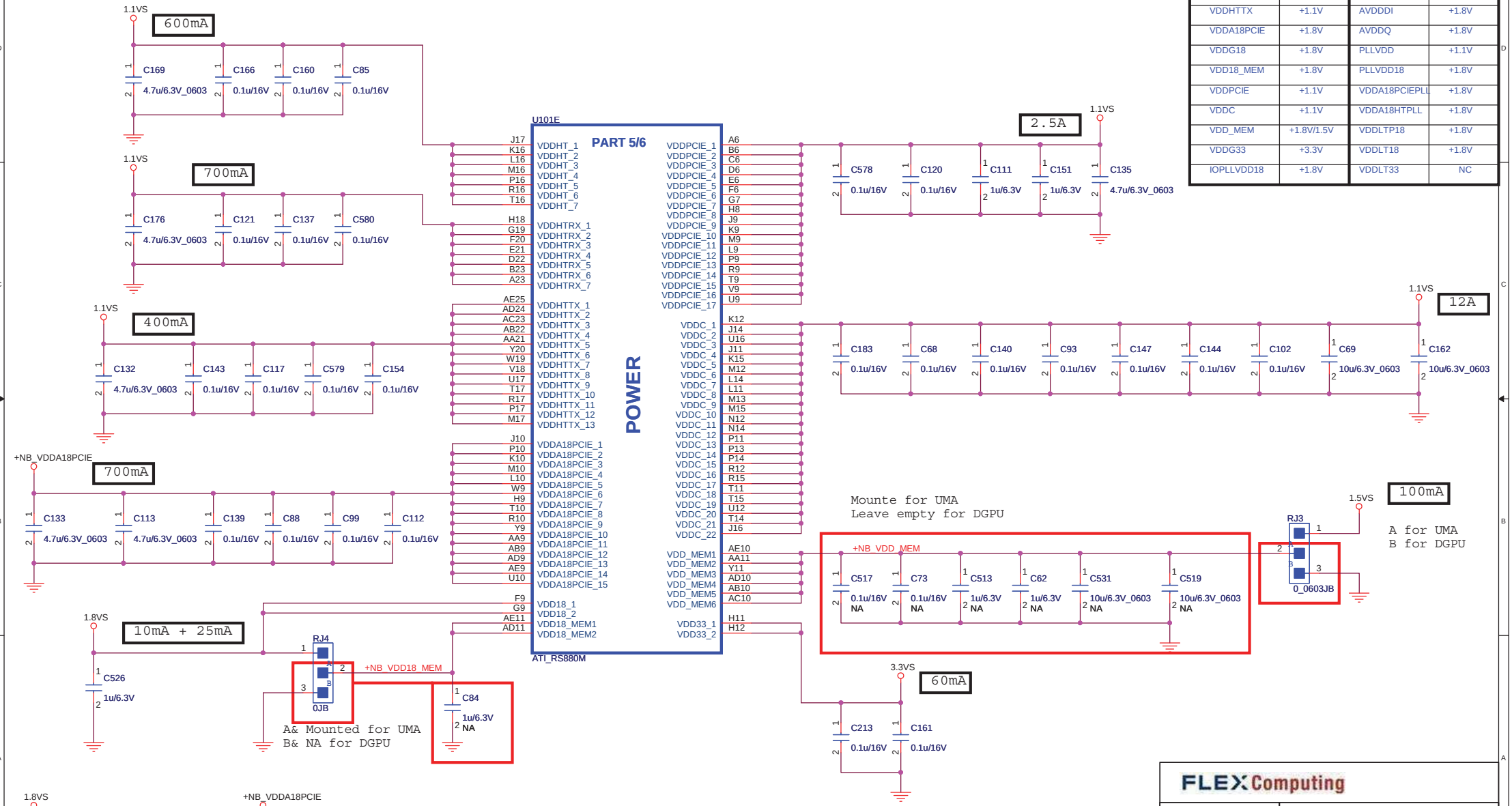


FLEX Computing	
Project Name : H510UA1	Title : RS880M - Side Port/ Strap/ GND
Size :	Document Number : HPMH-40GAB6300-D — Rev : D
Date: Thursday, December 30, 2010	Sheet : 9 of 51

NB PWR

RS880M POWER TABLE

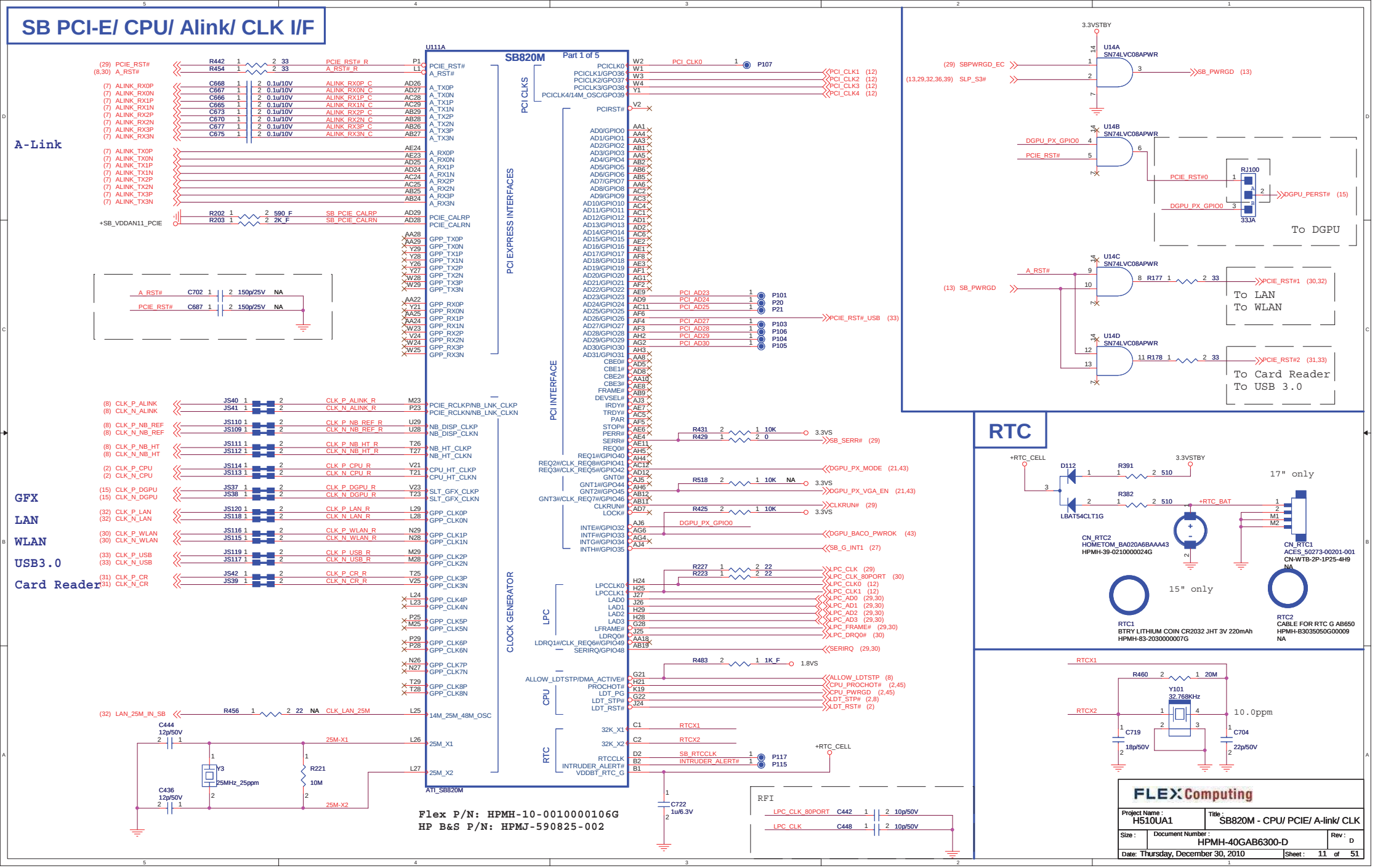
PIN NAME	RS880M	PIN NAME	RS880M
VDDHT	+1.1V	IOPLLVDD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.1V	AVDDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVDD	+1.1V
VDD18_MEM	+1.8V	PLLVDD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	+1.8V/1.5V	VDDLTP18	+1.8V
VDDG33	+3.3V	VDDLT18	+1.8V
IOPLLVDD18	+1.8V	VDDLT33	NC



FLEXComputing

Project Name : H510UA1	Title : RS880M - PWR
Size :	Document Number : HPMH-40GAB6300-D Rev : D
Date: Thursday, December 30, 2010	Sheet : 10 of 51

SB PCI-E/ CPU/ Alink/ CLK I/F



FLEX Computing	
Project Name : H510UA1	Title : SB820M - CPU/ PCIE/ A-link/ CLK
Size :	Document Number : HPMH-40GAB6300-D — Rev : D
Date: Thursday, December 30, 2010	Sheet : 11 of 51

SB820M Debug Straps

PciPllByp (PCI AD27)

Bypass PCI PLL
(Used in funcitonal test at tester):

L: Bypass internal PLL clock
H: Use internal PLL generated PLL CLK (Internal Pull-Up of 15Kohm)

ILAAutorunEnB (PCI AD26)

ILA Auto run Enable
L: ILA Auto run enable
H: ILA Auto run disable (Internal Pull-Up of 15Kohm)

FCClkByP (PCI AD25)

Bypass FC CLK
L: Bypass internal FC CLK (Used in funcitonal test at tester)
H: Use internal FC CLK

I2CROMEn (PCI AD24)

I2C ROM Enable. Load the setting for A-Link Express/ PLL/ music control from I2C ROM

L: Getting the value from I2C EPROM
H: Disable I2C ROM
(Internal Pull-Up of 15Kohm)

PCI_ROM_BOOT (PCI AD23)

Booting from PCI memory

L: Route ROM fetch tp PCI bus on the very first boot. Use ROMTYPE to determine the ROM type on the subsequent boots.
H: Use ROMTYPE straps to determine the ROM type
(Internal Pull-Up of 15Kohm)

PCIe EEPROM Data/ Clock (PCI_REQ3/ PCI_GNT3)

PCIe EEPROM Data/ Clock

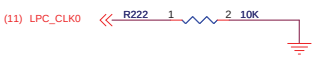
Connected to PCIe EEPROM SDA/ SCL pin or provided test point access for lad use.

SB820M H/W STRAPS

Type I are captured on RSMRST#
Type II are captured on PWRGD.

ECEnableStrap (LPCCLK0)

Embedded Controller (EC):
L: Disable
H: Enable



CLKGEN (LPCCLK1)

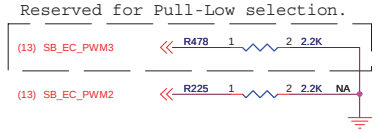
Define Clock Generator:
L: External clock mode
H: Internal clock mode

ROMTYPE_1&0 (EC_PWM3& EC_PWM2)

ROMTYPE_1 EC_PWM3	ROMTYPE_0 EC_PWM2	ROM type
0	0	FWH
0	1	LPC& PMC ROM
1	0	SPI
1	1	Reserve

Default Pull-High Pull-Low --> 2.2Kohm

Reserved for Pull-Low selection.



BIF_GEN2_COMPLIANCE_Strap (PCI CLK1)

Set PCIe to Gen II mode:
SB820M: Omly provision for Pull down is required, not install by default.

BootFailTmrEn (PCI CLK2)

Watchdog function:
L: Disable BootFailtmr function
H: Enable BootFailtmr function

DefaulStrapMode (PCI CLK3)

Default Debug Straps:
L: Disable Debug Straps
H: Select external Debug Straps

CPUClkSel (PCI CLK4)

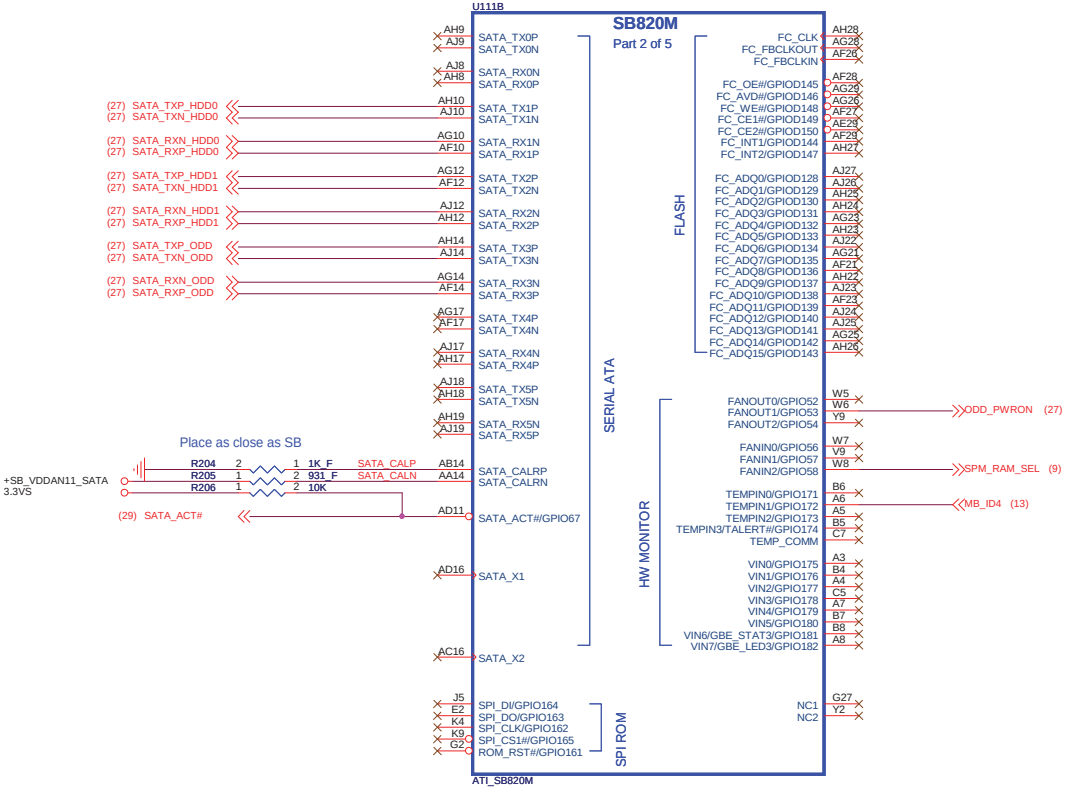
CPU/ NB HT Clock Selection:
L: Reserved
H: Required setting for integrated clock mode

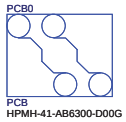
CoreSpeedMode (AZ_SDOUT)

Slow down core clock for low power mobile platform:

L: Performance Mode
H: Low Power Mode

SB SATA/ SPI/ STRAP





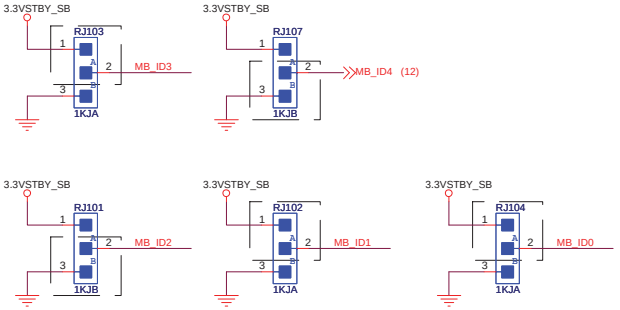
Type I : LPCCLK0, EC_PWM3& EC_PWM2
Type II : the rest of strapping

FLEX Computing

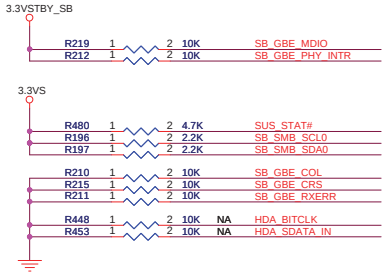
Project Name : H510UA1	Title : SB820M - SATA/ SPI/ Strap
Size :	Document Number : HPMH-40GAB6300-D Rev : D
Date: Thursday, December 30, 2010	Sheet : 12 of 51

SB ACPI/ USB/ HDA

Mother Board ID:



ID4	ID3	ID2	ID1	ID0	Board ID	Board ID
0	0	1	1	0	0x366A	Kelly 1.x UMA (IMR)
0	0	1	1	1	0x366B	Kelly 1.x Seymour XT (IMR)
0	1	0	0	0	0x366C	Kelly 1.x Whistler Pro (IMR)
0	1	0	0	1	0x1649	Kelly 1.x UMA
0	1	0	1	0	0x164A	Kelly 1.x Seymour XT
0	1	0	1	1	0x164B	Kelly 1.x Whistler Pro
0	1	1	0	0	0x164C	Young 1.x UMA
0	1	1	0	1	0x164D	Young 1.x Seymour XT
0	1	1	1	0	0x164E	Young 1.x Whistler Pro



Stage ID
High --> SI (Deflaut internal PU)
Low --> PV

R461 1K MB_ID5

U111D

SB820M
Part 4 of 5

P111	PCI_PME#	J2	PCI_PME#/GEVENT4#
	CR_GPIO	K1	RI#/GEVENT22#
		D3	SPI_CS3#/GBE_STAT1/GEVENT21#
(11,29,32,36,39)	SLP_S3#	F1	SLP_S3#
(29)	SLP_S5#	H1	SLP_S5#
(29)	SB_PWRBTN#	F2	PWR_BTN#
(11)	SB_PWRGD	H5	PWR_GOOD
(8)	SUS_STAT#	G6	SUS_STAT#
P114	SB_TEST0	B3	TEST0
P116	SB_TEST1	C4	TEST1/TMS
P23	SB_TEST2	F6	TEST2
(29)	A20GATE	AD21	GA20IN/GEVENT0#
(29)	KB_RST#	AE21	KBRST#/GEVENT1#
(29)	SB_EXT_SCI#	K2	LPC_PME#/GEVENT3#
(29)	SB_EXT_SMI#	J29	LPC_SMI#/GEVENT23#
		H2	GEVENT5#
P110	SB_SYS_RST#	J1	SYS_RESET#/GEVENT19#
(32,33)	PCIE_WAKE#	H6	WAKE#/GEVENT8#
		F3	IR_RX1/GEVENT20#
P109	SB_TRIP#	J6	THRMTRIP#/SMBALERT#/GEVENT2#
(8)	NB_PWRGD	AC19	NB_PWRGD
R241	NB_PWRGD_R		
(29)	RSMRST#	G1	RSMRST#
R240	RSMRST#_R		
		AD19	CLK_REQ4#/SATA_IS0#/GPIO64
(31)	CR_CLKREQ#	AA16	CLK_REQ3#/SATA_IS1#/GPIO63
P19	SB_GPIO50	AB21	SMARTVOLT1/SATA_IS2#/GPIO50
(32)	LAN_CLKREQ#	AC18	CLK_REQ0#/SATA_IS3#/GPIO60
		AF20	SATA_IS4#/FANOUT3/GPIO55
		AE19	SATA_IS5#/FANIN3/GPIO59
(35)	SPKR	AF19	SPKR/GPIO66
(5,6,30,36)	SB_SMB_SCL0	AD22	SCL0/GPIO43
(5,6,30,36)	SB_SMB_SDA0	AE22	SDA0/GPIO47
P25	SB_SMB_SCL1	F5	SCL1/GPIO227
P24	SB_SMB_SDA1	F4	SDA1/GPIO228
(33)	USB3_CLKREQ#	AH21	CLK_REQ2#/FANIN4/GPIO62
(30)	WLAN_CLKREQ#	AB18	CLK_REQ1#/FANOUT4/GPIO61
		E1	IR_LED#/LLB#/GPIO184
P100	SB_SMARTV2	AJ21	SMARTVOLT2/SHUTDOWN#/GPIO51
(9)	SPM_RST#	H4	DDR3_RST#/GEVENT7#
P113	SB_GBE_LED0	D5	GBE_LED0/GPIO183
		D7	GBE_LED1/GEVENT9#
		G5	GBE_LED2/GEVENT10#
		K3	GBE_STAT0/GEVENT11#
		AA20	CLK_REQG#/GPIO65/OSCIN
(29)	SIO_EXT_WAKE#	H3	BLINK/USB_OC7#/GEVENT18#
(31)	CR_GPIO	D1	USB_OC6#/IR_TX1/GEVENT6#
P112	SB_USB_OC5#	E4	USB_OC5#/IR_TX0/GEVENT17#
	SB_ODD_DA#	D4	USB_OC4#/IR_RX0/GEVENT16#
(27)	ODD_PLUGIN#	E8	USB_OC3#/AC_PRES/TDO/GEVENT15#
(33)	USB3_SMI#	F7	USB_OC2#/TCK/GEVENT14#
(34)	USB_OC1#	E7	USB_OC1#/TDI/GEVENT13#
(38)	USB_OC0#	F8	USB_OC0#/TRST#/GEVENT12#
R451	10K NA		
R449	33 HDA_BITCLK_R	M3	AZ_BITCLK
R444	33 HDA_SDATA_OUT_R	N1	AZ_SDOUT
		L2	AZ_SDIN0/GPIO167
		M2	AZ_SDIN1/GPIO168
		M1	AZ_SDIN2/GPIO169
		M4	AZ_SDIN3/GPIO170
R443	33 HDA_SYNC_R	N2	AZ_SYNC
R441	33 HDA_RESET#_R	P2	AZ_RST#
SB_GBE_COL		T1	GBE_COL
SB_GBE_CRS		T4	GBE_CRS
		L6	GBE_MDCK
SB_GBE_MDIO		L5	GBE_MDIO
		T9	GBE_RXCLK
		U1	GBE_RXD3
		U3	GBE_RXD2
		T2	GBE_RXD1
		U2	GBE_RXD0
		T5	GBE_RXCTL/RXDV
SB_GBE_RXERR		V5	GBE_RXERR
		P5	GBE_TXCLK
		M5	GBE_TXD3
		P9	GBE_TXD2
		T7	GBE_TXD1
		P7	GBE_TXD0
		M7	GBE_TXCTL/TXEN
		P4	GBE_PHY_PD
		M9	GBE_PHY_RST#
SB_GBE_PHY_INTR		V7	GBE_PHY_INTR
		E23	PS2_DAT/SDA4/GPIO187
		E24	PS2_CLK/SCL4/GPIO188
		F21	SPI_CS2#/GBE_STAT2/GPIO166
		G29	FC_RST#/GPIO160
MB_ID0		D27	
MB_ID1		F28	PS2KB_DAT/GPIO189
MB_ID2		F29	PS2KB_CLK/GPIO190
MB_ID3		E27	PS2M_DAT/GPIO191
			PS2M_CLK/GPIO192

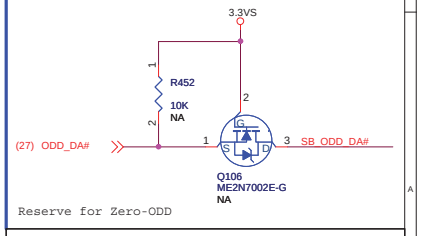
ATI_SB820M

ACPI / WAKE UP EVENTS
USB MISC
USB 1.1
GPIO
USB 2.0
USB OC
HD AUDIO
GBE LAN
EMBEDDED CTRL
EMBEDDED CTRL

			USBCLK/14M_25M_48M_OSC
A10	CLK_USB_48M_R	R479 22 NA	CLK_USB_48M (33)
G19	USB-RCOMP	R224 11.8K_F	USB_RCOMP
			USB_FSD1P/GPIO186
J10			USB_FSD1N
H11			
			USB_FSD0P/GPIO185
H9			USB_FSD0N
J8			
B12			USB_HSD13P
A12			USB_HSD13N
F11			USB_HSD12P
E11			USB_HSD12N
E14			USB_HSD11P
E12			USB_HSD11N
J12			USB_HSD10P
J14			USB_HSD10N
A13			USB_HSD9P
B13			USB_HSD9N
D13			USB_HSD8P
C13			USB_HSD8N
G12			USB_HSD7P
G14			USB_HSD7N
G16			USB_HSD6P
G18			USB_HSD6N
D16			USB_HSD5P
C16			USB_HSD5N
B14			USB_HSD4P
A14			USB_HSD4N
E18			USB_HSD3P
E16			USB_HSD3N
J16			USB_HSD2P
J18			USB_HSD2N
B17			USB_HSD1P
A17			USB_HSD1N
A16			USB_HSD0P
B16			USB_HSD0N
D25			SCL2/GPIO193
F23			SDA2/GPIO194
B26			SCL3_LV/GPIO195
E26			SDA3_LV/GPIO196
F25			EC_PWM0/EC_TIMER0/GPIO197
E22			EC_PWM1/EC_TIMER1/GPIO198
F22			EC_PWM2/EC_TIMER2/GPIO199
E21			EC_PWM3/EC_TIMER3/GPIO200
G24			KSI_0/GPIO201
G25			KSI_1/GPIO202
E28			KSI_2/GPIO203
E29			KSI_3/GPIO204
D29			KSI_4/GPIO205
D28			KSI_5/GPIO206
C29			KSI_6/GPIO207
C28			KSI_7/GPIO208
B28			KSO_0/GPIO209
A27			KSO_1/GPIO210
B27			KSO_2/GPIO211
D26			KSO_3/GPIO212
A26			KSO_4/GPIO213
C26			KSO_5/GPIO214
A24			KSO_6/GPIO215
B25			KSO_7/GPIO216
A25			KSO_8/GPIO217
D24			KSO_9/GPIO218
B24			KSO_10/GPIO219
C24			KSO_11/GPIO220
B23			KSO_12/GPIO221
A23			KSO_13/GPIO222
D22			KSO_14/GPIO223
C22			KSO_15/GPIO224
A22			KSO_16/GPIO225
B22			KSO_17/GPIO226

USB-TOUP_P (24) / USB-TOUP_N (24) — **Touch Screen**
USB-WEBCAM_P (28) / USB-WEBCAM_N (28) — **Web CAM**
USB-FP_P (28) / USB-FP_N (28) — **Finger Print**
USB-WLAN_P (30) / USB-WLAN_N (30) — **WLAN**
USB3_P (34) / USB3_N (34) — **Port 3**
USB2_P (34) / USB2_N (34) — **Port 2**
USB1_P (38) / USB1_N (38) — **Port 1**
USB0_P (38) / USB0_N (38) — **Port 0**

SB_EC_PWM2 (12)
SB_EC_PWM3 (12)



FLEX Computing

Project Name : H510UA1		Title : SB820M - ACPI/ USB/ HDA/ GLAN	
Size :	Document Number : HPMH-40GAB6300-D		Rev : D
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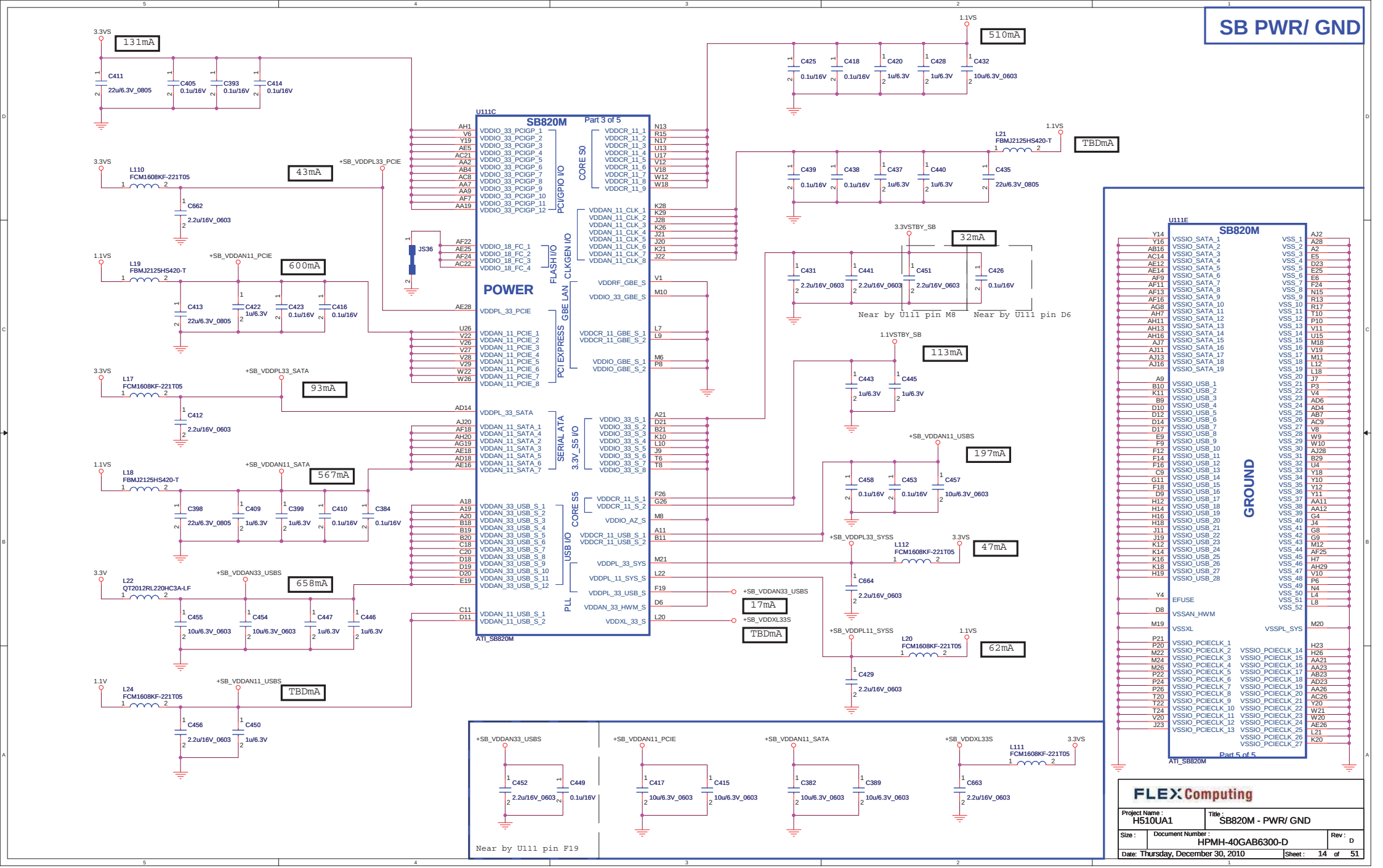
SB PWR/ GND
U111C
SB820M
Part 3 of 5
POWER
PCI/GPIO I/O
CORE S0
FLASH I/O
CLKGEN I/O
GBE LAN
PCI EXPRESS
SERIAL ATA
3.3V_S5 I/O
CORE S5
USB I/O
PLL
ATI_SB820M
U111E
GROUND
Part 5 of 5
131mA
43mA
600mA
93mA
567mA
658mA
TBDmA
510mA
32mA
113mA
197mA
47mA
17mA
62mA
Near by U111 pin M8
Near by U111 pin D6
Near by U111 pin F19
FLEXComputing
Project Name : H510UA1
Title : SB820M - PWR/ GND
Size :
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Rev : D
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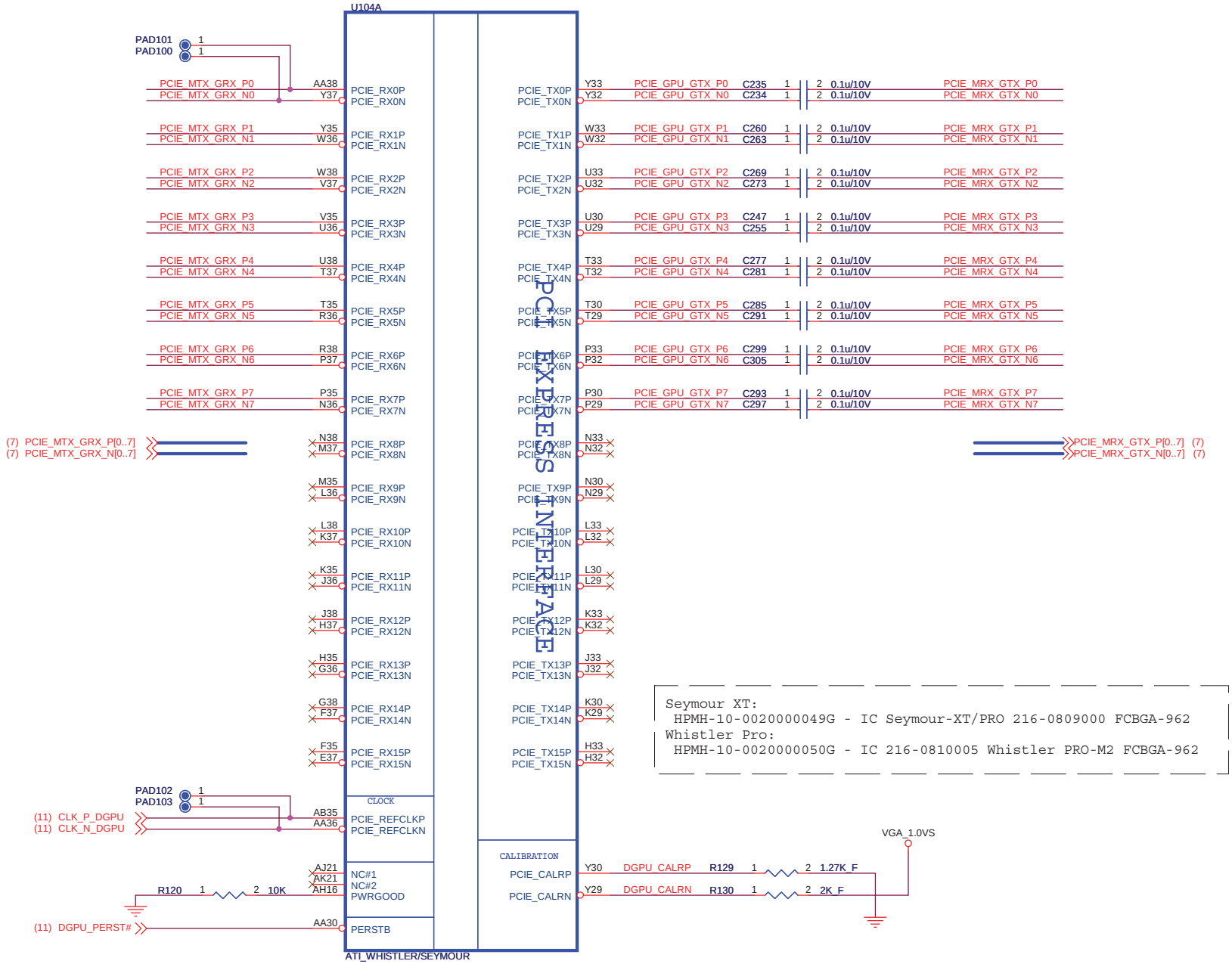
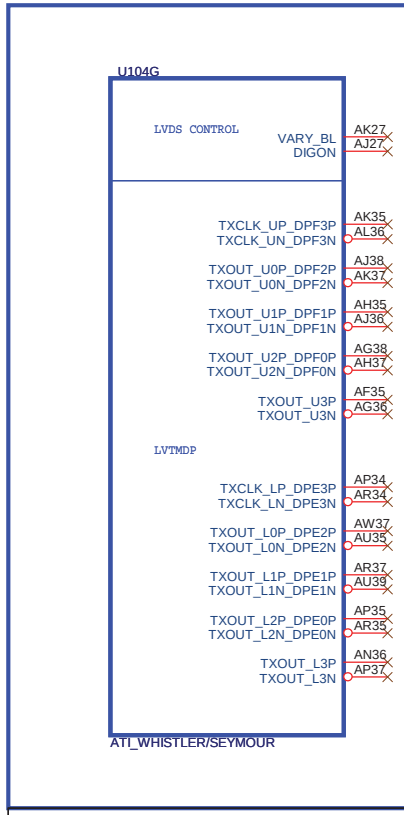
http://hobi-elektronika.net

DGPU PCIE/ LVDS

Seymour
Flex P/N: HPMH-10-0020000049G
HP B&S P/N: HPMJ-633843-001
Whistler
Flex P/N: HPMH-10-0020000050G
HP B&S P/N: HPMJ-628114-001



Seymour XT:
HPMH-10-0020000049G - IC Seymour-XT/PRO 216-0809000 FCBGA-962
Whistler Pro:
HPMH-10-0020000050G - IC 216-0810005 Whistler PRO-M2 FCBGA-962



PWRGOOD
For Broadway, Madison and Park the PWRGOOD ball must be conneccted to ground

FLEXComputing

Project Name : H510UA1	Title : DGPU - PCI-E/ LVDS I/F	
Size :	Document Number : HPMH-40GAB6300-D	Rev : D
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DGPU DISP/ THRM/ PM

	DVPDATA_2	DVPDATA_1	DVPDATA_0
Hynix (64Mx16) x4pcs	0	0	0
Samsung (64Mx16) x4pcs	1	0	0
Hynix (128Mx16) x4pcs	0	1	0
Samsung (128Mx16) x4pcs	1	1	0
Hynix (64Mx16) x8pcs	0	0	1
Samsung (64Mx16) x8pcs	1	0	1
Hynix (128Mx16) x8pcs	0	1	1
Samsung (128Mx16) x8pcs	1	1	1

64MX16
HYNIX:
Flex P/N: HPMH-14-00D0000040G - IC DDR3 H5TQ1G63DFR-11C 64MX16 FBGA-96
HP B&S P/N: HPMJ-506474-945
SAMSUNG:
Flex P/N: HPMH-14-00D0000042G - IC DDR3 K4W1G1646G-BC11 64MX16 FBGA-96
HP B&S P/N: HPMJ-506474-344

128MX16:
Hynix: HPMH-14-00D0000039G - IC DDR3 H5TQ2G63BFR-11C 128MX16 FBGA-96
Samsung: HPMH-14-00D0000043G - IC K4W2G1646C-HC11 128Mb*16 96 FBGA

VGA_1.8VS
VMEM ID
R342 1K
R341 1K
R343 1K
NC on Park
VMEM_ID0
VMEM_ID1
VMEM_ID2
PAD2 DGPU_DVPDATA3
NC on Park

U104B
MUTI GFX
DVPCNTL_MVP_0 DVPCNTL_MVP_1 DVPCNTL_0 DVPCNTL_1 DVPCNTL_2 DVPCLK
DVPDATA_0 DVPDATA_1 DVPDATA_2 DVPDATA_3 DVPDATA_4 DVPDATA_5 DVPDATA_6 DVPDATA_7 DVPDATA_8 DVPDATA_9 DVPDATA_10 DVPDATA_11 DVPDATA_12 DVPDATA_13 DVPDATA_14 DVPDATA_15 DVPDATA_16 DVPDATA_17 DVPDATA_18 DVPDATA_19 DVPDATA_20 DVPDATA_21 DVPDATA_22 DVPDATA_23
DPA: TXCAP_DPA3P TXCAM_DPA3N / TX0P_DPA2P TX0M_DPA2N / TX1P_DPA1P TX1M_DPA1N / TX2P_DPA0P TX2M_DPA0N
DPB: TXCBP_DPB3P TXCBM_DPB3N / TX3P_DPB2P TX3M_DPB2N / TX4P_DPB1P TX4M_DPB1N / TX5P_DPB0P TX5M_DPB0N
DPC: TXCCP_DPC3P TXCCM_DPC3N / TX0P_DPC2P TX0M_DPC2N / TX1P_DPC1P TX1M_DPC1N / TX2P_DPC0P TX2M_DPC0N
DPD: TXCDP_DPD3P TXCDM_DPD3N / TX3P_DPD2P TX3M_DPD2N / TX4P_DPD1P TX4M_DPD1N / TX5P_DPD0P TX5M_DPD0N
I2C: SCL SDA
GENERAL PURPOSE I/O: GPIO_0 GPIO_1 GPIO_2 GPIO_3_SMBDATA GPIO_4_SMBCLK GPIO_5_AC_BATT GPIO_6 GPIO_7_BLON GPIO_8_ROMSO GPIO_9_ROMSI GPIO_10_ROMSCK GPIO_11 GPIO_12 GPIO_13 GPIO_14_HPD2 GPIO_15_PWRCNTL_0 GPIO_16_SSIN GPIO_17_THERMAL_INT GPIO_18_HPD3 GPIO_19_CTF GPIO_20_PWRCNTL_1 GPIO_21_BB_EN GPIO_22_ROMCSB GPIO_23_CLKREQB
JTAG_TRSTB JTAG_TDI JTAG_TCK JTAG_TMS JTAG_TDO
GENERICA GENERICB GENERICC GENERICD GENERICE_HPD4 GENERICF GENERICG
HPD1
VREFG
DPLL_PVDD DPLL_PVSS DPLL_VDDC
PLL/CLOCK: XTALIN XTALOUT XO_IN SS_IN
THERMAL: DPLUS DMINUS
TS_FDO TS_A
TSVDD TSVSS
ATI_WHISTLER/SEYMOUR

VGA_3.3VS
R352 10K
D7 LRB501V-40T1G
(29) DGPU_AC_BATT
DGPU_AC_BATT_R
PAD16 DGPU_SMBSCL
PAD17 DGPU_SMBDAT
(18) DGPU_GPIO0 (18) DGPU_GPIO1 (18) DGPU_GPIO2
PAD19 DGPU_GPIO6
PAD8 DGPU_GPIO7
(18) DGPU_GPIO8 (18) DGPU_GPIO9
PAD12 DGPU_GPIO10
(18) DGPU_GPIO11 (18) DGPU_GPIO12 (18) DGPU_GPIO13
PAD7 DGPU_GPIO14
To PWR PWM (43) PWRPLAY_VID0
PAD10 DGPU_GPIO16
DGPU_ALERT#
PAD3 DGPU_GPIO18
DGPU_THRMTRIP
To PWR PWM (43) PWRPLAY_VID1 (18) DGPU_GPIO21 (18) DGPU_GPIO22
PAD4 DGPU_CLKREQ#
PAD5 DGPU_TRST#
PAD9 DGPU_TDI
PAD15 DGPU_TCK
PAD11 DGPU_TMS
PAD6 DGPU_TDO
(18) DGPU_GENERICC

VGA_1.8VS
R339 499_F
VREF=0.6V
R340 249_F
C558 0.1u/10V
+DGPU_VREFG

+DGPU_DPLL_PVDD
+DGPU_DPLL_VDDC
C574 22p/50V
CLK27M_IN
CLK27M_OUT
R372 1M
Y100 27MHz_20pF
C587 22p/50V
(30) THERMDA_DGPU
(30) THERMDC_DGPU
PAD22
DGPU_FDO
ADC input (range 0 1.0V). This analog input signal can be used to measure regulator current or temperature for Broadway
VGA_1.8VS
C598 1u/6.3V

DAC1: R G B HSYNC VSYNC RSET AVDD AVSSQ VDD1DI VSS1DI
DGPU_CRT_R R395 150 F
DGPU_CRT_G R393 150 F
DGPU_CRT_B R390 150 F
DGPU_HSYNC (18)
DGPU_VSYNC (18)
R126 499 F
VGA_1.8VS
C207 0.1u/10V
C206 0.1u/10V
DAC2: R2 R2B G2 G2B B2 B2B C Y COMP VDD2DI VSS2DI A2VDD A2VDDQ A2VSSQ R2SET
NC on Seymour / Whistler
GENLK_CLK/ GENLK_VSYNC
DGPU_H2SYNC (18)
DGPU_V2SYNC (18)
DDC/AUX: DDC1CLK DDC1DATA / AUX1P AUX1N / DDC2CLK DDC2DATA / AUX2P AUX2N / DDCCLK_AUX3P DDCDATA_AUX3N / DDCCLK_AUX4P DDCDATA_AUX4N / DDCCLK_AUX5P DDCDATA_AUX5N / DDC6CLK DDC6DATA / DDCCLK_AUX7P DDCDATA_AUX7N
DDCxx_AUX3x is NC on M92M2
DDCxx_AUX4x is NC on M92M2 and PARK
DDCxx_AUX7x is NC on M9x and PARK
DGPU_CRT_CLK2 P27
DGPU_CRT_DAT2 P26
DGPU_CRT_CLK P16
DGPU_CRT_DAT P17

(29) GPU_TRIP#
M8 ME2N7002E-G
DGPU_THRMTRIP
R73 100K

VGA_1.8VS
L108 FCM1608KF-121T06
+DGPU_DPLL_PVDD
C595 1u/6.3V
C594 0.1u/10V

VGA_1.0VS
L107 FCM1608KF-121T06
+DGPU_DPLL_VDDC
C590 1u/6.3V
C591 0.1u/10V

VGA_3.3VS
R389 10K DGPU_ALERT#
R358 10K DGPU_TRST#
R346 10K DGPU_TDI
R349 10K DGPU_TMS
R357 10K DGPU_TCK

FLEX Computing

Project Name : H510UA1	Title : DGPU - Display/ Thermal/ GPIO	
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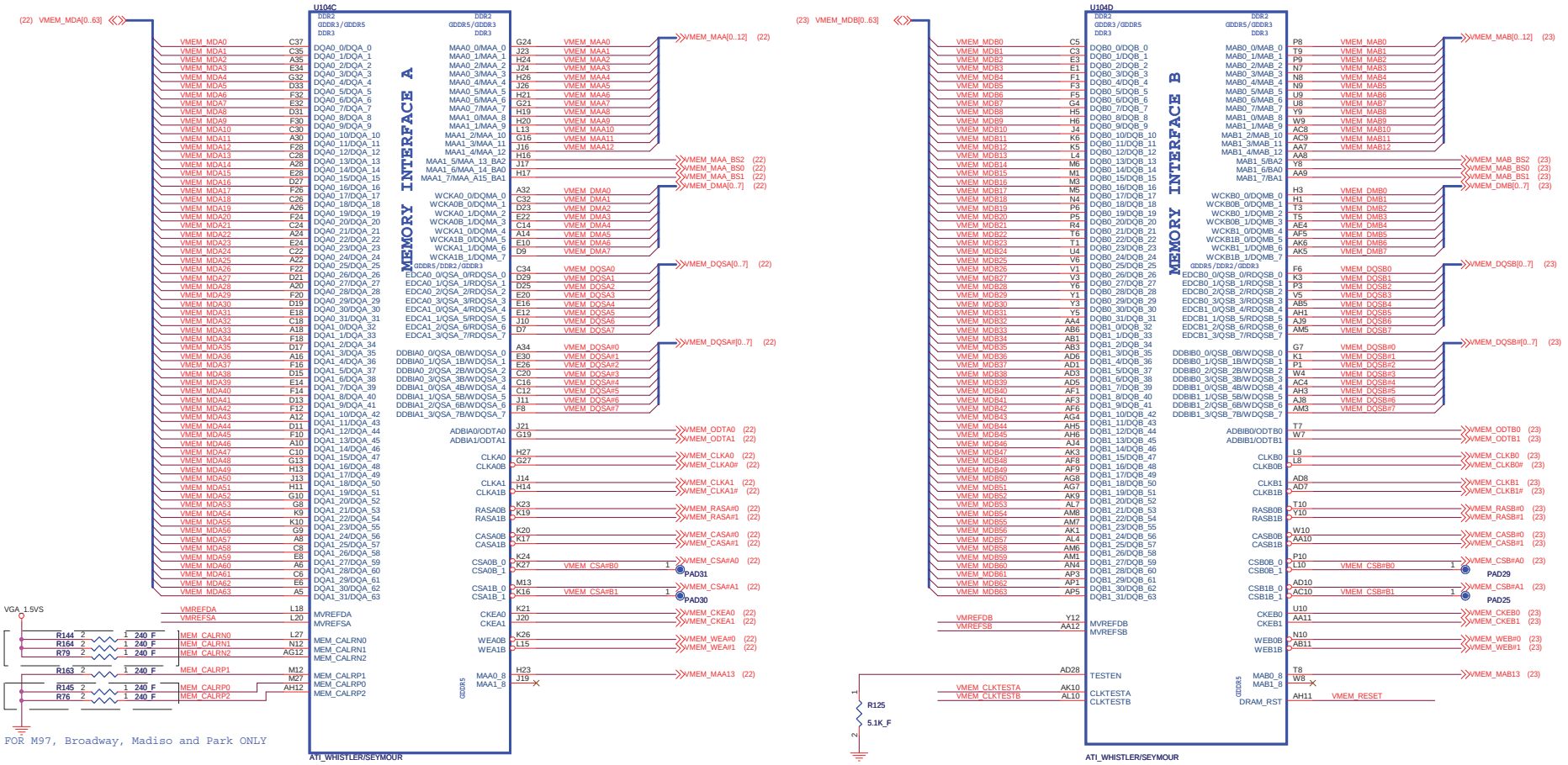
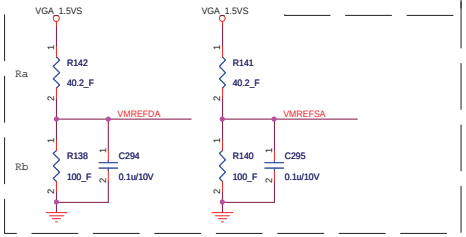
DGPU VRAM I/F



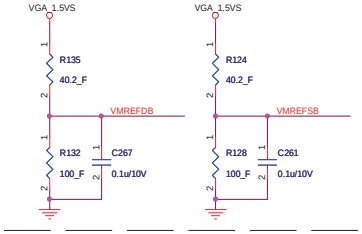
DIVIDER RESISTORS	DDR3/ GDDR3
MVREF TO 1.5V (Ra)	40.2R
MVREF TO GND (Rb)	100R

Place colse to Pin
For DDR3: 0.7 * VDDR1

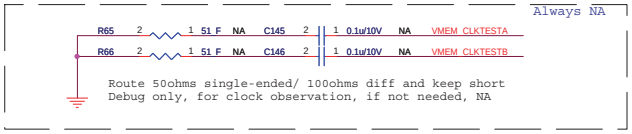
Seymour: NA
Whistler: Mounte

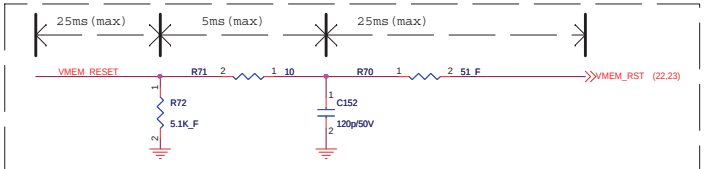


Place colse to Pin
For DDR3: 0.7 * VDDR1



Always NA





Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

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Project Name : H510UA1	Title : DGPU - VRAM I/F	
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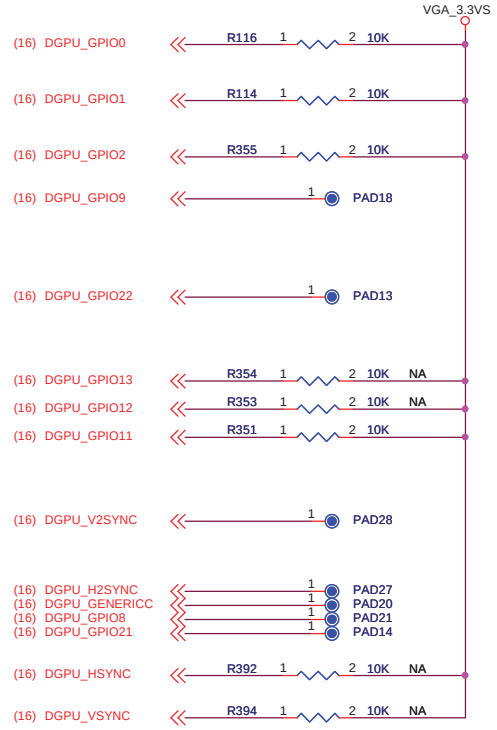
DGPU STRAP

CONFIGURATION STRAPS

STRAPS	PIN	DESCRIPTION	ASIC Deault	Status
TX_PWRS_ENB	GPIO0	Transmitter (Tx) power savings enable 0: 50% Tx output swing (DEFAULT) 1: Full Tx output swing	All Internal Pull Down	Mounted
TX_DEEMPH	GPIO1	PCI Express transmitter deemphasis enable. 0: Tx de-emphasis disabled (DEFAULT) 1: Tx de-emphasis enabled		Mounted
RESERVED	GPIO2	0 : PCIe device as 2.5 GT/s capable (DEFAULT) 1 : PCIe device as 5.0 GT/s capable		Mounted
VGA_DIS	GPIO9	VGA disable determines whether or not the card will be recognized as the system's VGA controller (via the SUBCLASS field in the PCI configuration space): 0 : VGA Controller capacity enabled (DEFAULT) 1 : The device will not be recognized as the system's VGA controller		NA
BIOS_ROM_EN	GPIO_22_ROMCSB	0 - Disable external BIOS ROM device (DEFAULT) 1 - Enable external BIOS ROM device		NA
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13 GPIO12 GPIO11	BIOS_ROM_EN = 1, Config[2:0] defines the ROM type. BIOS_ROM_EN = 0, Config[2:0] defines the primary memory aperture size. Size of the primary memory apertures CONFIG[2:0] 128 MB 000 256 MB 001 64MB 010 32MB 011		NA NA Mounted
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS L: Ignore VIP Device Strap (DEFAULT) H: Enable VIP Device Strap		NA
RSVD RSVD RSVD RSVD	H2SYNC GENERICC GPIO8 GPIO21_BB_EN			NA NA NA NA
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI		NA NA



Signal	Seymour/Whistler	Robson/ Park/ Medison/ Capilano/ Broadway
Ball AJ21 on M2 Ball AG13 on S3	SWAPLOCKA SwaplockA/ B signals can be optionally used on a multi-GPU design with multiple display outputs to allow all displays in a group (group A or group B) to update at the same time and have synchronous left/ right stereo timing. Genlock of the GPUs is also needed, either via a genlock system, or by feeding all GPUs with the same reference clock. Also connecting SwaplockB is preferred, but not required. SwaplockA/ B are open drain, 3.3V signals. If this feature is not required, these signals can be used as 3.3V GPIOs or left unconnected on the PCB.	Ball AJ21 is NC on M2 packages Ball AG13 is R2SET on S3 package
Ball AK21 on M2 Ball H12 on S3	SWAPLOCKB - see above On a multi-gpu design,SwaplockB from all GPUs are connected together with an external pull-up resistor (10K Ohms). If this feature is not required, these signals can be used as 3.3V GPIOs or left unconnected on the PCB.	Ball AK21 is NC on M2 packages Ball AH12 is DAC2 Output - on S3 package

Signal	Seymour/Whistler	Robson/ Park/ Medison/ Capilano/ Broadway
Ball AC32 on M2	NC	DAC2 Output-C on M2 package
Ball AA29 on M2	NC	R2SET on M2 package
Ball AD32 on M2	NC	DAC2 Output- Y
Ball AG33 on M2	NC	A2VDD
Ball AD33 on M2	NC	A2VDDQ
Ball AF33 on M2	TSVSSQ	A2VSSQ
Ball AG33, AG32 on M2	NC	VDD2DI/VSS2DI
H2SYNC	GENLK_CLK (3.3V): Reference clock input (3.3V) for pixel PLL received from frame-lock/ gen-lock interface	H2SYNC
V2SYNC	GENLK_VSYNC (3.3V): Frame timing indicator.Output to frame-lock/genlock interface	V2SYNC

FLEX Computing

Project Name : H510UA1	Title : DGPU - Strap	
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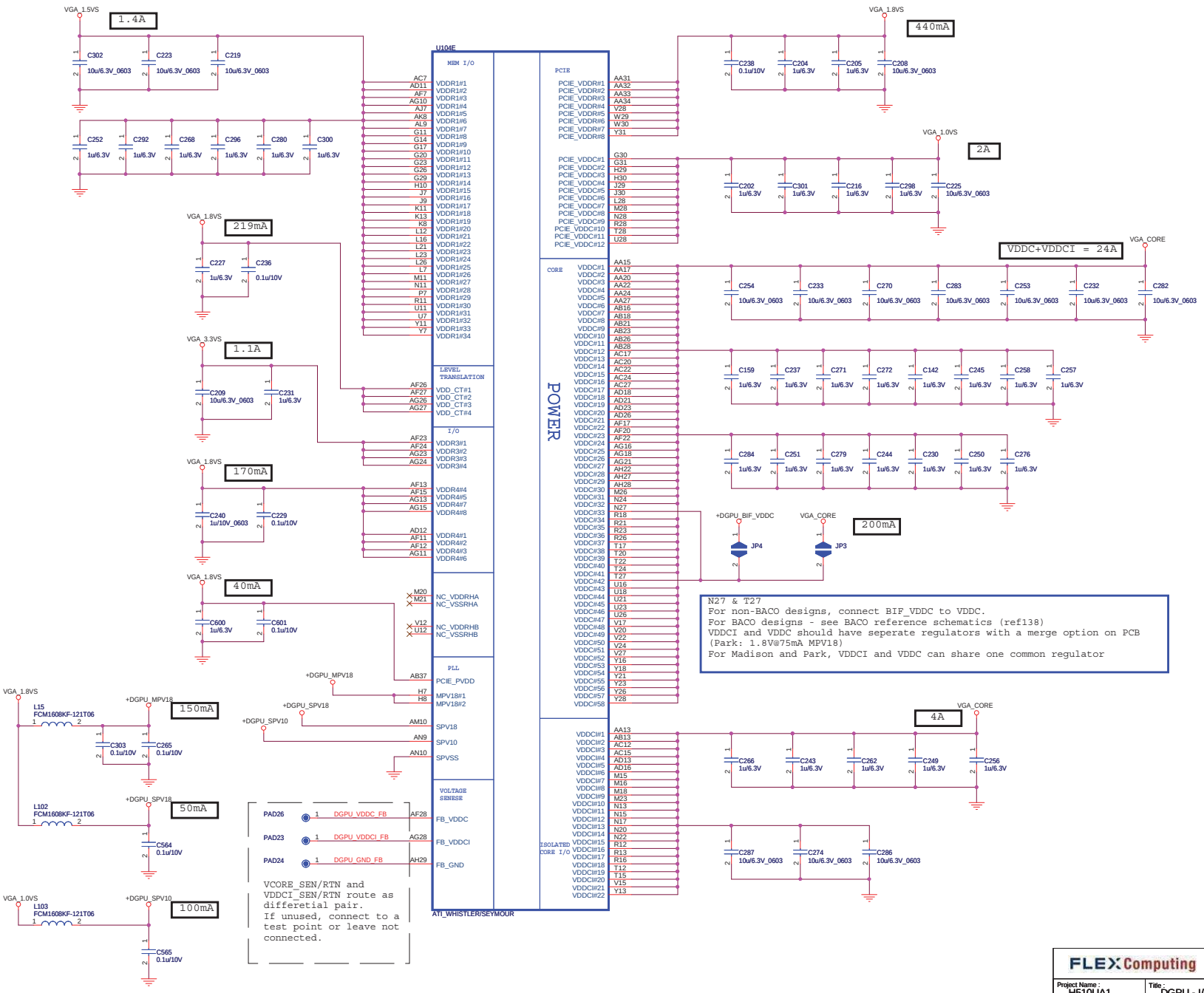
DGPU IO PWR/ GND



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FLEXComputing			
Project Name : H510UA1		Title : DGPU - I/O PWR	
Size :	Document Number : HPMH-40GAB6300-D		Rev : D
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DGPU DP PWR/ GND

U104F

PCIE_VSS#1 AB39
PCIE_VSS#2 E39
PCIE_VSS#3 F34
PCIE_VSS#4 F39
PCIE_VSS#5 G33
PCIE_VSS#6 G34
PCIE_VSS#7 H31
PCIE_VSS#8 H34
PCIE_VSS#9 H39
PCIE_VSS#10 J31
PCIE_VSS#11 J34
PCIE_VSS#12 K31
PCIE_VSS#13 K34
PCIE_VSS#14 K39
PCIE_VSS#15 L31
PCIE_VSS#16 L34
PCIE_VSS#17 M34
PCIE_VSS#18 M39
PCIE_VSS#19 N31
PCIE_VSS#20 N34
PCIE_VSS#21 P31
PCIE_VSS#22 P34
PCIE_VSS#23 P39
PCIE_VSS#24 R34
PCIE_VSS#25 T31
PCIE_VSS#26 T34
PCIE_VSS#27 T39
PCIE_VSS#28 U31
PCIE_VSS#29 U34
PCIE_VSS#30 V34
PCIE_VSS#31 V39
PCIE_VSS#32 W31
PCIE_VSS#33 W34
PCIE_VSS#34 Y34
PCIE_VSS#35 Y39

GND

GND#100 F15
GND#101 F17
GND#102 F19
GND#103 F21
GND#104 F23
GND#105 F25
GND#106 F27
GND#107 F29
GND#108 F31
GND#109 F33
GND#110 F7
GND#111 F9
GND#112 G2
GND#113 G6
GND#114 H9
GND#115 J2
GND#116 J27
GND#117 J6
GND#118 J8
GND#119 K14
GND#120 K7
GND#121 L11
GND#122 L17
GND#123 L2
GND#124 L22
GND#125 L24
GND#126 L6
GND#127 M17
GND#128 M22
GND#129 M24
GND#130 N16
GND#131 N18
GND#132 N2
GND#133 N21
GND#134 N23
GND#135 N26
GND#136 N6
GND#137 R15
GND#138 R17
GND#139 R2
GND#140 R20
GND#141 R22
GND#142 R24
GND#143 R27
GND#144 R6
GND#145 T11
GND#146 T13
GND#147 T16
GND#148 T18
GND#149 T21
GND#150 T23
GND#151 T26
GND#152 U15
GND#153 U17
GND#154 U2
GND#155 U20
GND#156 U22
GND#157 U24
GND#158 U27
GND#159 U6
GND#160 V11
GND#161 V16
GND#162 V18
GND#163 V21
GND#164 V23
GND#165 V26
GND#166 W2
GND#167 W6
GND#168 Y15
GND#169 Y17
GND#170 Y20
GND#171 Y22
GND#172 Y24
GND#173 Y27
GND#174 U13
GND#175 V13

GND#1 A3
GND#2 A37
GND#3 AA16
GND#4 AA18
GND#5 AA2
GND#6 AA21
GND#7 AA23
GND#8 AA26
GND#9 AA28
GND#10 AA6
GND#11 AB12
GND#12 AB15
GND#13 AB17
GND#14 AB20
GND#15 AB22
GND#16 AB24
GND#17 AB27
GND#18 AC11
GND#19 AC13
GND#20 AC16
GND#21 AC18
GND#22 AC2
GND#23 AC21
GND#24 AC23
GND#25 AC26
GND#26 AC28
GND#27 AC6
GND#28 AD15
GND#29 AD17
GND#30 AD20
GND#31 AD22
GND#32 AD24
GND#33 AD27
GND#34 AD9
GND#35 AE2
GND#36 AE6
GND#37 AF10
GND#38 AF16
GND#39 AF18
GND#40 AF21
GND#41 AG17
GND#42 AG2
GND#43 AG20
GND#44 AG22
GND#45 AG6
GND#46 AG9
GND#47 AH21
GND#48 AJ10
GND#49 AJ11
GND#50 AJ2
GND#51 AJ28
GND#52 AJ6
GND#53 AK11
GND#54 AK31
GND#55 AK7
GND#56 AL11
GND#57 AL14
GND#58 AL17
GND#59 AL2
GND#60 AL20
PX_EN/GND#61 AL21
GND#62 AL23
GND#63 AL26
GND#64 AL32
GND#65 AL6
GND#66 AL8
GND#67 AM11
GND#68 AM31
GND#69 AM9
GND#70 AN11
GND#71 AN2
GND#72 AN30
GND#73 AN6
GND#74 AN8
GND#75 AP11
GND#76 AP7
GND#77 AP9
GND#78 AR5
GND#79 B11
GND#80 B13
GND#81 B15
GND#82 B17
GND#83 B19
GND#84 B21
GND#85 B23
GND#86 B25
GND#87 B27
GND#88 B29
GND#89 B31
GND#90 B33
GND#91 B7
GND#92 B9
GND#93 C1
GND#94 C39
GND#95 E35
GND#96 E5
GND#97 F11
GND#98 F13

VSS_MECH#1 A39
VSS_MECH#2 AW1
VSS_MECH#3 AW39

ATI_WHISTLER/SEYMOUR

BACO design options as Apps Note
Seymour/ Whistler/ Robson supported
Park/ Madison/ Capilano/ Broadway not Applicable

For PX_EN, refer to the BACO reference schematics for detail.
PX_EN is used to control discrete GPU regulators for
PowerXpress (Switchable graphics) BACO mode.
A pull-down resistor is required. Leave signal unconnected if not used.

DGPU_PX_EN (21)
R119
5.1K_F

U104H

DP C/D POWER
DP A/B POWER
DP E/F POWER
DP PLL POWER

VGA_1.8VS
VGA_1.0VS

DPC_VDD18#1 AP20
DPC_VDD18#2 AP21
DPC_VDD10#1 AP13
DPC_VDD10#2 AT13
DPC_VSSR#1 AN17
DPC_VSSR#2 AP16
DPC_VSSR#3 AP17
DPC_VSSR#4 AW14
DPC_VSSR#5 AW16
DPD_VDD18#1 AP22
DPD_VDD18#2 AP23
DPD_VDD10#1 AP14
DPD_VDD10#2 AP15
DPD_VSSR#1 AN19
DPD_VSSR#2 AP18
DPD_VSSR#3 AP19
DPD_VSSR#4 AW20
DPD_VSSR#5 AW22
DPCD_CALR AW18
DGPU_DPCD_CALR

DPA_VDD18#1 AN24
DPA_VDD18#2 AP24
DPA_VDD10#1 AP31
DPA_VDD10#2 AP32
DPA_VSSR#1 AN27
DPA_VSSR#2 AP27
DPA_VSSR#3 AP28
DPA_VSSR#4 AW24
DPA_VSSR#5 AW26
DPB_VDD18#1 AP25
DPB_VDD18#2 AP26
DPB_VDD10#1 AN33
DPB_VDD10#2 AP33
DPB_VSSR#1 AN29
DPB_VSSR#2 AP29
DPB_VSSR#3 AP30
DPB_VSSR#4 AW30
DPB_VSSR#5 AW32
DPAB_CALR AW28
DGPU_DPAB_CALR

DPE_VDD18#1 AH34
DPE_VDD18#2 AJ34
DPE_VDD10#1 AL33
DPE_VDD10#2 AM33
DPE_VSSR#1 AN34
DPE_VSSR#2 AP39
DPE_VSSR#3 AR39
DPE_VSSR#4 AU37
DPF_VDD18#1 AF34
DPF_VDD18#2 AG34
DPF_VDD10#1 AK33
DPF_VDD10#2 AK34
DPF_VSSR#1 AF39
DPF_VSSR#2 AH39
DPF_VSSR#3 AK39
DPF_VSSR#4 AL34
DPF_VSSR#5 AM34
DPEF_CALR AM39
DGPU_DPEF_CALR

DPA_PVDD AU28
DPA_PVSS AV27
DPB_PVDD AV29
DPB_PVSS AR28
DPC_PVDD AU18
DPC_PVSS AV17
DPD_PVDD AV19
DPD_PVSS AR18
DPE_PVDD AM37
DPE_PVSS AN38
DPF_PVDD AL38
DPF_PVSS AM35

ATI_WHISTLER/SEYMOUR

R348 2 1 150_F DGPU_DPAB_CALR
R345 1 2 150_F DGPU_DPCD_CALR
R386 1 2 150_F DGPU_DPEF_CALR

Near by U104

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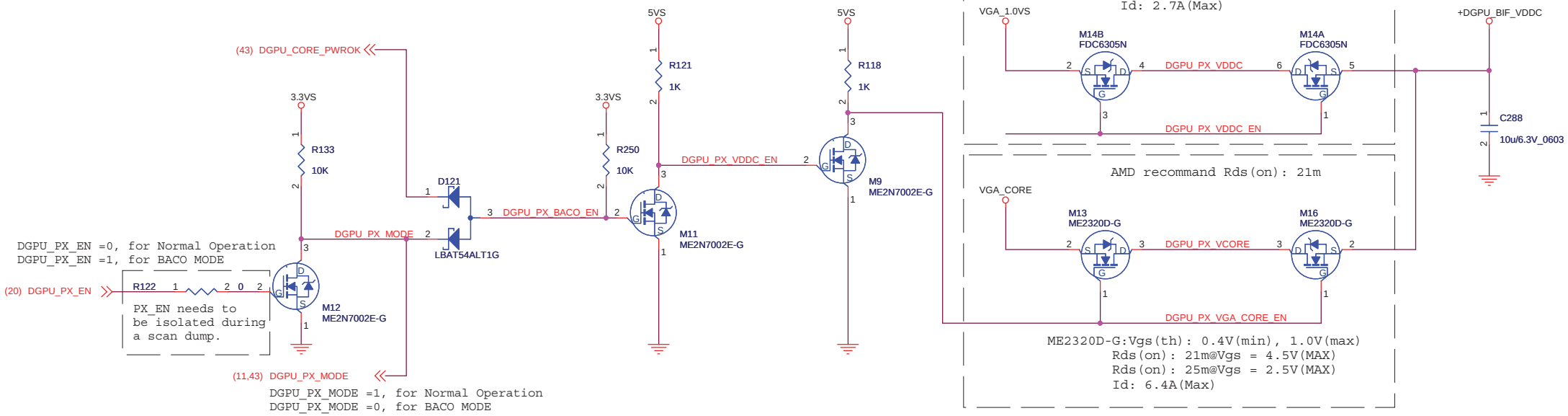
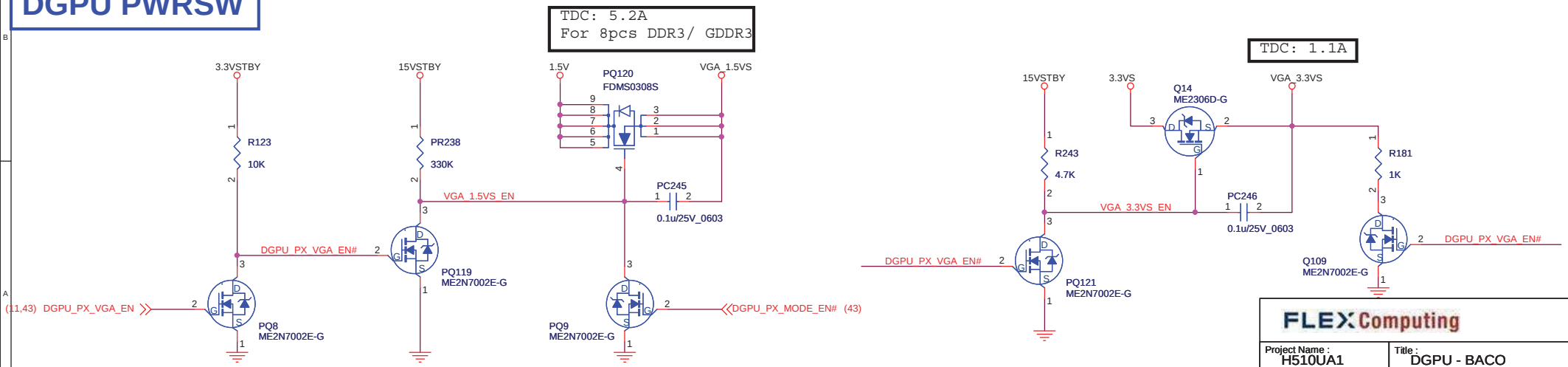
DGPU BACO



DGPU PWRSW



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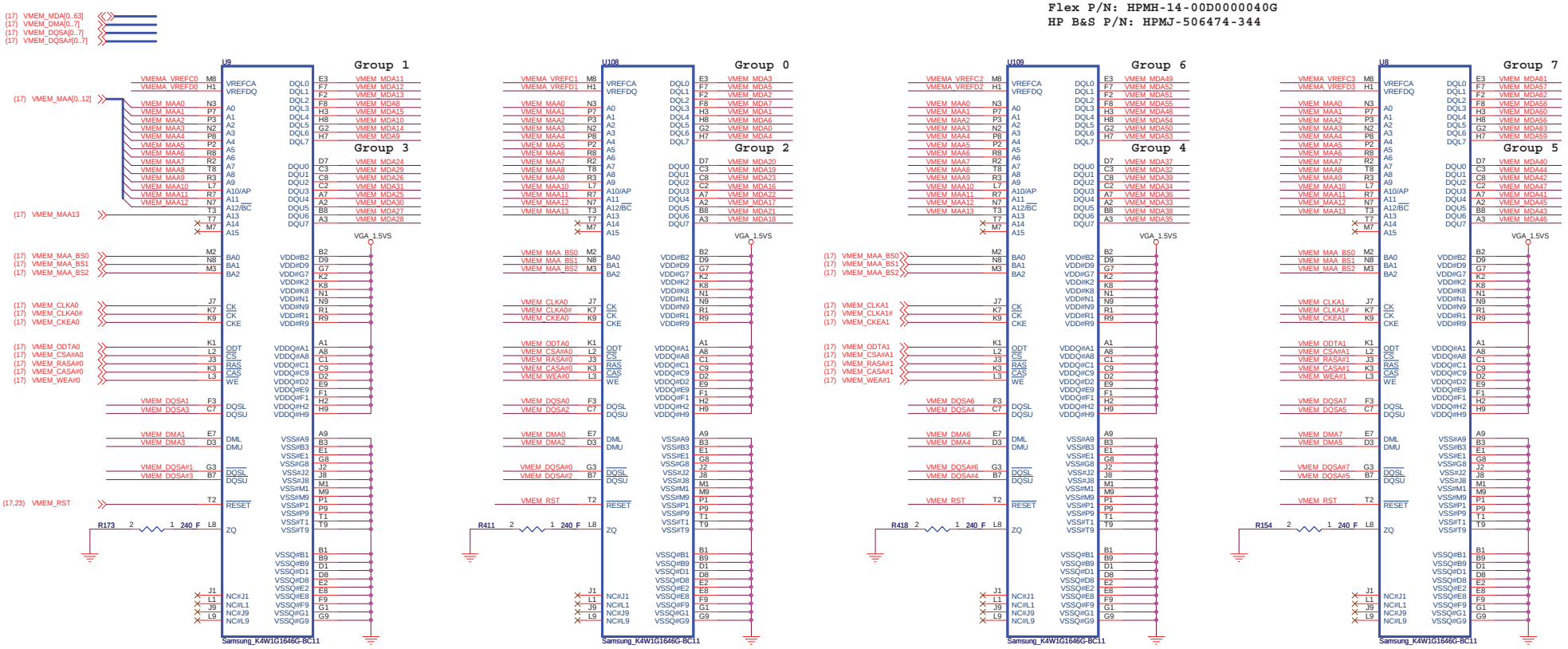
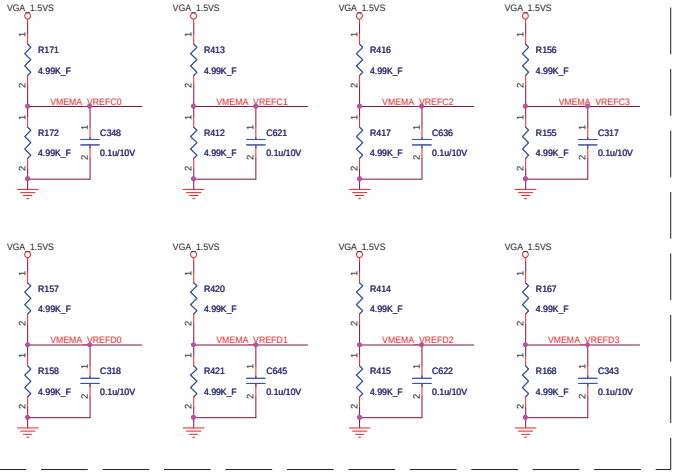
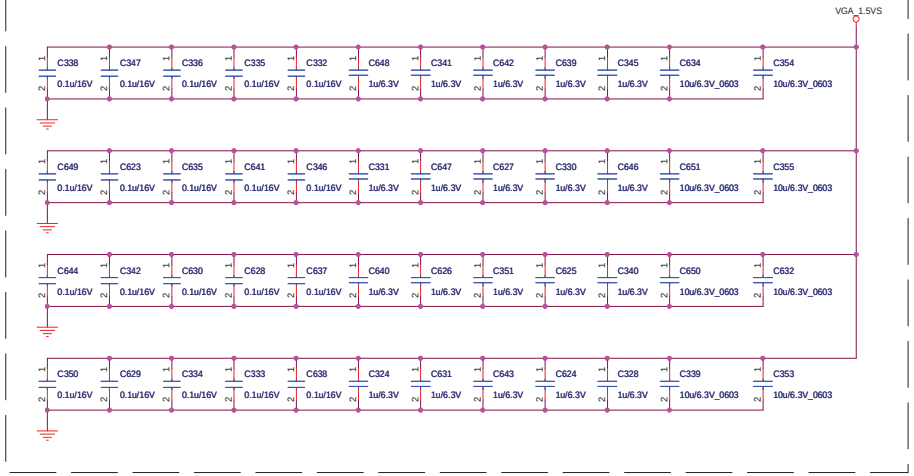
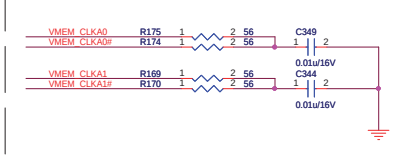
DGPU VRAM Channel - A

Samsung/ K4W1G1646G-BC11
Flex P/N: HPMH-14-00D0000042G
HP B&S P/N: HPMJ-506474-945
Hynix/ H5TQ1G63DFR-11C
Flex P/N: HPMH-14-00D0000040G
HP B&S P/N: HPMJ-506474-344









PCB Layout indicate

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FLEX Computing

Project Name : H510UA1	Title : DGPU - VRAM Channel - A	
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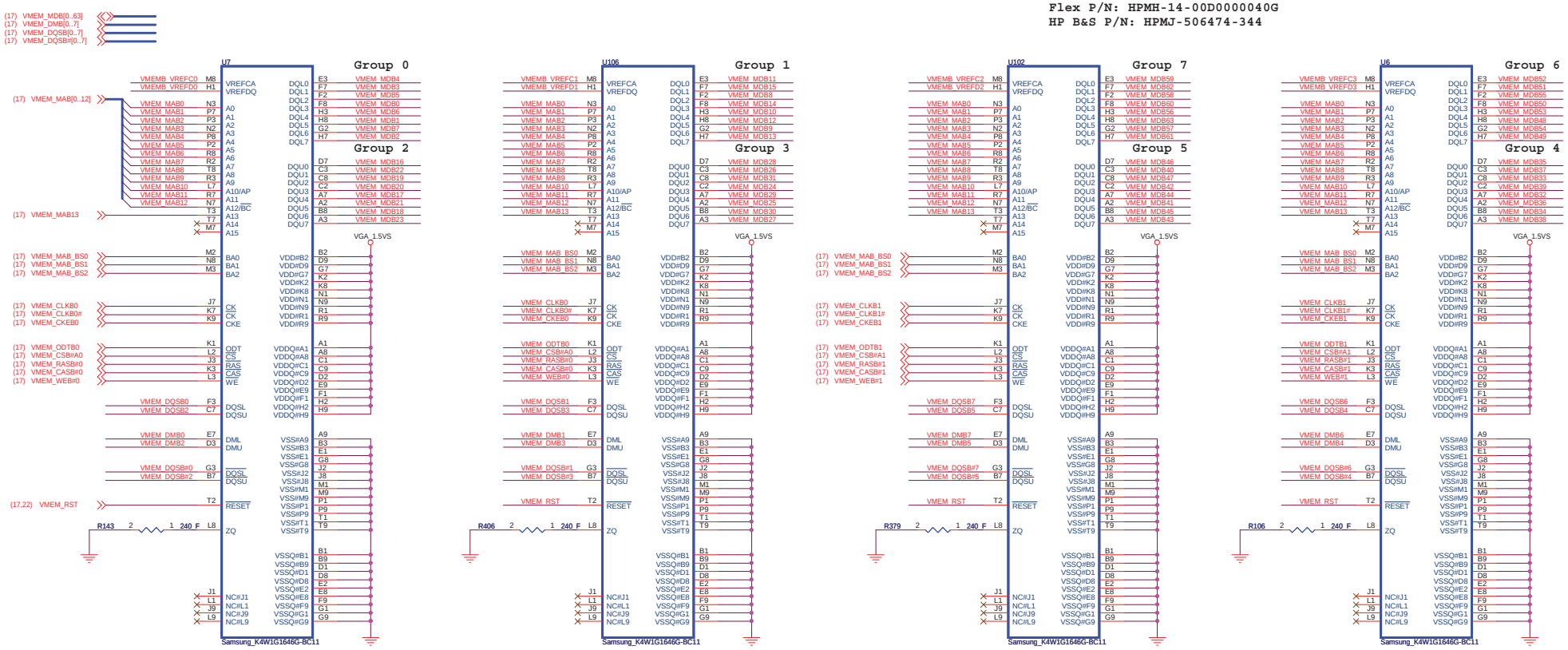
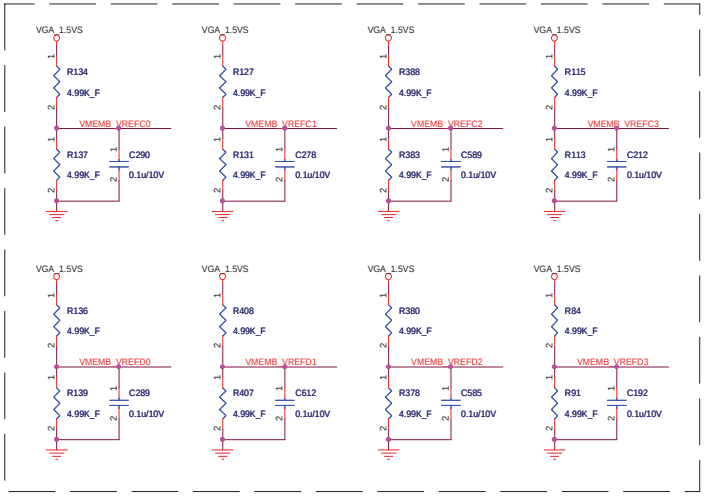
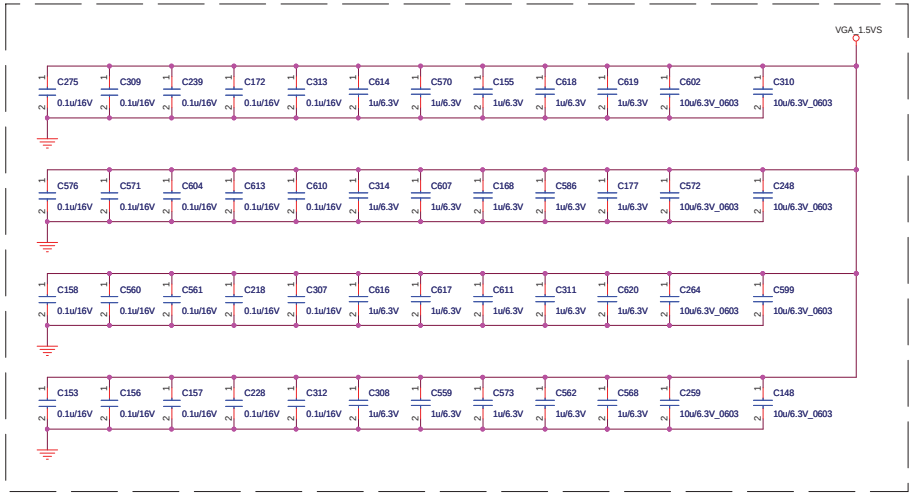
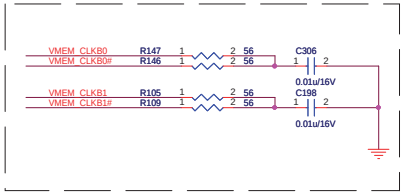
DGPU VRAM Channel - B

Samsung/ K4W1G1646G-BC11
Flex P/N: HPMH-14-00D0000042G
HP B&S P/N: HPMJ-506474-945
Hynix/ H5TQ1G63DFR-11C
Flex P/N: HPMH-14-00D0000040G
HP B&S P/N: HPMJ-506474-344

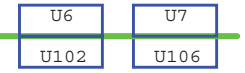








PCB Layout indicate



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FLEX Computing			
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Size :	Document Number : HPMH-40GAB6300-D		Rev : D
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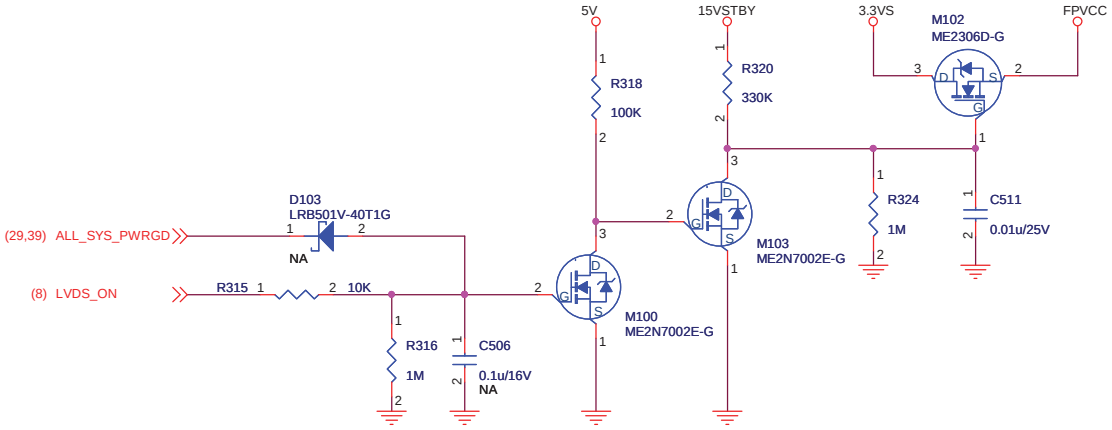
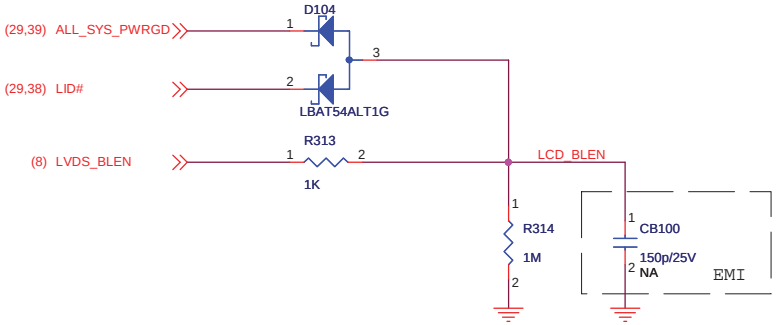
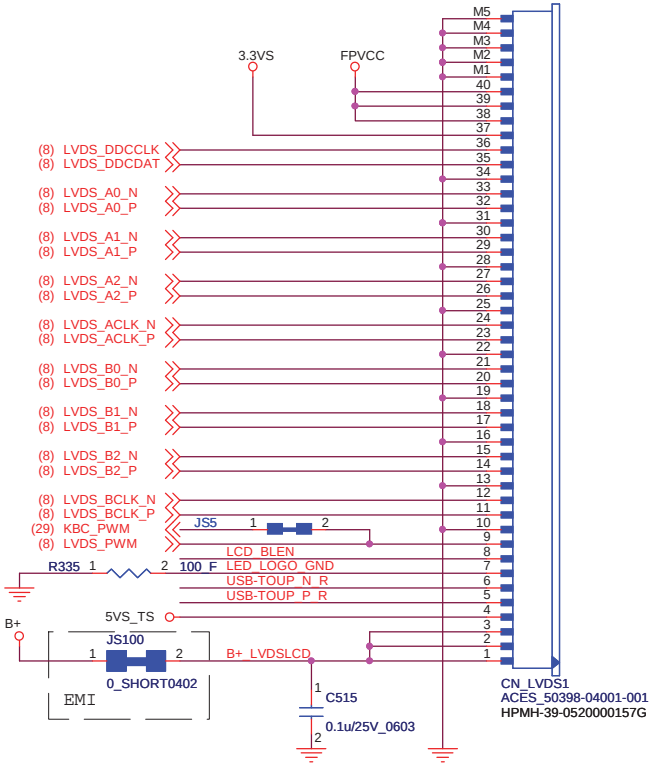
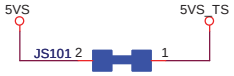
LVDS

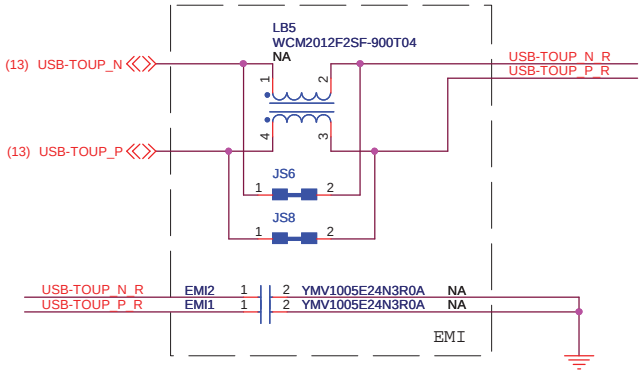


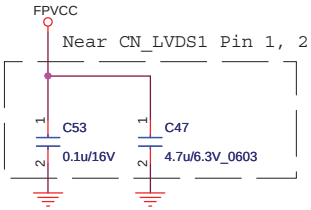


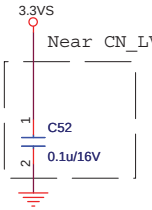


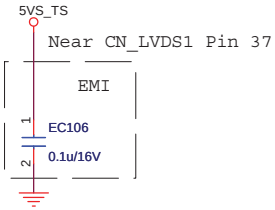
Touch Screen

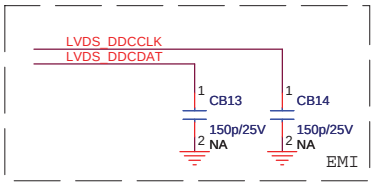








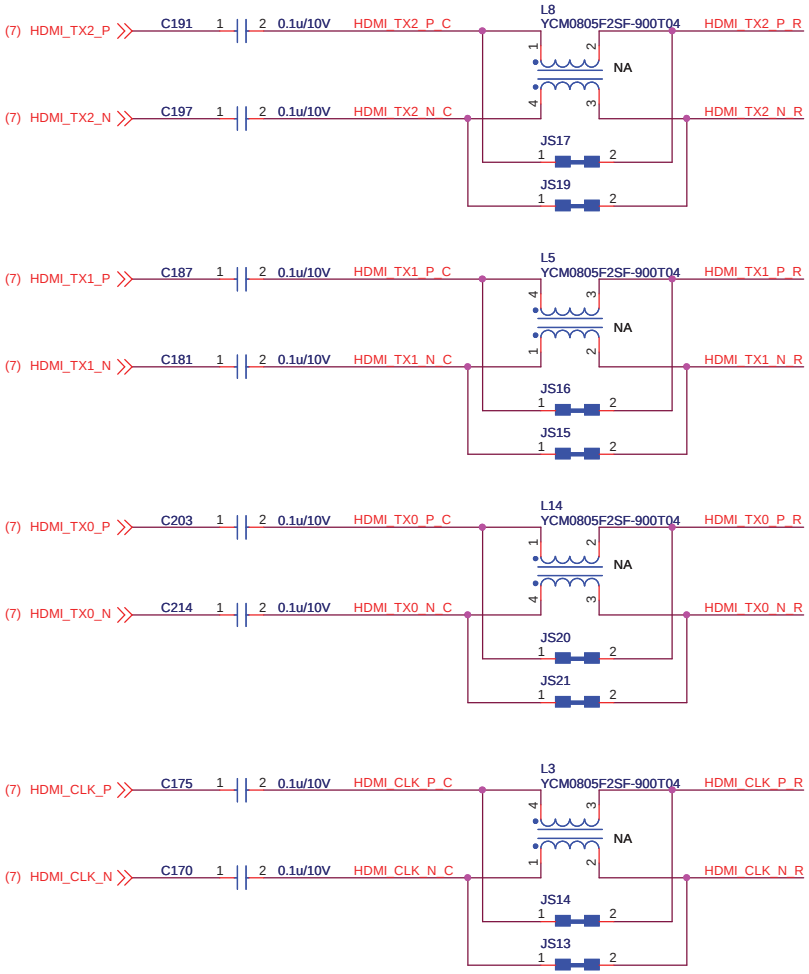


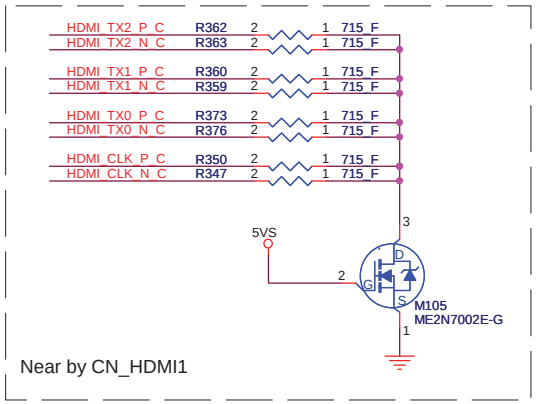


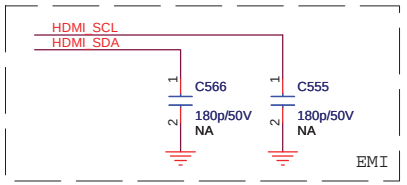
FLEXComputing

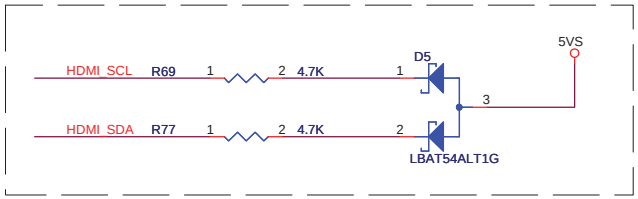
Project Name : H510UA1	Title : LVDS/ Touch Screen I/F
Size :	Document Number : HPMH-40GAB6300-D — Rev : D
Date: Thursday, December 30, 2010	Sheet : 24 of 51

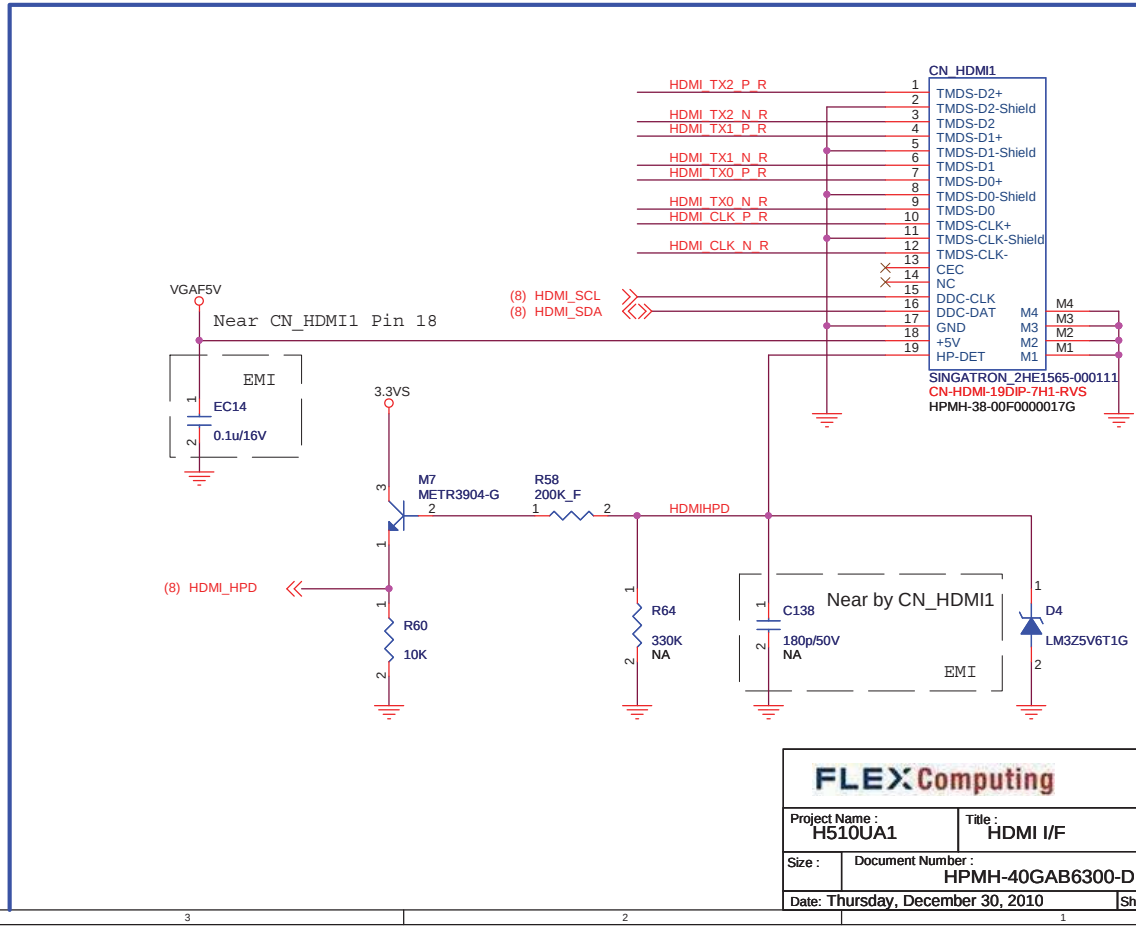
HDMI







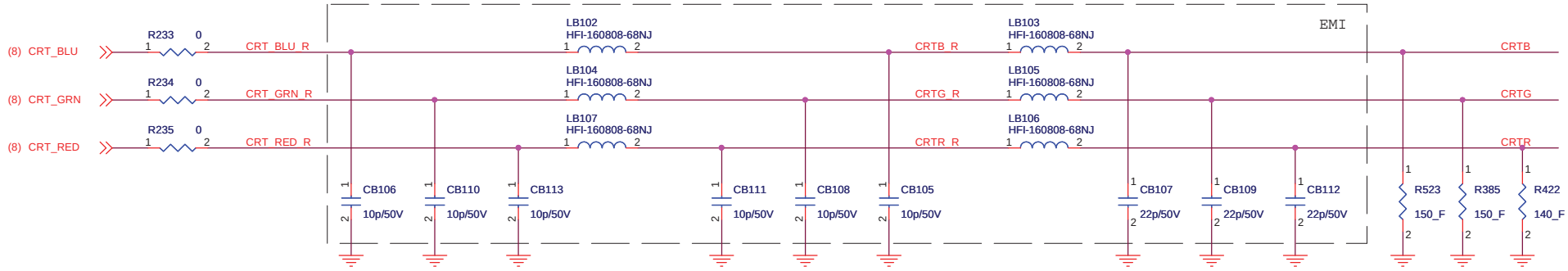


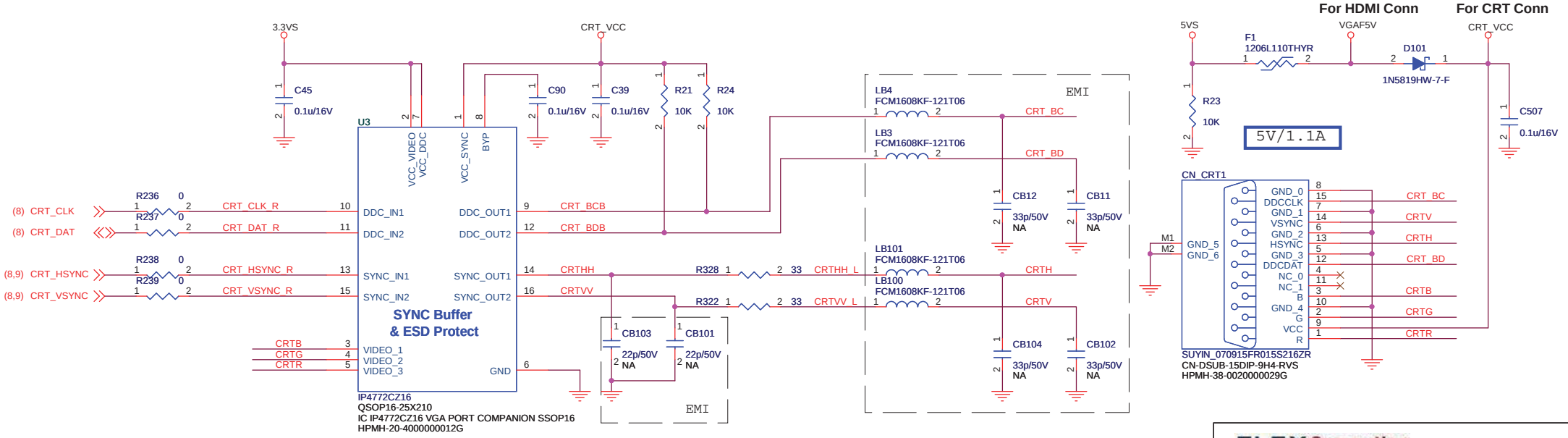


FLEXComputing

Project Name : H510UA1	Title : HDMI I/F	
Size :	Document Number : HPMH-40GAB6300-D	Rev : D
Date: Thursday, December 30, 2010	Sheet : 25 of 51	

CRT





FLEXComputing

Project Name : H510UA1	Title : D-sub I/F
Size :	Document Number : HPMH-40GAB6300-D / Rev : D
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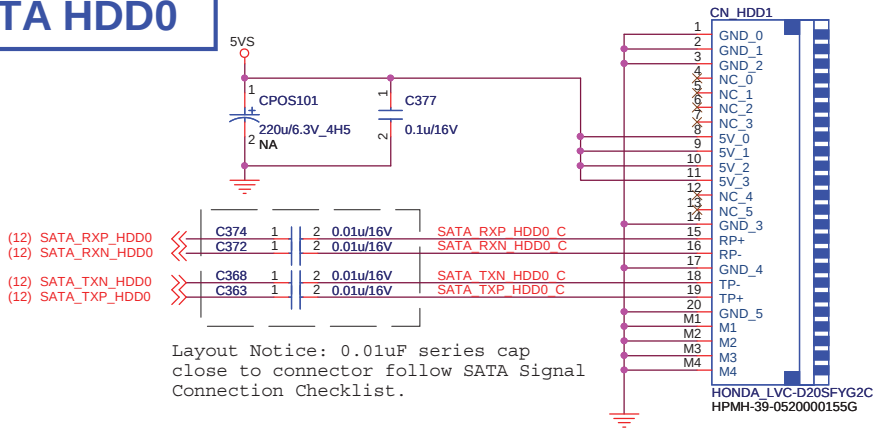
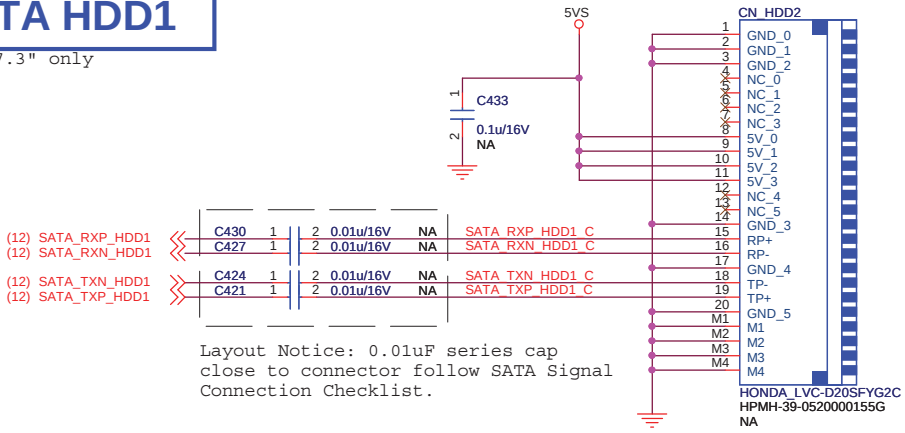
SATA HDD0



Layout Notice: 0.01uF series cap close to connector follow SATA Signal Connection Checklist.

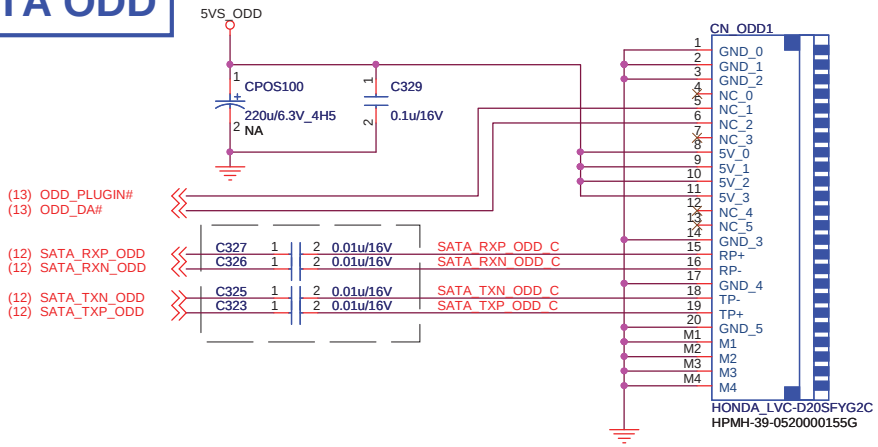
SATA HDD1

For 17.3" only

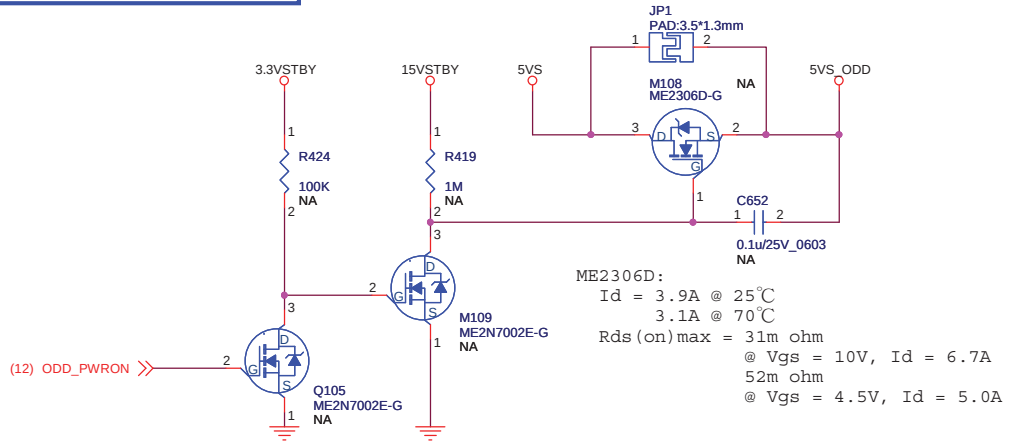


Layout Notice: 0.01uF series cap close to connector follow SATA Signal Connection Checklist.

SATA ODD

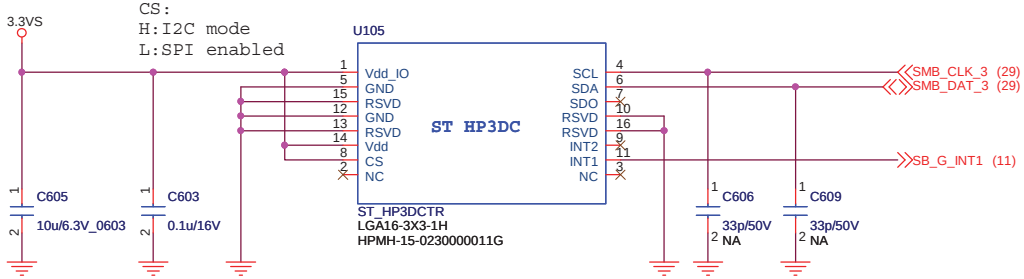


ODD Zero PWR



ME2306D:
Id = 3.9A @ 25℃
3.1A @ 70℃
Rds(on)max = 31m ohm
@ Vgs = 10V, Id = 6.7A
52m ohm
@ Vgs = 4.5V, Id = 5.0A

G-Sensor



G-SENSOR - ST HP3DC
3.3VS
ADDR: 0001100x(30h) - SDO PD
ADDR: 0011101x(32h) - SDO NC
SINK: ?mA@VoL=0.33V(MAX)

FLEXComputing

Project Name : H510UA1	Title : HDD/ ODD/ Zero PWR/ G-sensor
Size :	Document Number : HPMH-40GAB6300-D — Rev : D
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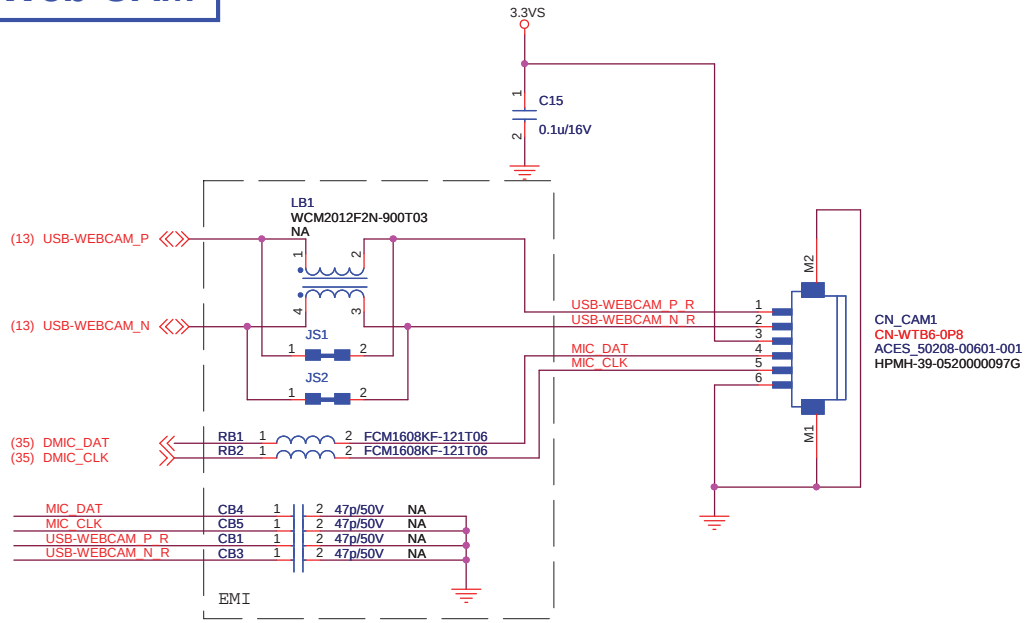
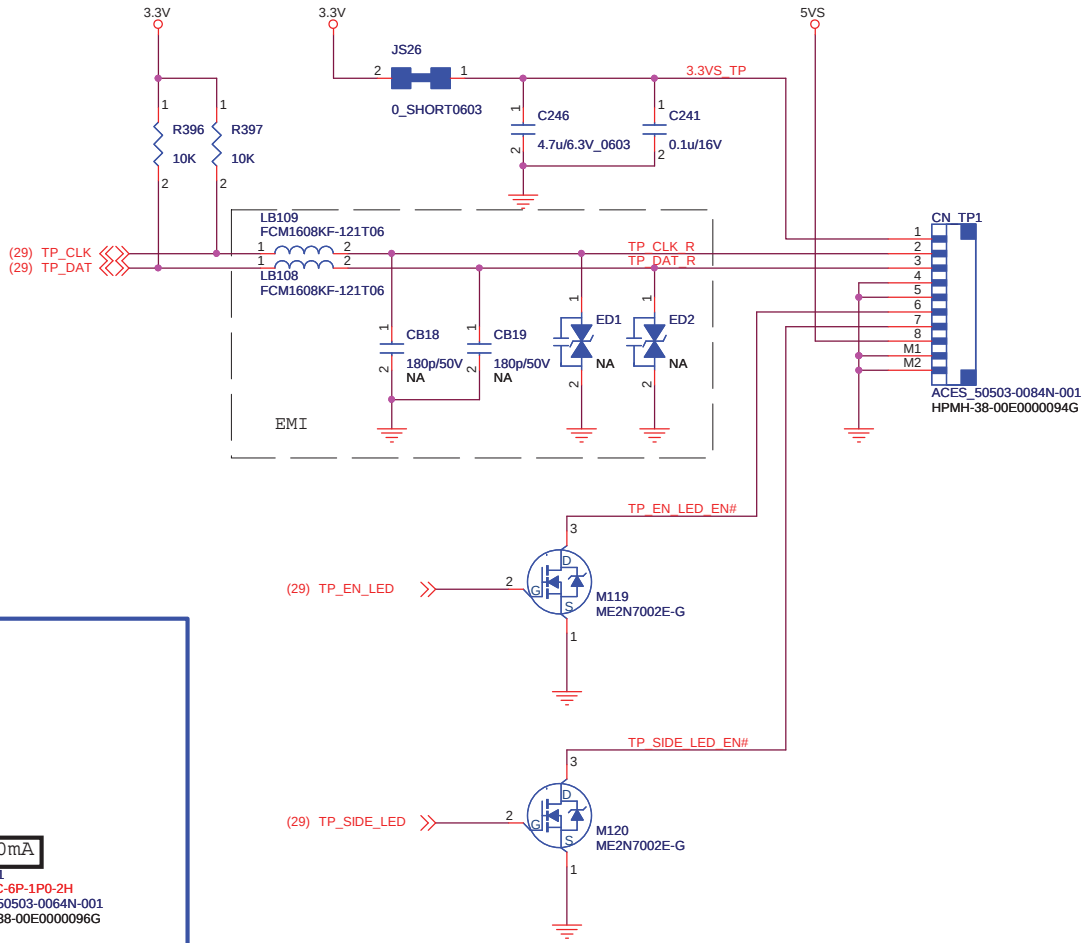
Web CAM

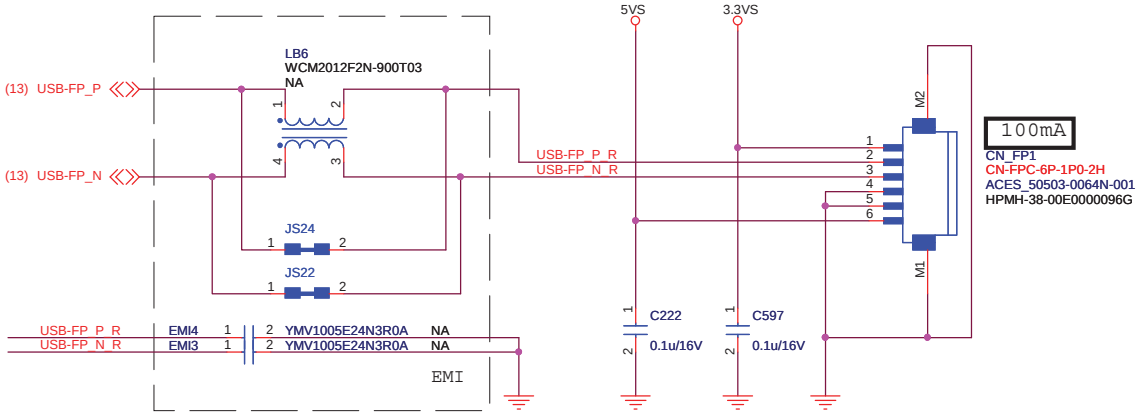


T/P



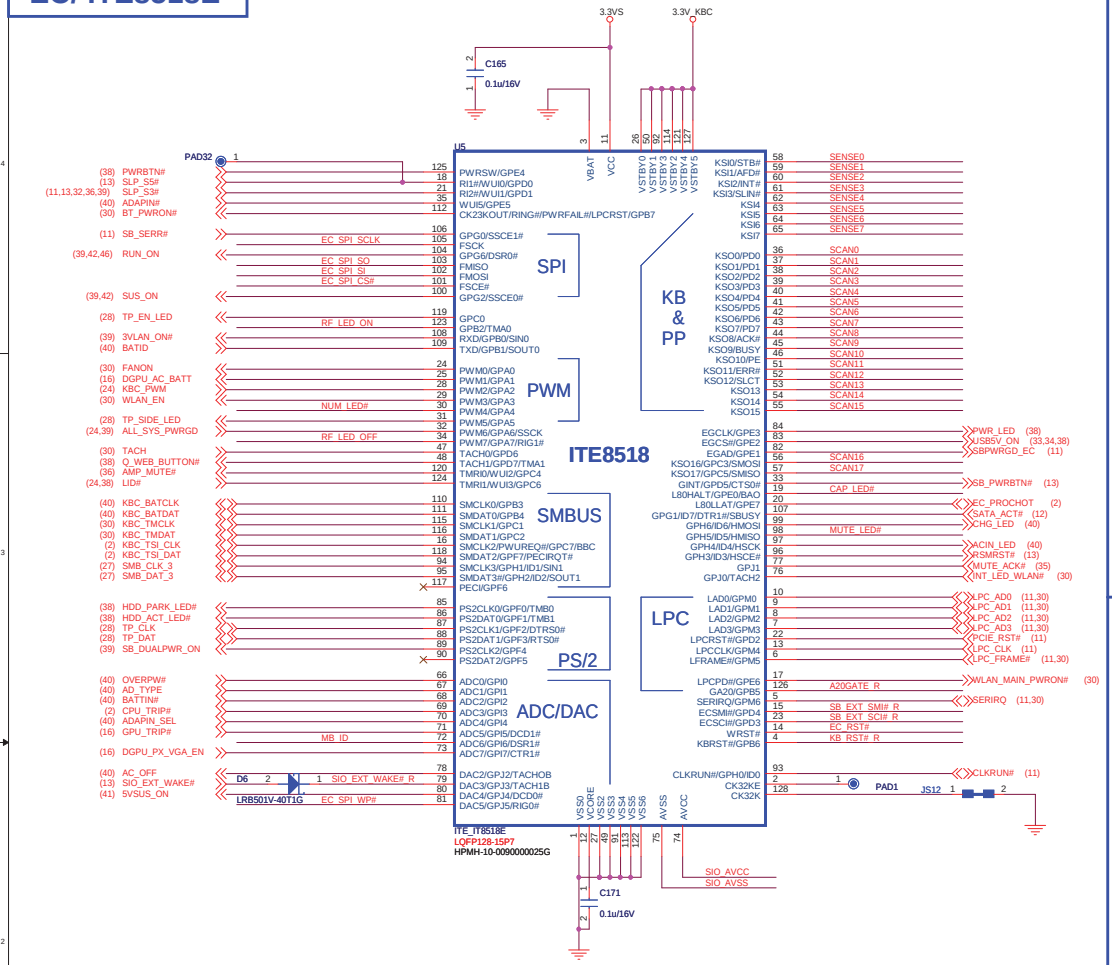
Finger Printer

Remve Finger Printer coponents for IMR

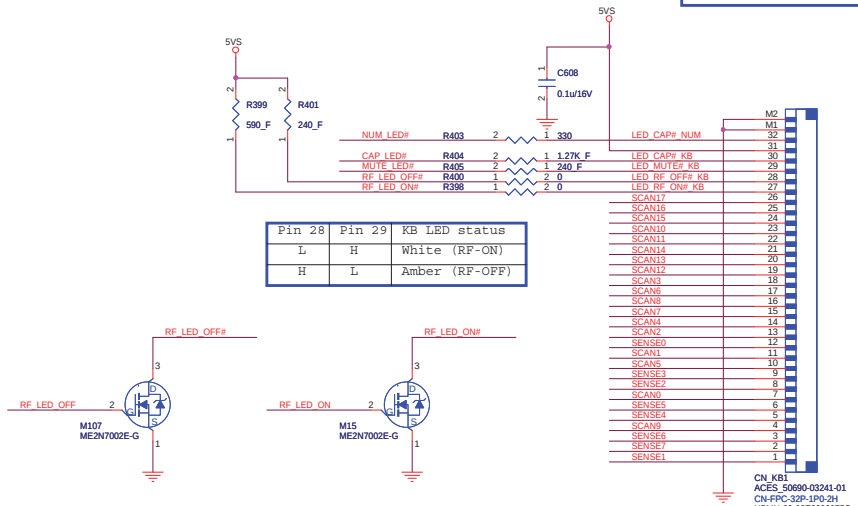


FLEXComputing		
Project Name : H510UA1	Title : WebCAM/ BT/ FPt/ Touch Screen	
Size :	Document Number : HPMH-40GAB6300-D	Rev : D
Date: Thursday, December 30, 2010	Sheet : 28 of 51	

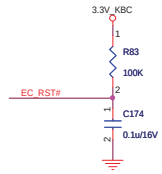
EC/ ITE8518E

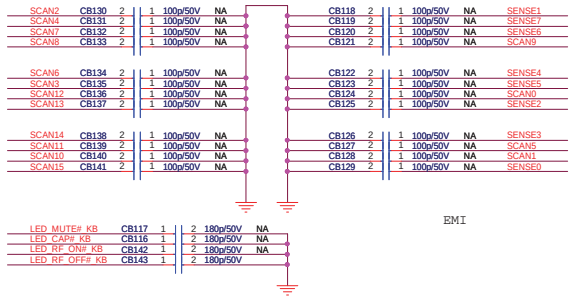


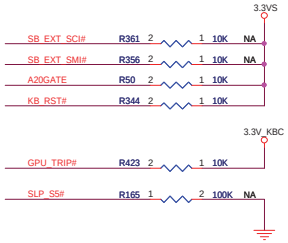
Keyboard Conn

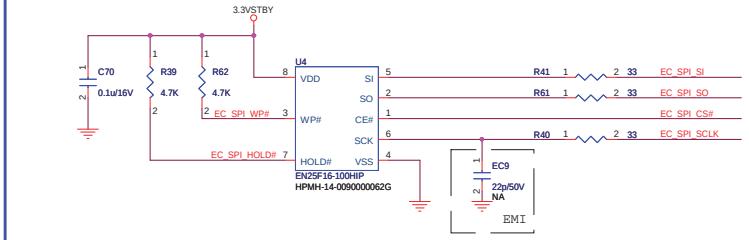


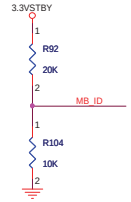
Pin 28	Pin 29	KB LED status
L	H	White (RF-ON)
H	L	Amber (RF-OFF)

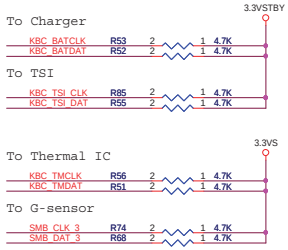


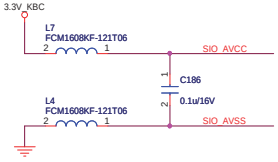


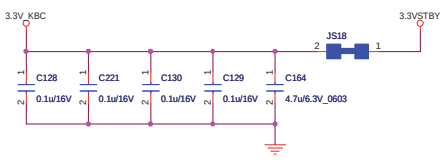


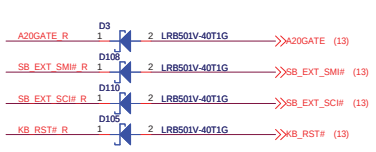












MB-ID		
3.3V	INTEL-DI	R92: 10K -- HPMH-30-301036-990G R104: NA
2.2V	INTEL-UI	R92: 10K -- HPMH-30-301036-990G R104: 20K -- HPMH-30-102036-990G
1.1V	AMD-DA	R92: 20K -- HPMH-30-102036-990G R104: 10K -- HPMH-30-301036-990G
GND	AMD-UA	R92: NA R104: 10K -- HPMH-30-301036-990G

FLEXComputing

Project Name : H510UA1	Title : EC/ ITE8518E
Size :	Document Number : HPMH-40GAB6300-D Rev : D
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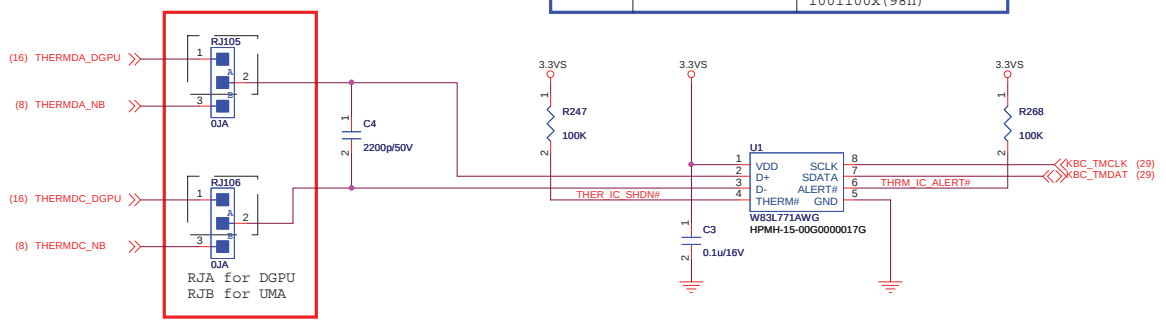
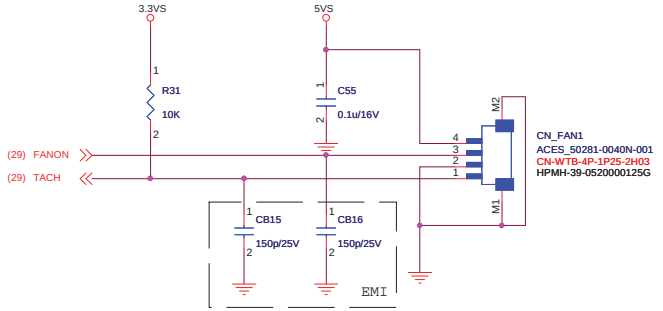
Thermal Sensor

THERMAL IC FOR CPU or DGPU

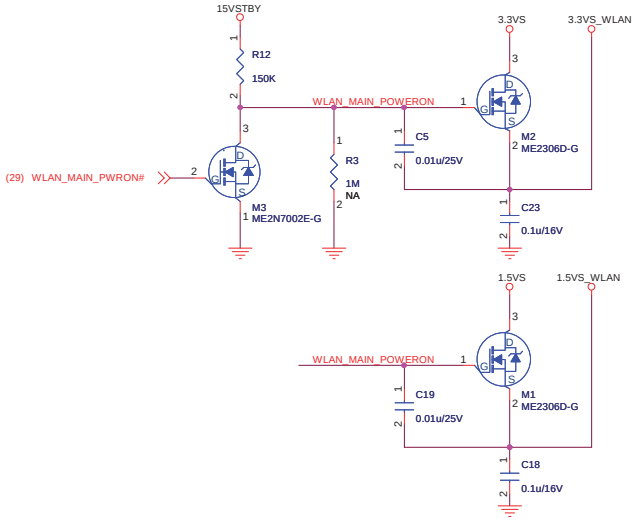
WINBOND	W83L771AWG	HPMH-15-00G0000017G 1001100x(98h)
TI	TMP431ADGKR	HPMH-15-0500000005G 1001100x(98h)

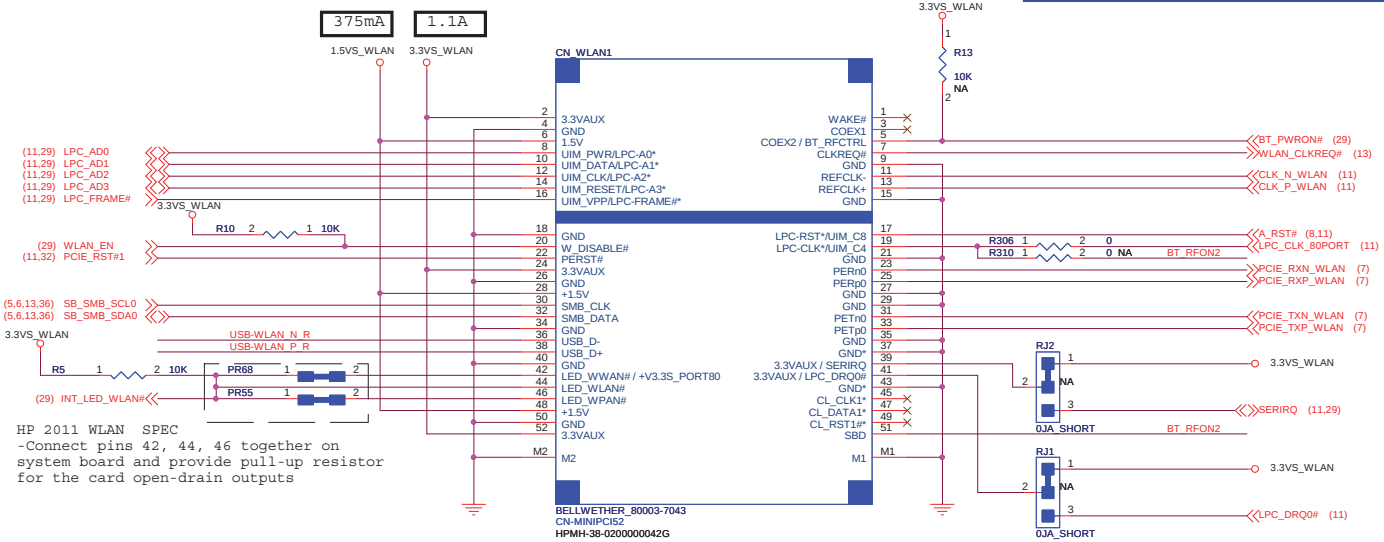


FAN

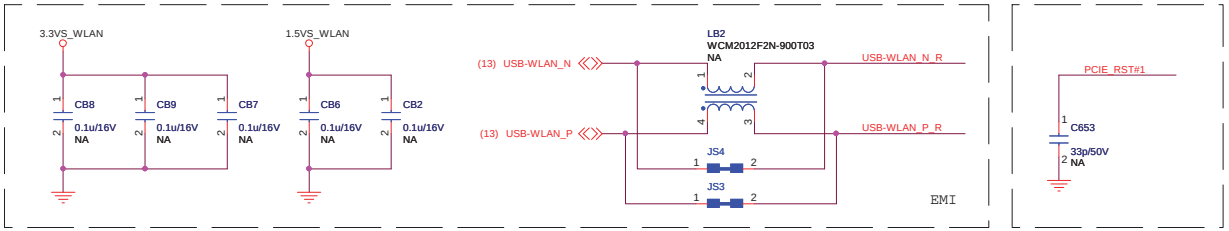


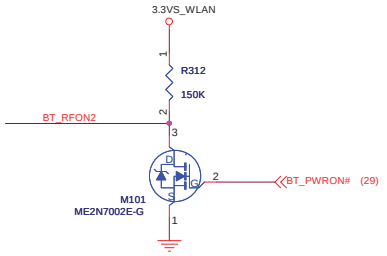
Mini PCI-E - WLAN (Half)





HP 2011 WLAN SPEC
-Connect pins 42, 44, 46 together on system board and provide pull-up resistor for the card open-drain outputs

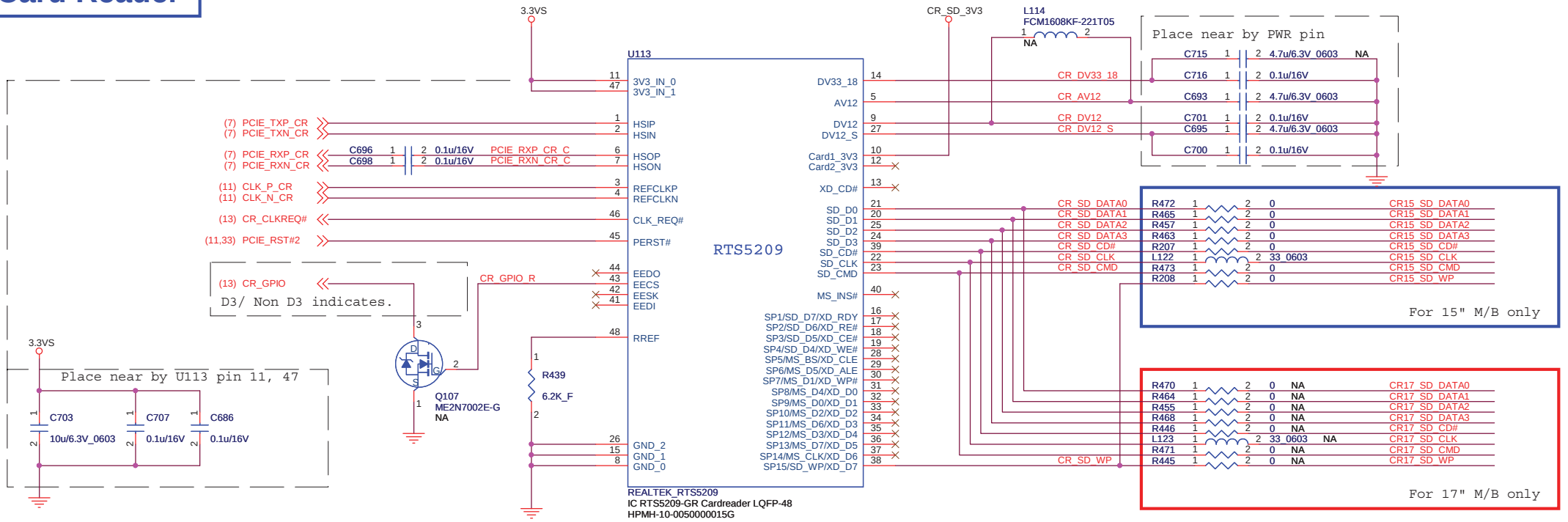




FLEX Computing

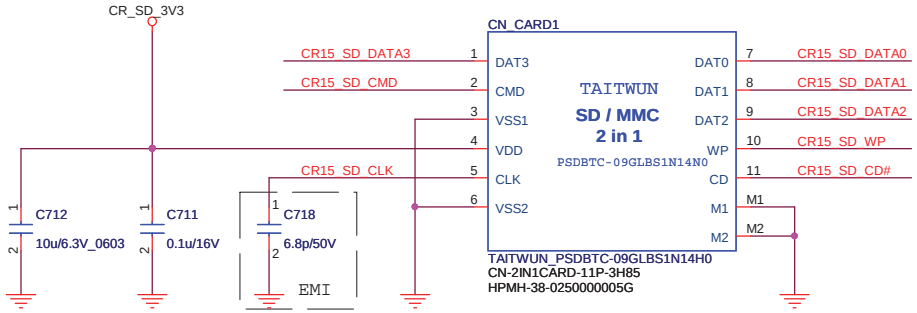
Project Name : H510UA1	Title : Thermal/ FAN/ WLAN/ HP-Logo
Size :	Document Number : HPMH-40GAB6300-D — Rev : D
Date: Tuesday, January 11, 2011	Sheet : 30 of 51

Card Reader



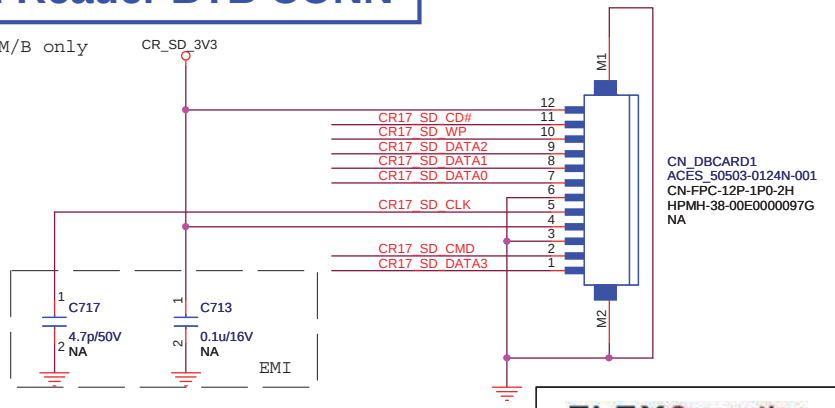
Card Reader CONN

For 15" M/B only



Card Reader BTB CONN

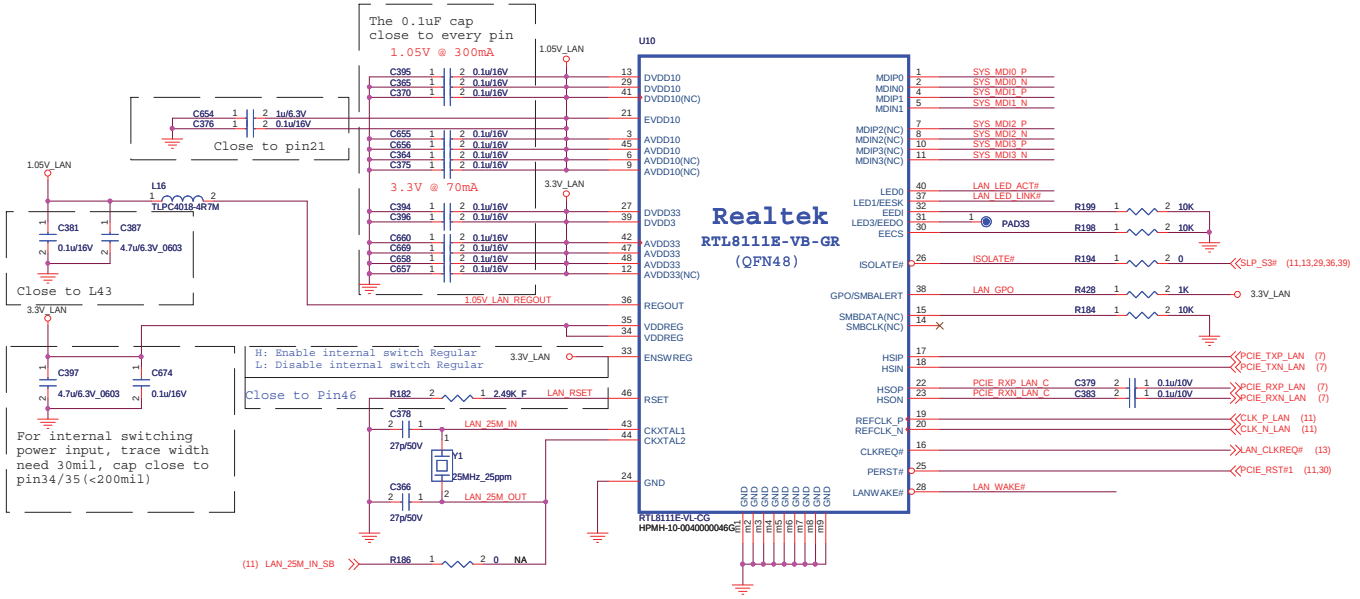
For 17" M/B only



FLEXComputing

Project Name : H510UA1	Title : Card Reader -- Realtek RTS5209
Size :	Document Number : HPMH-40GAB6300-D — Rev : D
Date: Thursday, December 30, 2010	Sheet : 31 of 51

GbLAN

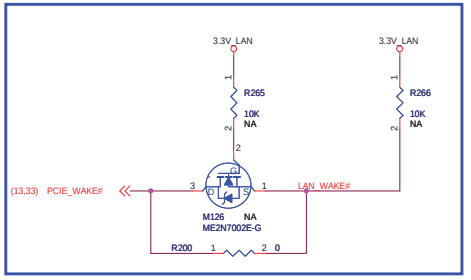


Mini-spec requirements:
10/100/1000 :
- Link :White
- Activity :Amber/Yellow

RTL8111E

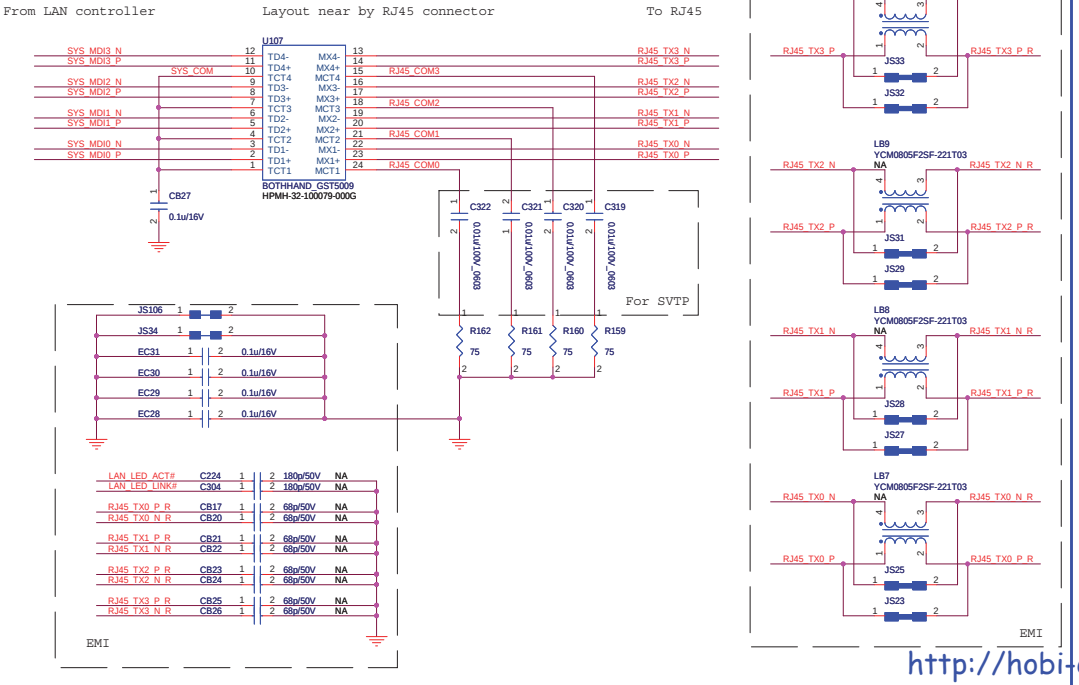
LEDS1-0	00	01	10	11
LED0	ACT ALL	LINK ALL /ACT ALL	LINK10 /ACT ALL	LINK10 /ACT10
LED1	LINK100	LINK100	LINK100	LINK100 /ACT100
LED3	LINK1000	LINK1000	LINK1000	LINK1000 /ACT1000

LEDS1-0s initial value comes from the EEPROM if there is no EEPROM, the default value is 11

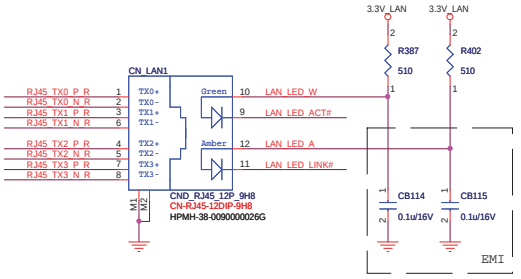


Transformer

Transformer :
Gbit P/N: 32-100079-000G(GST5009)
10/100 P/N: 32-0000000009G(TST1284)

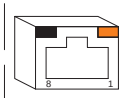


RJ45



Amber
Vf=2V If =20mA
White
Vf=3.2V If =30mA

Reference:
RJ45 Phone Jack
Pin define:
1 TXD+0
2 TXD-0
3 TXD+1
4 TXD+2
5 TXD-2
6 TXD-1
7 TXD+3
8 TXD-3



SVTP_v4.03 - 2.6 - Ethernet Checklist - Rev C.xls

- Ch.3.1.4.4
Some older cheap RJ-45s only populate pins 1,2,3,6. 10/100 requires the other 4 pins for grounding. Gigabit Ethernet requires all 8 pins for data signals.

- Ch.3.1.4.13
Resistance from RJ-45 shell to any other chassis ground point (ohms) less than 1 ohm

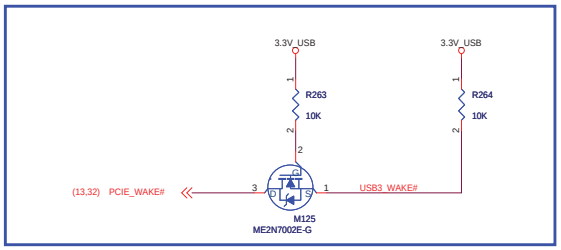
- Ch.3.1.4.14 & Ch.3.1.4.15
Protection against non-standard power-over-Ethernet (PoE) :
Resistance between pins 1,3 (TXD0P,TXD1P) and pins 4,7 (TXD2P,TXD3P) of the RJ-45 greater than 58K ohms.

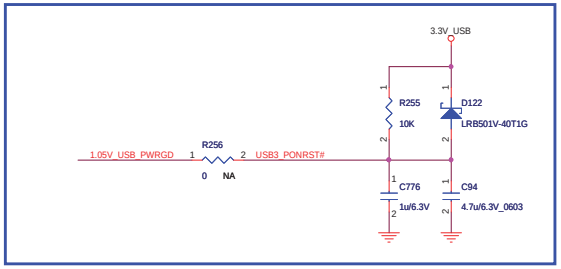
FLEXComputing

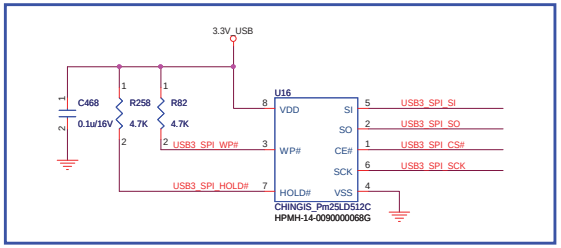
Project Name : H510UA1	Title : Gb LAN -- RL8111E-VB-GR
Size :	Document Number : HPMH-40GAB6300-D Rev : D
Date: Thursday, December 30, 2010	Sheet : 32 of 51

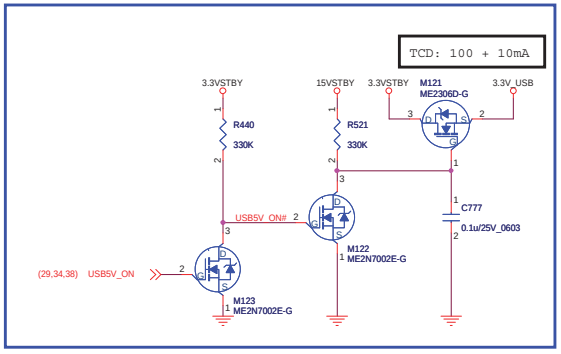
USB3.0 Controller

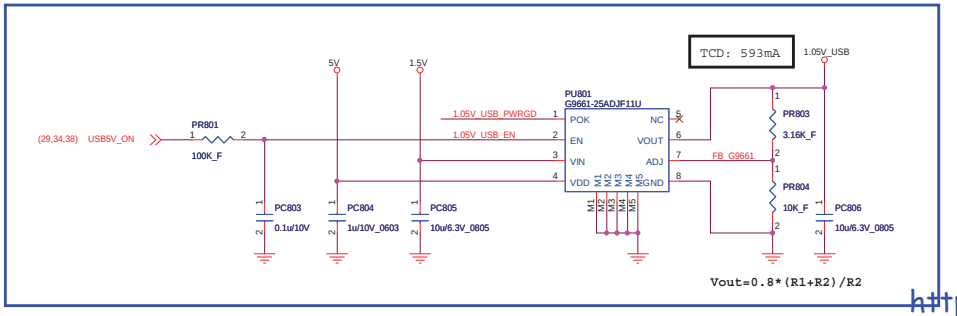
Leave empty for IMR

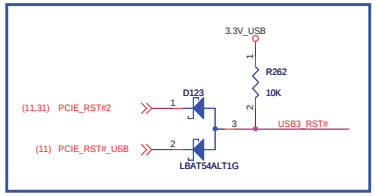


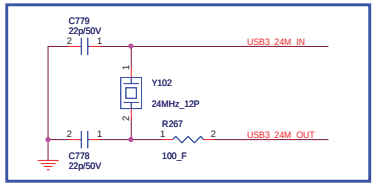


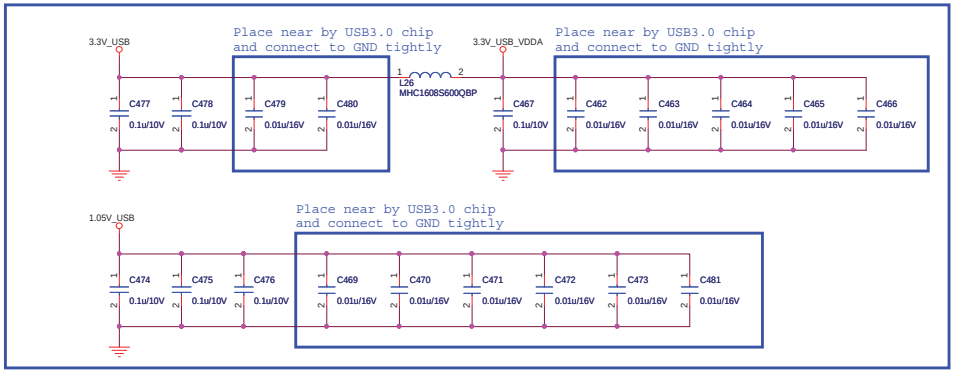








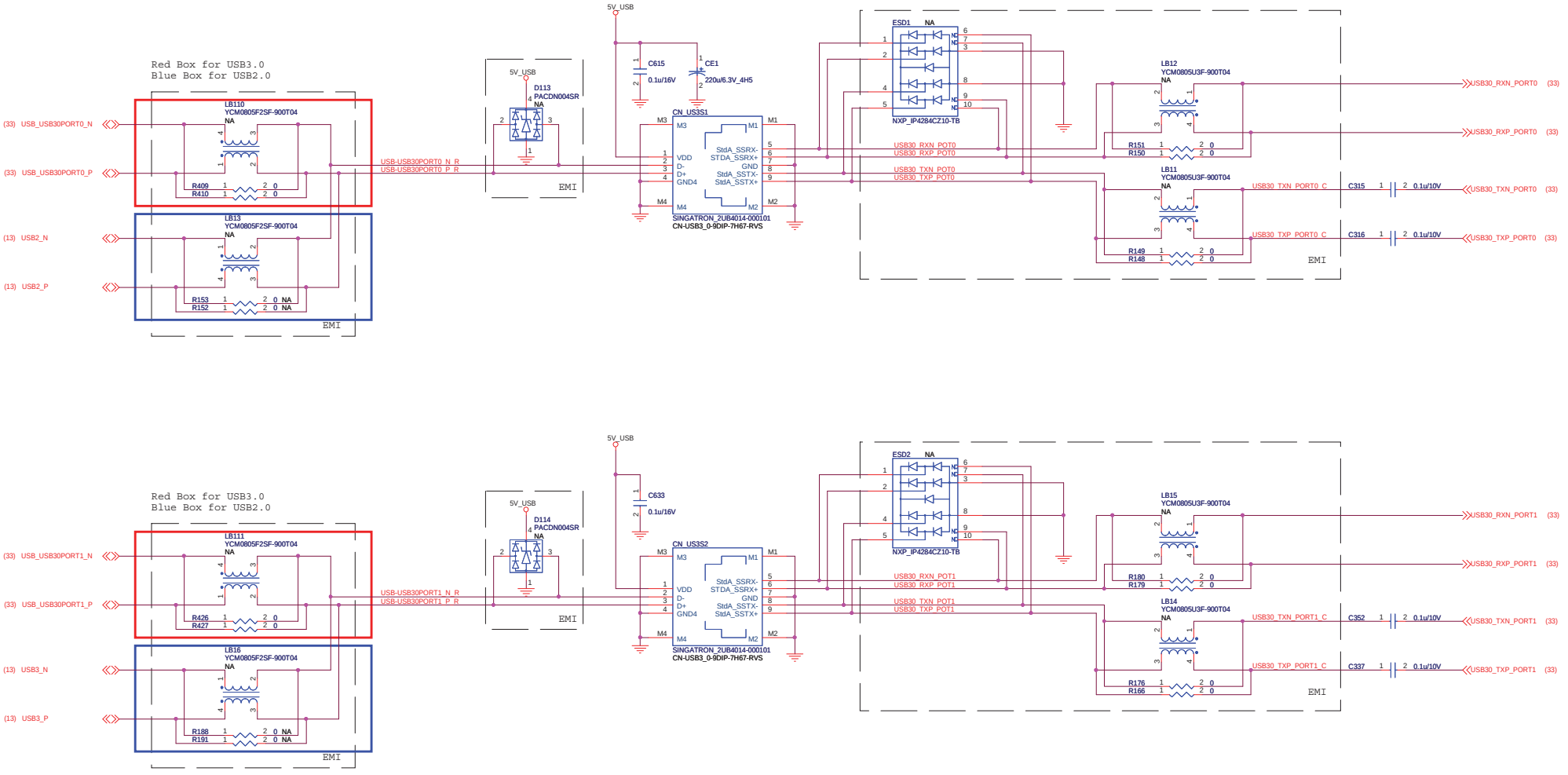




FLEXComputing

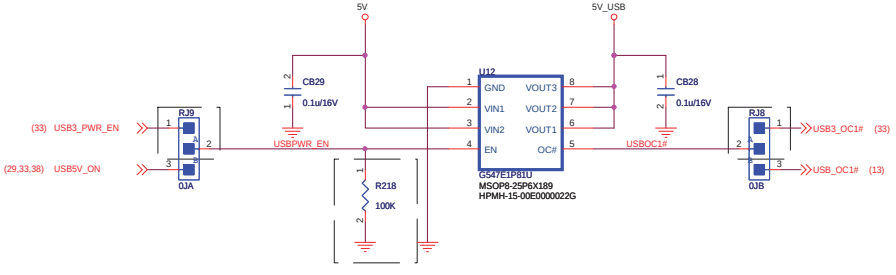
Project Name : H510UA1	Title : USB3.0 Controller -- uPD720200	
Size :	Document Number : HPMH-40GAB6300-D	Rev : D
Date: Thursday, December 30, 2010	Sheet : 33 of 51	

USB 3.0/ 2.0



USB PWR SW

USB 3.0: RJ8& RJ9 mounted A, B.
USB 2.0: RJ8& RJ9 mounted B, B.



For disable Power SW in G3.

USB3.0 Conn:
- HPMH-38-0040000065G -- CONN USB 3.0 9P 2UB4014-000101 SINGATRON
- HPMH-38-0040000067G -- CONN USB 3.0 9PIN TARA7-9Y5391 ACON
- HPMH-38-0040000068G -- CONN USB 3.0 9P USBF-D9F1-ANR1-00 E-CONN
- HPMH-38-0040000088G -- CONN USB3.0 1-1932354-1 9P H:7.4mm

USB2.0 Conn:
- HPMH-38-0040000066G -- CONN USB 2.0 4P 2UB4015-000111 SINGATRON
- HPMH-38-0040000070G -- CONN USB 2.0 4PIN UARBS-4K5986 ACON
- HPMH-38-0040000071G -- CONN USB 2.0 4P USBF-D4F1-ANR1-CA E-CONN

FLEXComputing

Project Name : H510UA1	Title : USB3.0 PWR/ USB I/F
Size :	Document Number : HPMH-40GAB6300-D Rev : D
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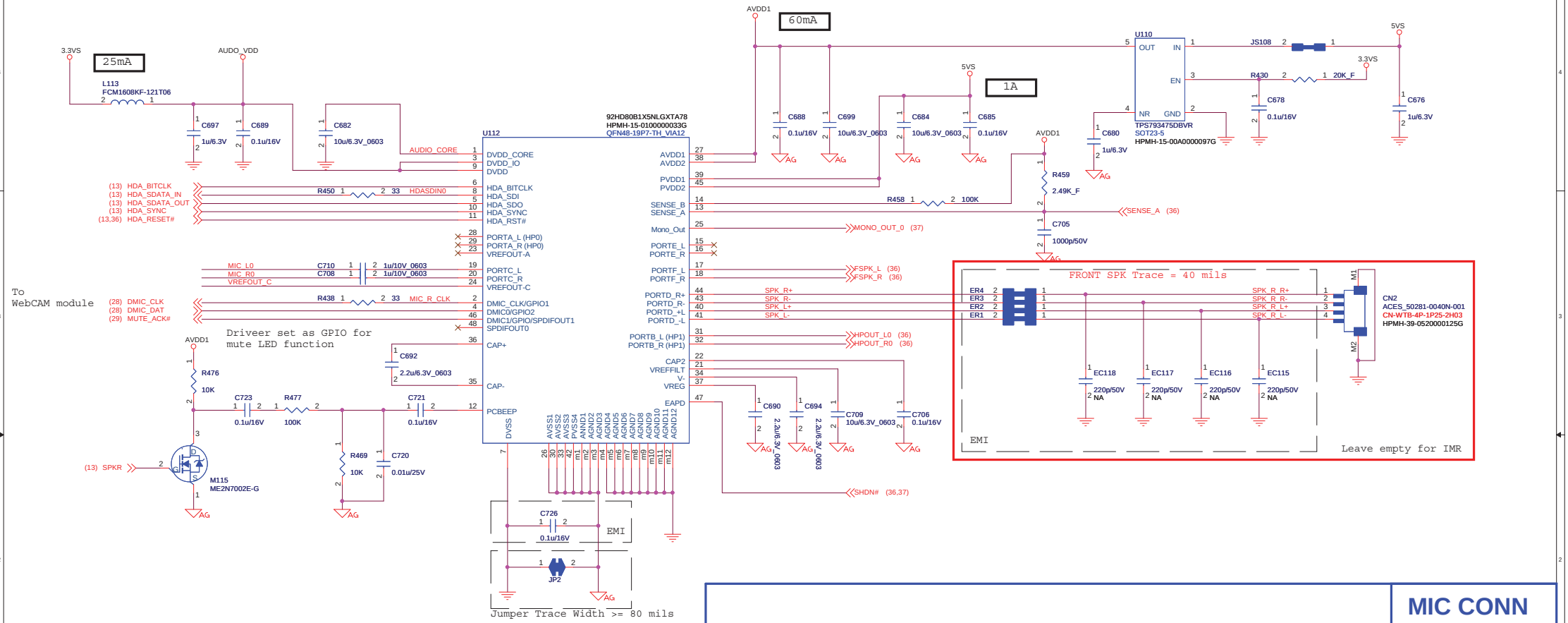
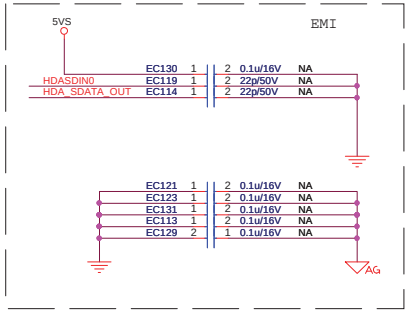
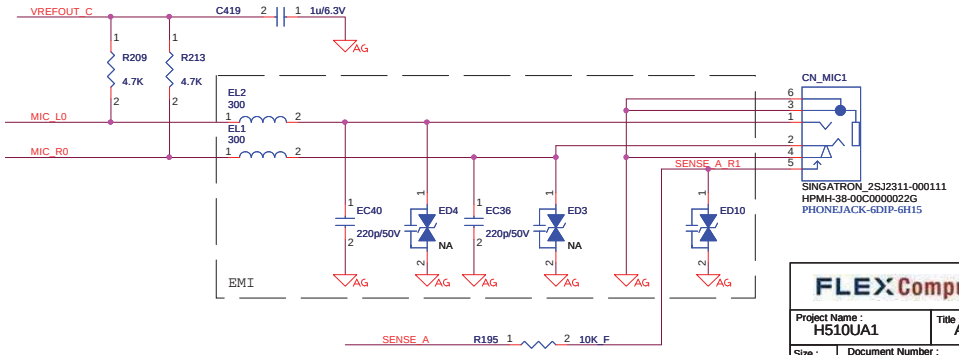
Audio CODEC





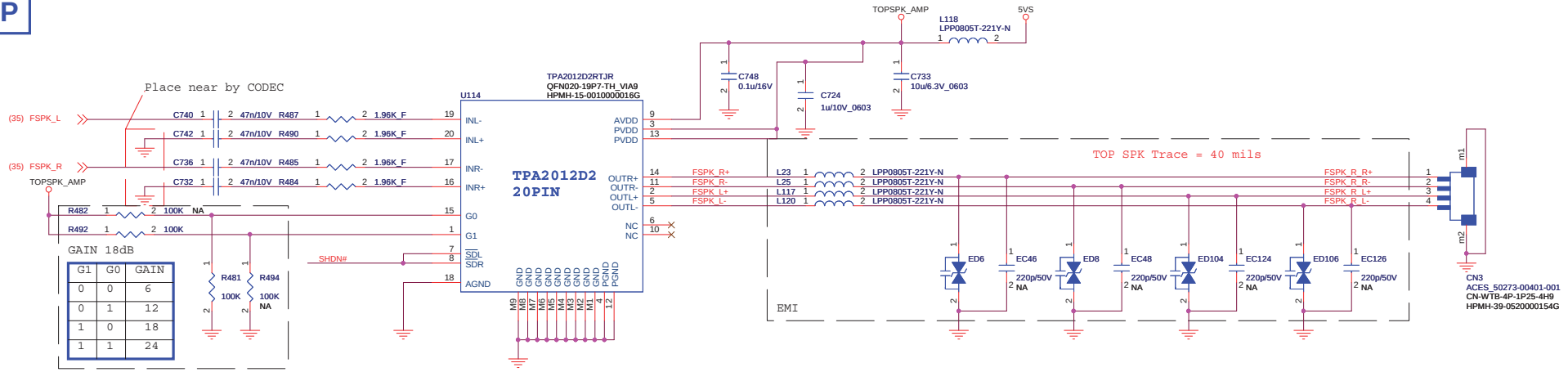
MIC CONN



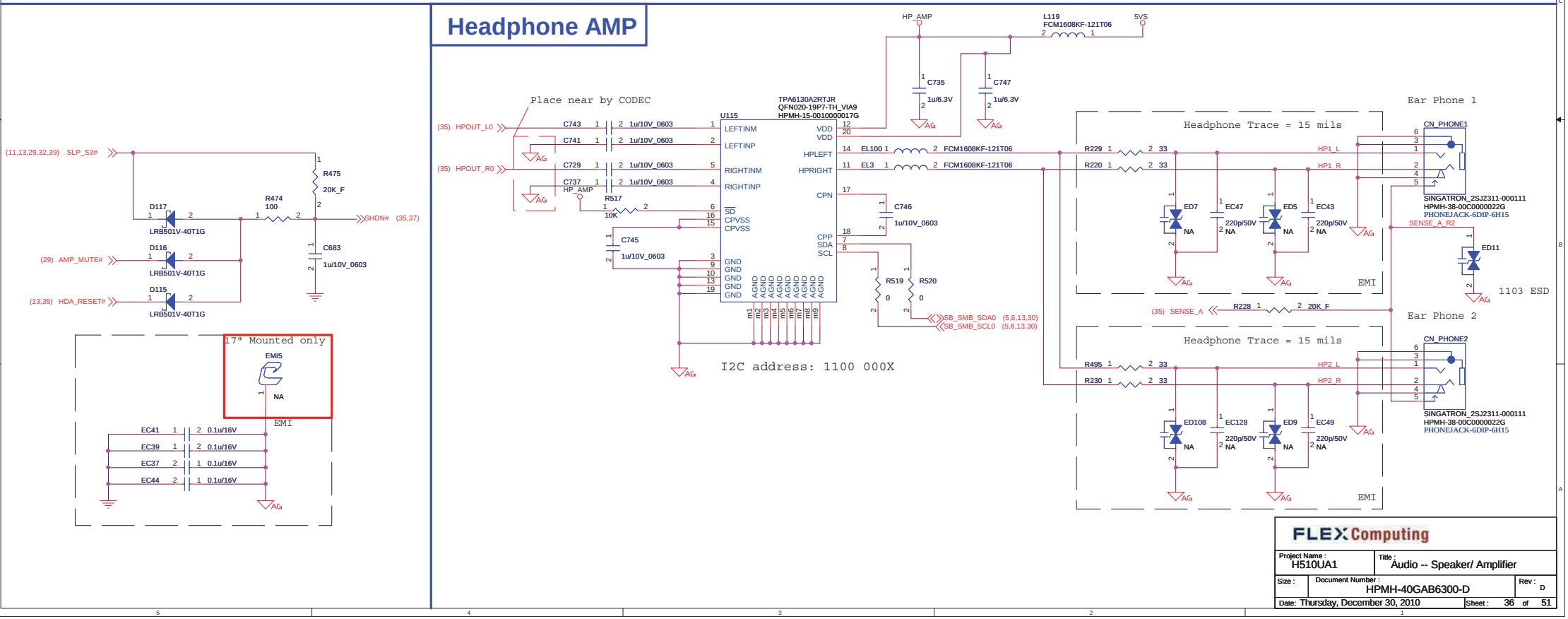
FLEX Computing

Project Name : H510UA1	Title : Audio -- IDT92HD80TA
Size :	Document Number : HPMH-40GAB6300-D — Rev : D
Date: Thursday, December 30, 2010	Sheet : 35 of 51

FRONT SPK AMP



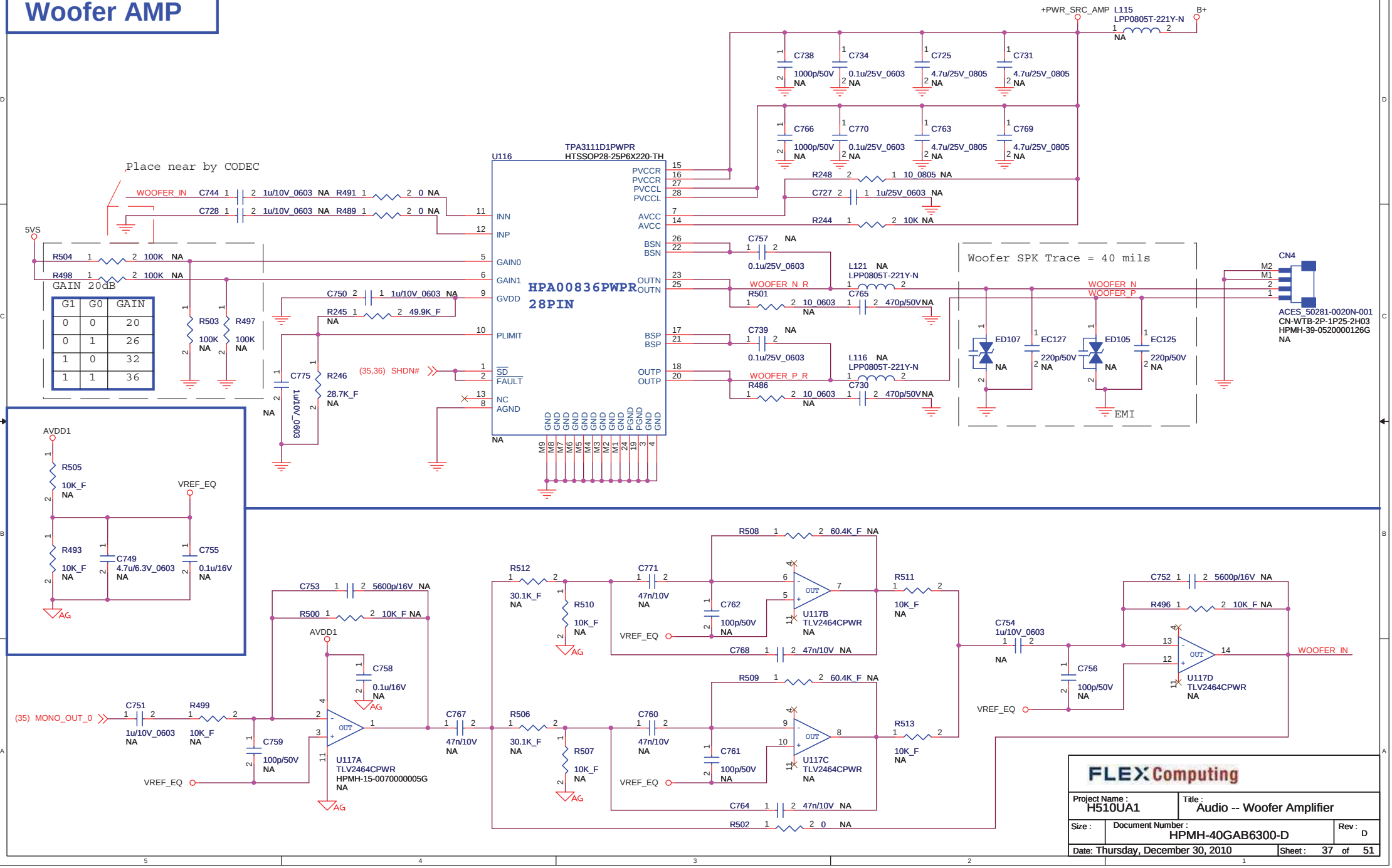
Headphone AMP



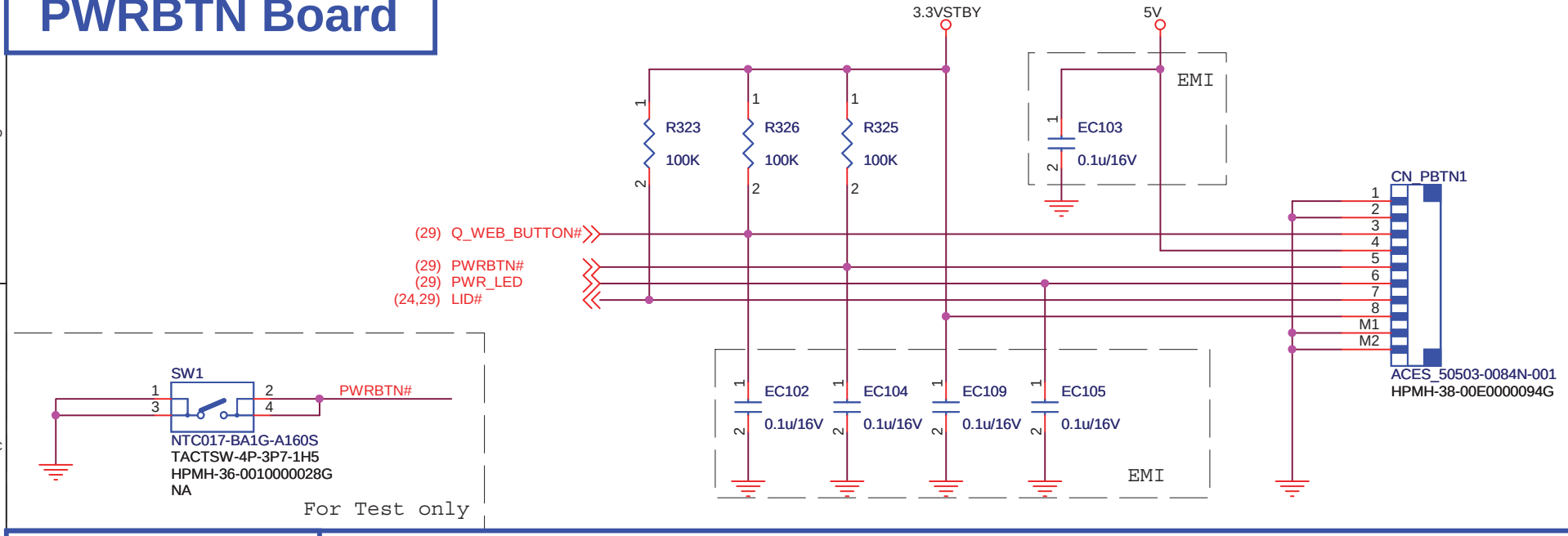
FLEX Computing

Project Name : H510UA1	Title : Audio -- Speaker/ Amplifier
Size :	Document Number : HPMH-40GAB6300-D — Rev : D
Date: Thursday, December 30, 2010	Sheet : 36 of 51

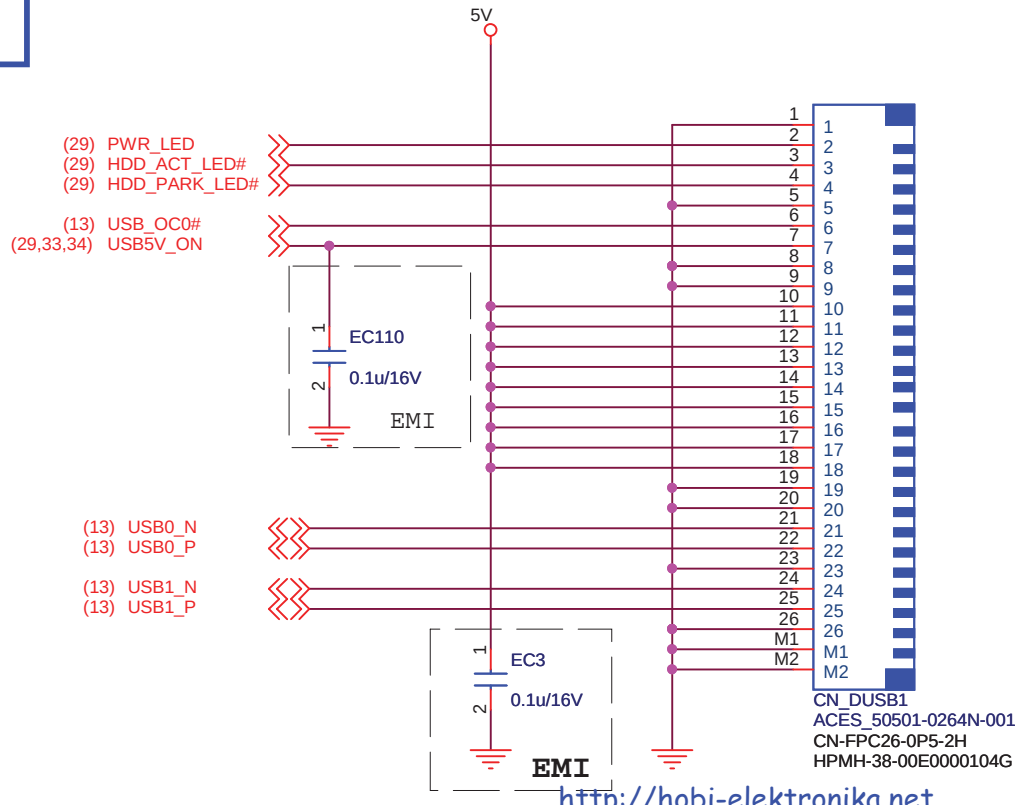
Woofer AMP



PWRBTN Board



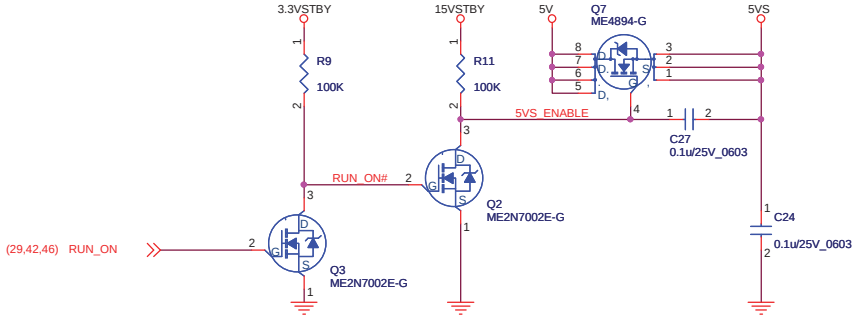
USB Board

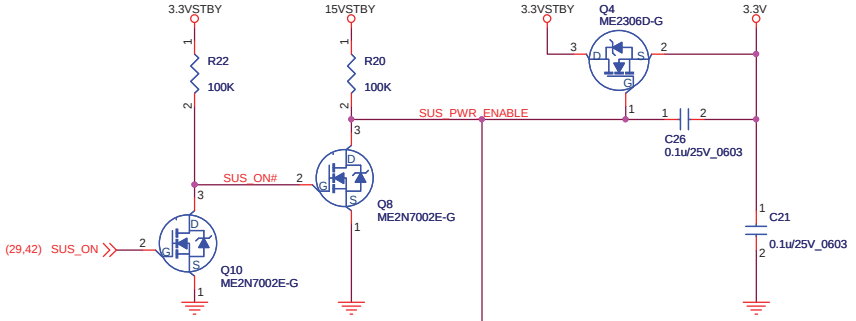


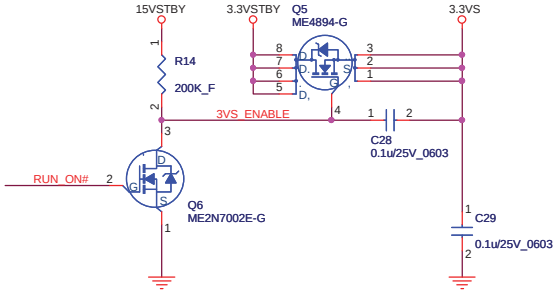
FLEXComputing

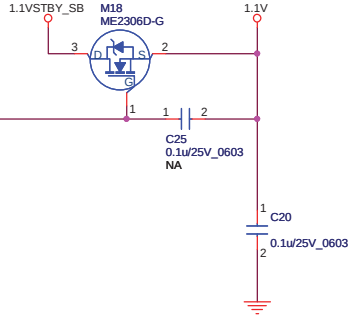
Project Name : H510UA1	Title : Daughter Board Connector	
Size :	Document Number : HPMH-40GAB6300-D	Rev : D
Date: Thursday, December 30, 2010	Sheet : 38 of 51	

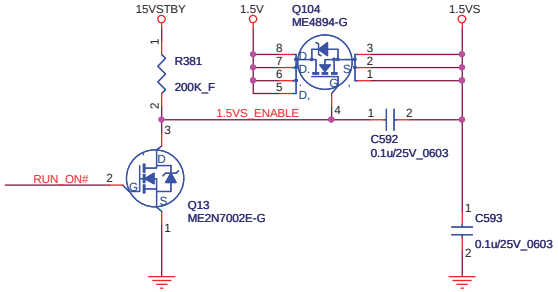
RUN/ SUS PWR

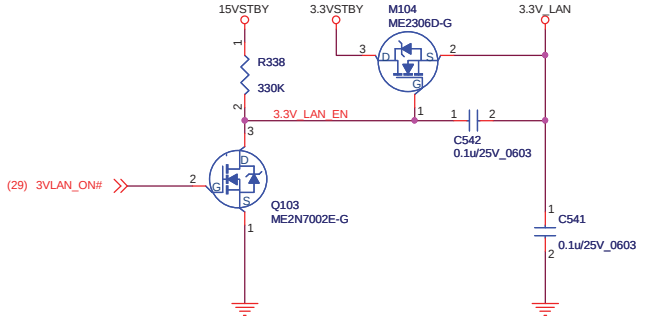


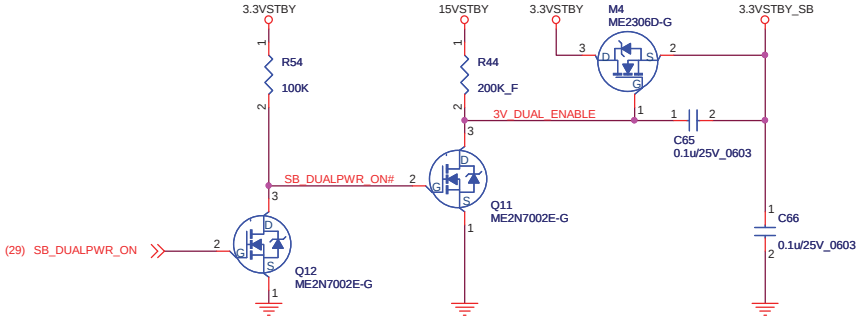




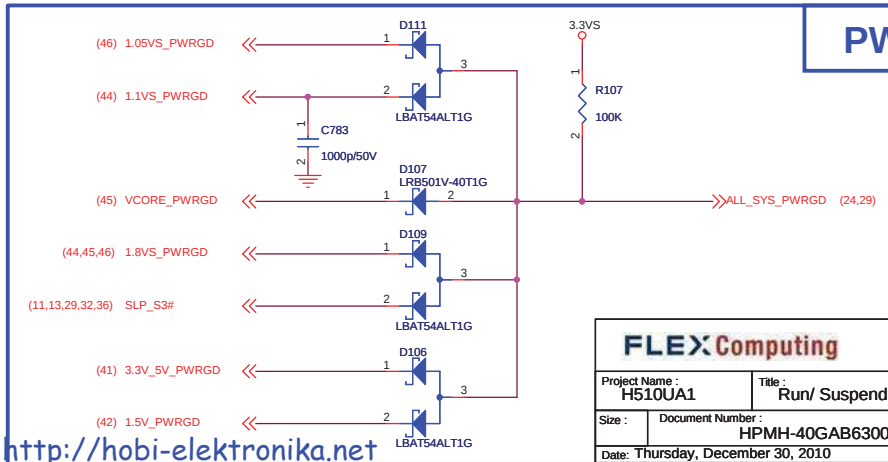








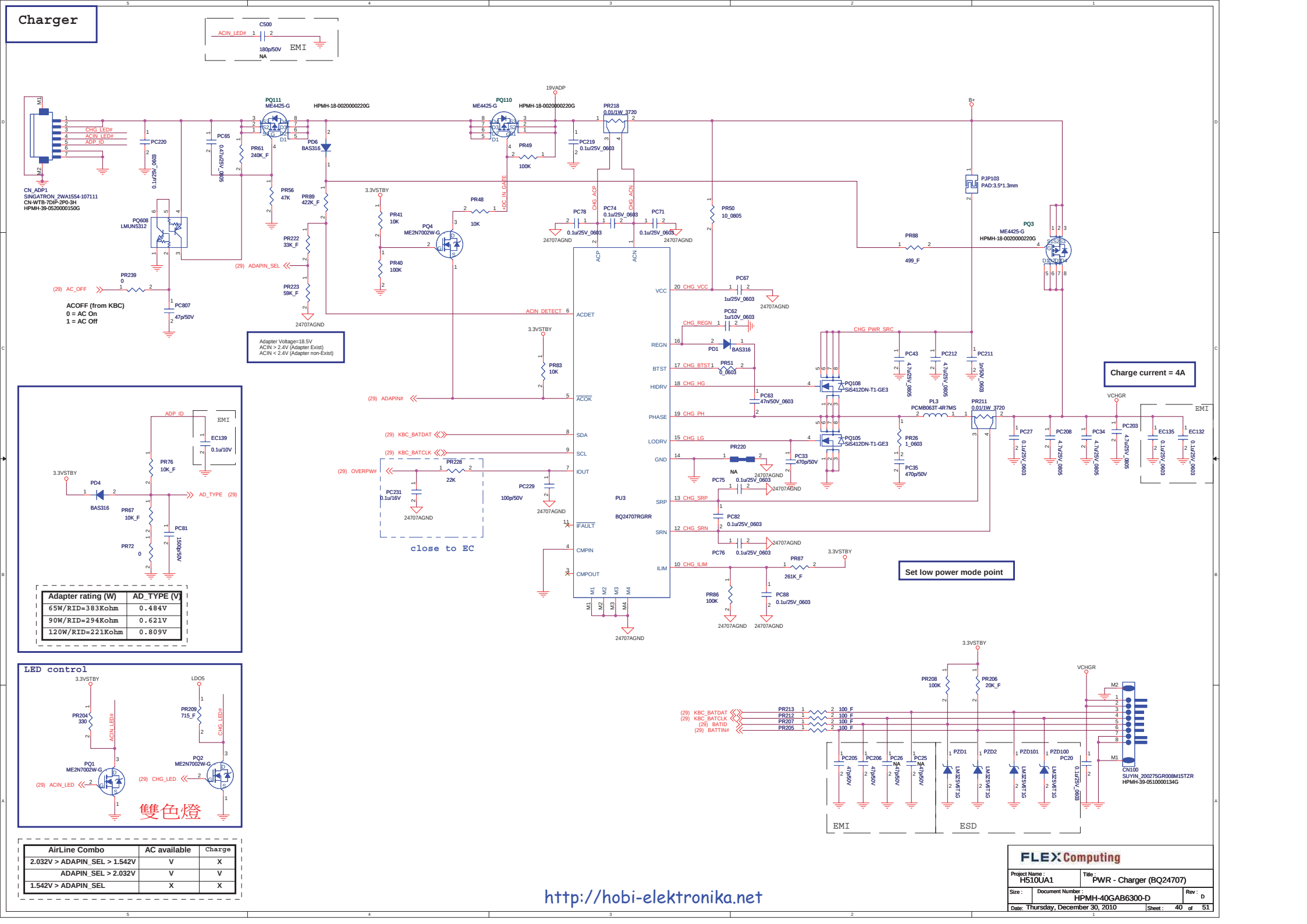
PWRGD



FLEX Computing

Project Name : H510UA1	Title : Run/ Suspend PWR switch
Size :	Document Number : HPMH-40GAB6300-D
Rev : D	
Date: Thursday, December 30, 2010	Sheet : 39 of 51

Charger


C500
ACIN_LED#
180p/50V
NA
EMI
CN_ADP1
SINGATRON_2WA1554-107111
CN-WTB-7DIP-2P0-3H
HPMH-39-0520000150G
CHG_LED#
ACIN_LED#
ADP_ID
PC220
0.1u/25V_0603
PC65
0.47u/25V_0805
PQ111
ME4425-G
HPMH-18-0020000220G
PD6
BAS316
PR61
240K_F
PR56
47K
PR89
422K_F
PR222
33K_F
PR223
59K_F
PQ608
LMUN5312
PR239
0
PC807
47p/50V
(29) AC_OFF
(29) ADAPIN_SEL
ACOFF (from KBC)
0 = AC On
1 = AC Off
24707AGND
Adapter Voltage=18.5V
ACIN > 2.4V (Adapter Exist)
ACIN < 2.4V (Adapter non-Exist)
19VADP
PQ110
ME4425-G
HPMH-18-0020000220G
PR218
0.01/1W_3720
PR49
100K
PC219
0.1u/25V_0603
DC_IN_GATE
3.3VSTBY
PR41
10K
PR40
100K
PR48
10K
PQ4
ME2N7002W-G
CHG_ACP
CHG_ACN
PC78
0.1u/25V_0603
PC74
0.1u/25V_0603
PC71
0.1u/25V_0603
PR50
10_0805
B+
PJP103
PAD:3.5*1.3mm
PR88
499_F
PQ3
ME4425-G
HPMH-18-0020000220G
ACIN_DETECT
ACDET
ACP
ACN
VCC
REGN
BTST
HIDRV
PHASE
LODRV
GND
SRP
SRN
ILIM
SDA
SCL
IOUT
IFAULT
CMPIN
CMPOUT
ACOK
PU3
BQ24707RGRR
CHG_VCC
PC67
1u/25V_0603
PC62
1u/10V_0603
CHG_REGN
PD1
BAS316
CHG_BTST
PR51
0_0603
CHG_HG
CHG_PH
CHG_LG
CHG_SRP
CHG_SRN
CHG_ILIM
CHG_PWR_SRC
PQ108
SiS412DN-T1-GE3
PQ105
SiS412DN-T1-GE3
PC63
47n/50V_0603
PR220
PC33
470p/50V
PC75
0.1u/25V_0603
PC82
0.1u/25V_0603
PC76
0.1u/25V_0603
PR87
261K_F
PR86
100K
PC88
0.1u/25V_0603
PC43
4.7u/25V_0805
PC212
4.7u/25V_0805
PC211
1u/50V_0603
PL3
PCMB063T-4R7MS
PR211
0.01/1W_3720
PR26
1_0603
PC35
470p/50V
PC27
0.1u/25V_0603
PC208
4.7u/25V_0805
PC34
4.7u/25V_0805
PC203
4.7u/25V_0805
EC135
0.1u/25V_0603
EC132
0.1u/25V_0603
VCHGR
Charge current = 4A
Set low power mode point
(29) ADAPIN#
(29) KBC_BATDAT
(29) KBC_BATCLK
(29) OVERPW#
PR228
22K
PC231
0.1u/16V
PC229
100p/50V
close to EC
ADP_ID
EC139
0.1u/10V
PR76
10K_F
PD4
BAS316
AD_TYPE (29)
PR67
10K_F
PR72
0
PC81
1500p/50V
Adapter rating (W) | AD_TYPE (V)
65W/RID=383Kohm | 0.484V
90W/RID=294Kohm | 0.621V
120W/RID=221Kohm | 0.809V
LED control
LDO5
PR204
330
PR209
715_F
PQ1
ME2N7002W-G
PQ2
ME2N7002W-G
(29) ACIN_LED
(29) CHG_LED
雙色燈
PR213
PR212
PR207
PR205
(29) BATID
(29) BATTIN#
100_F
PR208
100K
PR206
20K_F
PC205
PC206
PC26
PC25
NA
4.7u/50V
PZD1
PZD2
PZD101
PZD100
PC20
LM4625V6TLG
0.1u/25V_0603
CN100
SUYIN_200275GR008M15TZR
HPMH-39-0510000134G
EMI
ESD
AirLine Combo | AC available | Charge
2.032V > ADAPIN_SEL > 1.542V | V | X
ADAPIN_SEL > 2.032V | V | V
1.542V > ADAPIN_SEL | X | X
http://hobi-elektronika.net
FLEXComputing
Project Name : H510UA1
Title : PWR - Charger (BQ24707)
Size :
Document Number : HPMH-40GAB6300-D
Rev : D
Date: Thursday, December 30, 2010
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5V / 3.3VSTBY

Freq= 365KHz
TDC = 6 A
OCP = 10 A

Freq = 460KHz
TDC = 4 A
OCP = 5.7A

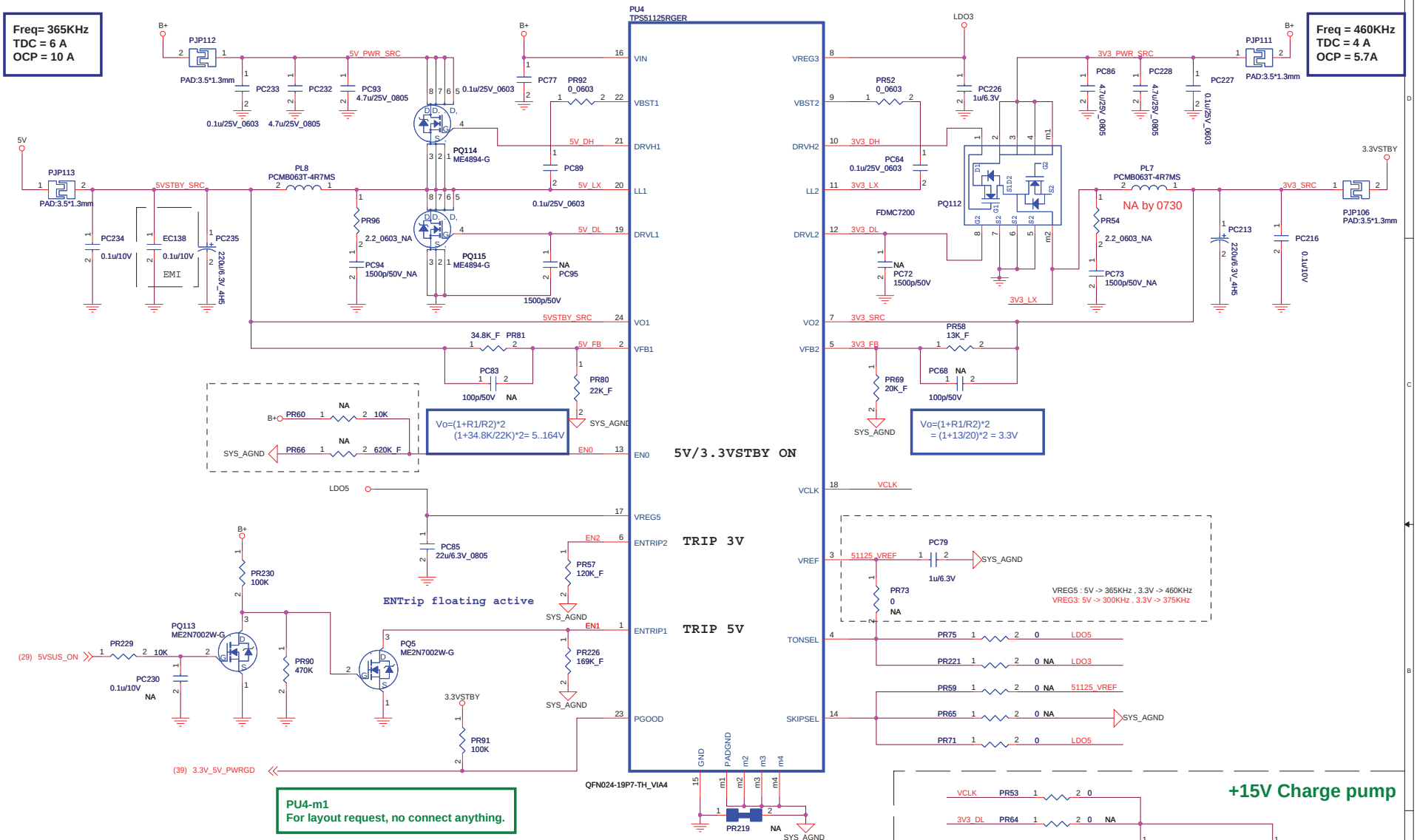


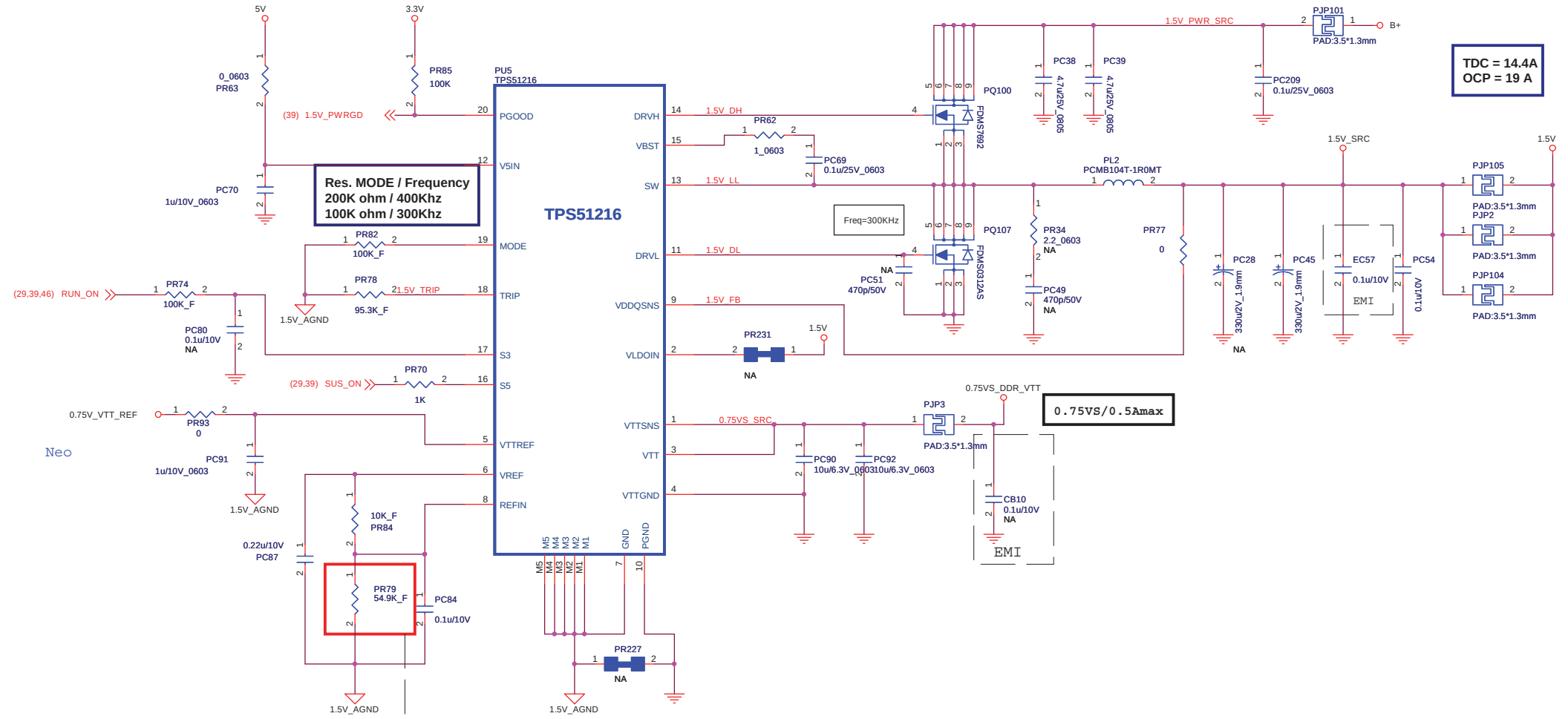
Table 3. Enabling State

EN0	ENTRIP1	ENTRIP2	VREF	VREG5	VREG3	CH1	CH2	VCLK
GND	Don't Care	Don't Care	Off	Off	Off	Off	Off	Off
R to GND	Off	Off	On	On	On	Off	Off	Off
R to GND	On	Off	On	On	On	On	Off	Off
R to GND	Off	On	On	On	On	Off	On	Off
R to GND	On	On	On	On	On	On	On	Off
Open	Off	Off	On	On	On	Off	Off	Off
Open	On	Off	On	On	On	On	Off	On
Open	Off	On	On	On	On	Off	On	Off
Open	On	On	On	On	On	On	On	On

FLEX Computing

Project Name : H510UA1	Title : PWR -- 3V/ 5V (TPS51125)
Size :	Document Number : HPMH-40GAB6300-D — Rev : D
Date: Thursday, December 30, 2010	Sheet : 41 of 51

1.5V



	UMA	Discret
PR79	49.9K ohm 1% HPMH-30-149921-990G	54.9K ohm 1% HPMH-30-154921-990G

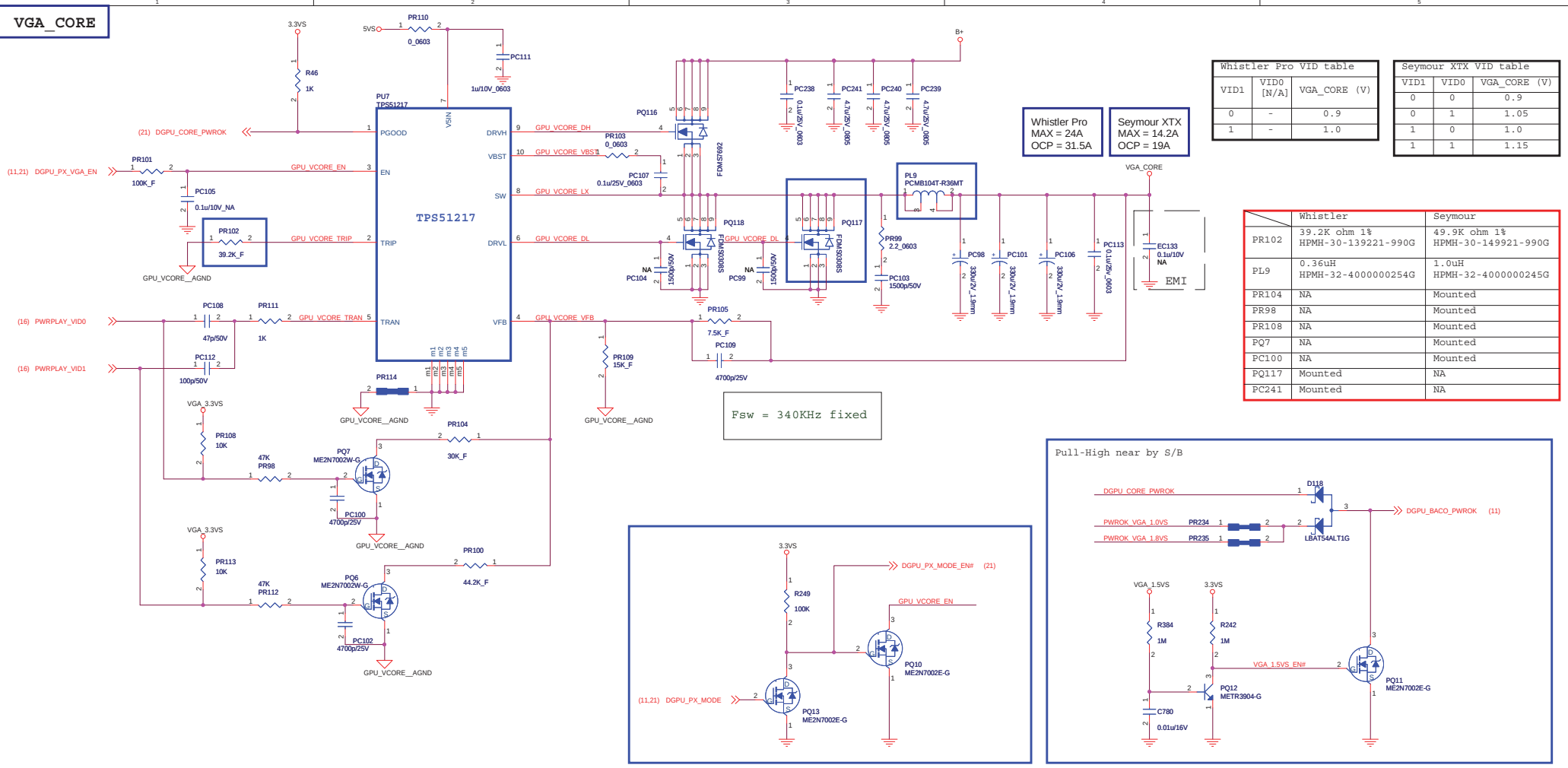
Table 1. S3 and S5 Control Table

STATE	S3	S5	VTTREF	VTT
S0	H	H	1	1
S3	L	H	1	0 (high-Z)
S4/S5	L	L	0 (discharge)	0 (discharge)

FLEXComputing

Project Name : H510UA1	Title : PWR -- DDR PWR (TPS51216)
Size :	Document Number : HPMH-40GAB6300-D Rev : D
Date: Thursday, December 30, 2010	Sheet : 42 of 51

VGA_CORE



Whistler Pro
MAX = 24A
OCP = 31.5A

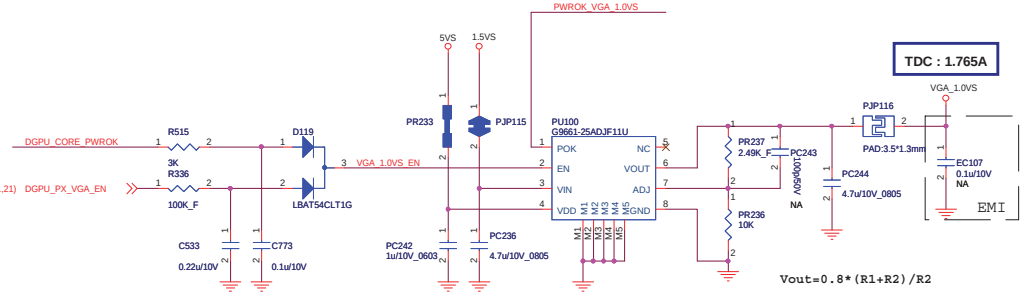
Seymour XTX
MAX = 14.2A
OCP = 19A

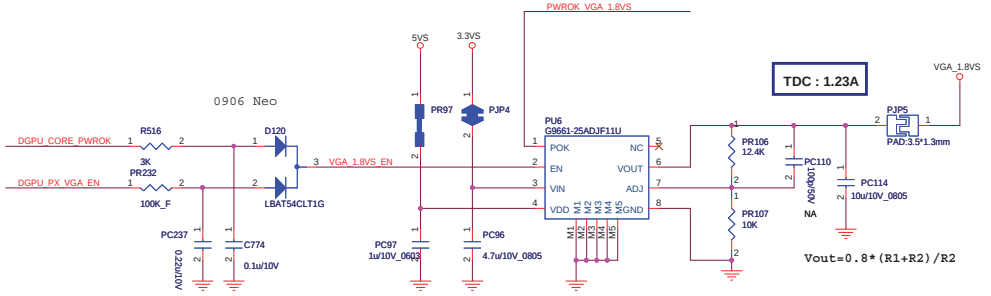
Whistler Pro VID table		
VID1	VID0 [N/A]	VGA_CORE (V)
0	-	0.9
1	-	1.0

Seymour XTX VID table		
VID1	VID0	VGA_CORE (V)
0	0	0.9
0	1	1.05
1	0	1.0
1	1	1.15

	Whistler	Seymour
PR102	39.2K ohm 1% HPMH-30-139221-990G	49.9K ohm 1% HPMH-30-149921-990G
PL9	0.36uH HPMH-32-4000000254G	1.0uH HPMH-32-4000000245G
PR104	NA	Mounted
PR98	NA	Mounted
PR108	NA	Mounted
PQ7	NA	Mounted
PC100	NA	Mounted
PQ117	Mounted	NA
PC241	Mounted	NA

Pull-High near by S/B

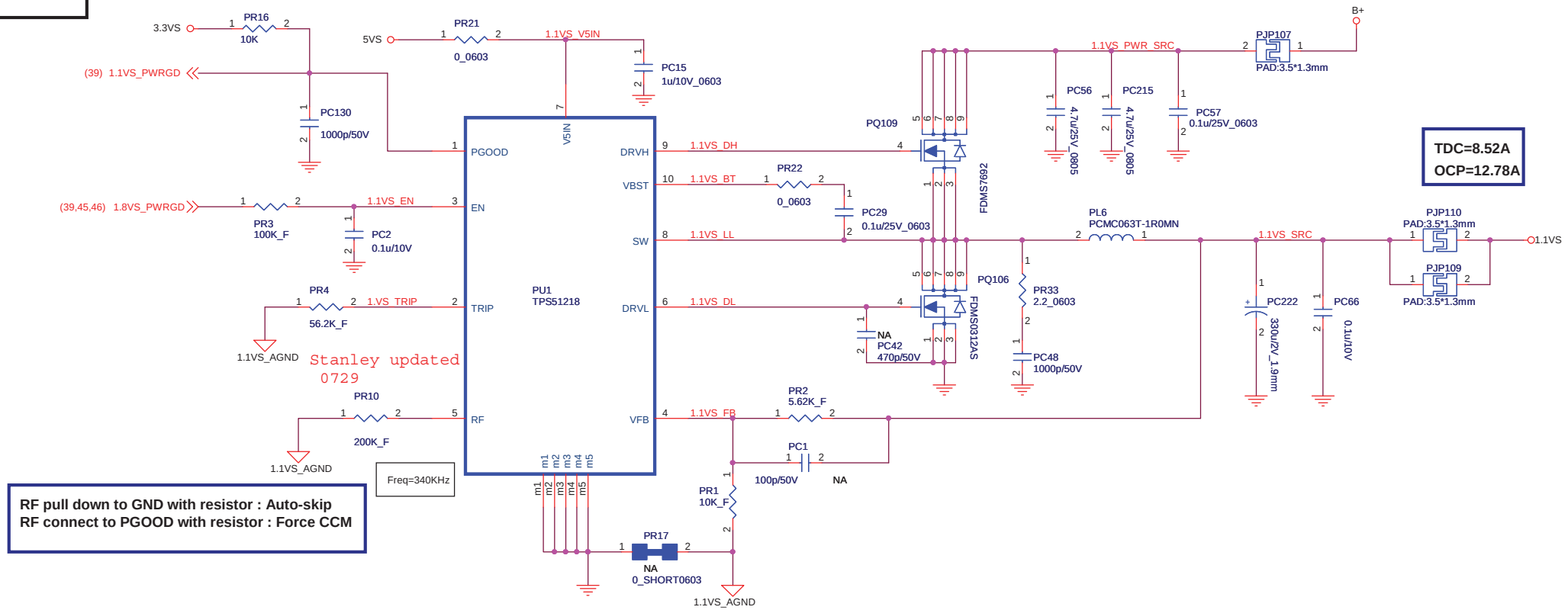




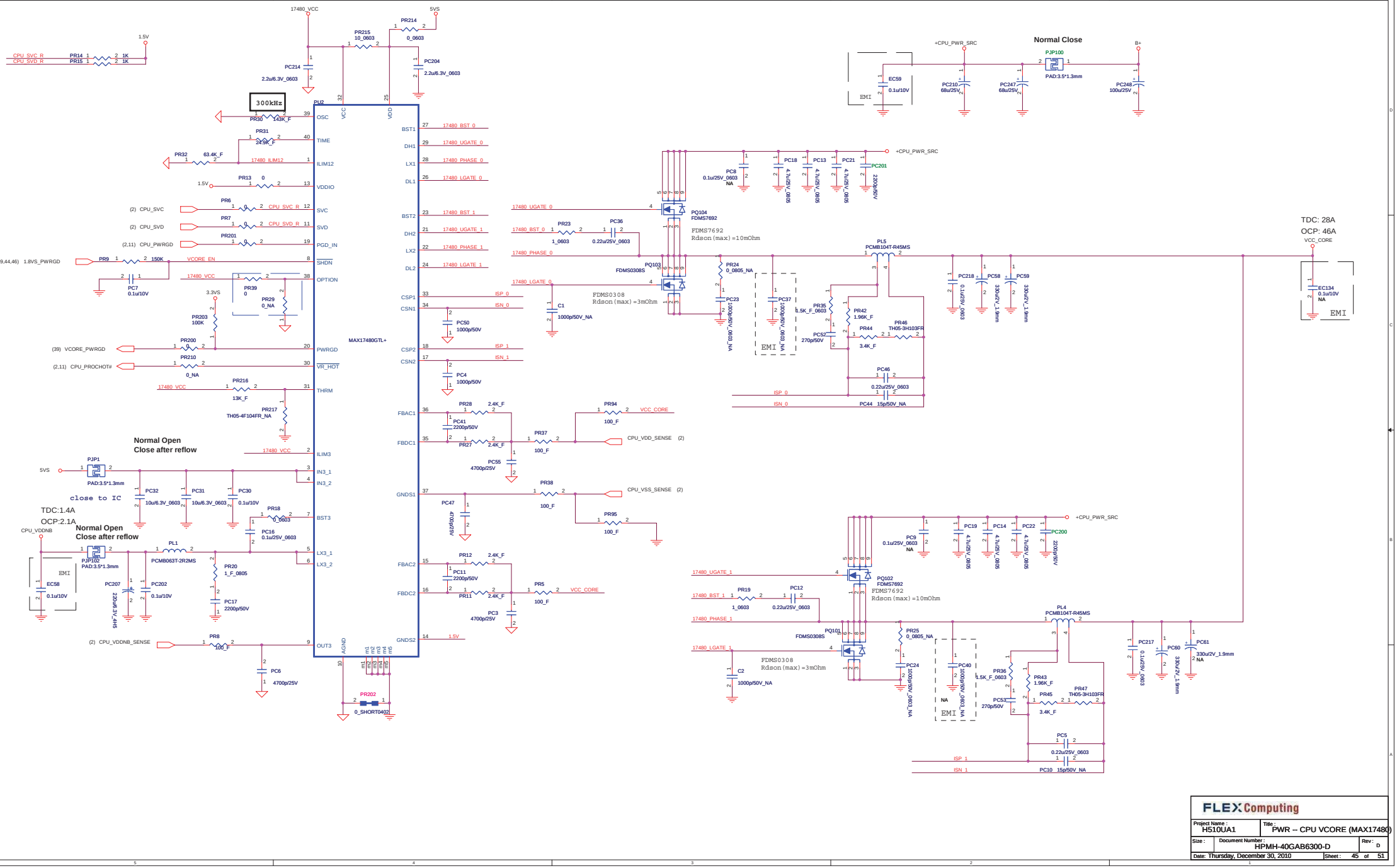
FLEX Computing

Project Name : H510UA1	Title : PWR - GPU Core (TPS51217)
Size :	Document Number : HPMH-40GAB6300-D Rev : D
Date: Tuesday, January 11, 2011	Sheet : 43 of 51

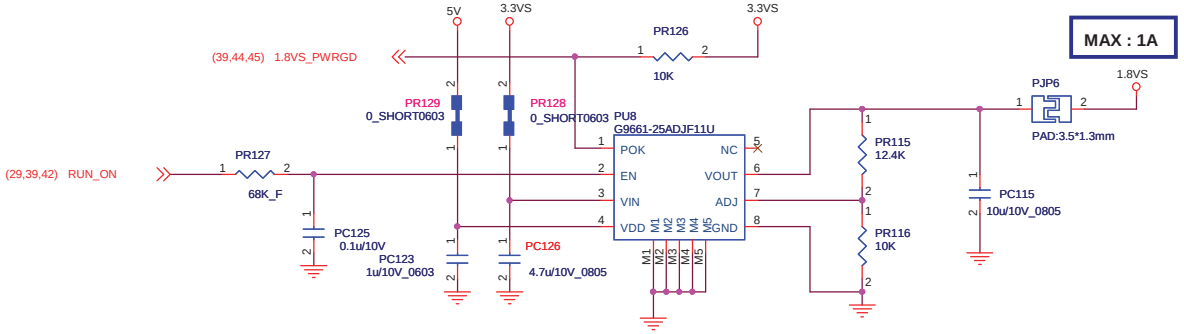
1.1VS



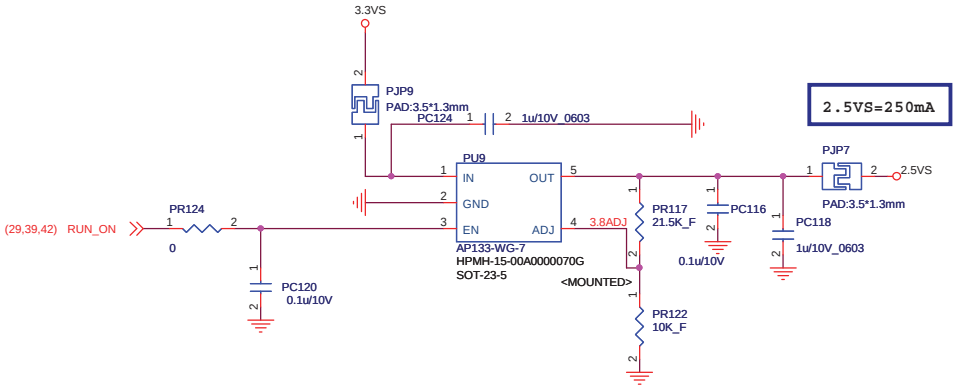
FLEX Computing		
Project Name : H510UA1	Title : PWR -- 1.1VS (TPS51218)	
Size :	Document Number : HPMH-40GAB6300-D	Rev : D
Date: Thursday, December 30, 2010	Sheet : 44 of 51	


MAX17480GTL+
300kHz
Normal Open
Close after reflow
close to IC
TDC:1.4A
OCP:2.1A
Normal Close
TDC: 28A
OCP: 46A
FDMS0308
Rdson(max)=3mOhm
FDMS7692
Rdson(max)=10mOhm
PCMB104T-R45MS
PCMB063T-2R2MS
EMI
+CPU_PWR_SRC
VCC_CORE
CPU_VDD_SENSE
CPU_VSS_SENSE
CPU_VDDNB
http://hobi-elektronika.net
FLEX Computing
Project Name : H510UA1
Title : PWR -- CPU VCORE (MAX17480)
Size :
Document Number : HPMH-40GAB6300-D
Rev : D
Date: Thursday, December 30, 2010
Sheet : 45 of 51

1.8VS

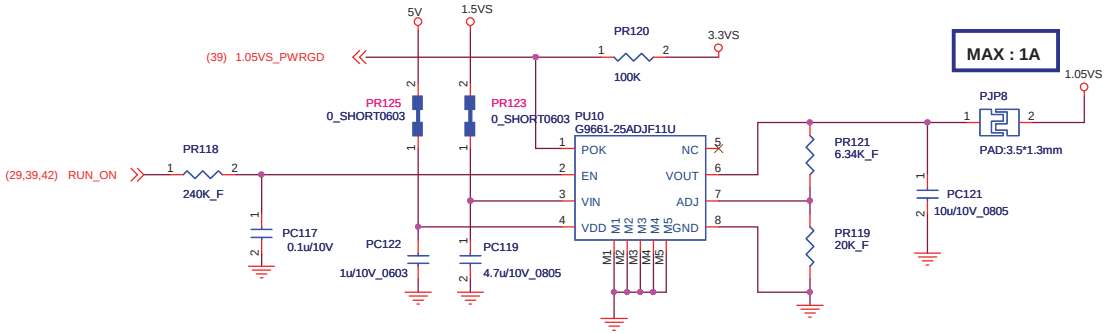


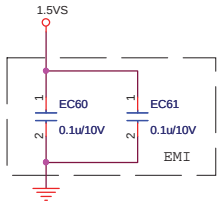
2.5VS



AP133:
Low dropout: 350mV at 300mA
EN logic low: <0.4V
EN logic high: >1.4V
Thermal shutdown: 145'C

1.05VS





FLEXComputing

Project Name : H510UA1	Title : PWR -- 1.8VS/ 1.05VS/ 2.5VS
Size :	Document Number : HPMH-40GAB6300-D
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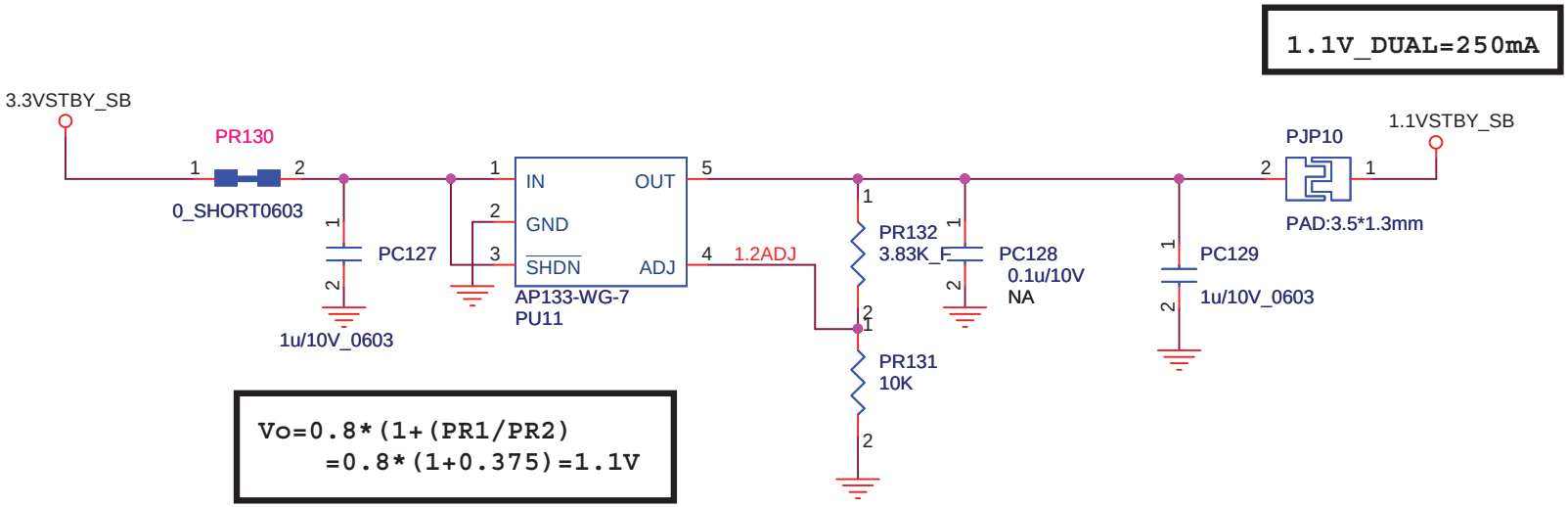
Date: Thursday, December 30, 2010	Sheet : 46 of 51

1.1VSTBY



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FLEX Computing		
Project Name : H510UA1	Title : PWR -- 1.1VSTBY_SB (AP133)	
Size :	Document Number : HPMH-40GAB6300-D	Rev : D
Date: Thursday, December 30, 2010	Sheet : 47 of 51	

Screw Hole

H9 PTH6B7_2.8 THR236B276_110
H17 PTH7B8_2.8 THR276B315_110
H21 PTH7B8_2.8 THR276B315_110
H10 PTH7B4.8_3.8 THR276B189_150
H11 PTH7B4.8_3.8 THR276B189_150
H15 PTH7B4.8_3.8 THR276B189_150
H16 PTH7B4.8_3.8 THR276B189_150
H18 PTH3.1B7_2.1 THR122B276_083
H19 PTH3.1B7_2.1 THR122B276_083
H20 PTH8B7_2.8 THR315B276_110
H7 PTH3.1B7_2.1 THR122B276_083
H2 PTH8B7_2.8 THR315B276_110
H1 PTH8B7_2.8 THR315B276_110
H5 PTH7B4.8_3.8 THR276B189_150
H6 PTH7B4.8_3.8 THR276B189_150
H12 PTH7B4.8_3.8 THR276B189_150
H13 PTH7B4.8_3.8 THR276B189_150
H14 PTH7B8_2.8 THR276B315_110
H3 PTH6.8_2.8 THR268_110
H8 NPTH2.7_2.2 NPTH106X087
H22 NPTH2.2 NPTH087
H4 NPTH2.7_2.2 NPTH106X087

EMI/ Moat CAP

B+ — EC1 1 2 0.1u/25V_0603 NA — 5V
3.3VS — EC8 1 2 0.1u/10V NA; EC13 1 2 0.1u/10V NA — 5V
3.3VS — EC101 1 2 0.1u/10V NA; EC100 1 2 0.1u/10V NA — 3.3VSTBY
1.1VS — EC112 1 2 0.1u/10V NA — VGA_1.5VS
3.3VS — EC15 1 2 0.1u/10V; EC21 1 2 0.1u/10V; EC65 1 2 0.1u/10V; EC66 1 2 0.1u/10V
3.3VS — EC4 1 2 0.1u/25V_0603 NA; EC2 1 2 0.1u/25V_0603 — B+
1.1VS — EC16 1 2 0.1u/10V; EC17 1 2 0.1u/10V; EC108 1 2 0.1u/10V
3.3VS — EC20 1 2 0.1u/10V NA; EC19 1 2 0.1u/10V NA — 1.1VS
1.1VS — C17 1 2 0.1u/10V; C22 1 2 0.1u/10V; C178 1 2 0.1u/10V
1.1VS — EC32 1 2 0.1u/10V NA; EC27 1 2 0.1u/10V NA — VGA_1.5VS
1.5V — EC12 1 2 0.1u/10V; EC6 1 2 0.1u/10V; EC11 1 2 0.1u/10V; EC5 1 2 0.1u/10V; EC10 1 2 0.1u/10V; EC7 1 2 0.1u/10V
5V — EC142 1 2 0.1u/10V; EC122 1 2 0.1u/10V; EC120 1 2 0.1u/10V NA; EC143 1 2 0.1u/10V; EC144 1 2 0.1u/10V; EC146 1 2 0.1u/10V; EC147 1 2 0.1u/10V; EC18 1 2 0.1u/10V
1.1VS — EC34 1 2 0.1u/10V NA
3.3VSTBY — EC56 1 2 0.1u/10V NA
B+ — EC22 1 2 0.1u/25V_0603; EC42 1 2 0.1u/25V_0603; EC50 1 2 0.1u/25V_0603; EC51 1 2 0.1u/25V_0603; EC55 1 2 0.1u/25V_0603; EC52 1 2 0.1u/25V_0603; EC53 1 2 0.1u/25V_0603; EC54 1 2 0.1u/25V_0603; EC62 1 2 0.1u/25V_0603; EC64 1 2 0.1u/25V_0603; EC63 1 2 0.1u/25V_0603
+CPU_PWR_SRC — EC140 1 2 0.1u/25V_0603; EC141 1 2 0.1u/25V_0603
5V_USB — EC35 1 2 0.1u/10V NA
1.5V_SRC — EC38 1 2 0.1u/10V NA

FID

FID1 FIDUCIAL CAD-016 NC, NO CONNECT TO ANY.
FID2 FIDUCIAL CAD-016 NC, NO CONNECT TO ANY.
FID3 FIDUCIAL CAD-016 NC, NO CONNECT TO ANY.
FID4 FIDUCIAL CAD-016 NC, NO CONNECT TO ANY.
FID5 FIDUCIAL CAD-016 NC, NO CONNECT TO ANY.
FID6 FIDUCIAL CAD-016 NC, NO CONNECT TO ANY.
FID7 FIDUCIAL CAD-016 NC, NO CONNECT TO ANY.
FID8 FIDUCIAL CAD-016 NC, NO CONNECT TO ANY.

FLEXComputing

Project Name : H510UA1	Title : Screw Hole/ EMI/ Unused
Size :	Document Number : HPMH-40GAB6300-D — Rev : D
Date: Thursday, December 30, 2010	Sheet : 48 of 51

Item	Fixed Issue	Reason for Change	Rev	PG#	Modify List	B Ver#	Phase
1	Rev. A Schematic released	Rev. A Schematic released	A			A0	DB
2	Modify F1 to smaller package	Modify F1 to smaller package	B	26	Modify F1 package to "FUSE-3L4X1W8X1H".	B0	SI
3	Add resistor for CPU test point resistor.	Add resistor for CPU test point resistor.	B	2	Add R514 for 80.6 ohm.	B0	SI
4	Add thermal sensor for NB thermal diode	Prevent N/B thermal break down	B	8, 30	Add RJ105, RJ106 and C772 to seperate DGPU& NB thermal signal.	B0	SI
5	Add DGPU CRT DDC source	Add DGPU CRT DDC channel for DDC6	B	16	Add U104 DDC channel test PAD (P27, P26) of pin AJ30, AJ31 (DDC6)	B0	SI
6	Modify CRT damping components.	Improve re-work performance	B	26	Modify JS102, JS103, JS104, JS7, JS9, JS10, JS11 to R233, R234, R235, R236, R237, R238, R239	B0	SI
7	Shift LAN transformer pin signal	Correct LAN transformer pin-out	B	32	Shift U107 pin-out to meet transformer spec	B0	SI
8	Update LAN 25M net-name	Correct LAN 25M for reserved signal.	B	32	Modify LAN 25M clock from S/B and named "LAN_25M_IN_SB"	B0	SI
9	Modify USB3.0 clock request signal	Modify USB3.0 clock request signal	B	33	Delete D7 for USB 3.0 clock request work properly	B0	SI
10	Reduce CPU/ DGPU screw hole size	To meet BGA& Screw hole keeping 3mm.	B	48	Reduce H5, H6, H12, H3 (CPU), H10, H11, H15, H16 (DGPU) to 7B4.8_3.8 mm	B0	SI
11	Prevent leakage current& fine-tune PWR seq	Prevent leakage current& fine-tune PWR seq	B	34, 39, 44, 45, 46	1. Modify R423 pin 1 to 3.3VSTBY 2. Leave C25 as empty for 1.1V seq 3. Modify R44 to 200K ohm 1% for 3.3VSTBY_SB seq. 4. Add R240, R241 for waveform improve 5. Add R519, R520 to Audio SM bus reserved. 6. Modify PR118 to 240Kohm 1% for 1.05VS seq. 7. Modify PR126 to 10Kohm for 1.8VS seq. 8. Modify PR9 to 150Kohm 1% for VCORE seq. 9. Modify PR3 to 100Kohm 1% for 1.1VS seq. 10. Del R82	B0	SI
12	Remove un-used circuit	Remove function by HP requirement	B		Remove Blue tooth& Keyboard bakclight circuit	B0	SI
13	Add KBC External Wake up event	Add KBC External Wake up event	B	13, 29	Add D6 and make link "SIO_EXT_WAKE#" from U5 pin 117 to U111 pin H3.	B0	SI
14	Modify components by ME/ height limitation	Modify components by ME/ height limitation	B	11, 28, 35, 37	1. Modify CN_RTC1 to ACES - "50273-0020N", CN2 to ACES - "50273-0020N", CN4 to ACES - "50281-00201", CN_LVDS1 to ACES "50398-04001" 2. Add M119, M120 for TP EN LED& TP Sidelight LED sinker.	B0	SI
15	Modify DGPU power sequence& BACO circuit	To meet DGPU power sequence& BACO required.	B	11, 21, 43	1. Modify U111 pin AH6 as "DGPU_PX_VGA_EN" 2. Modify PR238 to 620K ohm 1%. 3. Add R243, Q14, PQ121, PC246 for VGA_3.3VS gating circuit. 4. Modify VGA_1.5VS enable signal from DGPU_PX_EN to DGPU_PX_VGA_EN. 5. Delete D6 and connect DPGU_PX_MODE to BACO circuit as enable 6. Add D118, D119, D120, PR240, R249, R515, R516, C773, C774, PC130, PQ10, PQ11, PQ12, PQ13 for VGA PWR Seq. 7. Add JP3, JP4 for BACO mode reserved. 8. Add D121, R250, PQ9, PQ11, PQ12, R242 for DGPU_BACO PWROK seq. 9. Modify DGPU_PERST# from DGPU_PX_GPIO0 and PCIE_RST# combined. Or shorted by RJ100B from DGPU_GPIO0. 10. Modify entire 3.3VS of DGPU to VGA_3.3VS. 11. Update PCIE_RST#0 reset source.	B0	SI
16	DFB update	DFB update improvement (Factory)	B	26	Modify D101 to 1N5819HW-7-F.	B0	SI
17	X'tal accuracy modify	X'tal accuracy modify	B	11	1. Modify C704, C719 to 27pF for 32.768M Hz	B0	SI
18	Seperate PCI_WAKE# from different power source	Seperate PCI_WAKE# from different power source	B	11	Add D123, R200 and pull-high to 3.3V_LAN	B0	SI
19	Add transistor for LED sinker	Add transistor for LED sinker	B	28	Add M119& M120 for LED power sinker.	B0	SI
20	Update thermal circuit	Update thermal circuit	B	30	1. Add RJ105, RJ106, R247 for DGPU& NB thermal diode switch circuit. 2. Delete R23, R25, R30, R37, R38, R42, R43, C94, D1, D2, M5, M6, Q9.	B0	SI
21	Update USB3.0 solution to NEC	Update USB3.0 solution to NEC by HP required.	B	33	Modify USB3.0 soultion to NEC uDP720200	B0	SI
22	Audio circuit modify (Kevin.Yeh)	Audio circuit modify	B	36, 37	1. Modify R484, R485, R487& R490 to 1.96K ohm 1% 2. Add R517 (10K ohm) and pull-high to "HP_AMP". 3. Add R244, R245, R246, R248, C727, C775 for B+ break down issue.	B0	SI
23	Power circuit modify (Eva.Chao)	Power circuit modify	B	40, 42, 44, 45	1. Modify PR50, PC67 from 1206 to 0805& 0603 package. 2. Modify PC45, PC207 to 220uF/ 6.3V. 3. Leave PC22, PC45& PC61 empty. 4. Add PQ608, PR239 for AC-off funtion. 5. Modify PL8 to PCMC063T-3R3MN 6. Leave PR64 empty and PR53 mouted for charge-pump states. 7. Modify PR102 to 30.1K ohm 1%. 8. Modify PR16 to 10K ohm and Add PC130 for 1.1VS_PWRGD signal quality 9. Modify PC222 for double pulse issue.	B0	SI

Item	Fixed Issue	Reason for Change	Rev	PG#	Modify List	B Ver#	Phase
24	Prevent GPU ACAVIN leakage current	Prevent GPU ACAVIN leakage current	C	16	Add R352& D7 to prevent GPU ACAVIN leakage current.	C0	PV
25	Update USB3.0 circuit	Update USB3.0 circuit	C	33, 34	1. Add R263, R264& M125 for USB3.0 Wake up event. 2. Add R262& D123 for USB3.0 reset timing issue. 3. Modify L26 to package 0603 for parts lead time issue. 4. Correct Analog& Digital power source 5. Add R261 for SMI BOM option 6. Delete M17 and update power switch circuit. 7. Update U16 footprint	C0	PV
26	KBC SLP_S5# signal setting	KBC SLP_S5# signal setting	C	29	Add R165 to setting SLP_S5# GND level	C0	PV
27	Logo LED broken issue	Logo LED module didn't have current limit resistor	C	24	Add R335 for Logo LED current limit	C0	PV
28	Zero power ODD function removal	Zero power ODD function removal	C	27	Leave C652, M108, M109, Q105, Q106, R419, R424& R452 empty for Zero Power ODD function removal.	C0	PV
29	EEPROM WP#	Add EEPROM WP# from EC	C	29	Add EC pin 81 as EEPROM WP# signal for EEPROM Write Protection.	C0	PV
30	NEC USB3.0 device dispear issue	Fine-tune NEC USB3.0 power up seq	C	33	1. Add C94 for NEC uPD700200A global reset timing fine-tune 2. Add R259 as empty for CLKREQ external pull-high	C0	PV
31	GPU thermal trip normal operation status	Set GPU thermal trip normal operation status	C	2, 29	1. Add R423 for GPU thermal trip normal operation status 2. Add Q108 for CPU processor hot	C0	PV
32	Hall sensor sense issue	Hall sensor can't work fine	C	28, 38	Modify SW100, C510 to D/B and modify CN_PBTN1 to 8 pin to meet M.E. modify	C0	PV
33	PX mode GPU thermal sensor fail	EC can't check GPU thermal status	C	2, 21, 29 30	1. Remove Q101, R303 remove CPU thermal alert. 2. Add R268 pull-high at alert of thermal sensor. 3. Connect DGPU_PX_VGA_EN to EC for PX mode indicates. 4.Add Q109, R181 for thermal sensor leakage issue	C0	PV
34	Stage ID indicate	Indicate SI/ PV stage for SW	C	12	Add R461 for Stage ID (Deflaut internal PU: H-SI, L-PV)	C0	PV
35	Power seq fine-tune	Power seq fine-tune	C	33, 43	1. Modify PR801 to 100K_F for USB3.0 chip power seq 2. Modify R336, PR232 to 100K_F for VGA power seq	C0	PV
36	Power circuit modify (Staley Chiu)	Power circuit modify	C	41, 43, 44, 45, 46	1. PL8 change to 4R7 2. Leave PR66 as empty 3. PR81/ PR81 change to 22K/ 34.8K for USB port load issue 4. PR79 change to 54.9k for VRAM load issue 5. PR104 change to 30K for AMD VID Updated 6. PR100 change to 44.2k for AMD VID Updated 7. Modify MAX/OCP current text 8. Update VID table 9. PC114 change to 10u/10v0805 for Phase/Gain 10. PC222 change to 330u/2v for double purse 11. PC60 change to Panasonic source (use the same source with others) 12. Add PC247, PC248/ 68uF/25V for closing acoustic noise 13. PC115 change to 10u/10v0805 for Phase/Gain 14. PC121 change to 10u/10v0805 for Phase/Gain 15. Delete PJP114	C0	PV
37	RFI solution (Hank Tsai)	RFI solution	C	11	Modify C442, C448 to 10pF as mounted.	C0	PV
38	EMI solution (PV - Benson Ni)	Update EMI solution	C	30, 37, 38, 39, 40, 41, 42, 45, 46, 48	1. Modify CB15,CB16 as mounted. 2. Modify EC37,EC39,EC41,EC44 as mounted. 3. Modfy EC102,EC104,EC105 as mounted. 4. Add EC110/ 0.1uF bypass caps. Between USB conn pin7 (USB5V_ON) and GND. 5. Add EC139/ 0.1uF bypass caps.Between CN_ADP1 pin 5 and GND. Modify C500 as mounted. 6. Add EC138/ 0.1uF bypass caps. between 5VSTBY_SRC and GND. 7. Add EC57/ 0.1uF bypass caps. between 1.5V_SRC and GND. 8. Add EC45/ 0.1uF bypass caps. between CPU_VDDNB and GND. Add EC59/ 0.1uF bypass caps. between +CPU_PWR_SRC and GND. 9. Add EC60, EC61/ 0.1uF bypass caps. between 1.5VS and GND. 10. Modify EC5,EC6,EC7,EC10,EC11,EC12,EC108,EC122 as mounted. Add EC62, EC63, EC64/ 0.1uF bypass caps. between B+ and GND. Add EC65/ 0.1uF bypass caps. between 3.3VS and GND. Delete EC111,EC25,EC23,EC24,EC26,EC33,EC35,EC109,EC110,EC45,EC38.	C0	PV
39	ESD solution (PV - Stone Wang)	Update ESD solution	C	35, 36	1. EL1, EL2 from Bead 120ohm change to the Resistor 300ohm. 2. EC36, EC40 change to mounted. 3. Add a Varistor ED10 between CN_MIC1 pin5 and Net AGND. 4. ED3, ED4 change to 0603 Varistors. 5. Add a Varistor ED11 between CN_PHONE1 pin5 and Net AGND. 6. ED6, ED8, ED104, ED106 change to 0603 Varistors. 7. ED5, ED7, ED9, ED108 change to 0603 Varistors and keep them as empty	C0	PV

Item	Fixed Issue	Reason for Change	Rev	PG#	Modify List	B Ver#	Phase
40	RTC accurcy update (BOM)	RTC accurcy update	D	11	Modify C704& C719 to 22pF and 18pF.	D0	MV
41	Prevent adaptor level fail (Power)	Prevent adaptor level fail	D	40	Modify PR89 to 422Kohm 1%	D0	MV
42	Prevent leakage current from CRT	Prevent leakage current from CRT	D	26	Add R23 as 10Kohm to prevent leakage cuurent from CRT	D0	MV
43	Fine-tune LED brightness (BOM)	Fine-tune LED brightness by HP ID	D	29	1. Modify R399 to 590ohm 1% for RF on LED 2. Modify R401 to 240ohm 1% for RF off LED 3. Modify R404 to 1.27Kohm 1% for CAP lock LED 4. Modify R405 to 240ohm 1% for MUTE LED 5. Modify PR209 to 715ohm 1% for Charger LED	D0	MV
44	S5 wake-up event leakage issue (BOM)	Prevent leakage current from pull-high resistor	D	29	Leave R356, R361 as empty to prevent it.	D0	MV
45	DFX report improvement	Meet Factory DFX checking	D	45	Modify PJP100 to Normal close footprint	D0	MV
46	EMI solution improvement	EMI solution improvement	D	48	1. Modify EC15 from between 3.3VS& 5V to 3.3VS& GND 2. Modify EC18 from between 3.3VS& 5V to 5V& GND 3. Modify EC2 from between 3.3VS& B+ to B+& GND 4. Add EC35, EC38, EC66, EC140, EC141, EC142, EC143, EC144, EC146, EC147, EC148	D0	MV