Jones/Cujo BLOCK DIAGRAM

01

PCB STACK UP

8L Dis.

- LAYER 1 : TOP
- LAYER 2 : SGND
- LAYER 3 : IN2
- LAYER 4 : SGND1
- LAYER 5 : SVCC
- LAYER 6 : IN2
- LAYER 7 : SGND2
- LAYER 8 : BOT

Cable Docking PAGE 36
- VGA
- RJ-45
- CIR/Pwr btn
- SPDIF Out
- Stereo MIC
- Headphone Jack
- USB Port
- VOL Cntr

- SYSTEM CHARGER(ISL6251AHAZ-T) PAGE 37
- SYSTEM POWER ISL6237IRZ-T PAGE 38
- DDR II SMDDR_VTERM 1.8V/1.8VSUS(TPS51116REGR) PAGE 42
- VCCP +1.5V AND GMCH 1.05V(RT8204) PAGE 39
- VGACORE(1.025V)Oz8119 PAGE 41
- CPU CORE ISL6262A PAGE 40

CPU Penryn
478P (uPGA)/35W
PAGE 3,4

CPU THERMAL SENSOR PAGE 4

FSB 667/800/1066

14.318MHz

CLOCK GEN
ALPRS355B MLF64PIN
PAGE 2

CLK_CPU_BCLK, CLK_CPU_BCLK#
CLK_MCH_BCLK, CLK_MCH_BCLK#
DREFCLK, DREFCLK#
DREFSSCLK, DREFSSCLK#

NORTH BRIDGE
Cantiga
PM45,GM45
PAGE 5~9

Level Shift PAGE 20

27MHz

DDRII-SODIMM1 PAGE 10 — DDRII 667/800 MHz

DDRII-SODIMM2 PAGE 10 — DDRII 667/800 MHz

PCI-Express 16X

nVIDIA
NB9M-GE 64 Bit
NB9P-GS 128 Bit
PAGE 12~18
969p

Dual Link

HDMI CON PAGE 20

CRT PAGE 20

LCD CONN PAGE 19

Mini PCI-E Card x2
Express Card x1
Cable Docking x1
4,7,10,11

DMI LINK

32.768KHz

NBSRCCLK, NBSRCCLK#

SOUTH BRIDGE
ICH9-M
PAGE 21,22,23,24

SATA - HDD PAGE 32 — SATA0 150MB

SATA - CD-ROM PAGE 32 — SATA1 150MB

SATA - 2ndHDD PAGE 32 — SATA4 150MB

E-SATA PAGE 29 — SATA5 150MB

Accelerometer LIS3LV02DL PAGE 27 — SMBUS

USB2.0

0,1,8,9 — **USB2.0 Ports X4** PAGE 29

5 — **BlueTooth** PAGE 29

3 — **Webcam** PAGE 29

2 — **Fingerprint** PAGE 29

PCI-E

24.576Hz

Azalia

X2 — **Mini PCI-E Card** (Wireless LAN/TV) PAGE 35

X1 — **LAN** Realtek PCIE-LAN RTL8102E/8111C (10/100/GagaLAN) PAGE 30,31

X1 — **Express Card** (NEW CARD) PAGE 32

X1 — **JMICRO 380 for Discrete** PAGE25

Analog IDT92HD75B3 PAGE 26

MDC CONN PAGE 33

32.768KHz

LPC

ENE KBC
KB3926 C0
PAGE 34

Keyboard PAGE 33
Touch Pad PAGE 34

Capacitive Sense SW PAGE 33

SPI PAGE 22

AUDIO Amplifier TPA6047 PAGE 27

AUDIO Amplifier TPA3007D1 PAGE 28

25MHz

RJ45 PAGE 30

IEEE1394 connect for Discrete only PAGE 25

Memory CardReader PAGE 25

microphone PAGE 28

Audio Jacks (Phone/ MIC) PAGE 28

Jack to Speaker PAGE 27

Jack to Sub-Woofer PAGE 28

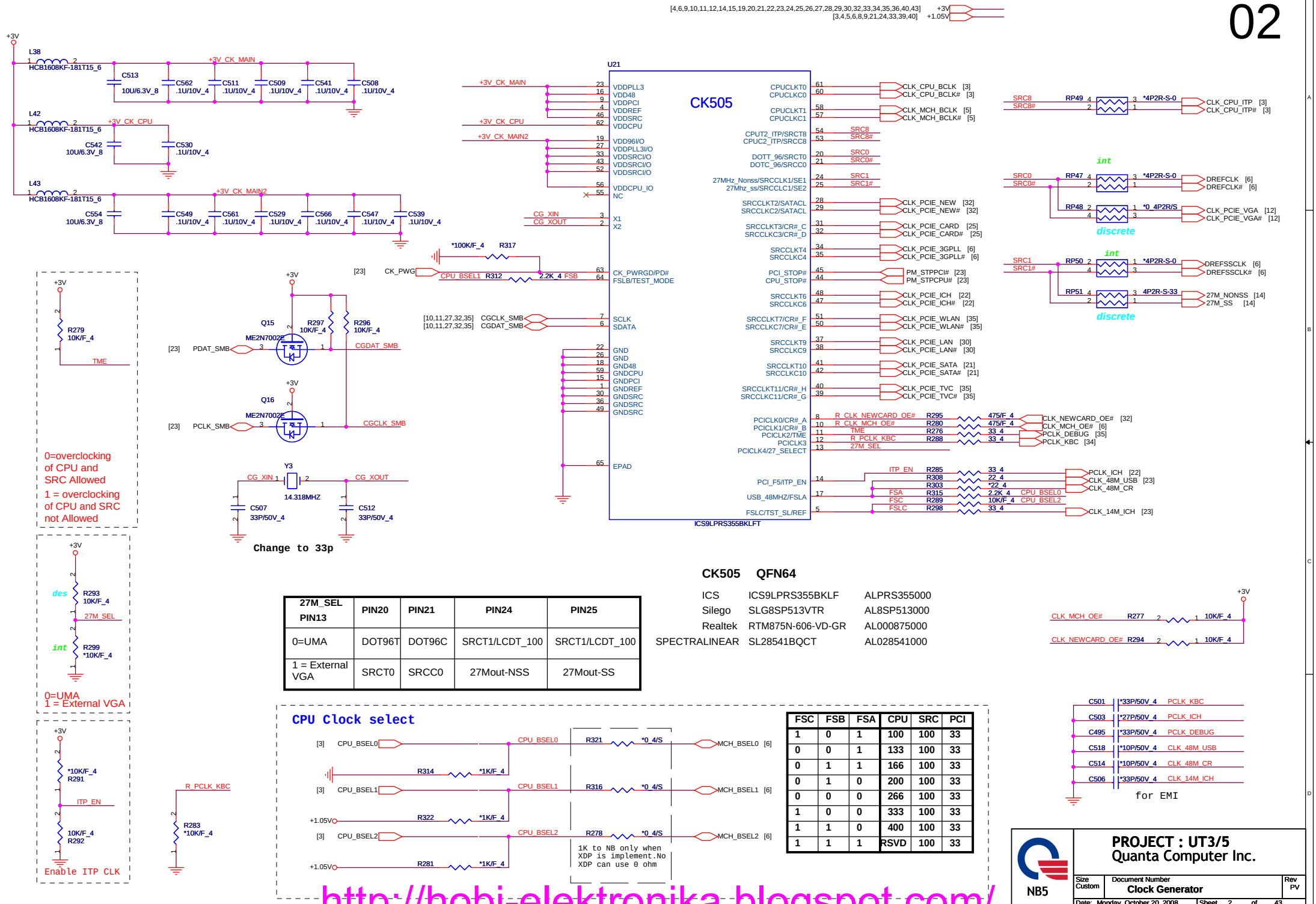
GMT G9931P1U
FAN PAGE 36

SPI PAGE 34

PROJECT : UT3/5
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	Block Diagram	PV
Date: Monday, October 20, 2008	Sheet 1 of 43	



27M_SEL PIN13	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100
1 = External VGA	SRCT0	SRCC0	27Mout-NSS	27Mout-SS

CK505 QFN64

ICS	ICS9LPRS355BKLF	ALPRS355000
Silego	SLG8SP513VTR	AL8SP513000
Realtek	RTM875N-606-VD-GR	AL000875000
SPECTRALINEAR	SL28541BQCT	AL028541000

FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

NB5

PROJECT : UT3/5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Clock Generator	PV

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U34A

ADDR GROUP_0

ADDR GROUP_1

CONTROL

XDP/ITP SIGNALS

THERMAL

MISC

H CLK

Quard Core Only

Penryn Ball-out Rev 1a

U34B

DATA GRP 0

DATA GRP 2

DATA GRP 1

DATA GRP 3

Penryn Ball-out Rev 1a

For QC CPU

For QC CPU

For QC CPU

For QC CPU

For QC CPU

	Rc
Dual Core	2K Ohm
Quard Core	1.74K Ohm

	COMP0/2	COMP1/3
Dual Core	27.4 Ohm (CS02742FB19)	54.9 Ohm (CS05492FB19)
Quard Core	24.9 Ohm (CS02492FB29)	49.9 Ohm (CS04992FB31)

MODEL	UT5 Quad Core	UT3 Dual Core
R28	*0_4	0_4

R542 -->1.74K for Quad Core

Add R61

DB modified

For QC Support

Don't install for DC

Change to +5V

Populate ITP700Flex for bringup

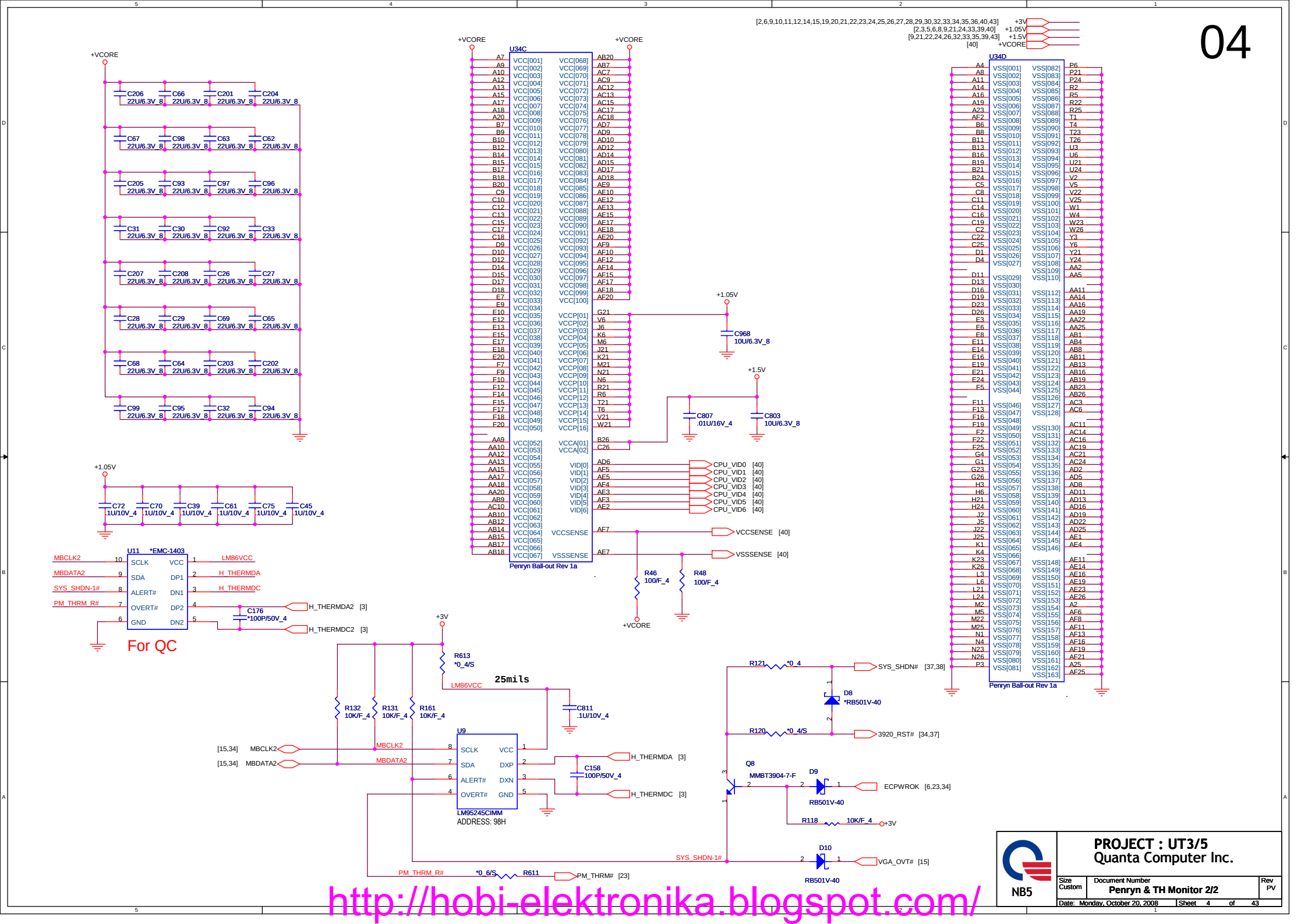
*ITP700Flex

PROJECT : UT3/5
Quanta Computer Inc.

NB5

Size: Custom | Document Number: Penryn 1/2 | Rev: PV

Date: Monday, October 20, 2008 | Sheet 3 of 43


04
+VCORE
C206 22U/6.3V_8
C66 22U/6.3V_8
C201 22U/6.3V_8
C204 22U/6.3V_8
C67 22U/6.3V_8
C98 22U/6.3V_8
C63 22U/6.3V_8
C62 22U/6.3V_8
C205 22U/6.3V_8
C93 22U/6.3V_8
C97 22U/6.3V_8
C96 22U/6.3V_8
C31 22U/6.3V_8
C30 22U/6.3V_8
C92 22U/6.3V_8
C33 22U/6.3V_8
C207 22U/6.3V_8
C208 22U/6.3V_8
C26 22U/6.3V_8
C27 22U/6.3V_8
C28 22U/6.3V_8
C29 22U/6.3V_8
C69 22U/6.3V_8
C65 22U/6.3V_8
C68 22U/6.3V_8
C64 22U/6.3V_8
C203 22U/6.3V_8
C202 22U/6.3V_8
C99 22U/6.3V_8
C95 22U/6.3V_8
C32 22U/6.3V_8
C94 22U/6.3V_8
+1.05V
C72 .1U/10V_4
C70 .1U/10V_4
C39 .1U/10V_4
C61 .1U/10V_4
C75 .1U/10V_4
C45 .1U/10V_4
U11 *EMC-1403
MBCLK2
MBDATA2
SYS_SHDN-1#
PM_THRM_R#
SCLK
SDA
ALERT#
OVERT#
GND
VCC
DP1
DN1
DP2
DN2
LM86VCC
H_THERMDA
H_THERMDC
C176 *100P/50V_4
H_THERMDA2 [3]
H_THERMDC2 [3]
For QC
U34C
Penryn Ball-out Rev 1a
VCCP[01]
VCCP[02]
VCCP[03]
VCCP[04]
VCCP[05]
VCCP[06]
VCCP[07]
VCCP[08]
VCCP[09]
VCCP[10]
VCCP[11]
VCCP[12]
VCCP[13]
VCCP[14]
VCCP[15]
VCCP[16]
VCCA[01]
VCCA[02]
VID[0]
VID[1]
VID[2]
VID[3]
VID[4]
VID[5]
VID[6]
VCCSENSE
VSSSENSE
C968 10U/6.3V_8
C807 .01U/16V_4
C803 10U/6.3V_8
CPU_VID0 [40]
CPU_VID1 [40]
CPU_VID2 [40]
CPU_VID3 [40]
CPU_VID4 [40]
CPU_VID5 [40]
CPU_VID6 [40]
VCCSENSE [40]
VSSSENSE [40]
R46 100/F_4
R48 100/F_4
U34D
Penryn Ball-out Rev 1a
+3V
+1.05V
+1.5V
R613 *0_4/S
25mils
C811 .1U/10V_4
R132 10K/F_4
R131 10K/F_4
R161 10K/F_4
U9
LM95245CIMM
ADDRESS: 98H
[15,34] MBCLK2
[15,34] MBDATA2
H_THERMDA [3]
H_THERMDC [3]
C158 100P/50V_4
R121 *0_4
R120 *0_4/S
D8 *RB501V-40
SYS_SHDN# [37,38]
3920_RST# [34,37]
Q8 MMBT3904-7-F
D9 RB501V-40
ECPWROK [6,23,34]
R118 10K/F_4
D10 RB501V-40
VGA_OVT# [15]
SYS_SHDN-1#
PM_THRM_R#
*0_6/S
R611
PM_THRM# [23]
PROJECT : UT3/5
Quanta Computer Inc.
NB5
Size Custom
Document Number
Penryn & TH Monitor 2/2
Rev PV
Date: Monday, October 20, 2008
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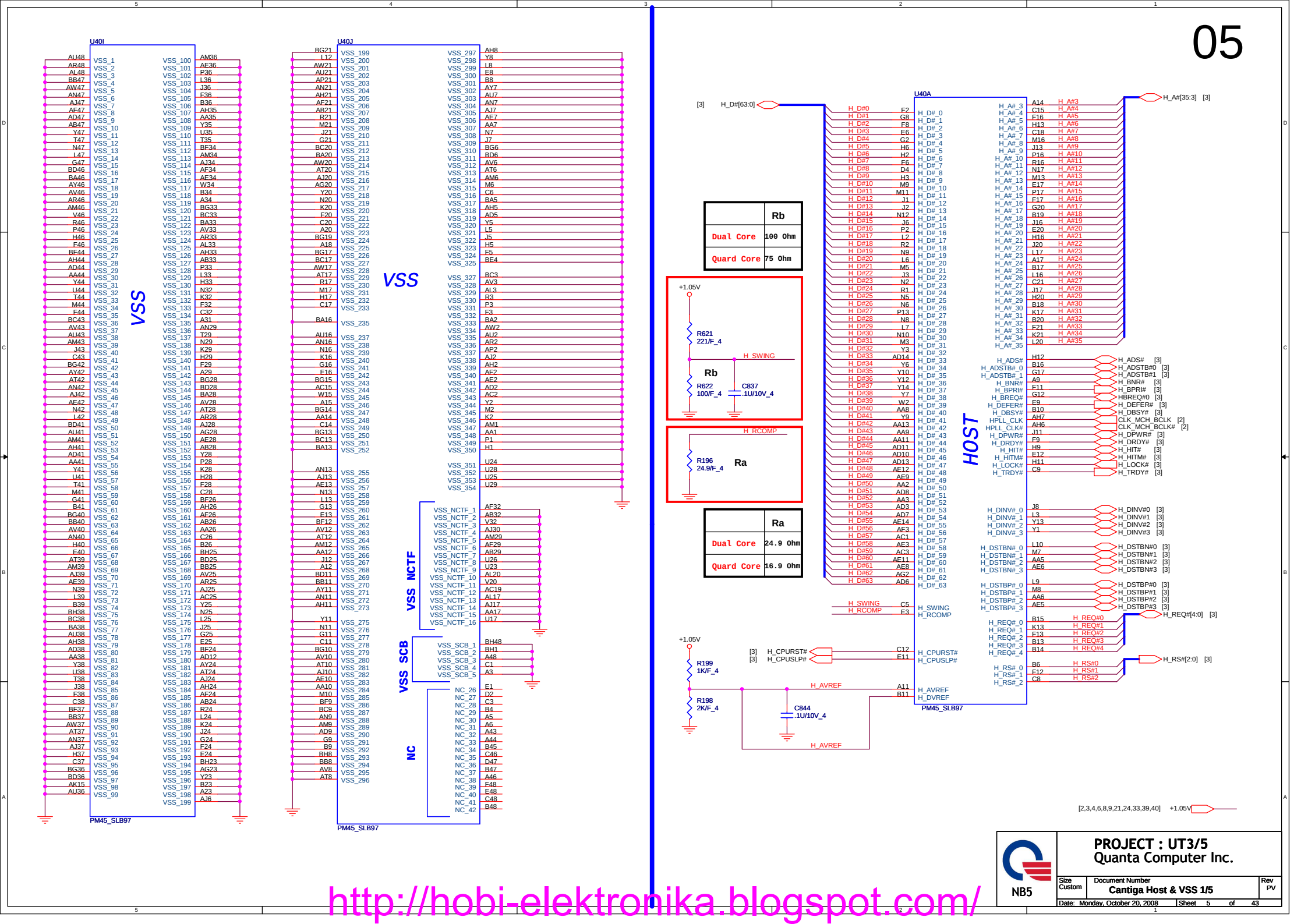
http://hobi-elektronika.blogspot.com/



MCH_CFG_5 DMIx2 selection
Low = DMI X2
High = DMI X4 (Default)

MCH_CFG_16 FSB Dynamic ODT
Low = Dynamic ODT disabled
High = Dynamic ODT enabled (default)

MCH_CFG_9 PCI Express Graphic Lane
Low: Reverse Lane
High: Normal operation(Default)

MCH_CFG_19 DMI Lane Reversal
Low = Normal operation (Default)
High = Reverse Lanes

MCH_CFG_6 iTPM Host Interface
Low =The iTPM Host Interface is enabled2
High = The iTPM Host Interface is disabled (default)

MCH_CFG_7 Intel (R) Management Engine Crypto
Low: Intel (R) Management Engine Crypto
TLS cipher suite with no confidentiality
High: Intel (R) Management Engine Crypto
TLS cipher suite with no confidentiality (Default)

MCH_CFG_10 PCIe Lookback Enable
Low = Enabled3
High: Disabled (Default)

MCH_CFG_12/13 XOR/ALLZ/CLOCK Un-gating

MCH_CFG_13	MCH_CFG_12	Configuration
0	0	Reserved
1	0	XOR Mode enabled
0	1	All-Z Mode enabled
1	1	Normal operation (Default)

MCH_CFG_20

Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE
Low = Only digital display port (SDVO/DP/iHDMI) or PCIE is operational (default)

High = Digital display port (SDVO/DP/iHDMI) and PCIE are operating simultaneously via the PEG port

MCH_CFG2:0

000 = FSB1066
010 = FSB800
011 = FSB667
Others = Reserved

U40B

RSVD
RSVD1 RSVD2 RSVD3 RSVD4 RSVD5 RSVD6 RSVD7 RSVD8 RSVD9 RSVD14 RSVD15 RSVD16 RSVD17 RSVD20 RSVD22 RSVD23 RSVD24 RSVD25

DDR CLK/ CONTROL/COMPENSATION
SA_CK_0 SA_CK_1 SB_CK_0 SB_CK_1 SA_CK#_0 SA_CK#_1 SB_CK#_0 SB_CK#_1 SA_CKE_0 SA_CKE_1 SB_CKE_0 SB_CKE_1 SA_CS#_0 SA_CS#_1 SB_CS#_0 SB_CS#_1 SA_ODT_0 SA_ODT_1 SB_ODT_0 SB_ODT_1 SM_RCOMP SM_RCOMP# SM_RCOMP_VOH SM_RCOMP_VOL SM_VREF SM_PWROK SM_REXT SM_DRAMRST#
M_A_CLK0 M_A_CLK1 M_B_CLK0 M_B_CLK1 M_A_CLK0# M_A_CLK1# M_B_CLK0# M_B_CLK1# M_A_CKE0 M_A_CKE1 M_B_CKE0 M_B_CKE1 M_A_CS#0 M_A_CS#1 M_B_CS#0 M_B_CS#1 M_A_ODT0 M_A_ODT1 M_B_ODT0 M_B_ODT1
SM_RCOMP_VOH SM_RCOMP_VOL SM_RCOMP SM_RCOMP# +0.9VSMVREF_MCH SW_PWROK_NB SM_REXT TP_SM_DRAMRST#
R219 80.6/F_4 R209 80.6/F_4 R237 10K/F_4 R207 499/F_4 TP34 +1.8VSUS

CLK
DPLL_REF_CLK DPLL_REF_CLK# DPLL_REF_SSCLK DPLL_REF_SSCLK# PEG_CLK PEG_CLK#
DREFCLK DREFCLK# DREFSSCLK DREFSSCLK# CLK_PCIE_3GPLL CLK_PCIE_3GPLL#

ME JTAG
TP36 ME_JTAG_TCK
TP32 ME_JTAG_TDI
TP29 ME_JTAG_TDO
TP28 ME_JTAG_TMS

DMI
DMI_RXN_0 DMI_RXN_1 DMI_RXN_2 DMI_RXN_3 DMI_TXP_0 DMI_TXP_1 DMI_TXP_2 DMI_TXP_3 DMI_TXN_0 DMI_TXN_1 DMI_TXN_2 DMI_TXN_3
DMI_TXN[3:0] DMI_TXP[3:0] DMI_RXN[3:0] DMI_RXP[3:0]

CFG
MCH_BSEL0 MCH_BSEL1 MCH_BSEL2 MCH_CFG_3 MCH_CFG_4 MCH_CFG_5 MCH_CFG_6 MCH_CFG_7 MCH_CFG_8 MCH_CFG_9 MCH_CFG_10 MCH_CFG_11 MCH_CFG_12 MCH_CFG_13 MCH_CFG_14 MCH_CFG_15 MCH_CFG_16 MCH_CFG_17 MCH_CFG_18 MCH_CFG_19 MCH_CFG_20

PM
PM_SYNC# PM_DPRSTP# PM_EXT_TS#_0 PM_EXT_TS#_1 PWROK RSTIN# THERMTRIP# DPRSLPVR
PM_EXTTS#0 PM_EXTTS#1 R201 100/F_4 RST_IN#_MCH

GRAPHICS VID
GFX_VID_0 GFX_VID_1 GFX_VID_2 GFX_VID_3 GFX_VID_4 GFX_VR_EN
GFXVR_VID_0 GFXVR_VID_1 GFXVR_VID_2 GFXVR_VID_3 GFXVR_VID_4 TP66 TP65 TP33 TP31 TP30 TP67

ME
CL_CLK CL_DATA CL_PWROK CL_RST# CL_VREF
CL_CLK0 CL_DATA0 ECPWROK CL_RST#0 MCH_CLVREF 0.35 V R257 1K/F_4 C451 1U/10V_4 R258 499/F_4

MISC
DDPC_CTRLCLK DDPC_CTRLDATA SDVO_CTRLCLK SDVO_CTRLDATA CLKREQ# ICH_SYNC# TSATN#
TP27 TP26 SDVO_CLK SDVO_DATA CLK_MCH_OE# MCH_ICH_SYNC# R200 56.2/F_4

HDA
HDA_BCLK HDA_RST# HDA_SDI HDA_SDO HDA_SYNC ACZ_SDIN3_MCH R638 *0 4/S
ACZ_BITCLK_MCH ACZ_RST#_MCH ACZ_SDIN3 ACZ_SDOUT_MCH ACZ_SYNC_MCH

NC
NC_1 NC_2 NC_3 NC_4 NC_5 NC_6 NC_7 NC_8 NC_9 NC_10 NC_11 NC_12 NC_13 NC_14 NC_15 NC_16 NC_17 NC_18 NC_19 NC_20 NC_21 NC_22 NC_23 NC_24 NC_25 NC_26

PM45_SLB97

ACZ_BITCLK_MCH R634 *33_4 C874 *33P/50V_4

+3V R235 10K/F_4 PM_EXTTS#0 R230 10K/F_4 PM_EXTTS#1

[2,4,9,10,11,12,14,15,19,20,21,22,23,24,25,26,27,28,29,30,32,33,34,35,36,40,43] +3V
[8,9,10,33,39,42] +1.8VSUS
[2,3,4,5,8,9,21,24,33,39,40] +1.05V
[2,3,4,5,8,9,21,24,33,39,40] +1.05V_PEG

U40C

LVDS
L_BKLT_CTRL L_BKLT_EN L_CTRL_CLK L_CTRL_DATA L_DDC_CLK L_DDC_DATA L_VDD_EN LVDS_IBG LVDS_VBG LVDS_VREFH LVDS_VREFL LVDSA_CLK# LVDSA_CLK LVDSB_CLK# LVDSB_CLK LVDSA_DATA#_0 LVDSA_DATA#_1 LVDSA_DATA#_2 LVDSA_DATA#_3 LVDSA_DATA_0 LVDSA_DATA_1 LVDSA_DATA_2 LVDSA_DATA_3 LVDSB_DATA#_0 LVDSB_DATA#_1 LVDSB_DATA#_2 LVDSB_DATA#_3 LVDSB_DATA_0 LVDSB_DATA_1 LVDSB_DATA_2 LVDSB_DATA_3
[15,19] DPST_PWM [15,19] LVDS_BLON R636 *0_4 DPST_PWM_INT R227 *0_4 LVDS_BLON_INT R229 *10K/F_4 L_CTRL_CLK
+3V R236 *10K/F_4 L_CTRL_DATA R640 *0_4 EDIDCLK_INT R239 *0_4 EDIDDATA_INT
[14,15,19] EDIDCLK [14,15,19] EDIDDATA
[15,19] DISP_ON R637 *0_4 DISP_ON_INT R646 *2.37K/F_4 LVDS_IBG TP70 LVDS_VBG LVDS_VREFH
[19] LA_CLK# [19] LA_CLK [19] LB_CLK# [19] LB_CLK
[19] LA_DATAN0 [19] LA_DATAN1 [19] LA_DATAN2 TP69 LA_DATAN3
[19] LA_DATAP0 [19] LA_DATAP1 [19] LA_DATAP2 TP68 LA_DATAP3
[19] LB_DATAN0 [19] LB_DATAN1 [19] LB_DATAN2 TP35 LB_DATAN3
[19] LB_DATAP0 [19] LB_DATAP1 [19] LB_DATAP2 TP37 LB_DATAP3

TV
TVA_DAC TVB_DAC TVC_DAC TV_RTN TV_DCONSEL_0 TV_DCONSEL_1
R211 *0_4 TV_COMP1 R213 *0_4 TV_Y/G1 R212 *0_4 TV_C/R1
Change to 75 ohm to GND
R626 *0_4 TV_DCONSEL0 R628 *0_4 TV_DCONSEL1
Change to 0 ohm to GND

VGA
CRT_BLUE CRT_GREEN CRT_RED CRT_IRTN CRT_DDC_CLK CRT_DDC_DATA CRT_HSYNC CRT_TVO_IREF CRT_VSYNC
[14,20] CRT_B R166 *0_4 CRT_B_1
[14,20] CRT_G R215 *150/F_4 R171 0 CRT_G_1 R221 *150/F_4
[14,20] CRT_R R179 *0_4 CRT_R_1 R217 *150/F_4
[14,20] DDCCLK R226 *0_4 DDCCLK_INT
[14,20] DDCDATA R228 *0_4 DDCDATA_INT
[14,20] HSYNC_COM R216 *33_4 HSYNC_INT R630 *1.02K/F_4 CRTIREF
[14,20] VSYNC_COM R220 *33_4 VSYNC_INT

PM45_SLB97

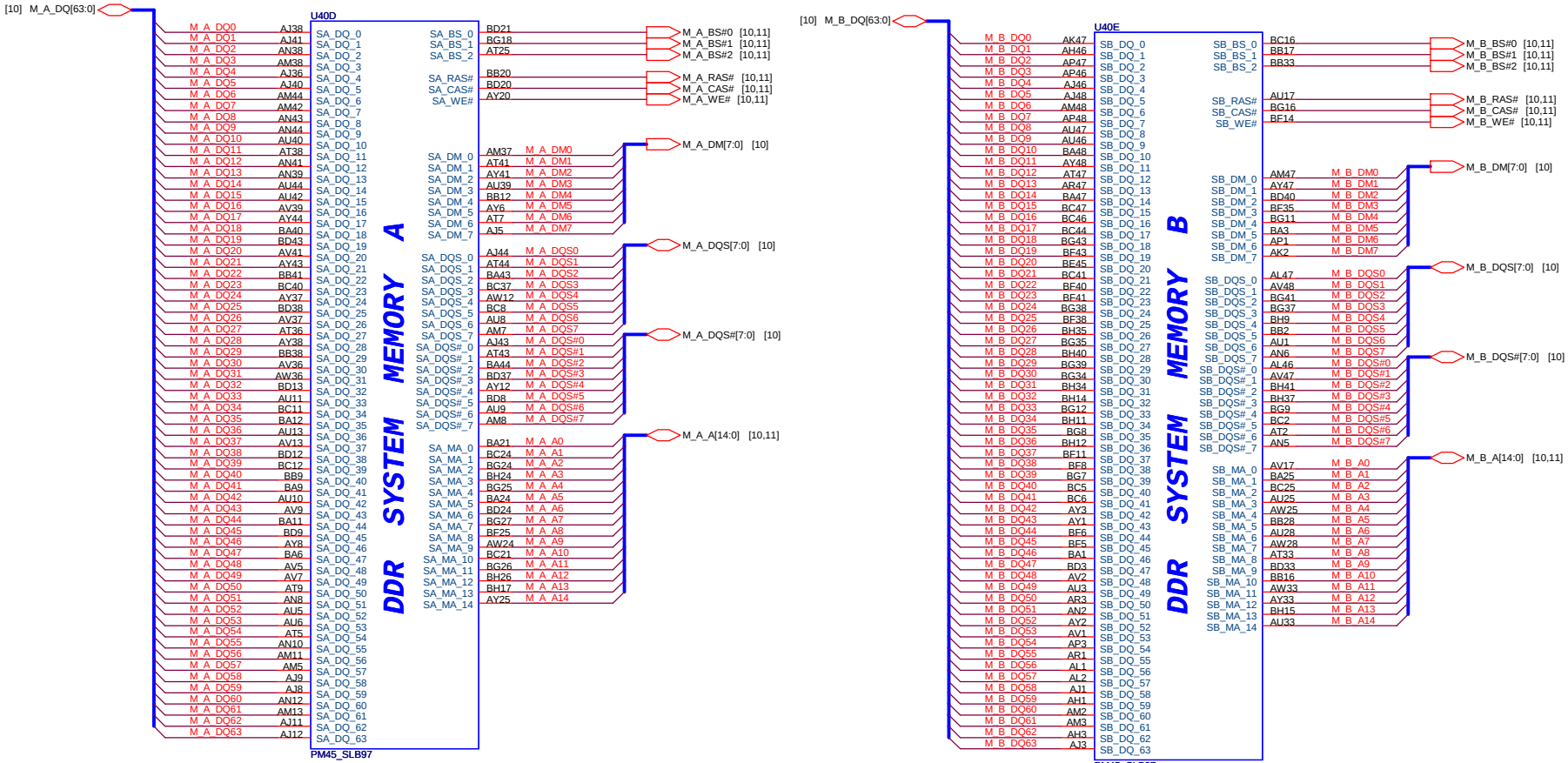
PCI-EXPRESS GRAPHICS
PEG_TX#[15:0] PEG_TX#[15:0] [12]
PEG_TX[15:0] PEG_TX[15:0] [12]
PEG_RX#[15:0] PEG_RX#[15:0] [12]
PEG_RX[15:0] PEG_RX[15:0] [12]
PEG_COMPI PEG_COMPO T37 PEG_COMP R241 49.9/F_4 +1.05V_PEG
PEG_RX#_0 PEG_RX#_1 PEG_RX#_2 PEG_RX#_3 PEG_RX#_4 PEG_RX#_5 PEG_RX#_6 PEG_RX#_7 PEG_RX#_8 PEG_RX#_9 PEG_RX#_10 PEG_RX#_11 PEG_RX#_12 PEG_RX#_13 PEG_RX#_14 PEG_RX#_15
PEG_RX#0 PEG_RX#1 PEG_RX#2 PEG_RX#3 PEG_RX#4 PEG_RX#5 PEG_RX#6 PEG_RX#7 PEG_RX#8 PEG_RX#9 PEG_RX#10 PEG_RX#11 PEG_RX#12 PEG_RX#13 PEG_RX#14 PEG_RX#15
PEG_RX_0 PEG_RX_1 PEG_RX_2 PEG_RX_3 PEG_RX_4 PEG_RX_5 PEG_RX_6 PEG_RX_7 PEG_RX_8 PEG_RX_9 PEG_RX_10 PEG_RX_11 PEG_RX_12 PEG_RX_13 PEG_RX_14 PEG_RX_15
PEG_RX0 PEG_RX1 PEG_RX2 PEG_RX3 PEG_RX4 PEG_RX5 PEG_RX6 PEG_RX7 PEG_RX8 PEG_RX9 PEG_RX10 PEG_RX11 PEG_RX12 PEG_RX13 PEG_RX14 PEG_RX15
int R182 HDMI_HPD# *0_4
PEG_TX#_0 PEG_TX#_1 PEG_TX#_2 PEG_TX#_3 PEG_TX#_4 PEG_TX#_5 PEG_TX#_6 PEG_TX#_7 PEG_TX#_8 PEG_TX#_9 PEG_TX#_10 PEG_TX#_11 PEG_TX#_12 PEG_TX#_13 PEG_TX#_14 PEG_TX#_15
PEG_TX_0 PEG_TX_1 PEG_TX_2 PEG_TX_3 PEG_TX_4 PEG_TX_5 PEG_TX_6 PEG_TX_7 PEG_TX_8 PEG_TX_9 PEG_TX_10 PEG_TX_11 PEG_TX_12 PEG_TX_13 PEG_TX_14 PEG_TX_15
C_PEG_TX#0 C_PEG_TX#1 C_PEG_TX#2 C_PEG_TX#3 C_PEG_TX#4 C_PEG_TX#5 C_PEG_TX#6 C_PEG_TX#7 C_PEG_TX#8 C_PEG_TX#9 C_PEG_TX#10 C_PEG_TX#11 C_PEG_TX#12 C_PEG_TX#13 C_PEG_TX#14 C_PEG_TX#15
C_PEG_TX0 C_PEG_TX1 C_PEG_TX2 C_PEG_TX3 C_PEG_TX4 C_PEG_TX5 C_PEG_TX6 C_PEG_TX7 C_PEG_TX8 C_PEG_TX9 C_PEG_TX10 C_PEG_TX11 C_PEG_TX12 C_PEG_TX13 C_PEG_TX14 C_PEG_TX15
C416 C423 C440 C431 C435 C437 C446 C455 C457 C447 C473 C465 C469 C433 C466 C470 C419 C418 C430 C424 C444 C445 C438 C453 C464 C439 C462 C458 C468 C432 C467 C471
1U/10V_4
PEG_TX#0 PEG_TX#1 PEG_TX#2 PEG_TX#3 PEG_TX#4 PEG_TX#5 PEG_TX#6 PEG_TX#7 PEG_TX#8 PEG_TX#9 PEG_TX#10 PEG_TX#11 PEG_TX#12 PEG_TX#13 PEG_TX#14 PEG_TX#15
PEG_TX0 PEG_TX1 PEG_TX2 PEG_TX3 PEG_TX4 PEG_TX5 PEG_TX6 PEG_TX7 PEG_TX8 PEG_TX9 PEG_TX10 PEG_TX11 PEG_TX12 PEG_TX13 PEG_TX14 PEG_TX15
dis

SM_RCOMP_VOH R225 1K/F_4 C363 01U/16V_4 C356 2.2U/6.3V_6 R222 3.01K/F_4
SM_RCOMP_VOL C386 01U/16V_4 C373 2.2U/6.3V_6 R218 1K/F_4

HP SVTP TEST
+1.8VSUS R253 *1K/F_4 R254 *0_4/S +0.9VSMVREF [10,42] R251 *1K/F_4
+0.9VSMVREF_MCH C426 1U/10V_4 C425 470P/50V_4

For UMA HDMI Function
PEG_TX0 PEG_TX#0 RP58 *4P2R-S-0 IN_D2 IN_D2#
PEG_TX1 PEG_TX#1 RP59 *4P2R-S-0 IN_D1 IN_D1#
PEG_TX2 PEG_TX#2 RP60 *4P2R-S-0 IN_D0 IN_D0#
PEG_TX3 PEG_TX#3 RP61 *4P2R-S-0 IN_CLK IN_CLK#
C416,C423,C440,C431
C419,C418,C430,C424
Need to install for GM
Level: 0.9V
+3V R552 *20K/F_4 HDMI_HPD# [20] HDMI_HPD_CON Q31 *ME2N7002E R550 *7.5K/F_4 R558 *100K/F_4
HPD# Inverting Level Shifting Circuit

PROJECT : UT3/5
Quanta Computer Inc.
Size: Custom | Document Number: Cantiga DMI/DISP 2/5 | Rev: PV
Date: Monday, October 20, 2006 | Sheet 6 of 43

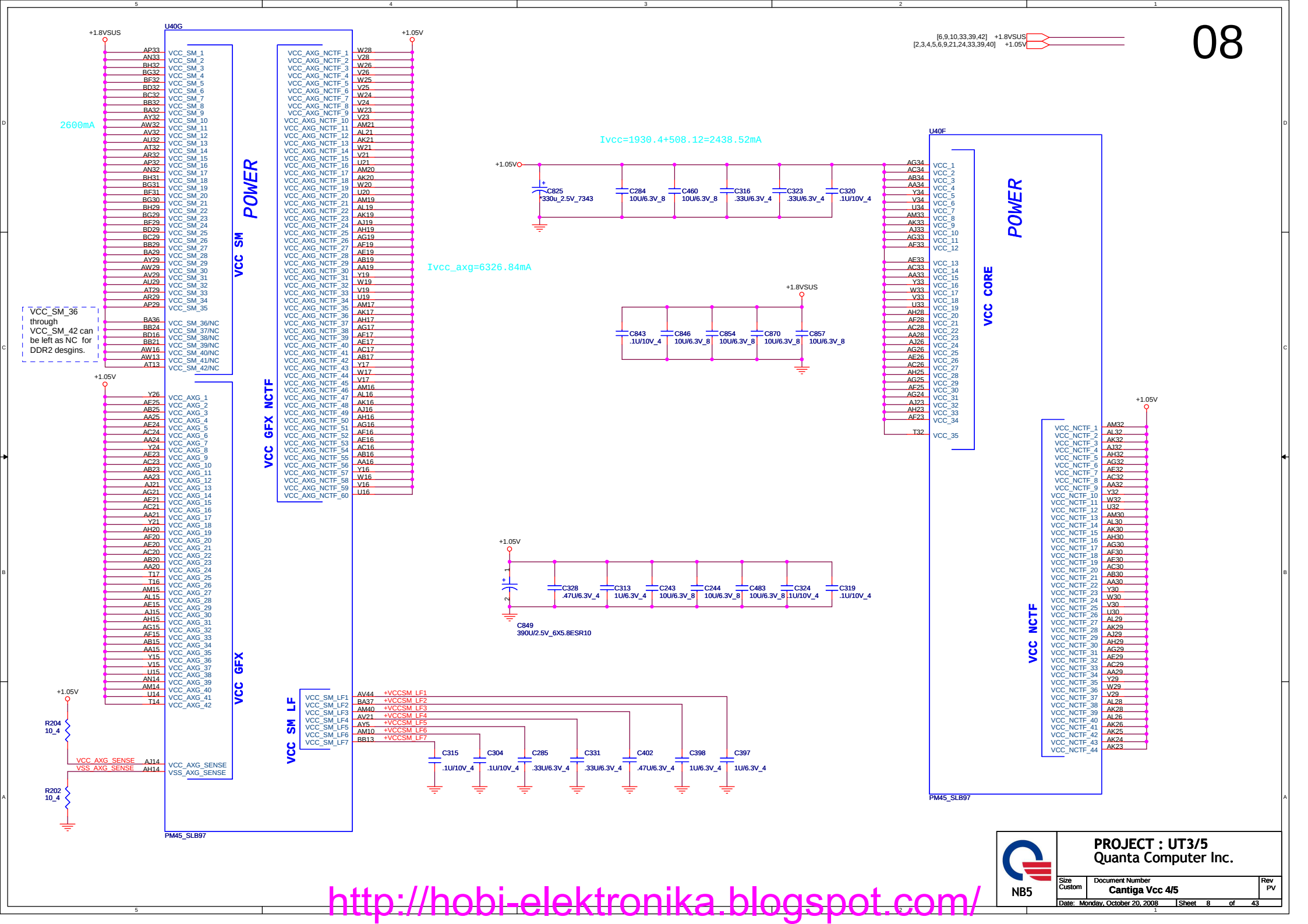


PROJECT : UT3/5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Cantiga DDR2 3/5	PV

Date: Monday, October 20, 2008 Sheet 7 of 43

NB5


08
U40G
U40F
POWER
VCC SM
VCC GFX NCTF
VCC SM LF
VCC GFX
VCC CORE
VCC NCTF
+1.8VSUS
+1.05V
2600mA
Ivcc=1930.4+508.12=2438.52mA
Ivcc_axg=6326.84mA
VCC_SM_36 through VCC_SM_42 can be left as NC for DDR2 desgins.
C825 *330u_2.5V_7343
C284 10U/6.3V_8
C460 10U/6.3V_8
C316 .33U/6.3V_4
C323 .33U/6.3V_4
C320 .1U/10V_4
C843 .1U/10V_4
C846 10U/6.3V_8
C854 10U/6.3V_8
C870 10U/6.3V_8
C857 10U/6.3V_8
C328 .47U/6.3V_4
C313 1U/6.3V_4
C243 10U/6.3V_8
C244 10U/6.3V_8
C483 10U/6.3V_8
C324 1U/10V_4
C319 .1U/10V_4
C849 390U/2.5V_6X5.8ESR10
R204 10_4
R202 10_4
VCC_AXG_SENSE
VSS_AXG_SENSE
C315 .1U/10V_4
C304 .1U/10V_4
C285 .33U/6.3V_4
C331 .33U/6.3V_4
C402 .47U/6.3V_4
C398 1U/6.3V_4
C397 1U/6.3V_4
PM45_SLB97
PM45_SLB97
[6,9,10,33,39,42] +1.8VSUS
[2,3,4,5,6,9,21,24,33,39,40] +1.05V
PROJECT : UT3/5
Quanta Computer Inc.
NB5
Size Custom
Document Number
Cantiga Vcc 4/5
Rev PV
Date: Monday, October 20, 2008
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http://hobi-elektronika.blogspot.com/

+1.05V [2,3,4,5,6,8,21,24,33,39,40]
+3V [2,4,6,10,11,12,14,15,19,20,21,22,23,24,25,26,27,28,29,30,32,33,34,35,36,40,43]
+1.5V [4,21,22,24,26,32,33,35,39,43]
+1.8VSUS [6,8,10,33,39,42]
+1.05V_PEG [2,3,4,5,6,8,21,24,33,39,40]

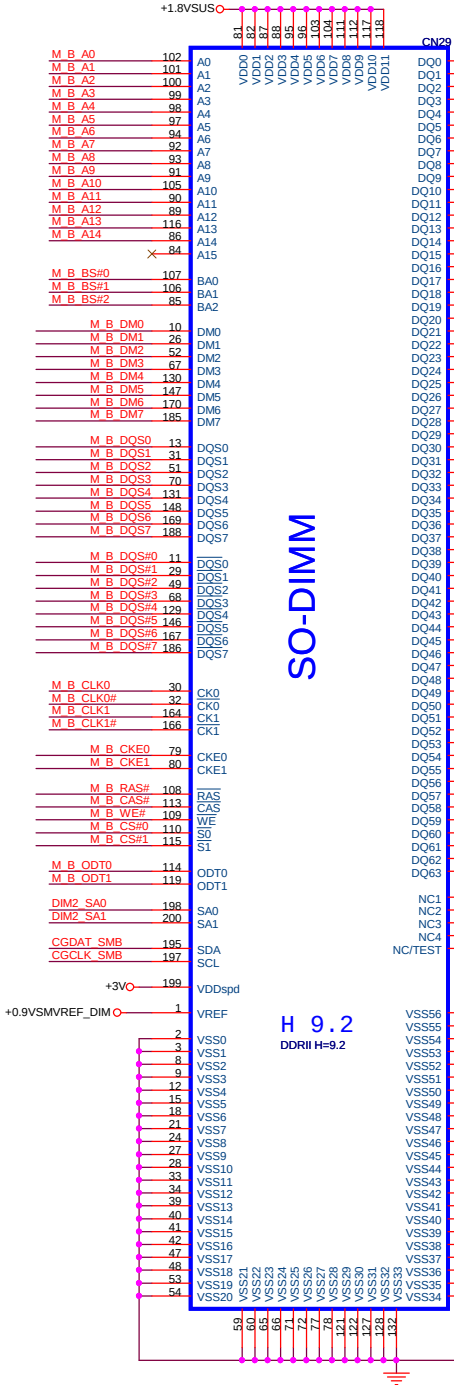
Change to CX000181016(180 ohm,1.5A) as current request
(L21,L22)

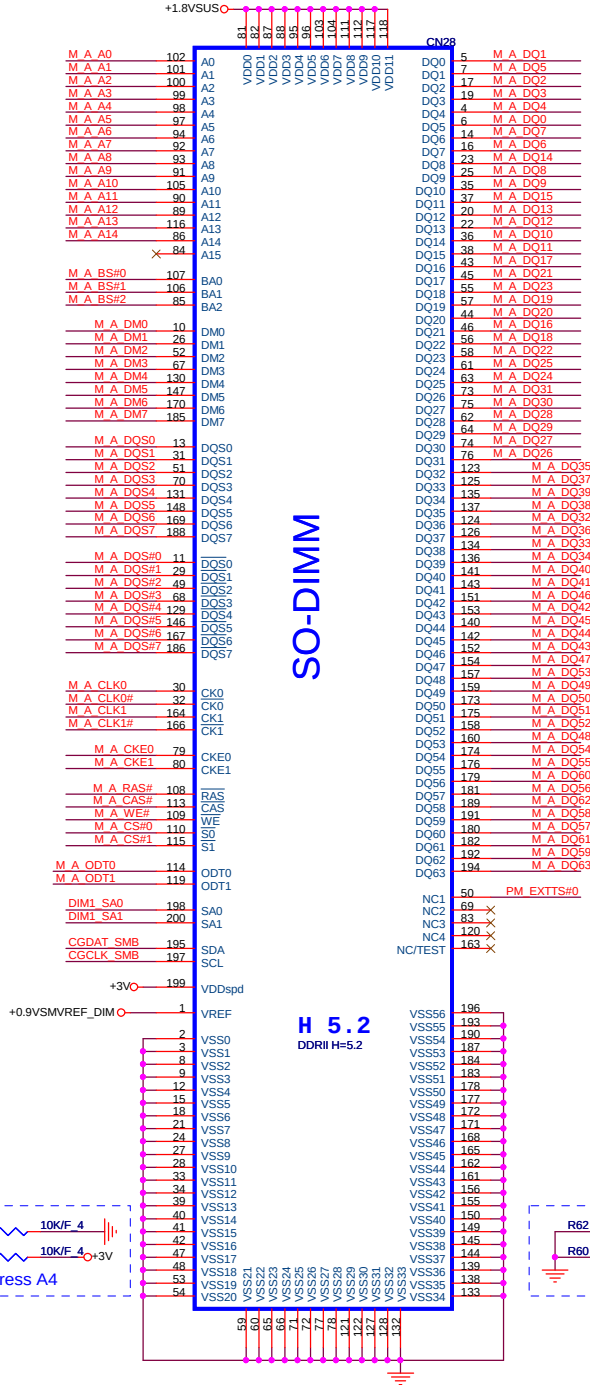
Intel Design Guide 1.5
thermal management is enabled on discrete graphics motherboard

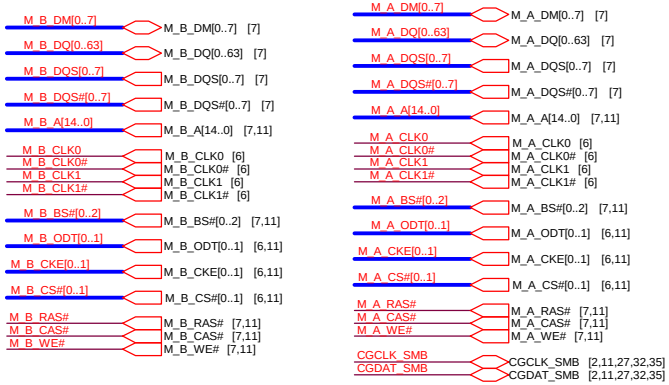
Modify to U40#AF1 power to +1.05V_MPLL as CRB change

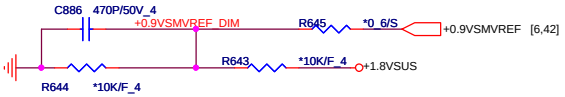
POWER

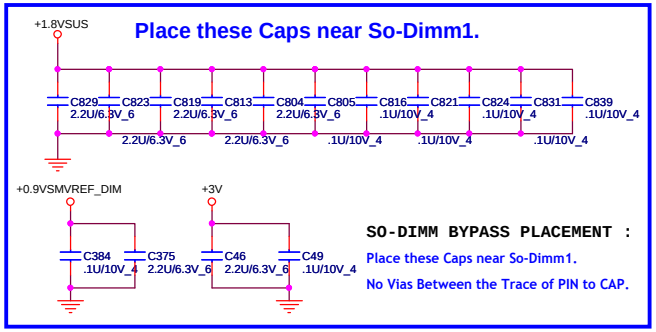
PROJECT : UT3/5
Quanta Computer Inc.
NB5
Size Custom | Document Number Cantiga Power 5/5 | Rev PV
Date: Monday, October 20, 2008 | Sheet 9 of 43

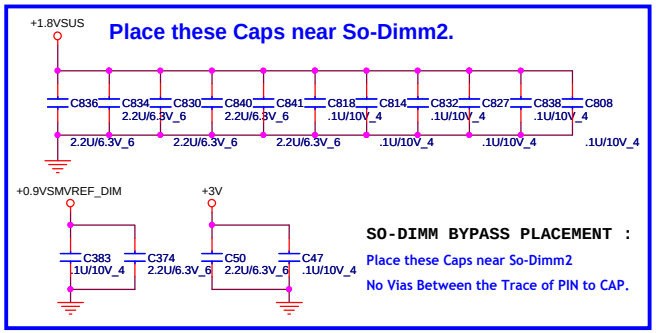












[6,8,9,33,39,42] +1.8VSUS
[2,4,6,9,11,12,14,15,19,20,21,22,23,24,25,26,27,28,29,30,32,33,34,35,36,40,43] +3V

NB5

PROJECT : UT3/5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR2 DIMM	PV

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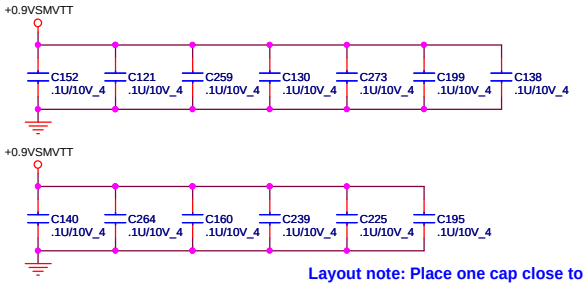
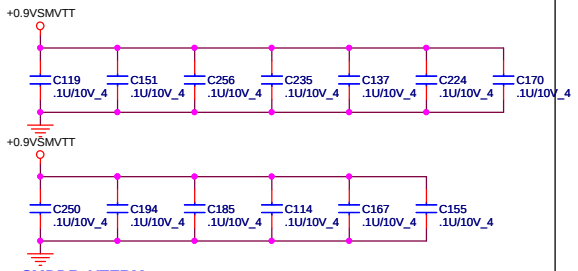
DDRII DUAL CHANNEL A,B.

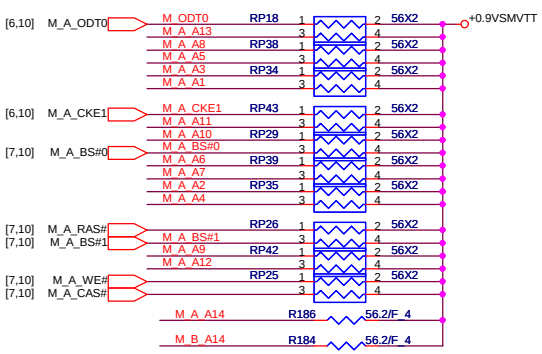
DDRII A CHANNEL

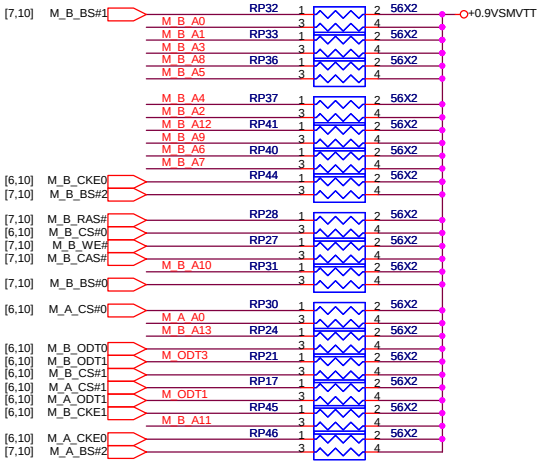


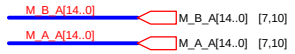
DDRII B CHANNEL

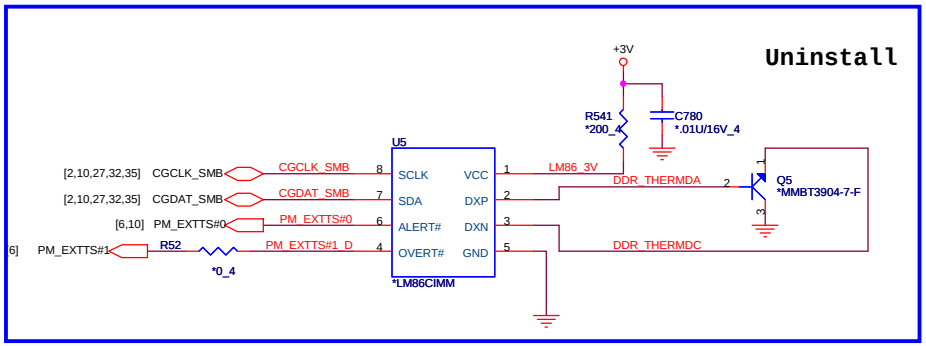


Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM









+0.9VSMVTT [42]

+3V [2,4,6,9,10,12,14,15,19,20,21,22,23,24,25,26,27,28,29,30,32,33,34,35,36,40,43]

NB5	PROJECT : UT3/5 Quanta Computer Inc.	
Size Custom	Document Number DDR2 termination	Rev PV
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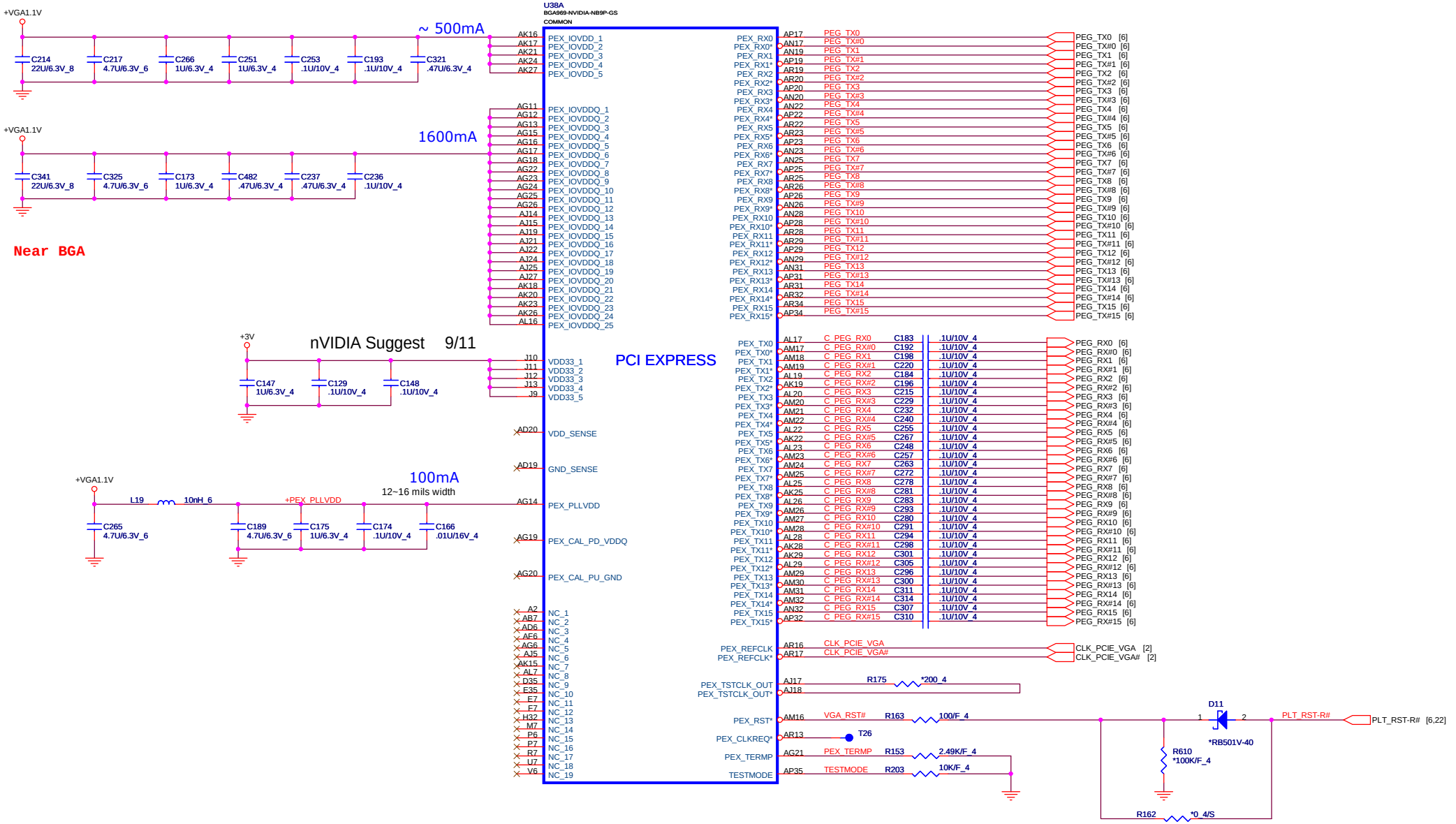

NB5	PROJECT : UT3/5 Quanta Computer Inc.	
Size: Custom	Document Number: NV9X (PCIE I/F) 1/5	Rev: PV
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U38B
BGA969-NVIDIA-NB9P-GS
COMMON

MEMORY I/F A

DB modified

U38C
BGA969-NVIDIA-NB9P-GS
COMMON

MEMORY I/F B

DB modified

for DDR2 need use CMD11(CKE) and CMD12(ODT)

use internal Vref, ext divider no stuff

For Debug only

15mils width

G96 only

R178 no stuff

R192 Install for DDR3

For G96 only
For NB9P-GS only

PROJECT : UT3/5
Quanta Computer Inc.

Size: Custom | Document Number: NV9X (MEMORY I/F) 2/5 | Rev: PV
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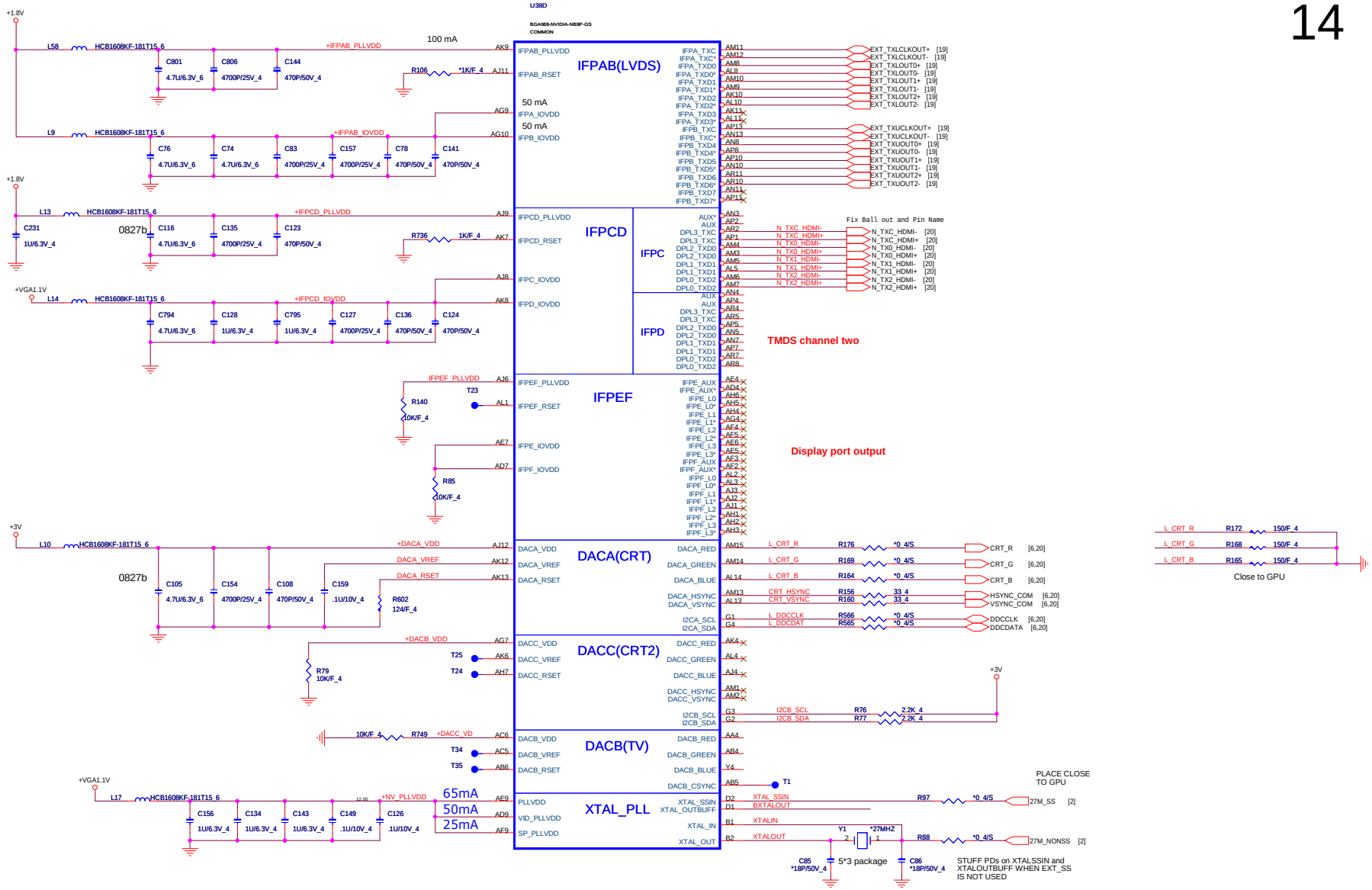
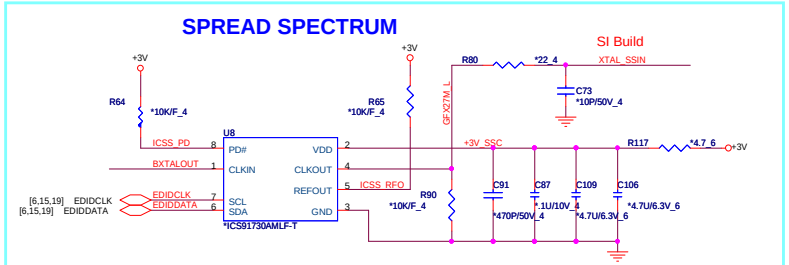
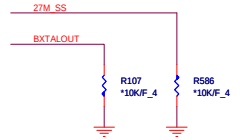
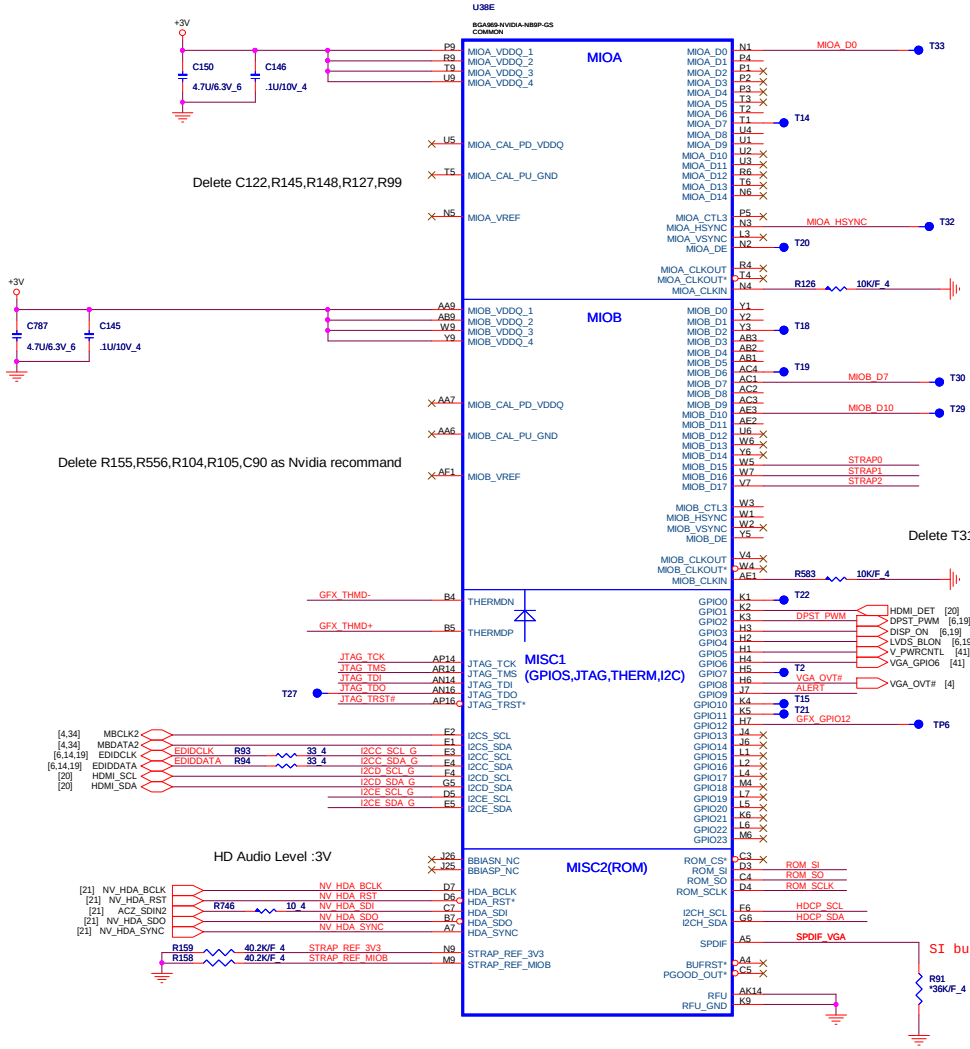






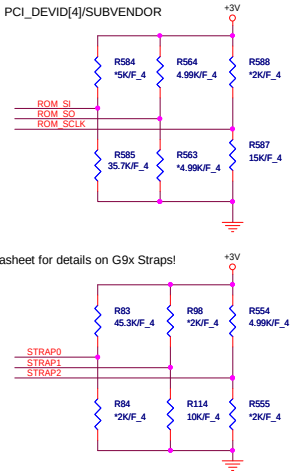
PROJECT : UT3/5
Quanta Computer Inc.

Size	Document Number	Rev
B	NVIDIA (DISPLAY) 3/5	PV
Date: Monday, October 20, 2008	Sheet 14 of 43	



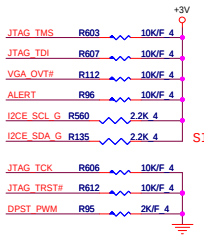
NB9P-GS (G96) Straps
NB9M-GE (G98) Straps
GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	PRIMARY DVI HOTPLUG
1	IN	N/A	SECONDARY DVI HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	FBVDD VID0
8	IN	LOW	THERMAL ALERT
9	OUT	LOW	FAN PWM
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	AC DETECT
13	OUT	LOW	PS CONTROL OR HDMI_CEC
14	OUT	HIGH	PS CONTROL



Logical Strap Bit Mapping

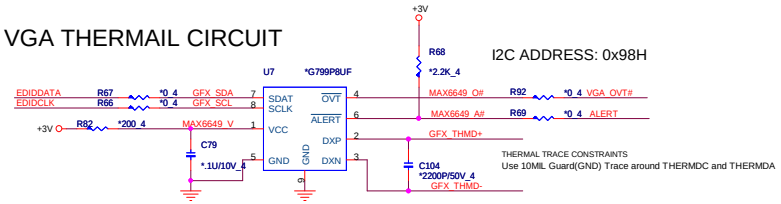
	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



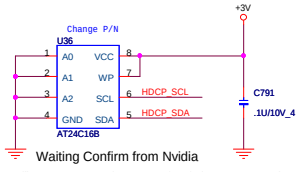
	Logical	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	XCLK_277	TVMODE2]	TVMODE[1]	TVMODE[0]	1000
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM100	0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	XXXX
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0001
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

VGA THERMAIL CIRCUIT

I2C ADDRESS: 0x98H

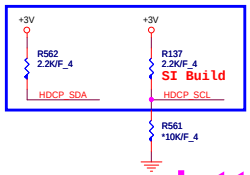


HDCP ROM



PV-2

Change R562 and R137 from 10k to 2.2k as Nvidia request



DHCP ROM	
HDCP_SCL	Low: Crypto ROM Hi: I2C ROM

NB9X VRAM Configuration Table

RAM_CFG[3:0]	DESCRIPTION	Vendor	
0111	DDR2 32Mx16x8, 128bit, 512MB	Hynix	HY5PS121621CFP-25
0110	DDR2 32Mx16x8, 128bit, 512MB	Qimonda	HYB18T512161B2F-25
0101	DDR2 32Mx16x8, 128bit, 512MB	Samsung	K4N51163QE-ZC25
other	Reserved		
0000	DDR2 64Mx16x4, 128bit, 512MB	Hynix	HY5PS1G1631CFR-25
0001	DDR2 64Mx16x4, 128bit, 512MB	Samsung	K4N1G164QQ-HC25

PCI_DEVID: STRAP2 R554

NB9M-GE	0x06E	8	1000	PU	5K
NB9M-GS	0x06E	9	1001	PU	10K
NB9P-GE2	0x064	8	1000	PU	5K
NB9P-GS	0x064	9	1001	PU	10K

CS33012FB18 RES CHIP 30.1K 1/16W +-1%(0402)
CS33572FB13 RES CHIP 35.7K 1/16W +-1%(0402)
CS34532FB18 RES CHIP 45.3K 1/16W +-1% (0402)

RAM ID: ROM_SI R585

32M*16	SAM	0101	PD	30.1K
	QIM	0110	PD	35.7K
	HYN	0111	PD	45.3K
64M*16	HYN	0000	PD	5K
	SAM	0001	PD	10K

NB5	PROJECT : UT3/5 Quanta Computer Inc.		
	Size: C	Document Number: NV9X (GPIO & STRRAPS) 4/5	Rev: PV
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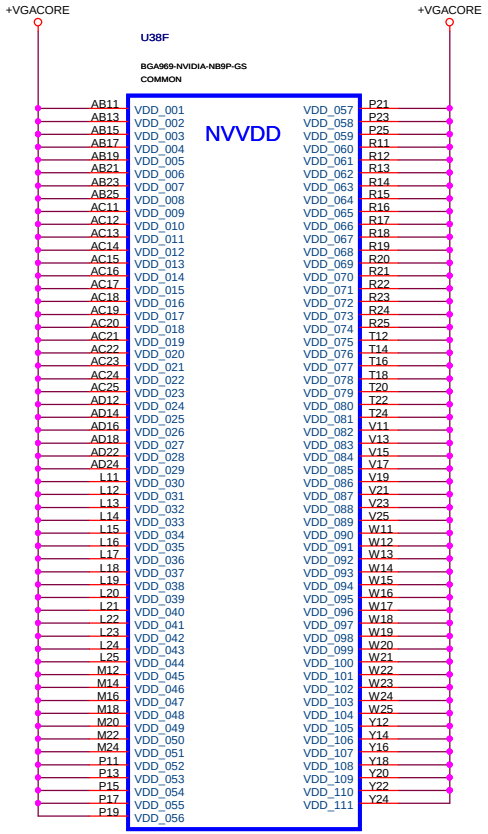
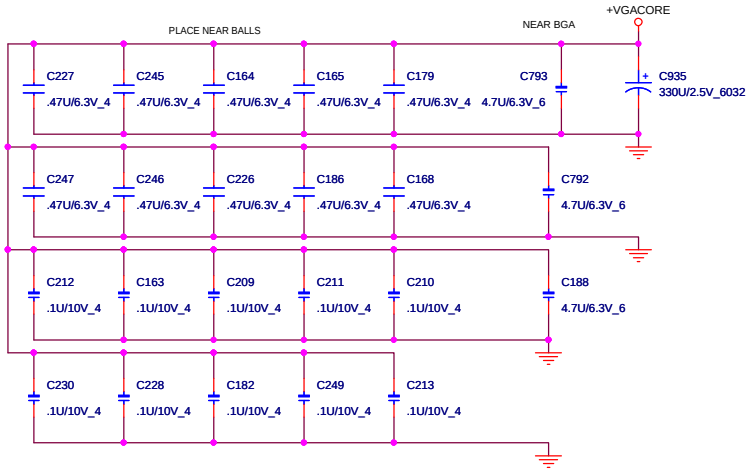
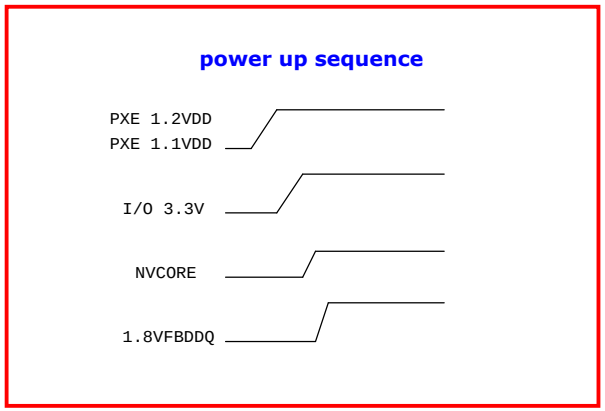
NVVDD Decoupling

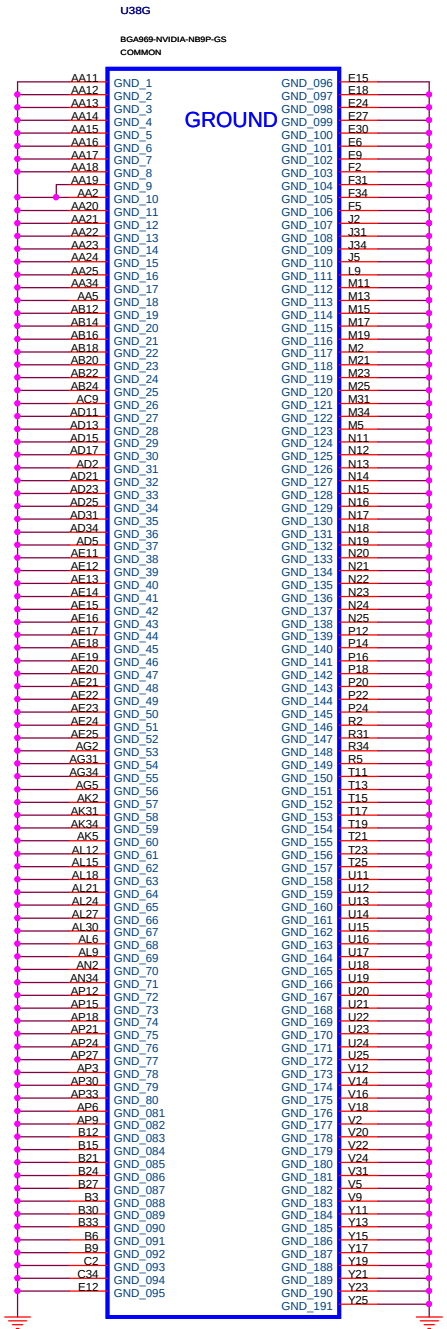




Follow Design Guide DG-03276-001 4.7uFx3 and 0.47x10 uF instead of 0.1uF x10

NB9M: VGACORE +0.90V (Normal) , +1.09V





PROJECT : UT3/5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NV9X (POWER & GND) 5/5	PV

NB5

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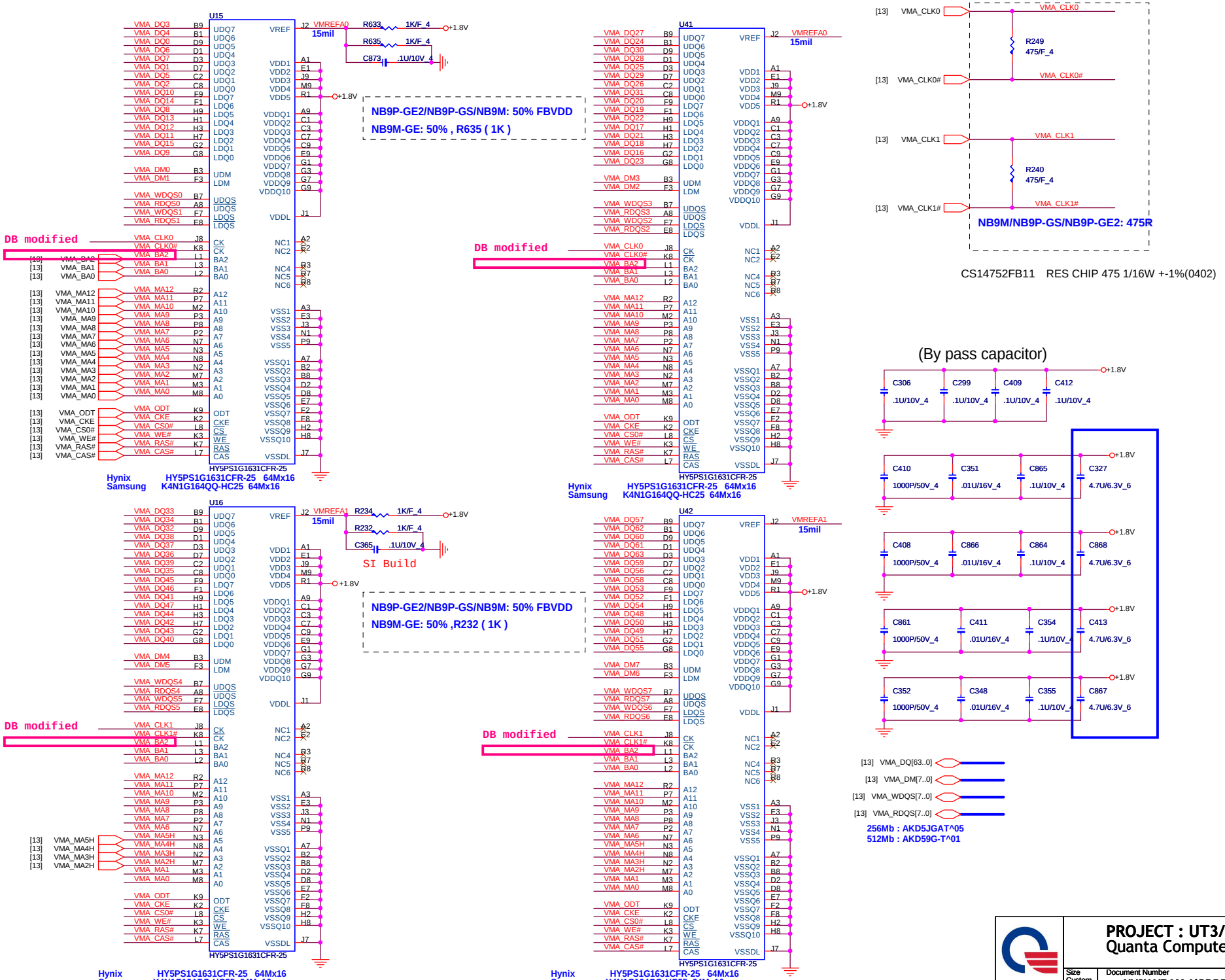

PROJECT : UT3/5	
Quanta Computer Inc.	
NB5	
Size: Custom	Document Number: NV9X VRAM-1(GDDR2 BGA84)
Rev: PV	
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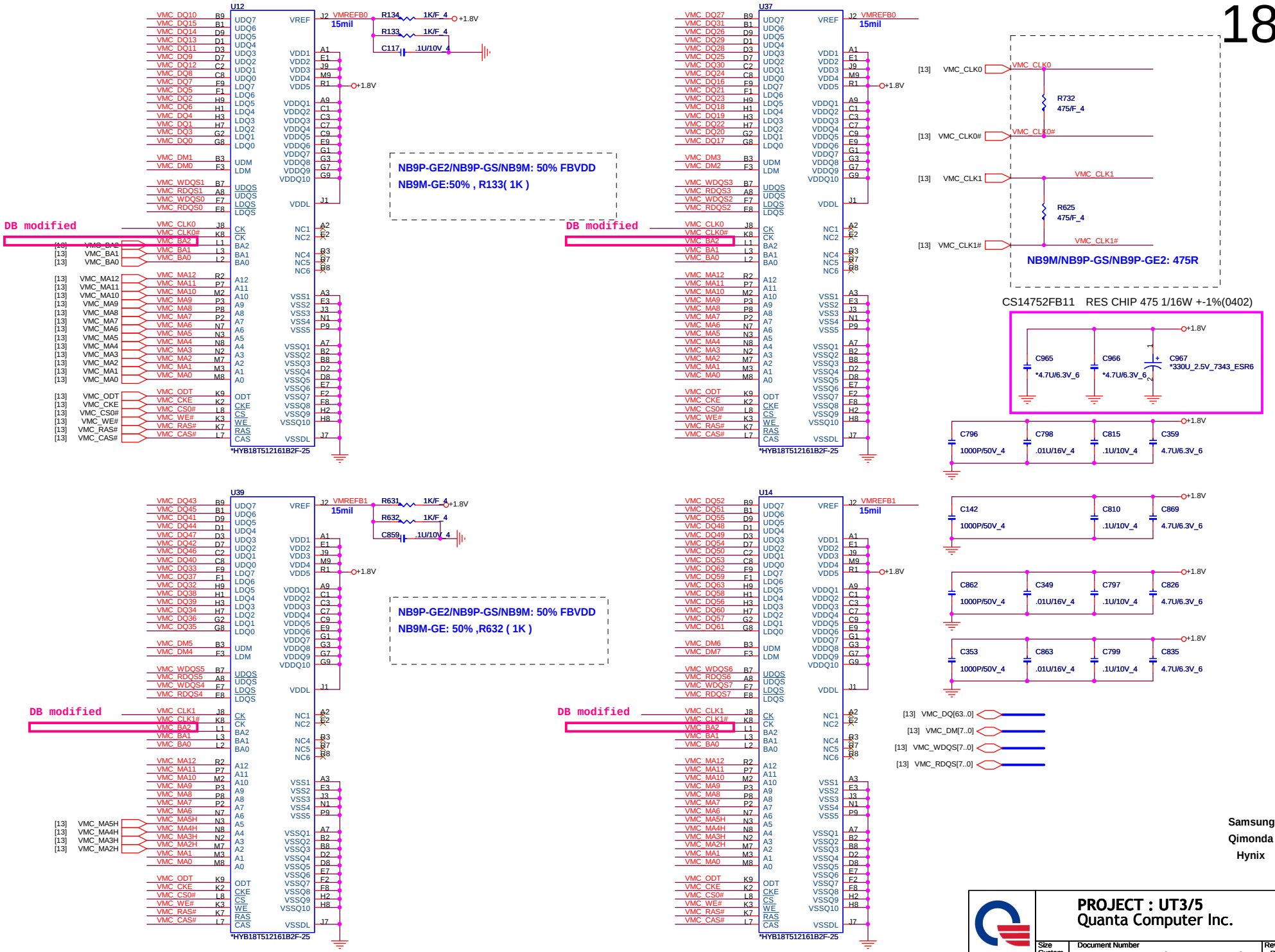

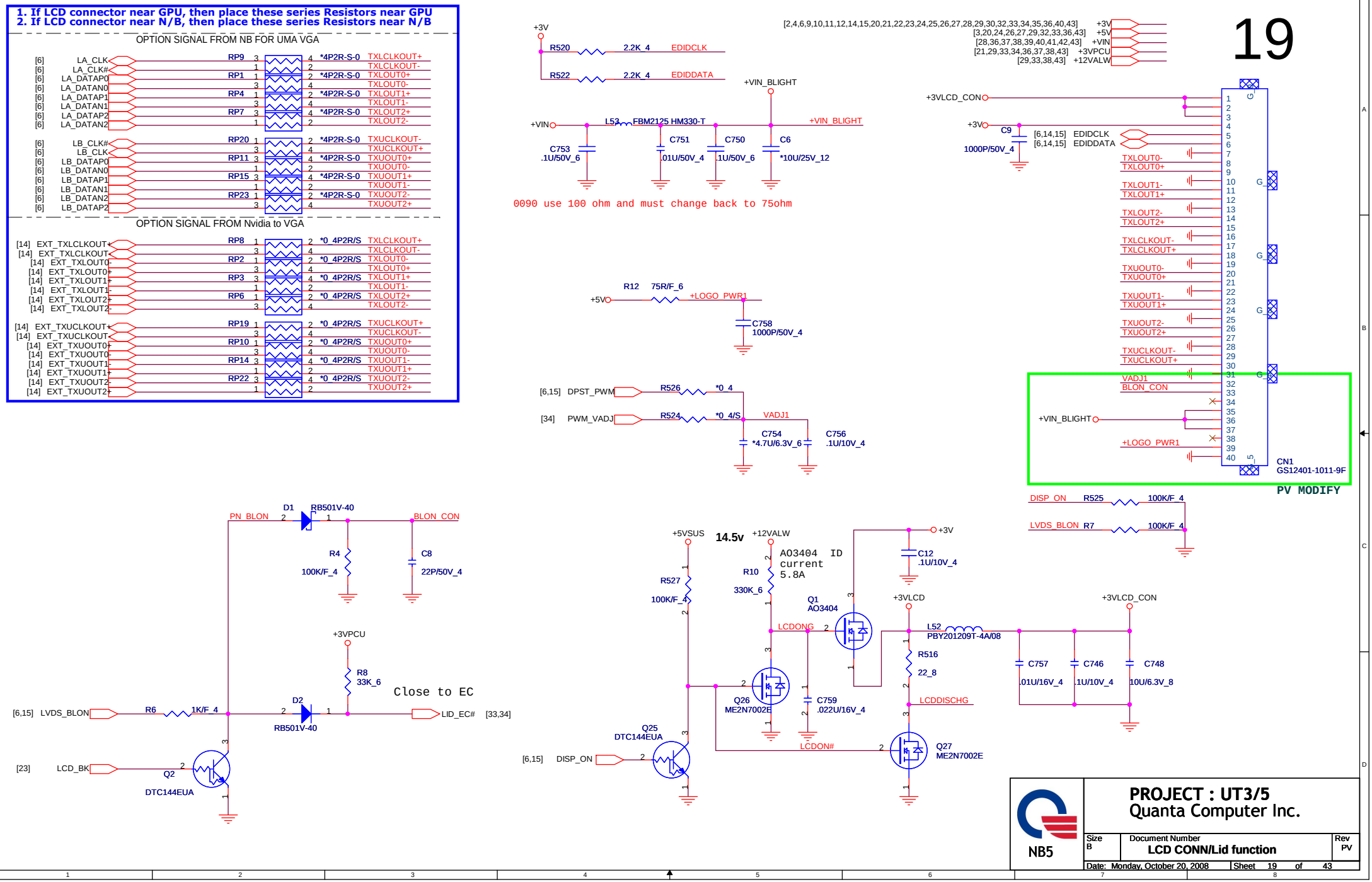

CRT PORT

Change Layout footprint to dsub-070546fr015sx68zr-15p-v

Change ESD protection to +5V

EMI

CRT CONN CN18

CRT SWITCH

U3 74CBT3257

inputs		function
/E	SET	
L	L	Y - port 0
L	H	Y - port 1
H	X	Disconnect

For UMA HDMI function

U35 *PI3VDP411LSZDE

POWER / CONTROL / GND

EQUALIZATION SETTING
PC1:PC0=0:0 8dB
PC1:PC0=0:1 4dB Recommanded
PC1:PC0=1:0 12dB
PC1:PC0=1:1 0dB

SCL/SDAZ Low-level input/output Voltage
CFG1:CFG0=0:0 VIL:<0.4V VOL:0.6V (Default)
CGF1:CGF0=0:1 VIL:<0.36V VOL:0.55V
CGF1:CGF0=1:0 VIL:<0.44V VOL:0.65V
CGF1:CGF0=1:1 VIL:<0.36V VOL:0.6V

HDMI PORT

DFHD19MR021

HDMI CONN

UMA : 0R
NB9M-GE/NB9P-GS: 0.1uF

Only for NVIDIA

for EMI request

PROJECT : UT3/5
Quanta Computer Inc.

NB5

Size C | Document Number CRT/PS8101 HDMI Conn | Rev PV

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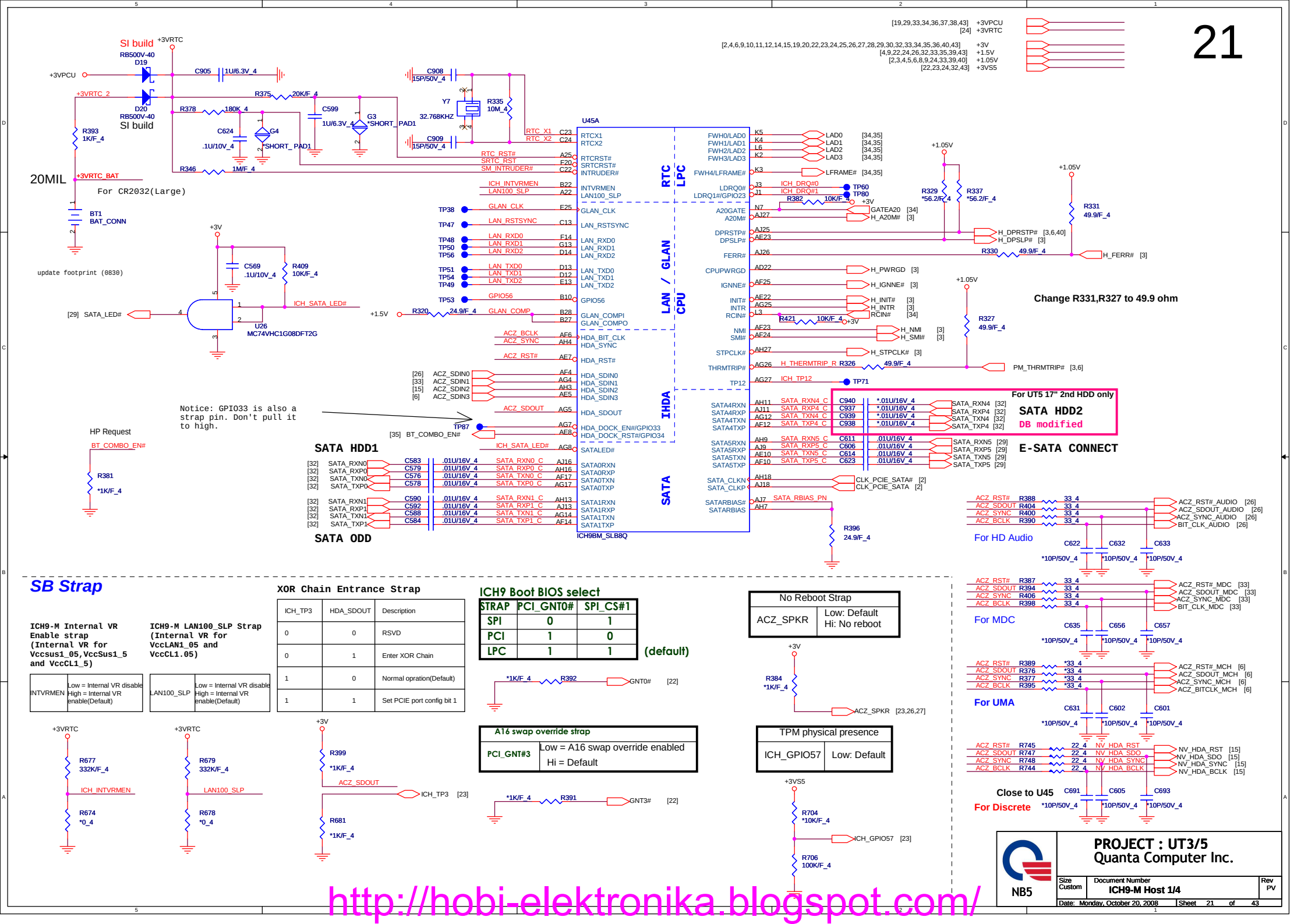
21
SI build
RB500V-40
D19
D20
+3VRTC
+3VPCU
+3VRTC_2
C905 1U/6.3V_4
R375 20K/F_4
R378 180K_4
C599 1U/6.3V_4
C624 .1U/10V_4
G3 *SHORT_PAD1
G4 *SHORT_PAD1
C908 15P/50V_4
C909 15P/50V_4
Y7 32.768KHZ
R335 10M_4
R393 1K/F_4
R346 1M/F_4
20MIL
+3VRTC_BAT
For CR2032(Large)
BT1
BAT_CONN
update footprint (0830)
C569 .1U/10V_4
R409 10K/F_4
U26
MC74VHC1G08DFT2G
[29] SATA_LED#
ICH_SATA_LED#
U45A
RTCX1
RTCX2
RTC_X1
RTC_X2
RTC_RST#
SRTC_RST
SM_INTRUDER#
INTVRMEN
LAN100_SLP
GLAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
GPIO56
GLAN_COMPI
GLAN_COMPO
R320 24.9/F_4
HDA_BIT_CLK
HDA_SYNC
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDOUT
HDA_DOCK_EN#/GPIO33
HDA_DOCK_RST#/GPIO34
SATALED#
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
ICH9BM_SLB8Q
RTC
LPC
LAN / GLAN
CPU
IHDA
SATA
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
LDRQ0#
LDRQ1#/GPIO23
A20GATE
A20M#
DPRSTP#
DPSLP#
FERR#
CPUPWRGD
IGNNE#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THRMTRIP#
TP12
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP
SATA_CLKN
SATA_CLKP
SATARBIAS#
SATARBIAS
R396 24.9/F_4
SATA_RBIAS_PN
LAD0 [34,35]
LAD1 [34,35]
LAD2 [34,35]
LAD3 [34,35]
LFRAME# [34,35]
ICH_DRQ#0
ICH_DRQ#1
TP60
TP80
R382 10K/F_4
GATEA20 [34]
H_A20M# [3]
H_DPRSTP# [3,6,40]
H_DPSLP# [3]
H_FERR# [3]
H_PWRGD [3]
H_IGNNE# [3]
H_INIT# [3]
H_INTR [3]
RCIN# [34]
R421 10K/F_4
H_NMI [3]
H_SMI# [3]
H_STPCLK# [3]
H_THERMTRIP_R
R326 49.9/F_4
PM_THRMTRIP# [3,6]
ICH_TP12
TP71
R329 *56.2/F_4
R337 *56.2/F_4
R331 49.9/F_4
R330 49.9/F_4
R327 49.9/F_4
+1.05V
+3V
Change R331,R327 to 49.9 ohm
For UT5 17" 2nd HDD only
SATA HDD2
DB modified
E-SATA CONNECT
SATA_RXN4_C C940 *.01U/16V_4
SATA_RXP4_C C937 *.01U/16V_4
SATA_TXN4_C C939 *.01U/16V_4
SATA_TXP4_C C938 *.01U/16V_4
SATA_RXN5_C C611 .01U/16V_4
SATA_RXP5_C C606 .01U/16V_4
SATA_TXN5_C C614 .01U/16V_4
SATA_TXP5_C C623 .01U/16V_4
CLK_PCIE_SATA# [2]
CLK_PCIE_SATA [2]
SATA HDD1
SATA ODD
SATA_RXN0_C AJ16
SATA_RXP0_C AH16
SATA_TXN0_C AF17
SATA_TXP0_C AG17
SATA_RXN1_C AH13
SATA_RXP1_C AJ13
SATA_TXN1_C AG14
SATA_TXP1_C AF14
ACZ_BCLK AE6
ACZ_SYNC AH4
ACZ_RST# AE7
ACZ_SDIN0 AF4
ACZ_SDIN1 AG4
ACZ_SDIN2 AH3
ACZ_SDIN3 AE5
ACZ_SDOUT AG5
TP87
BT_COMBO_EN#
Notice: GPIO33 is also a strap pin. Don't pull it to high.
HP Request
R381 *1K/F_4
For HD Audio
For MDC
For UMA
Close to U45
For Discrete
ACZ_RST#_AUDIO [26]
ACZ_SDOUT_AUDIO [26]
ACZ_SYNC_AUDIO [26]
BIT_CLK_AUDIO [26]
ACZ_RST#_MDC [33]
ACZ_SDOUT_MDC [33]
ACZ_SYNC_MDC [33]
BIT_CLK_MDC [33]
ACZ_RST#_MCH [6]
ACZ_SDOUT_MCH [6]
ACZ_SYNC_MCH [6]
ACZ_BITCLK_MCH [6]
NV_HDA_RST [15]
NV_HDA_SDO [15]
NV_HDA_SYNC [15]
NV_HDA_BCLK [15]
SB Strap
ICH9-M Internal VR Enable strap (Internal VR for Vccsus1_05,VccSus1_5 and VccCL1_5)
INTVRMEN Low = Internal VR disable High = Internal VR enable(Default)
ICH9-M LAN100_SLP Strap (Internal VR for VccLAN1_05 and VccCL1.05)
LAN100_SLP Low = Internal VR disable High = Internal VR enable(Default)
XOR Chain Entrance Strap
ICH_TP3 HDA_SDOUT Description
0 0 RSVD
0 1 Enter XOR Chain
1 0 Normal opration(Default)
1 1 Set PCIE port config bit 1
ICH9 Boot BIOS select
STRAP PCI_GNT0# SPI_CS#1
SPI 0 1
PCI 1 0
LPC 1 1
(default)
GNT0# [22]
GNT3# [22]
No Reboot Strap
ACZ_SPKR Low: Default Hi: No reboot
ACZ_SPKR [23,26,27]
A16 swap override strap
PCI_GNT#3 Low = A16 swap override enabled Hi = Default
TPM physical presence
ICH_GPIO57 Low: Default
ICH_GPIO57 [23]
R677 332K/F_4
R674 *0_4
R679 332K/F_4
R678 *0_4
R399 *1K/F_4
R681 *1K/F_4
ICH_TP3 [23]
R704 *10K/F_4
R706 100K/F_4
PROJECT : UT3/5
Quanta Computer Inc.
NB5
Size Custom
Document Number ICH9-M Host 1/4
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http://hobi-elektronika.blogspot.com/

SWAP PCIE PORT6 to PORT2 (Lan and New card swap) -->Rename the port name by function and port

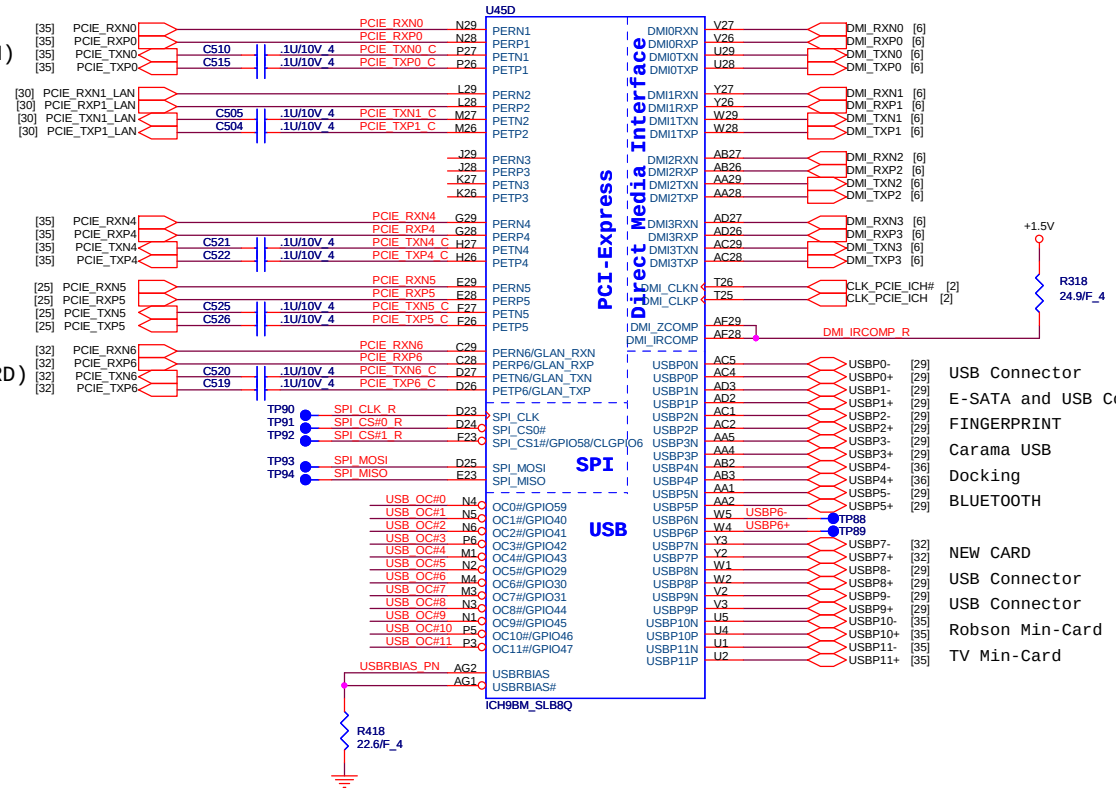
[4,9,21,24,26,32,33,35,39,43] +1.5V
[2,4,6,9,10,11,12,14,15,19,20,21,23,24,25,26,27,28,29,30,32,33,34,35,36,40,43] +3V
[23,29,35,39,40,41,43] +3VSUS

MINI CARD PCI-E(WLAN)

PCIE-LAN

TV CARD PCI-E

EXPRESS CARD (NEW CARD)



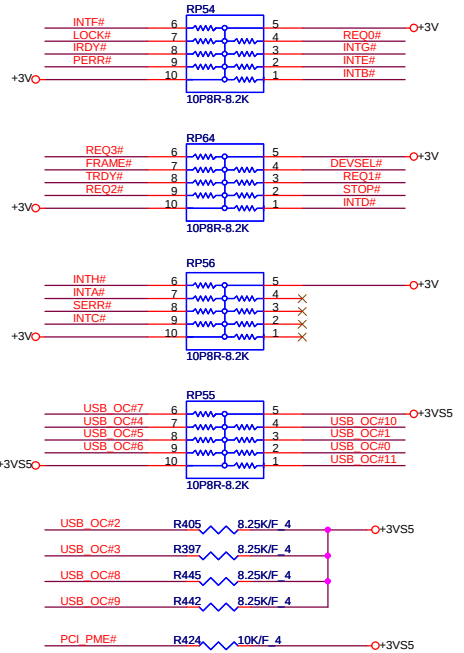
USB Connector
E-SATA and USB Connector
FINGERPRINT
Carama USB
Docking
BLUETOOTH

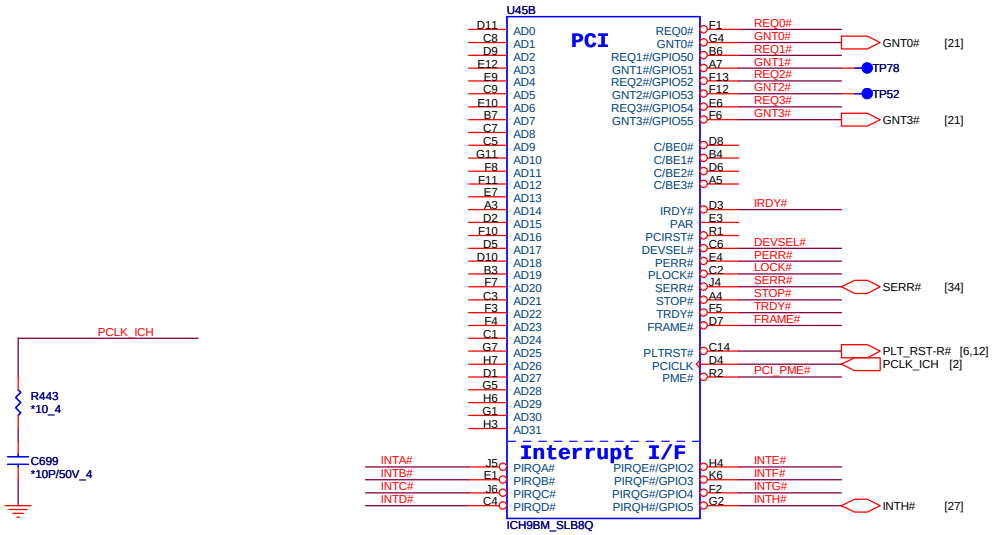
NEW CARD
USB Connector
USB Connector
Robson Min-Card
TV Min-Card

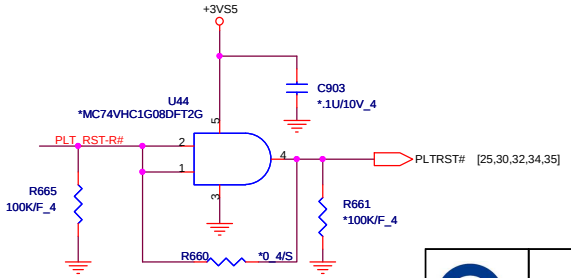
SI-2 Delete
Delete RP53,RP57 and tied from SB to CR(USB6)

des

int







PROJECT : UT3/5
Quanta Computer Inc.

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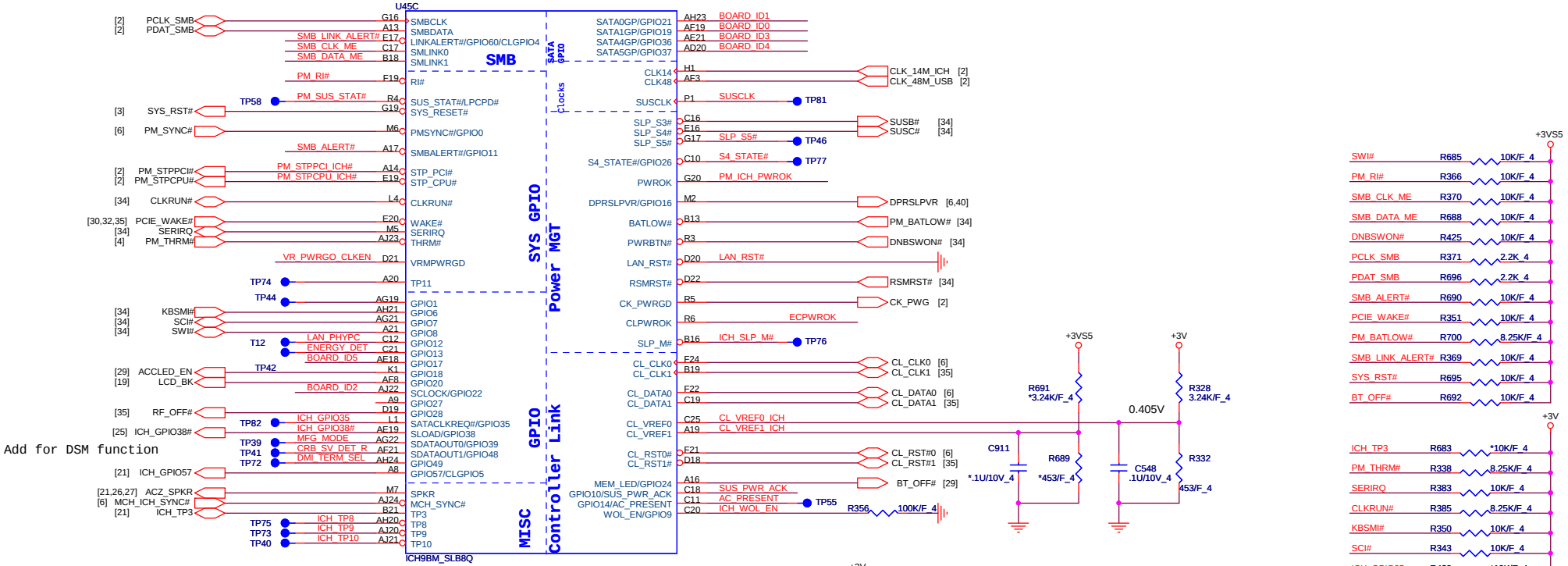
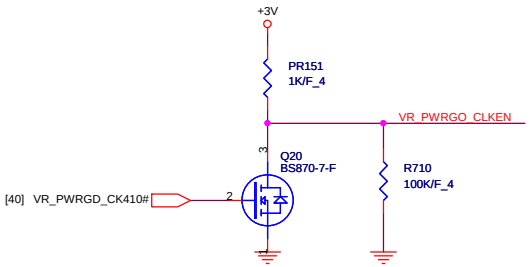
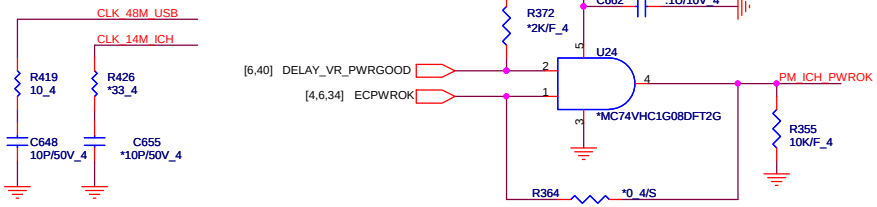
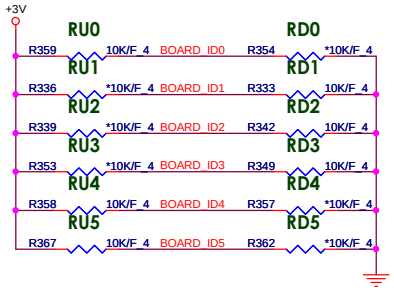
[4,9,21,22,24,26,32,33,35,39,43] +1.5V
[2,4,6,9,10,11,12,14,15,19,20,21,22,24,25,26,27,28,29,30,32,33,34,35,36,40,43] +3V
[21,22,24,32,43] +3VS5
[29,35,39,40,41,43] +3VSUS









Board ID	ID0	ID1	ID2	ID3	ID4	ID5
UT3/Dis./9M	RD0 (0)	RU1 (1)	RD2 (0)	NC	NC	RD5 (0)
UT3/UMA	RD0 (0)	RD1 (0)	NC	NC	NC	NC
UT5/Dis./M92	RU0 (1)	RU1 (1)	RD2 (0)	NC	NC	RU5 (1)
UT5/Dis./M96	RU0 (1)	RU1 (1)	RU2 (1)	NC	NC	RD5 (0)
UT5/UMA	RU0 (1)	RD1 (0)	NC	NC	NC	NC
UT3D/Dis./M92	RD0 (0)	RU1 (1)	RD2 (0)	NC	NC	RU5 (1)
UT3D/Dis./M96	RD0 (0)	RU1 (1)	RU2 (1)	NC	NC	RD5 (0)

Board ID	ID0	ID1	ID2	ID3	ID4	ID5
UT3/5	0=UT3 1=UT5					
UMA/Dis.		0=UMA 1=Dis.				
NV9M			0			0
ATI M92			0			1
ATI M96			1			0

NB5

PROJECT : UT3/5
Quanta Computer Inc.

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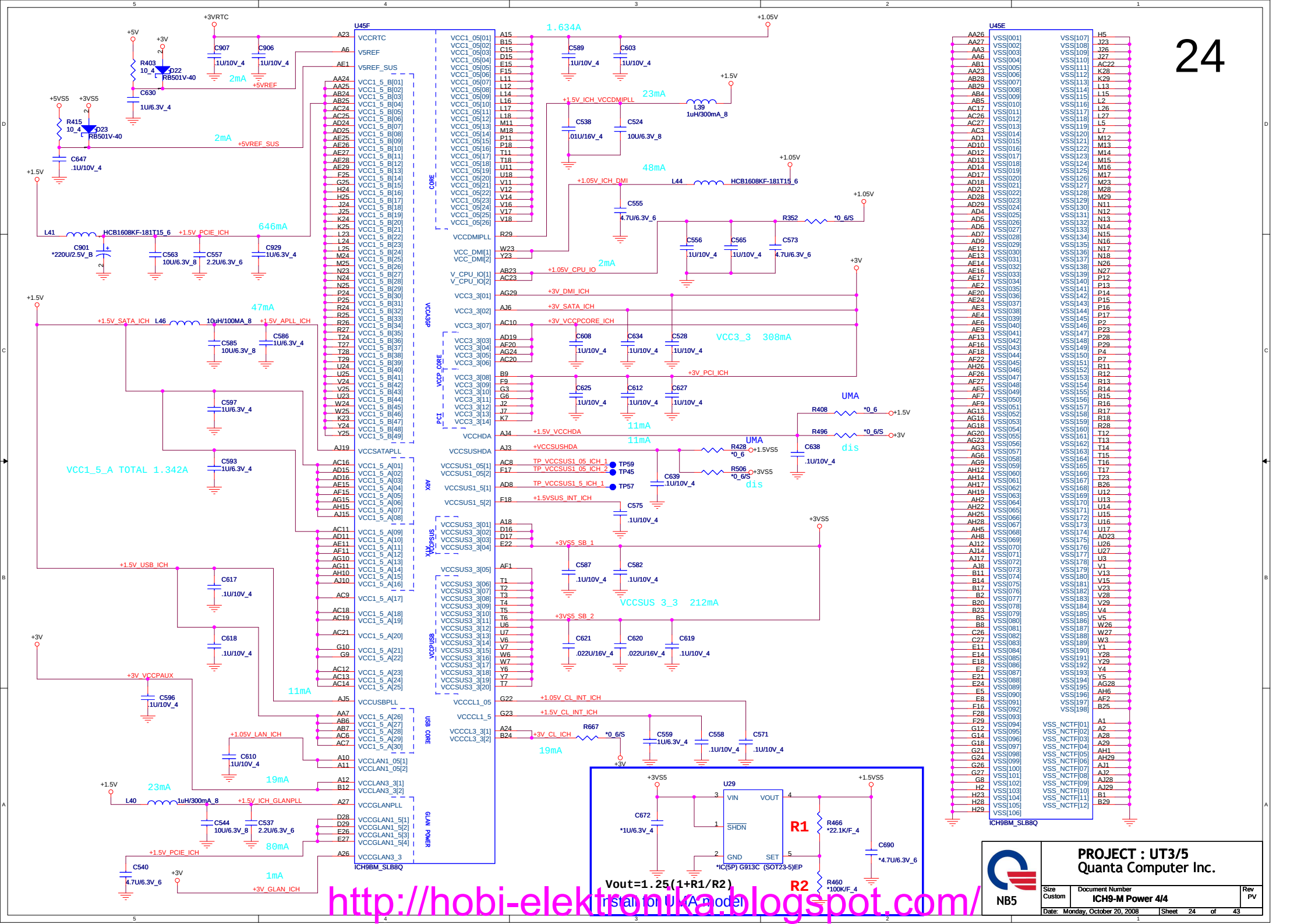
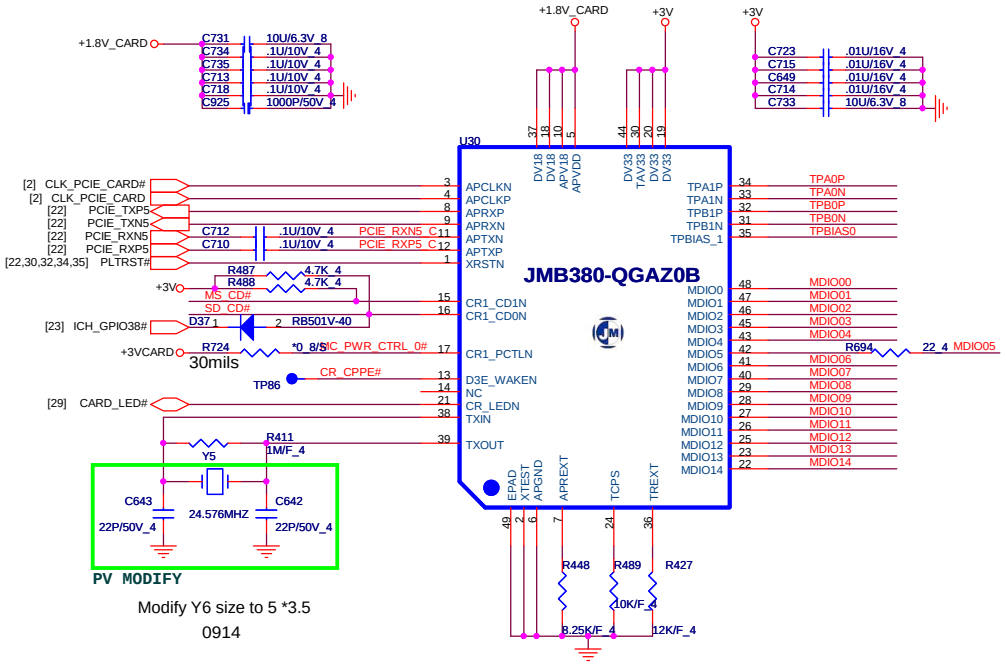
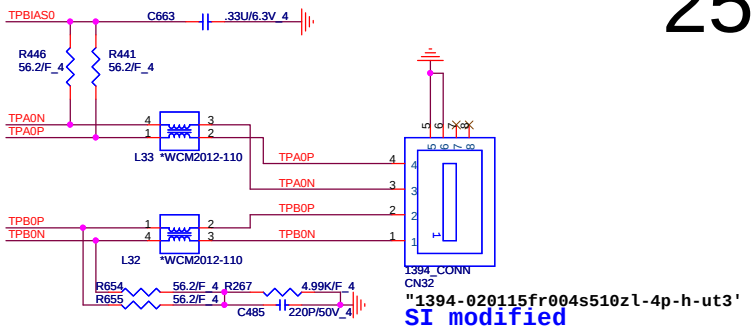
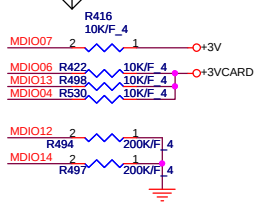






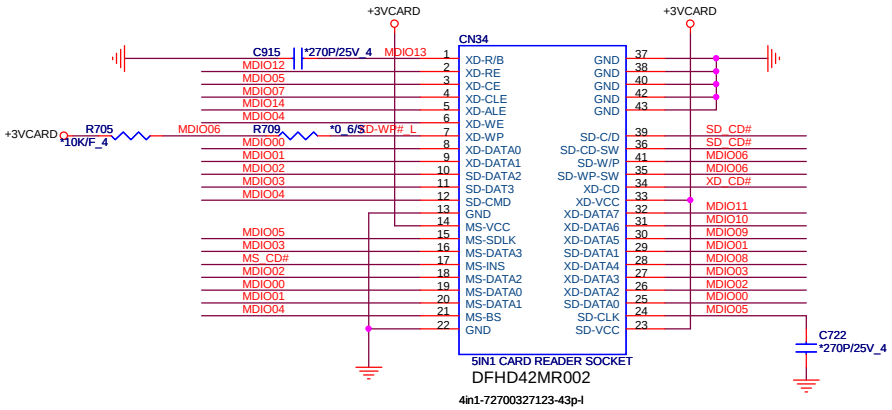
Change to 10K

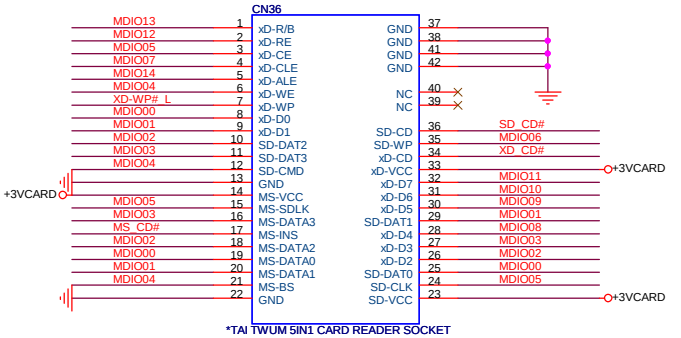


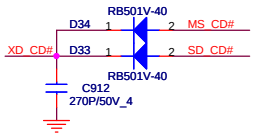
JMB 380 Note:

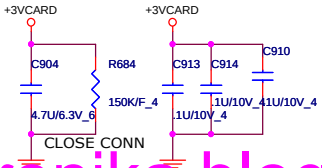
SD/MMC	MS	XD
MDID0 SD_DAT0	MS_D0	XD_D0
MDID1 SD_DAT1	MS_D1	XD_D1
MDID2 SD_DAT2	MS_D2	XD_D2
MDID3 SD_DAT3	MS_D3	XD_D3
MDID4 SD_CMD	MS_BS	XD_WE#
MDID5 SD_CLK	MS_SCLK	XD_CE#
MDID6 SD_WP		XD_WP#
MDID7		XD_CLE
MDID8 SD_DAT4		XD_D4
MDID9 SD_DAT5		XD_D5
MDID10 SD_DAT6		XD_D6
MDID11 SD_DAT7		XD_D7
MDID12		XD_RE#
MDID13		XD_R/B#
MDID14		XD_ALE
CR1_LEDN SD1_LED#	MS1_LED#	XD_LED#
CR1_PCTLN SD1_PCTL#	MS1_PCTL#	XD1_PCTL#
CR1_CD0 SD1_CD#		XD_CV#
CR1_CD1	MS1_CD#	XD_CD#

5 IN1 CARD READER
XD,MMC/SD,MS/MSP









NB5

PROJECT : UT3/5
Quanta Computer Inc.

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Custom	RTS5158 & CR SOCKET &HOLE	PV

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SI MODIFY

+3V_DVDD R571 *0_4 DVDD_LV

DB MODIFY

UMA +3V_1.5V_DVIO

+1.5V +3V_DVDD R454 *0_4 R517 *0_4/S Dis

C688 1U/10V_4

+3V_DVDD C695 1U/10V_4 C685 1U/6.3V_4 C716 10U/6.3V_8 DVDD_LV

+4.75VAVDD C721 1U/10V_4 C738 1U/6.3V_4 C770 1U/6.3V_4 C737 .1U/10V_4

Close to Pin38

AGND

+3V_DVDD Close to Pin9

+3V C684 1U/6.3V_4 C671 1U/10V_4 C669 10U/6.3V_8

U32 IDT 92HD75B3

Digital

Analog

DVDD_IO DVDD_CORE DVDD_LV AVDD1 AVDD2**

SDO BITCLK SDI_CODEC SYNC RESET#

VOL_UP/DMIC_0 VOL_DN/DMIC_1

GPIO 3 GPIO 5 GPIO 6 GPIO 7 / SPDIF OUT1 DMIC_CLK

SPDIF0 EAPD/GPIO0/SPDIF OUT 0 or 1

PAD NC NC NC NC NC/OTP DVSS AVSS2** AVSS1 VREFFILT CAP2

[21] ACZ_SDOUT_AUDIO
[21] BIT_CLK_AUDIO
[21] ACZ_SDIN0
[21] ACZ_SYNC_AUDIO
[21] ACZ_RST#_AUDIO

R452 22_4 ADC_BITCLK ACZ_SDIN0_ADC

[29] DIGITAL_D1
[27] HP_EAPD

C762 10P/50V_4 R471 *0_6/S

[27] IDT_GPIO3# IDT_GPIO3#

[28] SUB-MUTE# SUB-MUTE#

[36] PR_INSERT# IDT R726 *0_4/S
JACK_SEN# R723 *0_4

For IDT Dolby functionality.

[29] DIGITAL_CLK R476 22_6

C763 *10P/50V_4

[36] SPDIF
[27] EAPD#

C743 10U/6.3V_8 C739 1U/6.3V_4

AGND

PORTA_L PORTA_R

C628 47U/6.3V_3528 C629 47U/6.3V_3528 R569 60.4_4 R570 60.4_4

DOCK_LSPK+ [36] DOCK_RSPK+ [36]

TO DOCKING Speakers

PORTB_L PORTB_R VREFOUT-B

MIC1_L1 C711 2.2U/6.3V_6 EXT_MIC_L
MIC1_R1 C719 2.2U/6.3V_6 EXT_MIC_R
VREFOUT_B R482 4.7K_4 R492 4.7K_4 C717 1U/6.3V_4

TO Audio Jack MIC

SI MODIFY

LINE_OUTR R572 *0_4 SUB_OUTR [28]
LINE_OUTL R573 *0_4 SUB_OUTL [28]

TO Internal Speakers and Sub Woofer EQ

PORTC_L PORTC_R VREFOUT-C

C736 *1U/6.3V_4

PORT-D_L PORT-D_R

LINE_OUTL LINE_OUTL [27]
LINE_OUTR LINE_OUTR [27]

PORTE_L PORTE_R VREFOUT-E / GPIO 4

DOCK_MIC_L1 C697 2.2U/6.3V_6 DOCK_MIC_L2
DOCK_MIC_R1 C706 2.2U/6.3V_6 DOCK_MIC_R2
VREFOUT_E R499 *4.7K_4 R485 *4.7K_4 C742 *1U/6.3V_4

R463 1.21K_4 R462 10K/F_4 R474 10K/F_4 R475 1.21K_4

DOCK_MIC_L [36] DOCK_MIC_R [36]

TO DOCKING MIC

PORTF_L PORTF_R

HP-L HP-R

HP-L [27] HP-R [27]

TO Headphone jack

PCBEEP/Mono

C692 1U/10V_4 R438 47K_4 R450 10K/F_4 C675 1U/10V_4 R449 2.49K/F_4 R523 39.2K/F_4 R456 20K/F_4 C680 1000P/50V_4 R510 2.49K/F_4 R509 39.2K/F_4 R457 20K/F_4 C740 1000P/50V_4

ACZ_SPKR [21,23,27]

SENSE_A SENSE_B

+4.75VAVDD +4.75VAVDD

SB_A# SA_B# SB_E# SA_F#

DB MODIFY

SA_A# -->DOCK HP
SA_B# -->EXT MIC
SB_E# -->DOCK MIC
SA_F# -->EXT HP

Audio JACK: Normal Open

Reserve for EAPD#

+3V_DVDD R479 *5.11K/F_4 EAPD#

PORT	PLACE TO
MONO_OUT	X
PORT A	Docking Speakers
PORT B	M/B MIC
PORT C	X
PORT D	Internal Speckers
PORT E	Docking MIC
PORT F	HP OUT
DM	DIGITAL MIC

R501 *0_6/S
R500 *0_6/S
R480 *0_6/S
R473 *0_6/S
R440 *0_6/S
R491 *0_6/S
R472 *0_6/S

C741 1000P/50V_4

AGND

ADC_BITCLK ACZ_SDIN0_ADC

C687 *27P/50V_4 C686 *27P/50V_4

FOR EMI

HP_EAPD

TPA6040A4	Low enable
TPA6047A4	High enable

Codec

	92HD71	92HD75
R571	POP	NA
C716	NA	POP
R449 R510	5.11K	2.49K

5.11K P/N: CS25112FB15

TO AUDIO/B CON.

DFFC12FR293

C707 .1U/10V_4

CN17 AUDIO CONN

+5VPCU

[34,36] CIR_IN

[27] HPOUT_L
[27] HPOUT_R

HPOUT_L HPOUT_R SA_F# SA_B# EXT_MIC_L EXT_MIC_R

C705 *180P/50V_4 C704 *180P/50V_4

C703 *27P/50V_4 C702 *27P/50V_4

EMI 0828

AGND

DOCK MIC DETECT

+5V

R538 10K/F_4 R535 10K/F_4

Q30 ME2N7002E

SB_E#

DOCK_MIC_L R536 10K/F_4

DKMIC_SEN

Q29 MMBT3904-7-F

R537 47K_4 C779 1U/6.3V_4

Q28 MMBT3904-7-F

+5V

R568 47K_4 R556 47K_4

SB_A#

Q37 ME2N7002E

[36] JACK_SEN# R567 10K/F_4

Q38 MMBT3904-7-F

AGND

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Quanta Computer Inc.

NB5

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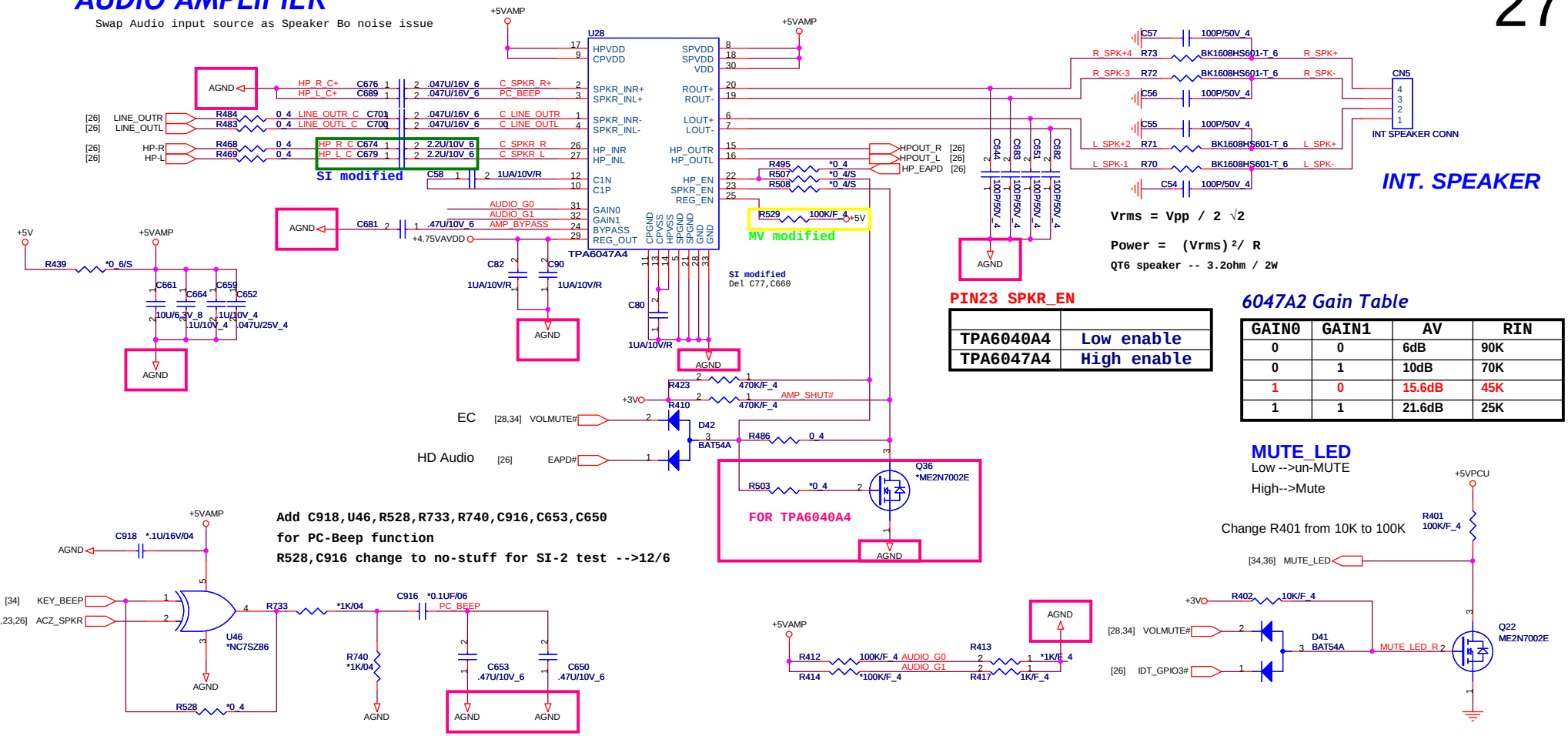
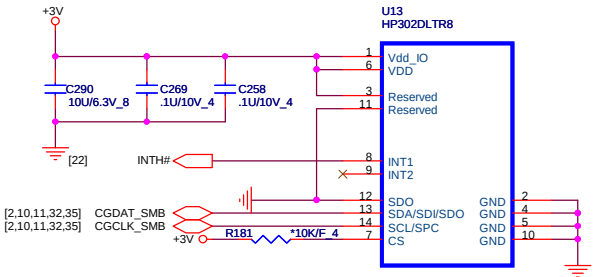
AUDIO AMPLIFIER

Swap Audio input source as Speaker Bo noise issue



Accelerometer Sensor

SGT-LIS302DLTR interrupt pin default is low / active Hi , BIOS need to programming 22h to change status from active Hi to low



Change R181 to no stuff as internal pull high

Pin 12: Low 38hex

Pin 12: unconnected/floating 3Ahex

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Size: Custom	Document Number: AMP_TPA6017/Accelerometer
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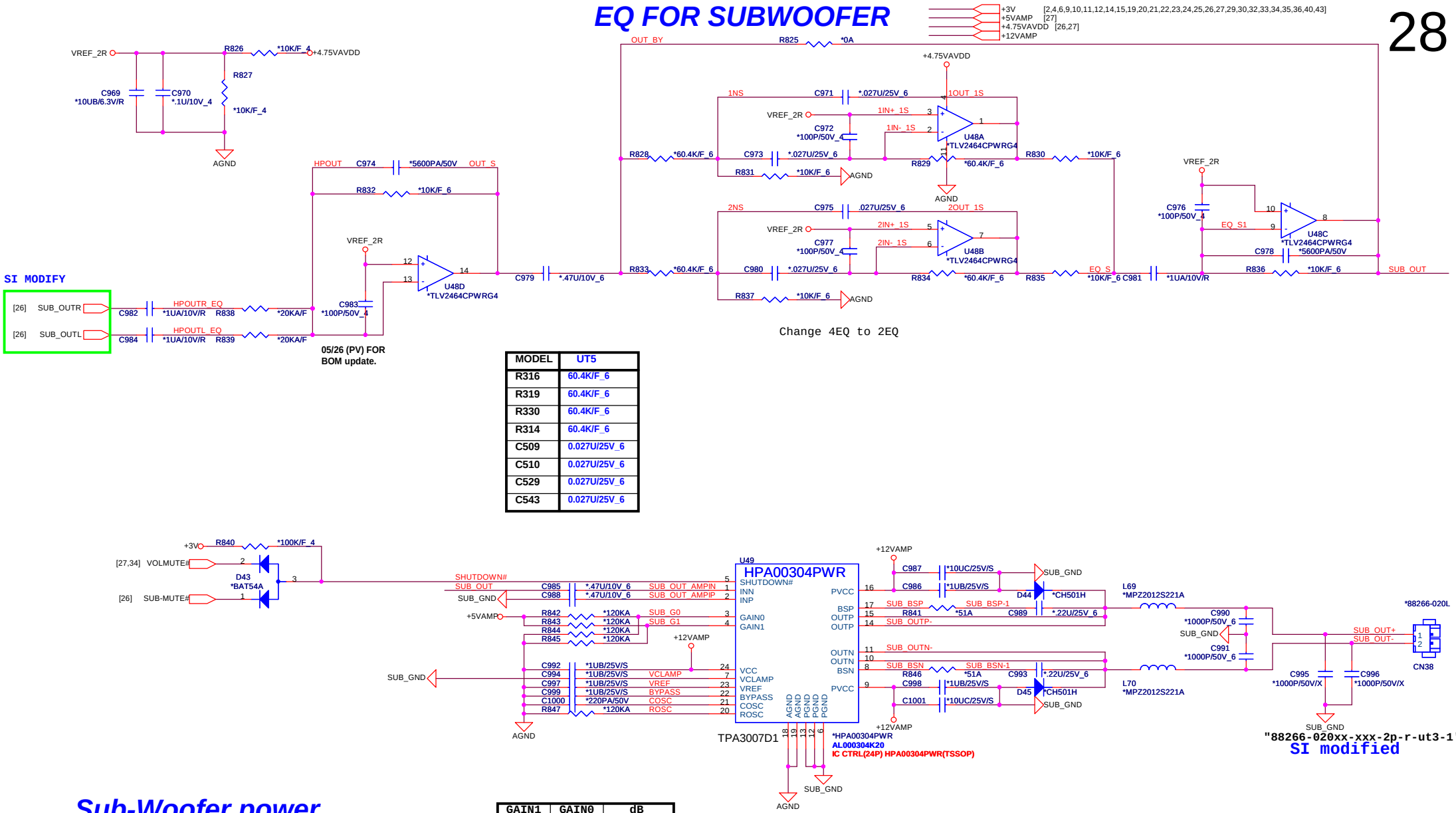
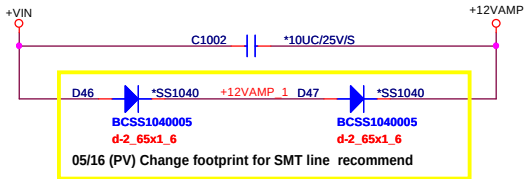
EQ FOR SUBWOOFER



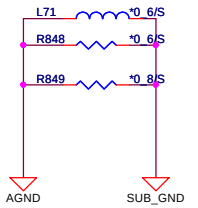
Change 4EQ to 2EQ

MODEL	UT5
R316	60.4K/F_6
R319	60.4K/F_6
R330	60.4K/F_6
R314	60.4K/F_6
C509	0.027U/25V_6
C510	0.027U/25V_6
C529	0.027U/25V_6
C543	0.027U/25V_6

Sub-Woofer power



GAIN1	GAIN0	dB
0	0	12
0	1	18
1	0	23.6
1	1	36



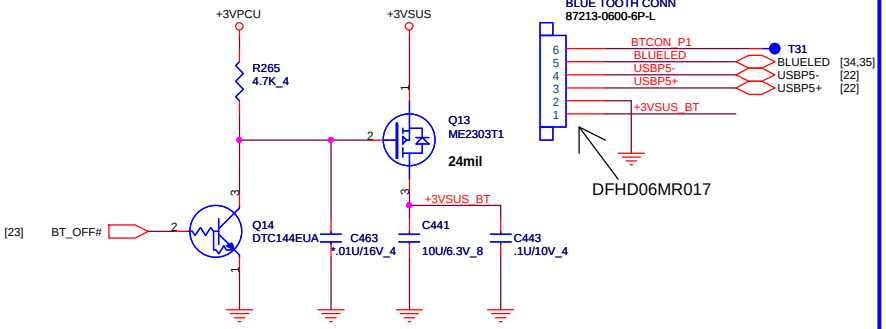
PROJECT : UT3/5
Quanta Computer Inc.

NB5

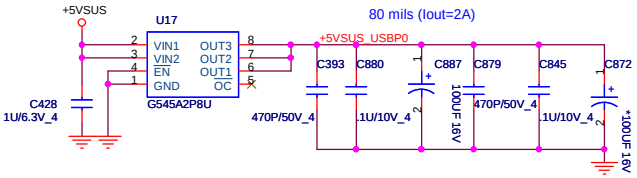
Size	Document Number	Rev
Custom	SUBWOOFER(EQ & AMP.)	PV

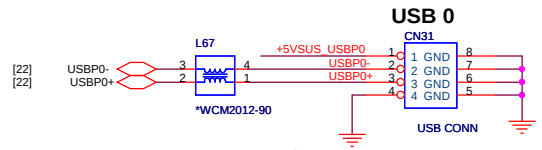
Date: Monday, October 20, 2008 Sheet 28 of 43

BLUETOOTH



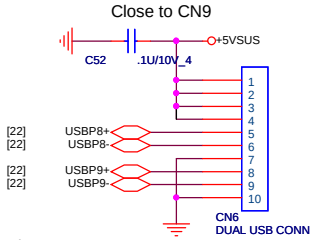
LEFT SIDE USBX1 and E-SATA/USB COMBO



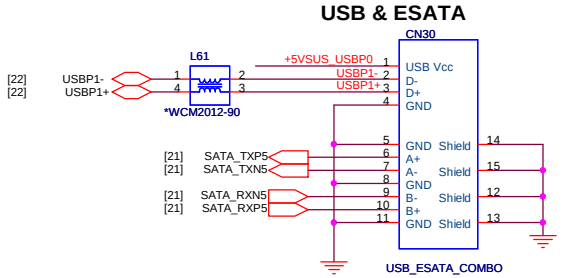


SI modified
usb-020173mr004s51-4p-r-h-ut3

RIGHT SIDE USBX2



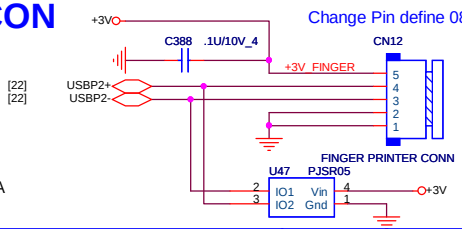
Change CN6 to BL123-10R-10P-L-QT6-A



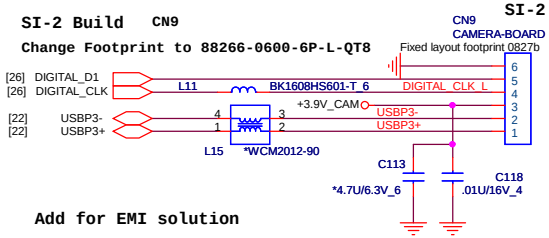
USB fingerprint CON

1. ESD GND
2. SYSTEM GND
3. USB-
4. USB+
5. USB PWR(+3V)

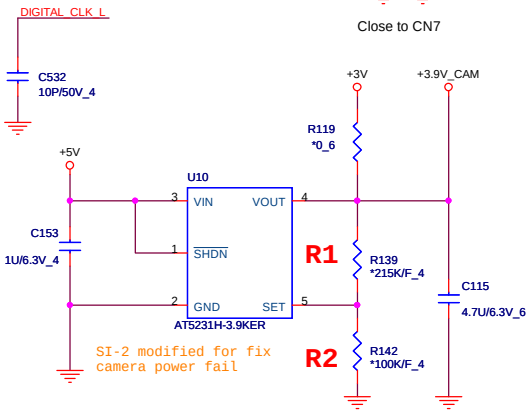
Change CN12 to BL123-05R-5P-L-QT6-A
Add U47 for Finger print USB signal



USB CAMERA /DIGITAL MIC CONNECT

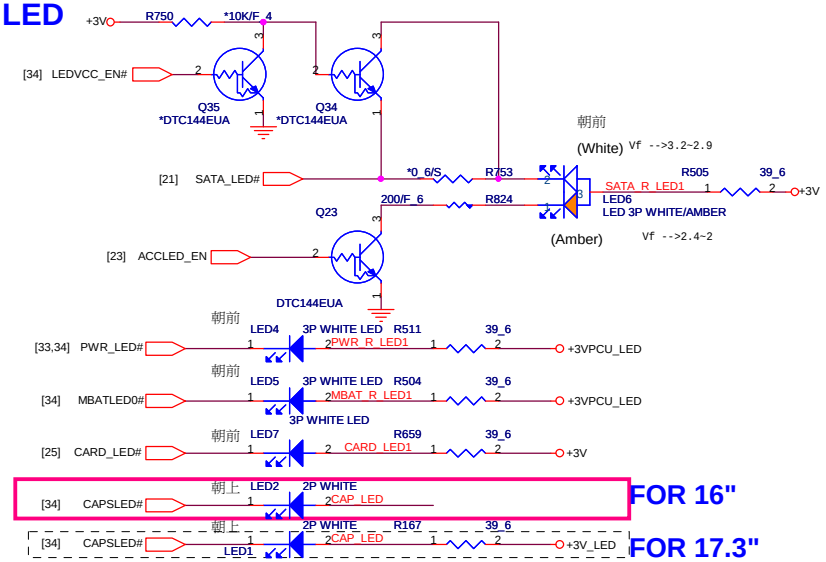


Add for EMI solution



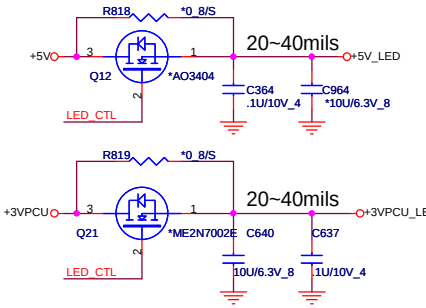
Vout=1.25(1+R1/R2)

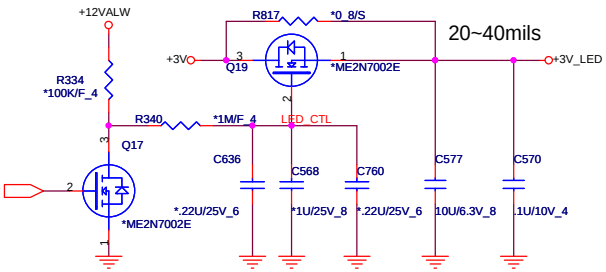
LED



LED PWR CONTROL

Change Q12 to AO3404 as LED current limited





MB5	PROJECT : UT3/5 Quanta Computer Inc.	
Size: Custom	Document Number: BT/WC/FT/TS/ESATA/USB	Rev: PV
Date: Monday, October 20, 2008	Sheet 29 of 43	

T : Stuffed for RTL8111C(10/100/1000)

E : Stuffed for 8101E/8102E(10/100)

For 8102E/8111C

[31] +CTRL15 — R648 *0_6 — +CTRL15_E
Stuffed for 8102E

[31] +FB12 — R641 *0_6/S — +LAN_A1.8_FB12
Stuffed for RTL8111C and nostuff 8102E

+LAN_D1.5 — R649 *0_6/S — +LAN_D1.5_SRVDD
Stuffed for 8102E/RTL8111C

+3VLANVCC — R647 *0_6/S — +CTRL15_E
C894 10U/6.3V_8 — C889 10U/6.3V_8 — C890 .1U/10V_4
+3VLANVCC — R247 *0_6/S — +3V_GVDD
enable switch regular
Stuffed for RTL8111C(10/100/1000)

Y2 25MHZ
C427 33P/50V_4 — C420 33P/50V_4
C414 *.1U/10V_4 — C417 *.1U/10V_4 — R233 2.49K/F_4 — LANRSET
PV MODIFY

8102E No Mount
8111C No Mount ,R247 mount

U18#63 wider than 40 mils
U18#1 wider than 60 mils

U18 — RTL8111C-VB-GR — Pin 65

Isolate pull low:
1.Can only disable RTL8111C.
2.RTL8101E can't disable

for 93C56 used. NC if 93C46 is used.
R653 *10K/F_4 — U43 *M93C46-WMN6TP — C897 *.1U/10V_4
3.24K/F_4 R652

C531 .1U/10V_4
New add and Close to Pin 5
From Vendor EMI suggest

R434
8111C = No Mount
8102E = Mount

R263 *1K/F_4 — R262 15K/F_4
Change back to R261 at 1/24
ISOLATEB — R261 100/F_4 — D38 *RB501V-40 — LAN_DISABLE# [34]

if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

R252 *0_6/S — R259 *0_6/S — LAN-AGND

T3 T4

PCIE_RXN1_LAN_L — C452 .1U/10V_4 — PCIE_RXN1_LAN [22]
PCIE_RXP1_LAN_L — C442 .1U/10V_4 — PCIE_RXP1_LAN [22]
CLK_PCIE_LAN# — CLK_PCIE_LAN# [2]
CLK_PCIE_LAN — CLK_PCIE_LAN [2]
PCIE_TXP1_LAN — PCIE_TXP1_LAN
PCIE_TXN1_LAN — PCIE_TXN1_LAN
PCIE_WAKE# — PCIE_WAKE#
PLTRST# — R248 *0_4/S
LAN_REST# — R246 *0_4

Swap PCIE from Port 6 to PCIE Port 1
Swap PCIE from Port 6 to PCIE Port 2

AL08111C001 IC CTRL(64P) RTL8111C-VB-GR(QFN)
AL08102E001 IC CTRL(64P) RTL8102E-VB-GR(QFN)

Remove 8111B and 8101E support in PV Build
1. Delete R264 (For 8111B)
2. Delete R650 and T28
3. Delete R651 and U18#33 for 8111B support
4. Delete R231 as RSET
5. Delete R242,R243,R244,R245,C394,C395 8101E support

LAN_GLINK10# — D36 BAT54A
LAN_GLINK100#
LAN_GLINK1000# — D35 — RB501V-40 — LAN_GLED#
LAN_TX# — R109 *0_4/S — LAN_YLED#
C48 *.01U/16V_4 — C88 *.01U/16V_4

Link

Stuffed for RTL8101E
+LAN_A1.8 — R589 *0_4

Add C898,C899,C900,C902 as HP request

U33 NS892402
C782 .01U/16V_4 — C783 .01U/16V_4 — C789 .01U/16V_4 — C790 .01U/16V_4
V_DAC
MDI0+ MDI0- MDI1+ MDI1- MDI2+ MDI2- MDI3+ MDI3-
TD1+ TD1- TD2+ TD2- TD3+ TD3- TD4+ TD4-
MX1+ MX1- MX2+ MX2- MX3+ MX3- MX4+ MX4-
SI Build
LAN_MCT0 — C898 0.01U/100V_0603 — R544 75/F_4 — LAN_MX0+ [36] — LAN_MX0- [36]
LAN_MCT1 — C899 0.01U/100V_0603 — R545 75/F_4 — LAN_MX1+ [36] — LAN_MX1- [36]
LAN_MCT2 — C900 0.01U/100V_0603 — R547 75/F_4 — LAN_MX2+ [36] — LAN_MX2- [36]
LAN_MCT3 — C902 0.01U/100V_0603 — R548 75/F_4 — LAN_MX3+ [36] — LAN_MX3- [36]
C781 1000P/3KV_1808

FOR EMI
C89 *.1U/10V_4
RJ45 CN24
+3V_LAN — R89 330/F_4 — LAN_GLED — LAN_GLED# — LED_GRE_P LED_GRE_N
LAN_MX3- LAN_MX3+ LAN_MX1- LAN_MX2- LAN_MX2+ LAN_MX1+ LAN_MX0- LAN_MX0+ — RX1- RX1+ RX0- TX1- TX1+ RX0+ TX0- TX0+
GND1 GND
FOR EMI
+3V_LAN — R87 330/F_4 — LAN_YLED — LAN_YLED# — LED_YEL_P LED_YEL_N
SI Build
C81 *.1U/10V_4
RJ45_CONN

NS892402:GIGABIT
NS892405:10/100

DB0AT9LAN05
DB0ZB1LAN04

PROJECT : UT3/5
Quanta Computer Inc.
Size: Custom — Document Number: NV-L111C/8101E/RJ45 — Rev: PV
Date: Monday, October 20, 2008 — Sheet 30 of 43

T : Stuffed for RTL8111C(10/100/1000)

E : Stuffed for 8101E/8102E(10/100)

LANVCC
1.2W
364mA

+3VLANVCC

Power trace Layout 寬度> 30mil

+3V_LAN

C454 .1U/10V_4
C475 .1U/10V_4
C477 .1U/10V_4
C399 .1U/10V_4

these CAP are for LAN CHIP LANVCC pins--16, 37, 46 and 53.placement close lan chip

C385 4.7U/6.3V_6
C480 .1U/10V_4

+3V_A_LAN

C401 .1U/10V_4
C434 .1U/10V_4

these CAP are for LAN CHIP LAN_A3.3 pins-- 2 and 59.placement close lan chip

8111C CV-4706MN00
8102E CS00004JA40

For Giga must change L65 to Inductor (Chipset include switch power)

+CTRL18 will become to switch power phase

placement close to lan chipset

L54 for Gaga lan use 4.7uH power choke
A>500mA tolerance ±15%

SI Build

+CTRL18

L65 4.7UH_2016

+FB12 [30]

L63 *0_8/S

Power trace Layout 寬度> 30mil

+LAN_A1.8

C884 *4.7U/6.3V_6

C931 *10U/6.3V_8 SI build
C930 10U/6.3V_8 SI build
C881 4.7U/6.3V_6
C876 4.7U/6.3V_6
C878 .1U/10V_4

C891 .1U/10V_4
C892 .1U/10V_4
C875 .1U/10V_4
C893 .1U/10V_4

these cap are for lan chip LAN_A1.8 pins--5, 8, 11 and 14. placement close chip

For 8102E

STUFF 100 ohm BEAD

+LAN_E1.8

R250 *0_8/S

C422 Change to 1u for 8102E

C421 .1U/10V_4
C422 1U/6.3V_4

LAN-AGND

these cap are for lan chip LAN_D1.8 pins, such as 22 and 28. placement close lan chip

Remove R250,L63,L66 -->For 8102E

L66 *0_8/S

Only For 8111C application

[30] +CTRL15

L64 *0_8

C883 *4.7U/6.3V_6
C888 *4.7U/6.3V_6
C895 *4.7U/6.3V_6
C896 *.1U/10V_4

For 8102E

+LAN_D1.5

Power trace Layout 寬度> 30mil

C474 .1U/10V_4
C479 .1U/10V_4
C459 .1U/10V_4
C456 .1U/10V_4
C472 .1U/10V_4
C461 .1U/10V_4
C476 .1U/10V_4
C415 .1U/10V_4
C478 .1U/10V_4
C400 .1U/10V_4

these cap are for lan chip LAN_D1.5 pins-- 15, 21, 32, 33, 38, 41, 43, 49, 52 and 58.placement close lan chip

Power domain chart

	RTL8111C(P) RTL8102E
LANVCC	3.3V
LAN_D1.8	1.2V
LAN_A1.8	1.2V
LAN_D1.5	1.2V

C422 change to 1uf

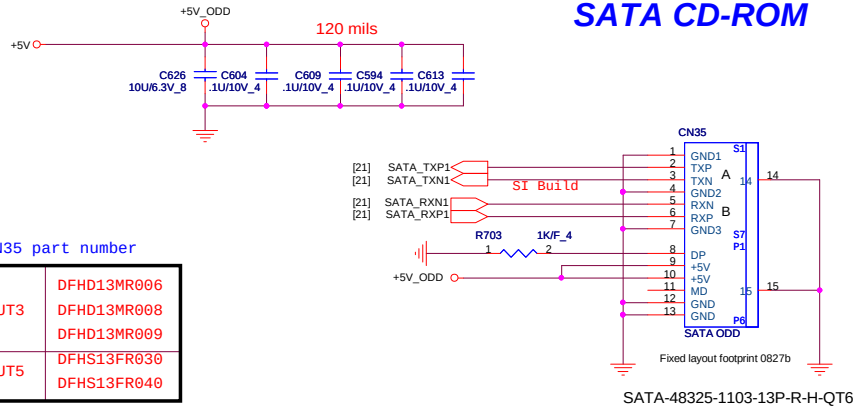
PROJECT : UT3/5
Quanta Computer Inc.

NB5

Size A3 | Document Number LAN Power | Rev PV

Date: Monday, October 20, 2008 | Sheet 31 of 43

SATA CD-ROM



CN35 part number

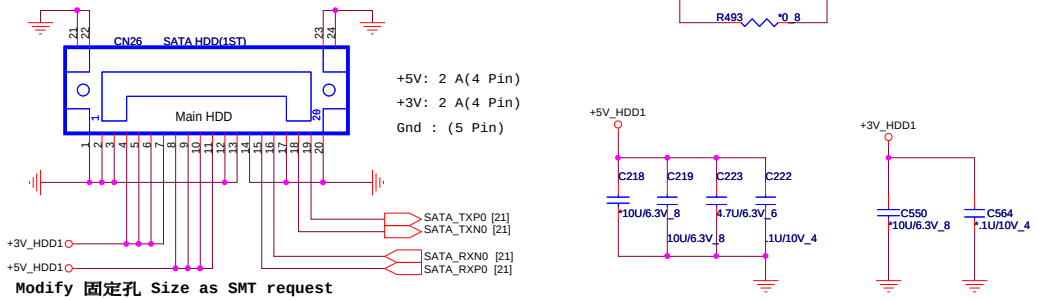
UT3	DFHD13MR006
	DFHD13MR008
	DFHD13MR009
UT5	DFHS13FR030
	DFHS13FR040

SATA-48325-1103-13P-R-H-QT6

SATA HDD CONNECTOR

DFHD20MR005

DC Current rating: 0.5 A



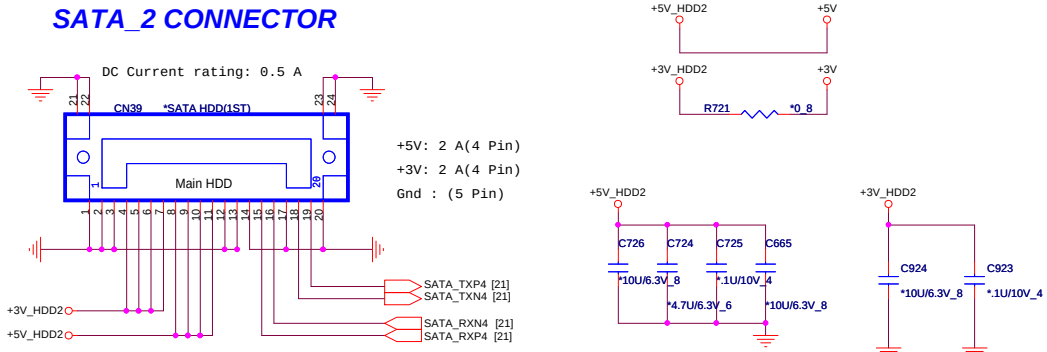
Modify 固定孔 Size as SMT request

GS12201-1011-9F-20P-L-QT6

DB modified

SATA_2 CONNECTOR

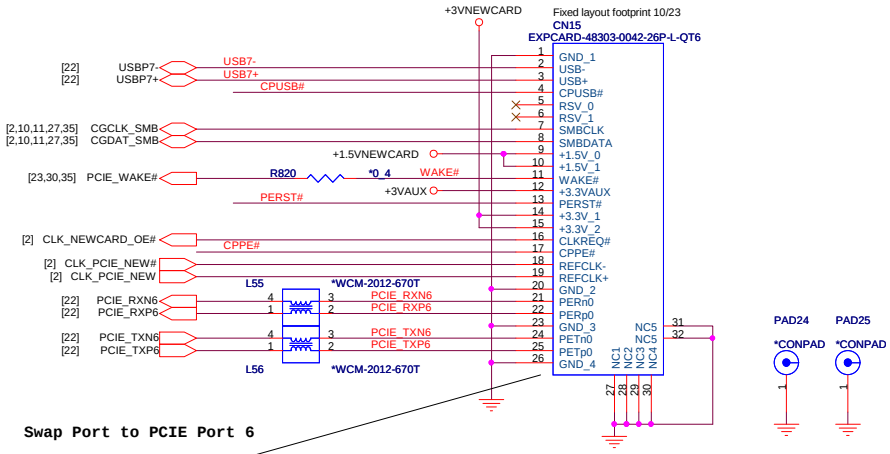
DC Current rating: 0.5 A



NEWCARD

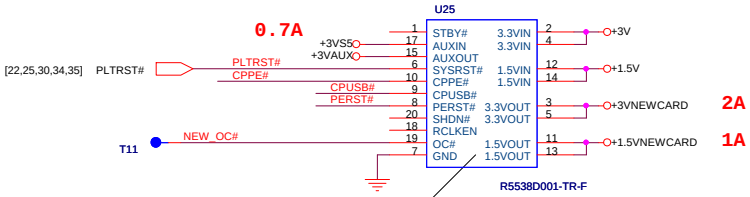
NEWCARD (PCIEXPRESS*1 + USB*1)

32

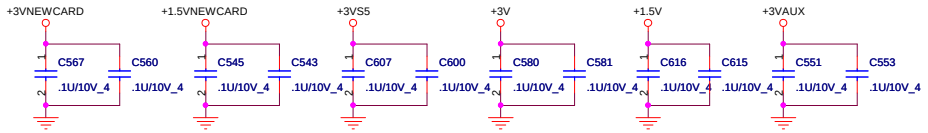


Swap Port to PCIE Port 6

Change CN15#31,32 as ME request for Hole pad
expcard-48303-0042-26p-l-qt6 as ME modify Pad size(pin31,32)
Move CN15#29,30 Pin as ME request(Molex confirm drawing)



add Pin 21~25 as U25 Thermal pad tied to Gnd



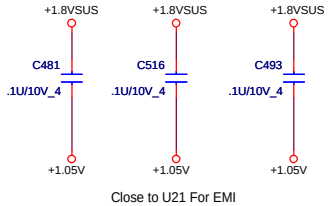
	Header	Housing
MLX	DFHD26MS012	DFHS26FR023
FOX	DFHD26MS013	DFHS26FR024
DGN	DFHD26MS017	DFHS26FR028

NB5

PROJECT : UT3/5
Quanta Computer Inc.

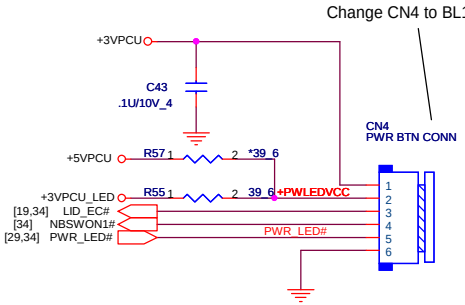
Size	Document Number	Rev
Custom	ODD/HDD/NEW CARD	PV

Date: Monday, October 20, 2008 Sheet 32 of 43



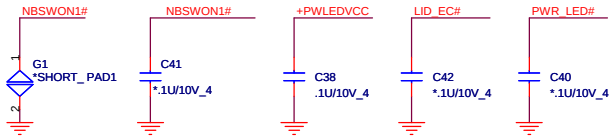
Close to U21 For EMI

Change CN4 to BL123-06R-6P-L-QT6-A



1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH
4. POWERON#
5. PWRLED#
6. GND

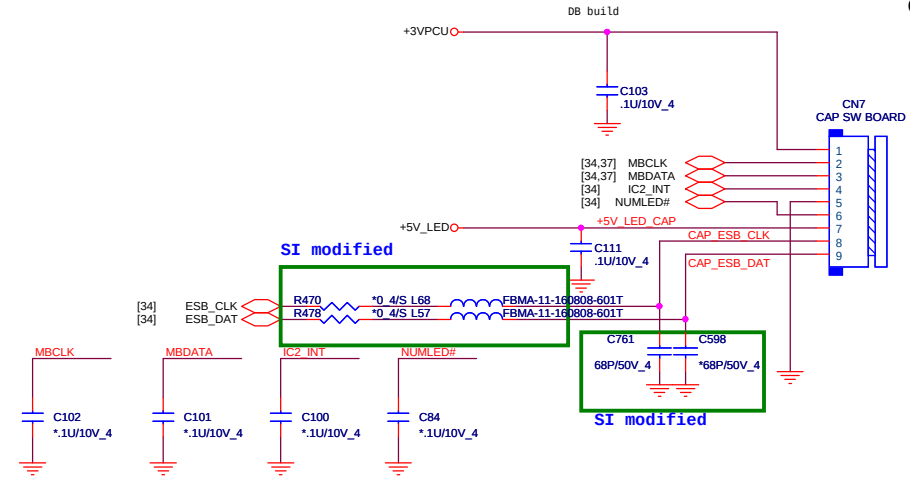
POWER BOTTON CONNECT



EMI 0828

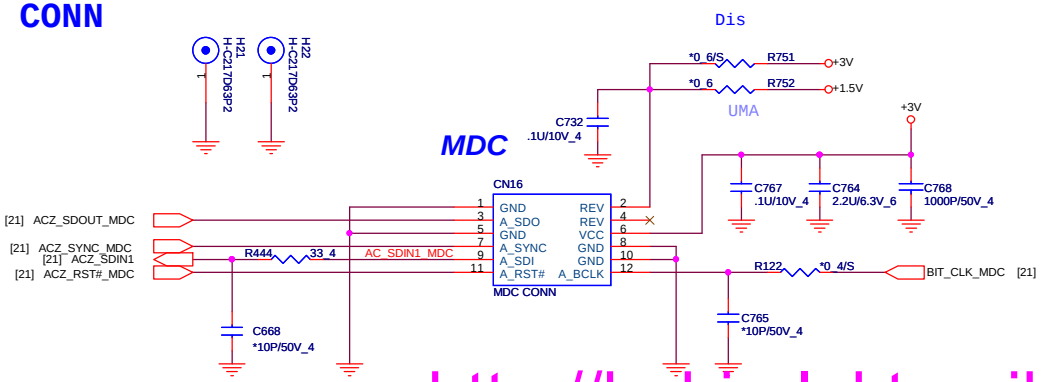
POWRER SW CONNECT

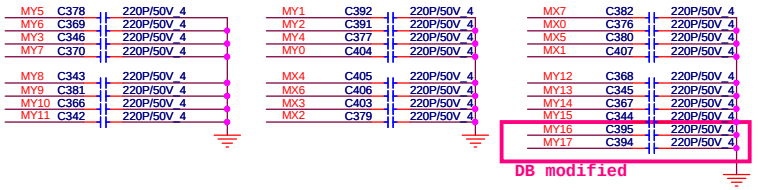
CAP SW CONNECT



1. +3VPCU
2. MBCLK
3. MBDATA
4. CAP_INT
5. GND
6. NUM LOCK LED
7. +5V_LED
8. ESB_CLK
9. ESB_DAT

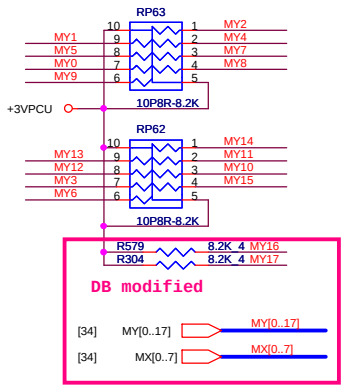
Modem CONN

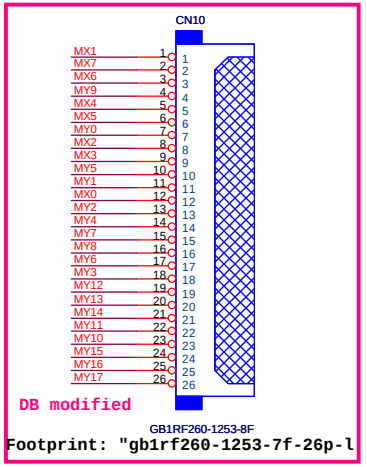




DB modified

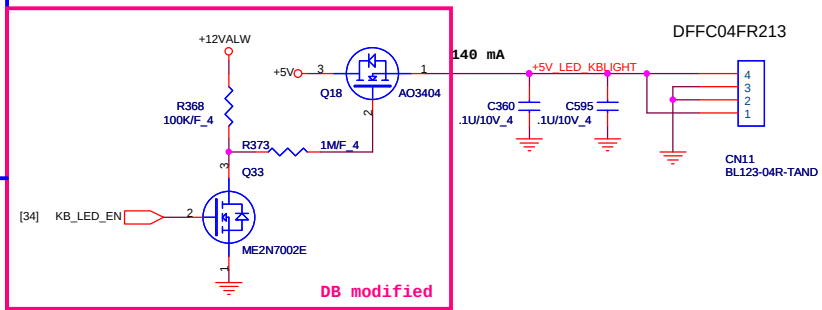
KEYBOARD PULL-UP





clear ABS 758 resin for key cap.
7 LEDs for 15.4" (total LED current 140mA)
11 LEDs for 17" (Total LED current 220mA)

DFFC04FR213



NB5

PROJECT : UT3/5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KB/CAP/POWER CONN/MDC	PV

Date: Monday, October 20, 2008 Sheet 33 of 43

Change U20 layout footprint
to LQFP128-16X16-4-AA1

U20

KB3926QF C0

DB modified

SI modified

R323 remove for KB3926 C version

For KB3926 B, C version

Hi ==> 120W
Low ==> 65W/90W

ID	R374	R379
UT3	10K	N/A
UT5	N/A	10K

R430 Change to 100k ohm ,pull low

Change to RB500 as Current loss

Add Pin 117,103 for DSM,116 for Bluetooth,Pin 23 for Key Beep to Amplifier
Add T37,T38,T39 for EC
Delete T10 and tie pin 117 from Lan for DSM

TOUCH PAD CONNECTOR

25 mils

CN13
TOUCH PAD CONN
DFFC12FR293

TOUCH PAD L/R FOR 16"

TOUCH PAD ON/OFF FOR 16"

close conn

TOUCH PAD L/R FOR 17.3"

TOUCH PAD ON/OFF FOR 17.3"

DB modified

Socket: DG008000031

MXIC AKE38FP0Z00
WINBOND AKE38ZP0N01
EON AKE38ZA0Q00

2M byte
SPI
BIOS

R273
64.9K -->65W CS36492FB17
33.2K -->90W CS33322FB13
Change to 1SS355 as Current loss

PROJECT : UT3/5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KB3926/ROM/TP	PV

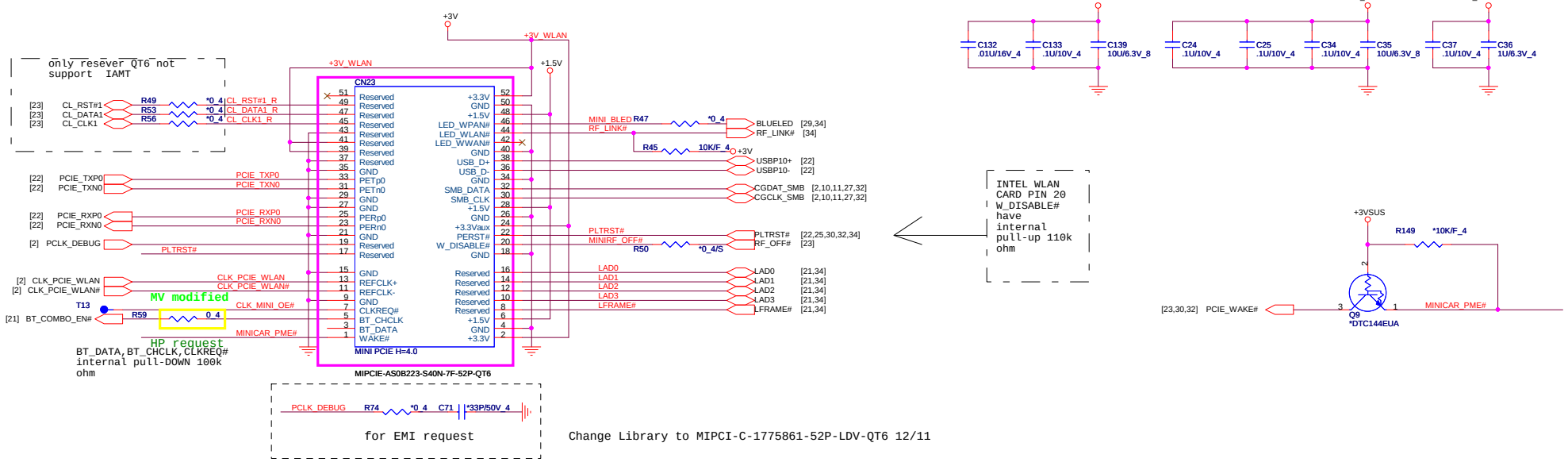
Date: Monday, October 20, 2008 Sheet 34 of 43

Mini PCI-E Card 1
WLAN

Delete R78 and tied the CN23#24 to R110 direction
Change CN23 layout footprint to MIPCIE-AS0B223-S40N-7F-52P-QT6 as ME drawing

Change net name

35



Change Library to MIPCI-C-1775861-52P-LDV-QT6 12/11

M/B Screw Hole

SI-2,h-e276x315d118p2

Modify H16 Hole size
H-TC256BC315D118P2

SI-2

New add as ME request

RF PAD

PAD10 PAD9 PAD6
*EMIPAD

New add as RF request

PAD13 PAD12 PAD11
*EMIPAD

New add as RF request

PAD23

ME PAD

PAD5 PAD4
*EMIPAD

PAD8
*EMIPAD

ME Routed spring

PAD17 PAD19
*Emi157x79 *ME_SPRING

Routed spring

Delete PAD14

PAD15
*MDC_SPRING

PAD16
*MDC_SPRING

EMI PAD

PAD2
*EMIPAD
Del PAD1

MV MODIFY

PAD21 PAD3
*EMIPAD *EMIPAD

ME-Ground Pad

PAD34
PV MODIFY

ME-Ground Pad

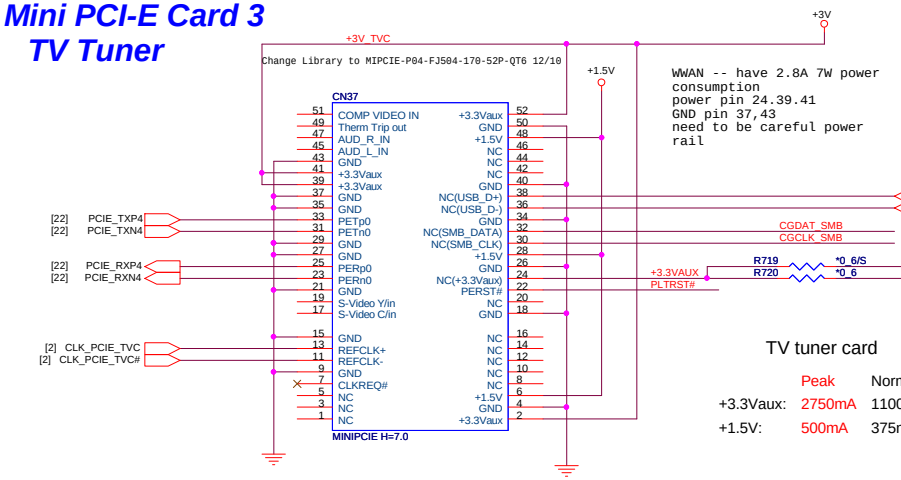
PAD35 PAD36
MV MODIFY

SI modified ME-Ground Pad

PAD26 PAD27 PAD28 PAD29 PAD30 PAD31 PAD32

Del PAD18 (Same as PAD26)

Mini PCI-E Card 3
TV Tuner



TV tuner card

	Peak	Normal
+3.3Vaux:	2750mA	1100mA
+1.5V:	500mA	375mA

PROJECT :	UT3/5
Quanta Computer Inc.	
Size: Custom	Document Number: MINI PCIE CONN X2 & HOLE
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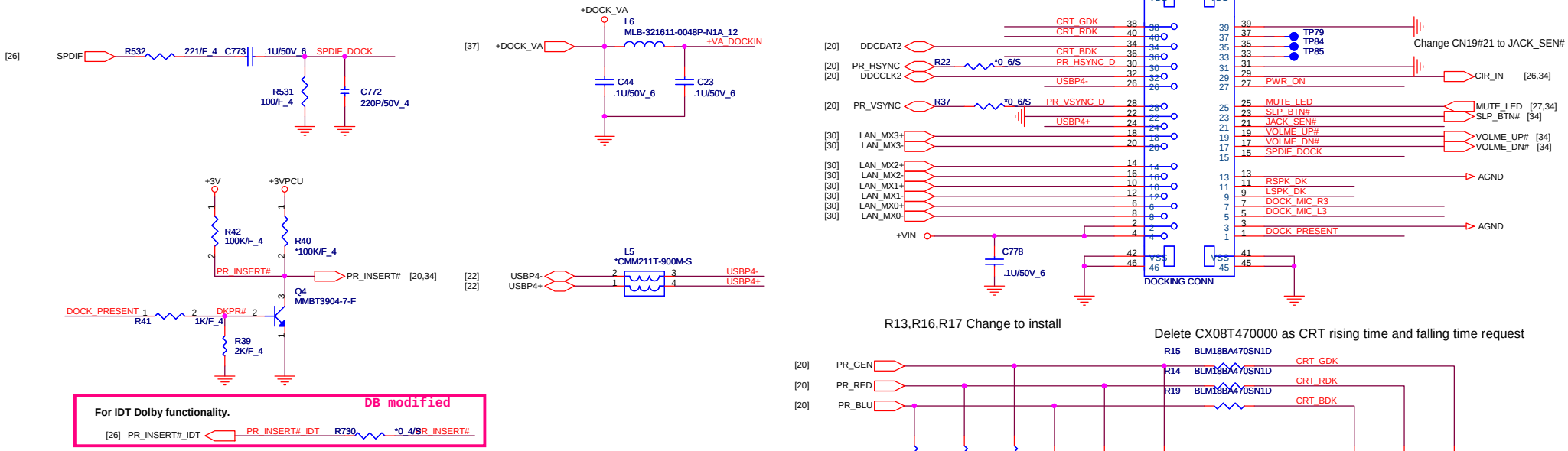
NB5

CABLE DOCK

support 6A 200mils
CX000480005



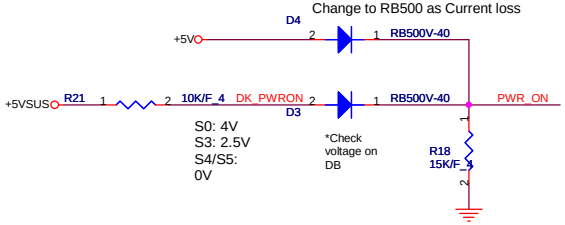
R13,R16,R17 Change to install

Delete CX08T470000 as CRT rising time and falling time request

For IDT Dolby functionality.

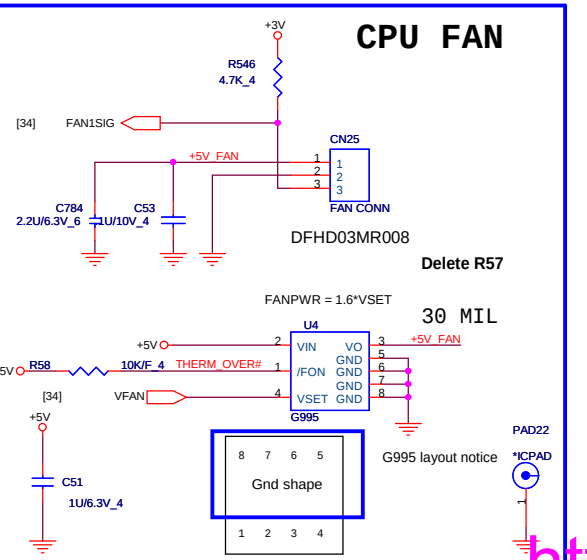
DB modified

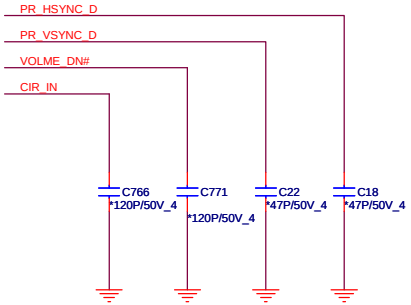
Change to RB500 as Current loss

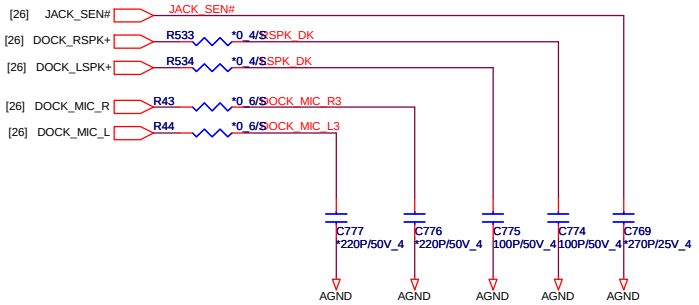


Add Loss net(GND Net)

CPU FAN







Change to Analog Gnd

NB5	PROJECT : UT3/5 Quanta Computer Inc.	
Size: Custom	Document Number: CABLE DOCKING/FAN	Rev: PV
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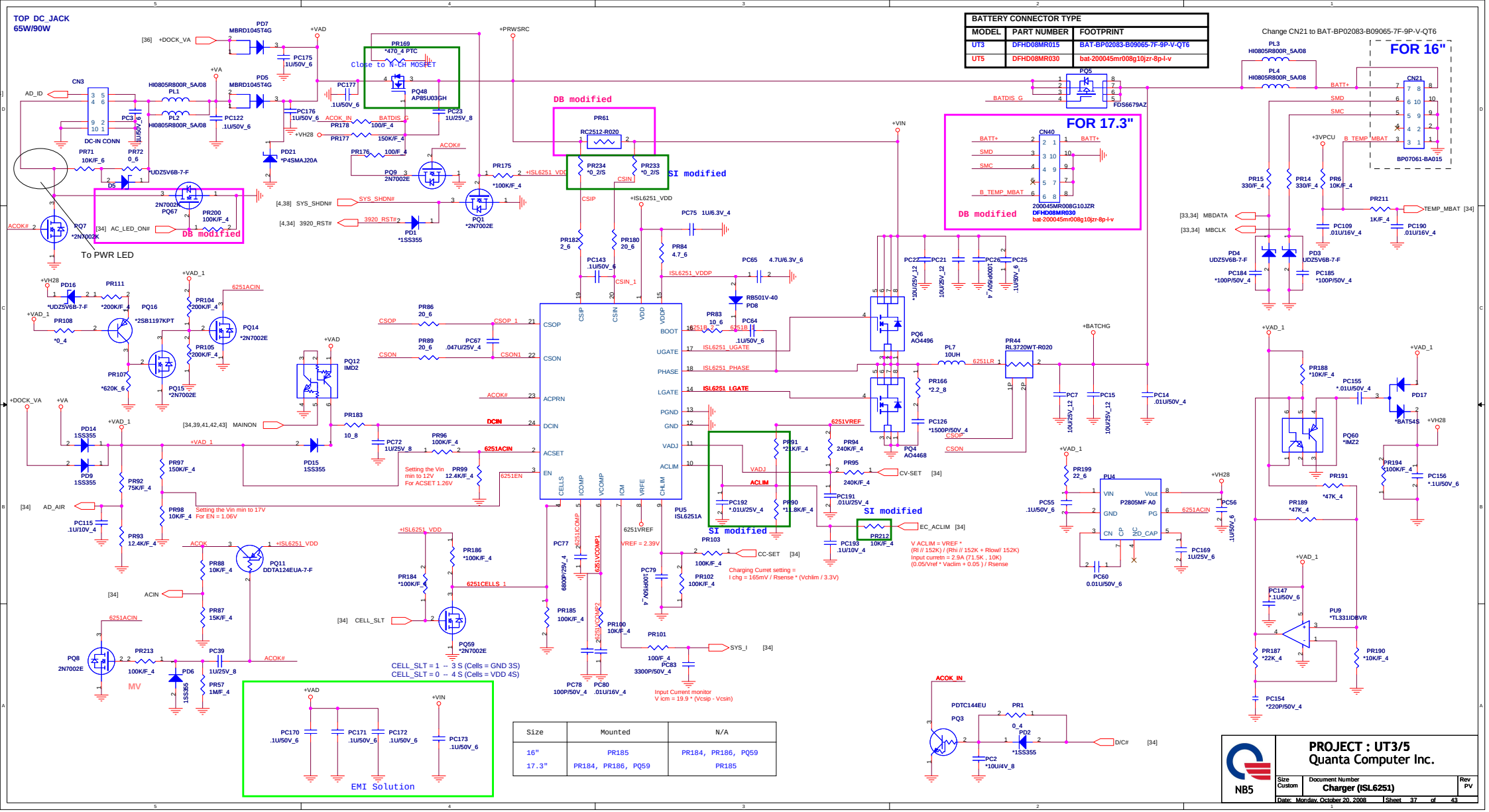


DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+12V_ALW

Place these CAPs close to FETs

Place these CAPs close to FETs

5 Volt +/- 5%
Countinue current:5A
Peak current:7.5A
OCP minimum 10A

3.3 Volt +/- 5%
Countinue current:5A
Peak current:7.5A
OCP minimum 9A

SI modified

SI modified

Rds(on) 20m ohm

Rds(on) 20m ohm

PU2 RT8206B

9	BYP	REFIN2	32
10	OUT1	ILIM2	31
11	FB1	OUT2	30
12	ILIM1	SKIP	29
13	PGOOD1	PGOOD2	28
14	ON1	ON2	27
15	DH1	DH2	26
16	LX1	LX2	25
37	PAD		
36	PAD		
39	PAD		
40	PAD		
38	PAD		42
35	PAD		41
34	PAD		
33	PAD		
17	BST1	BST2	24
18	DL1	DL2	23
19	VDD	PGND	22
20	N.C	AGND	21

1	DOREFIN	REF	8
2	LDO	TON	7
3	IN	VCC	6
4	N.C	ONLDO	5

PD48 UDZ5V6B-7-F

PD12 PD13 BAV99 BAV99

PQ55 AO4496 PQ47 AO4468 PQ49 AO4496 PQ50 AO4468

PL8 2.5uH/7.5A PL9 2.5uH_7.5A

PR21 1K/F_4 PR19 150K/F_4 PR22 *0_6/S PR214 *0_4 PR26 *47_6 PR25 *0_4 PR20 *0_4/S PR23 *0_4/S PR27 309K/F_4 PR39 309K/F_4 PR165 *2.2_8 PR31 *0_4 PR35 0_4 PR69 4.7_6 PR47 4.7_6 PR73 *0_6/S PR45 100K/F_4 PR168 *2.2_8 PR129 *1500P/50V_4 PR29 0_4 PR33 *0_4 PR36 *0_4/S

PC29 10U/25V_12 PC31 1000P/50V_4 PC30 .1U/50V_6 PC9 4.7U/6.3V_6 PC130 *0.1U/10V_4 PC13 .1U/50V_6 PC12 .1U/10V_4 PC11 1U/6.3V_4 PC4 .1U/50V_6 PC125 1000P/50V_4 PC6 10U/25V_12 PC134 330U/6.3V_6X5.8 PC135 .1U/10V_4 PC124 *1500P/50V_4 PC186 3300P/50V_4 PC49 .1U/50V_6 PC34 .1U/50V_6 PC62 .01U/50V_6 PC63 .01U/50V_6 PC52 1U/6.3V_4 PC70 0.1U/25V_8 PC71 2.2U/50V_8 PC138 .1U/10V_4 PC144 330U/6.3V_6X5.8 PC180 *.1U/10V_4 PC181 *.1U/10V_4

+VIN +5VALW +5V_VCC1 +5VPCU +5V_ALWP +3VPCU +3.3V_ALWP +12VALW +15VALW

5V_DH 5V_LX 5V_DL 3V_LX 3V_DH 3V_DL PGOOD1 PGOOD2

[4,37] SYS_SHDN#

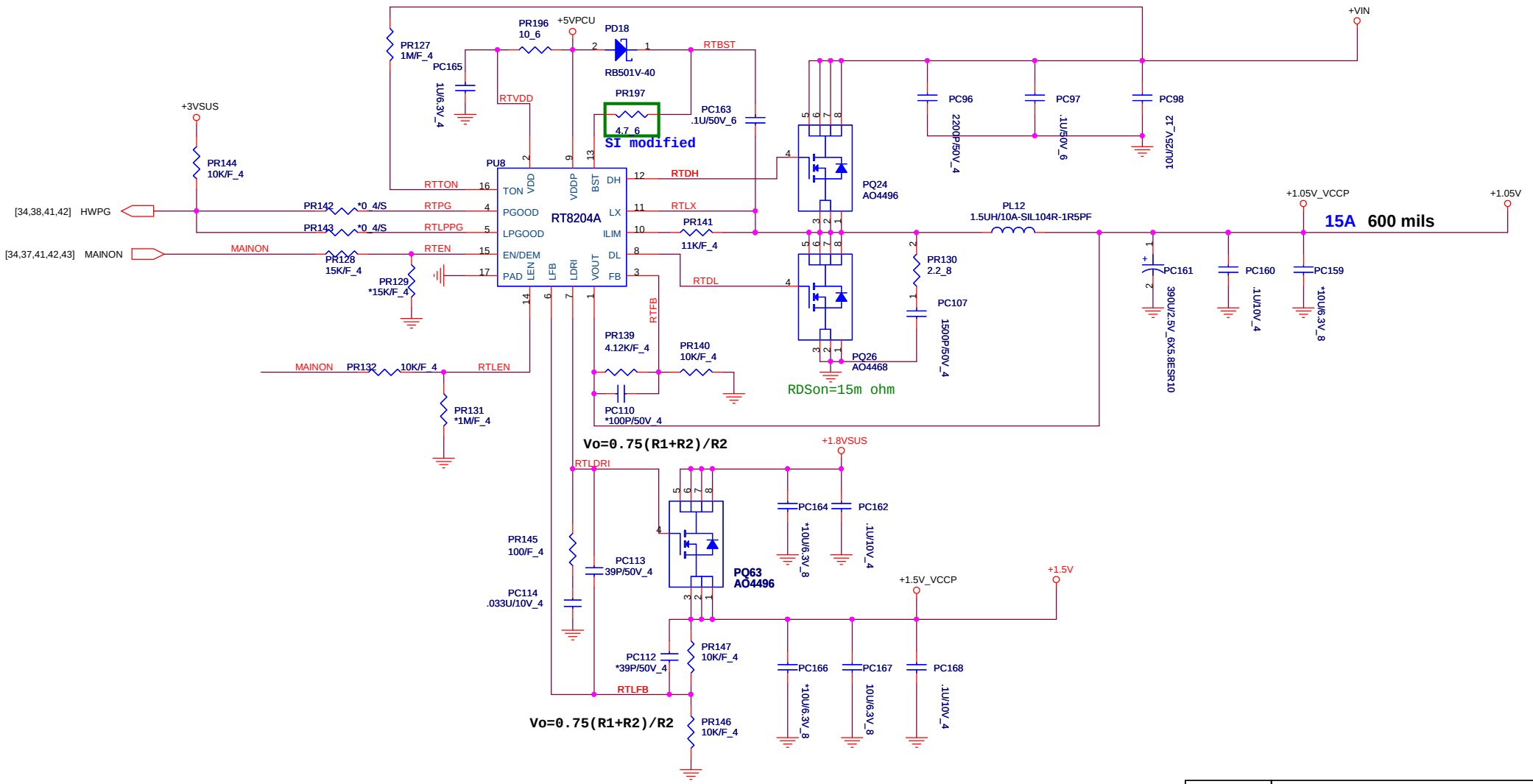
HWPG [34,39,41,42]

EMI reserved

NB5	PROJECT : UT3/5 Quanta Computer Inc.	
	Size B / Document Number +5V/+3V (ISL6237)	Rev PV
	Date: Monday, October 20, 2008	Sheet 38 of 43

VCCP1.05V & +1.5V

+1.05Volt +/- 5%
Countinue current:7.5A
Peak current:10A
OCP minimum 15A



NB5

PROJECT : UT3/5
Quanta Computer Inc.

Size	Document Number	Rev
B	+1.05V/+1.5V (RT8204)	PV

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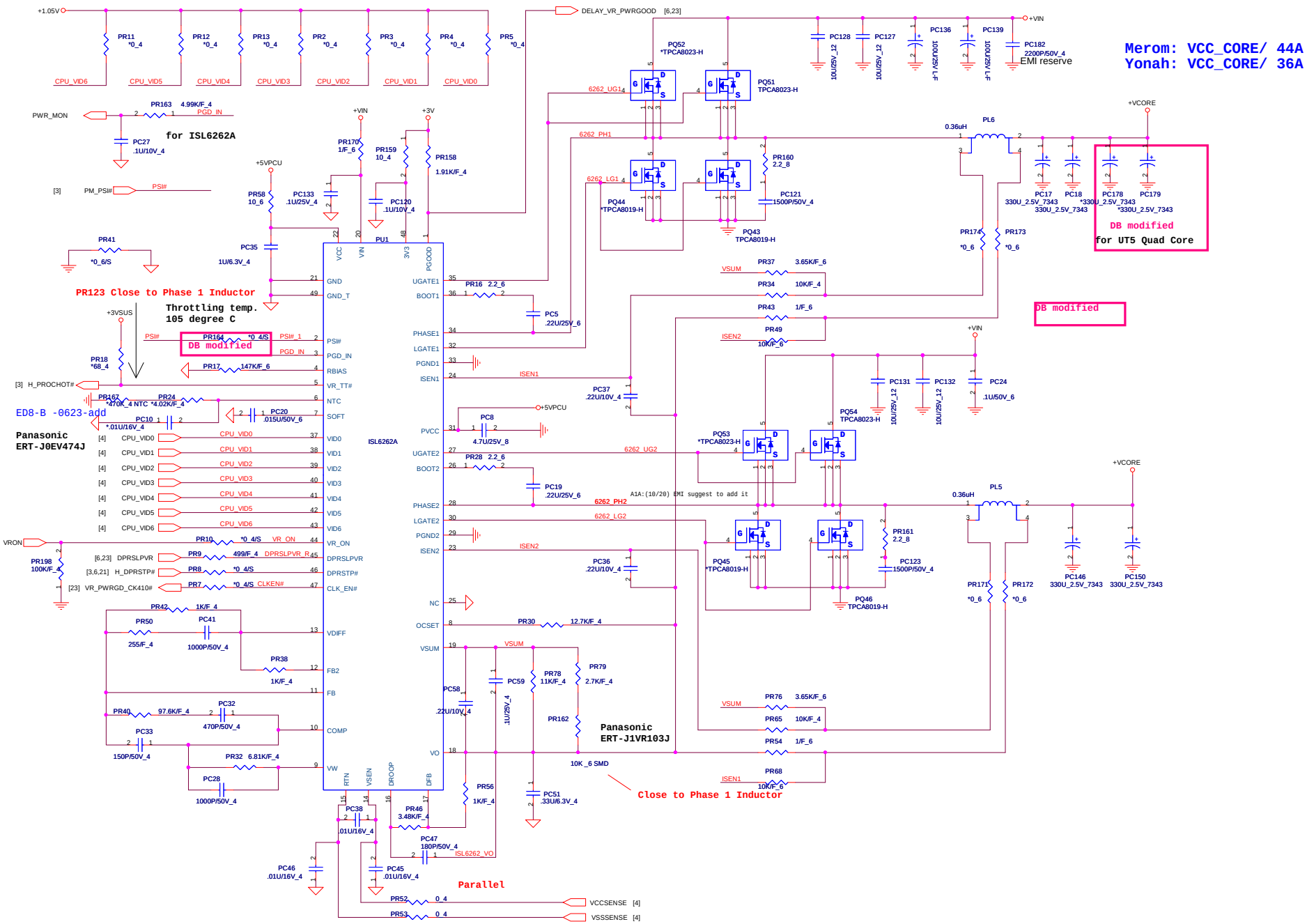
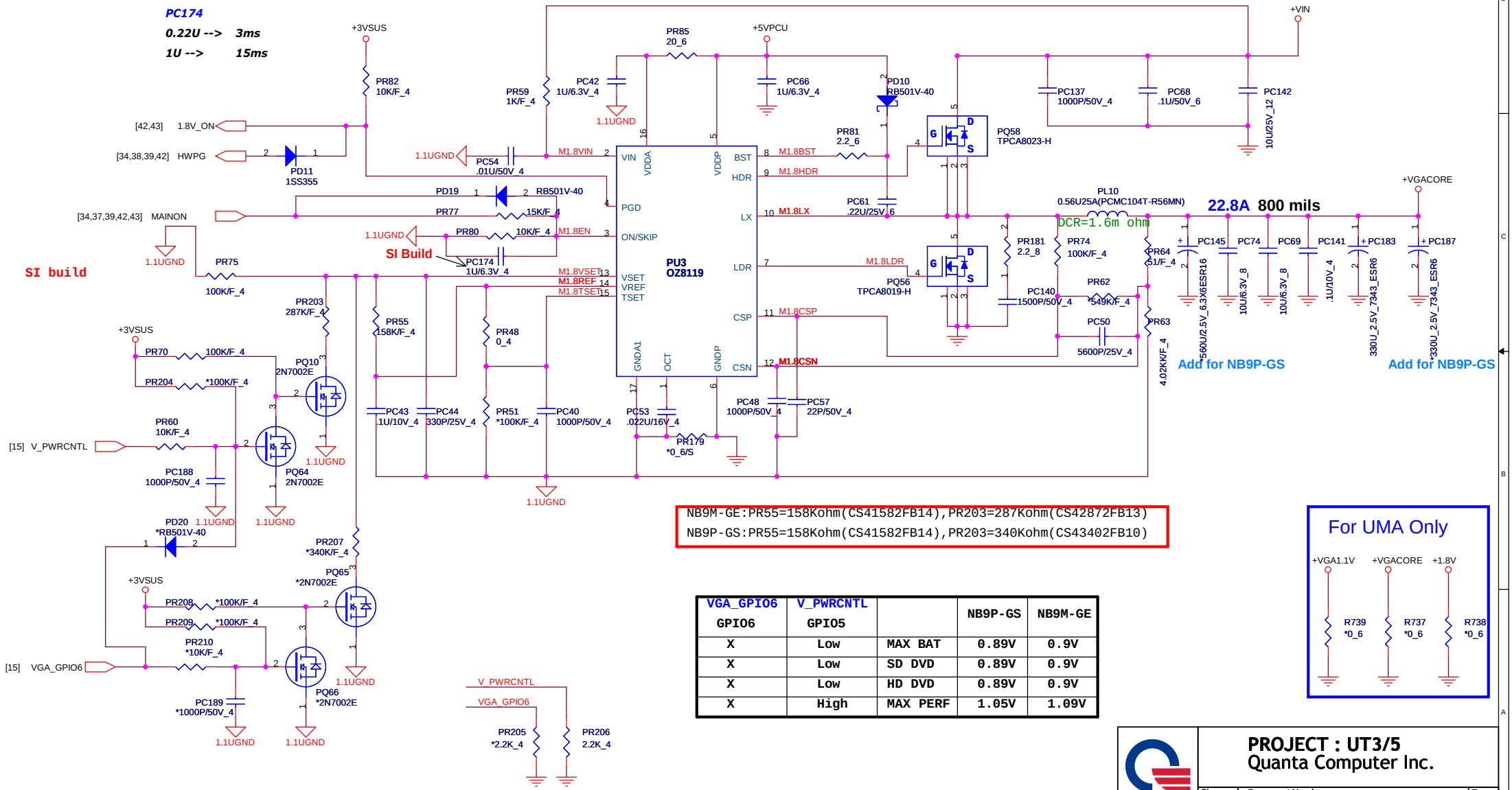


VGA Core & VCC1.1

+1.1Volt +/- 5%
Countinue current:17.54A
Peak current:22.8A
OCP minimum 23A



NB9M-GE:PR55=158Kohm(CS41582FB14),PR203=287Kohm(CS42872FB13)
NB9P-GS:PR55=158Kohm(CS41582FB14),PR203=340Kohm(CS43402FB10)

VGA_GPIO6 GPIO6	V_PWRCNTL GPIO5		NB9P-GS	NB9M-GE
X	Low	MAX BAT	0.89V	0.9V
X	Low	SD DVD	0.89V	0.9V
X	Low	HD DVD	0.89V	0.9V
X	High	MAX PERF	1.05V	1.09V

NB5

PROJECT : UT3/5
Quanta Computer Inc.

Size	Document Number	Rev
B	VGA Core OZ8119	PV

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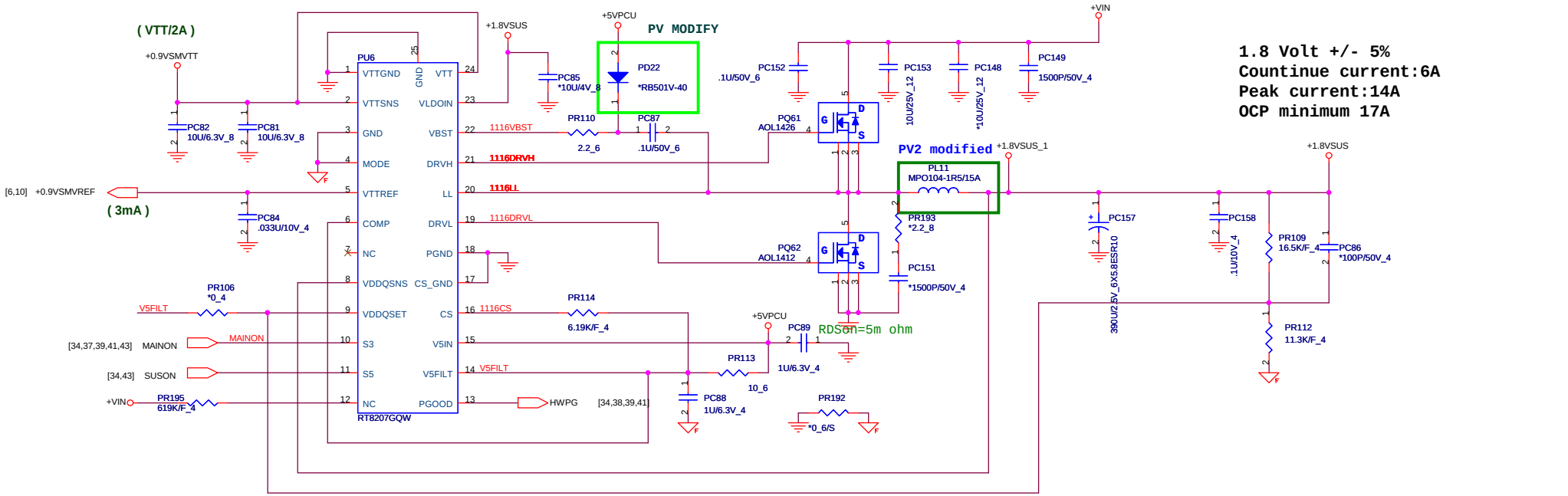
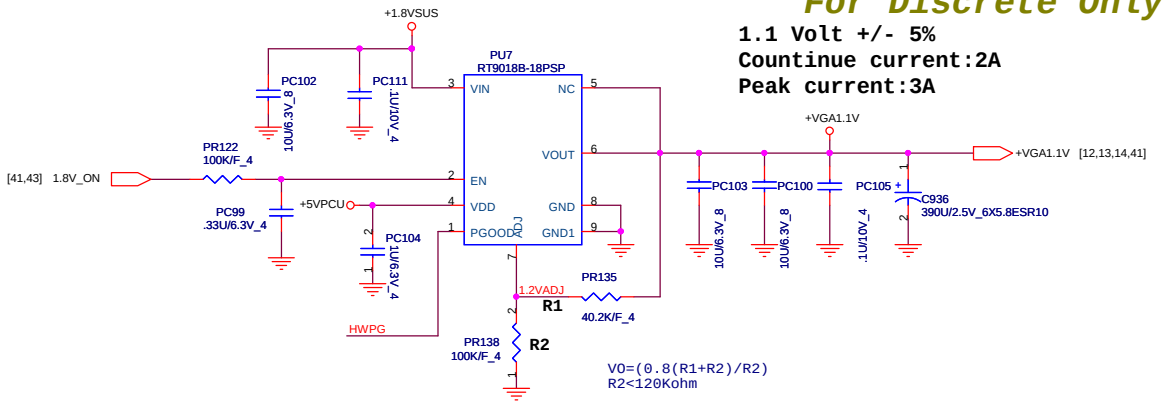
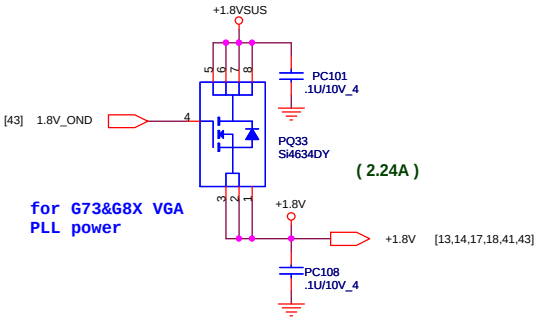


Change PR122 tied to 1.8V_ON as power sequence reuqest





PROJECT : UT3/5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	1.8V/DDR_VTER/+1.8v/+1.1V	PV

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NB5