Compal confidential

Schematics Document

Mobile Penryn uFCPGA with Intel Cantiga_GM+ICH9-M core logic

2008-01-01

Diễn Đàn
KyThuatViTinh.Com

Digitally signed by dd
DN: cn=dd, o=dd, ou=dd, email=dddd@yahoo.com, c=US
Date: 2009.11.12 09:03:29 +07'00'

機密 等級 硬體二部
產出人員
產出日期
解密日期

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Title: *Cover Sheet*

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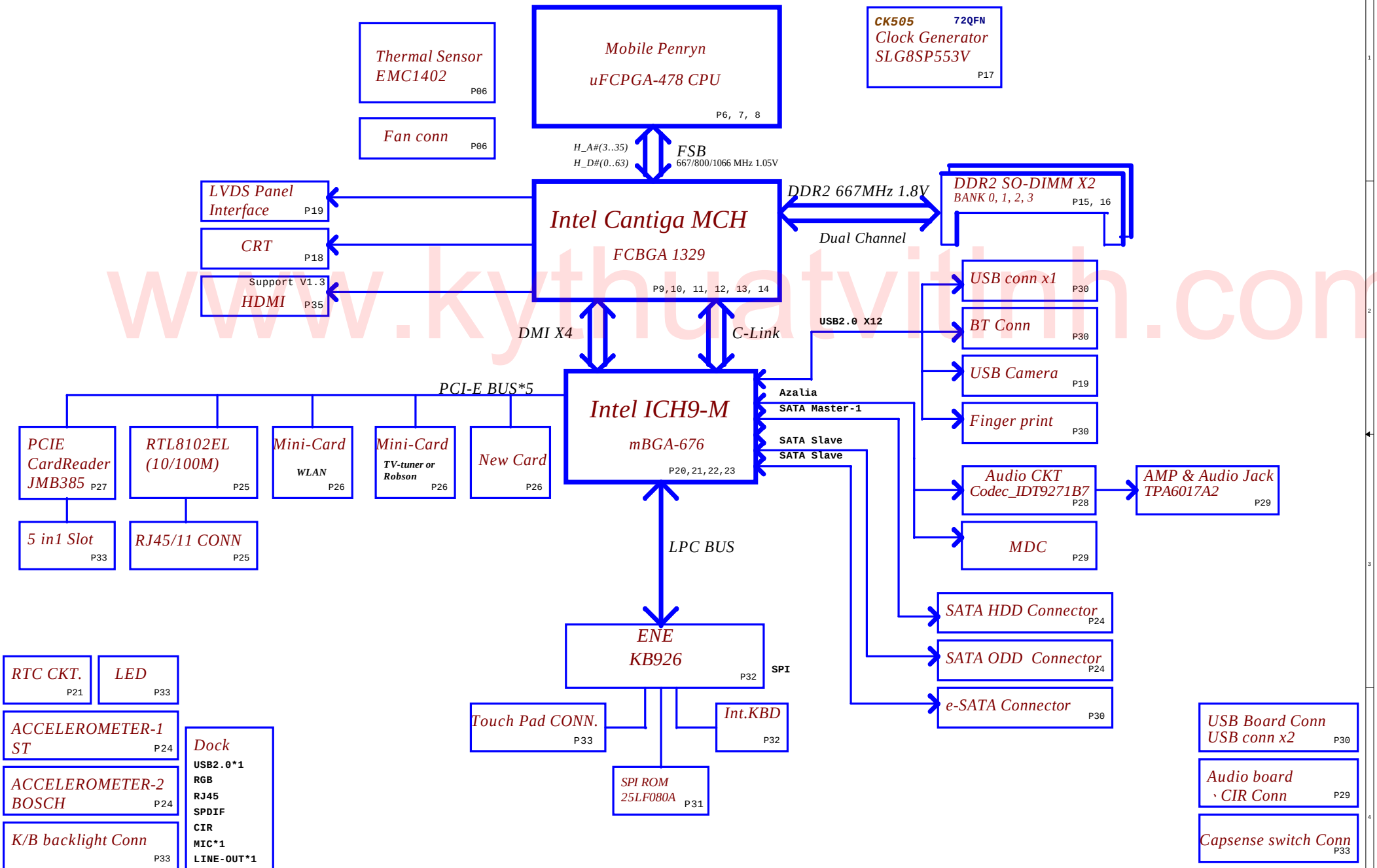
Montevina Consumer 14" UMA



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Title	Block Diagram		
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Voltage Rails

O MEANS ON X MEANS OFF

power plane / State	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE +2.5VS +1.8VS
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :

: means Digital Ground

: means Analog Ground

@ :	means just reserve , no build
45@ :	means need be mounted when 45 level assy or rework stage.
DEBUG@ :	means just reserve for debug.
BATT @ :	means need be mounted when 45 level assy or rework stage.
CONN@ :	means ME part
ESATA @ :	means just reserve for ESATA
GS @ :	means just reserve for G sensor
FP @ :	means just reserve for Finger Print
Multi @ :	means just reserve for Multi Bay
NewC@ :	means just reserve for New card
DOCK@ :	means just reserve for Docking
Main@ :	means just reserve for Main stream
OPP@ :	means just reserve for OPP
2MiniC@ :	means just reserve for 2nd Mini card slot

USB assignment:

USB-0	Right side
USB-1	Right side
USB-2	Left side(with ESATA)
USB-3	Dock
USB-4	Camera
USB-5	WLAN
USB-6	Bluetooth
USB-7	Finger Printer
USB-8	MiniCard(WWAN/TV)
USB-9	Express card
USB-10	X
USB-11	X

PCIe assignment:

PCIe-1	TV /WWAN/Robeson
PCIe-2	X
PCIe-3	WLAN
PCIe-4	GLAN (Realtek)
PCIe-5	Card reader
PCIe-6	New Card

SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	Thermal Sensor	SODIMM	CLK CHIP	MINI CARD	LCD	Cap sensor board	NEW CARD	G sensor
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X	V	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X	X	V	V
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V	X	X	X

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

43154432L01 : Main@/DEBUG@/DOCK@/NewC@/FP@/ESATA@/GS@/Multi@/2MiniC@
43154432L02 : Main@/DEBUG@/DOCK@/NewC@/FP@/ESATA@/GS@/2MiniC@
43154432L03 : Main@/DEBUG@/DOCK@/NewC@/FP@/2MiniC@
43154432L04 : OPP@/DEBUG@
43154432L05 : OPP@/DEBUG@

43154432L01 : UMA GM PA FF (SI-1)
43154432L02 : UMA GM PR FF (SI-1)
43154432L03 : UMA GL PR FF-
43154432L04 : UMA GM OPP (SI-1)
43154432L05 : UMA GL OPP

Cantiga GM45 B0(QR32) : SA00001P930
ICH9M A2 ES2 Base : SA00002AN10

DA600007100 --->Main
DAZ03V00100 --->OPP

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Title: Notes List

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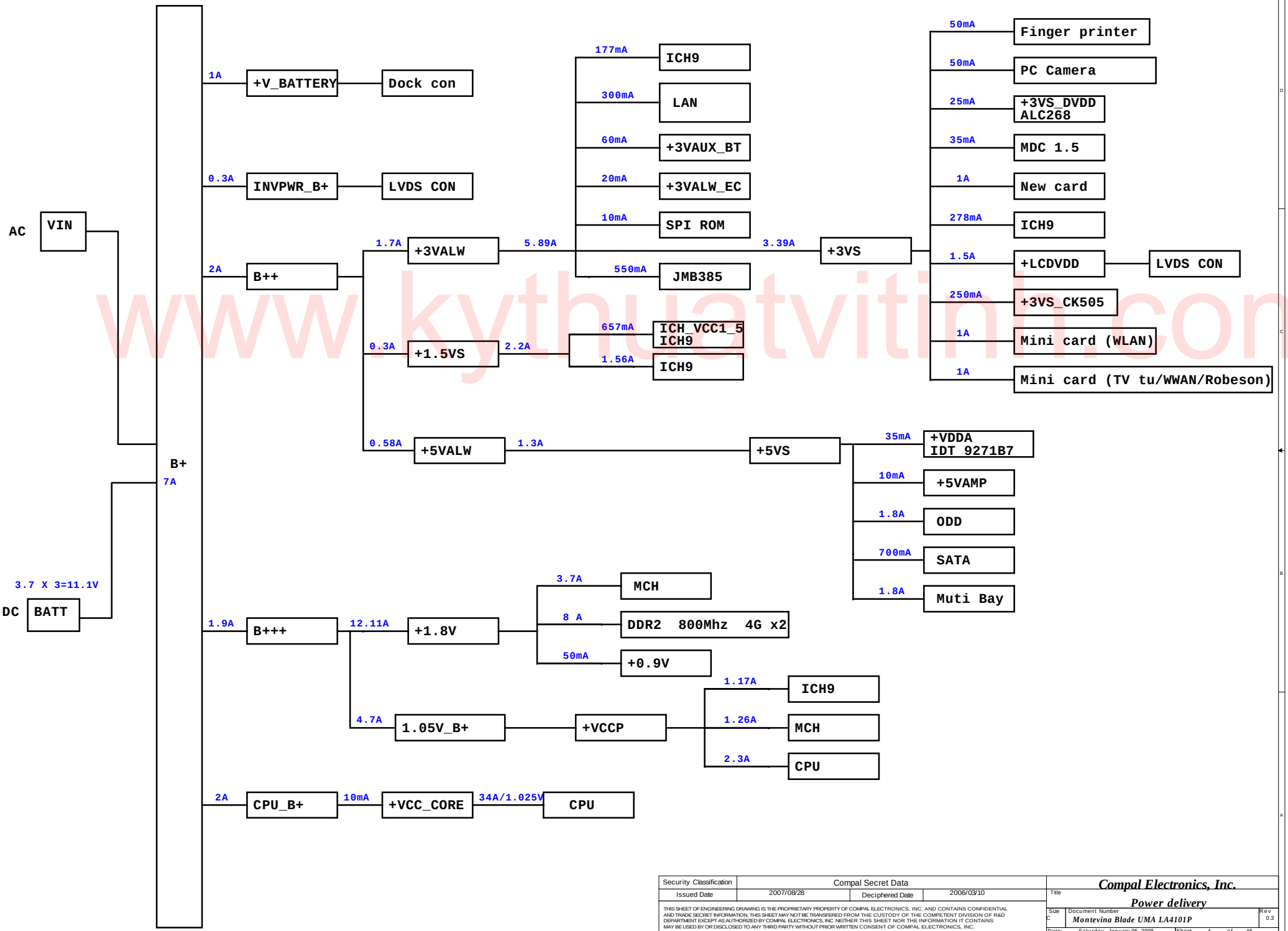

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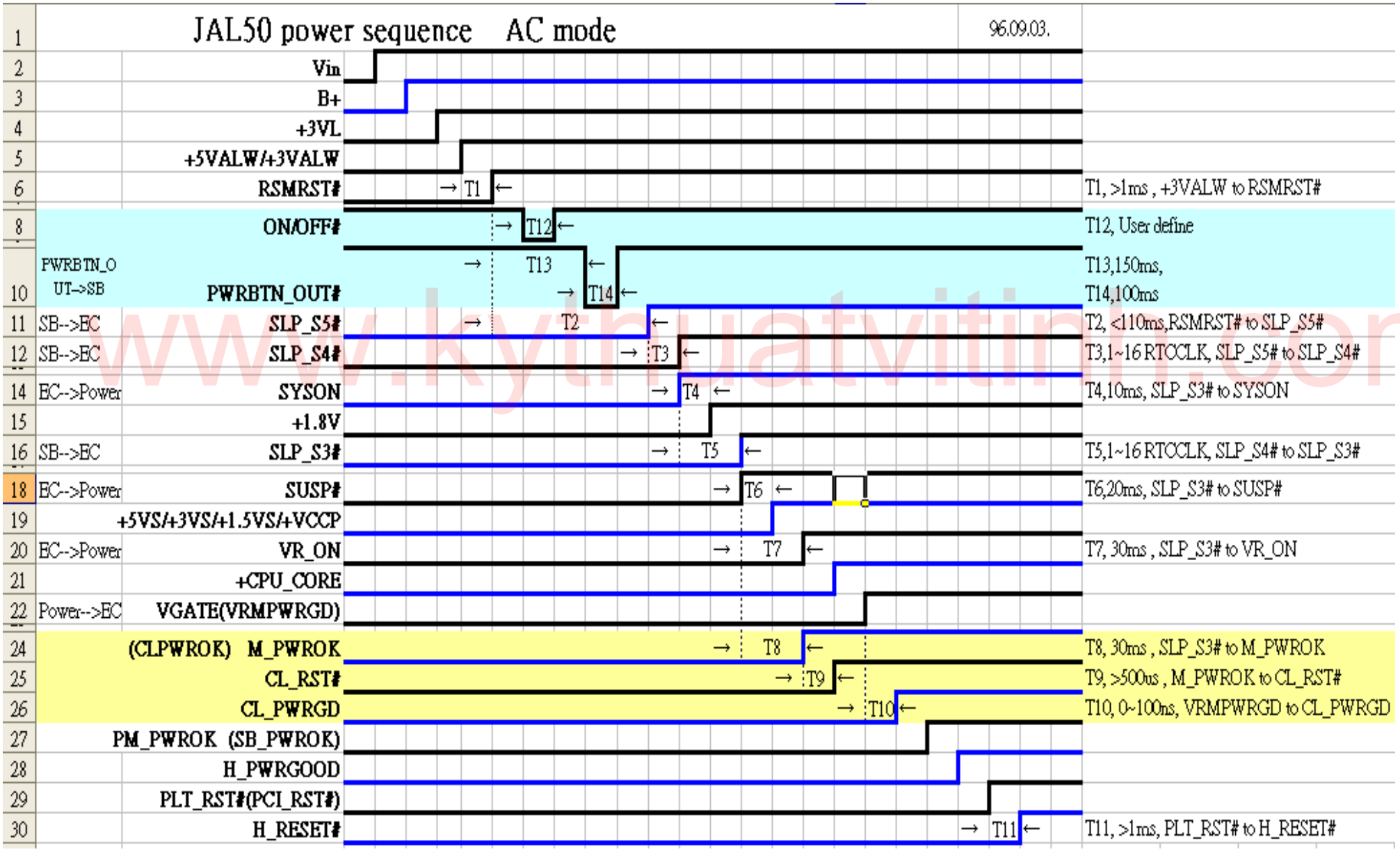

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Compal Electronics, Inc.

Title: **Power sequence**

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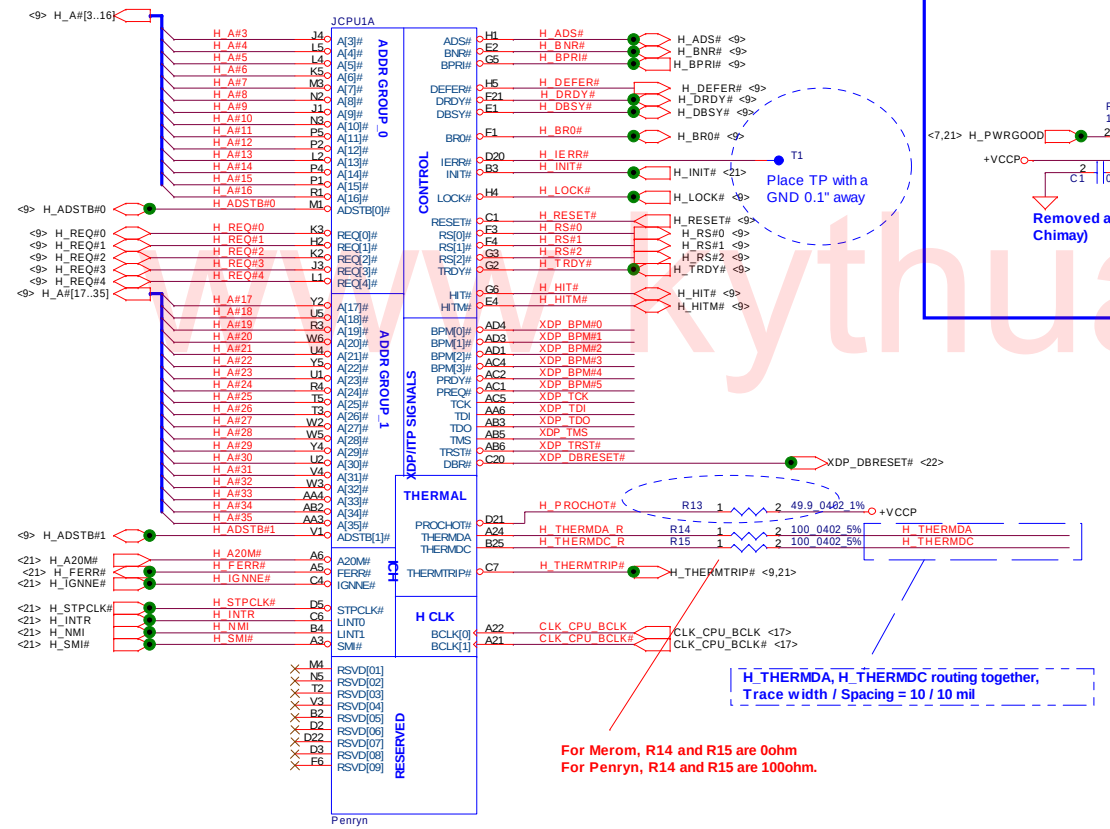
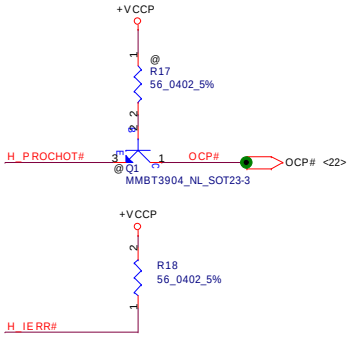
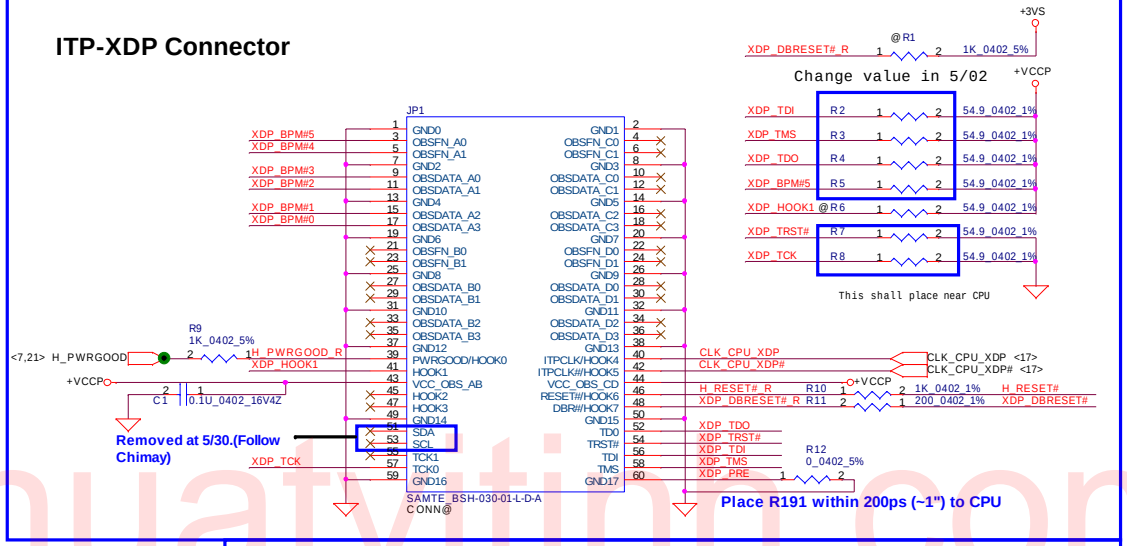
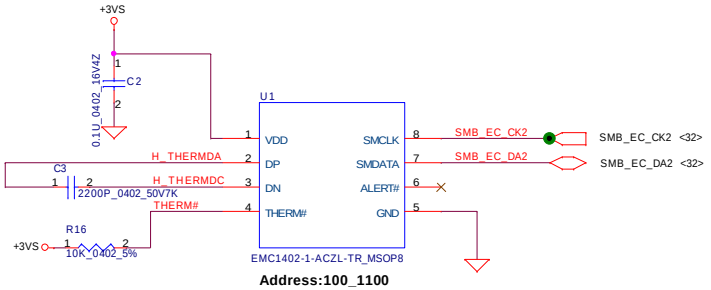


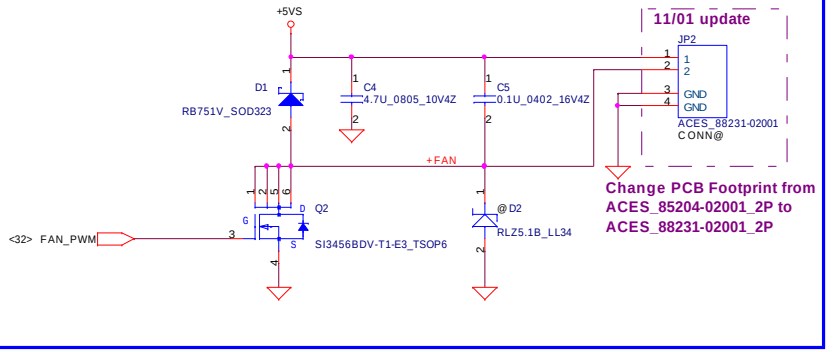


ITP-XDP Connector





PWM Fan Control circuit



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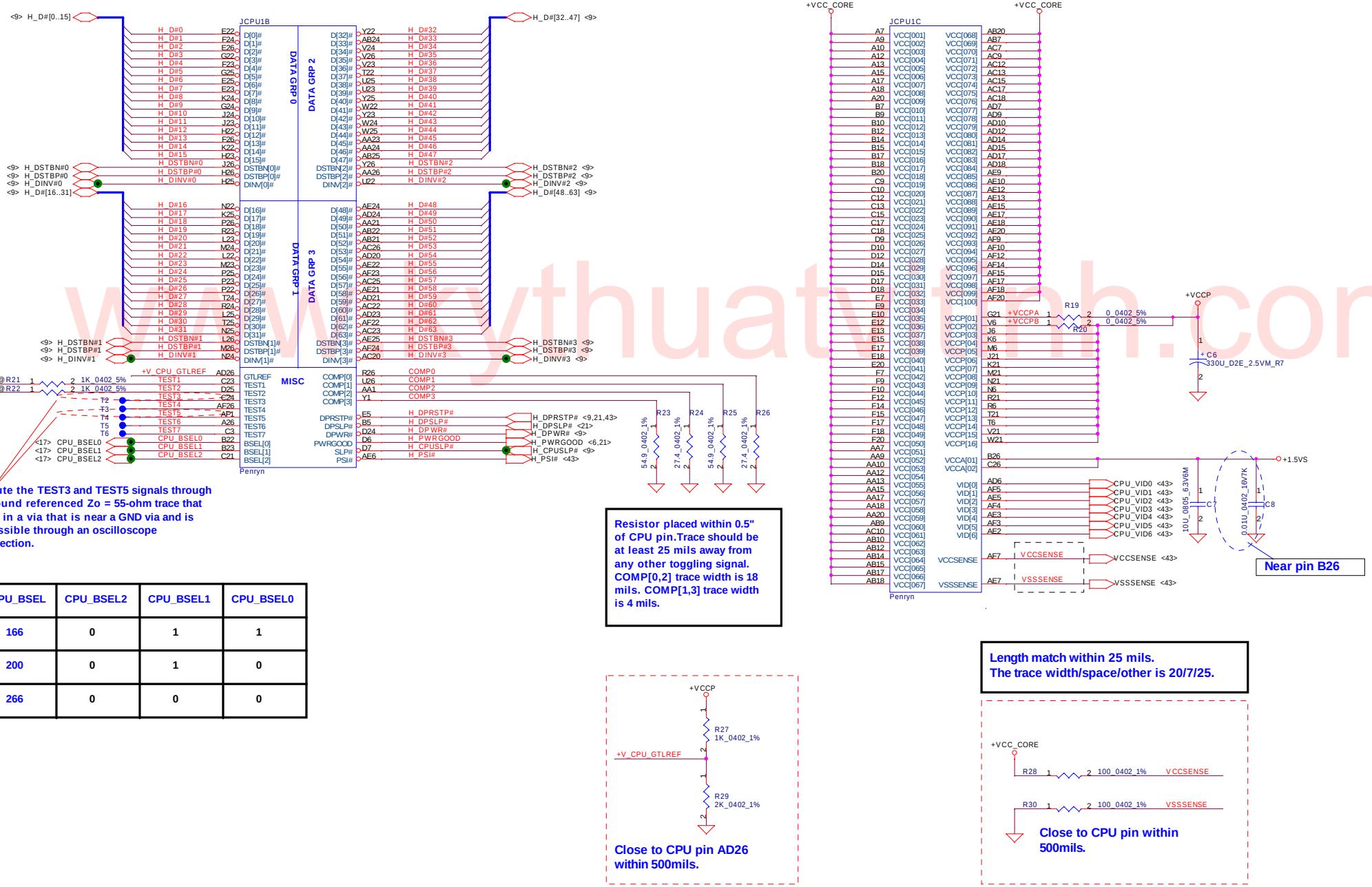

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

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Title: Penryn(2/3)-AGTL+/ITP-XDP

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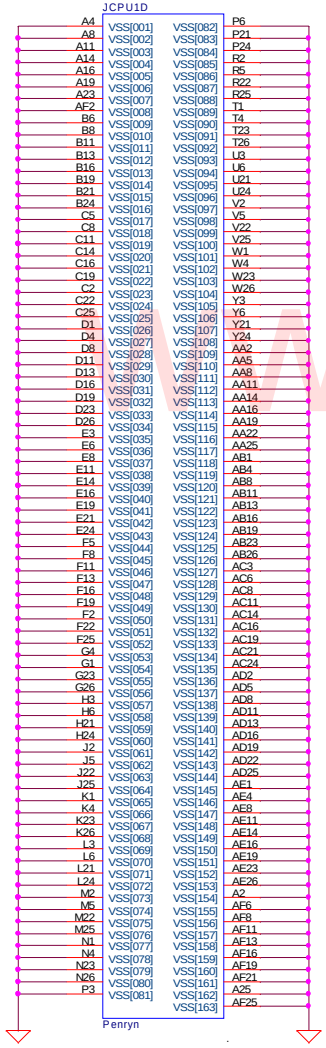
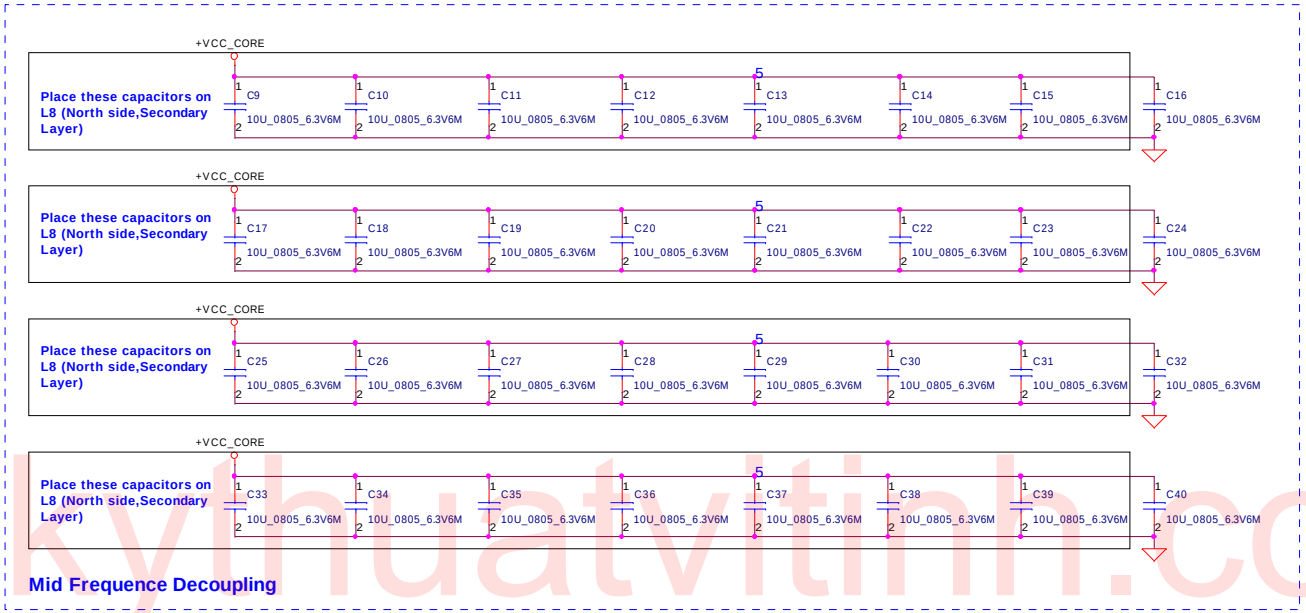
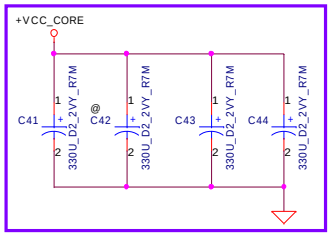


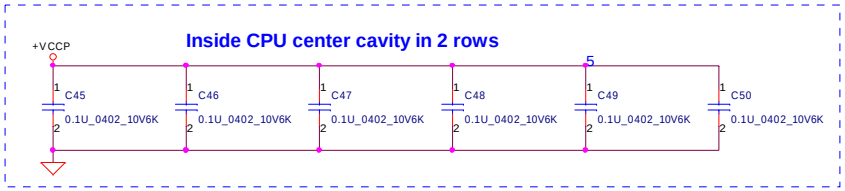


Near CPU CORE regulator

ESR <= 1.5m ohm
Capacitor > 1980uF



11/21 Change ESR=7m ohm



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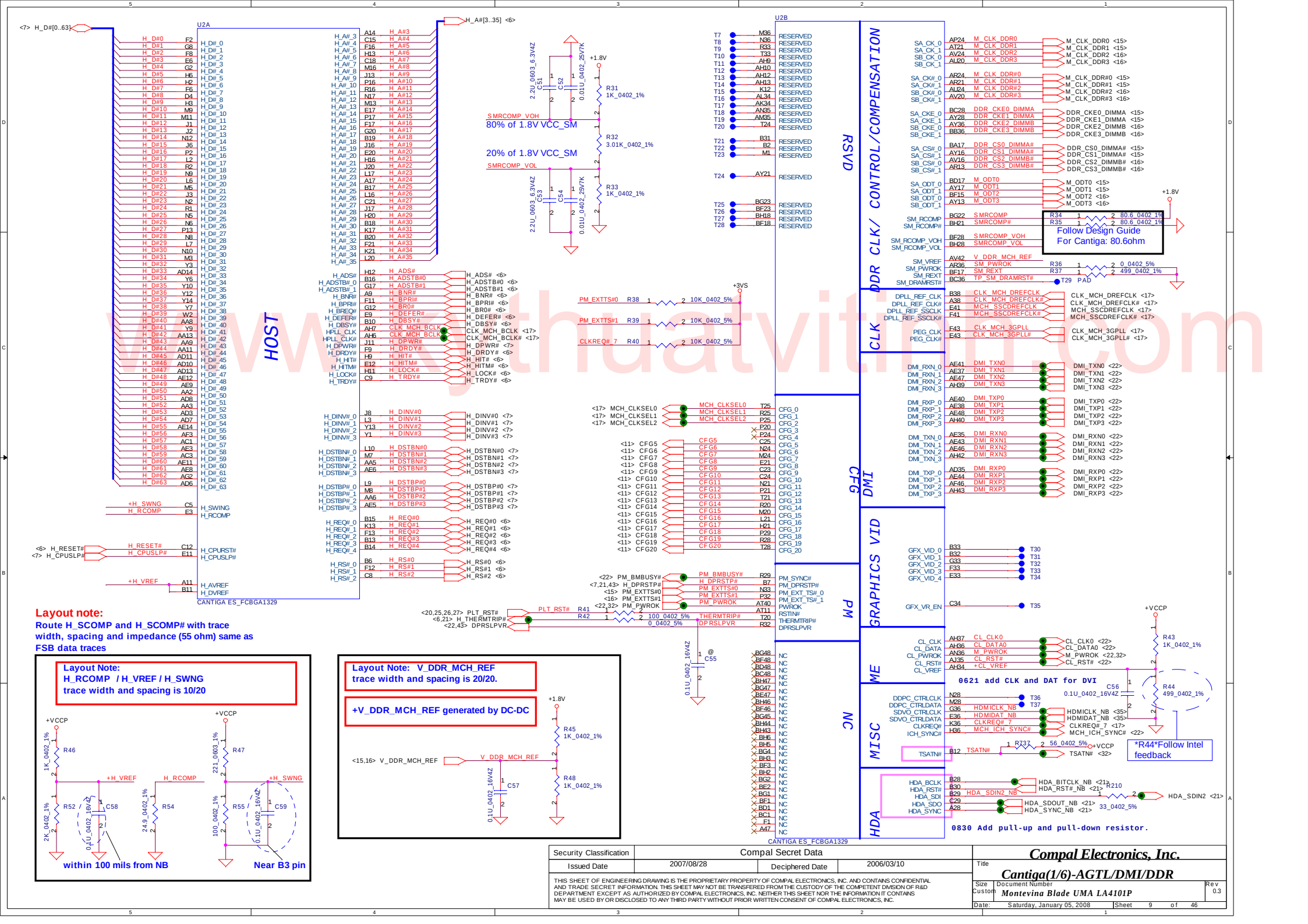
U2A
HOST
CANTIGA ES_FCBGA1329
U2B
RSVD
DDR CLK/ CONTROL/COMPENSATION
CLK
CFG
DMI
GRAPHICS VID
PM
ME
NC
MISC
HDA
CANTIGA ES_FCBGA1329
SMRCOMP_VOH
80% of 1.8V VCC_SM
SMRCOMP_VOL
20% of 1.8V VCC_SM
Follow Design Guide
For Cantiga: 80.6ohm
Layout note:
Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces
Layout Note:
H_RCOMP / H_VREF / H_SWNG
trace width and spacing is 10/20
within 100 mils from NB
Near B3 pin
Layout Note: V_DDR_MCH_REF
trace width and spacing is 20/20.
+V_DDR_MCH_REF generated by DC-DC
0621 add CLK and DAT for DVI
*R44*Follow Intel feedback
0830 Add pull-up and pull-down resistor.
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Title
Cantiga(1/6)-AGTL/DMI/DDR
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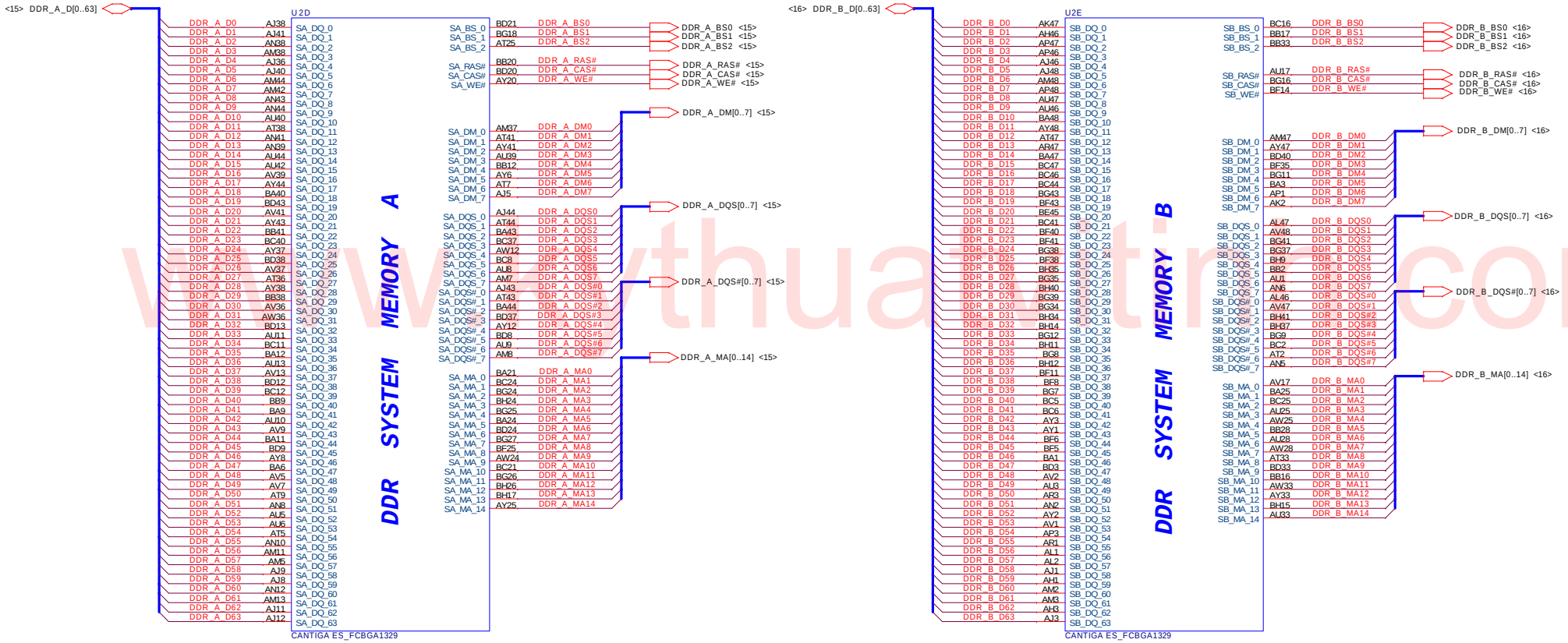
Rev
0.3
Date:
Saturday, January 05, 2008
Sheet
9
of
46



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Title: **Cantiga(2/6)-DDR2 A/B CH**

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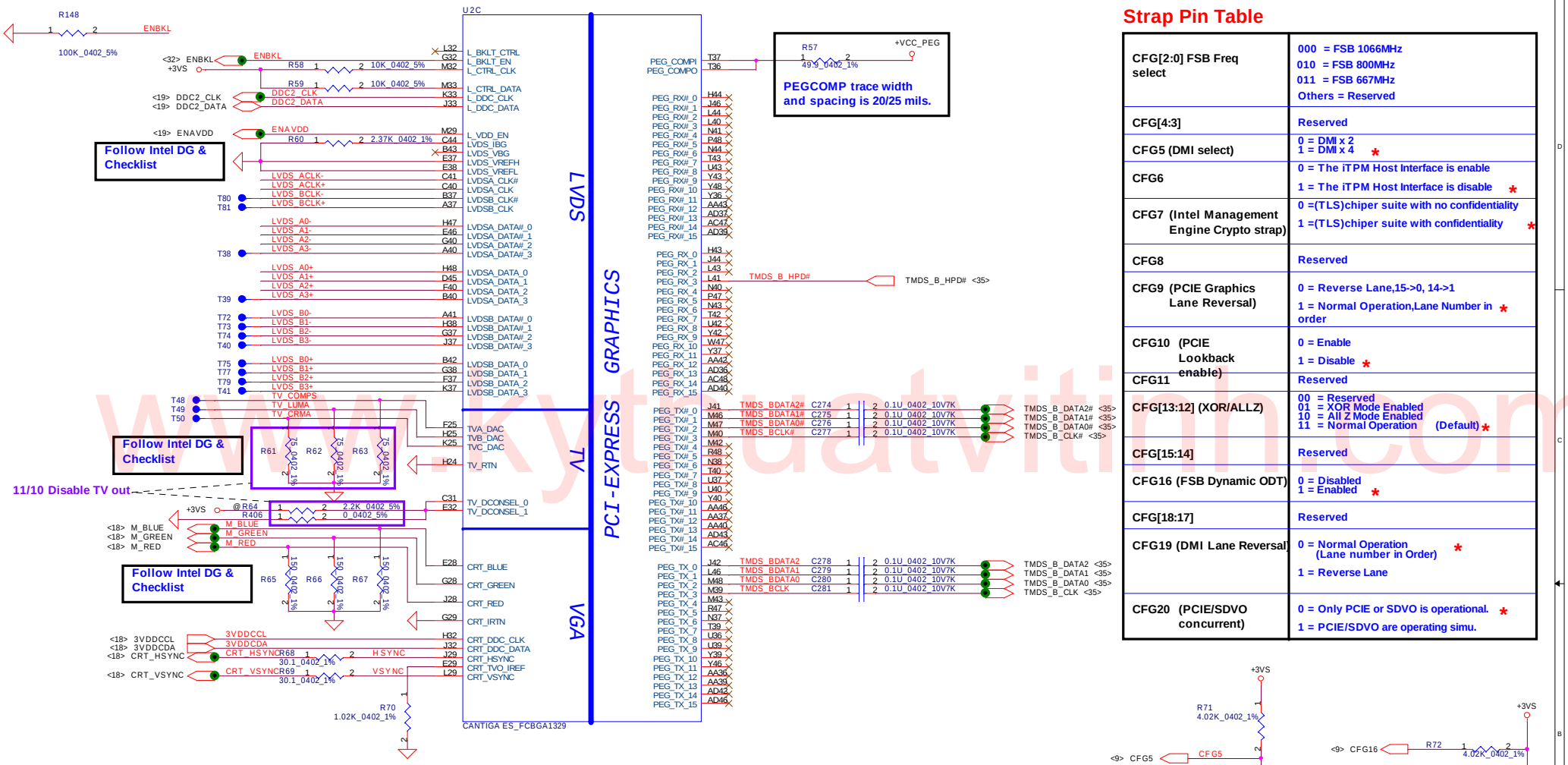

Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 =(TLS)chiper suite with no confidentiality 1 =(TLS)chiper suite with confidentiality *
CFG8	Reserved
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIE Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational. * 1 = PCIE/SDVO are operating simu.

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Title: **Cantiga(3/6)-VGA/LVDS/TV**

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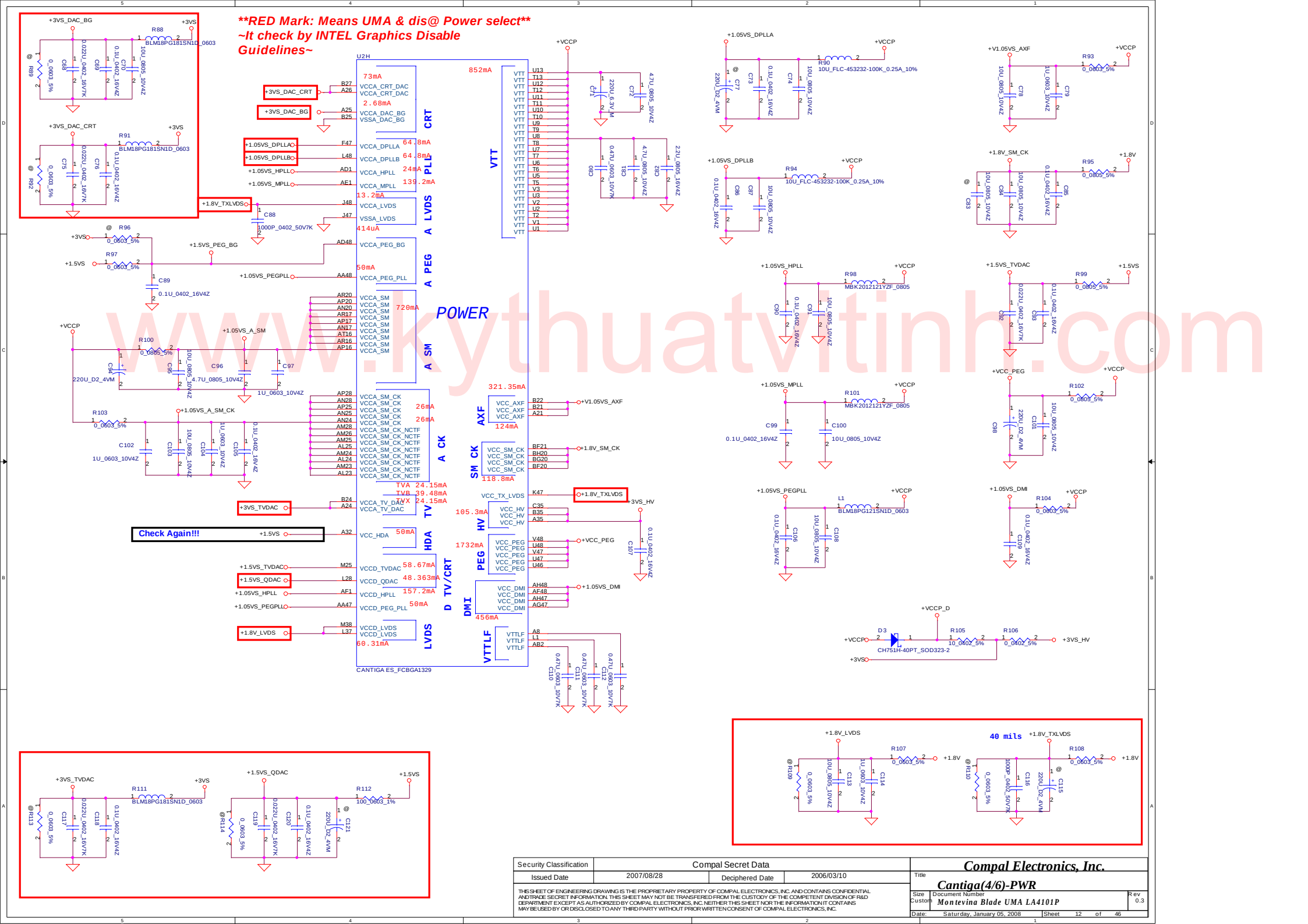

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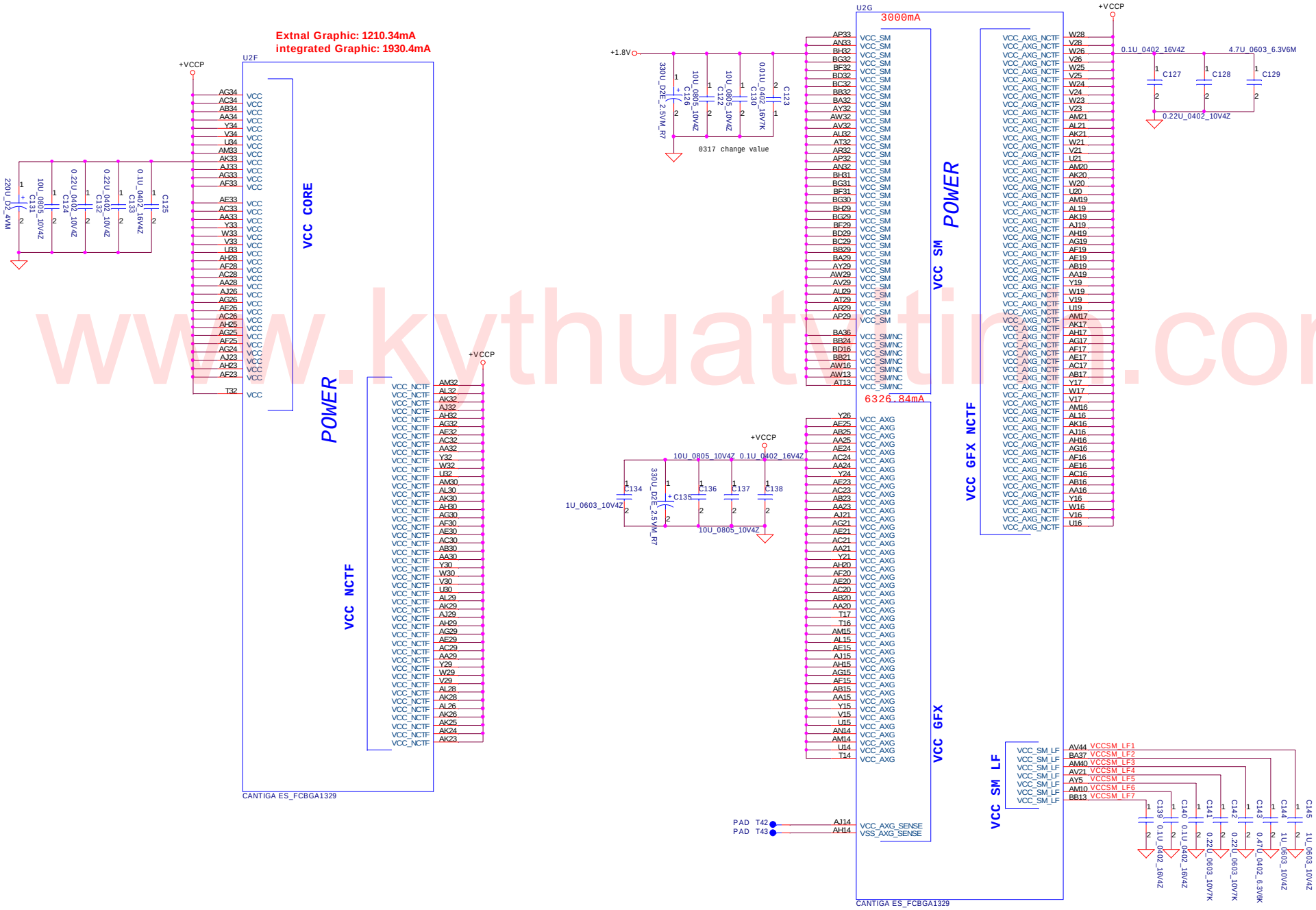

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Title: **Cantiga(5/6)-PWR/GND**

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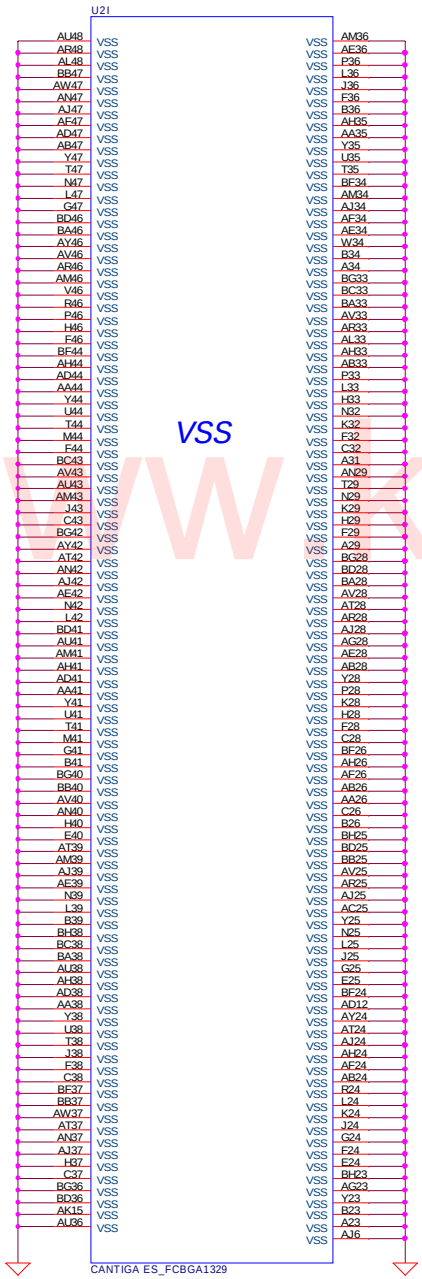

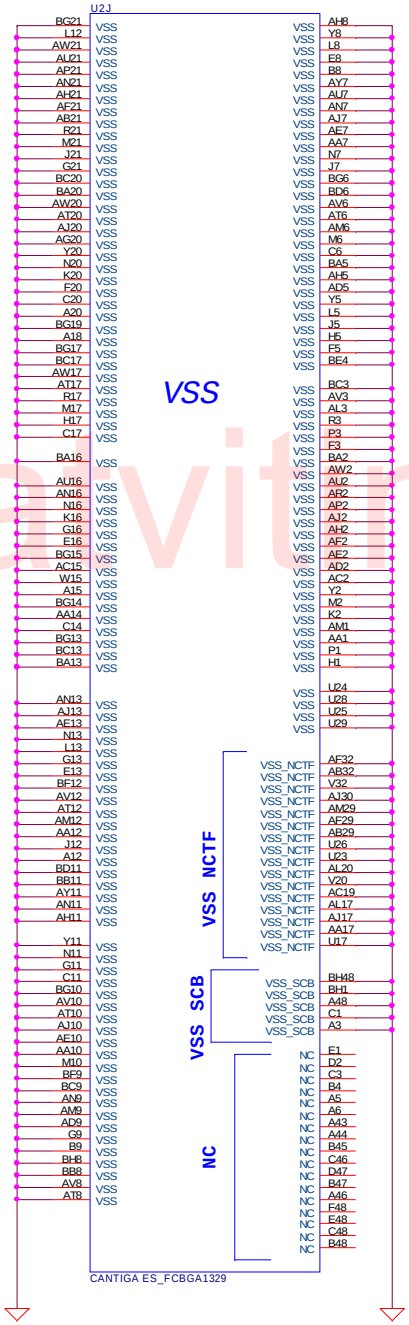

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Size	Document Number	Rev
Custom	Montevina Blade UMA LA4101P	0.3

Date: Saturday, January 05, 2008 | Sheet 14 of 46

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<10> DDR_A_DQS#[0..7]
<10> DDR_A_D[0..63]
<10> DDR_A_DM[0..7]
<10> DDR_A_DQS[0..7]
<10> DDR_A_MA[0..14]

Layout Note:
Place near JP3

+1.8V
2.2U_0805_16V4Z C152
2.2U_0805_16V4Z C147
2.2U_0805_16V4Z C153
2.2U_0805_16V4Z C154
2.2U_0805_16V4Z C155
0.1U_0402_16V4Z C156
0.1U_0402_16V4Z C148
0.1U_0402_16V4Z C149
0.1U_0402_16V4Z C157
330U_D2E_2.5VM_R7 C150

Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

+0.9V
0.1U_0402_16V4Z C158
0.1U_0402_16V4Z C159
0.1U_0402_16V4Z C160
0.1U_0402_16V4Z C161
0.1U_0402_16V4Z C162
0.1U_0402_16V4Z C163
0.1U_0402_16V4Z C164
0.1U_0402_16V4Z C165
0.1U_0402_16V4Z C166
0.1U_0402_16V4Z C167
0.1U_0402_16V4Z C168
0.1U_0402_16V4Z C169
0.1U_0402_16V4Z C170

Layout Note:
Place these resistor closely JP3,all trace length Max=1.5"

+0.9V
56_0404_4P2R_5% RP1: DDR_A_MA8, DDR_A_MA5
RP2: DDR_A_BS2, DDR_CKE0_DIMMA
RP3: DDR_A_MA1, DDR_A_MA3
RP4: DDR_A_MA7, DDR_A_MA6
RP5: DDR_A_RAS#, DDR_CS0_DIMMA#
RP6: DDR_A_MA12, DDR_A_MA9
RP7: DDR_A_BS0, DDR_A_MA10
RP8: DDR_A_MA4, DDR_A_MA2
RP9: DDR_A_CAS#, DDR_A_WE#
RP10: DDR_A_MA0, DDR_A_BS1
RP11: DDR_CS1_DIMMA#, M_ODT1
RP12: M_ODT0, DDR_A_MA13
RP13: DDR_A_MA11, DDR_CKE1_DIMMA, DDR_A_MA14
R117 56_0402_5%

+1.8V
V_DDR_MCH_REF
V_DDR_MCH_REF <9,16>
2.2U_0805_16V4Z C146
0.1U_0402_16V4Z C151

JDIMM1

		DDR_A_D5	DDR_A_D4
		DDR_A_D0	DDR_A_D1
		DDR_A_DM0	
		DDR_A_D6	DDR_A_DQS#0
		DDR_A_D7	DDR_A_DQS0
		DDR_A_D13	DDR_A_D2
		DDR_A_D12	DDR_A_D3
		DDR_A_DM1	
		M_CLK_DDR0 <9>	DDR_A_D8
		M_CLK_DDR#0 <9>	DDR_A_D9
		DDR_A_D15	DDR_A_DQS#1
		DDR_A_D14	DDR_A_DQS1
			DDR_A_D11
			DDR_A_D10
		DDR_A_D20	DDR_A_D16
		DDR_A_D21	DDR_A_D17
		PM_EXTTS#0 <9>	DDR_A_DQS#2
		DDR_A_DM2	DDR_A_DQS2
		DDR_A_D23	DDR_A_D18
		DDR_A_D22	DDR_A_D19
		DDR_A_D28	DDR_A_D29
		DDR_A_D25	DDR_A_D24
		DDR_A_DQS#3	DDR_A_DM3
		DDR_A_DQS3	
		DDR_A_D31	DDR_A_D26
		DDR_A_D30	DDR_A_D27
		DDR_CKE1_DIMMA	DDR_CKE0_DIMMA <9>
			DDR_A_BS2 <10>
		DDR_A_MA14	
		DDR_A_MA11	DDR_A_MA12
		DDR_A_MA7	DDR_A_MA9
		DDR_A_MA6	DDR_A_MA8
		DDR_A_MA4	DDR_A_MA5
		DDR_A_MA2	DDR_A_MA3
		DDR_A_MA0	DDR_A_MA1
		DDR_A_BS1	DDR_A_MA10
		DDR_A_RAS#	DDR_A_BS0 <10>
		DDR_CS0_DIMMA#	DDR_A_WE# <10>
		M_ODT0	DDR_A_CAS#
		DDR_A_MA13	DDR_CS1_DIMMA# <9>
			M_ODT1 <9>
		DDR_A_D32	DDR_A_D37
		DDR_A_D33	DDR_A_D36
		DDR_A_DM4	DDR_A_DQS#4
		DDR_A_D34	DDR_A_DQS4
		DDR_A_D35	DDR_A_D39
		DDR_A_D40	DDR_A_D38
		DDR_A_D41	DDR_A_D45
		DDR_A_DQS#5	DDR_A_D44
		DDR_A_DQS5	DDR_A_DM5
		DDR_A_D43	DDR_A_D47
		DDR_A_D42	DDR_A_D46
		DDR_A_D52	DDR_A_D49
		DDR_A_D53	DDR_A_D48
		M_CLK_DDR1 <9>	
		M_CLK_DDR#1 <9>	
		DDR_A_DM6	DDR_A_DQS#6
		DDR_A_D51	DDR_A_DQS6
		DDR_A_D55	DDR_A_D54
		DDR_A_D57	DDR_A_D50
		DDR_A_D56	DDR_A_D61
		DDR_A_DQS#7	DDR_A_D60
		DDR_A_DQS7	DDR_A_DM7
		DDR_A_D62	DDR_A_D59
		DDR_A_D63	DDR_A_D58
			CLK_SMBDATA <16,17>
			CLK_SMBCLK <16,17>
			+3VS

FOX_ASOA426-M4R-TR
CONN@

2.2U_0603_6.3V4Z C171
0.1U_0402_16V4Z C172
R115 10K_0402_5%
R116 10K_0402_5%

SO-DIMM A

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Issued Date	2006/02/13	Deciphered Date	2006/03/10

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Compal Electronics, Inc.
Title: DDRII-SODIMM SLOT1
Size: Custom | Document Number: Montevina Blade UMA LA4101P | Rev: 0.3
Date: Saturday, January 05, 2008 | Sheet 15 of 46

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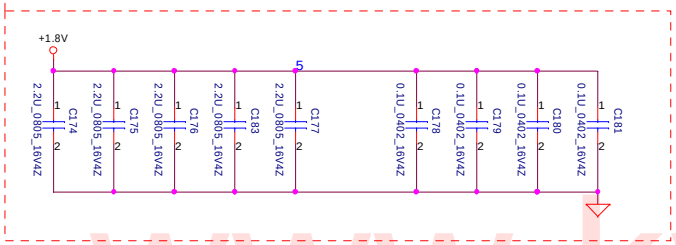
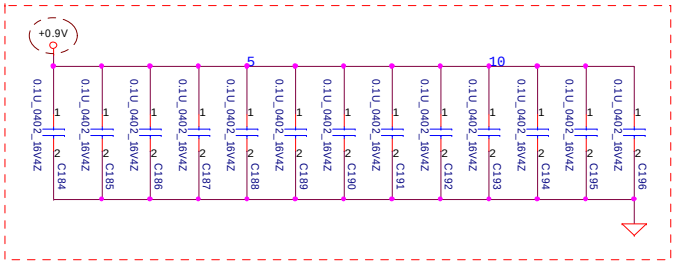
<10> DDR_B_DQS#[0..7]
<10> DDR_B_D[0..63]
<10> DDR_B_DM[0..7]
<10> DDR_B_DQS[0..7]
<10> DDR_B_MA[0..14]

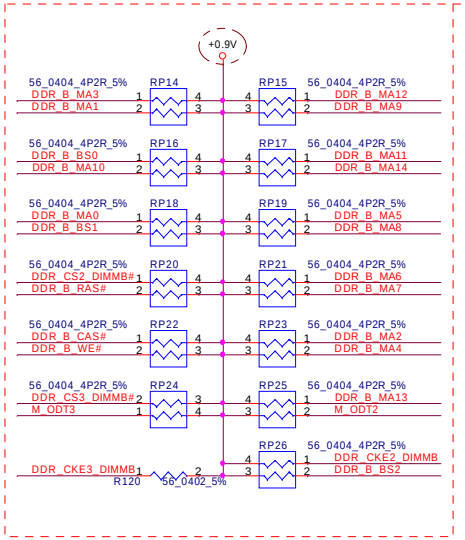
Layout Note:
Place near JP10

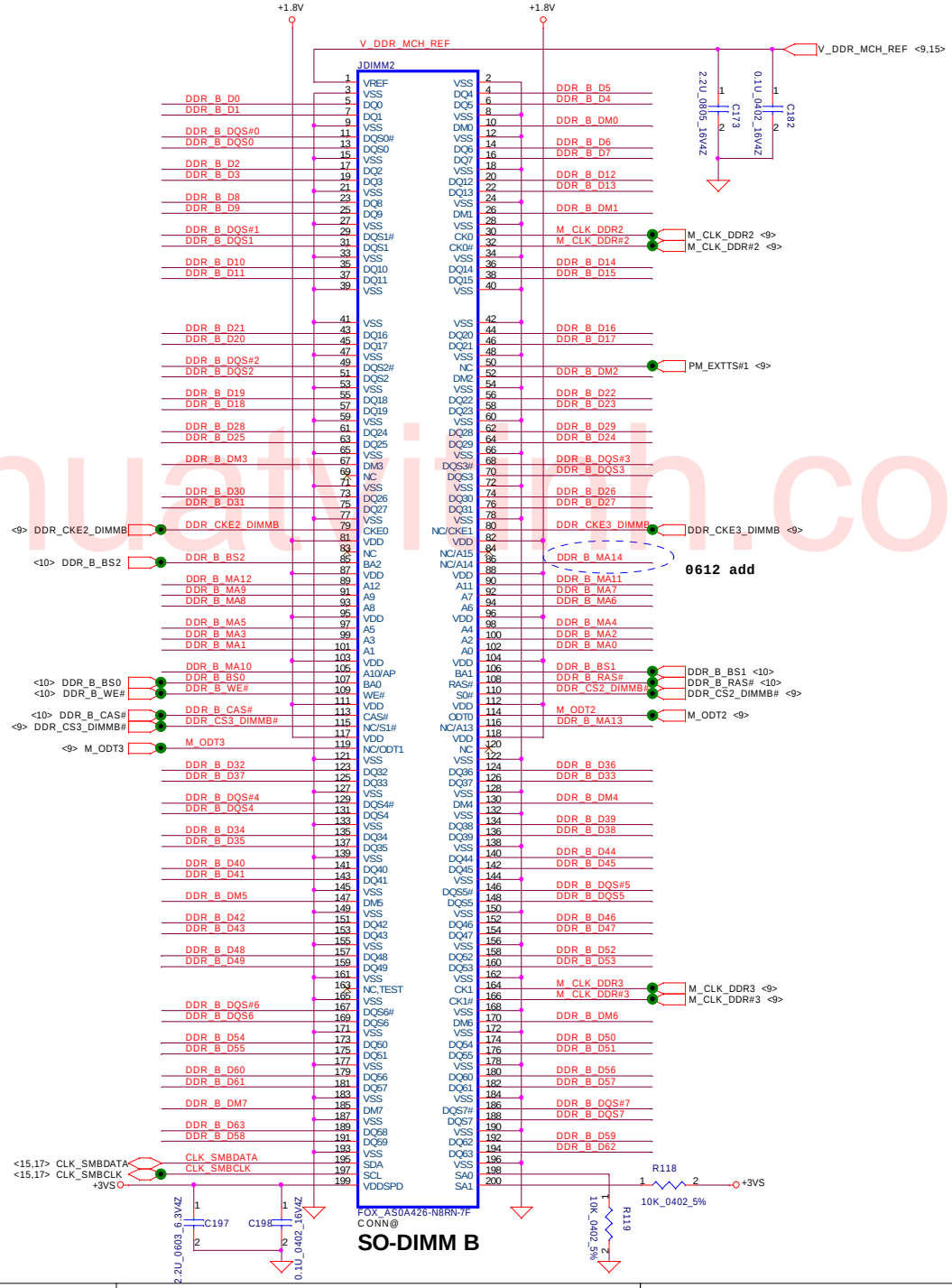


Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS



Layout Note:
Place these resistor closely JP3,all trace length Max=1.5"





Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

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Compal Electronics, Inc.

Title: **DDRII-SODIMM SLOT2**

Size	Document Number	Rev
	Montevina Blade UMA LA4101P	0.3

Date: Saturday, January 05, 2008 | Sheet 16 of 46

FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					

Routing the trace at least 10mil

Place close to U51

Vendor suggests 22pF

Change 33M and 48M damping to 39M by EMI request

No Debug port anymore

SLG8SP553VTR_QFN72_10x10

ITP_EN	0 = SRC8/SRC8# 1 = ITP/ITP#
PCI_CLK3	0 = Enable DOT96 & SRC1(UMA) 1 = Enable SRC0 & 27MHz(DIS)

<BOM Structure>

Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/03/10

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Compal Electronics, Inc.

Title: Clock Generator CK505

Size: | Document Number: Montevina Blade UMA LA4101P | Rev: 0.3

Date: Saturday, January 05, 2008 | Sheet 17 of 46

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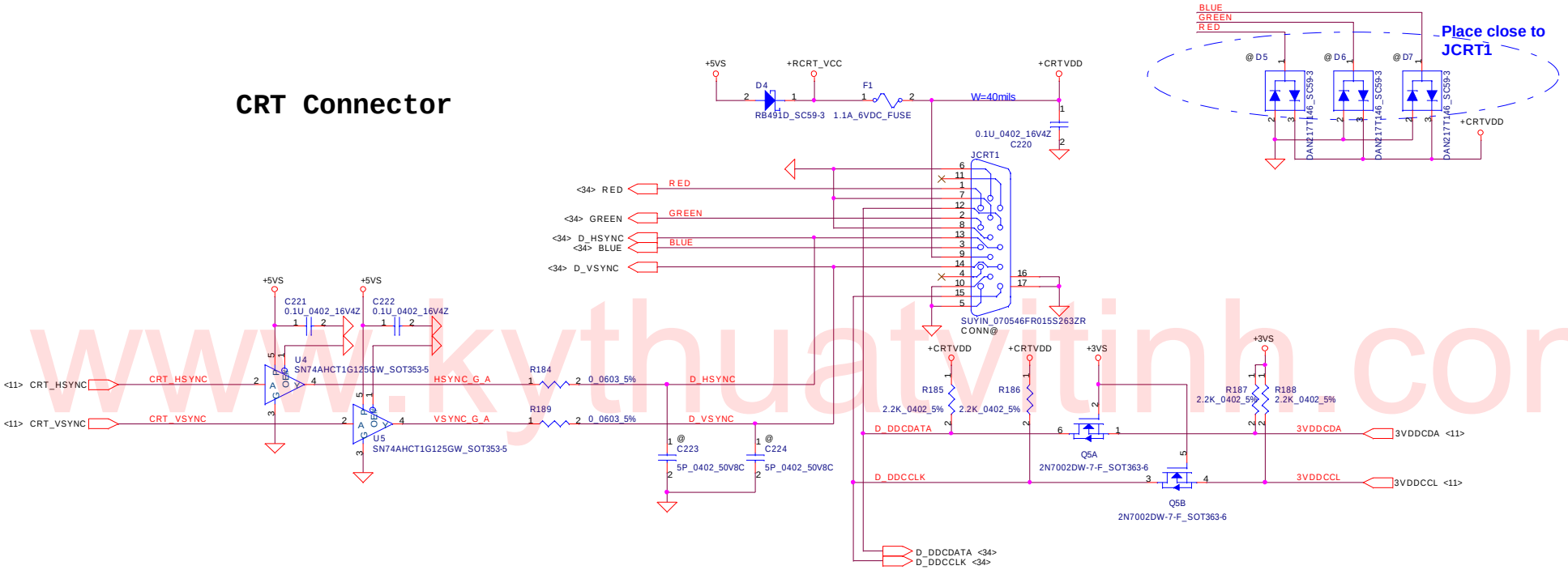
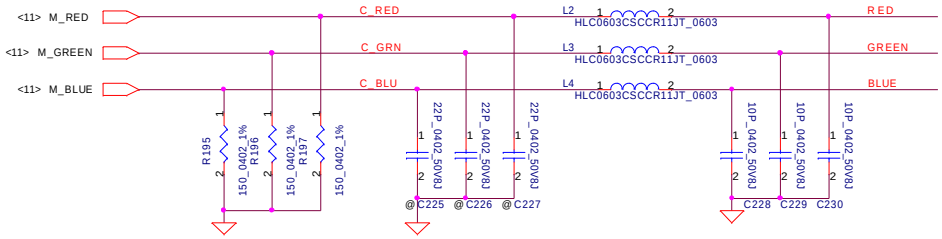
CRT Connector



CRT Termination/EMI Filter

11/07 Change CRT lounting NB-->Docking-->CRT connector



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Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

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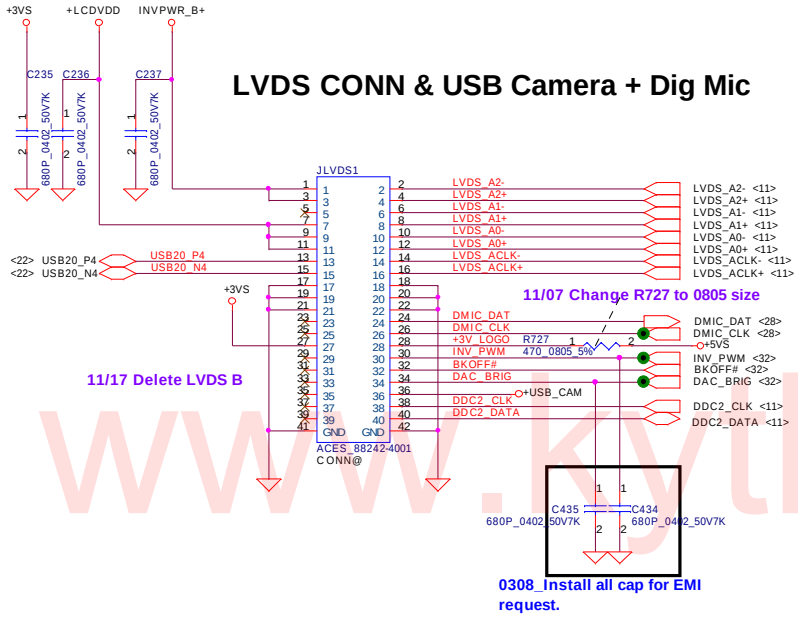
Compal Electronics, Inc.			
Title	CRT Connector		
Size	Document Number	Montevina Blade UMA LA4101P	Rev 0.3
Date: Saturday, January 05, 2008	Sheet 18 of 46		

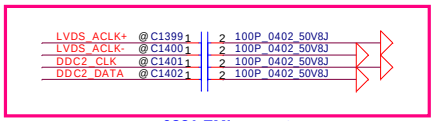
LVDS CONN & USB Camera + Dig Mic



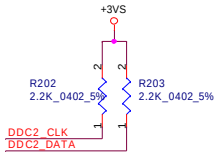
11/07 Change R727 to 0805 size

11/17 Delete LVDS B

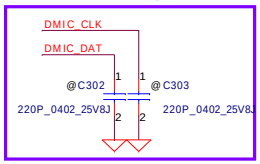
0308_Install all cap for EMI request.



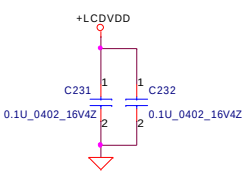
0831 EMI request

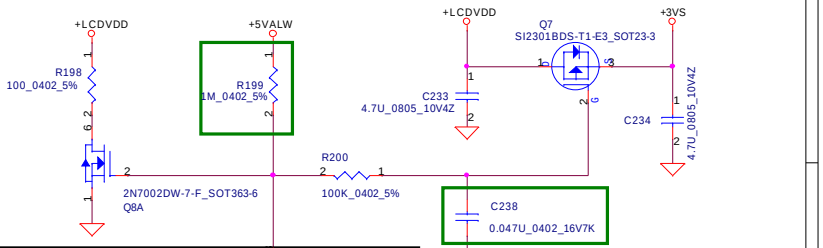


Must close JLVDS1pin 24、26



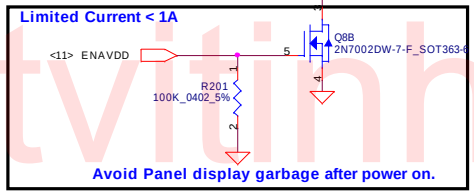
11/09 EMI reserver



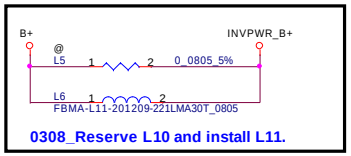


01/03 Change to 0.047u to meet T1 timing

Limited Current < 1A

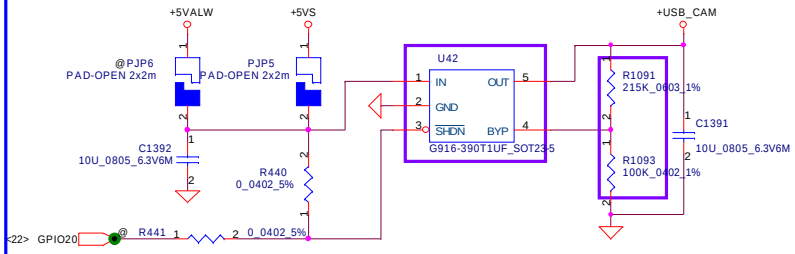


Avoid Panel display garbage after power on.



0308_Reserve L10 and install L11.

USB Camera



11/07 Change U42 to 3.9V LDO(Adjustable)

11/07 Change R1091 to 215K、R1093 to 100K

11/08 Change C1391、C1392 to 0805 size

+USB_CAM is +3.9VS, R1091:215K; R1093:100Kohm +USB_CAM=1.25(1+R1091/R1093)

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Issued Date	2007/08/28	Deciphered Date	2006/07/26

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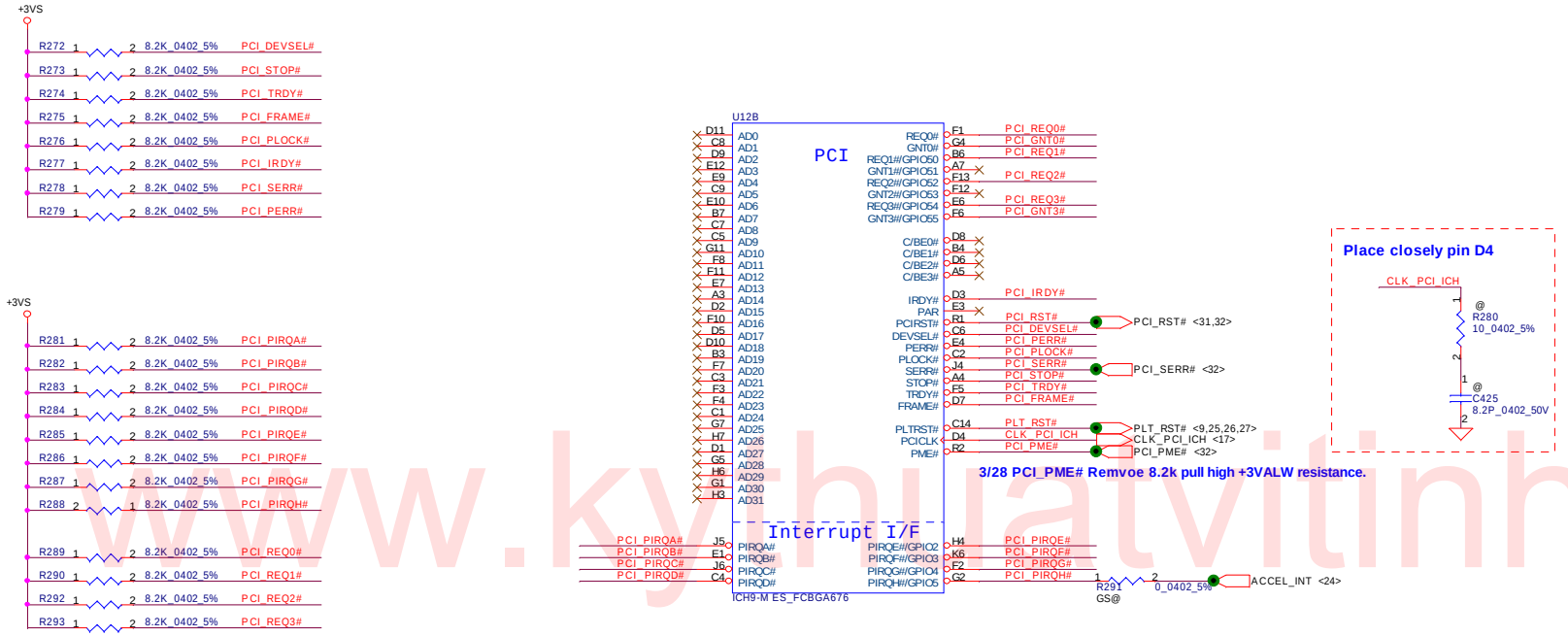
Compal Electronics, Inc.			
Title	LCD CONN.		
Size	Document Number	Montevina Blade UMA LA4101P	Rev 0.3
Date: Saturday, January 05, 2008	Sheet 19 of 46		



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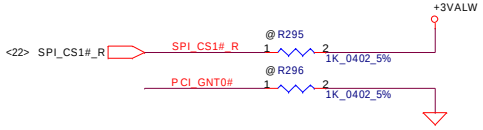
A16 swap override Strap

PCI_GNT3#	Low= A16 swap override Enble High= Default *

Boot BIOS Strap

PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *



Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/03/10

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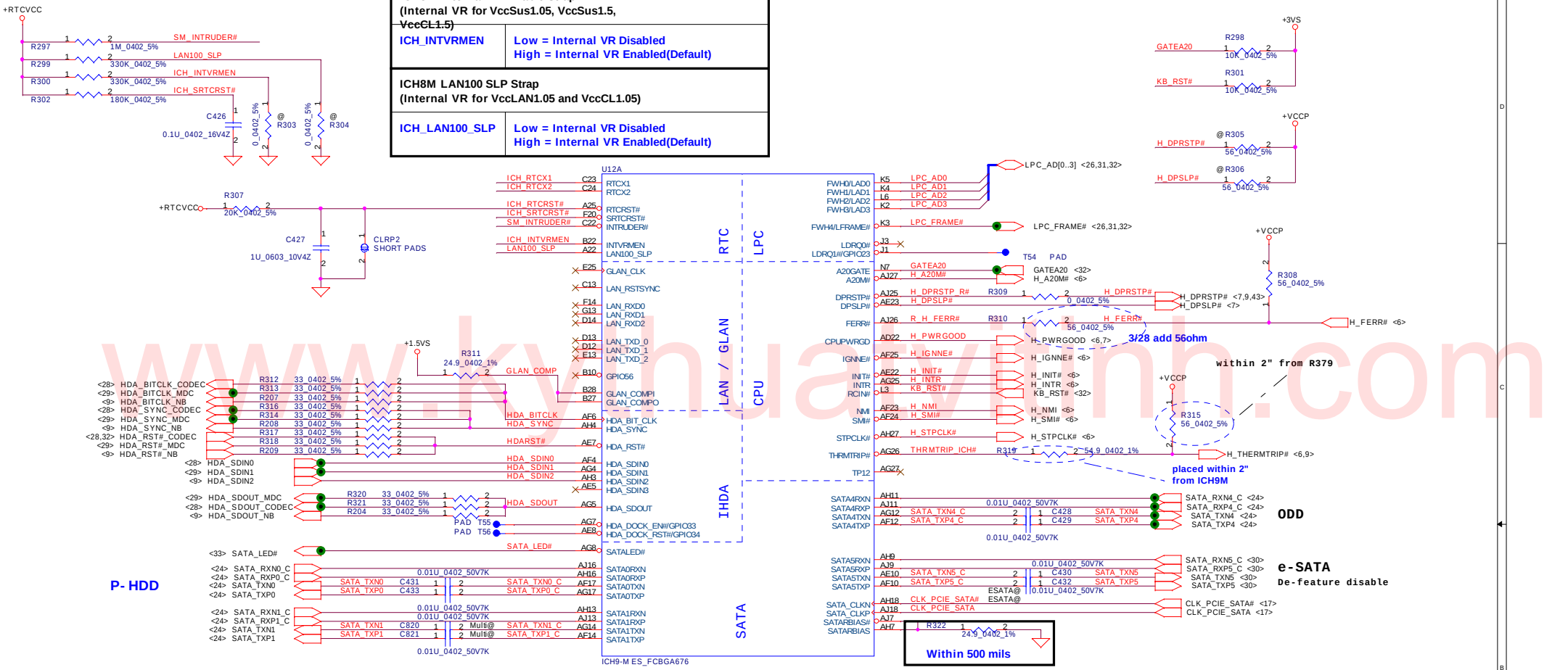
Compal Electronics, Inc.	
Title	ICH9(1/4)-PCI/INT
Size	Document Number: Montevina Blade UMA LA4101P
Rev	0.3
Date: Saturday, January 05, 2008	Sheet 20 of 46

ICH8M Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)	
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)

ICH8M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)	
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)



ICH_RSVD	HDA_SDOUT_CODEC	
0	0	
0	1	
1	0	
1	1	

Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/03/10

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Compal Electronics, Inc.

Title: ICH9(2/4)_LAN,HD,IDE,LPC

Size: Custom | Document Number: Montevina Blade UMA LA4101P | Rev: 0.3

Date: Saturday, January 05, 2008 | Sheet 21 of 46

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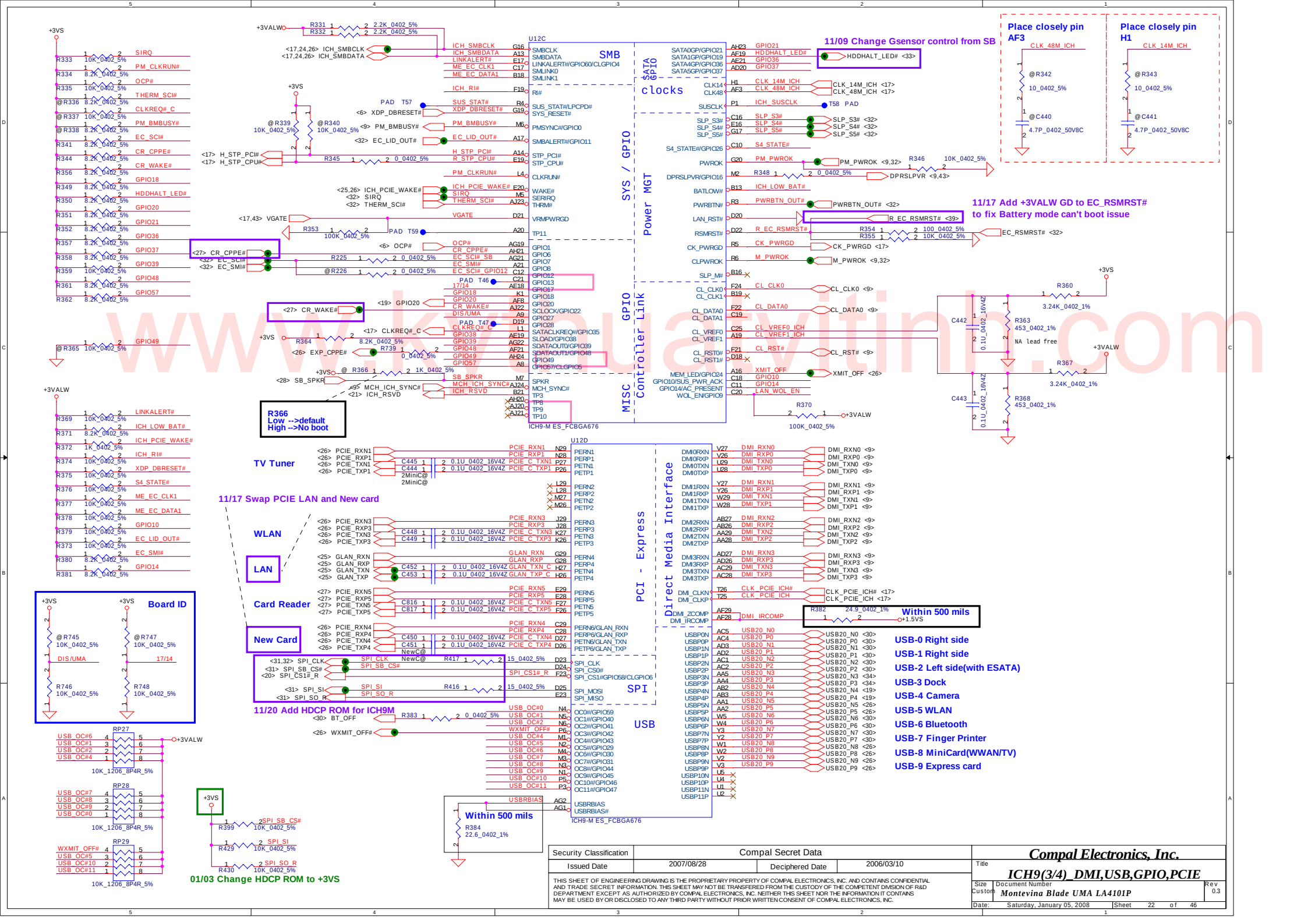

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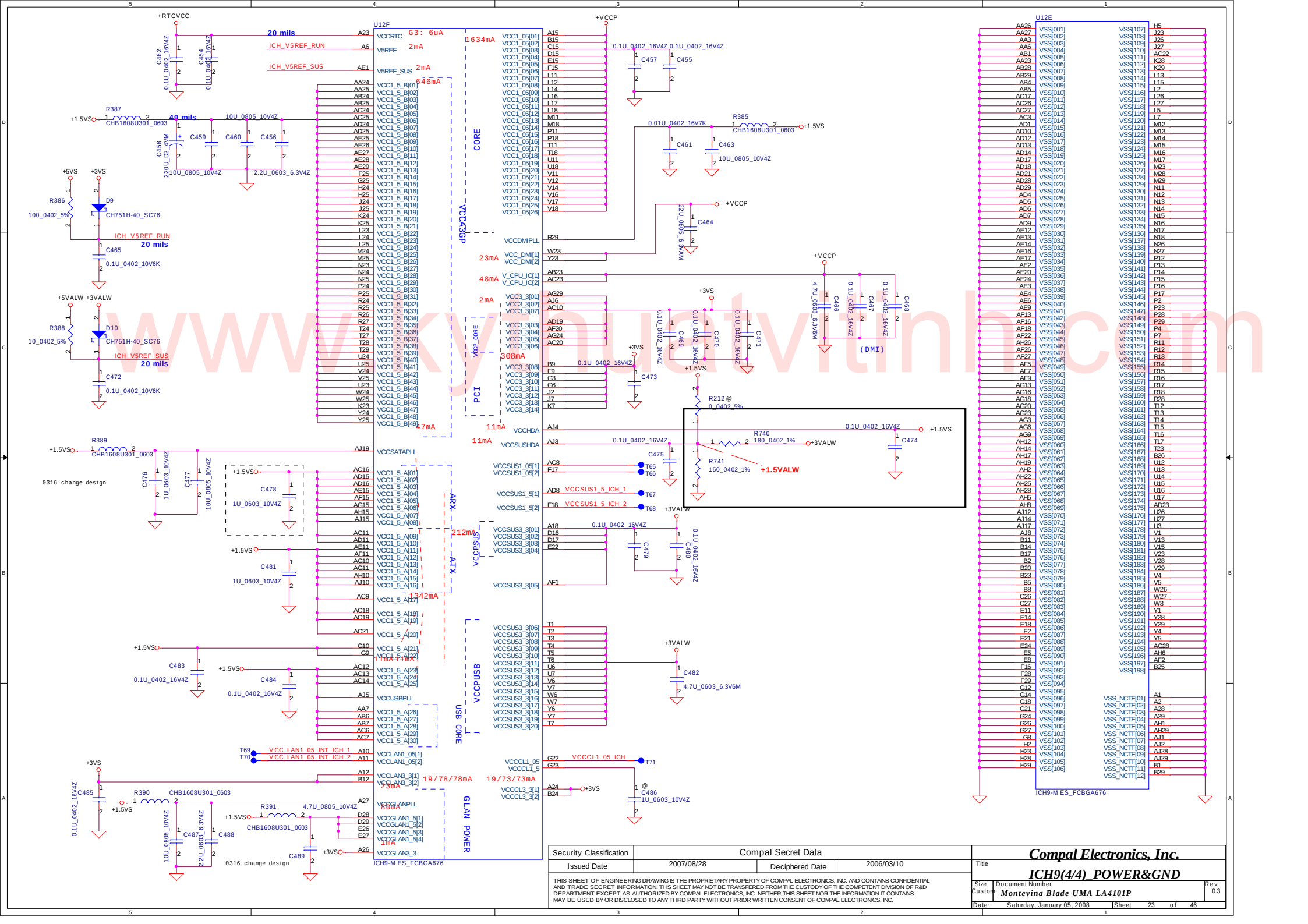

Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/03/10

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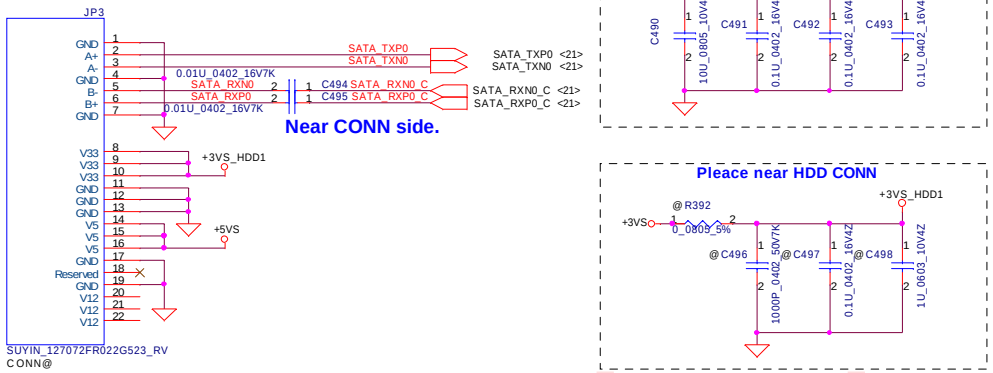
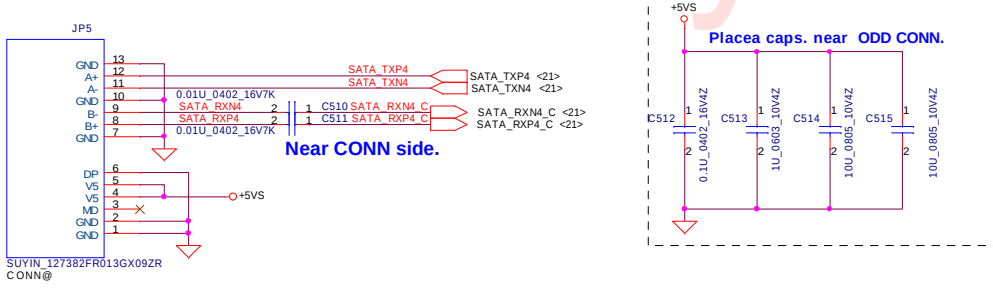
Compal Electronics, Inc.			
Title: ICH9(4/4)_POWER&GND			
Size: Custom	Document Number: Montevina Blade UMA LA4101P		Rev: 0.3
Date: Saturday, January 05, 2008	Sheet 23 of 46		

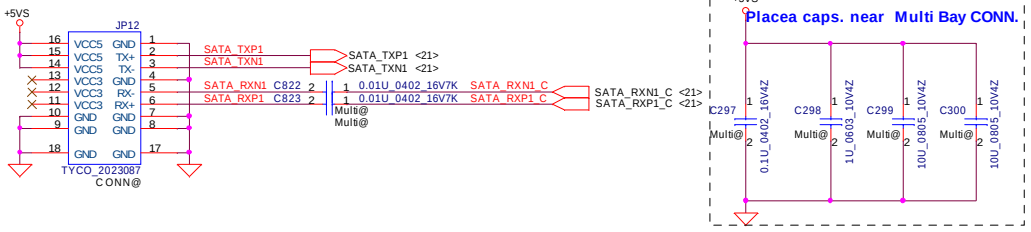
HDD Connector



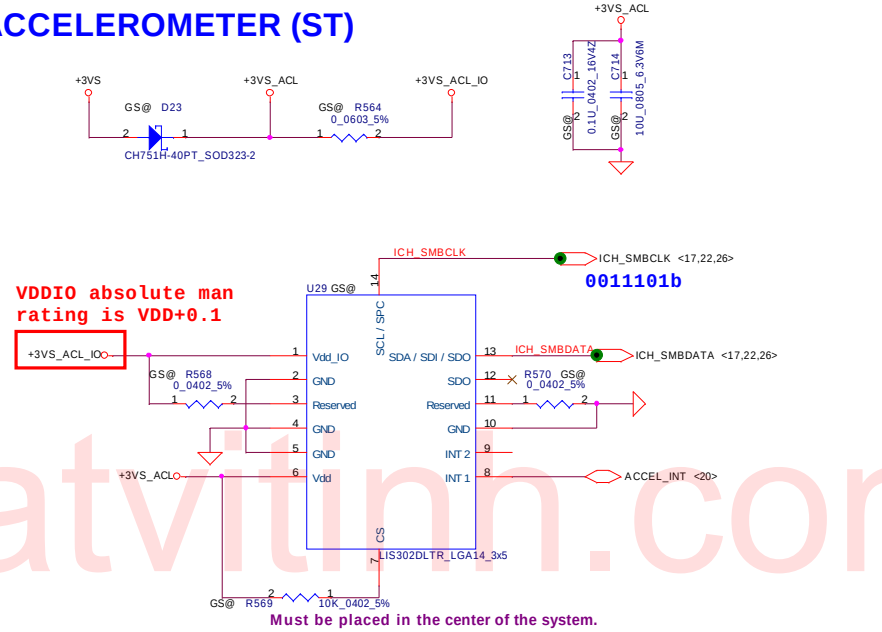
CD-ROM Connector



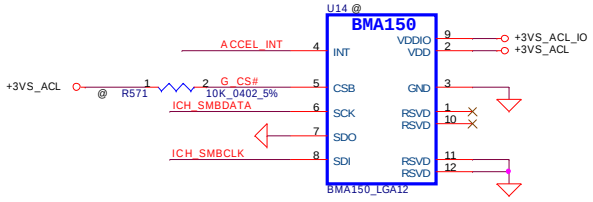
Multi Bay



ACCELEROMETER (ST)



ACCELEROMETER (Bosch)



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PCB-MB

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Issued Date	2007/08/28	Deciphered Date	2006/03/10

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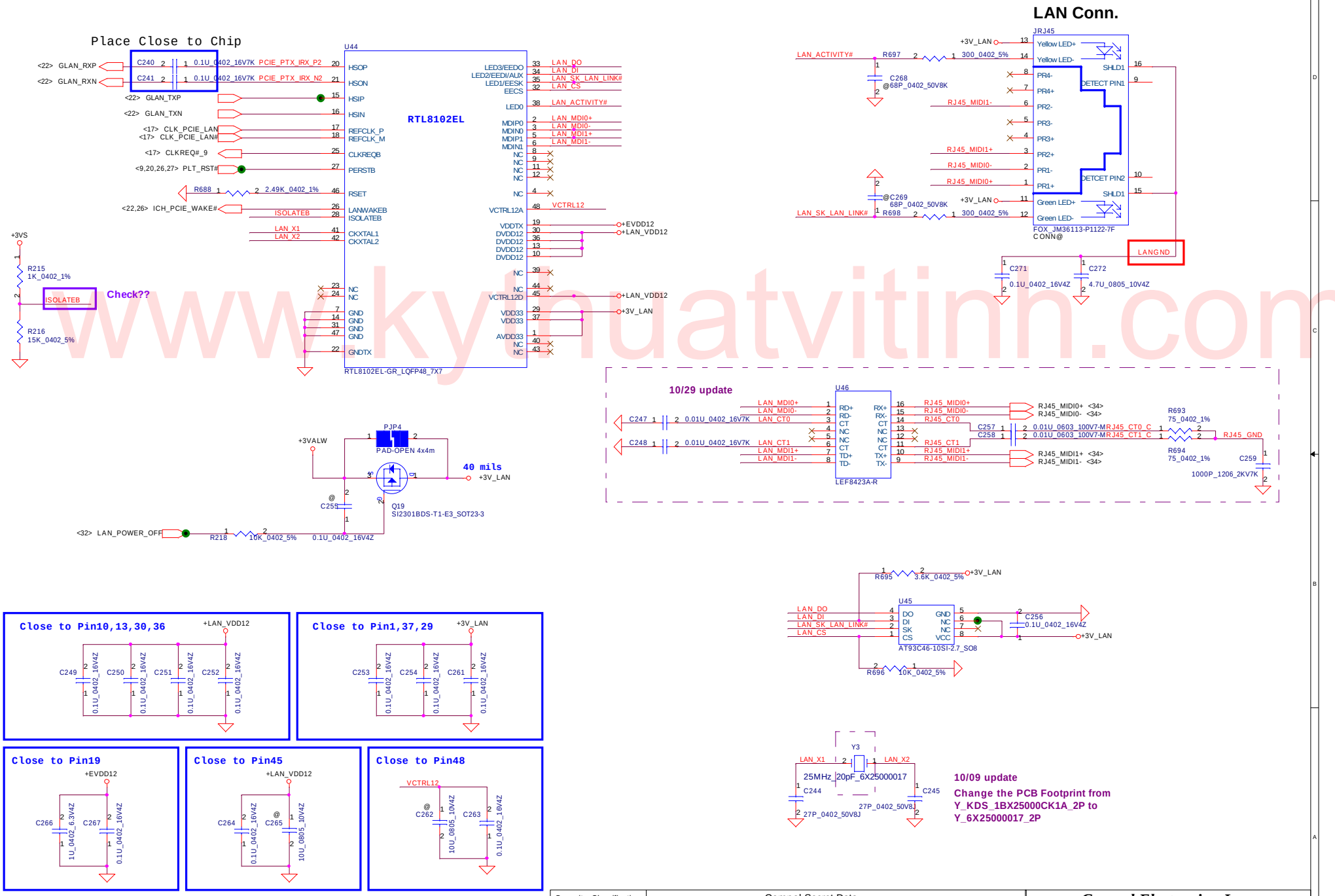
Compal Electronics, Inc.

Title: **HDD & CDROM**

Size: Custom | Document Number: **Montevina Blade UMA LA4101P** | Rev: 0.3

Date: Saturday, January 05, 2008 | Sheet 24 of 46



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Issued Date	2007/08/28	Deciphered Date	2007/06/30

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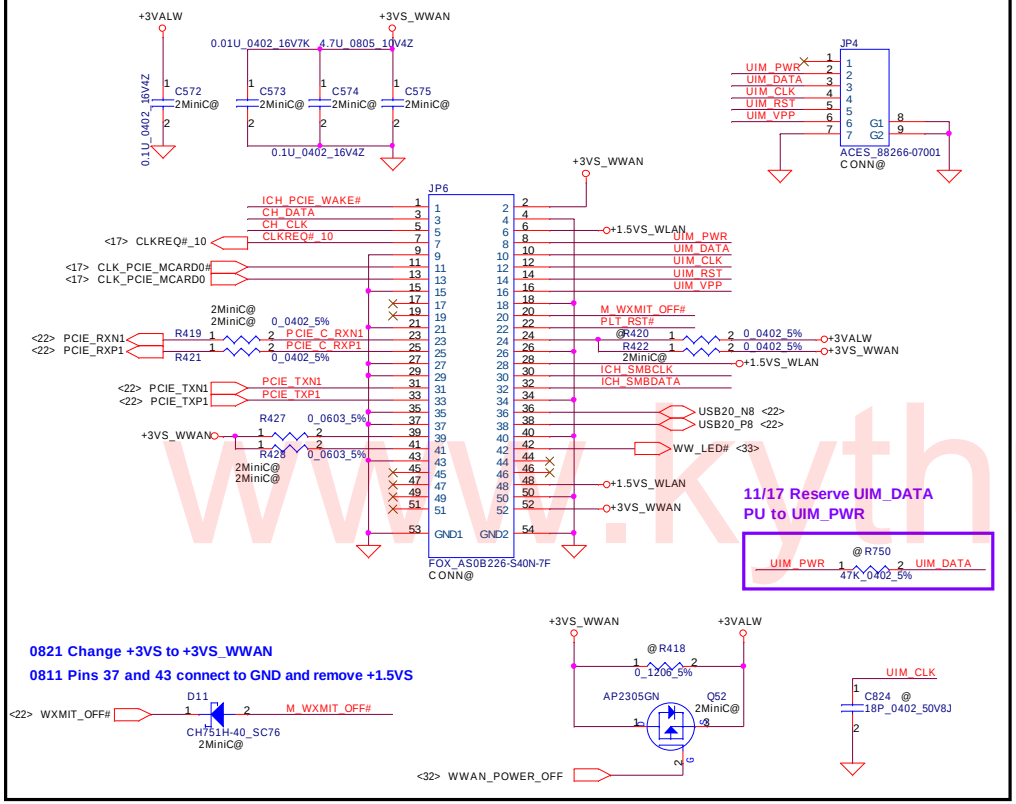
Compal Electronics, Inc.

Title: RTL8102EL LAN

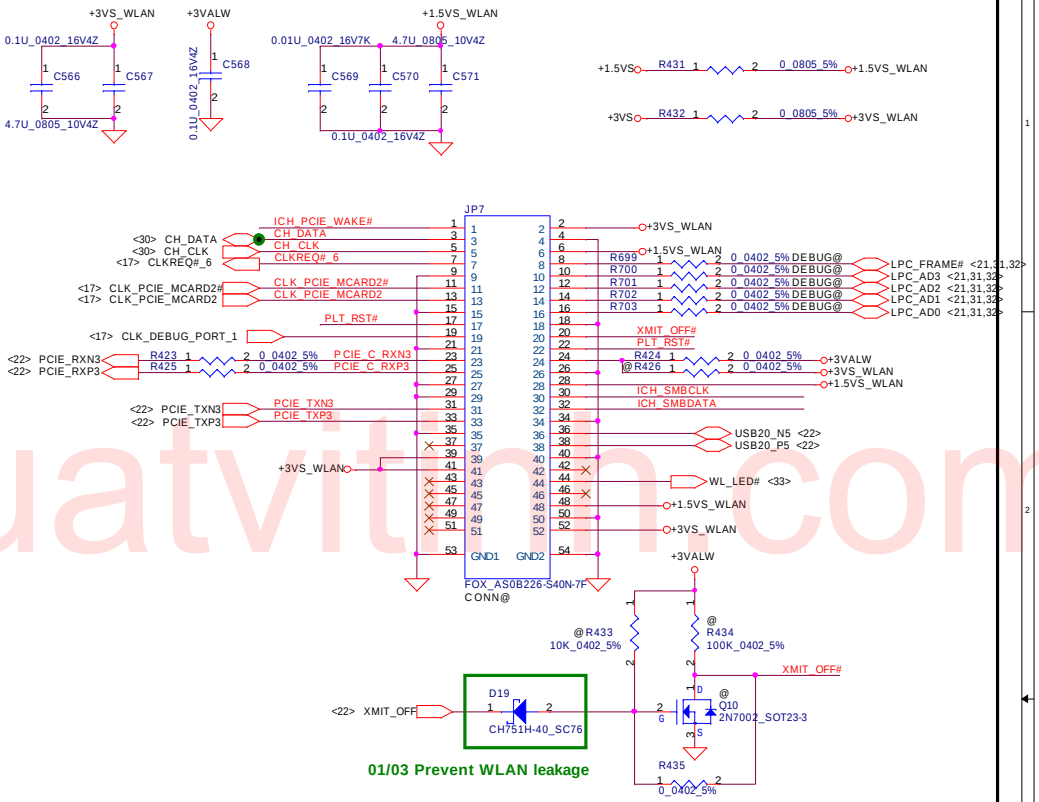
Size: Custom | Document Number: Montevina Blade UMA LA4101P | Rev: 0.3

Date: Saturday, January 05, 2008 | Sheet 25 of 46

Mini Card 0--TV tuner/WWAN/Robson SIM card Connector

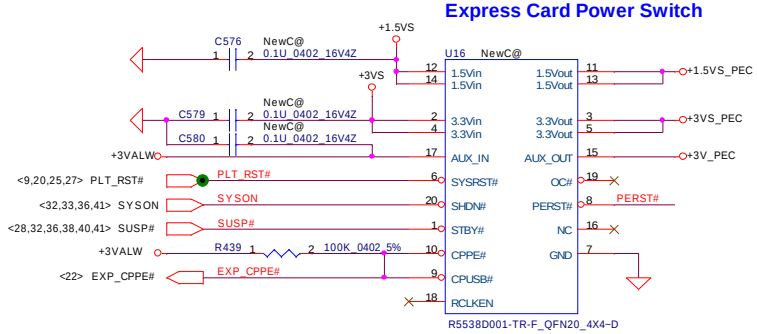


Mini Card 2---WLAN



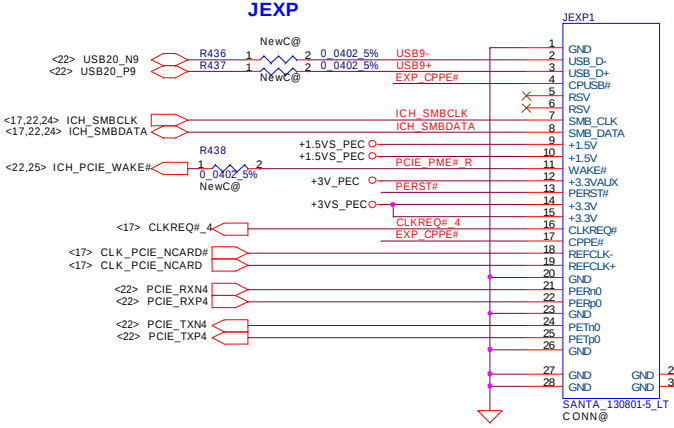
New Card

Express Card Power Switch

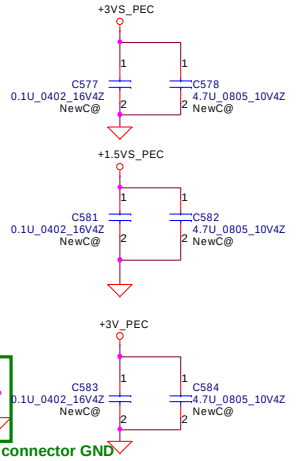


internal pull high to 3.3Vaux-in
EC need setting at Hi-Z & output Low

Close to JEXP



Near to Express Card slot.



01/03 New card PTH connector GND

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Issued Date	2007/08/28	Deciphered Date	2006/07/26

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Compal Electronics, Inc.	
Title	WLAN, WWAN, New Card
Size	Document Number: Montevina Blade UMA LA4101P
Rev	0.3
Date: Saturday, January 05, 2008	Sheet 26 of 46

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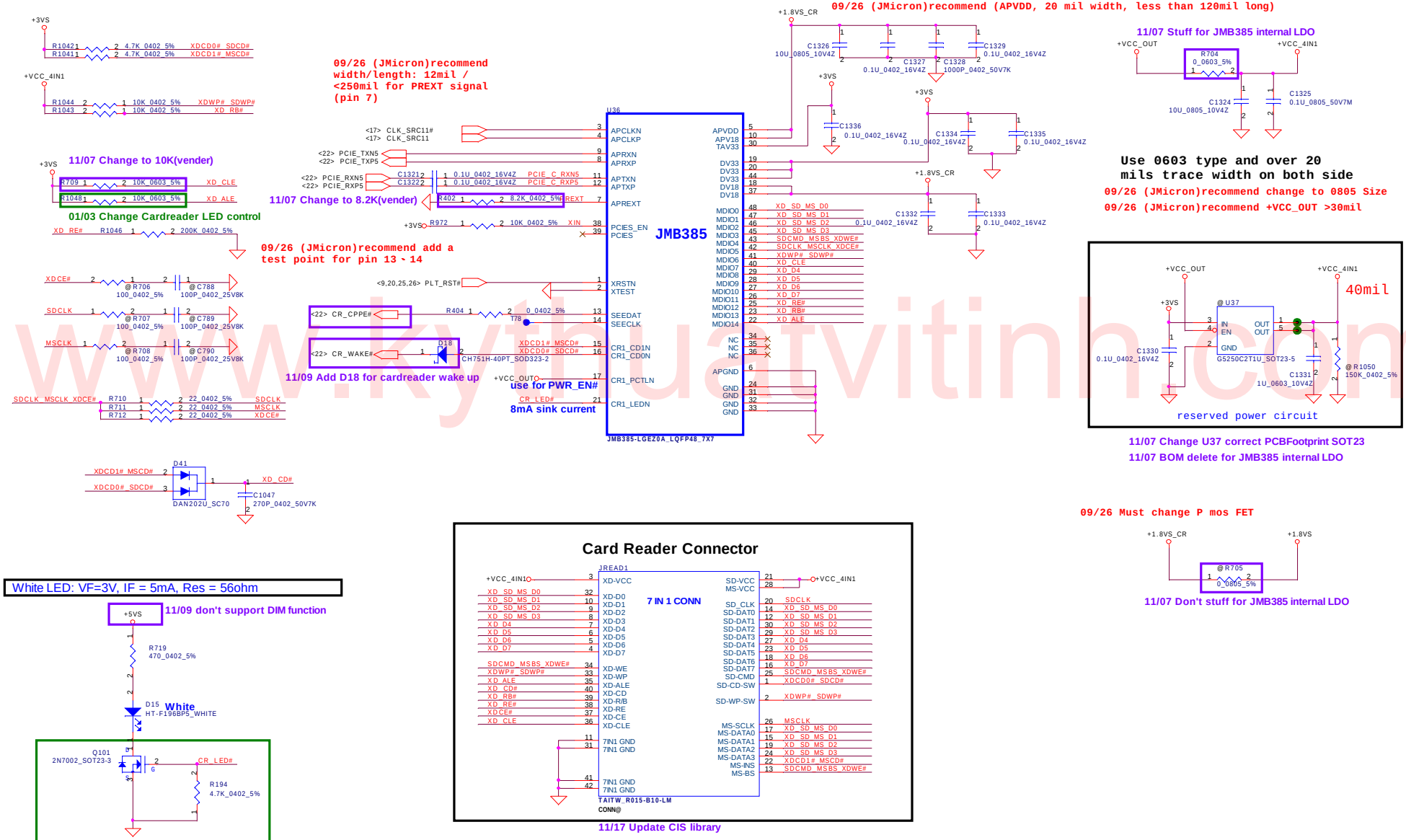

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Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/10/06

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Compal Electronics, Inc.

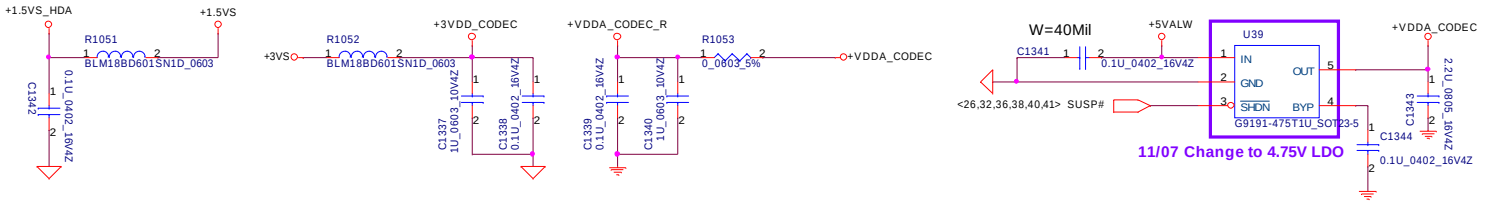
Title: **USB CardReader&CONN**

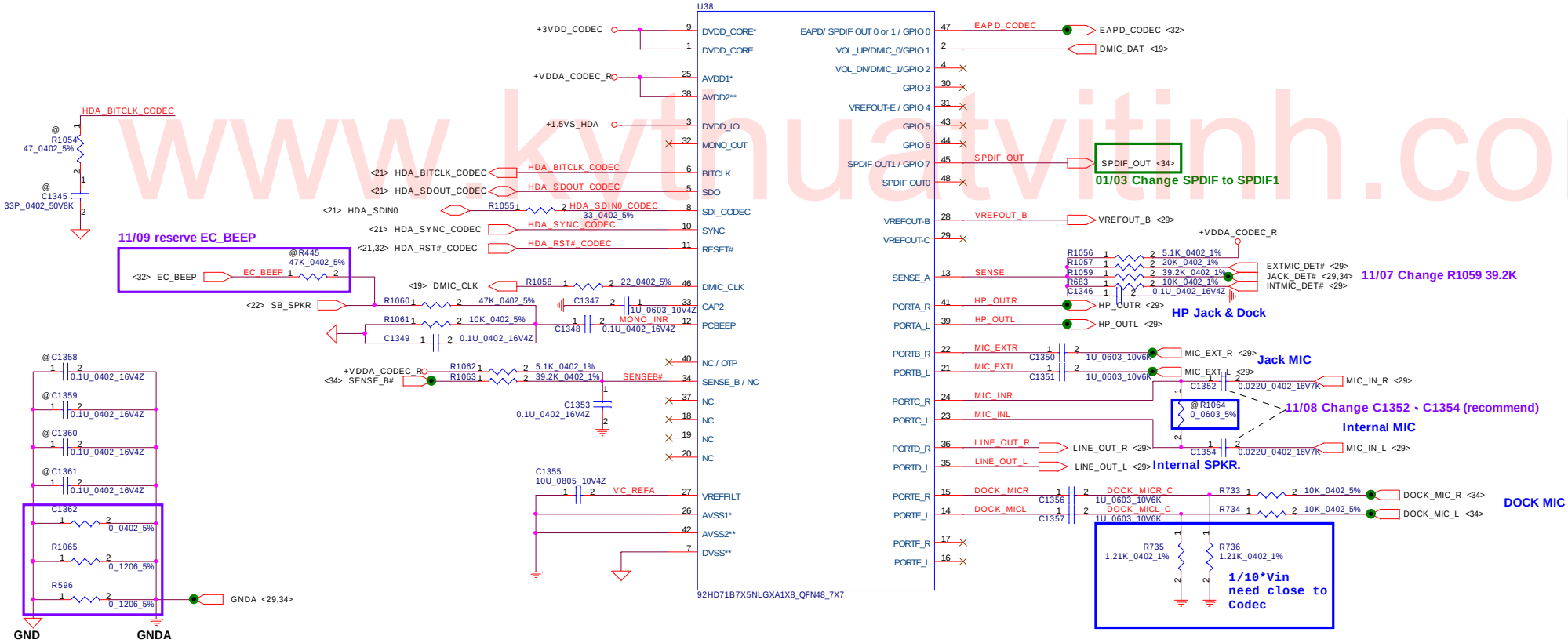
Size	Document Number	Rev
Custom	Montevina Blade UMA LA4101P	0.3

Date: Saturday, January 05, 2008 Sheet 27 of 46

CODEC POWER

(4.75V(4.56~4.94V))
300mA





SENSE A		SENSE B	
Port	Resistor	Port	Resistor
A	39.2K	E	39.2K
B	20K	F	20K
C	10K	G	10K
D	5.11K	H	5.11K

Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

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Title	Codec_IDT9271B7		
Size: Custom	Document Number: Montevina Blade UMA LA4101P		Rev: 0.3
Date: Saturday, January 05, 2008	Sheet 28 of 46		

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GAIN0	GAIN1	Av(inv)
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

11/17 Change to15.6 dB

15.6 dB

Keep 10 mil width

12/18 Shut down pop noise

11/07 Add 10K PU

11/07 Add Capacitor avoid DC lever to Docking audio

8/31EMI request

11/07Change JP60 PCB Footprint from ACES_85204-04001_4P to ACES_88231-04001_4P

SPEAKER

Audio/B & CIR

HP OUT

HP OUT For Docking

HP OUT For M/B

EXTMIC IN

INTMIC IN

MDC 1.5 Conn.

MDC Standoff

Connector for MDC Rev1.5

Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

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Title: AMP & Audio Jack

Size: Custom | Document Number: Montevina Blade UMA LA4101P | Rev: 0.3

Date: Saturday, January 05, 2008 | Sheet 29 of 46

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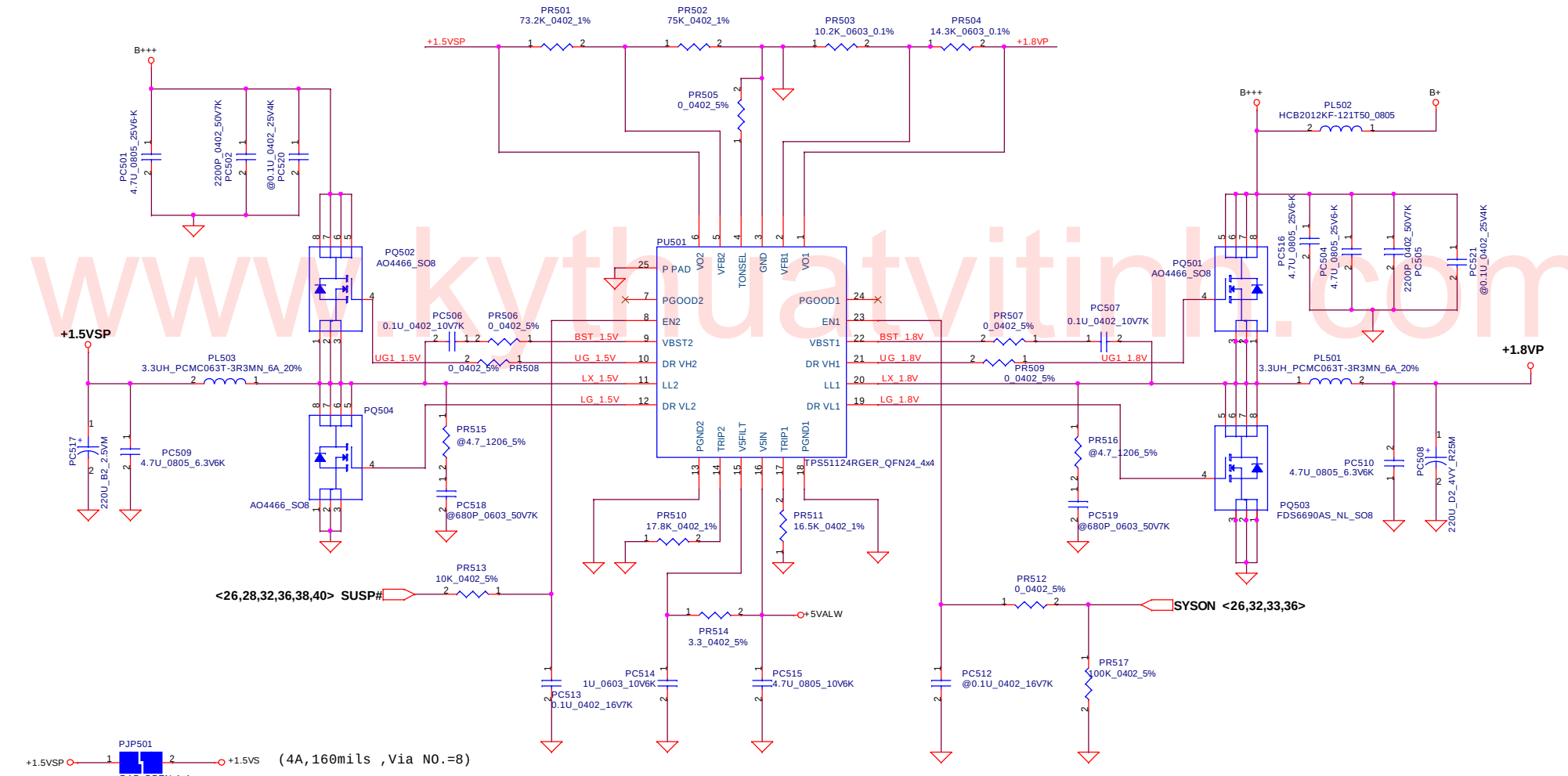

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Issued Date	2007/05/29	Deciphered Date	2008/05/29

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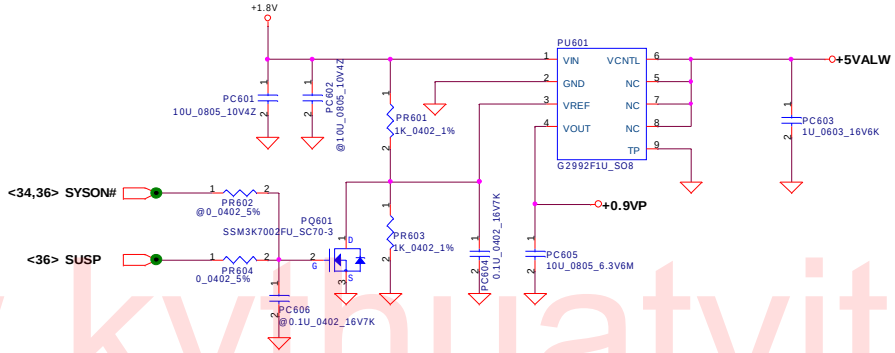
Compal Electronics, Inc.

Title: **1.5VSP/1.8VP**

Size	Document Number	Rev
	Montevina Blade UMA LA4101P	0.3

Date: Saturday, January 05, 2008 Sheet 41 of 46



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(2A,80mils ,Via NO.= 4)

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Issued Date	2006/11/23	Deciphered Date	2007/11/23

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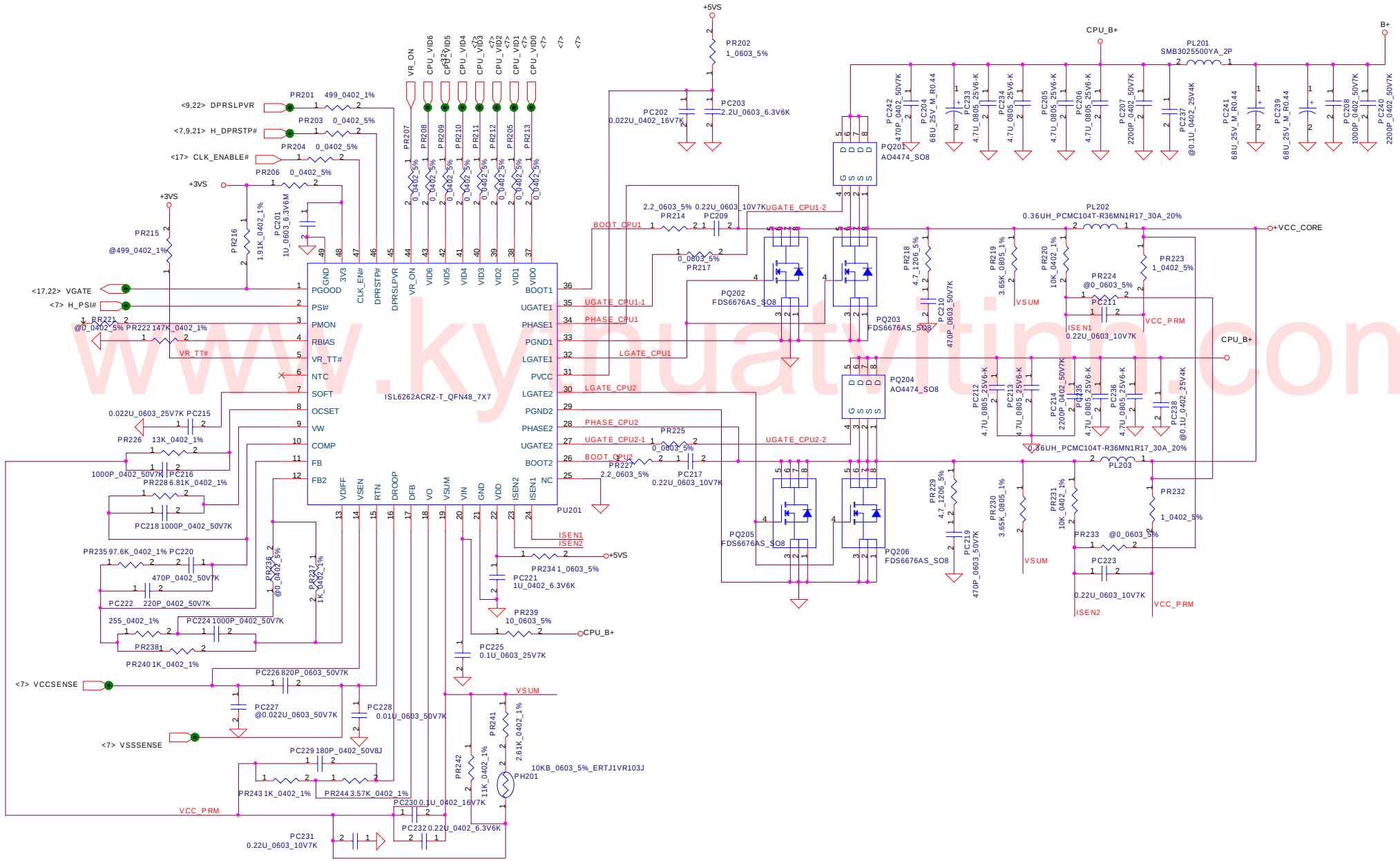
Compal Electronics, Inc.

Title: **0.9VP/1.1V_PCIE**

Size | Document Number: **Montevina Blade UMA LA4101P** | Rev: 0.3

Date: Saturday, January 05, 2008 | Sheet 42 of 46



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Compal Electronics, Inc.

Title: **+CPU_CORE**

Size	Document Number	Rev
Custom		0.3

Date: Saturday, January 05, 2008 | Sheet 43 of 46

Item	Fixed Issue (Reason for change)	PAGE	Modify List	Date	Phase
1	Transation Fail	08	C41、C42、C43、C44 Change ESR=7m ohm	11/21	SI-1
2	Disable TV out function from Docking	11、34	R61、R62、R63 change to 75 Ohm、TV_DCONSEL_0、TV_DCONSEL_1 connect to GND	11/07	SI-1
3	Update Connetor Library		CRT(JCRT1)、HDMI(JHDMI1)、ESATA(JP53)、Finger print(JJP24)、FAN(JP2)、Speaker(JP60)、Multi bay(JP12)、Dual LED(D53、D12)	11/17	SI-1
4	Delete LVDS B channel	11、19	Schematic Delete	11/17	SI-1
5	USB camera Footprint error	19	Change U42 to G916-390T1UF SOT23, it adjustable mode, R1091=215K，R1093=100K	11/07	SI-1
6	Reserve Card reader D3E function	22、27	GPIO6= CR_CPPE#，GPIO22=CR_WAKE#	11/17	SI-1
7	Swap PCIE LAN and New card	22	Swap PCIE4 and PICE6	11/17	SI-1
8	Add HDCP ROM for ICH9M	22、31	Add HDCP ROM for ICH9M	11/17	SI-1
9	Change G sensor control from SB、LED drive by +5VS	22、33	Change G sensor control from SB	11/17	SI-1
10	Avoid Battery mode can't boot issue	22、39	Add +3VALW GD to EC_RSMRST# to fix Battery mode can't boot issue	11/17	SI-1
11	Add G sensor ST and Bosch	24	Add G sensor ST and Bosch	11/17	SI-1
12	Change LAN solution (Marvell to Realtek)	25	Change LAN solution (Marvell to Realtek)	11/17	SI-1
13	LAN can't work	25	U46 Change to correct transformer type	11/17	SI-1
14	Cardreader schematic review and update, add D3E function	27	R709-->10K、R402-->8.2K、R704-->Stuff、R705-->@、U37-->@、Cardreader LED-->+5VS、add D3E function	11/17	SI-1
15	Jack can't detect normal	28	R1059 change from 39.2 to 39.2K	11/17	SI-1
16	Speaker work un normal	28	Add and Stuff C1362、R1065、R596	11/17	SI-1
17	HP audio team recommend	28、29	C285~C292、C1352、C1354 change to 0.022U、Amp output setup to 15.6 dB、Reserve C305、C306 for GNDA and GND	11/17	SI-1
18	Audio jack can't detect normal	29	Add Pull up resistor R401 to +3VALW	11/17	SI-1
19	Docking HP audio test fail	29	Add C295□BC296 to avoid DC level, and add R409、R410 to reduce HP out level	11/17	SI-1
20	Leakage problem	32	Correct direction pretect leakage	11/07	SI-1
21	EC pin define update	32	Delete EC_PME#、SYSON PU、SUSP# PU、LID_SW# change to +3VALW、Delete CLKRUN#、R582->@ for C0 chip、CIR PU+5VL、add 100P to BATT_OVP(EC_recommend)	11/07	SI-1
22	Can't Hibernation(SLP_S4#)	32	Connect SLP_S4# to SB	11/17	SI-1
23	EC can't receive docking present	34	CONA# change +3VL	11/12	SI-1
24	HDMI can't detect	35	DDC _EN must enable 、TMDS_B_HPD# inverse	11/07	SI-1
25	LVDS power on timing	19	C238 change to 0.047u to meet TI timing	01/03	SI-2
26	Prevent WWAN nosie	21	Add 12p on HDA_SDOUT and HDA_SDOUT	01/03	SI-2
27	Power leakage	21、31	Change HDCP ROM to +3VS power plane	01/03	SI-2
28	Prevent WLAN leakage	26	Add Diode prevent WLAN leakage	01/03	SI-2

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Title: PIR
Size: Document Number: Montevina Blade UMA LA4101P Rev: 0.3
Date: Saturday, January 05, 2008 Sheet 44 of 46

Item	Fixed Issue (Reason for change)	PAGE	Modify List	Date	Phase
29	New card PTH connector GND	26	New card PTH connector GND	01/03	SI-2
30	Change Cardreader LED control	27	Change Cardreader LED control	01/03	SI-2
31	Change SPDIF to SPDIF1	28	Change to SPDIF1	01/03	SI-2
32	Shut down pop noise	29	Change C293 to 1U	01/03	SI-2
33	Change BT power to +3VS	30	Change BT power to +3VS	01/03	SI-2
34	EMI Request	31	SPI_FSEL#、SPI_CLK_R、SPI_FWR# reserver RC	01/03	SI-2
35	Reserver 0 ohm co lay with common choke	35	Reserver 0 ohm co lay with common choke	01/03	SI-2
36	Sparate+5VS and +3VS power timing	36	Sparate+5VS and +3VS power timing	01/03	SI-2
37	Keyboard backlight reserve a 0805 size resistor	33	Keyboard backlight reserve a 0805 size resistor	01/03	SI-2
38	Change Lid switch connector type	33	Change Lid switch connector type	01/03	SI-2
39					
40					
41					
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54					
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56					

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Version Change List (P. I. R. List) for Power Circuit

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	37	DC Connector /CPU_OTP	11/06	Compal	Add PD4 & PC12	Add PD4 & PC12	
2	39	3.3VALWP/5VALWP	11/06	Compal	for Layout	Change PQ301 cancel PQ303	
3	38	Charger	11/06	Compal	EMI solution	Add pc128	
4	43	+CPU_CORE	11/06	Compal	EMI solution	Add PC240	
5	39	3.3VALWP/5VALWP	11/14	Compal	for Layout	Change PL303 and PC310	
6	38	Charger	12/31	Compal	EMI solution	Add PC129, PC130, PC131, PC132, PC133	
7	43	+CPU_CORE	12/31	Compal	EMI solution	Add PC242	
8	39	3.3VALWP/5VALWP	12/31	Compal	PWR request	Add PU302, control signal changed to ACOFF	
9							
10							
11							
12							
13							
14							

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