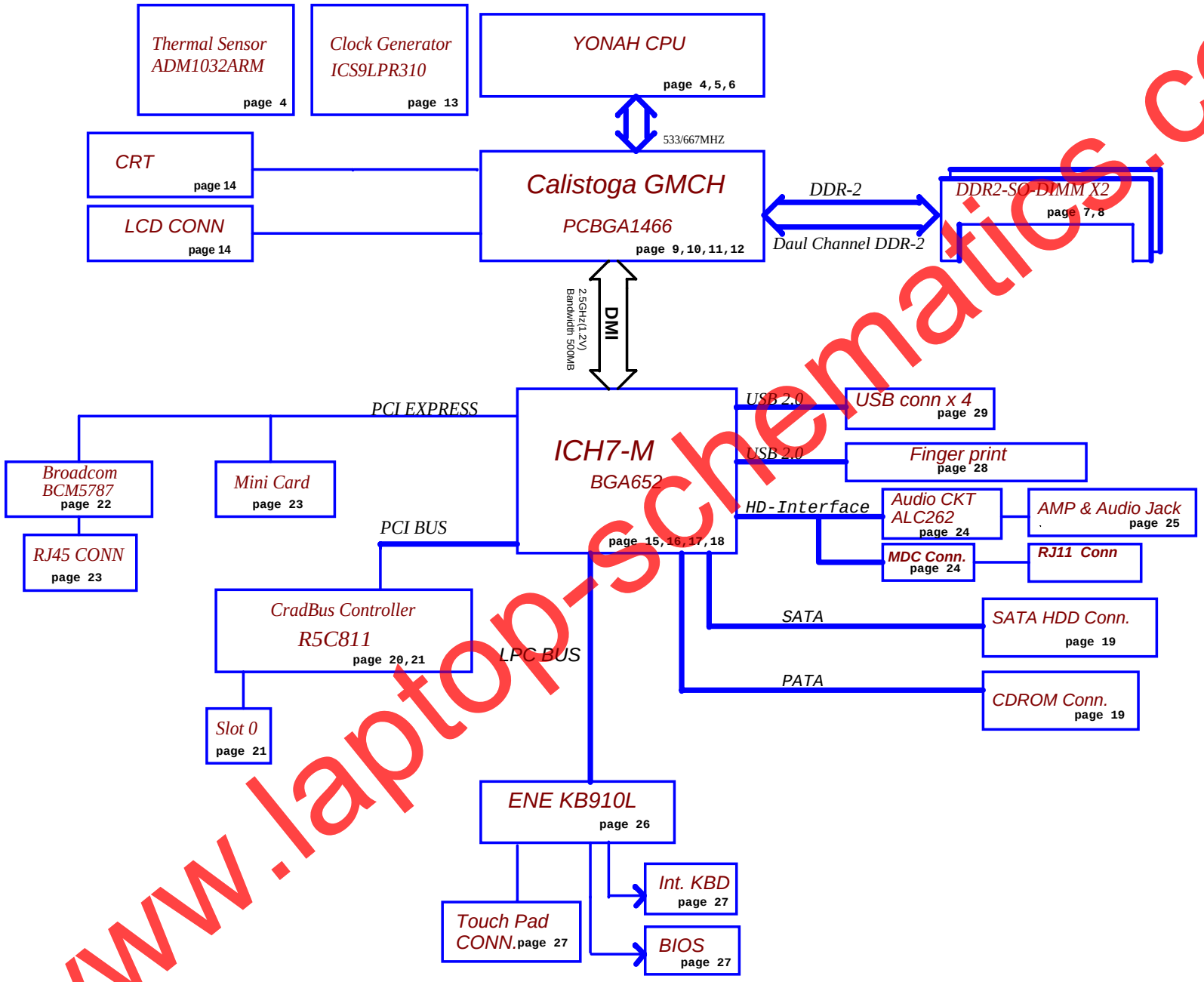
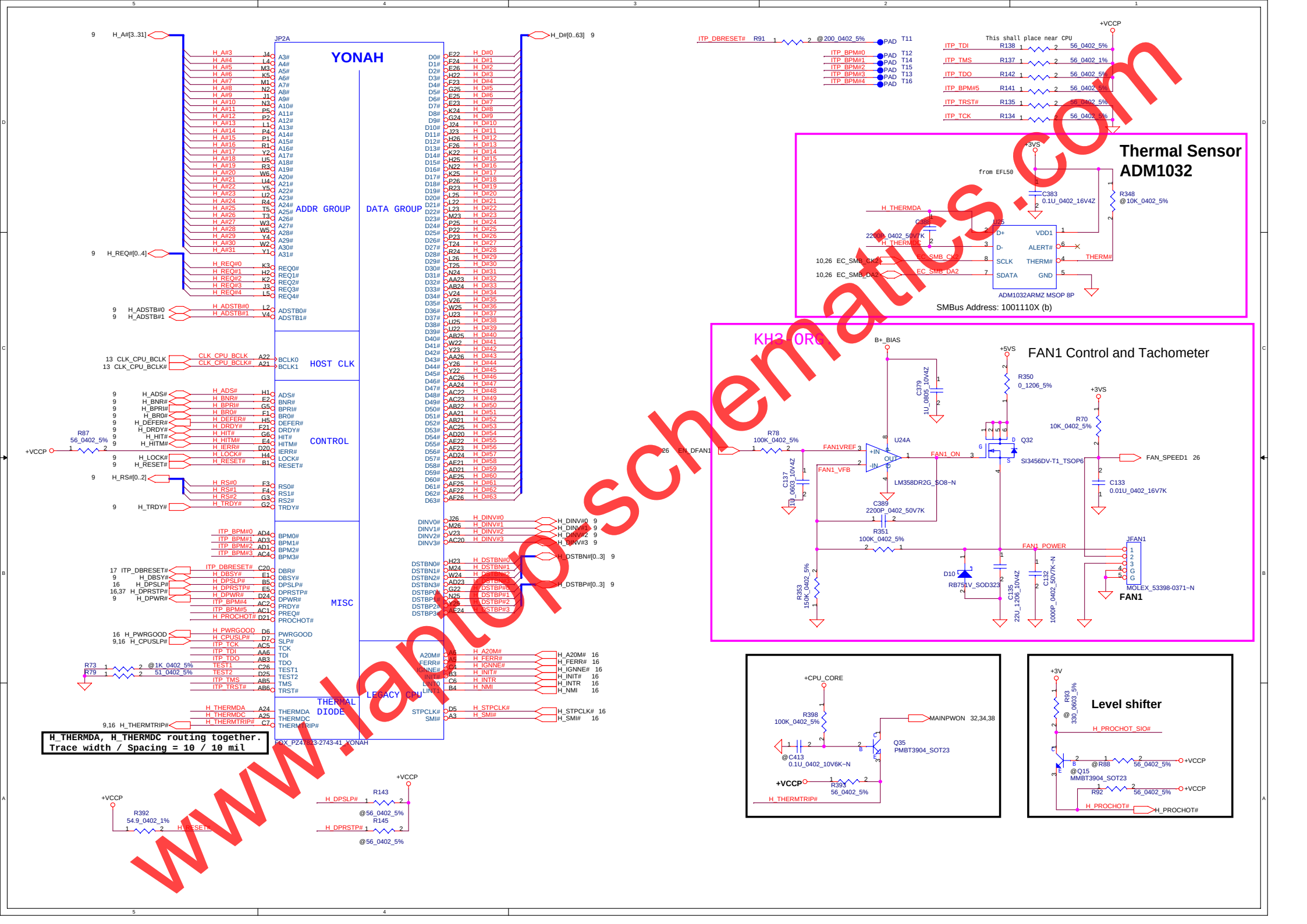
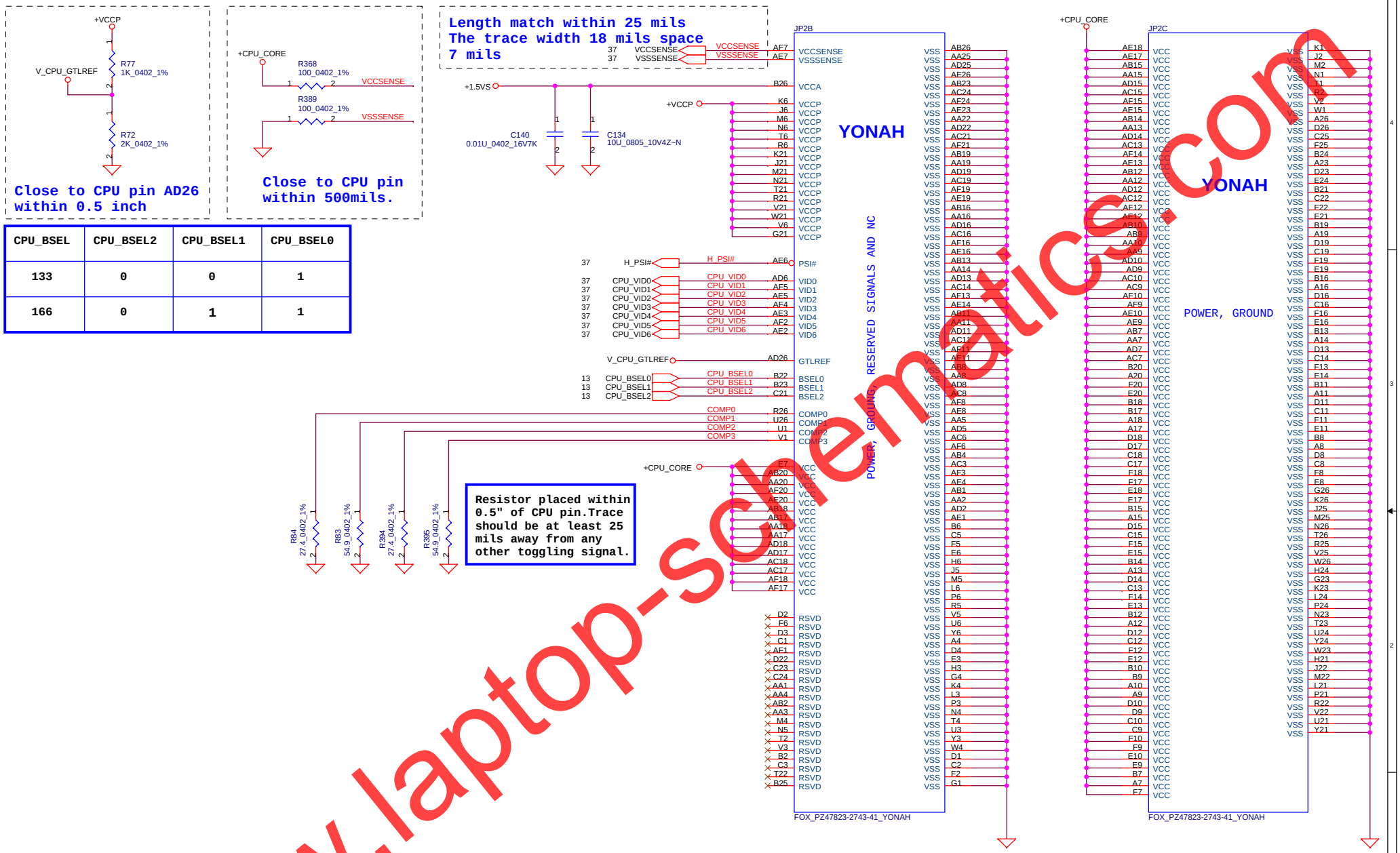
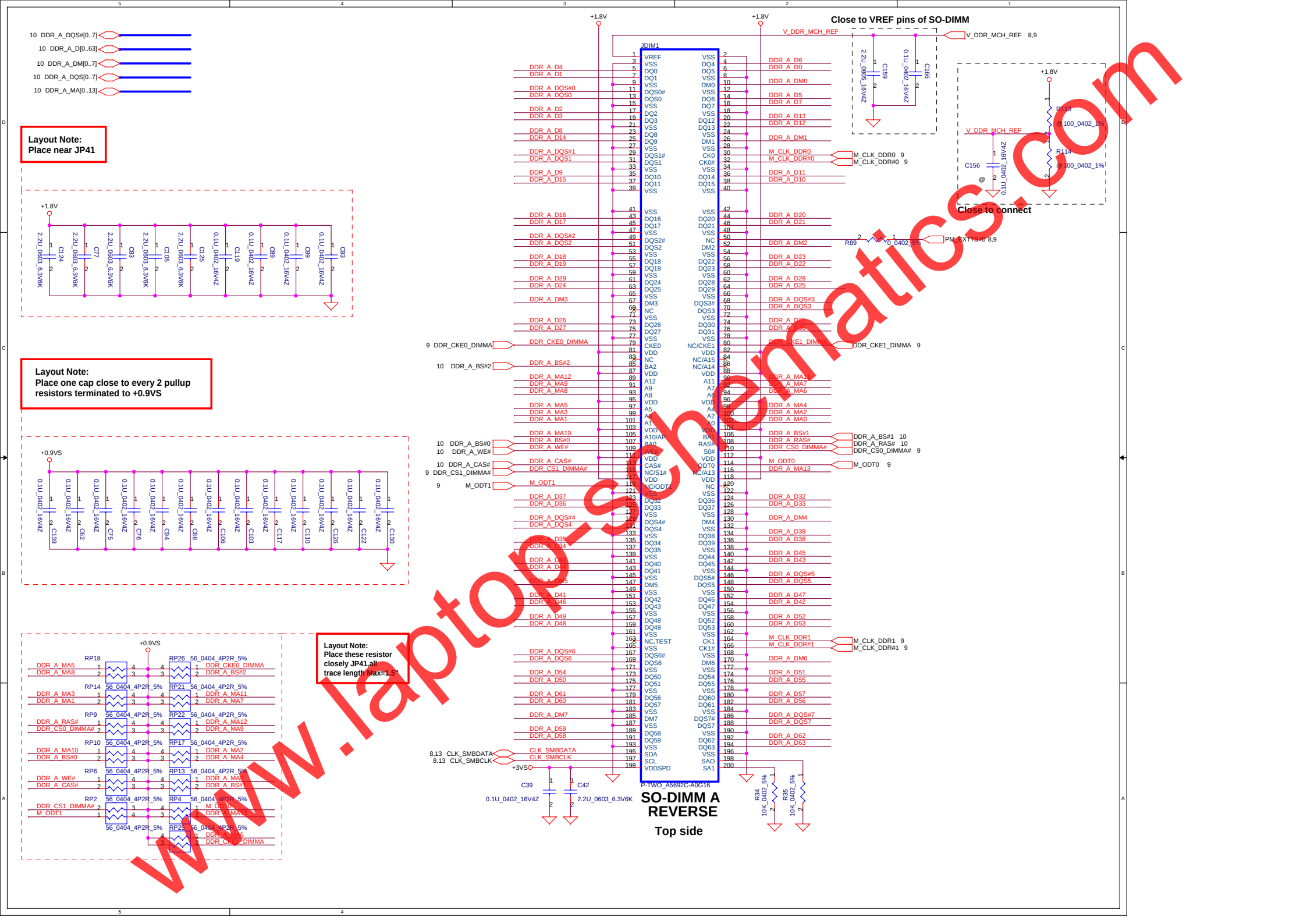






CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1


10 DDR_A_DQS#[0..7]
10 DDR_A_D[0..63]
10 DDR_A_DM[0..7]
10 DDR_A_DQS[0..7]
10 DDR_A_MA[0..13]
Layout Note:
Place near JP41
+1.8V
2.2U_0603_6.3V6K
0.1U_0402_16V4Z
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS
+0.9VS
Layout Note:
Place these resistor
closely JP41,all
trace length Max=1.5"
+0.9VS
RP18
RP26_56_0404_4P2R_5%
RP14
RP21_56_0404_4P2R_5%
RP9
RP22_56_0404_4P2R_5%
RP10
RP17_56_0404_4P2R_5%
RP6
RP13_56_0404_4P2R_5%
RP2
RP4_56_0404_4P2R_5%
56_0404_4P2R_5%
RP25_56_0404_4P2R_5%
DDR_A_MA5
DDR_A_MA8
DDR_CKE0_DIMMA
DDR_A_BS#2
DDR_A_MA3
DDR_A_MA1
DDR_A_MA11
DDR_A_MA7
DDR_A_RAS#
DDR_CS0_DIMMA#
DDR_A_MA12
DDR_A_MA9
DDR_A_MA10
DDR_A_BS#0
DDR_A_MA2
DDR_A_MA4
DDR_A_WE#
DDR_A_CAS#
DDR_A_BS#1
DDR_A_MA0
DDR_CS1_DIMMA#
M_ODT1
DDR_A_MA6
DDR_CKE1_DIMMA
+1.8V
+3VS
JDIM1
P-TWO_A5692C-A0G16
SO-DIMM A
REVERSE
Top side
Close to VREF pins of SO-DIMM
V_DDR_MCH_REF
V_DDR_MCH_REF 8,9
C159
C106
Close to connect
R113
R114
@100_0402_1%
C156
R89
0_0402_5%
PM_EXTTS#0 8,9
DDR_A_D4
DDR_A_D1
DDR_A_DQS#0
DDR_A_DQS0
DDR_A_D2
DDR_A_D3
DDR_A_D8
DDR_A_D14
DDR_A_DQS#1
DDR_A_DQS1
DDR_A_D9
DDR_A_D15
DDR_A_D16
DDR_A_D17
DDR_A_DQS#2
DDR_A_DQS2
DDR_A_D18
DDR_A_D19
DDR_A_D29
DDR_A_D24
DDR_A_DM3
DDR_A_D26
DDR_A_D27
DDR_A_D37
DDR_A_D36
DDR_A_DQS#4
DDR_A_DQS4
DDR_A_D35
DDR_A_D34
DDR_A_D41
DDR_A_D46
DDR_A_D49
DDR_A_D48
DDR_A_DQS#6
DDR_A_DQS6
DDR_A_D54
DDR_A_D50
DDR_A_D61
DDR_A_D60
DDR_A_DM7
DDR_A_D59
DDR_A_D58
CLK_SMBDATA
CLK_SMBCLK
C39
C42
0.1U_0402_16V4Z
2.2U_0603_6.3V6K
R34
R35
10K_0402_5%
DDR_A_D6
DDR_A_D0
DDR_A_DM0
DDR_A_D5
DDR_A_D7
DDR_A_D13
DDR_A_D12
DDR_A_DM1
M_CLK_DDR0
M_CLK_DDR#0
DDR_A_D11
DDR_A_D10
DDR_A_D20
DDR_A_D21
DDR_A_DM2
DDR_A_D23
DDR_A_D22
DDR_A_D28
DDR_A_D25
DDR_A_DQS#3
DDR_A_DQS3
DDR_A_D31
DDR_A_D30
DDR_CKE1_DIMMA
DDR_A_MA11
DDR_A_MA7
DDR_A_MA6
DDR_A_MA4
DDR_A_MA2
DDR_A_MA0
DDR_A_BS#1
DDR_A_RAS#
DDR_CS0_DIMMA#
M_ODT0
DDR_A_MA13
DDR_A_D32
DDR_A_D33
DDR_A_DM4
DDR_A_D39
DDR_A_D38
DDR_A_D45
DDR_A_D43
DDR_A_DQS#5
DDR_A_DQS5
DDR_A_D47
DDR_A_D42
DDR_A_D52
DDR_A_D53
M_CLK_DDR1
M_CLK_DDR#1
DDR_A_DM6
DDR_A_D51
DDR_A_D55
DDR_A_D57
DDR_A_D56
DDR_A_DQS#7
DDR_A_DQS7
DDR_A_D62
DDR_A_D63
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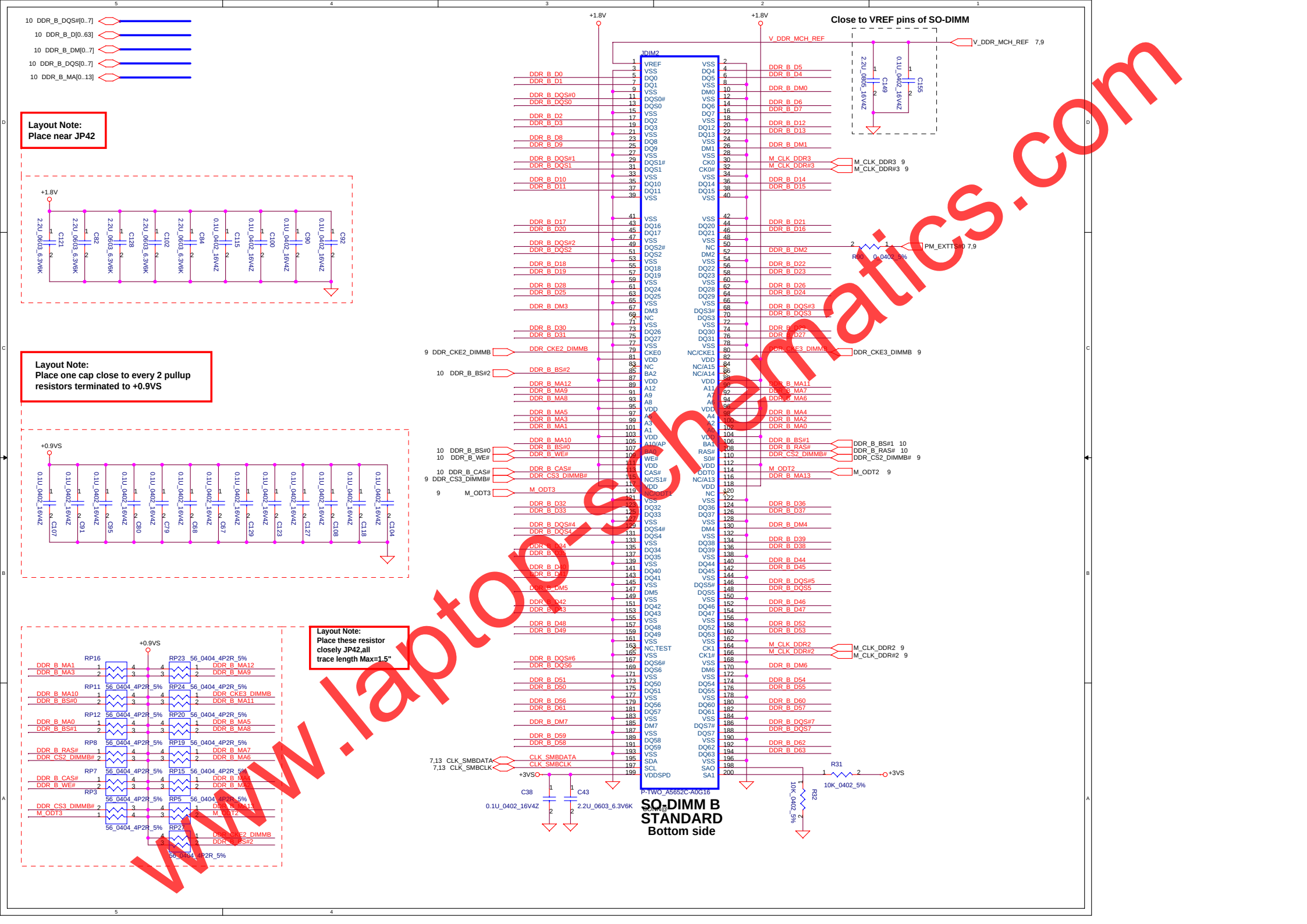
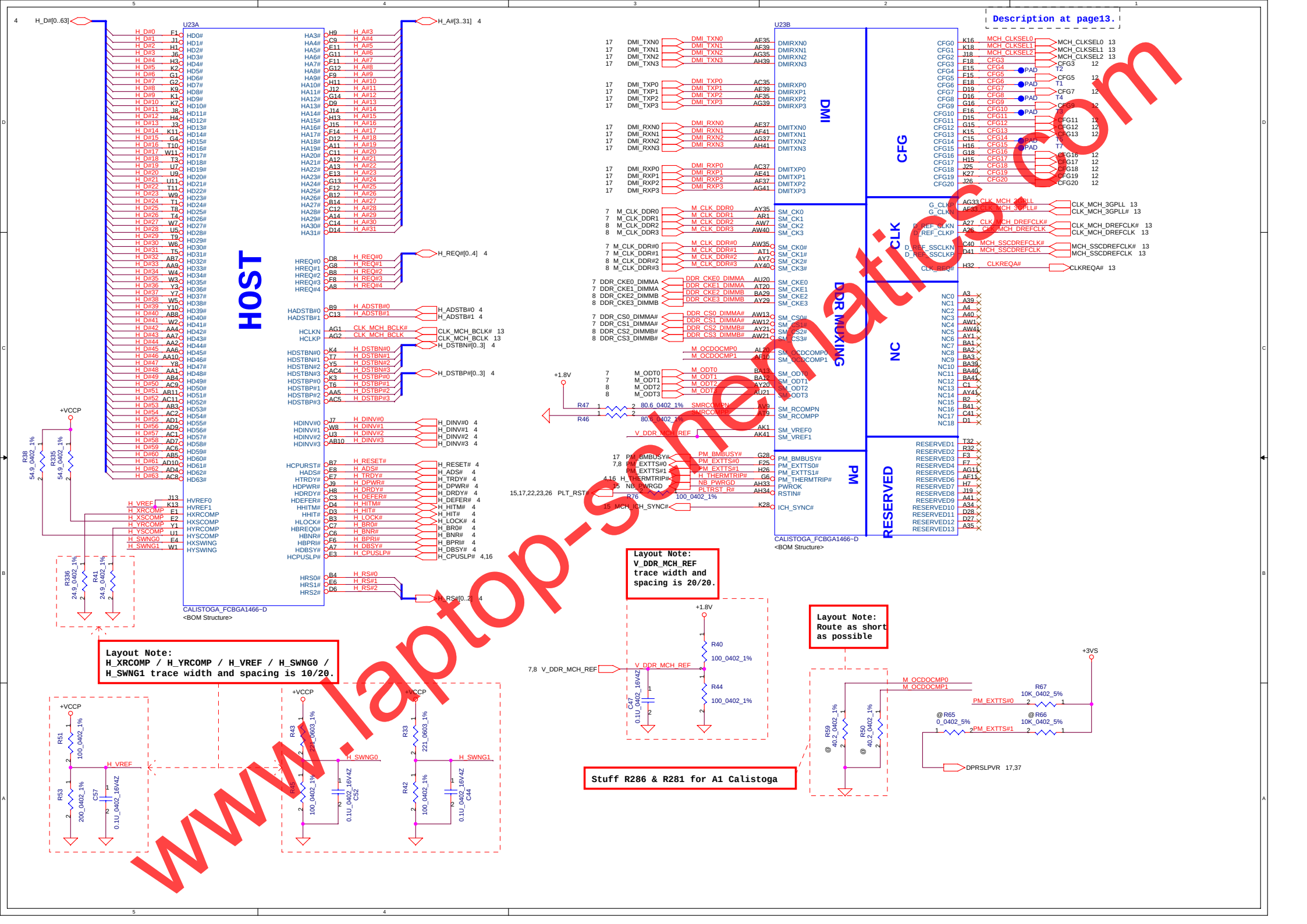
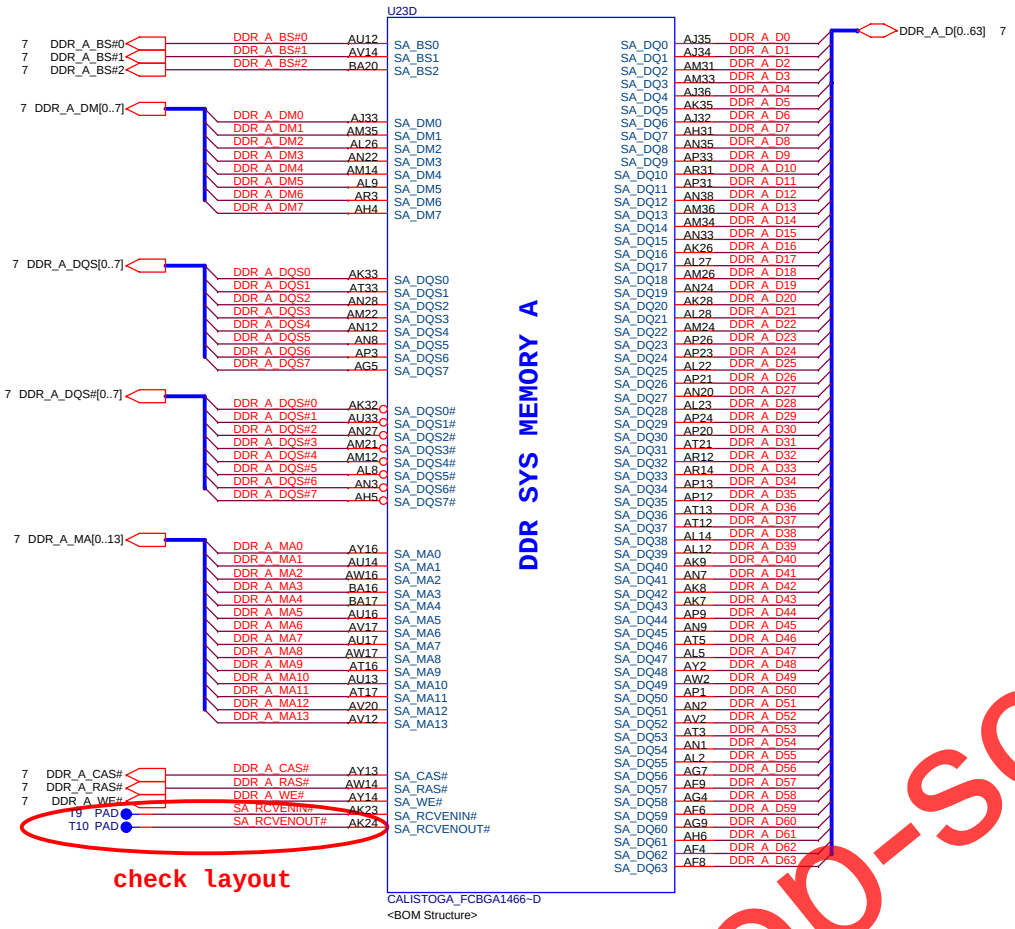
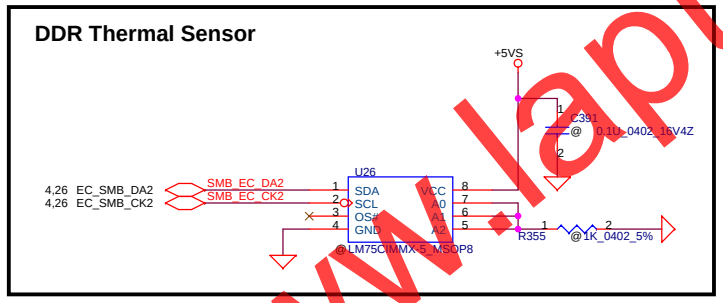
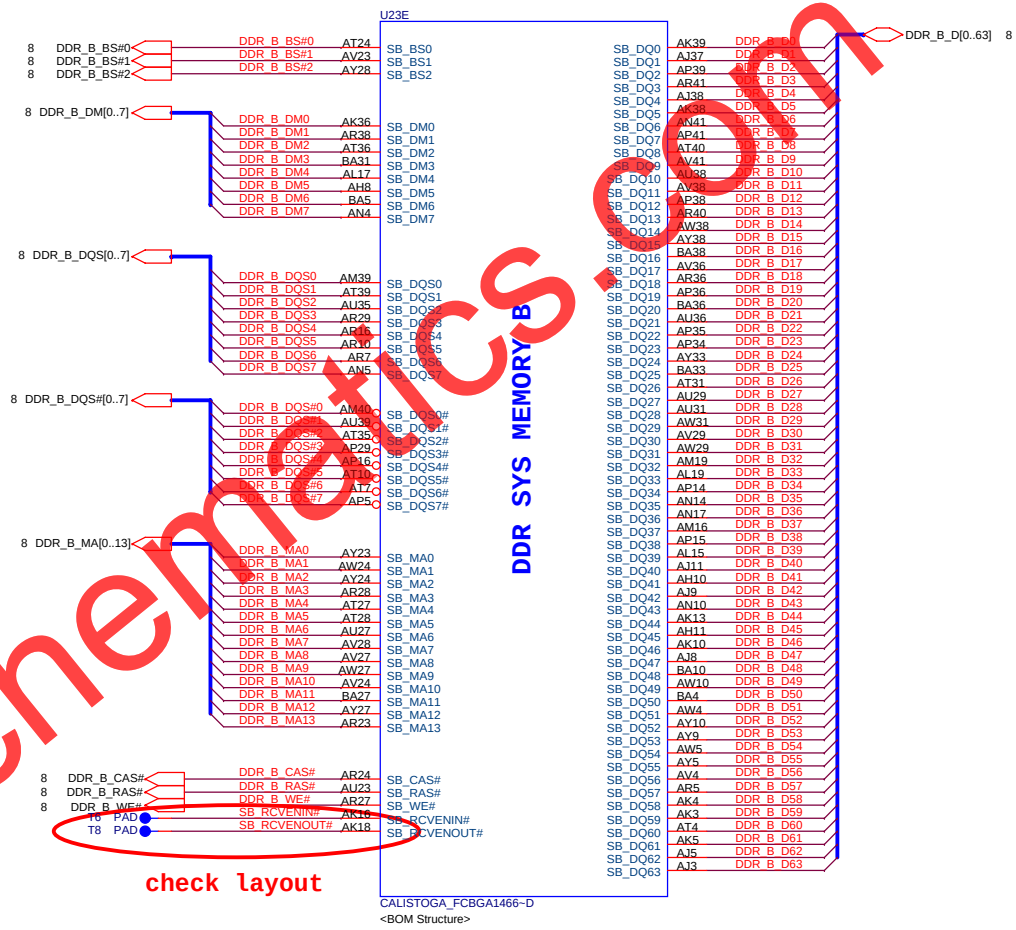
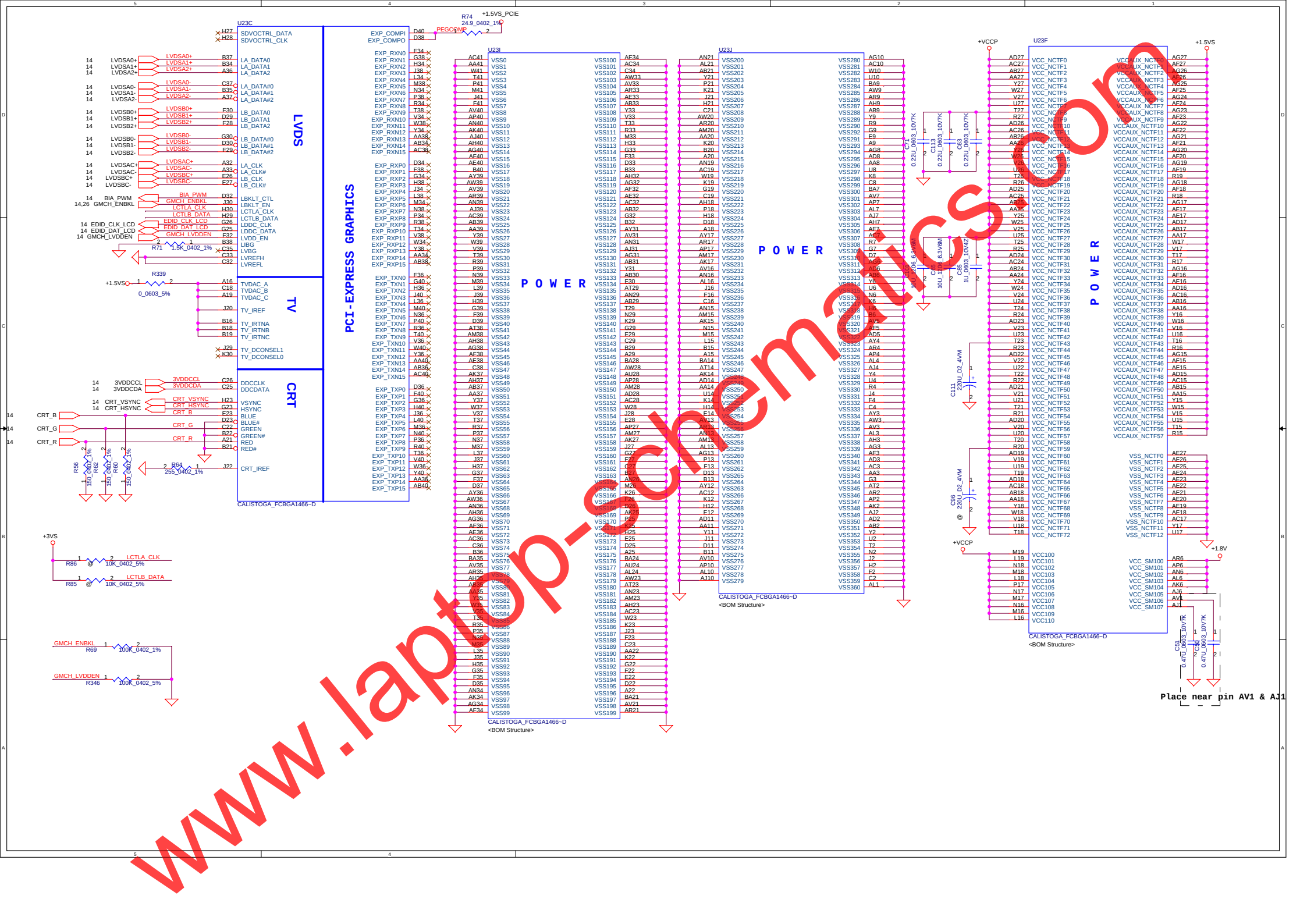


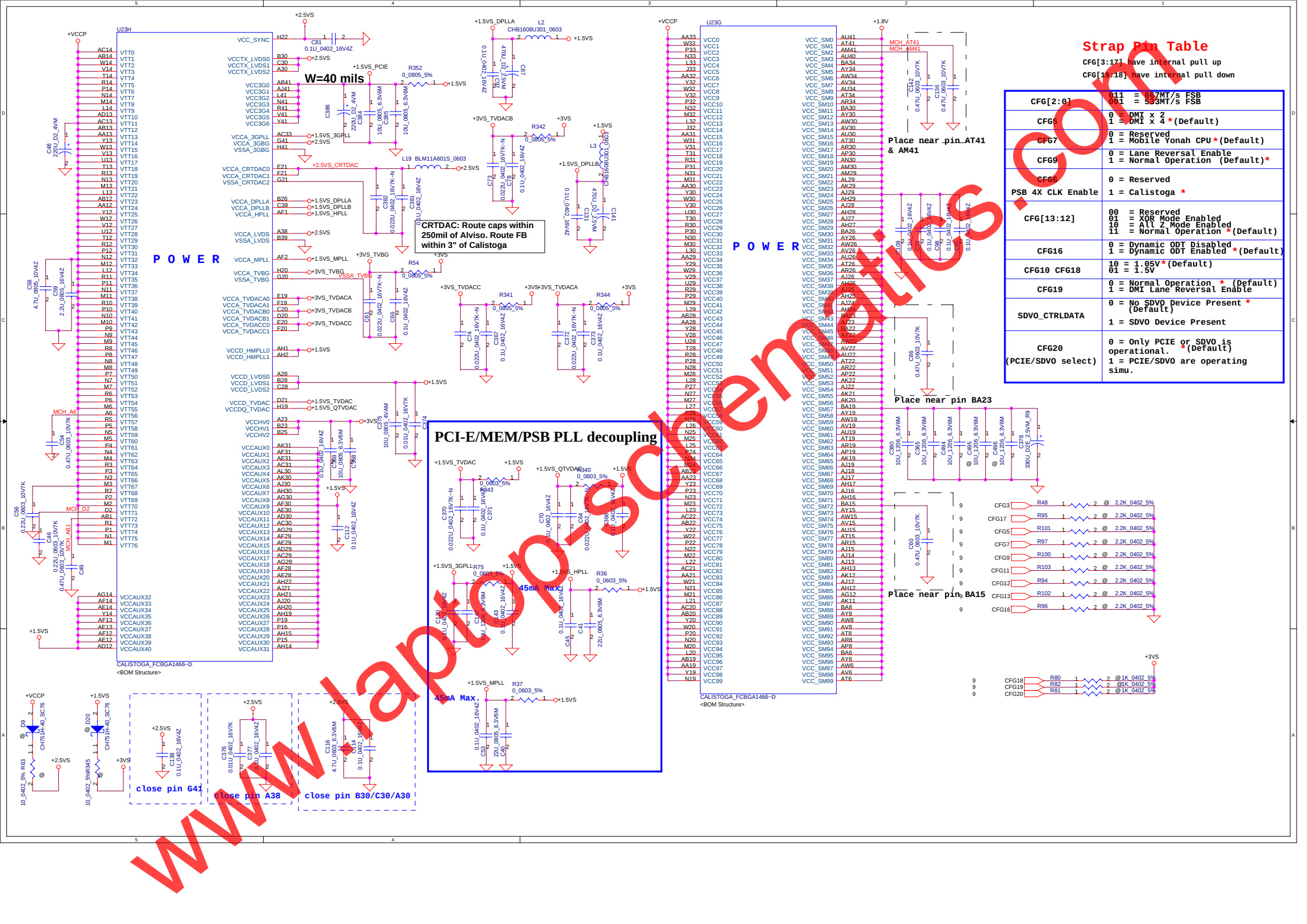


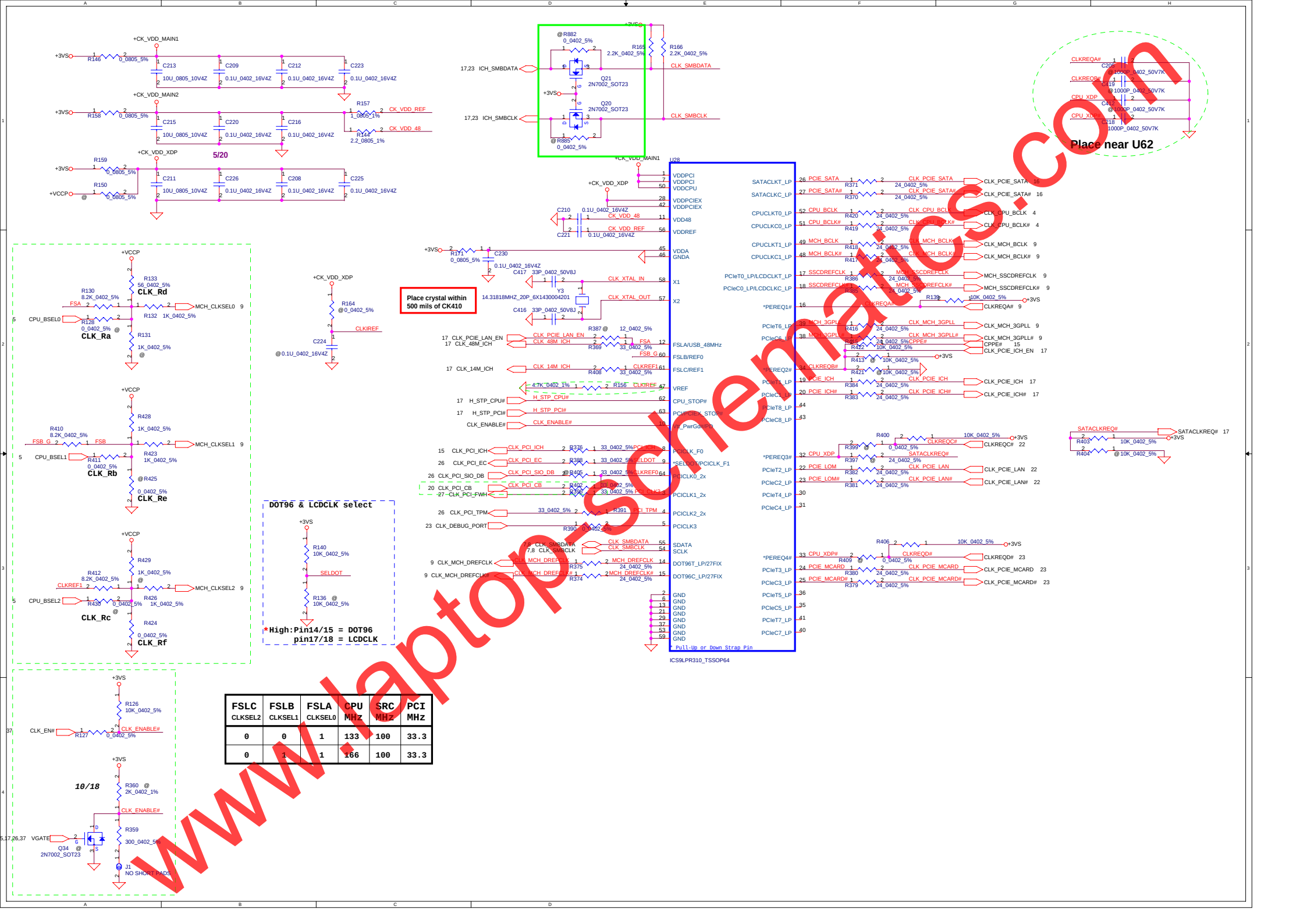




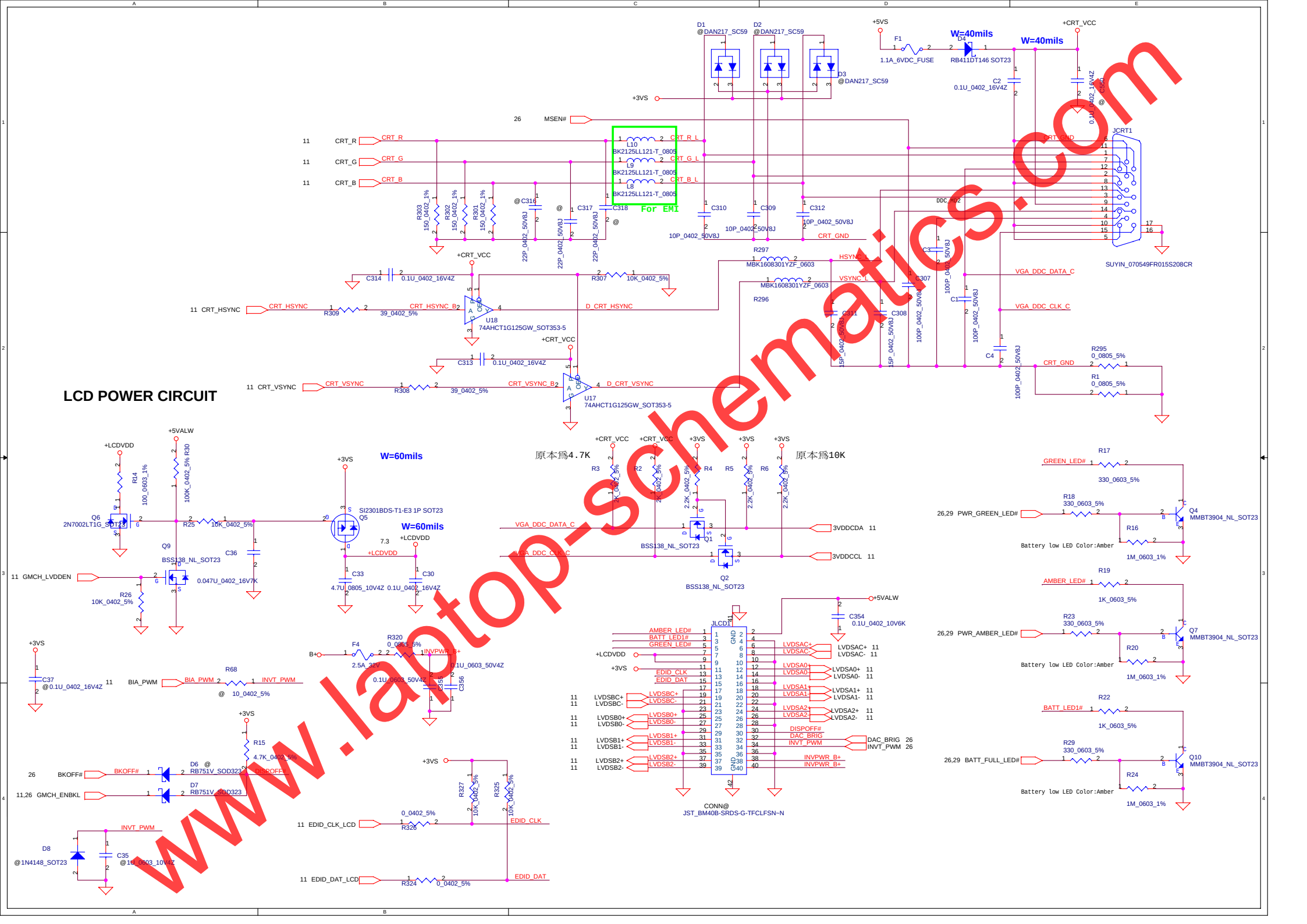


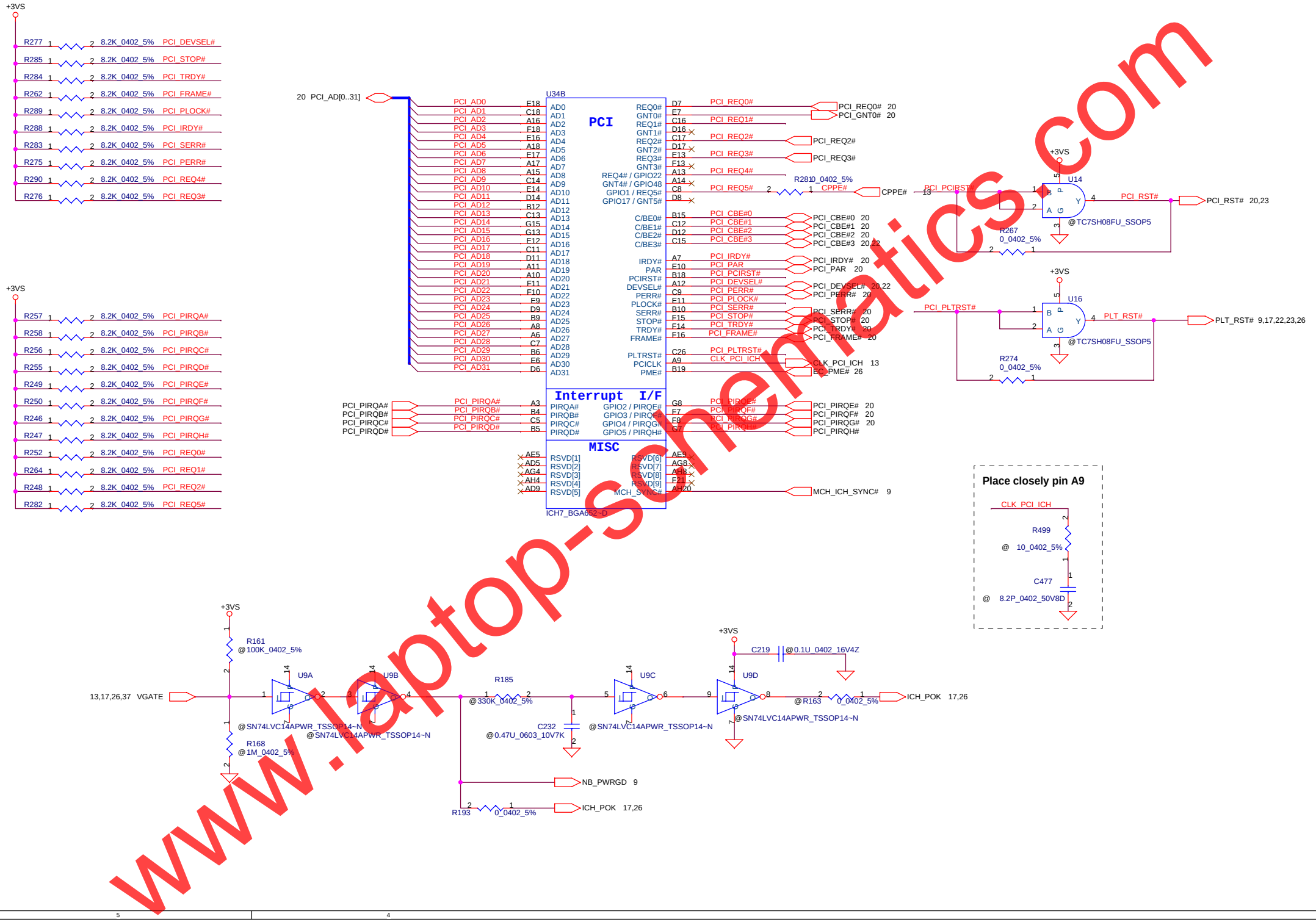


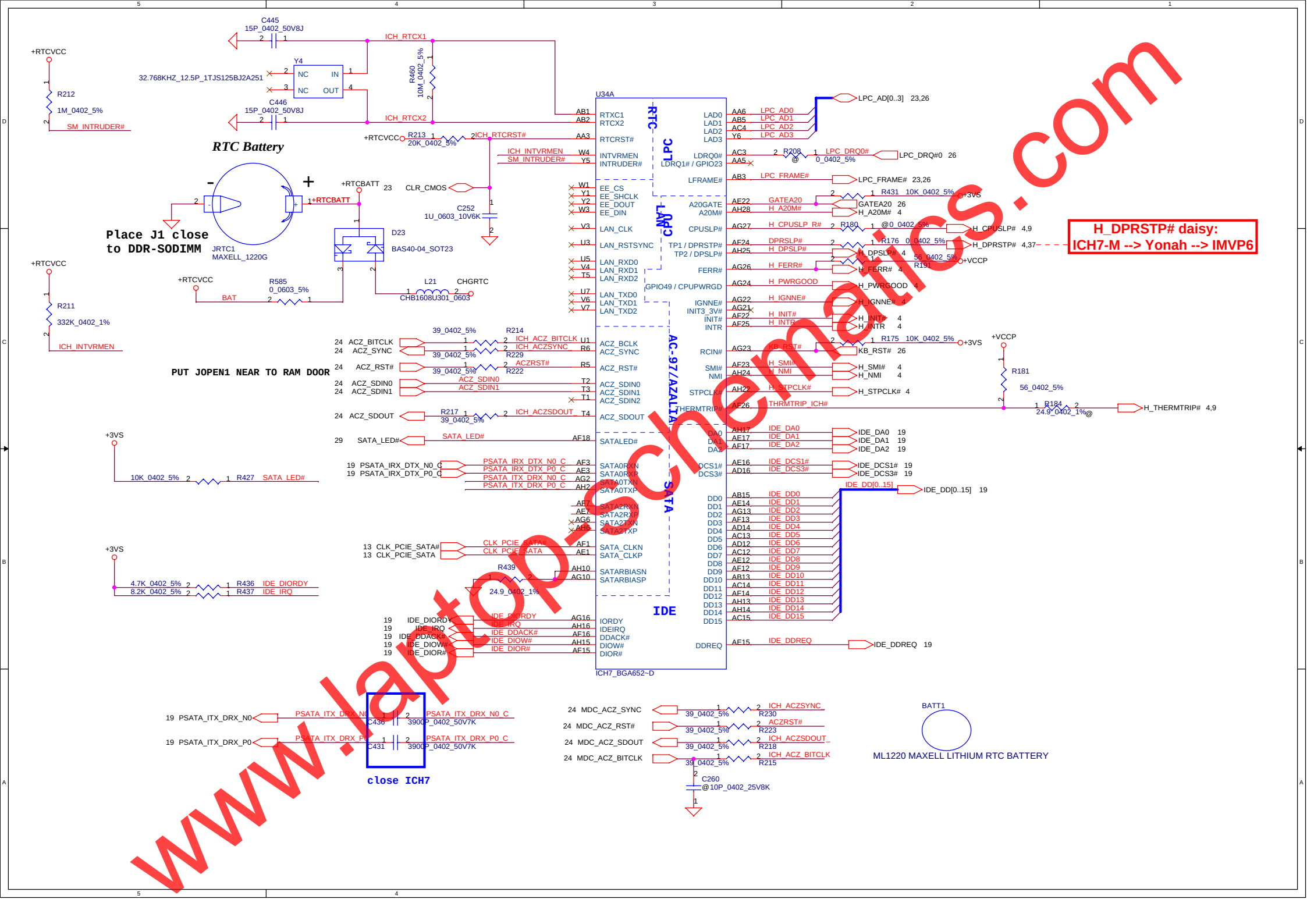




FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	1	133	100	33.3
0	1	1	166	100	33.3






RTC Battery
Place J1 close to DDR-SODIMM
PUT JOPEN1 NEAR TO RAM DOOR
close ICH7
ML1220 MAXELL LITHIUM RTC BATTERY
H_DPRSTP# daisy:
ICH7-M --> Yonah --> IMVP6
U34A
ICH7_BGA652~D
RTC
LPC
LAN
AC-97/AZALIA
SATA
IDE
C445 15P_0402_50V8J
C446 15P_0402_50V8J
Y4 32.768KHZ_12.5P_1TJS125BJ2A251
R460 10M_0402_5%
R212 1M_0402_5%
R211 332K_0402_1%
R213 20K_0402_5%
C252 1U_0603_10V6K
D23 BAS40-04_SOT23
JRTC1 MAXELL_1220G
R585 0_0603_5%
L21 CHB1608U301_0603
R214 R229 R222 R217 R427 R436 R437 R439
R208 R431 R176 R180 R175 R181 R184 R191
C436 C431 C260
BATT1
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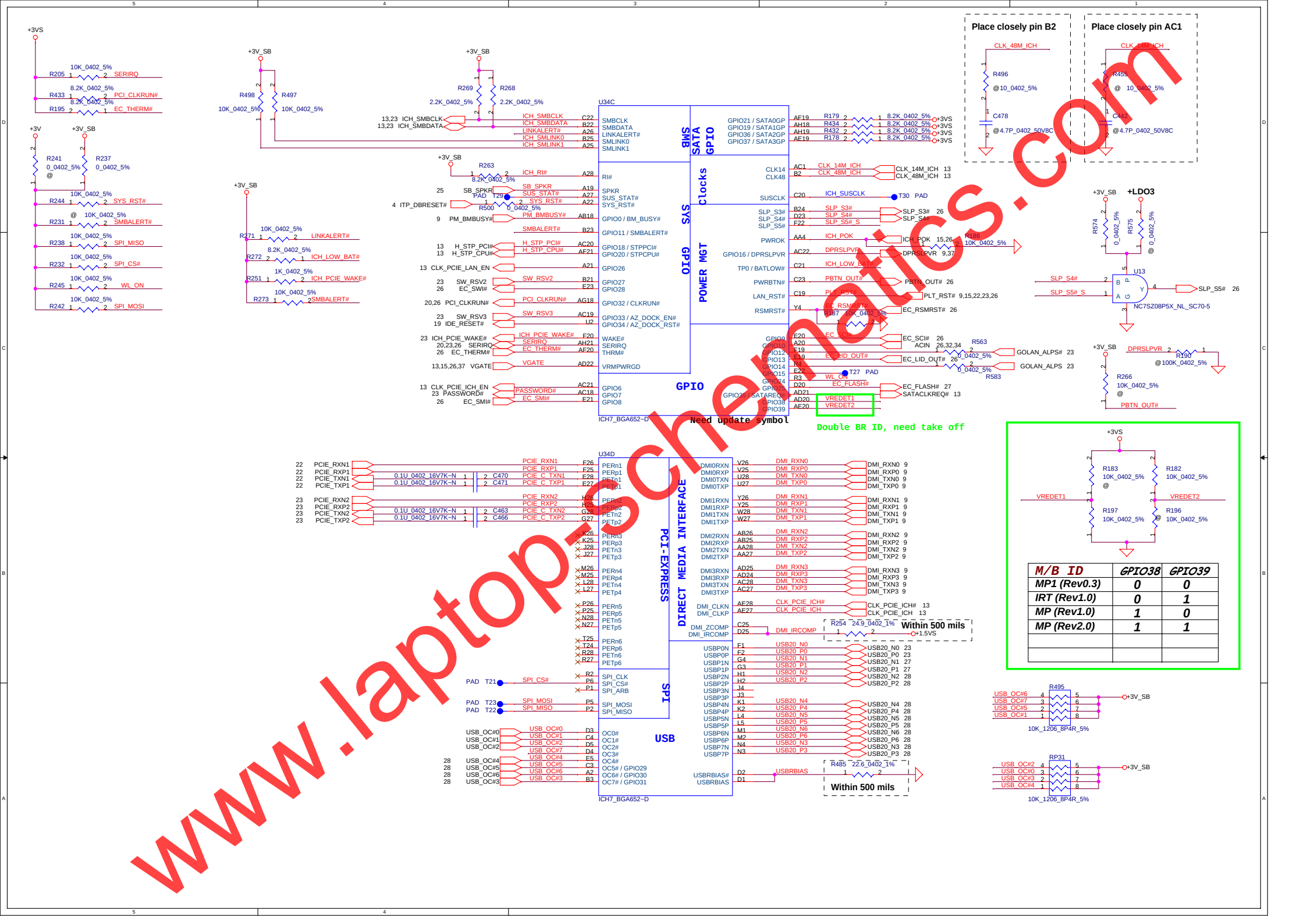
Place closely pin B2
Place closely pin AC1
Need update symbol
Double BR ID, need take off
Within 500 mils
Within 500 mils
GPIO
USB
SPI
PCI-EXPRESS
DIRECT MEDIA INTERFACE
SMB
SATA GPIO
Clocks
SYS
GPIO
POWER MGT
ICH7_BGA652-D
U34C
U34D
U13
+LDO3
M/B ID | GPIO38 | GPIO39
MP1 (Rev0.3) | 0 | 0
IRT (Rev1.0) | 0 | 1
MP (Rev1.0) | 1 | 0
MP (Rev2.0) | 1 | 1
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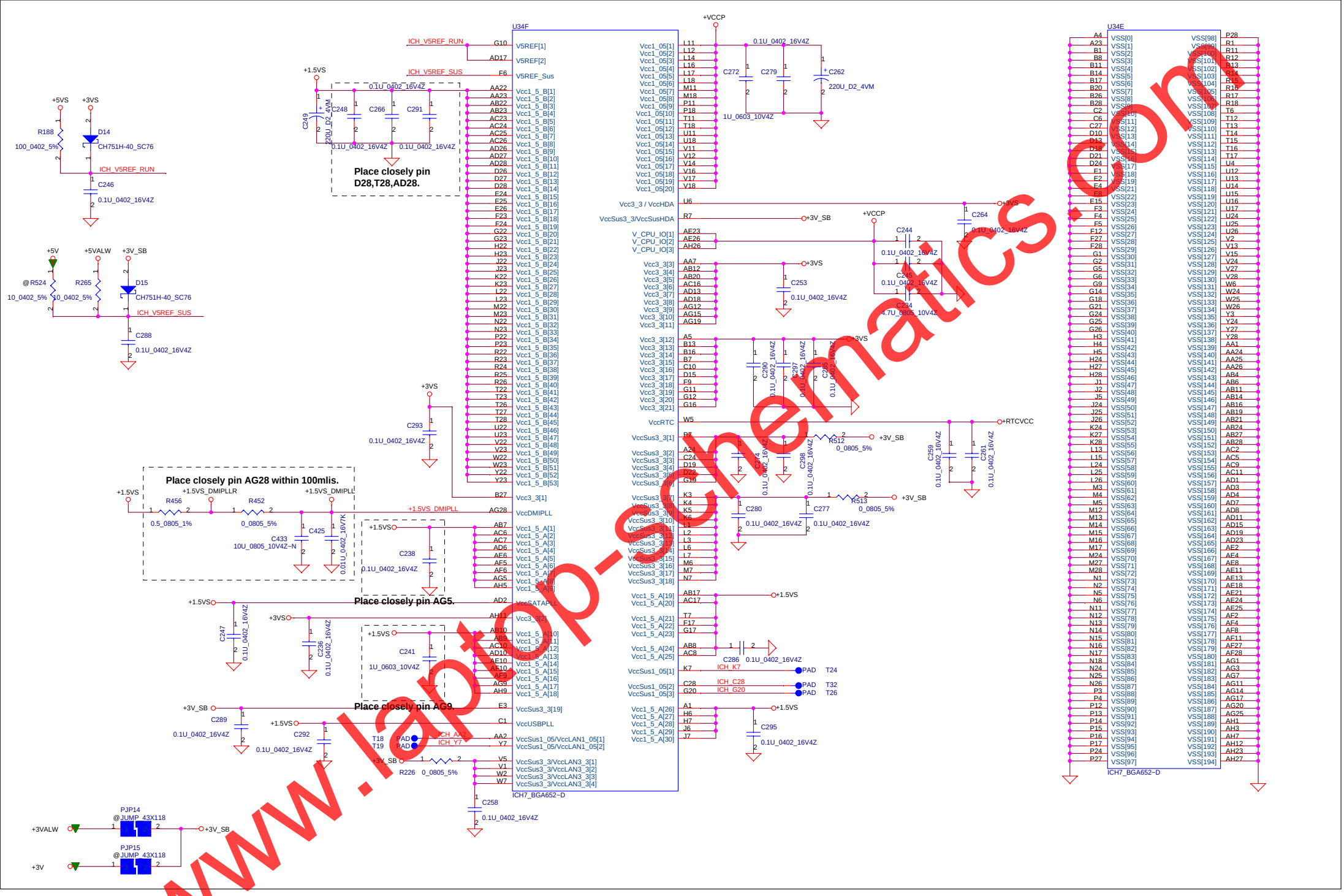
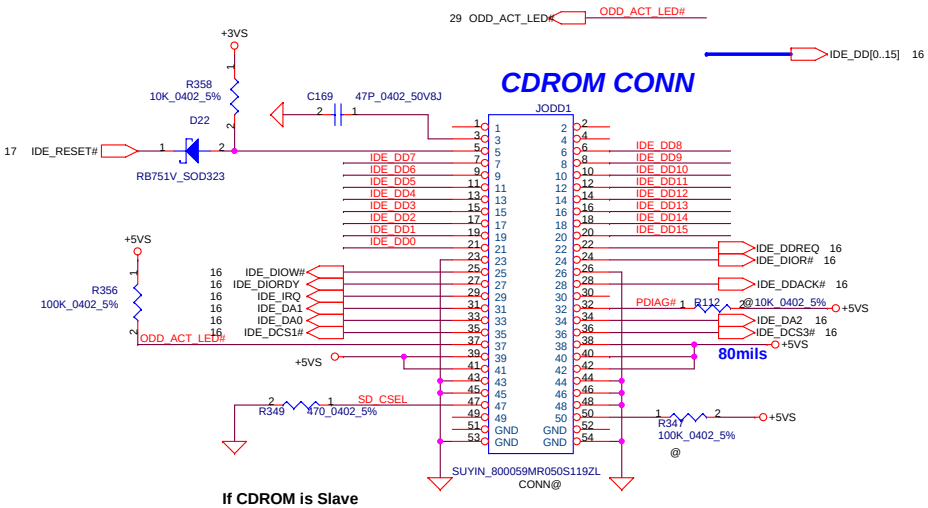
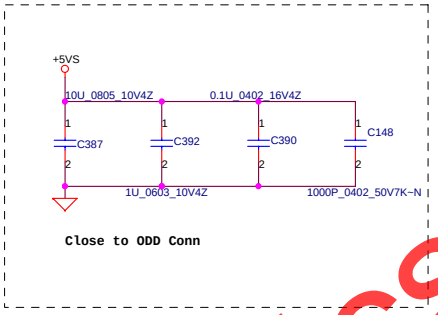
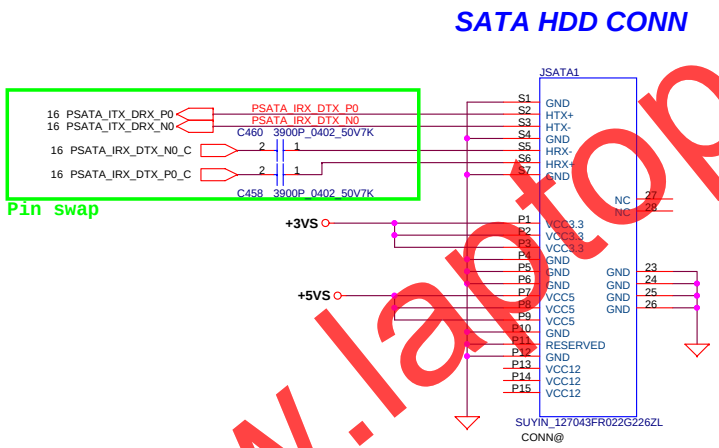
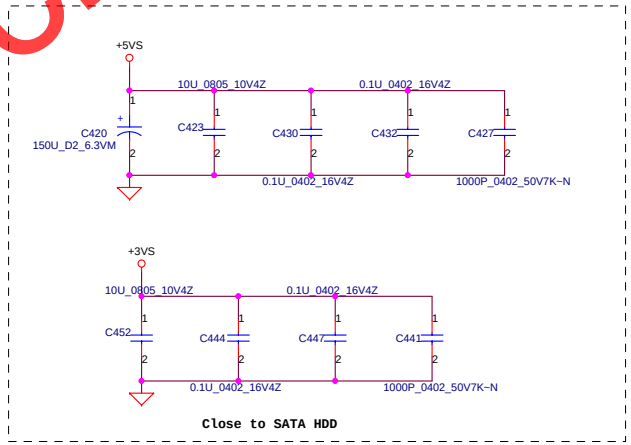
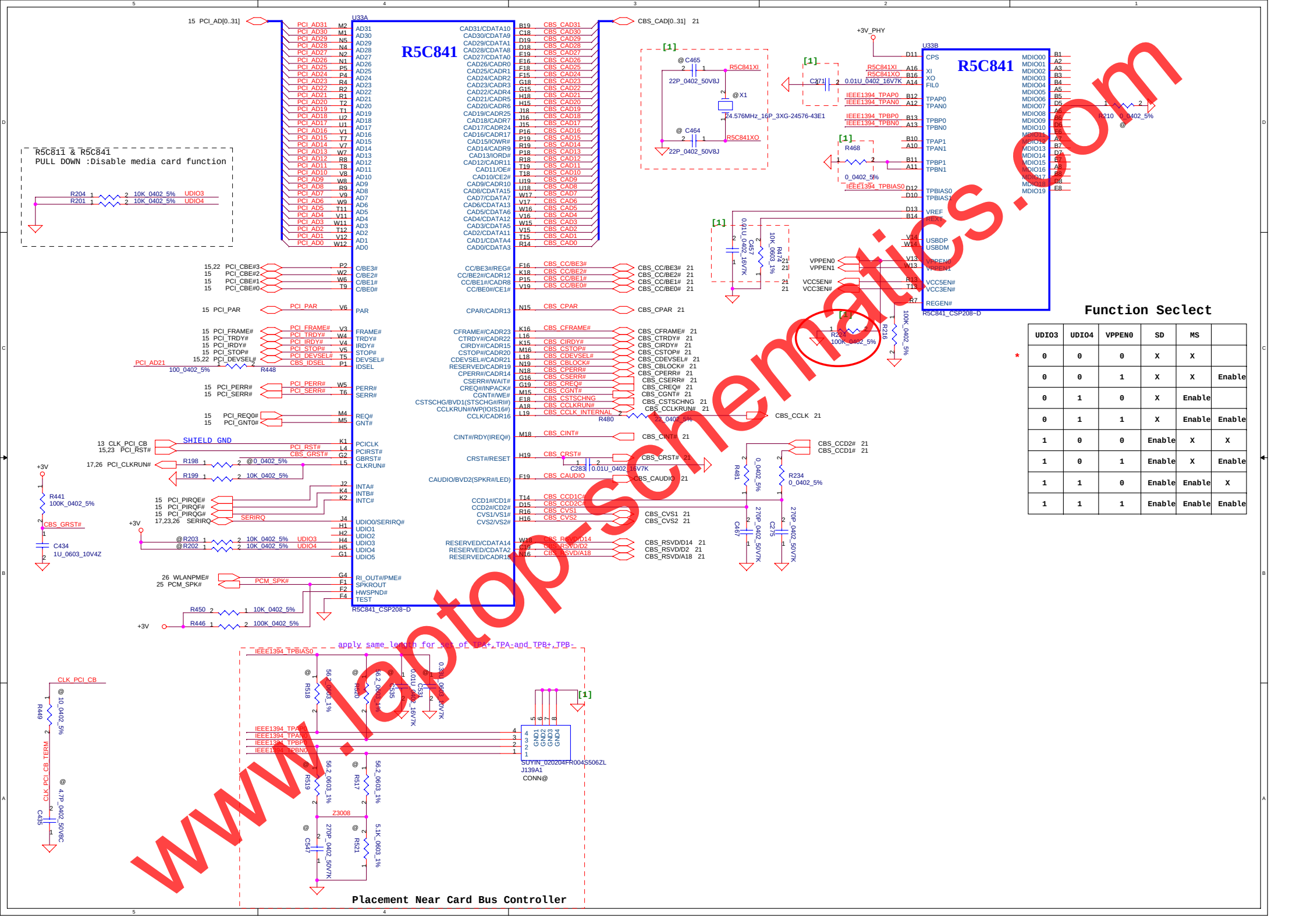


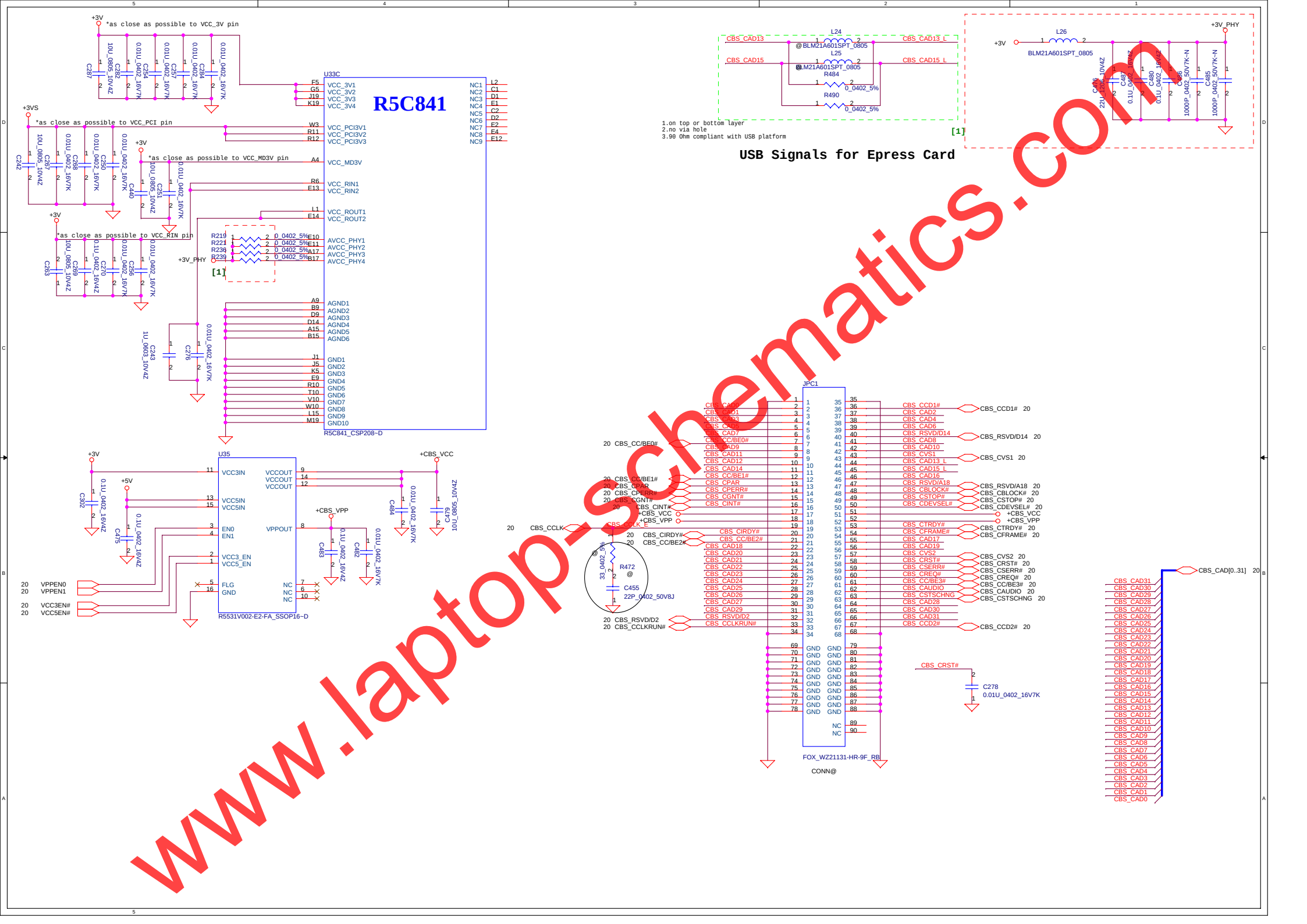


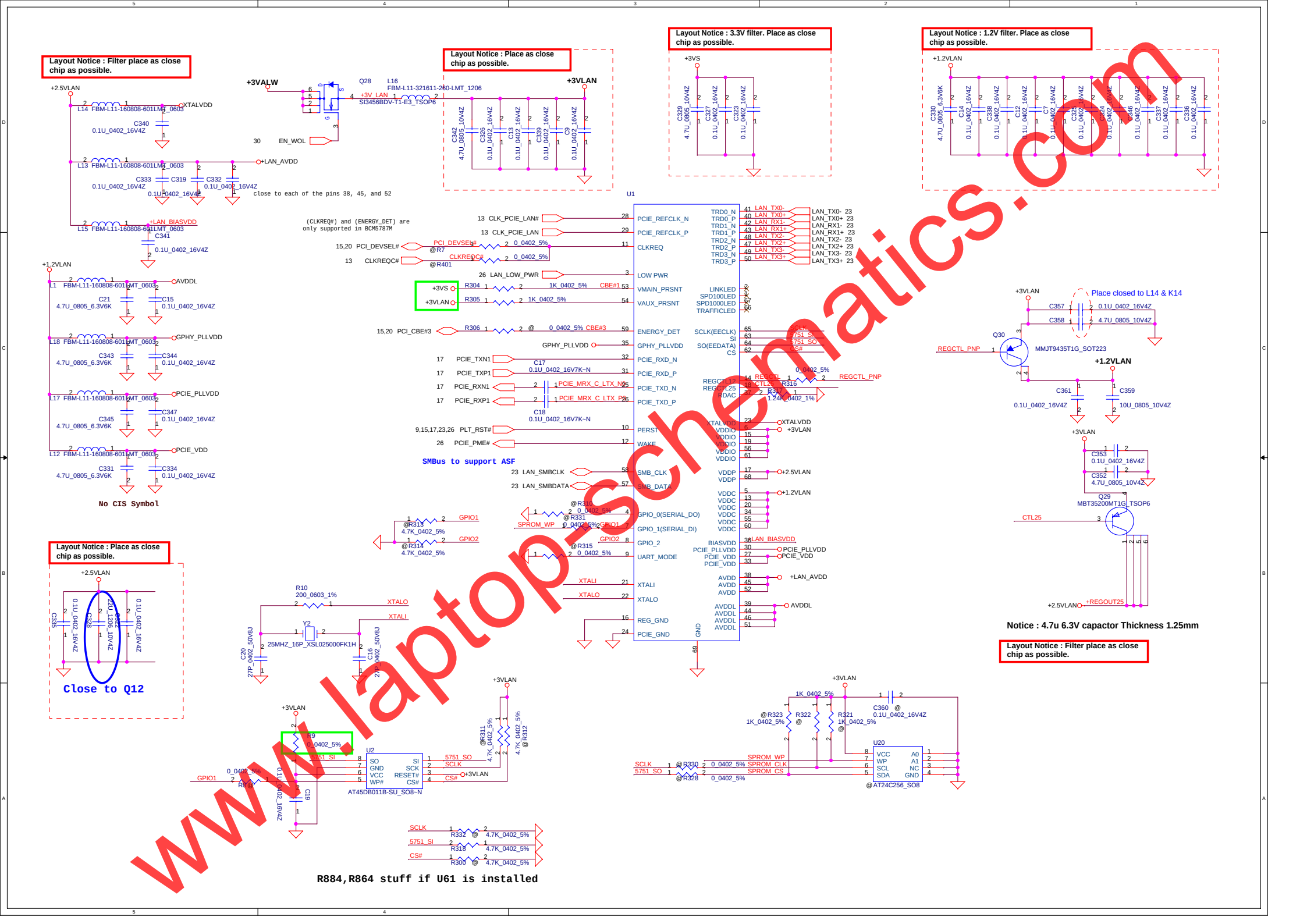







R5C841
R5C841
R5C841 & R5C841
PULL DOWN :Disable media card function
Function Seclect
UDIO3 UDIO2 VPPEN0 SD MS
0 0 0 X X
0 0 1 X X Enable
0 1 0 X Enable
0 1 1 X Enable Enable
1 0 0 Enable X X
1 0 1 Enable X Enable
1 1 0 Enable Enable X
1 1 1 Enable Enable Enable
Placement Near Card Bus Controller
apply same length for set of TPA+,TPA- and TPB+,TPB-
SHIELD GND
www.laptop-schematics.com




Layout Notice : Filter place as close chip as possible.
Layout Notice : Place as close chip as possible.
Layout Notice : 3.3V filter. Place as close chip as possible.
Layout Notice : 1.2V filter. Place as close chip as possible.
+2.5VLAN
+3VALW
+3VLAN
+3VS
+1.2VLAN
XTALVDD
+LAN_AVDD
+LAN_BIASVDD
AVDDL
GPHY_PLLVDD
PCIE_PLLVDD
PCIE_VDD
close to each of the pins 38, 45, and 52
No CIS Symbol
Close to Q12
U1
(CLKREQ#) and (ENERGY_DET) are only supported in BCM5787M
SMBus to support ASF
Place closed to L14 & K14
Notice : 4.7u 6.3V capactor Thickness 1.25mm
Layout Notice : Filter place as close chip as possible.
R884,R864 stuff if U61 is installed
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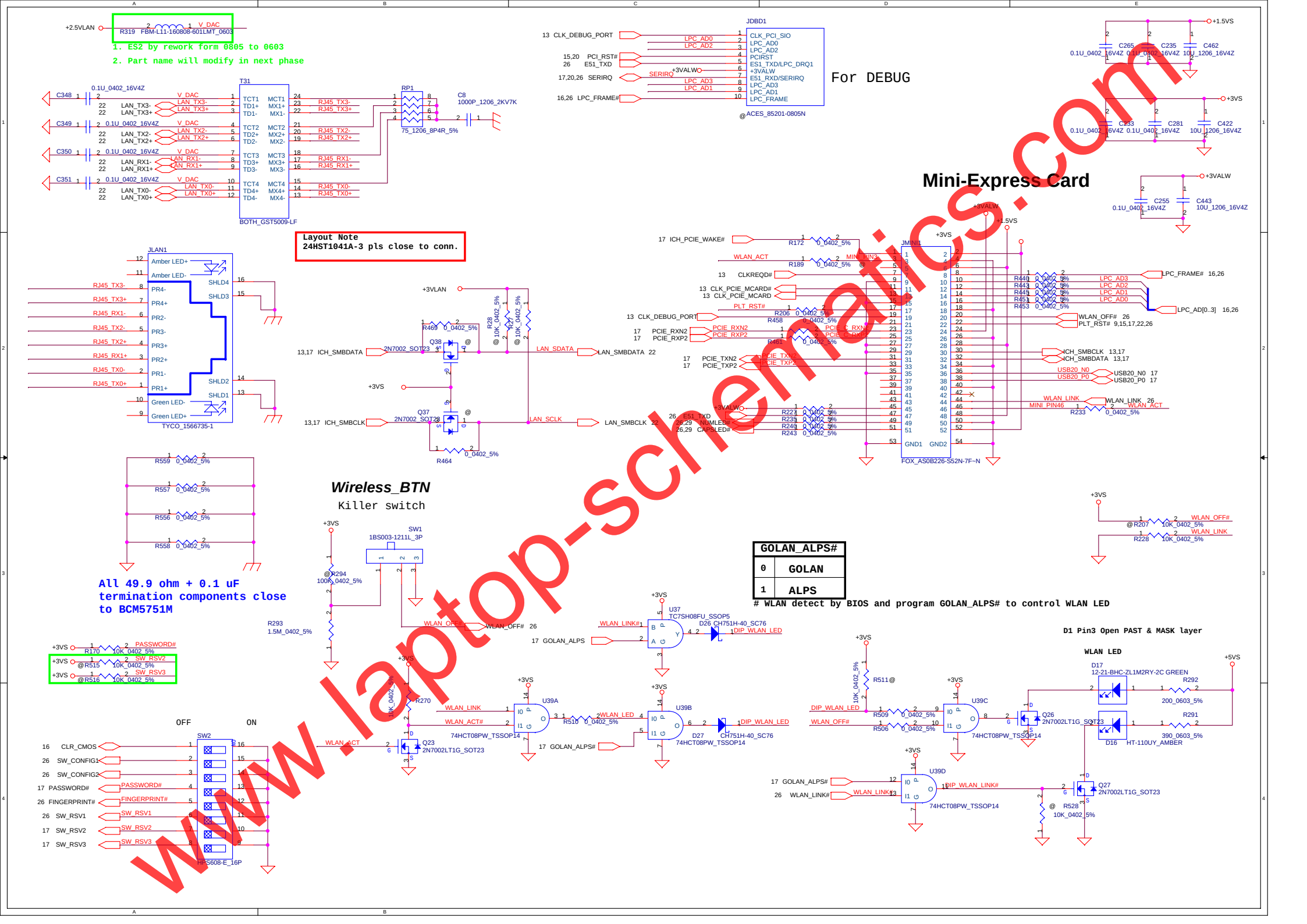
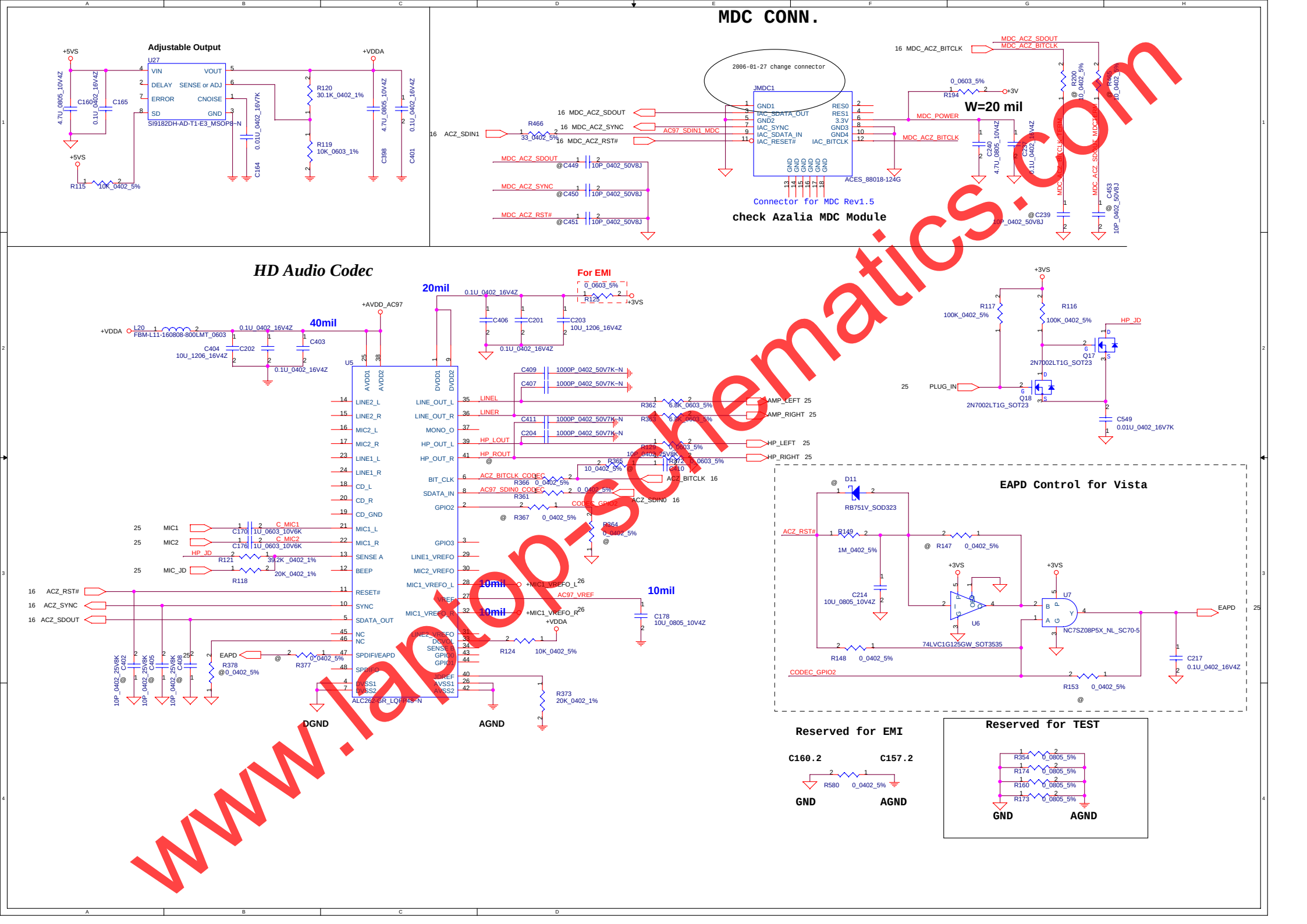
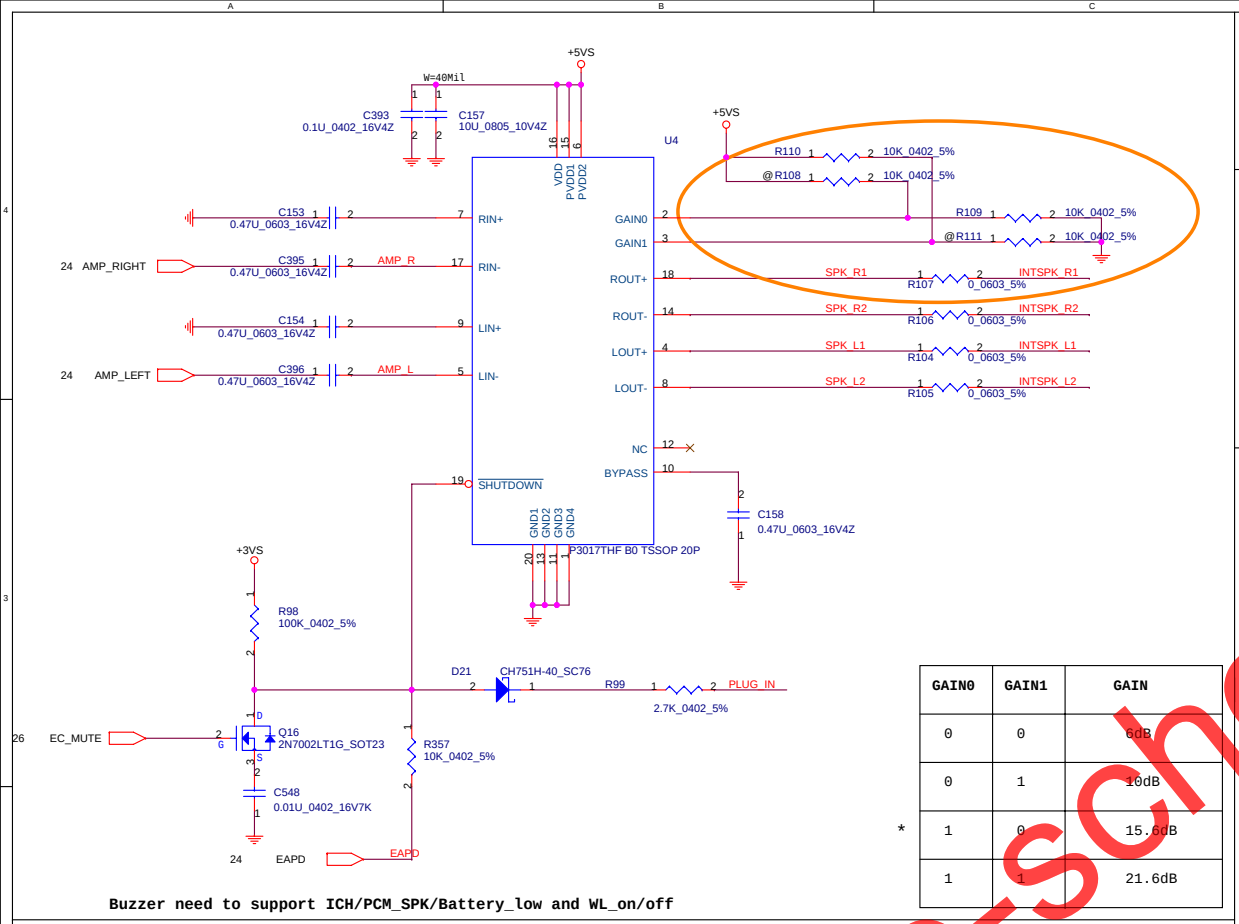
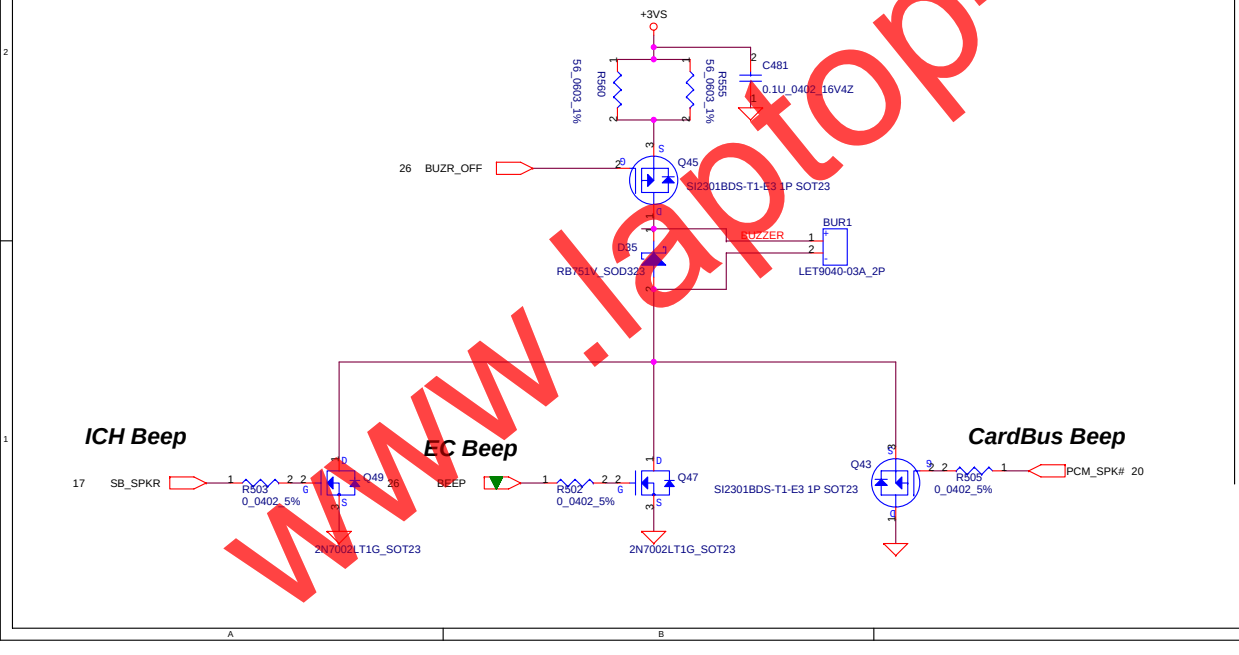

1. ES2 by rework form 0805 to 0603
2. Part name will modify in next phase
For DEBUG
Mini-Express Card
Layout Note
24HST1041A-3 pls close to conn.
Wireless_BTN
Killer switch
All 49.9 ohm + 0.1 uF termination components close to BCM5751M
GOLAN_ALPS#
0 GOLAN
1 ALPS
WLAN detect by BIOS and program GOLAN_ALPS# to control WLAN LED
D1 Pin3 Open PAST & MASK layer
WLAN LED
www.laptop-schematics.com


MDC CONN.
Adjustable Output
U27
SI9182DH-AD-T1-E3_MSOP8-N
2006-01-27 change connector
JMDC1
ACES_88018-124G
Connector for MDC Rev1.5
check Azalia MDC Module
W=20 mil
HD Audio Codec
ALC262_SR_LQFP48-N
For EMI
20mil
40mil
10mil
EAPD Control for Vista
Reserved for EMI
Reserved for TEST
DGND
AGND
GND
www.laptop-schematics.com

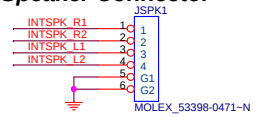


GAIN0	GAIN1	GAIN
0	0	6dB
0	1	10dB
* 1	0	15.6dB
1	1	21.6dB

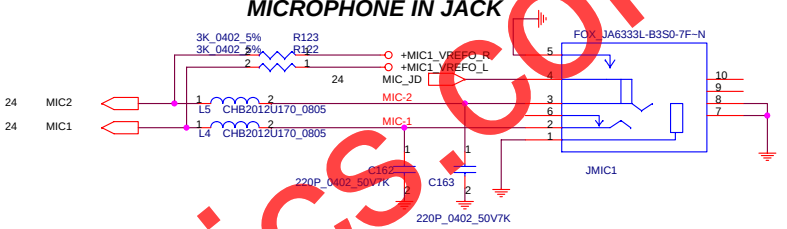
Buzzer need to support ICH/PCM_SPK/Battery_low and WL_on/off



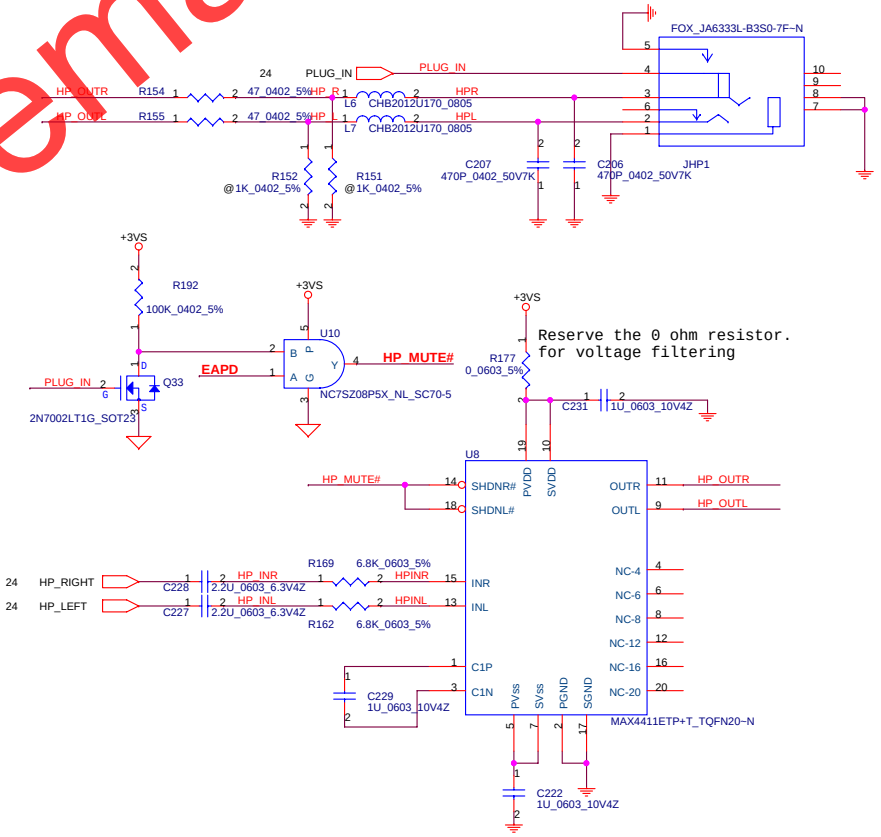
Speaker Connector

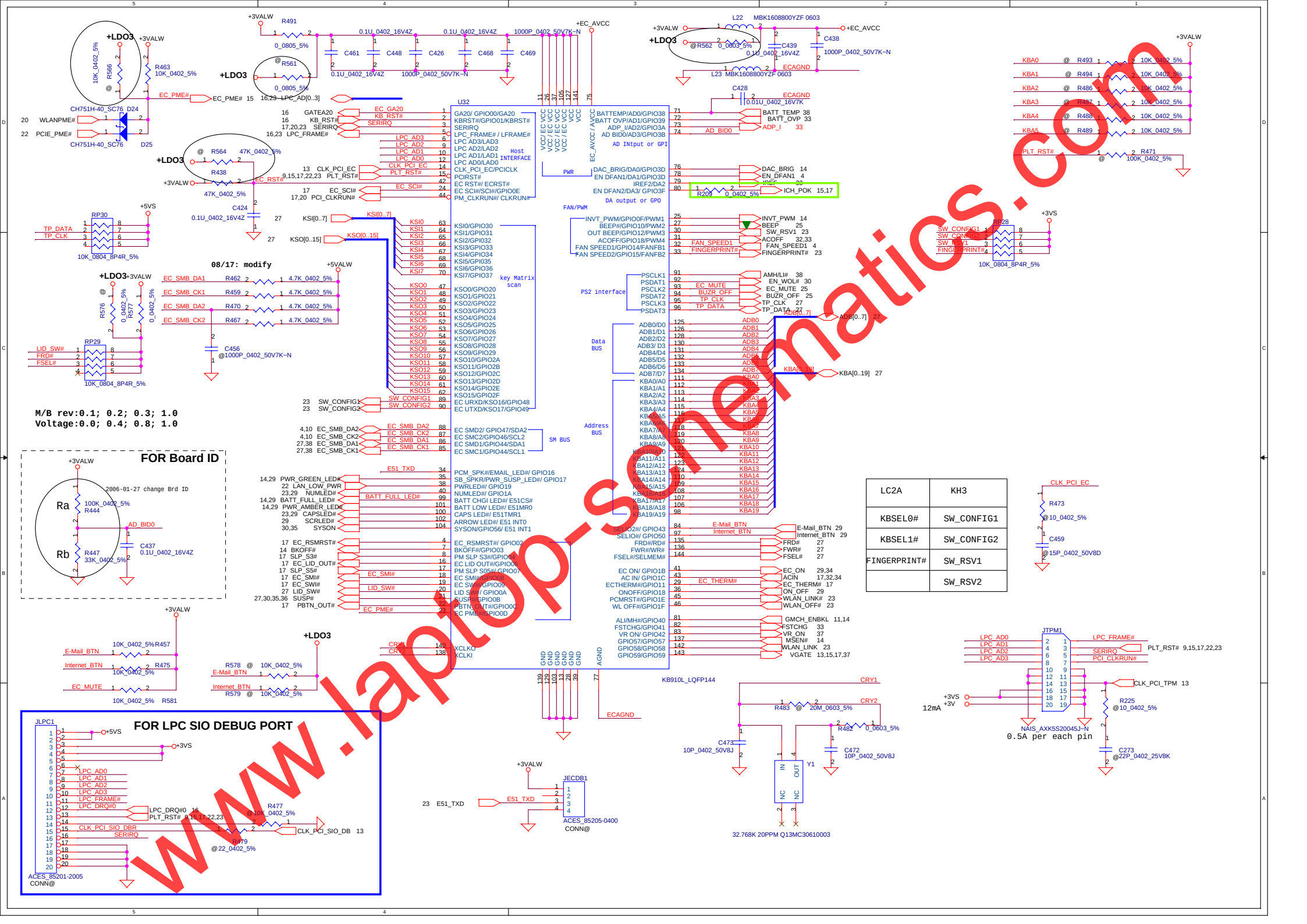


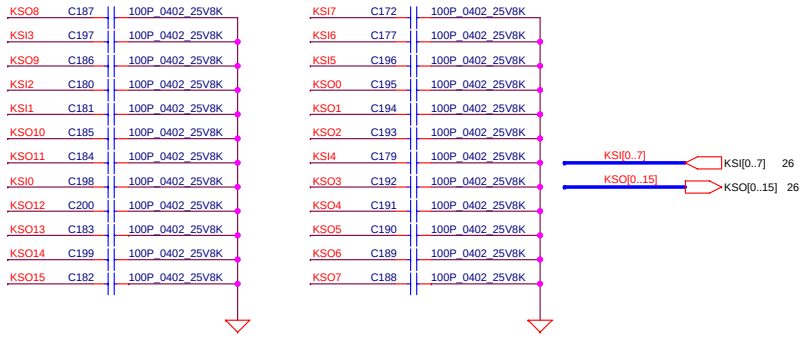
MICROPHONE IN JACK



HEADPHONE OUT JACK



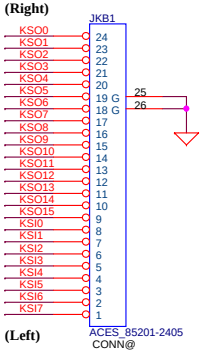




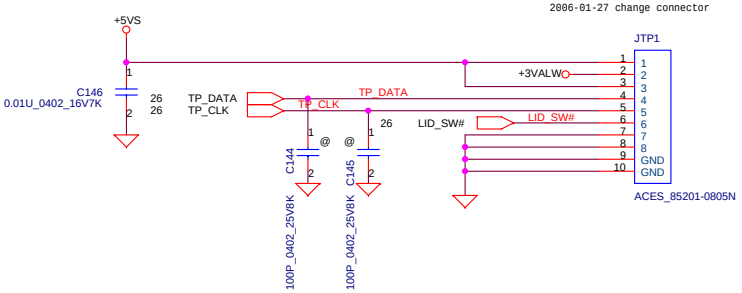
INT_KBD CONN.

TO M/B

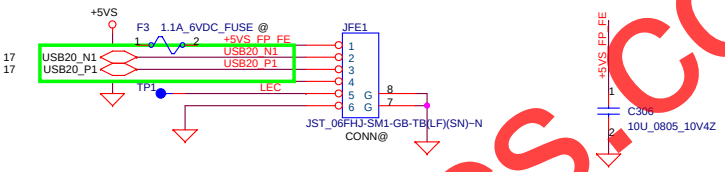
(Right)



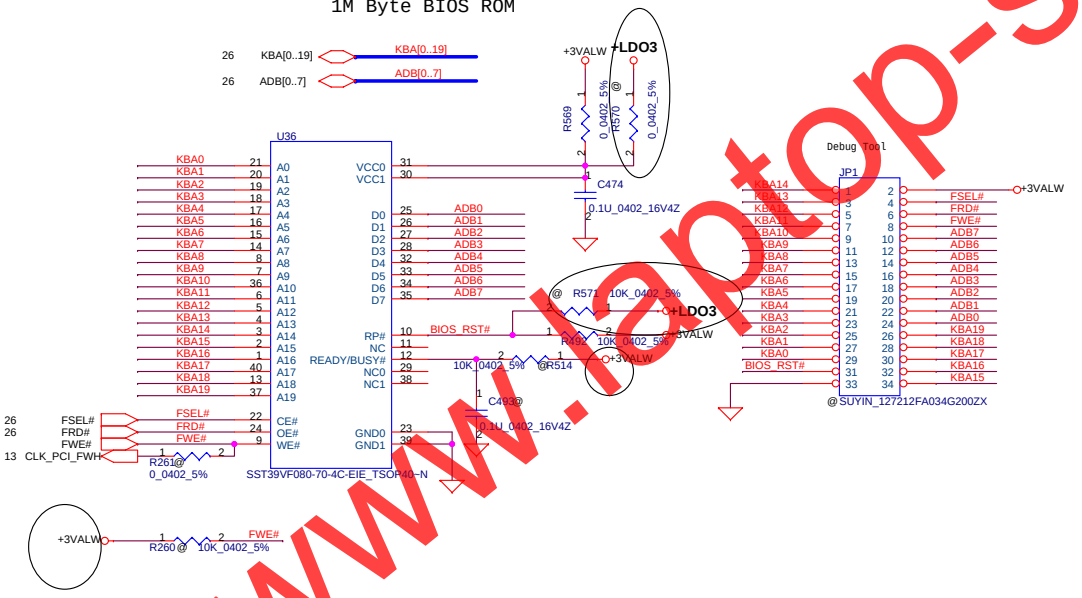
(Left)

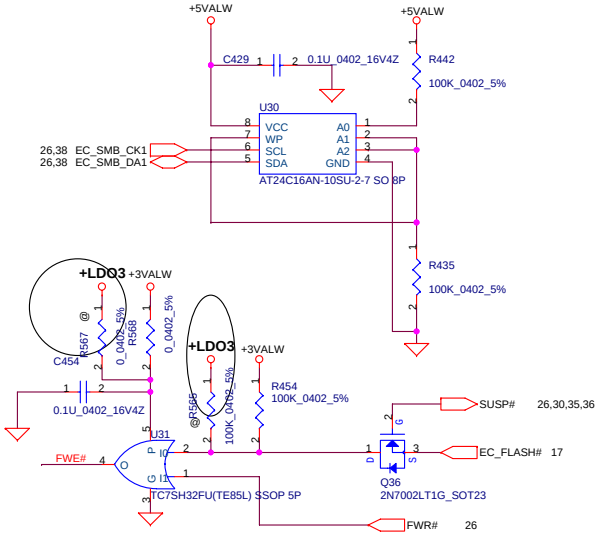


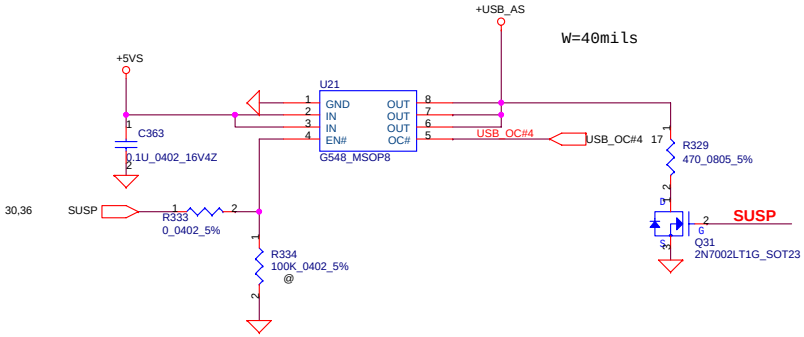
Felica Conn

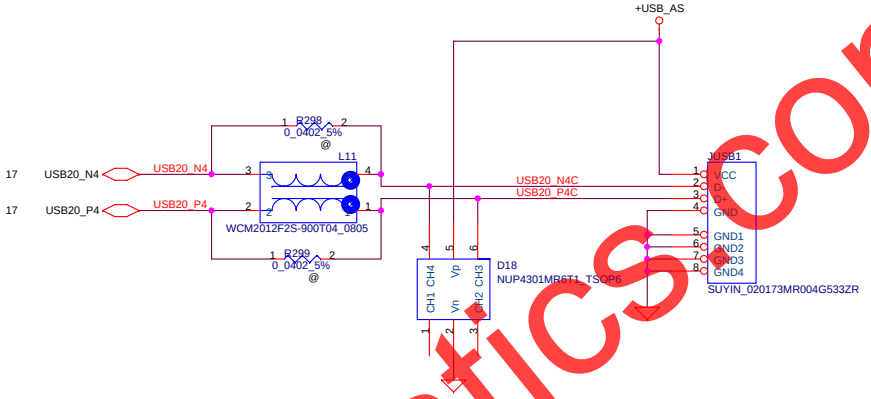


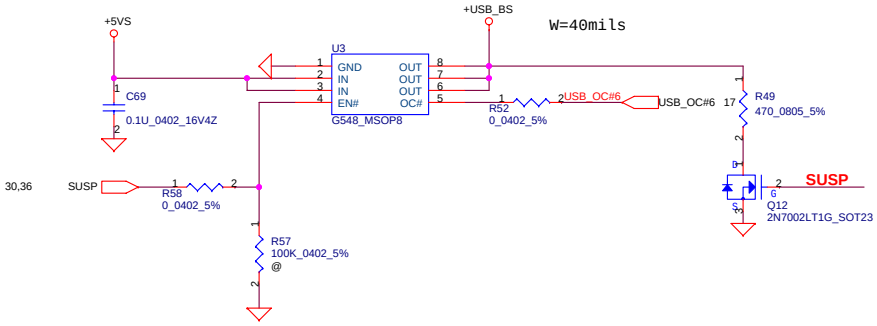
1M Byte BIOS ROM

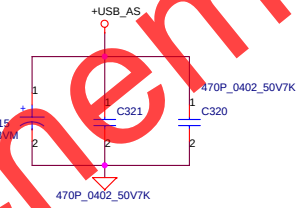


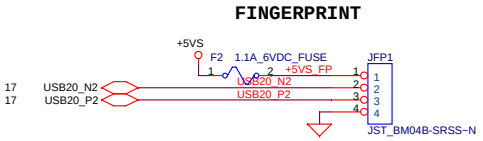


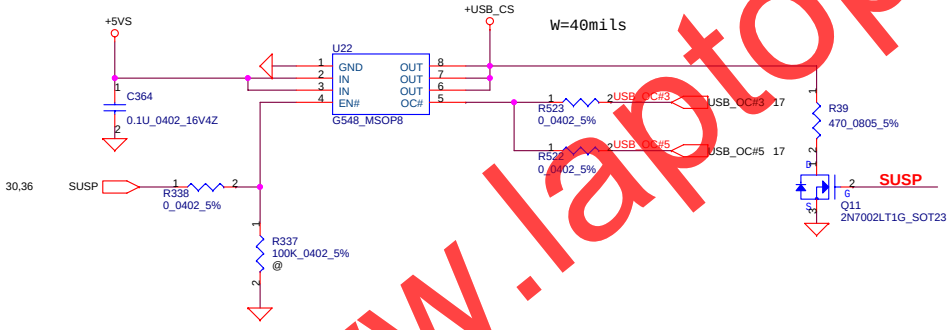


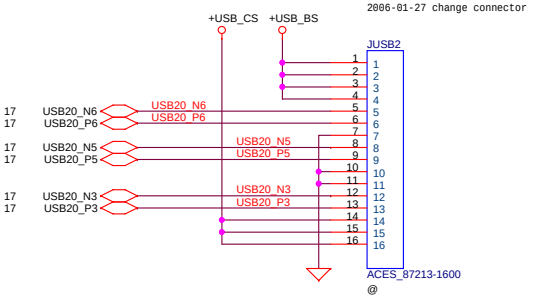


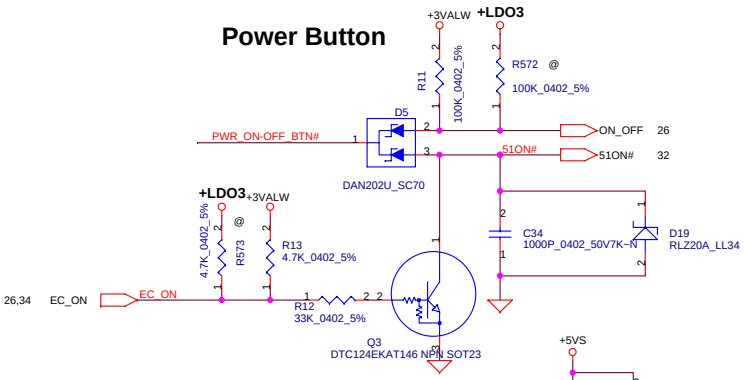




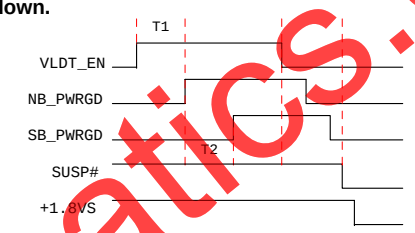


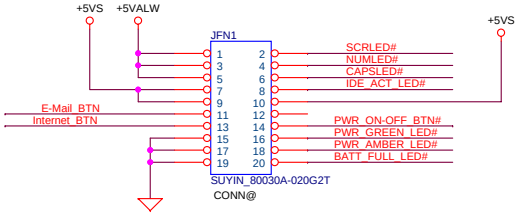


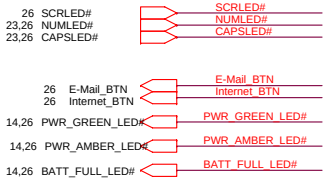


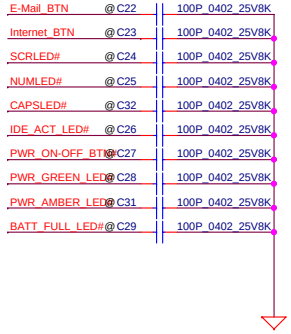


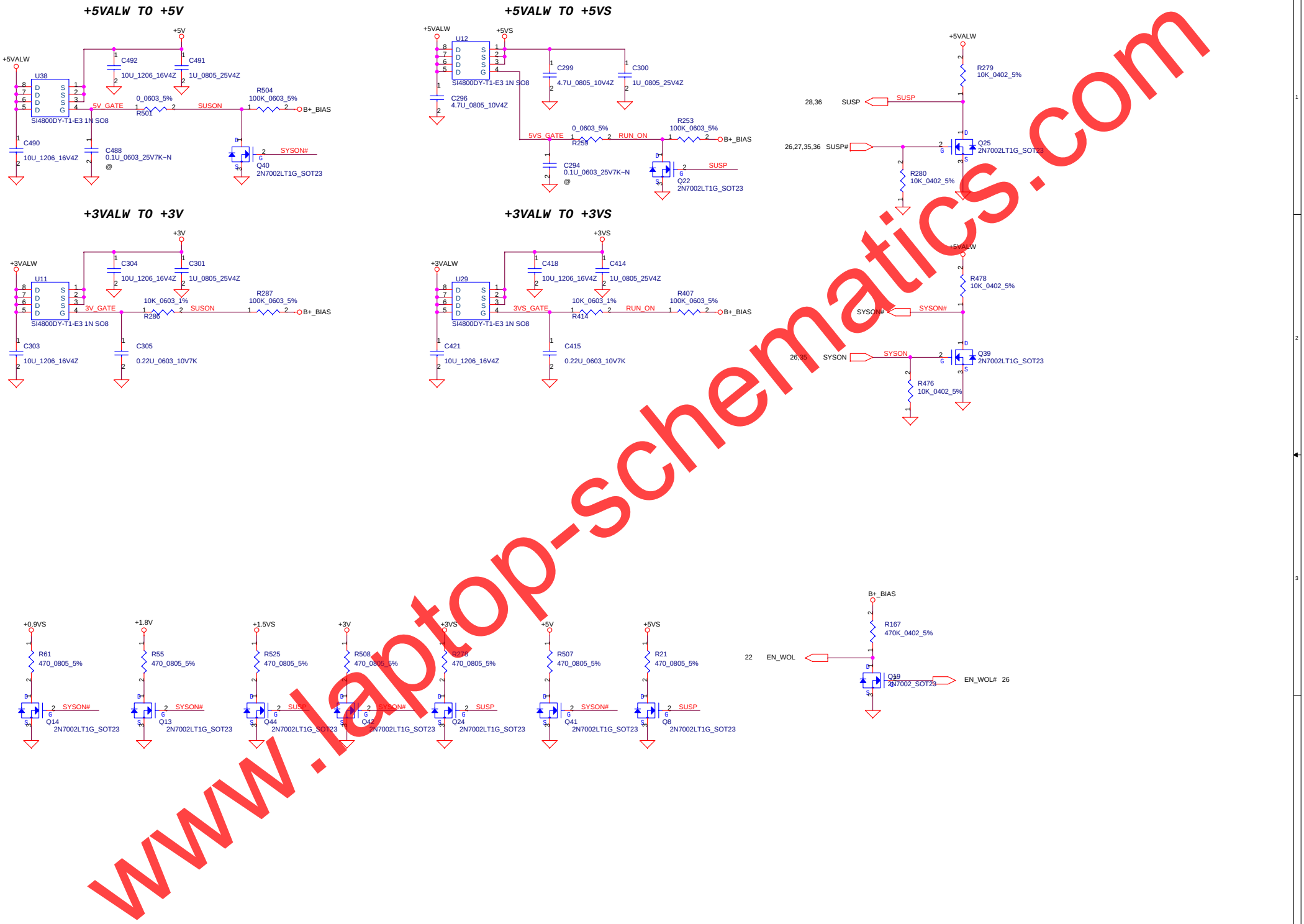
note:T1 minimum 15ms,T2 minimum 33ms/maximum 500ms, SUSP# goes to low after SB_PWRGD goes to low for power down.

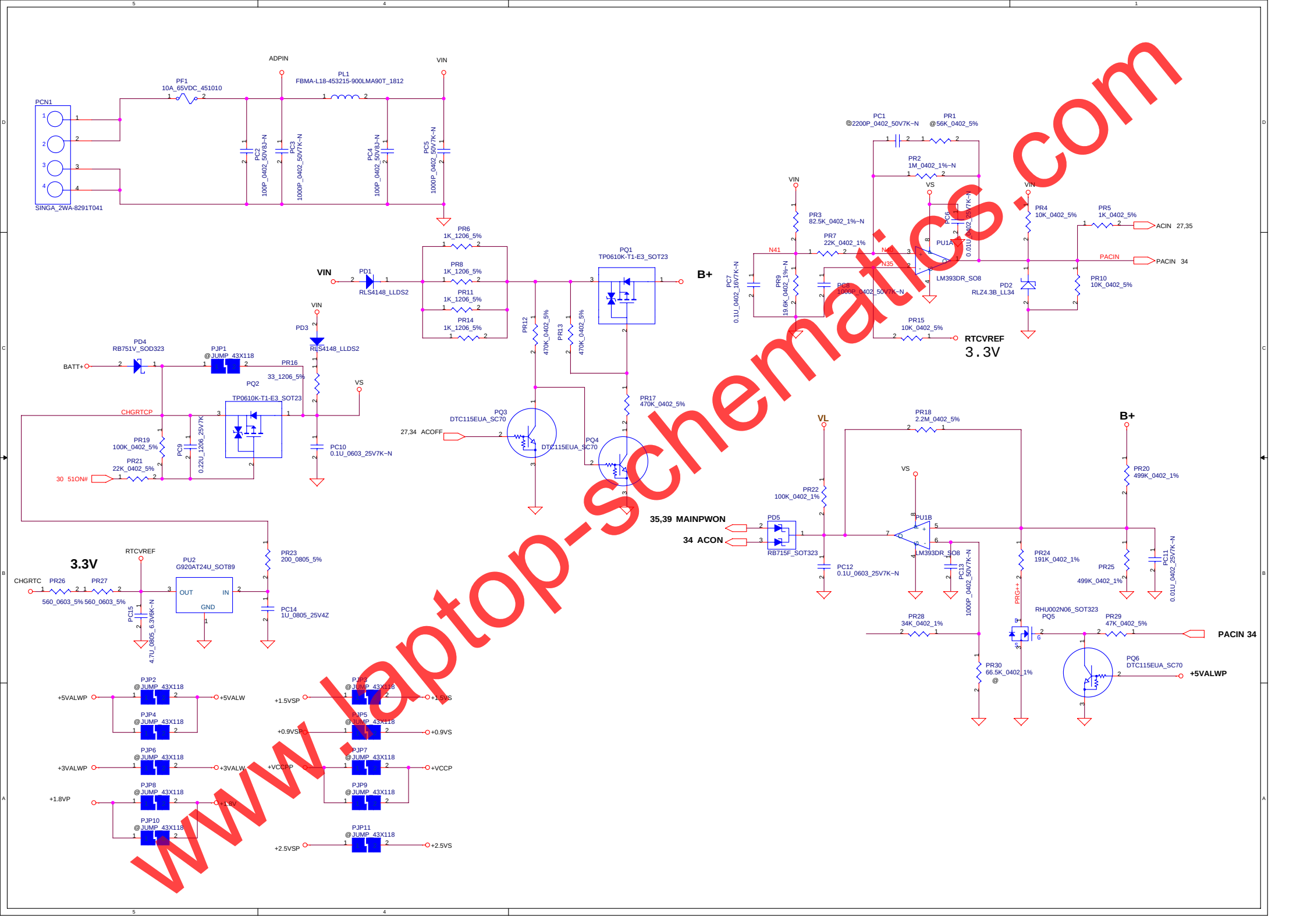


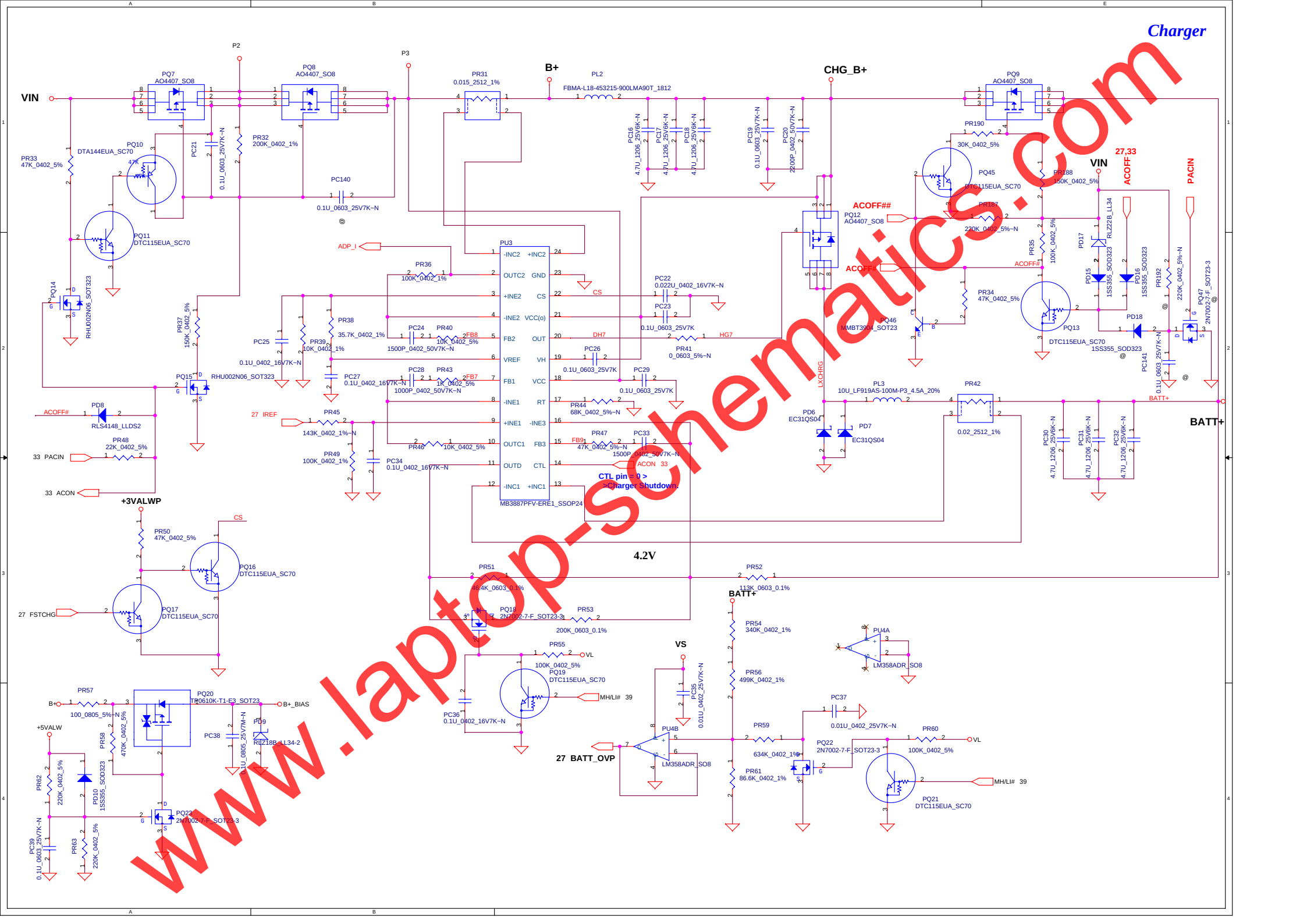




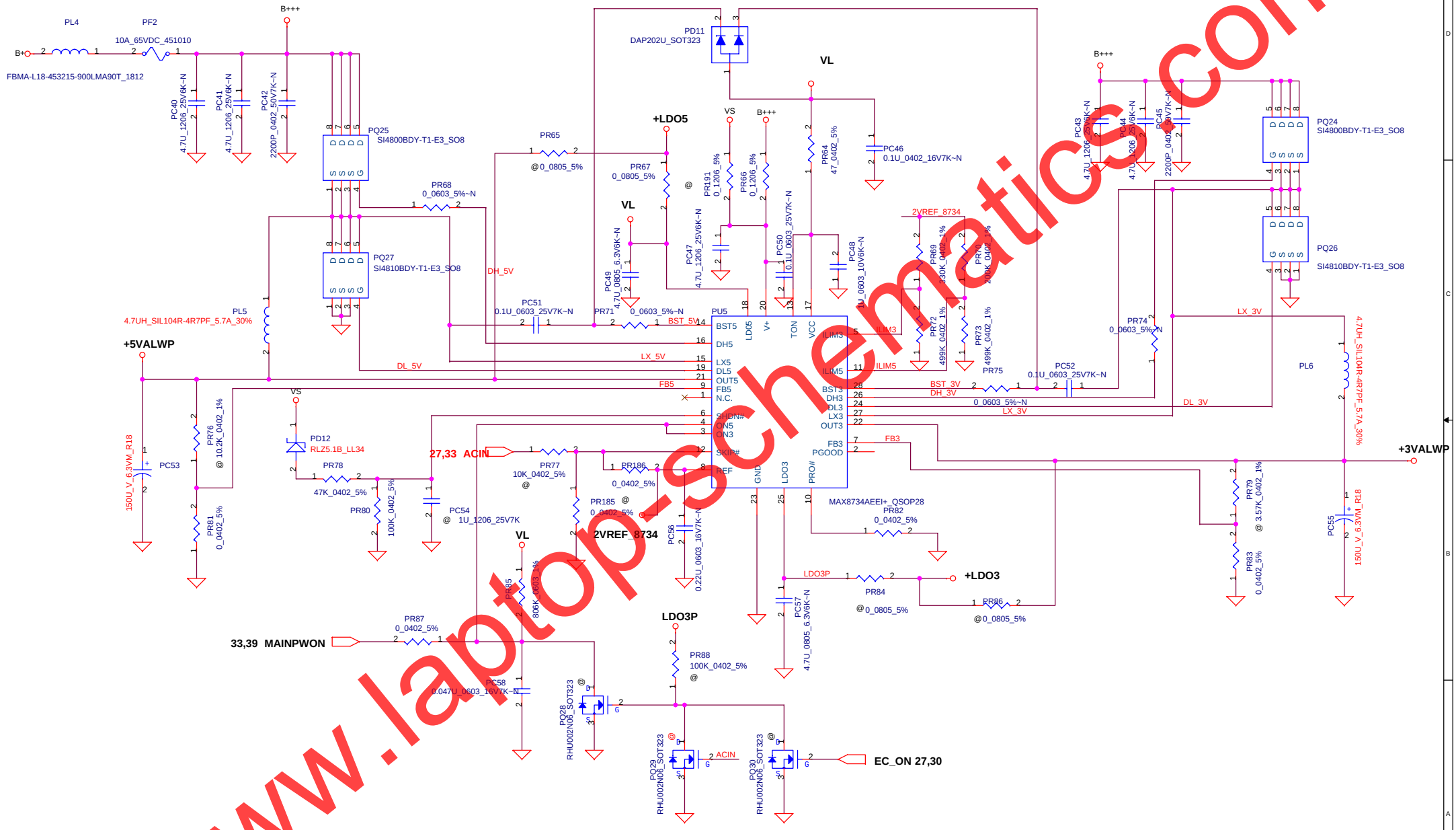


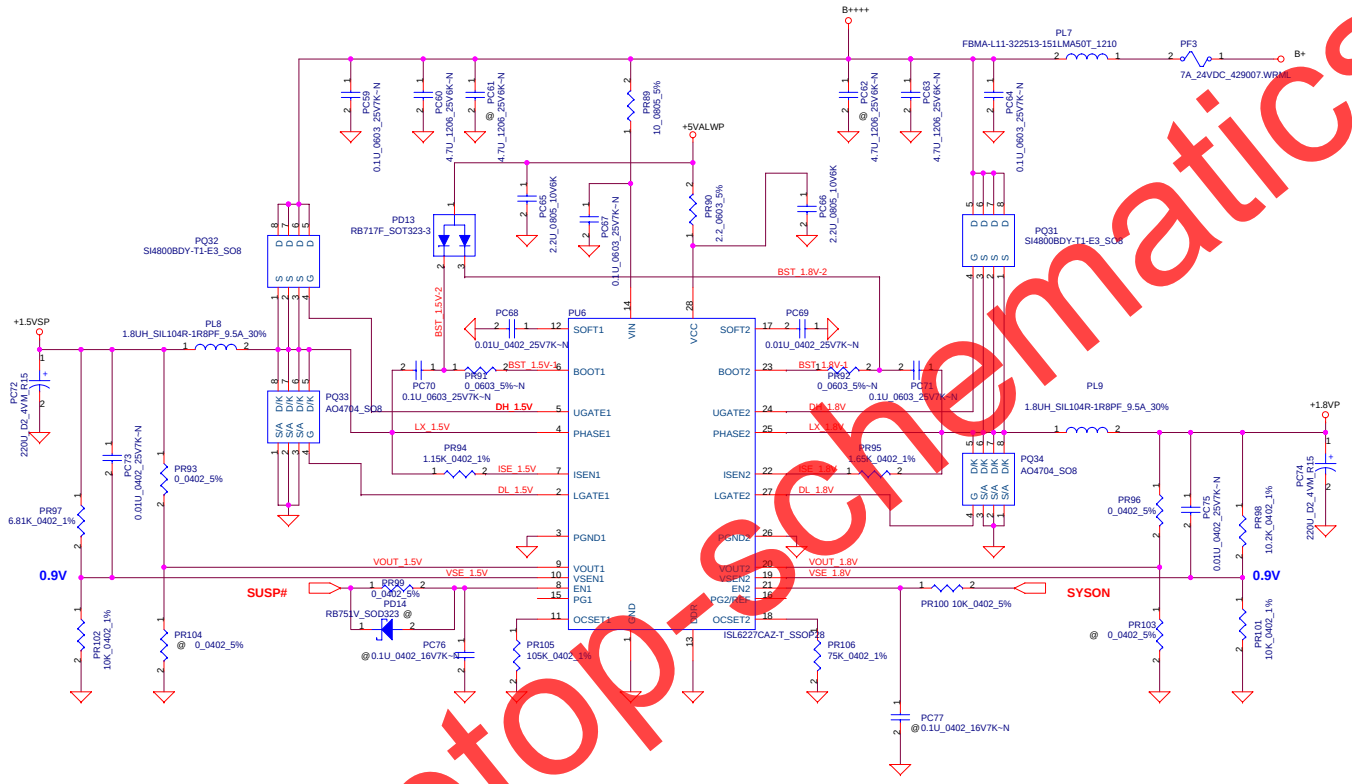


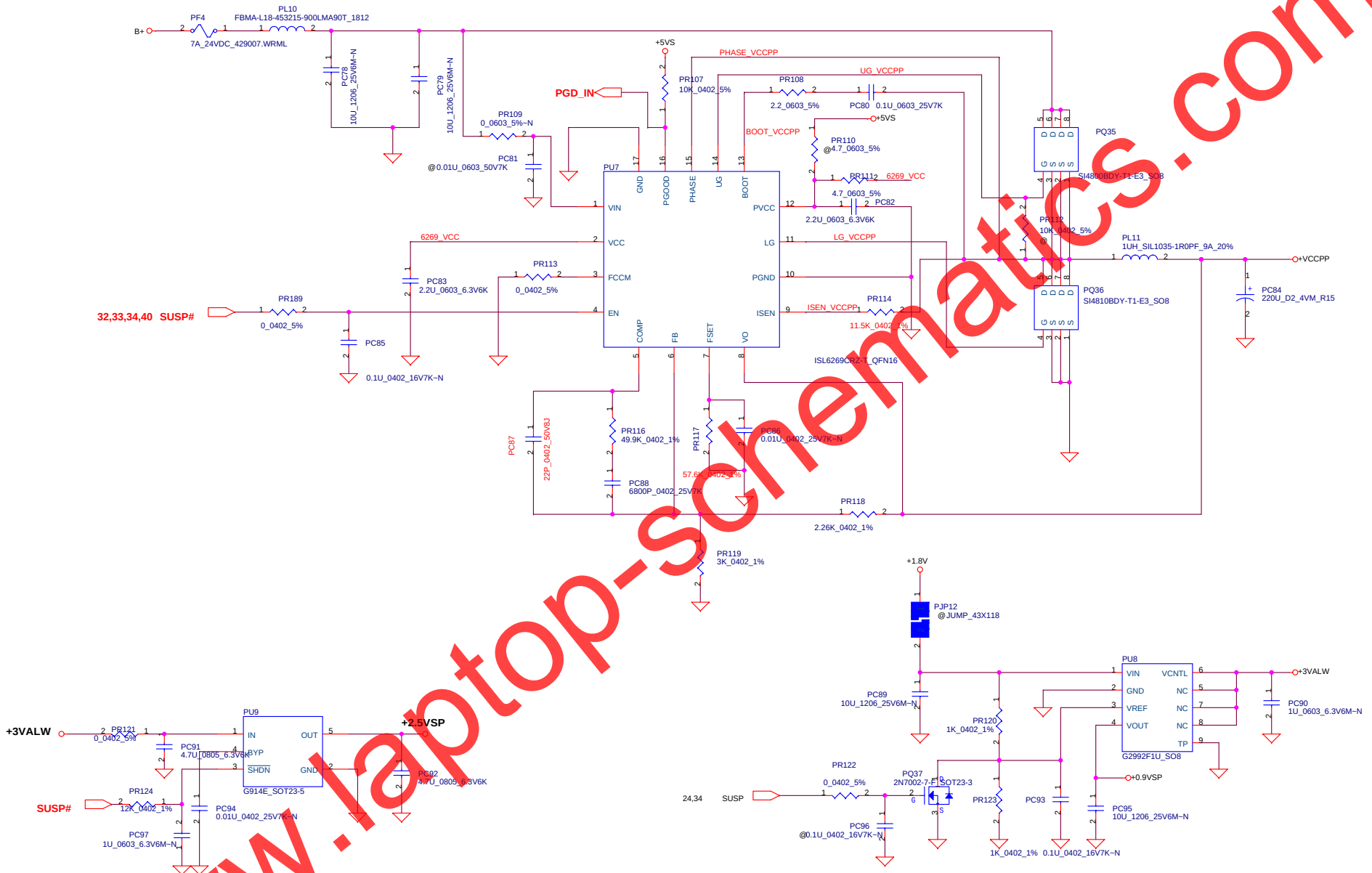


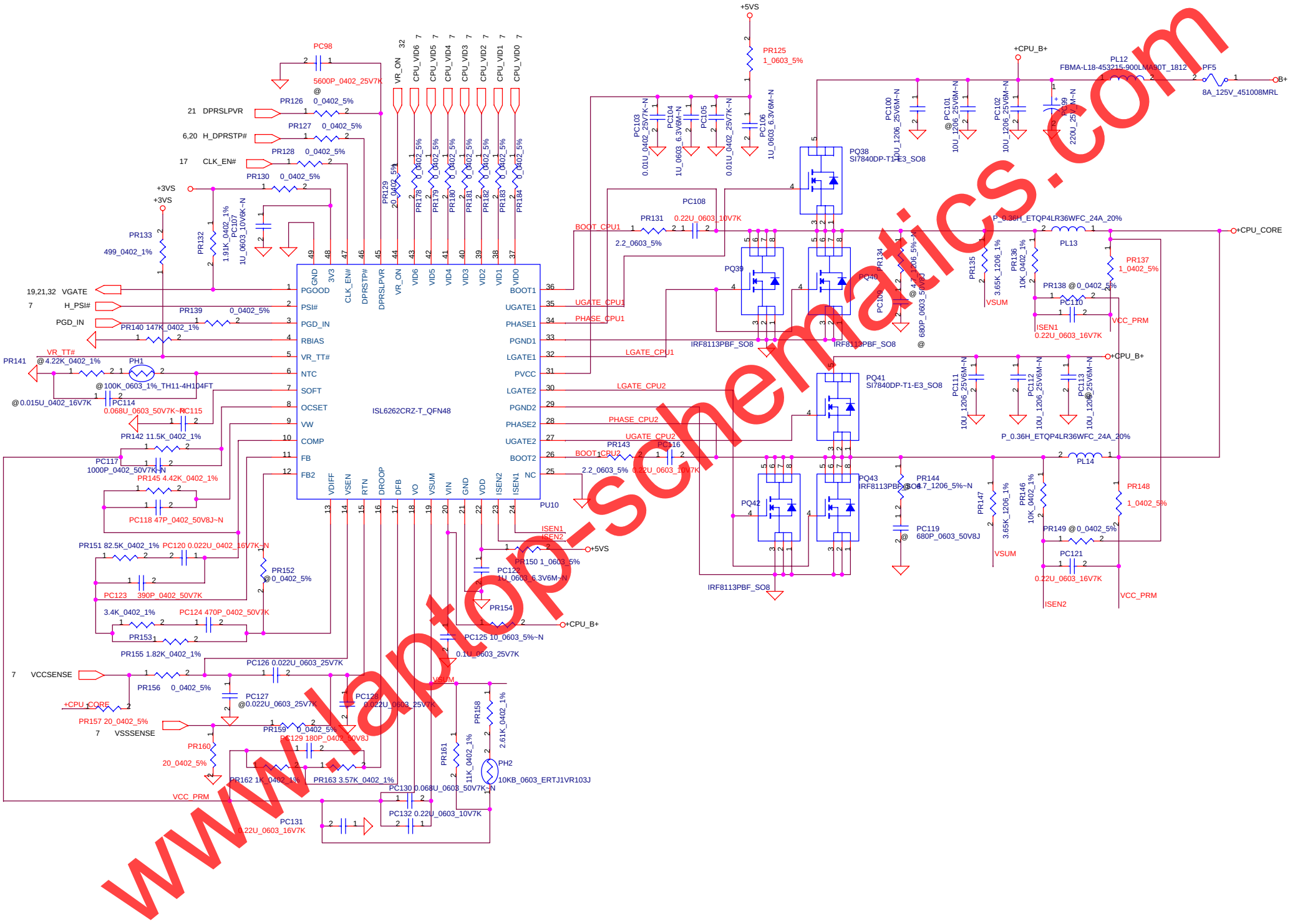


+3.3VALWP/+5VALWP









Battery Connect/OTP