

Compal confidential

Schematics Document Mobile Penryn uFCPGA with Intel Cantiga_PM+ICH9-M core logic

2008-02-25



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Size	Document Number	Rev		
Custom	LA-4102P Blade discrete	0.4		
Date	Monday, February 25, 2008	Sheet	1	of 53

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Voltage Rails

O MEANS ON

X MEANS OFF

power plane State	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE +2.5VS +1.8VS +NVVDD +PCIE
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :

 : means Digital Ground

 : means Analog Ground

@ : means just reserve , no build
DEBUG@ : means just reserve for debug.

USB assignment:

USB-0 Right side
USB-1 Right side
USB-2 Left side(with ESATA)
USB-3 Dock
USB-4 Camera
USB-5 WLAN
USB-6 Bluetooth
USB-7 Finger Printer
USB-8 MiniCard(WWAN/TV)
USB-9 Express card
USB-10 X
USB-11 X

PCIe assignment:

PCIe-1 TV tuner(WWAN/Robeson)
PCIe-2 X
PCIe-3 WLAN
PCIe-4 GLAN (Marvell)
PCIe-5 Card reader
PCIe-6 New Card

SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	Thermal Sensor	SODIMM	CLK CHIP	MINI CARD	Sensor board	NB9M Thermal Sensor	NB9M	G-sensor
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	V	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X	V	V	X
ICH_SMBCLK ICH_SMBDATA	ICH9	X	X	X	X	V	V	V	X	X	X	V

NB9M SMBUS Control Table

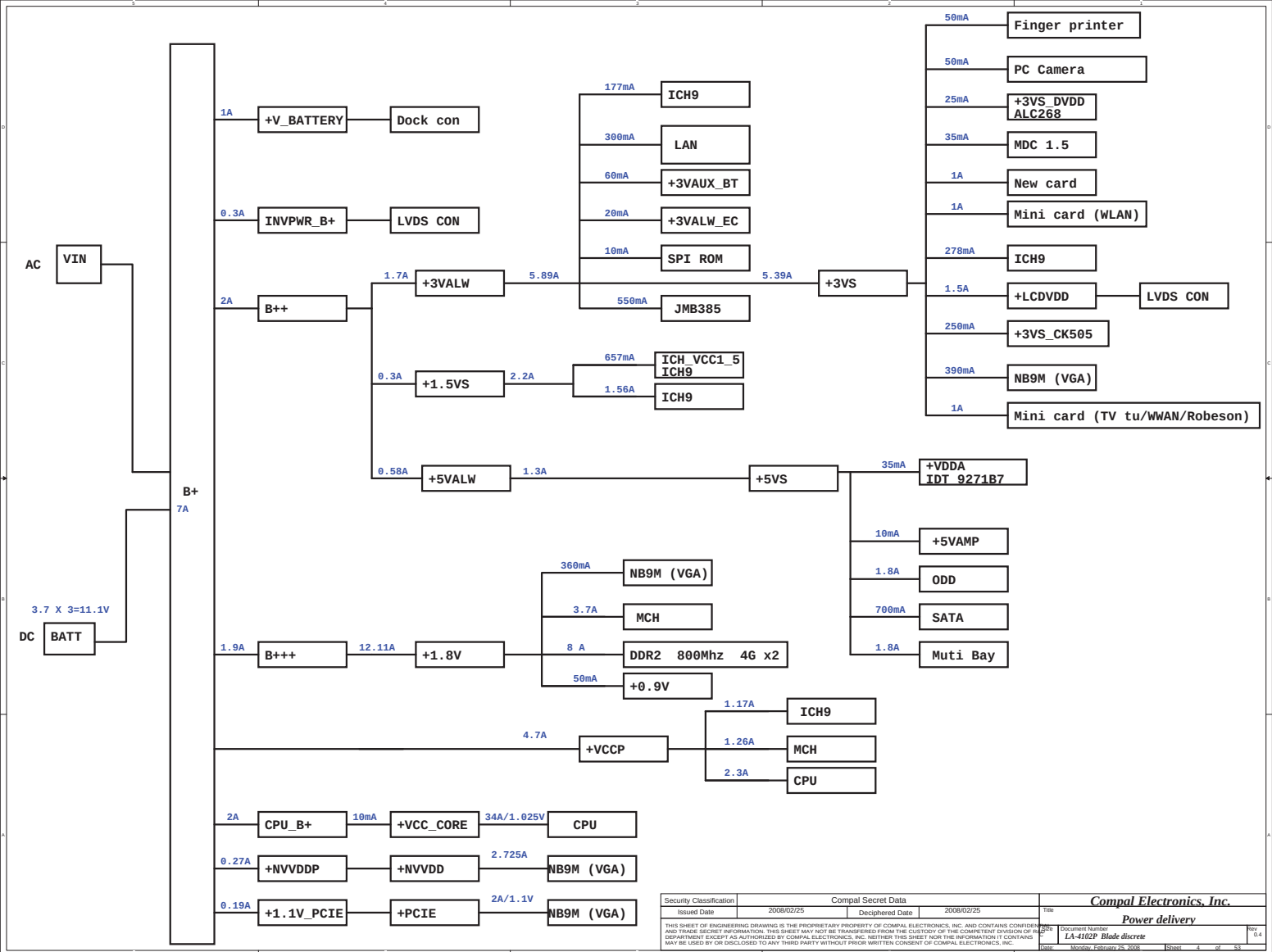
	SOURCE	LVDS	CRT	HDMI
DDC2_DATA DDC2_CLK	NB9M	V	X	X
3VDDCDA 3VDDCCL	NB9M	X	V	X
HDMIDAT_VGA HDMICLK_VGA	NB9M	X	X	V

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

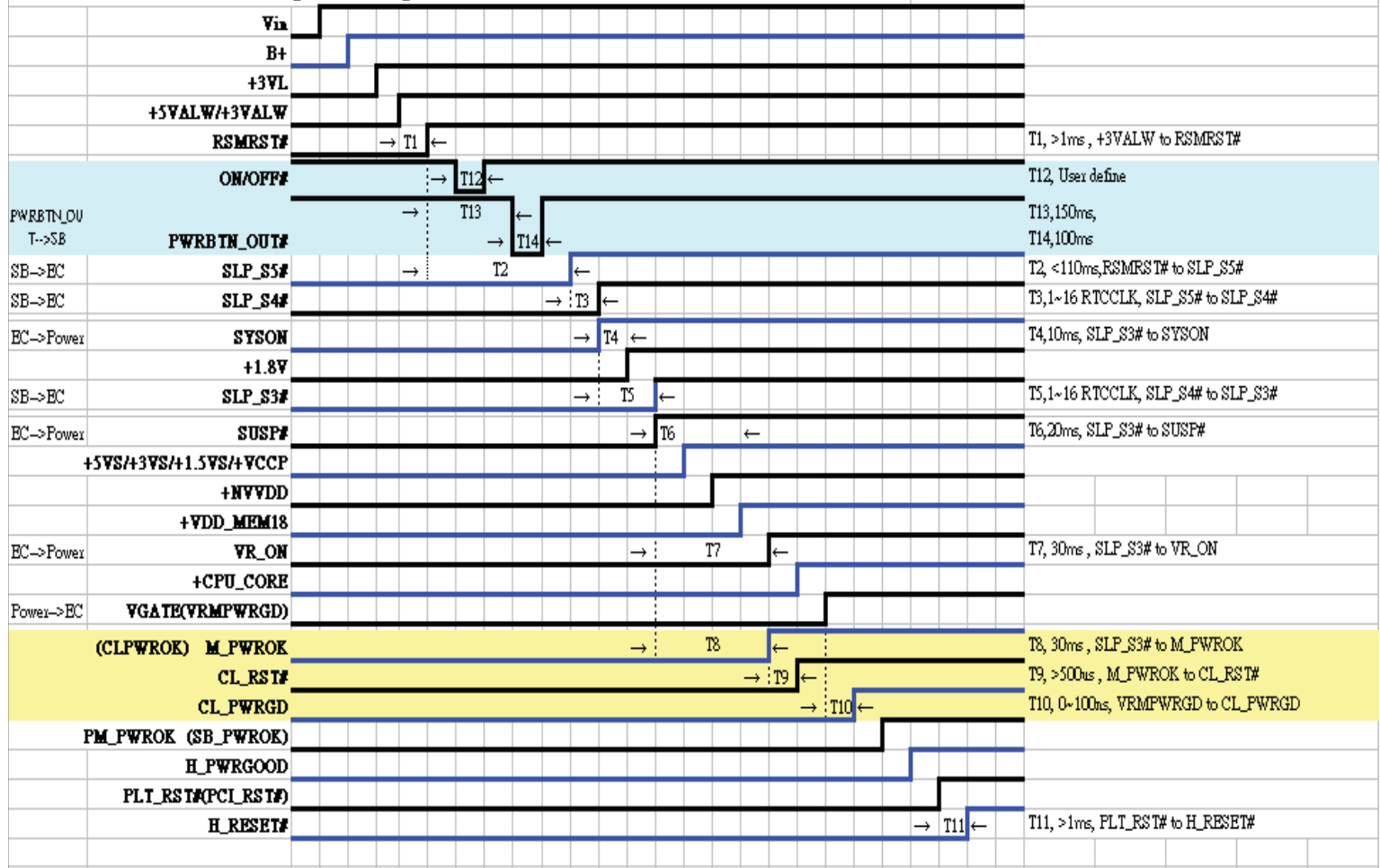
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				Custom	LA-4102P Blade discrete	0.4
				Date	Monday, February 25, 2008	Sheet 3 of 53

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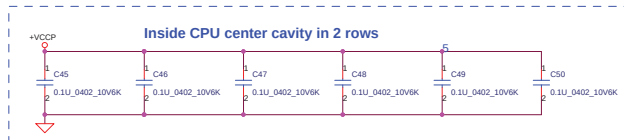
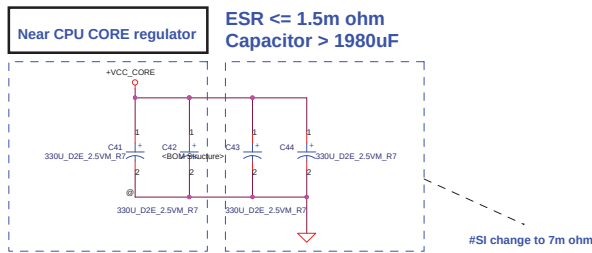
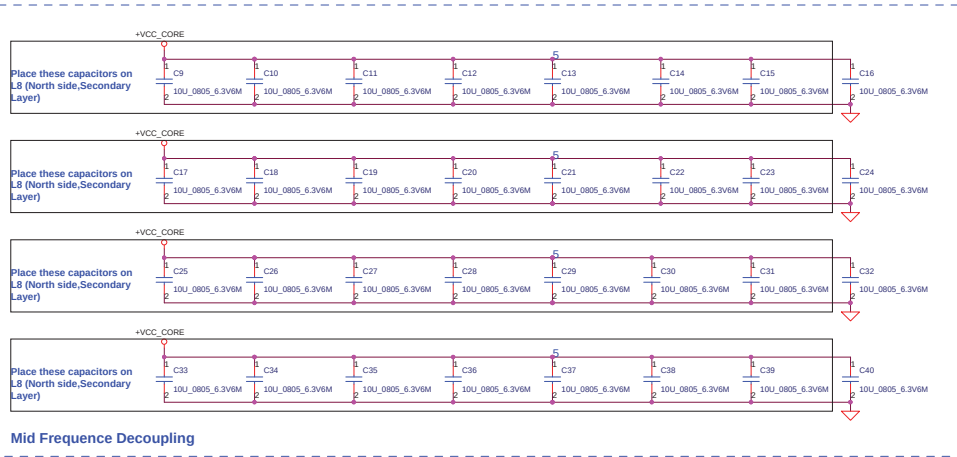
JAL50 Discrete power sequence AC mode



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				Document Number	LA-4102P Blade discrete
				Date	Monday, February 25, 2008
				Sheet	5 of 53

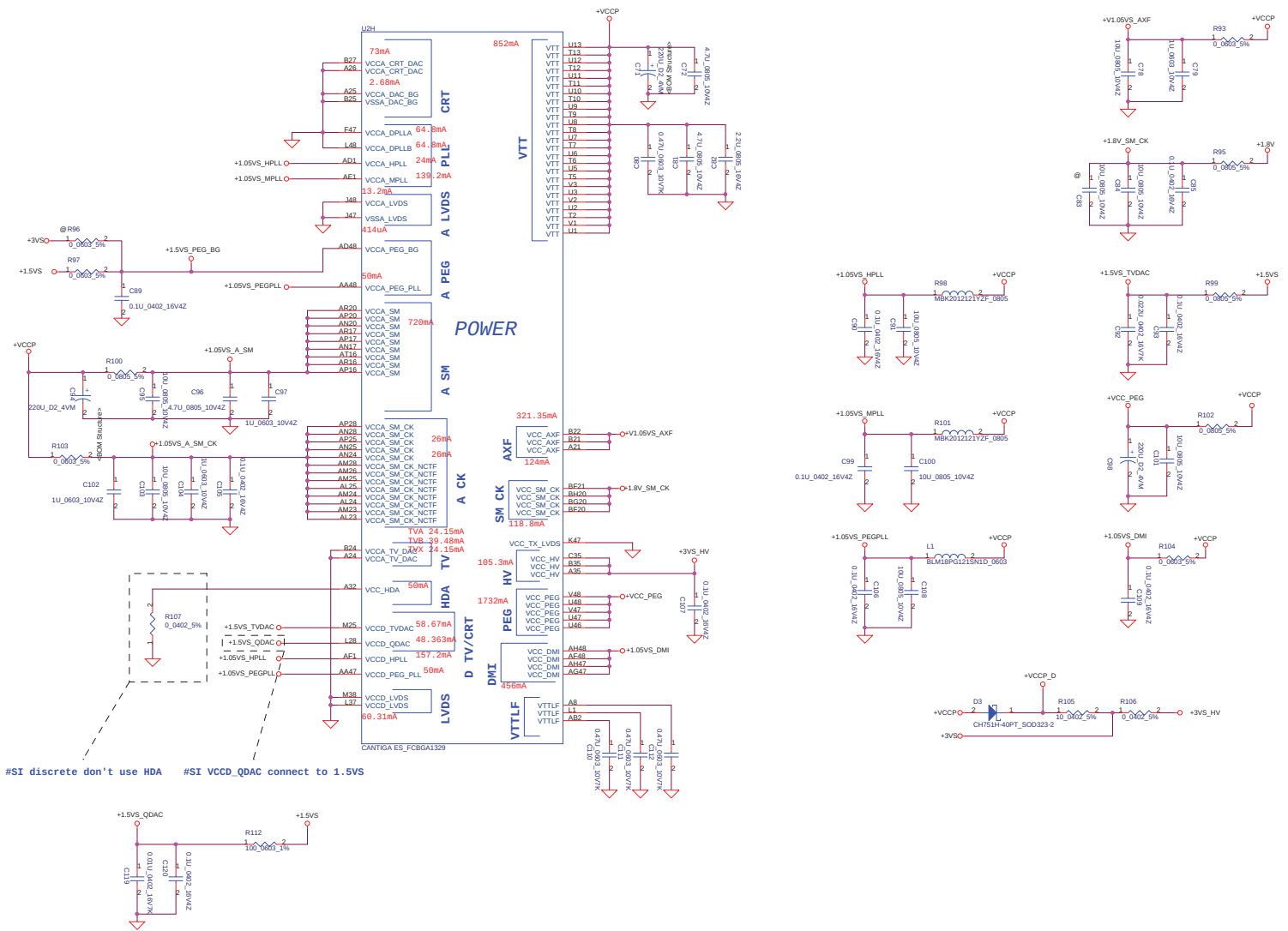
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JCPUID		
A4	VSS[001]	P6
A4	VSS[002]	P21
A11	VSS[003]	P24
A14	VSS[004]	P2
A16	VSS[005]	P22
A19	VSS[006]	P22
A23	VSS[007]	P22
AF2	VSS[008]	T1
B6	VSS[009]	VSS[090]
B8	VSS[010]	T26
B11	VSS[011]	T23
B13	VSS[012]	VSS[092]
B16	VSS[013]	VSS[094]
B19	VSS[014]	VSS[095]
B21	VSS[015]	VSS[096]
B24	VSS[016]	VSS[097]
C5	VSS[017]	VSS[098]
C8	VSS[018]	VSS[099]
C11	VSS[019]	VSS[100]
C14	VSS[020]	VSS[101]
C16	VSS[021]	VSS[102]
C19	VSS[022]	VSS[103]
C2	VSS[023]	VSS[104]
C22	VSS[024]	VSS[105]
C25	VSS[025]	VSS[106]
D1	VSS[026]	VSS[107]
D4	VSS[027]	VSS[108]
D6	VSS[028]	VSS[109]
D11	VSS[029]	VSS[110]
D16	VSS[030]	VSS[111]
D19	VSS[031]	VSS[112]
D23	VSS[032]	VSS[113]
D26	VSS[033]	VSS[114]
D29	VSS[034]	VSS[115]
E3	VSS[035]	VSS[116]
E6	VSS[036]	VSS[117]
F1	VSS[037]	VSS[118]
F14	VSS[038]	VSS[119]
F16	VSS[039]	VSS[120]
F19	VSS[040]	VSS[121]
F24	VSS[041]	VSS[122]
F26	VSS[042]	VSS[123]
F29	VSS[043]	VSS[124]
F3	VSS[044]	VSS[125]
F8	VSS[045]	VSS[126]
F11	VSS[046]	VSS[127]
F13	VSS[047]	VSS[128]
F16	VSS[048]	VSS[129]
F19	VSS[049]	VSS[130]
F2	VSS[050]	VSS[131]
F22	VSS[051]	VSS[132]
F25	VSS[052]	VSS[133]
G1	VSS[053]	VSS[134]
G23	VSS[054]	VSS[135]
G26	VSS[055]	VSS[136]
H3	VSS[056]	VSS[137]
H6	VSS[057]	VSS[138]
H21	VSS[058]	VSS[139]
H24	VSS[059]	VSS[140]
J2	VSS[060]	VSS[141]
J22	VSS[061]	VSS[142]
J25	VSS[062]	VSS[143]
K1	VSS[063]	VSS[144]
K4	VSS[064]	VSS[145]
K23	VSS[065]	VSS[146]
K26	VSS[066]	VSS[147]
L3	VSS[067]	VSS[148]
L6	VSS[068]	VSS[149]
L21	VSS[069]	VSS[150]
L24	VSS[070]	VSS[151]
M2	VSS[071]	VSS[152]
M5	VSS[072]	VSS[153]
M22	VSS[073]	VSS[154]
M25	VSS[074]	VSS[155]
M29	VSS[075]	VSS[156]
N1	VSS[076]	VSS[157]
N14	VSS[077]	VSS[158]
N19	VSS[078]	VSS[159]
N23	VSS[079]	VSS[160]
N26	VSS[080]	VSS[161]
P1	VSS[081]	VSS[162]
P19	VSS[082]	VSS[163]

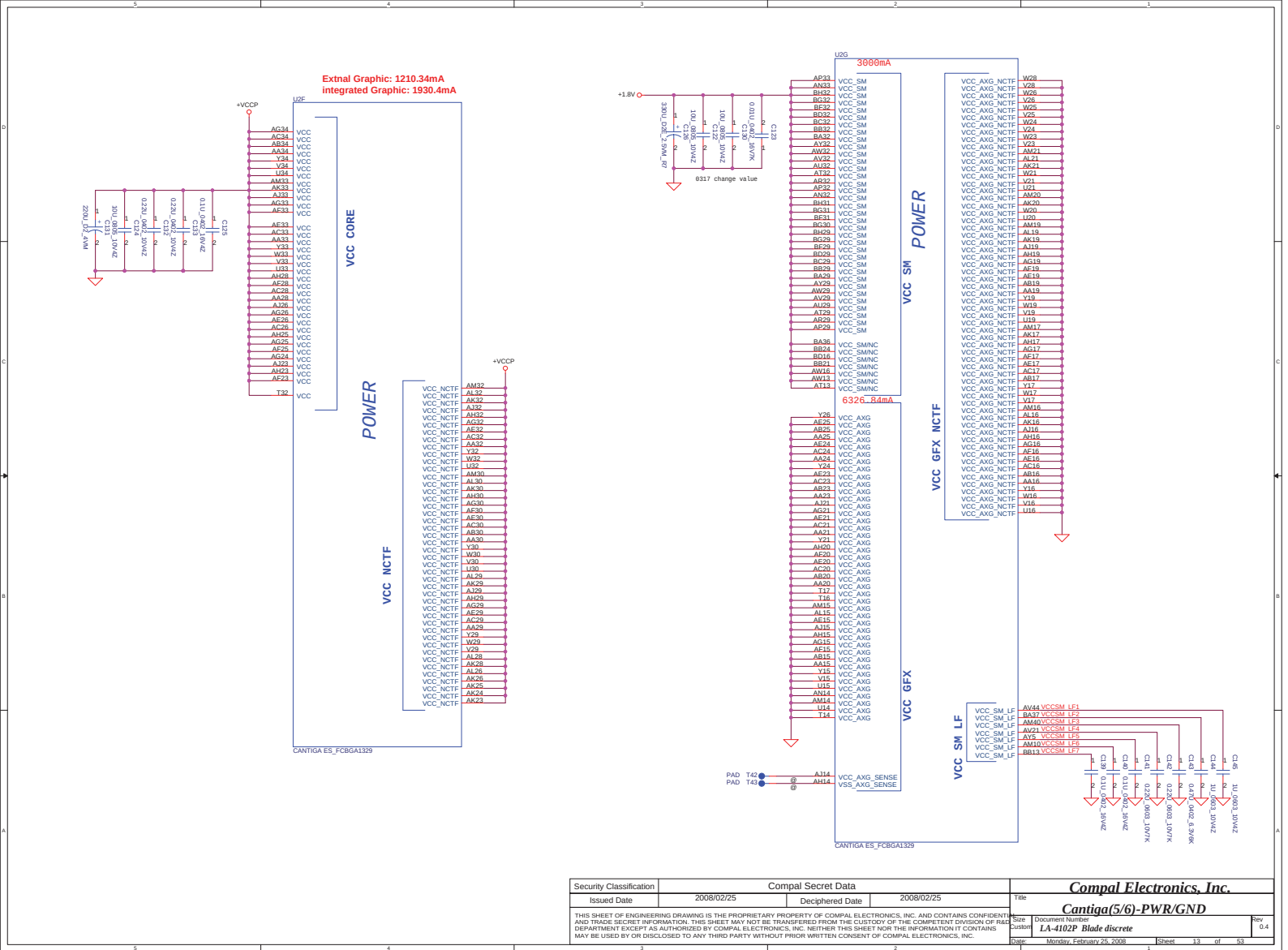


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				Sheet	8 of 53

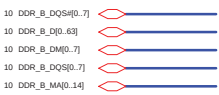
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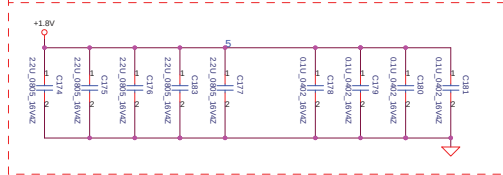
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				Document Number
				LA-4102P Blade discrete
				Rev
				0.4
				Date
				Monday, February 25, 2008
				Sheet
				12 of 53



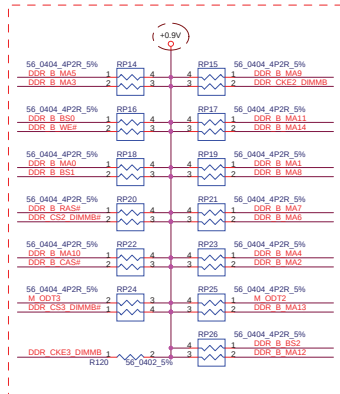
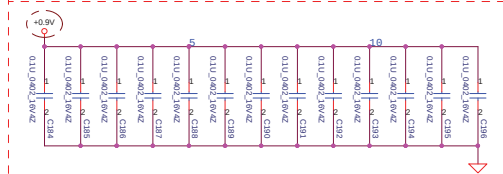
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Issued Date	2008/02/25	Deciphered Date	2008/02/25	DDRII-SODIMM SLOT1 LA-4102P Blade discolor
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			Drawn 2008/02/25 Checked 2008/02/25	63



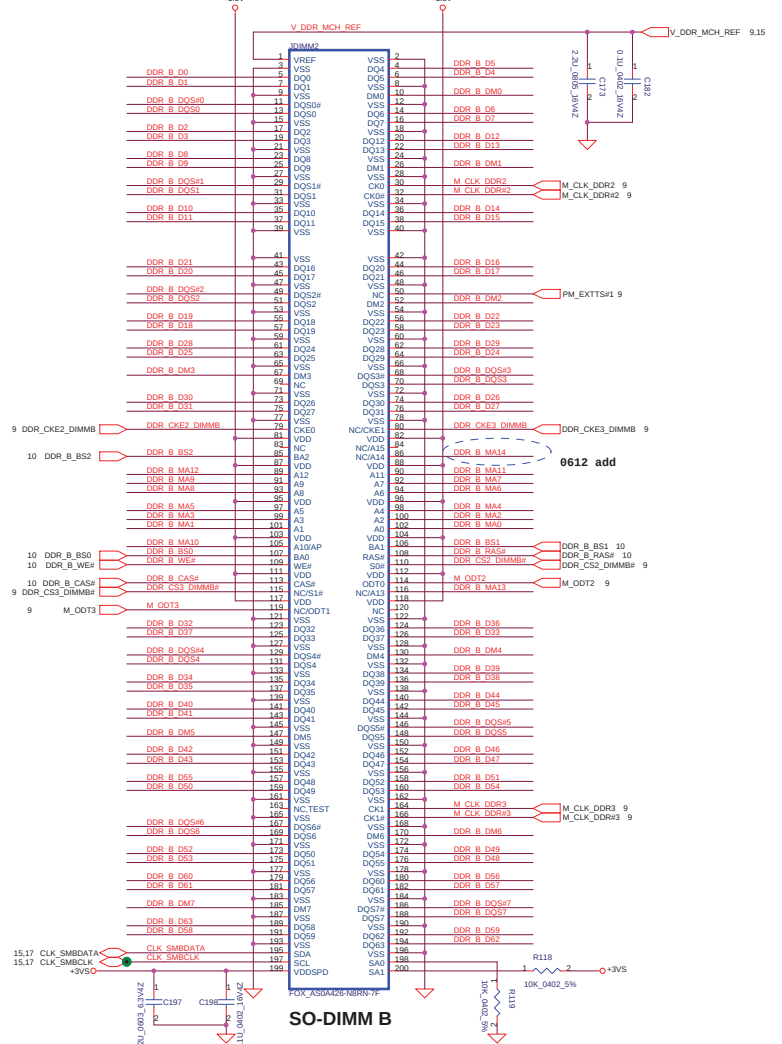
Layout Note:
Place near JP10



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V5



Layout Note:
Place these resistor closely JP3, all trace length Max=1.5"



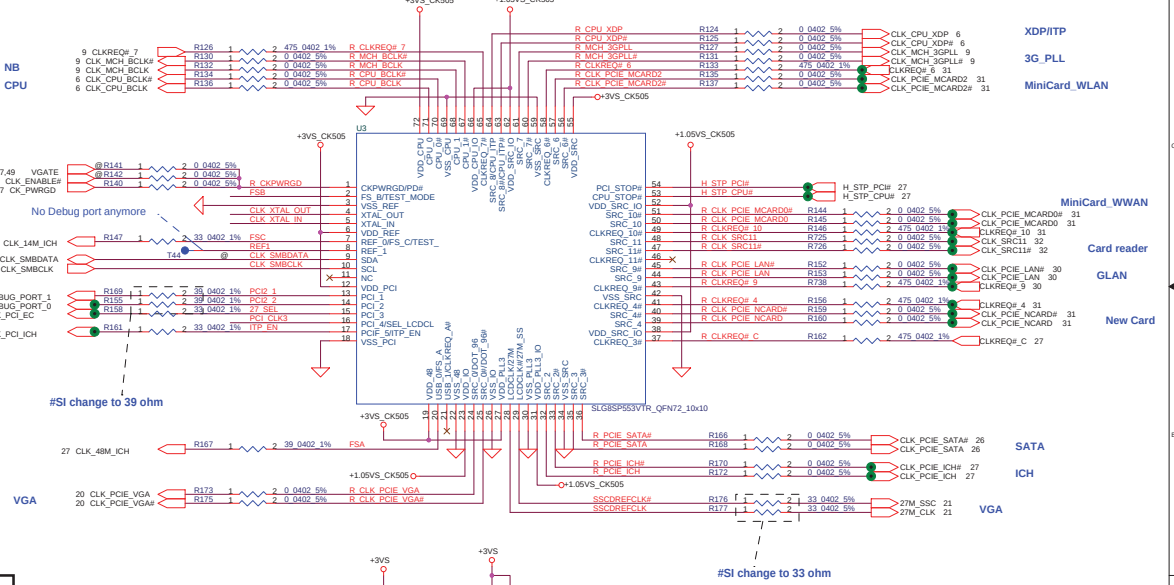
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Issued Date	2008/02/25	Deciphered Date	2009/02/25	Title	DDR2-SODIMM SLOT2
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				Rev	0.4
				Date	Monday, February 25, 2008
				Sheet	18 of 53

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Routing the trace at least 10mil

Place close to U51

Vendor suggests 22pF



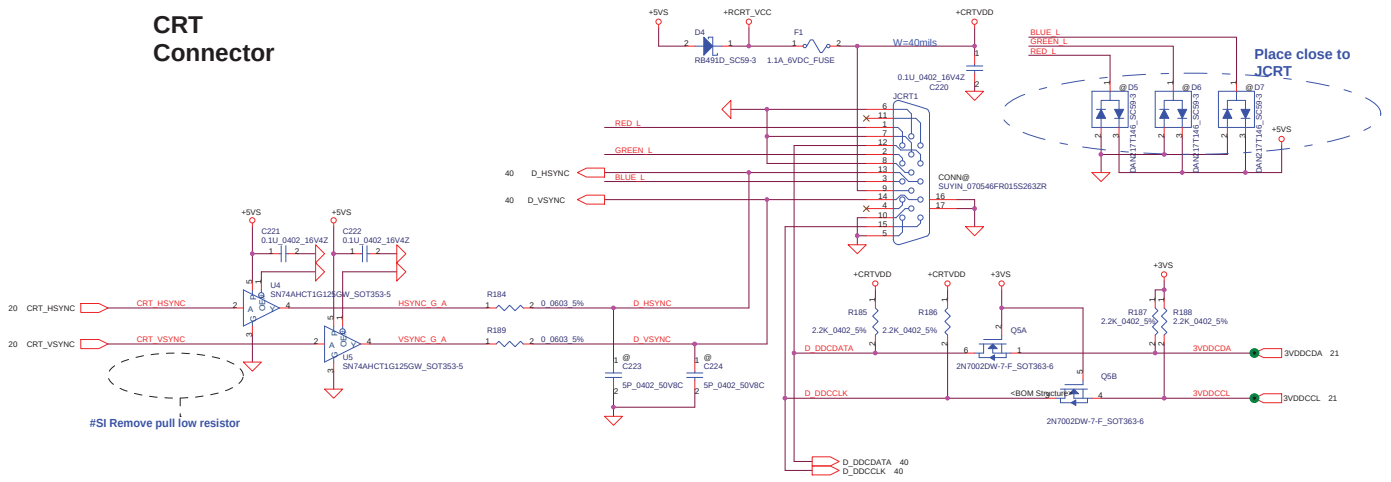
#SI change to 33 ohm

#PV for WWAN noise add 12P

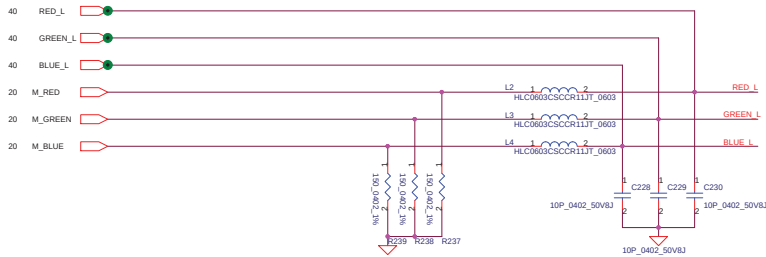
21.27.31.37	ICH_SMBDATA	2	CLK_48M_ICH
21.27.31.37	ICH_SMBCLK	4	CLK_14M_ICH
21.27.31.37	ICH_SMBCLK	4	CLK_PCI_ICH
21.27.31.37	ICH_SMBCLK	4	CLK_PCI_EC

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					Rev 0.4
				LA-1022 Blde discrete	
Drawn				Monday, February 25, 2008	Sheet 17 of 53

CRT Connector



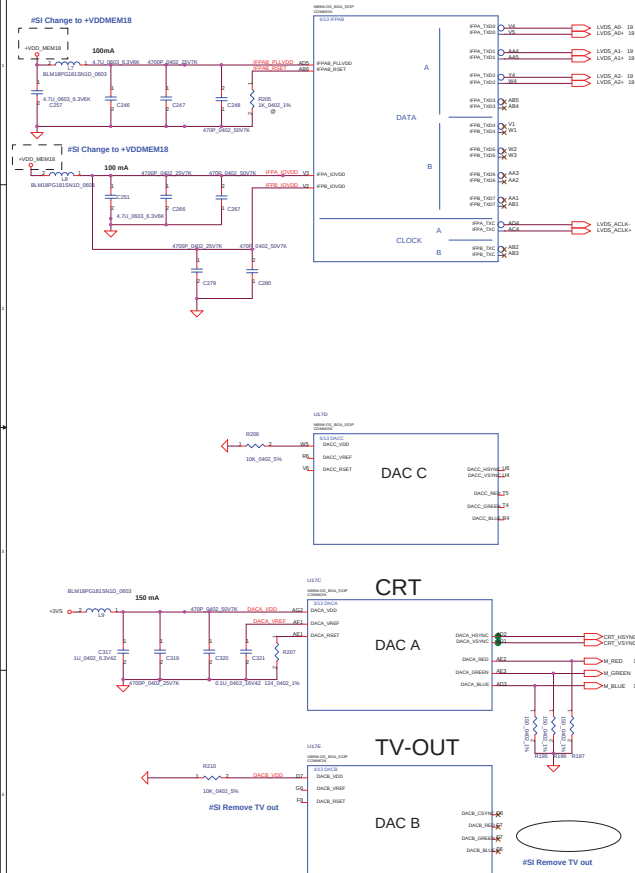
#SI Remove pull low resistor



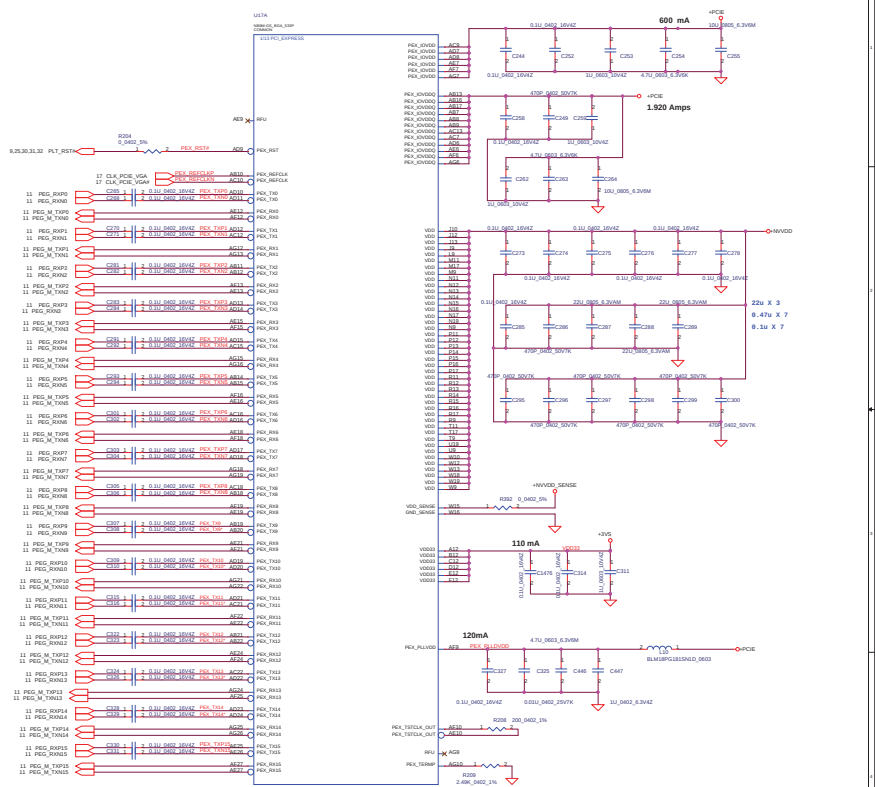
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				Document Number
				LA-4102P Blade discrete
				Rev
				0.4
				Date
				Monday, February 25, 2008
				Sheet
				18 of 53

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LVDS & DAC Interface



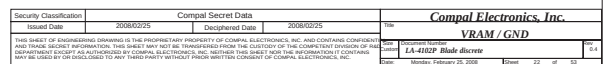
PEG Interface



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APPROVED BY: LA-0102				Rev	

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23 MDA[15..0] MDA[15..0]
23 MDA[31..16] MDA[31..16]
24 MDA[47..32] MDA[47..32]
24 MDA[63..48] MDA[63..48]

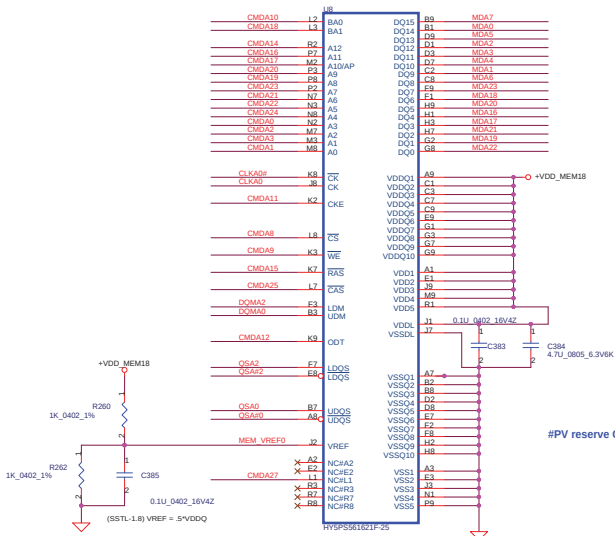
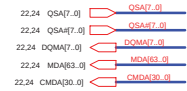


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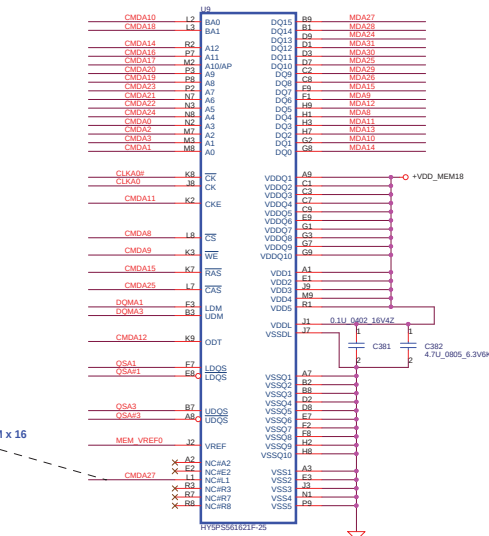
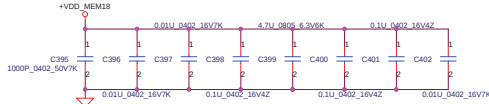
VRAM DDR2 chips (256MB & 512MB)

32Mx16 DDR2 400MHz *4==>256MB

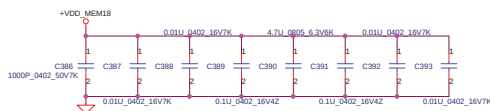
64Mx16 DDR2 400MHz*4==>512MB



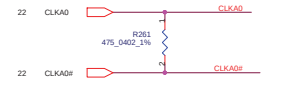
DDR2 BGA MEMORY



DDR BGA MEMORY



DATA Bus		
Address	0..31	32..63
CMD0	A3	
CMD1	A0	A0
CMD2	A2	
CMD3	A1	A1
CMD4		A3
CMD5		A4
CMD6		A5
CMD7		
CMD8	CS#	CS#
CMD9	WE#	WE#
CMD10	BA0	BA0
CMD11	CKE	CKE
CMD12	ODT	ODT
CMD13		
CMD14	A12	A12
CMD15	RAS#	RAS#
CMD16	A11	A11
CMD17	A10	A10
CMD18	BA1	BA1
CMD19	A8	A8
CMD20	A9	A9
CMD21	A6	A6
CMD22	A5	
CMD23	A7	A7
CMD24	A4	
CMD25	CAS#	CAS#
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		
CMD29		
CMD30		



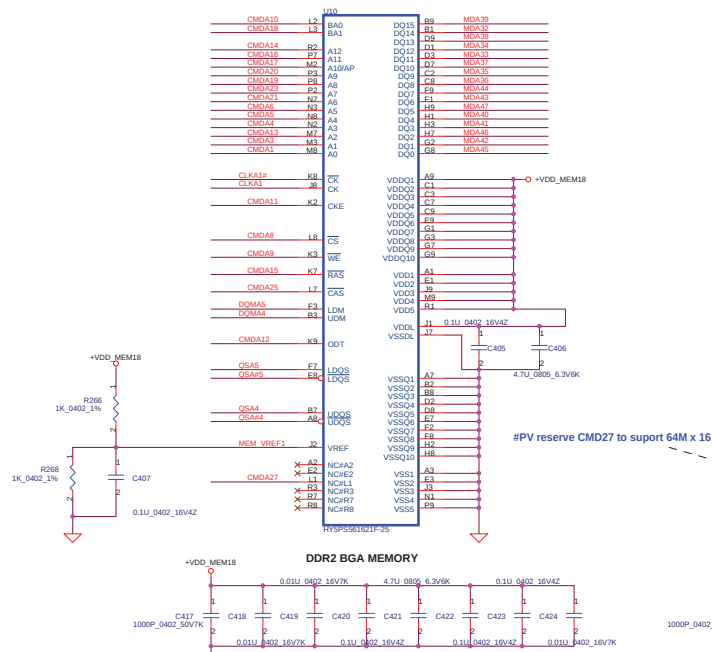
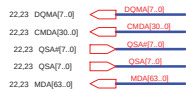
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				Date Monday, February 25, 2008 Sheet 7 of 16

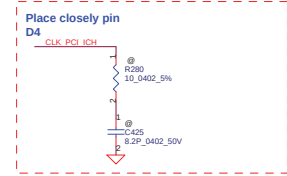
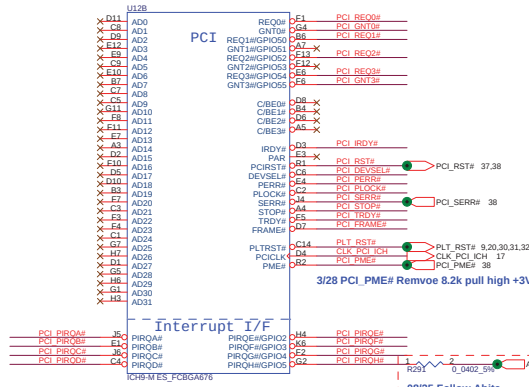
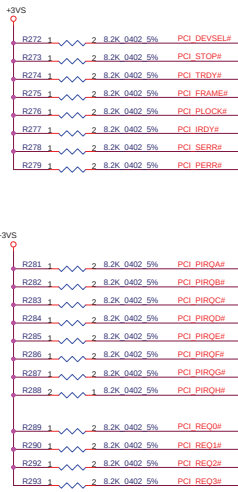
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VRAM DDR2 chips (256MB & 512MB)

32Mx16 DDR2 400MHz *4==>256MB

64Mx16 DDR2 400MHz*4==>512MB





A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enble High= Default *



Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *

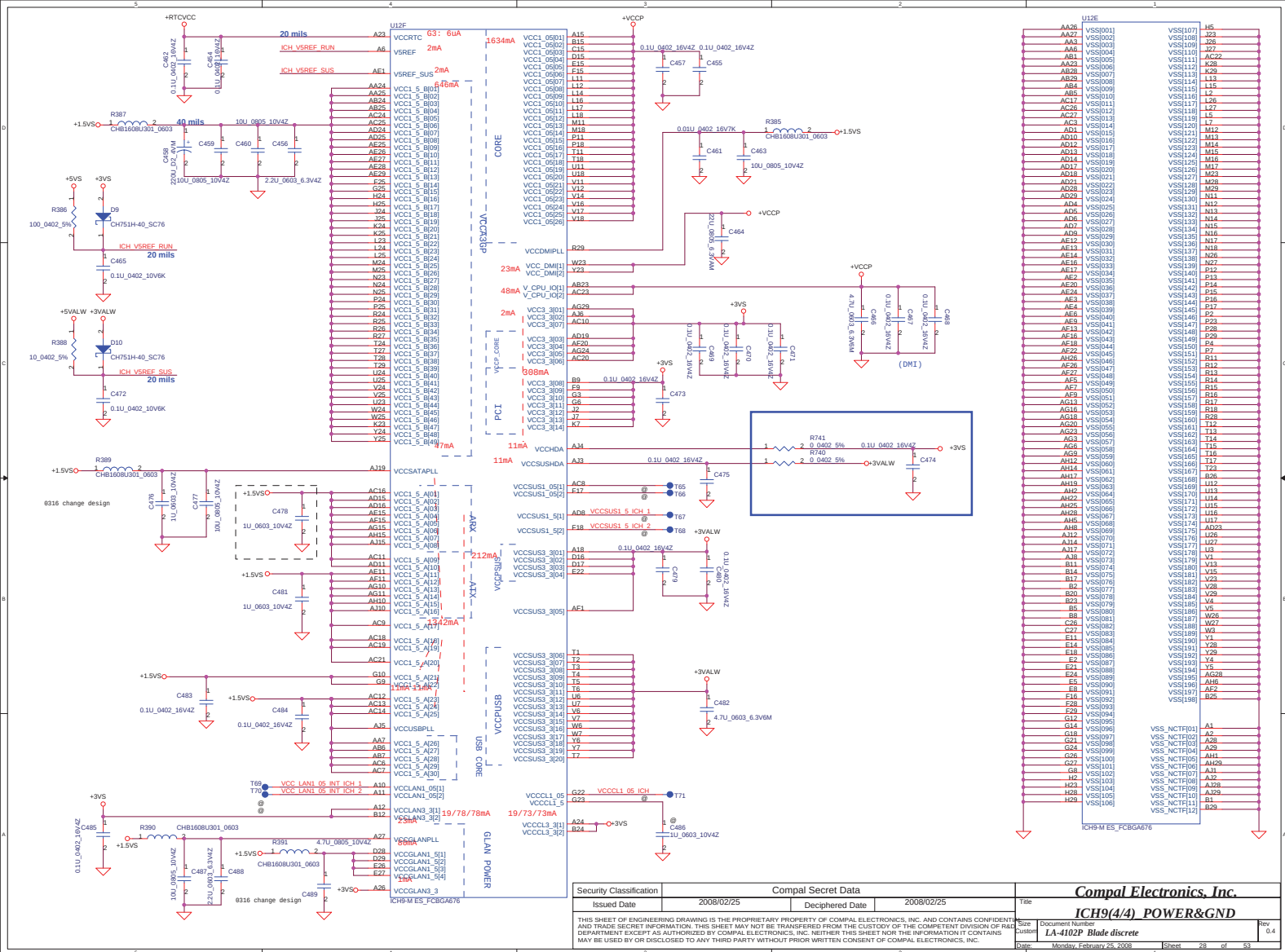


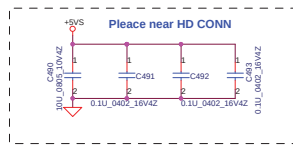
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				Rev	0.4
				Date	Monday, February 25, 2008
				Sheet	26 of 53

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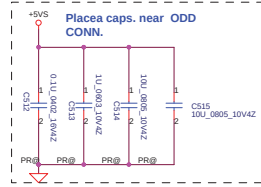
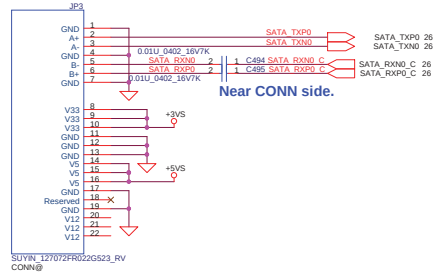
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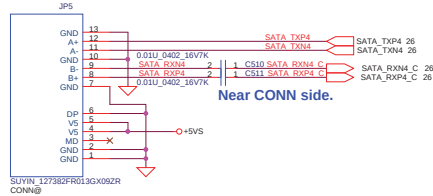




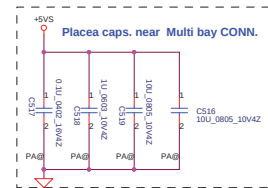
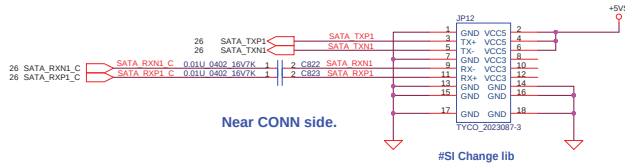
HDD Connector



CD-ROM Connector

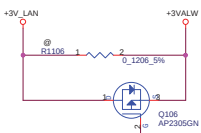


Multi Bay Connector

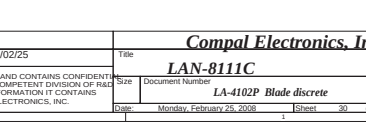
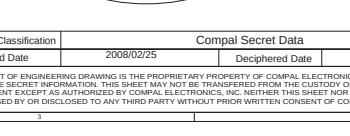
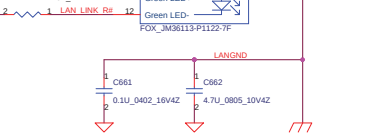
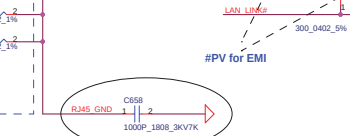
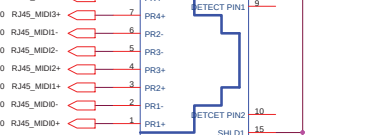
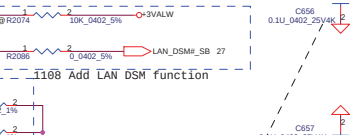
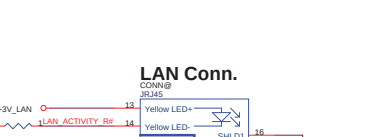
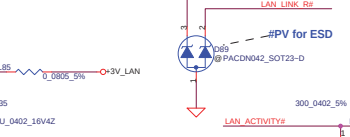
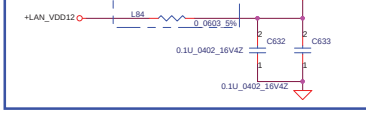
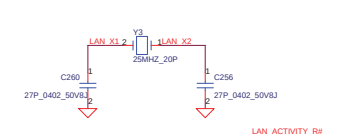
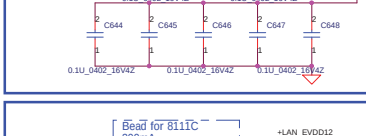
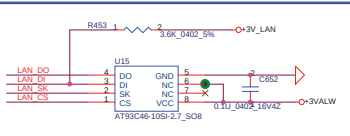
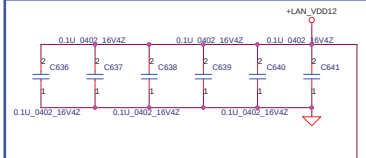
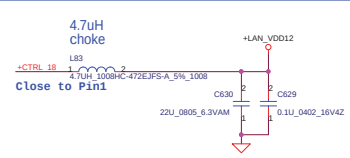
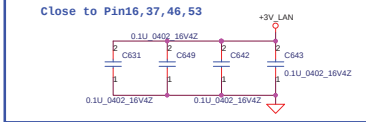
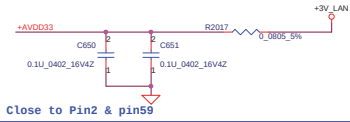
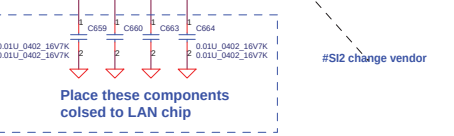
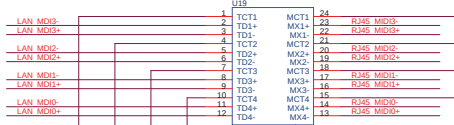
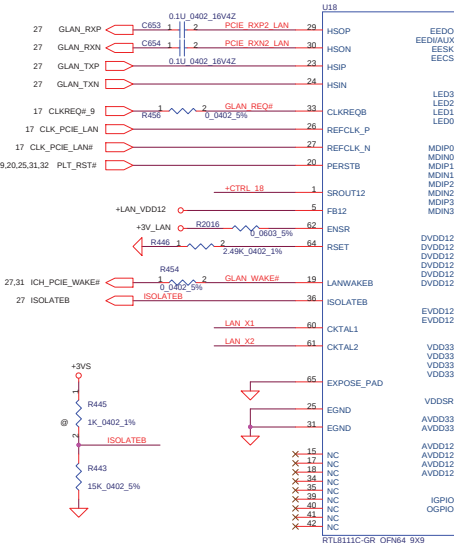


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				Document Number
				LA-4102P Blade discrete
				Rev
				0.4
				Date
				Monday, February 25, 2008
				Sheet
				28 of 53

1025 add to meet HP request



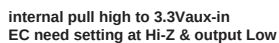
Place Close to Chip



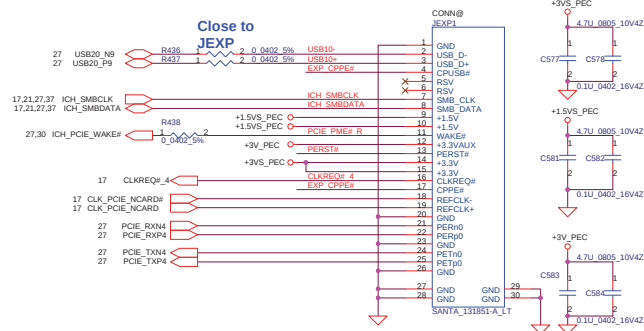
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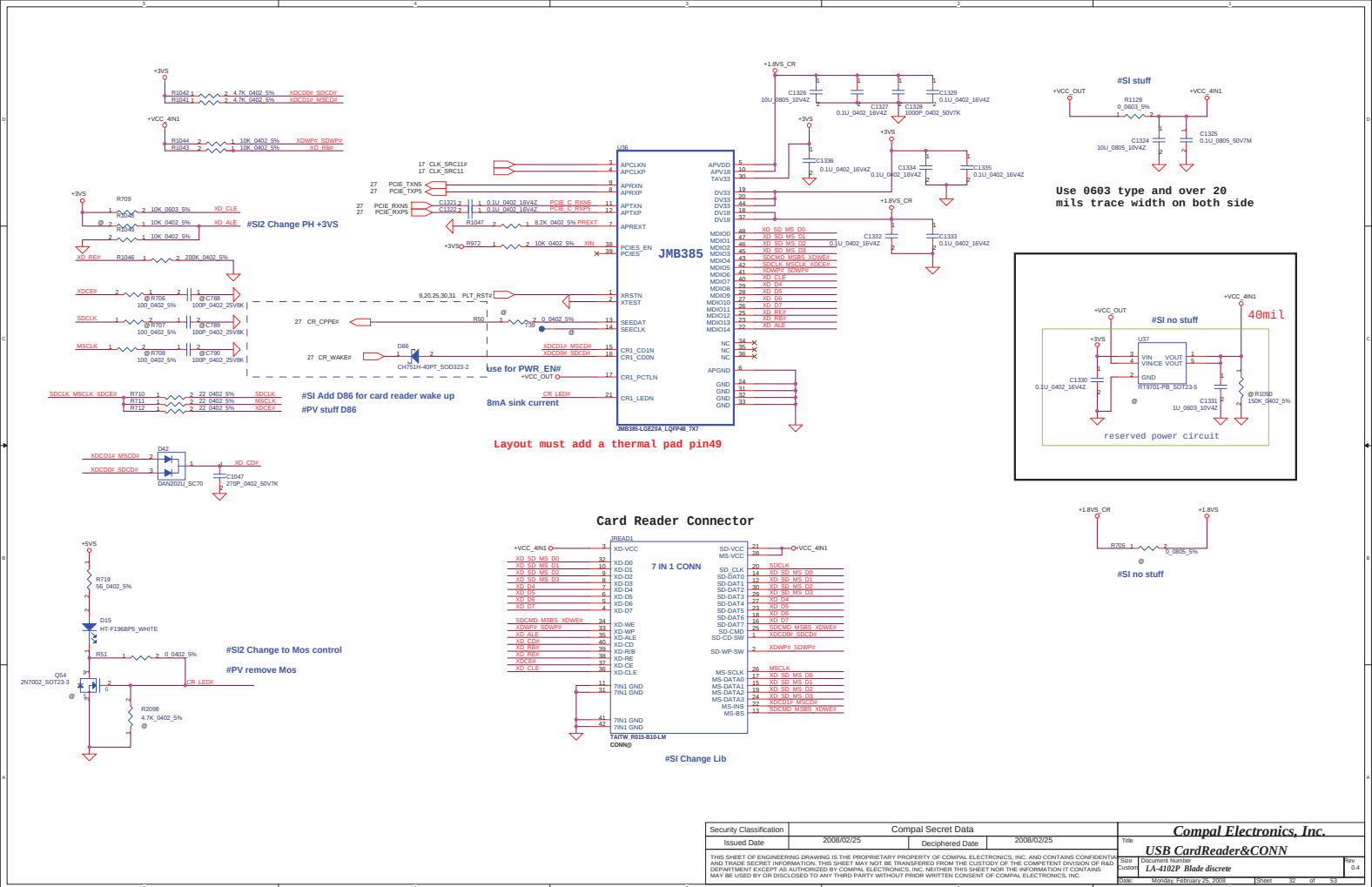
SIM card Connector



Near to Express Card slot.



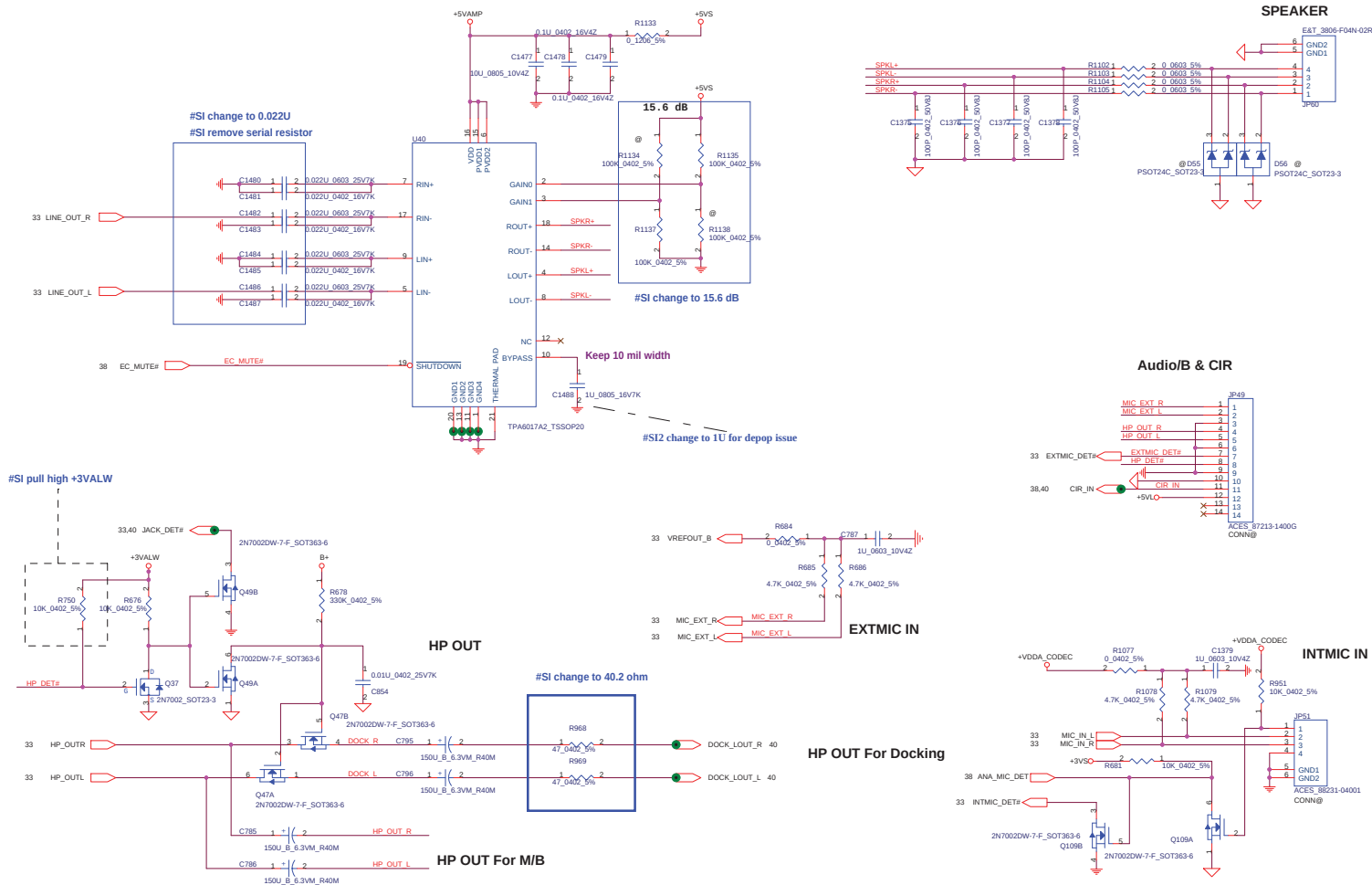
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Date:	Monday, February 25, 2008	Page	31	of 53



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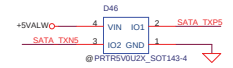
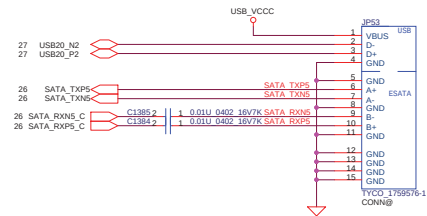
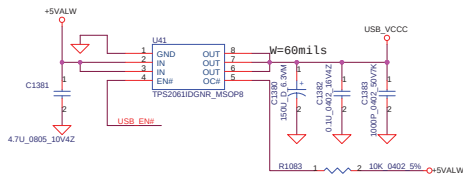
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Date			Monday, February 25, 2008	Rev 0.4
Sheet			34	of 53



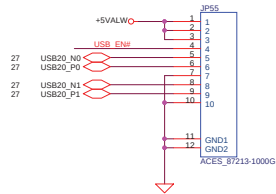
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				Date	Monday, February 25, 2008
				Sheet	35 of 53
				Rev	0.4

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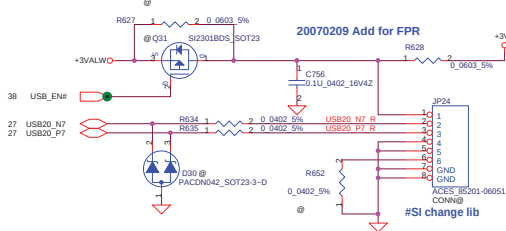
Left side ESATA/USB combination Connector



USB cable connector for Right side

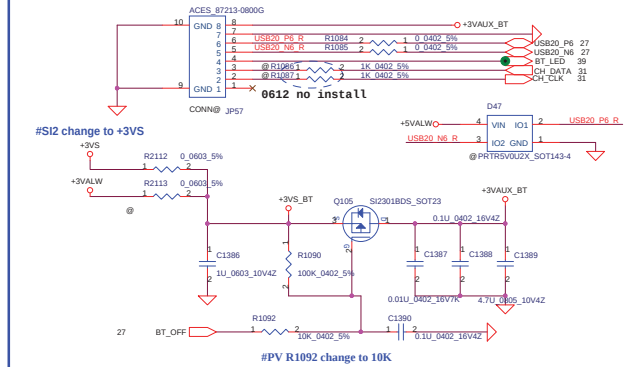


Finger printer



BT Connector

Need change to New version

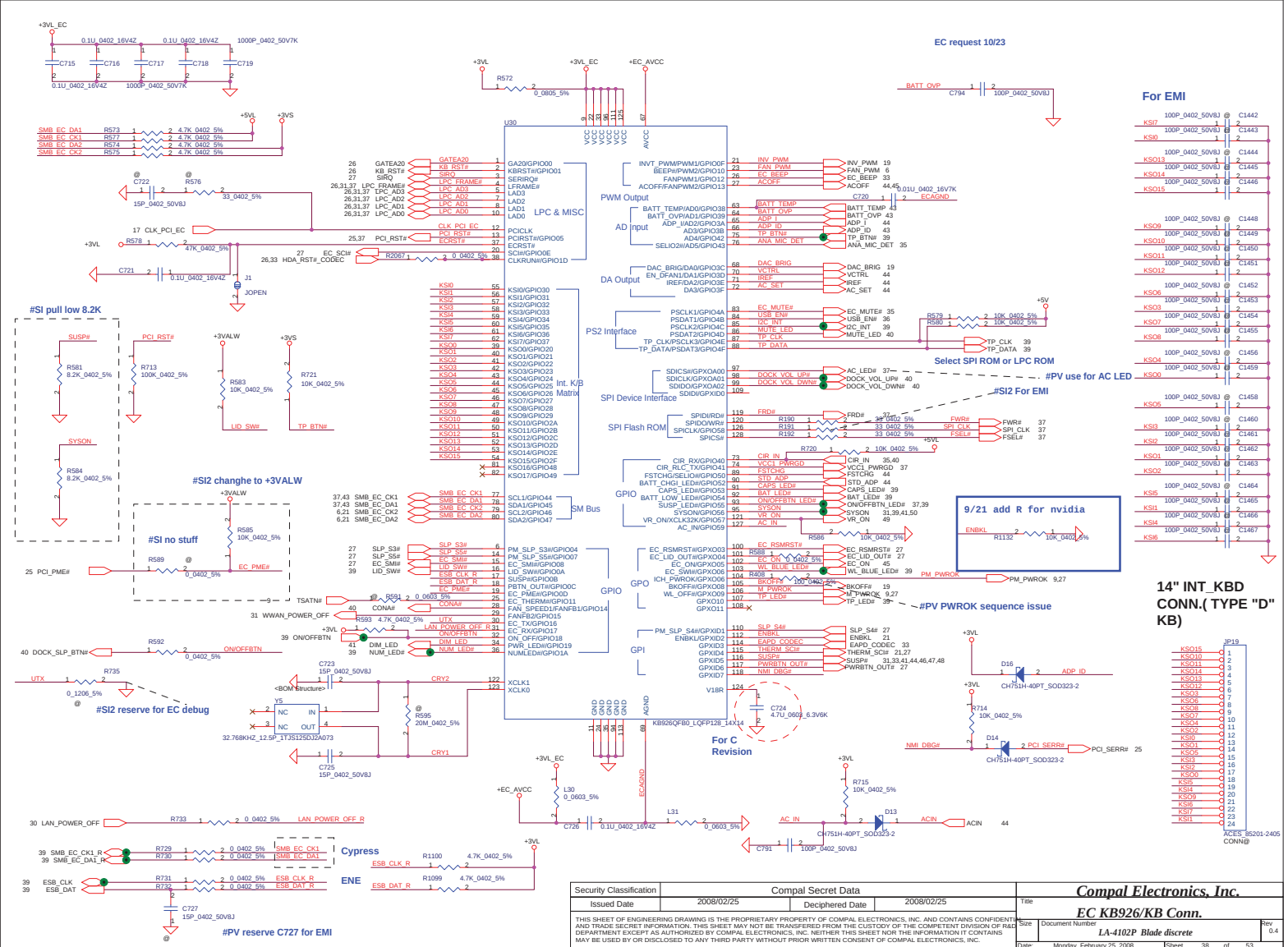


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				Date	Munday, February 25, 2008
				Sheet	38 of 53

Compal Electronics, Inc.

USB, BT, eSATA

LA-4102P Blade discrete



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System LED



38 CAPS_LED# 1 D50 HT-F1968PS_WHITE 2 R1095 200_0402_5% 3 5V5_LED

White

White

38 BAT_LED# 1 D52 HT-F1968PS_WHITE 2 R1097 200_0402_5% 3 5VALW_LED

White

QSMF-C1GE_AMBER-WHITE

White

26 SATA_LED# 1 R1098 200_0402_5% 2 5V5_LED

White

27 HDDHALT_LED# 3 R173 200_0402_5% 4 3V5

AMBER

AB887 D53

White

ON/OFFBTN_LED# 1 D17 HT-F1968PS_WHITE 2 R880 200_0402_5% 3 5VALW_LED

System Power LED

[illegible]

The diagram illustrates the ACES i6201-1005N connector with the following components and connections:

- ESB Signals:**
 - ESB_CLK:** Connected to R2116 and C2123, with a 33_0402_5% resistor and 15P_0402_50V8J capacitor.
 - ESB_DAT:** Connected to R2117 and C2124, with a 33_0402_5% resistor and 15P_0402_50V8J capacitor.
- Power and Ground:**
 - +5V_LED:** Connected to pin 5 of the connector.
 - +3V_LED:** Connected to pin 1 of the connector.
 - +3V_L:** Connected to pin 1 of the connector, with a 33_0402_5% resistor and 15P_0402_50V8J capacitor.
 - Ground:** Connected to pins 10, 11, and 12 of the connector.
- Signal Connections:**
 - SMB_EC_CLK1_R:** Connected to pin 1.
 - SMB_EC_CLK:** Connected to pin 2.
 - ESB_DAT:** Connected to pin 3.
 - I2C_INT:** Connected to pin 4.
 - NUM_LED#:** Connected to pin 5.
 - SMB_EC_DAL1_R:** Connected to pin 6.
- Other Components:**
 - C2134:** A 33_0402_5% resistor and 15P_0402_50V8J capacitor connected to ground.
 - ACES i6201-1005N (CONN):** The main connector component.

Pin connection diagram for the ACES B5201-04051 connector. The diagram shows a blue connector with pins 1 through 6. Pin 1 is connected to +5VALW_LED. Pin 2 is connected to 38 ON/OFFBTN. Pin 3 is connected to 37,38 ON/OFFBTN_LED#. Pin 4 is connected to G1. Pin 5 is connected to G2. Pin 6 is connected to CONN#.

[illegible]

The schematic diagram illustrates the electrical connections for the T/P Board, divided into three main sections:

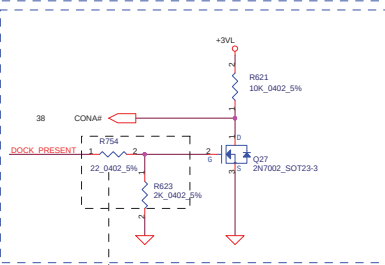
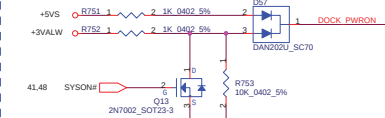
- TouchPAD ON/OFF LED:** This section shows the connection for the LED. It includes a +5V supply, a 10k resistor (R610), and a 200 ohm resistor (R609). The LED is connected to the PA and PR pins of the QSMF-C16E-AMBER-WHITE LED driver. The PA and PR pins are connected to the TP_LED# signal. The LED is also connected to the TP_LED# signal through a 10k resistor (R613).
- T/P Board:** This section shows the connection for the T/P Board. It includes a +5V supply, a 10k resistor (R611), and a 200 ohm resistor (R609). The LED is connected to the PA and PR pins of the QSMF-C16E-AMBER-WHITE LED driver. The PA and PR pins are connected to the TP_LED# signal. The LED is also connected to the TP_LED# signal through a 10k resistor (R613).
- T/P Power:** This section shows the connection for the T/P Power. It includes a +5V supply, a 10k resistor (R612), and a 200 ohm resistor (R609). The LED is connected to the PA and PR pins of the QSMF-C16E-AMBER-WHITE LED driver. The PA and PR pins are connected to the TP_LED# signal. The LED is also connected to the TP_LED# signal through a 10k resistor (R613).

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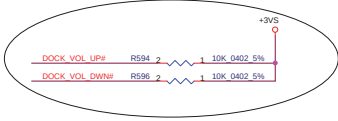
Atlas/ Saturn Dock

DOCK_PWR_ON Spec

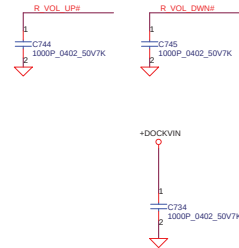
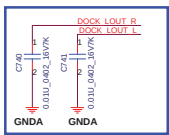
0V = Notebook S4/S5, Dock off
2.5V = Notebook S3, Dock on
4V = Notebook S0, Dock on



#SI2 Add pull up

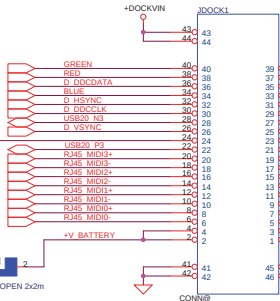


11/17 update

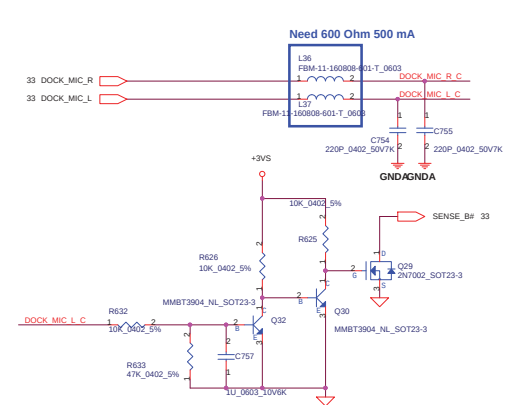


need change to reverse type connector

#SI2 change ping 31,39,22 connect to GND



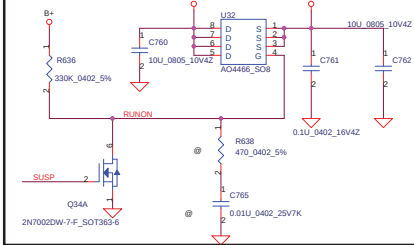
MIC_Dock



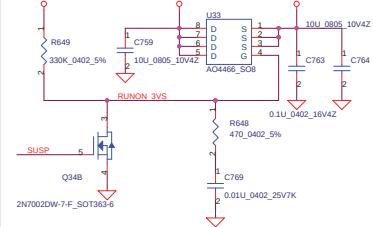
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DOCK CONN.				LA-4102P Blade discrete
Date: Monday, February 25, 2008				Sheet 40 of 53

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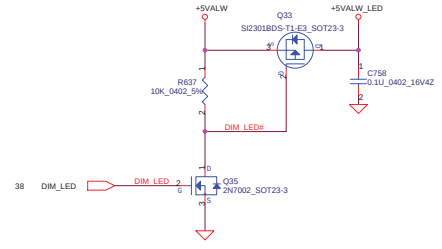
+5VALW to +5VS Transfer



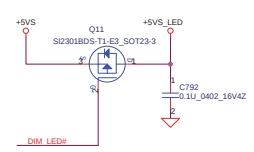
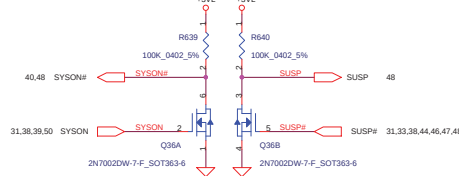
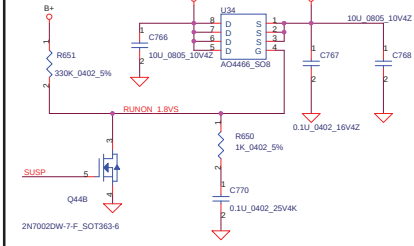
+3VALW to +3VS Transfer



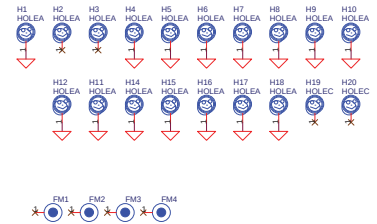
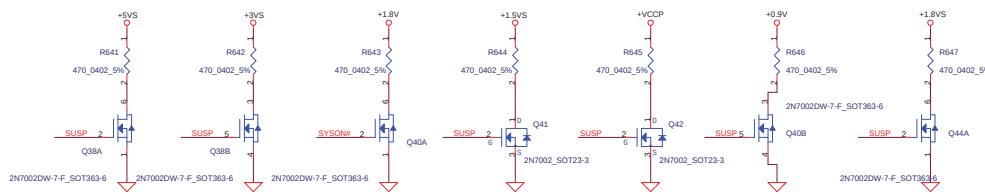
DIM LED



+1.8V to +1.8VS Transfer

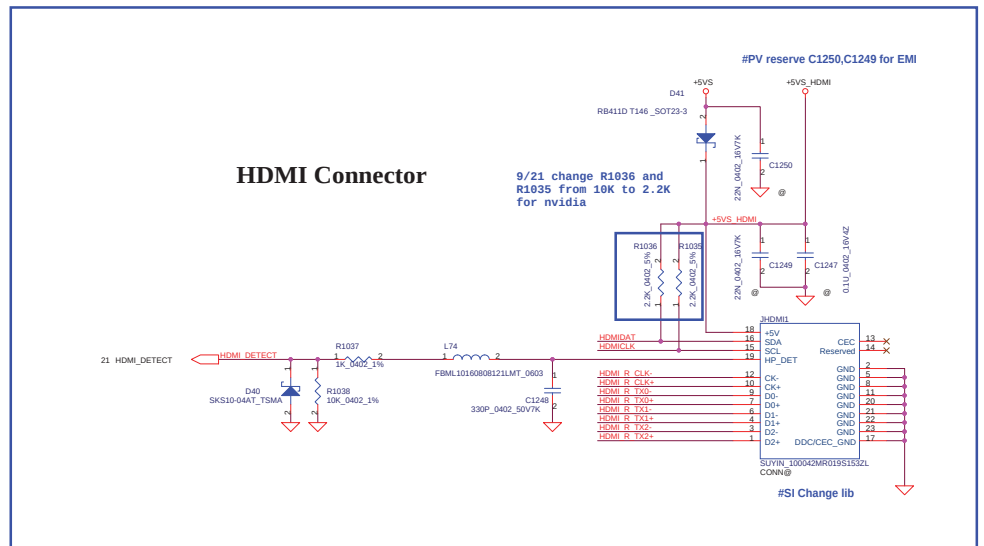
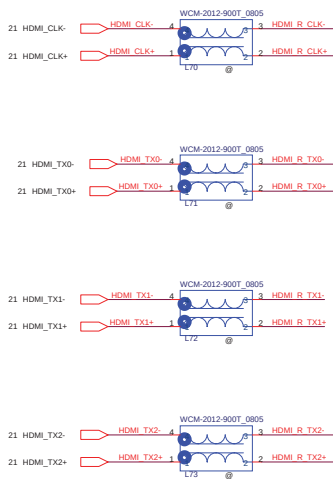
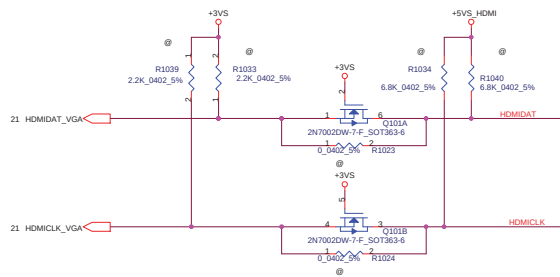


Discharge circuit



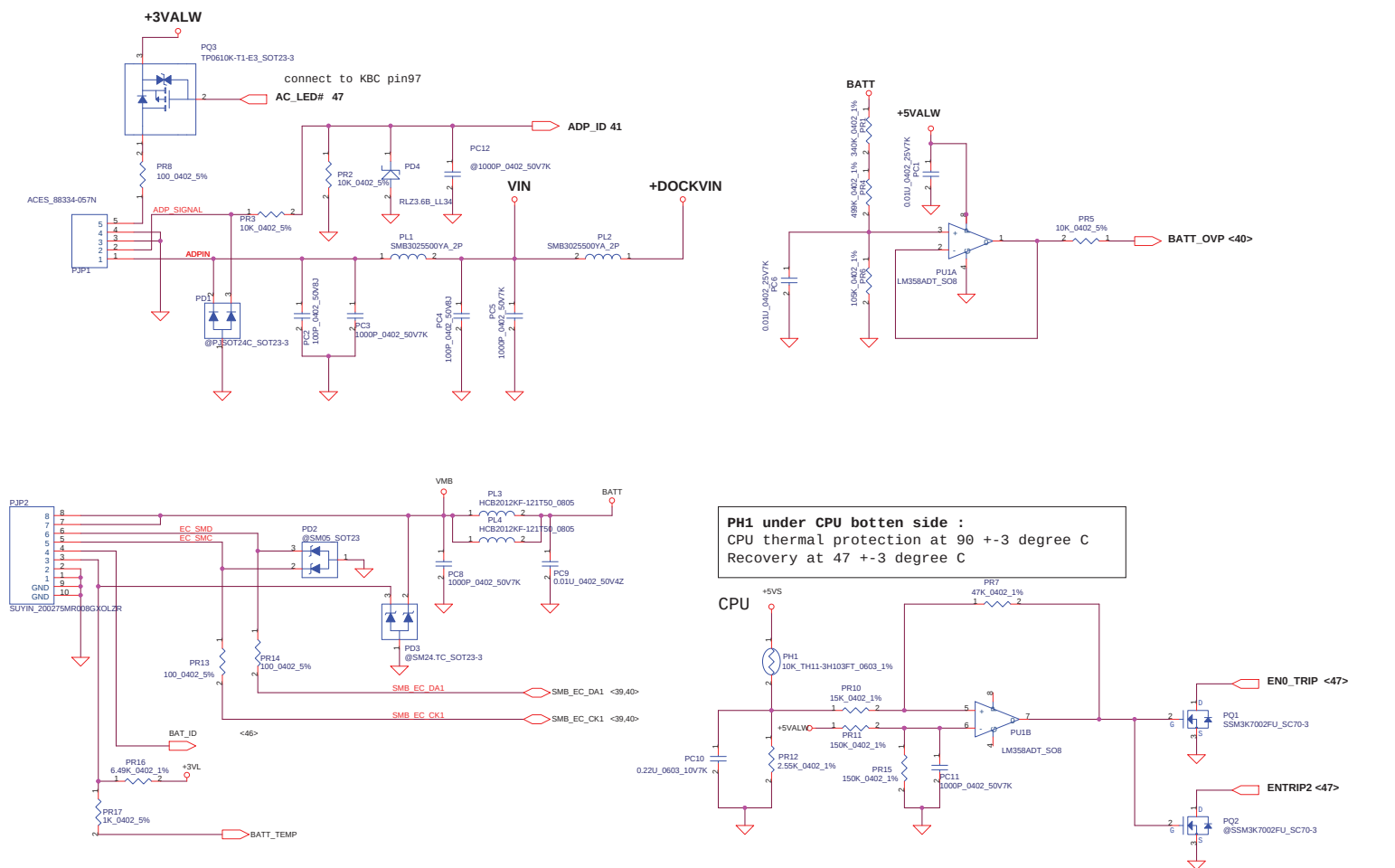
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				Document Number
				LA-4102P Blade discrete
				Rev
				0.4
				Date
				Monday, February 25, 2008
				Sheet
				41 of 53

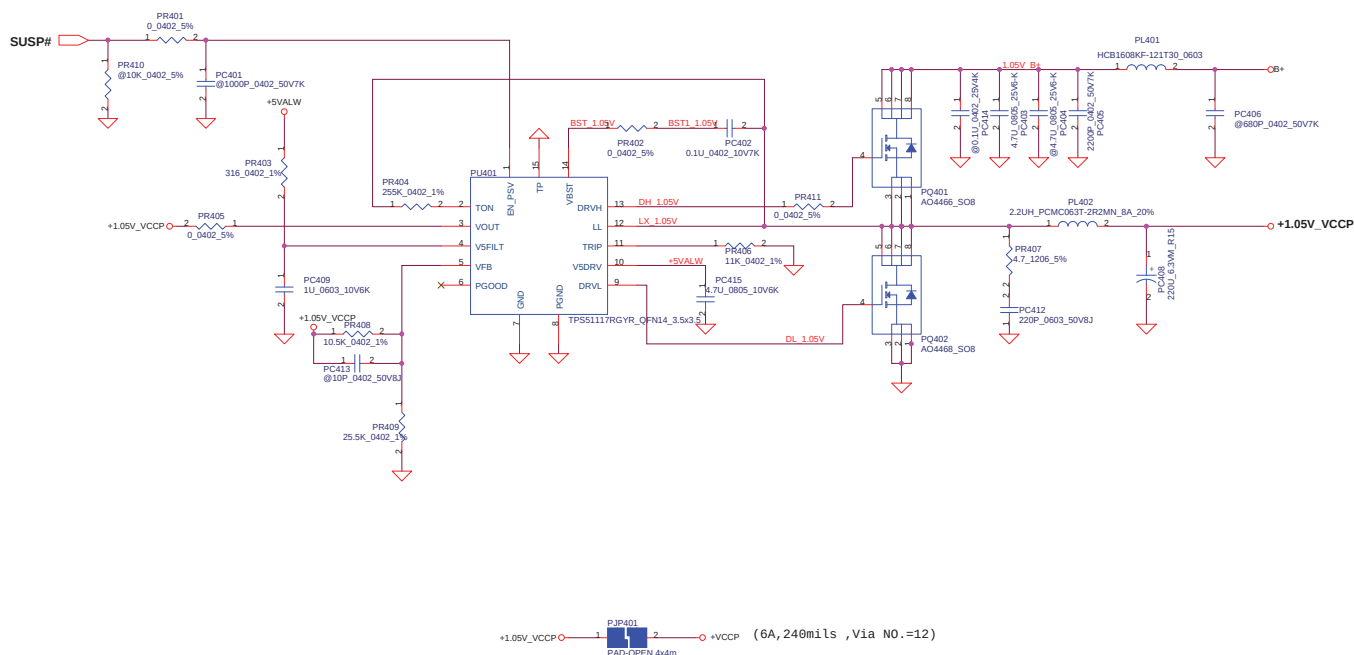
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				LA-4102P Blade discrete
				Rev
				0.4
				Date
				Monday, February 25, 2008
				Sheet
				42 of 53

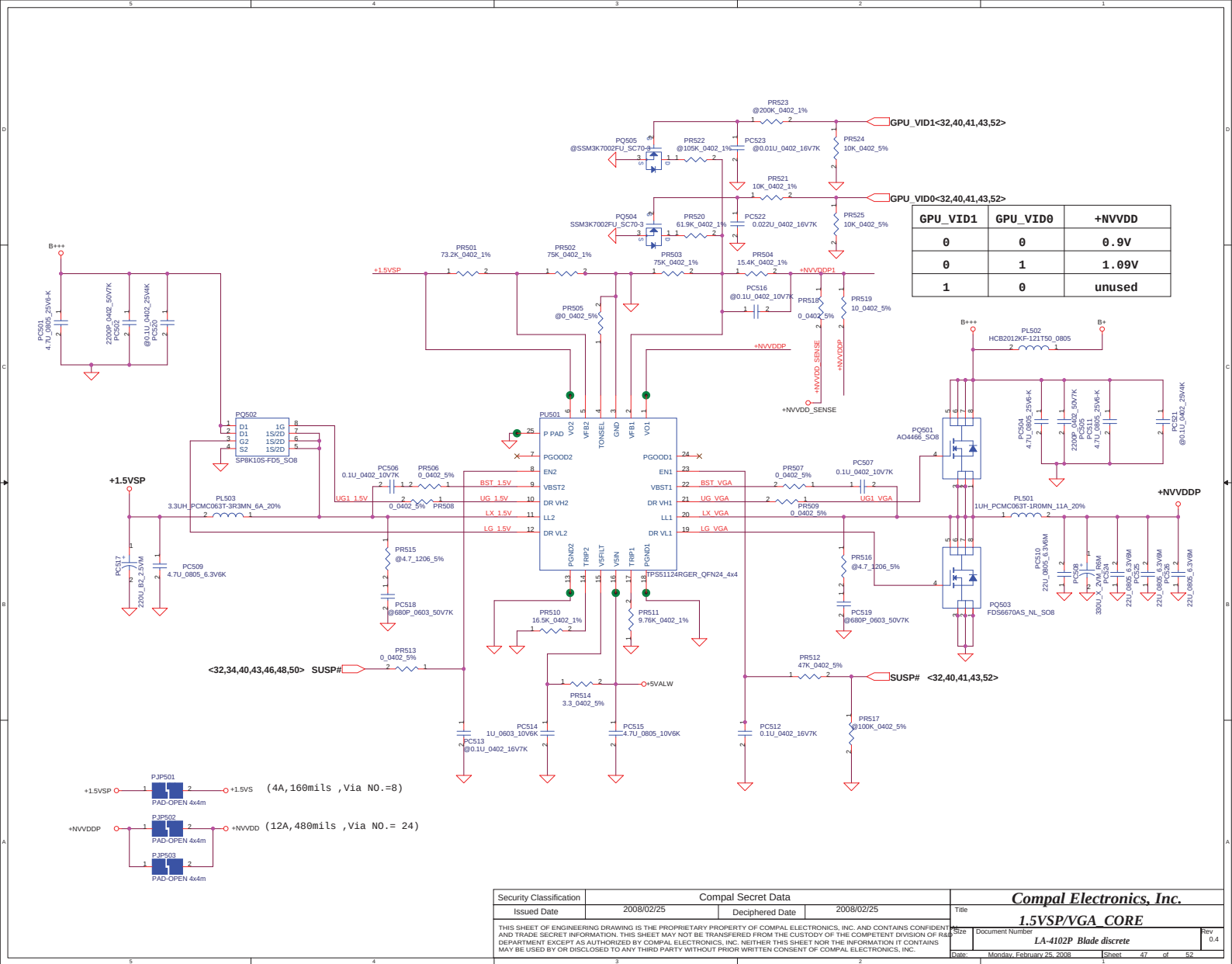
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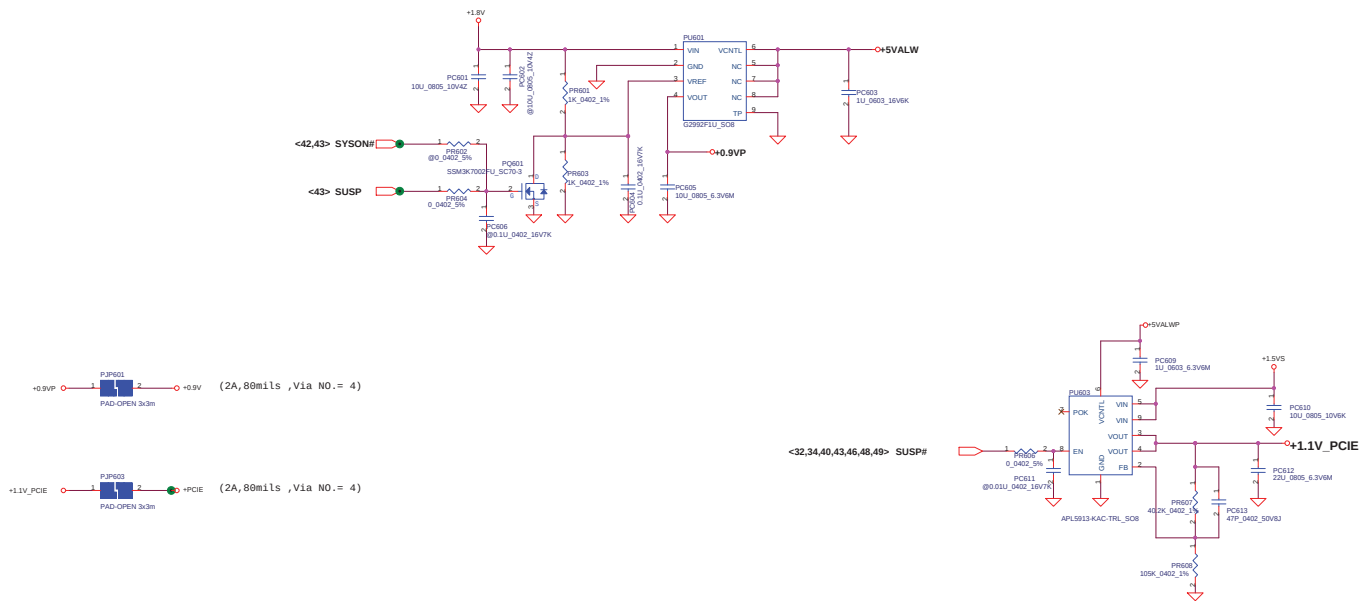


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			LA-4102P Blade discrete	0.4
			Date: Monday, February 25, 2008	Sheet 46 of 52

<http://laptop-motherboard-schematic.blogspot.com/>

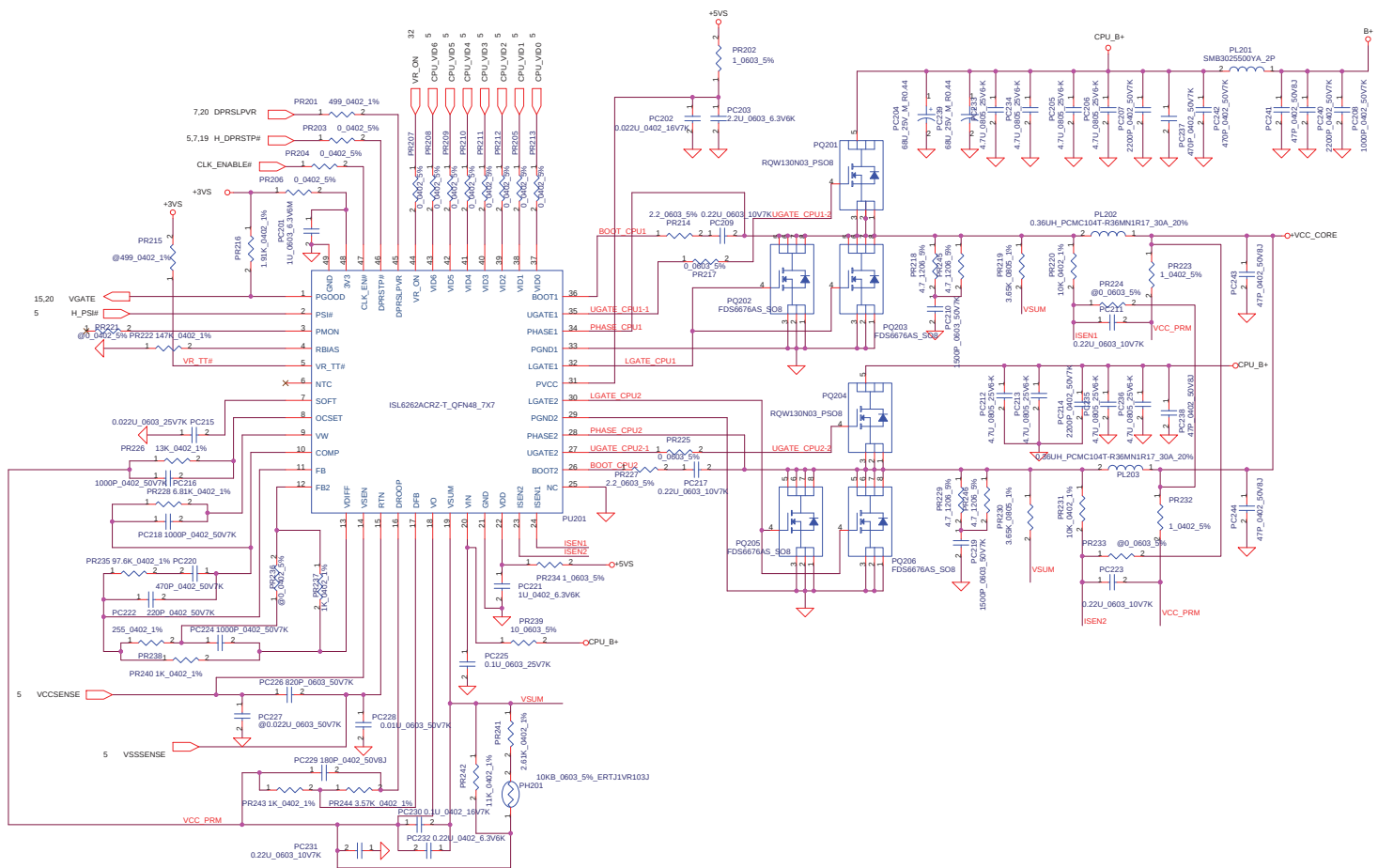


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				Document Number
				Rev
				04
				Date
				Monday, February 25, 2008
				Drawn
				48
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				52

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+CPU CORE

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Rev 0.4

Monday, February 25, 2008

Sheet 49 of 52

<http://laptop-motherboard-schematic.blogspot.com/>

Version Change List (P. I. R. List) for Power Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.																																			
1	43	DC Connector /CPU_OTP	11/06	Compal	Add PD4 & PC12	Add PD4 & PC12																																				
2	45	3.3VALWP/5VALWP	11/06	Compal	for Layout	Change PQ301, cancel PQ303.																																				
3	44	Charger	11/06	Compal	EMI solution	Add PC128																																				
4	49	CPU_CORE	11/06	Compal	EMI solution	Add PC240																																				
5	47	1.5VSP/VGA_CORE	11/06	Compal	for VGA voltage steps	Add PQ505, PR523, PR524, PR525																																				
6	45	3.3VALWP/5VALWP	12/31	Compal	PWR request	Add PU302, control signal changed to ACOFF																																				
7	44	Charger	12/31	Compal	EMI solution	Add PC129, PC130, PC131, PC132, PC133																																				
8	49	+CPU_CORE	12/31	Compal	EMI solution	Add PC242																																				
9	47	+1.5VSP/VGA COREP	01/02	Compal	HW request	Change PR513 to 0_ohm																																				
10	44	Charger	01/02	Compal	EMI solution	Add PC135 and PR141																																				
11	49	+CPU_CORE	02/15	Compal	Change high-side MOS for WWAN	Change PQ201 and PQ204 to powerpak																																				
12	43	DC Connector /CPU_OTP	02/15	Compal	AC LED change to KBC control	ACLED# connect to EC pin 97																																				
13	43	DC Connector /CPU_OTP	02/19	Compal	WWAM issue	add PC241 47pF																																				
14	49	+CPU_CORE	02/19	Compal	WWAM issue	add PC243 PC244 47pF																																				
<table><tr><td colspan="2">Security Classification</td><td colspan="3">Compal Secret Data</td><td colspan="2">Title</td></tr><tr><td colspan="2">Issued Date</td><td colspan="2">2008/02/25</td><td colspan="2">Deciphered Date</td><td colspan="2">2009/02/25</td></tr><tr><td colspan="6" rowspan="4">THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</td><td>Size</td><td>Document Number</td><td>Rev.</td></tr><tr><td>Custom</td><td colspan="2">LA-4102P Blade discrete</td><td>0.4</td></tr><tr><td>Date</td><td colspan="2">Monday, February 25, 2008</td><td>Sheet 53 of 52</td></tr><tr><td colspan="3"></td><td></td></tr></table>							Security Classification		Compal Secret Data			Title		Issued Date		2008/02/25		Deciphered Date		2009/02/25		THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.						Size	Document Number	Rev.	Custom	LA-4102P Blade discrete		0.4	Date	Monday, February 25, 2008		Sheet 53 of 52				
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						Date	Monday, February 25, 2008		Sheet 53 of 52																																	

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Item	Fixed Issue (Reason for change)	PAGE	Modify List	Date	Phase
1	Transation Fail	08	C41 、 C42 、 C43 、 C44 Change ESR=7m ohm	11/21	DB
2	Disable TV out function from Docking	20	TV signal unconnected,DACB_VDD pull low 10K (R948).	11/07	DB
3	Update Connetor Library		CRT(JCRT1) 、 HDMI(JHDMI1) 、 ESATA(JP53) 、 Finger print(JJP24) 、 FAN(JP2) 、 Speaker(JP60) 、 Multi bay(JP12) 、 Dual LED(D53 、 D54	11/17	DB
4	Delete LVDS B channel	19,20	Schematic Delete	11/17	DB
5	USB camera Footprint error	19	Change U42 to G916-390T1UF SOT23, it adjustable mode, R1091=215K 、 R1093=100K,Add GPIO 20 to turn off power	11/07	DB
6	Reserve Card reader D3E function	27,32	GPIO6= CR_CPPE# 、 GPIO22=CR_WAKE#	11/17	DB
7	Swap PCIE LAN and New card	27	Swap PCIE4 and PICE6	11/17	DB
8	Change GPU 1.8VS power	20 、 21	Change 1.8VS to +VDD_MEM18	11/17	DB
9	Change G sensor control from SB 、 LED drive by +5VS	27 、 39	Change G sensor control from SB	11/17	DB
10	Avoid Battery mode can't boot issue	38 、 45	Add +3VALW GD to EC_RSMRST# to fix Battery mode can't boot issue	11/17	DB
11	Add G sensor ST and Bosch	37	Add G sensor ST and Bosch	11/17	DB
12	Change LAN solution (Marvell to Realtek)	30	Change LAN solution (Marvell to Realtek)	11/17	DB
13	LAN transformer interfere	30	U19 Change to correct transformer type	11/17	DB
14	Cardreader schematic review,add D3E function	32	R709-->10K 、 R1047-->8.2K 、 R1128-->Stuff 、 R705-->@ 、 U37-->@ 、 Cardreader LED-->+5VS 、 add D3E function	11/17	DB
15	Jack can't detect normal	33	R1059 change from 39.2 to 39.2K	11/17	DB
16	Docking can not power on	40	Add power on circuit D57,Q13R751,R752,R753	11/17	DB
17	HP audio team recommend	33 、 35	C1480-C1487 、 C1352 、 C1354 change to 0.022U 、 Amp output setup to 15.6 dB 、 Reserve C747 、 C748 for GNDA and GND	11/17	DB
18	Audio jack can't detect normal	35	Add Pull up resistor R750 to +3VALW	11/17	DB
19	Docking HP audio test fail	35	Add C795 、 C796 to avoid DC level, and add R968 、 R969 to reduce HP out level	11/17	DB
20	Leakage problem	38	Correct direction preteck leakage	11/07	DB
21	EC pin define update	38	Delete EC_PME# 、 SYSON_PU 、 SUSP#_PU 、 LID_SW# change to +3VALW 、 Delete CLKRUN# 、 R582->@ for C0 chip 、 C1R_PU+5VL 、 add 100P to BATT_OVP(EC recommend)	11/07	DB
22	Can't Hibernation(SLP_S4#)	38	Connect SLP_S4# to SB	11/17	DB
23	EC can't receive docking present	40	CONA# change +3VL	11/12	DB
24	Reserve capacitor on digital MIC for EMI request	19	Add C496,C498	11/07	DB
25	Add 2N7002 to GND on HDMI to avoid leakage.	21	Add Q74	01/04	SI
26	+VDD_MEM18 to +1.8VS, change to jummpers	22	Delete R1124,R1125 add PJP605	01/04	SI
27	HDCP ROM fail. HDCP_SCL need pull high.	22	R224 no stuff. R213 stuff.	01/04	SI
28	Reserve capacitor on digital MIC for SED. WWAN noise	26	Add C499,C502	01/04	SI

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					LA-4102P Blade discrete
				Date	Monday, February 25, 2008
				Sheet	52 of 53
				Rev	0.4

Item	Fixed Issue (Reason for change)	PAGE	Modify List	Date	Phase
1	Change transformer vendor	30	change U19 library	01/04	SI
2	XMIT_OFF add a diode to avoid leakage.	31	Add D88	01/04	SI
3	Card reader recommend	32	XD_ALE need pull +3VS not pull low.	01/04	SI
4	change Q54 from transistor to MOS for cardreader LED.	32	Change Q54	01/04	SI
5	speaker pop issue	35	Change C1488 to 1U	01/04	SI
6	Reserve capacitor on SPI_FSEL#,CLK#,FER for EMI request	36	Add C2125,C2126,C2127	01/04	SI
7	Change EC_PME pull high from +3VL to +3VALW	38	R585 stuff	01/04	SI
8	Reserve damping resistor on SPI_CLK for EMI request	38	Add R191	01/04	SI
9	WLAN LED issue,WL_BLUE_LED# pull +3VS	39	Add R716	01/04	SI
10	Add bypass capacitance on sensor bottom	39	Add C261(4.7U)	01/04	SI
11	EC can't detect DOCK_PRESENT.	40	change R754 to 22 Ohm,R623 to 2K	01/04	SI
12	Add DOCK_VOL_UP#,DOCK_VOL_Down# pull +3VS	40	Add R594,R596	01/04	SI
13	SPDIF issue	40	follow Vader	01/04	SI
14	Docking CRT blurred	40	Change ping 31,39,22 connect to GND	01/04	SI
15	Change R650 and C770 to modify the power sequence	41	change R650 to 1K, C770 to 0.1u	01/04	SI
16	Add 12P on CLK_14M_ICh for WWAN noise	17	Add 12P on CLK_14M_ICh	02/15	PV
17	BKOFF# reserve pull low 10K	19	reserve R717	02/15	PV
18	Reserve CMD27 to support 64M X16	7,8	Reserve CMD27 to support 64M X16	02/15	PV
19	Reserve cap on HDA_BITCLK for WWAN noise issue	26	Reserve cap on HDA_BITCLK	02/15	PV
20	Reserve to prevent ESD issue	30	Reserve ESD diode on LAN LED pin	02/15	PV
21	Change WLAN and WWAN 0402 resistor to 0805	31	Change WLAN and WWAN 0402 resistor to 0805, and WLAN change to +3VS power plane	02/15	PV
22	Direct drive LED, and add D3E function diode	32	Direct drive LED and XD_ALE Pull L, and add D86 for D3E function	02/15	PV
23	Change R1092 value on BT power switch Gate	36	Change R1092 to 10K	02/15	PV
24	Correct AC_LED control by EC	38	AC_LED Change controll by EC	02/15	PV
25	Change all LED limit current resistor to 200 ohm	39	Change all LED limit current resistor to 200 ohm and add Touch pad LED for PR	02/15	PV
26	Add 33 ohm for MUTE_LED and DOCK_SLP_BTN#	40	Add 33 ohm for MUTE_LED and DOCK_SLP_BTN#	02/15	PV
27	follow check list ver:1.5	6	change R13 to 56 ohm;change R2~R8 to 51 ohm;change R11 to 0ohm	02/20	PV
28	Reserve Cap for EMI	42	add C1250,C1249	02/20	PV

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				Date	Monday, February 25, 2008
				Sheet	53 of 53
				Rev	0.4

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