

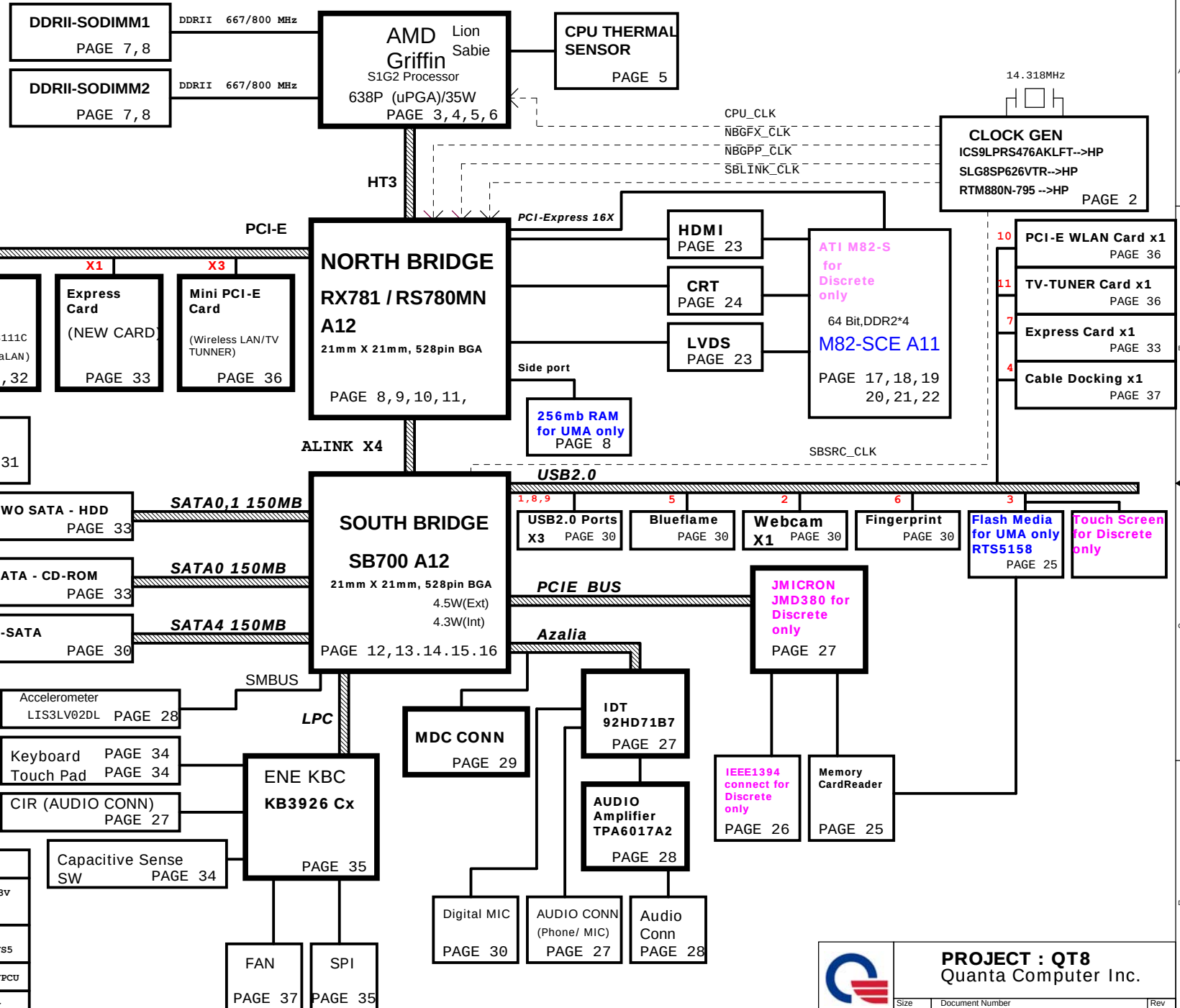
QT8 SYSTEM DIAGRAM



01

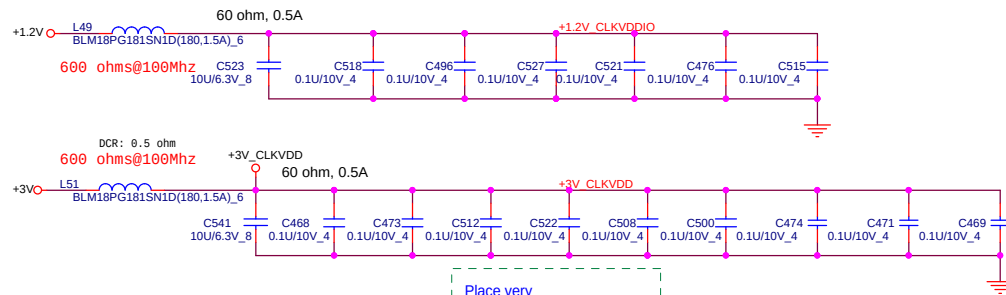
PCB STACK UP

LAYER 1 : TOP
LAYER 2 : IN1
LAYER 3 : IN2
LAYER 4 : VCC
LAYER 5 : IN3
LAYER 6 : BOT

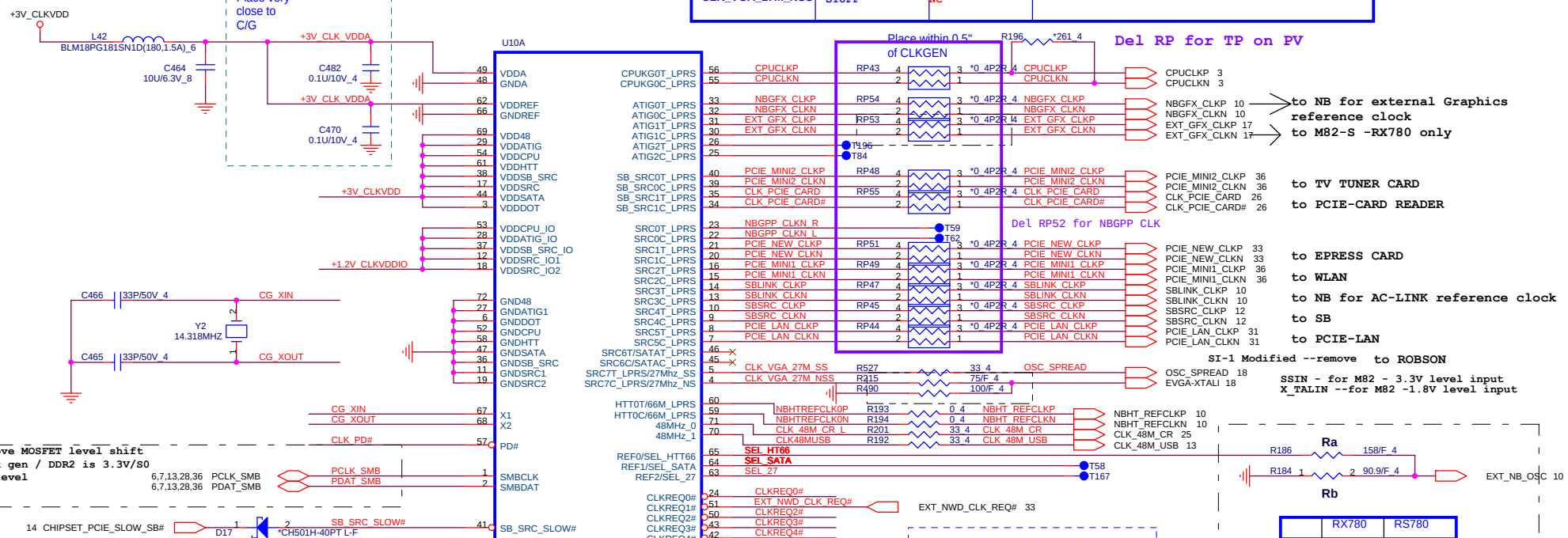


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Size Custom	Document Number	Rev 1A
	Block Diagram	
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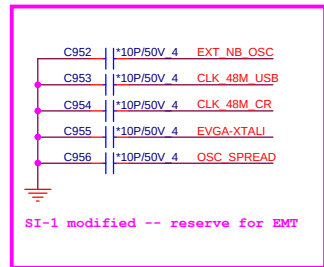


CLOCKS name	RX780	RS780	Clock pin function
NBGF_X_CLKP NBGF_X_CLKN	RP64 STUFF	RP64 STUFF	to NB for VGA reference clock
EXT_GFX_CLKP EXT_GFX_CLKN	RP66 STUFF	RP66 NC	to M82-S external reference clock -RX780 only
NBGP_P_CLKP NBGP_P_CLKN	RP70 STUFF	RP70 NC	to NB for RX780 for PCIEX2 interface reference clock only RS780 is internal share with AC-LINK clock, RS780 not need
SBLINK_CLKP SBLINK_CLKN	RP72 STUFF	RP72 STUFF	to NB for AC-LINK reference clock
CLK_VGA_27M_SS CLK_VGA_27M_NSS	R653, R656, R612 STUFF	R653, R656, R612 NC	To M82-S 27Mhz - RX780 only

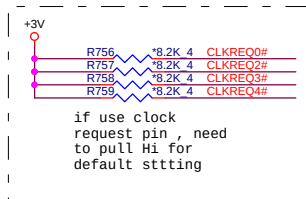


can remove MOSFET level shift
SB/clock gen / DDR2 is 3.3V/80
power level

when driven lowSB_SRC clocks slow only supported with
to reduced setpoint custom CG IC



SI-1 modified -- reserve for EMT



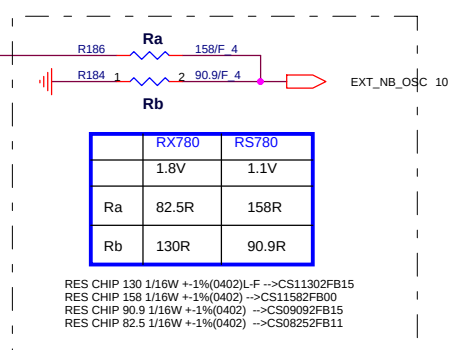
if use clock
request pin, need
to pull Hi for
default setting

ICS ICS9LPR476BKLFT--AJRS4760000
SLG SLG8SP626VTR--AJ006260000
RTL RTM880N-795-- AJ008800000

* default

SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1	100 MHz non-spreading differential SRC clock
	0*	100 MHz spreading differential SRC clock
SEL_27	1*	27MHz non-spreading singled clock
	0	100 MHz spreading differential SRC clock

Clock chip has internal serial
terminations
for differential pairs, external resistors
are reserved for debug purpose.

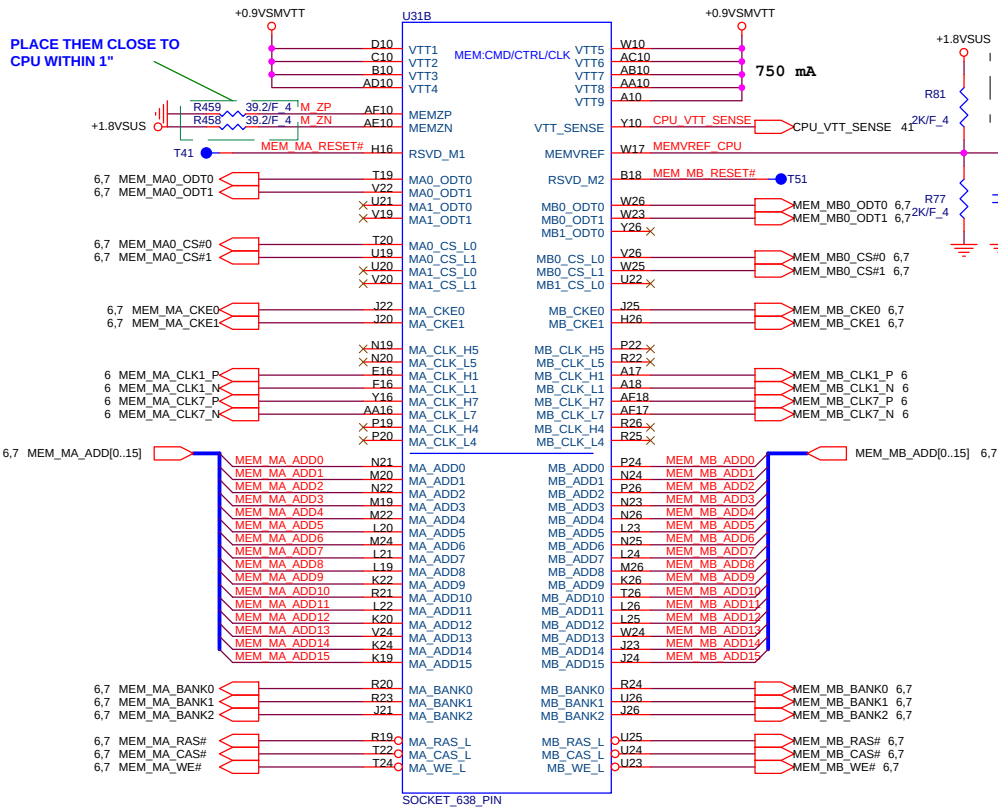


RES CHIP 130 1/16W +-1%(0402)-L-F -->CS11302FB15
RES CHIP 158 1/16W +-1%(0402) -->CS11582FB00
RES CHIP 90.9 1/16W +-1%(0402) -->CS09092FB15
RES CHIP 82.5 1/16W +-1%(0402) -->CS08252FB11

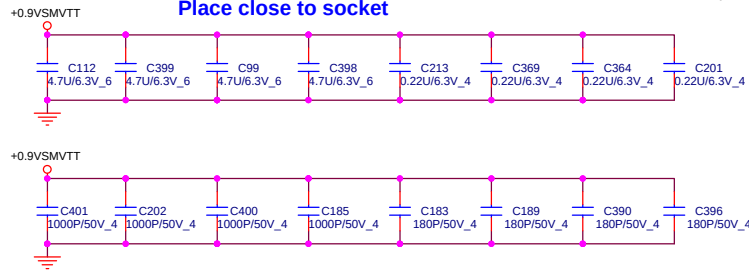


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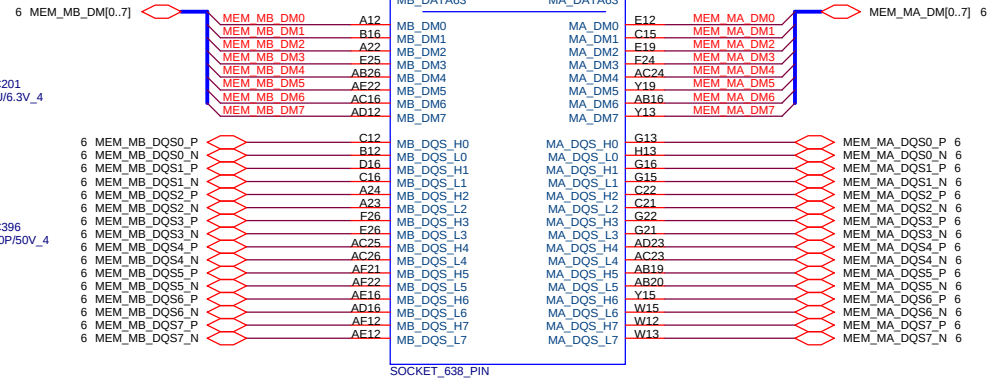
Processor Memory Interface

PLACE THEM CLOSE TO
CPU WITHIN 1"

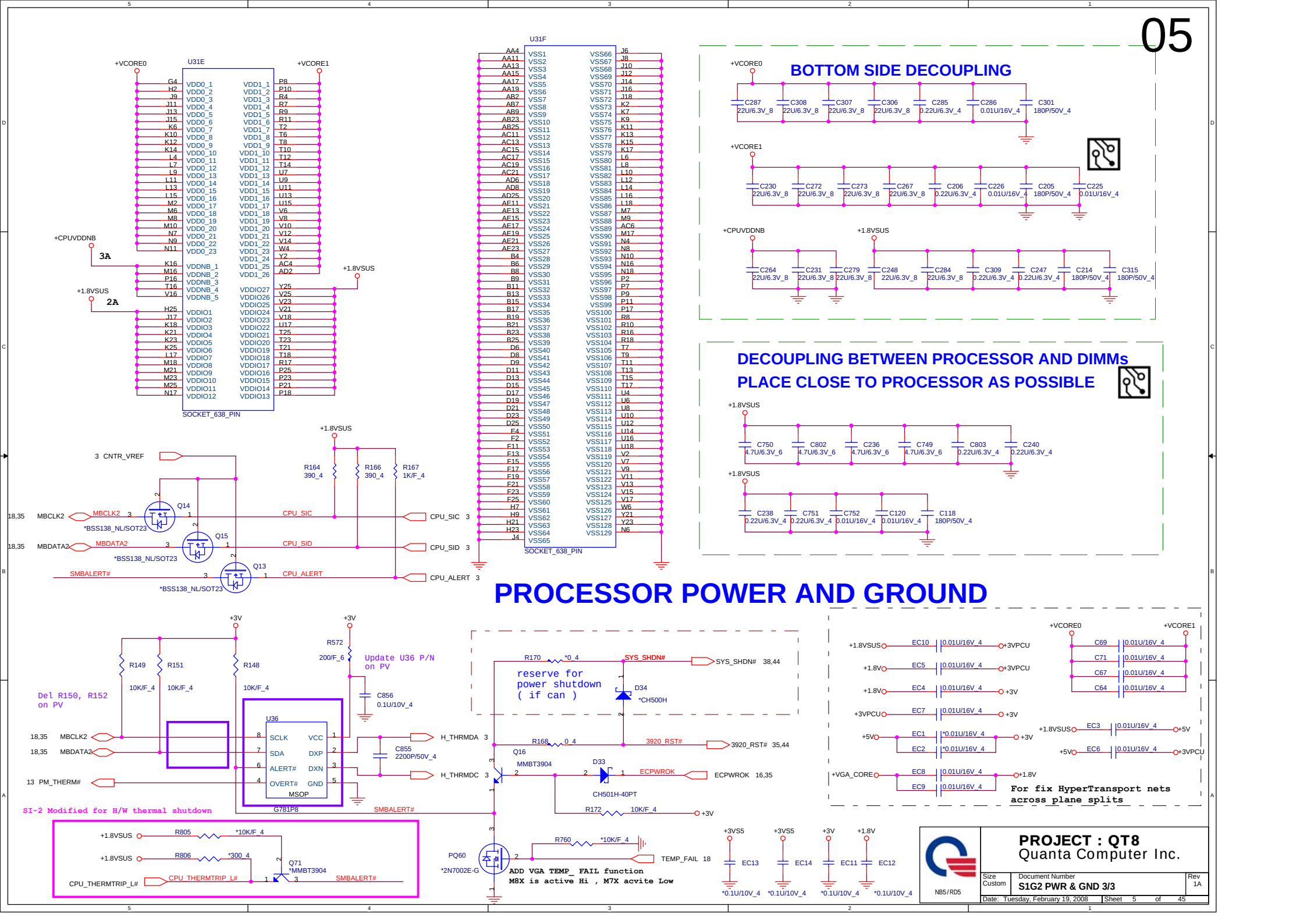
Place close to socket



Close to CPU within 1500 mils



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05

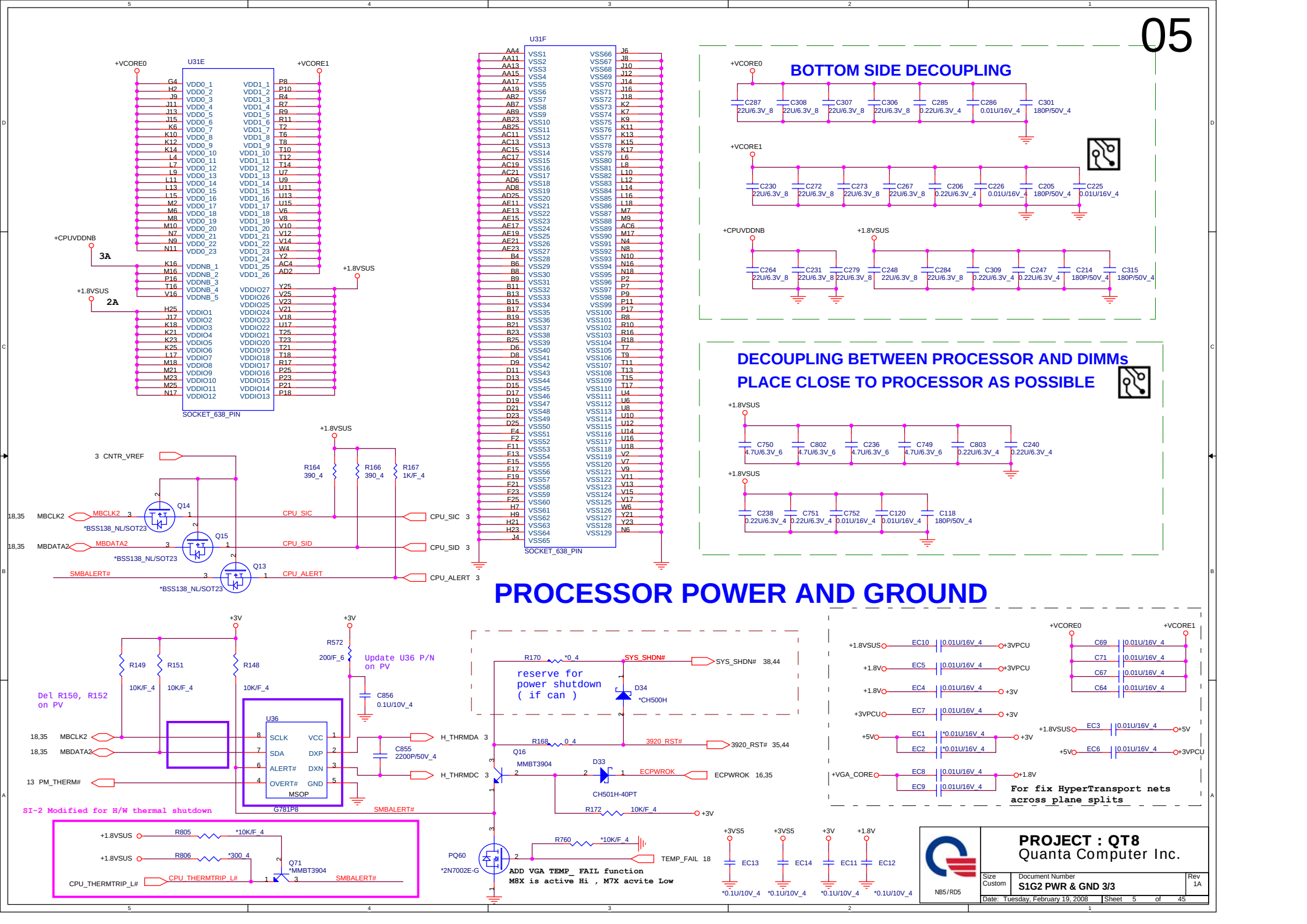
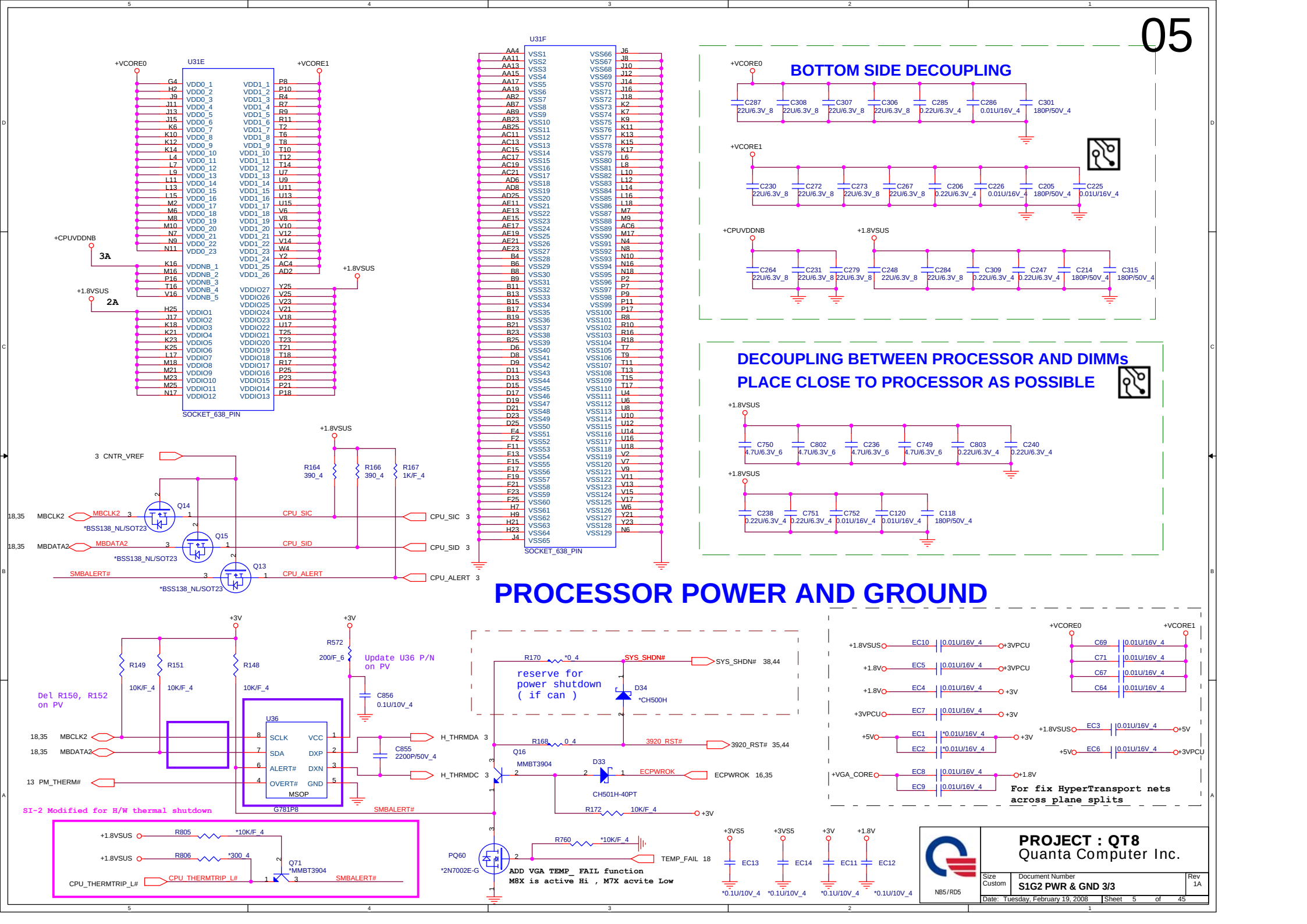
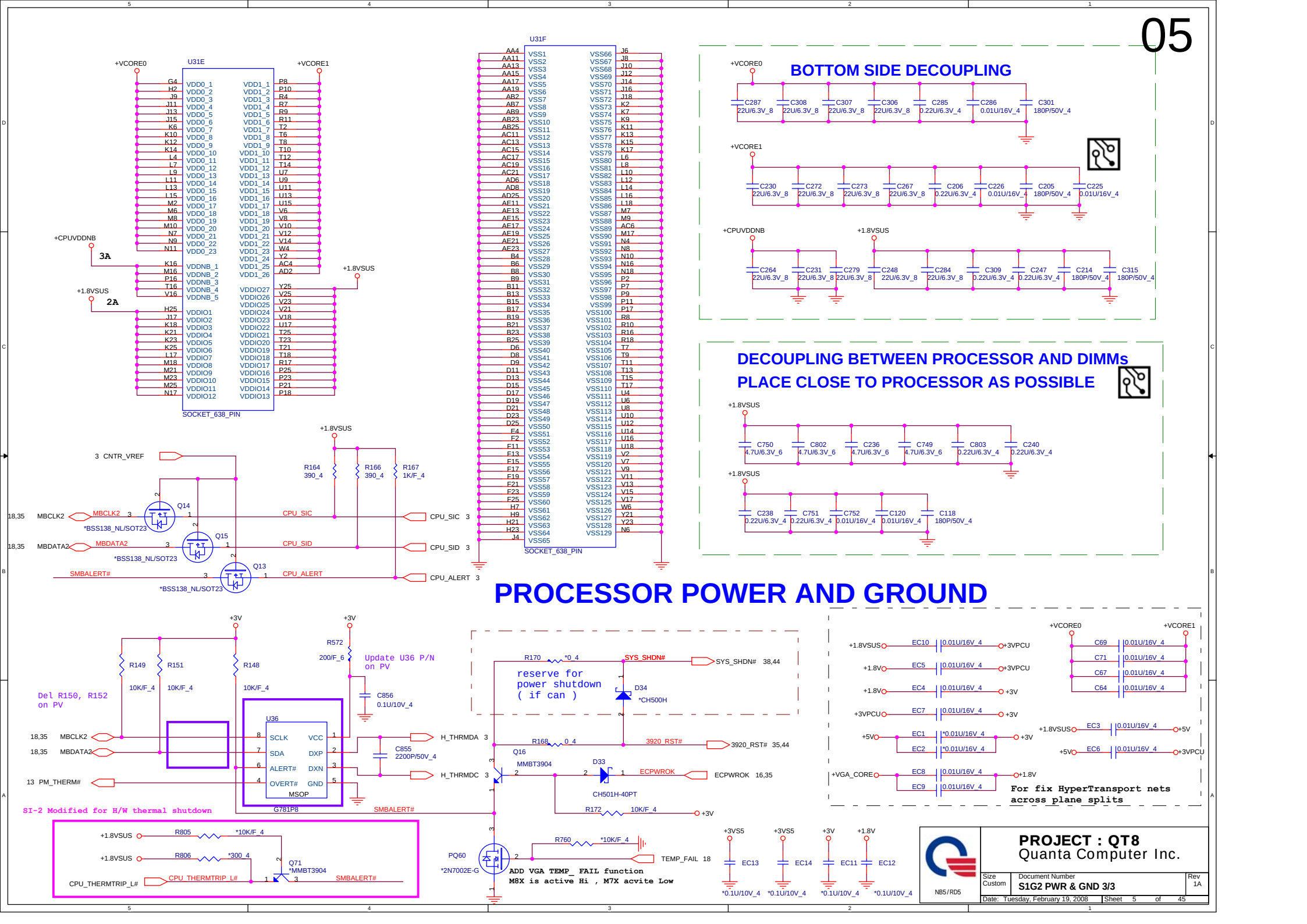
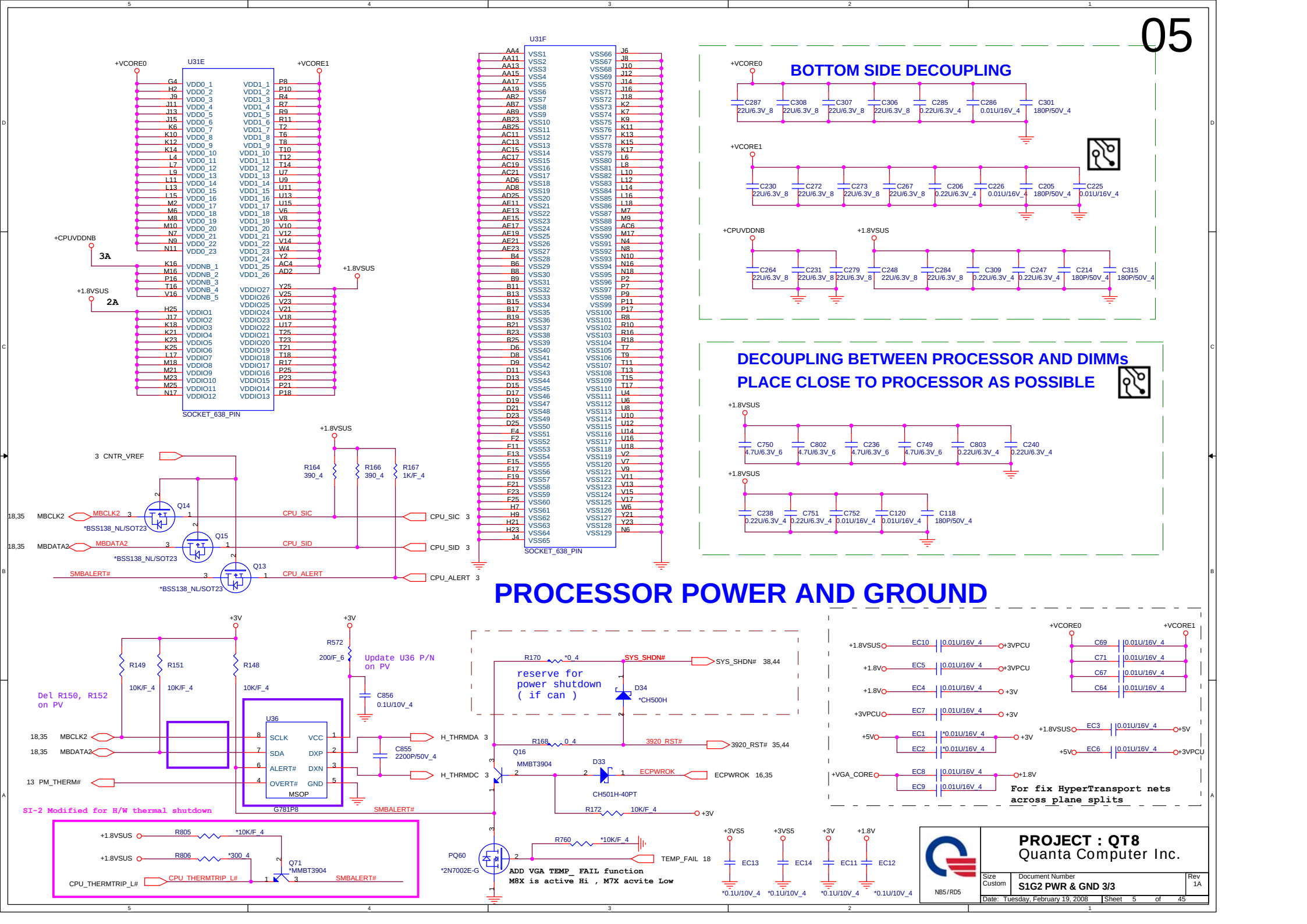
PROCESSOR POWER AND GROUND

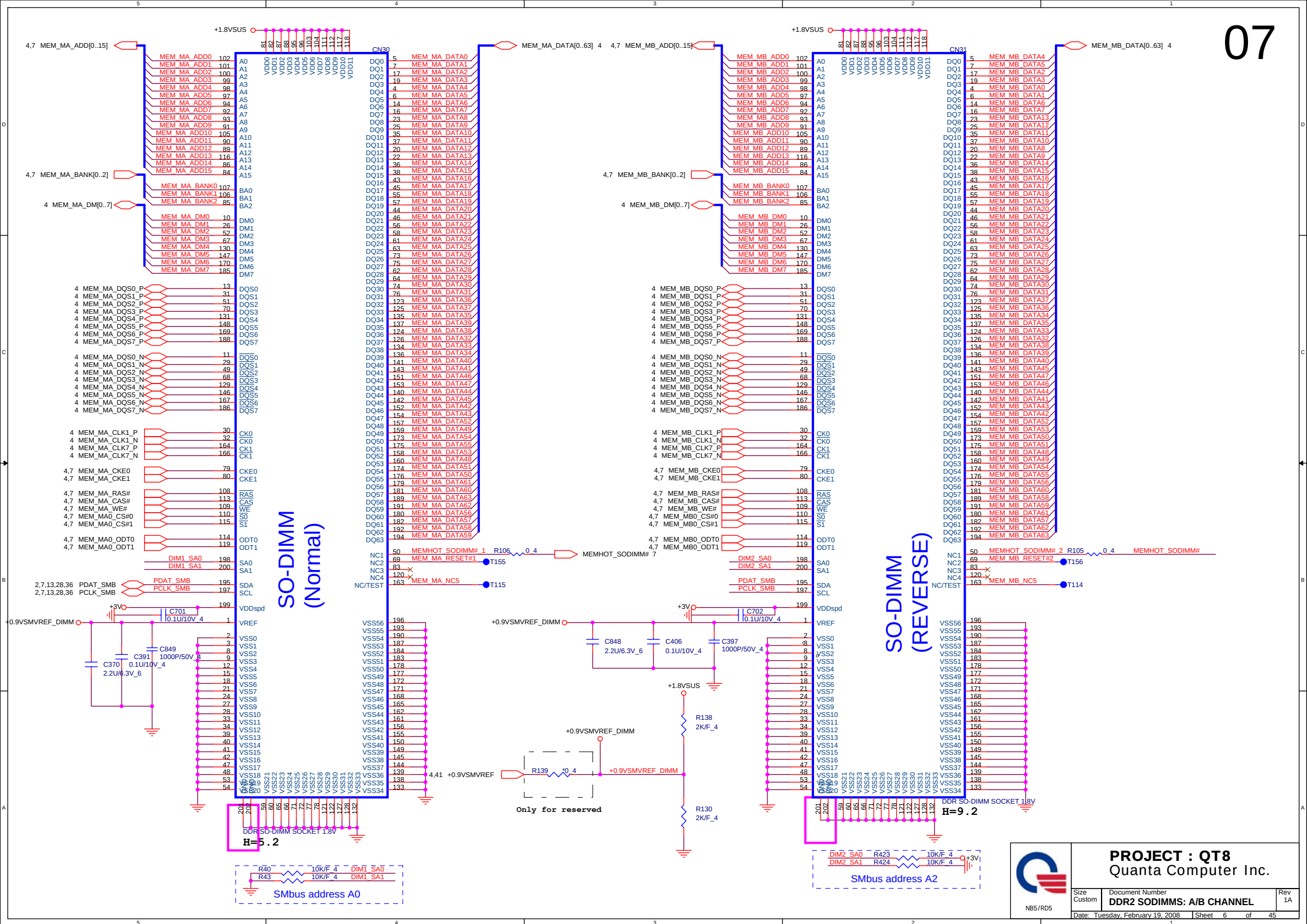
BOTTOM SIDE DECOUPLING

DECOUPLING BETWEEN PROCESSOR AND DIMMs
PLACE CLOSE TO PROCESSOR AS POSSIBLE

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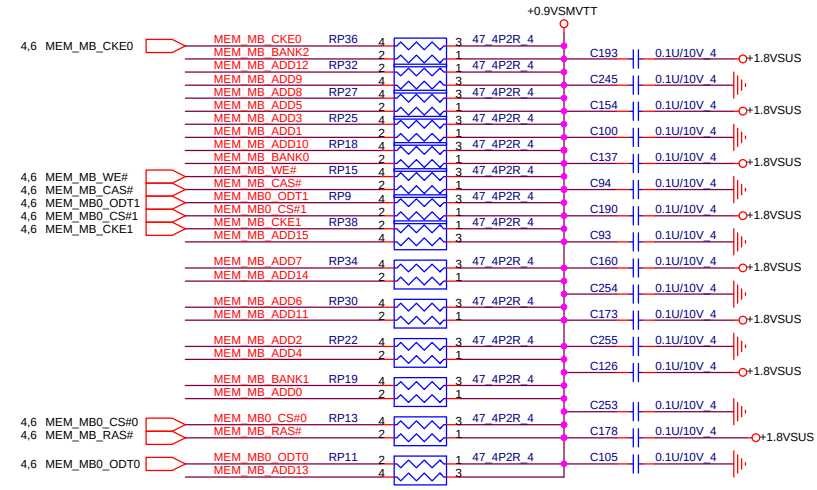
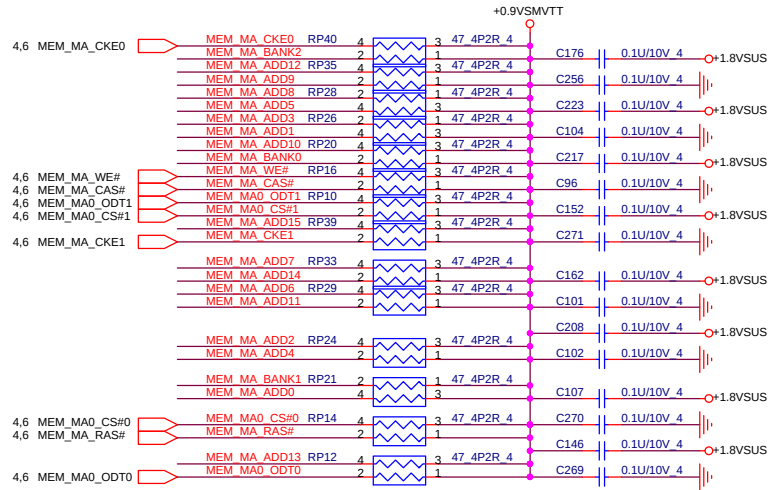
Size Custom Document Number S1G2 PWR & GND 3/3 Rev 1A
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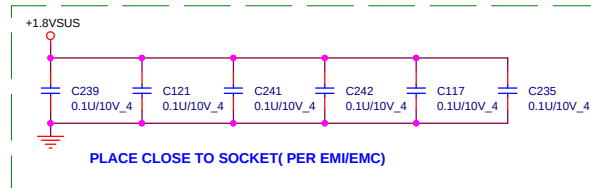


4,6 MEM_MA_ADD[0..15]  MEM_MA_ADD[0..15]
4,6 MEM_MA_BANK[0..2]  MEM_MA_BANK[0..2]

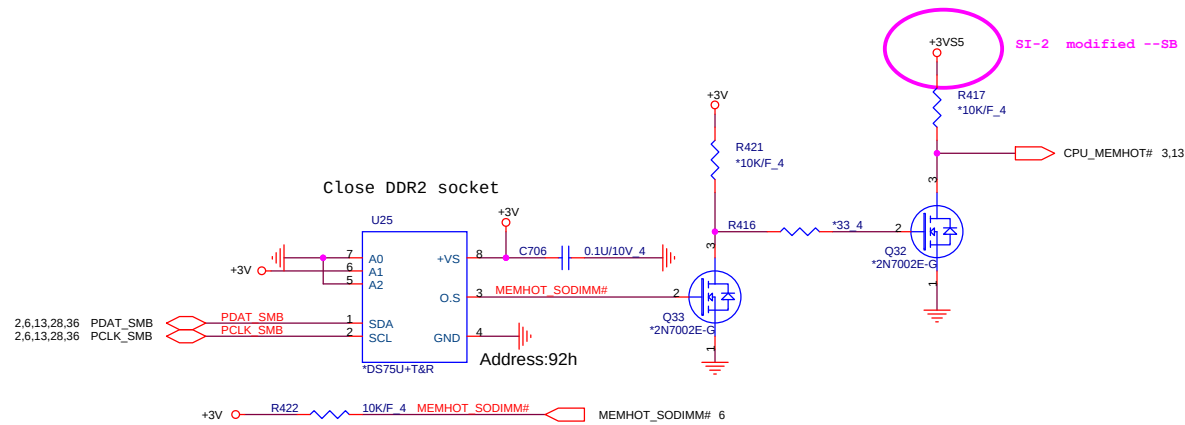
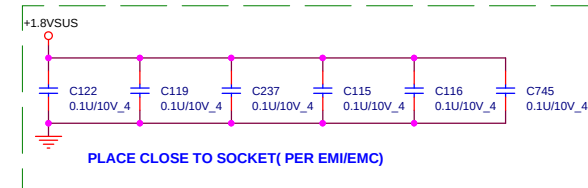
4,6 MEM_MB_ADD[0..15]  MEM_MB_ADD[0..15]
4,6 MEM_MB_BANK[0..2]  MEM_MB_BANK[0..2]



PLACE CLOSE TO PROCESSOR
WITHIN 1.5 INCH

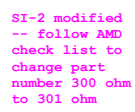


PLACE CLOSE TO PROCESSOR
WITHIN 1.5 INCH



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NB5/RD5		
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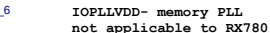
```
RES CHIP 1.21K 1/16W +-1%(0402)
P/N : CS21212FB18
```



```
RES CHIP 301 1/16W +-1%(0402)
P/N : CS13012FB14
```

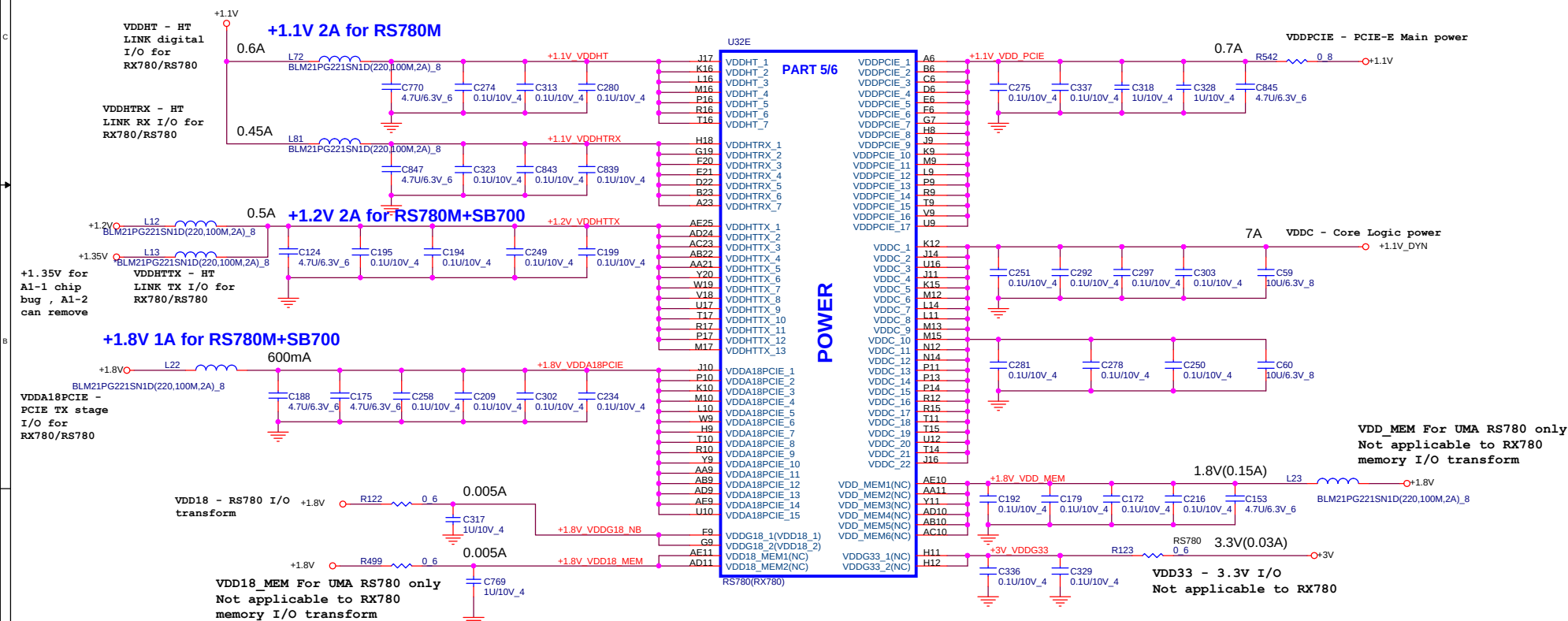


	U3D2	PAR
2	MEM_A0(NC)	
6	MEM_A1(NC)	
1	MEM_A2(NC)	
5	MEM_A3(NC)	
2	MEM_A4(NC)	
6	MEM_A5(NC)	
4	MEM_A6(NC)	
3	MEM_A7(NC)	
4	MEM_A8(NC)	
5	MEM_A9(NC)	
6	MEM_A10(NC)	
3	MEM_A11(NC)	
4	MEM_A12(NC)	
4	MEM_A13(NC)	
6	MEM_BA0(NC)	
7	MEM_BA1(NC)	
7	MEM_BA2(NC)	
2	MEM_CASb(NC)	
3	MEM_CASb(NC)	
8	MEM_WEB(NC)	
8	MEM_CbS(NC)	

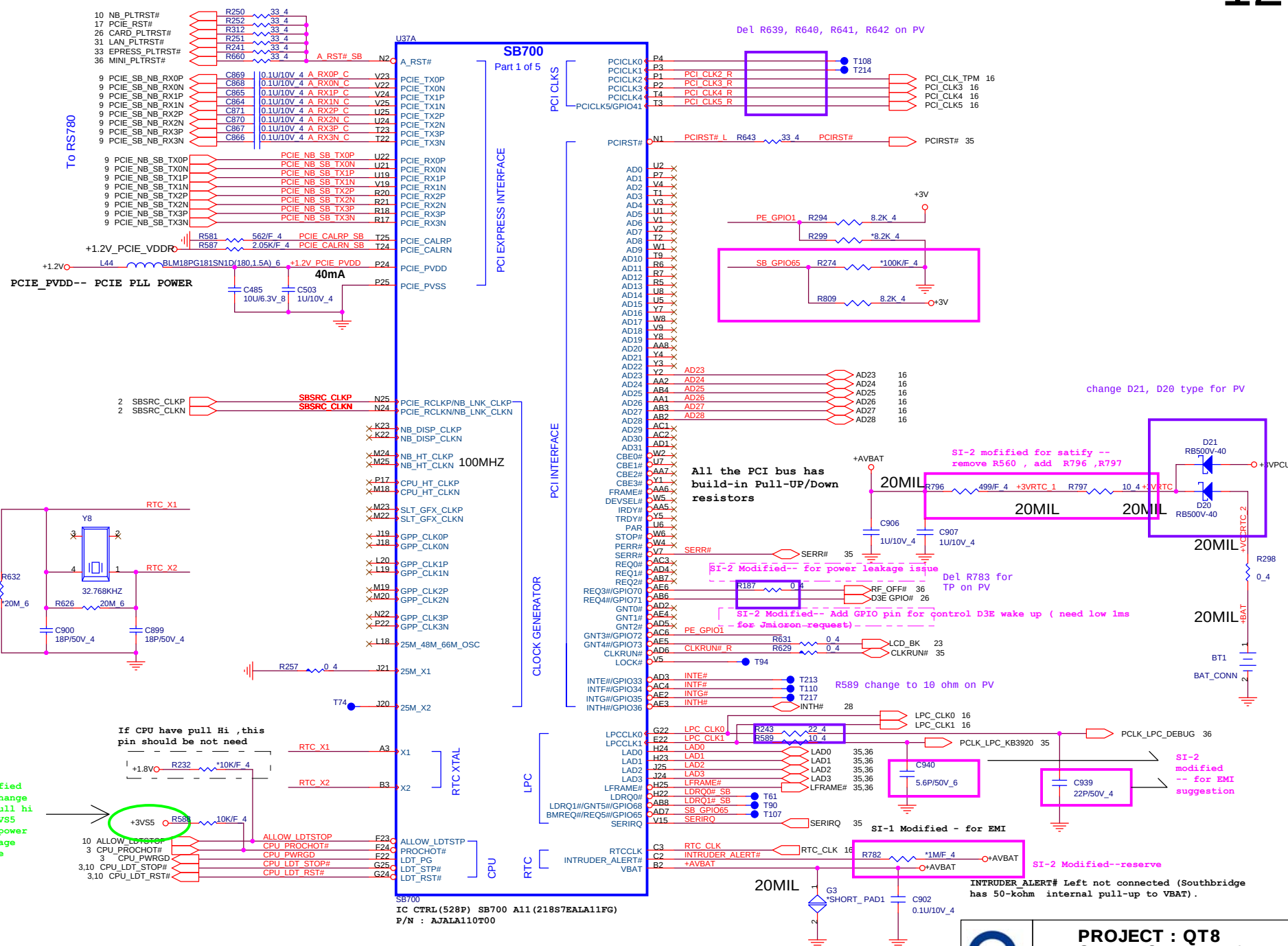


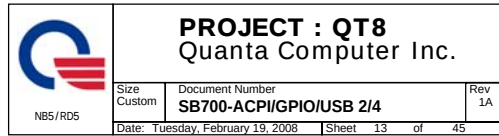
RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RX780	RS780	PIN NAME	RX780	RS780
VDDHT	+1.1V	+1.1V	IOPLLVD	NC	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	NC	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	NC	+1.8V
VDDG18	+1.8V	+1.8V	PLLVD	NC	+1.1V
VDD18_MEM	NC	+1.8V	PLLVD18	NC	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	NC	+1.8V/1.5V	VDDLTP18	NC	+1.8V
VDDG33	NC	+3.3V	VDDL18	NC	+1.8V
IOPLLVD18	NC	+1.8V	VDDL133	NC	NC



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SATA PORT 0,1,2,3
can support AHCI
mode

PLACE SATA AC COUPLING
CAPS CLOSE TO SB600

SATA1

SATA ODD

E-SATA

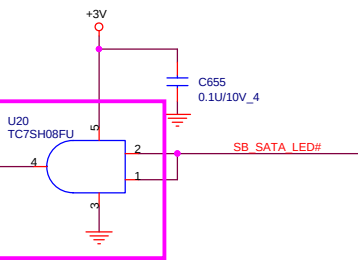
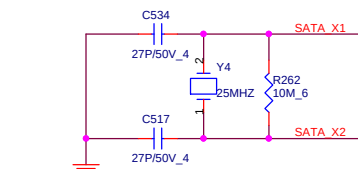
SATA PORT 4,5 are
only support IDE
mode

SATA PORT 4,5 are
only support IDE
mode

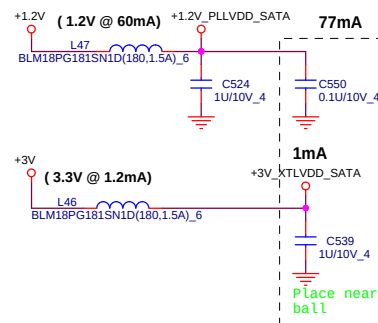
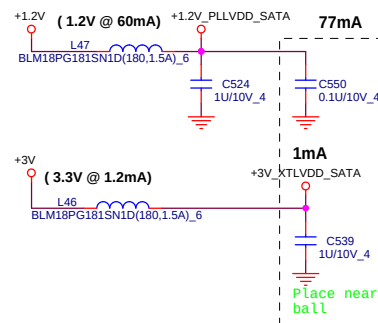
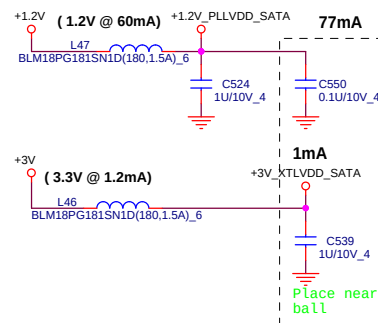
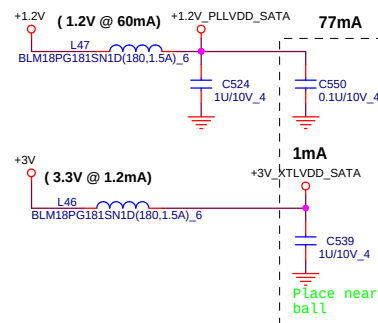
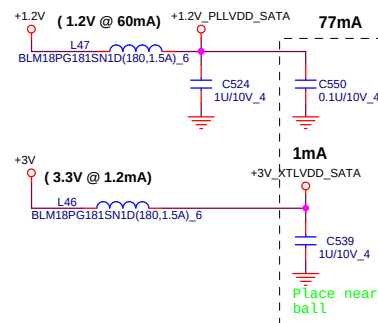
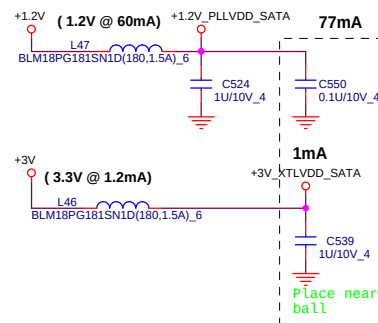
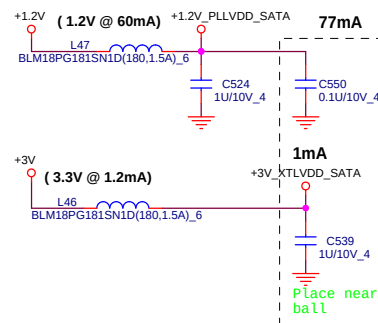
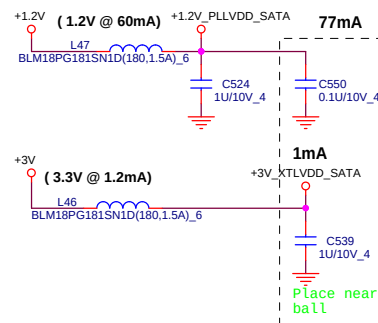
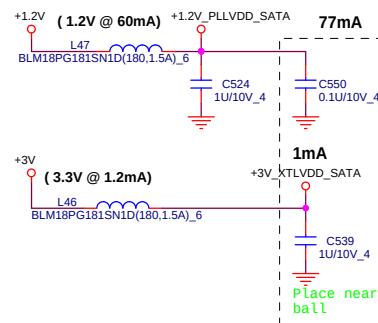
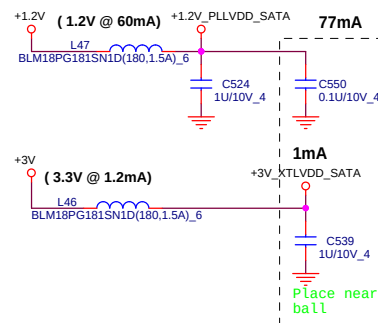
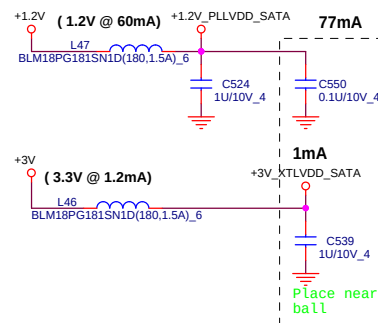
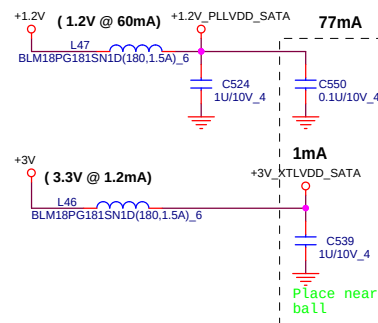
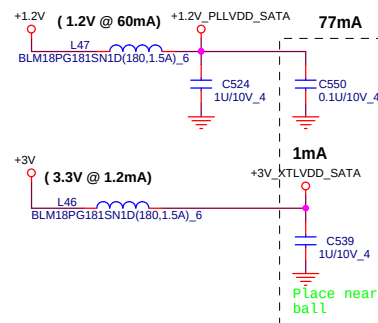
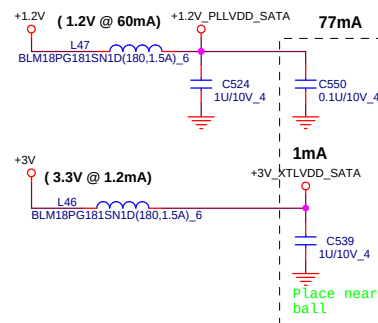
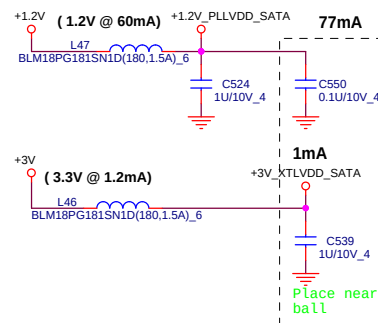
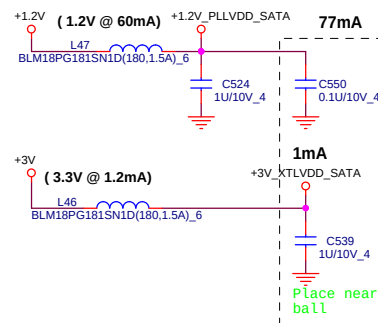
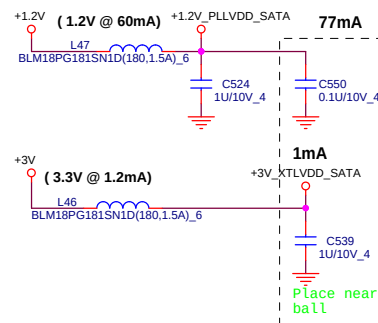
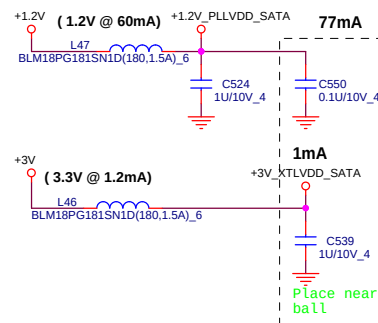
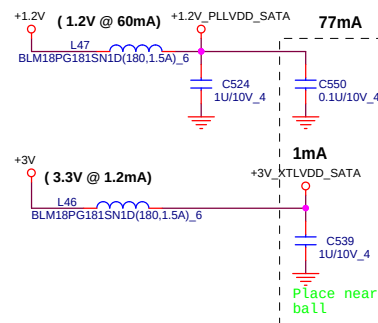
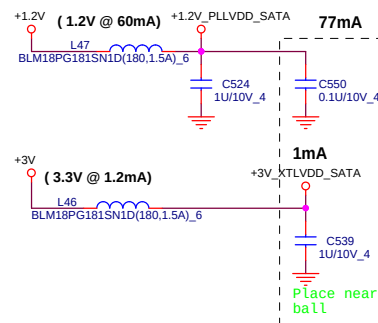
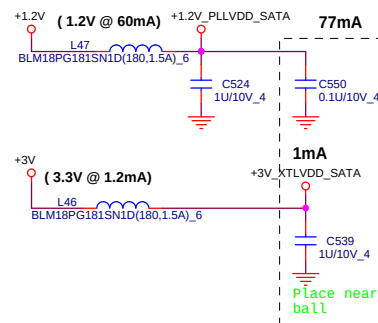
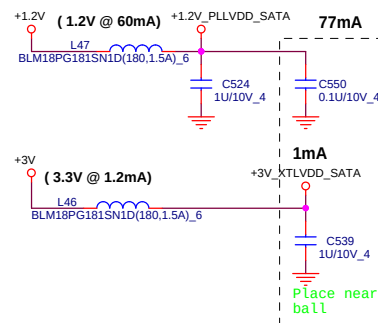
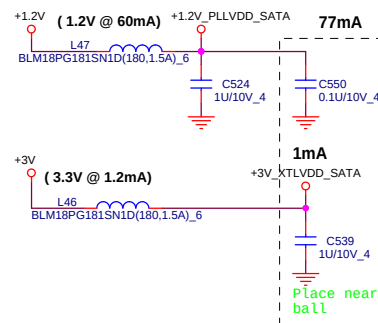
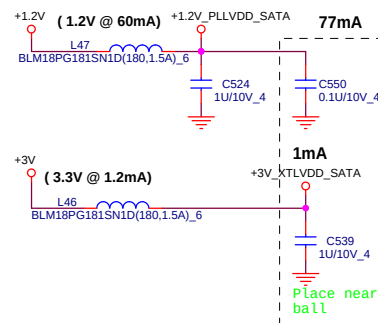
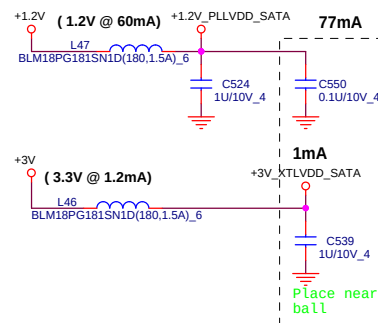
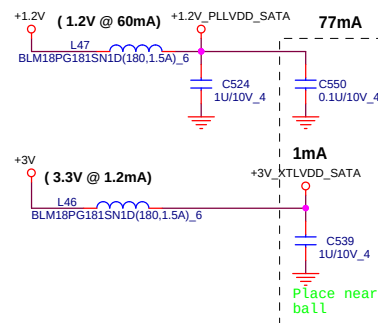
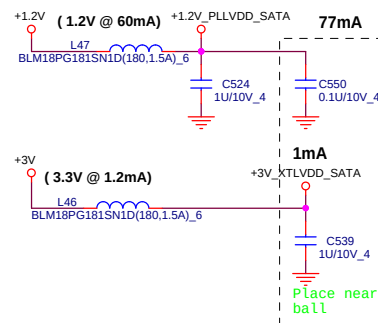
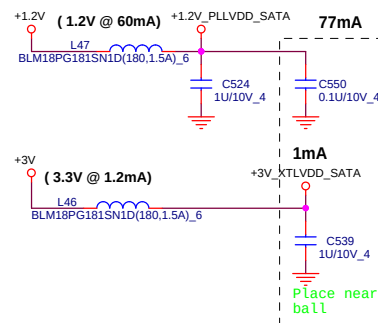
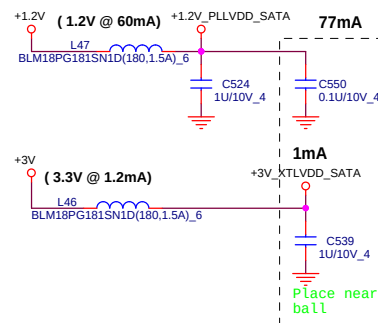
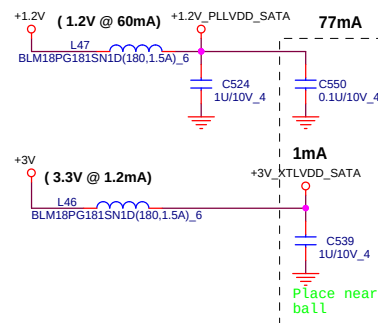
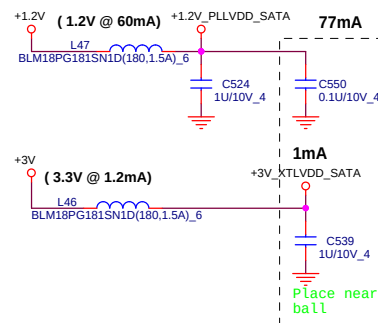
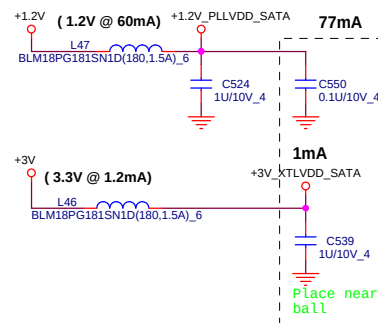
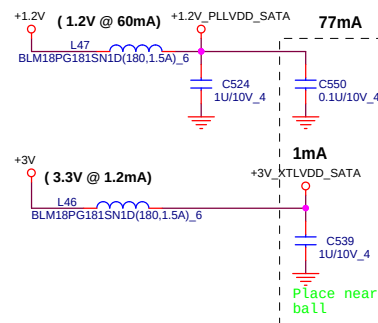
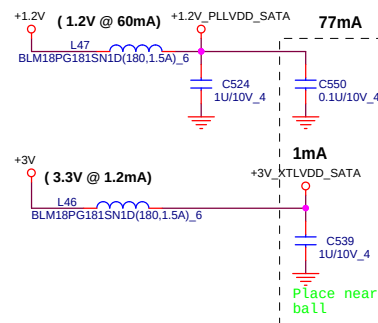
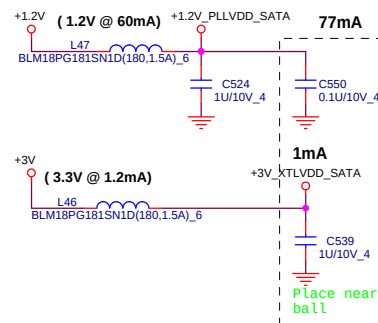
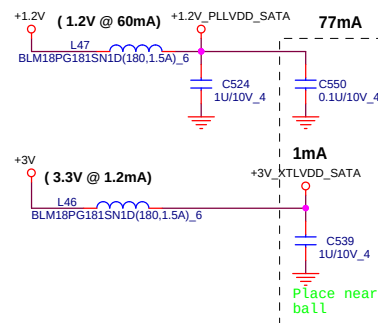
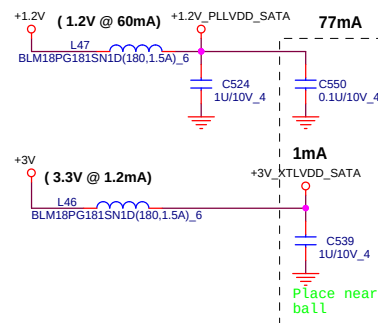
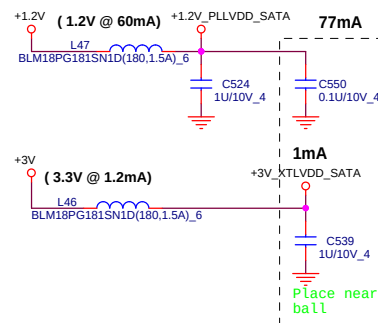
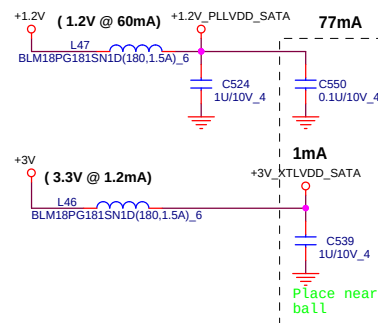
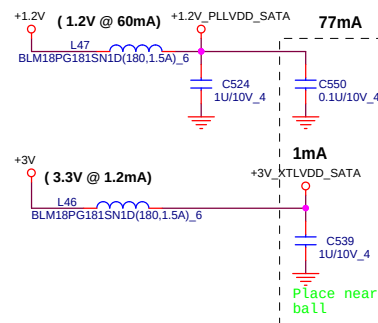
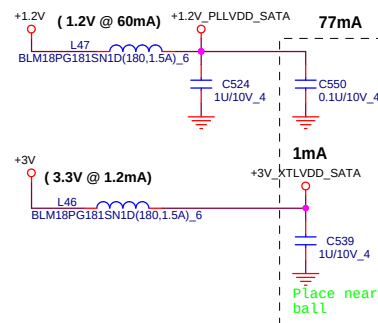
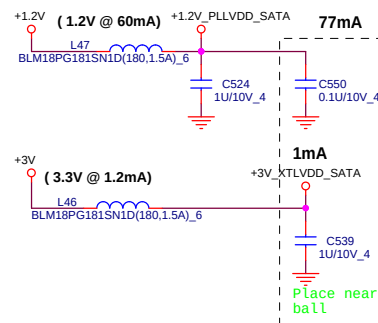
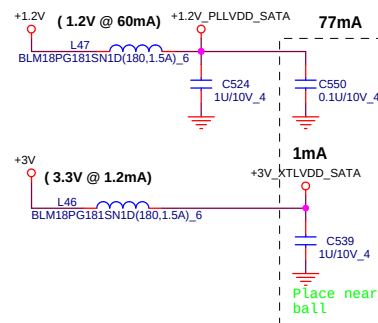
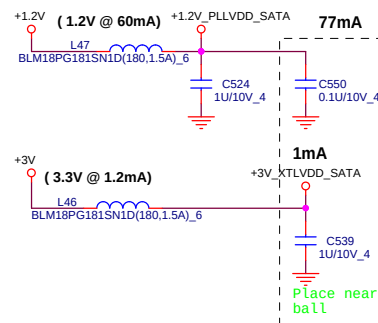
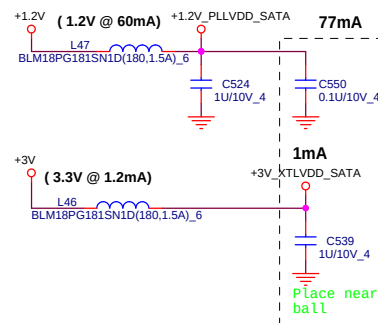
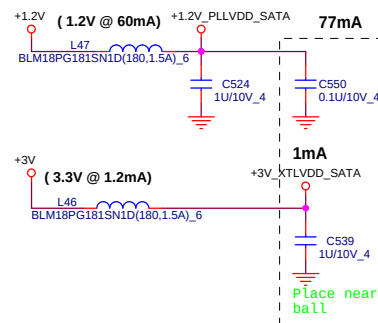
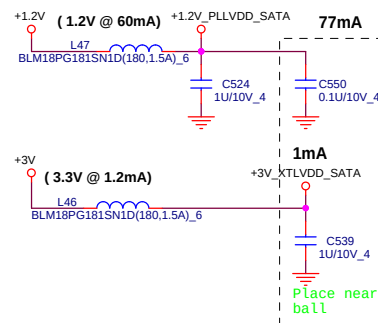
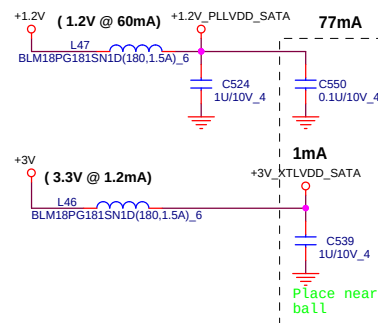
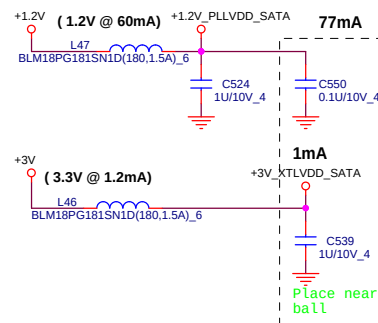
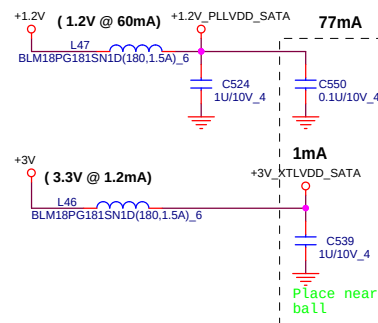
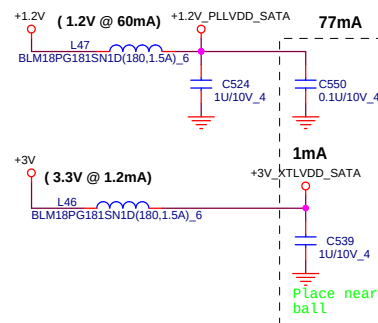
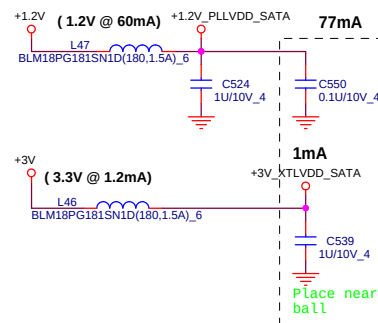
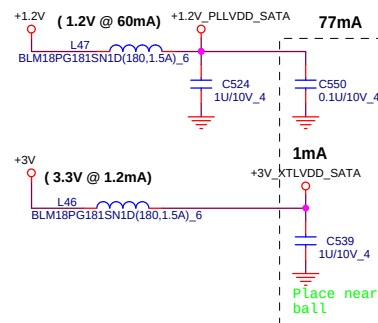
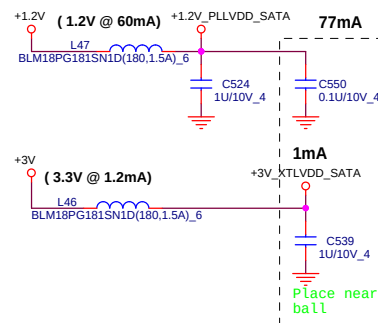
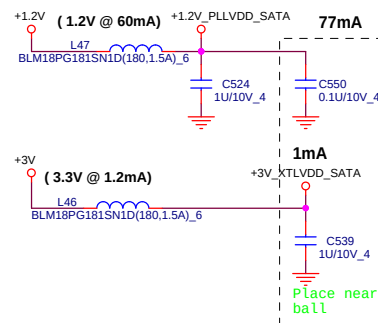
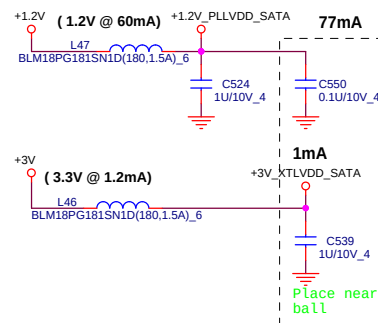
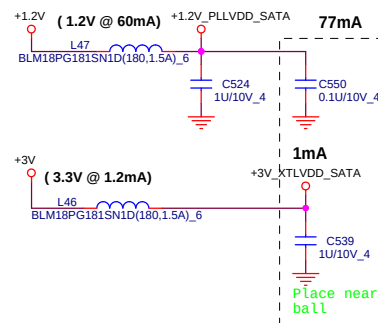
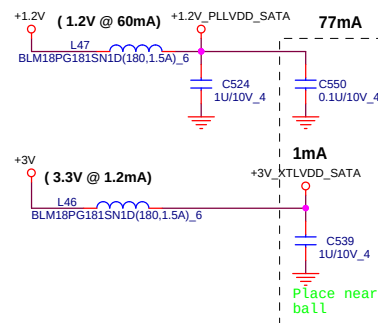
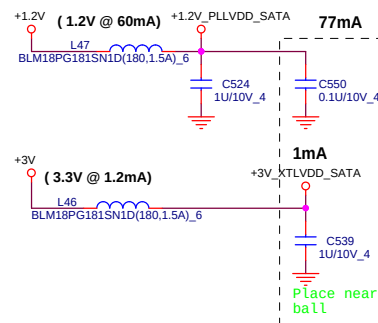
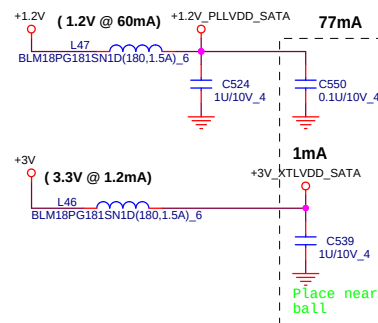
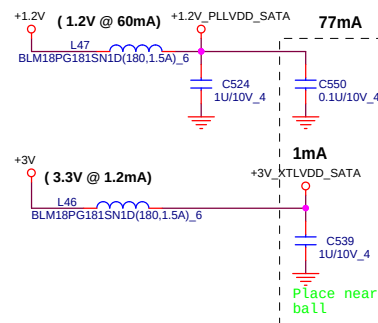
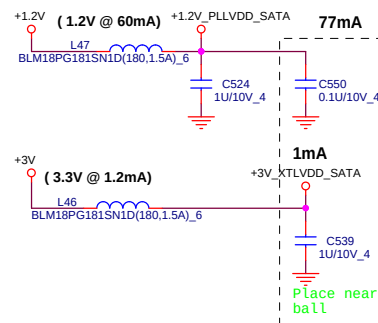
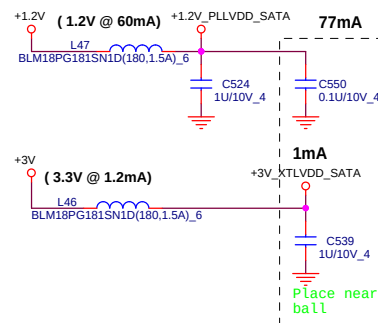
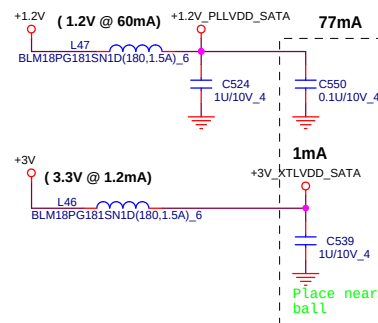
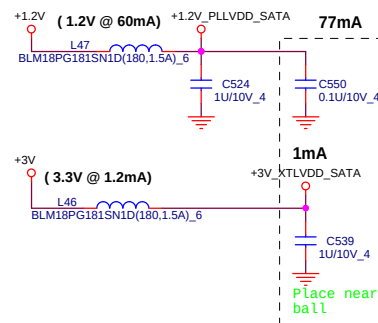
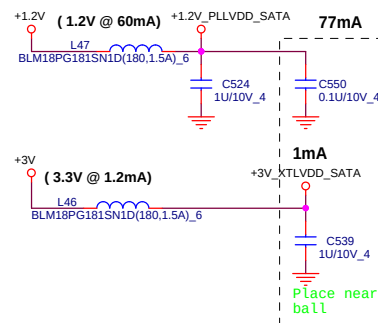
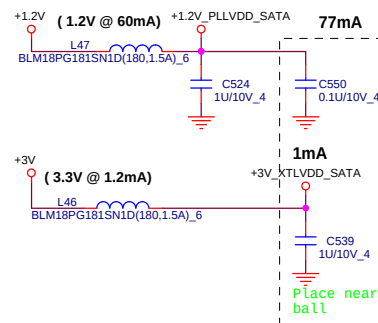
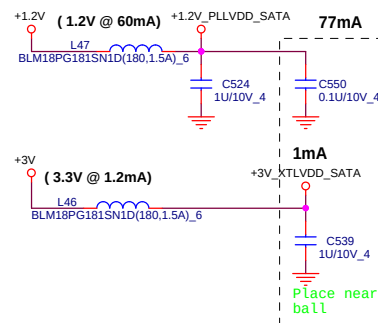
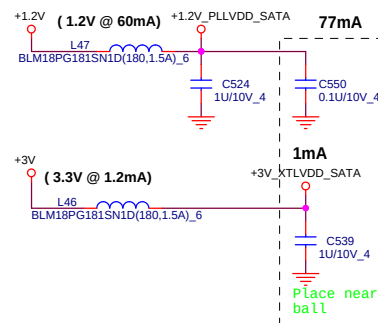
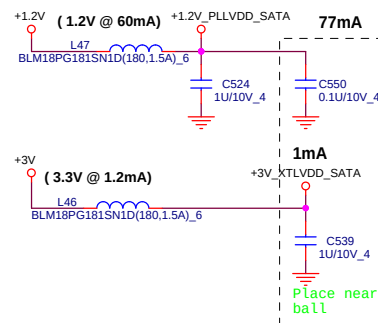
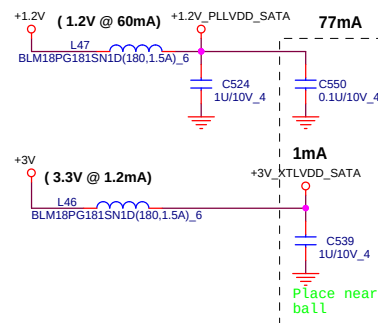
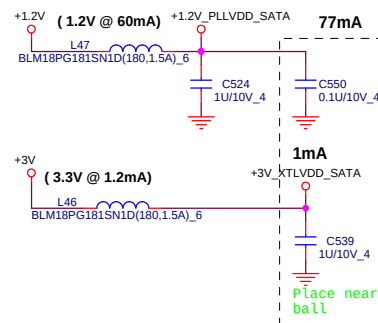
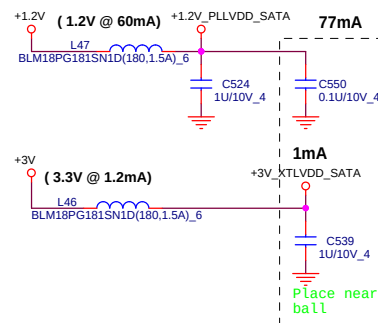
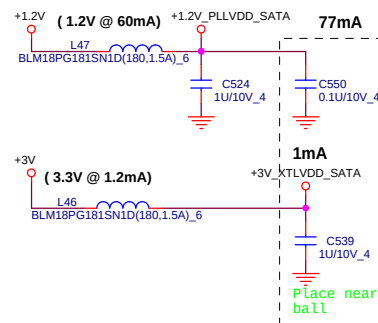
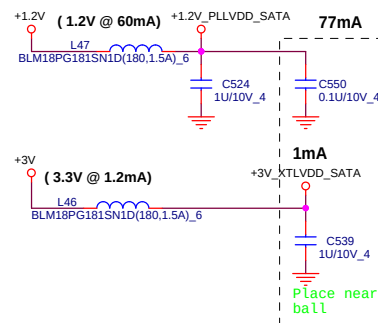
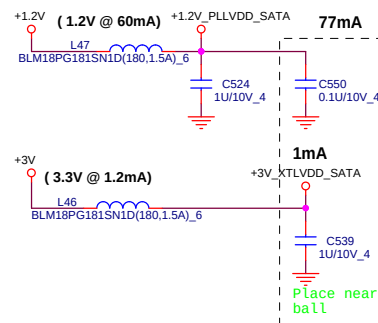
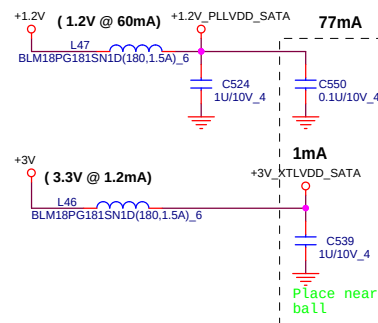
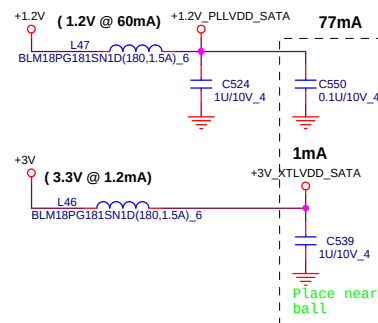
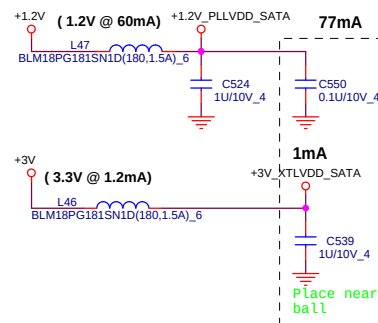
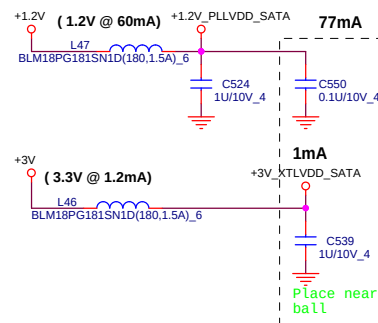
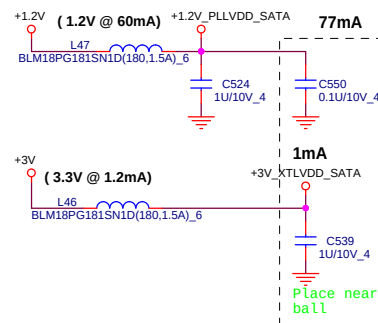
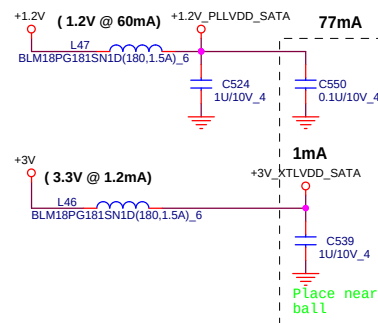
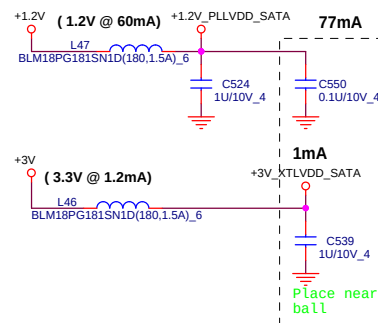
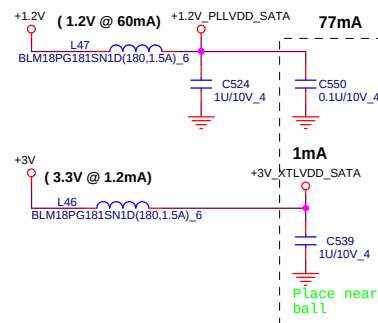
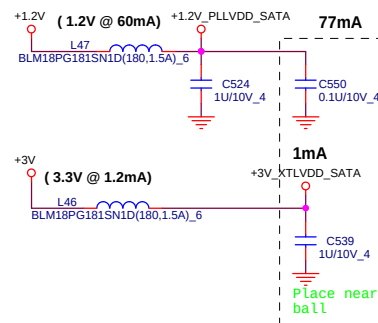
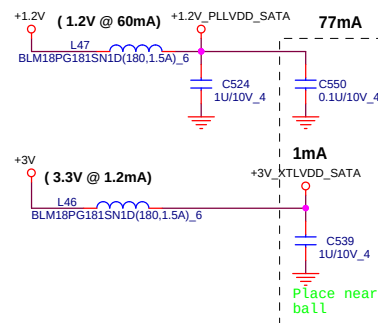
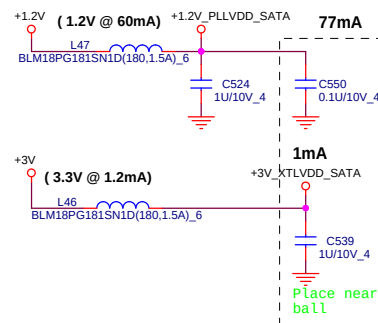
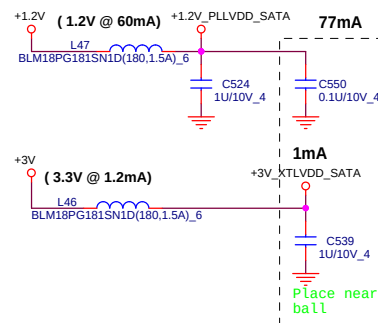
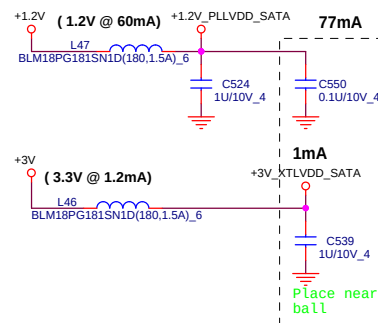
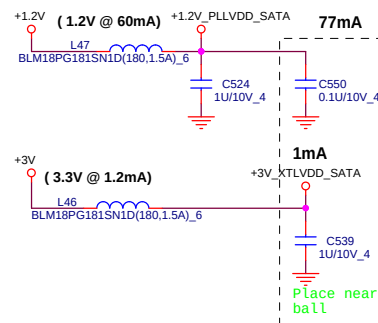
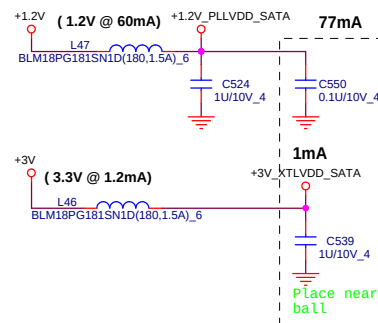
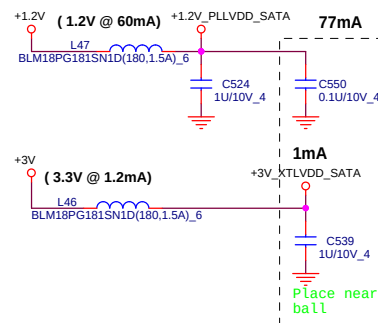
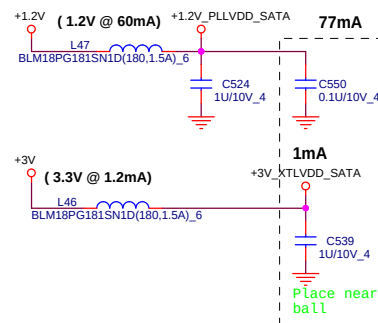
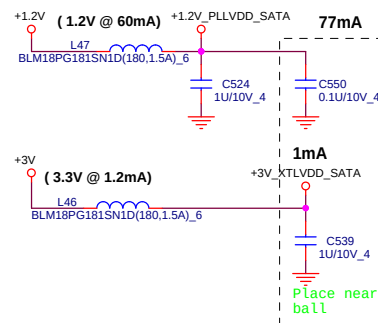
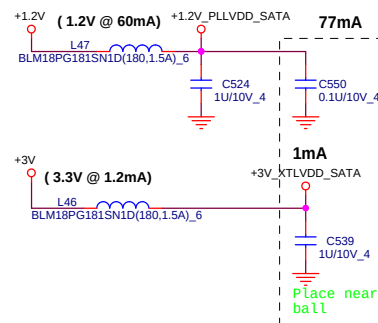
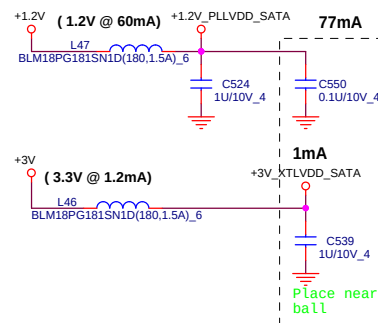
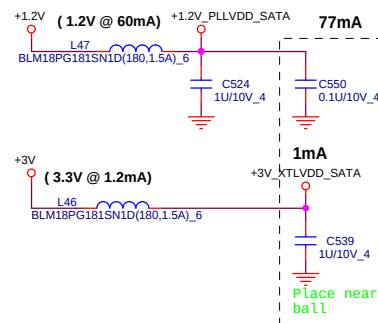
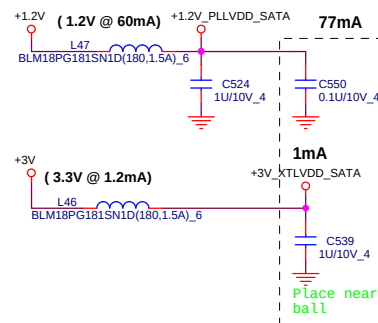
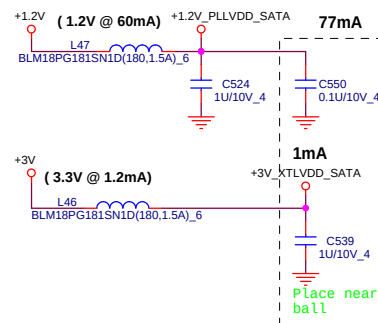
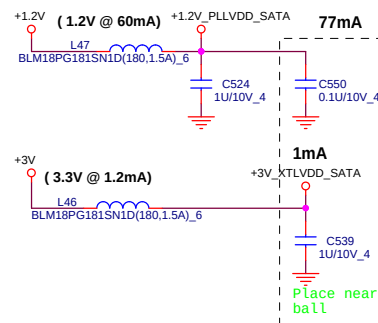
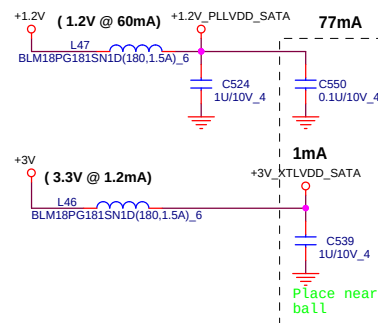
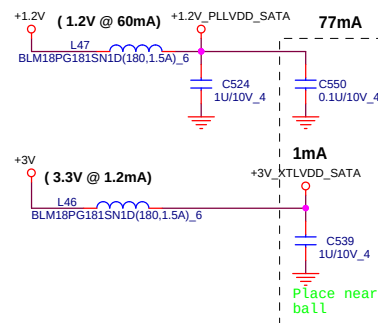
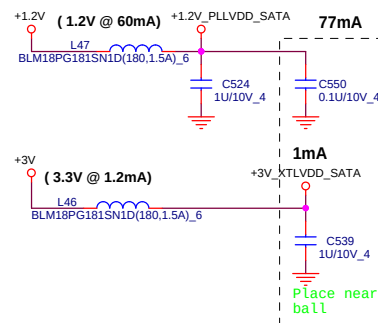
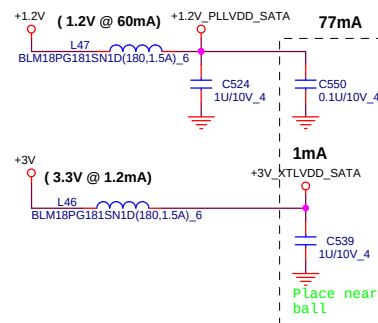
NOTE:
R361 IS 1K 1% FOR 25MHz
XTAL, 4.99K 1% FOR 100MHz
INTERNAL CLOCK

PLVDD_SATA--
SATA PLL
POWER

XTLVDD_SATA-- SATA
crystal power

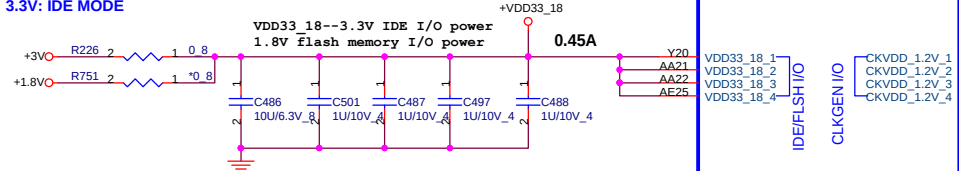


SI-2 modified for SATA LED fail issue



1.8V : FLASH MEMORY MODE(DEFAULT)

1.8V : FLASH MEMORY MODE(DEFAULT)
3.3V: IDE MODE



PCIE_VDDR--PCIE I/O power

+1.2V_0 L89

844mA

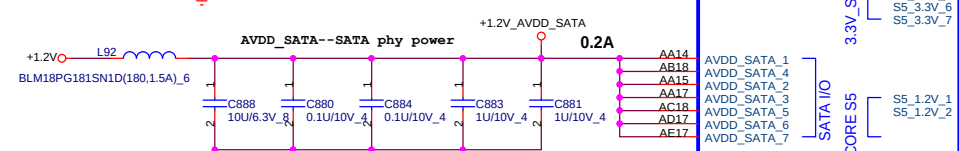
PCIE_VDDR_1
PCIE_VDDR_2
PCIE_VDDR_3
PCIE_VDDR_4
PCIE_VDDR_5
PCIE_VDDR_6
PCIE_VDDR_7

A-LINK I/O

S5_3.3V_1
S5_3.3V_2
S5_3.3V_3
S5_3.3V_4
S5_3.3V_5

C477 10U/6.3V_8
C502 1U/10V_4
C484 1U/10V_4
C504 1U/10V_4
C492 1U/10V_4
C483 1U/10V_4

P18
P19
P20
P21
P22
P23
P24
R25



For support USB wakeup-->3V_S5

AVDDTX--USB Phy Analog I/O power

+3V USB

0.2A

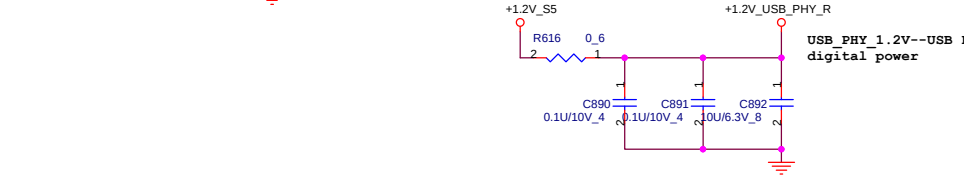
AVDDTX_0
AVDDTX_1
AVDDTX_2
AVDDTX_3
AVDDTX_4
AVDDTX_5
AVDDR_X_0
AVDDR_X_1
AVDDR_X_2
AVDDR_X_3
AVDDR_X_4
AVDDR_X_5

V5_VREF
AVDDCK_3.3V
AVDDCK_1.2V

PLL

USB I/O

SB700



The schematic diagram illustrates the power supply for the USB PHY 1.2V. It features a +1.2V_SS input connected to a resistor R616 (0.6 ohms) and a +1.2V_USB_PHY_R input. The circuit includes three capacitors: C890 (0.1uF/10V_4), C891 (0.1uF/10V_4), and C892 (100uF/6.3V_8). The output is labeled USB_PHY_1.2V--USB Phy digital power.

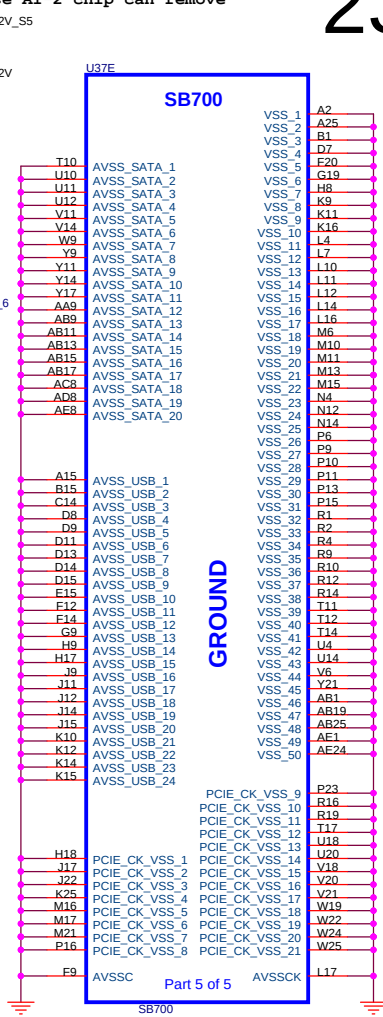
3V

L48
BLM18PG181SN1D(180.15A)_6

3V_AVDDCK

AVDDCK 3.3V--Analog
system PLL power

C516
2.2U/6.3V_6



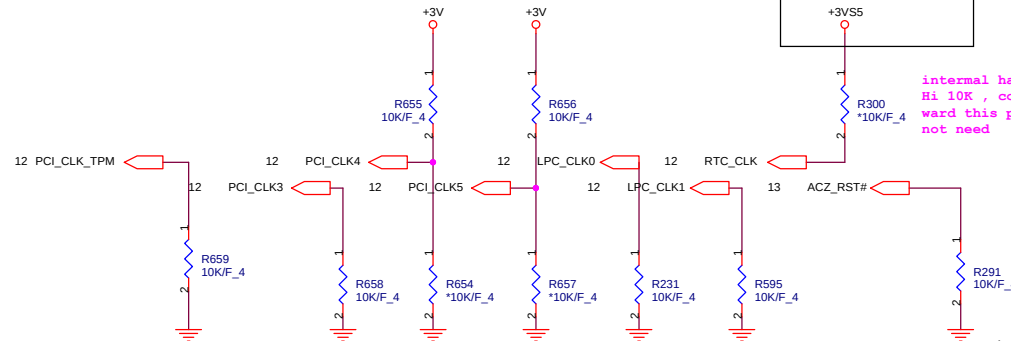


OVERLAP COMMON PADS WHERE
POSSIBLE FOR DUAL-OP RESISTORS.

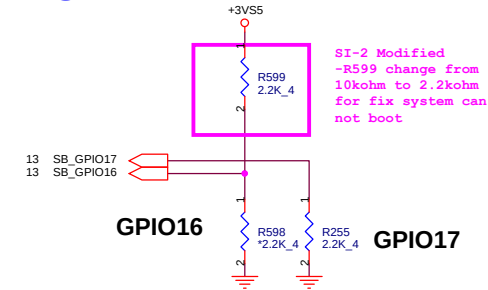
16

It must ready
refofe RSMRST#

REQUIRED STRAPS



	PCI_CLK_TPM	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	IMC ENABLED	CLKGEN ENABLED	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			IMC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT

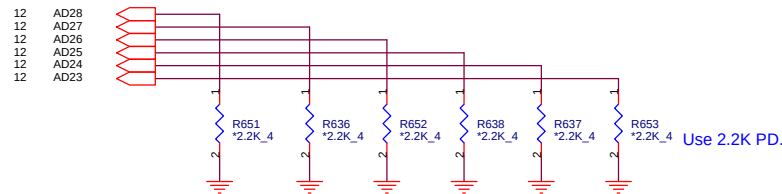


GPIO16 GPIO17

TYPE	GPIO16	GPIO17
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC

DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

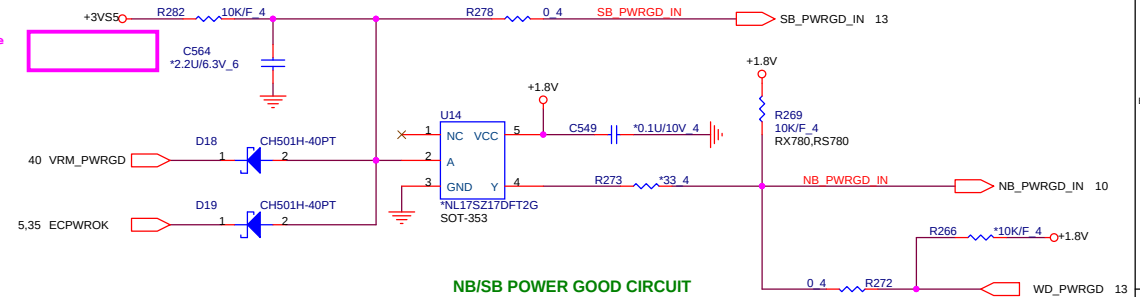


	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

NB_PWRGD_IN:
RS780/RX780 = 1.8V; RS740 = 3.3V
Do NOT share it with SB_PWRGD when use Internal Clk Gen
(Need SB PLL initialize firstly)

SI-2 modified -- confirm AMD R563 need to stuff

SI-2 modified -- remove
+3V pull Hi resistor .



NB/SB POWER GOOD CIRCUIT

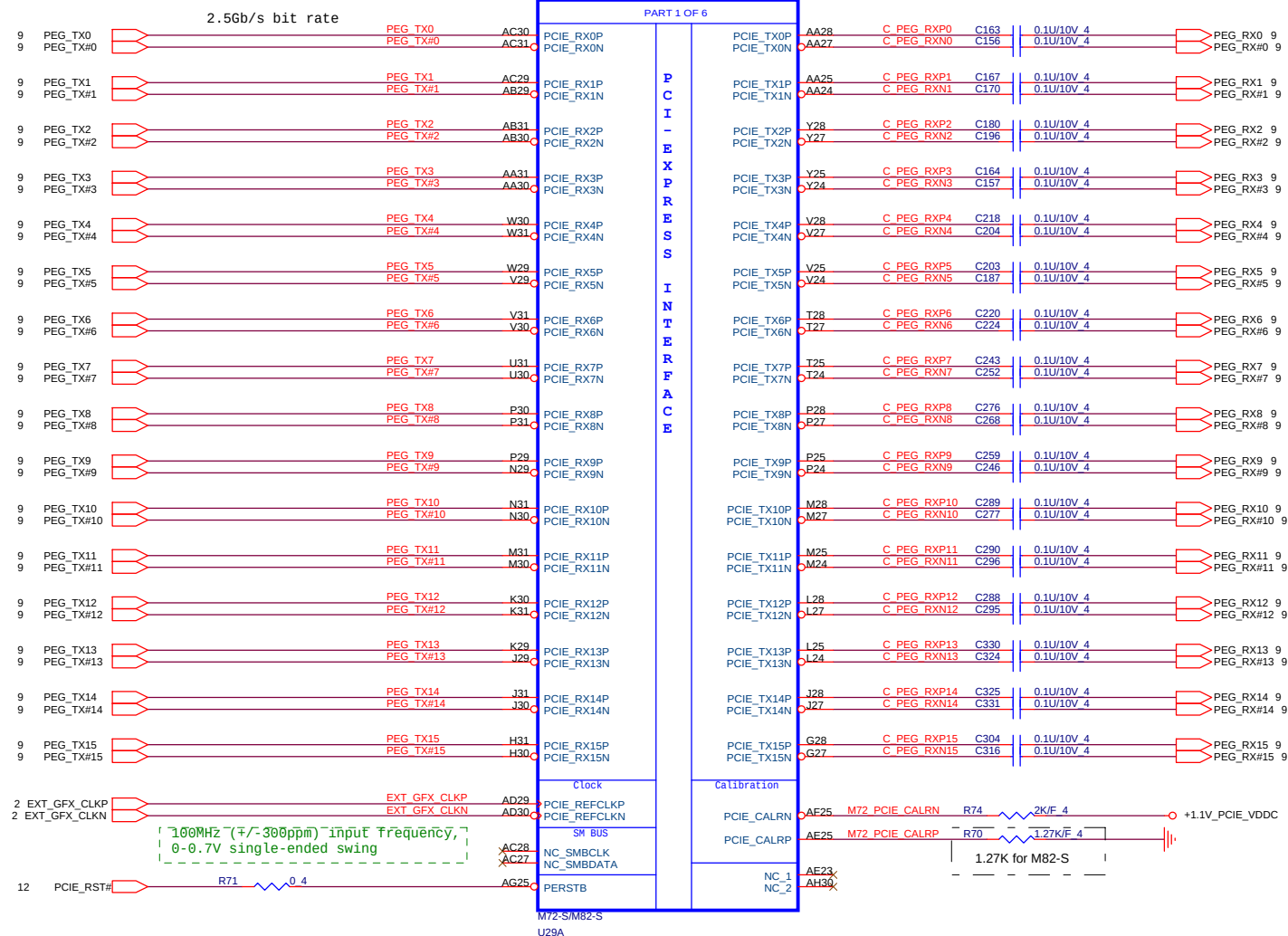
AL17SZ17000 IC(5P) NL17SZ17DFT2G(SOT-353) SOT-353
ALUC1G17000 IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5) SOT23-5



PROJECT : QT8
Quanta Computer Inc.

Size Custom Document Number
SB700-STRAPS Rev 1A
Date: Tuesday, February 19, 2008 Sheet 16 of 45

IC CTRL (632P) 216-0707001-00 (BGA)
VGA P/N : AJ070700T00

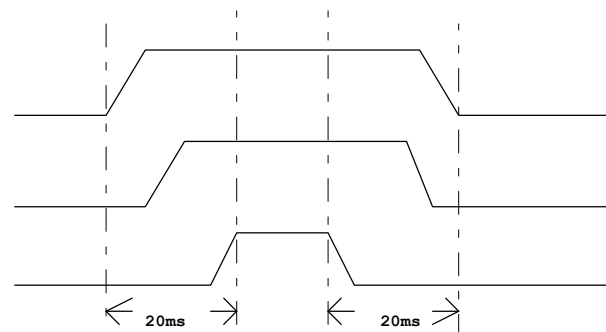


POWER
+PCIE_VDDR=1.2V
+VDD_MEM1.8V=1.8V
+VGA_CORE=1.0~1.1V - M62S, M71S
0.95~1.1V - M72S

VGA Core BPP
VGA Core VDDC

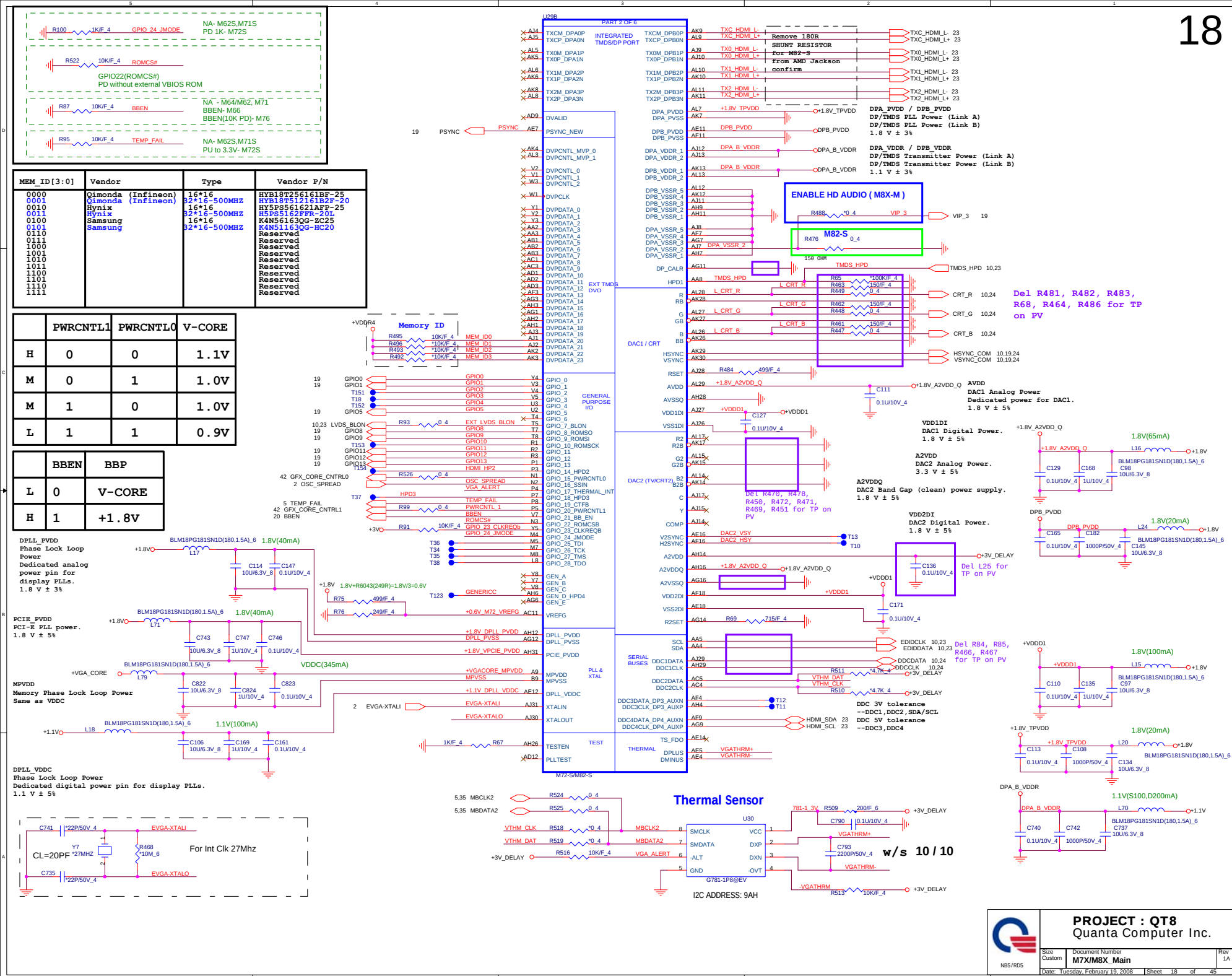
+1.8V PCIE_VDDR
+1.8V PCIE_PVDD
+1.8V VDDR1

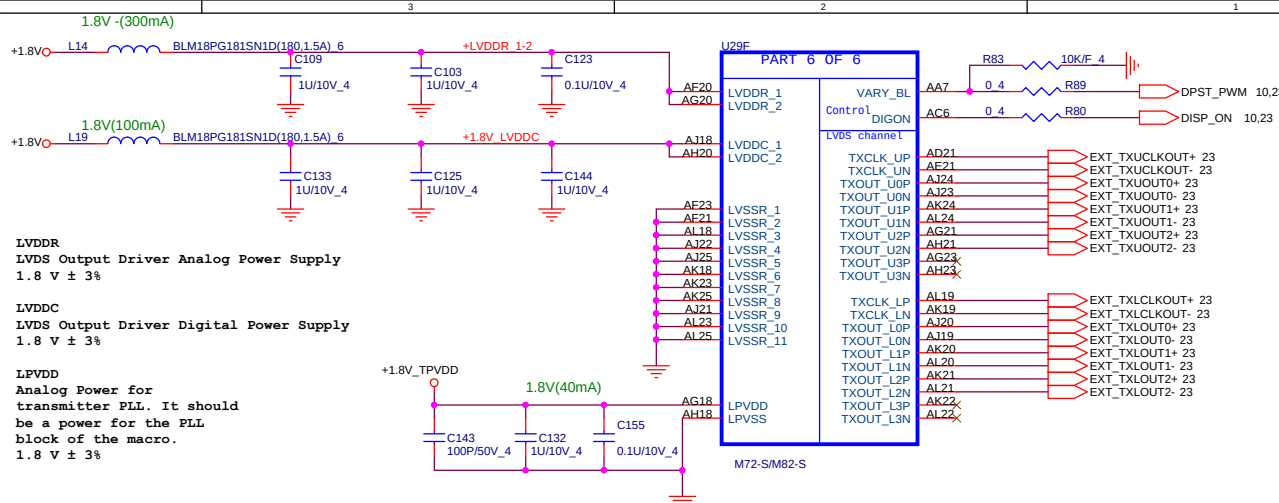
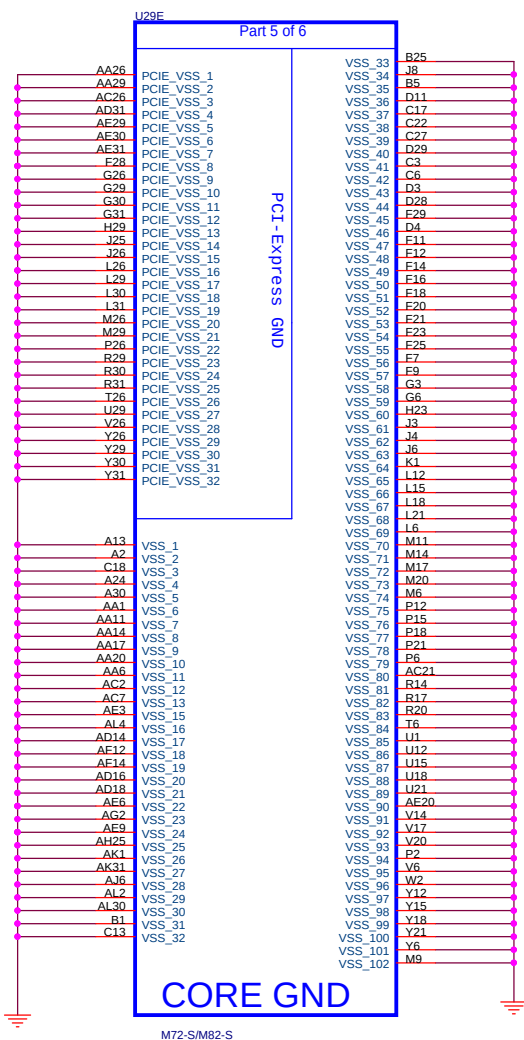
3.3V_Delay VDDR3



PROJECT : QT8
Quantia Computer Inc.

Size Custom Document Number M7X/M8X_PCIE_Interface Rev 1A
Date: Tuesday, February 19, 2008 Sheet 17 of 45





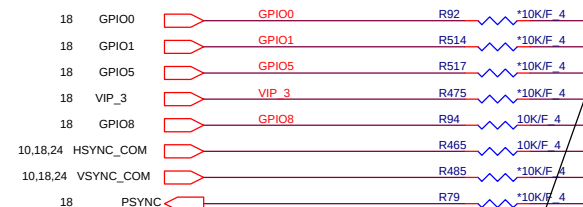
CONFIGURATION STRAPS

PIN	DESCRIPTION OF DEFAULT SETTINGS	M82-S
GPIO0	PCIE FULL TX OUTPUT SWING	0
GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	0
GPIO5	Allows either PCIE 2.5GT/s or 5GT/s operation	REV
VIP3	ENABLE HD AUDIO (M8X-M)	1
GPIO8	ENABLE HD AUDIO (M82-S)	1
HSYNC	ENABLED HDMI	1

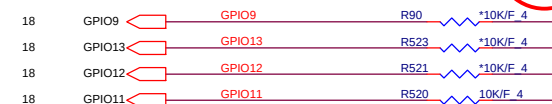
Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

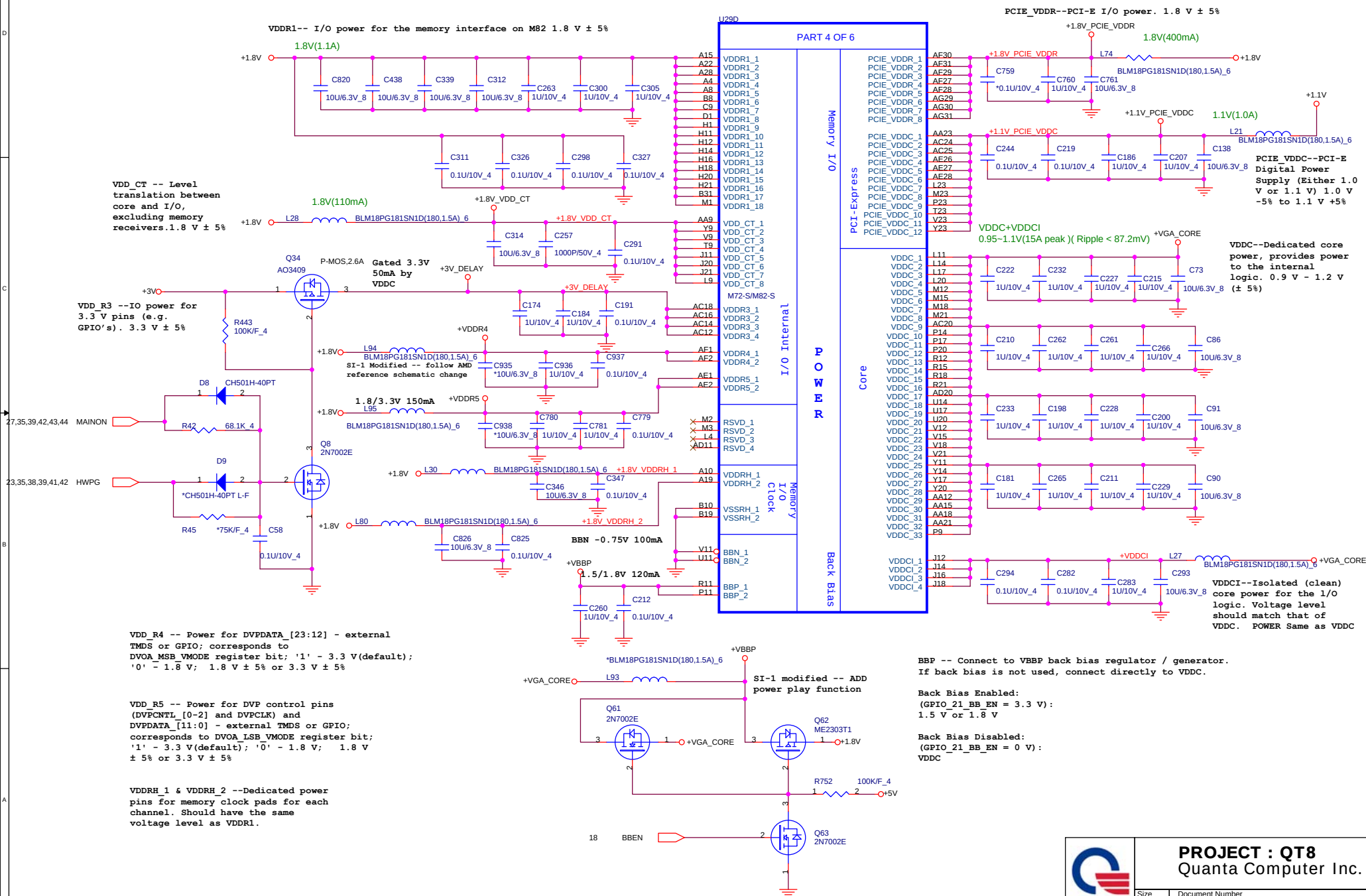


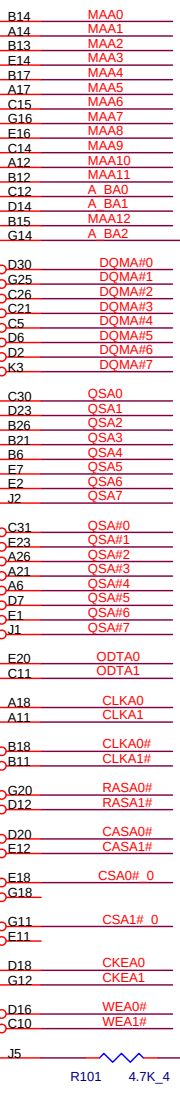
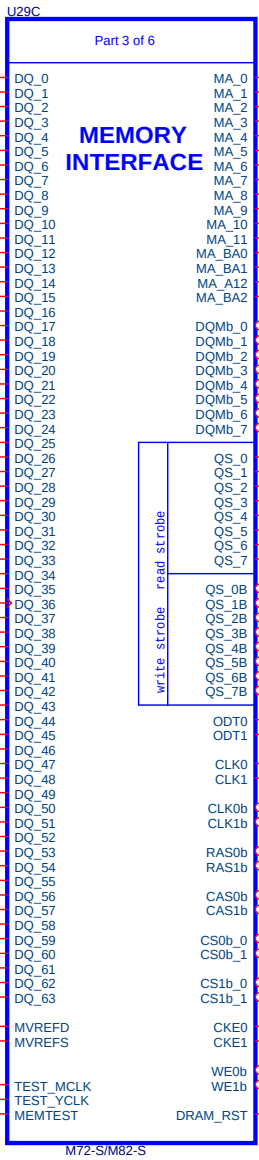
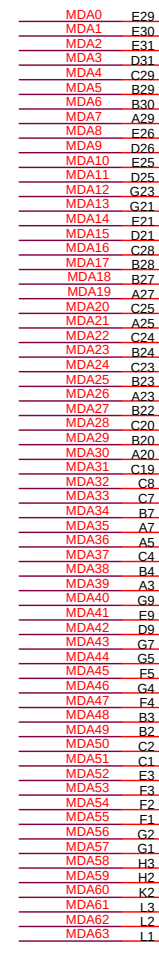
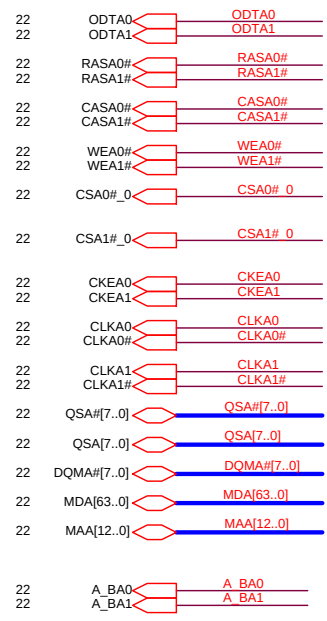
SI-1 Modified -- follow AMD reference schematic change for reduce leakage to VDDR3 BUS



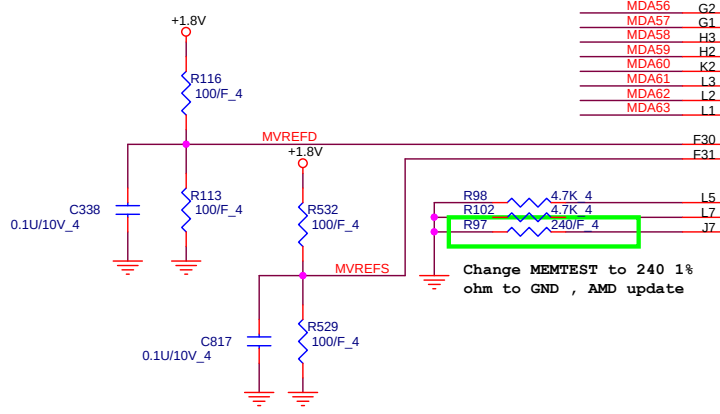
PROJECT : QT8
Quanta Computer Inc.

Size Custom Document Number M7X/M8X_GND / LVDS/ Straps Rev 1A
Date: Tuesday, February 19, 2008 Sheet 19 of 45



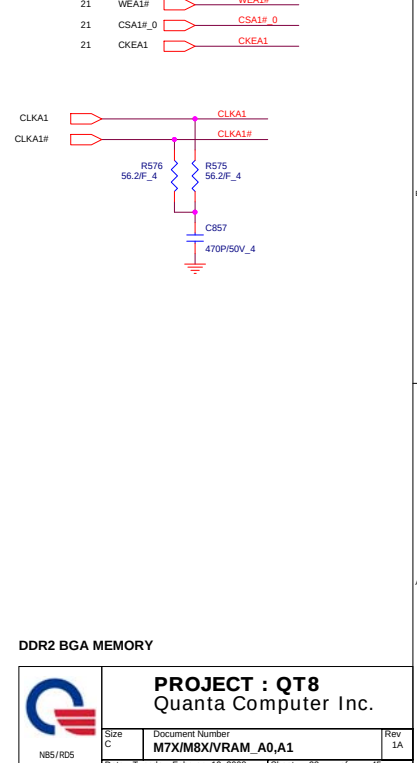
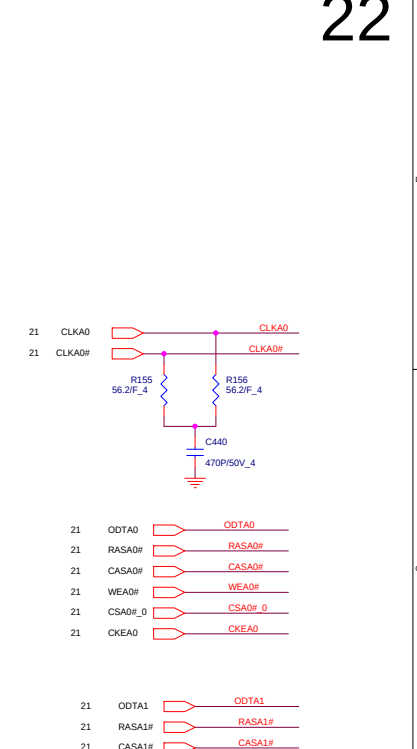


A_BA2 22
SI-1 modified --
for support
1Gbit VRAM (64M
x 16)



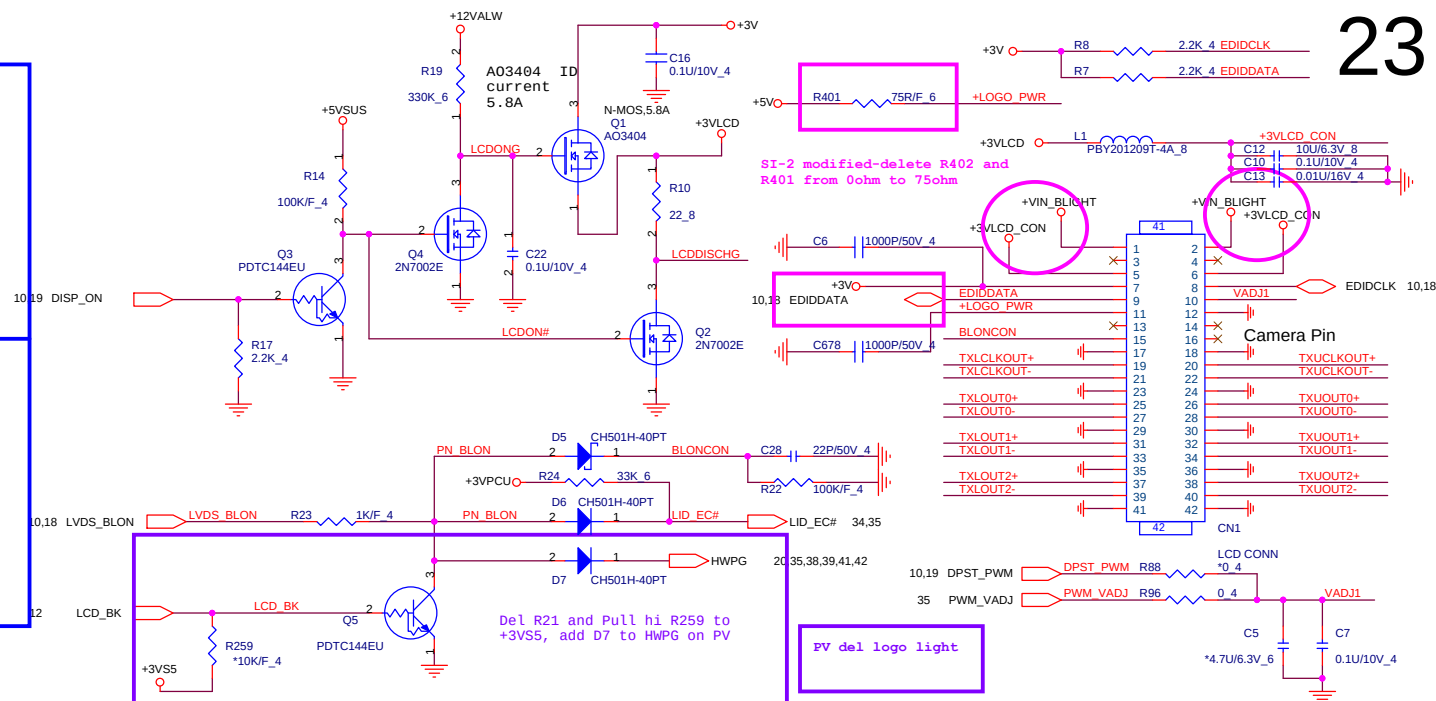
PROJECT : QT8
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Size B	Document Number M7X/M8X/MEM_Interface	Rev 1A
Date: Tuesday, February 19, 2008	Sheet 21 of 45	



10	LA_CLK	LA_CLK	RP3	1	2	0_4P2R_4	TXCLKOUT+
10	LA_CLK#	LA_CLK#		3	4		TXCLKOUT-
10	LA_DATAP0	LA_DATAP0	RP1	1	2	0_4P2R_4	TXLOUT0+
10	LA_DATAN0	LA_DATAN0		3	4		TXLOUT0-
10	LA_DATAP1	LA_DATAP1	RP4	1	2	0_4P2R_4	TXLOUT1+
10	LA_DATAN1	LA_DATAN1		3	4		TXLOUT1-
10	LA_DATAP2	LA_DATAP2	RP5	1	2	0_4P2R_4	TXLOUT2+
10	LA_DATAN2	LA_DATAN2		3	4		TXLOUT2-
10	LB_CLK	LB_CLK	RP2	3	4	0_4P2R_4	TXCLKOUT+
10	LB_CLK#	LB_CLK#		1	2		TXCLKOUT-
10	LB_DATAP0	LB_DATAP0	RP6	1	2	0_4P2R_4	TXLOUT0+
10	LB_DATAN0	LB_DATAN0		3	4		TXLOUT0-
10	LB_DATAP1	LB_DATAP1	RP8	3	4	0_4P2R_4	TXLOUT1+
10	LB_DATAN1	LB_DATAN2		1	2		TXLOUT1-
10	LB_DATAP2	LB_DATAP2	RP7	3	4	0_4P2R_4	TXLOUT2+
10	LB_DATAN2			1	2		TXLOUT2-

EXT_TXLCLKOUT-	EXT_TXLCLKOUT-	RP59	1	2	0_4P2R_4	TXLCLKOUT-
EXT_TXLCLKOUT+	EXT_TXLCLKOUT+	RP59	3	4		TXLCLKOUT+
EXT_TXLOUT0-	EXT_TXLOUT0-	RP57	1	2	0_4P2R_4	TXLOUT0-
EXT_TXLOUT0+	EXT_TXLOUT0+	RP57	3	4		TXLOUT0+
EXT_TXLOUT1-	EXT_TXLOUT1-	RP60	1	2	0_4P2R_4	TXLOUT1-
EXT_TXLOUT1+	EXT_TXLOUT1+	RP60	3	4		TXLOUT1+
EXT_TXLOUT2-	EXT_TXLOUT2-	RP61	1	2	0_4P2R_4	TXLOUT2-
EXT_TXLOUT2+	EXT_TXLOUT2+	RP61	3	4		TXLOUT2+
EXT_TXLCLKOUT-	EXT_TXLCLKOUT-	RP58	1	2	0_4P2R_4	TXLCLKOUT-
EXT_TXLCLKOUT+	EXT_TXLCLKOUT+	RP58	3	4		TXLCLKOUT+
EXT_TXLOUT0+	EXT_TXLOUT0+	RP62	3	4	0_4P2R_4	TXLOUT0+
EXT_TXLOUT0-	EXT_TXLOUT0-	RP62	1	2		TXLOUT0-
EXT_TXLOUT1-	EXT_TXLOUT1-	RP64	1	2	0_4P2R_4	TXLOUT1-
EXT_TXLOUT1+	EXT_TXLOUT1+	RP64	3	4		TXLOUT1+
EXT_TXLOUT2-	EXT_TXLOUT2-	RP63	1	2	0_4P2R_4	TXLOUT2-
EXT_TXLOUT2+	EXT_TXLOUT2+	RP63	3	4		TXLOUT2+

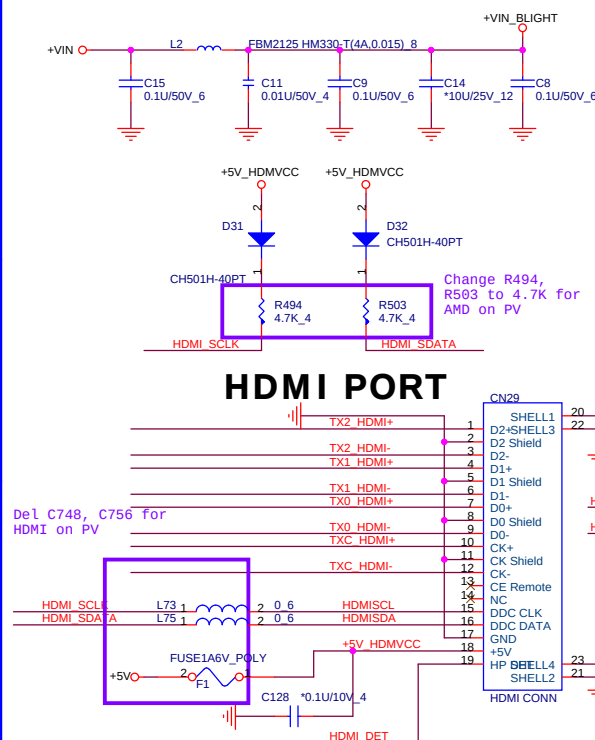
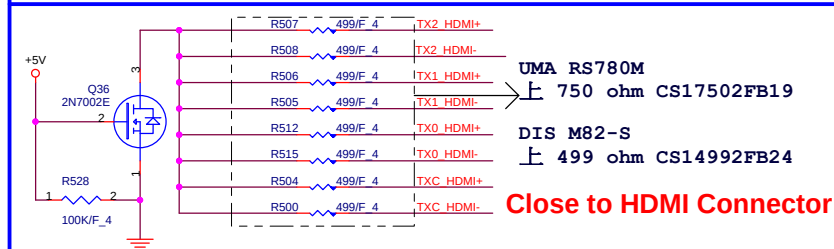


From RS780M

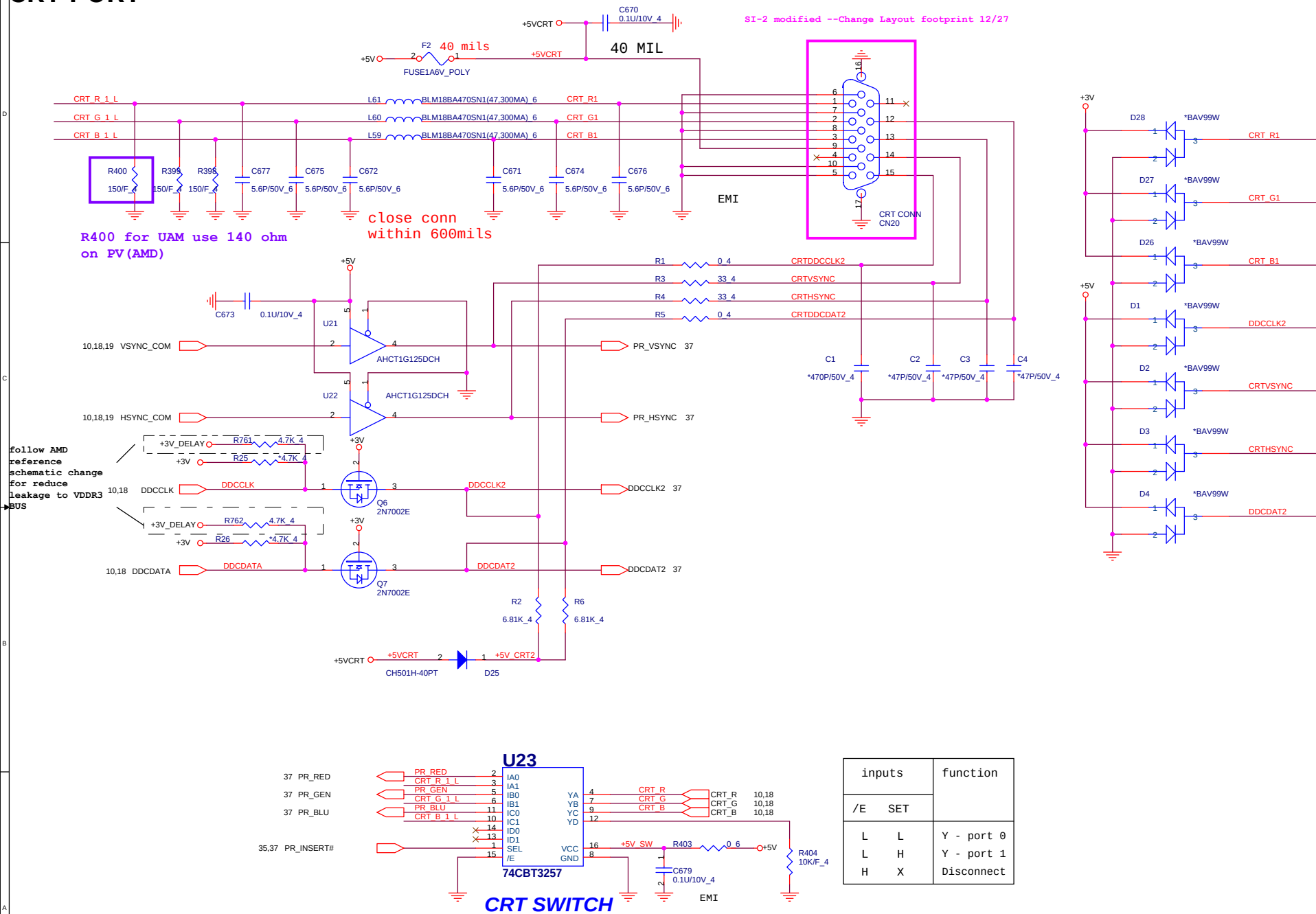
From RS780M						for Layout concern ,placement close north bridge						for Layout concern ,placement close HDMI conn					
9	C_PEG_TX#15	C_PEG_TX#15 C386	*0.1U/10V	4	TX2 HDMI+L	TX2 HDMI+L 3	4	*0.4P2R	4	TX2 HDMI+							
9	C_PEG_TX15	C_PEG_TX15 C387	*0.1U/10V	4	TX2 HDMI+L	TX2 HDMI+L 1	2		2	TX2 HDMI+							
9	C_PEG_TX#14	C_PEG_TX#14 C388	*0.1U/10V	4	TX1 HDMI-L	TX1 HDMI-L 3	4	*0.4P2R	4	TX1 HDMI-							
9	C_PEG_TX14	C_PEG_TX14 C389	*0.1U/10V	4	TX1 HDMI+L	TX1 HDMI+L 1	2		2	TX1 HDMI-							
9	C_PEG_TX#13	C_PEG_TX#13 C355	*0.1U/10V	4	TX0 HDMI-L	TX0 HDMI-L 3	4	*0.4P2R	4	TX0 HDMI+							
9	C_PEG_TX13	C_PEG_TX13 C344	*0.1U/10V	4	TX0 HDMI+L	TX0 HDMI+L 1	2		2	TX0 HDMI-							
9	C_PEG_TX#12	C_PEG_TX#12 C827	*0.1U/10V	4	TXC HDMI-L	TXC HDMI-L 3	4	*0.4P2R	4	TXC HDMI-							
9	C_PEG_TX12	C_PEG_TX12 C828	*0.1U/10V	4	TXC HDMI+L	TXC HDMI+L 1	2		2	TXC HDMI+							

18	TX2_HDMI_L	TX2 HDMI L	C794	0.1u/10V_4	TX2 HDMI-
18	TX2_HDMI_L+	TX2 HDMI L+	C789	0.1u/10V_4	TX2 HDMI+
18	TX1_HDMI_L	TX1 HDMI L	C782	0.1u/10V_4	TX1 HDMI-
18	TX1_HDMI_L+	TX1 HDMI L+	C786	0.1u/10V_4	TX1 HDMI+
18	TX0_HDMI_L	TX0 HDMI L	C799	0.1u/10V_4	TX0 HDMI-
18	TX0_HDMI_L+	TX0 HDMI L+	C797	0.1u/10V_4	TX0 HDMI+
18	TXC_HDMI_L	TXC HDMI L	C768	0.1u/10V_4	TXC HDMI-
18	TXC_HDMI_L+	TXC HDMI L+	C776	0.1u/10V_4	TXC HDMI+

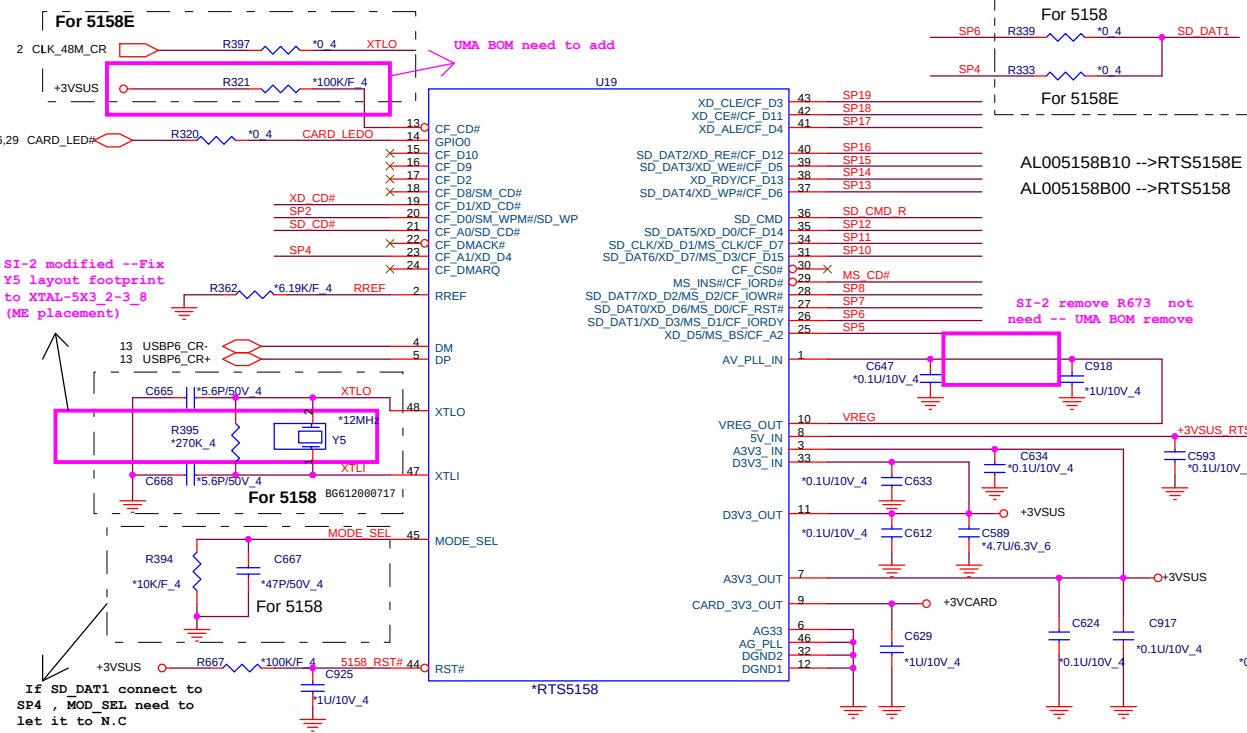
for Layout concern, placement close HDMI conn

[illegible]

CRT PORT

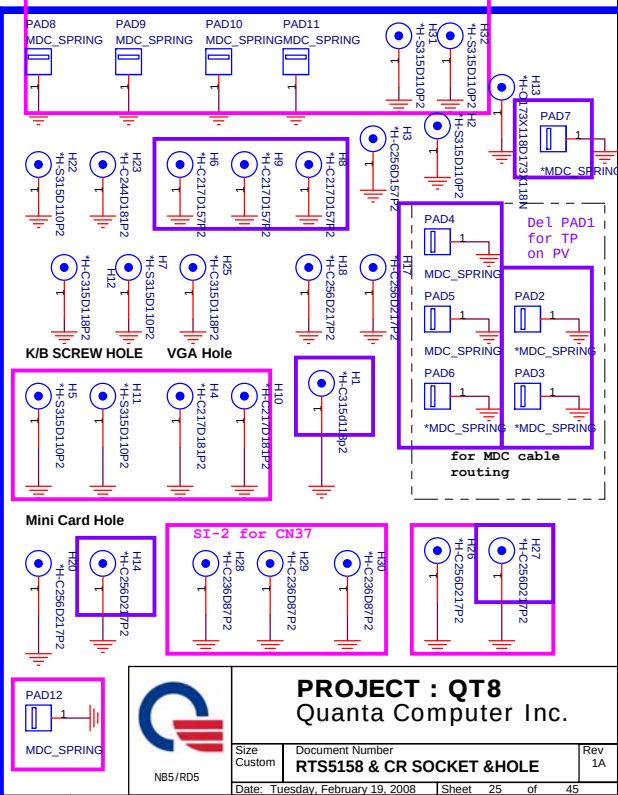
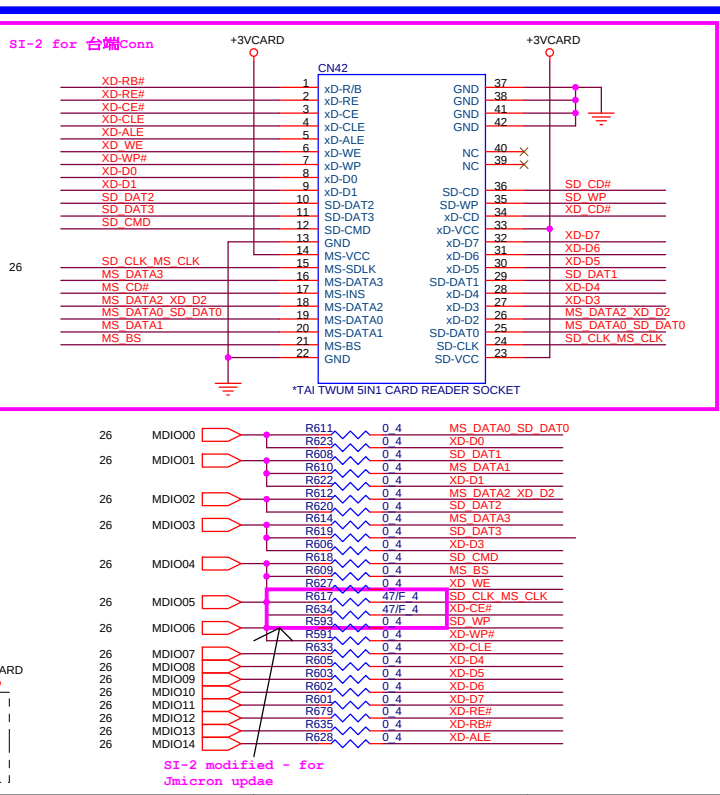
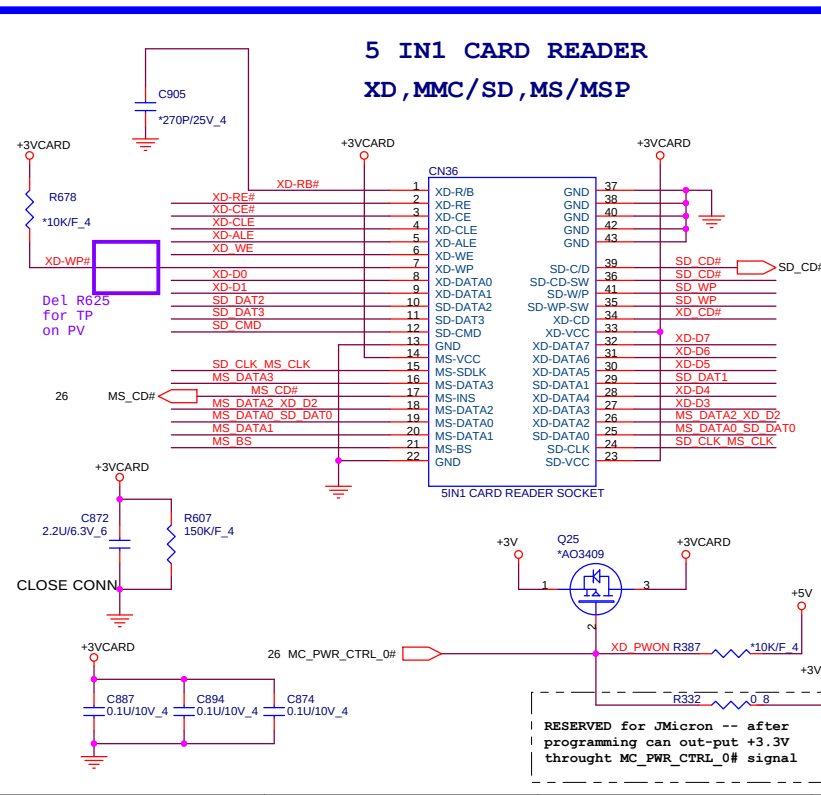
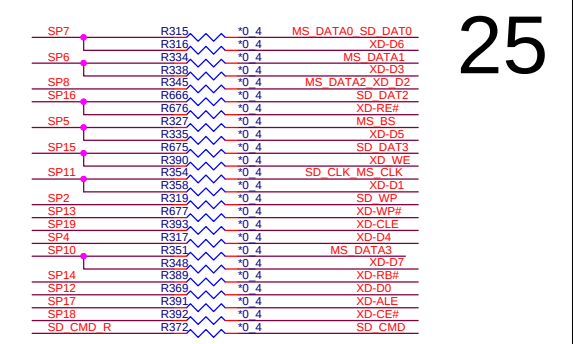


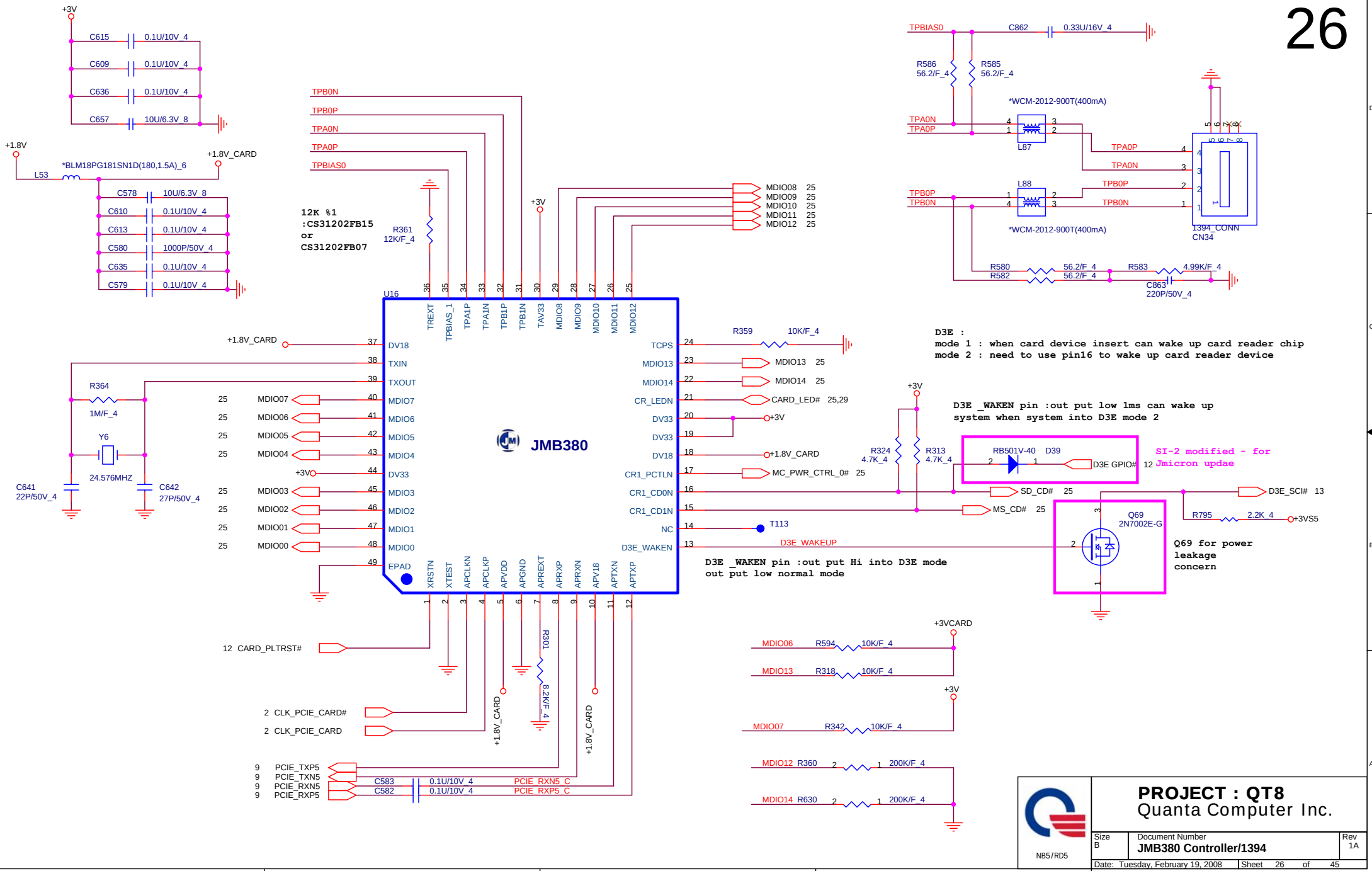
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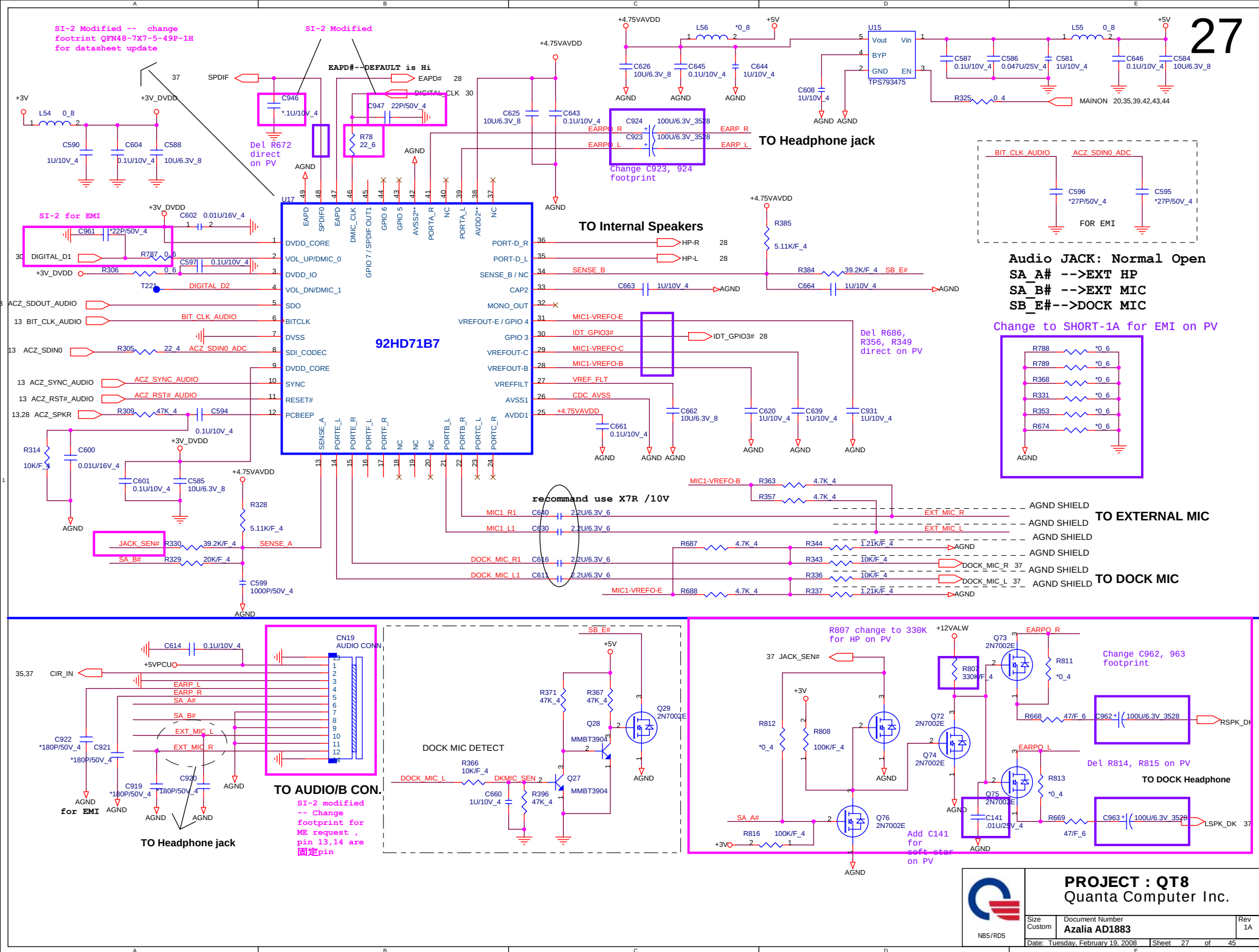
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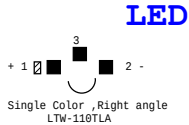
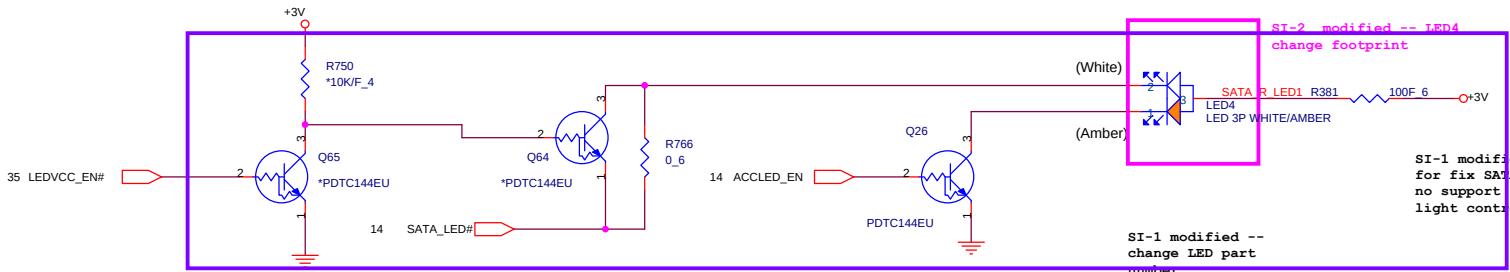
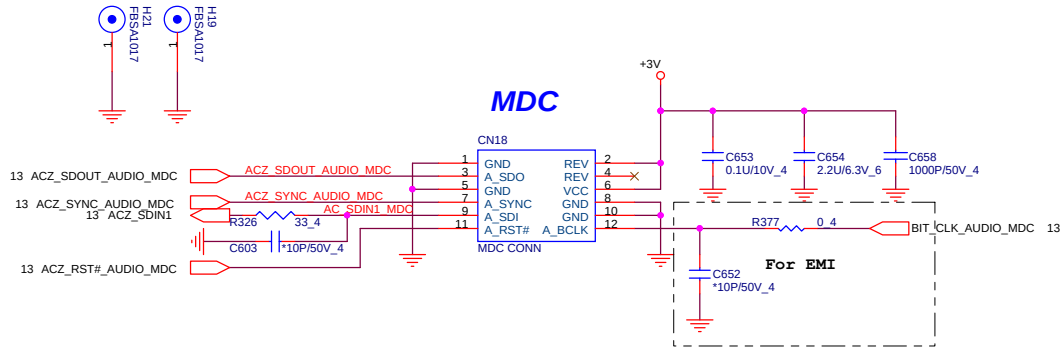
SD/MMC	MS	XD
SP1 SD WP		XD_CD#
SP2 SD CD#		
SP3 SD DAT1	XD D4	
SP4 SD DAT1	XD D5	
SP5 SD DAT1	XD D6	
SP6 SD DAT1	XD D7	
SP7 SD DAT1	XD D8	
SP8 SD DAT1	XD D9	
SP9 SD DAT1	XD D10	
SP10 SD DAT1	XD D11	
SP11 SD DAT1	XD D12	
SP12 SD DAT1	XD D13	
SP13 SD DAT1	XD D14	
SP14 SD DAT1	XD D15	
SP15 SD DAT1	XD D16	
SP16 SD DAT1	XD D17	
SP17 SD DAT1	XD D18	
SP18 SD DAT1	XD D19	
SP19 SD DAT1	XD D20	



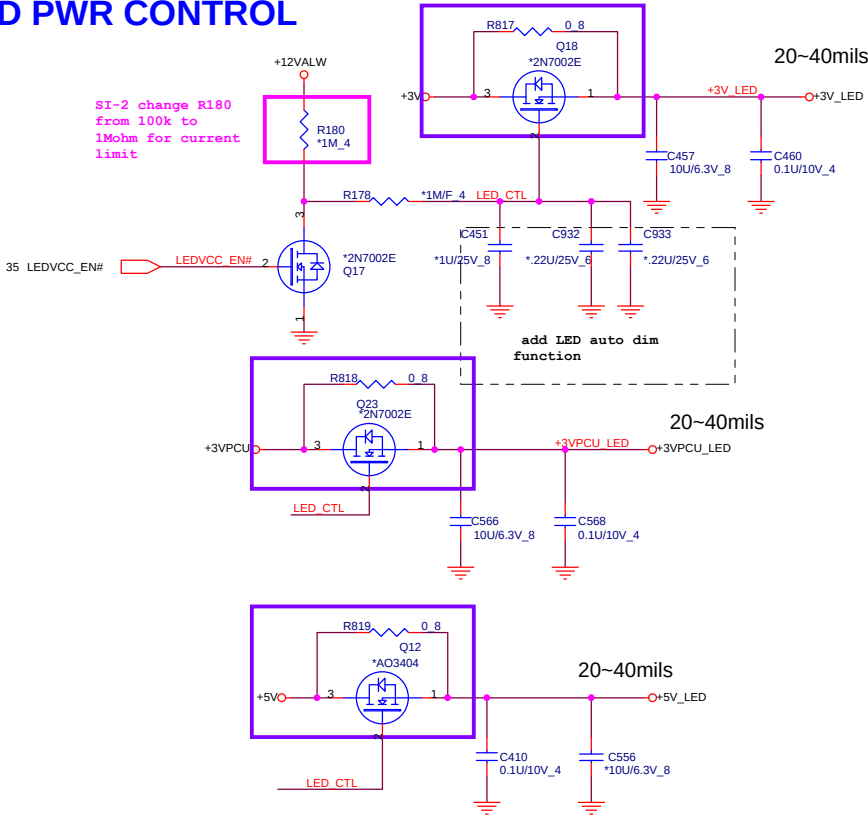


SI-2 Modified

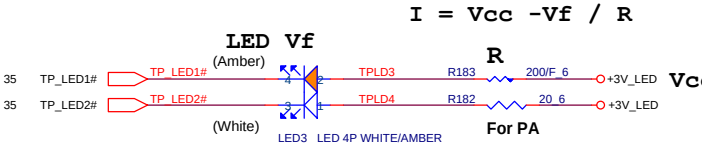
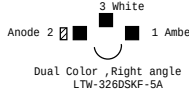
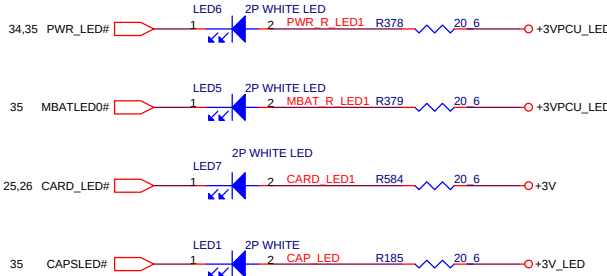




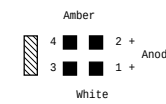
LED PWR CONTROL



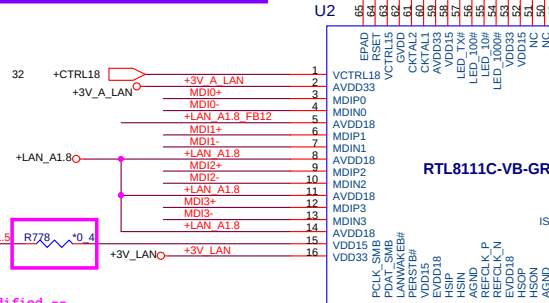
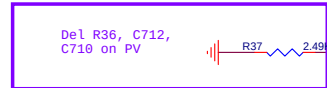
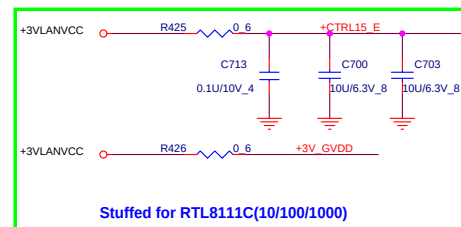
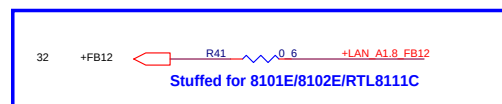
Del R380
Change R381 to 100
Add R766, R817, R818,
R819
LED PWR control no-stuff
on PV



$$I = \frac{V_{cc} - V_f}{R}$$

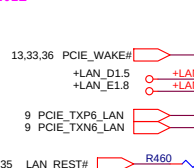


Del R50 on PV



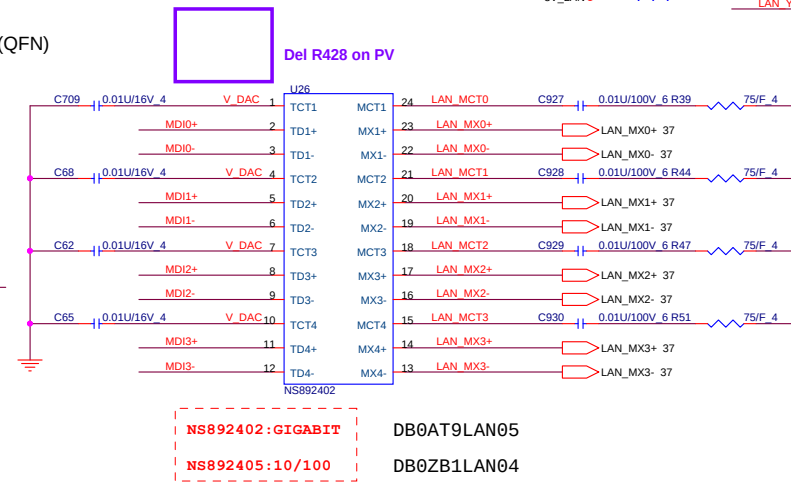
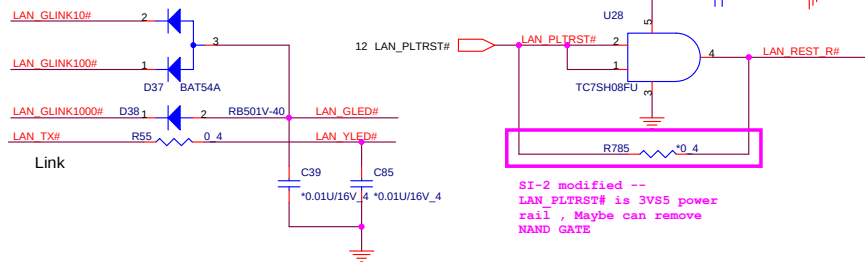
R778
SI-2 modified --
RTL8111C remove,
RTL8111B, 8101E, 8102E
need to stuff

Del R429, R431, R433, R435,
C718, C726 for 8111B on PV



AL08111C001 IC CTRL(64P) RTL8111C-VB-GR(QFN)

AL08101E005 IC(64P)RTL8101E-GR(QFN)

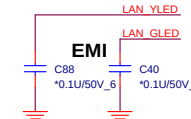


use BIOS to programming
EEPROM, EEDI should be
pull Hi

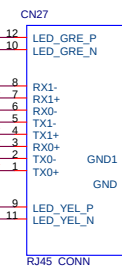
R46
only for 8111B,
8101E&8102E&8111C can
remove

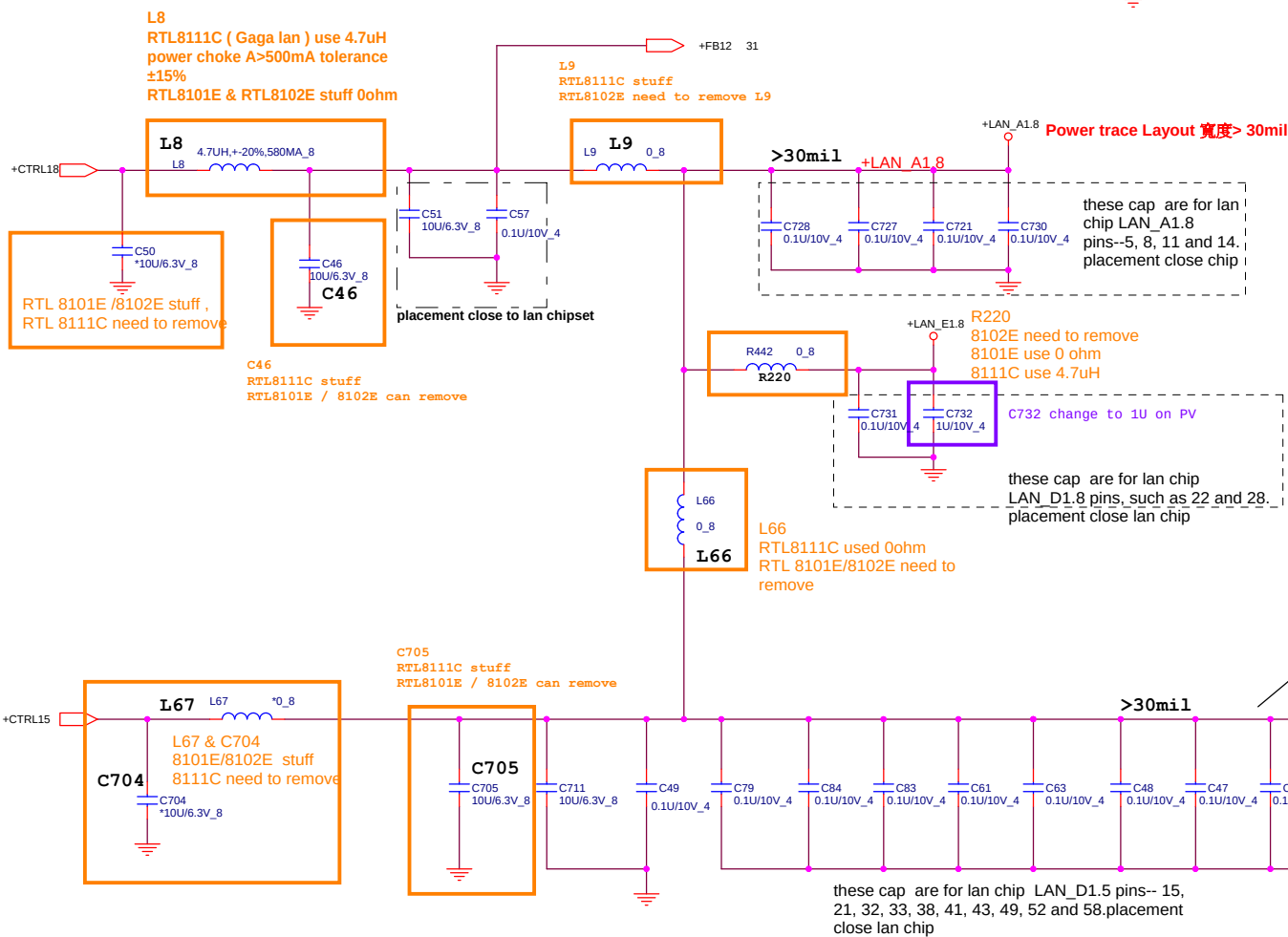
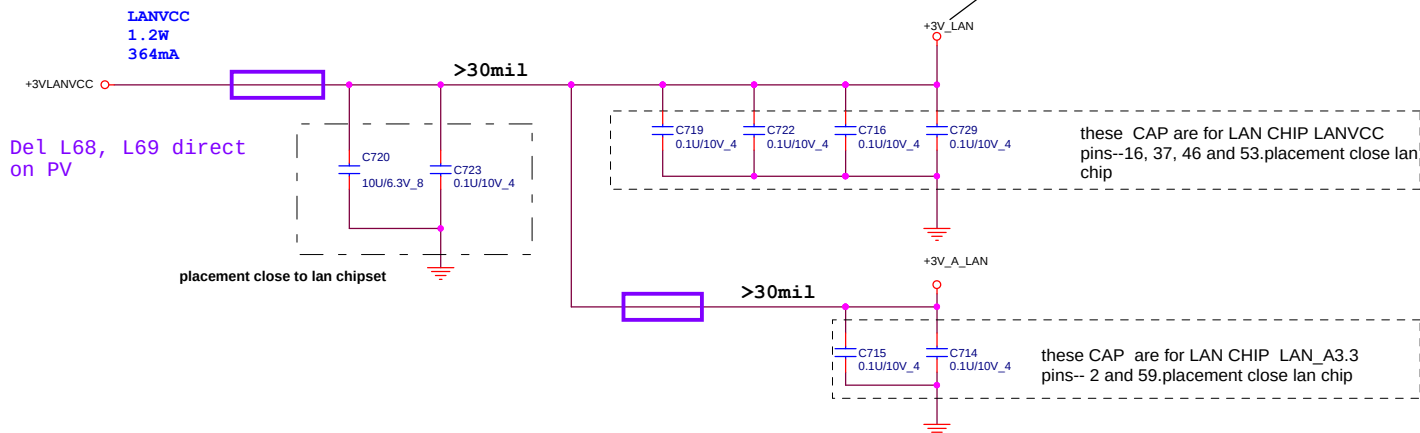
Remove R456 and Add D42 on PV

if ISOLATEB pin
pull-low, the LAN
chip will not drive
it's PCI-E outputs
(excluding
PCIE_WAKE# pin)



RJ45





Power domain chart

	RTL8111B / RTL8101E	RTL8111C RTL8102E
LANVCC	3.3V	3.3V
LAN_D1.8	1.8V	1.2V
LAN_A1.8	1.8V	1.2V
LAN_D1.5	1.5V	1.2V



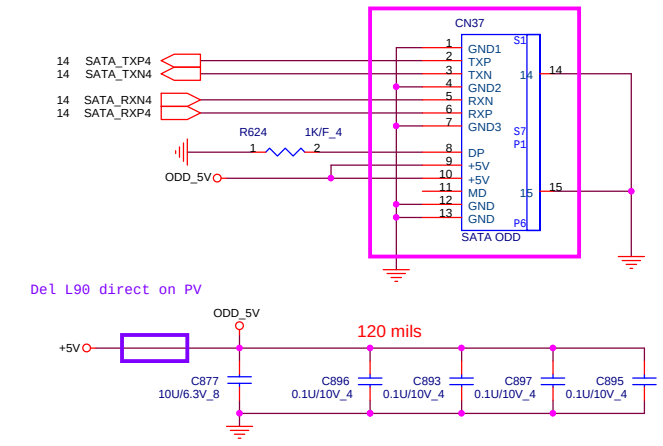
NBS/RD5

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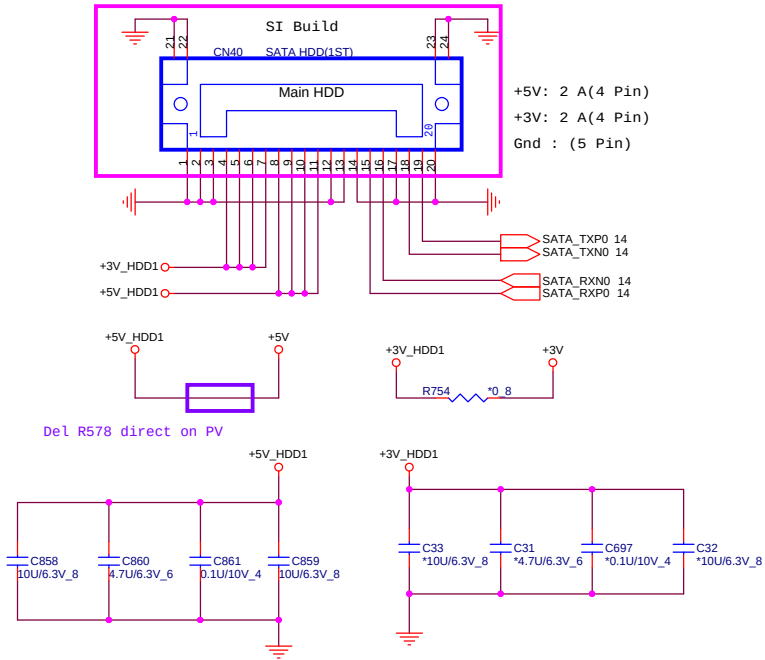
Size	Document Number	Rev
Custom	LAN Power	1A
Date: Tuesday, February 19, 2008	Sheet 32 of 45	

SATA CD-ROM

SI-2 Modified footprint -- Modify 12/27



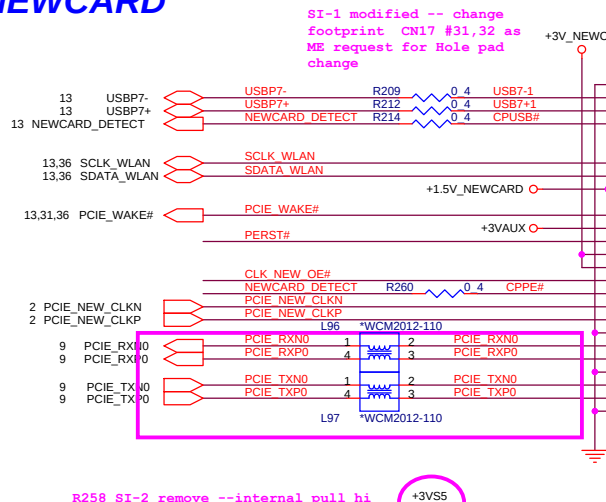
SI-2 Modified footprint -- Modify 固定孔 Size as SMT request



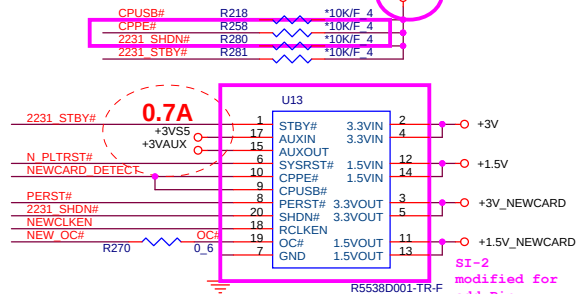
NEWCARD

NEWCARD (PCIEXPRESS*1 + USB*1)

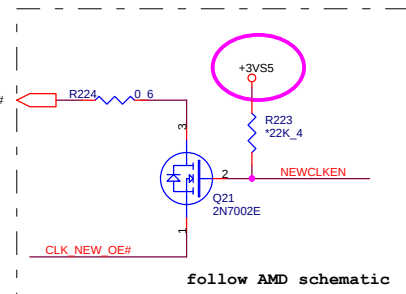
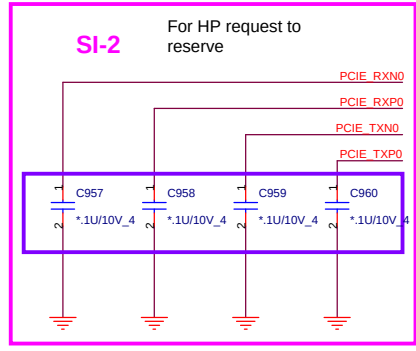
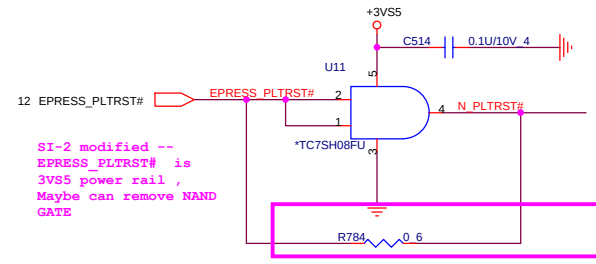
33



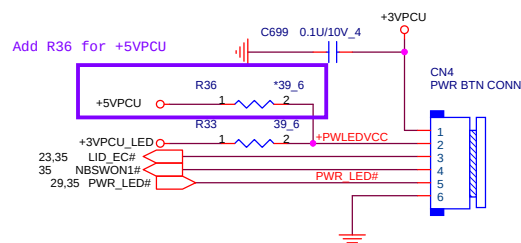
R258 SI-2 remove --internal pull hi



R5538 NEW CARD POWER SWITCH	
pin name	pull hi/low
CPPE#	internal pull up to AUXIN
SYSRST#	internal pull up to AUXIN
CPUSB##	internal pull up to AUXIN
PERST#	a logic level power good
SHDN#	internal pull up to AUXIN
RCLKEN	internal pull up to AUXIN
OC#	over current status
STBY#	internal pull up to AUXIN

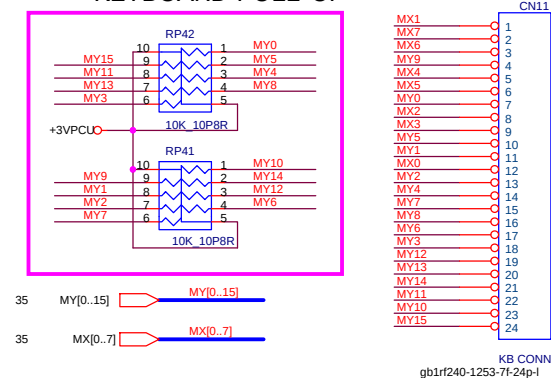


34

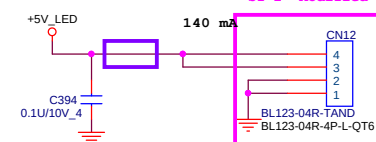


-
- Diagram showing the connection of 12 Mylar capacitors (MY1 to MY12) to a common ground. The capacitors are arranged in three columns. Each capacitor is labeled with its part number, value (220P/50V 4), and a color code (MY# C###). The capacitors are connected to a common ground line at the bottom.
- | Capacitor | Value | Color Code | | | | | |
|-----------|------------|------------|------------|-----------|------------|-----------|------------|
| MY5 C379 | 220P/50V 4 | MY1 C836 | 220P/50V 4 | MY7 C384 | 220P/50V 4 | | |
| MY6 C833 | 220P/50V 4 | MY2 C835 | 220P/50V 4 | MY8 C376 | 220P/50V 4 | | |
| MY3 C375 | 220P/50V 4 | MY4 C377 | 220P/50V 4 | MY9 C403 | 220P/50V 4 | | |
| MY7 C834 | 220P/50V 4 | MY0 C381 | 220P/50V 4 | MY10 C830 | 220P/50V 4 | | |
| | | | | MY11 C373 | 220P/50V 4 | | |
| | | | | MX4 C402 | 220P/50V 4 | | |
| | | | | MX6 C383 | 220P/50V 4 | MY12 C832 | 220P/50V 4 |
| | | | | MX3 C837 | 220P/50V 4 | MY13 C374 | 220P/50V 4 |
| | | | | MX2 C380 | 220P/50V 4 | MY14 C831 | 220P/50V 4 |
| | | | | | | MY15 C372 | 220P/50V 4 |

KEYBOARD PULL-UP



SI-2 Modified 12/27

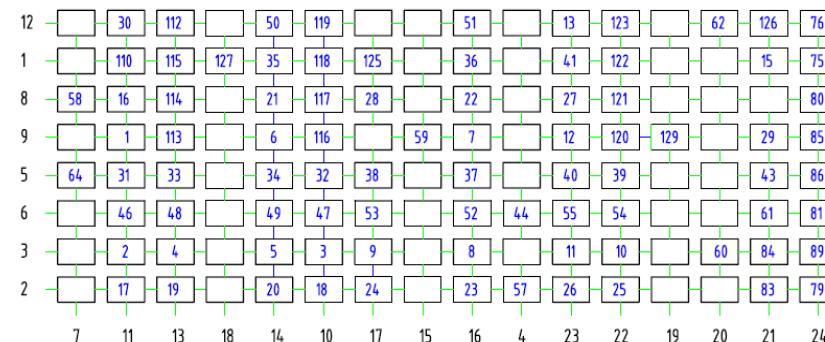


- SI-2 Modified

[illegible]

1. +3VPCU
2. MBCLK
3. MBDATA
4. CAP_INT
5. GND
6. NUM LOCK LED
7. +5V
8. ESB_CLK
9. ESB_DAT

PV modified:
CN8 update type
Add L57, L77, C904, C621 for ESB
Del R104, R103

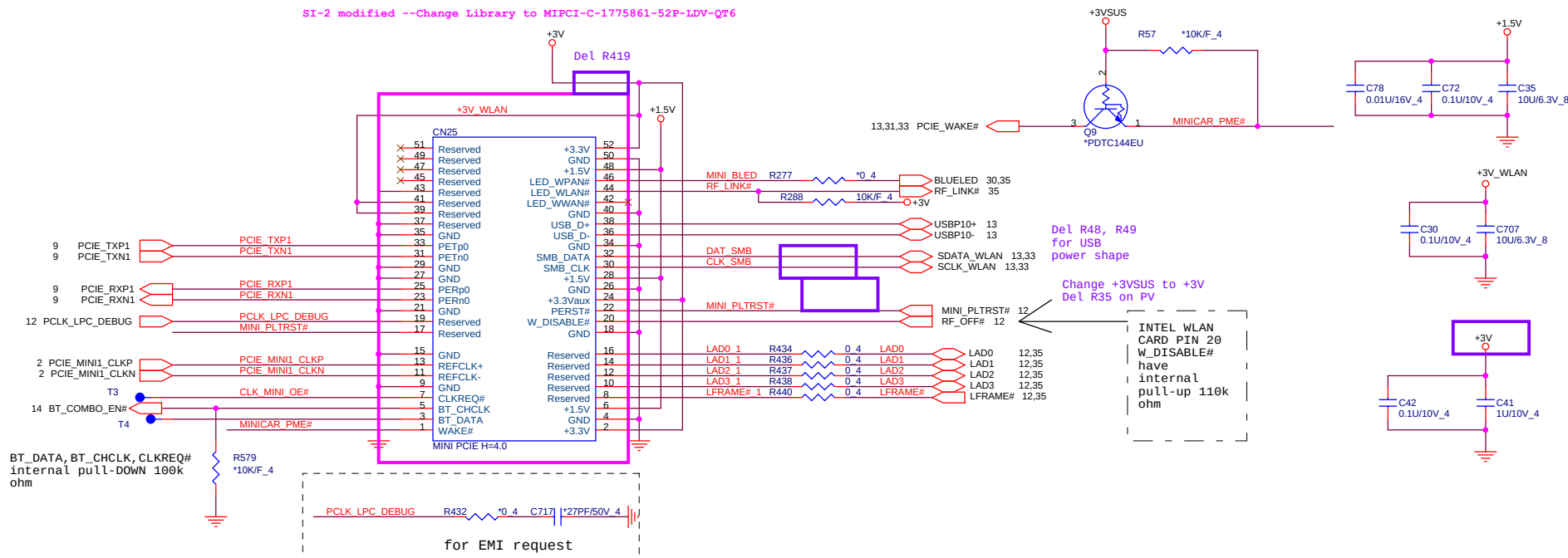


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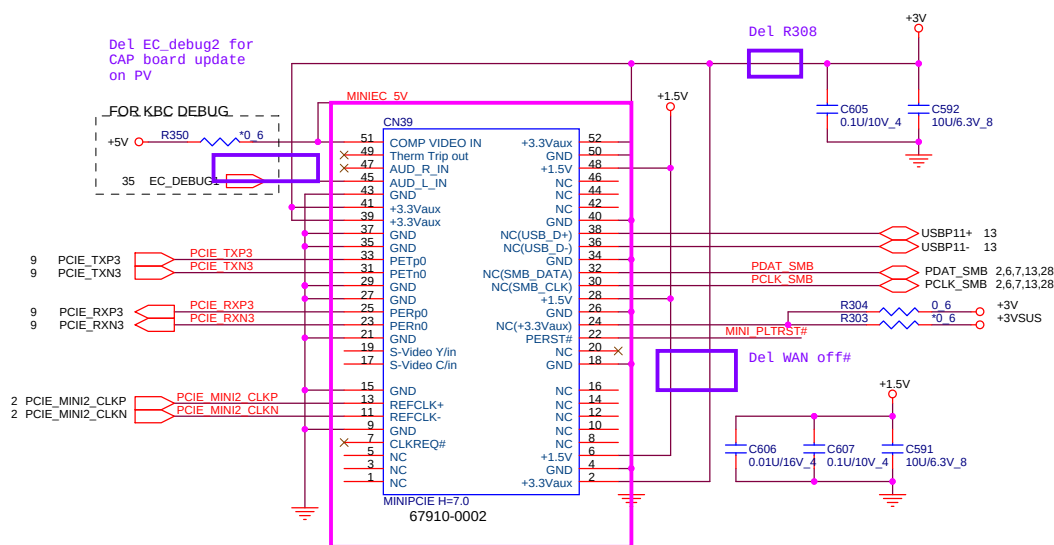
Size Custom	Document Number LED/KEYBOARD/SW	Rev 1A
Date: Tuesday, February 19, 2008		Sheet 34 of 45

Mini PCI-E Card 1 WLAN

SI-2 modified --Change Library to MIPCI-C-1775861-52P-LDV-QT6



Mini PCI-E Card 2 TV tuner card



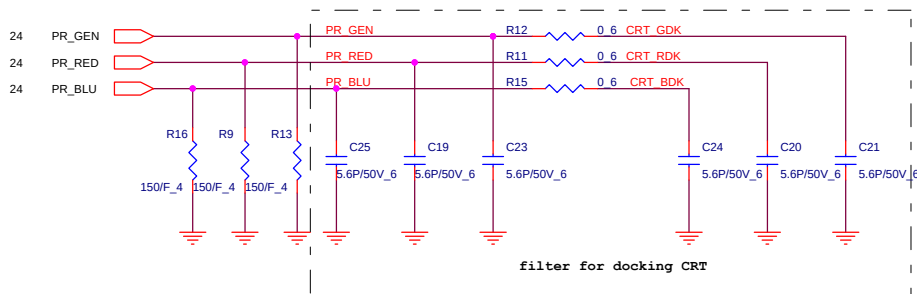
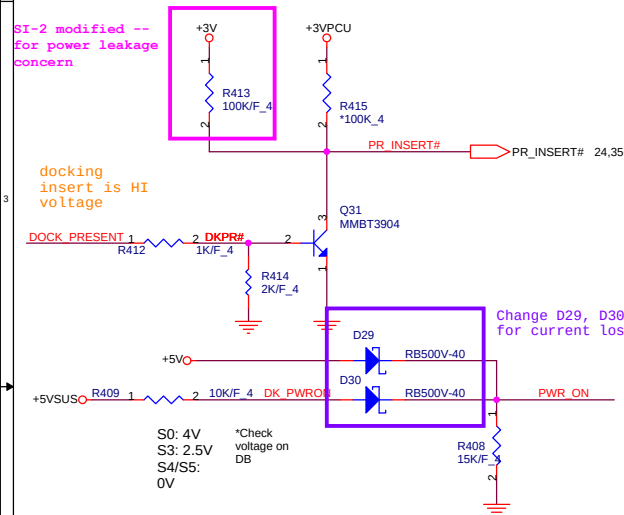
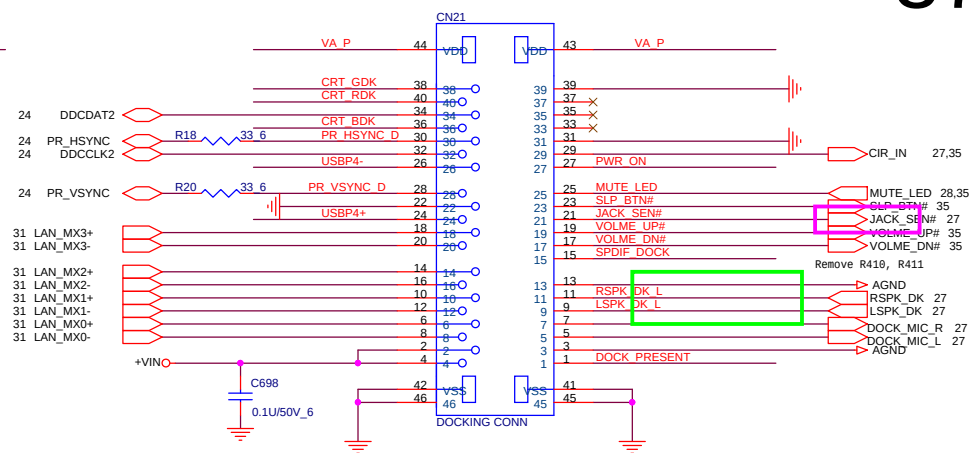
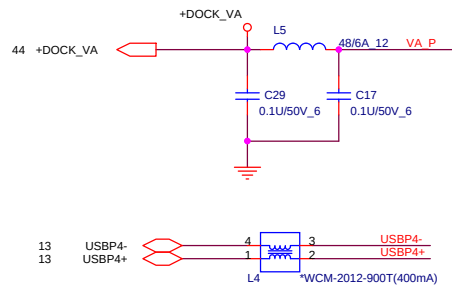
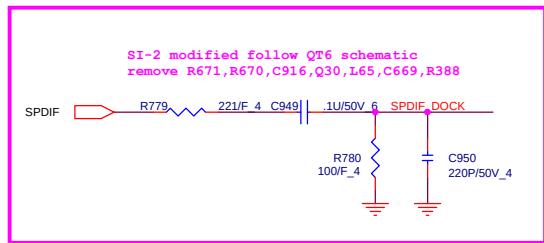
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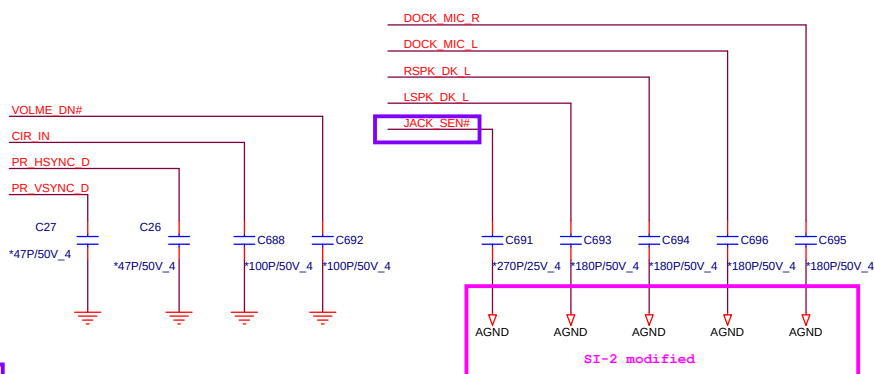
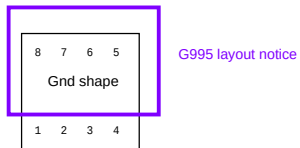
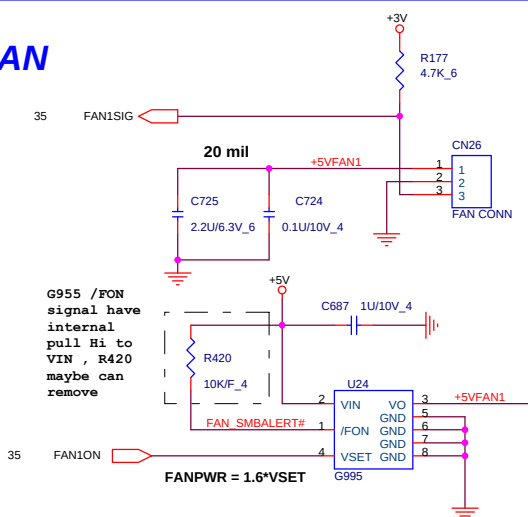
PROJECT : QT8
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Size Custom	Document Number Mini CARD X 3	Rev 1/
Date: Tuesday, February 19, 2008		Sheet 36 of 45

CABLE DOCK

support 6A 200mils
CX000480005

CPU FAN



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Size Custom	Document Number CABLE DOCKING/FAN	Rev 1A
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 +5VPCU 27,28,34,35,39,40,41,42,43

 +3VPCU 5,12,23,29,30,34,35,37,40,41,42,44

 +3VS5 13,25,30,36,39,41,43

 +3VS5 5,7,12,13,14,15,16,23,26,33,43

 +5VS5 23,30,35,37,43

 +5V 5,15,20,23,24,25,27,28,29,30,33,36,37,39,42,43

 +LANVCC

 +VIN

+5VPCU
C/C: 8A
P/C: 10A

TON: 5V / 3.3V
GND = 400 / 500KHz
REF = 400 / 300KHz
VCC = 200 / 300KHz

Place these C.
close to FETs

3.3 Volt +/- 5%

+3VPCU
C/C: 8A
P/C: 10A

SI-1 Modified
-ECAP6 3X6 1-7 2-QT8

+3V
6.76A

s0-s1

+3VS5
0.5A

S0-S5

+3VSUS
1.84A

S0-S3

+5VSUS
4.5A

S0-S3

+LANVCC
0.27A

For EMI-SI

+5V
4.31A

s_0-s_1

PC195

USD 

For ENI, ST

F01 EMI-31



PC194
0.1U/10VC_4

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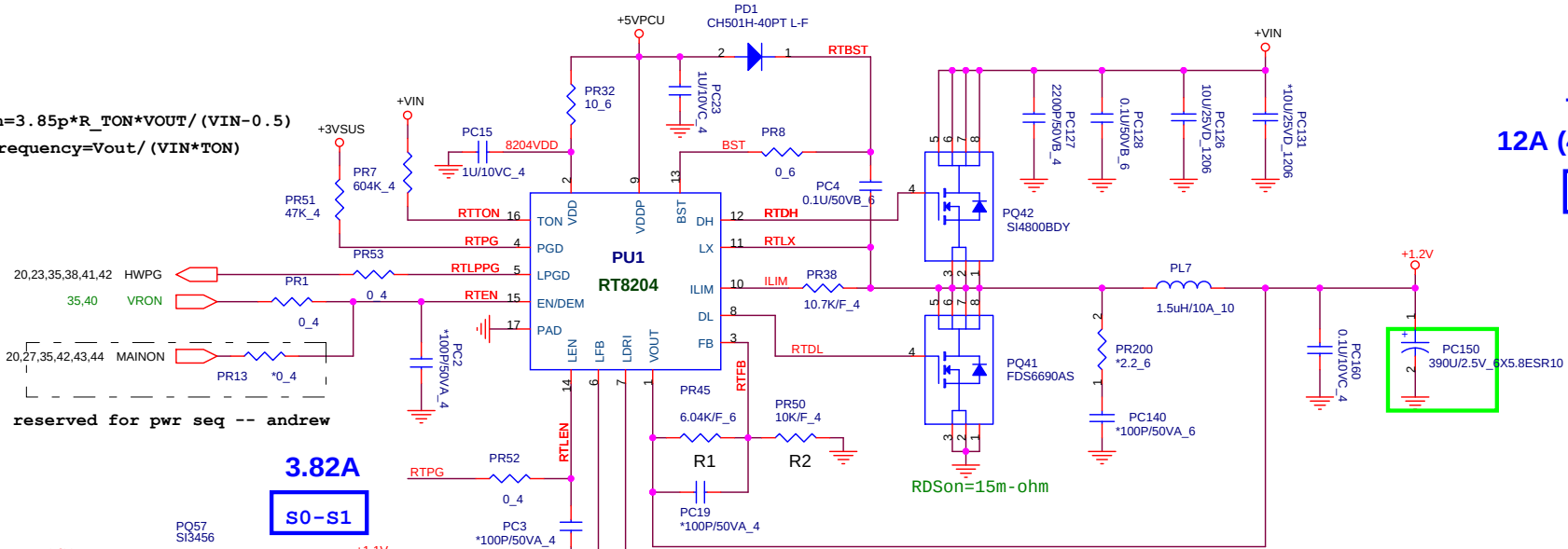


NR5/RD5

$$T_{on} = 3.85p \cdot R_{TON} \cdot V_{OUT} / (V_{IN} - 0.5)$$

$$Frequency = V_{out} / (V_{IN} \cdot T_{ON})$$

+1.2V
12A (4.3A+7.0A)
S0-S1



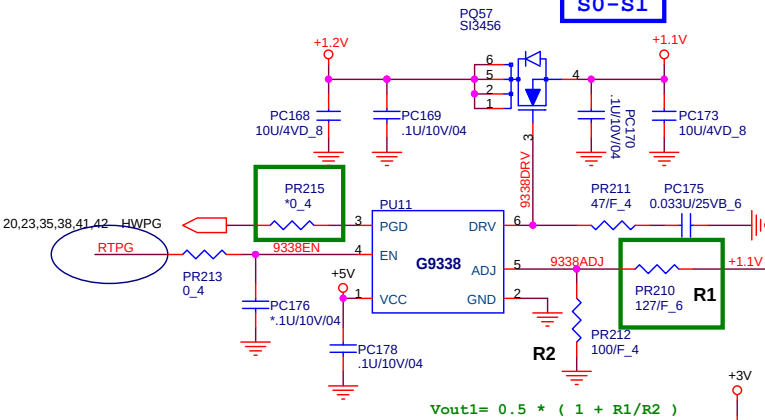
3.82A
S0-S1

$$V_o = 0.75 (R_1 + R_2) / R_2$$

$$R_{ILIM} = I_{LIMIT} \cdot R_{sense} / 20\mu A$$

Keep R2 higher than 10Kohm

+1.1V 9,10,11,18,20,43
+1.2V 2,3,11,12,14,15
+1.1V_DYN 11



+1.1V
7.0A
S0-S1

DYN_PWR_EN	High	Low
+1.1V_DYN	1.0	1.1

PR31 for UMA only



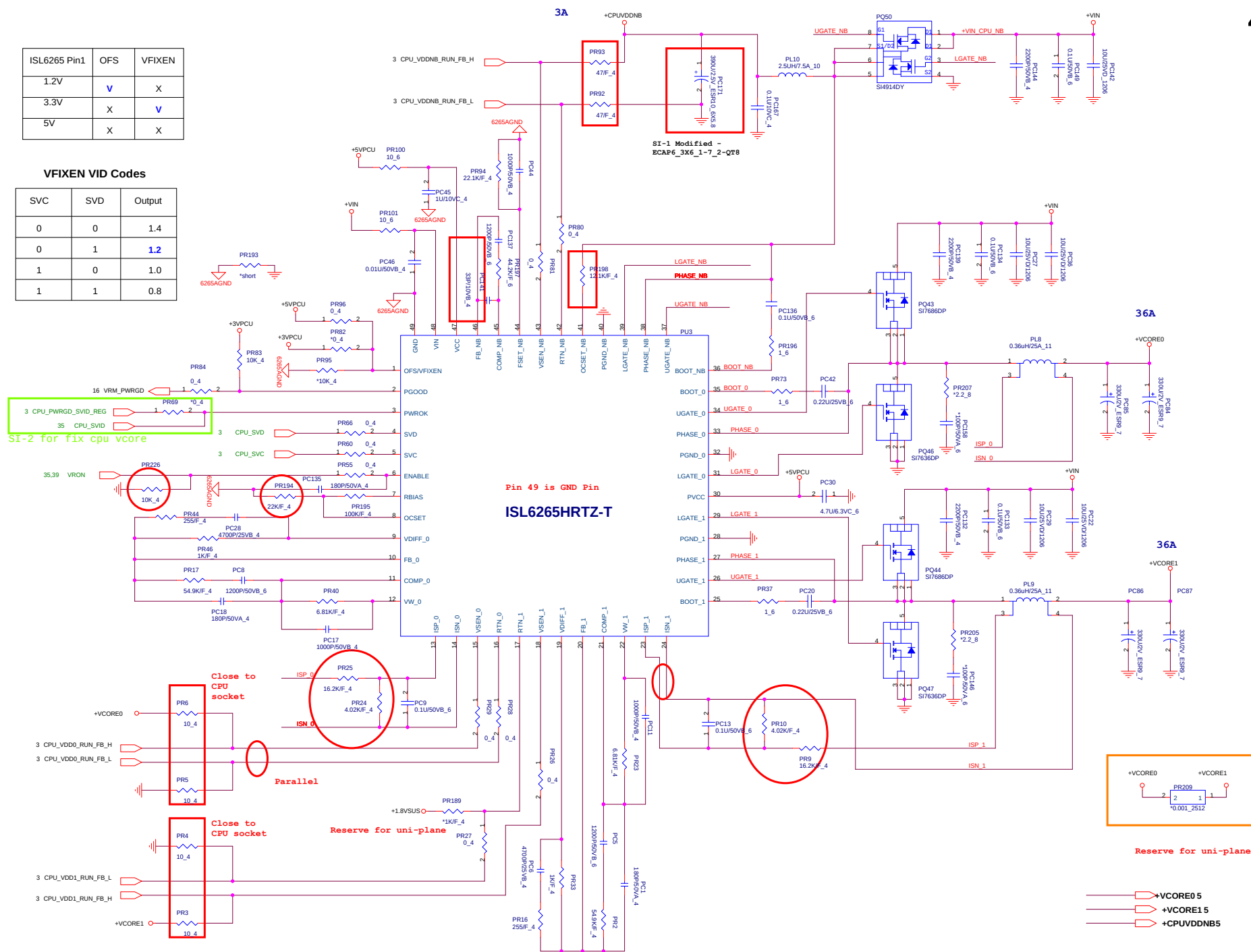
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B	+1.2V & +1.1V(RT8204)	1A
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ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V	X	X

VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8

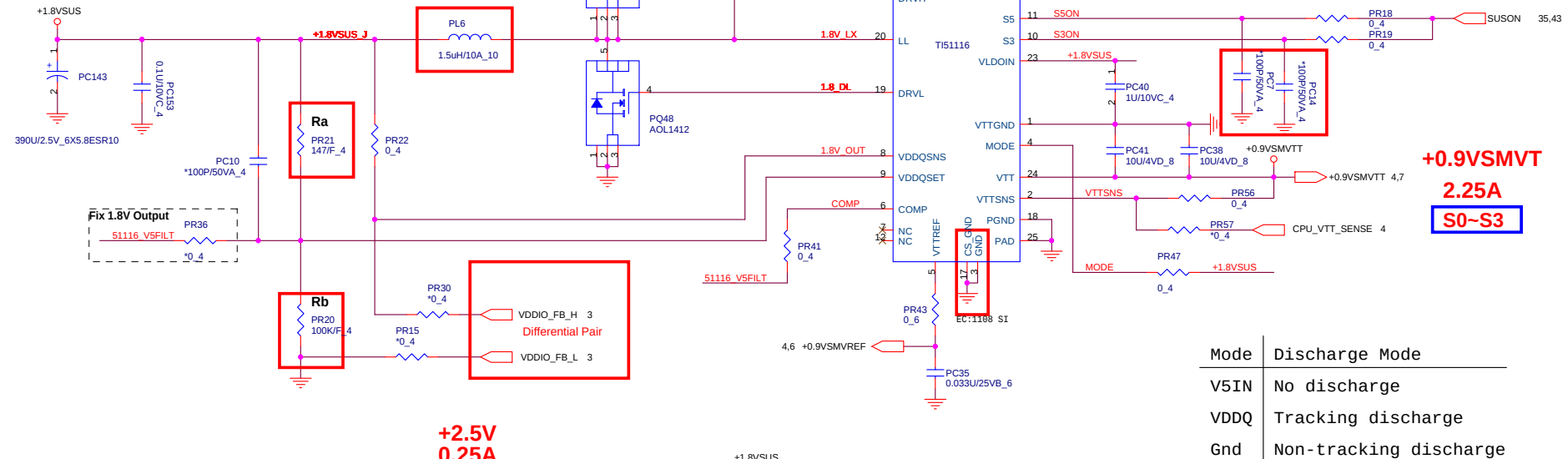


 +2.5V 3
 +1.8VSUS 3,4,5,6,7,40,42,43

$I_{lim}(Valley) = 10\mu A * R_{ILIM}/R_{DS_ON}$
 For OCP set.

+1.8VSUS
23.65A
S0~S3

$R_a = (V_{out} - 0.75) / 0.75 * R_b$
 R_b value from 100K to 300K ohm



+2.5V
0.25A
S0~S1

For EMI-SI

+1.8V
10.4A
S0~S1

For EMI-SI

Discrete: SI4856
 UMA: SI4800

$$V_{TRIP}(mV) = R_{TRIP}(Kohm) * 10(\mu A)$$

$$I_{OCP} = V_{trip}/R_{ds_on} + I_{Ripple}/2$$

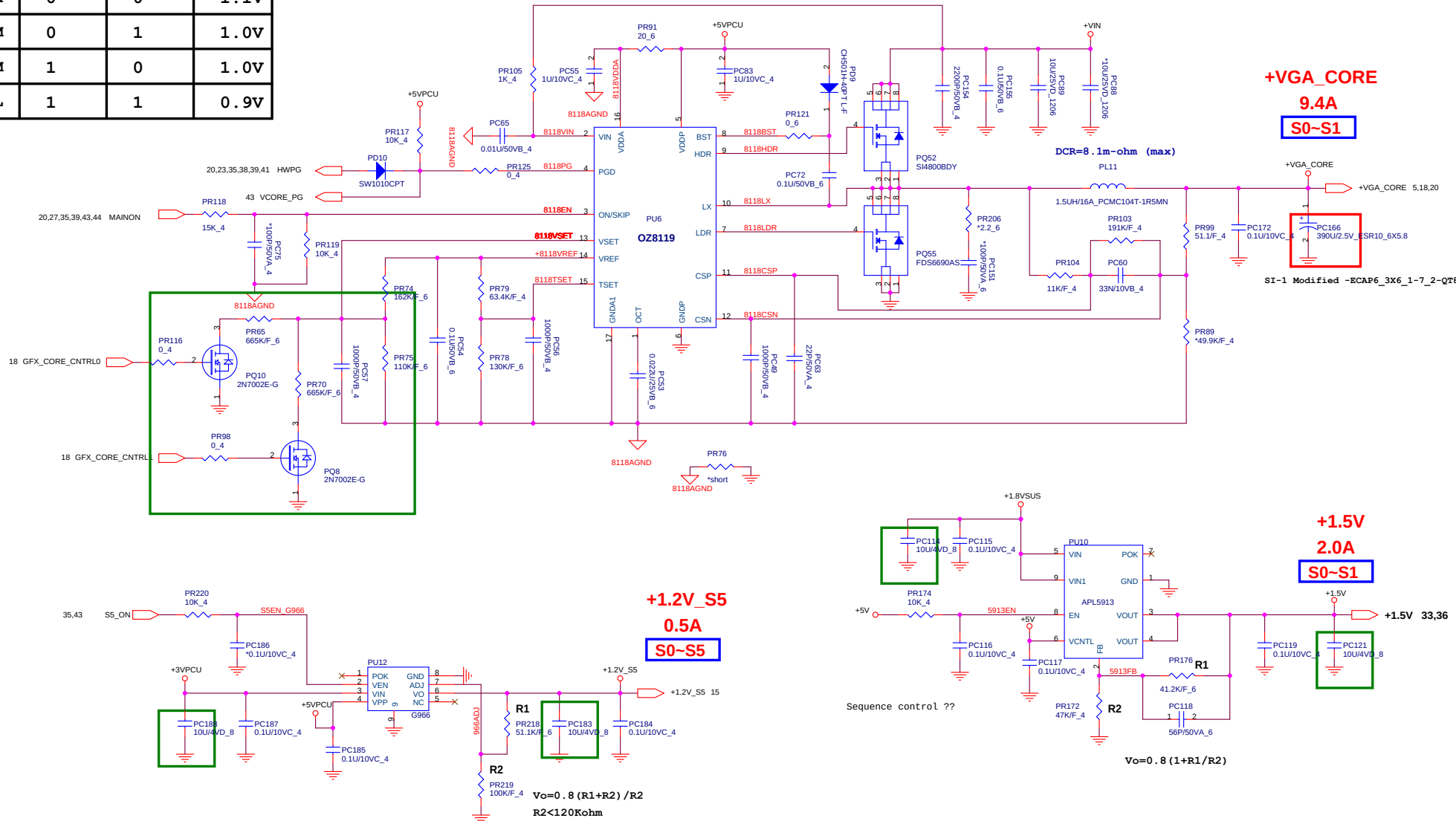
VDDQSET	VDDQ(V)	VTTREF and Vtt	Note
GND	2.5	V_ vddqsns/2	DDR
V5IN	1.8	V_ vddqsns/2	DDR2
FB	adjustable	V_VDDQSNS/2	1.5V<VDDQ<3V

ATI M82-SE

42

+VGA_CORE5,18,20
+1.2V_S5 15
+1.5V 33,36

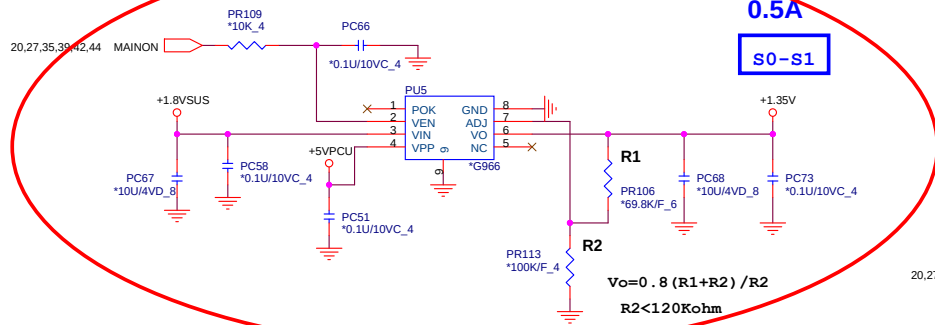
	PWRCNTL1	PWRCNTL0	V-CORE
H	0	0	1.1V
M	0	1	1.0V
M	1	0	1.0V
L	1	1	0.9V



SI-1 Modified - can remove +1.35V for AMD update

0.5A

S0-S1



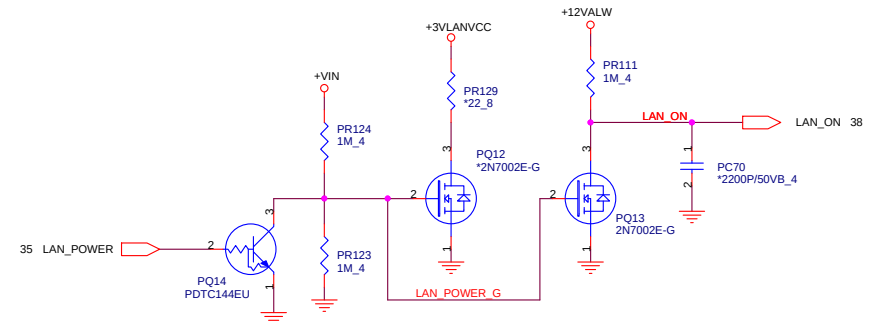
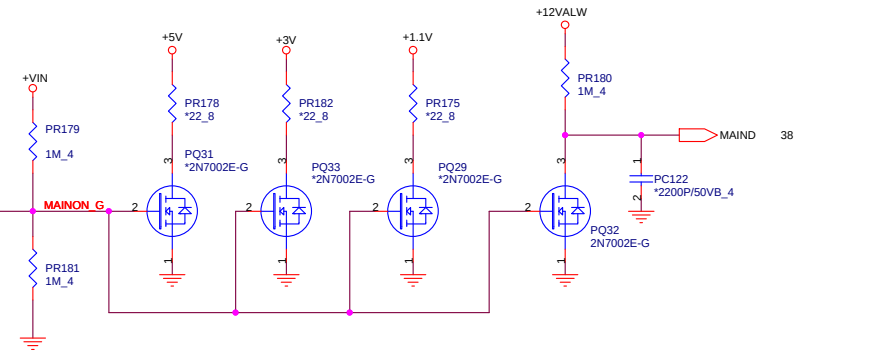
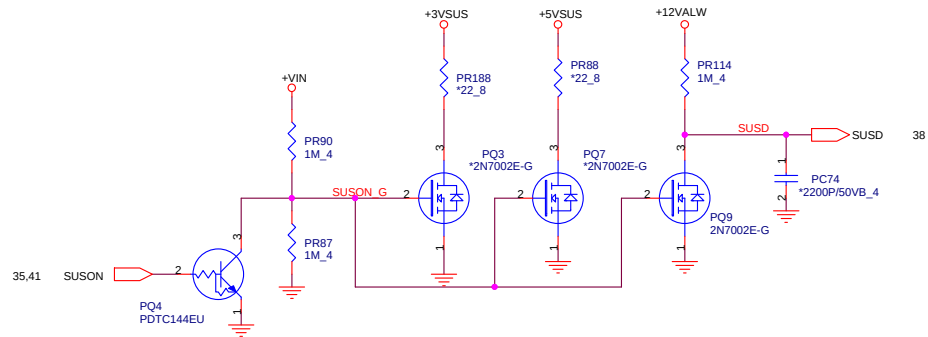
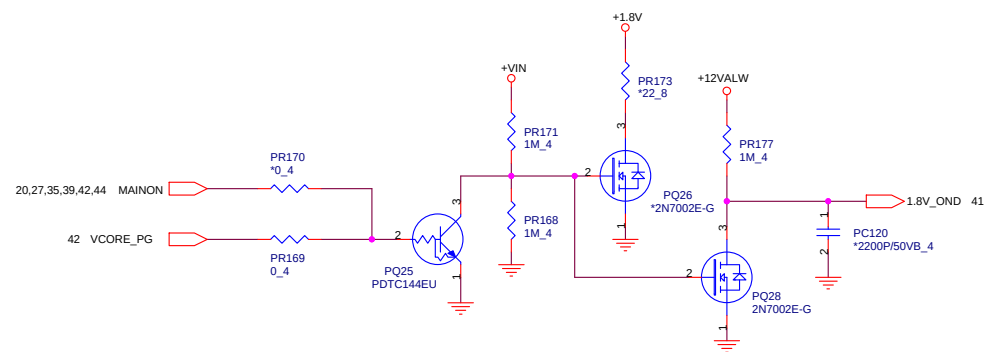
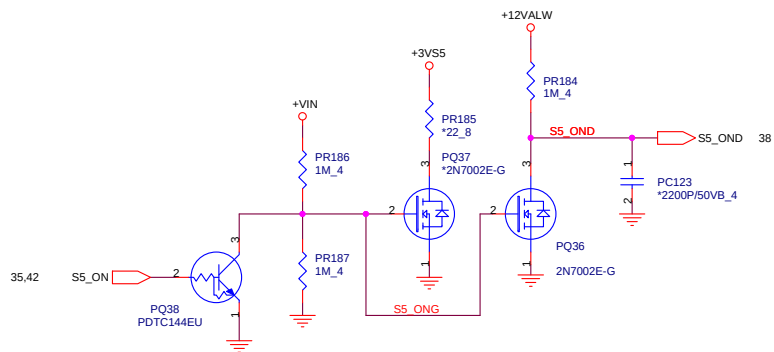
20,27,35,39,42,44

MAINON

2

PQ30

PDTTC144EU

*For Discrete Only*

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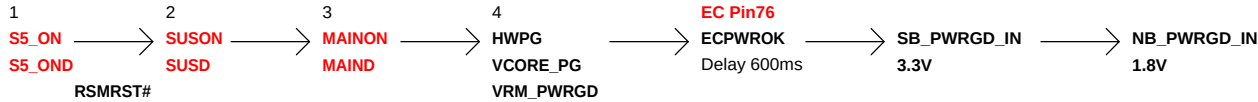
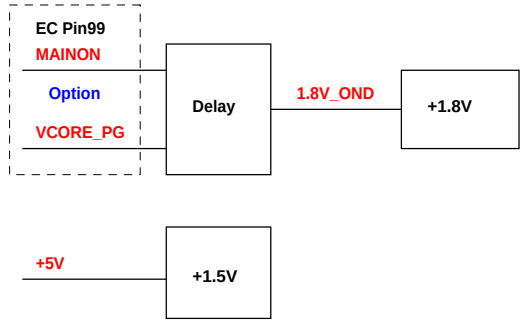
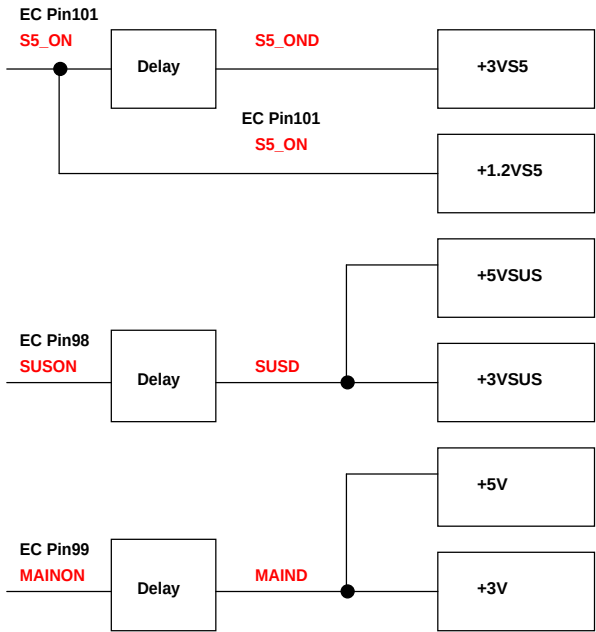
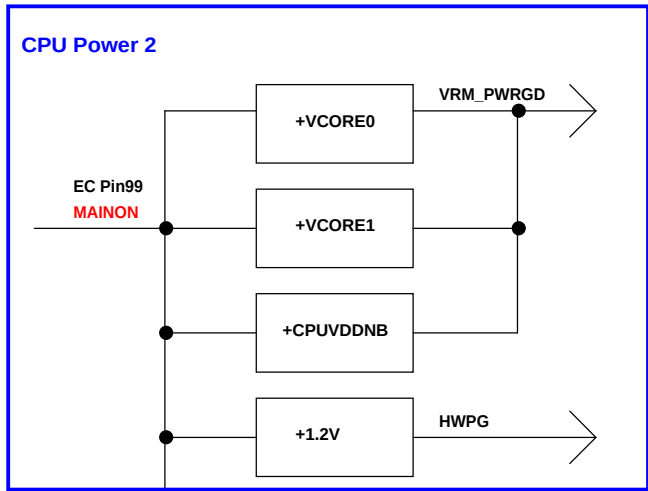
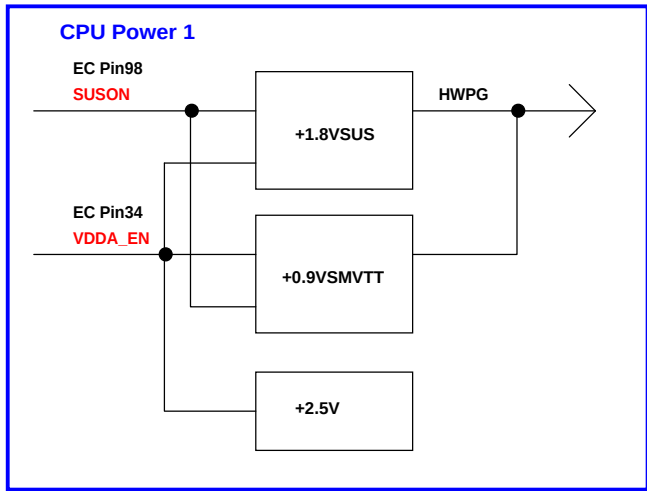
Size
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Document Number
DISCHARGE

Rev
 1A

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