Compal confidential

Schematics Document

Mobile Merom uFCPGA with Intel Crestline + ICH8-M core logic

IBT00 LA-3262P Discrete VGA (M64)

2007-08-02 REV:1A

機密 等級 研發二部 產品人員 產品日期 解密日期

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.			
Title: Cover Sheet			
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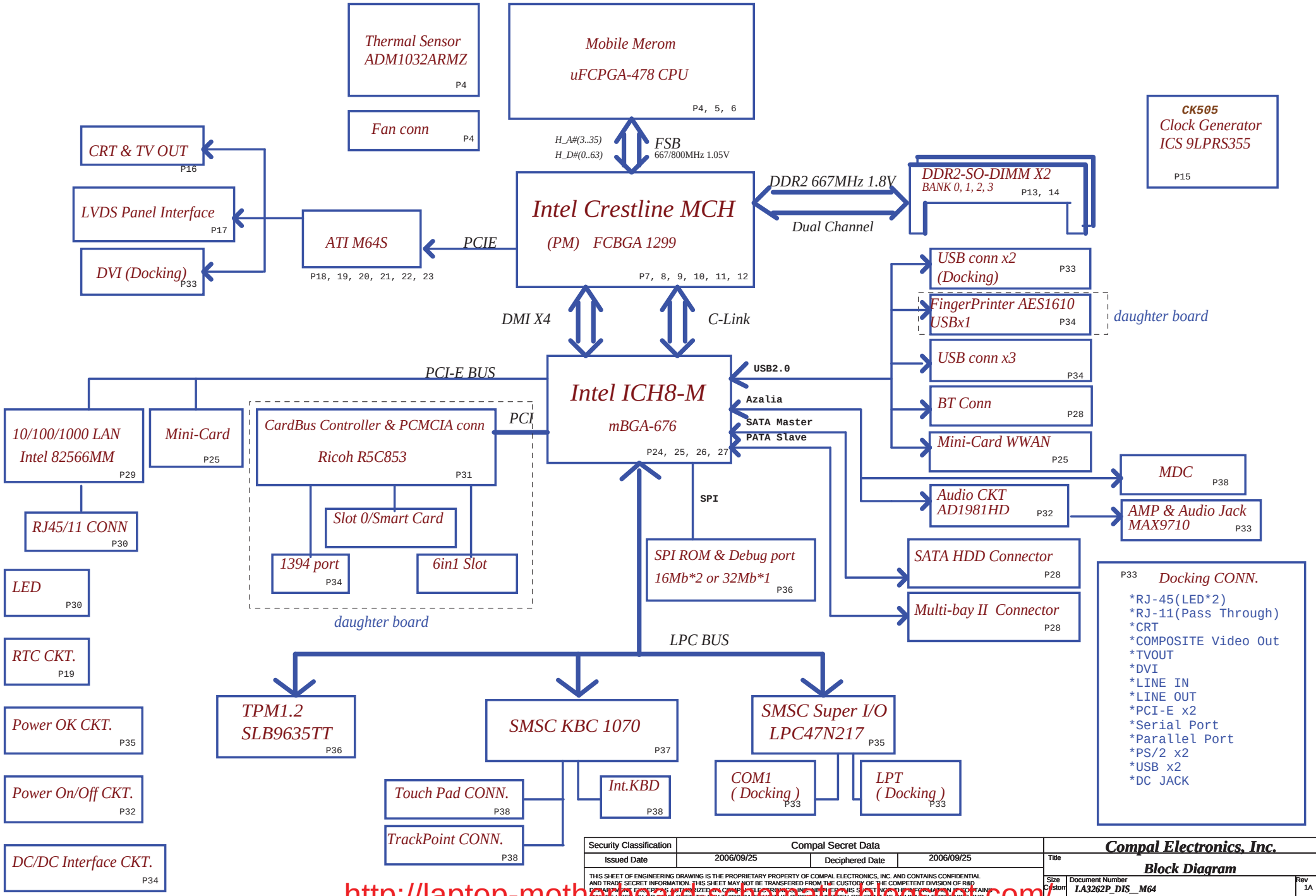
File Name : LA-3262P

Chimay Discrete



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Title: Block Diagram		
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Voltage Rails

O MEANS ON X MEANS OFF

power plane / State	+B LDO3 LDO5	+5VALW +3VALW	+1.8V +5V +0.9V	+5VS +3VS +2.5VS +1.8VS +1.5VS +1.25VS +VGA_CORE +CPU_CORE +VCCP	+3VM +1.05VM +1.25VM	CLOCK
S0	O	O	O	O	O	O
S3/M1	O	O	O	X	O	O
S3	O	O	O	X	O	O
S5 S4/AC	O	O	X	X	O	O
S5 S4/ Battery only	O	X	X	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X	X	X

PCI Devices

EXTERNAL	IDSEL#	REQ/GNT#	PIRQ
CARD BUS & 1394	AD22	2	C,D,E,G

DMA Channel	Device
DMA0	MODEM / LAN
DMA1	ECP
DMA2	~~FLOPPY DISK~~
DMA3	AUDIO
DMA4	(Cascade)
DMA5	Unused
DMA6	Unused
DMA7	Unused

USB PORT#	Destination
0	Walk-up0 (Right side)
1	Fingerprint
2	Reserve
3	WWAN
4	Walk-up1 (Left Side)
5	Walk-up2 (Left Side)
6	Bluetooth
7	Reserve
8	Docking
9	Docking

IRQ	Device
0	System Timer
1	Keyboard
2	N/A
3	Serial port (COM2),LAN/Modem
4	Serial port (COM1)
5	Audio/VGA
6	~~Floppy~~
7	Parallel port
8	System CMOS/Real-time clock
9	Microsoft ACPI
10	N/A,Momem,LAN
11	Mass strorage control/ PCI simple communication control
12	synactic PS2 port GlidePAD
13	Numeric Data Process
14	Primary IDE interface,HDD
15	Secondary IDE innterface,CD-ROM
16	Mobile Intel Crestline Express Chipset Family Microsoft UAA Bus Driver for High Definition Audio Intel 82801H (ICH8 Family) PCI Express Root Port -27D0 Broadcom NetXtreme Gigabit Ethernet
17	Intel 82801H (ICH8 Family)PCI Express Root Port - 27D2 Broadcom 802.11b/g WLAN Intel 82801H (ICH8 Family)USB Universal Host Controll
18	Intel 82801H (ICH8 Family)USB Universal Host Controll Ricoh R5C853 Cardbus Control Ricoh R5C853 Integrates FlashMedia Control Ricoh R5C853 Gemcore based SmartCard Control
19	Intel 82801H (ICH8 Family)PCI Express Root Port - 27D6 Intel 82801H (ICH8 Family)USB Universal Host Controll
20	Intel 82801H (ICH8 Family)USB Universal Host Controll Intel 82801H (ICH8 Family)USB2 Enhanced Host Controll
21	Intel 82801H (ICH8 Family)USB Universal Host Controll
22	SDA Standard Compliant SD Host Controller
23	HP Mobile Data Protection Sensor

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Title: Notes List

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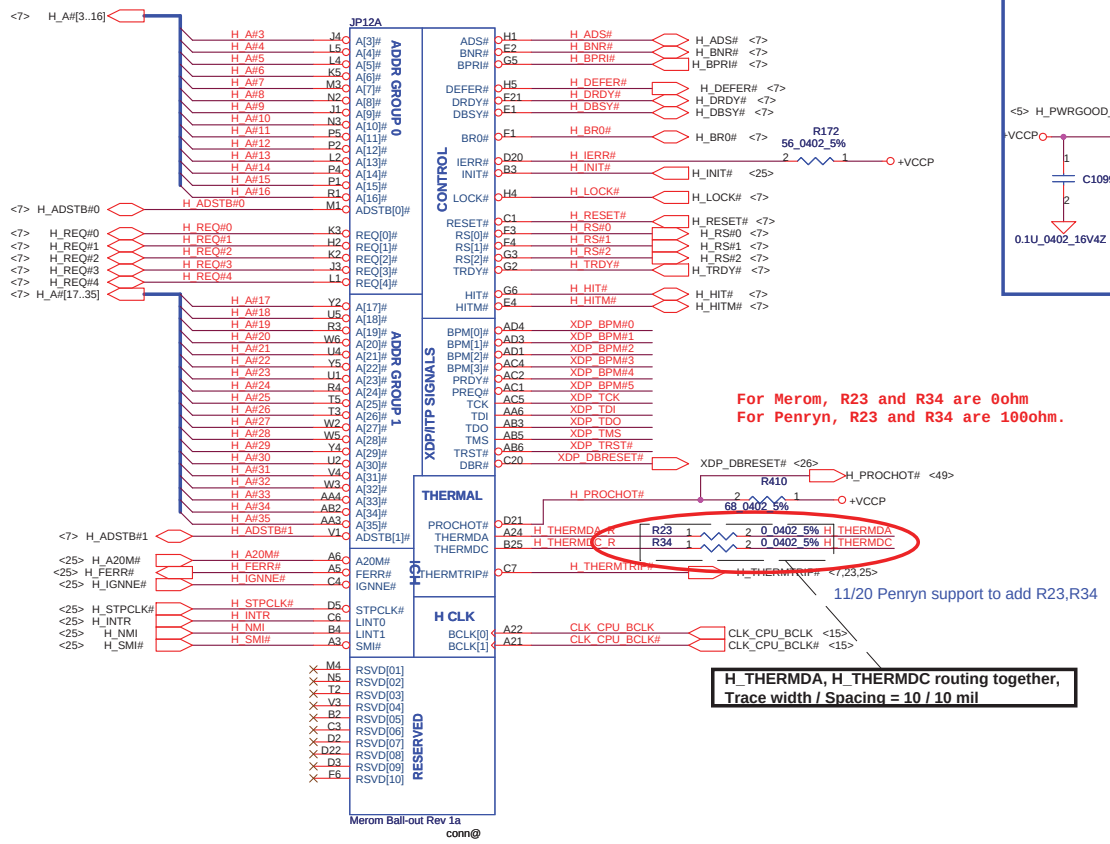
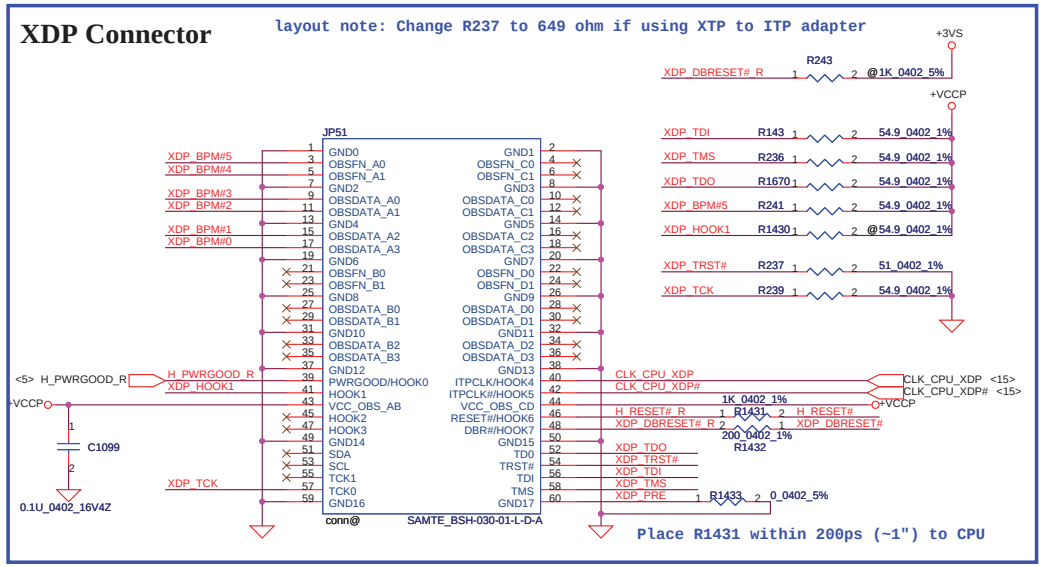
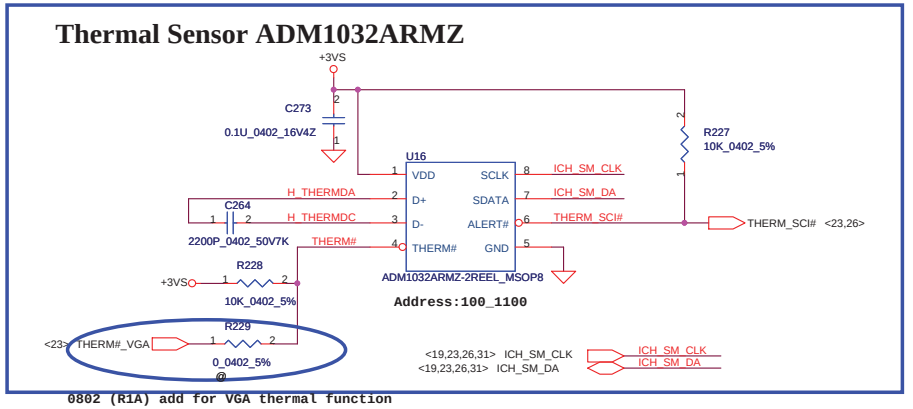


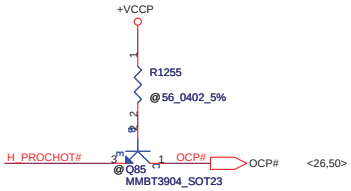


For Merom, R23 and R34 are 0ohm
For Penryn, R23 and R34 are 100ohm.

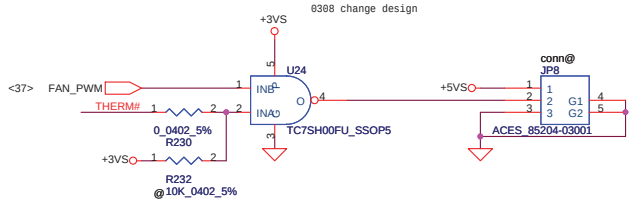
11/20 Penryn support to add R23,R34

H_THERMDA, H_THERMDC routing together, Trace width / Spacing = 10 / 10 mil





PWM Fan Control circuit



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Title	Compal Electronics, Inc.		
	Merom(1/3)-AGTL+/XDP		
Size: Custom	Document Number: LA3262P_DIS__M64		Rev: 1A
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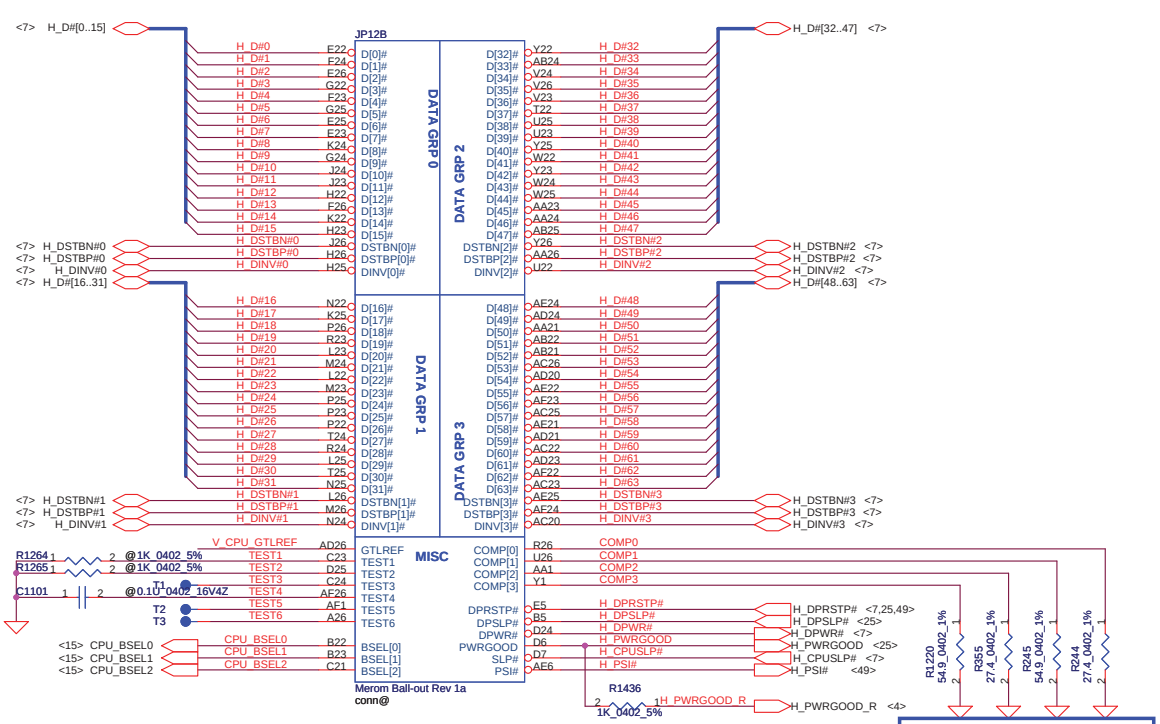
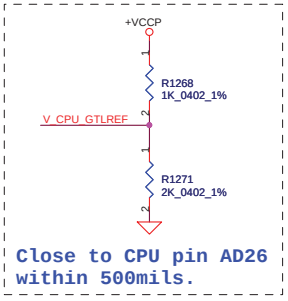


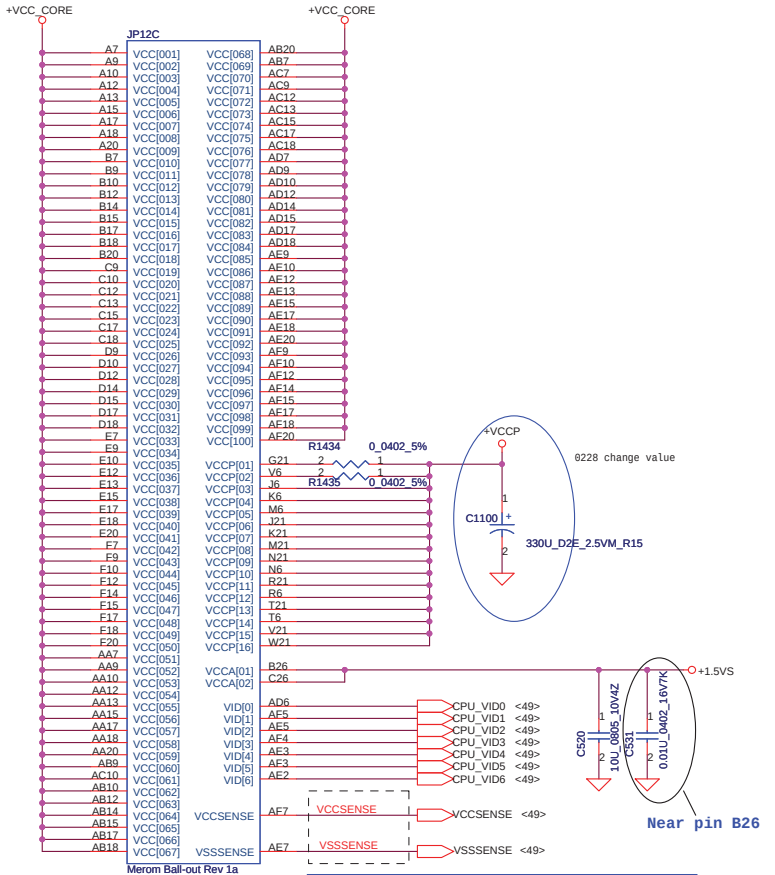
layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

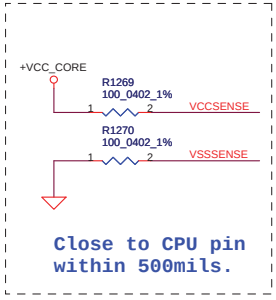
Resistor placed within 0.5" of CPU pin.Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.



Close to CPU pin AD26 within 500mils.



Length match within 25 mils. The trace width/space/other is 20/7/25.



Close to CPU pin within 500mils.

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Compal Electronics, Inc.	
Title	Merom(2/3)-AGTL+/PWR
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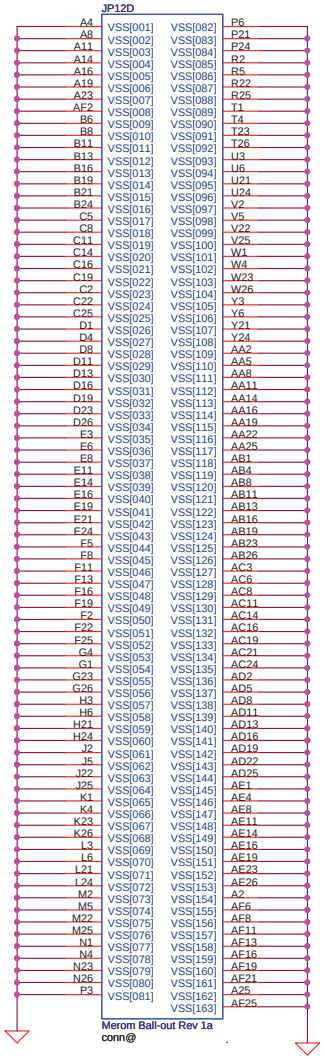
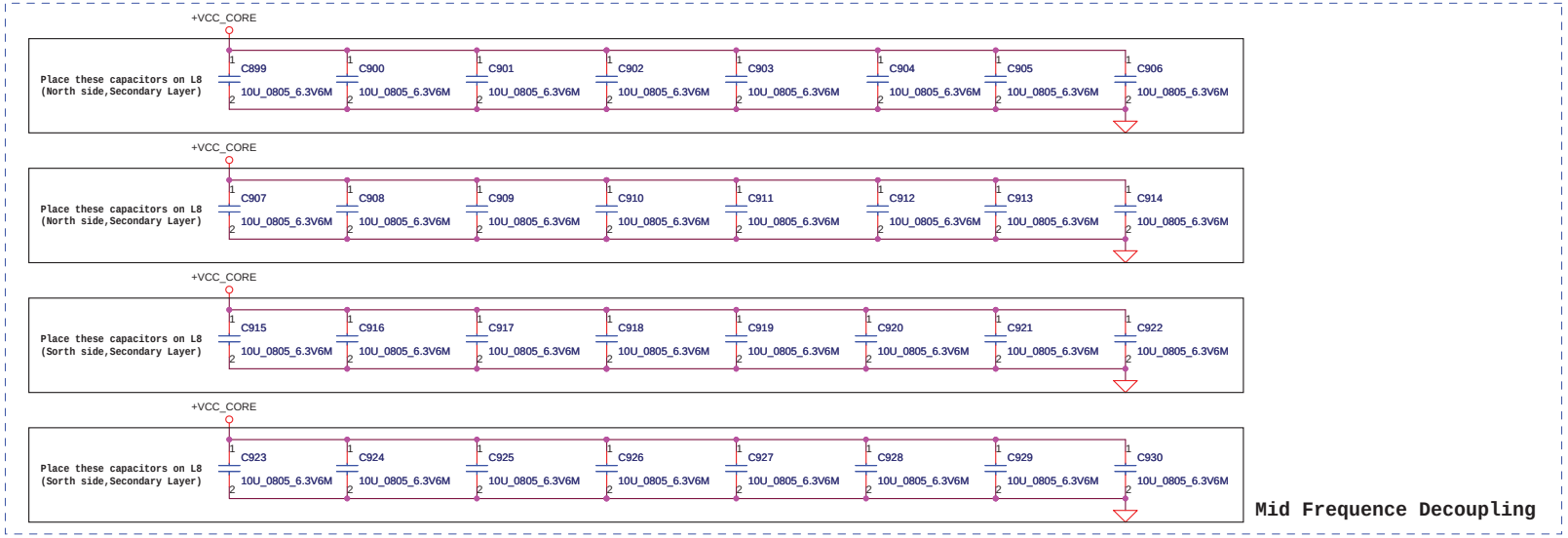
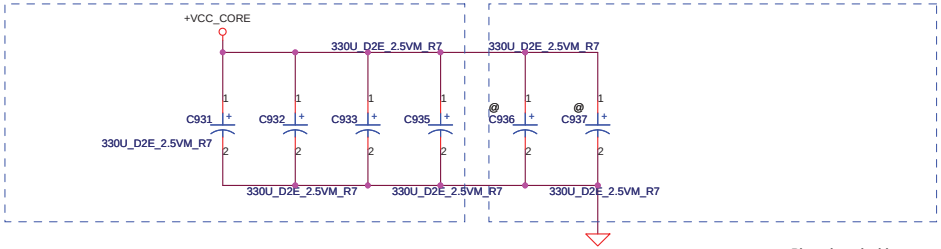
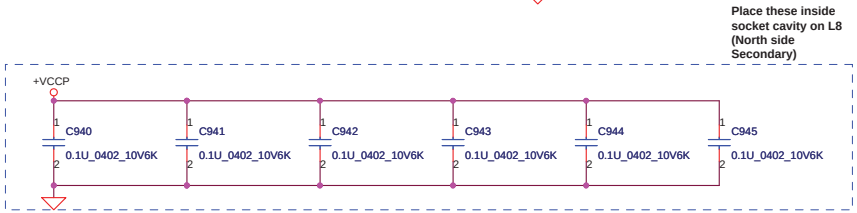




Near CPU CORE regulator

ESR <= 1.5m ohm
Capacitor > 1980uF





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Compal Electronics, Inc.			
Title: Merom(3/3)-GND&Bypass			
Size: Custom	Document Number: LA3262P_DIS_M64		Rev: 1A
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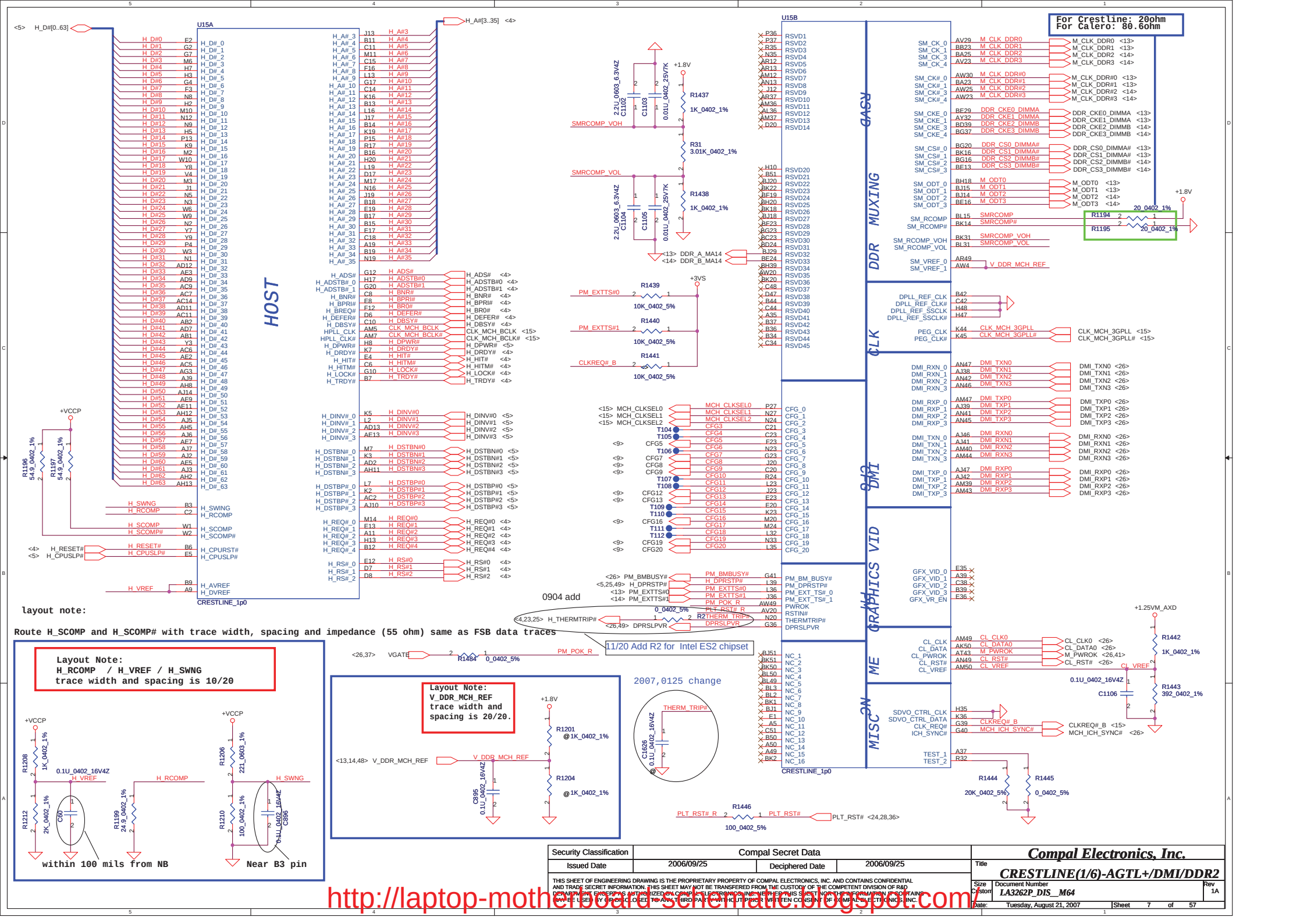

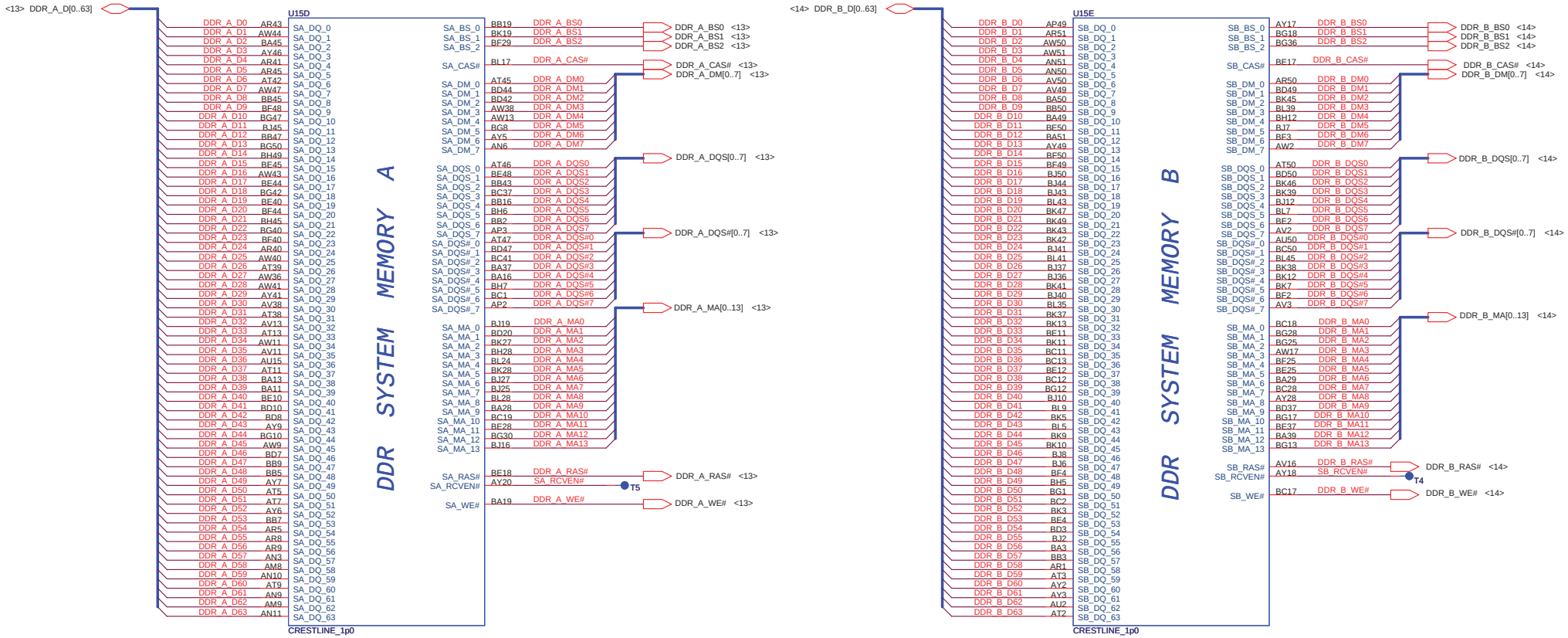

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Compal Electronics, Inc.			
Title: CRESTLINE((2/6)-DDR2 A/B CH			
Size: Custom	Document Number: LA3262P_DIS__M64		Rev: 1A
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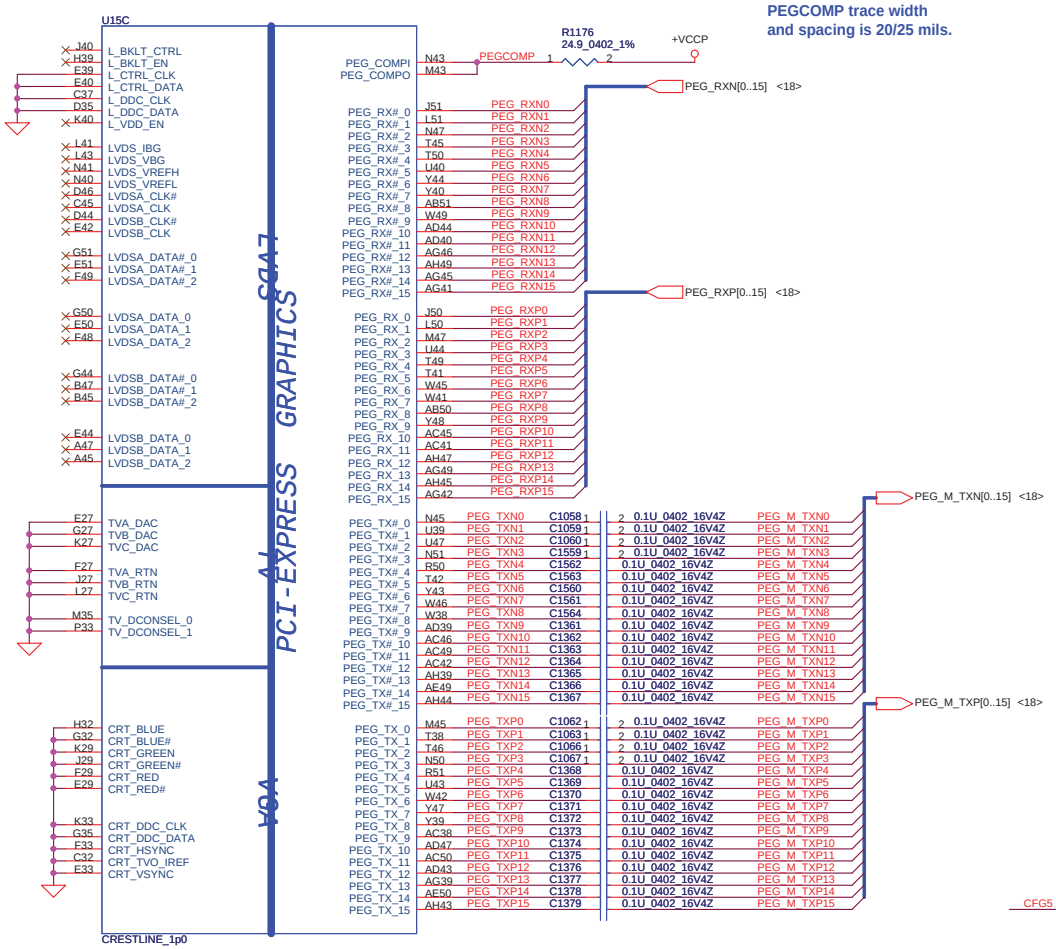
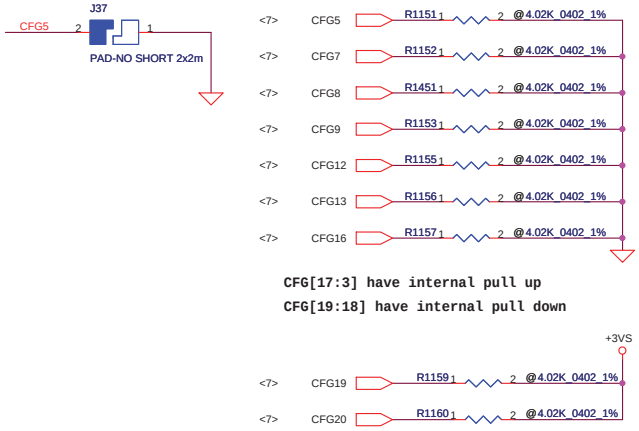


PEGCOMP trace width
and spacing is 20/25 mils.

Strap Pin Table

CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIE)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational. * 1 = PCIE/SDVO are operating simu.



CFG[17:3] have internal pull up
CFG[19:18] have internal pull down

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Issued Date	2006/09/25	Deciphered Date	2006/09/25

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Title: CRESTLINE((3/6)-VGA/LVDS/TV

Size	Document Number	Rev
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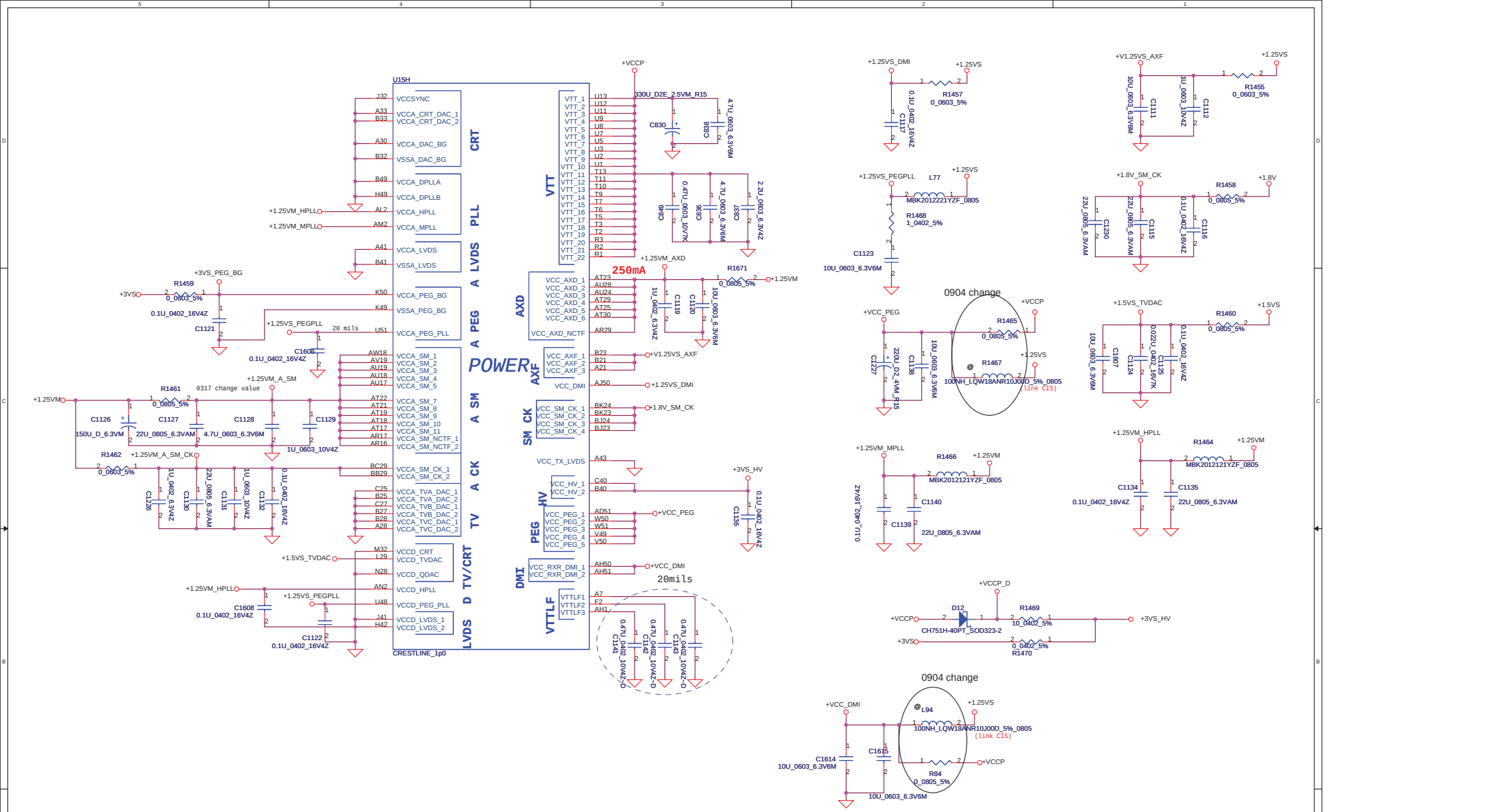

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Title: **CRESTLINE(4/6)-PWR**

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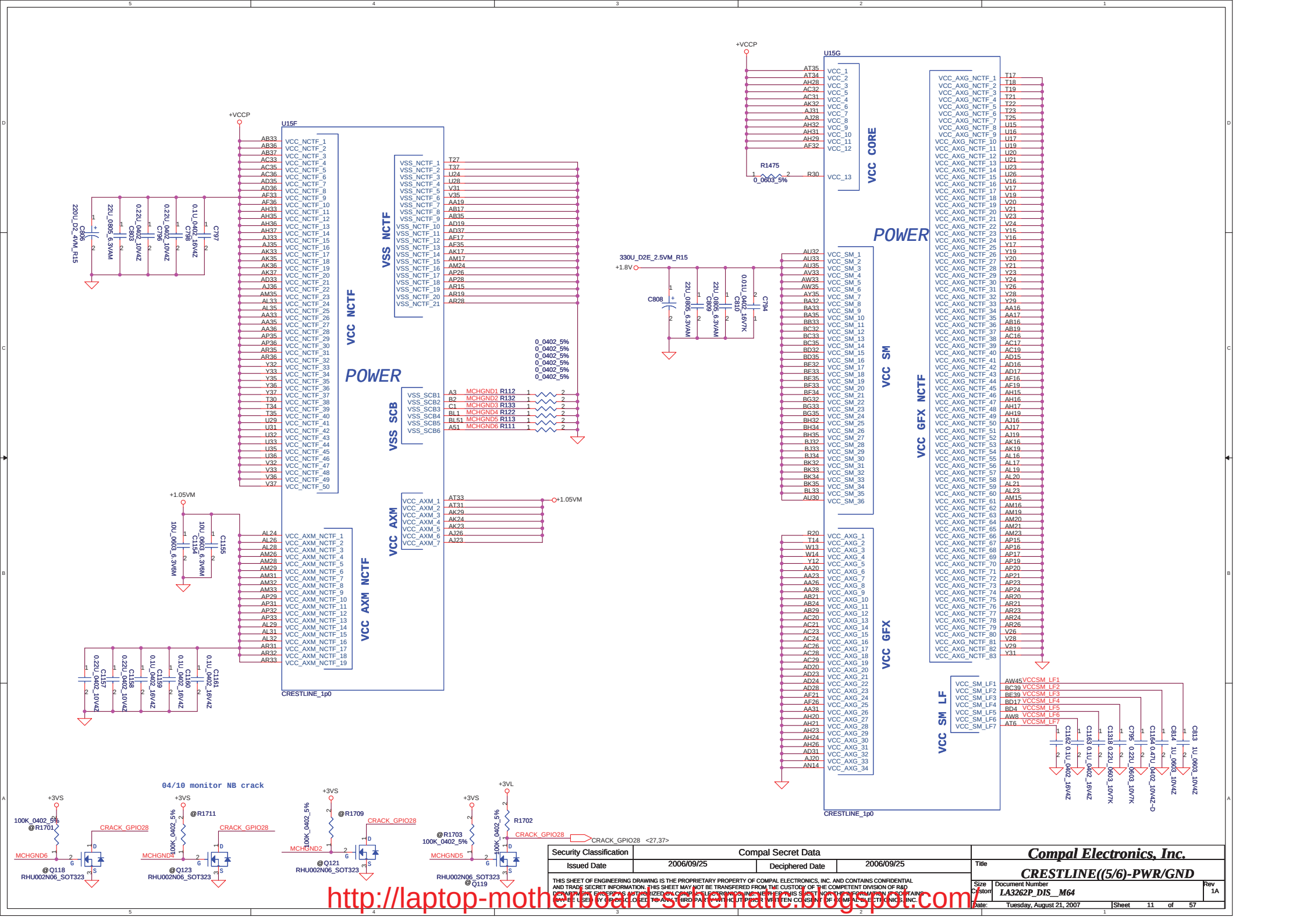

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Title: **CRESTLINE((5/6)-PWR/GND**

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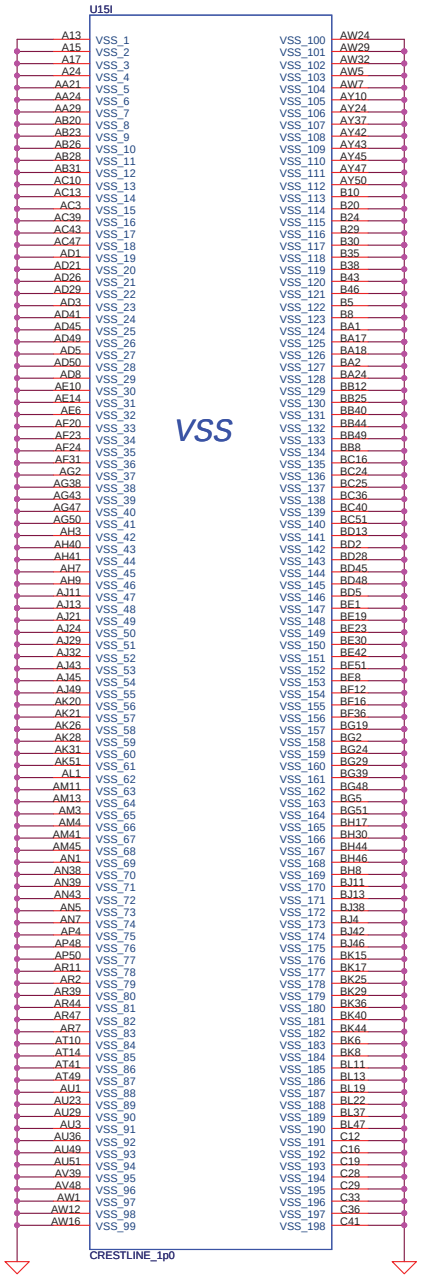

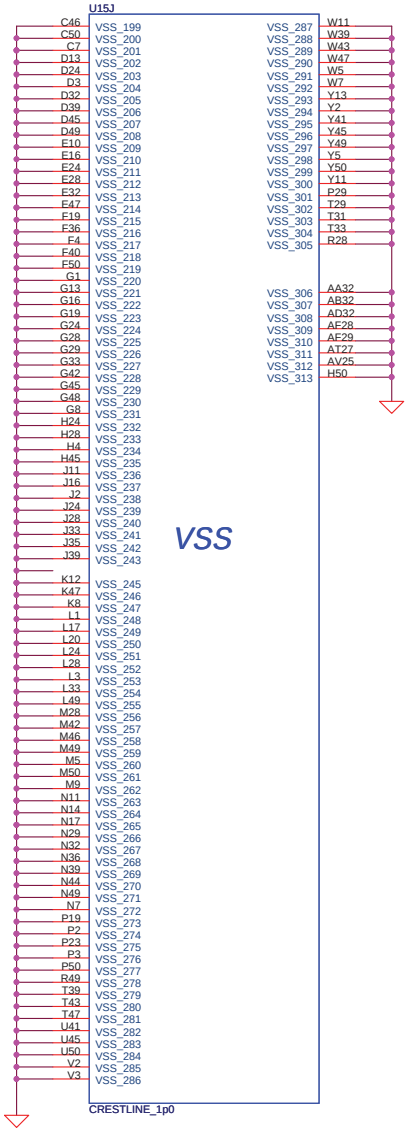

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Title	CRESTLINE((6/6)-PWR/GND	
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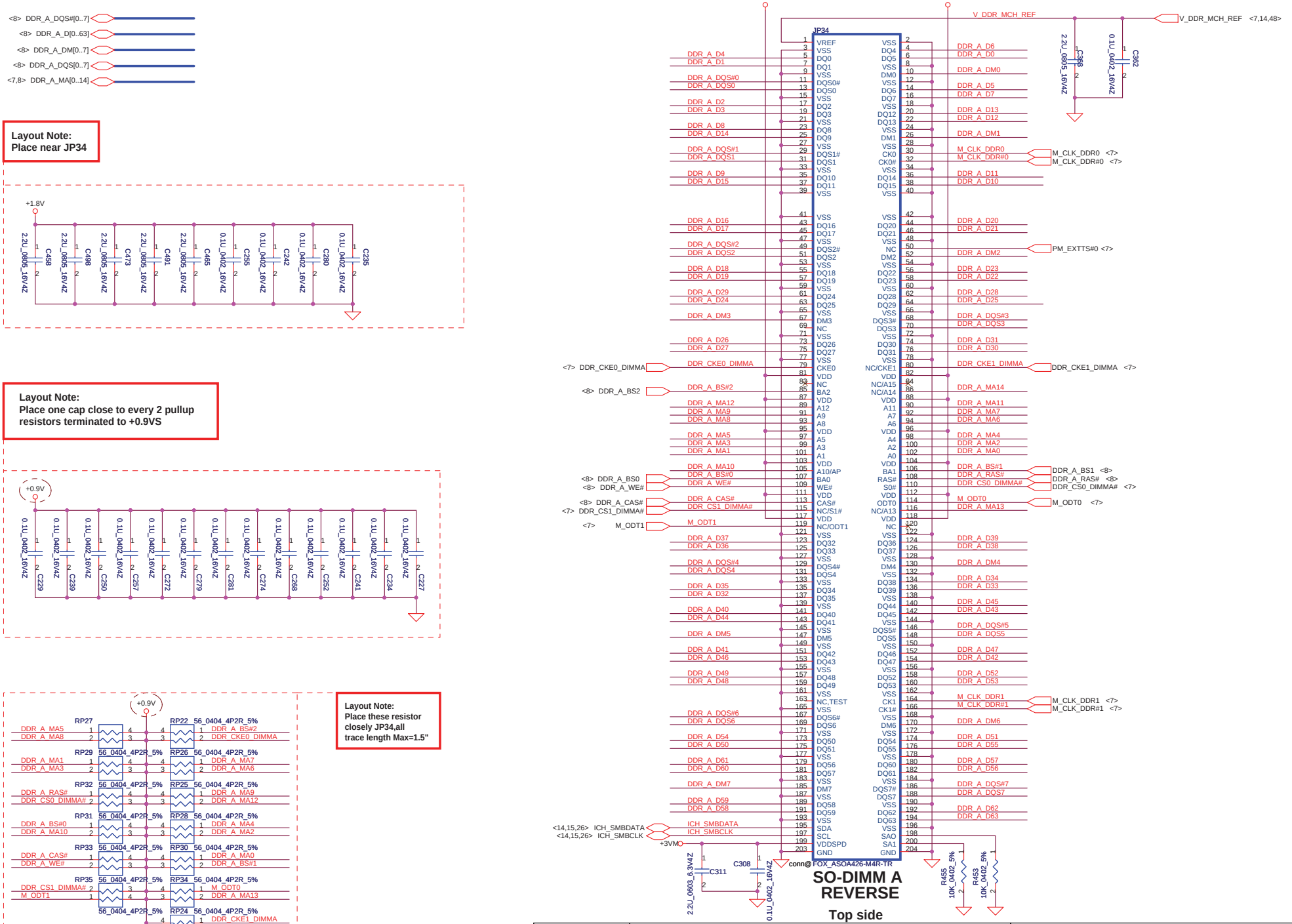

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Issued Date	2006/09/25	Deciphered Date	2006/09/25

Compal Electronics, Inc.			
Title: DDRII-SODIMM SLOT1			
Size: Custom	Document Number: LA3262P_DIS__M64		Rev: 1A
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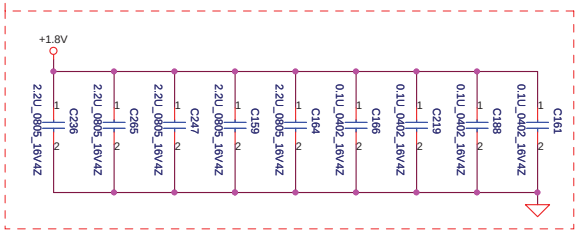
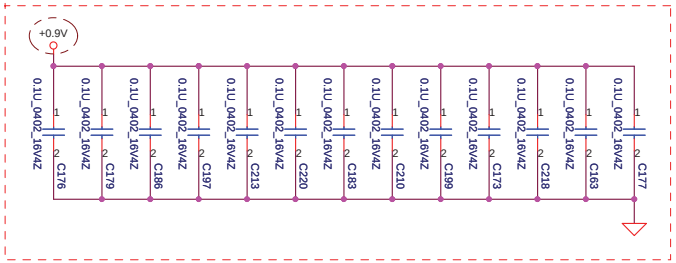
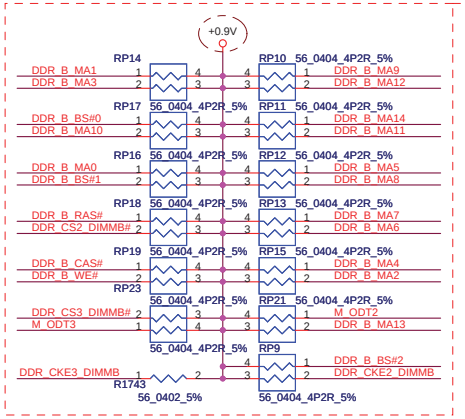
<8> DDR_B_DQS#[0..7]
<8> DDR_B_D[0..63]
<8> DDR_B_DM[0..7]
<8> DDR_B_DQS[0..7]
<7,8> DDR_B_MA[0..14]

Layout Note:
Place near JP10

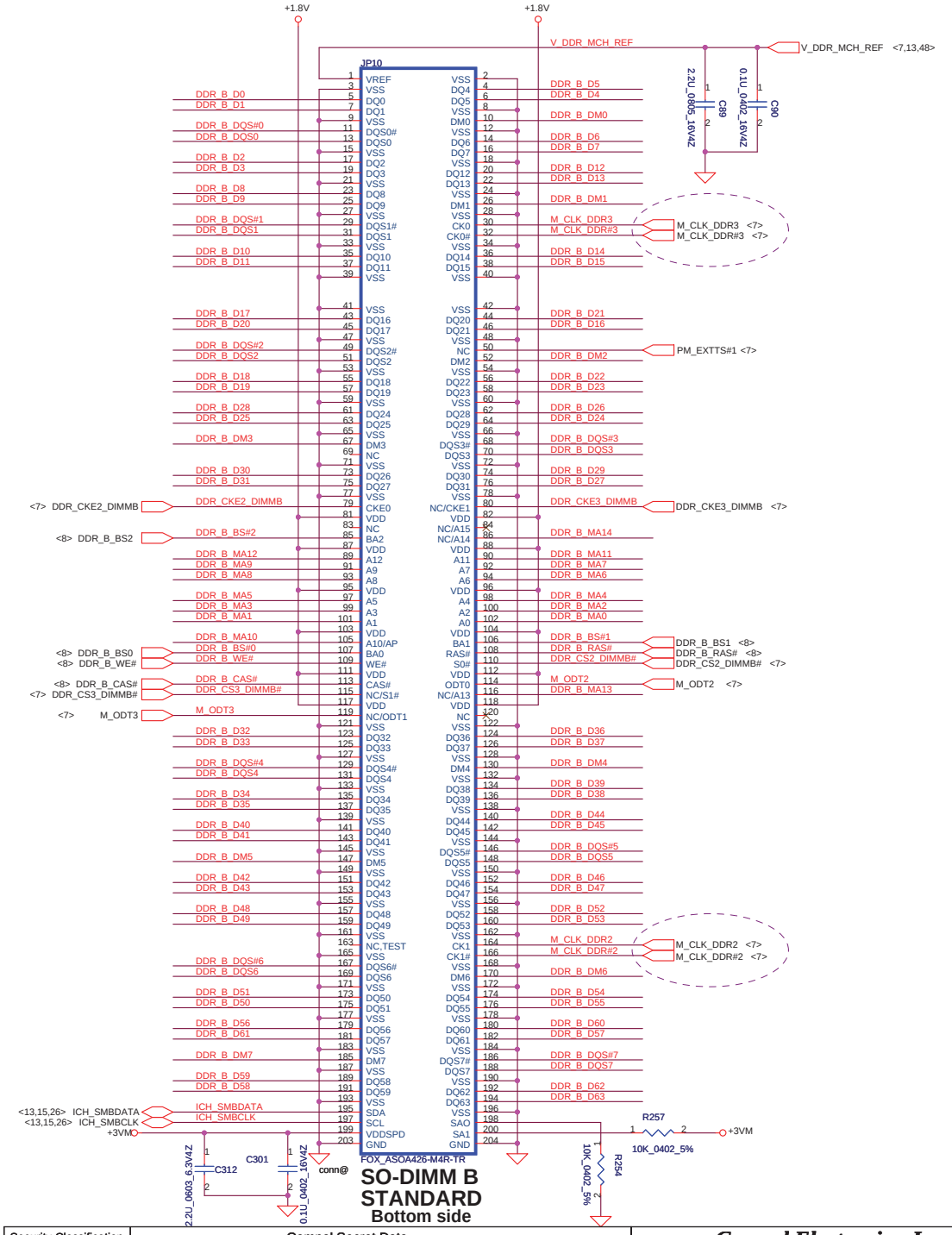


Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS





Layout Note:
Place these resistor closely JP10,all trace length Max=1.5"



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Title: **DDRII-SODIMM SLOT2**

Size	Document Number	Rev
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FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	1	0	200	100	33.3
0	1	1	166	100	33.3

FSB Frequency Selet:

CPU Driven	Stuff	R1107	R1135	R1083			
*(Default)	No Stuff	R1074	R1086	R1098	R1113	R1128	R1139
667MHz	Stuff	R1086	R1139	R1135	R1074	R1139	R1135
	No Stuff	R1083	R1107	R1128			
		R1113	R1098				
800MHz	Stuff	R1135	R1139				
	No Stuff	R1083	R1086	R1098	R1128		
		R1074	R1107	R1113			

+3VM_CK505 — R1066 0_1206_5% — +3VM

C1165 10U_0603_6.3V6M; C1166 0.1U_0402_16V4Z; C1167 0.1U_0402_16V4Z; C1168 0.1U_0402_16V4Z; C1169 0.1U_0402_16V4Z; C1170 0.1U_0402_16V4Z; C1171 0.1U_0402_16V4Z

Place close to U7

R1068 0_1206_5% — +1.25VM — +1.25VM_CK505

C1172 10U_0603_6.3V6M; C1173 0.1U_0402_16V4Z; C1174 0.1U_0402_16V4Z; C1353 10U_0603_6.3V6M; C1354 0.1U_0402_16V4Z; C1355 0.1U_0402_16V4Z

C353 CLK_48M_ICH 5P_0402_50V8C
C357 CLK_14M_ICH 4.7P_0402_50V8C
C372 CLK_PCI_ICH 4.7P_0402_50V8C
C373 CLK_14M_KBC 4.7P_0402_50V8C
C374 CLK_14M_SIO 4.7P_0402_50V8C
C375 CLK_PCI_EC 4.7P_0402_50V8C
C376 CLK_PCI_TCG 4.7P_0402_50V8C
C378 CLK_PCI_PCM 4.7P_0402_50V8C
C379 CLK_PCI_SIO 4.7P_0402_50V8C
C380 CLK_DEBUG_PORT 5P_0402_50V8C

R1074 @ — +VCCP 56_0402_5%
R1078 2.2K_0402_5% — FSA — MCH_CLKSEL0 <7>
<5> CPU_BSEL0 — R1083 0_0402_5% — R1079 1K_0402_5% — R1086 @1K_0402_5%

1111 Add CLRP4,CLRP5 for 667/800 FSB select
SHORT CLRP5, NO SHORT CLRP4 -- FSB 800
SHORT CLRP4, NO SHORT CLRP5 -- FSB 667

+VCCP — R1098 @1K_0402_5% — FSB — MCH_CLKSEL1 <7>
<5> CPU_BSEL1 — R1107 0_0402_5% — R1105 1K_0402_5% — @R1113 0_0402_5%

+VCCP — R1128 @1K_0402_5% — R1130 10K_0402_5% — FSC — MCH_CLKSEL2 <7>
<5> CPU_BSEL2 — R1135 0_0402_5% — R1131 1K_0402_5% — @R1139 0_0402_5%

U7 — +3VM_CK505

VDD_PCI 2; VDD48 9; VDDPLL3 16; VDDREF 61; VDDSRC 39; VDDCPU 55
+1.25VM_CK505 — VDD96_IO 12; VDDPLL3_IO 20; VDDSRC_IO 26; VDDSRC_IO 36; VDDCPU_IO 49

<26> CLKSATAREQ# — 475_0402_1% R1692 — PCI0/CR#_A 1
<7> CLKREQ#_B — 475_0402_1% R1693 — PCI_CLK1 3 — PCI1/CR#_B
PCI2_TME 4 — PCI2/TME — 22_0402_5% R1097
<31,36> CLK_DEBUG_PORT — 12_0402_5% R1114
<35> CLK_PCI_SIO — 12_0402_5% R1140 — PCI_CLK3 5 — PCI3
<36> CLK_PCI_TCG — 12_0402_5% R1110
<37> CLK_PCI_EC — 12_0402_5% R1141 — 27_SEL 6 — PCI4/27_Select
<31> CLK_PCI_PCM — 22_0402_5% R1117 — ITP_EN 7 — PCIF5/ITP_EN

CLK_XTAL_IN 60 — X1
CLK_XTAL_OUT 59 — X2

<26> CLK_48M_ICH — R1077 33_0402_5% — FSA 10 — USB_48MHZ/FSLA
FSB 57 — FSLB/TEST MODE
<26> CLK_14M_ICH — 33_0402_1% R1087
<35> CLK_14M_SIO — 33_0402_1% R1088
<37> CLK_14M_KBC — 33_0402_1% R1089 — FSC 62 — REF0/FSLC/TEST_SEL
+1.25VM_CK505 — VDDSRC_IO 45

GNDSRC 42; GNDPCI 8; GND48 11; GND 15; GND 19; GNDCPU 52; GNDSRC 23; GNDSRC 29; GNDREF 58

NC 48
SCLK 64 — ICH_SMBCLK <13,14,26>
SDATA 63 — ICH_SMBDATA <13,14,26>
PCI_STOP# 38 — H_STP_PCI# <26>
CPU_STOP# 37 — H_STP_CPU# <26>
CPU0 54 — CLK_CPU_BCLK <4>
CPU0# 53 — CLK_CPU_BCLK# <4>
CPU1_F 51 — CLK_MCH_BCLK <7>
CPU1#_F 50 — CLK_MCH_BCLK# <7>
SRC8/ITP 47 — @R1033 0_0402_5% — R_CPU_XDP R1447 0_0402_5% — CLK_CPU_XDP <4>; CLK_PCIE_Rob <31>
SRC8#/ITP# 46 — R_CPU_XDP# 0_0402_5% — CLK_PCIE_Rob# <31>; CLK_CPU_XDP# <4>
R1448 @R1143
SRC10 35 — CLK_PCIE_DOCK# <39>
SRC10# 34 — CLK_PCIE_DOCK <39>
SRC11/CR#_H 33 — CLKREQ# H — R1695 — R149 10K_0402_5% +3VS — 475_0402_1% — CPPE# <39>
SRC11#/CR#_G 32 — R_CLKREQ# G — R1694 — 475_0402_1% — CLKREQ#_G <31>
R150 10K_0402_5% +3VS
SRC9 30 — CLK_PCIE_MCARD <31>
SRC9# 31 — CLK_PCIE_MCARD# <31>
SRC7/CR#_F 44 — R_CLKREQ# F — R1900 475_0402_1% — CLKREQ# F — R1899 10K_0402_5% +3VS — CLKREQ#_F
SRC7#/CR#_E 43 — R_CLKREQ# E — @R1901 475_0402_1% — CLKREQ# E — @R1902 10K_0402_5% +3VS — CLKREQ#_E <19,31>
SRC6 41 — CLK_PCIE_VGA <18>
SRC6# 40 — CLK_PCIE_VGA# <18>
SRC4 27 — CLK_MCH_3GPLL <7>
SRC4# 28 — CLK_MCH_3GPLL# <7>
SRC3/CR#_C 24 — CLK_PCIE_ICH <26>
SRC3#/CR#_D 25 — CLK_PCIE_ICH# <26>
SRC2/SATA 21 — CLK_PCIE_SATA <25>
SRC2#/SATA# 22 — CLK_PCIE_SATA# <25>
SRC1/SE1/27MHz_NonSS 17 — R_27MHz — R1686 0_0402_5%
SRC1#/SE2/27MHz_SS 18 — R_27MSSC — R1687 0_0402_5% — 27M_CLK <19>; 27M_SSC <19>
11/20 For EMI request to install R1687
SRC0/DOT96 13
SRC0/DOT96# 14
CK_PWRGD/PD# 56 — CK_PWRGD <26>

ICS9LPRS355AKLFT_TSSOP64

* Internal Pull-Up Resistor
** Internal Pull-Down Resistor

For ITP_EN, 0 =SRC8/SRC8#; 1 = ITP/ITP#
For 27_SEL, 0 = Enable DOT96 & SRC1,
1= Enable SRC0 & 27MHz
For PCI2_TME, 0 = Overclocking of CPU and SRC Allowed
1 = Overclocking of CPU and SRC NOT allowed

+3VS — @ R1245 10K_0402_5% — ITP_EN — R1247 10K_0402_5%
+3VS — R1690 10K_0402_5% — 27_SEL — @ R1691 10K_0402_5%
+3VS — R1108 10K_0402_5% — PCI2_TME — R1246 10K_0402_5% @

CLK_XTAL_OUT — CLK_XTAL_IN — 14.31818MHZ_16P — Y6
C509 18P_0402_50V8J — C505 18P_0402_50V8J

Routing the trace at least 10mil

Security Classification	Compal Secret Data		
Issued Date	2006/09/25	Deciphered Date	2006/09/25

Compal Electronics, Inc.

Title: **Clock generator**

Size	Document Number	Rev
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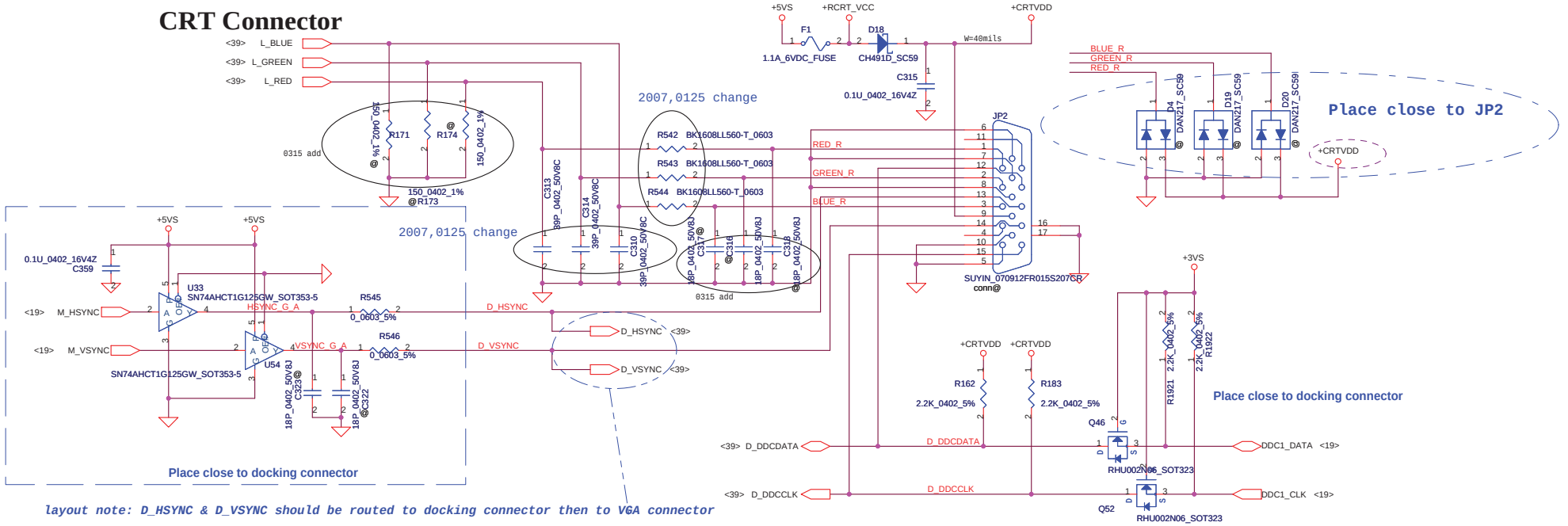
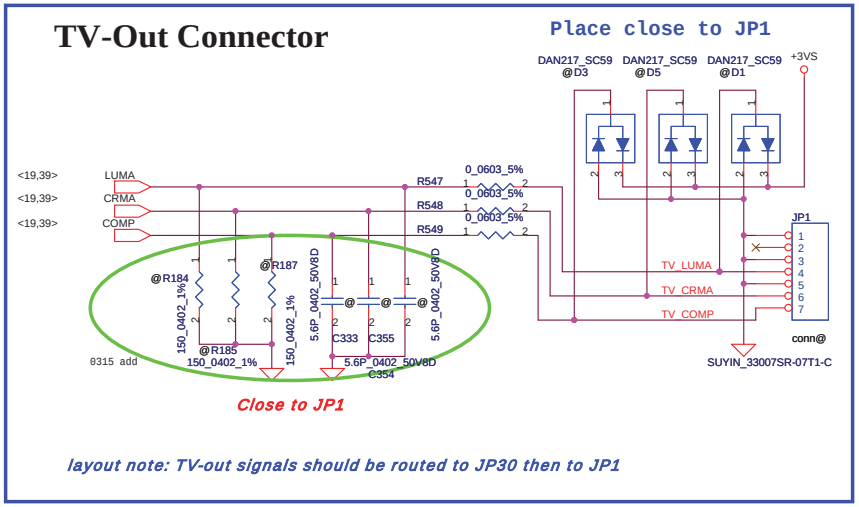
CRT Connector



layout note: D_HSYNC & D_VSYNC should be routed to docking connector then to VGA connector

TV-Out Connector



layout note: TV-out signals should be routed to JP30 then to JP1

Security Classification	Compal Secret Data		
Issued Date	2006/09/25	Deciphered Date	2006/09/25

Compal Electronics, Inc.			
Title	CRT & TVout Connector		
Size	Document Number	LA3262P_DIS__M64	Rev 1A
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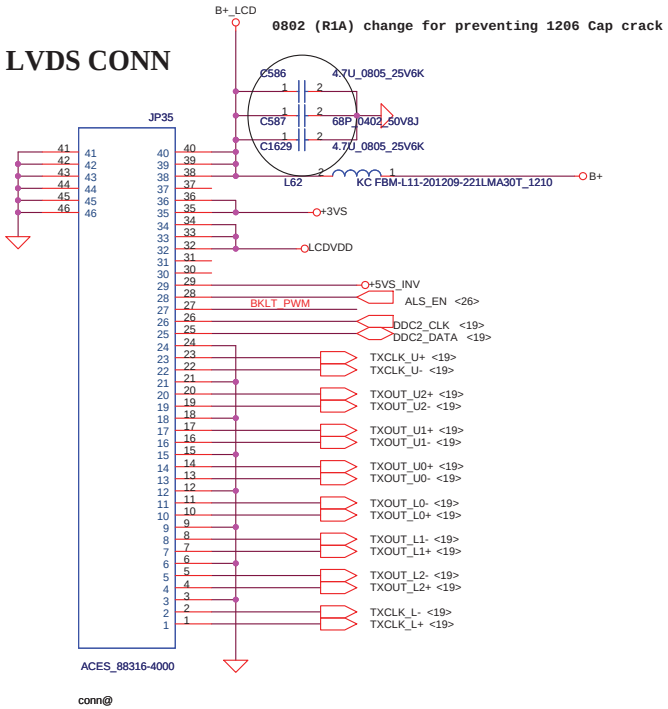
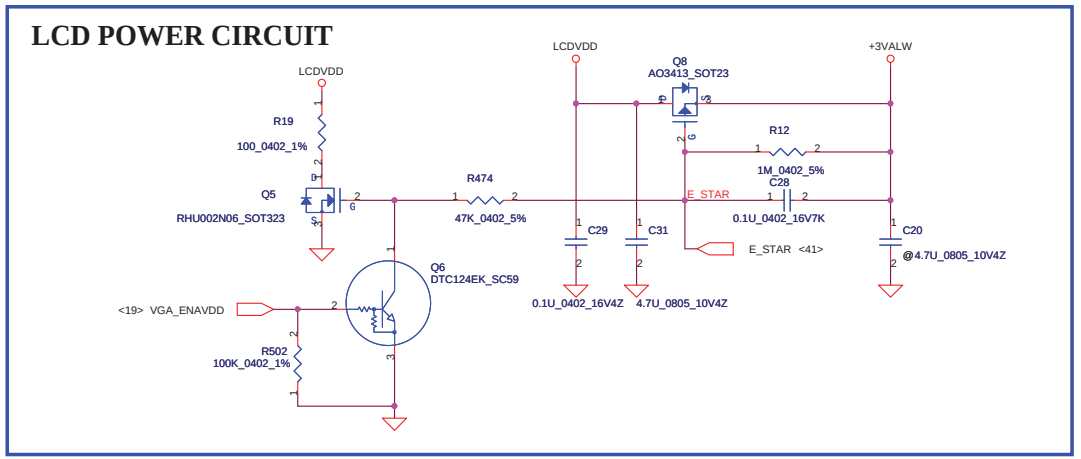
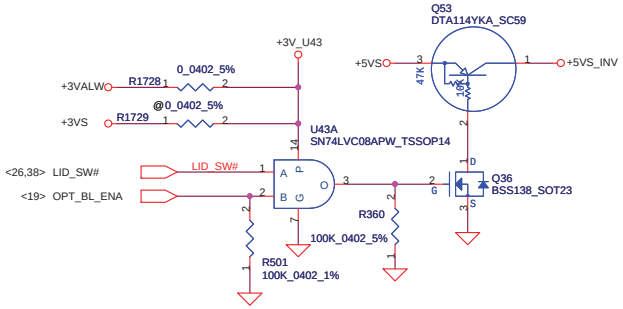
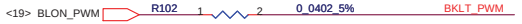
LVDS CONN



LCD POWER CIRCUIT







Support 3V inverter

Security Classification	Compal Secret Data		
Issued Date	2006/09/25	Deciphered Date	2006/09/25

Compal Electronics, Inc.	
Title	LCD CONN.
Size	Document Number: LA3262P_DIS__M64
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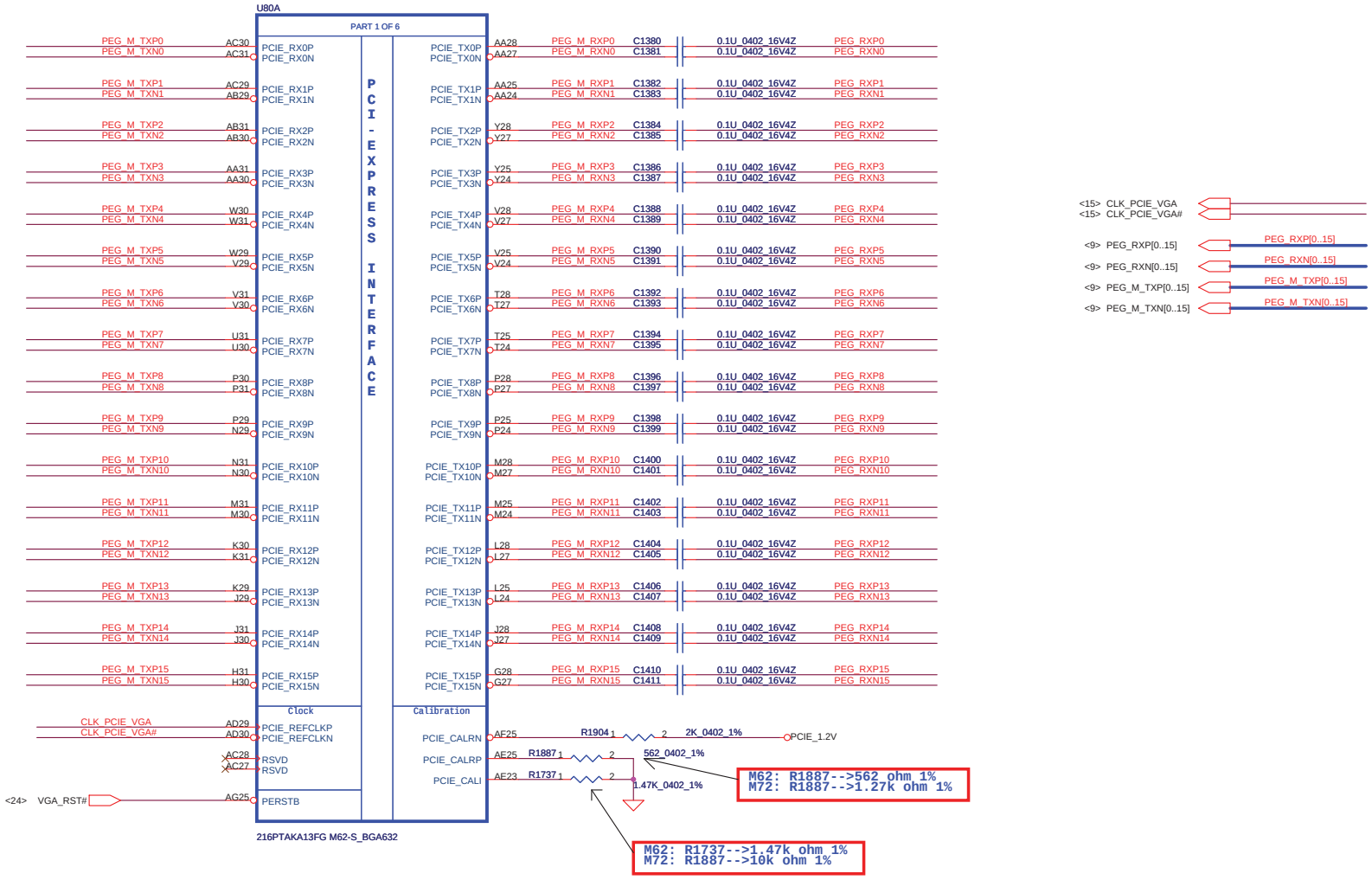

Security Classification	Compal Secret Data		
Issued Date	2006/09/25	Deciphered Date	2006/09/25

Compal Electronics, Inc.	
Title	M62-S PCIE interface
Size	Document Number: LA3262P_DIS__M64
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20070719 change for DVI high resolution issue

Close to U80

BLM18PG121SN1D_0603 L93 1U_0402_6.3V4Z MPVDD VGA_VCORE C1437 C1450 C10 10U_0603_4V6M 0.1U_0402_16V4Z

Close to U80

BLM18PG121SN1D_0603 L87 +2.5VS 170MA, 20mils 0.1U_0402_16V4Z +DPLL_PVDD C1584 C1585 C1427 1U_0402_6.3V4Z 10U_0603_6.3V6M

BLM18PG121SN1D_0603 10U_0603_6.3V6M PCIE_1.2V R1797 PCIE_PVDD C1428 1U_0402_6.3V4Z C6 C9 0.1U_0402_16V4Z

BLM18PG121SN1D_0603 R1891 PCIE_1.2V DPLL_VDDC C1435 C1436 1U_0402_6.3V4Z 1U_0402_6.3V4Z

U80B

PART 2 OF 6

VID_0 VID_1 VID_2 VID_3 VID_4 VID_5 VID_6 VID_7 VHAD_0 VHAD_1 VPHCTL VPCLK0 VIPCLK PSYNC DVALID SDA SCL DVPCNTL_MVP_0 DVPCNTL_MVP_1 DVPCNTL_0 DVPCNTL_1 DVPCNTL_2 DVPCLK DVPDATA_0 DVPDATA_1 DVPDATA_2 DVPDATA_3 DVPDATA_4 DVPDATA_5 DVPDATA_6 DVPDATA_7 DVPDATA_8 DVPDATA_9 DVPDATA_10 DVPDATA_11 DVPDATA_12 DVPDATA_13 DVPDATA_14 DVPDATA_15 DVPDATA_16 DVPDATA_17 DVPDATA_18 DVPDATA_19 DVPDATA_20 DVPDATA_21 DVPDATA_22 DVPDATA_23

VIP / I2C

VIP Host/External TMDS

GPIO_0 GPIO_1 GPIO_2 GPIO_3 GPIO_4 GPIO_5 GPIO_6 GPIO_7_BLON GPIO_8_ROMSO GPIO_9_ROMSI GPIO_10_ROMSCK GPIO_11 GPIO_12 GPIO_13 GPIO_14_HPD2 GPIO_15_PWRCNTL_0 GPIO_16_SSIN GPIO_17_THERMAL_INT GPIO_18_HPD3 GPIO_19_CTF GPIO_20_PWRCNTL_1 GPIO_21_BB_EN GPIO_22_ROMCSB GPIO_23_CLKREQB GPIO_24_TRST GPIO_25_TDI GPIO_26_TCK GPIO_27_TMS GPIO_28_TDO GENERICA GENERICB GENERICC VREFG

General Purpose I/O

DPLL_PVDD DPLL_PVSS PCIE_PVDD PCIE_PVSS MPVDD MPVSS XTALIN XTALOUT DPLL_VDDC NC_10

PLL & XTAL

VIDEO & MULTIMEDIA

Integrated TMDS: TXCM TXCP TX0M TX0P TX1M TX1P TX2M TX2P TPVDD TPVSS TXVDDR_1 TXVDDR_2 TXVDDR_3 TXVDDR_4 TXVSSR_1 TXVSSR_2 TXVSSR_3 TXVSSR_4 TXVSSR_5 TXVSSR_6 NC_5 NC_6 NC_7 NC_8 NC_9

DAC / CRT: R RB G GB B BB HSYNC VSYNC RSET AVDD AVSSQ VDD1DI VSS1DI

DAC2 (TV/CRT2): R2 R2B G2 G2B B2 B2B C C2B Y COMP V2SYNC H2SYNC A2VDD A2VDDQ A2VSSQ VDD2DI VSS2DI R2SET

Monitor Interface: HPD1 DDC1DATA DDC1CLK DDC2DATA DDC2CLK DDC3DATA DDC3CLK

Thermal: TS_FDO DPLUS DMINUS

Test: TESTEN PLLTEST

216PTAKA13FG M62-S_BGA632

<17> DDC2_DATA <17> DDC2_CLK R1752 2.2K_0402_5% +3VS R1755 2.2K_0402_5%

T88 PAD T89 PAD T90 PAD T91 PAD T92 PAD <23> VRAM_ID0 <23> VRAM_ID1 <23> VRAM_ID2 <23> VRAM_ID3

<23> GPIO0 <23> GPIO1 GPIO4 <23> GPIO5 <23> GPIO6

<17> OPT_BL_ENA

T113PAD T115PAD <23> GPIO11 T114PAD <23> GPIO13

<51> POW_SW <15> 27M_SSC

+3VS R1760 499_0402_1% VGA_VREF R1769 499_0402_1% C2 0.1U_0402_16V4Z

M62S: R1769-->499 ohm 1% M72S: R1769-->249 ohm 1%

Place those components as close as U80 within 500 mils.

@R1787 10K_0402_5% +3VS <15,31> CLKREQ#_E PAD T97 R1791 1K_0402_5% T98 PAD T99 PAD T100PAD T101PAD T102PAD T103PAD VGA_VREF

+DPLL_PVDD PCIE_PVDD MPVDD

<15> 27M_CLK 110_0402_1% R1449 R1449 Close to C1565 R1450 82_0402_5%

XIN XOUT 18P_0402_50V8J C1565 @ 18P_0402_50V8J C1566 @

Close to U80 AJ31 and AJ30 pins

M62S: R1450-->330 ohm 1% > ~ 1.1V

100_0402_1% R1740 DVI_CLK- <39> DVI_CLK+ <39>
100_0402_1% R1742 DVI_TX0- <39> DVI_TX0+ <39>
100_0402_1% R1745 DVI_TX1- <39> DVI_TX1+ <39>
100_0402_1% R1746 DVI_TX2- <39> DVI_TX2+ <39>

+TPVDD 1U_0402_6.3V4Z C1415 Closed to U80

+TXVDDR C1414 0.1U_0402_16V4Z C1552 1U_0402_6.3V4Z

VGA_RED R1775 470_0402_1% M_HSYNC <16> M_VSYNC <16> +AVDD C1418 1U_0402_6.3V4Z

VGA_GRN VGA_BLU C1421 1U_0402_6.3V4Z

VDDDI_25 C1422 1U_0402_6.3V4Z

VGA_CRMA VGA_LUMA VGA_COMP R1793 715_0402_1% C1426

+A2VDD

DVI_DETECT <39>

DDC1_DATA <16> DDC1_CLK <16> R1796 4.7K_0402_5% DVI_DAT <39> DVI_CLK <39> R1799 4.7K_0402_5% +3VS

DVI

ICH_SM_DA <4,23,26,31> ICH_SM_CLK <4,23,26,31>

thermal

VGA_THERMDA <23> VGA_THERMDC <23> R1800 1K_0402_5%

U80F

PART 6 OF 6

+LVDDR C1412 1U_0402_6.3V4Z AE20 AG20 AJ18 AH20 AF23 AF21 AL18 AJ22 AJ25 AK18 AK23 AK25 AJ21 AL23 AL25 AG18 AH18

LVDDR_1 LVDDR_2 LVDDC_1 LVDDC_2 LVSSR_1 LVSSR_2 LVSSR_3 LVSSR_4 LVSSR_5 LVSSR_6 LVSSR_7 LVSSR_8 LVSSR_9 LVSSR_10 LVSSR_11 LPVDD LPVSS

+LPVDD C1416 1U_0402_6.3V4Z C1417 100N_0402_50V7M

Control VARY_BL DIGON

LVDS channel

TXCLK_UP TXCLK_UN TXOUT_U0P TXOUT_U0N TXOUT_U1P TXOUT_U1N TXOUT_U2P TXOUT_U2N TXOUT_U3P TXOUT_U3N TXCLK_LP TXCLK_LN TXOUT_L0P TXOUT_L0N TXOUT_L1P TXOUT_L1N TXOUT_L2P TXOUT_L2N TXOUT_L3P TXOUT_L3N

10K_0402_5% R1905 BLON_PWM <17> VGA_ENAVDD <17>

TXCLK_U+ <17> TXCLK_U- <17> TXOUT_U0+ <17> TXOUT_U0- <17> TXOUT_U1+ <17> TXOUT_U1- <17> TXOUT_U2+ <17> TXOUT_U2- <17>

TXCLK_L+ <17> TXCLK_L- <17> TXOUT_L0+ <17> TXOUT_L0- <17> TXOUT_L1+ <17> TXOUT_L1- <17> TXOUT_L2+ <17> TXOUT_L2- <17>

0906 change

216PTAKA13FG M62-S_BGA632

Note: CRT / TV-out should route to JP30 first then to the JP1 & JP2 on system side.

CRT Termination/EMI Filter

Place Closed to U80

VGA_RED L28 HLC0603CSCC39NJT_0603 C_RED_L L31 HLC0603CSCCR11JT_0603 RED <39>

VGA_GRN L35 HLC0603CSCC39NJT_0603 C_GRN_L L34 HLC0603CSCCR11JT_0603 GREEN <39>

VGA_BLU L27 HLC0603CSCC39NJT_0603 C_BLU_L L26 HLC0603CSCCR11JT_0603 BLUE <39>

R1763 75_0402_1% R1764 75_0402_1% R1765 75_0402_1%

C193 22P_0402_50V8J C237 22P_0402_50V8J C232 22P_0402_50V8J @C195 10P_0402_50V8J @C245 10P_0402_50V8J @C244 10P_0402_50V8J

Note: TV-out should route to JP30 first then to the JP1 & JP2 on system side.

TV-Out Termination/EMI Filter

Place close to U80

VGA_COMP L38 CHB1608U301_0603 COMP <16,39>

VGA_LUMA L37 CHB1608U301_0603 LUMA <16,39>

VGA_CRMA L17 CHB1608U301_0603 CRMA <16,39>

R1778 75_0402_1% R1779 75_0402_1% R1780 75_0402_1%

C7 5.6P_0402_50V8D C238 5.6P_0402_50V8D C251 5.6P_0402_50V8D C8 5.6P_0402_50V8D C243 5.6P_0402_50V8D C253 5.6P_0402_50V8D

0314 change design

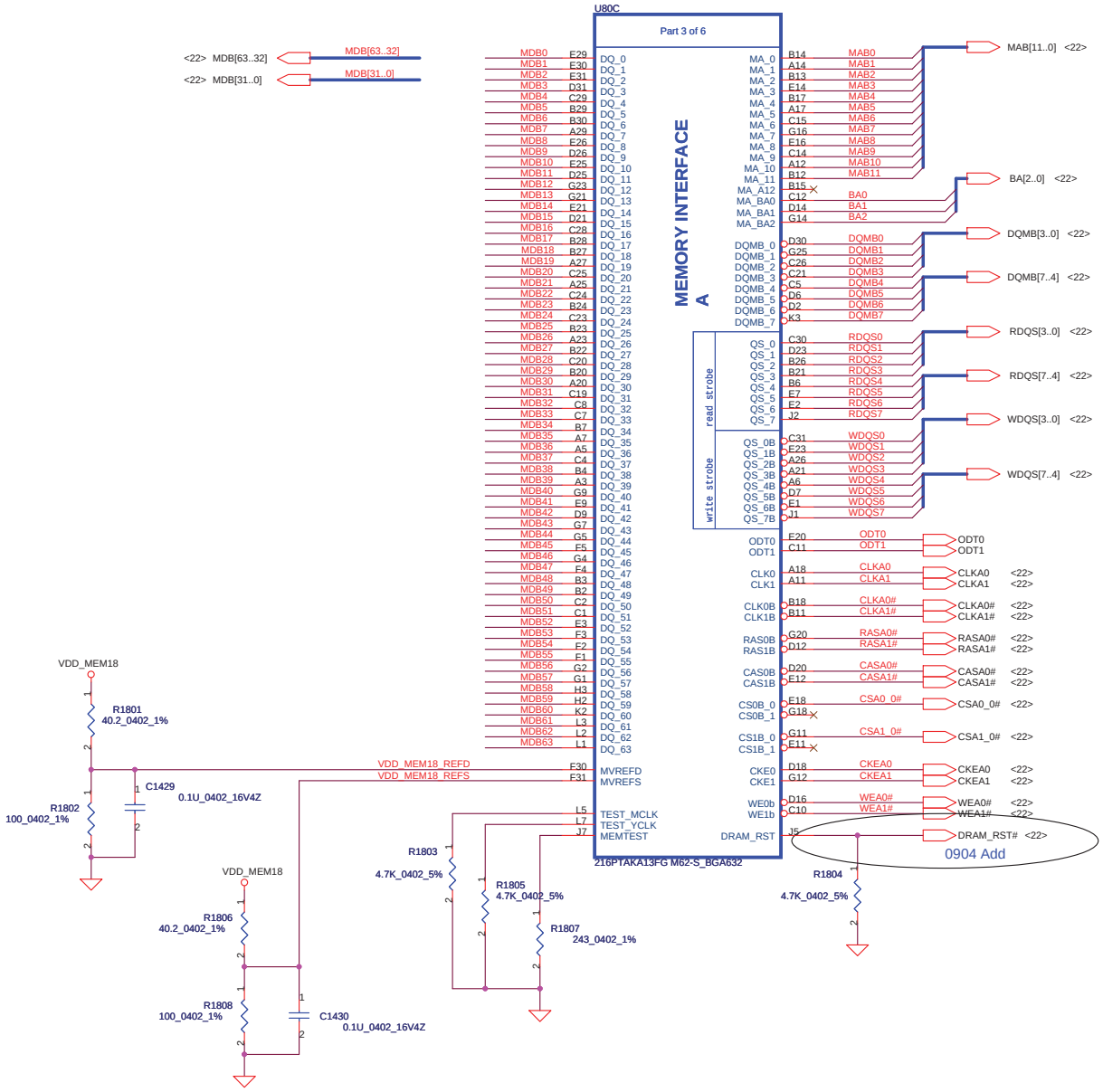
Security Classification	Compal Secret Data		
Issued Date	2006/09/25	Deciphered Date	2006/09/25

Compal Electronics, Inc.

Title: M62-S CRT/LVDS/TV-OUT

Size: Document Number: LA3262P_DIS__M64 Rev: 1A

Date: Tuesday, August 21, 2007 Sheet 19 of 57

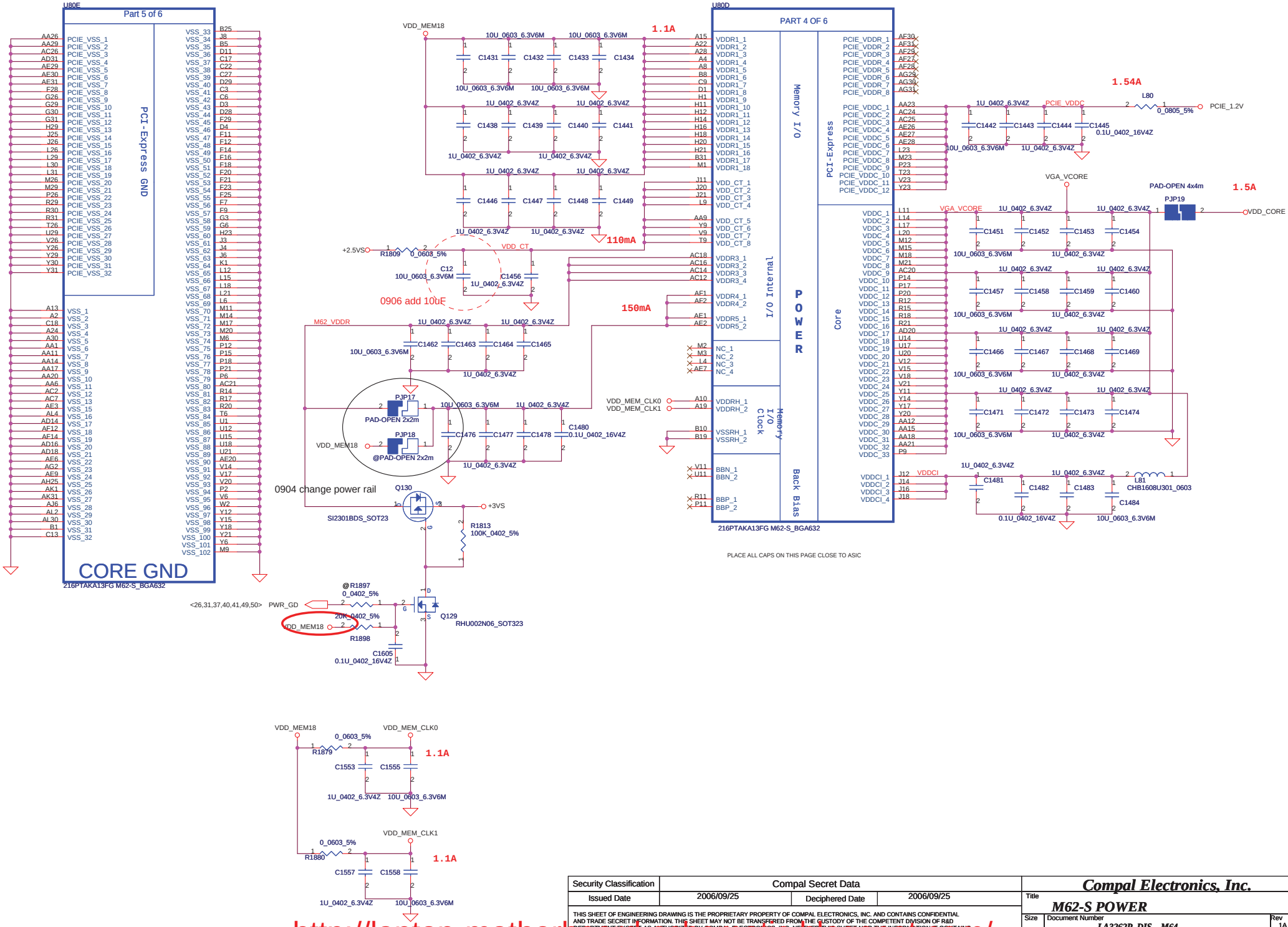


Compal Electronics, Inc.

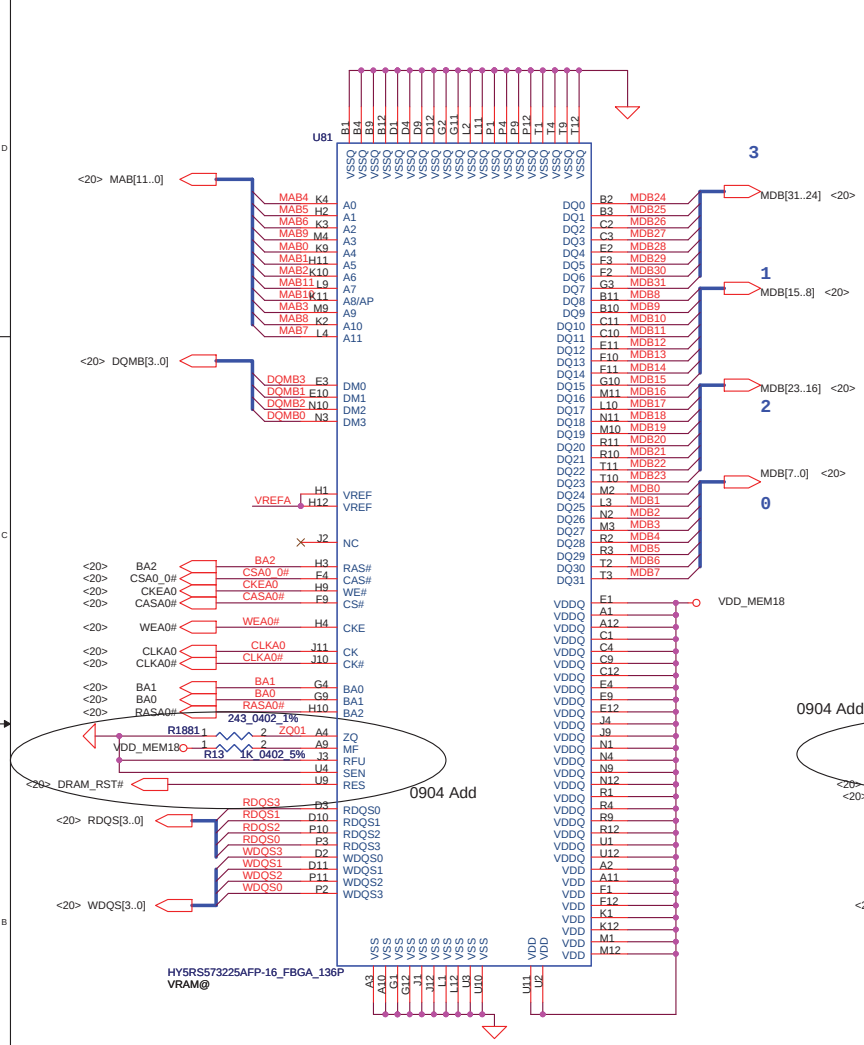
Title: **M62-S MEM**

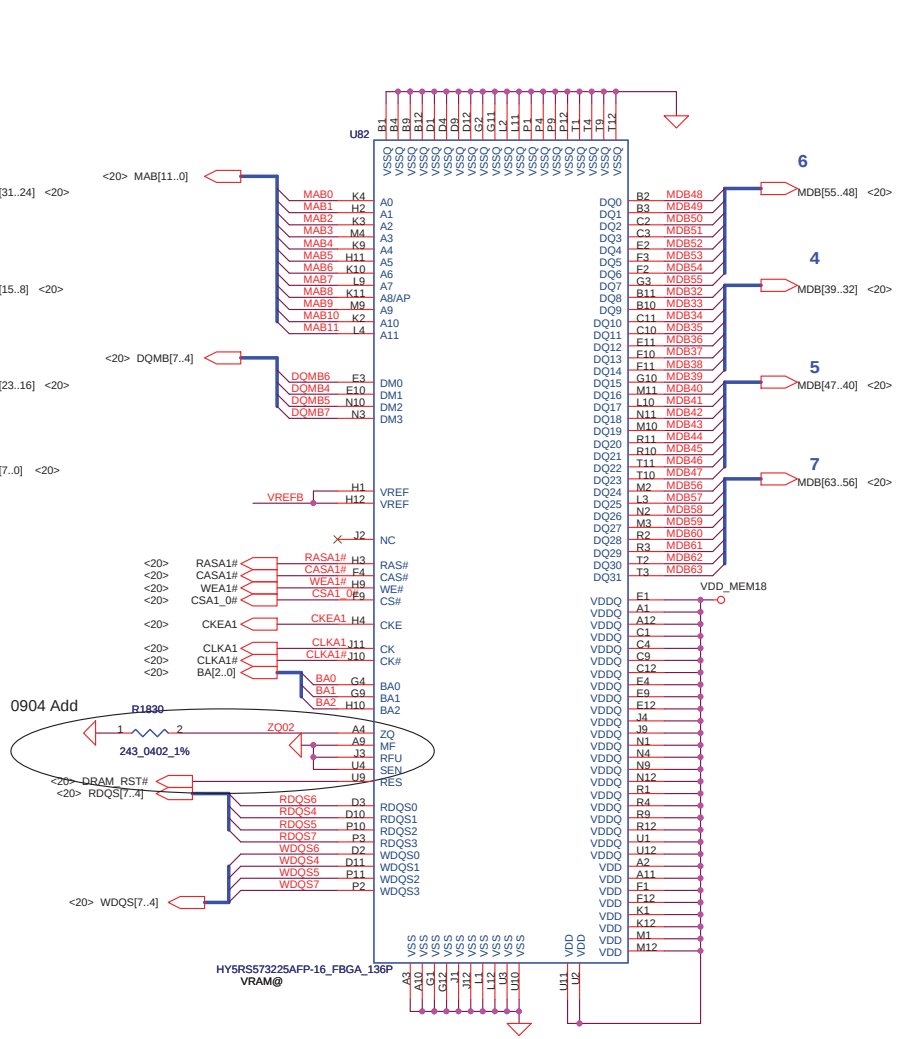
Size	Document Number	Rev
	LA3262P_DIS__M64	1A

Date: Tuesday, August 21, 2007 | Sheet 20 of 57

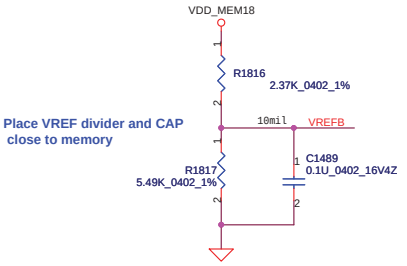


DDR3 VRAM: 8Mx32/16Mx32 FBGA_136P 2 pcs

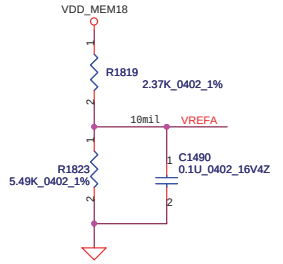


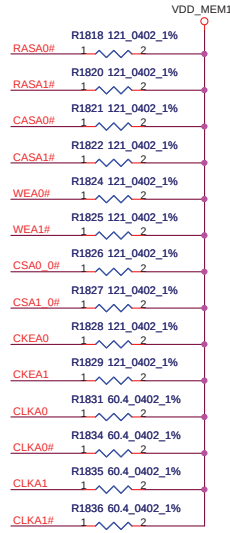


Place VREF divider and CAP close to memory

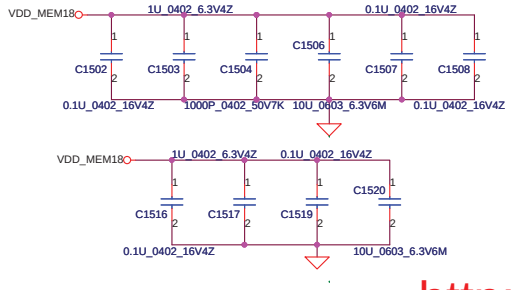


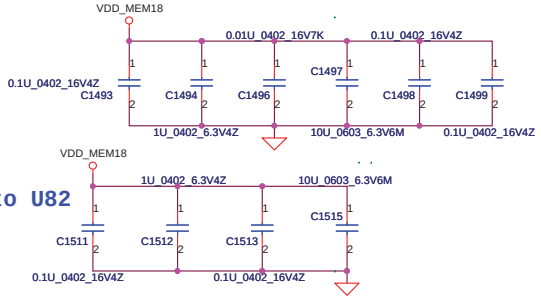
Place VREF divider and CAP close to memory





Place close to U81





Place close to U82

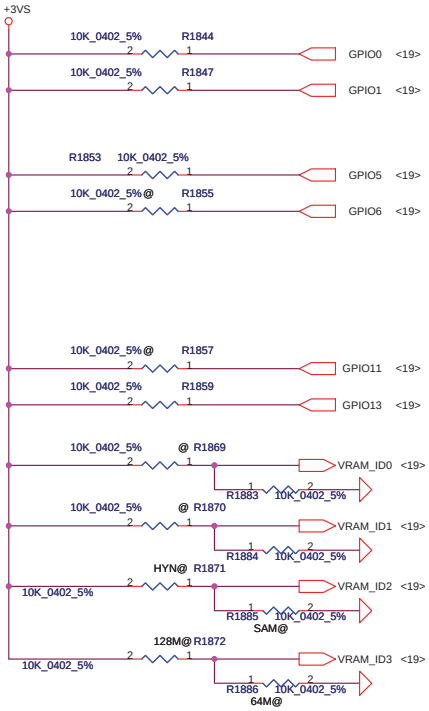
Security Classification	Compal Secret Data		
Issued Date	2006/09/25	Deciphered Date	2006/09/25

Compal Electronics, Inc.

Title: M62-S VRAM

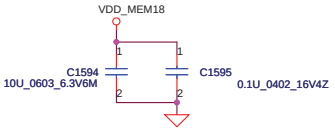
Size | Document Number: LA3262P_DIS__M64 | Rev: 1A

Date: Tuesday, August 21, 2007 | Sheet 22 of 57

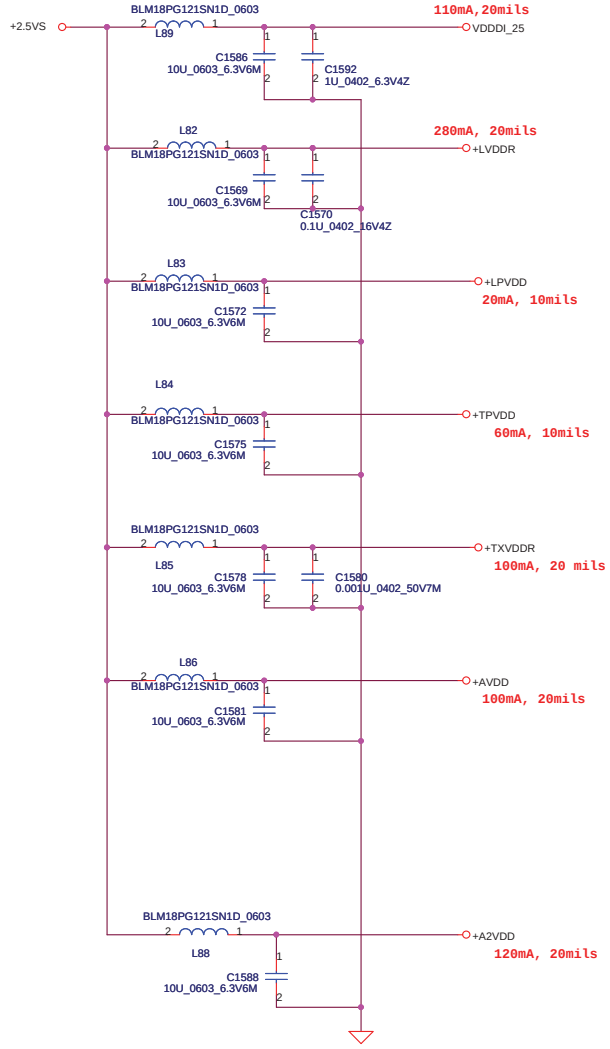


STRAPS	PIN	DESCRIPTION OF RECOMMENDED SETTING	RECOMMENDED
TX_PWRS_ENB	GPIO0	FULL SWING internal pull down	1
TX_DEEMPH_EN	GPIO1	Transmitter De-emphasis Enable internal pull down	1
DEBUG_ACCESS	GPIO4	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible internal pull down	0
PLL_IBIAS_RD	GPIO[6:5]	Bias Currentfor the PCIE PHY PLL	GPIO6-->0 GPIO5-->1
ROMIDCFG[3:0] internal pull down	GPIO [9,13,12,11]		
		No ROM , with 128M frame buffer	0 0 0 X
		No ROM , with 64M frame buffer	0 1 0 X
VRAM_ID[0:3]	DVPDATA (20,21,22,23)		VRAM_ID 0, 1, 2, 3
		Samsung 8Mx32 1.8V	0 0 0 0
		Samsung 16Mx32 1.8V	0 0 0 1
		Hynix 8Mx32 1.8V	0 0 1 0
		Hynix 16Mx32 1.8V	0 0 1 1

Closed to U80



Closed to U80

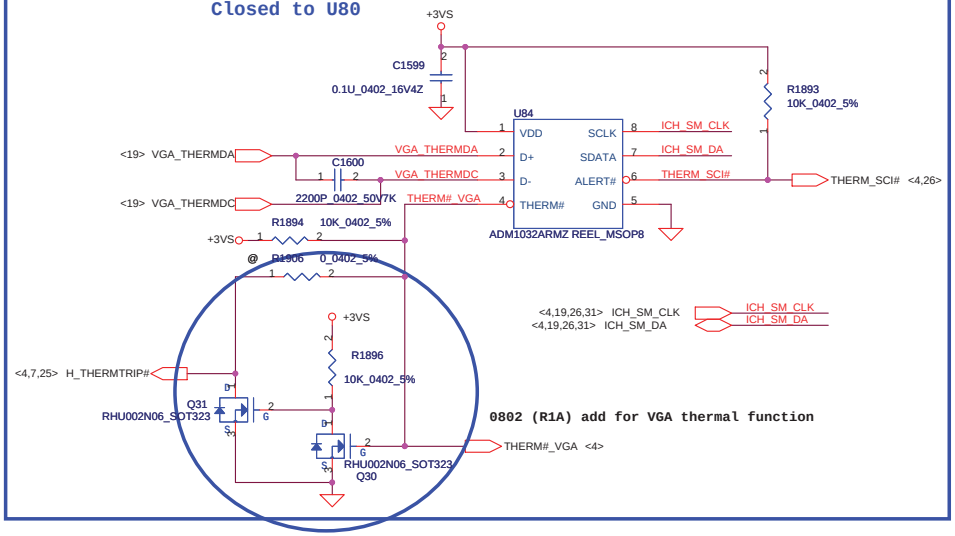


ZZZ5
Samsung VRAM group
Samsung@

ZZZ4
Hynix VRAM group
Hynix@

VGA Thermal Sensor ADM1032ARMZ

Closed to U80



Security Classification	Compal Secret Data		
Issued Date	2006/09/25	Deciphered Date	2006/09/25

Compal Electronics, Inc.

Title: **M62-S Filters / Strap**

Size	Document Number	Rev
	LA3262P_DIS__M64	1A

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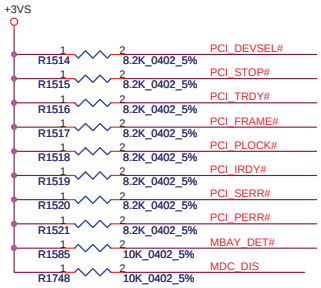
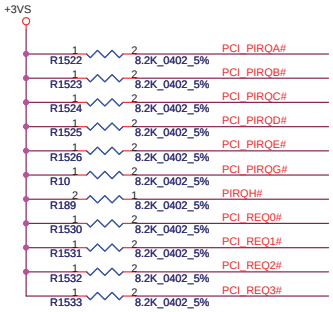
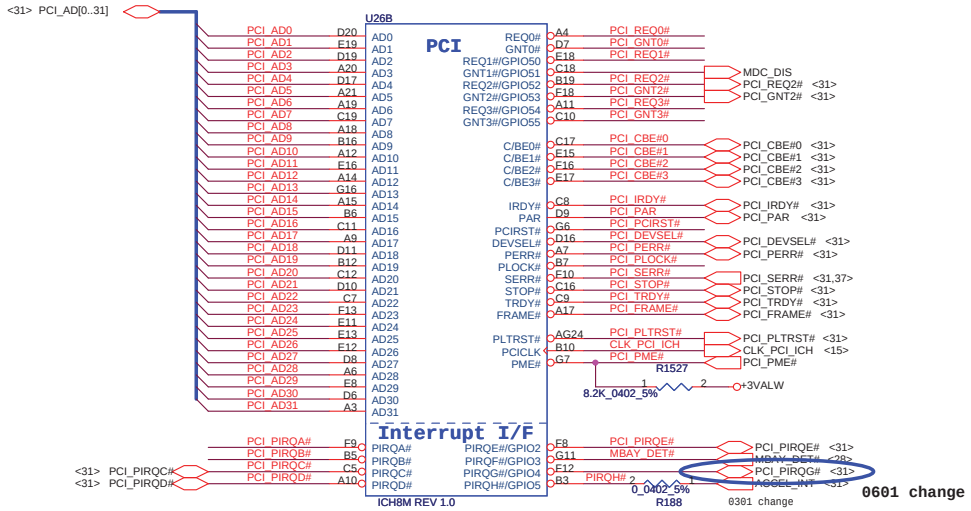
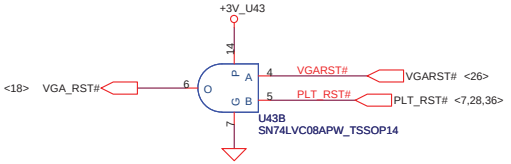
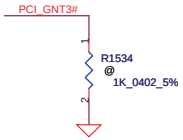




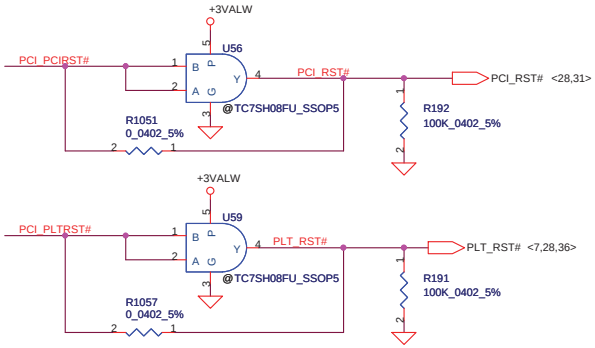


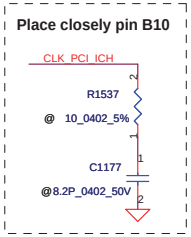




A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enble High= Default*

Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI *
1	0	PCI
1	1	LPC





Security Classification	Compal Secret Data		
Issued Date	2006/09/25	Deciphered Date	2006/09/25

Compal Electronics, Inc.			
Title	ICH8(1/4)-PCI/INT		
Size	Document Number		Rev
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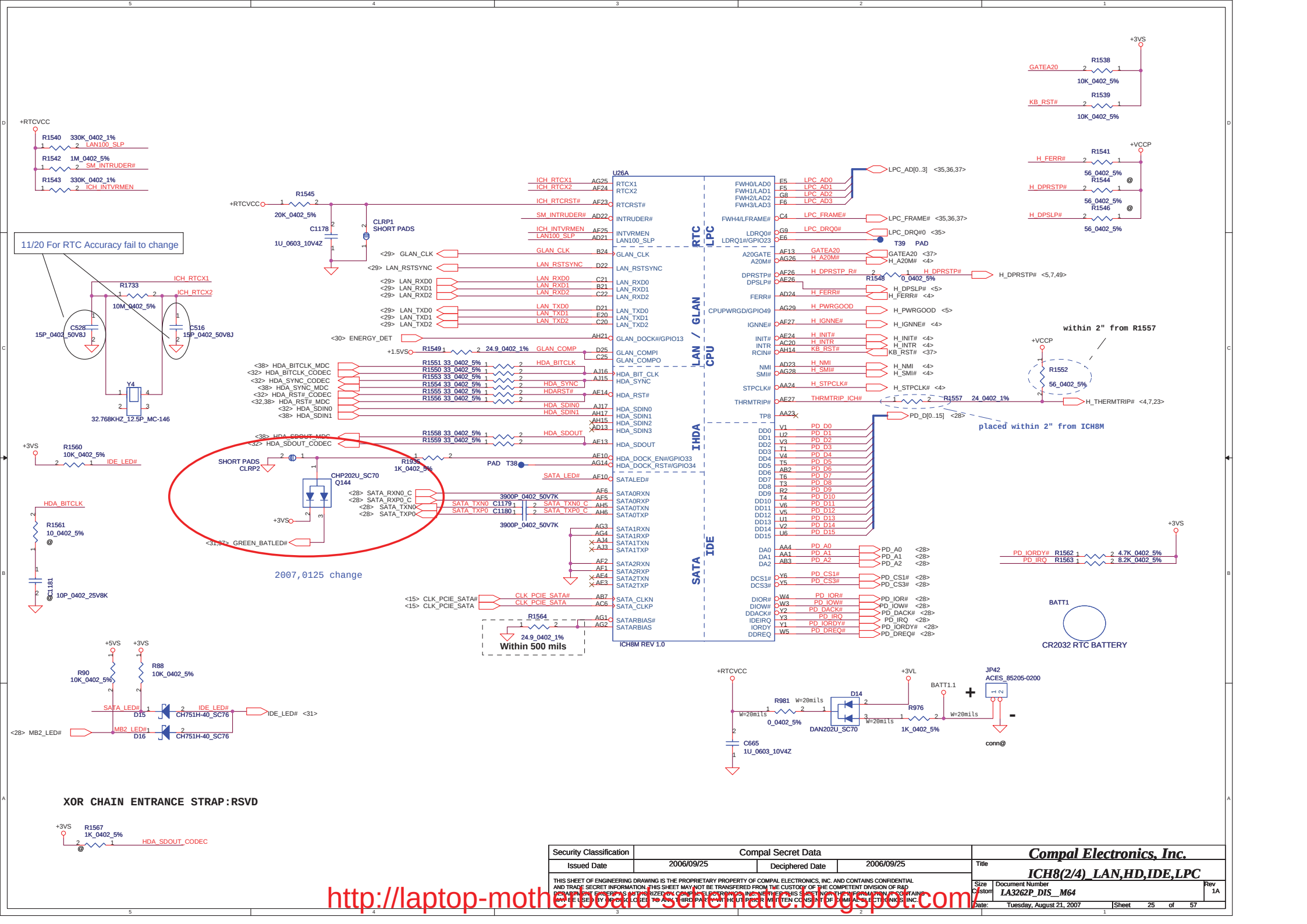

Security Classification	Compal Secret Data		
Issued Date	2006/09/25	Deciphered Date	2006/09/25

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Compal Electronics, Inc.

Title: ICH8(2/4)_LAN,HD,IDE,LPC

Size	Document Number	Rev
Custom	LA3262P_DIS_M64	1A

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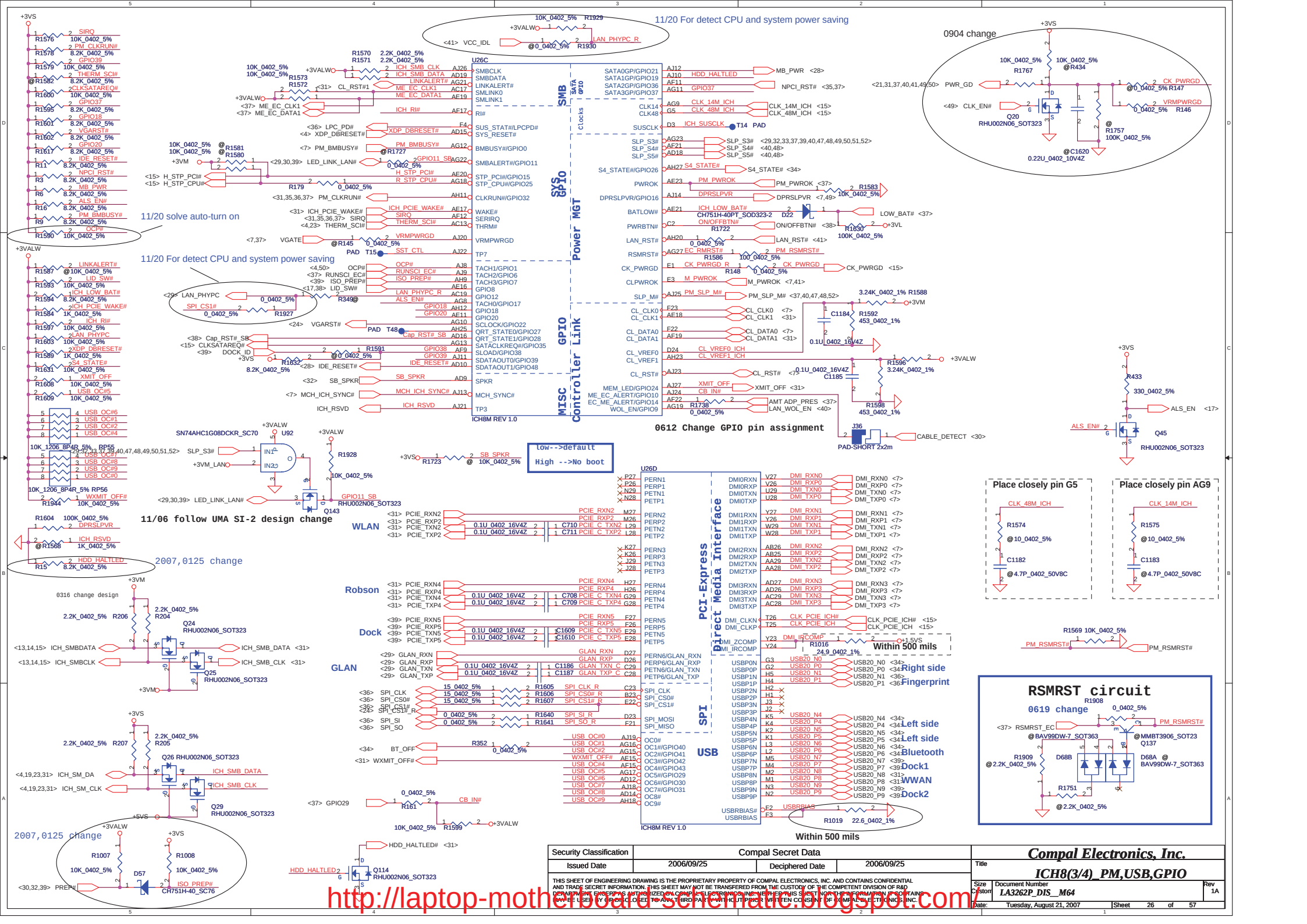

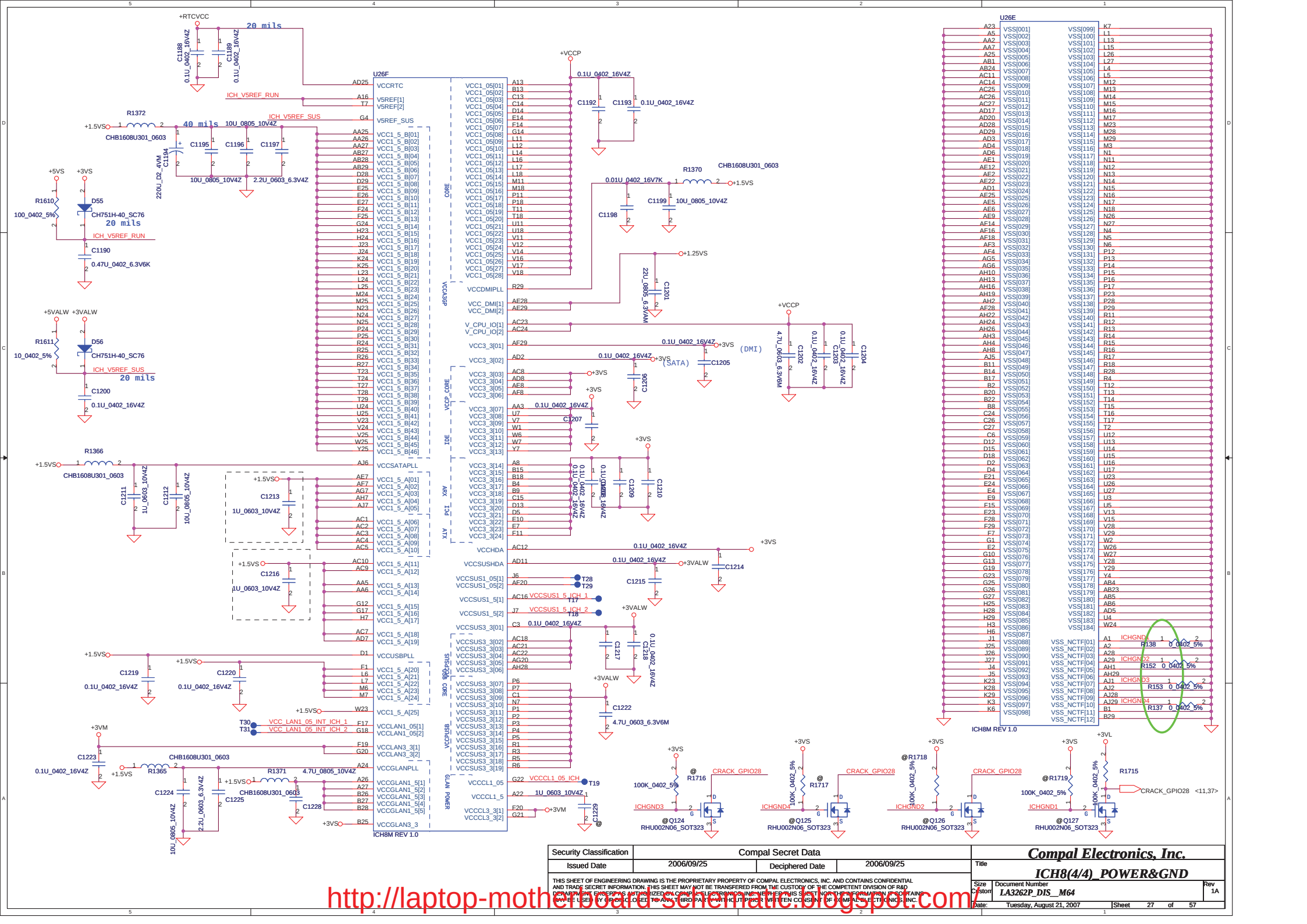
U26F
ICH8M REV 1.0
U26E
ICH8M REV 1.0
+RTCVCC
20 mils
ICH_V5REF_RUN
ICH_V5REF_SUS
40 mils
10U_0805_10V4Z
2.2U_0603_6.3V4Z
CHB1608U301_0603
CH751H-40_SC76
+5VS
+3VS
+5VALW
+3VALW
+1.5VS
+1.25VS
+VCCP
+3VM
+3VL
+3VS
(DMI)
(SATA)
VCCRTC
V5REF[1]
V5REF[2]
V5REF_SUS
VCCDMIPLL
VCC_DMI[1]
VCC_DMI[2]
V_CPU_IO[1]
V_CPU_IO[2]
VCCSATAPLL
VCCUSBPLL
VCCHDA
VCCSUSHDA
VCCLAN1_05[1]
VCCLAN1_05[2]
VCCLAN3_3[1]
VCCLAN3_3[2]
VCCGLANPLL
VCCGLAN1_5[1]
VCCGLAN1_5[2]
VCCGLAN1_5[3]
VCCGLAN1_5[4]
VCCGLAN1_5[5]
VCCGLAN3_3
VCCCL1_05
VCCCL1_5
VCCCL3_3[1]
VCCCL3_3[2]
VCCSUS1_05[1]
VCCSUS1_05[2]
VCCSUS1_5[1]
VCCSUS1_5[2]
VCCSUS3_3[01]
VCCSUS3_3[02]
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VCCSUS3_3[19]
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VCC_LAN1_05_INT_ICH_2
VCCSUS1_5_ICH_1
VCCSUS1_5_ICH_2
VCCCL1_05_ICH
1U_0_603_10V4Z
4.7U_0805_10V4Z
4.7U_0603_6.3V6M
0.1U_0402_16V4Z
0.01U_0402_16V7K
0.47U_0402_6.3V6K
10_0402_5%
100_0402_5%
100K_0402_5%
CRACK_GPIO28
RHU002N06_SOT323
ICHGND1
ICHGND2
ICHGND3
ICHGND4
VSS[001]
VSS[002]
VSS[003]
VSS[004]
VSS[005]
VSS[006]
VSS[007]
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Security Classification
Compal Secret Data
Issued Date
2006/09/25
Deciphered Date
2006/09/25
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Compal Electronics, Inc.
Title
ICH8(4/4)_POWER&GND
Size
C
Document Number
LA3262P_DIS__M64
Rev
1A
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Tuesday, August 21, 2007
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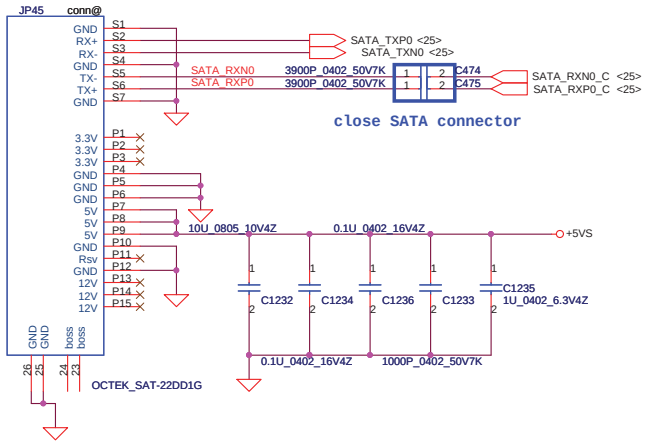
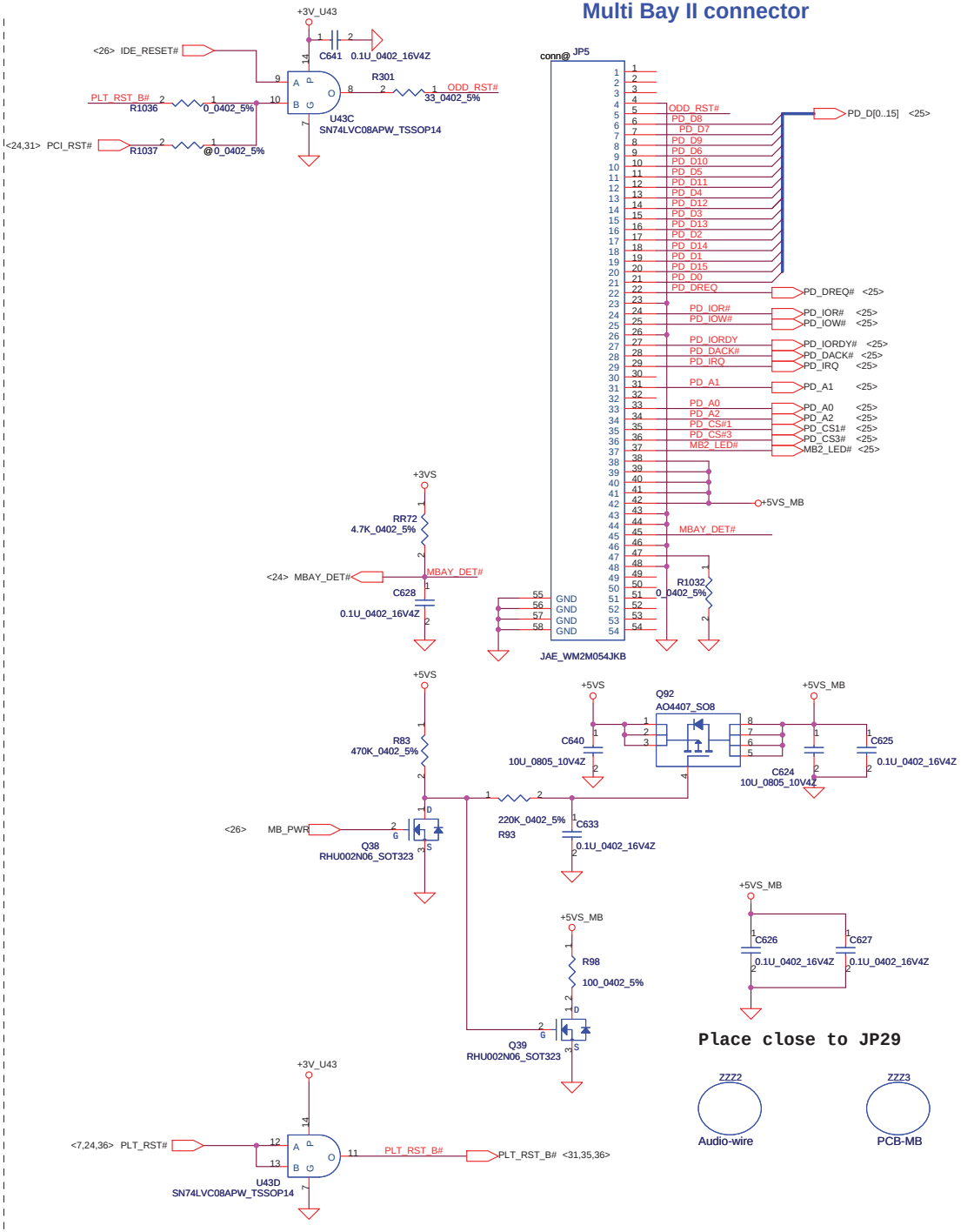
of
57
http://laptop-motherboard-schematic.blogspot.com/



Multi Bay II connector



Security Classification	Compal Secret Data		
Issued Date	2006/09/25	Deciphered Date	2006/09/25

Compal Electronics, Inc.

Title: **HDD & CDROM**

Size	Document Number	Rev
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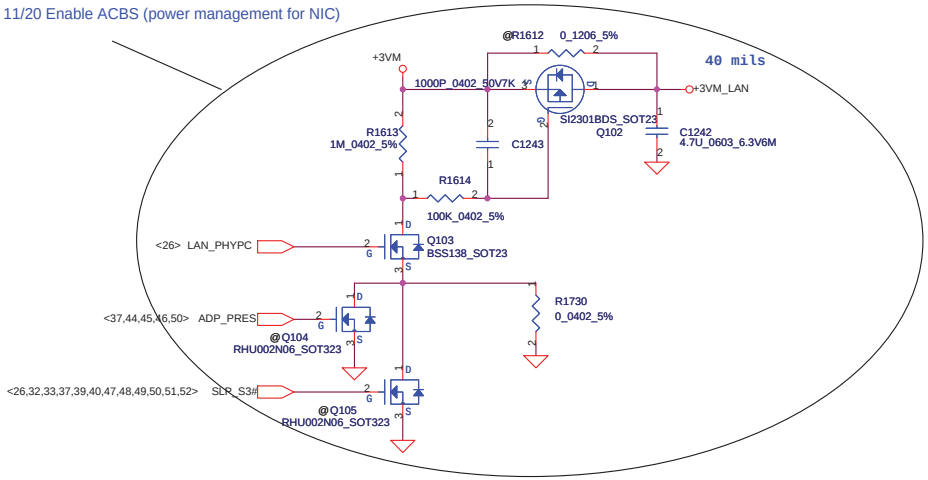
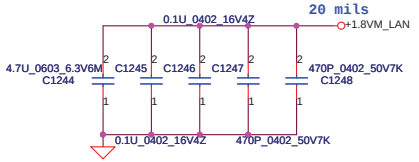
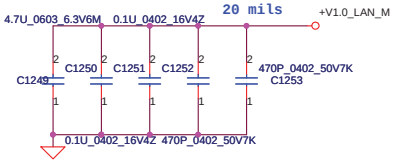
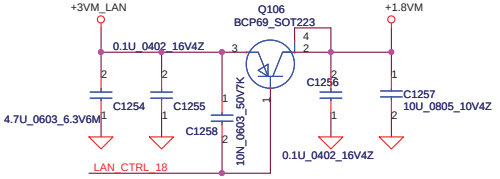
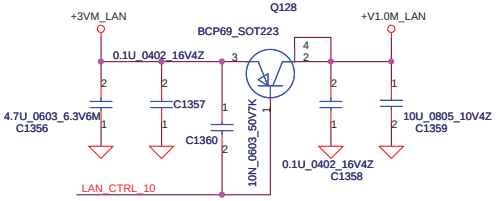
11/20 Enable ACBS (power management for NIC)

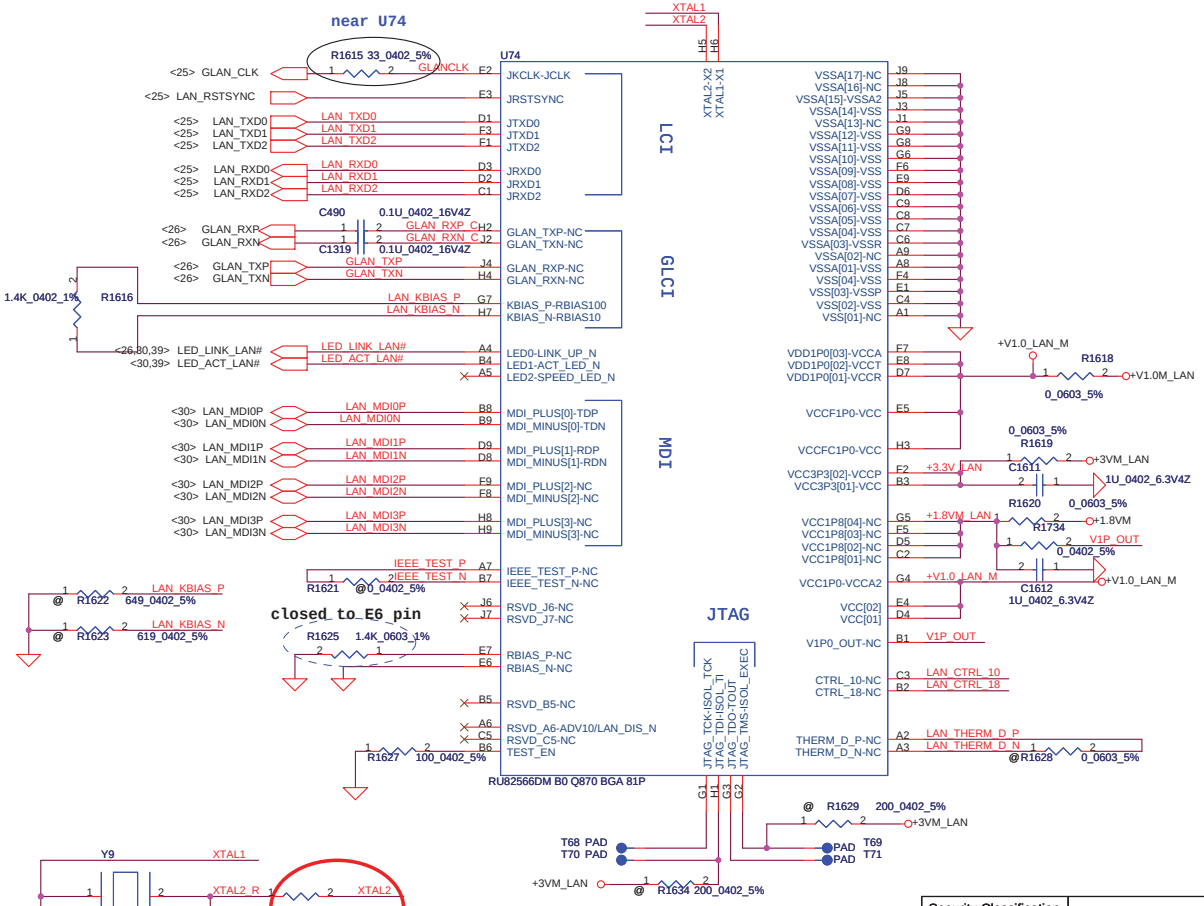












Security Classification	Compal Secret Data		
Issued Date	2006/09/25	Deciphered Date	2006/09/25

Compal Electronics, Inc.	
Title	Intel 82566 Nineveh
Size	Document Number: LA3262P_DIS__M64
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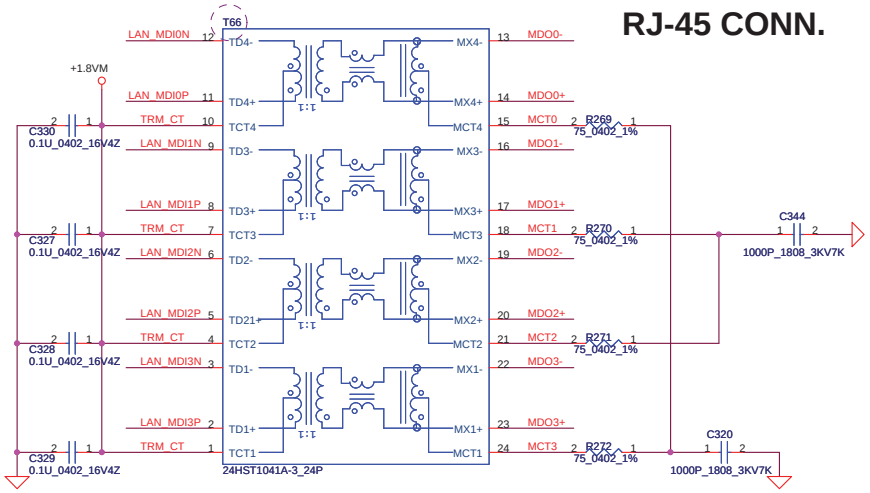
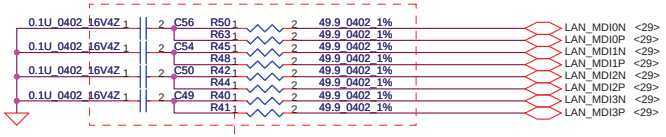
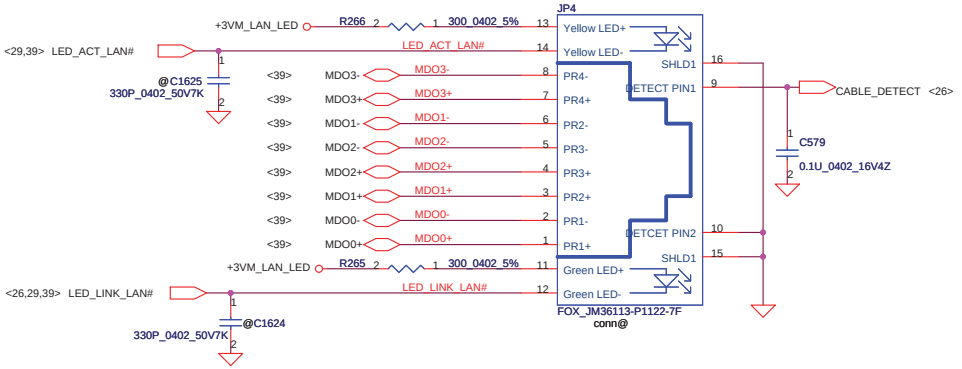
RJ-45 CONN.

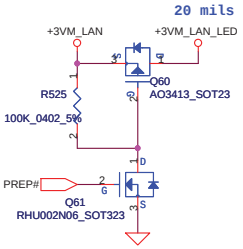




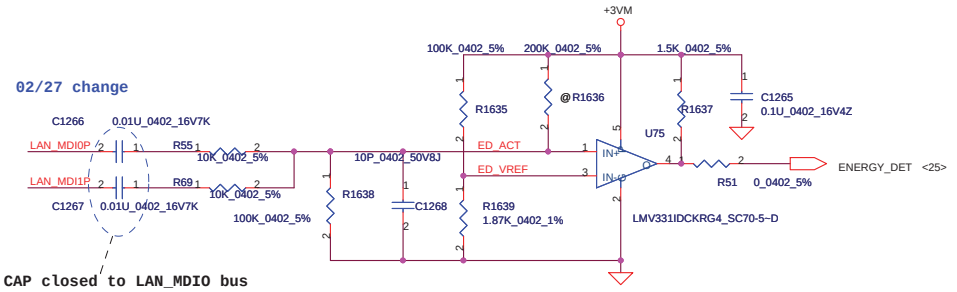
Layout Notice : Place termination as close as Intel 82566 as possible

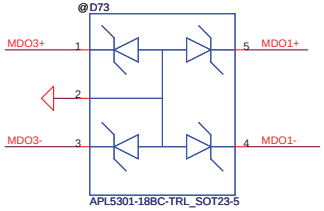
Note: MDO[3..0]+/- signals should route to JP4 first then to JP30.

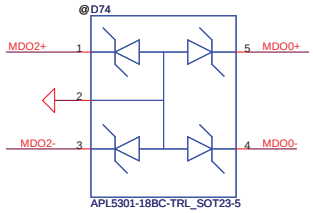




LAN ENERGY DET







Security Classification	Compal Secret Data		
Issued Date	2006/09/25	Deciphered Date	2006/09/25

Compal Electronics, Inc.			
Title: Magnetic & RJ45/RJ11			
Size	Document Number: LA3262P_DIS__M64		Rev: 1A
Date: Tuesday, August 21, 2007	Sheet 30 of 57		

B/B connector with PCI / LED / FIR / SC interface

0915 Change 1394 signals

JP13

ACES_88394-1A71

0622 change to support AMT

0731 Install R1383 and no install R1382, do not support wake on WWAN card

0811 Isolate SLOT power from SYSTEM power.

Mini-Express Card--WWAN

0821 Change +3VS to +3VS_WWAN

0811 Pins 37 and 43 connect to GND and remove +1.5VS

0821 Delete SW1,C986,R521,D65,R200

2007,0125 change

0811 Reserve for SIM card does not meet rise time and a pull-up resistor is needed.

Mini-Express Card---WLAN

0824 Add +1.5VS_WLAN

0811 Isolate SLOT power from SYSTEM power.

0821 Install R1364

0906 Remove debug resistors

0906 Remove debug resistors

0612 change power plane

0821 Change +3VS to +3VS_WLAN

0627 Add 0 ohm on PIN 42,46

0627 PIN37,43 connected to GND
PIN39,41 connected to +3VS

0811 No install R1418,R1358,R1359,R1360

0906 Remove debug resistors

JP44

MOLEX 67910-0002 52P

0811 HP request

ACCELEROMETER

0313 change design

U64

LIS3LV02DL-TR_LGA16

0619 Follow ST Demo circuit

0619 Follow ST Demo circuit

Must be placed in the center of the system.

Security Classification	Compal Secret Data		
Issued Date	2006/09/25	Deciphered Date	2006/09/25

Compal Electronics, Inc.

Title: Mini-Card/Mini-PCI/Accelerometer

Size: | Document Number: LA3262P_DIS__M64 | Rev: 1A

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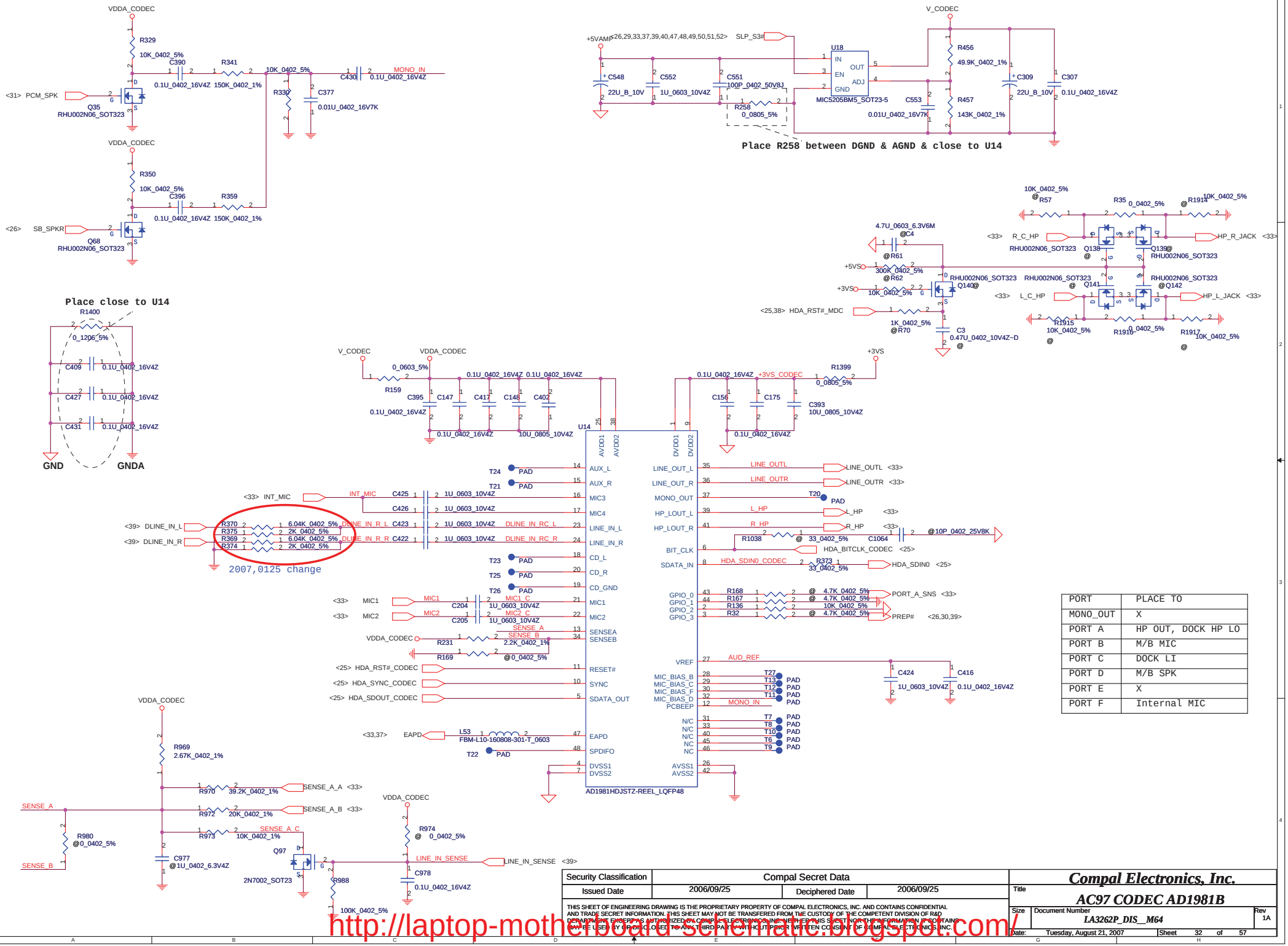

PORT	PLACE TO
MONO_OUT	X
PORT A	HP OUT, DOCK HP LO
PORT B	M/B MIC
PORT C	DOCK LI
PORT D	M/B SPK
PORT E	X
PORT F	Internal MIC

Security Classification	Compal Secret Data		
Issued Date	2006/09/25	Deciphered Date	2006/09/25

Compal Electronics, Inc.	
Title	AC97 CODEC AD1981B
Size	Document Number: LA3262P_DIS__M64
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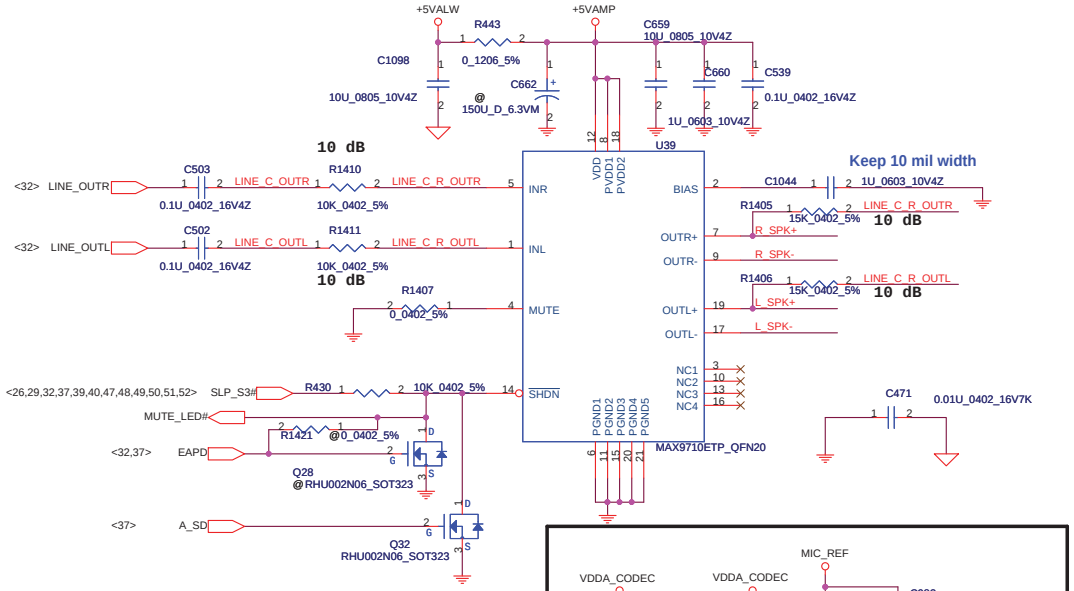
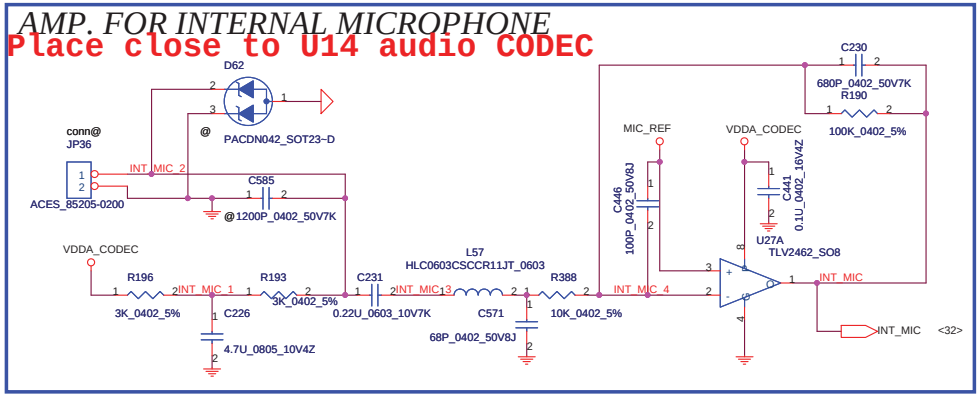
AMP. FOR INTERNAL SPEAKER



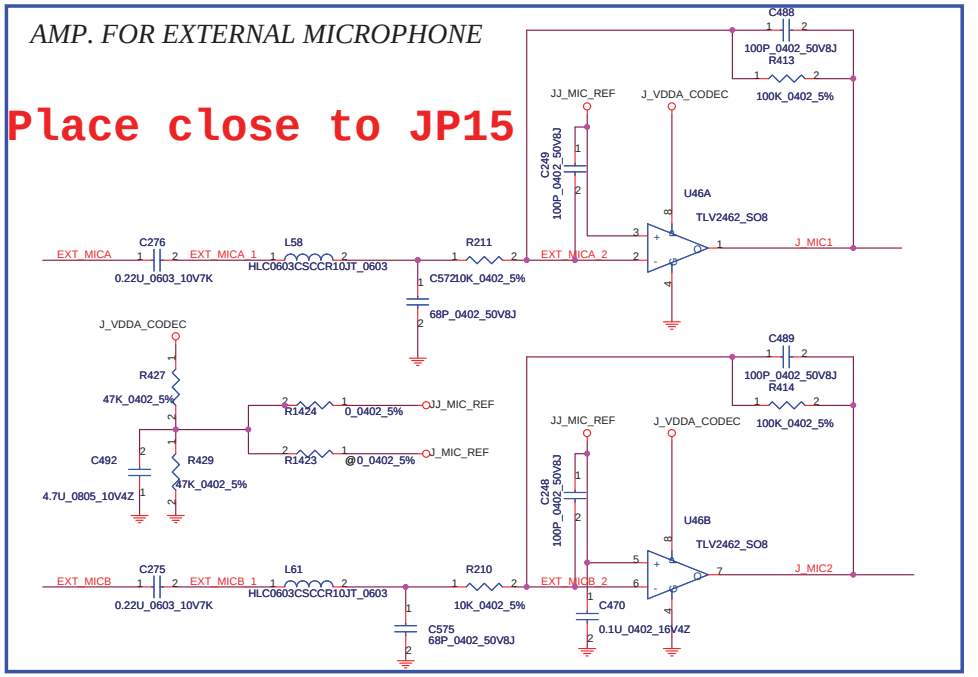
AMP. FOR INTERNAL MICROPHONE

Place close to U14 audio CODEC

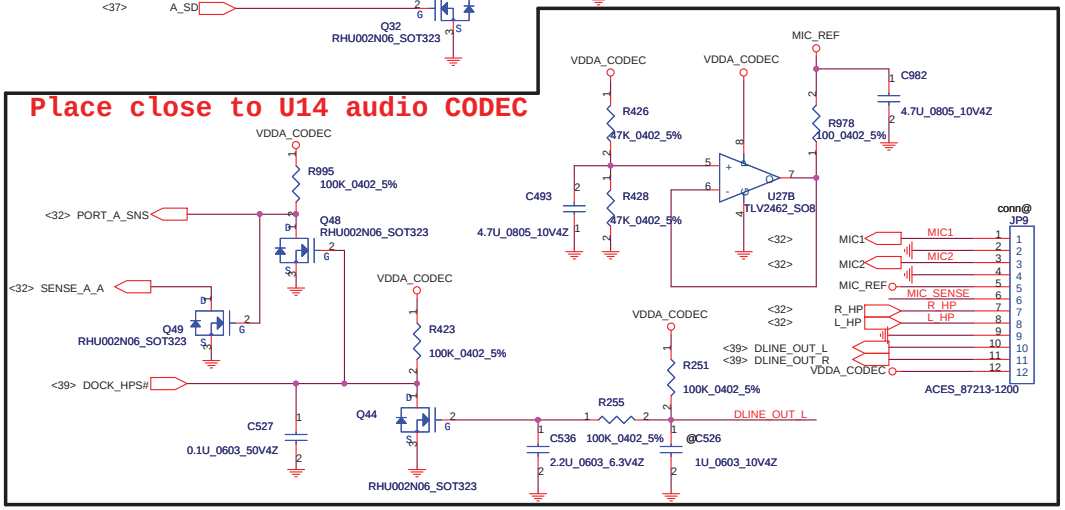


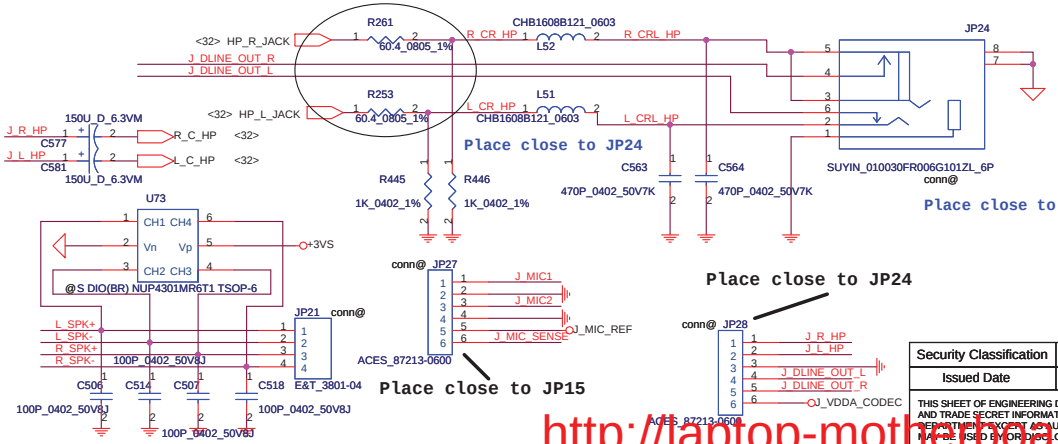
AMP. FOR EXTERNAL MICROPHONE

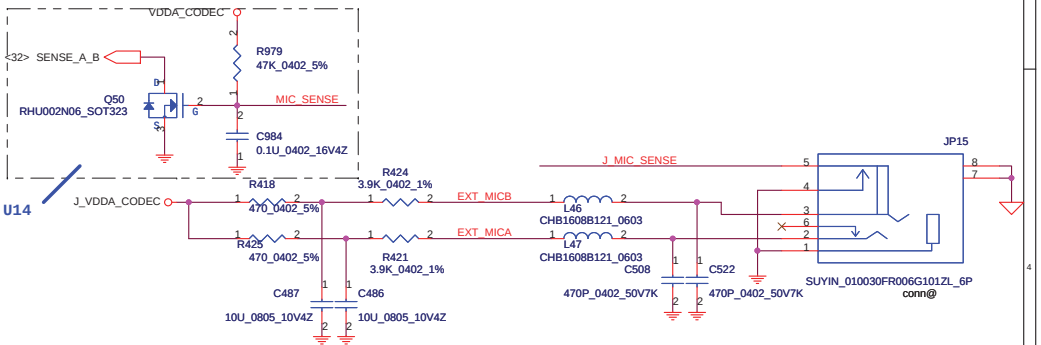
Place close to JP15



Place close to U14 audio CODEC







Security Classification	Compal Secret Data		
Issued Date	2006/09/25	Deciphered Date	2006/09/25

Compal Electronics, Inc.			
Title: AMP & Audio Jack			
Size	Document Number: LA3262P_DIS__M64		Rev: 1A
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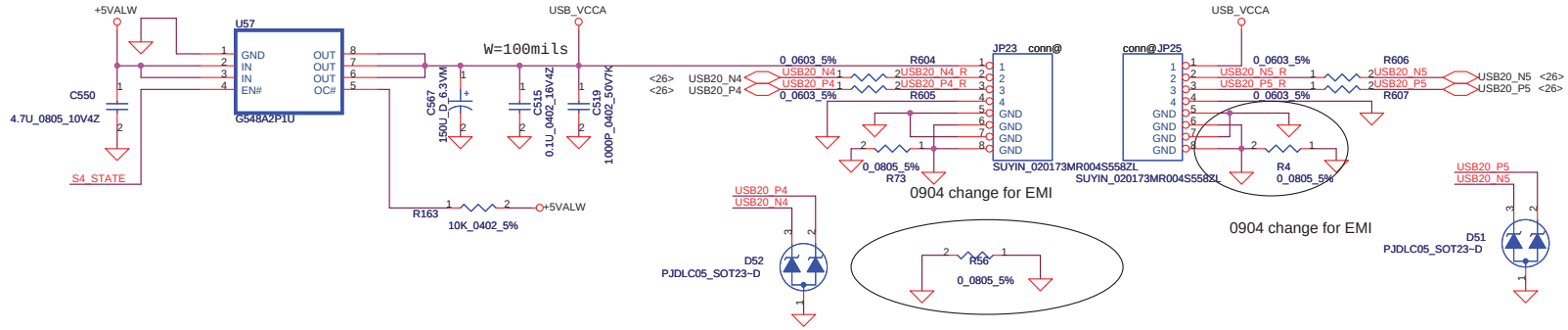
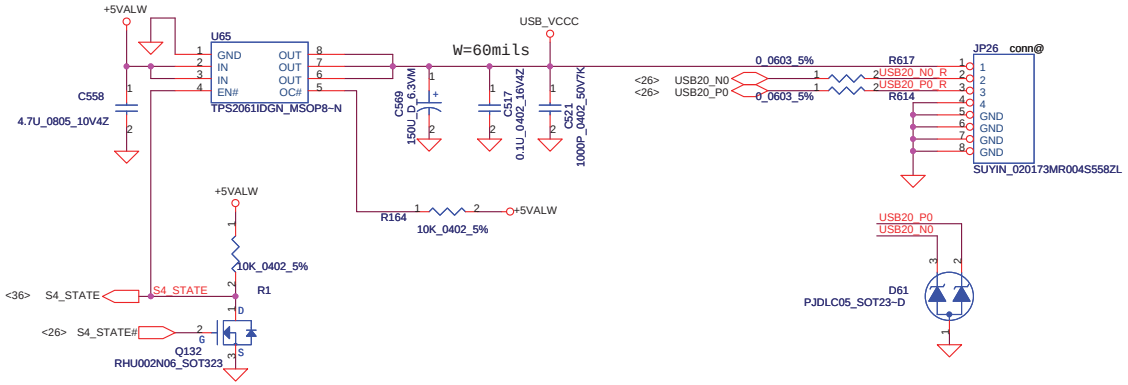
Left side USB CONNECTOR 0



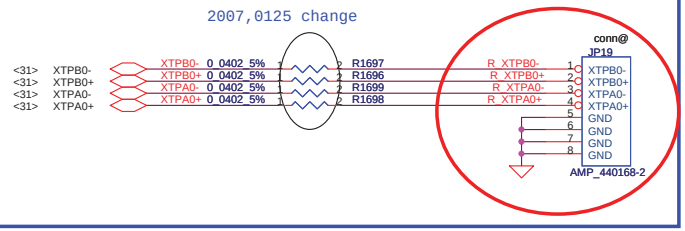
Left side USB CONNECTOR 1

Right side USB CONNECTOR 0

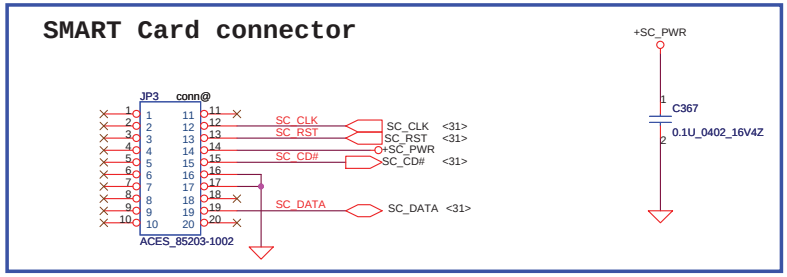


1394 connector

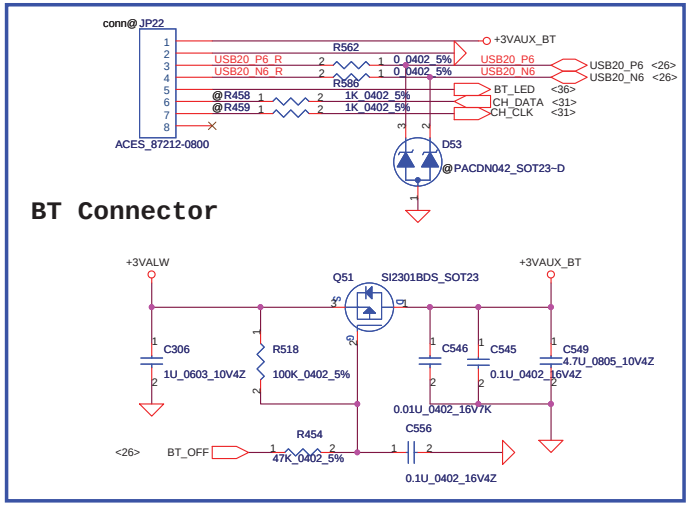
11/06 fix DB2 1394 can not detect issue



SMART Card connector

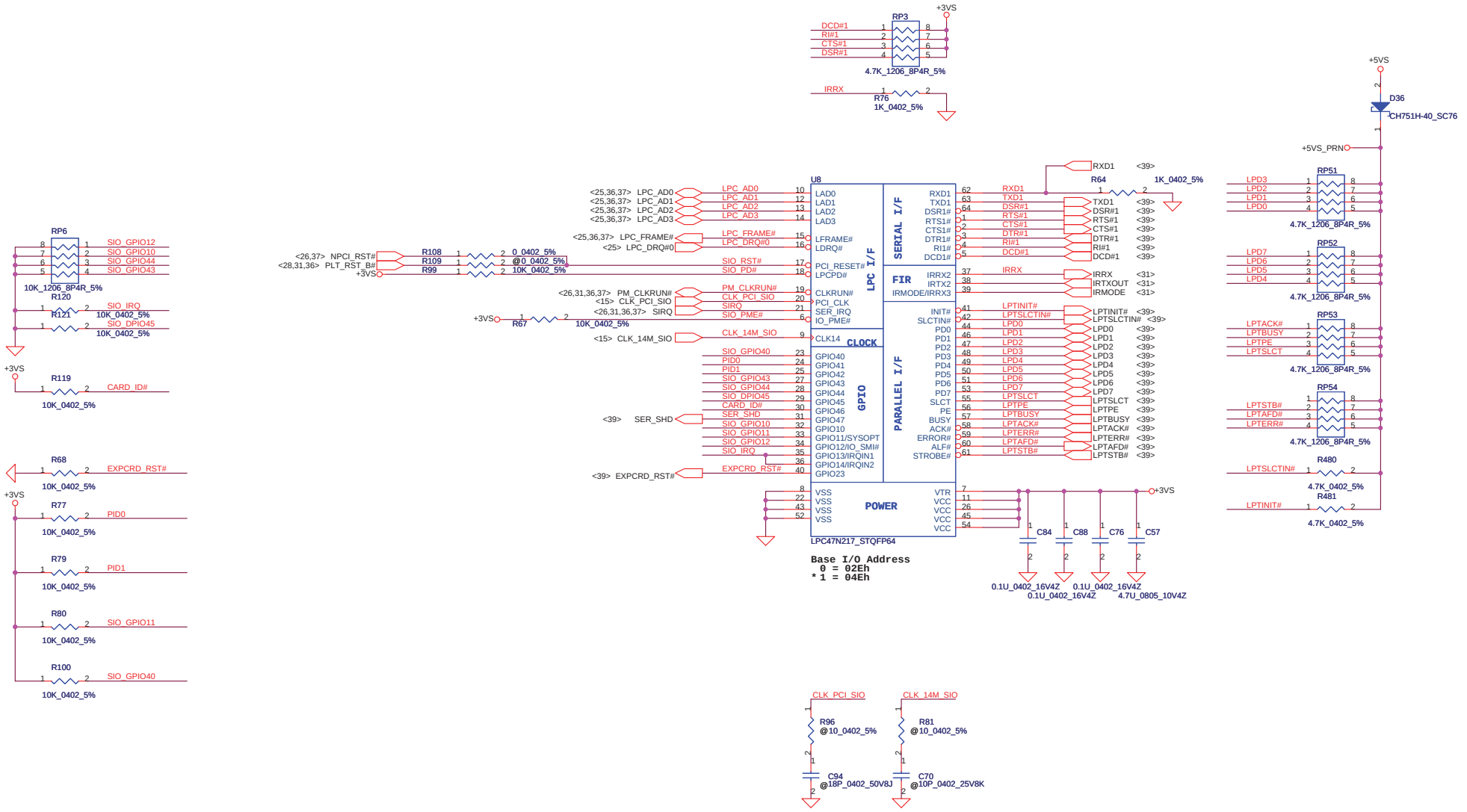


BT Connector



Security Classification	Compal Secret Data		
Issued Date	2006/09/25	Deciphered Date	2006/09/25

Compal Electronics, Inc.			
Title: USB & BT Connector			
Size	Document Number: LA3262P_DIS__M64		Rev: 1A
Date: Tuesday, August 21, 2007		Sheet 34 of 57	



Security Classification	Compal Secret Data		
Issued Date	2006/09/25	Deciphered Date	2006/09/25

Compal Electronics, Inc.			
Title	SUPER I/O LPC47N217		
Size	Document Number		Rev
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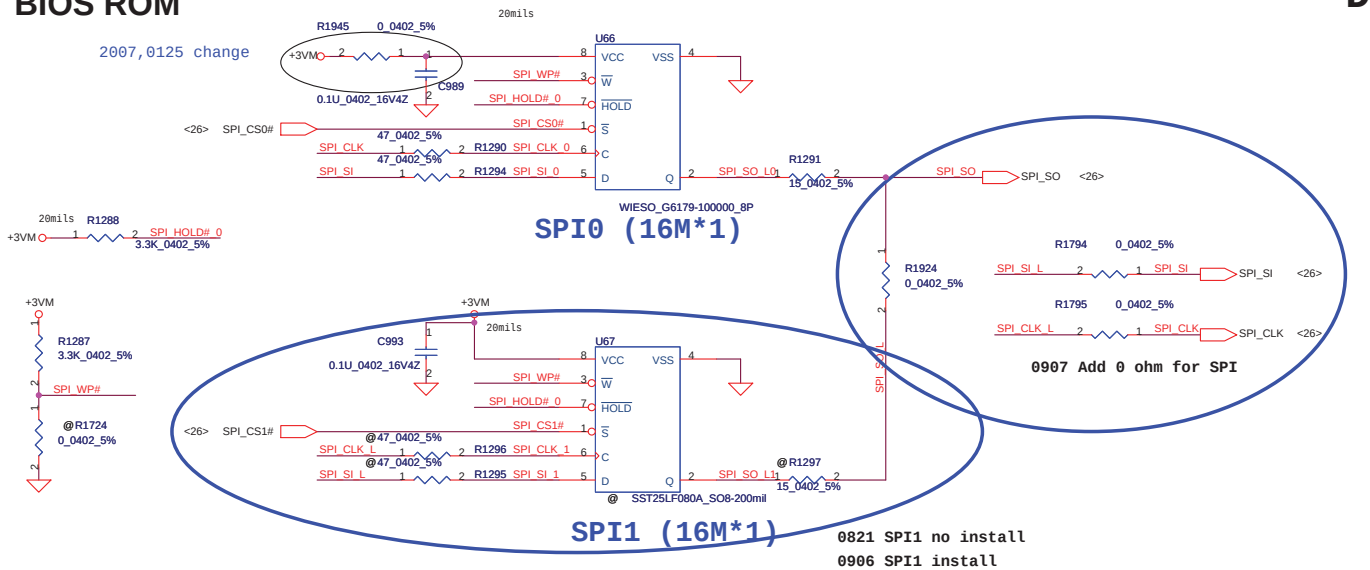
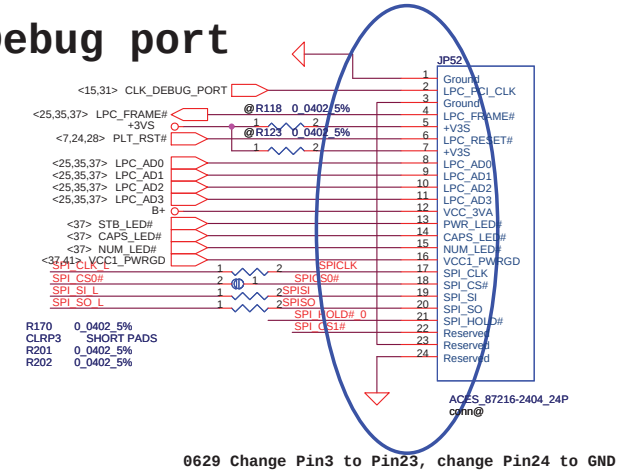
BIOS ROM

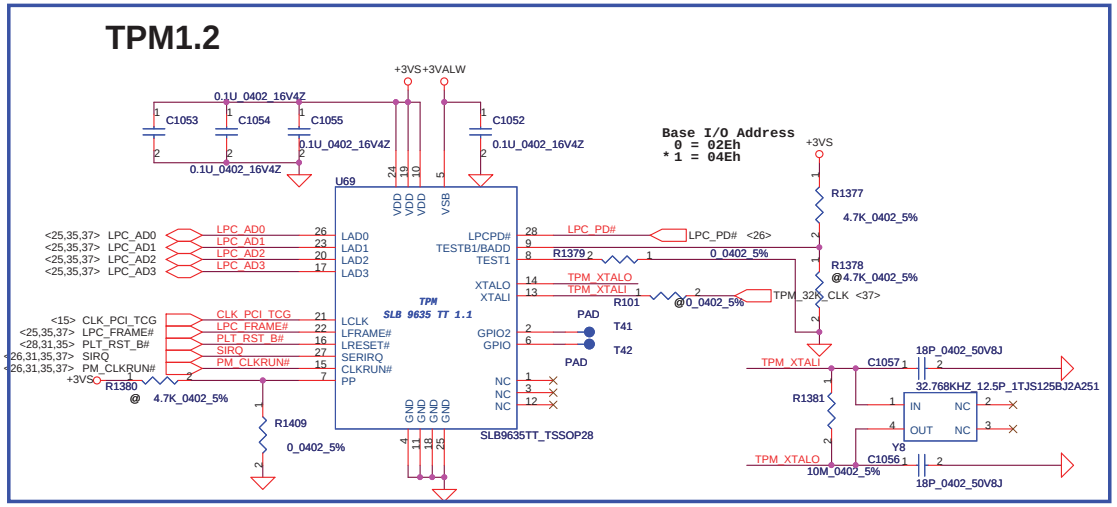
2007,0125 change



Debug port

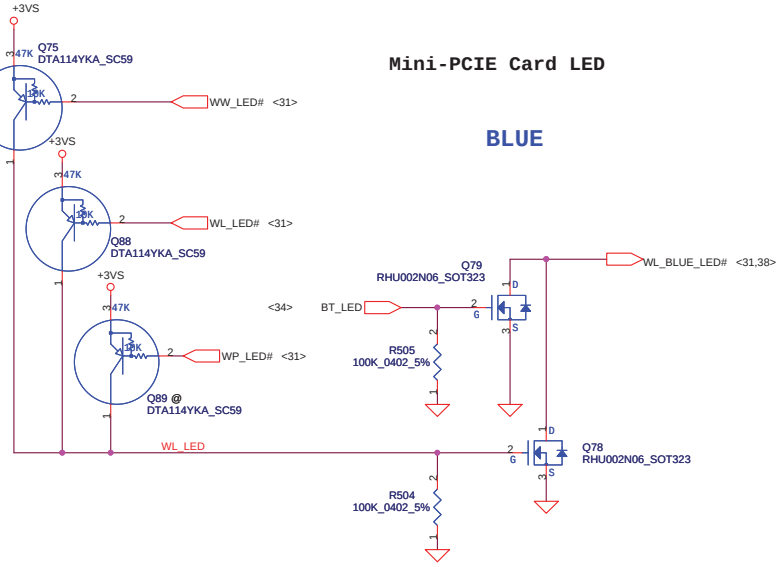


TPM1.2

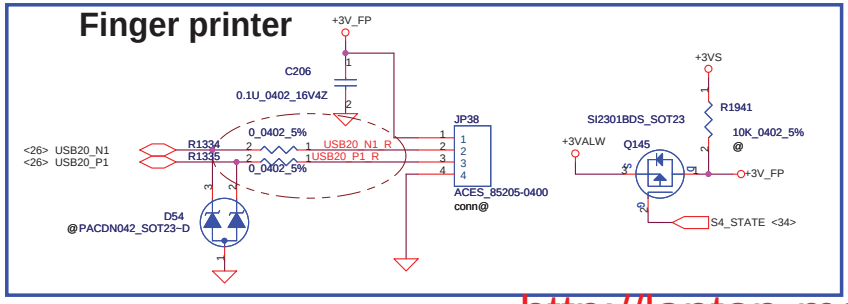


Mini-PCIE Card LED

BLUE



Finger printer



Security Classification	Compal Secret Data		
Issued Date	2006/09/25	Deciphered Date	2006/09/25

Compal Electronics, Inc.	
Title	TCG/BIOS ROM/PS2/LED/SW
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2/22 change

U47 SMSC_1070_TQFP-128P

Keyboard/Mouse Interface

General Purpose I/O Interface

Access Bus Interface

Miscellaneous

LPC Bus

Power Mgmt/SIRQ

KBC1070_VTQFP128

BIOS debug port
Place under KB area

For KBC debugging used.

AGND FILTER

11/20 for solve PM_PWROK glitch on power up

Security Classification	Compal Secret Data		
Issued Date	2006/09/25	Deciphered Date	2006/09/25

Compal Electronics, Inc.

Title: LPC47N1021

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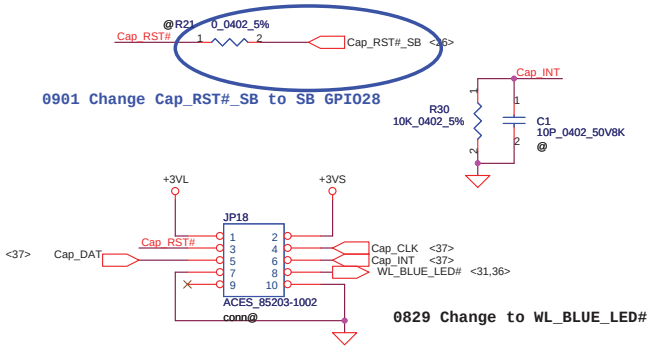
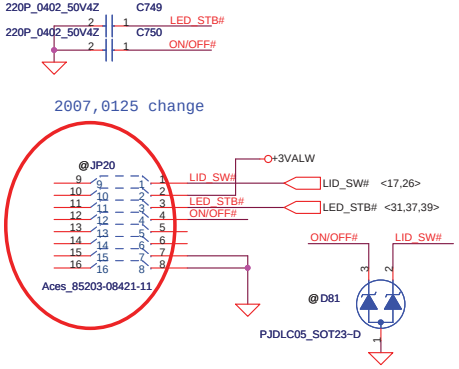
SWITCH BOARD.

0622 change

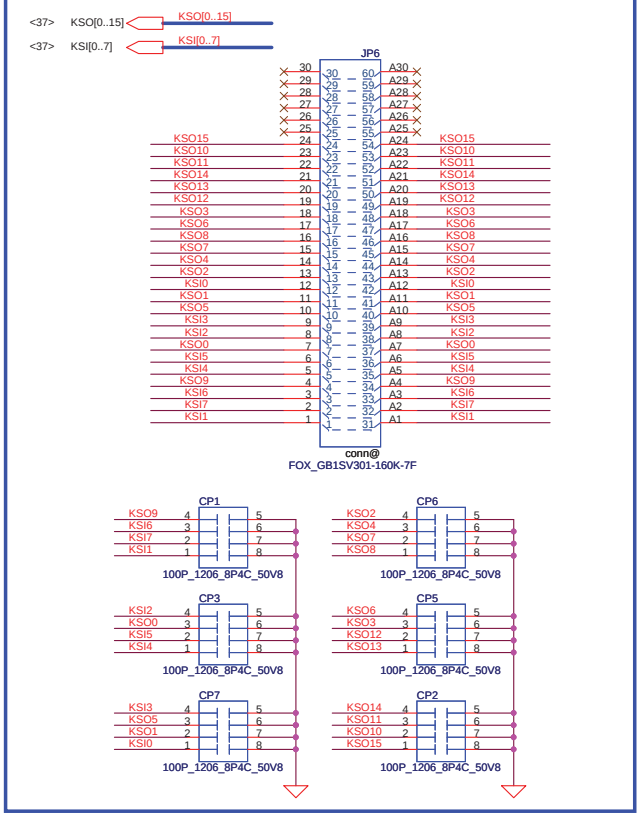


WL,Vol up,Vol down,Mute,Present button



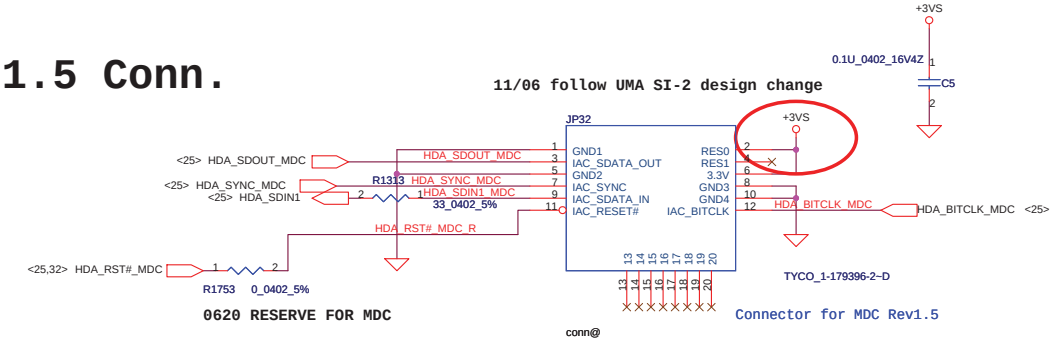
On/off ,information button

INT_KBD CONN.

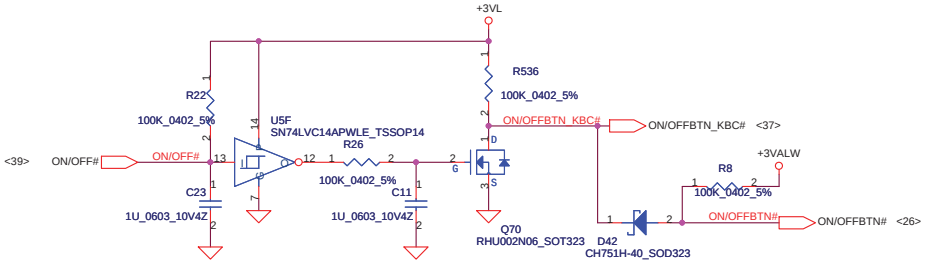


MDC 1.5 Conn.

11/06 follow UMA SI-2 design change

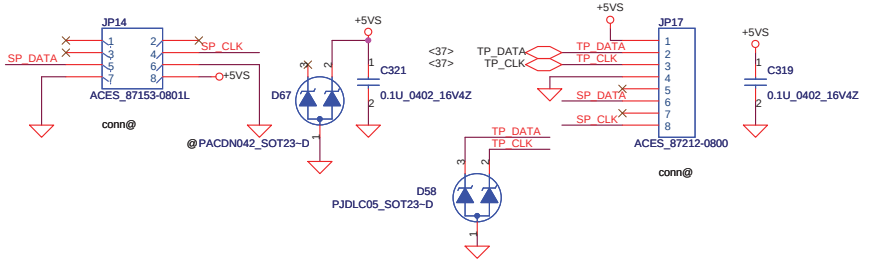


Power button



TrackPoint CONN.

T/P BOARD.



Security Classification	Compal Secret Data		
Issued Date	2006/09/25	Deciphered Date	2006/09/25

Compal Electronics, Inc.			
Title	MDC/KBD/ON_OFF/LID		
Size	Document Number		Rev
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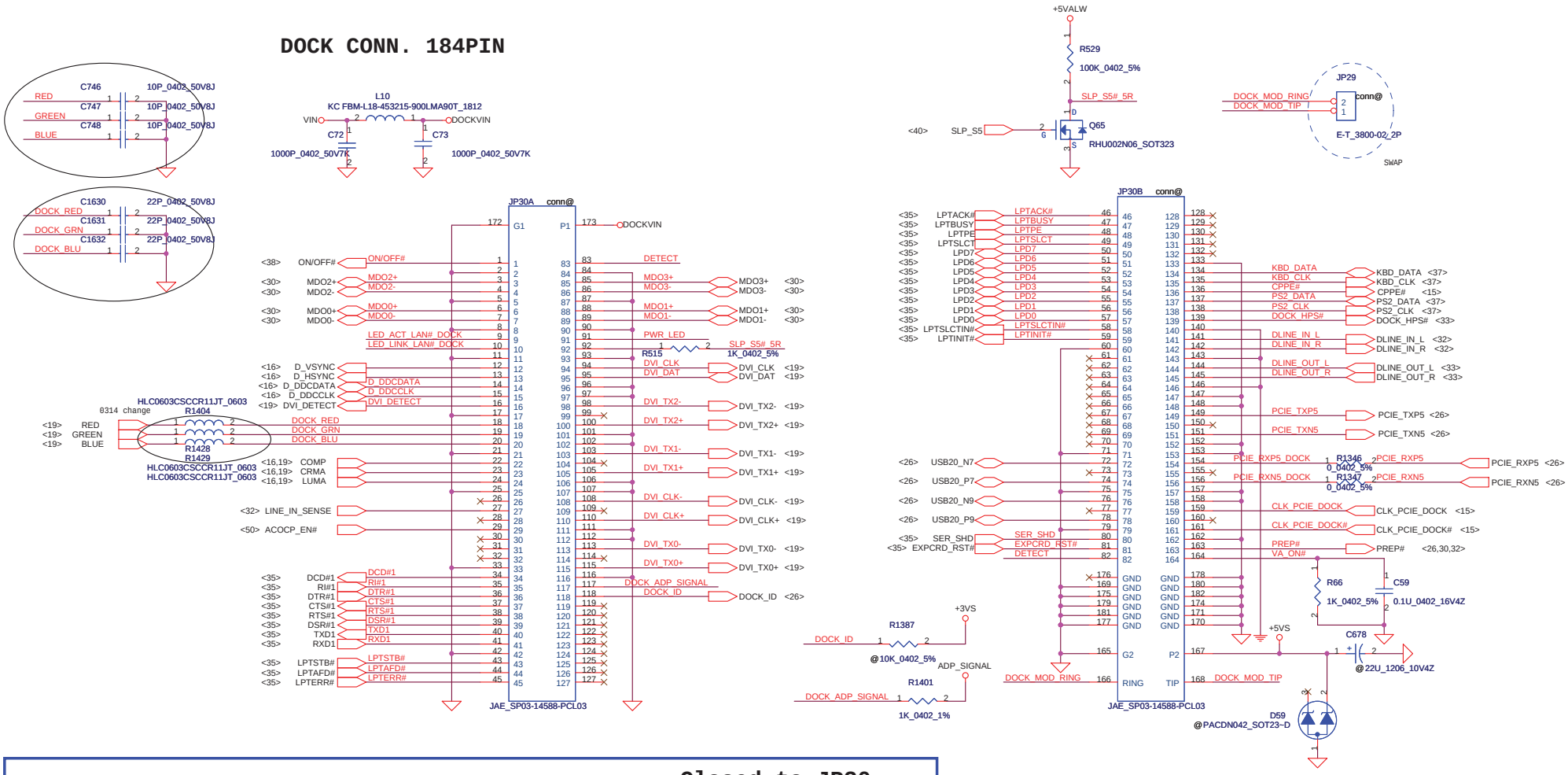
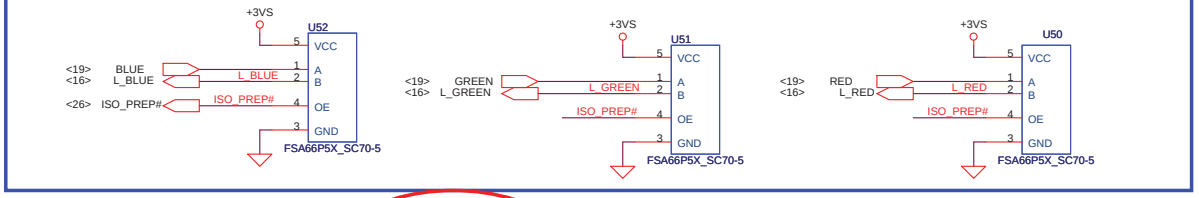
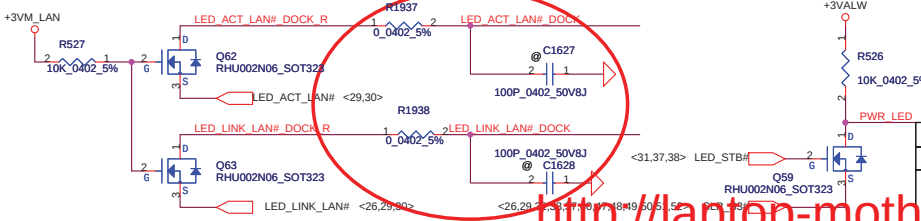
DOCK CONN. 184PIN



Closed to JP30

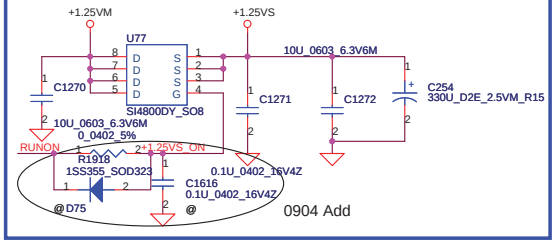




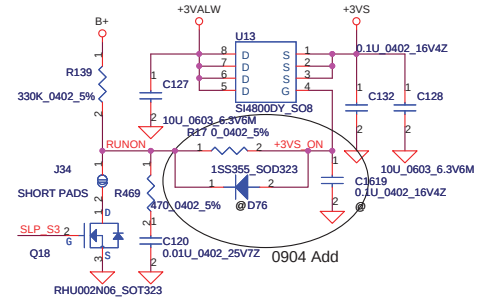
Security Classification	Compal Secret Data		
Issued Date	2006/09/25	Deciphered Date	2006/09/25

Compal Electronics, Inc.			
Title: Docking CONN.			
Size	Document Number: LA3262P_DIS__M64		Rev: 1A
Date: Tuesday, August 21, 2007	Sheet 39 of 57		

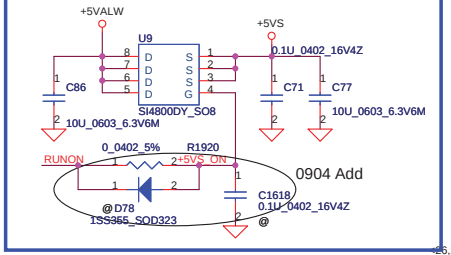
+1.25VM to +1.25VS Transfer



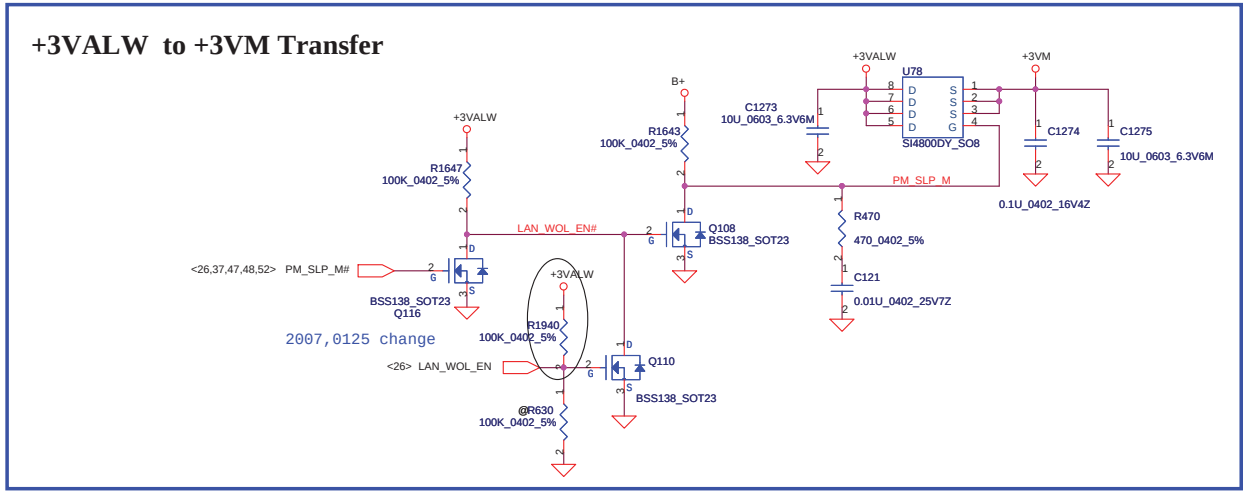
+3VALW to +3VS Transfer



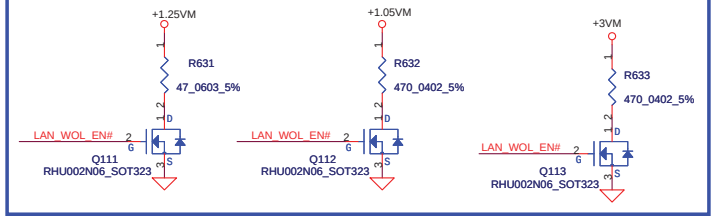
+5VALW to +5VS Transfer



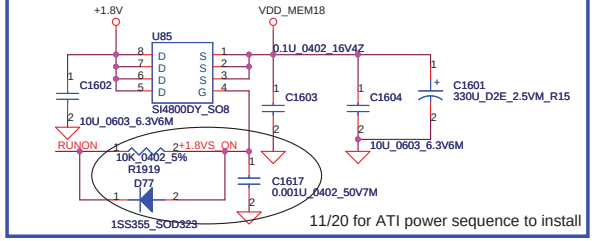
+3VALW to +3VM Transfer

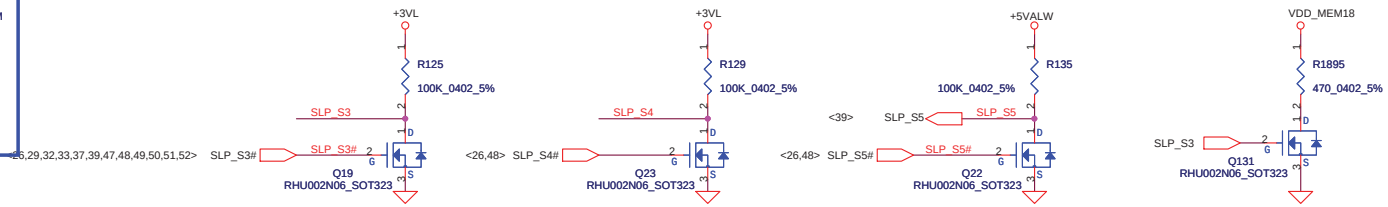


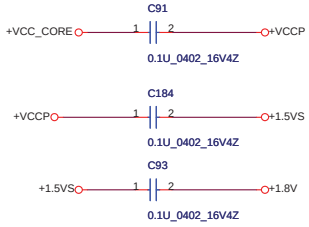
Discharge circuit-2 for V-M



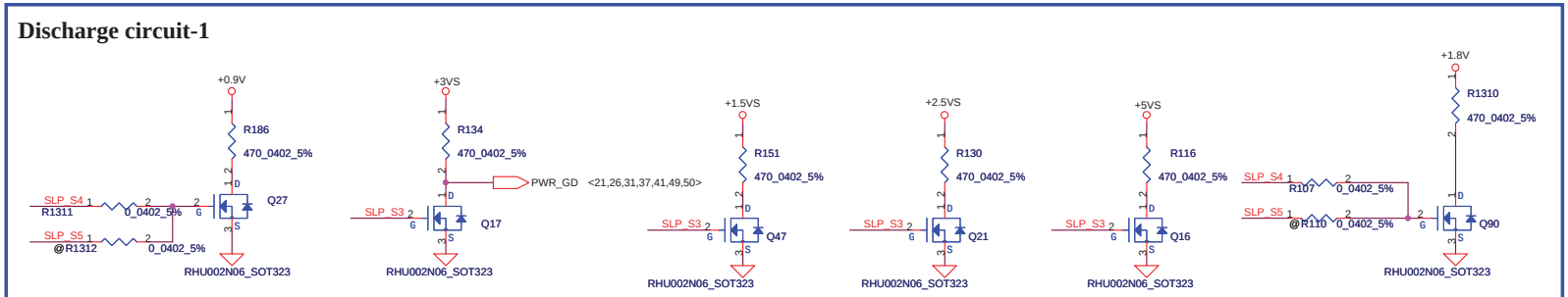
+1.8V to VDD_MEM18 Transfer







Discharge circuit-1



Security Classification	Compal Secret Data		
Issued Date	2006/09/25	Deciphered Date	2006/09/25

Compal Electronics, Inc.

Title: DC/DC Circuits

Size: | Document Number: LA3262P_DIS__M64 | Rev: 1A

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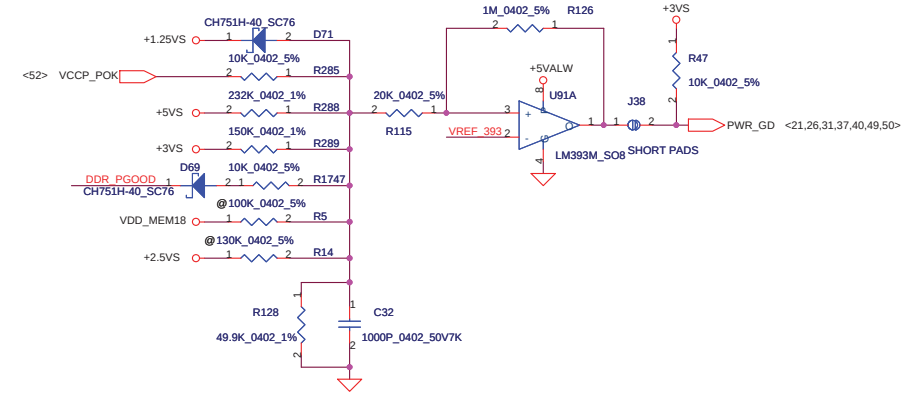
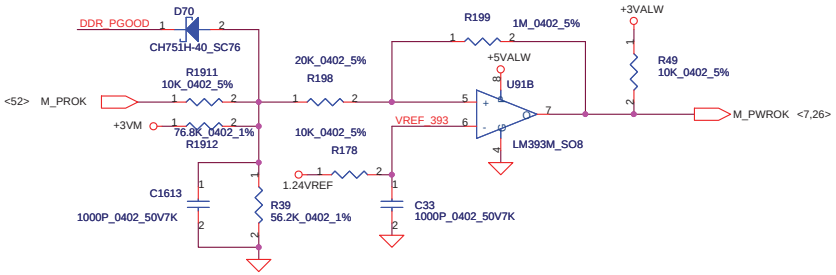
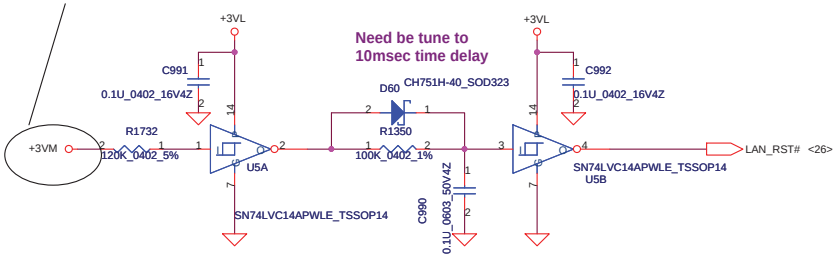
PWR_OK circuit



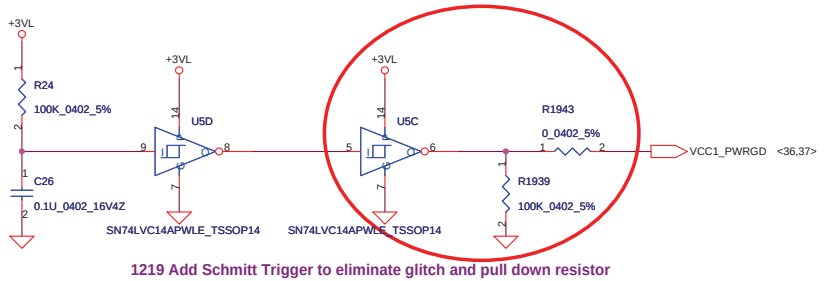


LAN_RST circuit

11/20 Enable ACBS (power management for NIC)



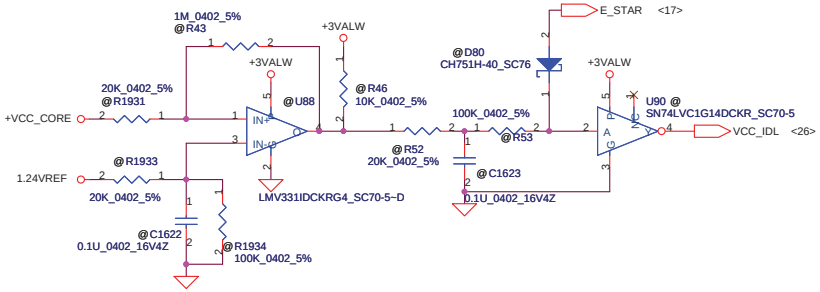
KBC PWR_OK circuit

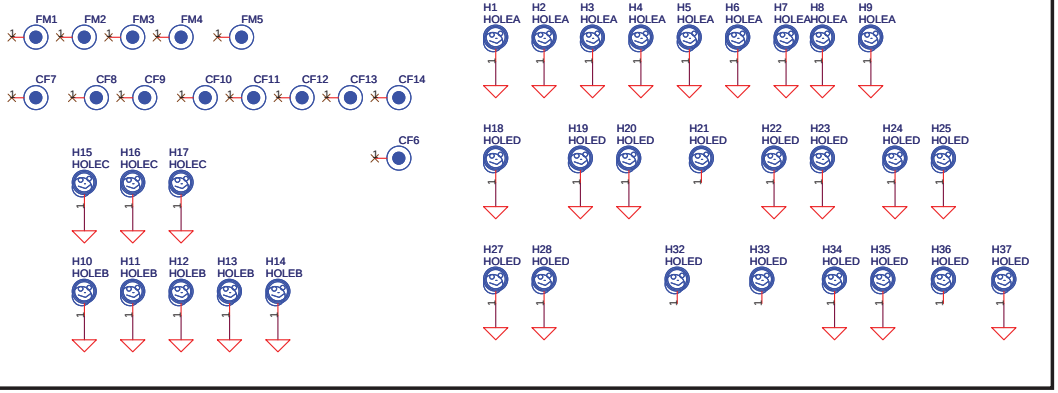


1219 Add Schmitt Trigger to eliminate glitch and pull down resistor

Energy Star for CPU

1114 Add





Security Classification	Compal Secret Data		
Issued Date	2006/09/25	Deciphered Date	2006/09/25

Compal Electronics, Inc.		
Title: POK CKT		
Size	Document Number: LA3262P_DIS__M64	Rev: 1A
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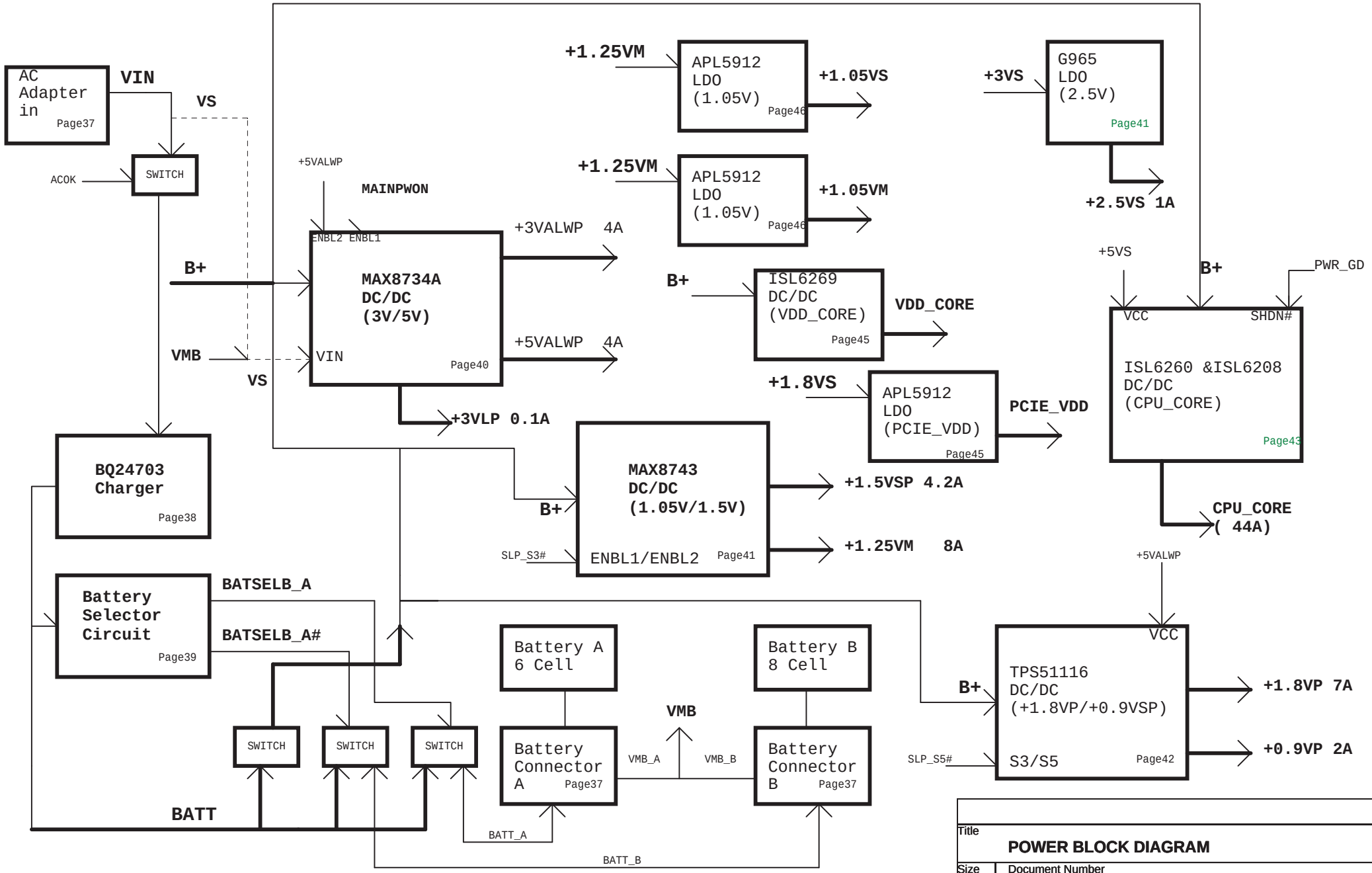

Title: POWER BLOCK DIAGRAM

Size | Document Number | Rev

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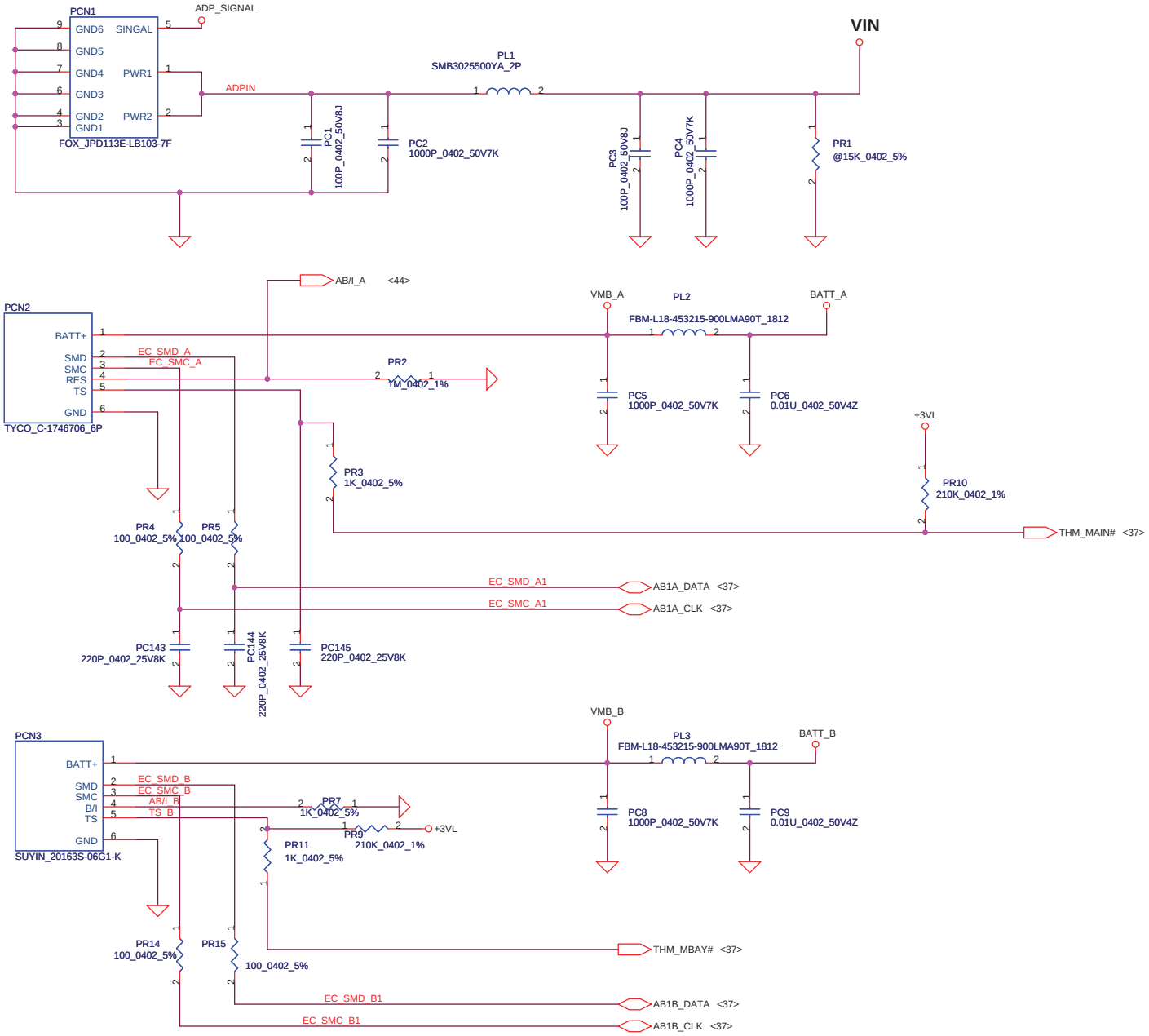

Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **BATTERY CONN**

Size	Document Number	Rev
Custom	LA3262P_DIS__M64	

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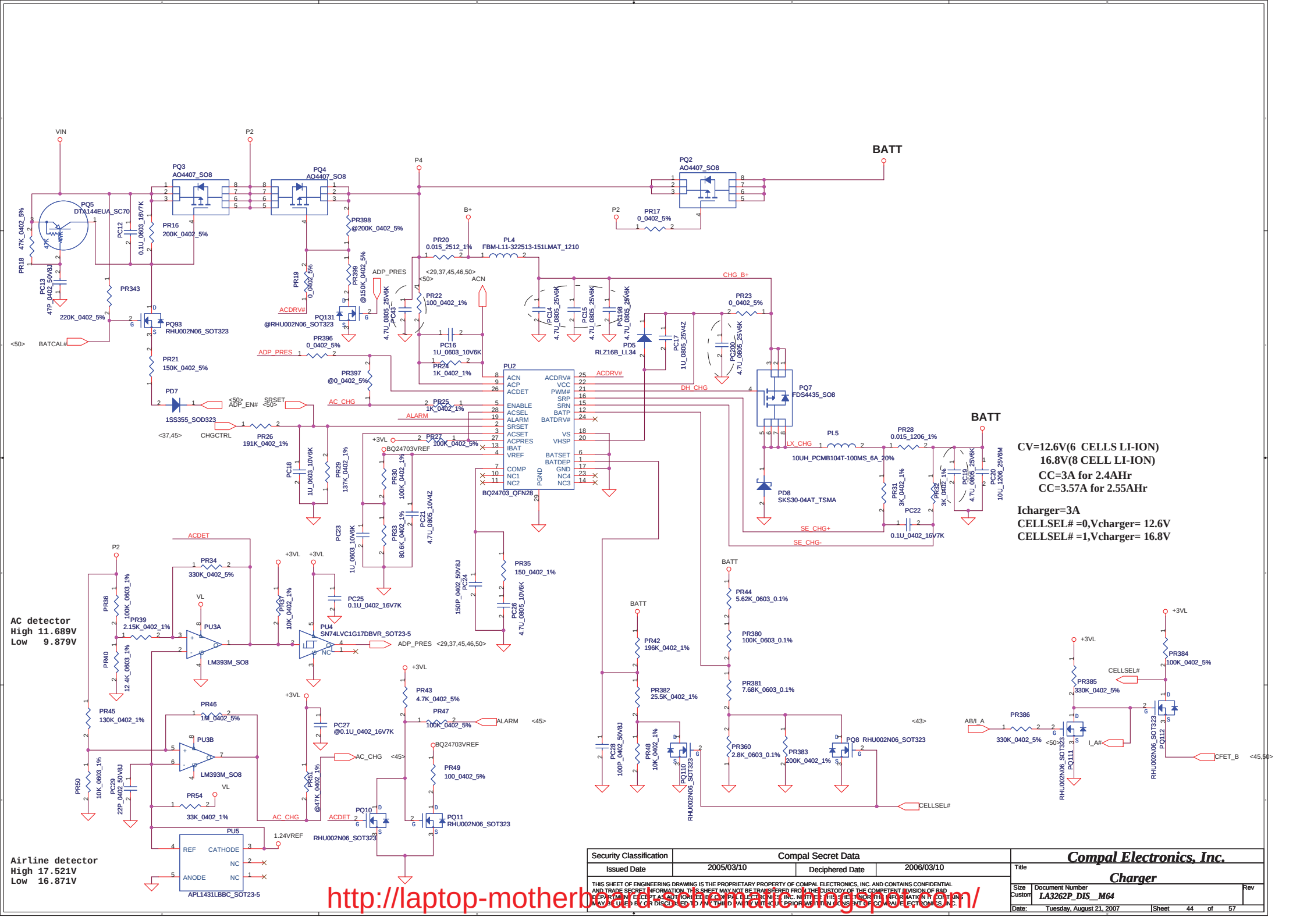

Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **Charger**

Size	Document Number	Rev
Custom	LA3262P_DIS__M64	

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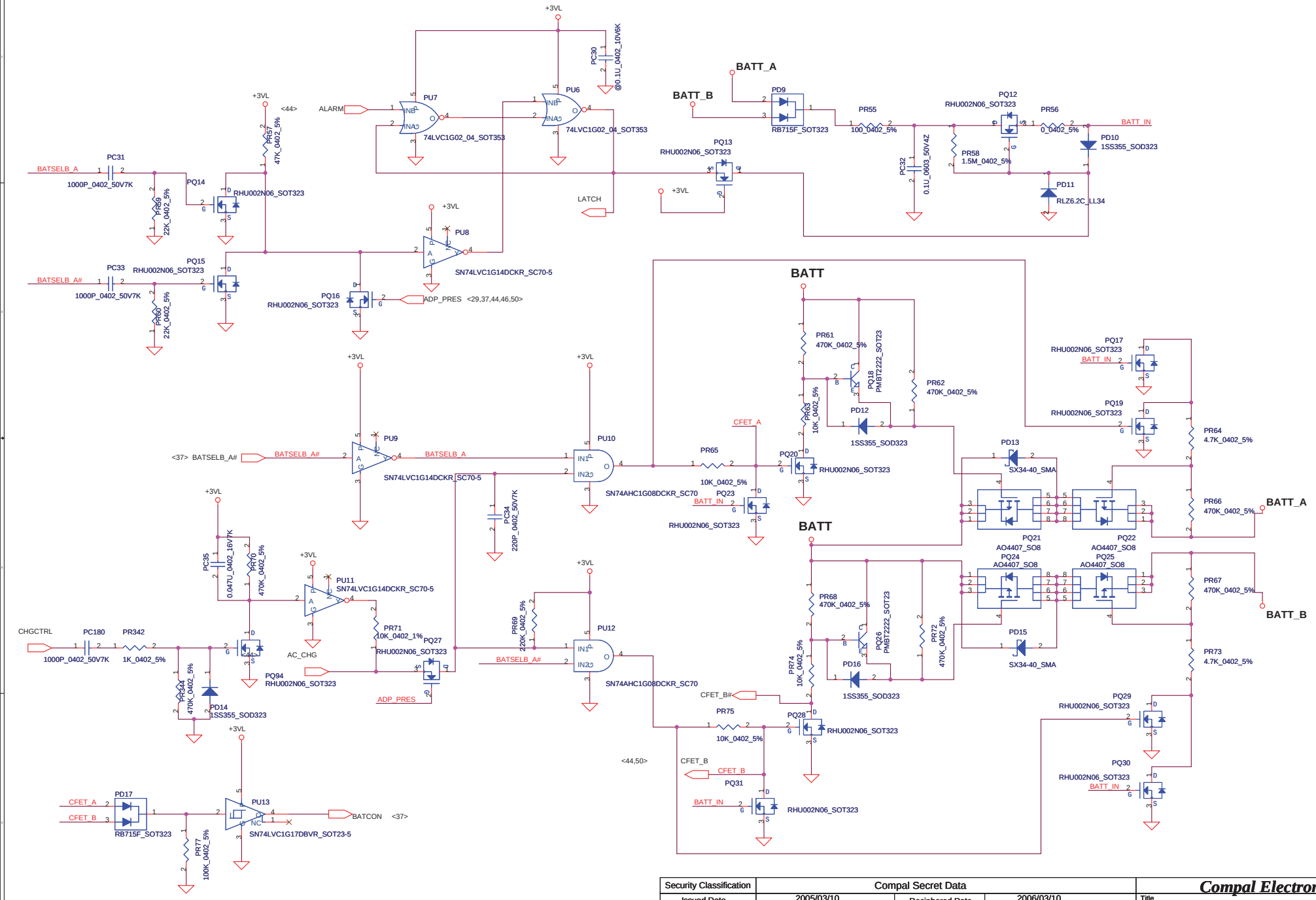

Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **Battery selector**

Size	Document Number	Rev
Custom	LA3262P_DIS__M64	

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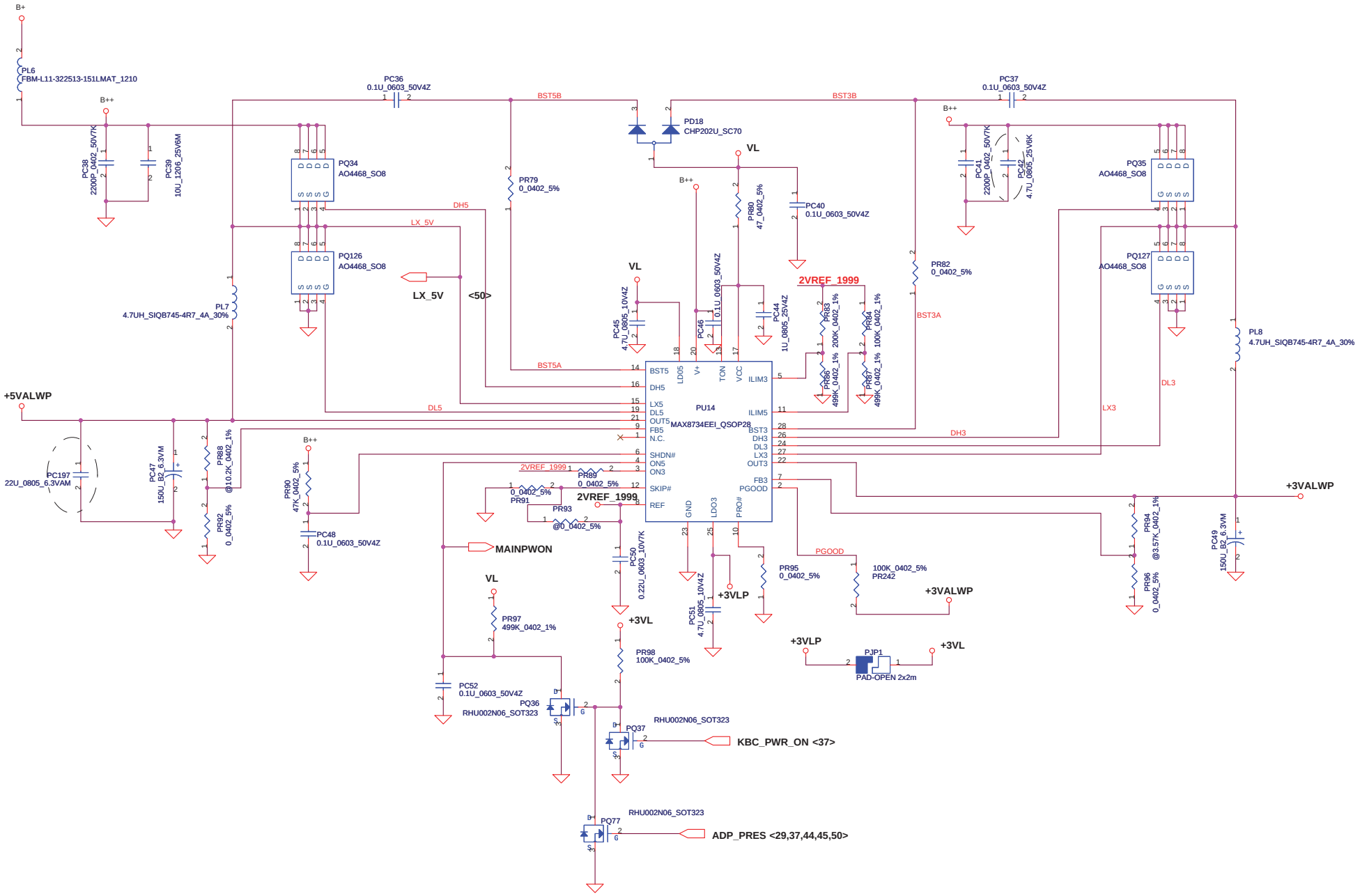
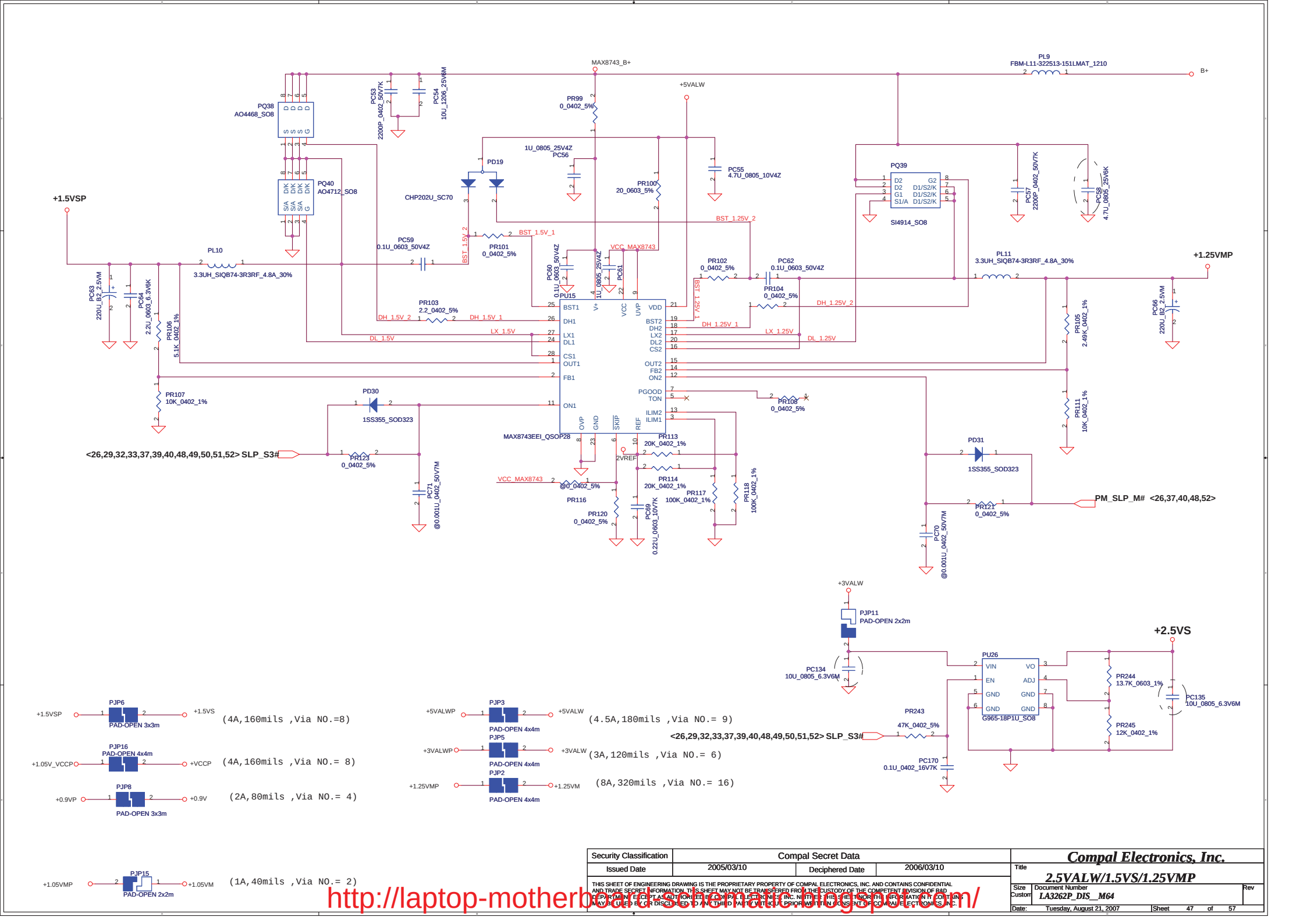


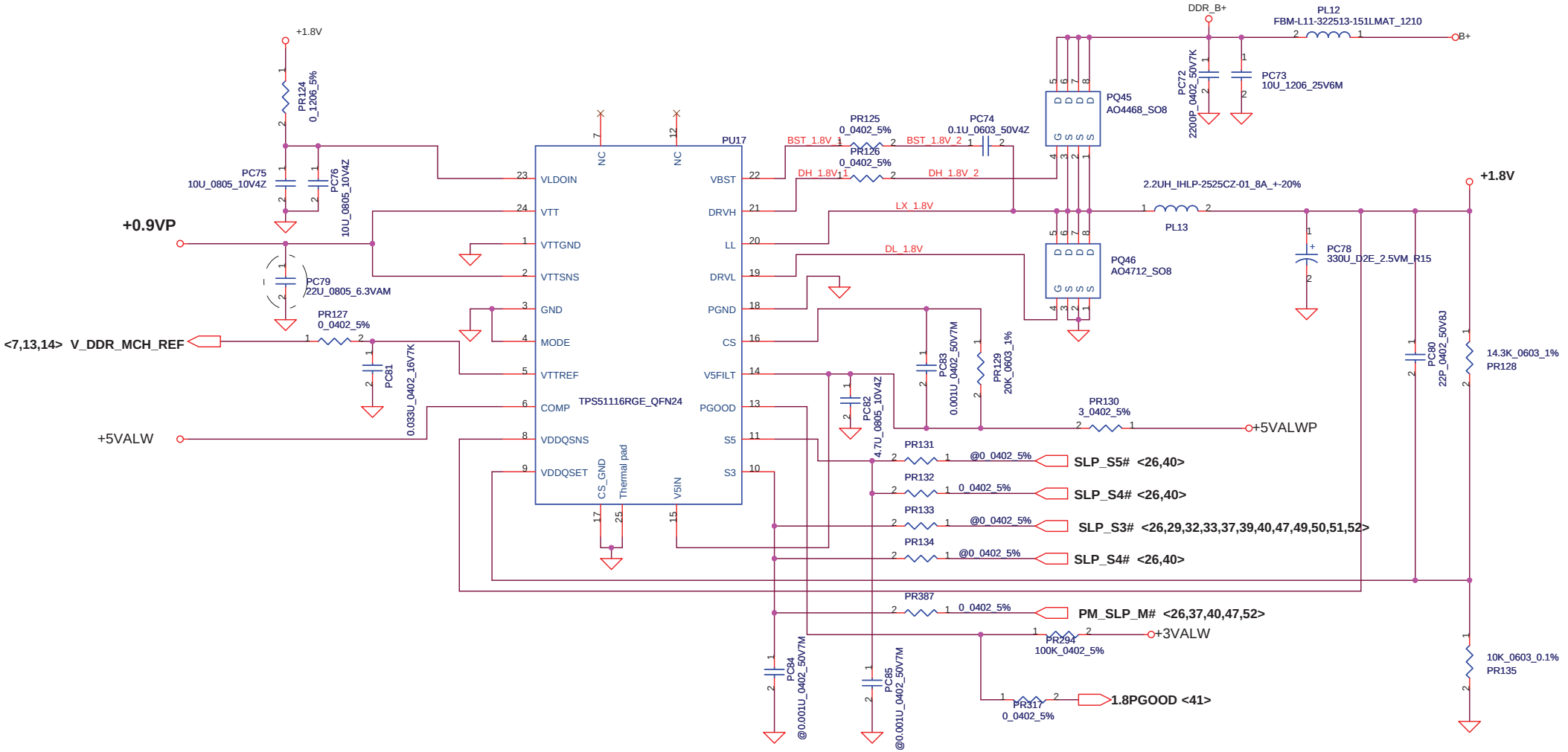
Security Classification	Compal Secret Data		
Issued Date	2005/03/01	Deciphered Date	2006/03/01

Title	3.3V / 5V		
Size B	Document Number LA3262P_DIS__M64		Rev 1A
Date: Tuesday, August 21, 2007	Sheet 46 of 57		



Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

Compal Electronics, Inc.			
Title: 2.5VALW/1.5VS/1.25VMP			
Size: Custom	Document Number: LA3262P_DIS__M64		Rev
Date: Tuesday, August 21, 2007	Sheet 47 of 57		



Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **1.8V/0.9VS**

Size	Document Number	Rev
B	LA3262P_DIS__M64	

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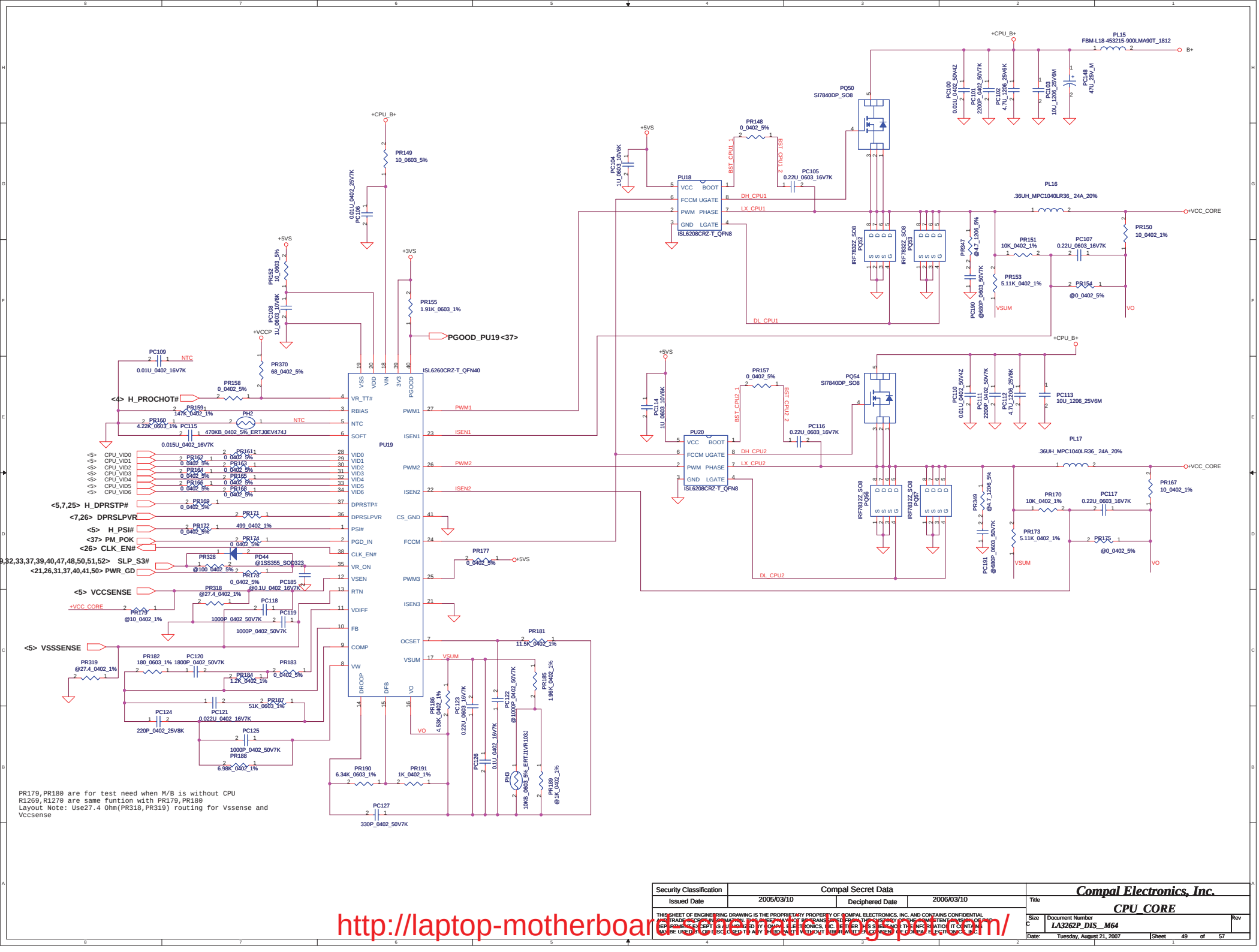

Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: CPU_CORE

Size	Document Number	Rev
C	LA3262P_DIS__M64	

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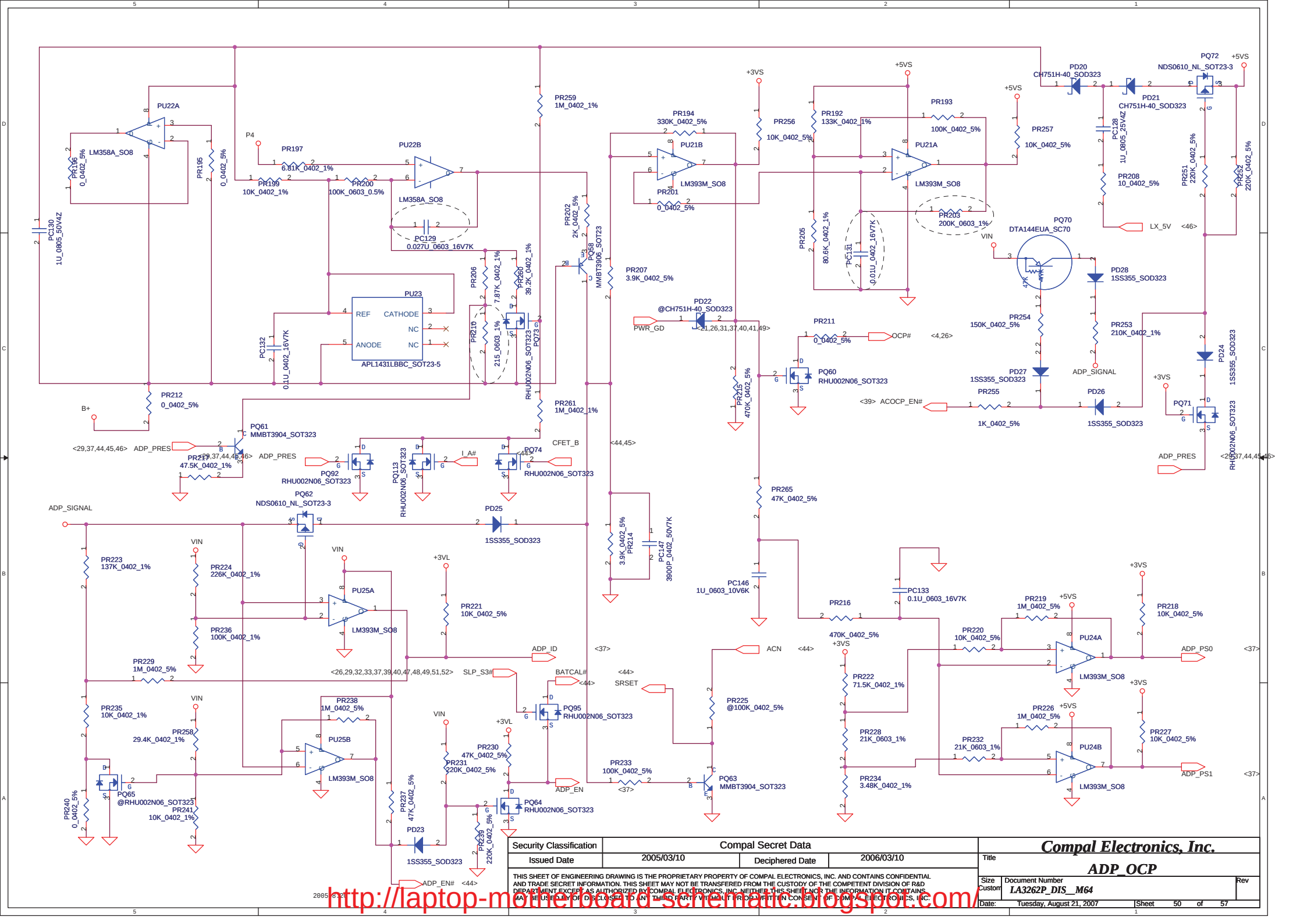

Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **ADP_OCP**

Size	Document Number	Rev
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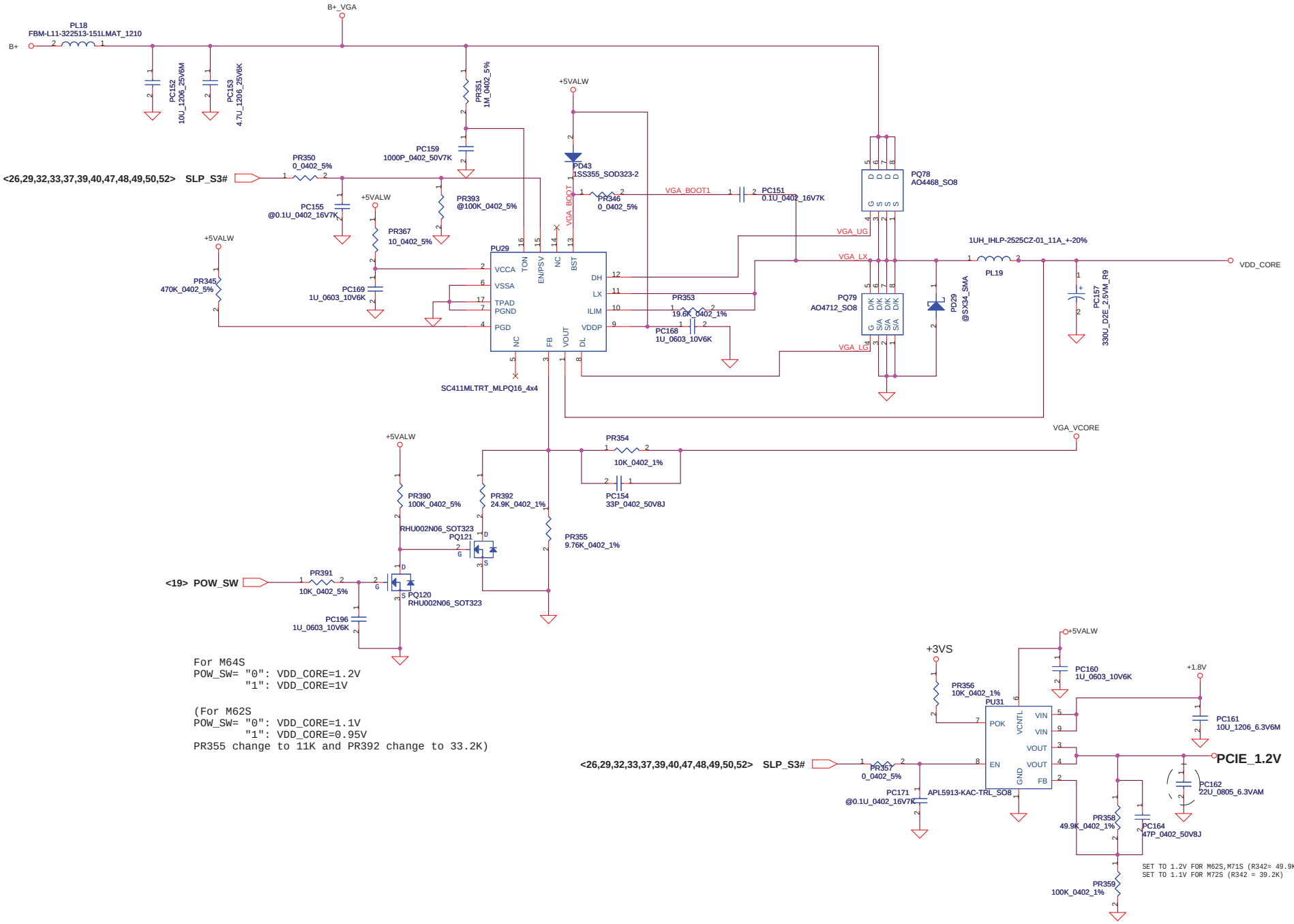

Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **VDD_CORE**

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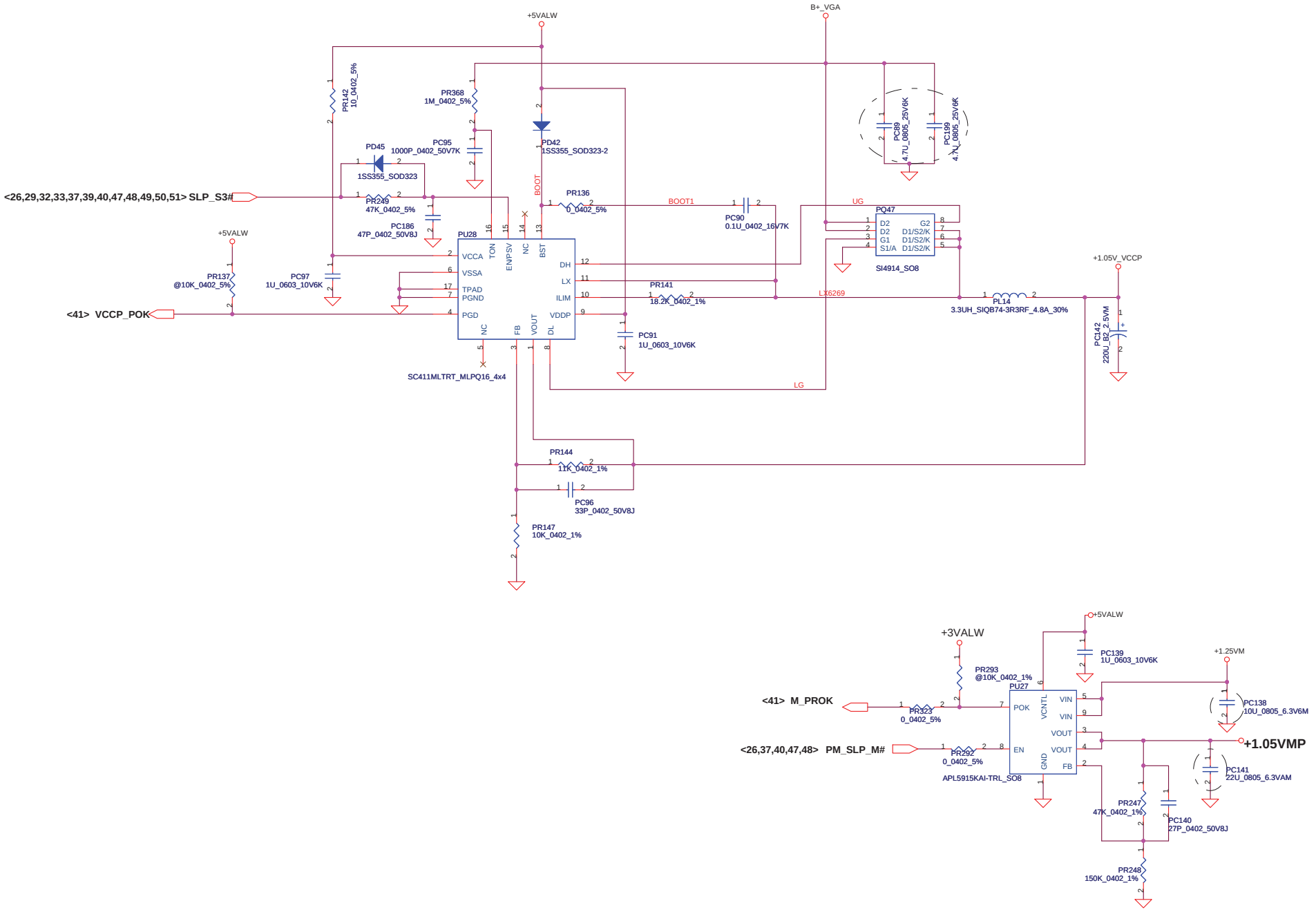

Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **+1.25VMP/+1.05V_VCCP**

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Version Change List (P. I. R. List) for Power Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Cut in
1	43 44 50	DCIN/ BATTERY CONN Charger ADP_OCP	2006/09/07	HP R.L.	Change charger control from HW to FW	All the related components	DB1B
2	50	ADP_OCP	2006/10/12	HP R.L.	Identify 65W adapter as "light"	Change PR223 from 180K to 147K	DB2
3	51	VDD_CORE /PCIE_VDD	2006/10/12	HP R.L.	Change VGA chipset from ATi M62S to M64S	Change PR355 from 11K to 9.76K Change PR392 from 33.2K to 24.9K	DB2
4	52	+1.25VMP/ +1.05V_VCCP	2006/10/12	HW Tony J	For HW's requirement, fine tune +1.05V_VCCP sequence	Change PR249 from 0 to 47K Add PC186 as 47pF Install PD45	DB2
5	51	VDD_CORE /PCIE_VDD	2006/10/12	PWR Francis H	Fine tune PCIE_VDD	Change PR358 from 47K to 49.9K Change PR359 from 150K to 100K	DB2
6	51	VDD_CORE /PCIE_VDD	2006/11/08	HW Tony J	Fine tune the GPU "Power Play" sequence	Add PC196 as 1uf	SI
8	51	VDD_CORE /PCIE_VDD	2006/11/08	HW Tony J	Fine tune the power sequence of PCIE_VDD	Change PU31 pin5, 9 source from VDD_MEM18 to +1.8V	SI
9	44	Charger	2006/11/08	PWR Francis H	Base on "Energy STAR" spec, reduce S5 and S3 power consumption (AC mode)	Uninstall PQ11	SI
10	48	1.8V/0.9V	2006/11/08	HP	Add PM_SLP_M# sequence	Add PR387	SI
11	52	+1.25VMP/ +1.05V_VCCP	2006/11/20	HW Tony J	For HW's requirement, fine tune +2.5VS sequence	Change PR243 to 47K, Change PC170 to 0.1uF	SI
12	52	+1.25VMP/ +1.05V_VCCP	2007/2/28	HW Tony J	Fine tune the +2.5VS power level to 2.57V (typ)	Change PR244 from 13K to 13.7K	SI2
13	50	ADP_OCP	2007/2/28	HP R.L.	System identity	Change PR223 from 147K to 137K	SI2
14	44	Charger	2007/3/1	PWR Francis H	Reserve circuit for testing Energy STAR	Reserve PR397, PR398, PR399 and PQ131 Add PR396 as 0 ohm.	PV
15	51	VDD_CORE /PCIE_VDD	2007/3/1	PWR Francis H	MOSFET change for M64s (original design is for M72)	Change PQ78 from IRF7413Z to AO4468 Change PQ79 from IRF8113 to AO4712 Change PR353 from 6.81K to 19.6K	PV
16	50	ADP_OCP	2007/4/12	HP R.L.	Fine tune system OCP setting for battery spec	Change PR210 from 422 to 215 Change PC129 from .22u to .027u Change PR203 from 604K to 200K Change PC131 from .027u to .01u	MV
17	44 46 47 48 51 52	Charger 3.3V/5V 1.5VS/1.25VM +1.25VMP/ 1.8V/0.9V VDD_CORE /PCIE_VDD +1.25VMP/ +1.05V_VCCP	2007/7/30	HP R.L.	Change some MLCCs size from 1206 to 0805	1. Change PC14 from 10u_1206 to 4.7u_0805 Add PC198 as 4.7u_0805 2. Change PC89 from 10u_1206 to 4.7u_0805 Add PC199 as 4.7u_0805 3. Change PC15, PC19, PC42 and PC58 from 4.7u_1206 to 4.7u_0805 4. Change PC79, PC141, PC162 and PC197 from 22u_1206 to 22u_0805 5. Change PC134, PC135 and PC138 from 10u_1206 to 10u_0805	MP
18	44	Charger	2007/7/30	TI	For TI's suggestion, add 4.7u at VCC pin	Add PC200 as 4.7u_0805	MP

	Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
<2006.09.11>	1		Dseign issue (Lost VRAM RST pin)	20, 22	Add DRAM_RST# from VGA to VRAM	0.2
	2		Dseign issue (LVDS channel error)	19	Swapped LVDS upper and lower channel	0.2
	3		Dseign issue (HSYNC & VSYNC error)	19	Swapped VSYNC & HSYNC each other	0.2
	4		isolate ESD to CPU core via USB and 1394 conn's pin	34	Add R4, R73 and R56	0.2
	5		Follow ATI design suggestion for VDDR4, VDDR5	21	change and reserve two jopens for +1.8VS and +3VS power rails	0.2
	6		Follow ATI design suggestion for DPLL_VDDC	21	delete R1892	0.2
	7		follow ATI power sequence	40	Add +1.25VS, +3VS, +5VS and VDD_MEM18 delay circuits.	0.2
<2006.10.14>	1		RGB signal EA failed and CRT display garbage	16, 19	Change CRT circuit from MAX9511 to RLC circuit.	0.3
	2		RGB signal EA failed and CRT display garbage	39	Change CRT circuit from MAX9511 to RLC circuit. Add Q/Switch circuit.	0.3
	3		follow ATI power sequence	21	install R1898 aand C1605, uninstall R1897	0.3
	4		Increase VDD_MEM18 via holes	23	VDD_MEM18 no power noise, remove 1206 size resister.	0.3
	5		Cancel Kill switch function on Chimay	28	uninstall JP53, R1906, R1736 and Q136	0.3
	6		change 1394 bus route on board	31	re-define JP13 pins' assignment	0.3
	7		implement one 4MB SPI chip	36	add R1794, R1795, R1924	0.3
	8		implement 30pins KBC connector	38	re-define KBC connector JP6 pins assignment	0.3
<2006.11.20>	1		HP request, support Penryn CPU	4	Add R23, R34	0.4
	2		For Intel ES2 Crestline thermtrip pin.	7	Add R2	0.4
	3		For EMI request enable 27MHz_SSC	15	install R1687	0.4
	4		For Intel ES2 NB 800/667M Hz issue	15	Add CLRP4, CLRP5 to select FSB speed.	0.4
	5		For RTC Accuracy fail to change	25	Change C528, C516 to 15pf	0.4
	6		For detect CPU and system power saving	26	Add some components	0.4
	7		Solve auto-turn on	26	install R1590 pull up to +3valw, uninstall R1727	0.4
	8		Enable ACBS (power management for NIC)	29	install Q102, uninstall R1612, Q104, Q105	0.4
	9		Enable ACBS (power management for NIC)	30	Change R1639 value to 1.87k	0.4

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	Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
<2006.11.20>	10		Add Energy Star for CPU schematics	41	reserve R1931, R1934, R1933, C1622, U88, U90, R43, R46, R52, R53, C1623, D80	0.4
	11		Enable ACBS (power management for NIC)	41	Change R1732 pin2 from +3VM_Lan to +3VM	0.4
	12		HP request	38	MDC power change to +3vs	0.4
	13		Follow ATI power sequence	40	Install D77, C1617, change R1919 to 10K	0.4
<2007.01.25>	1		For HP request	40	Add R1940 and pull up +3valw	0.5
	2		For 3VL/VCC1_PWRGD glitch change	41	Add U5C and R1939 pull down	0.5
	3		For KBC VCC2 connection to 3VS	37	install R1646, C75	0.5
	4		For HP request	25	Add Q144 and R1935 instead of D75	0.5
	5		For HP request to install BGA CRACK components	27 12		0.5
	6		For solving Power wireset interfere Fan	38	change JP20 connector Footprint	0.5
	7		For Intel Crestline thermtrip shutdowm	7	Reserve 0.1uf *1 for THERMTRIP#	0.5
	8		For possible Leak during ACBS on PREP# signal	26	Change pull up to +3valw	0.5
	9		For HP request to change Line-in BOM	32	R370, R369 change to 6.04k, R374, R375 change to 2.00k	0.5
	10		For SIM connector supply chain	31	SIM connector footprint change	0.5
	11		For LMV331 supply chain, change to LMV393	41	change U76 & U86 to U91	0.5
	12		For EMI changes for VGA CRT	16	Install C310,C313,C314,R542,R543,R544	0.5
	13		For EMI changes for LED_LAN_DOCK	33	Add R1805,R1806	0.5
	14		For HP request, change R1780.1 to UIM_PWR	31	change R1780.1 to UIM_PWR	0.5
	15		For Intel NIC crystal design	29	Add R1936 30ohm value	0.5
	16		For G-Sensor LED	26	HDD_HALTLED (R15) pull down	0.5
	17		For Intel new design	26	Remove pull ups for STP_PCI# and STP_CPU# uninstall R1581, R1580	0.5
	18		For HP request	36	Add CLRP6 for SPI ROM	0.5
	19		For VGA wavy isse	17	Change C586 to 10uf_1206, add C1629 10uf_1206	0.5

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<2007.02.14>

Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
1		Add FP power supply circuit for Vista	41	reserve R1931, R1934, R1933, C1622, U88, U90, R43, R46, R52, R53, C1623, D80	0.4
2		Enable ACBS (power management for NIC)	41	Change R1732 pin2 from +3VM_Lan to +3VM	0.4
3		HP request	38	MDC power change to +3vs	0.4
4		Follow ATI power sequence	40	Install D77, C1617, change R1919 to 10K	0.4
5		For HP request	40	Add R1940 and pull up +3valw	0.5
6		For 3VL/VCC1_PWRGD glitch change	41	Add U5C and R1939 pull down	0.5
7		For KBC VCC2 connection to 3VS	37	install R1646, C75	0.5
8		For HP request	25	Add Q144 and R1935 instead of D75	0.5
		For HP request to install BGA CRACK components	27 12		0.5
		For solving Power wireset interfere Fan	38	change JP20 connector Footprint	0.5
		For Intel Crestline thermtrip shutdowm	7	Reserve 0.1uf *1 for THERMTRIP#	0.5
		For possible Leak during ACBS on PREP# signal	26	Change pull up to +3valw	0.5
9		For HP request to change Line-in BOM	32	R370, R369 change to 6.04k, R374, R375 change to 2.00k	0.5
10		For SIM connector supply chain	31	SIM connector footprint change	0.5
11		For LMV331 supply chain, change to LMV393	41	change U76 & U86 to U91	0.5
12		For EMI changes for VGA CRT	16	Install C310,C313,C314,R542,R543,R544	0.5
13		For EMI changes for LED_LAN_DOCK	33	Add R1805,R1806	0.5
14		For HP request, change R1780.1 to UIM_PWR	31	change R1780.1 to UIM_PWR	0.5
15		For Intel NIC crystal design	29	Add R1936 30ohm value	0.5
16		For G-Sensor LED	26	HDD_HALTLED (R15) pull down	0.5
17		For Intel new design	26	Remove pull ups for STP_PCI# and STP_CPU# uninstall R1581, R1580	0.5
18		For HP request	36	Add CLRP6 for SPI ROM	0.5
19		For VGA wavy isse	17	Change C586 to 10uf_1206, add C1629 10uf_1206	0.5

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<2007.08.02>

Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
1		Solve VGA can not thermal shutdown and KB dissolve	4	Add R229 (non-install) and contact to THERM#_VGA	1A
2		prevent Cap crack to change Cap size	17	C1629 & C586 size change from 1206 to 0805	1A
3		Solve VGA can not thermal shutdown and KB dissolve	23	Add R1906 (non-install) and R1896 install Add Q30 & Q31	1A
4		Prevent GPIO33 leakage	25	Change Q144 to CHP202U_SC70	1A
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