

Compal confidential

Schematics Document

Mobile Yonah uFCPGA with Intel Calistoga_GM/PM+ICH7-M core logic

2006-07-24

REV:1.0



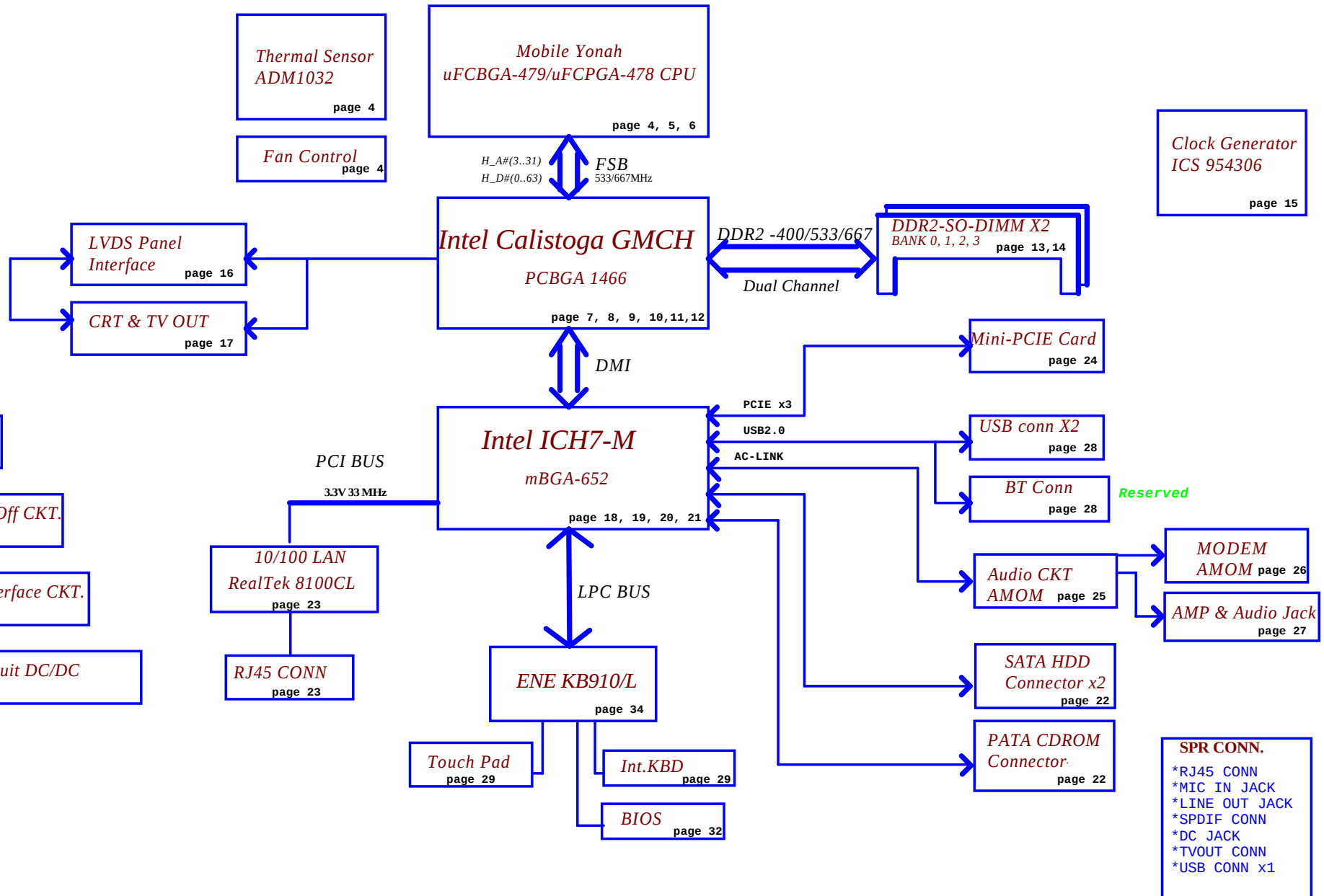
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				Custom	LA-3342P	1.0
				Date:	Thursday, July 27, 2006	Sheet 1 of 40

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						Size	Document Number			Rev
							LA-3342P			1.0
Date:		Thursday, July 27, 2006		Sheet		2		of 40		

Voltage Rails

power plane State	+B LD03 LD05	+5VALW +3VALW	+1.8V +5V	+5VS +3VS +2.5VS +1.5VS +0.9VS +CPU_CORE +VCCP
S0	0	0	0	0
S1	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

0 MEANS ON
X MEANS OFF

PCI Devices

EXTERNAL	IDSEL#	REQ/GNT#	PIRQ
CARD BUS & 1394	AD22	2	C,D,E,G
RealTekK 8100CL	AD24	1	A

Load BOM check item

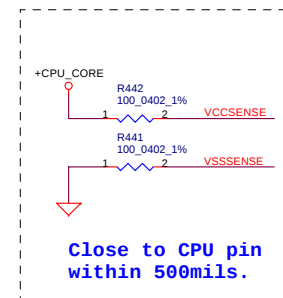
- 1.U31 GM/PM/GML part number
- 2.U6 ICH7 part number

BOM: 43144132L01 (GM)
43144132L02 (GML)

Jump-Short:

PJP4,PJP6,PJP7,PJP8,PJP10,PJP12,PJP14,PJP18,PJP19,PJP20,PJP25

MV step from PIRQE change to PIRQA for LAN poor performance.



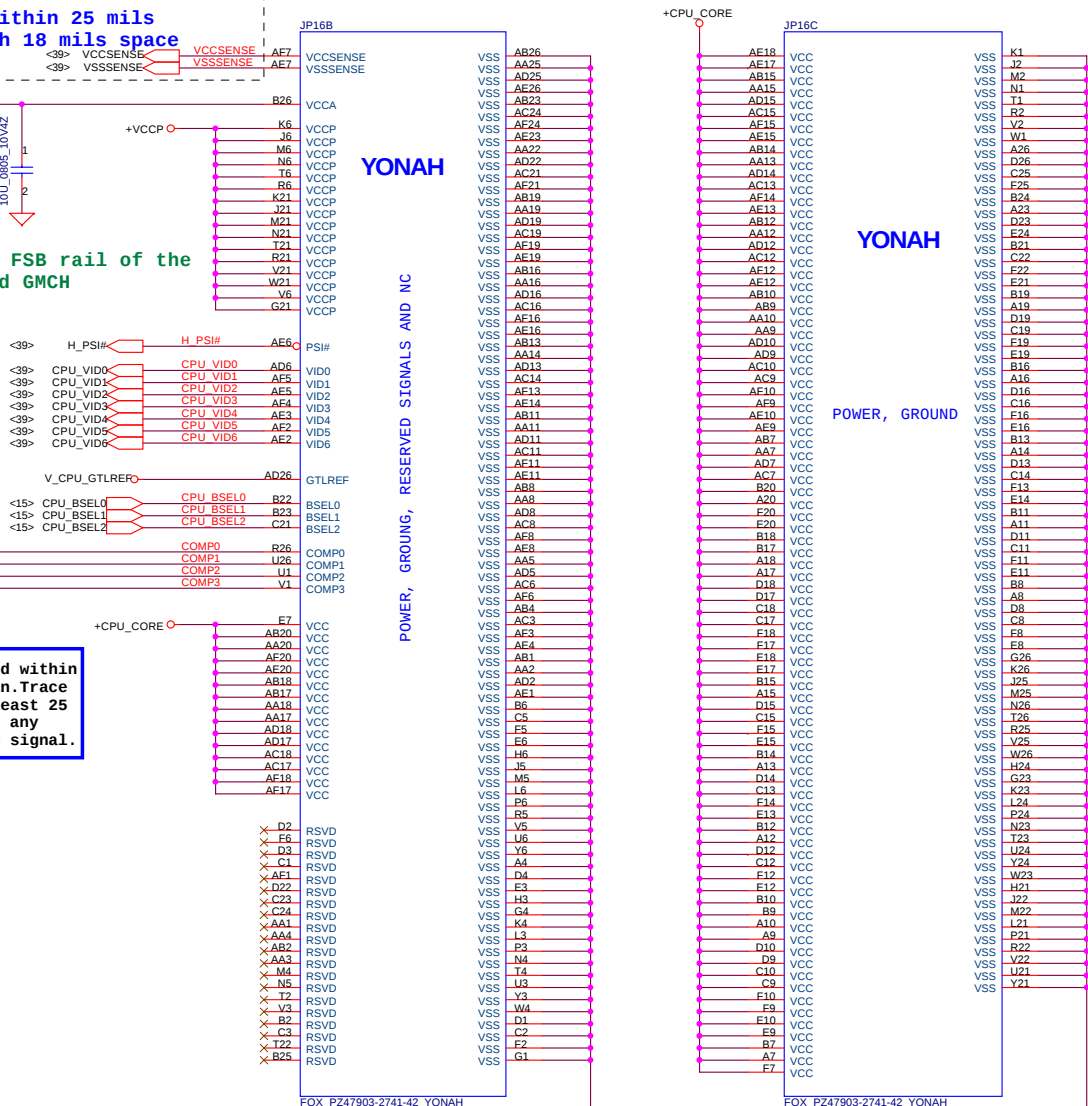
+1.5v is a power source required by the PL clock generator on the processorsilicon

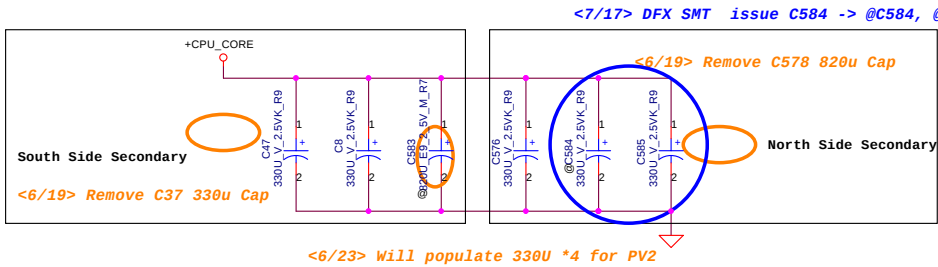
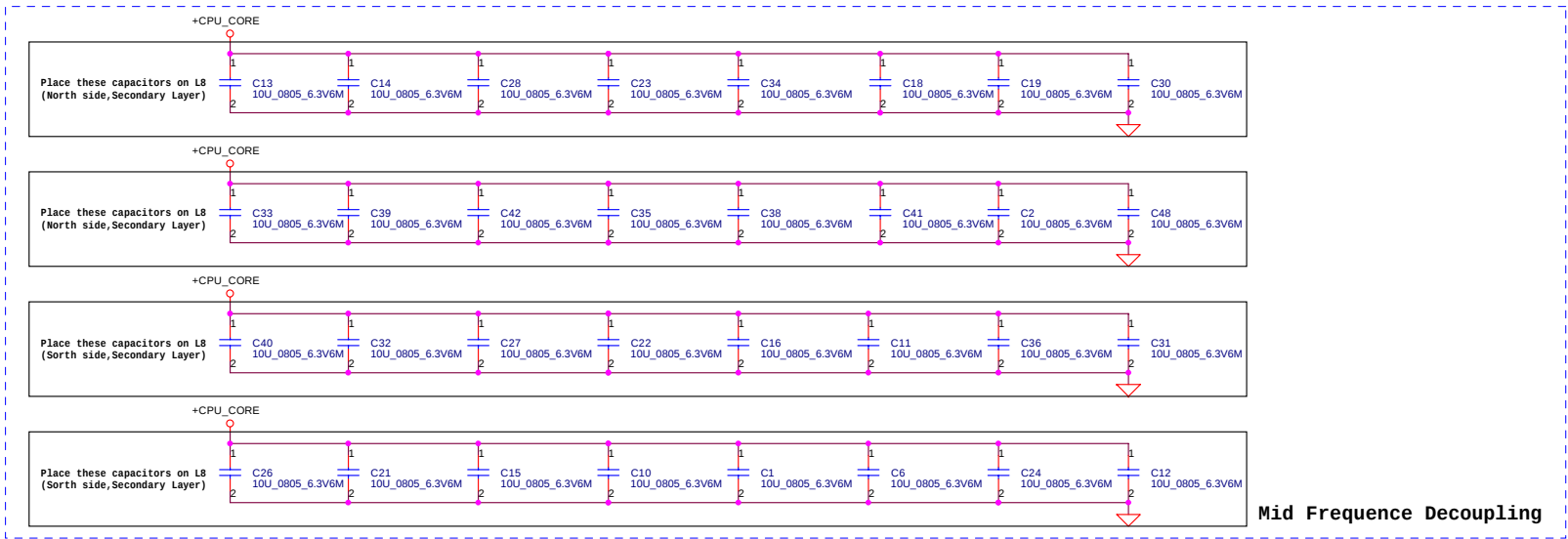
Length match within 25 mils
The trace width 18 mils space
7 mils

+VCCP is the FSB rail of the processor and GMCH

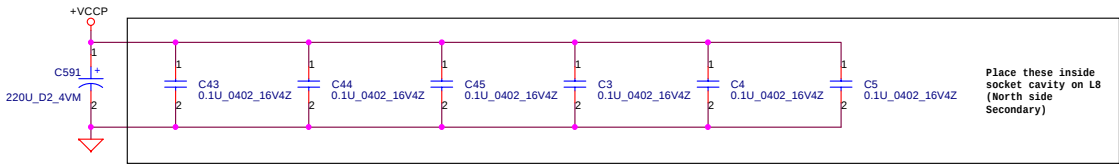
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1

Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal.

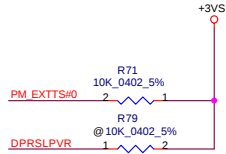
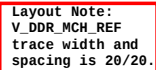
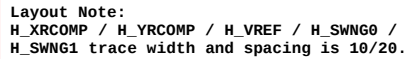




ESR <= 1.5m ohm
Capacitor > 1980uF



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				Custom	LA-3342P
Date: Thursday, July 27, 2006				Sheet	6 of 40
				Rev	0.1

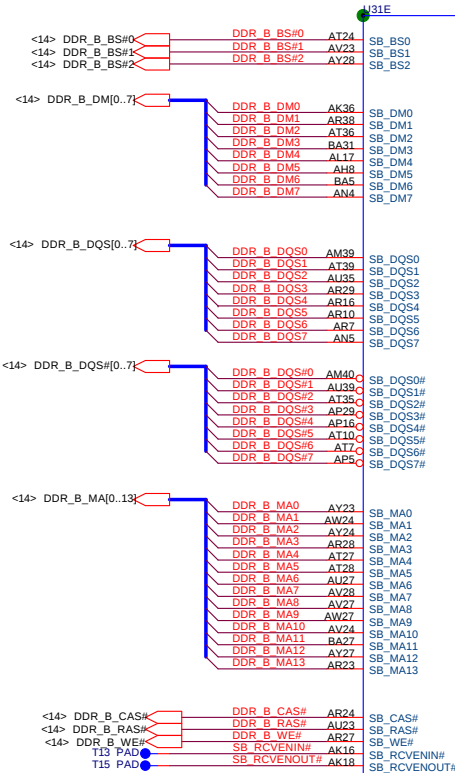
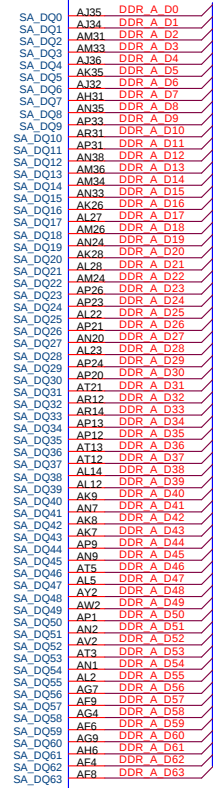


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				Customer	LA-3342P
Date: Thursday, July 27, 2006				Sheet	7 of 40
				Rev	0.1



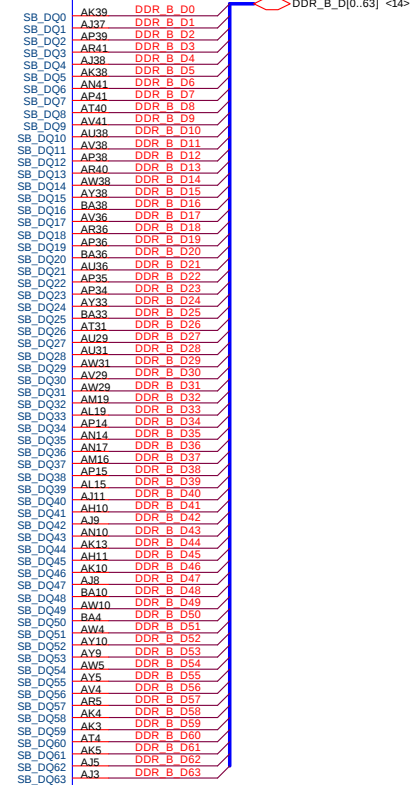
CALISTOGA_FCBGA1466-D

DDR SYS MEMORY A



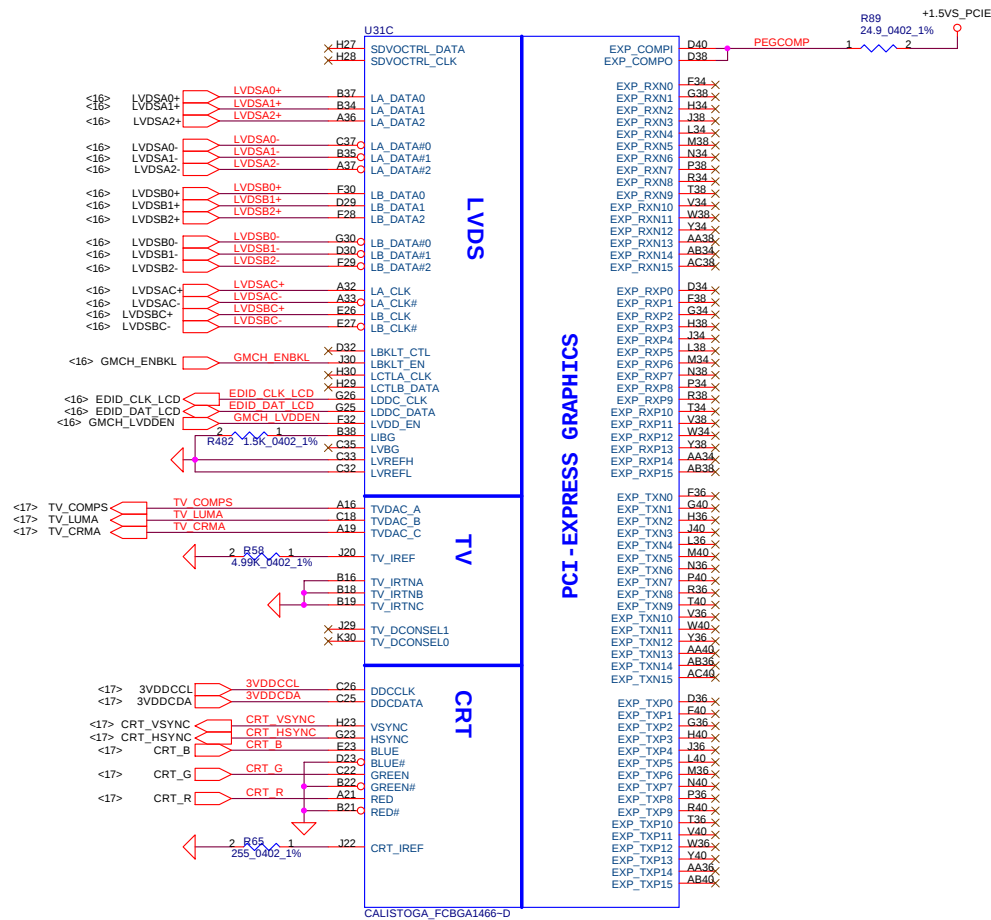
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DDR SYS MEMORY B

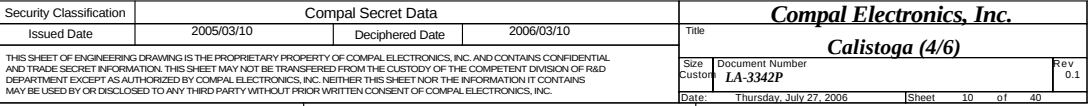


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				Custom	LA-3342P
				Date:	Thursday, July 27, 2006
				Sheet	8 of 40
				Rev	0.1

Calistoga (2/6)



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						Date:		Thursday, July 27, 2006		Sheet 9 of 40	



Strap Pin Table

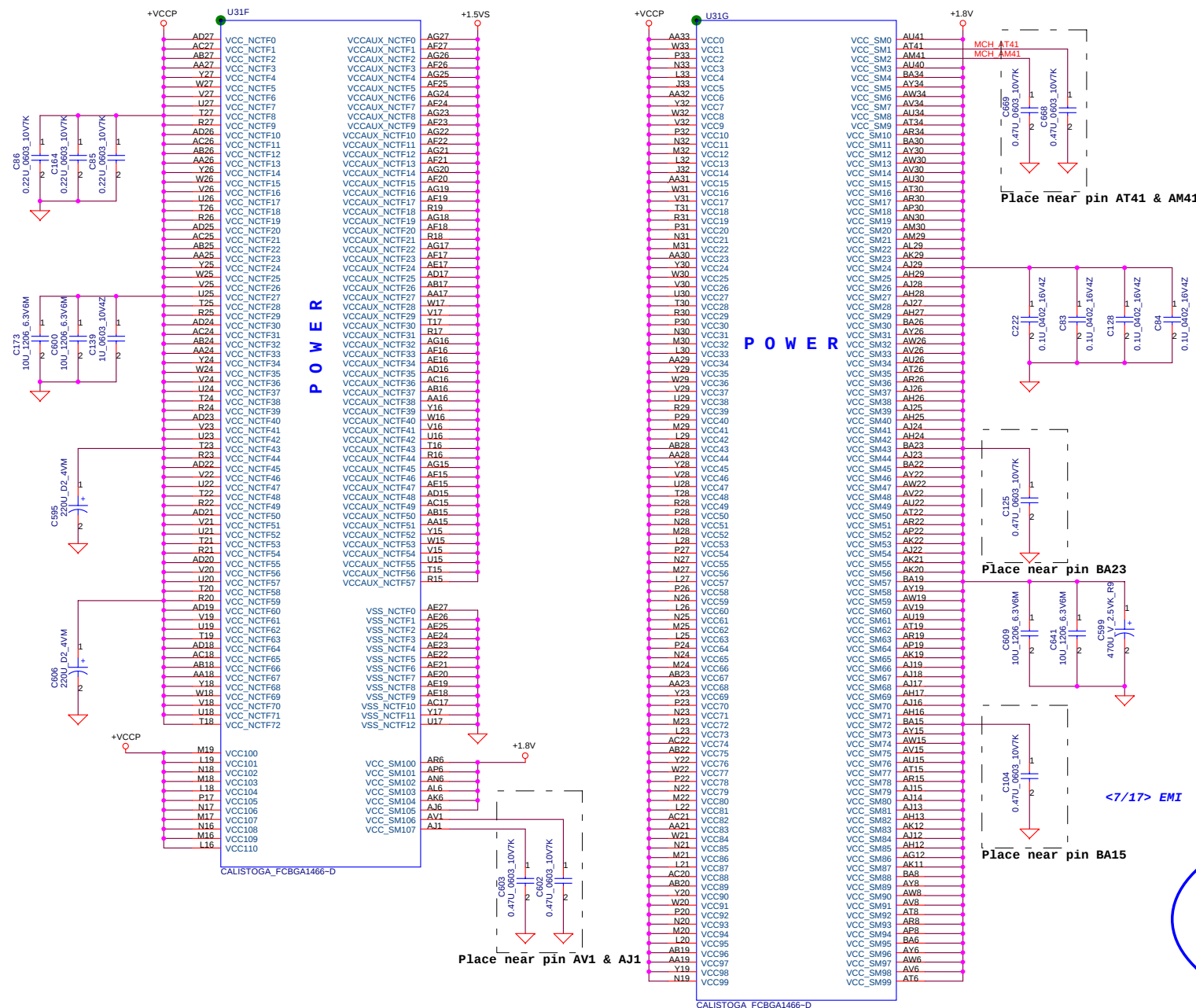
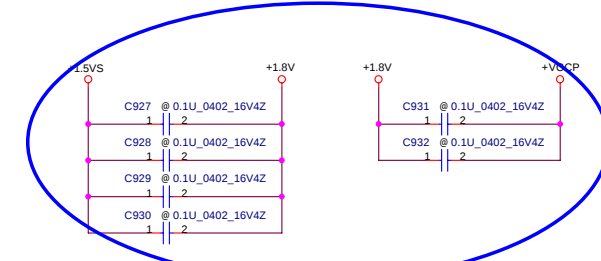
CFG[3:17] have internal pull up
CFG[19:18] have internal pull down

CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4*(Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU*(Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation (Default)*
CFG6	0 = Reserved
PSB 4X CLK Enable	1 = Calistoga *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation *(Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG10 CFG18	10 = 1.05V*(Default) 01 = 1.5V
CFG19	0 = No SDVO Device Present *(Default) 1 = DMI Lane Reversal Enable
SDVO_CTRLDATA	0 = No SDVO Device Present 1 = SDVO Device Present
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. *(Default) 1 = PCIE/SDVO are operating simu.

<7>	CFG5	R48	1	2	@ 2.2K 0402 5%
<7>	CFG7	R54	1	2	@ 2.2K 0402 5%
<7>	CFG9	R51	1	2	@ 2.2K 0402 5%
<7>	CFG11	R47	1	2	@ 2.2K 0402 5%
<7>	CFG12	R49	1	2	@ 2.2K 0402 5%
<7>	CFG13	R50	1	2	@ 2.2K 0402 5%
<7>	CFG16	R53	1	2	@ 2.2K 0402 5%

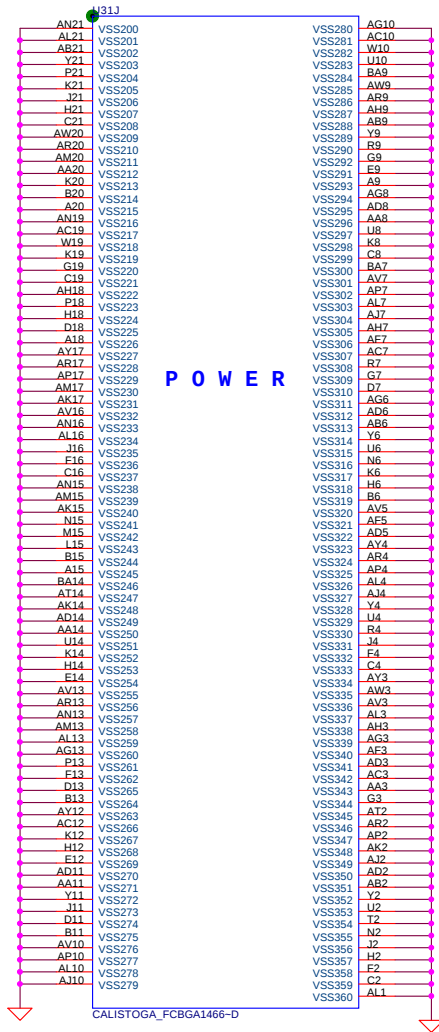
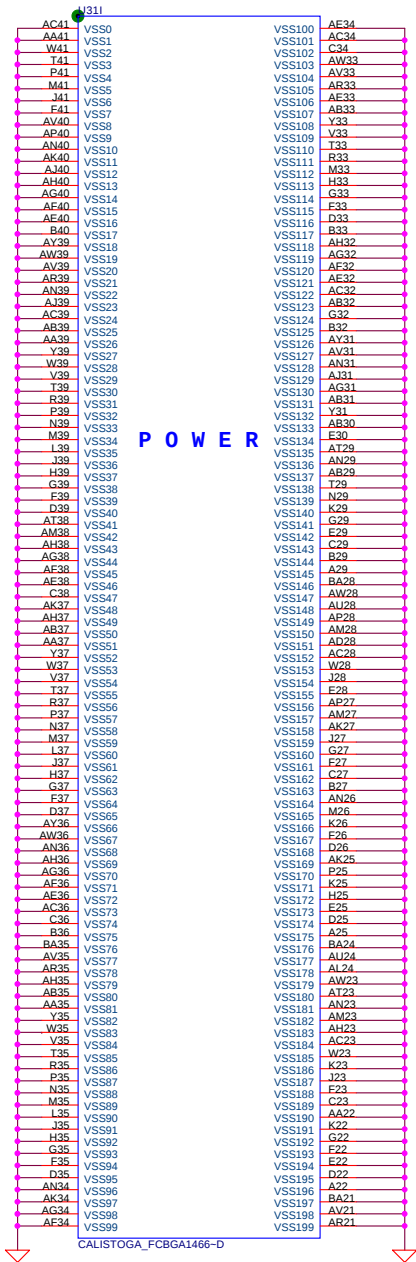
<7>	CFG18	R74	1	2	@ 1K 0402 5%
<7>	CFG19	R82	1	2	@ 1K 0402 5%
<7>	CFG20	R87	1	2	@ 1K 0402 5%

<7/17> EMI issue, add new parts C927,C928,C929,C930, C931,C932

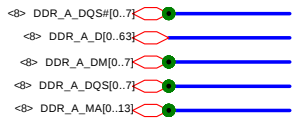


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				Date	Thursday, July 27, 2006
				Sheet	11 of 40
				Rev	1.0

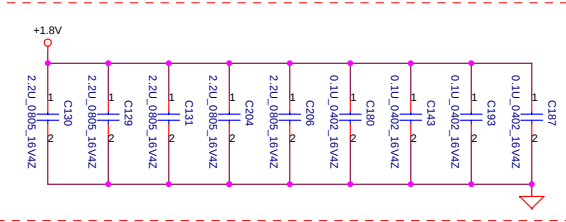
Calistoga (5/6)



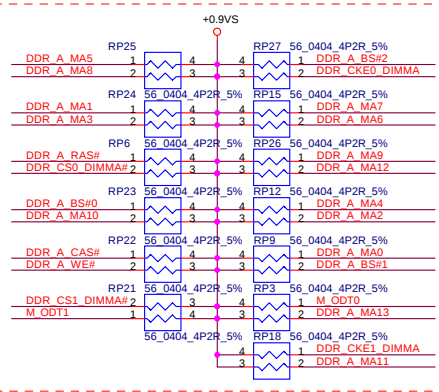
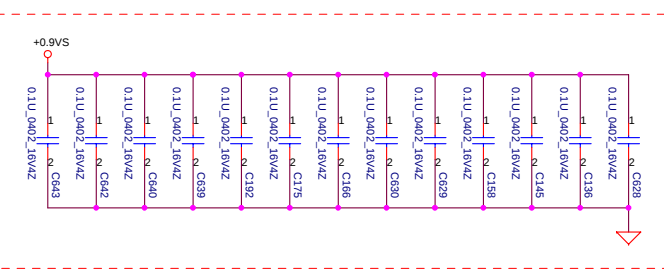
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				Date: Thursday, July 27, 2006	Rev 0.1
				Sheet 12	of 40



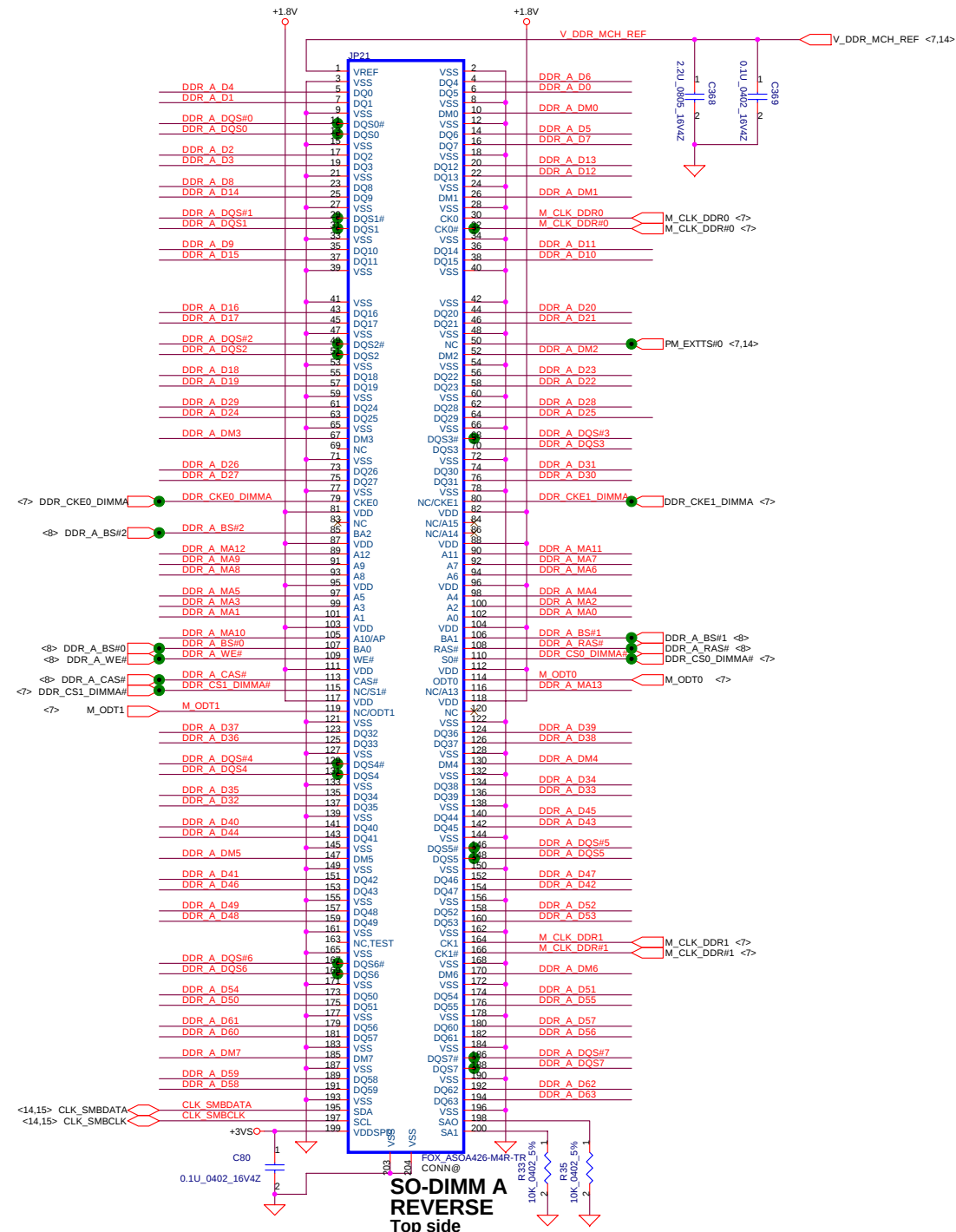
Layout Note:
Place near JP41



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



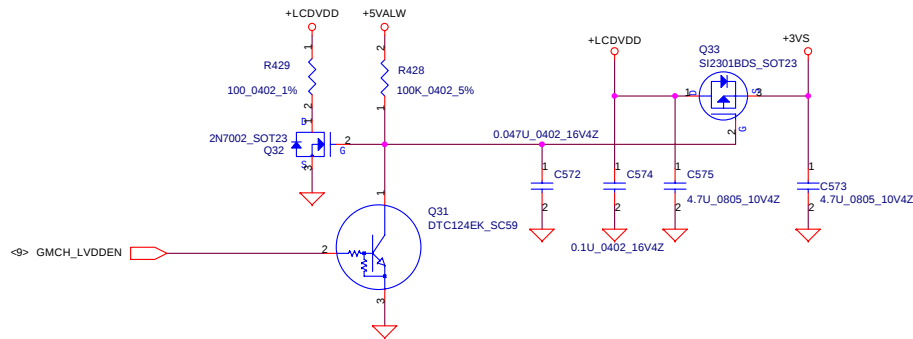
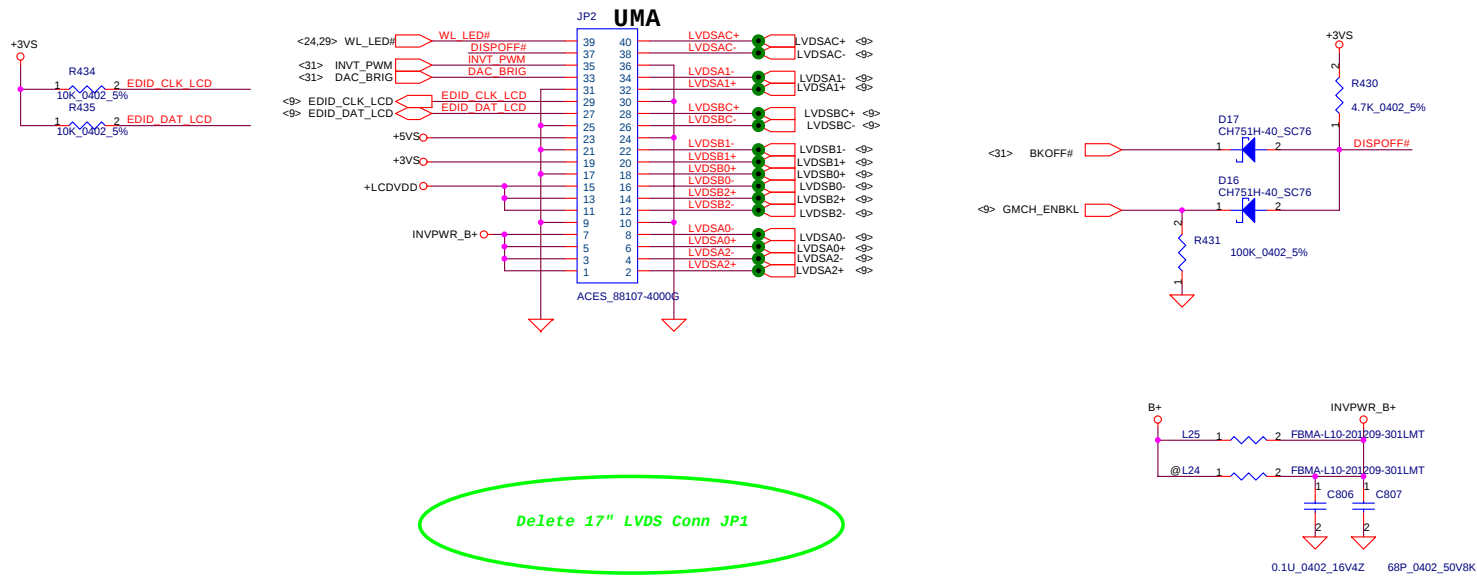
Layout Note:
Place these resistor closely JP41,all trace length Max=1.5"



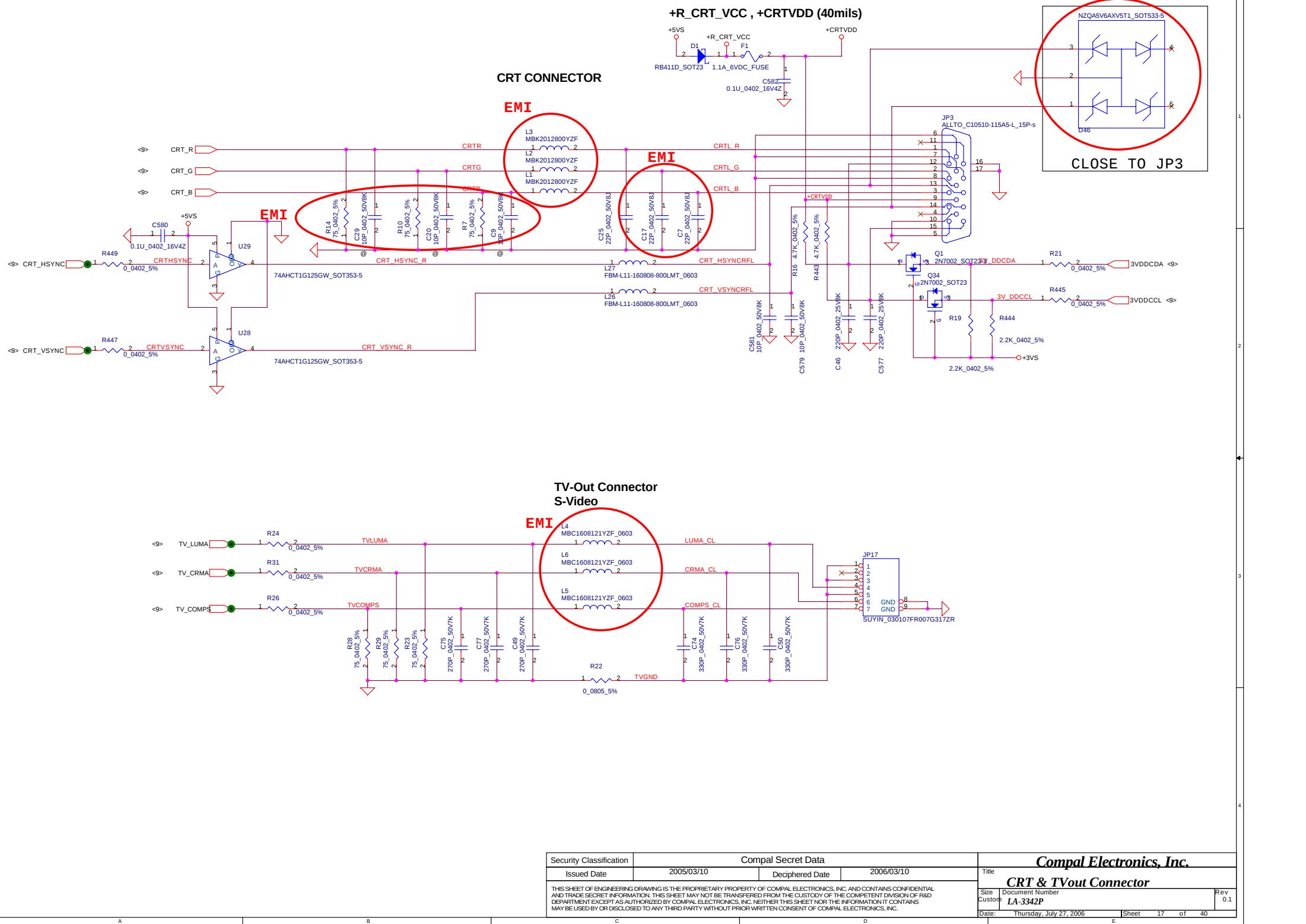
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Date:				Thursday, July 27, 2006				Sheet 13 of 40			
Size				Document Number				Rev			
LA-3342P				0.1				0.1			

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					LA-3342P
				Rev	0.1
Date:		Thursday, July 27, 2006		Sheet	14 of 40

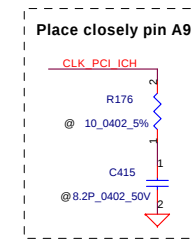
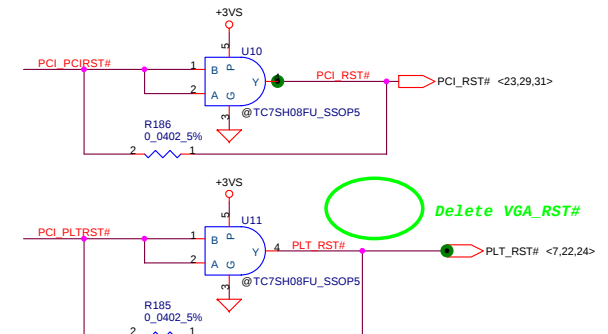
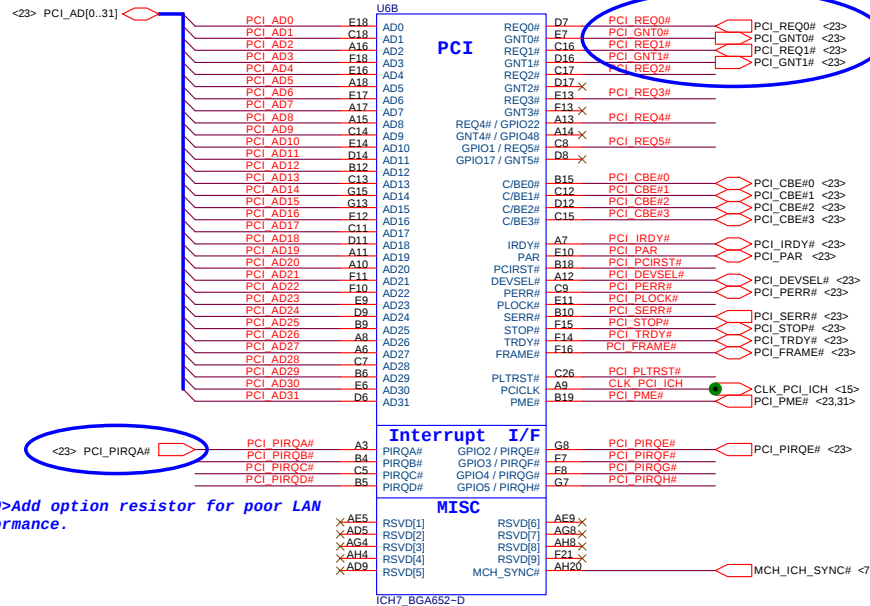
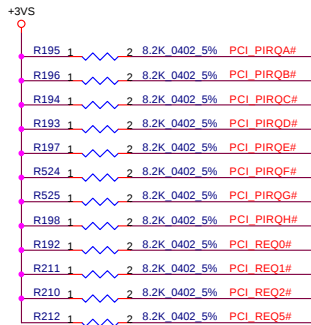
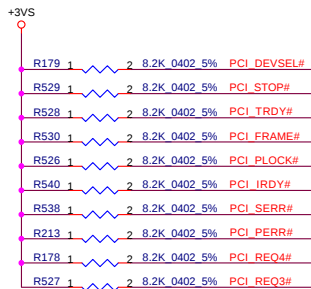
LCD Panel & inverter Connector



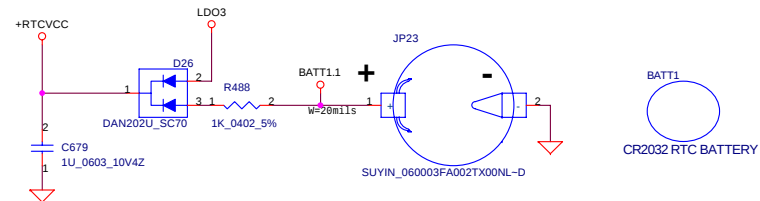
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				Custom	LA-3342P
				Date	Thursday, July 27, 2006
				Sheet	16 of 40
				Rev	0.1



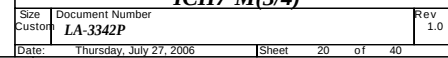
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Date:		Thursday, July 27, 2006		Sheet	17 of 40

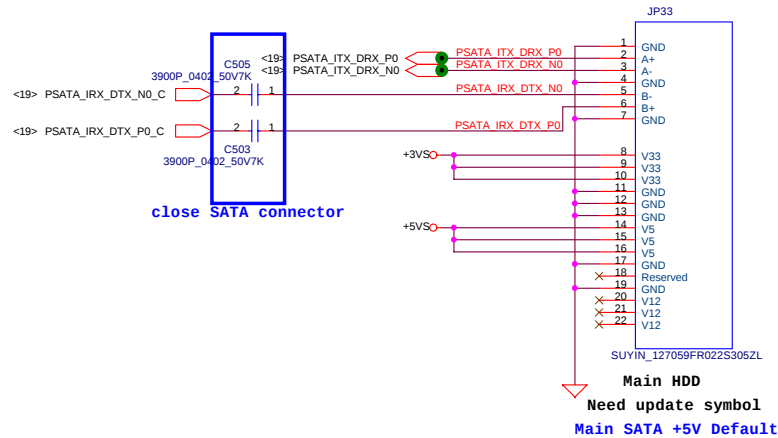
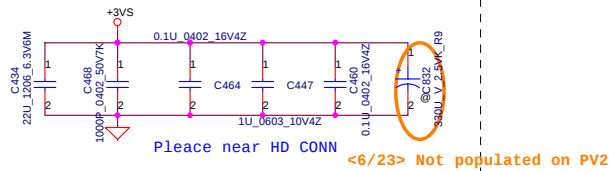
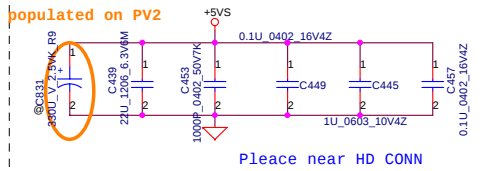


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				Date:	Thursday, July 27, 2006
				Sheet	18 of 40
				Rev	0.1

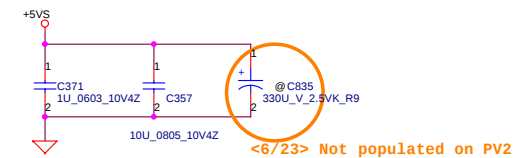
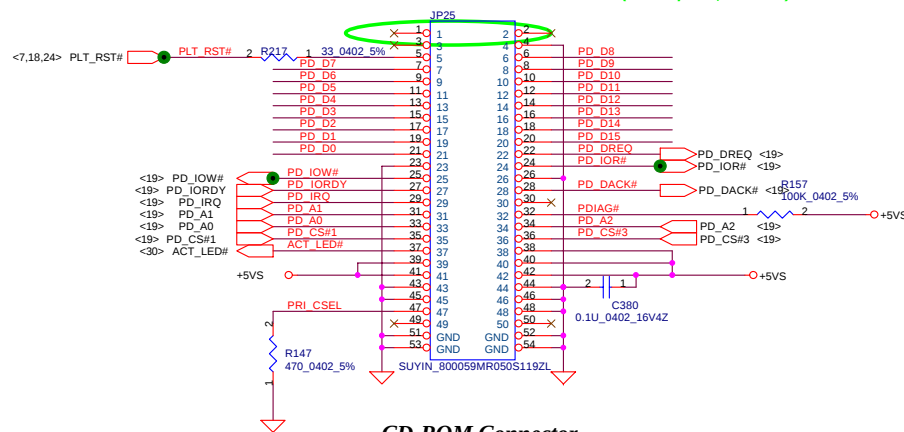


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Size	Document Number	Rev	
Custom	LA-3342P	0.1	
Date:	Thursday, July 27, 2006	Sheet	19 of 40



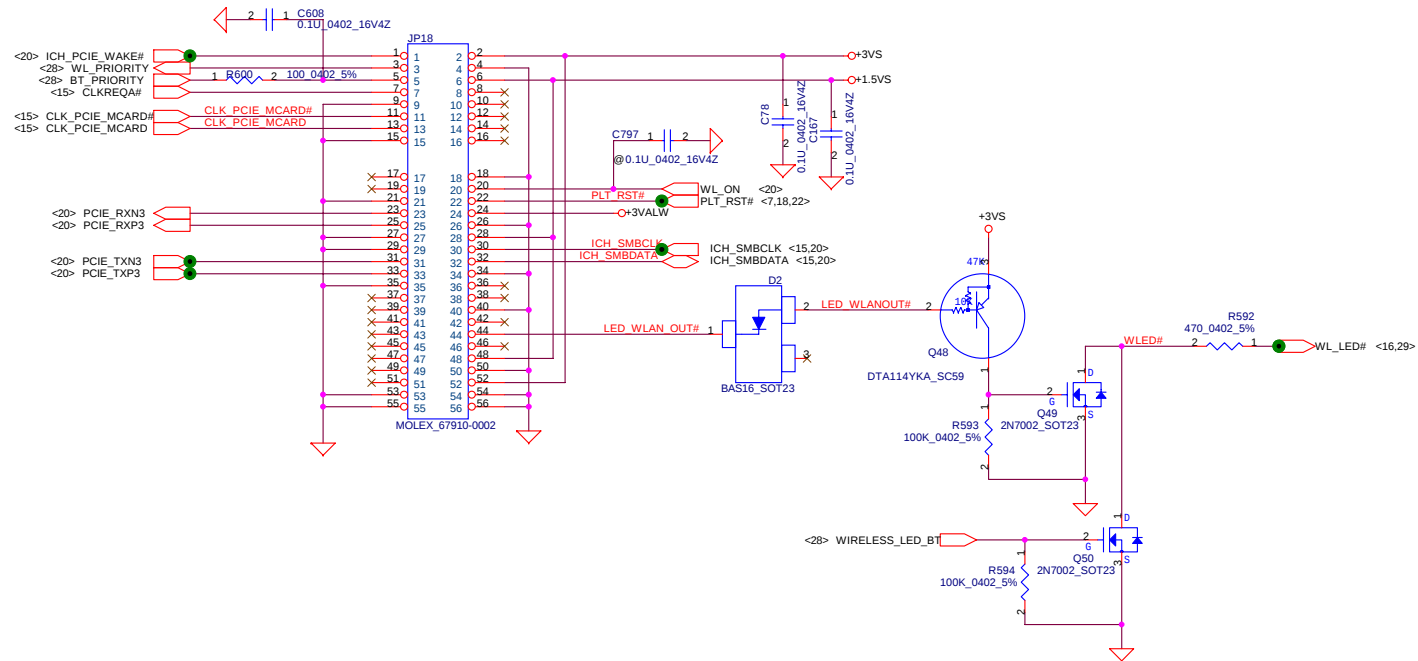


Delete CD traces (JP25 pin1,2 and3)



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				Cust	LA-3342P	0.1
				Date:	Thursday, July 27, 2006	Sheet 22 of 40

Mini-Express Card(Slot 1-WLAN)



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				Custom	LA-3342P
				Date	Thursday, July 27, 2006
				Sheet	24 of 40
				Rev	0.1

<6/12> Remove PCM_SPK

For Layout:

Place decoupling caps near the power pins of SmartAMC device.

Delete CD traces

<6/12> Remove Docking line out

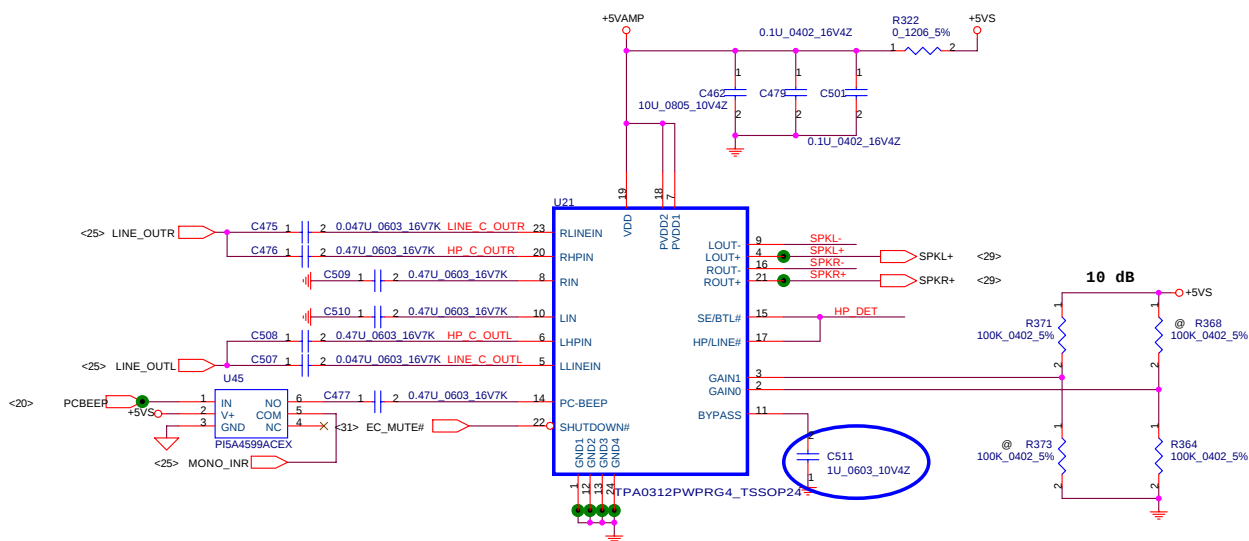
<6/12> Remove Docking MIC

<6/12> Remove JACK_DET from Docking

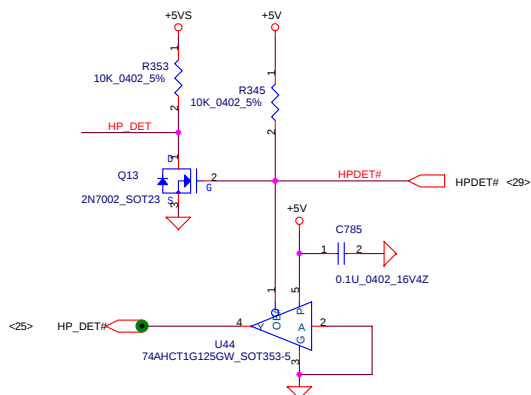
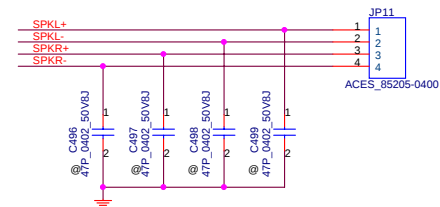
HP_DET#	JACK_DET#	PORT-A	PORT-B	EQ
0	0	ON	OFF	Disable
0	NC	ON	OFF	Disable
NC	0	OFF	ON	Disable
NC	NC	ON	OFF	Enable

MIC_DET	PORT-C	PORT-F
0	ON	OFF
NC	OFF	ON

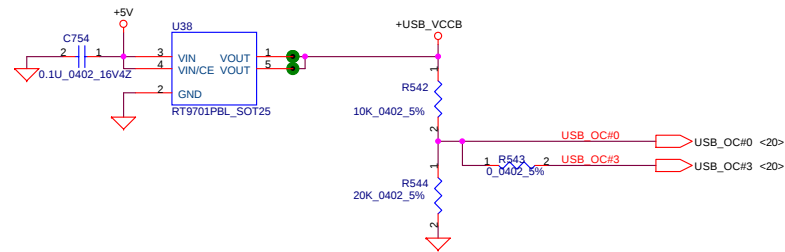
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				Custom	LA-3342P
				Date	Thursday, July 27, 2006
				Sheet	25 of 40
				Rev	0.1



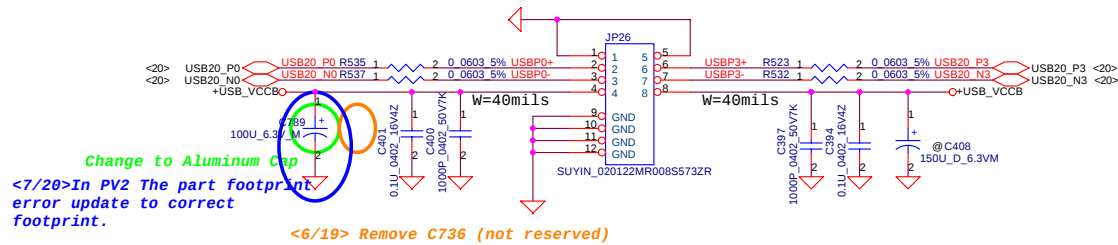
Gain Settings			
GAIN0	GAIN1	SE/BTL#	Av(inv)
0	0	0	6 dB
0	1	0	* 10 dB
1	0	0	15.6 dB
1	1	0	21.6 dB
X	X	1	4.1 dB



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Issued Date	2005/03/10	Deciphered Date	2006/03/10	AMP & Audio Jack	
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				Date	Thursday, July 27, 2006
				Sheet	27 of 40
				Rev	0.1

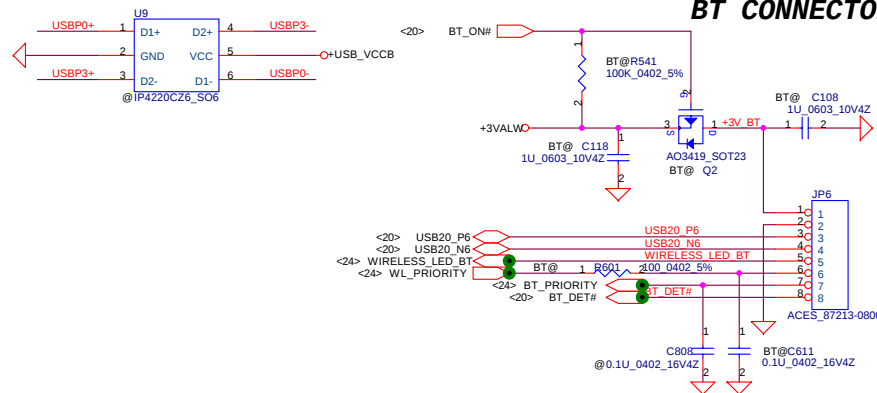


USB CONNECTOR (Left side)



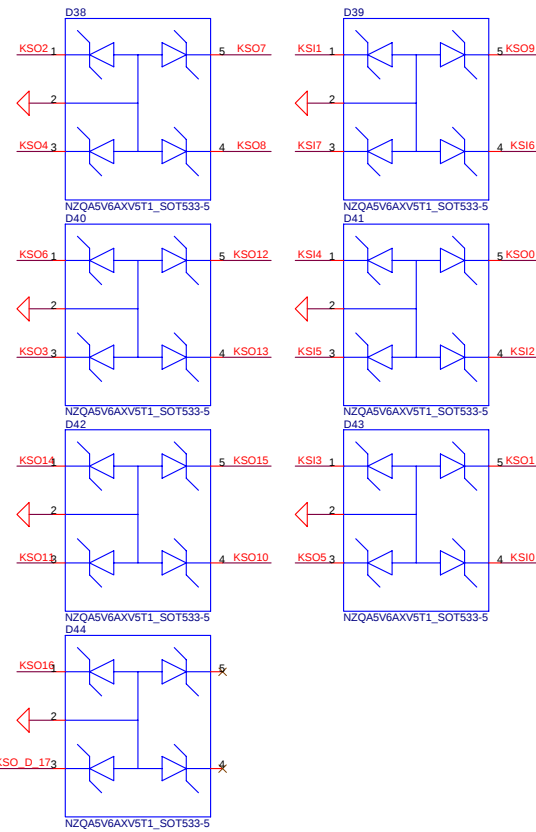
BT CONNECTOR

Reserve Bluetooth

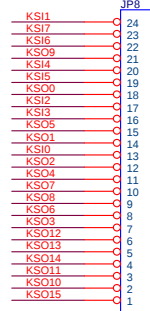


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Issued Date	2005/03/10	Deciphered Date	2006/03/10	Title	Bluetooth & USB CONN.
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				Custom	1.0
				Date:	Thursday, July 27, 2006
				Sheet	28 of 40

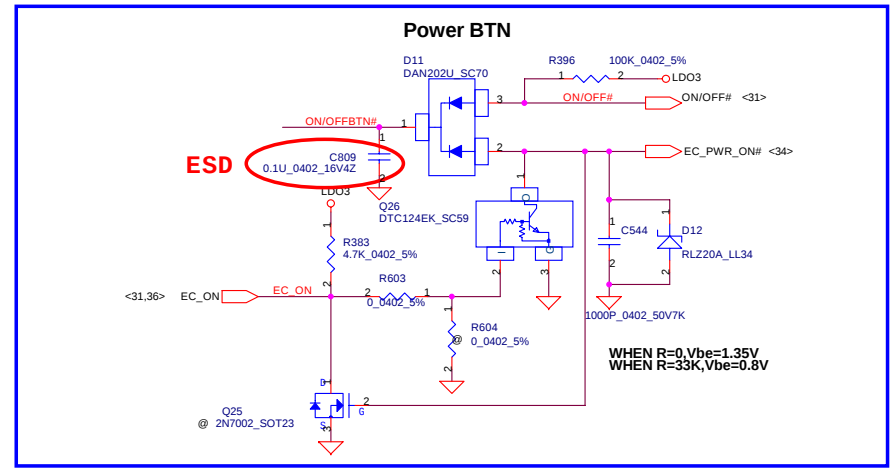
KSI[0..7] <31>
KSO[0..16] <31>



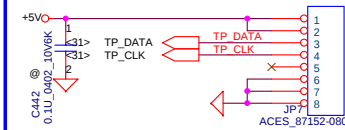
15.4 (TYPE "C" KB)



ACES_85201-2405

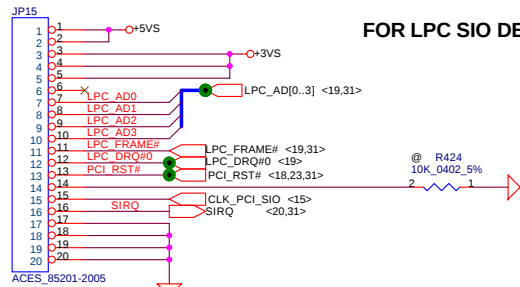


TP to MB CONN(15.4)

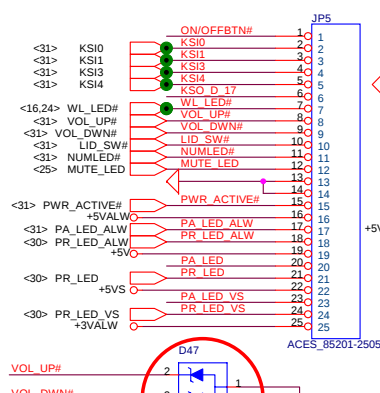


<6/21> Remove CIR

FOR LPC SIO DEBUG PORT

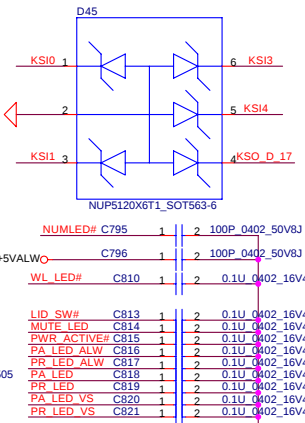


Switch board conn

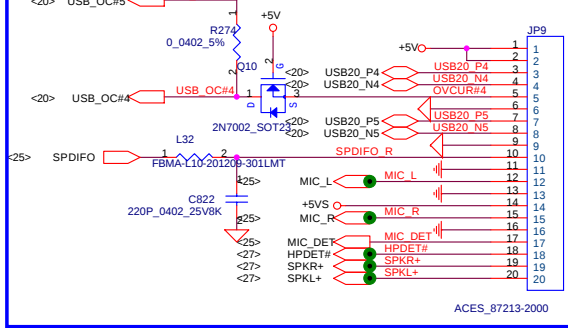


ESD

ACES_85201-2505



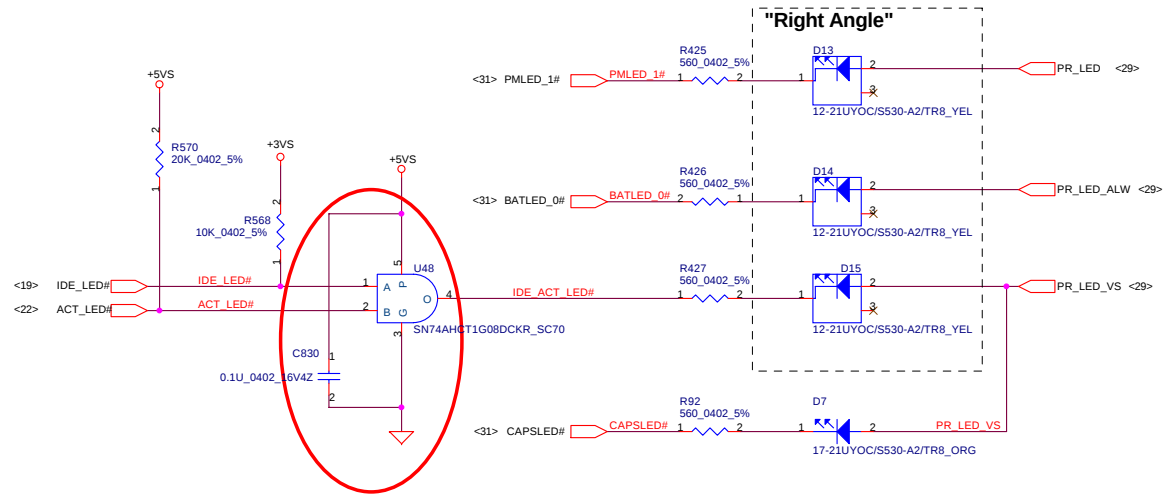
Audio board conn



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				Date	Thursday, July 27, 2006
				Sheet	29 of 40

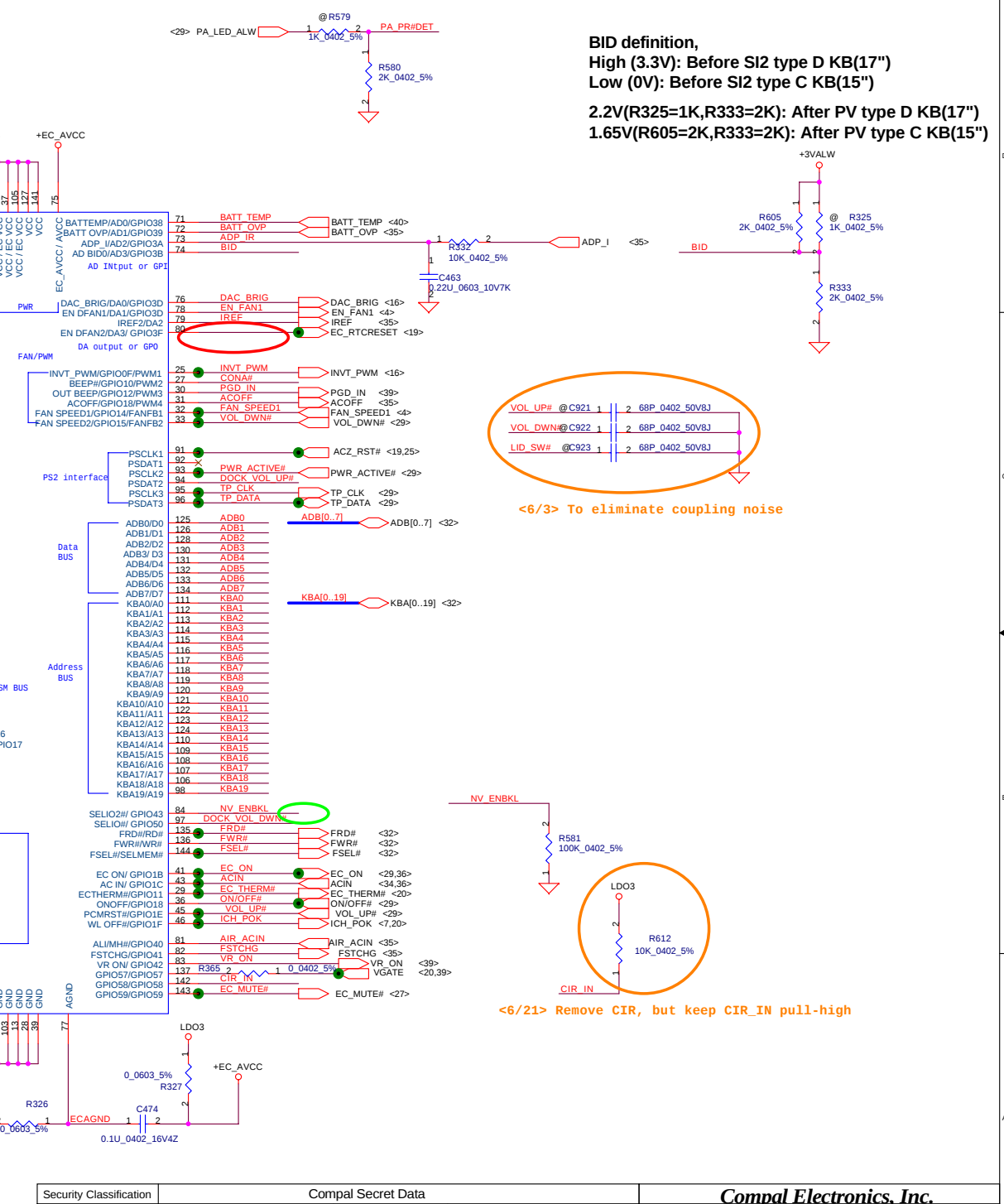
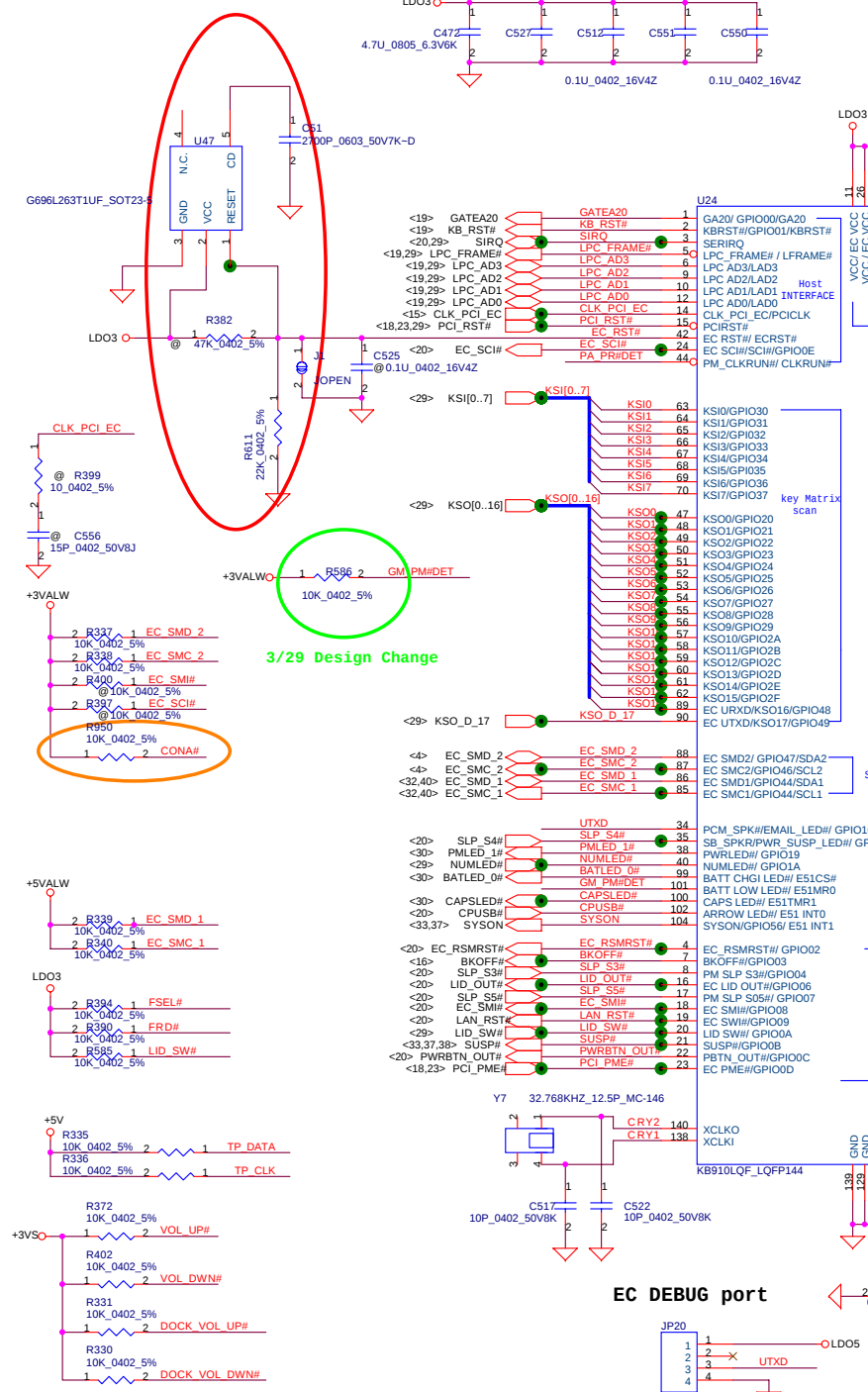
For PR

FOR POWER BUTTON BACKLIGHT SYSTEM POWER



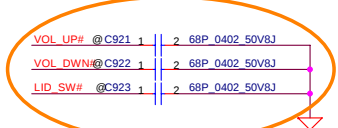
Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		INDICATE LED	
2005/03/10		2006/03/10		Size	
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		LA-3342P		0.1	
Date:		Thursday, July 27, 2006		Sheet 30 of 40	

Cd(uF)=T(ms) / 1685
Cd=2700PF -----> T=3.6ms

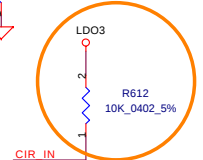


BID definition,
High (3.3V): Before SI2 type D KB(17")
Low (0V): Before SI2 type C KB(15")

2.2V(R325=1K,R333=2K): After PV type D KB(17")
1.65V(R605=2K,R333=2K): After PV type C KB(15")



<6/3> To eliminate coupling noise

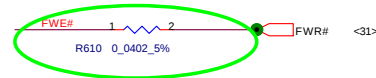
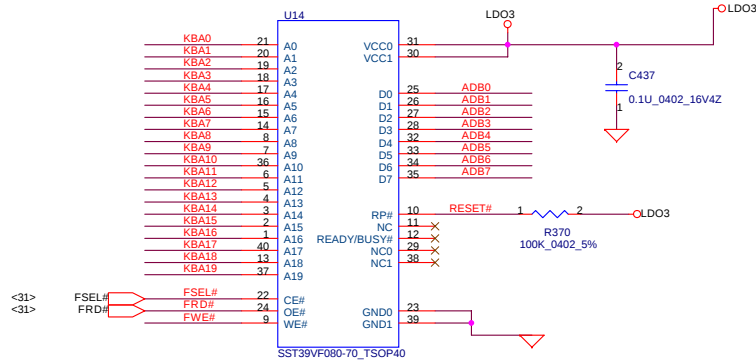
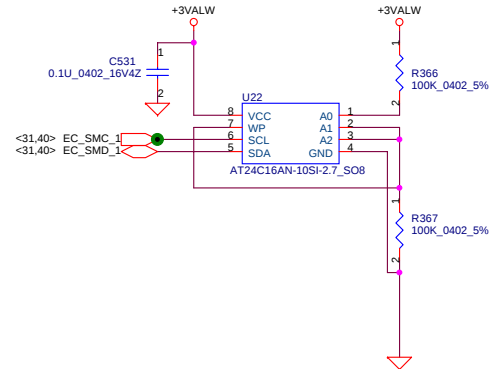
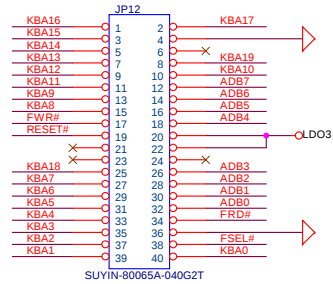


<6/21> Remove CIR, but keep CIR_IN pull-high

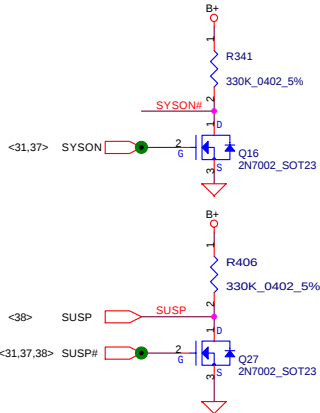
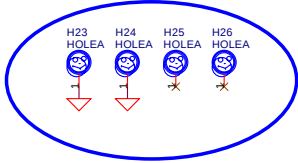
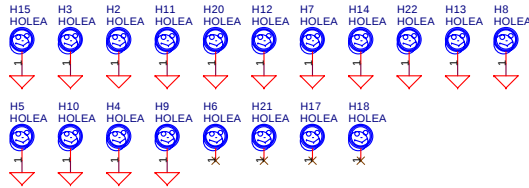
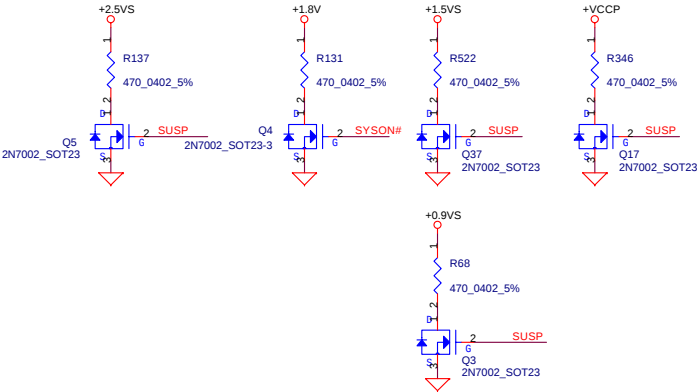
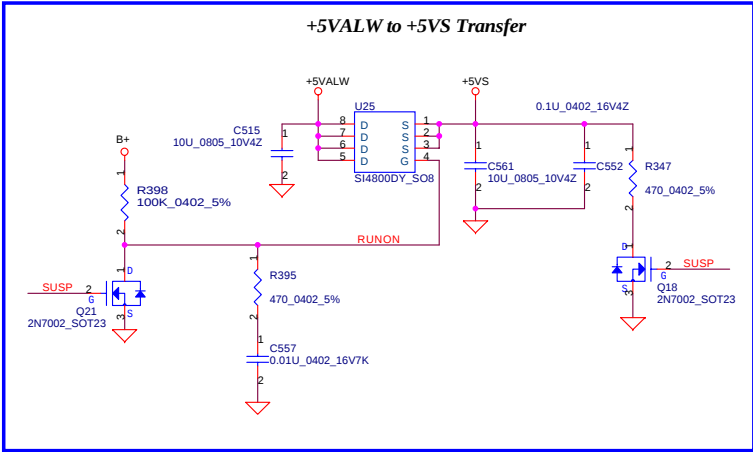
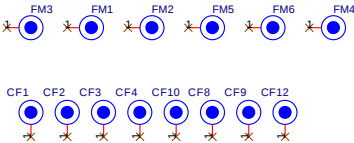
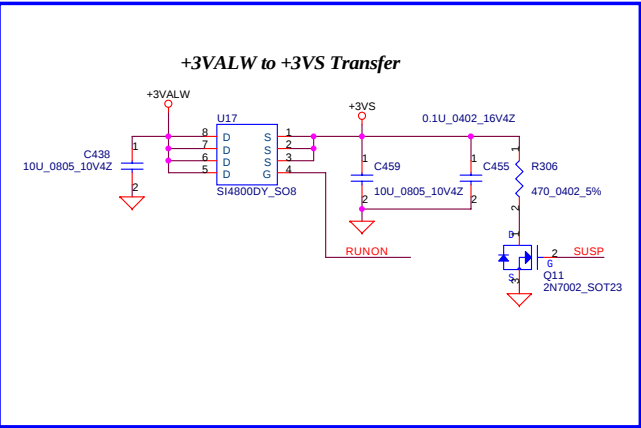
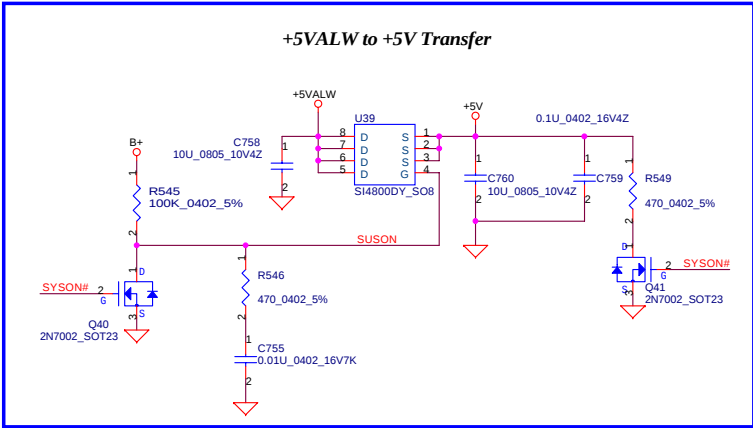
EC DEBUG port

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				Date	Thursday, July 27, 2006
				Sheet	31 of 40

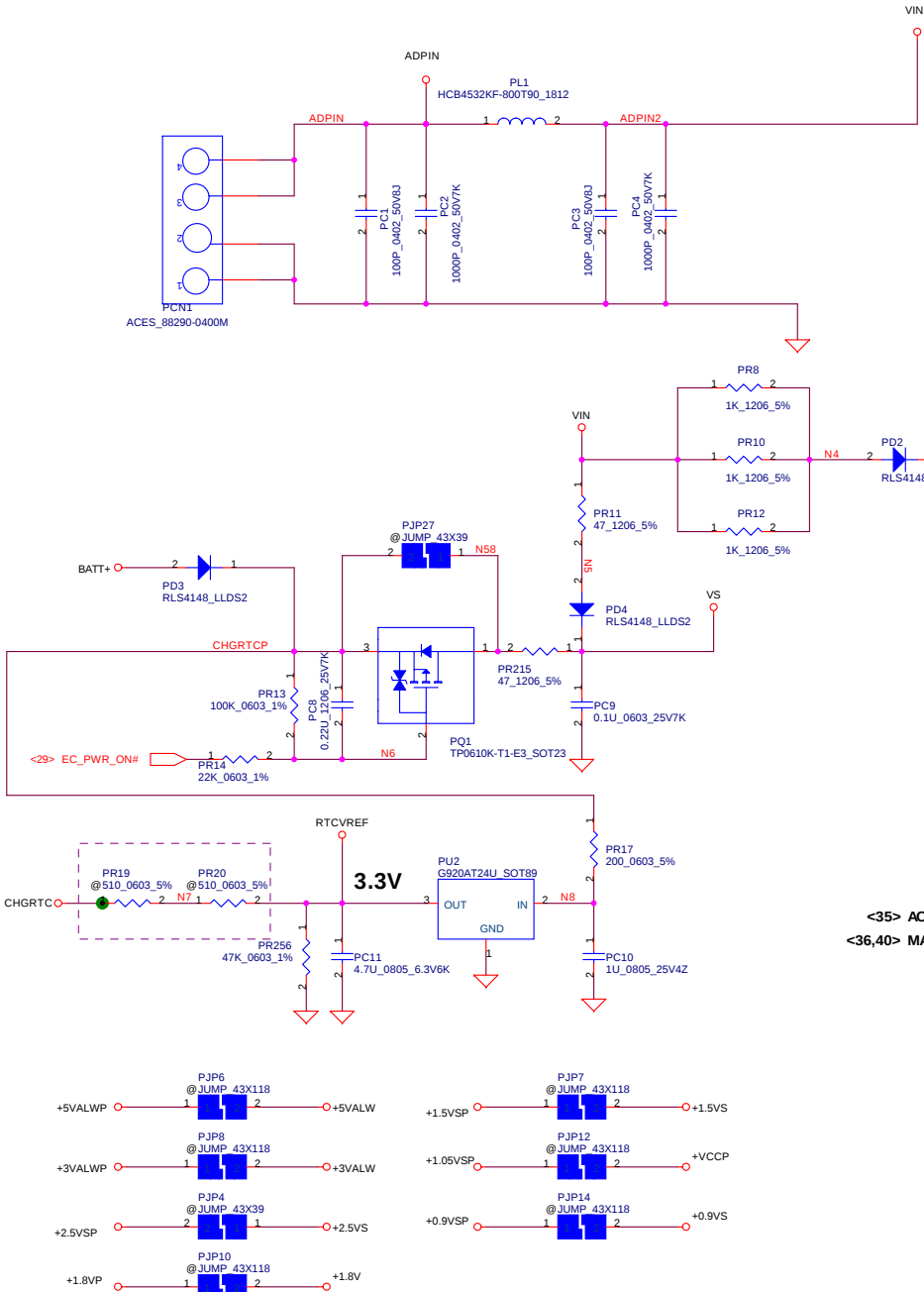
<31> ADB[0..7] ADB[0..7]
<31> KBA[0..19] KBA[0..19]



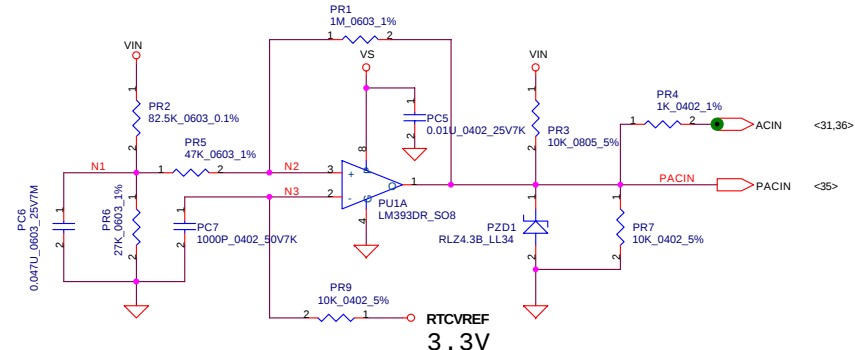
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2005/03/10				2006/03/10				Title			
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								0.1			
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								Thursday, July 27, 2006			
								Sheet			
								32 of 40			



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				Date:	Thursday, July 27, 2006
				Sheet	33 of 40
				Rev	0.1

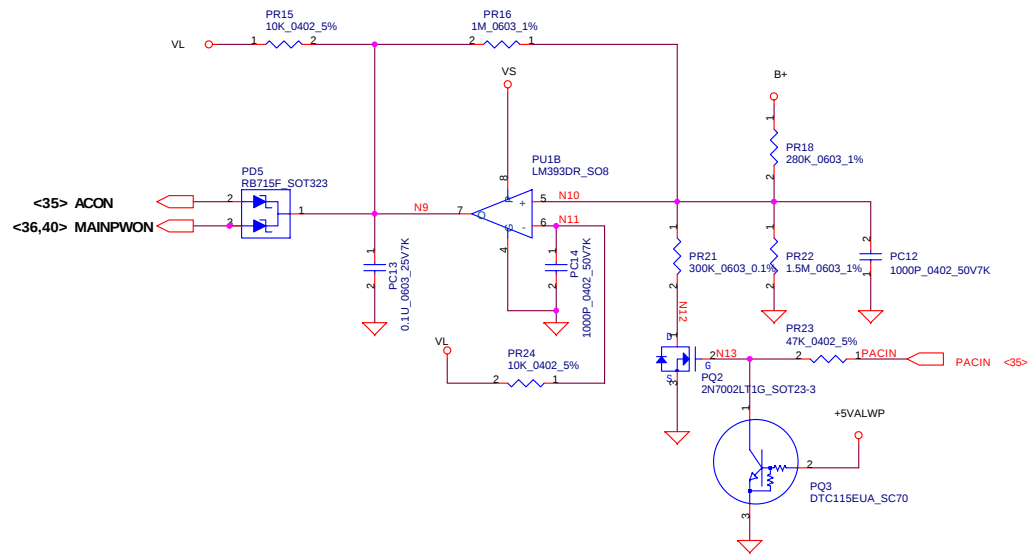


Vin Detector :			
14.698	14.285	13.879	
13.818	13.411	13.000	



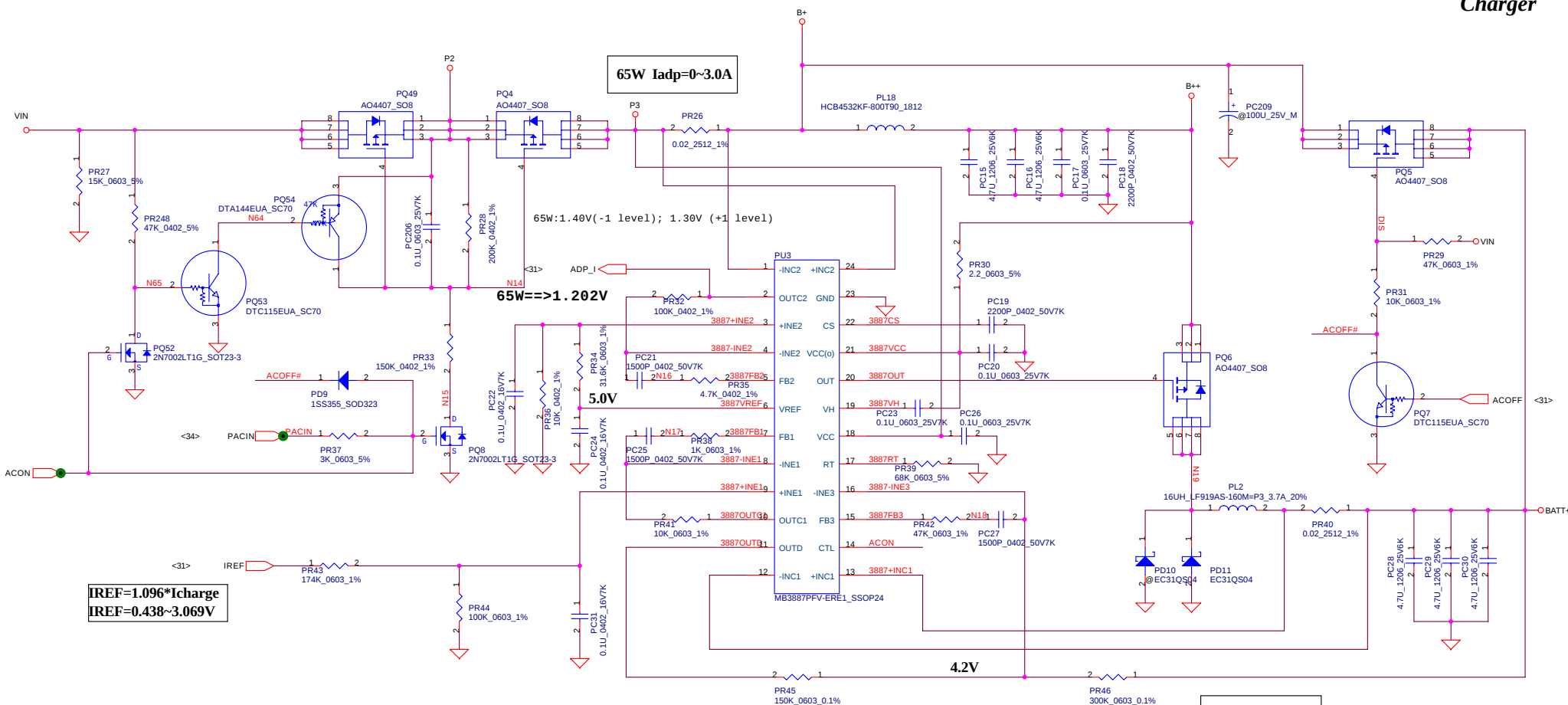
ACIN:			
Precharge detector			
12.384	12.000	11.624	
10.927	10.600	10.223	

BATT			
Precharge detector			
7.558	7.333	7.112	
6.108	5.933	5.704	

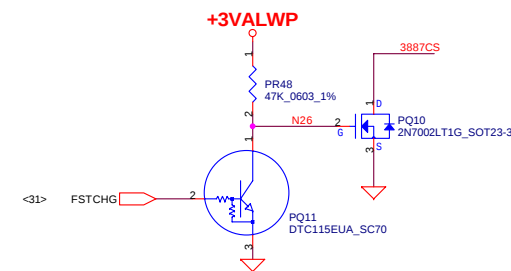
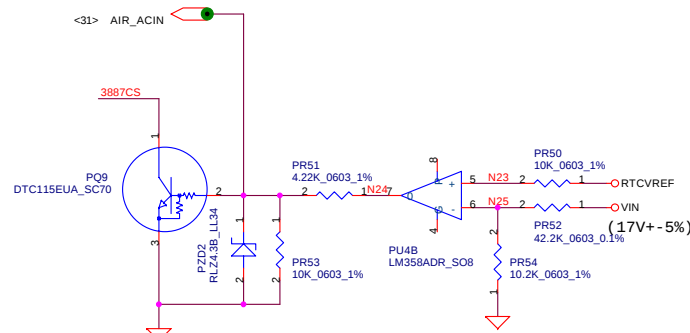
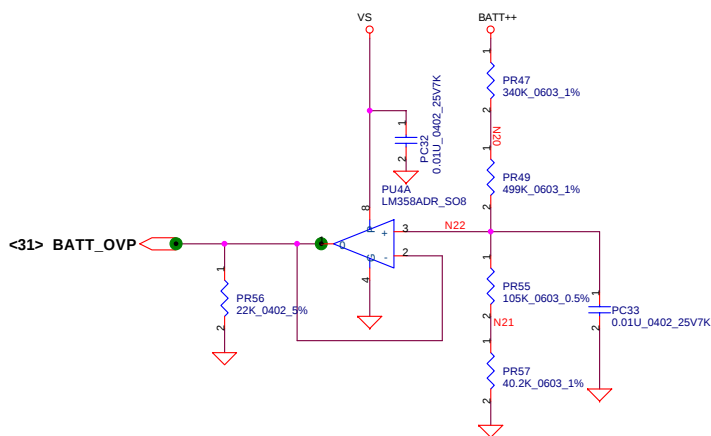


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						Customer				0.2	
						Date:		Thursday, July 27, 2006		Sheet 34 of 40	

Charger

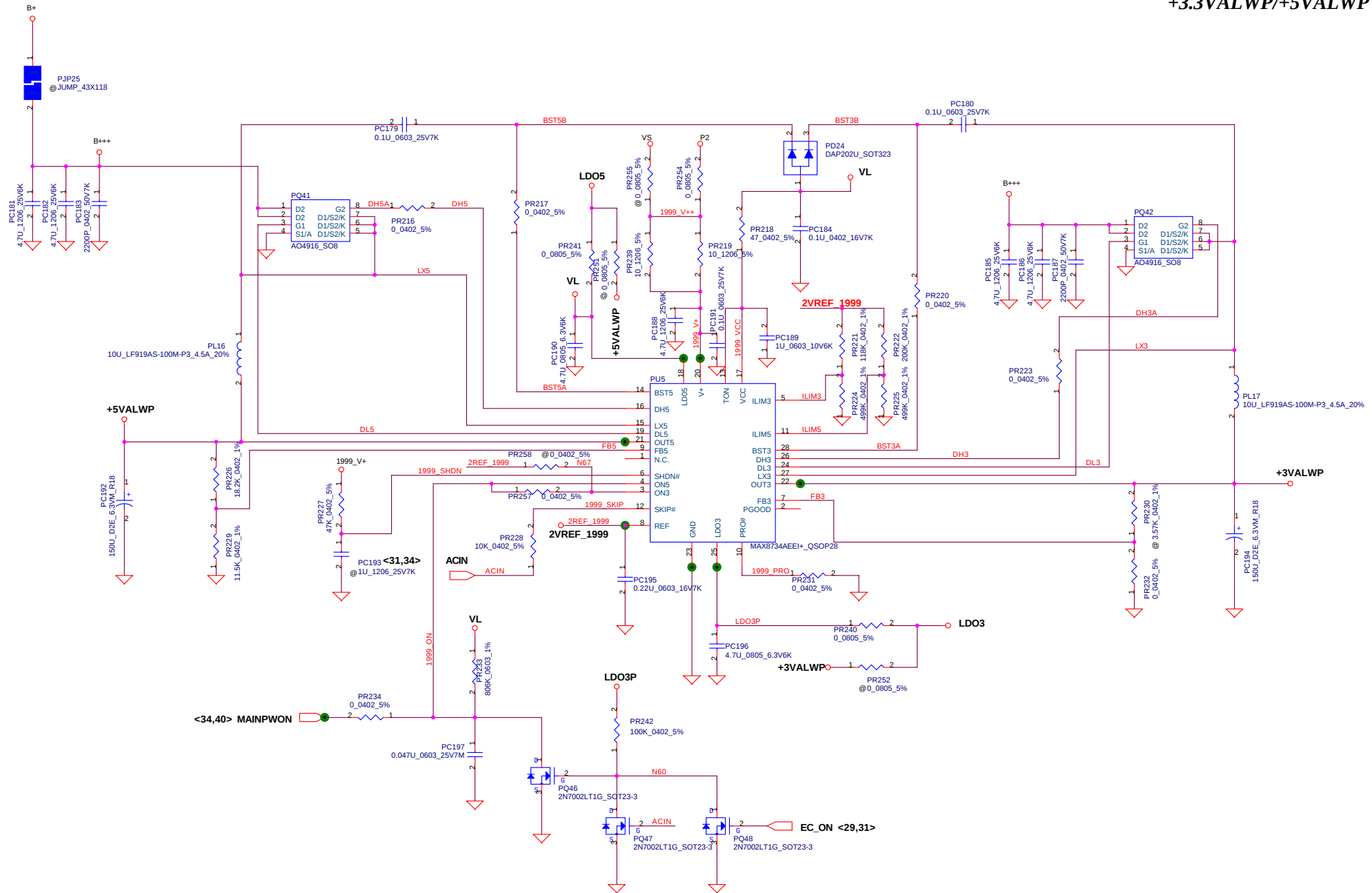


3S2P/3S4P : 13.5V--> BATT_OVP= 2.0V
(BAT_OVP=0.14753 *BATT+)



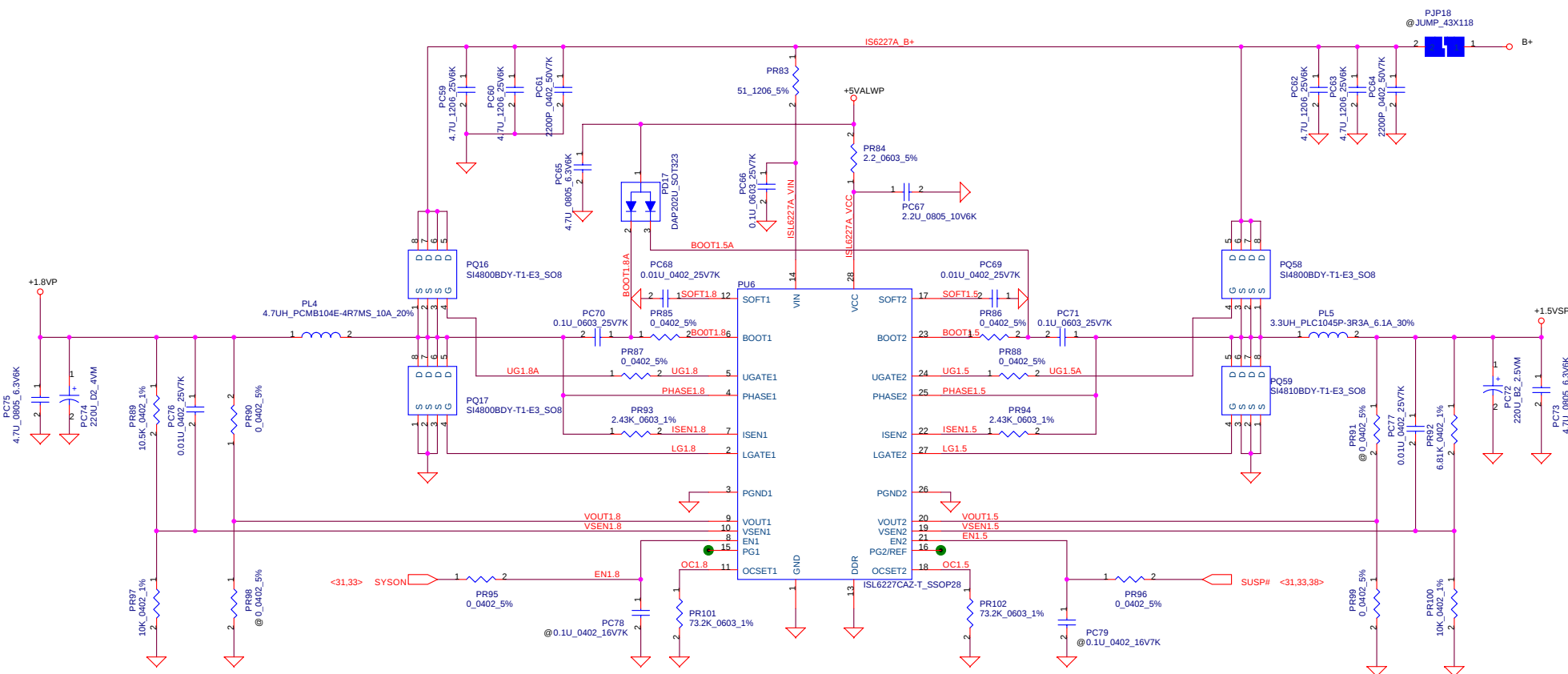
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				Custom	
				Date:	Thursday, July 27, 2006
				Sheet	35 of 40

+3.3VALWP/+5VALWP

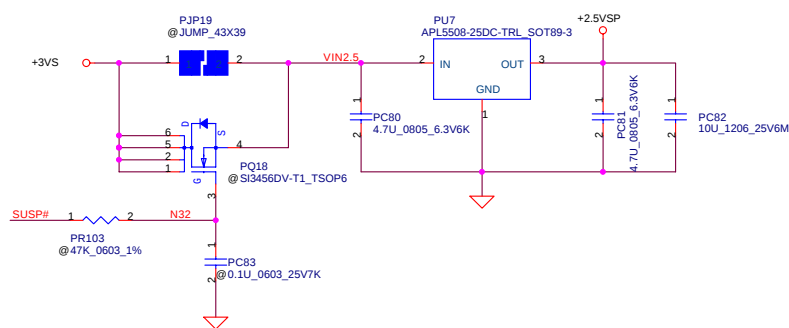


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Issued Date	2006/04/03	Deciphered Date	2007/04/03	Title +3VALWP/+5VALWP		
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				Custm		
				Date:	Thursday, July 27, 2006	Sheet 36 of 40

+2.5VSP/+1.8VP/+1.5VSP

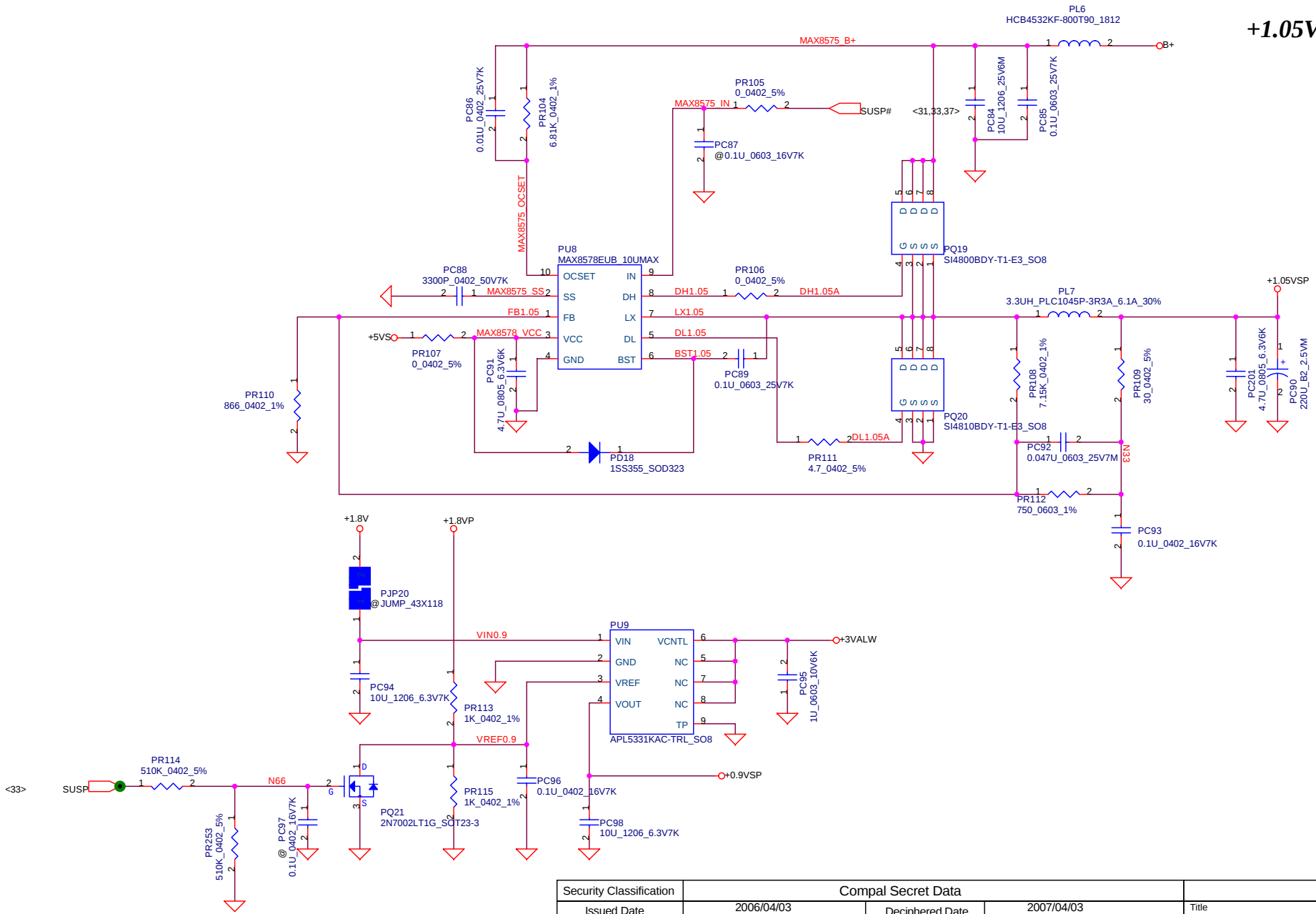


(400mA, 40mils, Via NO.= 1)

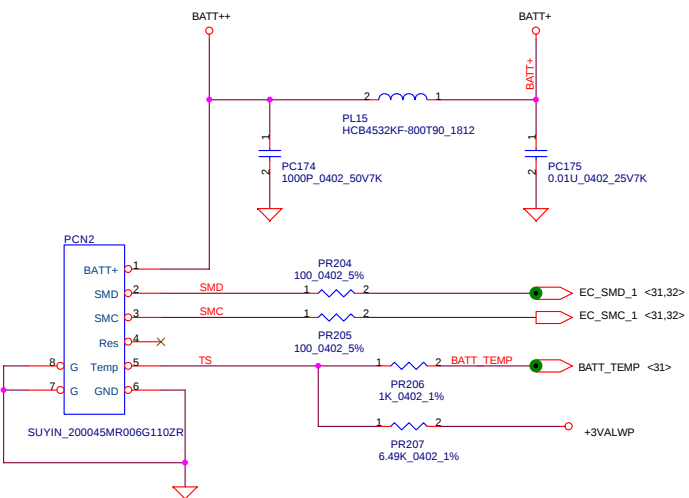


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						+2. 5VSP/+1. 8VP/+1. 5VSP
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Size		Document Number				Rev
Custom						
Date:		Thursday, July 27, 2006		Sheet 37 of 40		

+1.05V_VCCPP/+0.9VSP

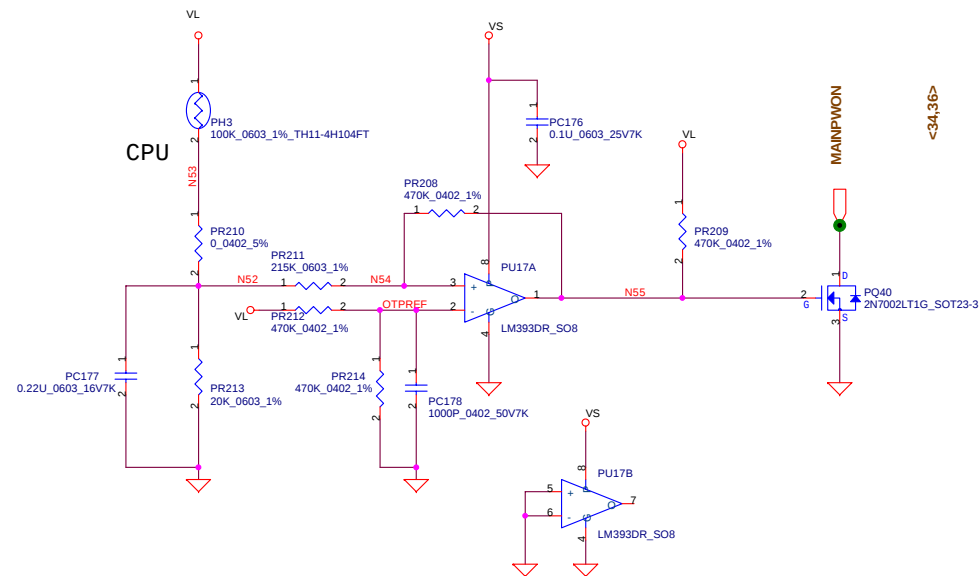


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Size	Document Number			Rev	
Date:	Thursday, July 27, 2006			Sheet	38 of 40



PJPB1 battery connector
SMART
Battery:
1.BATT+
2.SMBD
3.SMBC
4.Res
5.Temp
6.GND

PH1 under CPU botten side :
CPU thermal protection at 90 +-3 degree C
Recovery at 50 +-3 degree C



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					Size	Document Number	Rev
					Custom	Information	
Date:		Thursday, July 27, 2006		Sheet	40 of 40		