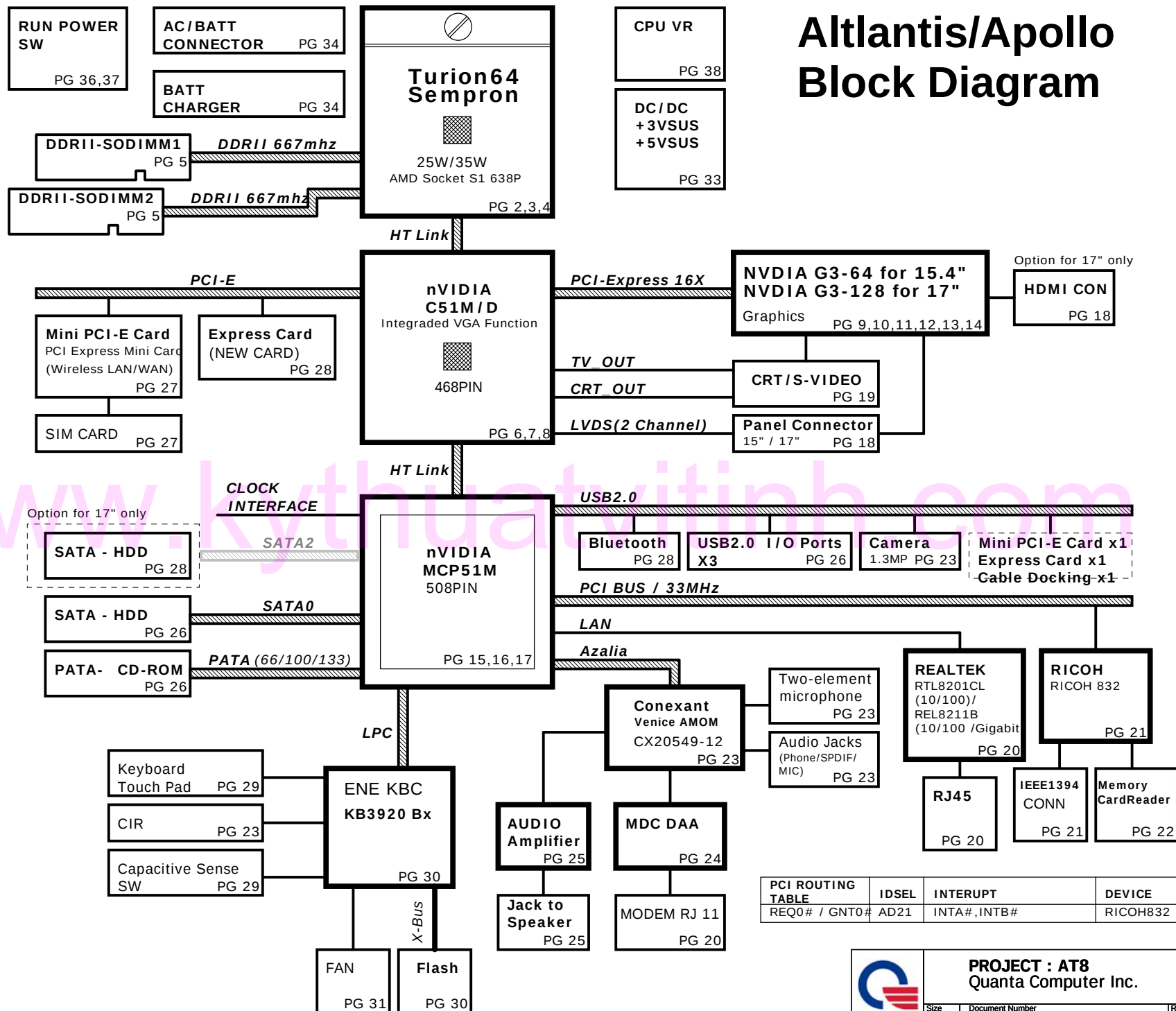
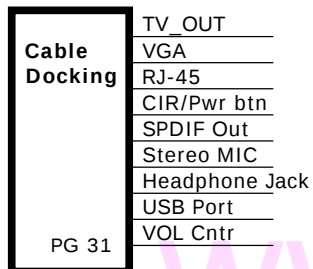


PCB STACK UP

LAYER 1 : TOP
LAYER 2 : SGND1
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : IN3
LAYER 7 : SGND2
LAYER 8 : BOT



VAULE DEFINE
A=0603,B=0805,C=1206,F=1%,
OTHER IS 0402

EXAMPLE
10R=10ohm(0402)
10A=10ohm(0603)
10B=10ohm(0805)
10C=10ohm(1206)
10/F=10ohm(0402 and 1%)

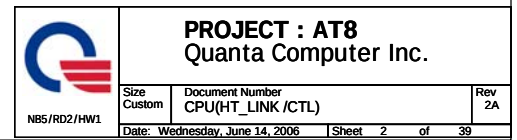
Atlantis/Apollo Block Diagram

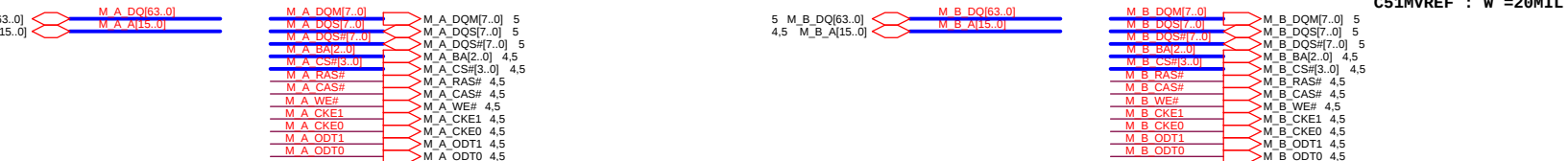
PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD21	INTA#,INTB#	RICOH832

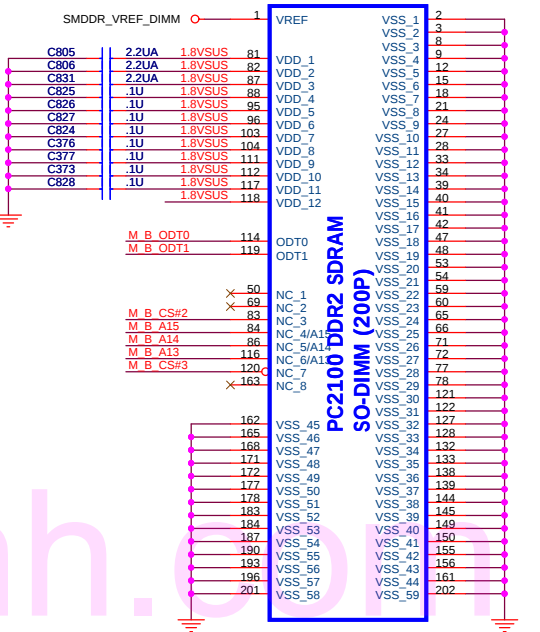


PROJECT : AT8
Quanta Computer Inc.

Size Custom	Document Number Block Diagram	Rev 1A
Date: Wednesday, June 14, 2006	Sheet 1 of 39	







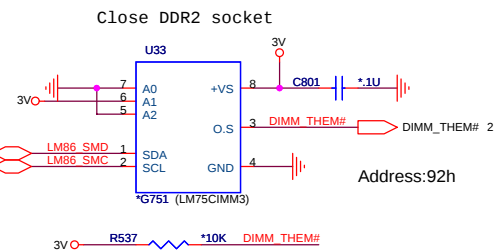
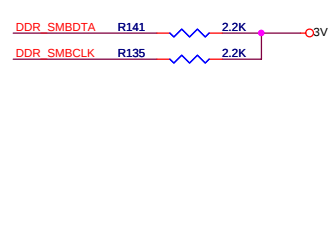
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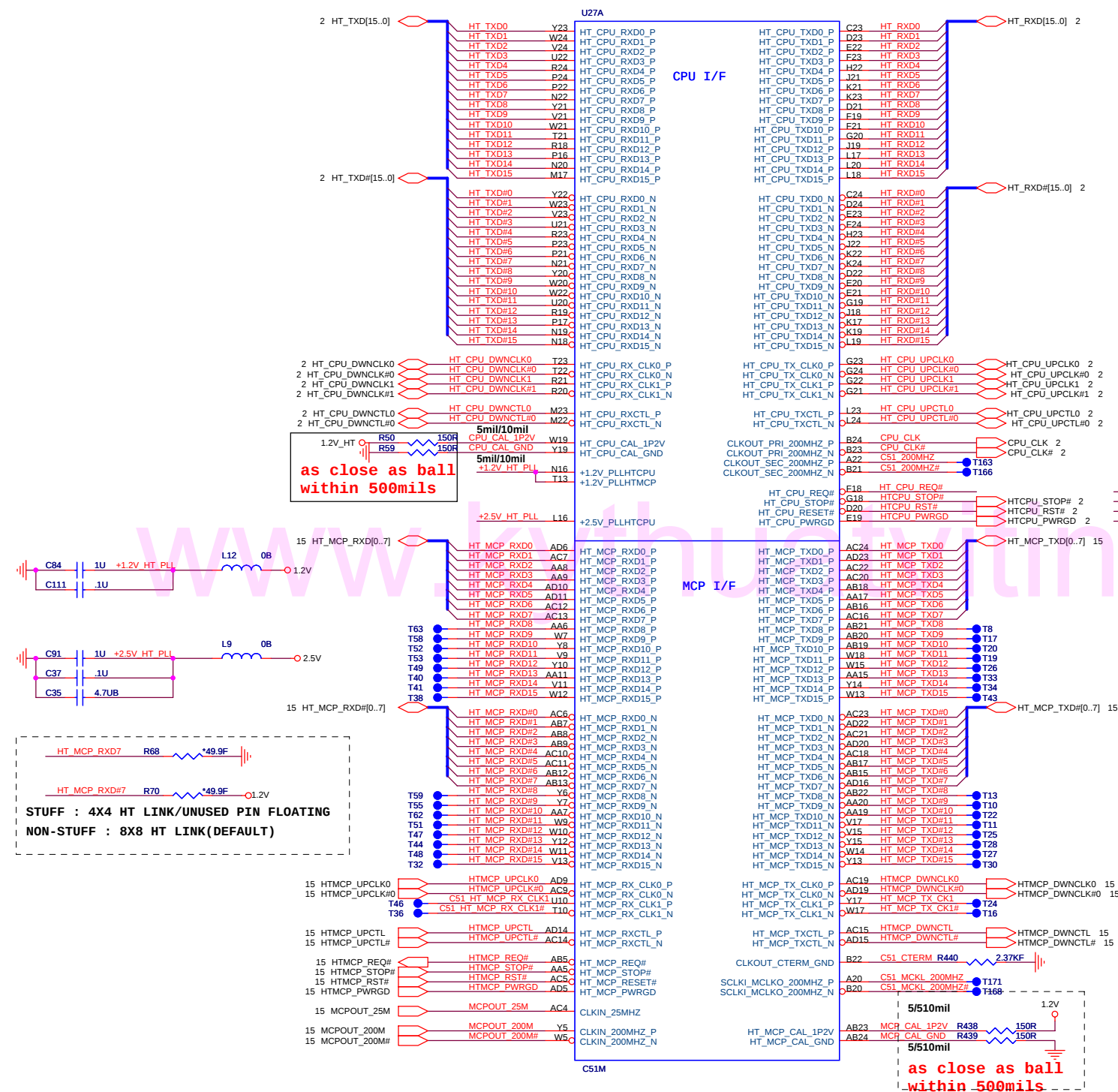
SMDDR_VREF_DIMM :
TRACE WIDTH > 20 MIL
PUT BYPASS CAP ON EACH DIMM

```



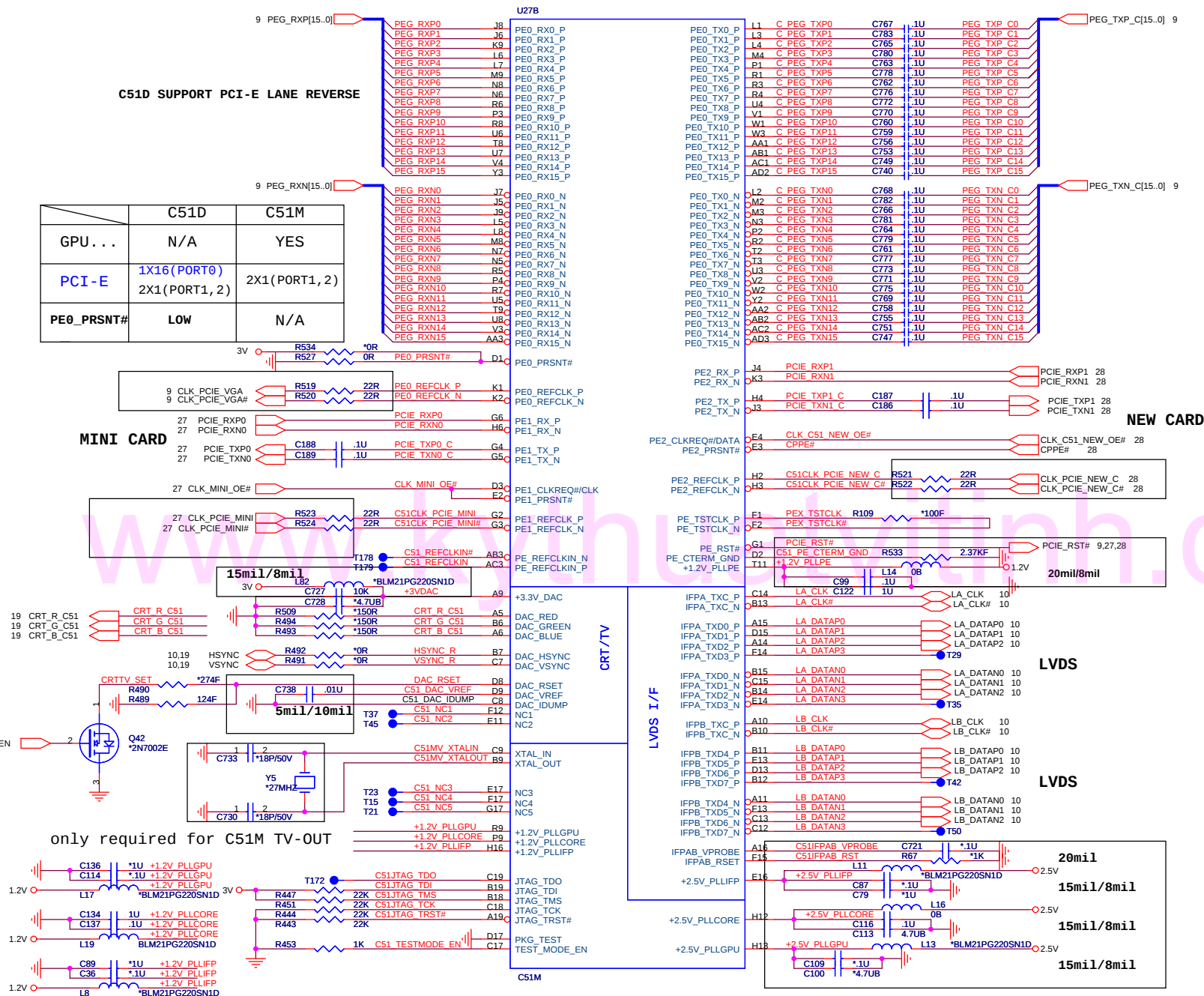
CKE 2,3







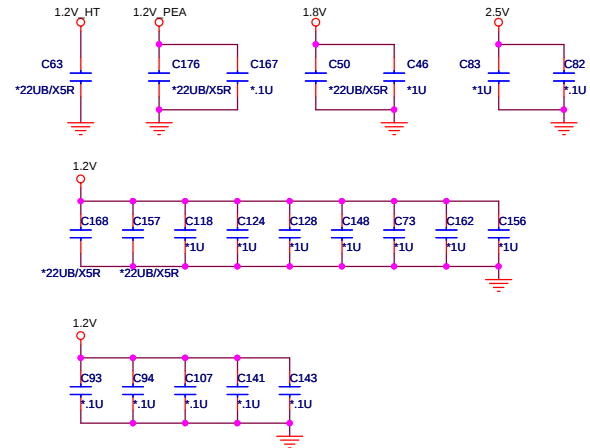
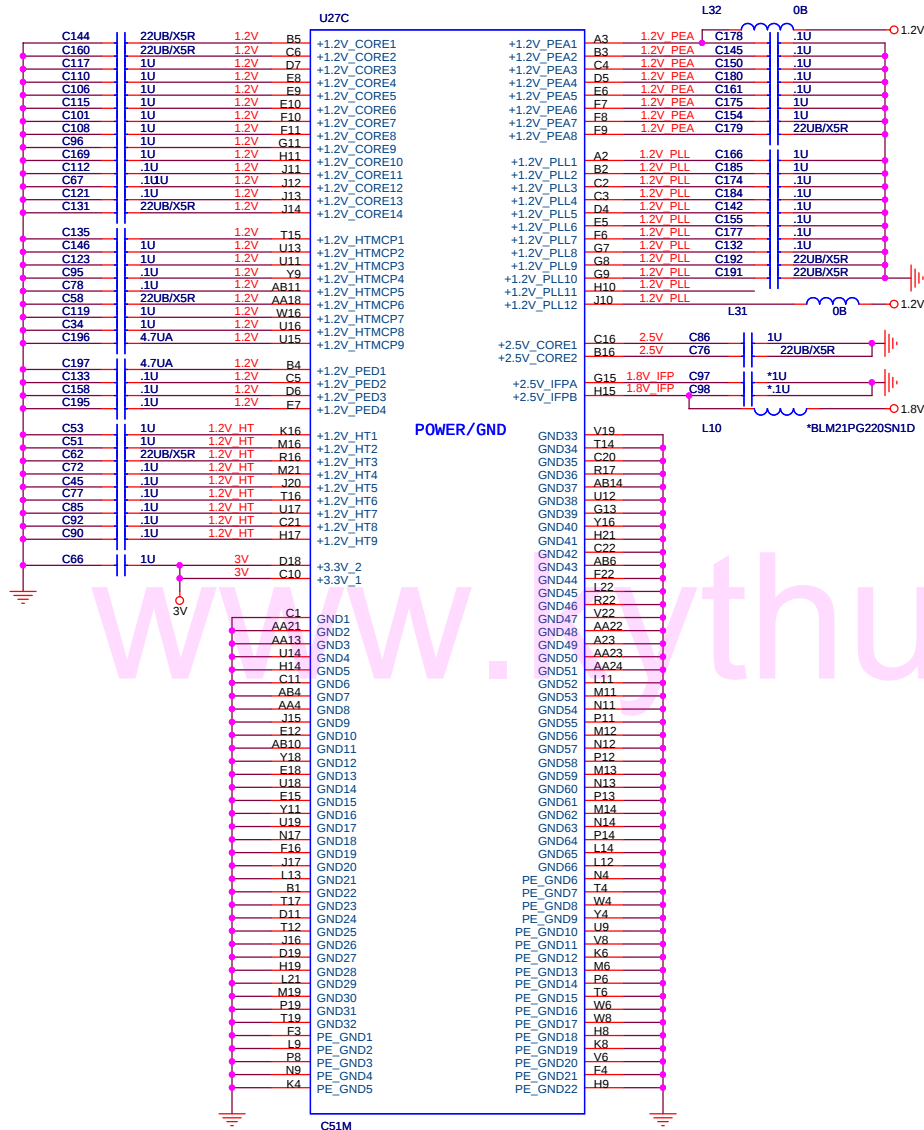
	C51D	C51M
GPU . . .	N/A	YES
PCI-E	1X16(PORT0) 2X1(PORT1, 2)	2X1(PORT1, 2)
PE0_PRSENT#	LOW	N/A

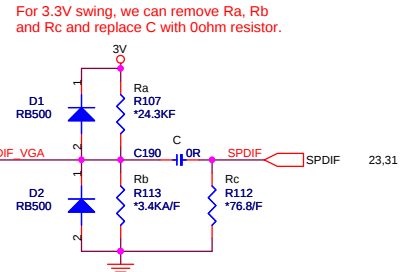


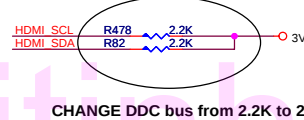
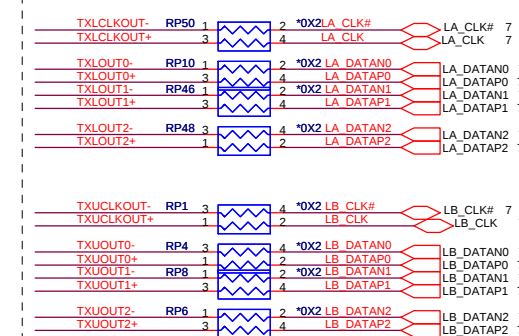
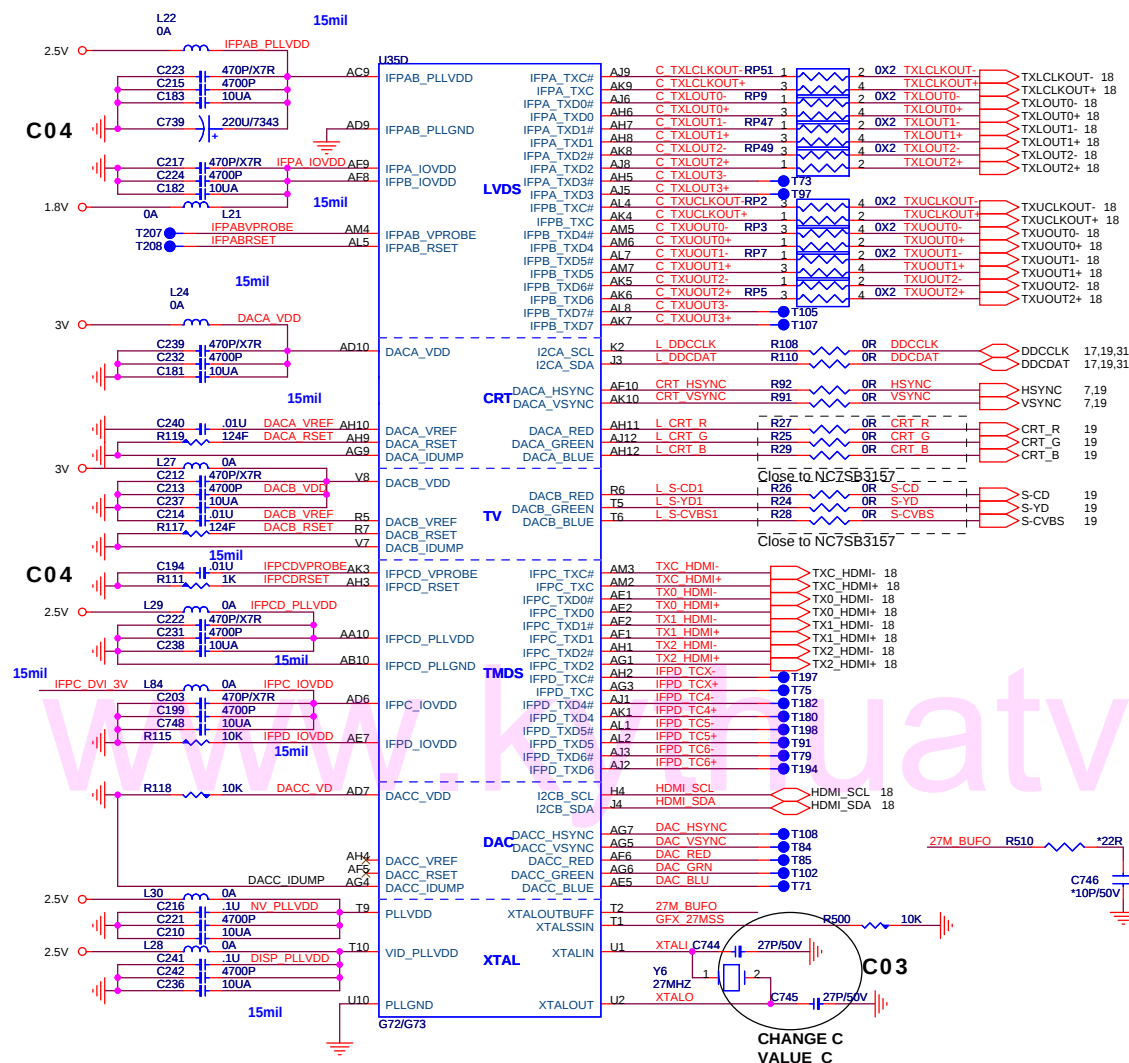
C51D Unused Power	Ball Terminations
C51D Signal Name	Termination
+1.2V_PLLGPU	Leave NC
+1.2V_PLLIFF	Leave NC
+2.5V_IFPA	Leave NC
+2.5V_IFPB	Leave NC
+2.5V_PLLIFF	Leave NC
+2.5V_PLLGPU	Leave NC
+3.3V_DAC	to GND directly
DAC_RSET	1240hm to GND
DAC_VREF	0.01u to GND

```
TRACE WIDTH :
C51_PE_CTERM_GND 5mil/5mil
C51IFPAB_VPROBE
C51IFPAB_RST
C51_DAC_VREF 5mil/10mil
+1.2V_PLLPE +1.2V_PLLIFP
+2.5V_PLLTFP +1.2V_PLLCOR
+2.5V_PLLCORE +1.2V_PLLGPU
+2.5V_PL LPGPU
```

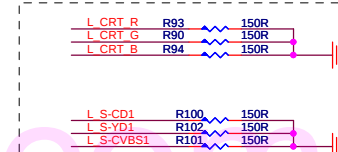
C51M/C51D POWER PLANE/GND & BYPASS



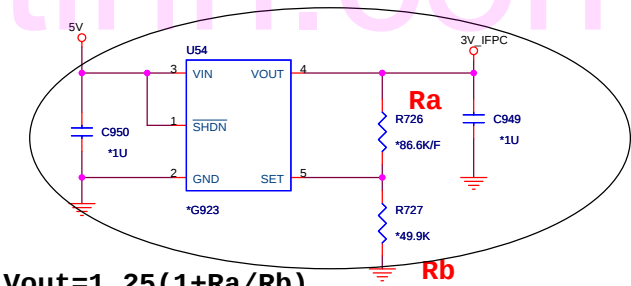


UMA ONLY

CHANGE DDC bus from 2.2K to 2K

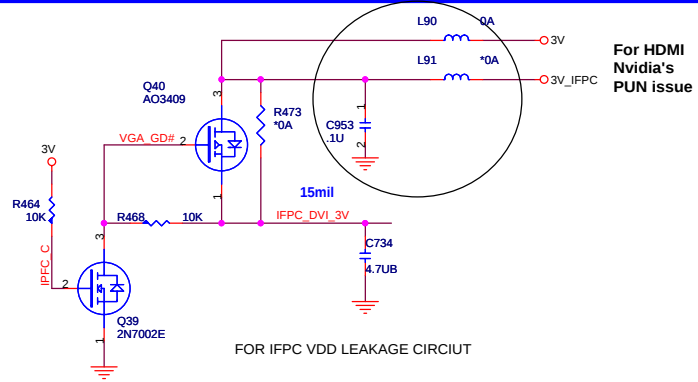


Close to GPU

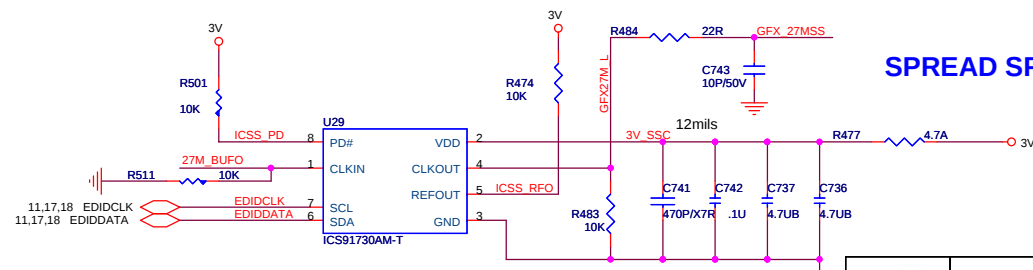


For HDMI
Nvidia's
PUN
issue

$$V_{out} = 1.25 (1 + R_a/R_b)$$



For HDMI
Nvidia's
PUN issue



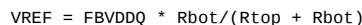
SPREAD SPECTRUM

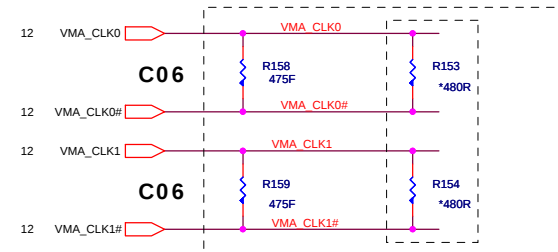
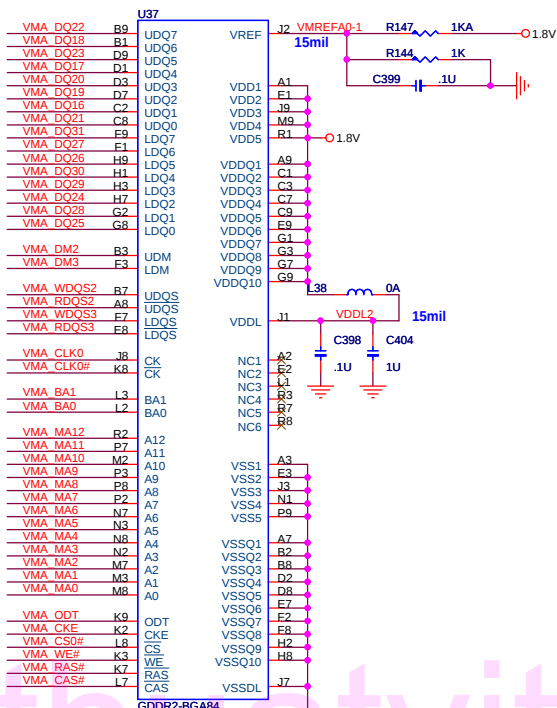
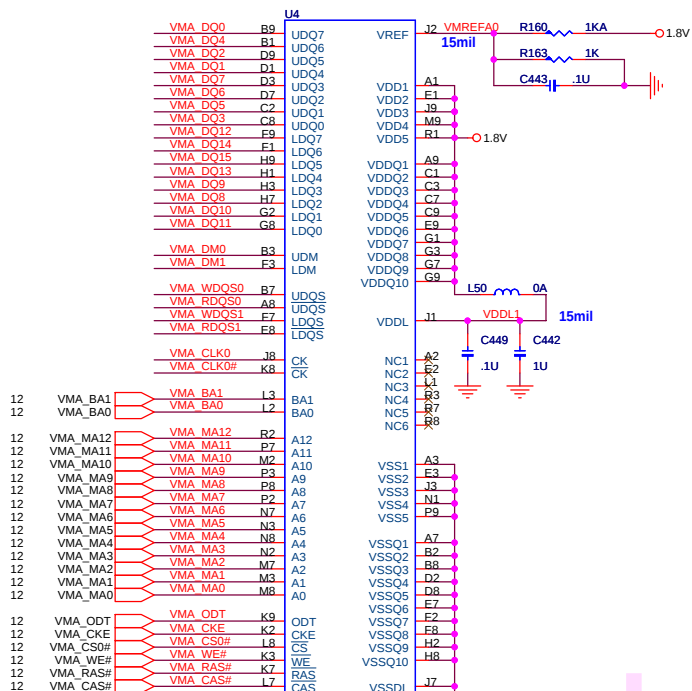
I2C ADDRESS: 0xD4H



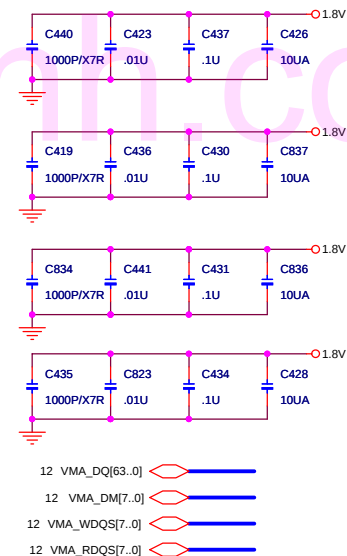
PROJECT : AT8
Quanta Computer Inc.

Size Custom	Document Number GFX(LVDS, CRT, TV)	Rev 2A
Date: Wednesday, June 14, 2006		Sheet 10 of 39





G72M: 120 ohm
G73M: 470-490 ohm

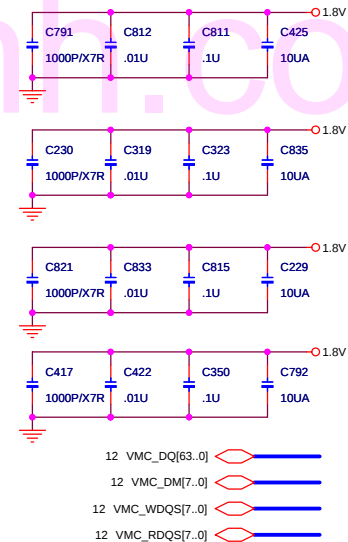
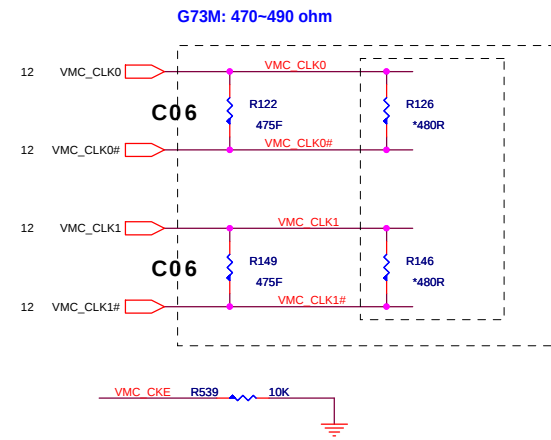
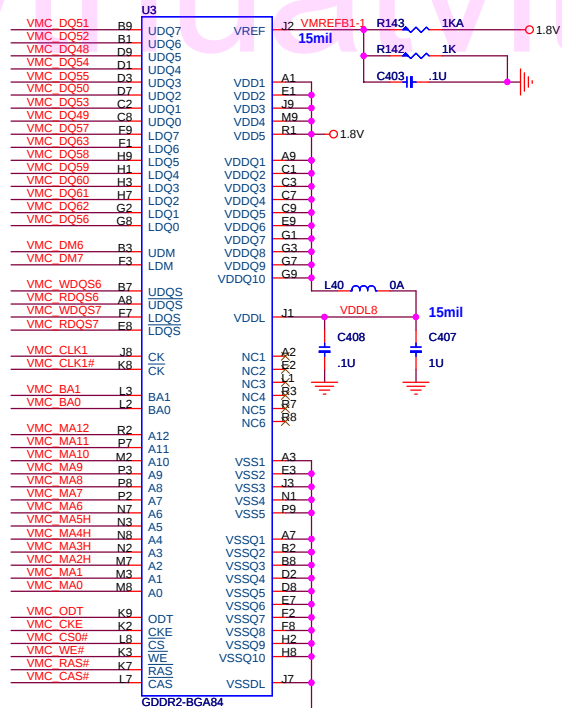
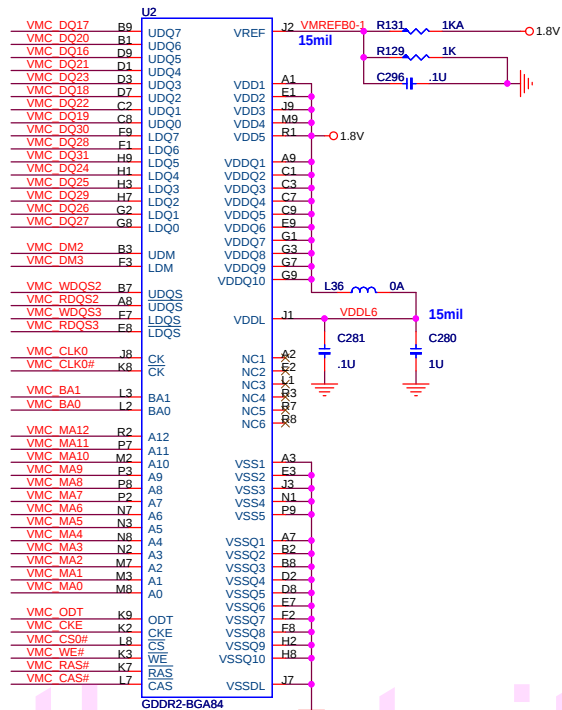
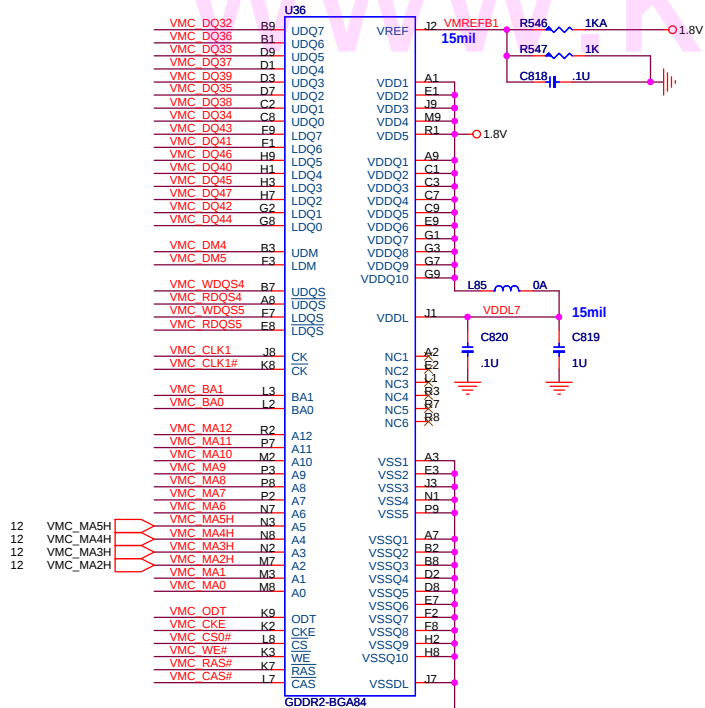
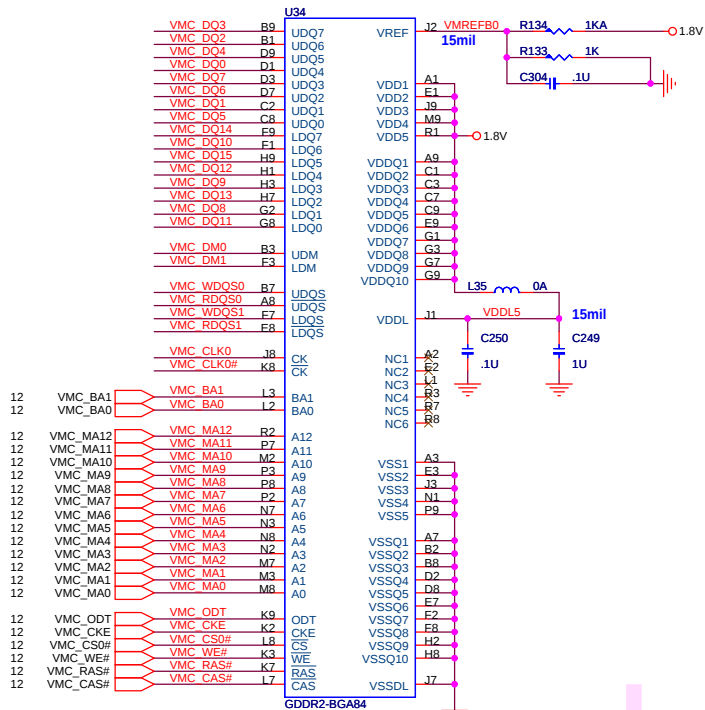


256Mb : AKD5JGAT*05
512Mb : AKD59G-T*01

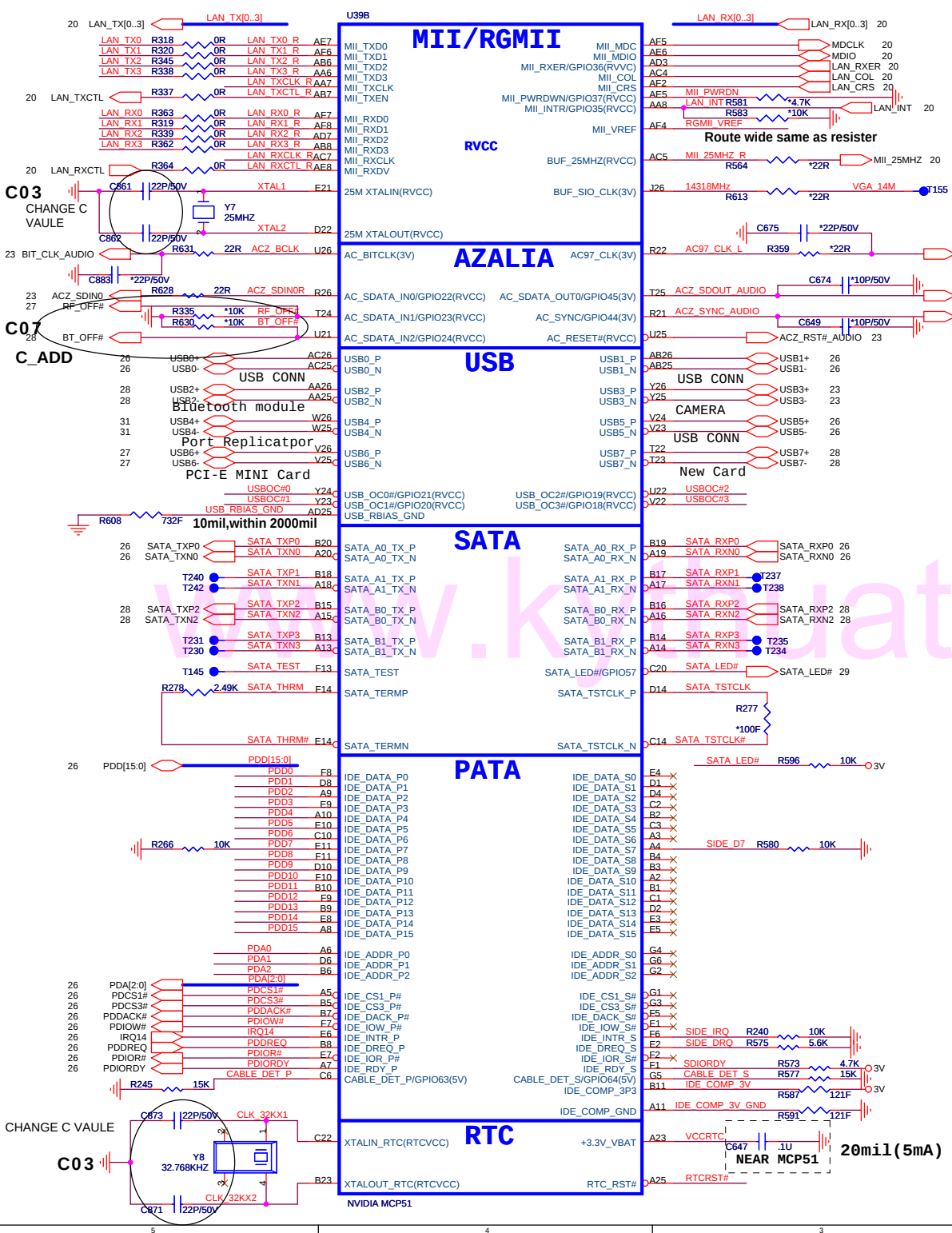


PROJECT : AT8
Quanta Computer Inc.

Size Custom	Document Number VRAM-1 (GDDR2)	Rev 1A
Date: Wednesday, June 14, 2006	Sheet 13	of 39

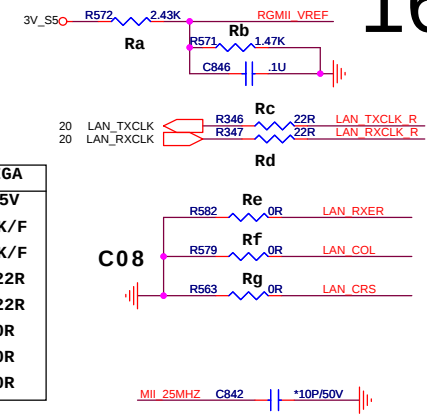


256Mb : AKD5JGAT*05
 512Mb : AKD59G-T*01



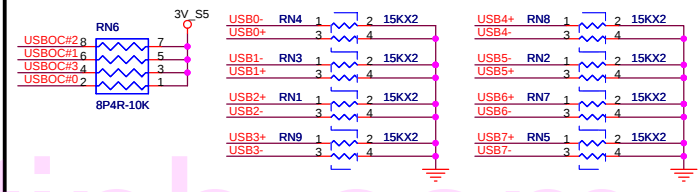
10/100 - GIG LAN STUFF OPTION

16

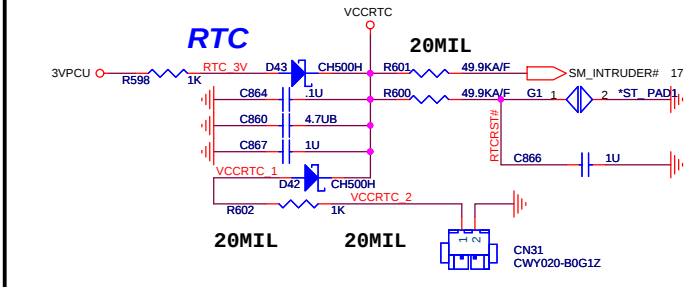


	10/100	GIGA
VREF	1.65V	1.25V
Ra	1K/F	2.43K/F
Rb	1K/F	1.47K/F
Rc	0R	22R
Rd	0R	22R
Re	NC	0R
Rf	NC	0R
Rg	NC	0R

C_CHANGE



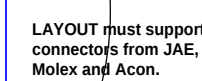
ACZ_SPKR STRAP (Boot Mode)	ACZ_RST# STRAP (LAN)
0 User Table*	0 MII
1 Safe Table	1 RGMII*
*DEFAULT	*DEFAULT
SPIDF0 STRAP (SIO CLK)	SUSCLK STRAP (MCP MODE)
0 14.318MHZ*	0 NORMAL*
1 24.000MHZ	1 SLAVE
*DEFAULT	*DEFAULT





PROJECT : AT8
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Size Custom	Document Number MCP51 (1 of 3)	Rev 3A
Date: Wednesday, June 14, 2006		Sheet 16 of 39

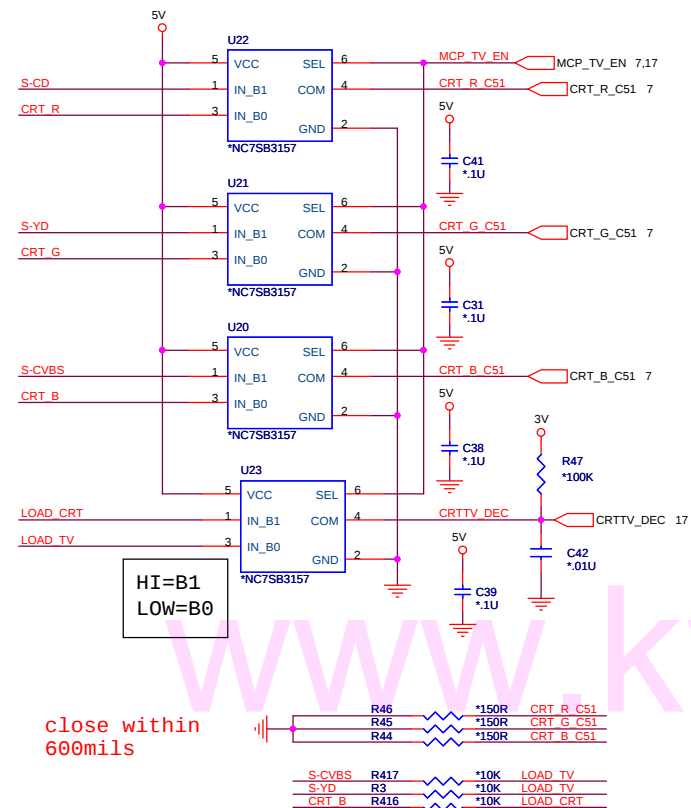


NB5/RD2/HW

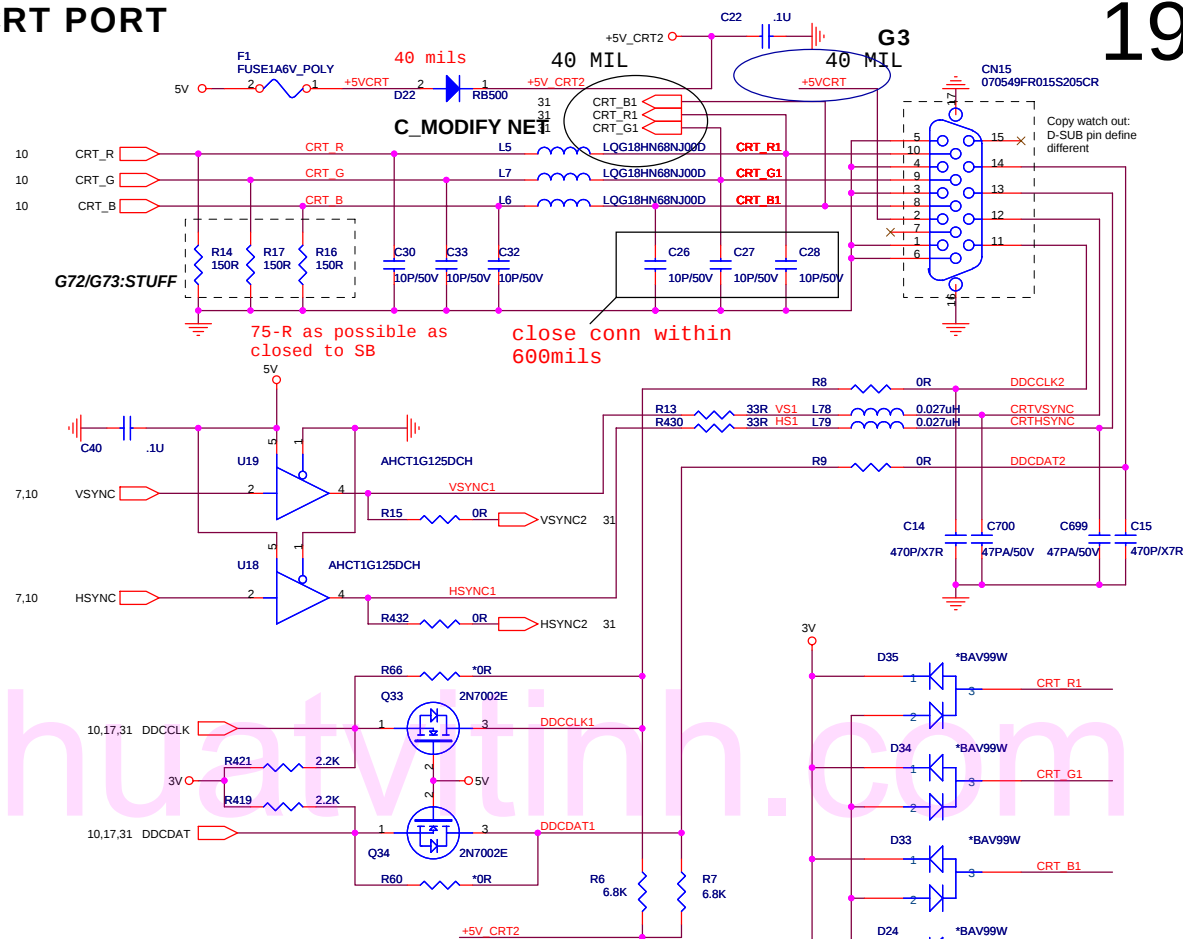
PROJECT : AT8
Quanta Computer Inc.

Size Custom	Document Number LCD CONN,HDMI CONN	Rev 3
Date: Wednesday, June 14, 2006	Sheet 18 of 39	

For UMA only



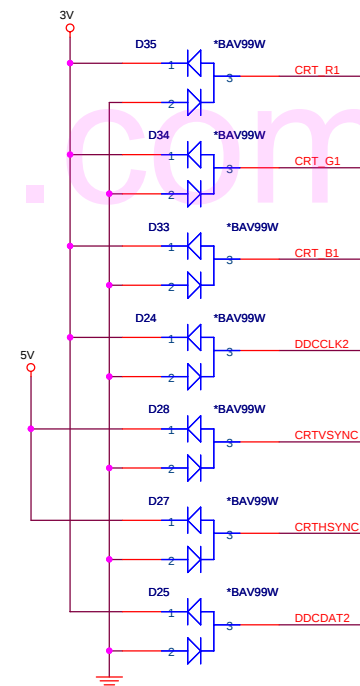
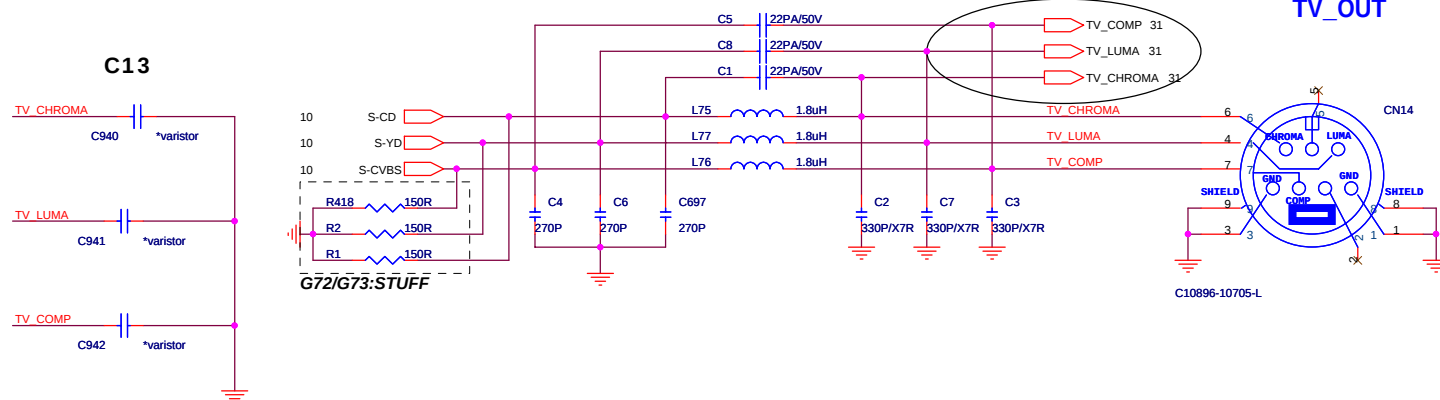
CRT PORT



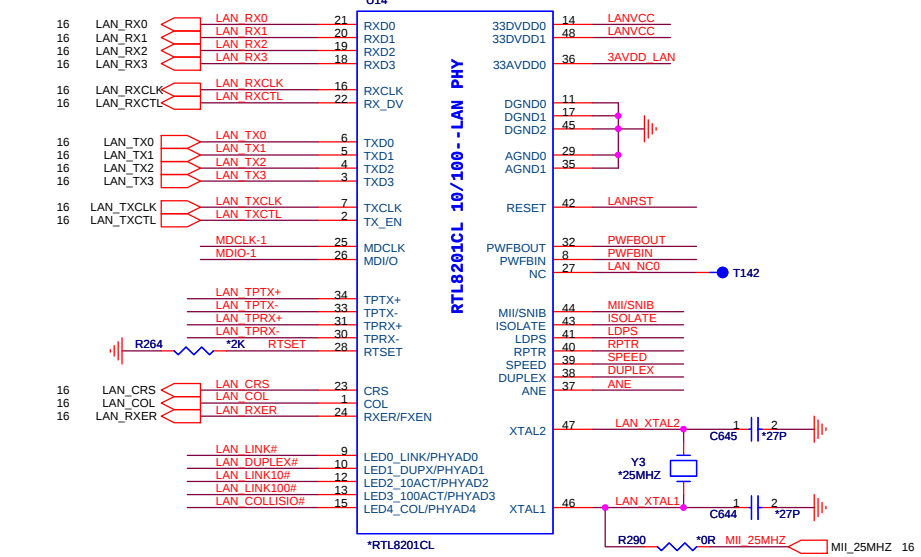
19

C_MODIFY NET

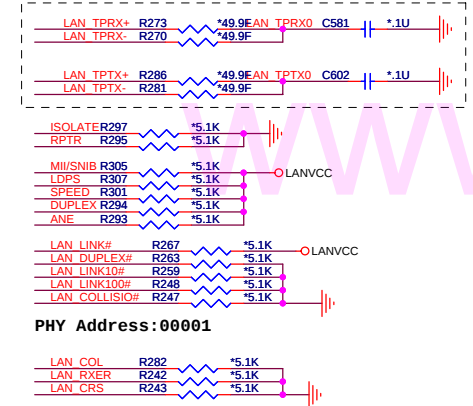
TV_OUT



10/100M

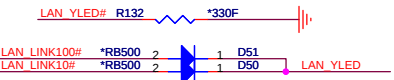
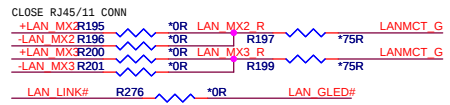
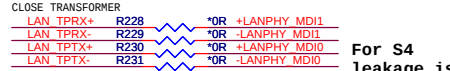


Close To RTL8201CL



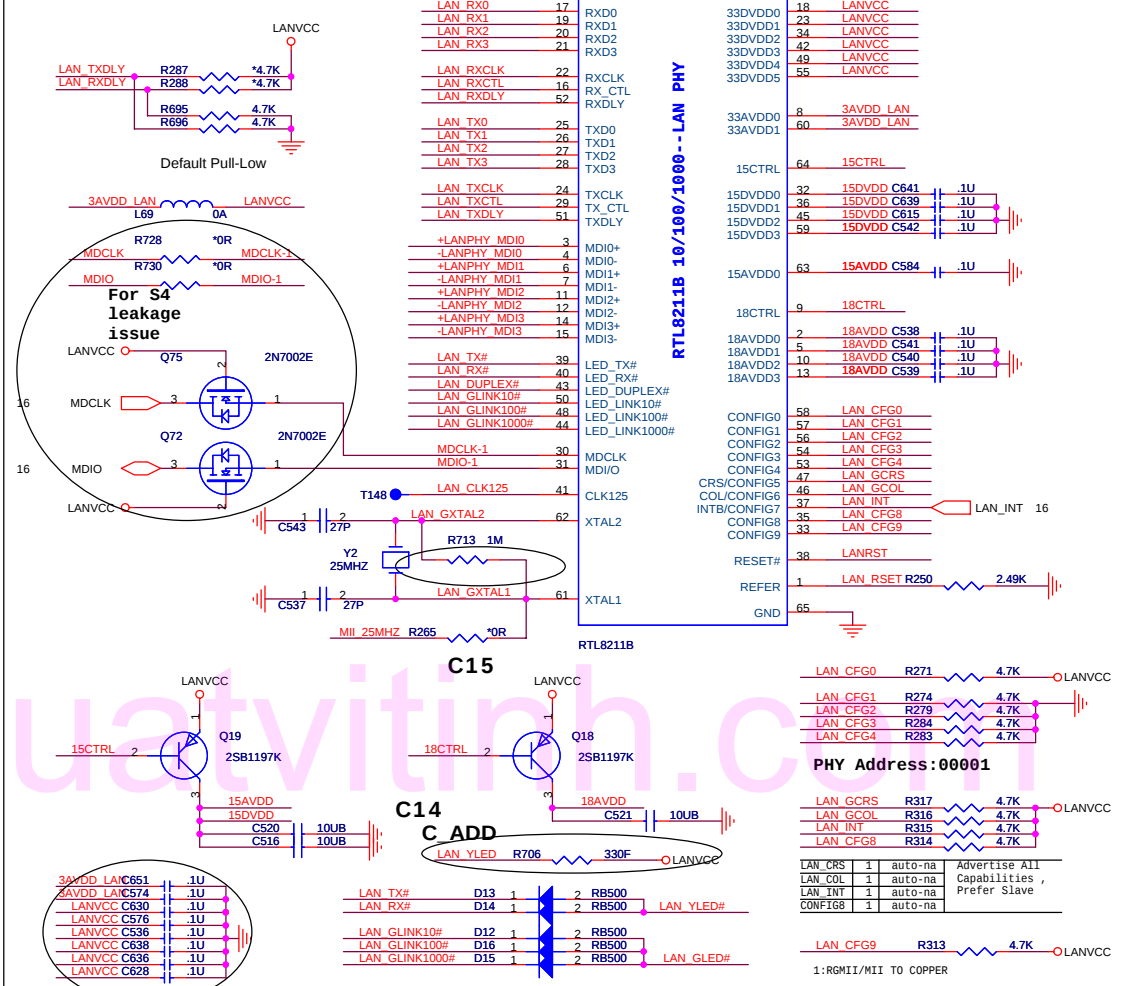
PHY Address:00001

LAN_COL	1	Default	RTL8201B LED
LAN_RXER_R	1	Default	Fiber Mode
LAN_CRIS	0	Default	UTP Mode
LAN_CRIS	0	Default	Ensuring operating at normal mode

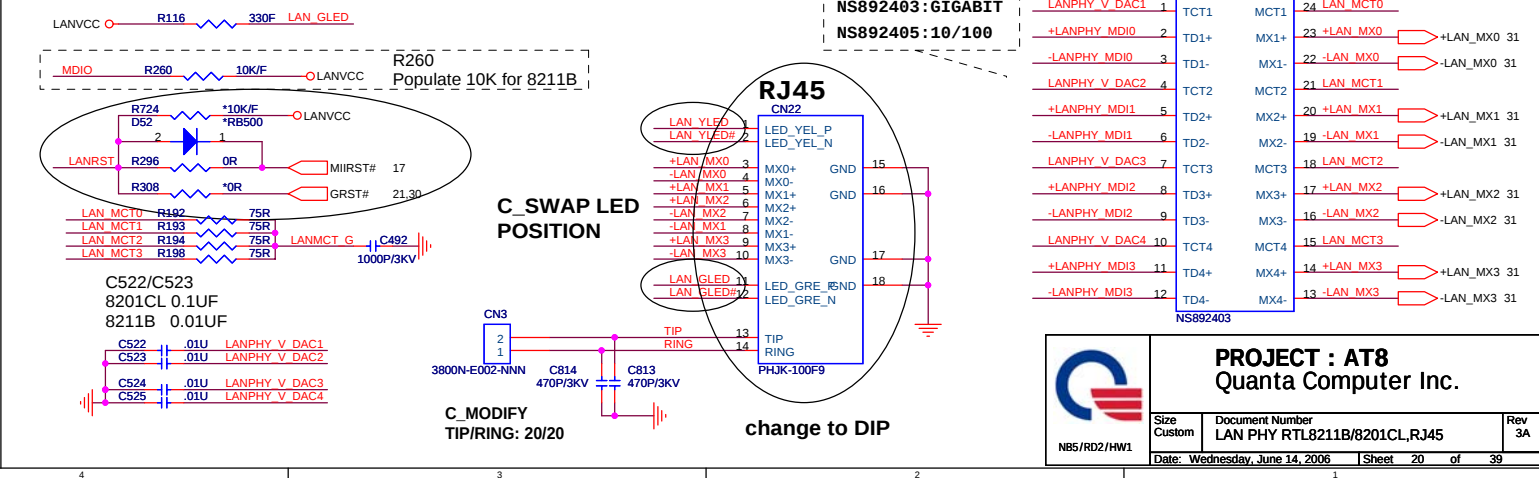


LINK10/100# assert high while system power up.

10/100/1000M

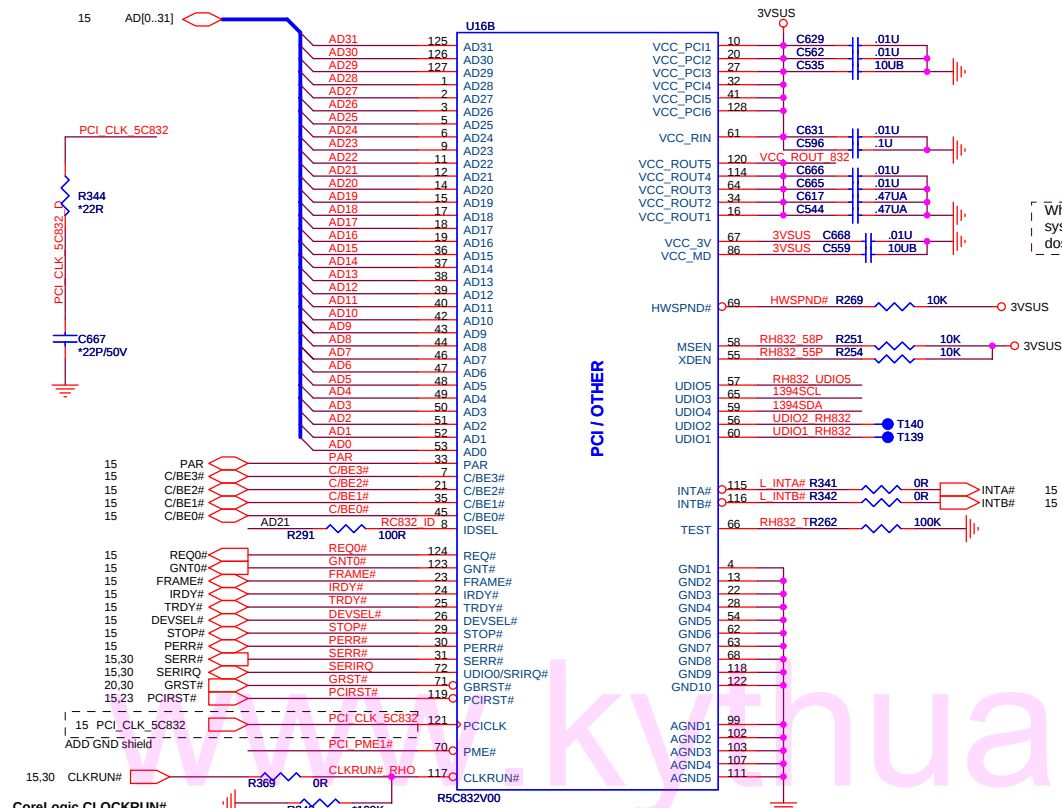


LAYOUT REPLACE_C FOR EMI



PROJECT : AT8
Quanta Computer Inc.

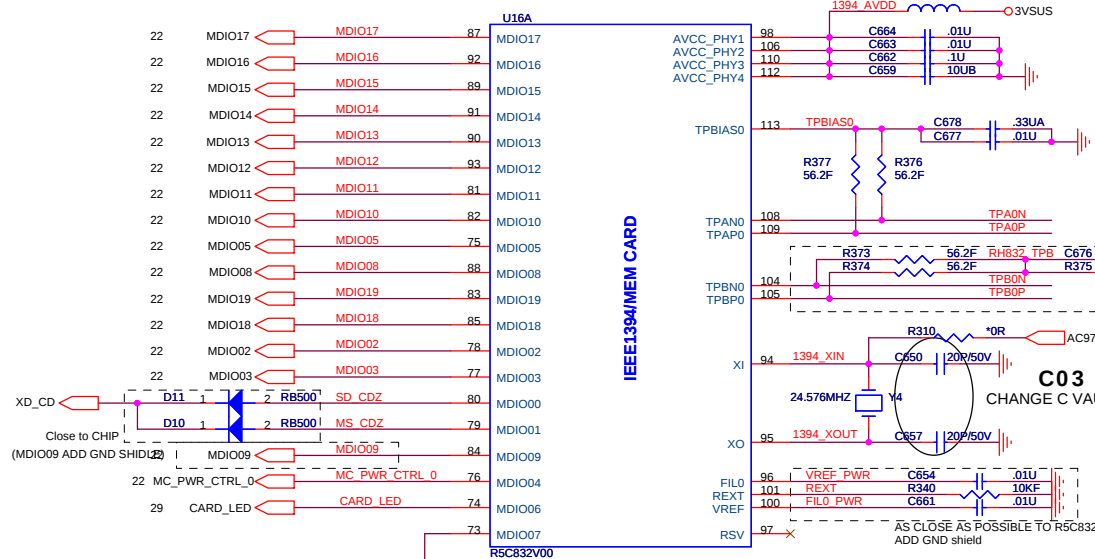
Size Custom	Document Number LAN PHY RTL8211B/8201CL_RJ45	Rev 3A
Date: Wednesday, June 14, 2006	Sheet 20 of 39	



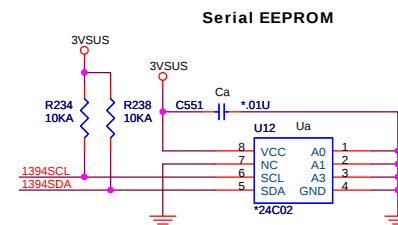
CoreLogic CLOKRUN#
When CLKRUN# is controlled by system, the pull-down resistor(R14) dose not need to apply.

PCI / OTHER

IEEE1394/MEM CARD

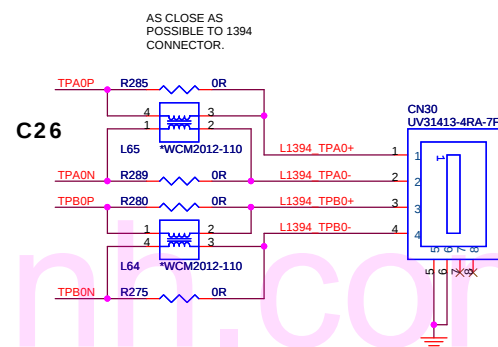


When HWSPND# is controlled by system, the pull-up resistor(R2) dose not need to apply.

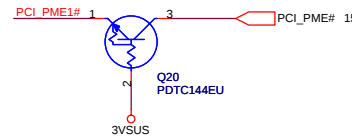
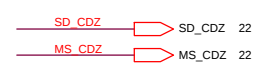


* NOT Use EEPROM :
Ra : installed
Rb,Ua,Ca : NOT installed

* Use EEPROM :
Rb,Ua,Ca : installed
Ra : NOT installed



*TPA/TPA# ,TPB/TPB# pair trace : As close as possible.
*TPA/TPA# ,TPB/TPB# pair trace : Same length electrically And layout with shields.
Termination resistor for TPA+/- TPB+/- : As close as possible to its cable driver (device pin out).



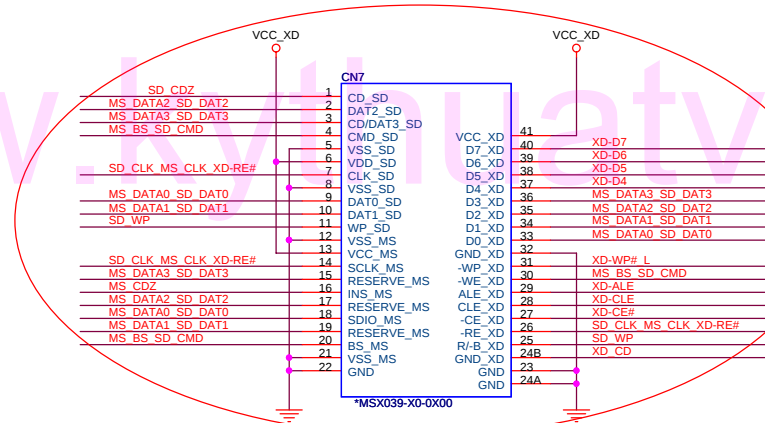
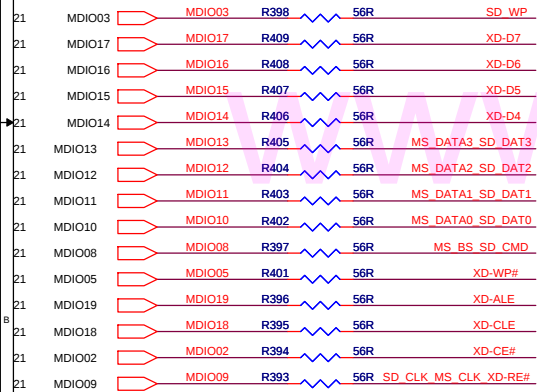
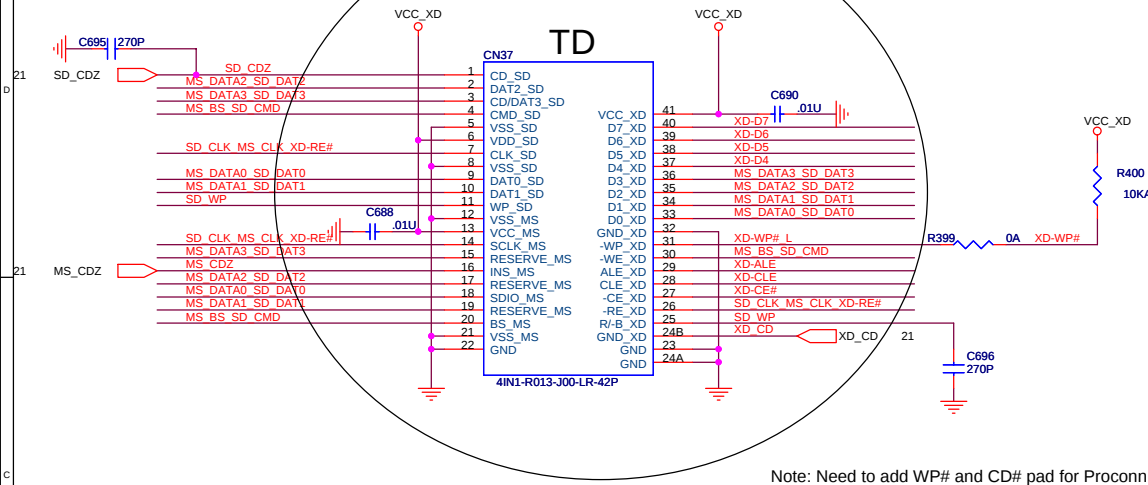
PROJECT : AT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	R5C832 CONTROL	1A
Date: Wednesday, June 14, 2006	Sheet 21 of 39	

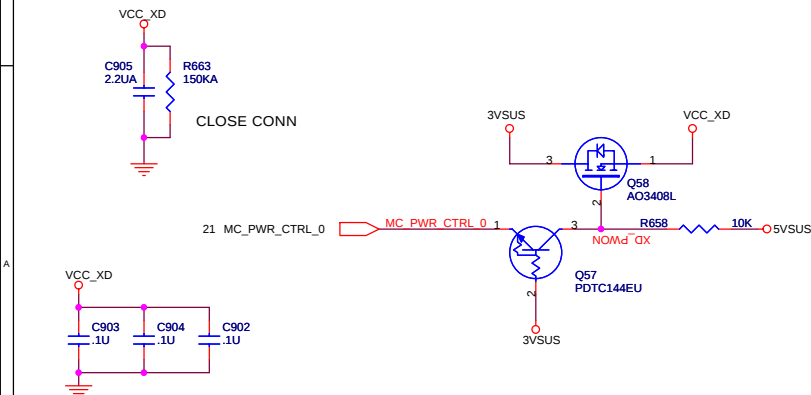
4 IN1 CARD READER

XD, MMC/SD, MS/MSP

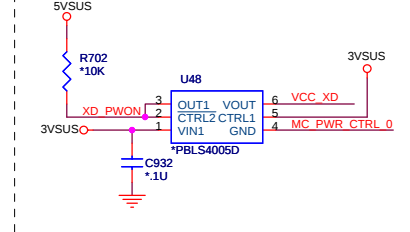
CHECK CONN.



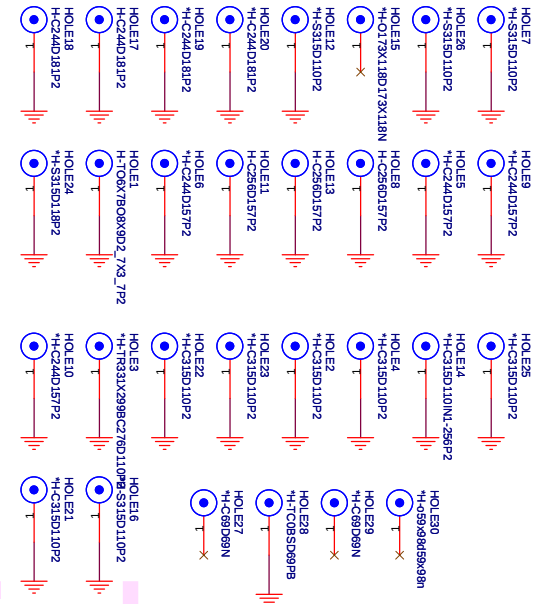
2'nd source



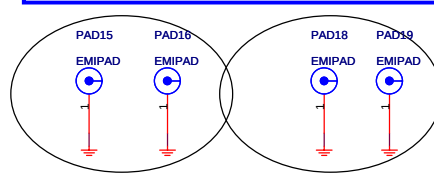
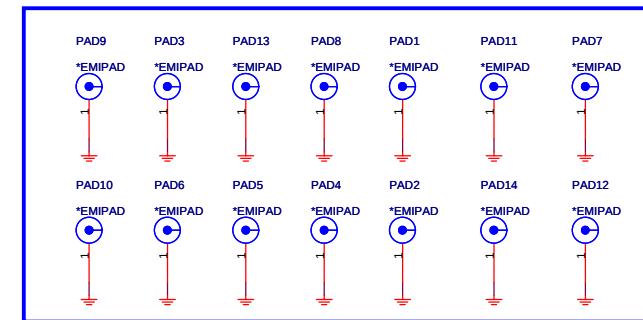
Reserve



SCREW HOLE



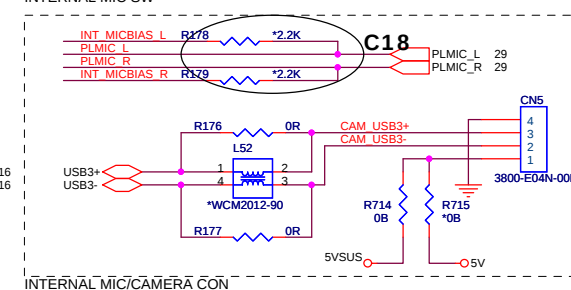
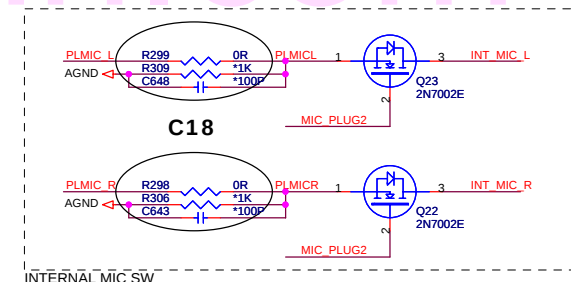
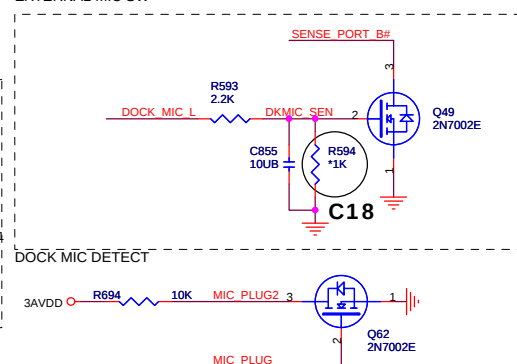
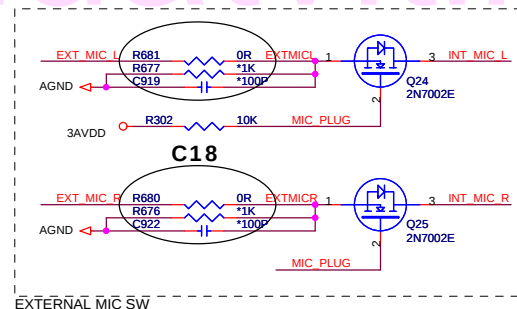
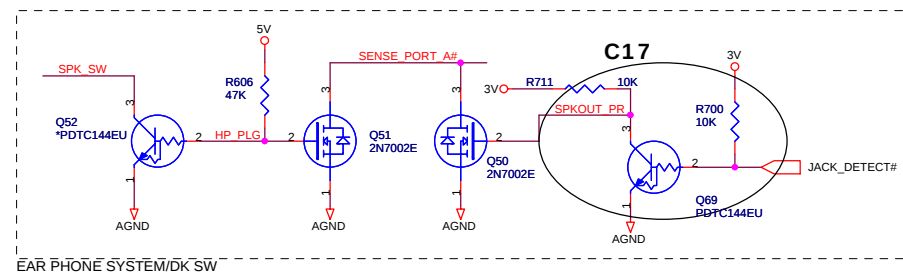
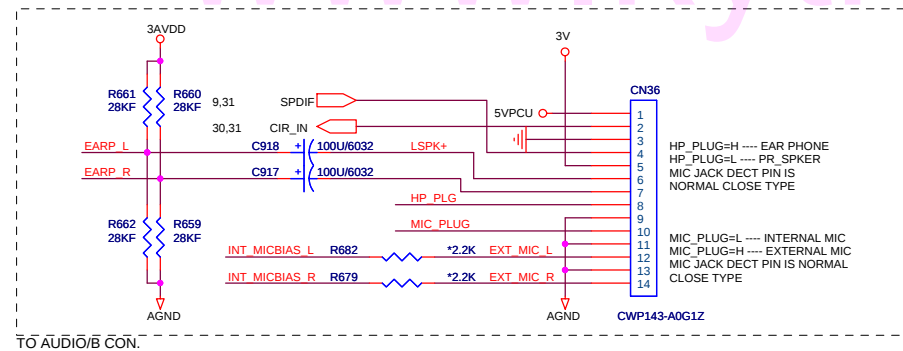
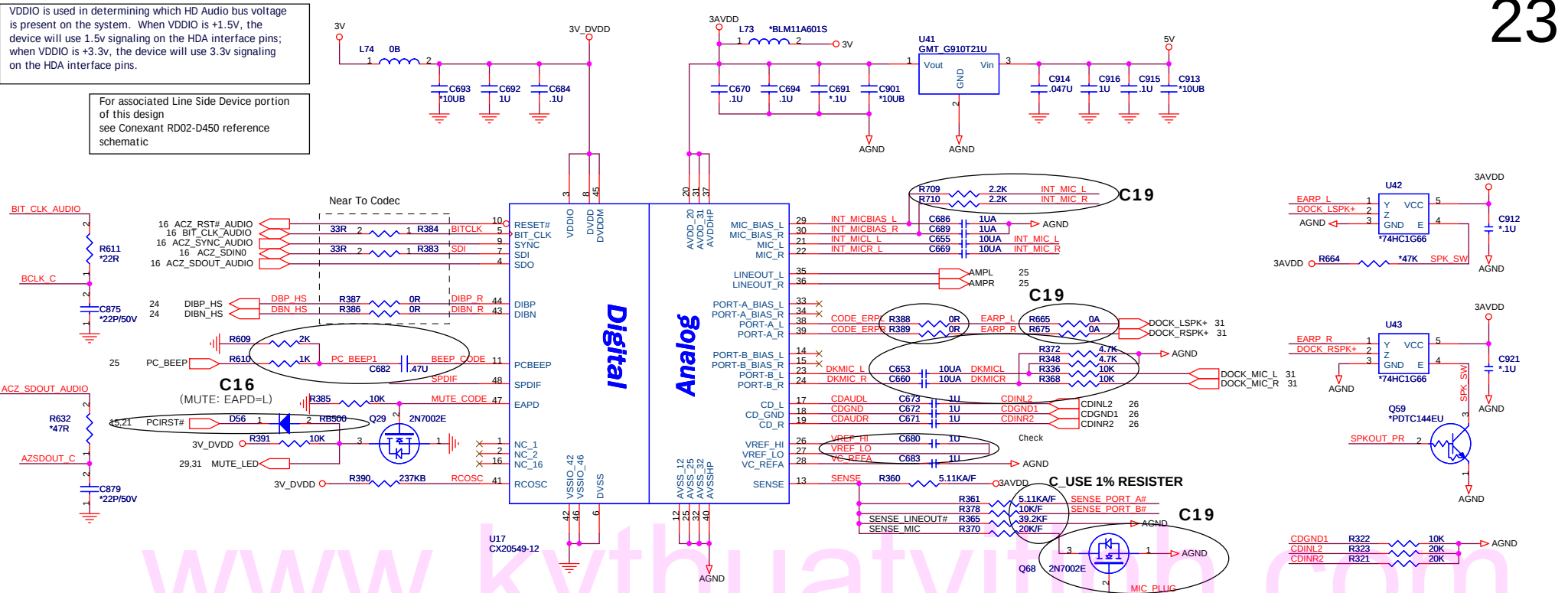
EMI PAD

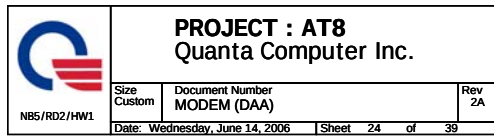


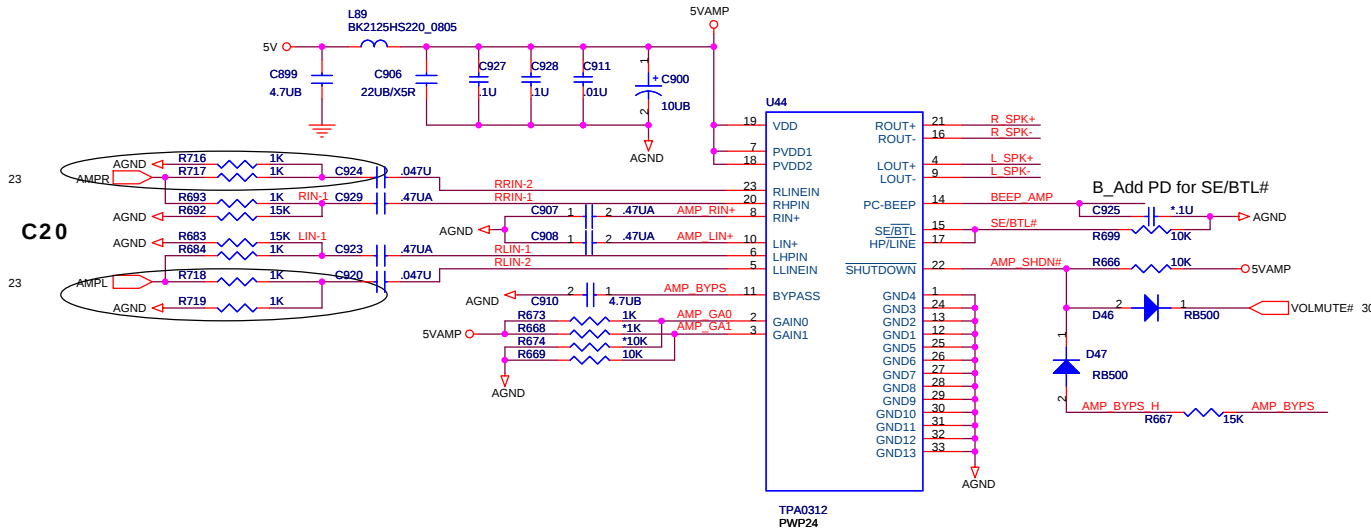
C_ADD

		PROJECT : AT8	
		Quanta Computer Inc.	
Size Custom	Document Number CARD READER CONN	Rev 3A	
Date: Wednesday, June 14, 2006		Sheet	22 of 39

For associated Line Side Device portion
of this design
see Conexant RD02-D450 reference
schematic

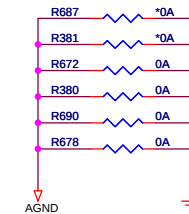






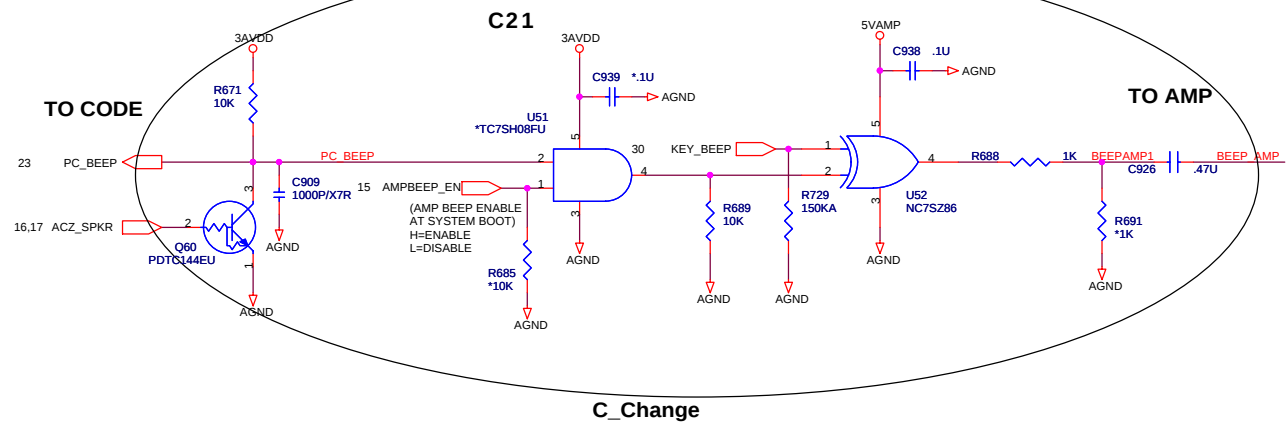
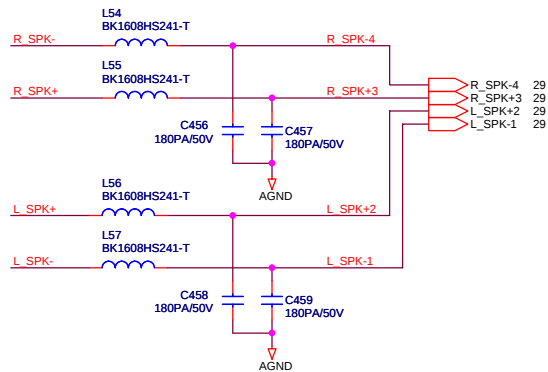
0312 Gain Table

GAIN0	GAIN1	SE/BTL	AV(INV)
0	0	0	6dB
0	1	0	10dB
1	0	0	15.6dB
1	1	0	21.6dB
x	x	1	4.1dB

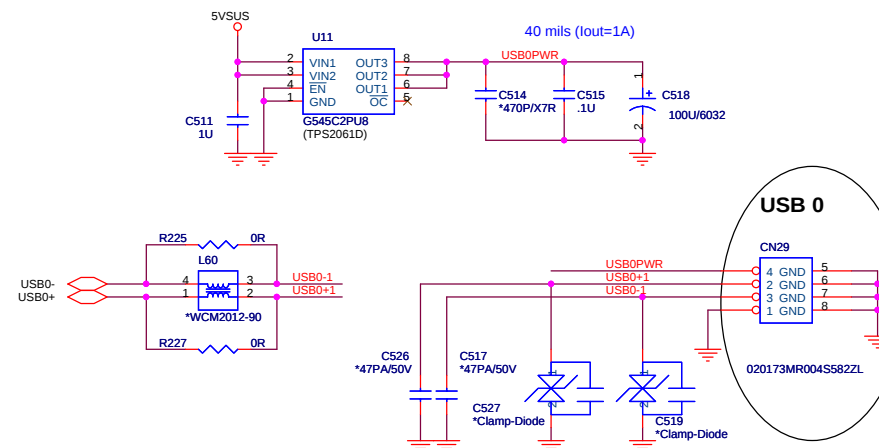
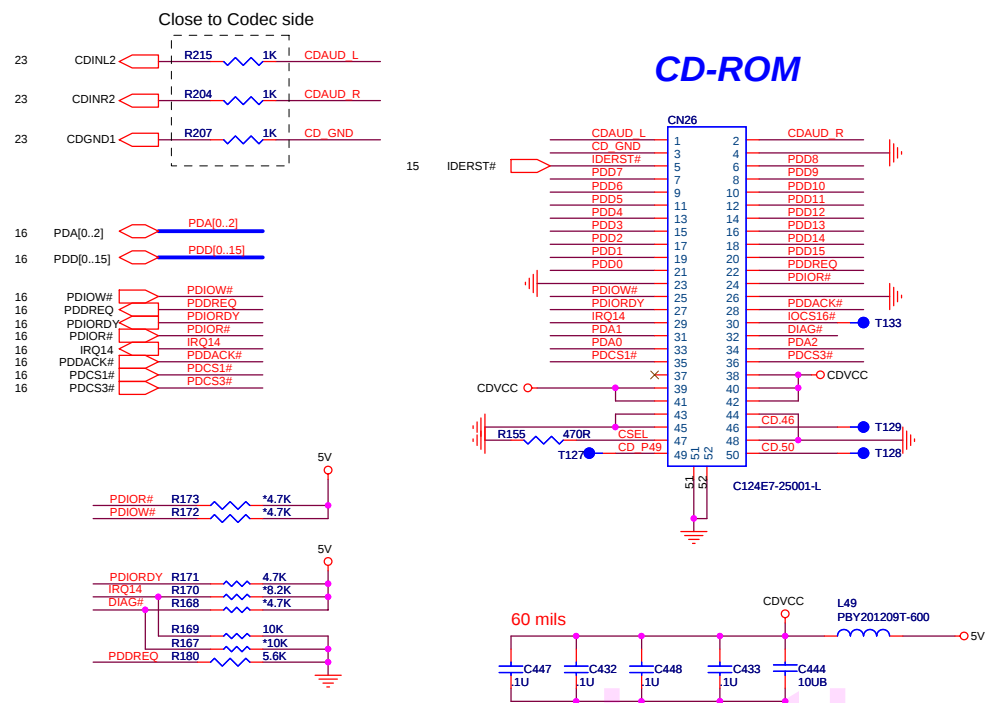


INT. SPEAKER

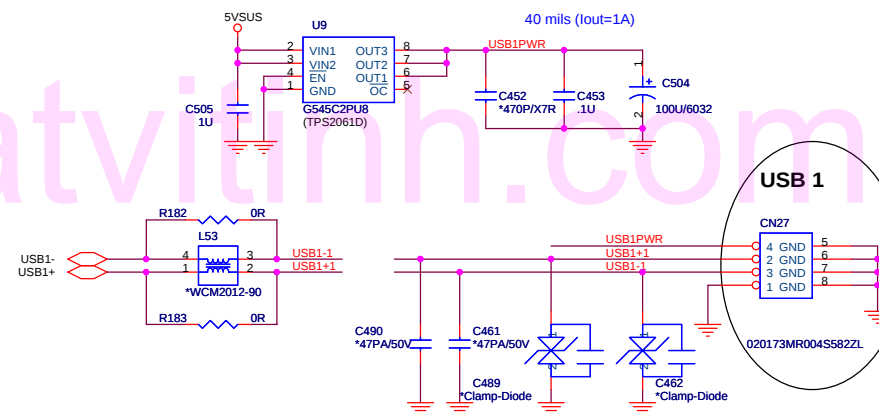
PCSPK BEEP



USBX2

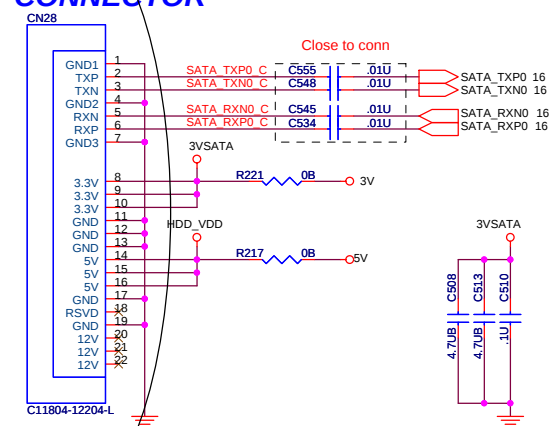


change to DIP



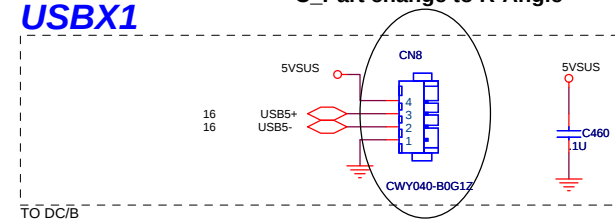
change to DIP

**SATA_1
CONNECTOR**

C_CHANGE
FOOTPRINT

USBX1

C_Part change to R-Angle

 $\overline{TO} \overline{DC/B}$ 

NB5/RD2/HW1

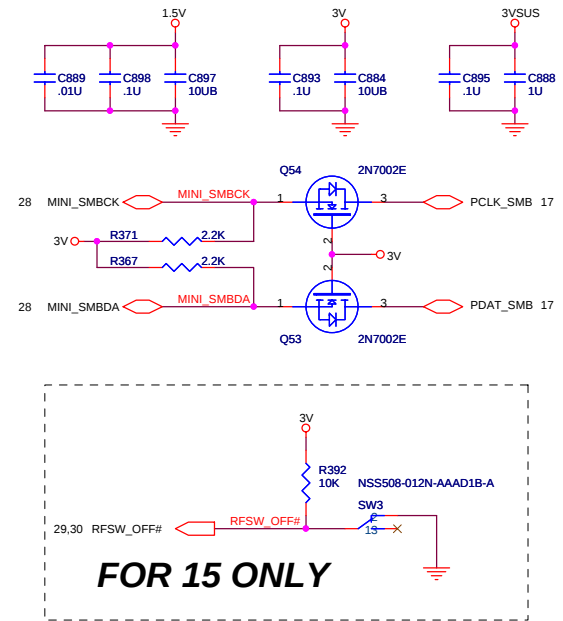
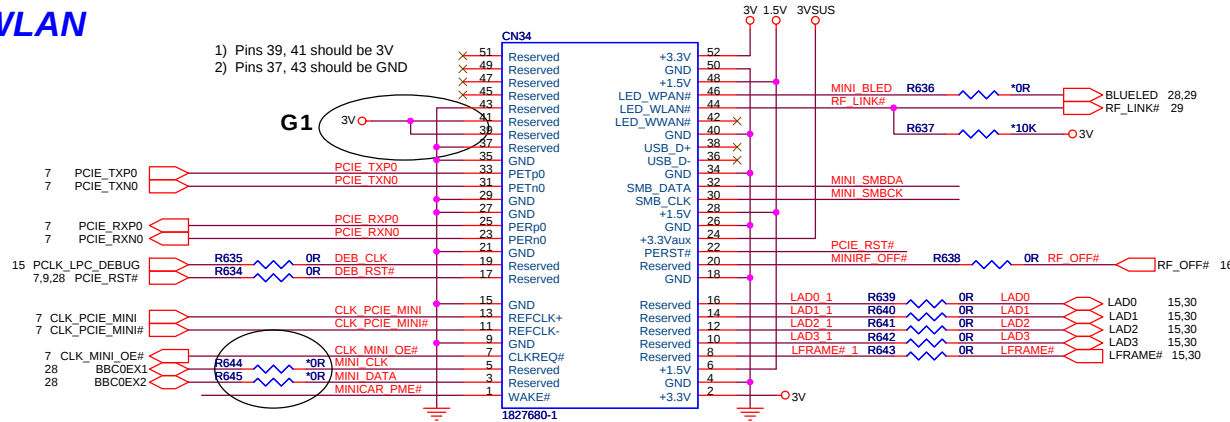
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Quanta Computer Inc.

Size Custom	Document Number SATA HDD, CD-ROM, USBX2	Rev 3A
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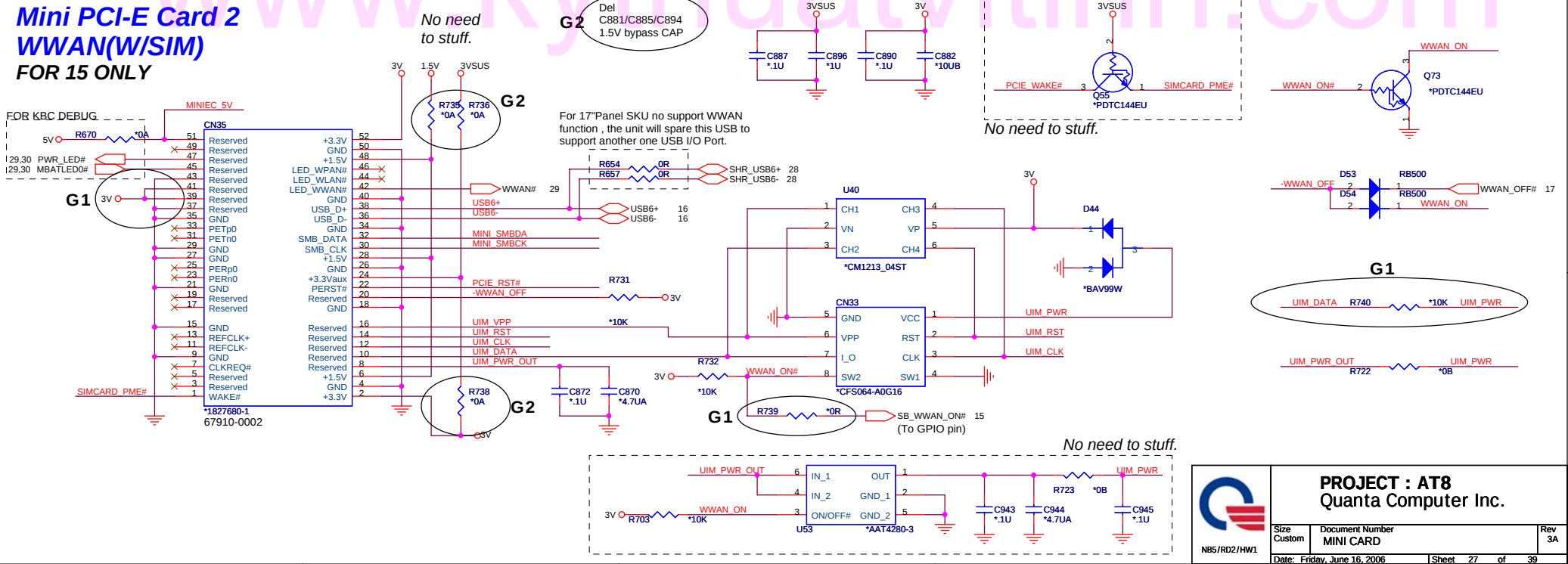
Mini PCI-E Card 1 WLAN

27

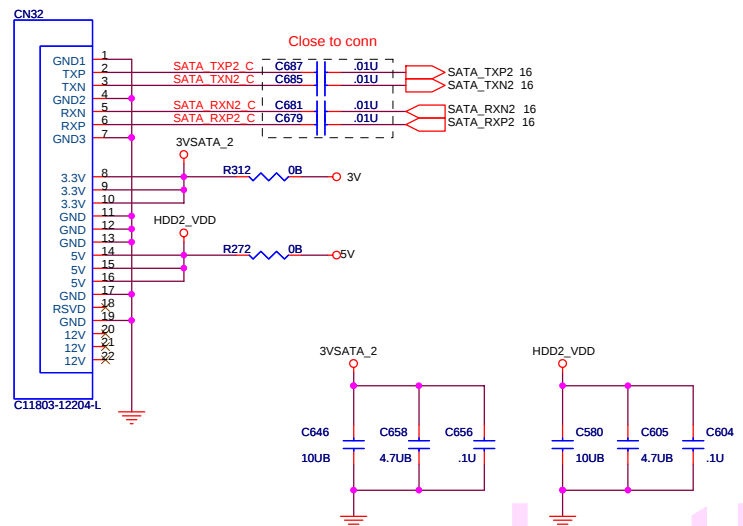
- 1) Pins 39, 41 should be 3V
- 2) Pins 37, 43 should be GND



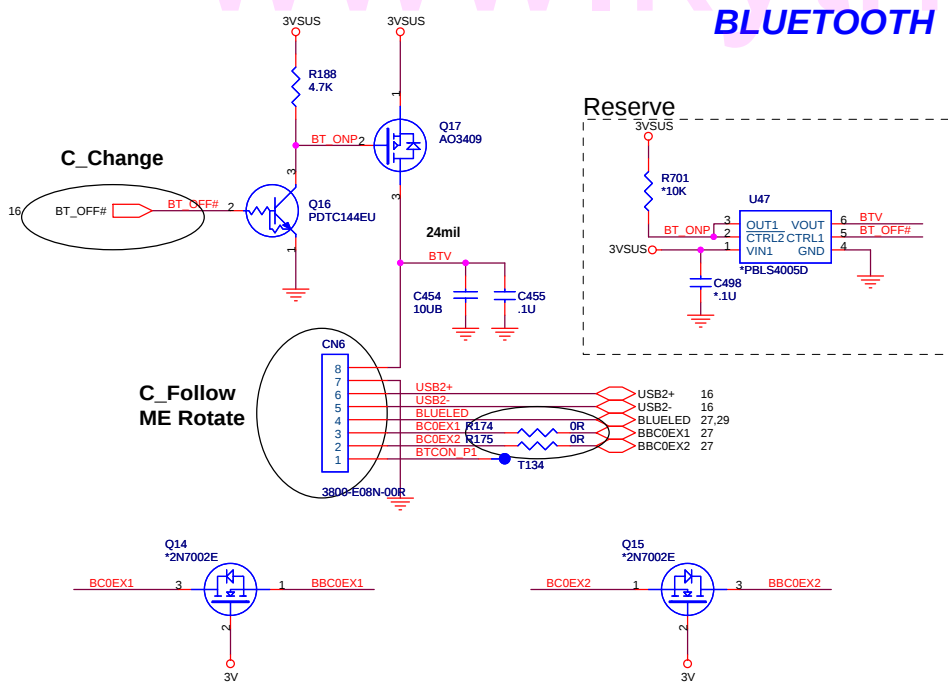
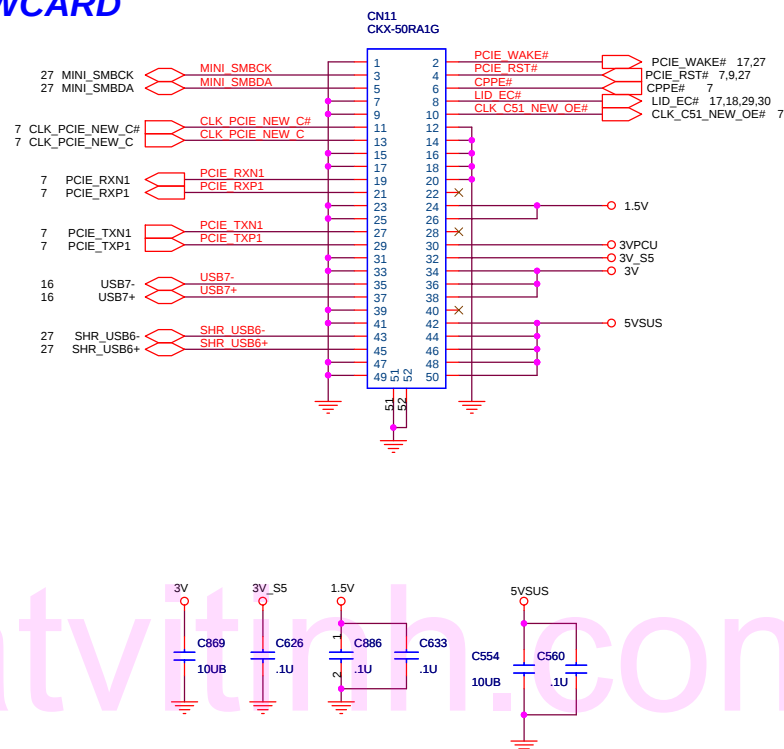
Mini PCI-E Card 2 WWAN(W/SIM) FOR 15 ONLY



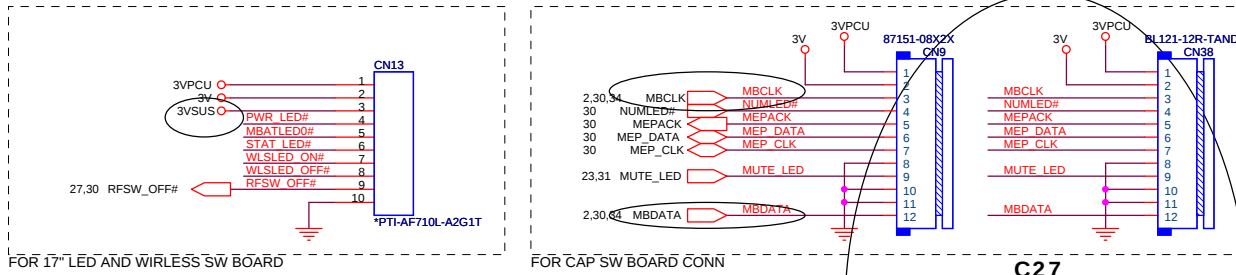
SATA_2 CONNECTOR
For 17"W Second HDD



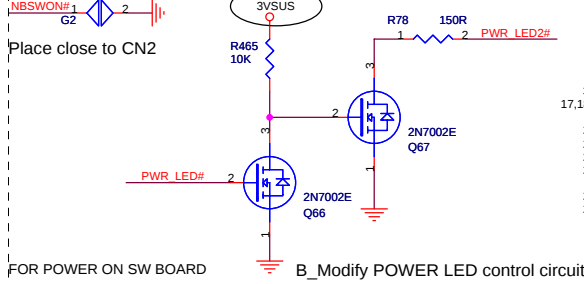
BLUETOOTH

**NEWCARD**

C_RESERVE FOR 2'ND SOURCE
C_CHANGE FOOTPRINT

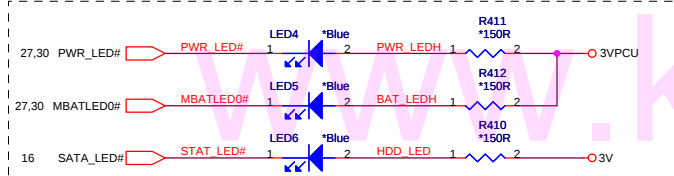


IB_ADD *ST_PAD1 C_MODIFY

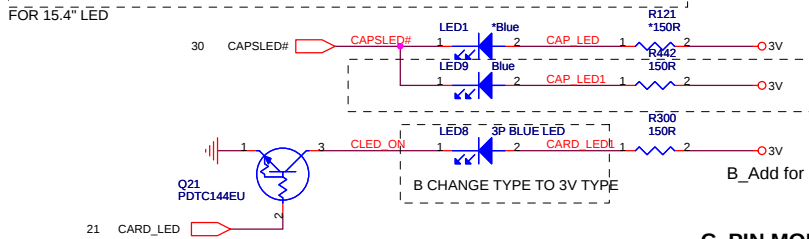


FOR POWER ON SW BOARD

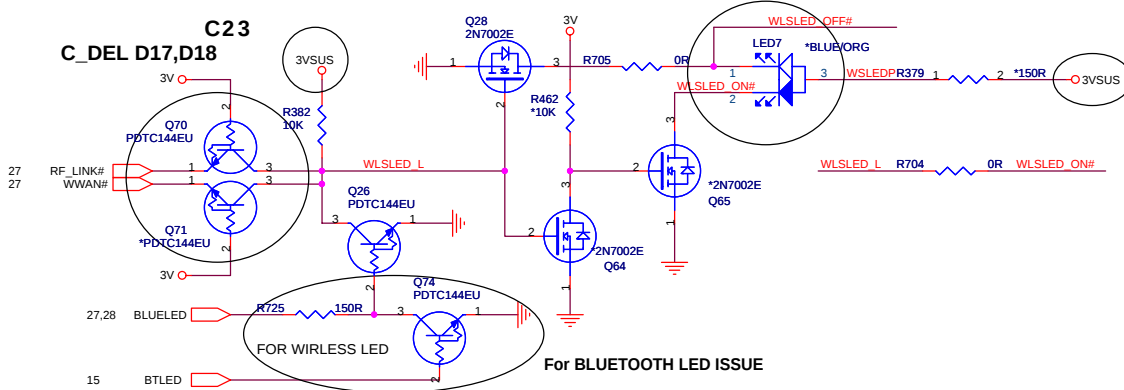
B_Modify POWER LED control circuit



FOR 15.4" LED

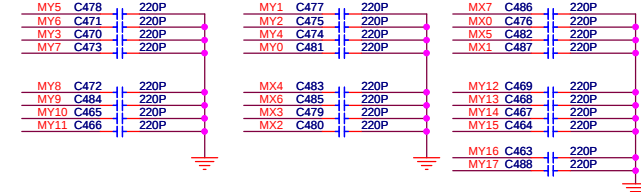


PIN MODIFY

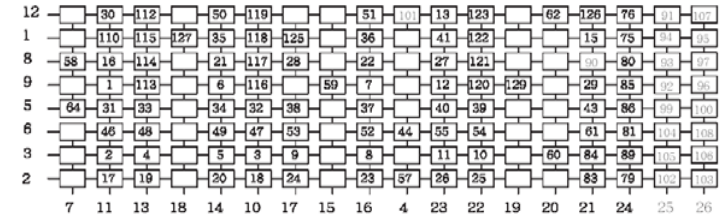
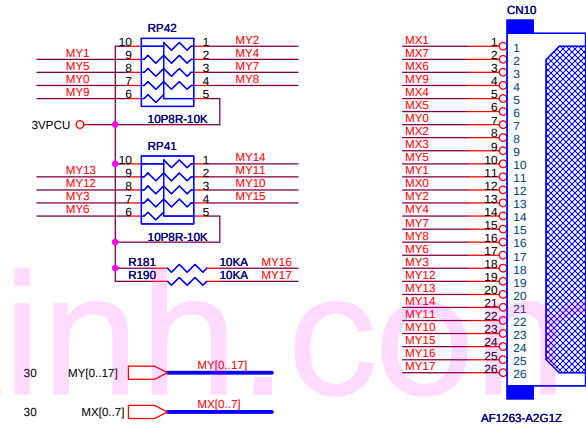


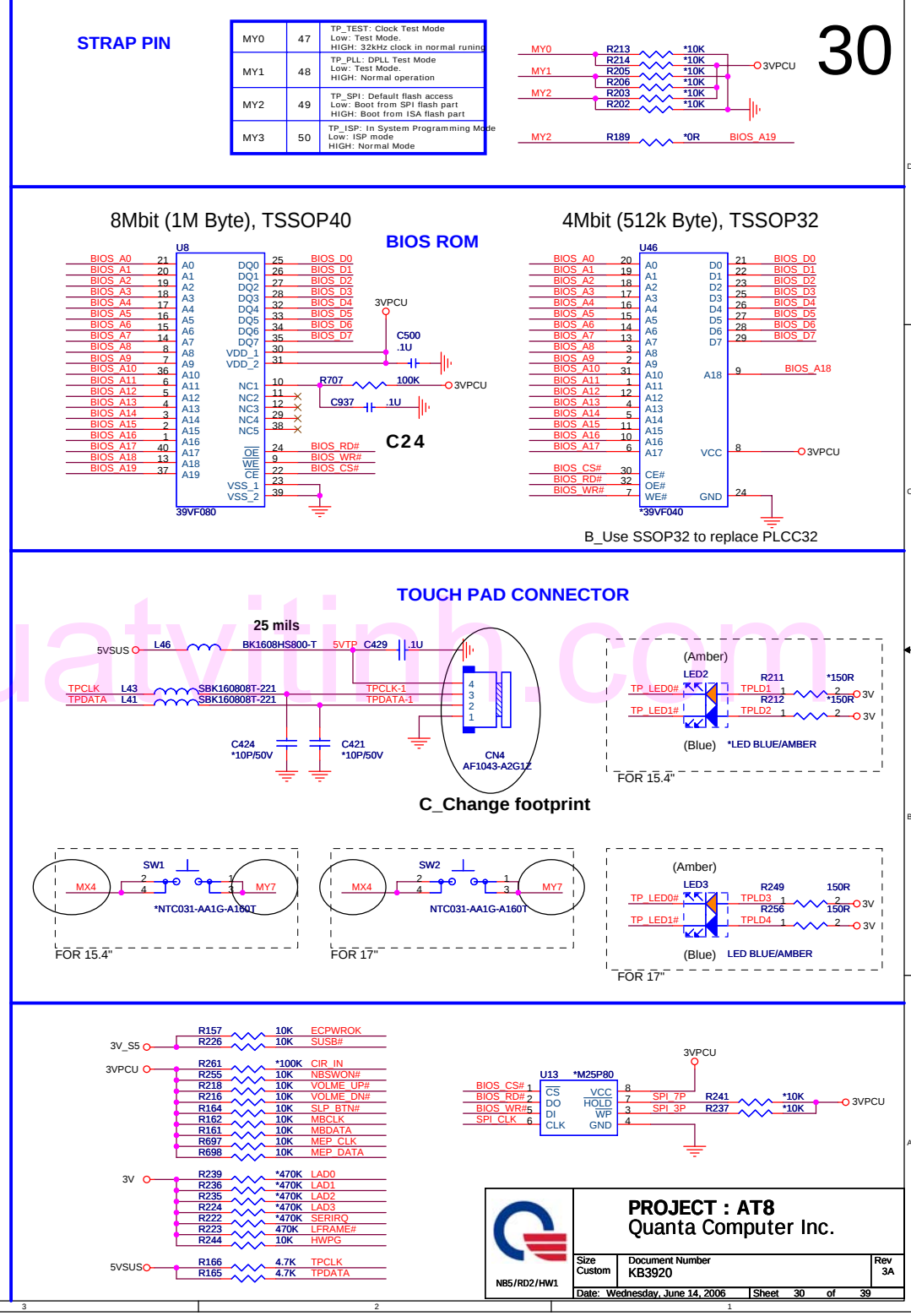
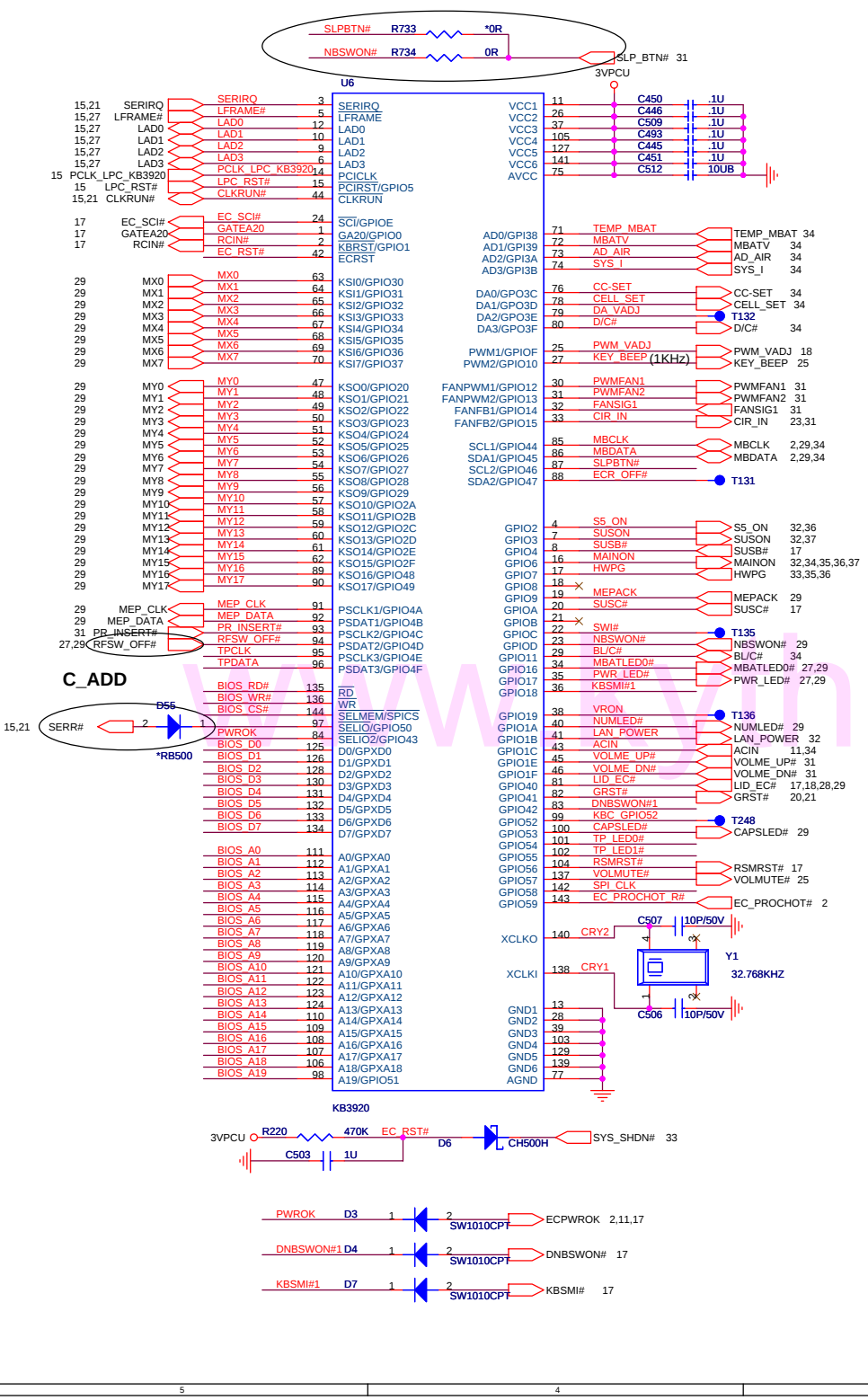
C23
C_DEL D17,D18

PIN MODIFY

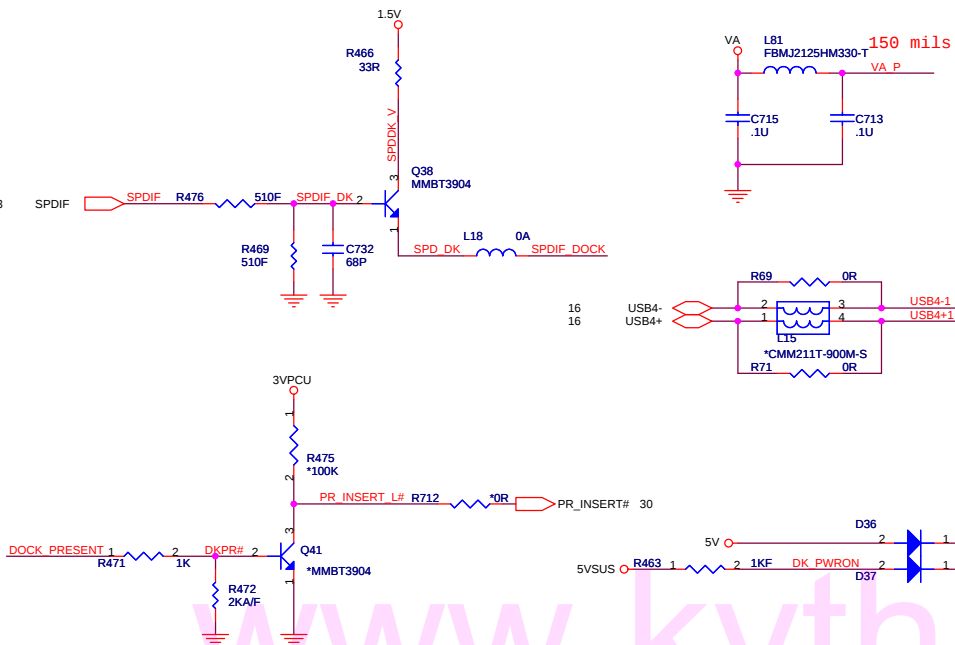


KEYBOARD PULL-UP

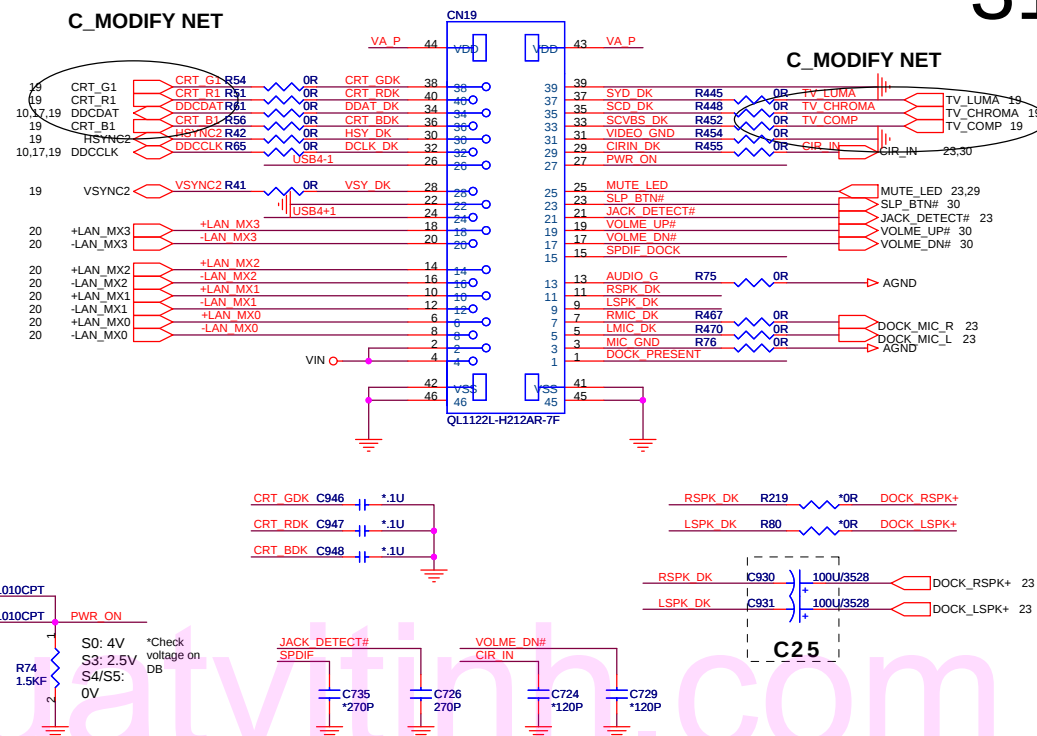




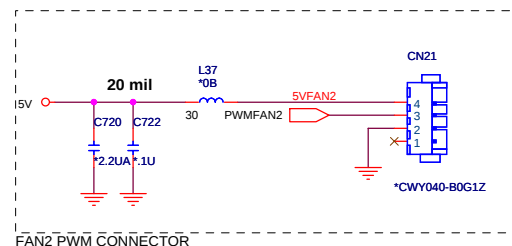
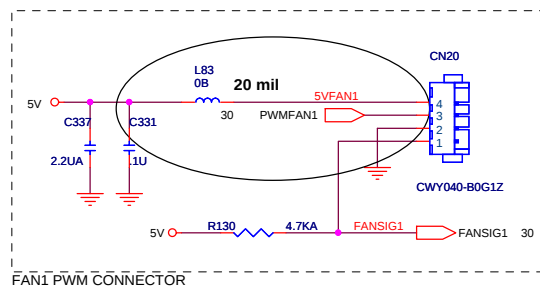
CABLE DOCK



C_MODIFY NET

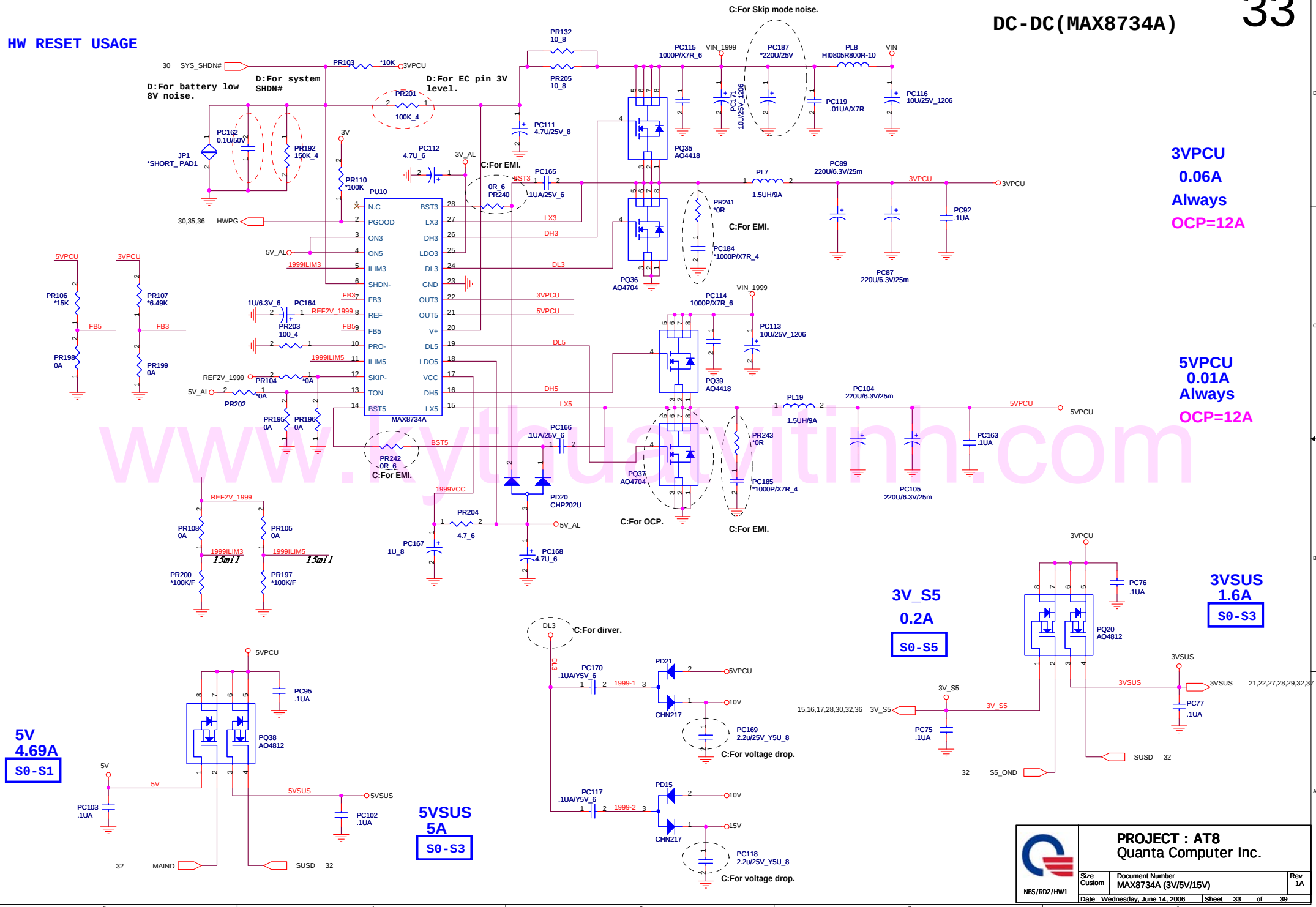


FAN



DC-DC (MAX8734A)

HW RESET USAGE



Adapter
19V/3.4A/65W
4.75A/90W

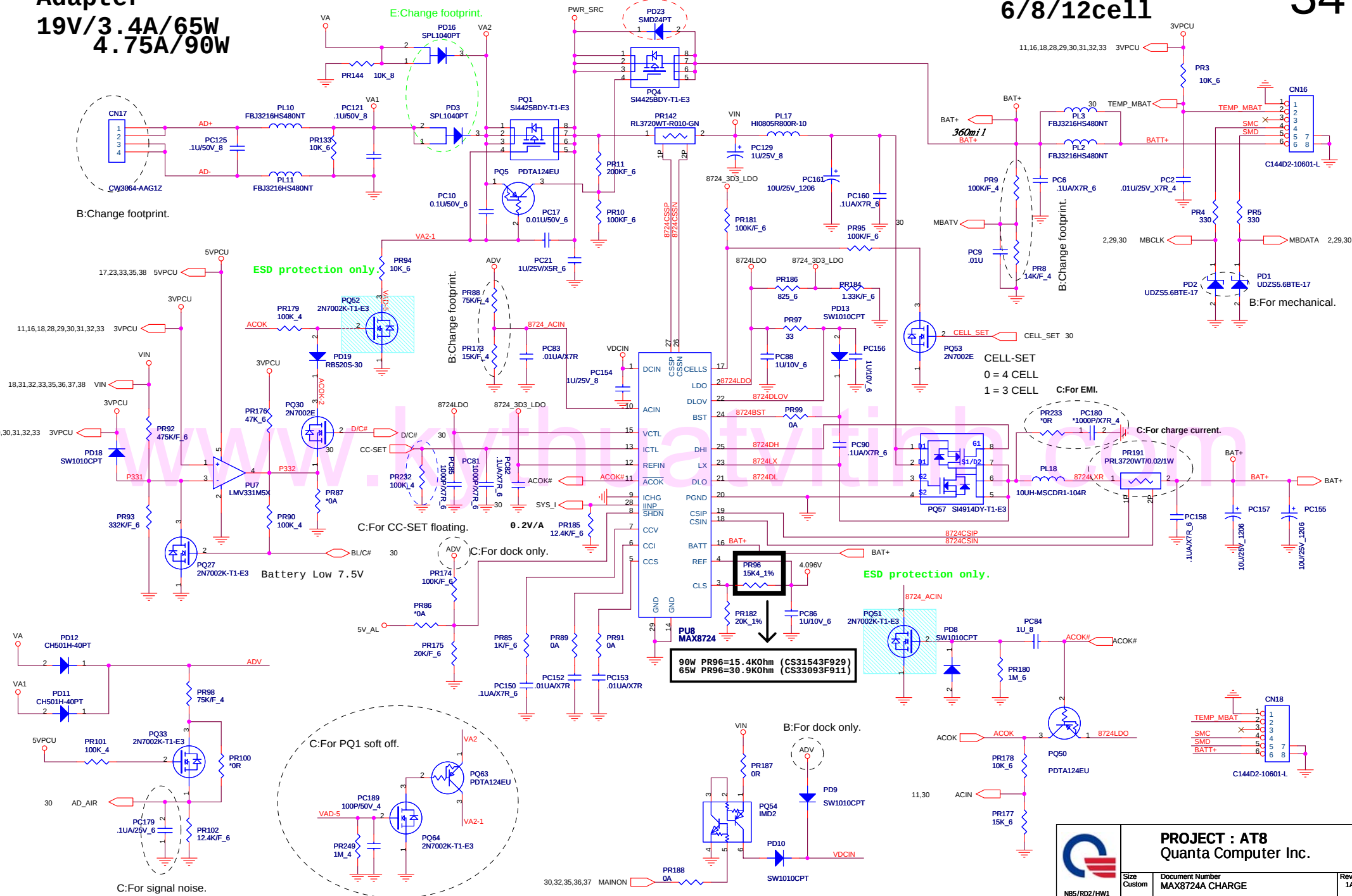
From Docking CNN

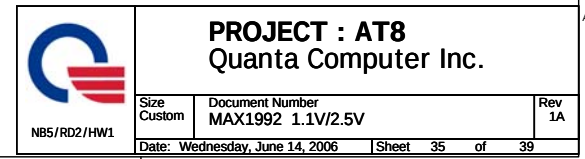
D:For discharge current.

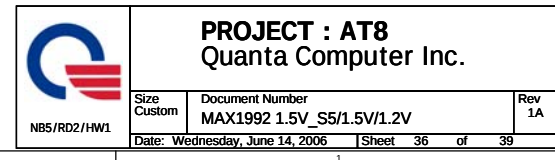
MAX8724A

Battery
6/8/12cell

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1.8VSUS
9.1A

S0-S3

1.8 Volt +/-5%
Design Current:15.0A
OCP: Max. 18.0A

C:For voltage drop.

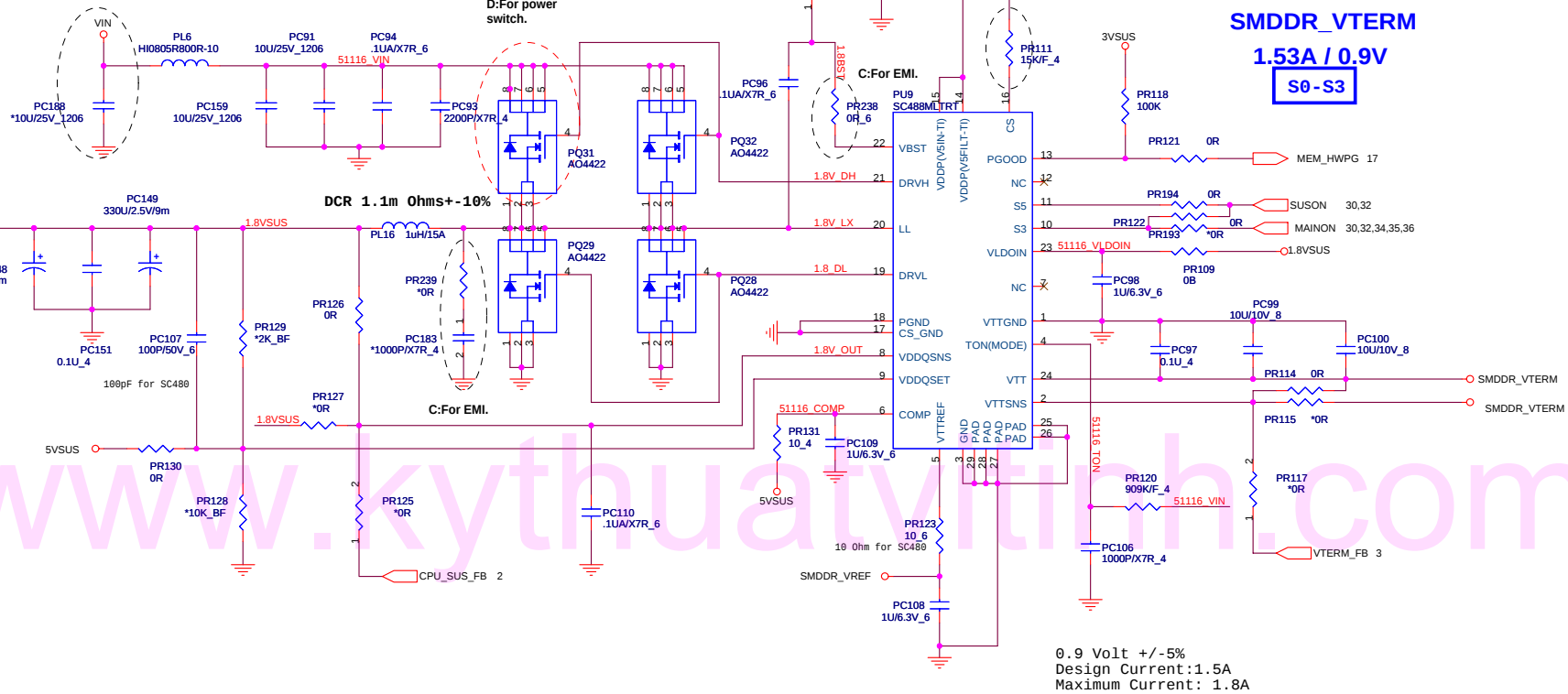
D:For power switch.

B:For OCP set.

SMDDR_VTERM

1.53A / 0.9V

S0-S3

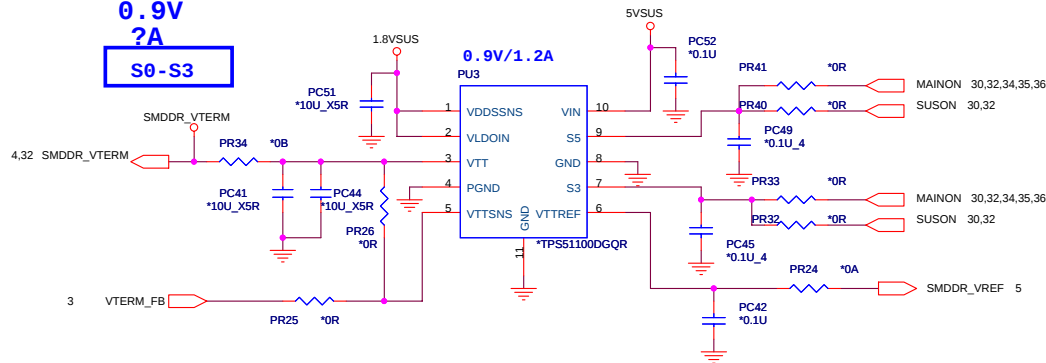


SMDDR_VTERM

0.9V

?A

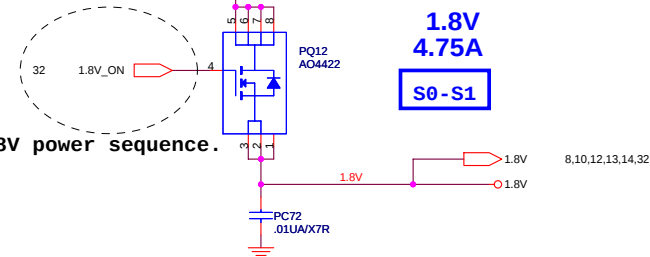
S0-S3



C:For 1.8V power sequence.

1.8V
4.75A

S0-S1



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