

PCB STACK UP

6L Dis.

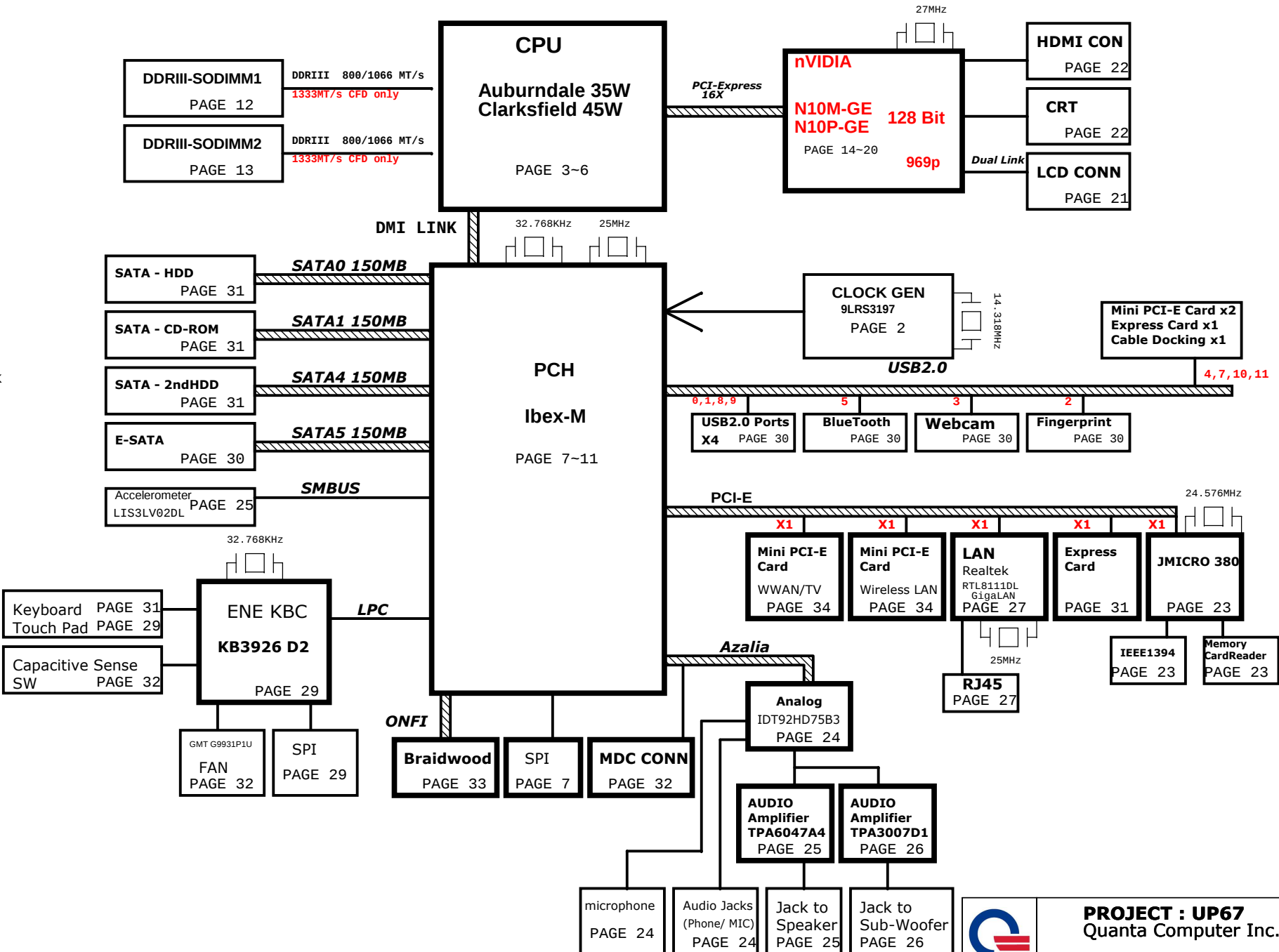
Jones/Cujo 2.0 (UP6/7) BLOCK DIAGRAM

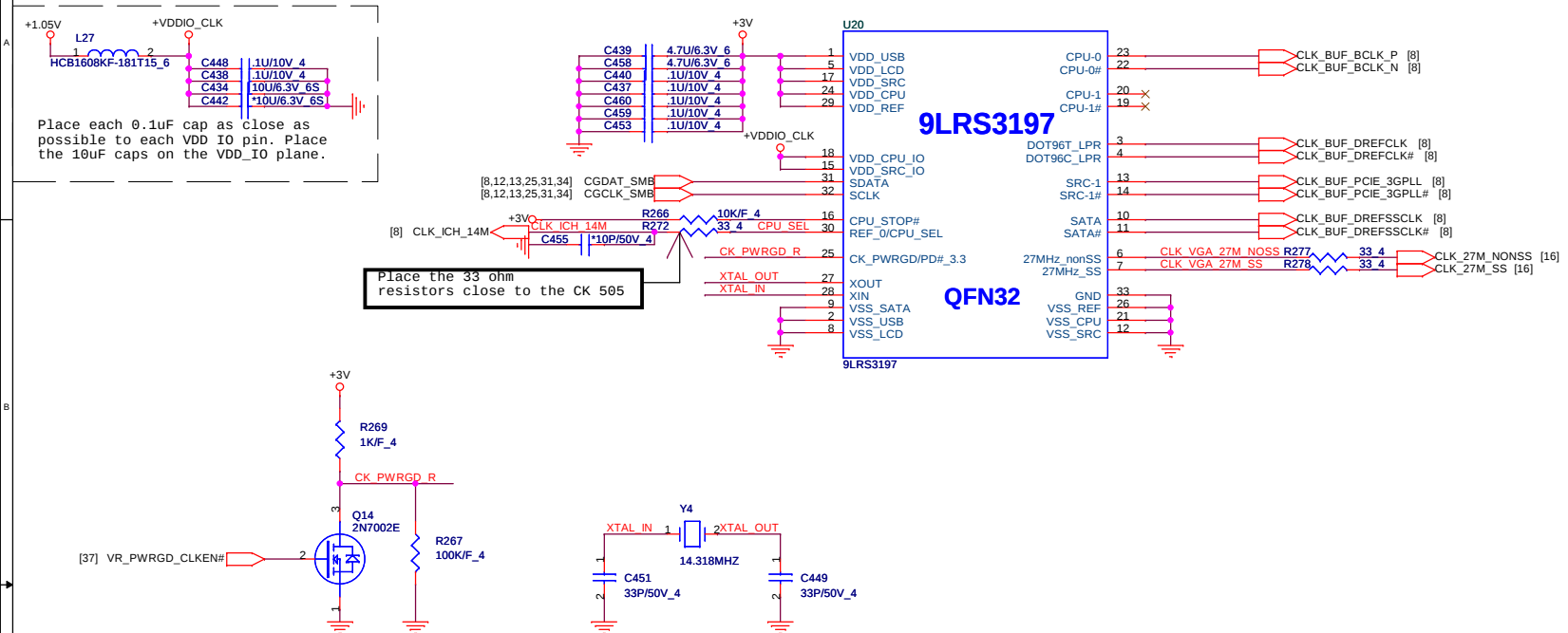
01

- LAYER 1 : TOP
- LAYER 2 : SGND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : SVCC
- LAYER 6 : BOT

- Cable Docking**
- VGA
 - RJ-45
 - CIR/Pwr btn
 - SPDIF Out
 - Stereo MIC
 - Headphone Jack
 - USB Port
 - VOL Cntr
- PAGE 32

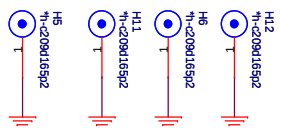
- SYSTEM POWER RT8206B PAGE 35
- VCCP +1.1VTT(RT8208A) AND PCH 1.05V(RT8204) PAGE 36
- CPU CORE ISL6251A PAGE 41
- VGACORE(1.025V) RT8208A PAGE 38
- DDR III SMD DR_VTERM 1.5V/1.5VSUS(RT8207) PAGE 39
- SYSTEM CHARGER(ISL6251AHAZ-T) PAGE 40



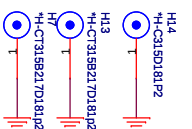


	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

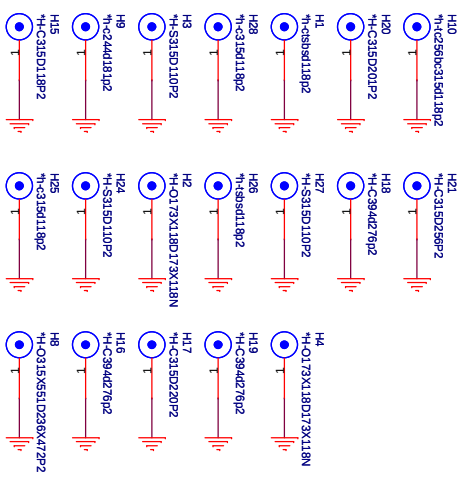
CPU bracket Hole.



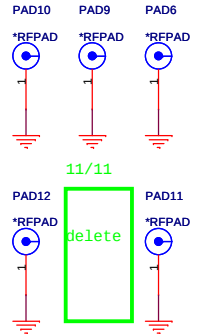
VGA bracket Hole.



M/B Screw Hole



RF PAD



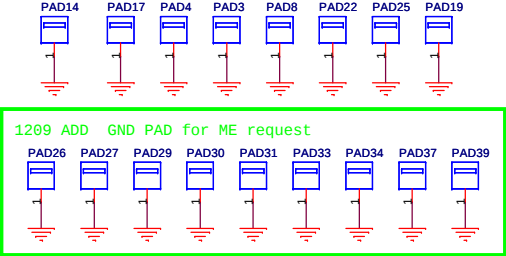
ME PAD



Routed spring

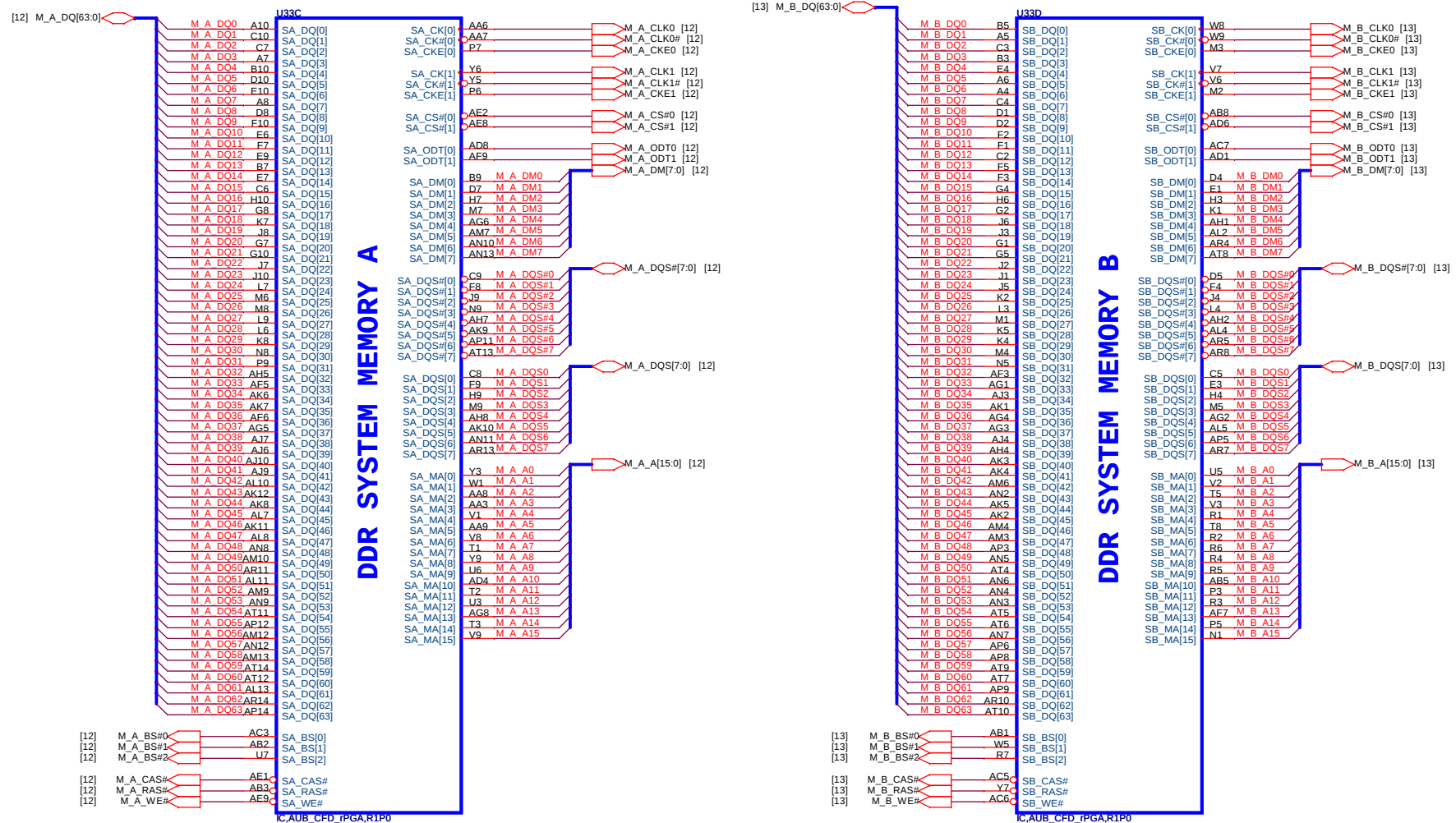


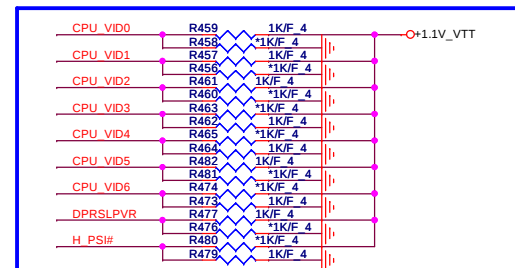
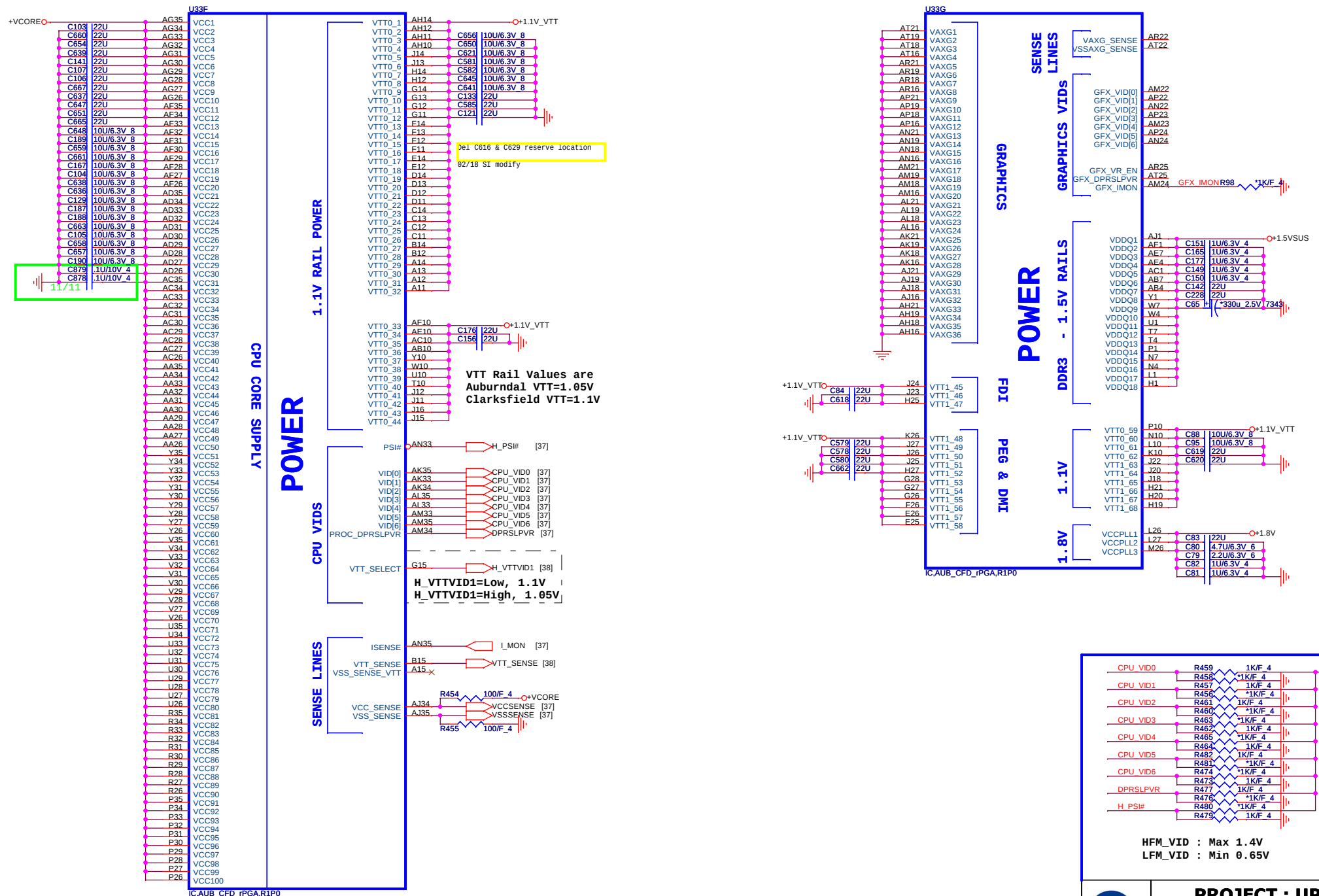
ME-Ground Pad





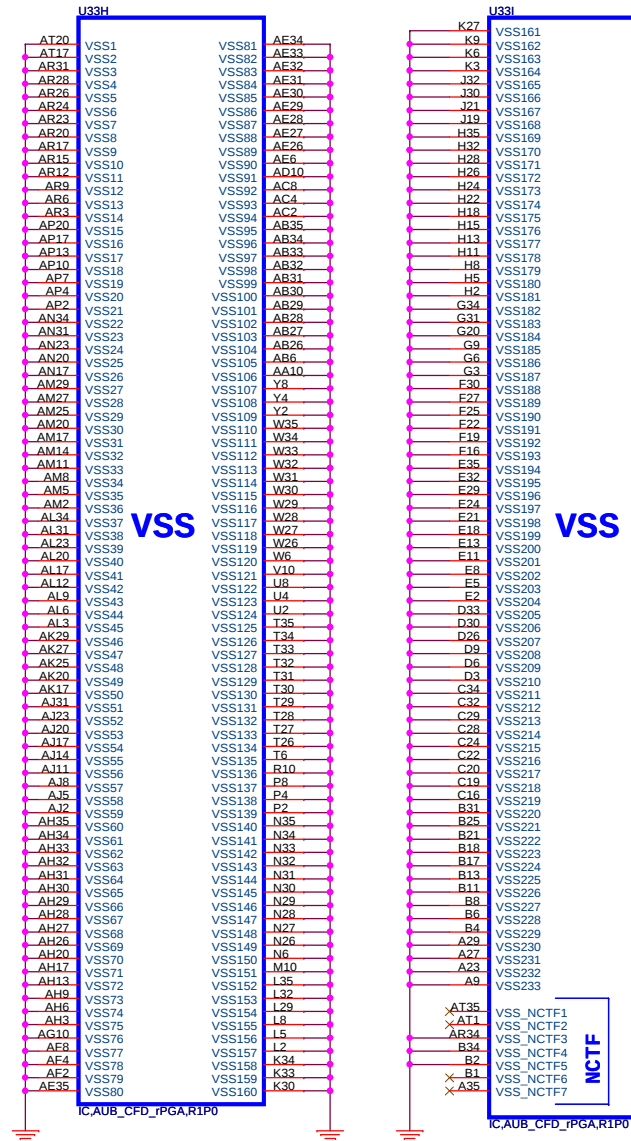
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)





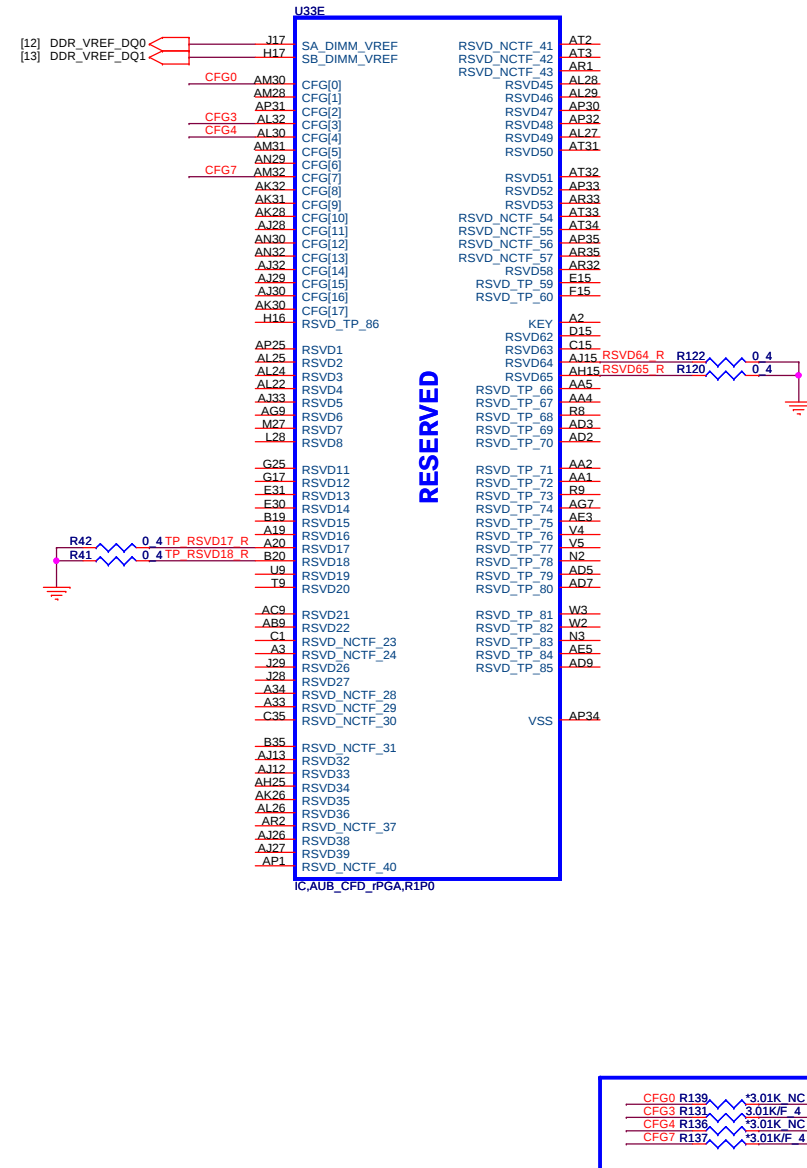
HFM_VID : Max 1.4V
LFM_VID : Min 0.65V

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01k $\pm$ 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



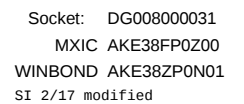
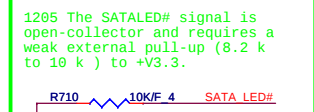
	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0 , 14 -> 1

```
CFG[ 1:0 ] - PCI_Epress Configuration Select
* 11= 1 x 16 PEG
* 10= 2 x 8 PEG
```



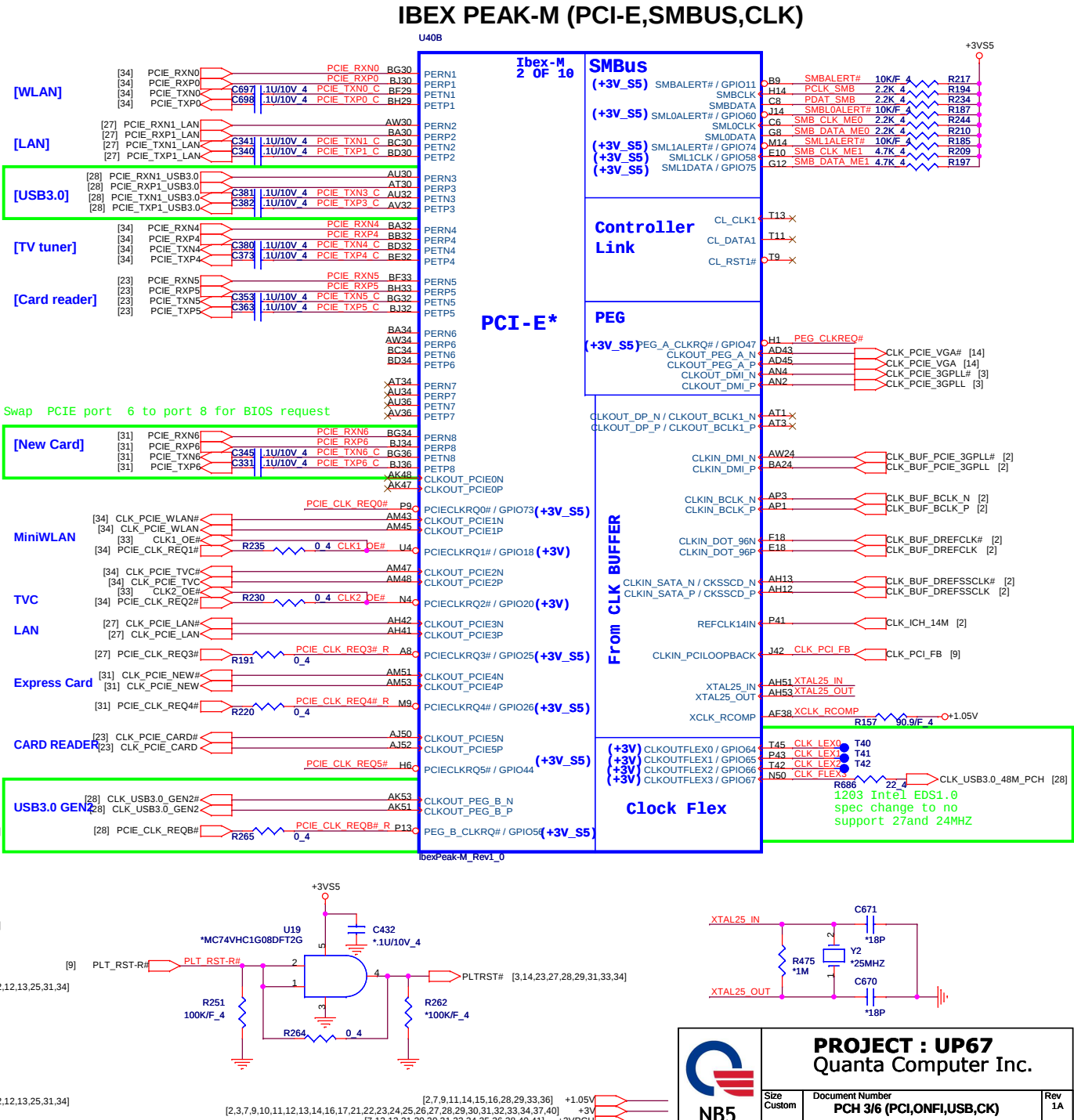
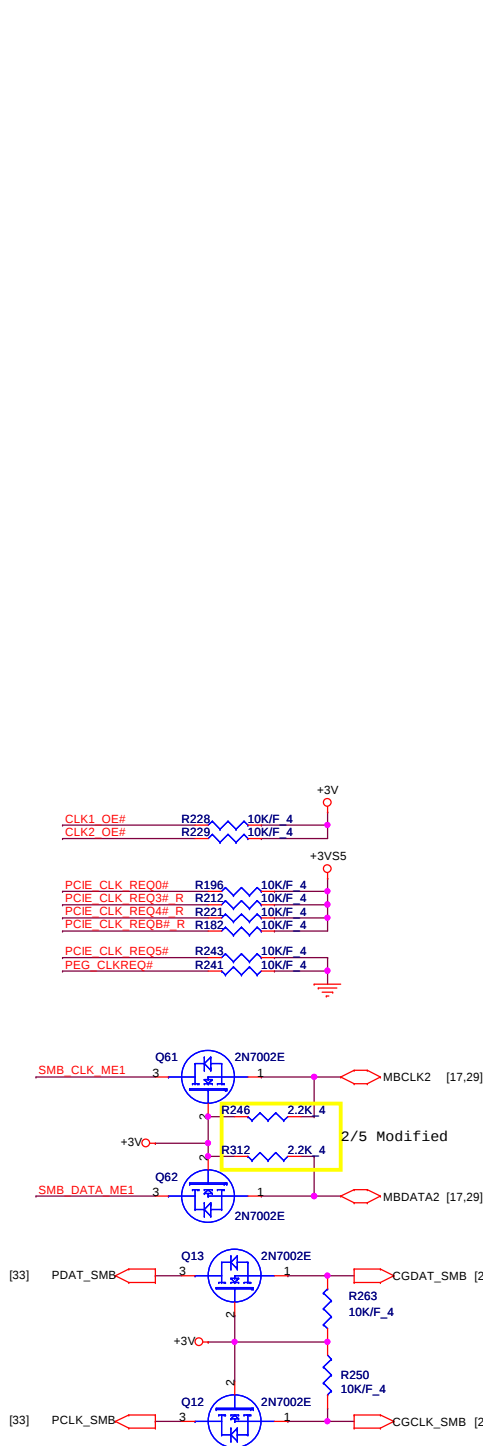
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Size Custom	Document Number PROCESSER 4/4(GND)	Rev 1A
Date: Friday, February 27, 2009	Sheet 6 of 45	

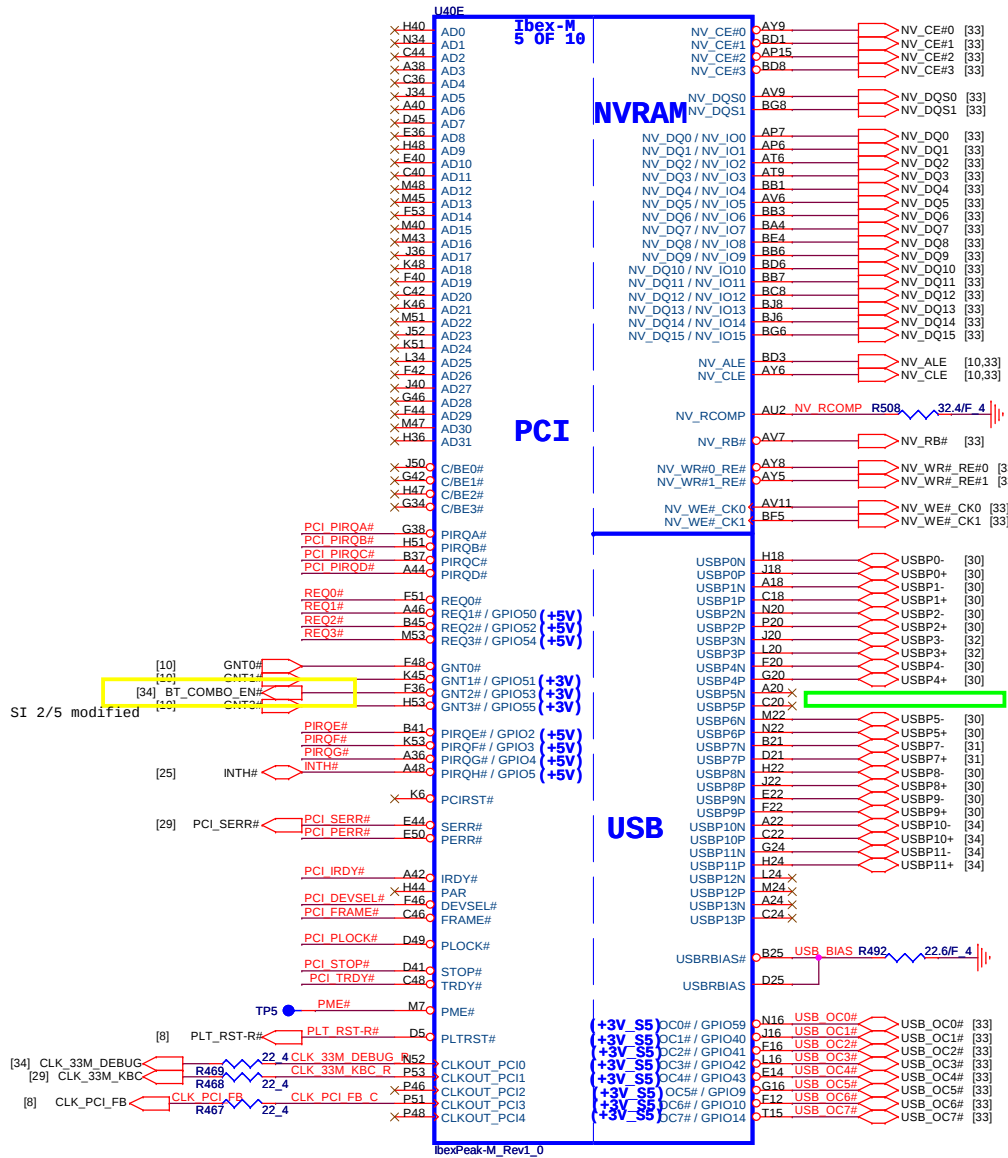


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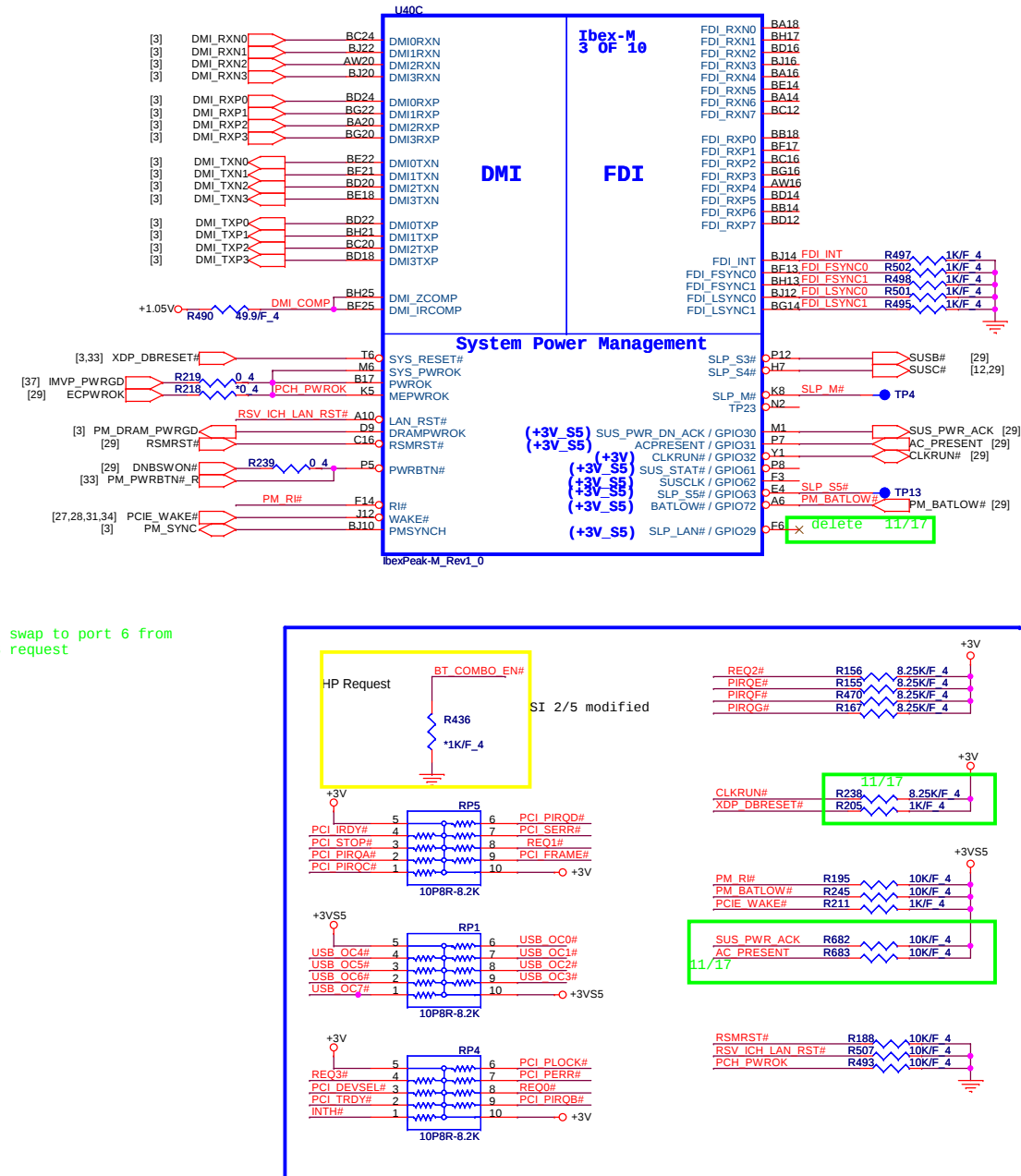
Size Custom	Document Number PCH 2/6 (SATA,HDA,LPC)	Rev 1A
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IBEX PEAK-M (PCI,USB,NVRAM)

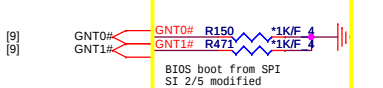
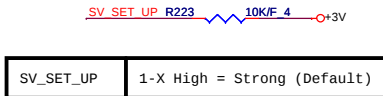
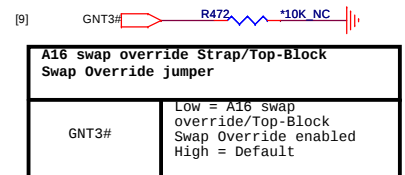
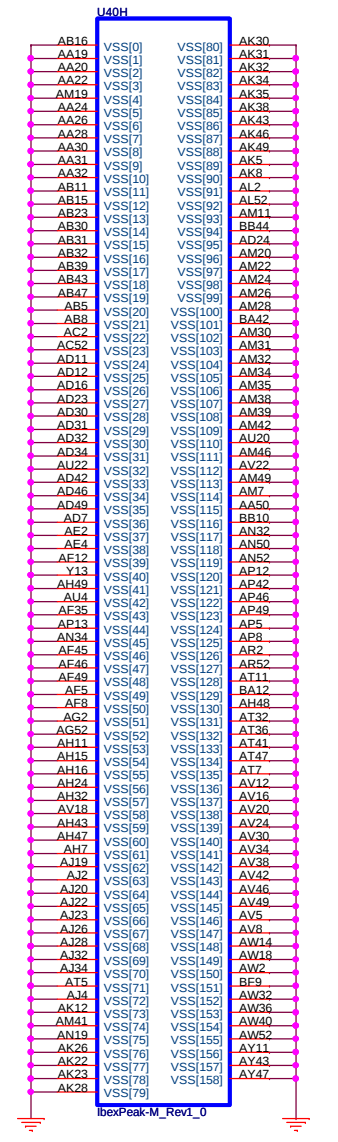


IBEX PEAK-M (DMI,FDI,GPIO)



IBEX PEAK-M (GND)

10



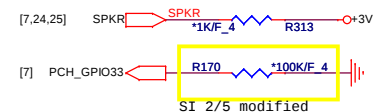
Boot BIOS Strap		
PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI



Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable

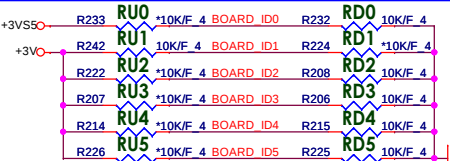
DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

No Reboot Strap



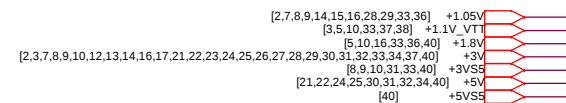
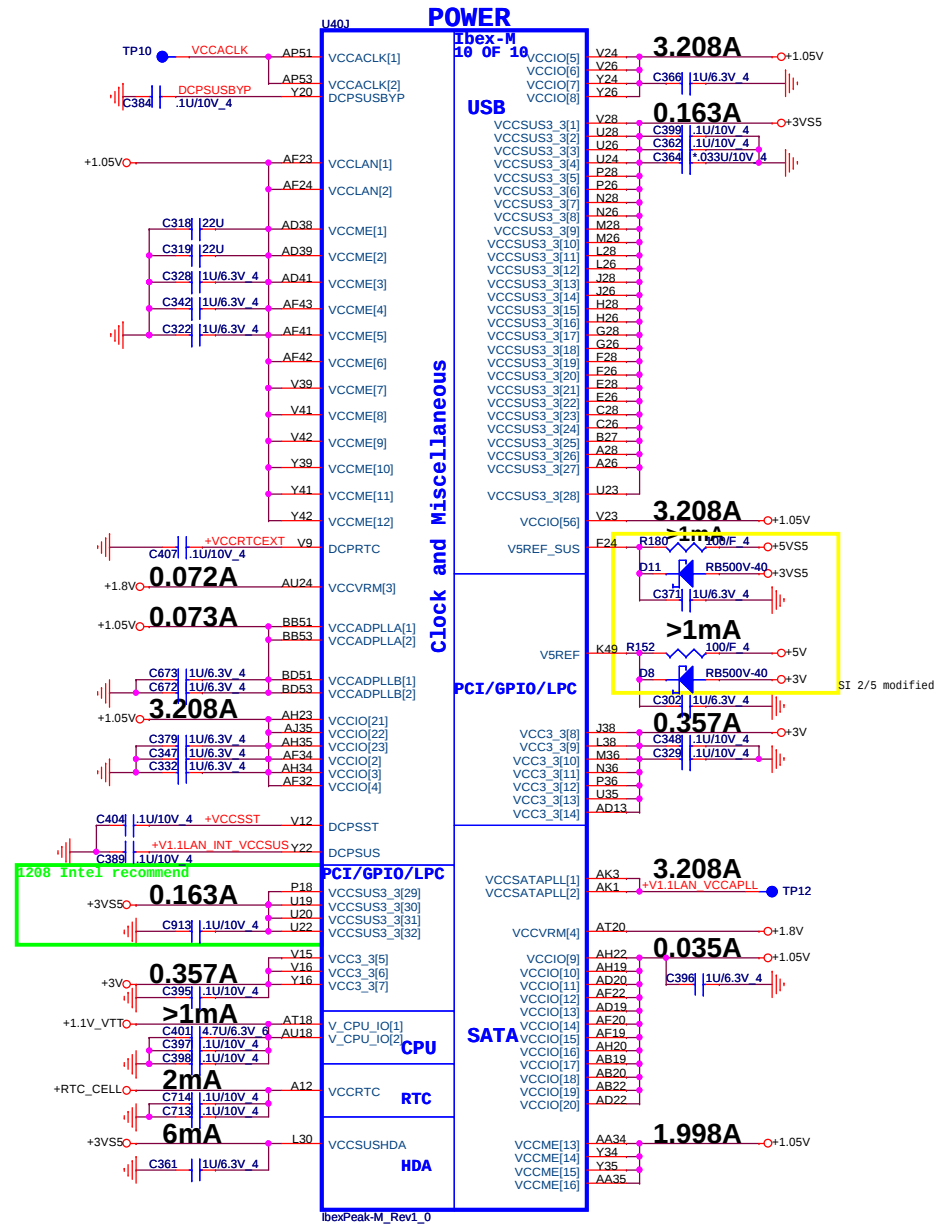
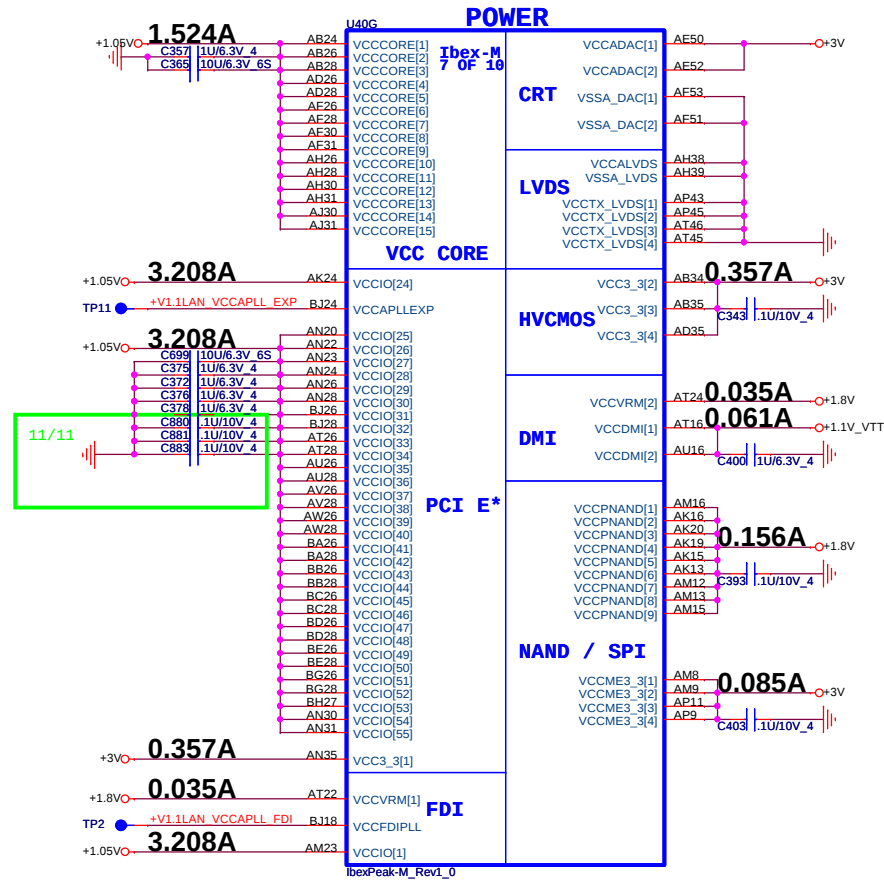
Board ID	ID0	ID1	ID2	ID3	ID4	ID5
UP6/7	0=UP6 1=UP7					
UMA/Dis.		0=UMA 1=Dis.				
Project name			00=Jones/Cujo 2.0 (Clarksfield) 10=Jones/Cujo 2.1 (Auburdale UMA)			
ROM Size					0= 2M 1= 4M	

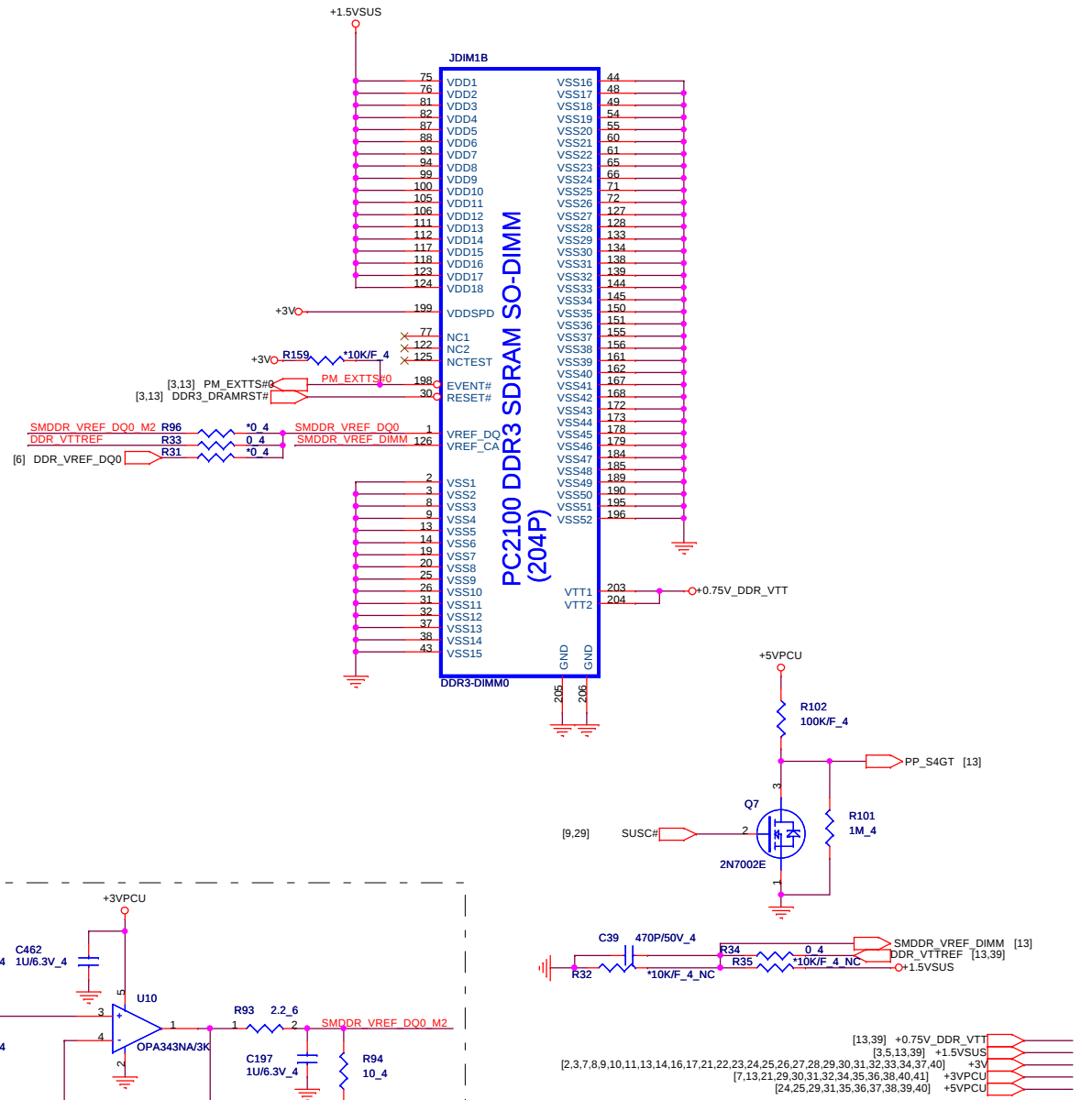
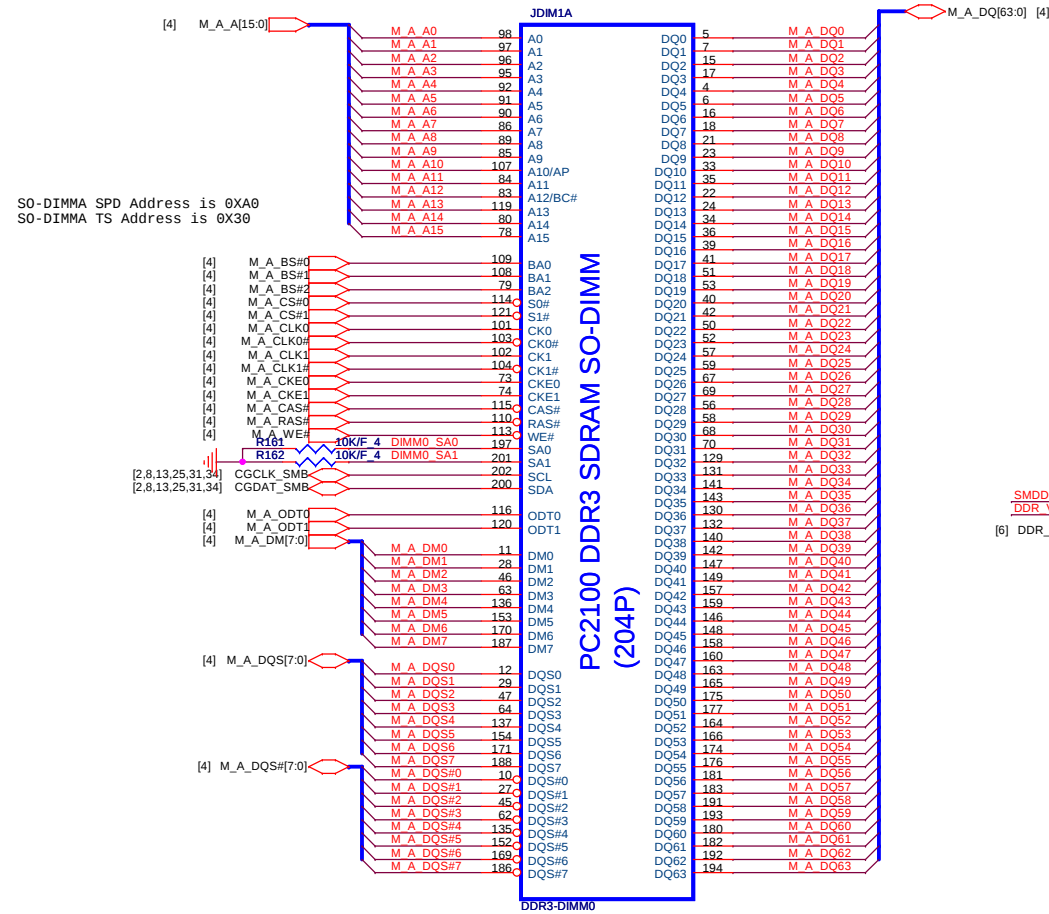
Board ID	ID5	ID4	ID3	ID2	ID1	ID0
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RD1 (0)	RU0 (1)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RU1 (1)	RD0 (0)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RU1 (1)	RU0 (1)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RD1 (0)	RD0 (0)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RD1 (0)	RU0 (1)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RU1 (1)	RD0 (0)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RU1 (1)	RU0 (1)



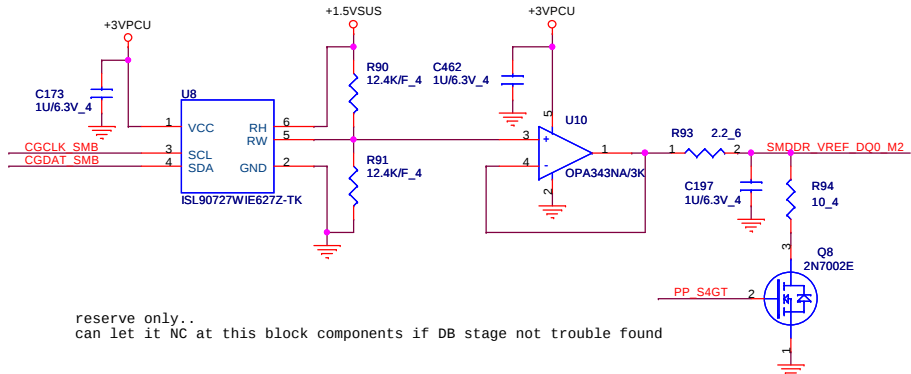
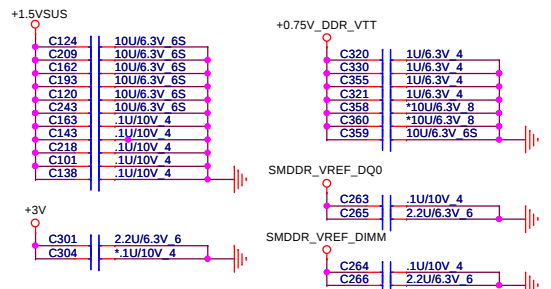
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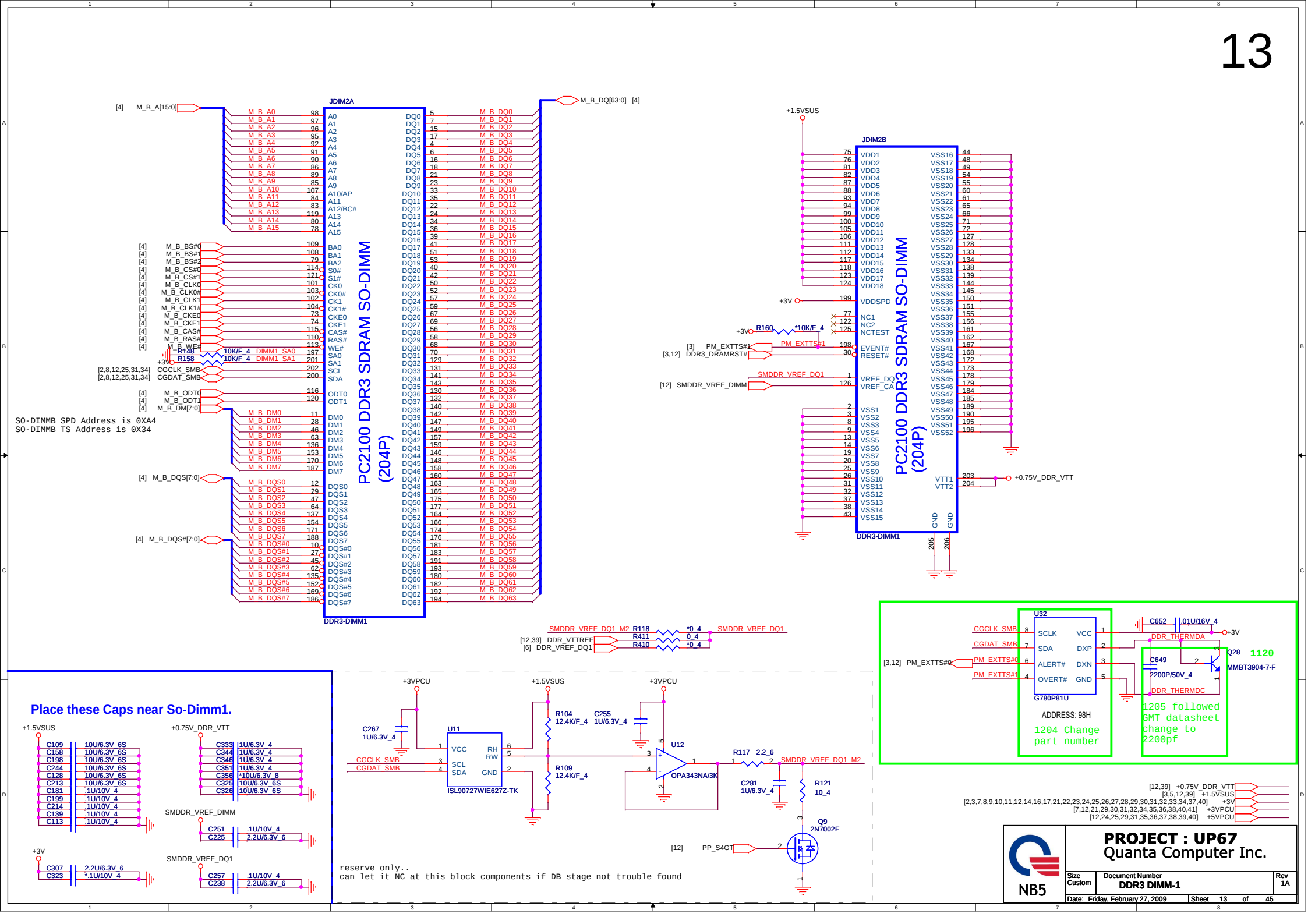
Size Custom	Document Number PCH 4/6 (GPIO & Strap)	Rev 1A
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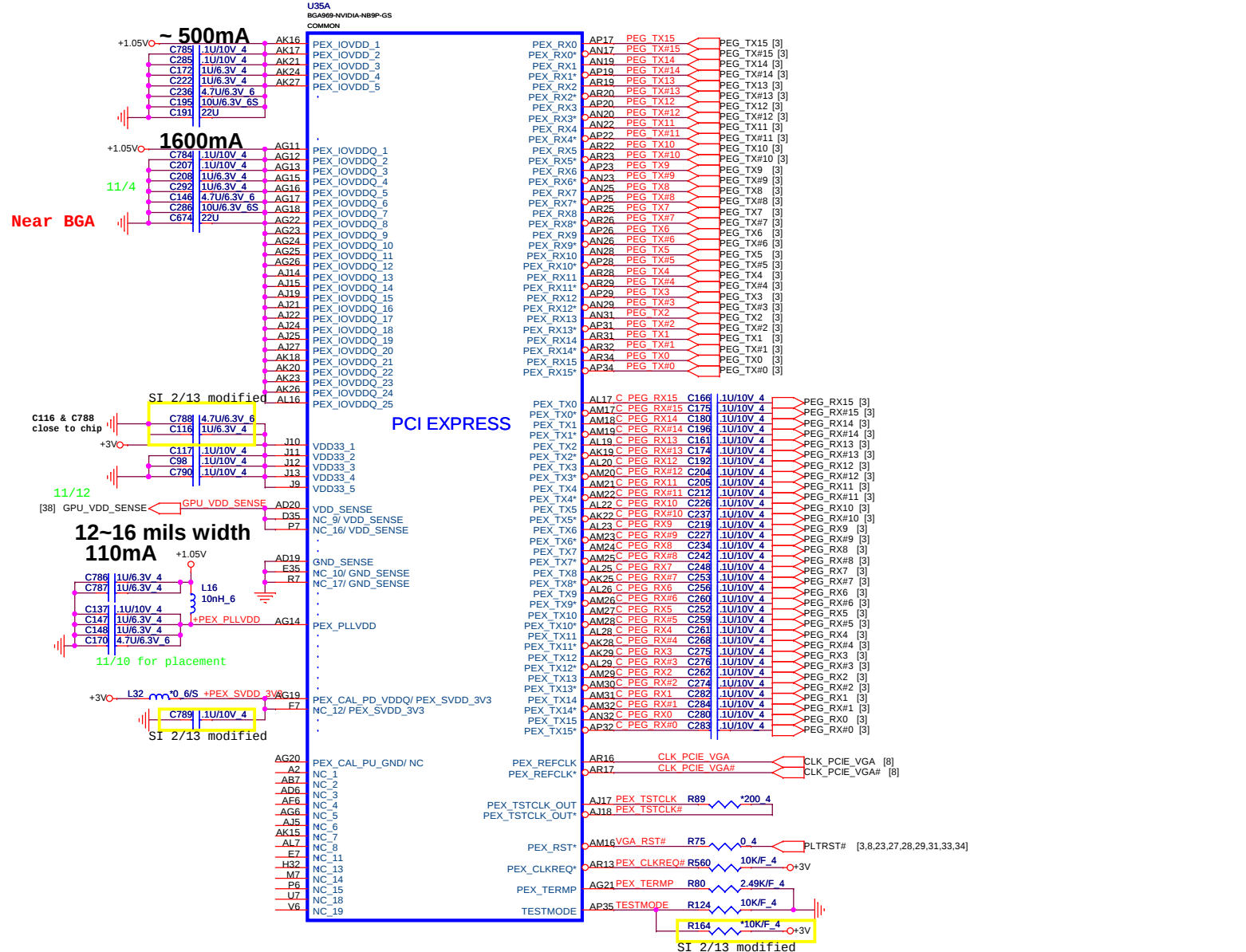


Place these Caps near So-Dimm0.

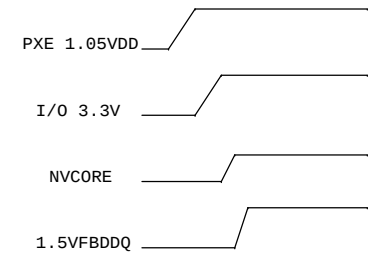




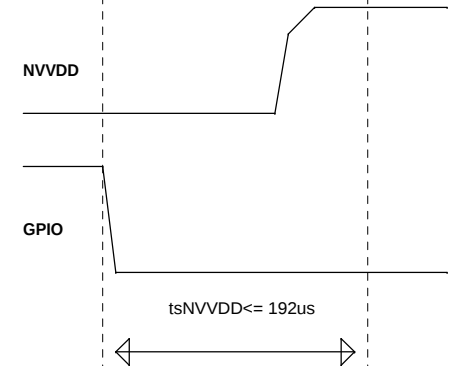
PEX_IOVDD+PEX_IOVDDQ+PEX_PLLVDD > 2.2A



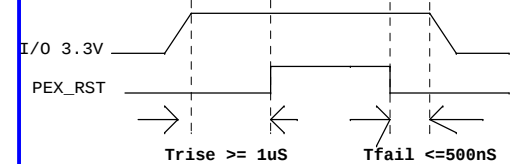
power up sequence



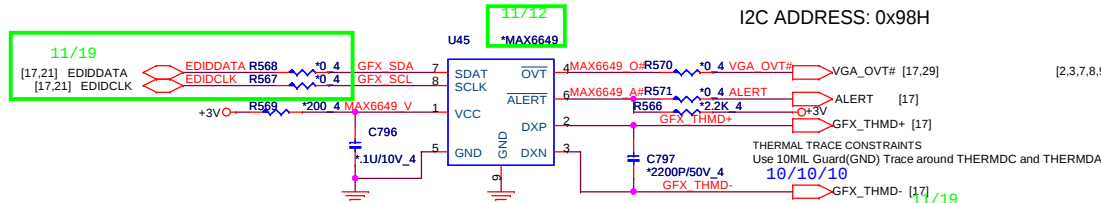
NB9M: VGACORE +0.90V (Normal) , +1.09V
NVVDD Maximum Settling Time



PEX_RST timing



VGA Thermal Circuit



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U35B

BGA669-NVIDIA-NB9P-GS
COMMON12/02 modify
package for N10

[19] FBA_CMD0 V32 FBA_CMD0
[19] FBA_CMD1 W31 FBA_CMD1
[19] FBA_CMD2 Y32 FBA_CMD2
[19] FBA_CMD3 AB35 FBA_CMD3
[19] FBA_CMD4 AB34 FBA_CMD4
[19] FBA_CMD5 W35 FBA_CMD5
[19] FBA_CMD6 W33 FBA_CMD6
[19] FBA_CMD7 W30 FBA_CMD7
[19] FBA_CMD8 T34 FBA_CMD8
[19] FBA_CMD9 T35 FBA_CMD9
[19] FBA_CMD10 T35 FBA_CMD10
[19] FBA_CMD11 AB31 FBA_CMD11
[19] FBA_CMD12 Y30 FBA_CMD12
[19] FBA_CMD13 Y32 FBA_CMD13
[19] FBA_CMD14 AA30 FBA_CMD14
[19] FBA_CMD15 AA32 FBA_CMD15
[19] FBA_CMD16 Y33 FBA_CMD16
[19] FBA_CMD17 U32 FBA_CMD17
[19] FBA_CMD18 Y31 FBA_CMD18
[19] FBA_CMD19 U34 FBA_CMD19
[19] FBA_CMD20 Y35 FBA_CMD20
[19] FBA_CMD21 W34 FBA_CMD21
[19] FBA_CMD22 Y30 FBA_CMD22
[19] FBA_CMD23 U35 FBA_CMD23
[19] FBA_CMD24 U30 FBA_CMD24
[19] FBA_CMD25 U33 FBA_CMD25
[19] FBA_CMD26 AB30 FBA_CMD26
[19] FBA_CMD27 AB33 FBA_CMD27
[19] FBA_CMD28 T33 FBA_CMD28
[19] FBA_CMD29 W29 FBA_CMD29
[19] FBA_CMD30 FBA_CMD30

12/02 modify
package for N10

VMA_DM0 P32 FBA_DQM0
VMA_DM1 H34 FBA_DQM1
VMA_DM2 J30 FBA_DQM2
VMA_DM3 P30 FBA_DQM3
VMA_DM4 AF32 FBA_DQM4
VMA_DM5 AL32 FBA_DQM5
VMA_DM6 AL34 FBA_DQM6
VMA_DM7 AF35 FBA_DQM7
VMA_WDQS0 L34 FBA_DQS_WP0
VMA_WDQS1 H35 FBA_DQS_WP1
VMA_WDQS2 J32 FBA_DQS_WP2
VMA_WDQS3 N31 FBA_DQS_WP3
VMA_WDQS4 AE31 FBA_DQS_WP4
VMA_WDQS5 AJ32 FBA_DQS_WP5
VMA_WDQS6 AJ34 FBA_DQS_WP6
VMA_WDQS7 AC33 FBA_DQS_WP7
VMA_RDQS0 L35 FBA_DQS_RN0
VMA_RDQS1 G35 FBA_DQS_RN1
VMA_RDQS2 H31 FBA_DQS_RN2
VMA_RDQS3 N32 FBA_DQS_RN3
VMA_RDQS4 AD32 FBA_DQS_RN4
VMA_RDQS5 AJ31 FBA_DQS_RN5
VMA_RDQS6 AJ35 FBA_DQS_RN6
VMA_RDQS7 AC34 FBA_DQS_RN7

P29 FBA_WCK0
R29 FBA_WCK0_N
L28 FBA_WCK1
M29 FBA_WCK1_N
AG29 FBA_WCK2
AH29 FBA_WCK2_N
AD29 FBA_WCK3
AE29 FBA_WCK3_N

+1.5V

MEMORY I/F A

FBA_CLK0 T32 VMA_CLK0
FBA_CLK0# T31 VMA_CLK0#
FBA_CLK1 AC31 VMA_CLK1
FBA_CLK1# AC30 VMA_CLK1#

FB_VREF

For Debug only

FBA_DEBUG T30 FBA_DEBUG R110 *10K/F 4 +1.5V

FB_LLAVDD0 AG27 FB PLLAVDD L17 PB1Y60808T-301Y-N 6 +1.05V
FB_PLLAVDD0 AE27 C254 4.7U/6.3V 6 SI 2/13 modified
C171 1U/6.3V 4

Memory clk spread :
down 1.25% (
30-33KHZ)
use internal Vref, ext
divider no stuff

+1.5V

C145 0.01U/16V 4
C246 0.01U/16V 4
C687 0.01U/16V 4
C250 0.01U/16V 4
C258 1U/10V 4
C223 1U/10V 4
C653 1U/10V 4
C391 0.047U/16V 4
C655 0.047U/16V 4
C303 0.047U/16V 4
C800 4.7U/6.3V 6
C801 4.7U/6.3V 6

SI 2/13 modified

U35C

BGA669-NVIDIA-NB9P-GS
COMMON12/02 modify
package for N10

[20] FBC_CMD0 C17 FBC_CMD0
[20] FBC_CMD1 D18 FBC_CMD1
[20] FBC_CMD2 F21 FBC_CMD2
[20] FBC_CMD3 A23 FBC_CMD3
[20] FBC_CMD4 D21 FBC_CMD4
[20] FBC_CMD5 B23 FBC_CMD5
[20] FBC_CMD6 E20 FBC_CMD6
[20] FBC_CMD7 C21 FBC_CMD7
[20] FBC_CMD8 F20 FBC_CMD8
[20] FBC_CMD9 FBC_CMD9
[20] FBC_CMD10 F19 FBC_CMD10
[20] FBC_CMD11 F23 FBC_CMD11
[20] FBC_CMD12 A22 FBC_CMD12
[20] FBC_CMD13 B17 FBC_CMD13
[20] FBC_CMD14 F24 FBC_CMD14
[20] FBC_CMD15 C25 FBC_CMD15
[20] FBC_CMD16 E22 FBC_CMD16
[20] FBC_CMD17 C20 FBC_CMD17
[20] FBC_CMD18 B22 FBC_CMD18
[20] FBC_CMD19 A19 FBC_CMD19
[20] FBC_CMD20 D22 FBC_CMD20
[20] FBC_CMD21 FBC_CMD21
[20] FBC_CMD22 D20 FBC_CMD22
[20] FBC_CMD23 E19 FBC_CMD23
[20] FBC_CMD24 D19 FBC_CMD24
[20] FBC_CMD25 C19 FBC_CMD25
[20] FBC_CMD26 F22 FBC_CMD26
[20] FBC_CMD27 FBC_CMD27
[20] FBC_CMD28 C23 FBC_CMD28
[20] FBC_CMD29 B20 FBC_CMD29
[20] FBC_CMD30 A20 FBC_CMD30

12/02 modify
package for N10

VMC_DM0 A16 FBC_DQM0
VMC_DM1 D10 FBC_DQM1
VMC_DM2 F11 FBC_DQM2
VMC_DM3 D15 FBC_DQM3
VMC_DM4 D27 FBC_DQM4
VMC_DM5 D34 FBC_DQM5
VMC_DM6 A34 FBC_DQM6
VMC_DM7 D28 FBC_DQM7
VMC_WDQS0 C14 FBC_DQS_WP0
VMC_WDQS1 A10 FBC_DQS_WP1
VMC_WDQS2 E10 FBC_DQS_WP2
VMC_WDQS3 D14 FBC_DQS_WP3
VMC_WDQS4 F26 FBC_DQS_WP4
VMC_WDQS5 D32 FBC_DQS_WP5
VMC_WDQS6 A32 FBC_DQS_WP6
VMC_WDQS7 B26 FBC_DQS_WP7
VMC_RDQS0 B14 FBC_DQS_RN0
VMC_RDQS1 B10 FBC_DQS_RN1
VMC_RDQS2 D9 FBC_DQS_RN2
VMC_RDQS3 E14 FBC_DQS_RN3
VMC_RDQS4 F26 FBC_DQS_RN4
VMC_RDQS5 A31 FBC_DQS_RN5
VMC_RDQS6 A31 FBC_DQS_RN6
VMC_RDQS7 A26 FBC_DQS_RN7

G14 FBC_WCK0
G15 FBC_WCK0_N
G11 FBC_WCK1
G12 FBC_WCK1_N
G27 FBC_WCK2
G28 FBC_WCK2_N
G24 FBC_WCK3
G25 FBC_WCK3_N

+1.5V

MEMORY I/F C

FB_CAL_PD_VDDQ K27 FB_CAL_PD_VDDQ R98 40.2/F 4 +1.5V

FB_CAL_PU_GND L27 FB_CAL_PU_GND R100 40.2/F 4

FB_CAL_TERM_GND M27 FB_CAL_TERM_GND R107 40.2/F 4 12/16 Modified

FBC_DEBUG G19 FBC_DEBUG R92 *10K/F 4 +1.5V

NC/FB_LLAVDD1 J19

NC/FB_PLLAVDD1 J18

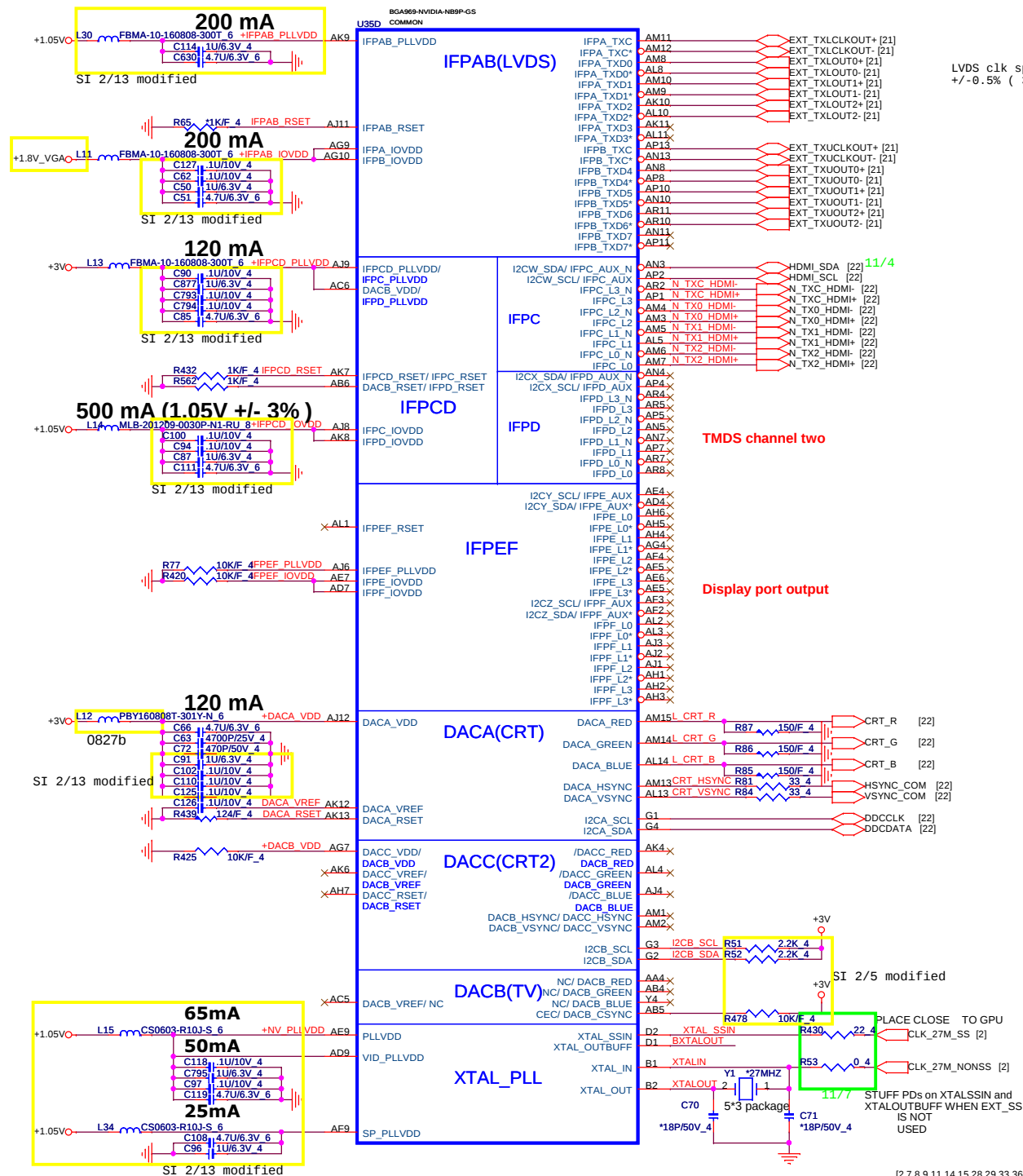
R92 no stuff



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[2,7,8,9,11,14,16,28,29,33,36] +1.05V
[19,20,31,34,36,39,40] +1.5V



LVDS clk spread : Center
+/-0.5% (30~33KHZ)

[2,7,8,9,11,14,15,28,29,33,36] +1.05V
[5,10,11,33,36,40] +1.8V
[2,3,7,8,9,10,11,12,13,14,17,21,22,23,24,25,26,27,28,29,30,31,32,33,34,37,40] +3V

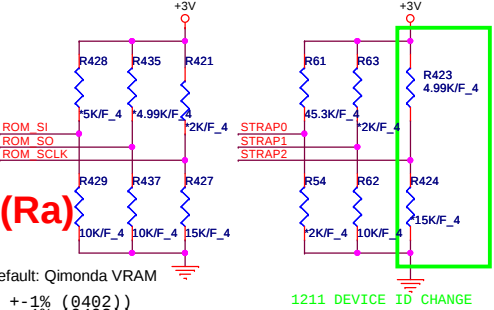


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SEE Datasheet for details on N10P Straps!

PCI_DEVID[4]/SUBVENDOR



CHIP	PCI_DEVID:	STRAP2
N10P-GE	0x0A28	1000 PU 5K
N10M-GE	0x0A68	1000 PU 5K

Logical Strap Bit Mapping		
	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

CS31002FB26 (RES CHIP 10K 1/16W +-1% (0402))
CS31502FB09 (RES CHIP 15K 1/16W +-1% (0402))
CS32002FB02 (RES CHIP 20K 1/16W +-1% (0402))

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO NB10X	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1000
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0001
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI
0000	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Reserved		
0001	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Qimonda	IDGH1G-04A1F1C-16X	PD 10K
0010	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Hynix	H5TQ1G63BFR-12C	PD 15K
0011	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Samsung	K4W1G1646E-EC12	PD 20K
0101		Reserved		
0110				
XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Hynix	H5TQ1G63AFR-14C	
XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Samsung	K4W1G1646D-EC12	

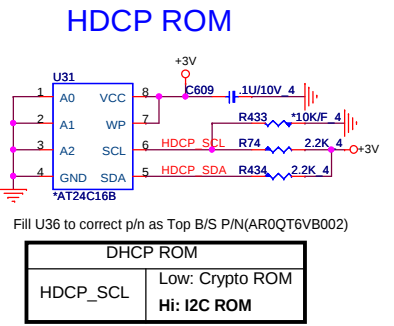
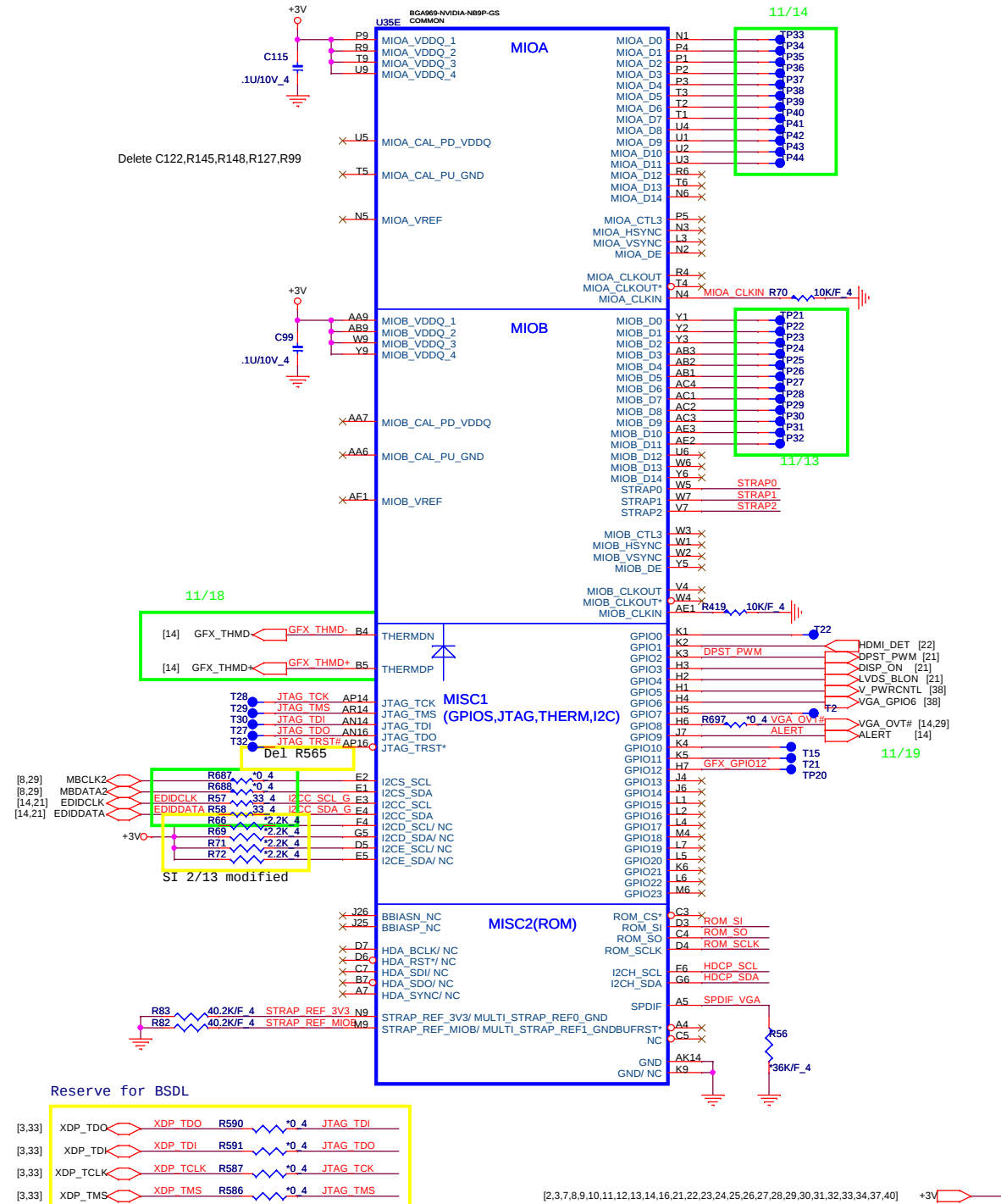
GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	NVVDD VID2 11/13
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL 11/13
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL



PROJECT : UP67
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N10X (GPIO & STRAPS) 4/5	2A
Date: Monday, March 02, 2009 Sheet 17 of 45		



DHCP ROM	
HDCP_SCL	Low: Crypto ROM Hi: I2C ROM



Del all VRAM termination (RP16-RP75)

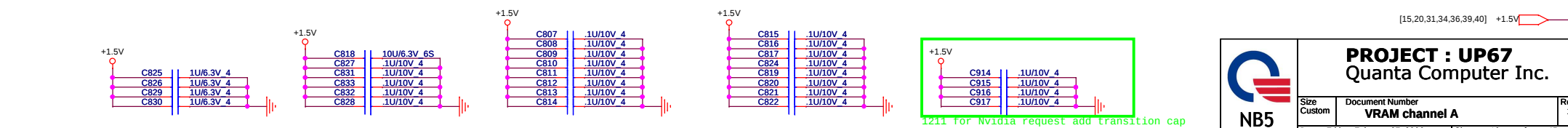
SI 2/5 modified



PROJECT : UP67
Quanta Computer Inc.

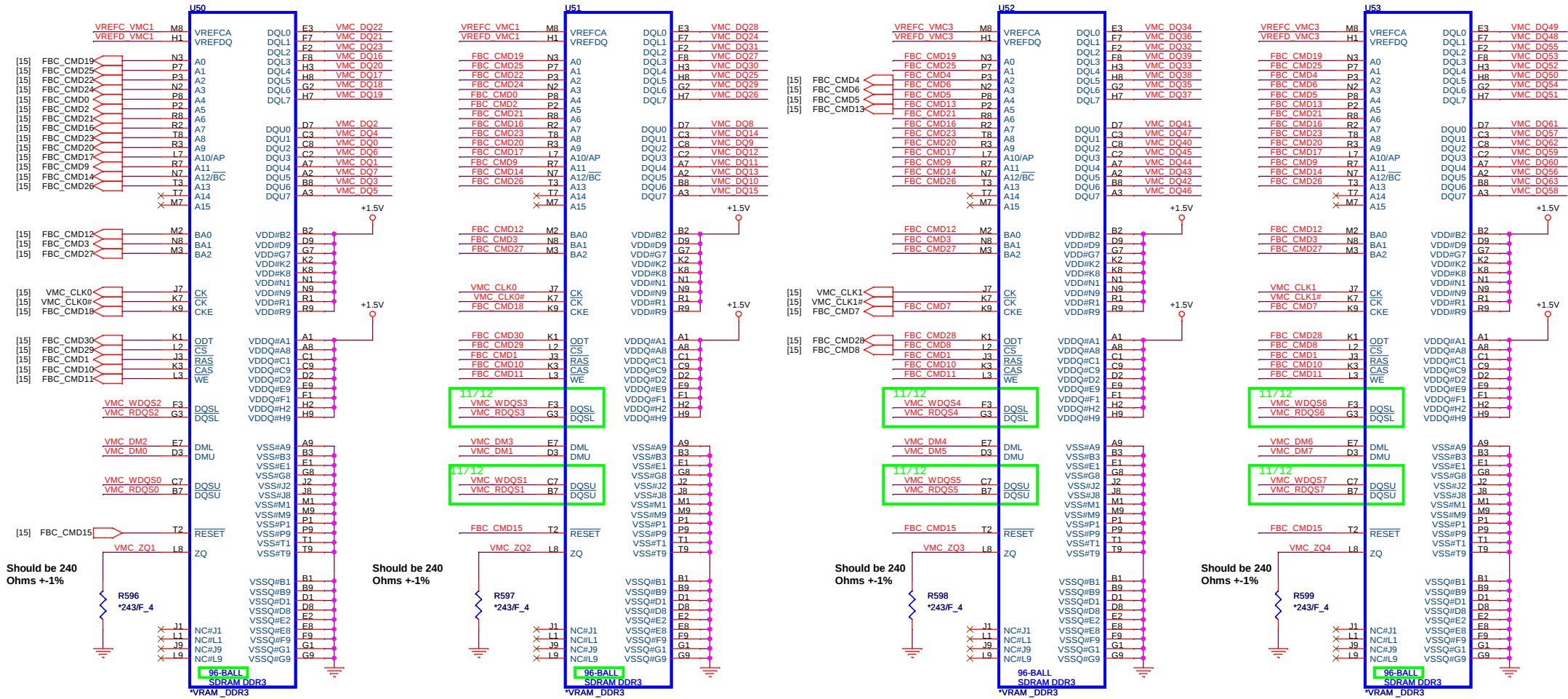
Size Custom	Document Number N10X (POWER & GND) 5/5	Rev 2A
Date: Friday, February 27, 2009		Sheet 18 of 45

[38] +VGACORE
[15,19,20,31,34,36,39,40] +1.5V



CHANNEL B: 256MB/512MB DDR3

[15] VMC_DQ[63..0]
[15] VMC_DM[7..0]
[15] VMC_WDQS[7..0]
[15] VMC_RDQS[7..0]



Should be 240 Ohms +-1%

R596 *243/F_4

96-BALL SDRAM DDR3

Should be 240 Ohms +-1%

R597 *243/F_4

96-BALL SDRAM DDR3

Should be 240 Ohms +-1%

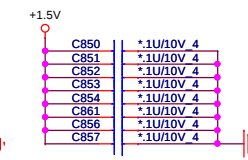
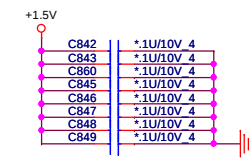
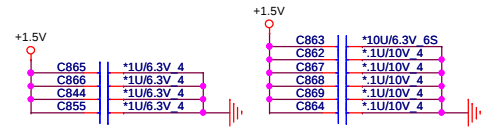
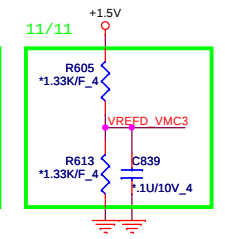
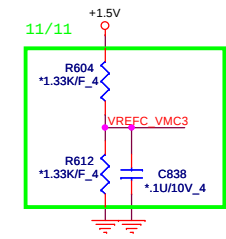
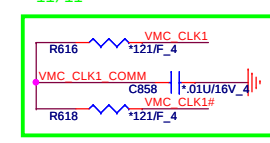
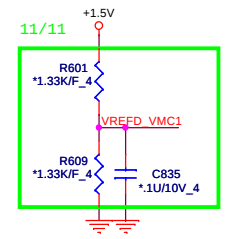
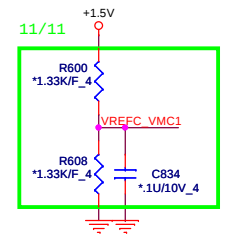
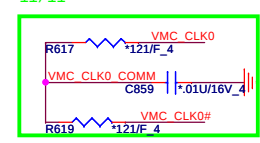
R598 *243/F_4

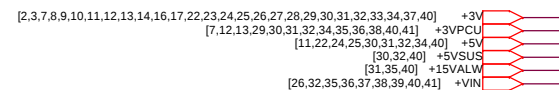
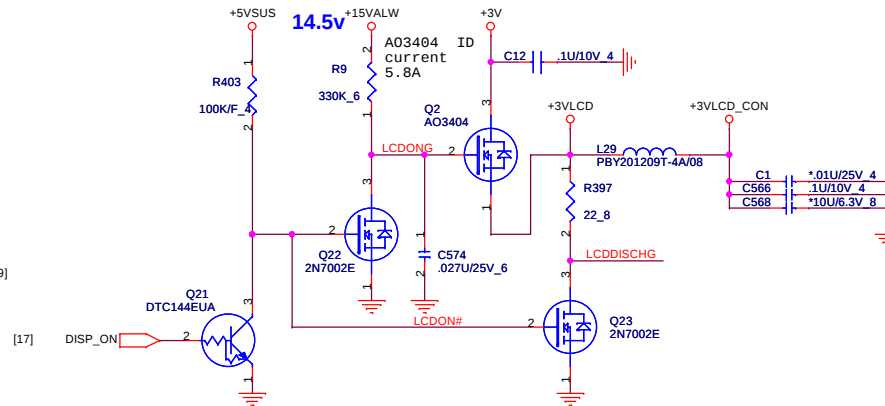
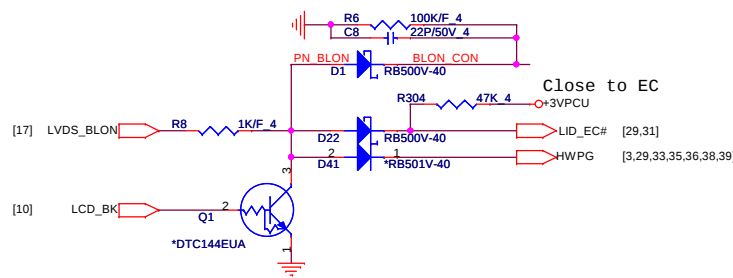
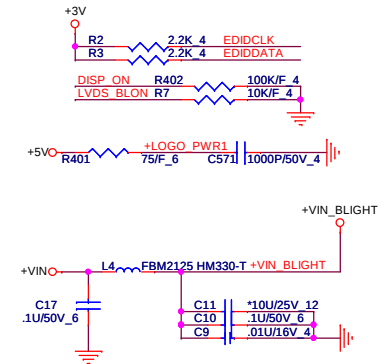
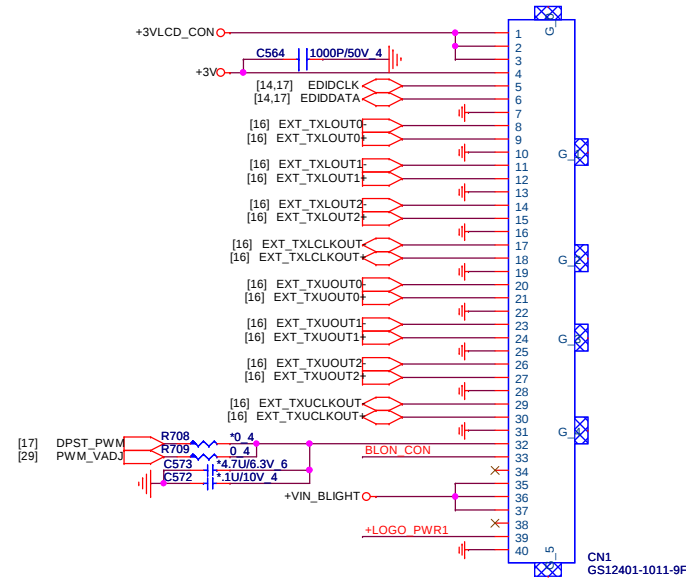
96-BALL SDRAM DDR3

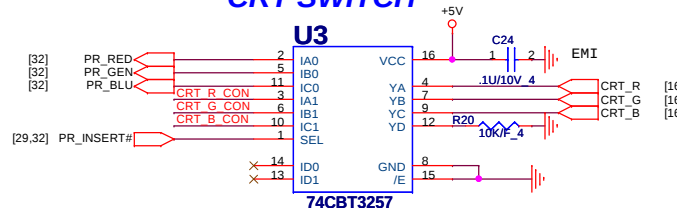
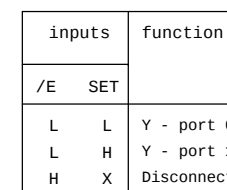
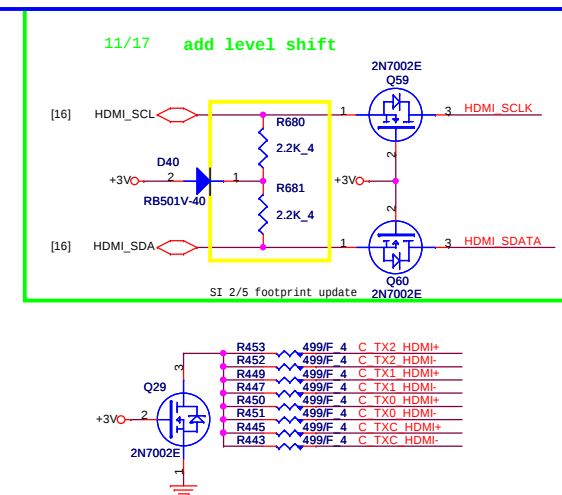
Should be 240 Ohms +-1%

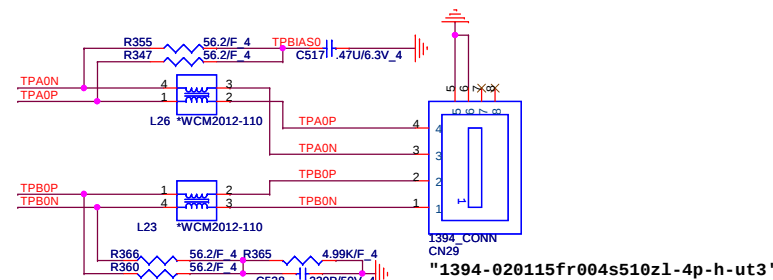
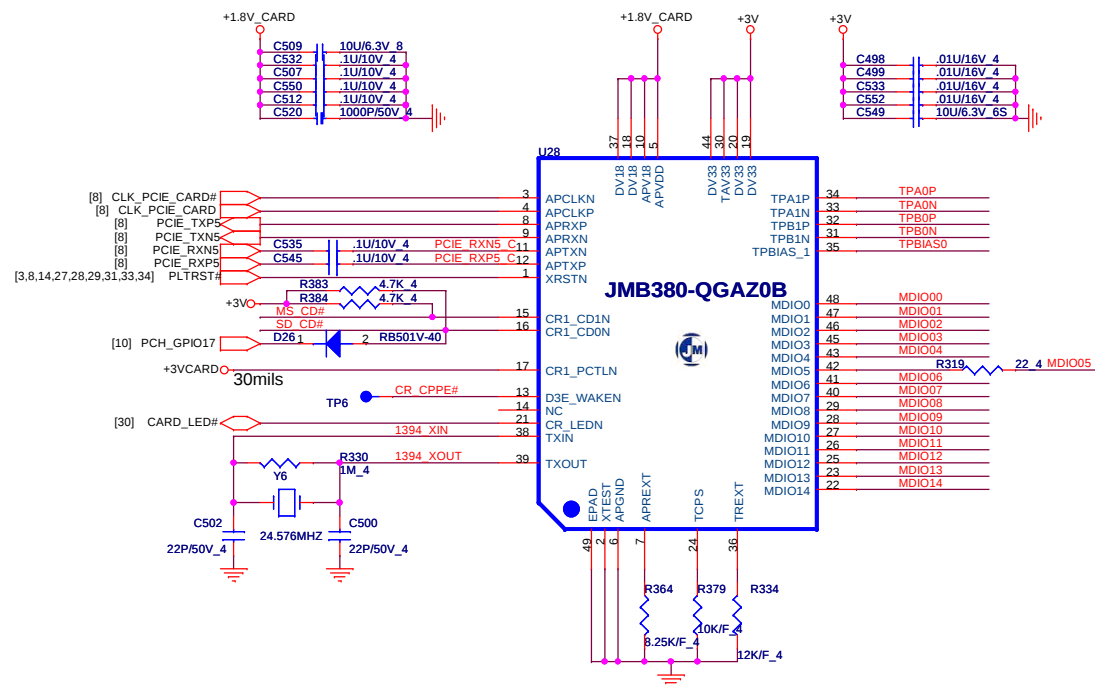
R599 *243/F_4

96-BALL SDRAM DDR3





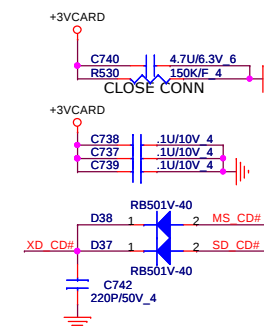
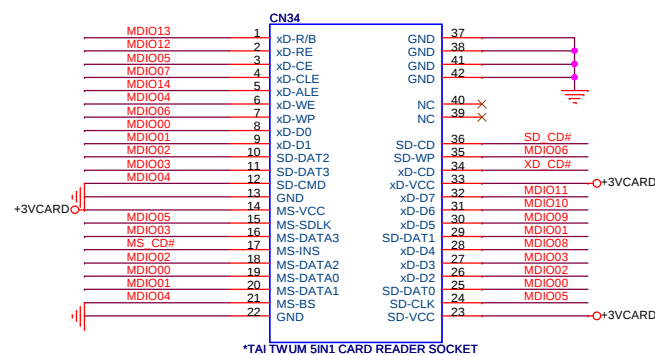
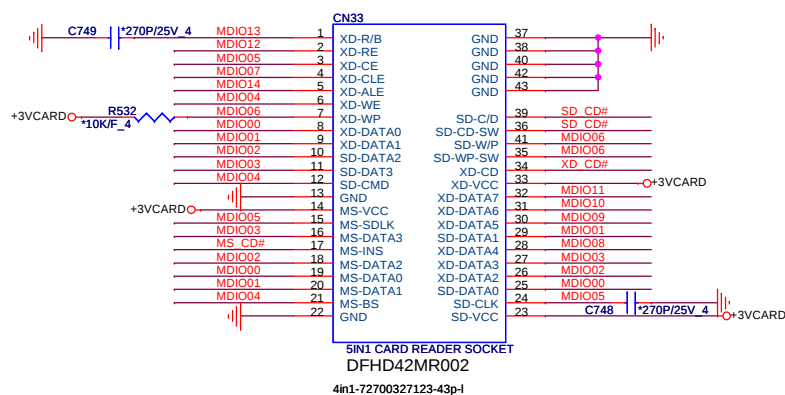
[illegible]



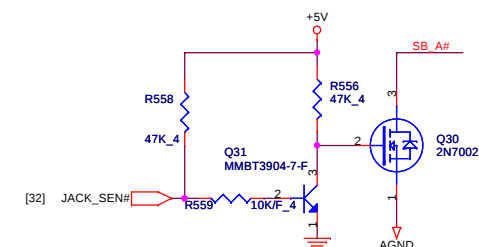
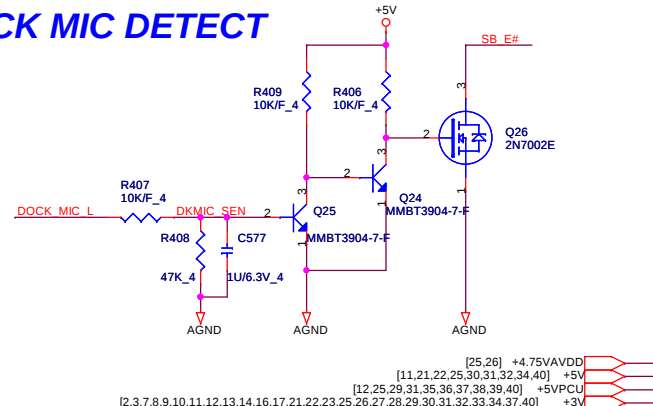
JMB 380 Note:

	SD/MMC	MS	XD
MID00	SD DAT0	MS D0	XD D0
MID01	SD DAT1	MS D1	XD D1
MID02	SD DAT2	MS D2	XD D2
MID03	SD DAT3	MS D3	XD D3
MID04	SD CMD	MS BS	XD WE#
MID05	SD CLK	MS SCLK	XD CE#
MID06	SD WP		XD WP#
MID07			XD CLE
MID08	SD DAT4		XD D4
MID09	SD DAT5		XD D5
MID10	SD DAT6		XD D6
MID11	SD DAT7		XD D7
MID12			XD RE#
MID13			XD R/B#
MID14			XD ALE
CR1_LE0N	SD1 LED#	MS1 LED#	XD LED#
CR1_PCTLN	SD1 PCTL#	MS1 PCTL#	XD PCTL#
CR1_CD0	SD1 CD#		XD CV#
CR1_CD1		MS1 CD#	XD CD#

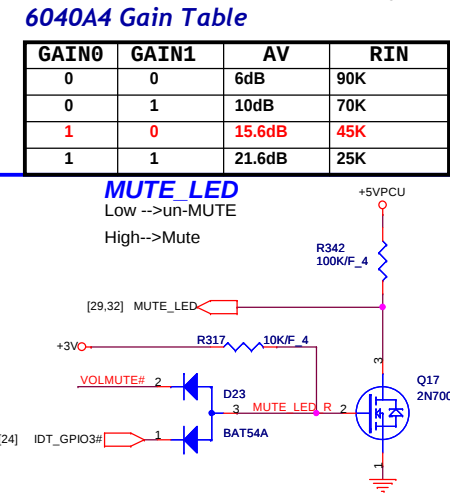
5 IN1 CARD READER
XD, MMC/SD, MS/MSP



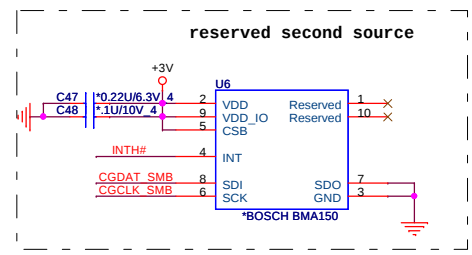
DOCK MIC DETECT



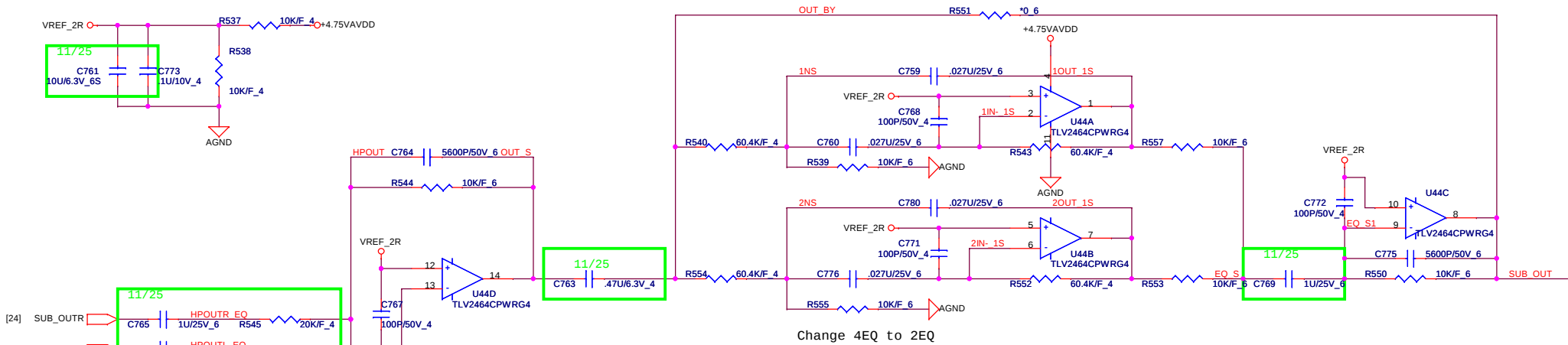
25



SGT-LIS302DLTR interrupt pin
default is low / active Hi , BIOS
need to programming 22h to change
status from active Hi to low

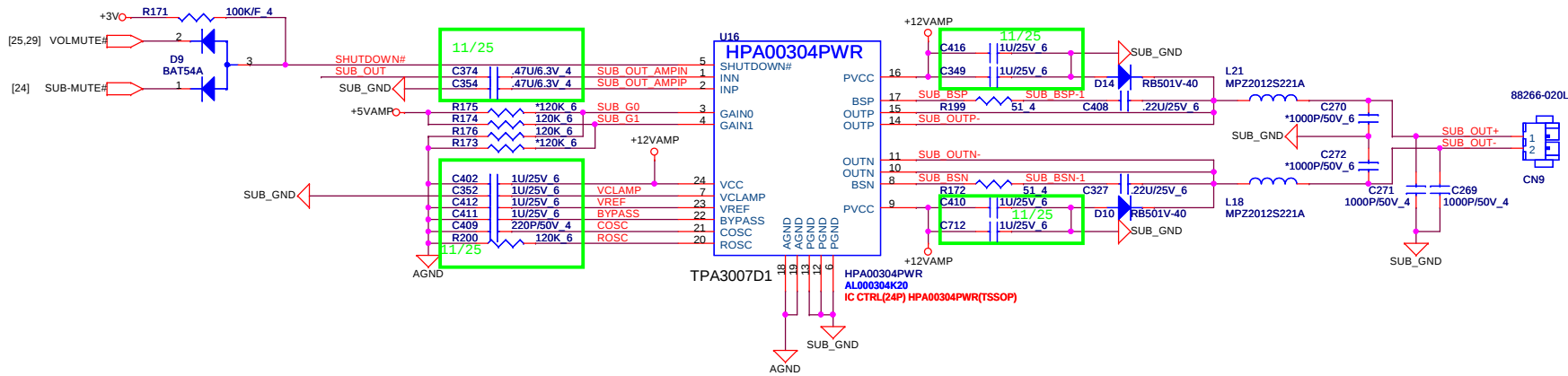


[2,3,7,8,9,10,11,12,13,14,16,17,21,22,23,24,26,27,28,29,30,31,32,33,34,37,40] +3V
[11,21,22,24,30,31,32,34,40] +5V
[24,26] +4.75VAVDD
[26] +5VAMP



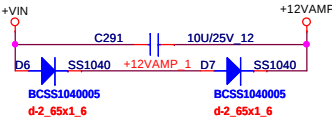
MODEL	UP7
R316	60.4K/F_6
R319	60.4K/F_6
R330	60.4K/F_6
R314	60.4K/F_6
C509	0.027U/25V_6
C510	0.027U/25V_6
C529	0.027U/25V_6
C543	0.027U/25V_6

Change 4EQ to 2EQ

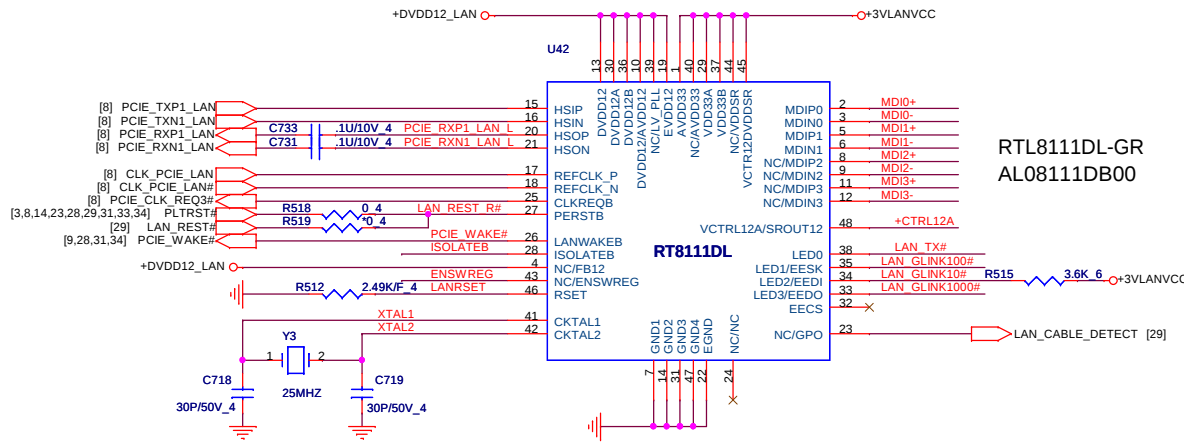


Sub-Woofer power

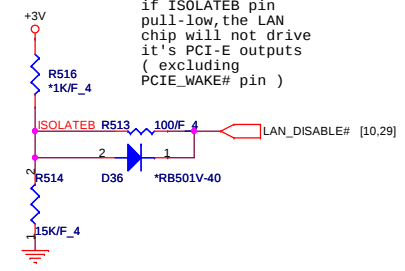
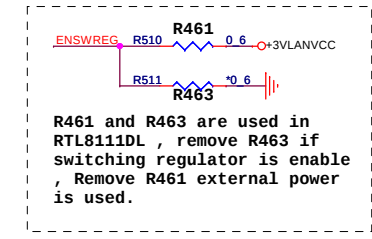
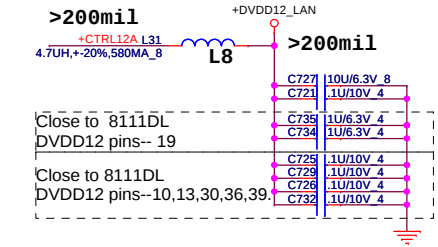
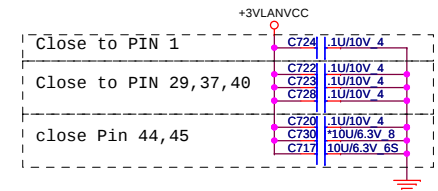
GAIN1	GAIN0	dB
0	0	12
0	1	18
1	0	23.6
1	1	36



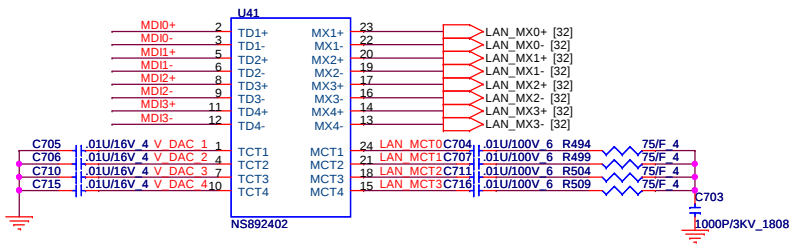
[24,25] +4.75VAVDD
[25] +5VAMP
[21,32,35,36,37,38,39,40,41] +VIN
[2,3,7,8,9,10,11,12,13,14,16,17,21,22,23,24,25,27,28,29,30,31,32,33,34,37,40] +3V



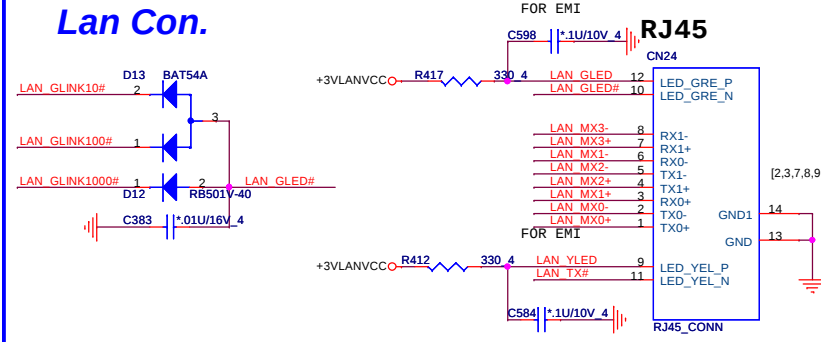
RTL8111DL-GR
AL08111DB00



Transformer for 10/100/1000



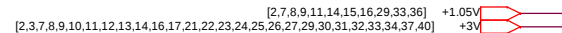
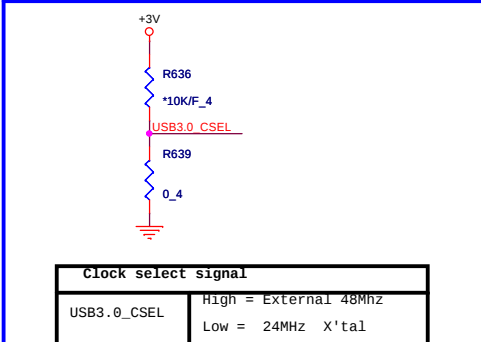
Lan Con.

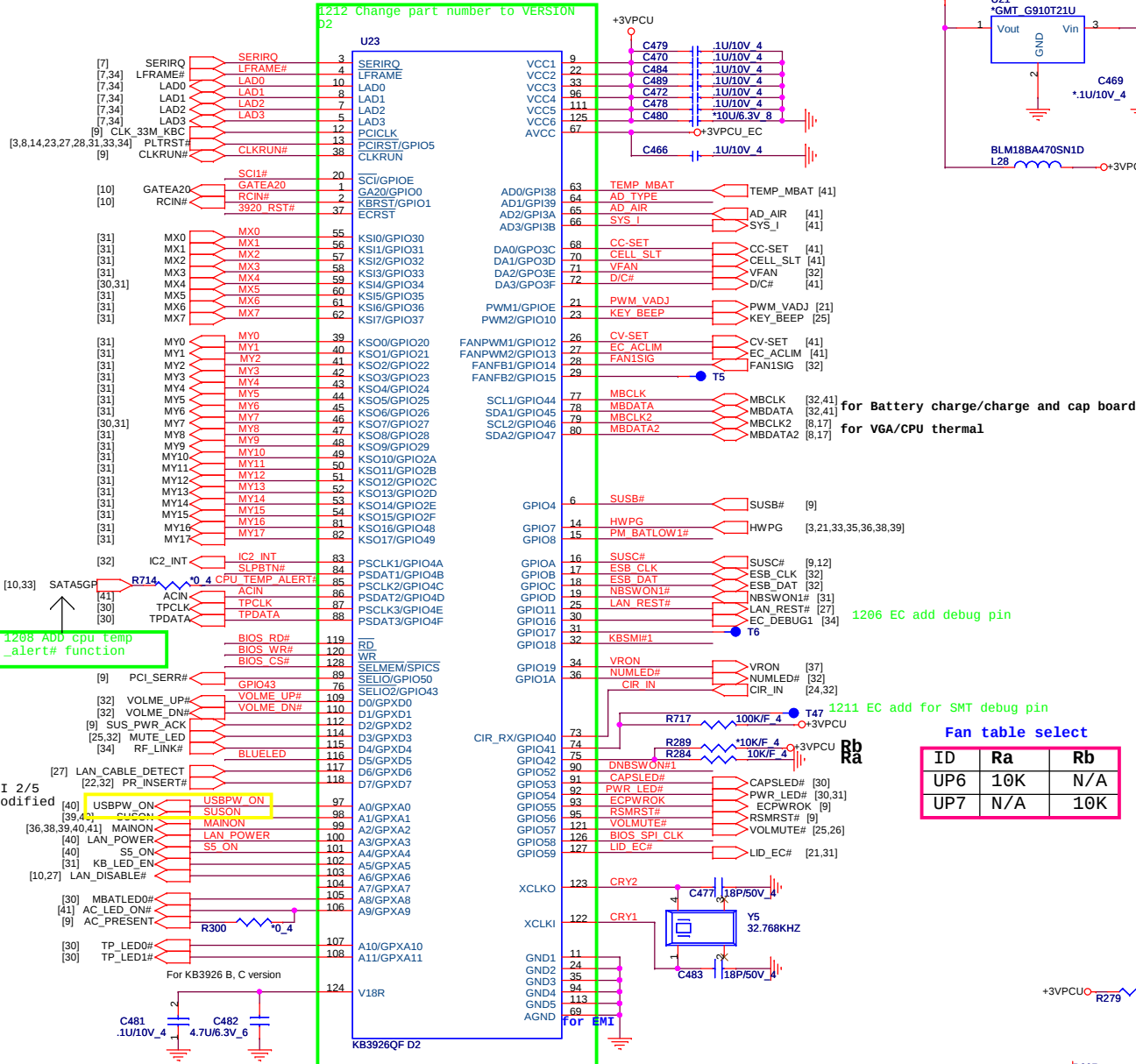




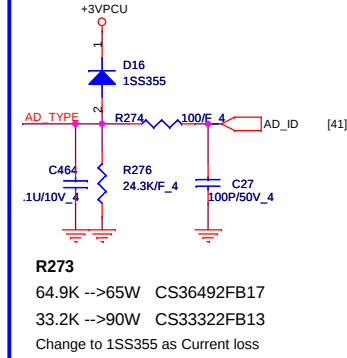
NB5

NB5

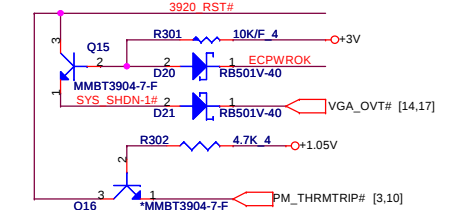




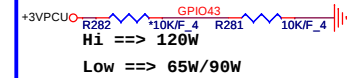
adapter Type check



thermal shutdown circuit

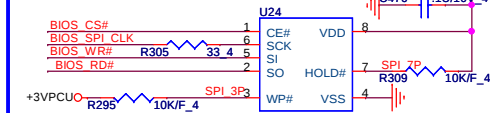


adapter select for EC

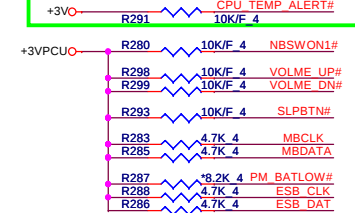


512K byte SPI EC ROM

Socket: DG008000031
MXIC AKE3KZP0001
WINBOND AKE37ZN0N00
AMIT AKE38ZN0800



1208 ADD cpu temp _alert# function



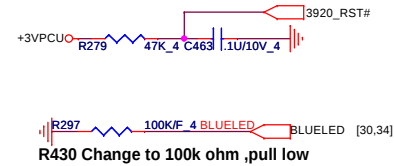
Change to RB501 as Current loss



Add Pin 117,103 for DSM,116 for Bluetooth,Pin 23 for Key Beep to Amplifier
Delete T10 and tie pin 117 from Lan for DSM

Fan table select

ID	Ra	Rb
UP6	10K	N/A
UP7	N/A	10K



11/6 for EMI



[2,3,7,8,9,10,11,12,13,14,16,17,21,22,23,24,25,26,27,28,30,31,32,33,34,37,40]
[7,12,13,21,30,31,32,34,35,36,38,40,41]
[12,24,25,31,35,36,37,38,39,40]

+1.05V

+3V

+3VPCU

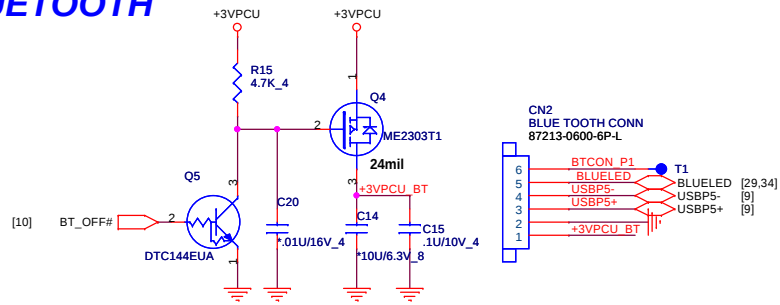
+5VPCU



PROJECT : UP67
Quanta Computer Inc.

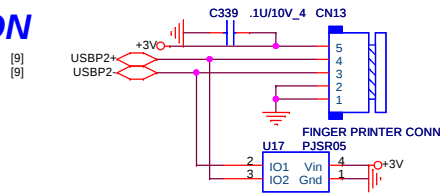
Size	Document Number	Rev
Custom	KB3926/ROM/TP	1A
Date:	Friday, February 27, 2009	Sheet 29 of 45

BLUETOOTH



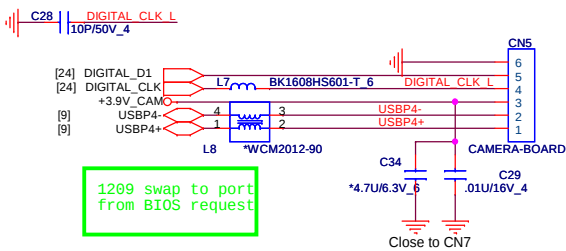
USB fingerprint CON

1. ESD GND
2. SYSTEM GND
3. USB-
4. USB+
5. USB PWR(+3V)

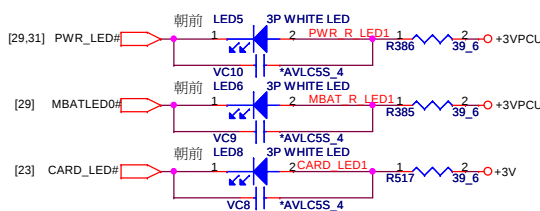


USB CAMERA /DIGITAL MIC CONNECT

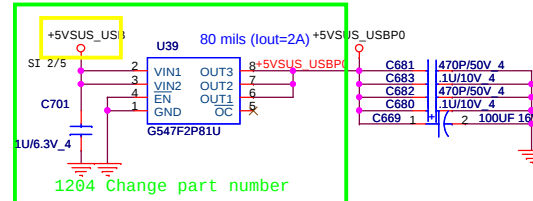
Add for EMI solution



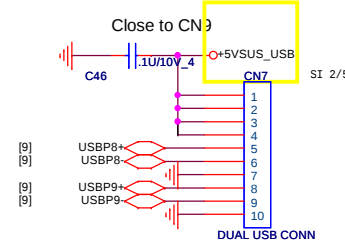
$$V_{out} = 1.25(1 + R_1/\bar{R}_2)$$



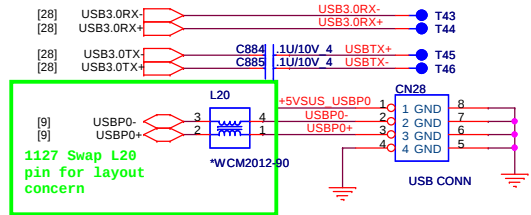
LEFT SIDE USBX1 and E-SATA/USB COMBO



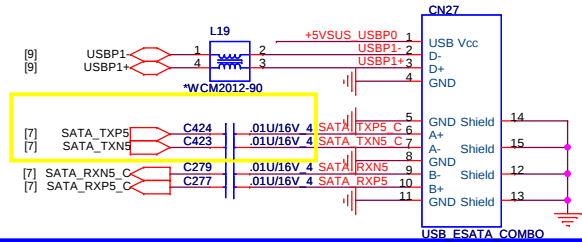
RIGHT SIDE USBX2



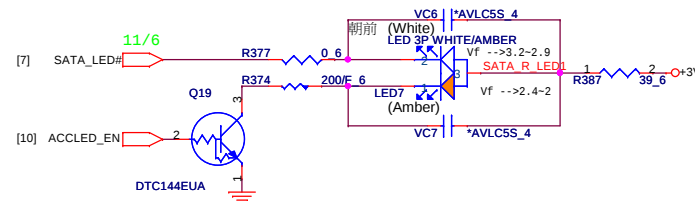
Waiting USB3.0 connector



USB & ESATA

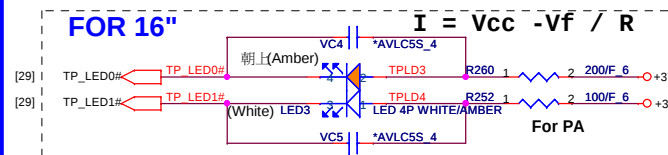


LED

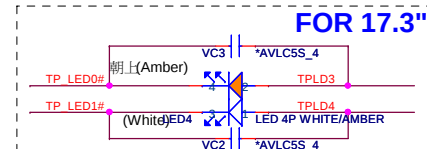


FOR 16"

FOR 17.3"

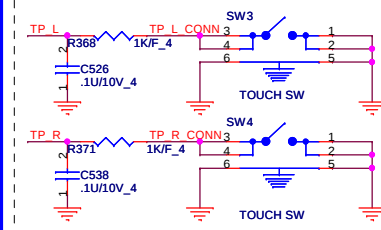


FOR 17.3"

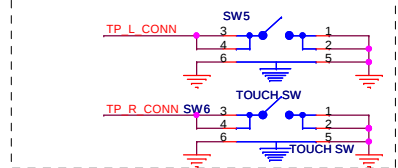


TOUCH PAD CONNECTOR & ON/OFF BOTTOM

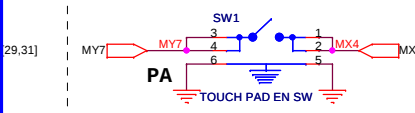
TOUCH PAD L/R **FOR 16"**



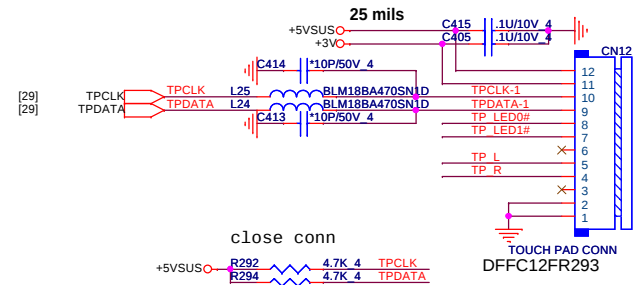
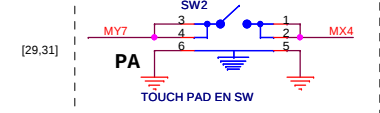
TOUCH PAD L/R **FOR 17.3"**



TOUCH PAD ON/OFF
FOR 16"



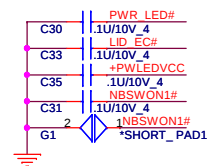
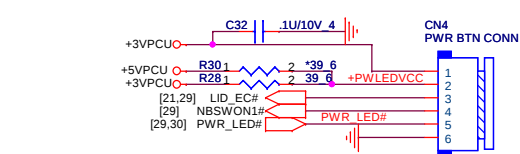
TOUCH PAD ON/OFF
FOR 17.3"



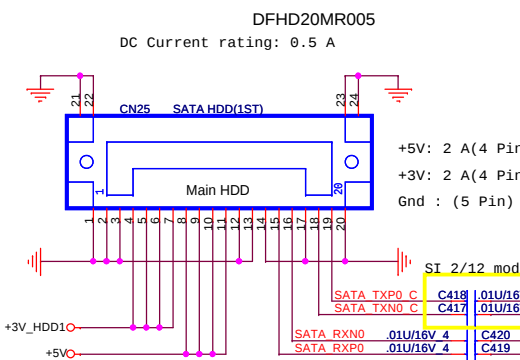
PROJECT : UP67
Quanta Computer Inc.

Size Custom	Document Number BT/WC/FT/ESATA/USB/LED	Rev 1A
Date: Friday, February 27, 2009		Sheet 30 of 45

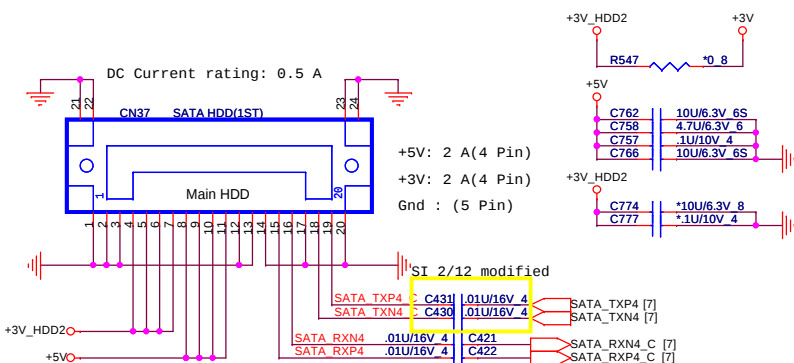
POWER BOTTON CONNECT



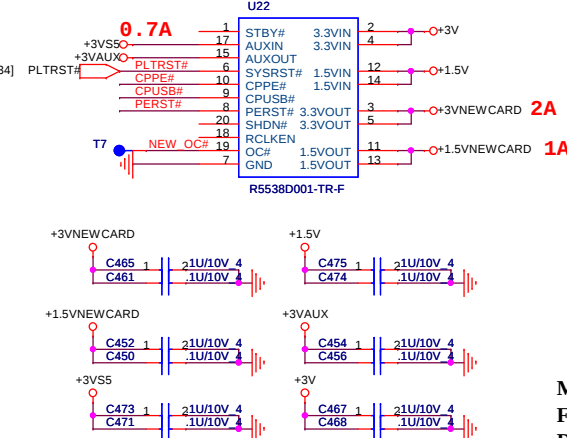
SATA HDD CONNECTOR



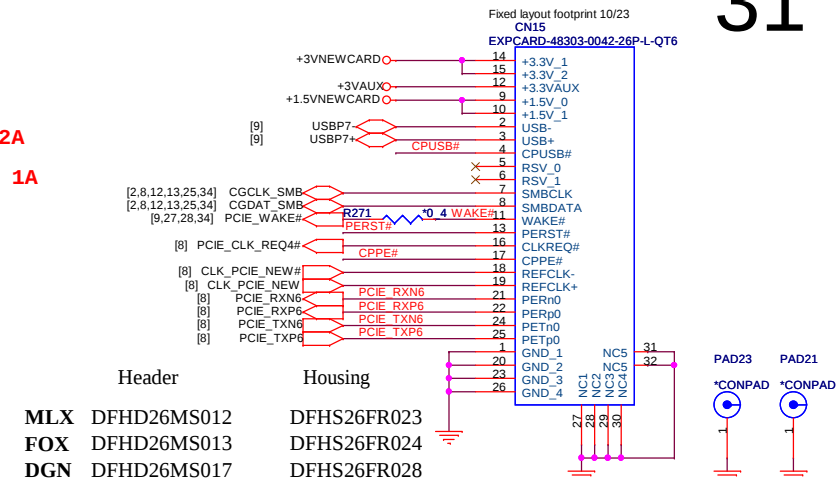
SATA_2 CONNECTOR



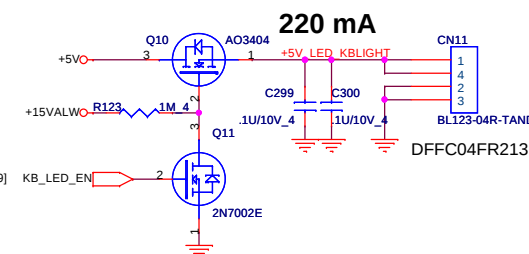
NEWCARD



NEWCARD (PCIEXPRESS*1 + USB*1)

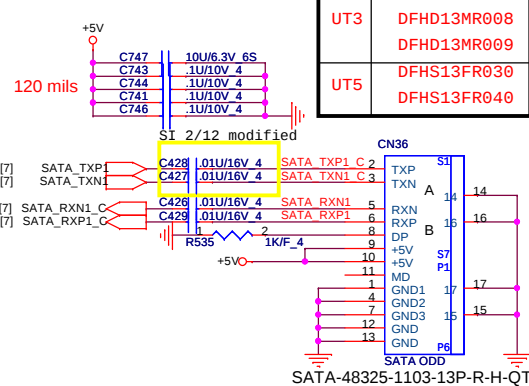


Backlight Keyboard Con.

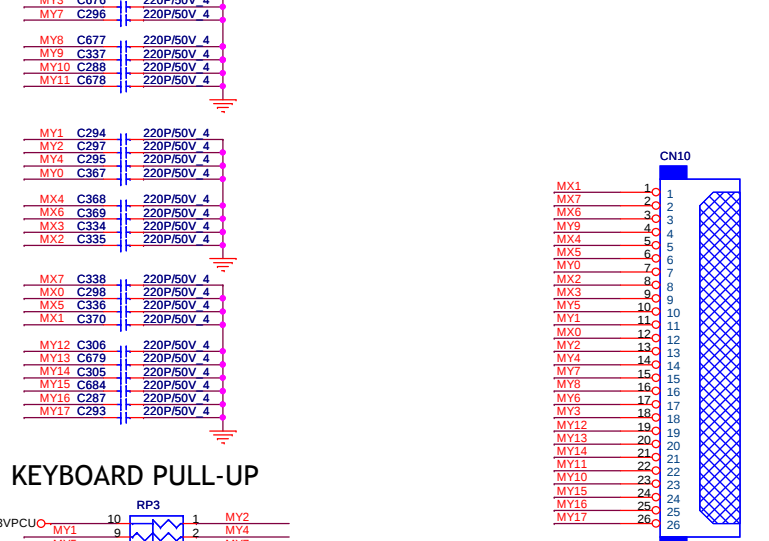


clear ABS 758 resin for key cap.
7 LEDs for 15.4" (total LED current 140mA)
11 LEDs for 17" (Total LED current 220mA)

SATA CD-ROM



KEYBOARD Con.



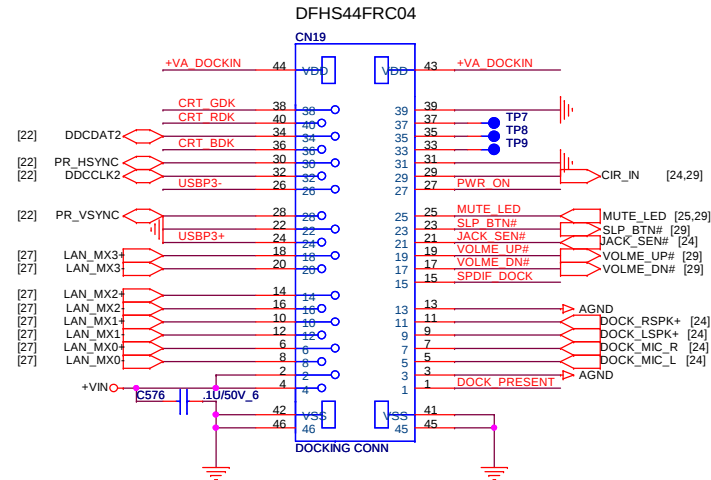
GB1RF260-1253-BF
[29,30] MY[0..17]
[29,30] MX[0..7]



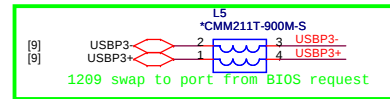
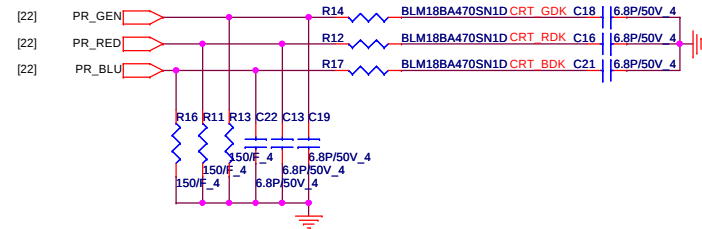
PROJECT : UP67
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ODDI/HDD/NEW CARD/PW/KB	1A
Date: Friday, February 27, 2009	Sheet 31 of 45	

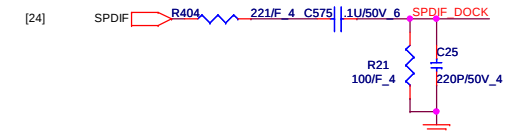
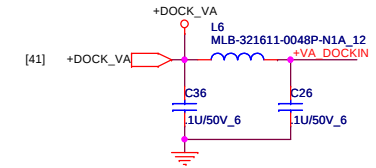
CABLE DOCK



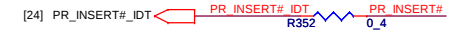
Delete CX08T470000 as CRT rising time and falling time request



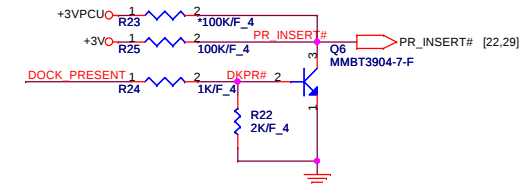
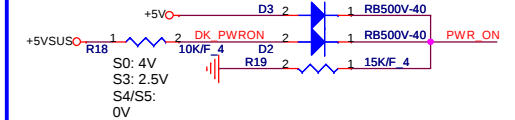
32



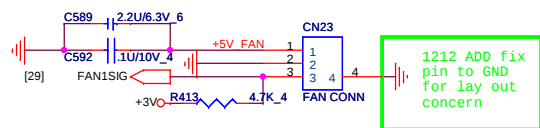
For IDT Dolby functionality.



Change to RB500 as Current loss



CPU FAN



DFHD03MR008

1204 Change part number

FANPWR = 1.6*VSET

30 MIL

G991PV11

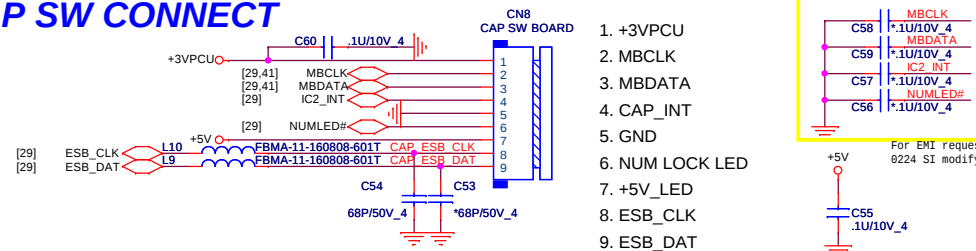
G995 layout notice

Gnd shape

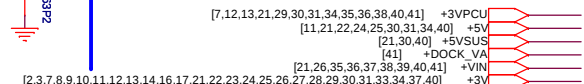
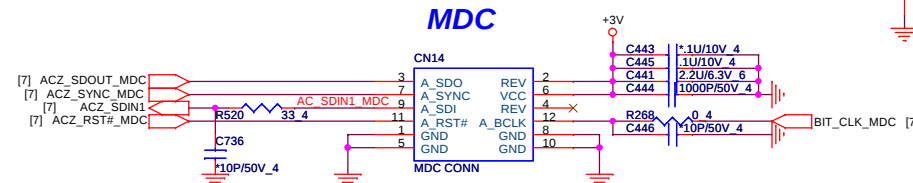
8 7 6 5 4 3 2 1

1 2 3 4

CAP SW CONNECT

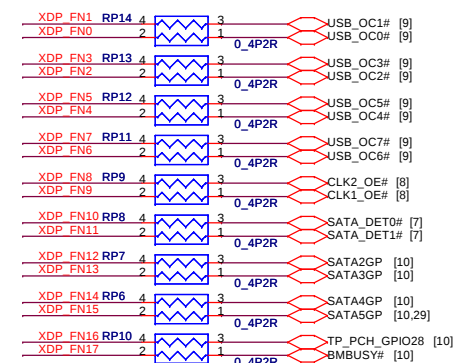
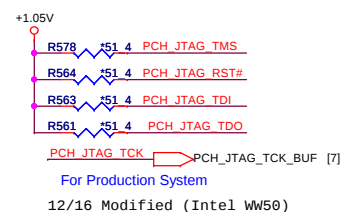
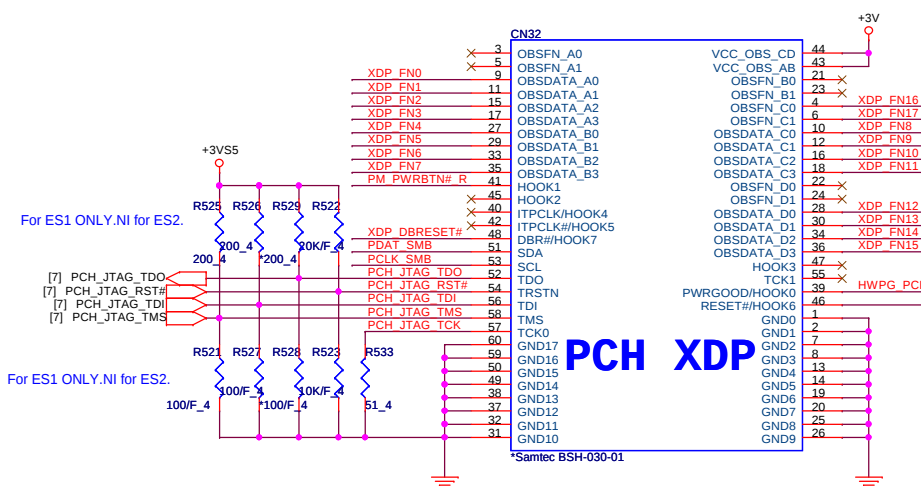
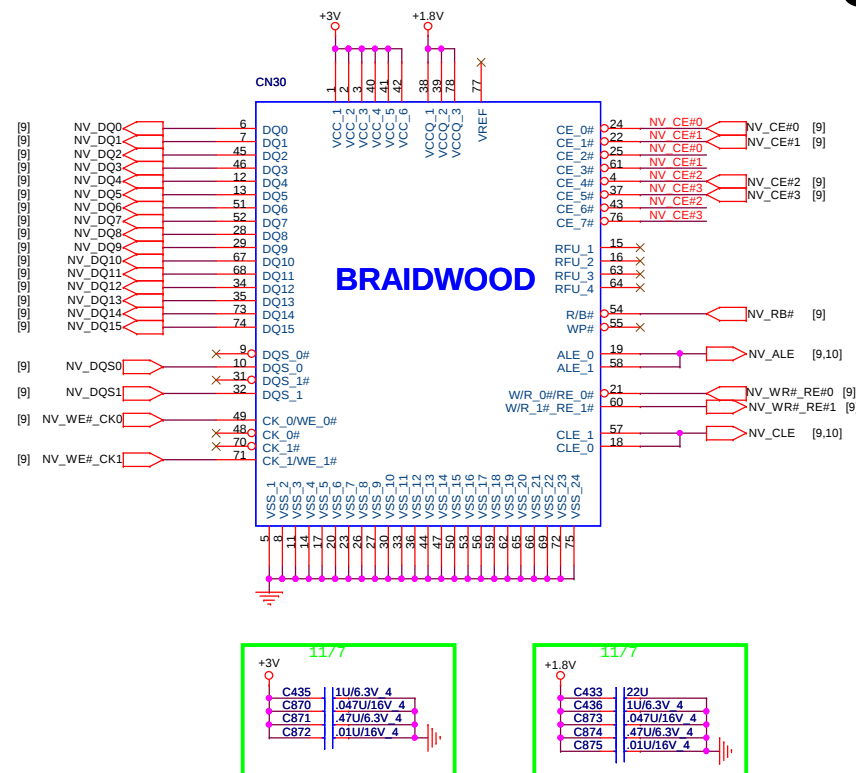
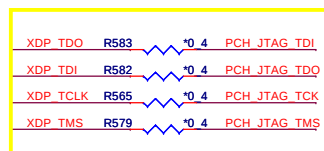


Modem CONN

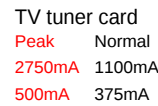


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Quanta Computer Inc.

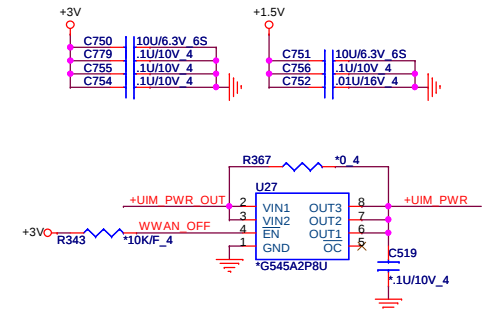
Size	Document Number	Rev
Custom	DOCKING/FAN/CAP/MDC	1A
Date: Monday, March 02, 2009	Sheet 32 of 45	

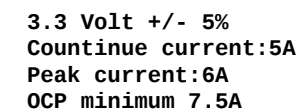


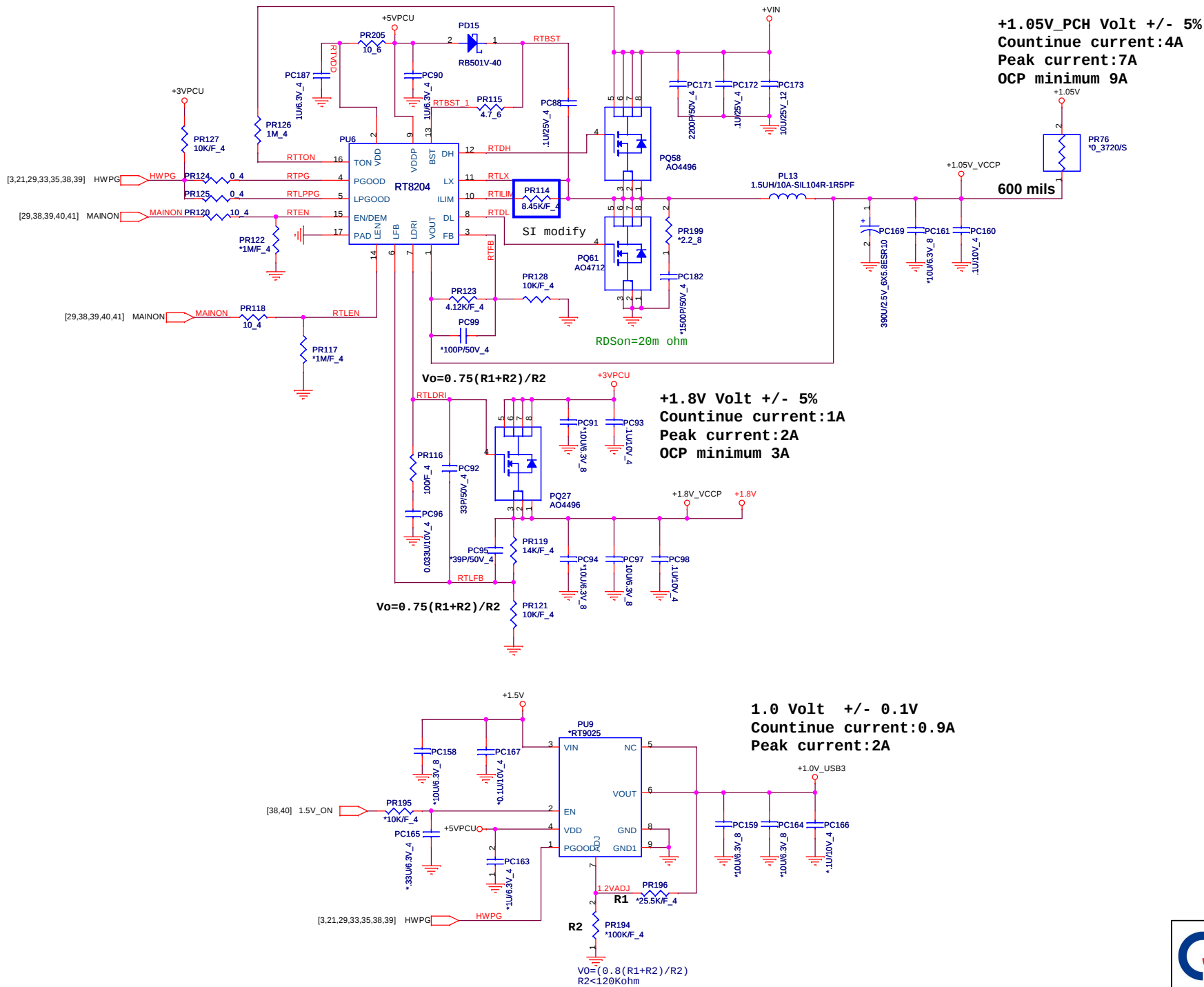
34



Peak	Normal
2750mA	1100mA
500mA	375mA

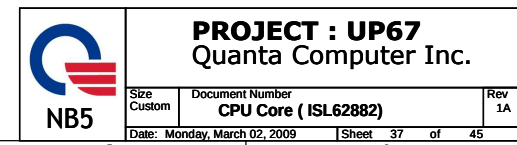






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 Quanta Computer Inc.

Size	Document Number	Rev
Custom	+5V/+3V (RT8206B)	1A
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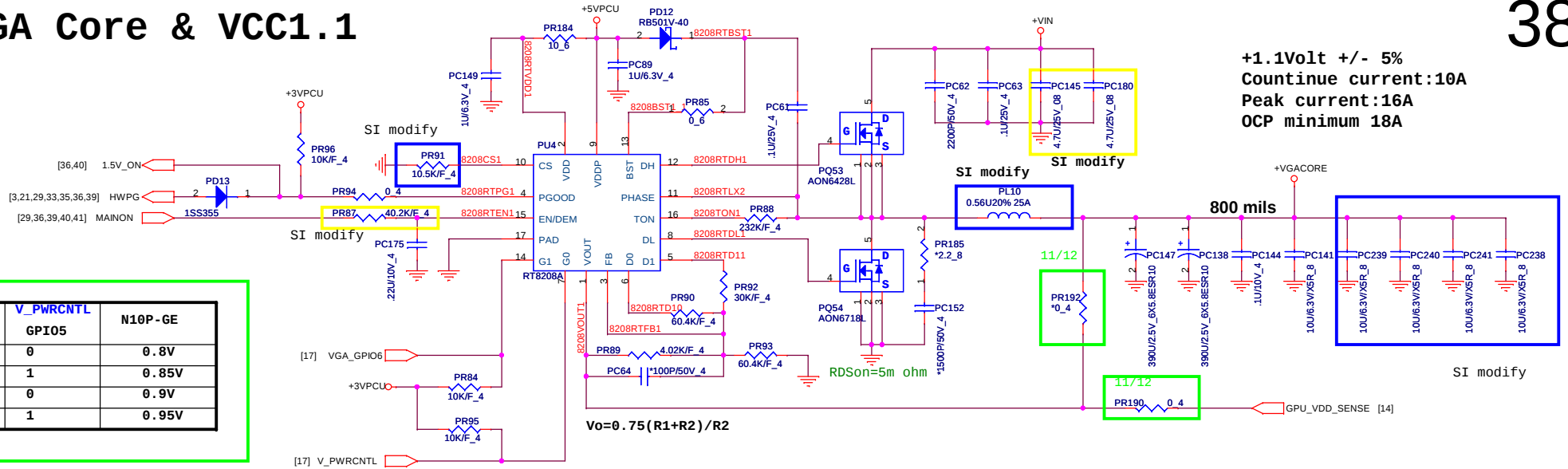


VGA Core & VCC1.1

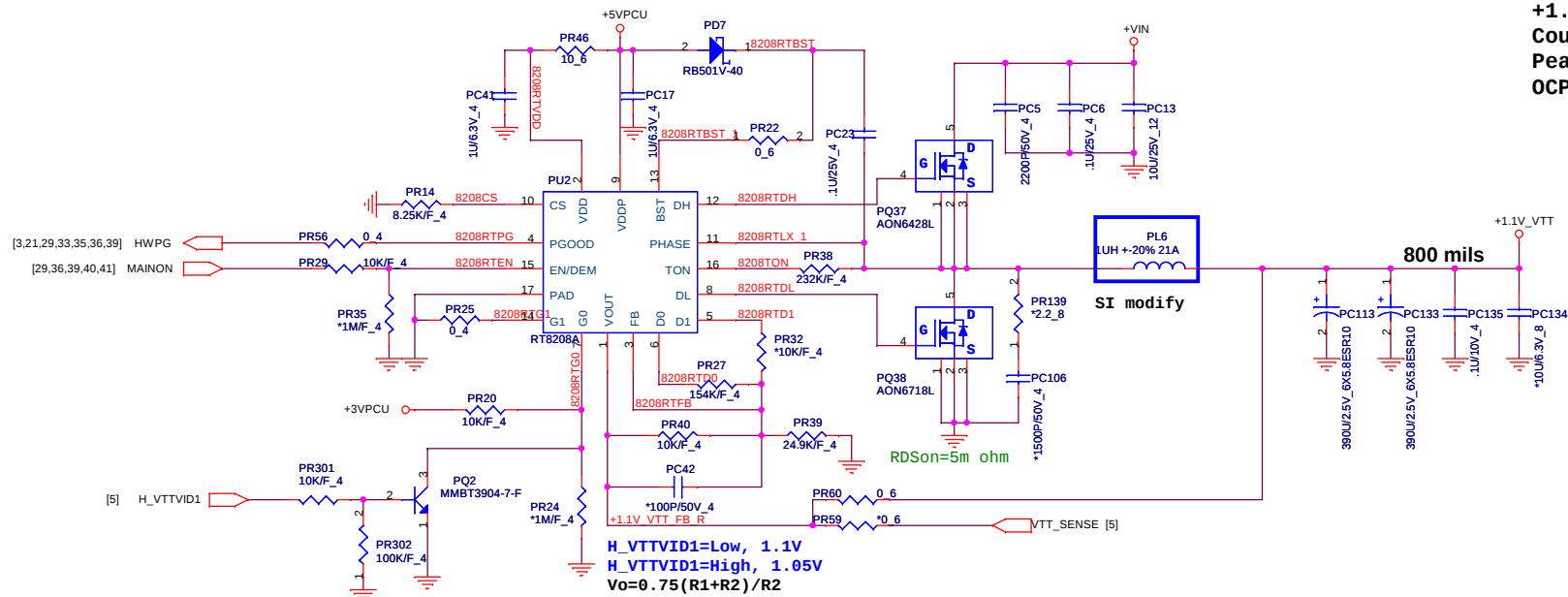
38

11/13

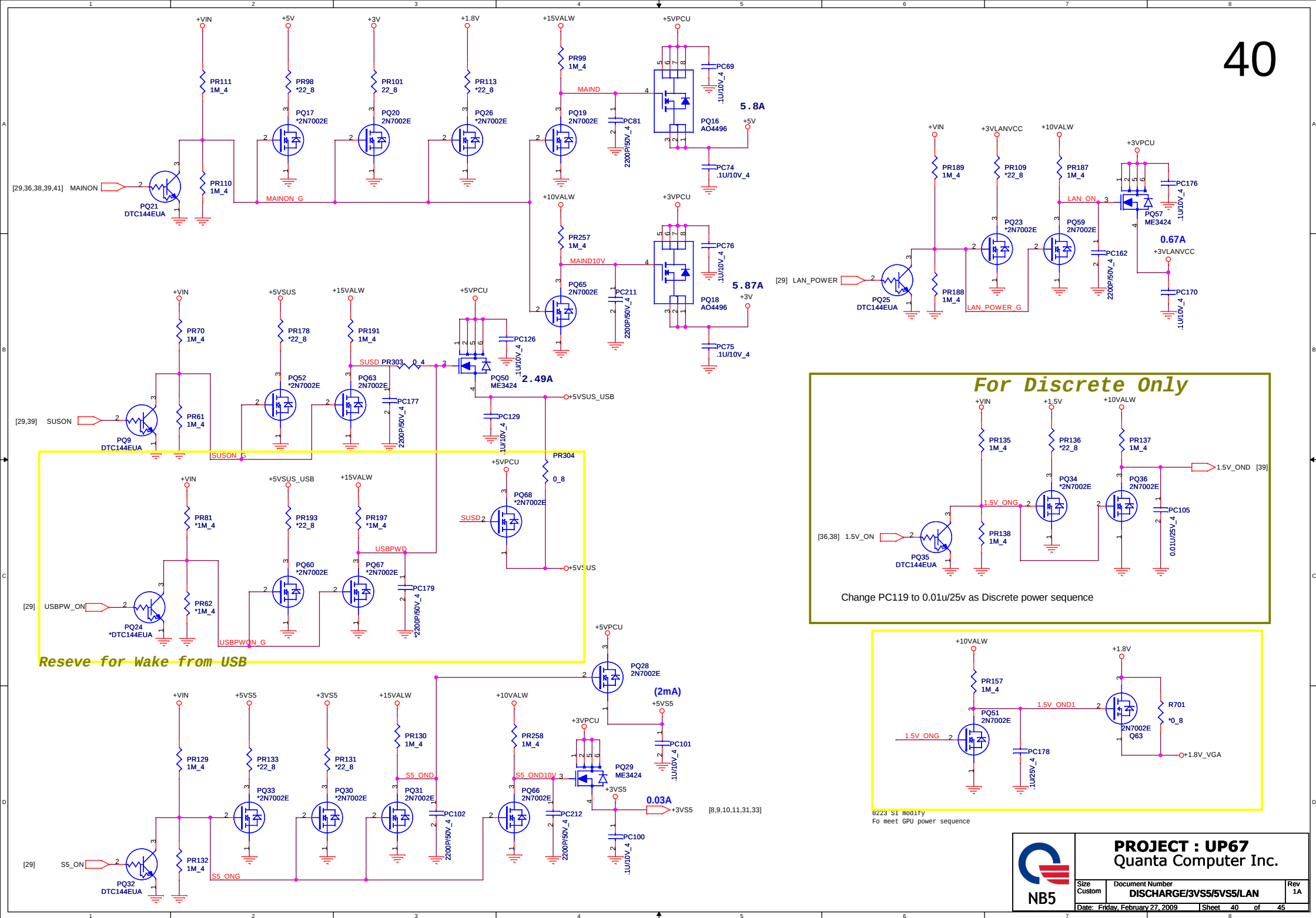
VGA_GPIO6	V_PWRCNTL	N10P-GE
0	0	0.8V
0	1	0.85V
1	0	0.9V
1	1	0.95V



+1.1Volt +/- 5%
Countinue current:10A
Peak current:16A
OCP minimum 18A

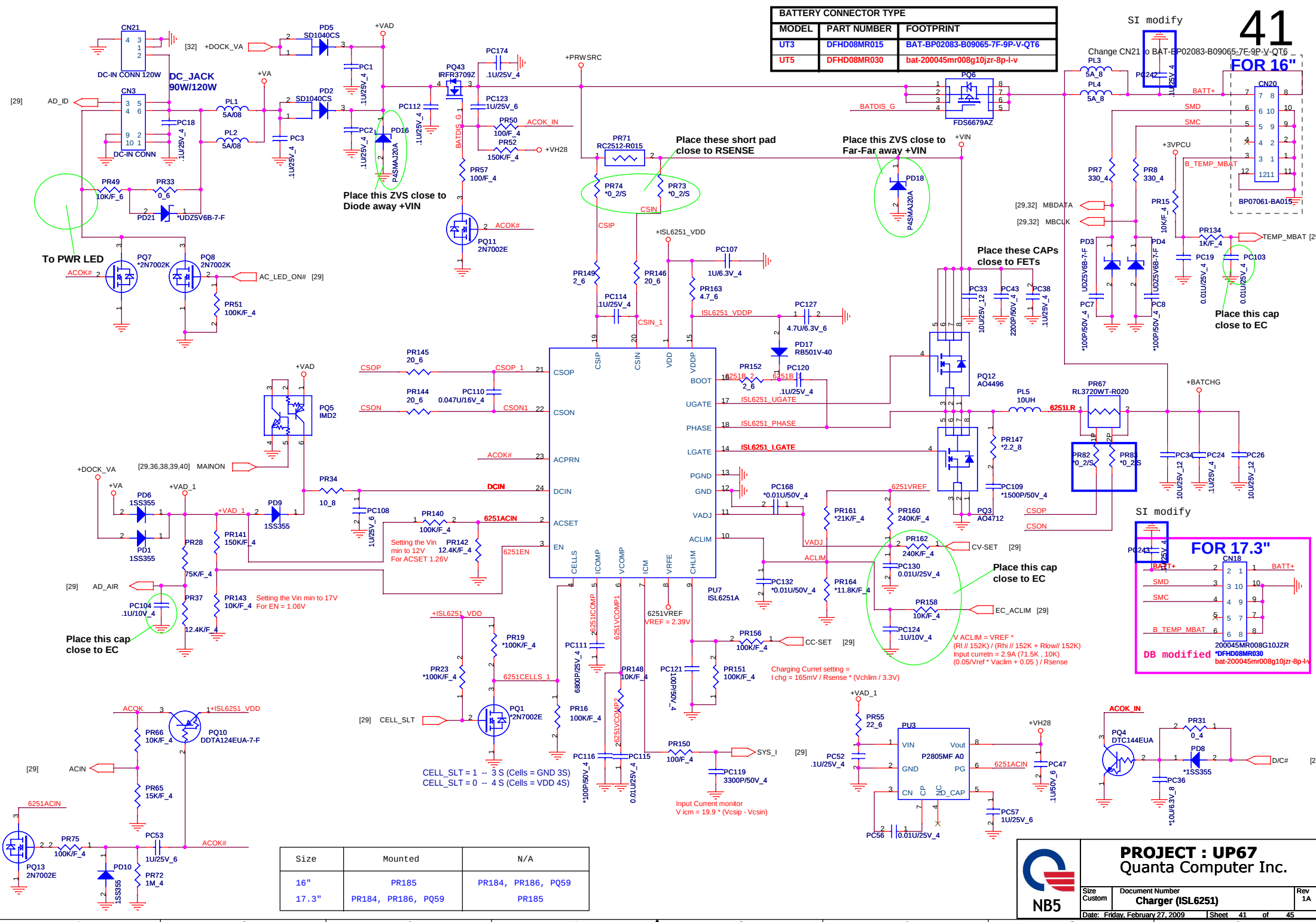


+1.1V_PCH Volt +/- 5%
Countinue current:12A
Peak current:15A
OCP minimum 18A



BATTERY CONNECTOR TYPE		
MODEL	PART NUMBER	FOOTPRINT
UT3	DFHD08MR015	BAT-BP02083-B09065-7F-9P-V-QT6
UT5	DFHD08MR030	bat-200045mr008g10jzr-8p-l-v

SI modify
41
FOR 16"



SI modify

FOR 17.3"

DB modified

200045MR008G10JZR
DFHD08MR030
bat-200045mr008g10jzr-8p-l-v

Size	Mounted	N/A
16"	PR185	PR184, PR186, PQ59
17.3"	PR184, PR186, PQ59	PR185

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Size Custom	Document Number Charger (ISL6251)	Rev 1A
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Power up sequence

