

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : SGND1
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : IN3
LAYER 7 : SGND2
LAYER 8 : BOT

Cable Docking

TV_OUT
VGA
RJ-45
CIR/Pwr btn
SPDIF Out
Stereo MIC
Headphone Jack
USB Port
VOL Cntr

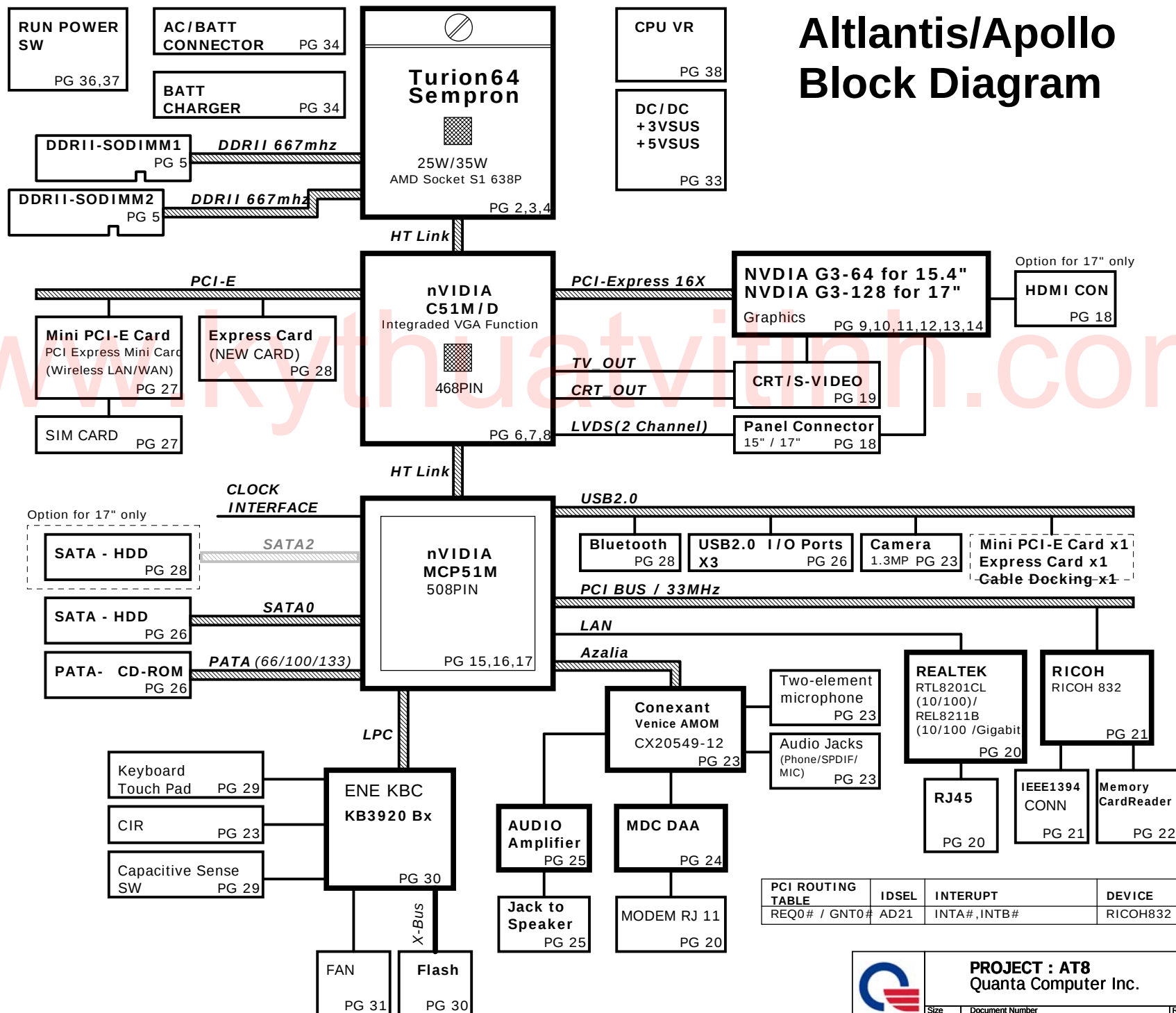
PG 31

VAULE DEFINE

A=0603,B=0805,C=1206,F=1%,
OTHER IS 0402

EXAMPLE

10R=10ohm(0402)
10A=10ohm(0603)
10B=10ohm(0805)
10C=10ohm(1206)
10/F=10ohm(0402 and 1%)



Atlantis/Apollo Block Diagram



NBS/RD2/HW1

PROJECT : AT8
Quanta Computer Inc.

Size Custom	Document Number Block Diagram	Rev 1A
Date: Wednesday, June 14, 2006		Sheet 1 of 39

U268

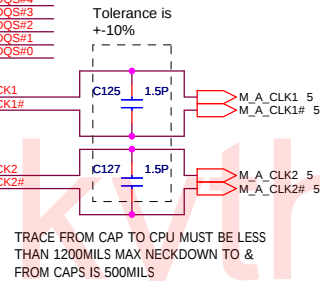
M A DQ63 AB12	MA_DATA[63]	MA_DM[7]	Y13 M A DQM7
M A DQ62 AB12	MA_DATA[62]	MA_DM[6]	AB16 M A DQM6
M A DQ61 AA14	MA_DATA[61]	MA_DM[5]	Y19 M A DQM5
M A DQ60 AB14	MA_DATA[60]	MA_DM[4]	AC24 M A DQM4
M A DQ59 W11	MA_DATA[59]	MA_DM[3]	E24 M A DQM3
M A DQ58 Y12	MA_DATA[58]	MA_DM[2]	E19 M A DQM2
M A DQ57 AD13	MA_DATA[57]	MA_DM[1]	C15 M A DQM1
M A DQ56 AB13	MA_DATA[56]	MA_DM[0]	E12 M A DQM0
M A DQ55 AD15	MA_DATA[55]		
M A DQ54 AB15	MA_DATA[54]		
M A DQ53 AB17	MA_DATA[53]		
M A DQ52 Y17	MA_DATA[52]	MA_DQS[7]	W12 M A DQS7
M A DQ51 Y14	MA_DATA[51]	MA_DQS[6]	Y15 M A DQS6
M A DQ50 W14	MA_DATA[50]	MA_DQS[5]	AB19 M A DQS5
M A DQ49 W16	MA_DATA[49]	MA_DQS[4]	AD23 M A DQS4
M A DQ48 AD17	MA_DATA[48]	MA_DQS[3]	G22 M A DQS3
M A DQ47 Y18	MA_DATA[47]	MA_DQS[2]	C22 M A DQS2
M A DQ46 AD19	MA_DATA[46]	MA_DQS[1]	G16 M A DQS1
M A DQ45 AD21	MA_DATA[45]	MA_DQS[0]	G13 M A DQS0
M A DQ44 AB21	MA_DATA[44]	MA_DQS#7	W13 M A DQS#7
M A DQ43 AB18	MA_DATA[43]	MA_DQS#6	W15 M A DQS#6
M A DQ42 AA18	MA_DATA[42]	MA_DQS#5	AB20 M A DQS#5
M A DQ41 AA20	MA_DATA[41]	MA_DQS#4	AC23 M A DQS#4
M A DQ40 Y20	MA_DATA[40]	MA_DQS#3	MA_DQS#3
M A DQ39 AA22	MA_DATA[39]	MA_DQS#2	C21 M A DQS#2
M A DQ38 Y22	MA_DATA[38]	MA_DQS#1	G15 M A DQS#1
M A DQ37 W21	MA_DATA[37]	MA_DQS#0	H13 M A DQS#0
M A DQ36 W22	MA_DATA[36]		
M A DQ35 AA21	MA_DATA[35]		
M A DQ34 AB22	MA_DATA[34]	MA0_CLK[1]	E16 M A CK1
M A DQ33 AB24	MA_DATA[33]	MA0_CLK#1	E16 M A CK1#
M A DQ32 Y24	MA_DATA[32]		
M A DQ31 H22	MA_DATA[31]		
M A DQ30 H20	MA_DATA[30]		
M A DQ29 E22	MA_DATA[29]	MA0_CLK[2]	Y16 M A CK2
M A DQ28 E21	MA_DATA[28]	MA0_CLK#2	AA16 M A CK2#
M A DQ27 J19	MA_DATA[27]		
M A DQ26 H24	MA_DATA[26]		
M A DQ25 E22	MA_DATA[25]		
M A DQ24 E20	MA_DATA[24]		
M A DQ23 C23	MA_DATA[23]		
M A DQ22 B22	MA_DATA[22]		
M A DQ21 E18	MA_DATA[21]		
M A DQ20 E16	MA_DATA[20]		
M A DQ19 E20	MA_DATA[19]		
M A DQ18 D22	MA_DATA[18]		
M A DQ17 C19	MA_DATA[17]		
M A DQ16 G18	MA_DATA[16]		
M A DQ15 G17	MA_DATA[15]		
M A DQ14 C17	MA_DATA[14]		
M A DQ13 E14	MA_DATA[13]		
M A DQ12 E14	MA_DATA[12]		
M A DQ11 H17	MA_DATA[11]		
M A DQ10 E17	MA_DATA[10]	MA_BANK[2]	K22 M A BA2
M A DQ9 E15	MA_DATA[9]	MA_BANK[1]	R20 M A BA1
M A DQ8 H15	MA_DATA[8]	MA_BANK[0]	T22 M A BA0
M A DQ7 E13	MA_DATA[7]		
M A DQ6 C13	MA_DATA[6]		
M A DQ5 H12	MA_DATA[5]		
M A DQ4 G14	MA_DATA[4]		
M A DQ3 G14	MA_DATA[3]	MA_RAS#	P20 M A RAS#
M A DQ2 H14	MA_DATA[2]	MA_CAS#	U20 M A CAS#
M A DQ1 F12	MA_DATA[1]	MA_WE#	U21 M A WE#
M A DQ0 G12	MA_DATA[0]		
M A A15 K19	MA_ADD[15]	MA0_CS#3	V19 M A CS#3
M A A14 K20	MA_ADD[14]	MA0_CS#2	J22 M A CS#2
M A A13 V24	MA_ADD[13]	MA0_CS#1	V22 M A CS#1
M A A12 K24	MA_ADD[12]	MA0_CS#0	T19 M A CS#0
M A A11 L20	MA_ADD[11]		
M A A10 R19	MA_ADD[10]		
M A A9 L19	MA_ADD[9]		
M A A8 L22	MA_ADD[8]	MA_CKE[1]	J20 M A CKE1
M A A7 L21	MA_ADD[7]	MA_CKE[0]	J21 M A CKE0
M A A6 M19	MA_ADD[6]		
M A A5 M20	MA_ADD[5]		
M A A4 M24	MA_ADD[4]		
M A A3 M22	MA_ADD[3]	MA0_ODT[1]	V20 M A ODT1
M A A2 N22	MA_ADD[2]	MA0_ODT[0]	U19 M A ODT0
M A A1 N21	MA_ADD[1]		
M A A0 R21	MA_ADD[0]		

AMD S1 SOCKET

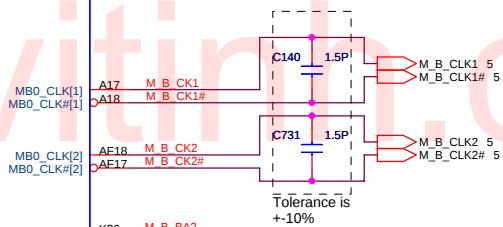
U26C

M B DQ63 AD11	MB_DATA[63]	MB_DM[7]	AD12 M B DQM7
M B DQ62 AF11	MB_DATA[62]	MB_DM[6]	AC16 M B DQM6
M B DQ61 AF14	MB_DATA[61]	MB_DM[5]	AE22 M B DQM5
M B DQ60 AF14	MB_DATA[60]	MB_DM[4]	AB26 M B DQM4
M B DQ59 Y11	MB_DATA[59]	MB_DM[3]	E25 M B DQM3
M B DQ58 AB11	MB_DATA[58]	MB_DM[2]	A22 M B DQM2
M B DQ57 AC12	MB_DATA[57]	MB_DM[1]	B16 M B DQM1
M B DQ56 AF13	MB_DATA[56]	MB_DM[0]	A12 M B DQM0
M B DQ55 AF15	MB_DATA[55]		
M B DQ54 AF16	MB_DATA[54]		
M B DQ53 AC18	MB_DATA[53]	MB_DQS[7]	AF12 M B DQS7
M B DQ52 AF19	MB_DATA[52]	MB_DQS[6]	AE16 M B DQS6
M B DQ51 AD14	MB_DATA[51]	MB_DQS[5]	AE21 M B DQS5
M B DQ50 AC14	MB_DATA[50]	MB_DQS[4]	AC25 M B DQS4
M B DQ49 AF18	MB_DATA[49]	MB_DQS[3]	E26 M B DQS3
M B DQ48 AD18	MB_DATA[48]	MB_DQS[2]	A24 M B DQS2
M B DQ47 AD20	MB_DATA[47]	MB_DQS[1]	D16 M B DQS1
M B DQ46 AC20	MB_DATA[46]	MB_DQS[0]	C12 M B DQS0
M B DQ45 AF23	MB_DATA[45]	MB_DQS#7	AE12 M B DQS#7
M B DQ44 AF24	MB_DATA[44]	MB_DQS#6	AD18 M B DQS#6
M B DQ43 AF20	MB_DATA[43]	MB_DQS#5	AE22 M B DQS#5
M B DQ42 AF20	MB_DATA[42]	MB_DQS#4	AC26 M B DQS#4
M B DQ41 AD22	MB_DATA[41]	MB_DQS#3	AE22 M B DQS#3
M B DQ40 AC22	MB_DATA[40]	MB_DQS#2	AE23 M B DQS#2
M B DQ39 AF25	MB_DATA[39]	MB_DQS#1	C16 M B DQS#1
M B DQ38 AD26	MB_DATA[38]	MB_DQS#0	B12 M B DQS#0
M B DQ37 AA25	MB_DATA[37]		
M B DQ36 AA28	MB_DATA[36]		
M B DQ35 AE24	MB_DATA[35]		
M B DQ34 AD24	MB_DATA[34]		
M B DQ33 AA23	MB_DATA[33]		
M B DQ32 AA24	MB_DATA[32]		
M B DQ31 G24	MB_DATA[31]		
M B DQ30 G23	MB_DATA[30]		
M B DQ29 D26	MB_DATA[29]		
M B DQ28 C26	MB_DATA[28]		
M B DQ27 G26	MB_DATA[27]		
M B DQ26 G25	MB_DATA[26]		
M B DQ25 E24	MB_DATA[25]		
M B DQ24 E23	MB_DATA[24]		
M B DQ23 C24	MB_DATA[23]		
M B DQ22 B24	MB_DATA[22]		
M B DQ21 B20	MB_DATA[21]		
M B DQ20 B20	MB_DATA[20]		
M B DQ19 C25	MB_DATA[19]		
M B DQ18 D24	MB_DATA[18]		
M B DQ17 A21	MB_DATA[17]		
M B DQ16 D20	MB_DATA[16]		
M B DQ15 D18	MB_DATA[15]		
M B DQ14 C18	MB_DATA[14]		
M B DQ13 D14	MB_DATA[13]		
M B DQ12 C14	MB_DATA[12]		
M B DQ11 A20	MB_DATA[11]		
M B DQ10 A19	MB_DATA[10]		
M B DQ9 A16	MB_DATA[9]		
M B DQ8 A15	MB_DATA[8]		
M B DQ7 A13	MB_DATA[7]		
M B DQ6 D12	MB_DATA[6]		
M B DQ5 E11	MB_DATA[5]		
M B DQ4 B14	MB_DATA[4]		
M B DQ3 B14	MB_DATA[3]		
M B DQ2 A14	MB_DATA[2]		
M B DQ1 A11	MB_DATA[1]		
M B DQ0 C11	MB_DATA[0]		
M B A15 J25	MB_ADD[15]		
M B A14 J26	MB_ADD[14]		
M B A13 W25	MB_ADD[13]		
M B A12 L23	MB_ADD[12]		
M B A11 L25	MB_ADD[11]		
M B A10 U25	MB_ADD[10]		
M B A9 L24	MB_ADD[9]		
M B A8 M26	MB_ADD[8]		
M B A7 L26	MB_ADD[7]		
M B A6 N23	MB_ADD[6]		
M B A5 N24	MB_ADD[5]		
M B A4 N25	MB_ADD[4]		
M B A3 N26	MB_ADD[3]		
M B A2 P24	MB_ADD[2]		
M B A1 P26	MB_ADD[1]		
M B A0 T24	MB_ADD[0]		
M B DQ[63..0]	MB_ADD[15]		
M B DQ[63..0]	MB_ADD[14]		
M B DQ[63..0]	MB_ADD[13]		
M B DQ[63..0]	MB_ADD[12]		
M B DQ[63..0]	MB_ADD[11]		
M B DQ[63..0]	MB_ADD[10]		
M B DQ[63..0]	MB_ADD[9]		
M B DQ[63..0]	MB_ADD[8]		
M B DQ[63..0]	MB_ADD[7]		
M B DQ[63..0]	MB_ADD[6]		
M B DQ[63..0]	MB_ADD[5]		
M B DQ[63..0]	MB_ADD[4]		
M B DQ[63..0]	MB_ADD[3]		
M B DQ[63..0]	MB_ADD[2]		
M B DQ[63..0]	MB_ADD[1]		
M B DQ[63..0]	MB_ADD[0]		

AMD S1 SOCKET



TRACE FROM CAP TO CPU MUST BE LESS
THAN 1200MILS MAX NECKDOWN TO &
FROM CAPS IS 500MILS



5 M_A_DQ[63..0]	M A DQ[63..0]	M A DQM[7..0]	M A DQM[7..0] 5
4.5 M_A_A[15..0]	M A A[15..0]	M A DQS[7..0]	M A DQS[7..0] 5
		M A BA[2..0]	M A BA[2..0] 4.5
		M A CS[3..0]	M A CS[3..0] 4.5
		M A RAS#	M A RAS# 4.5
		M A CAS#	M A CAS# 4.5
		M A WE#	M A WE# 4.5
		M A CKE1	M A CKE1 4.5
		M A CKE0	M A CKE0 4.5
		M A ODT1	M A ODT1 4.5
		M A ODT0	M A ODT0 4.5

5 M_B_DQ[63..0]	M B DQ[63..0]	M B DQM[7..0]	M B DQM[7..0] 5
4.5 M_B_A[15..0]	M B A[15..0]	M B DQS[7..0]	M B DQS[7..0] 5
		M B BA[2..0]	M B BA[2..0] 4.5
		M B CS[3..0]	M B CS[3..0] 4.5
		M B RAS#	M B RAS# 4.5
		M B CAS#	M B CAS# 4.5
		M B WE#	M B WE# 4.5
		M B CKE1	M B CKE1 4.5
		M B CKE0	M B CKE0 4.5
		M B ODT1	M B ODT1 4.5
		M B ODT0	M B ODT0 4.5

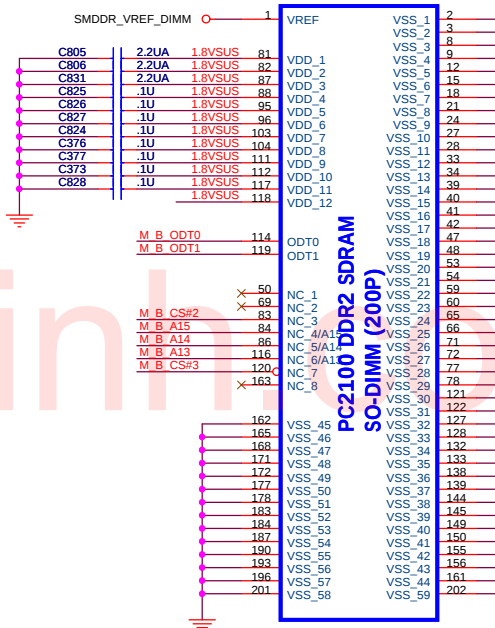
M B DQM[7..0]	M B DQM[7..0] 5
M B DQS[7..0]	M B DQS[7..0] 5
M B BA[2..0]	M B BA[2..0] 4.5
M B CS[3..0]	M B CS[3..0] 4.5
M B RAS#	M B RAS# 4.5
M B CAS#	M B CAS# 4.5
M B WE#	M B WE# 4.5
M B CKE1	M B CKE1 4.5
M B CKE0	M B CKE0 4.5
M B ODT1	M B ODT1 4.5
M B ODT0	M B ODT0 4.5

C51MVREF : W =20MIL AND SPACE = 20MIL

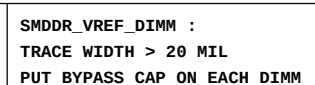


PROJECT : AT8
Quanta Computer Inc.

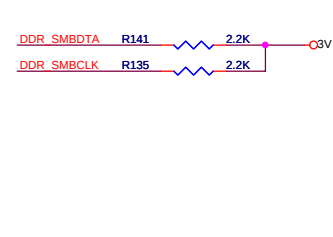
Size	Document Number	Rev
Custom	CPU(MEM/IF)	1A
Date: Wednesday, June 14, 2006	Sheet 3 of 39	

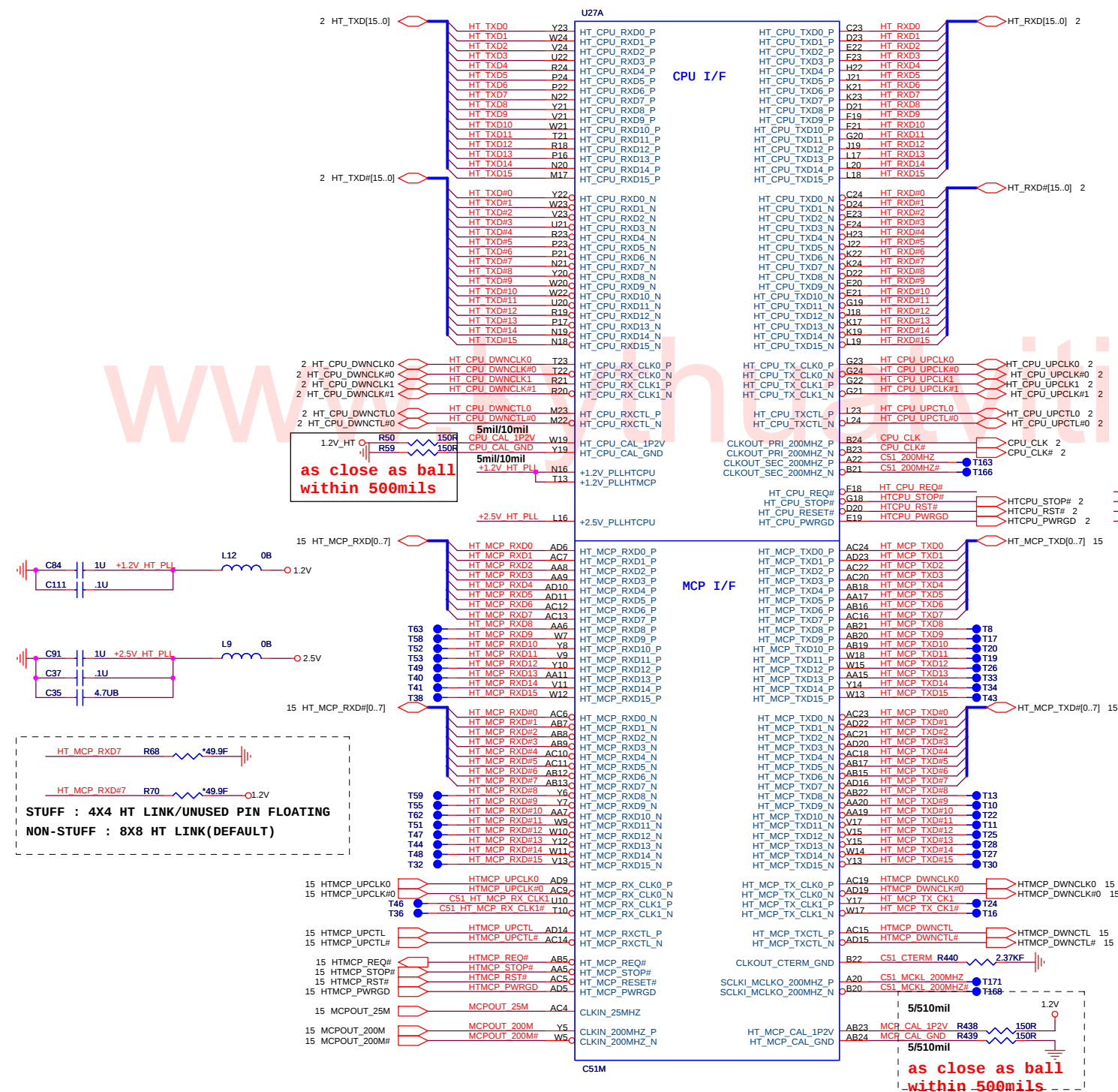


2,7,8,9,10,11,15,16,17,18,19,23,26,27,28,29,30,32,33,35,36,38
US 2,3,4,32,36,37



Address:92h

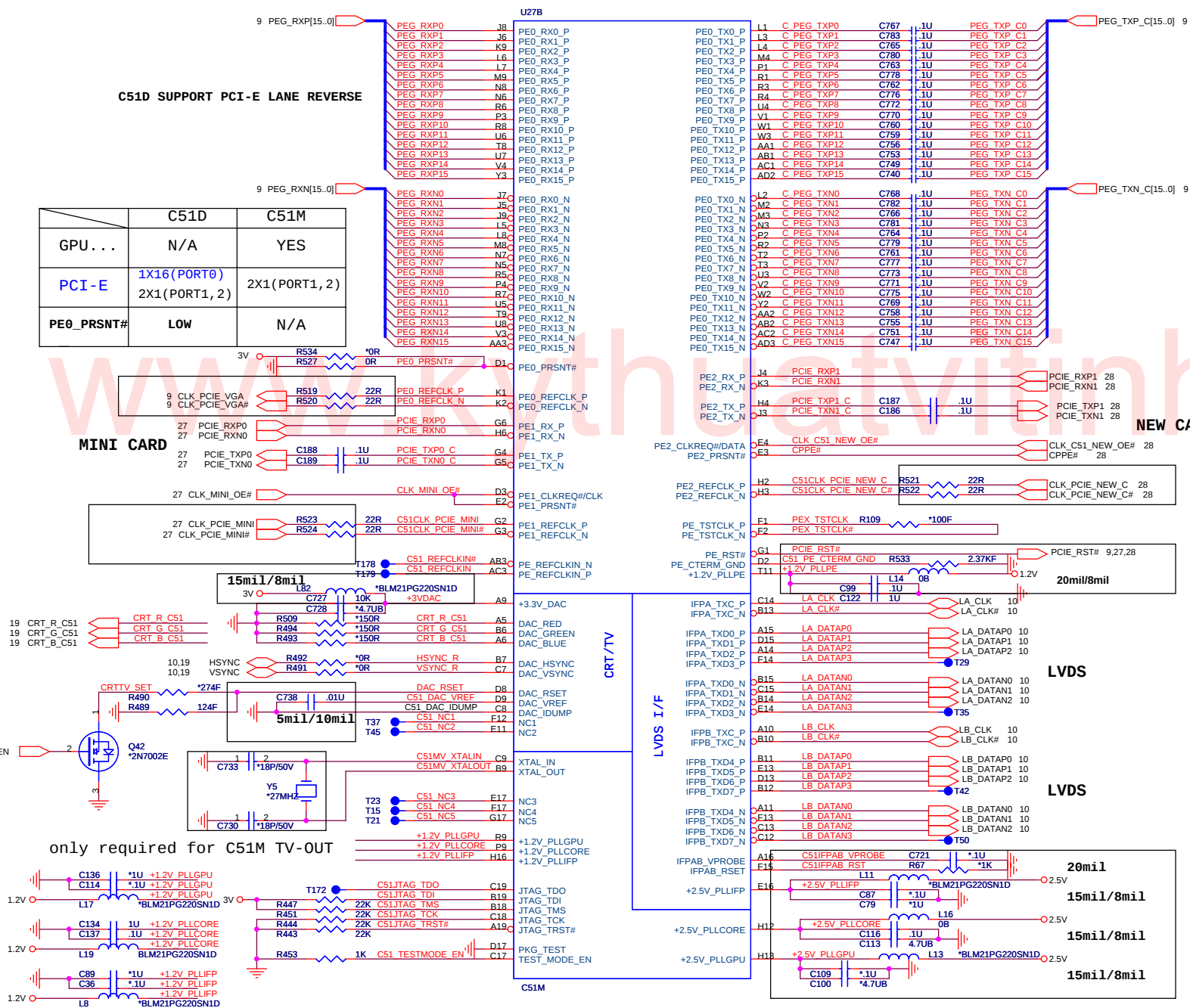




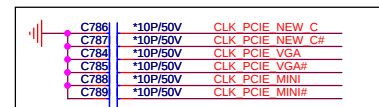
C51D SUPPORT PCI-E LANE REVERSE

	C51D	C51M
GPU...	N/A	YES
PCI-E	1X16(PORT0) 2X1(PORT1, 2)	2X1(PORT1, 2)
PE0_PRST#	LOW	N/A

MINI CARD



NEW CARD



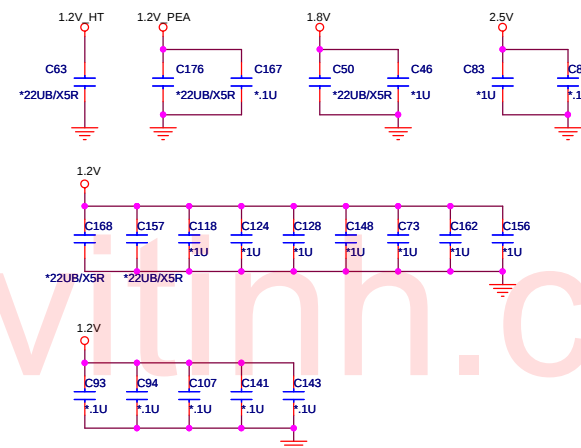
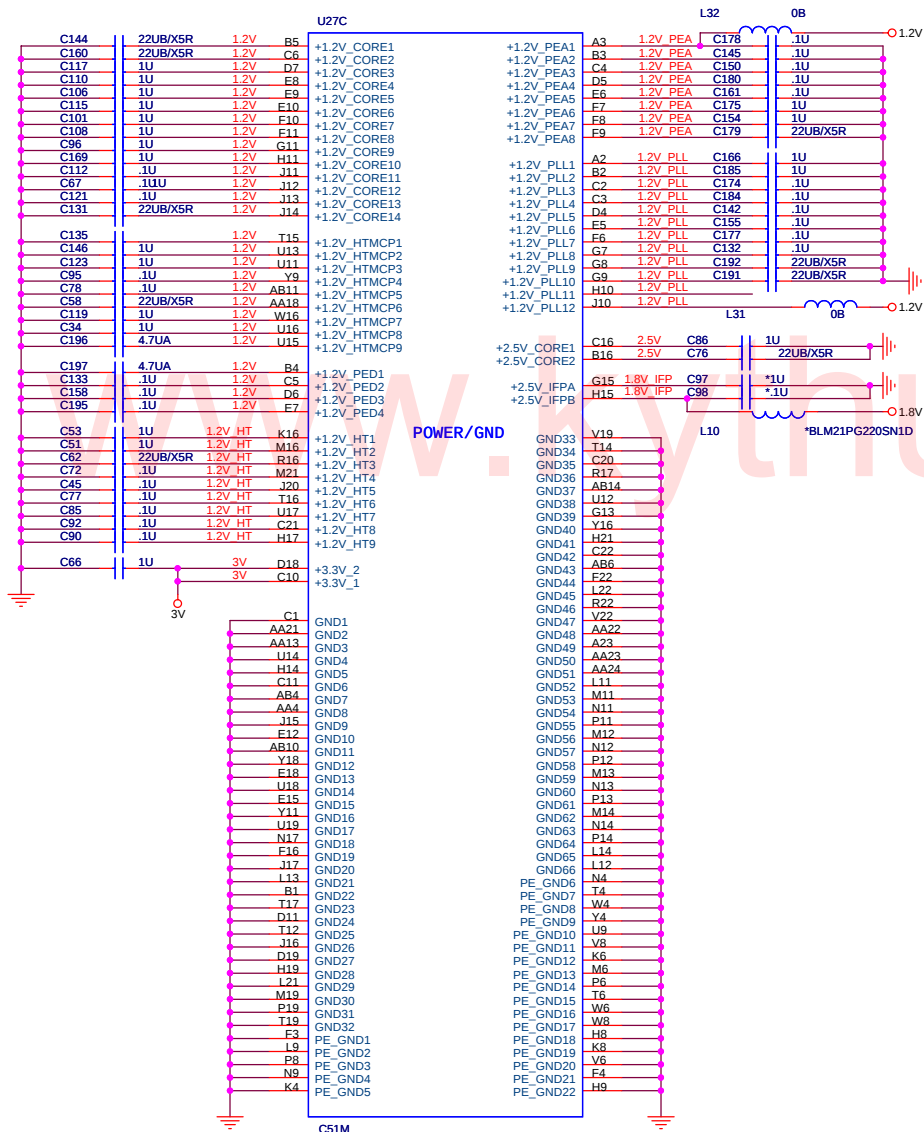
C51D Unused Power Ball Terminations	
C51D Signal Name	Termination
+1.2V_PLLGPU	Leave NC
+1.2V_PLLIFP	Leave NC
+2.5V_IFPA	Leave NC
+2.5V_IFPB	Leave NC
+2.5V_PLLIFP	Leave NC
+2.5V_PLLGPU	Leave NC
+3.3V_DAC	to GND directly
DAC_RSET	1240hm to GND
DAC_VREF	0.01u to GND

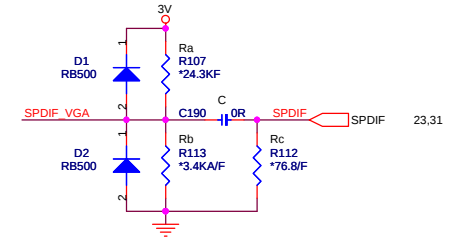
TRACE WIDTH :	
C51 PE_CTERM_GND	5mil/5mil
C51IFPAB_VPROBE	
C51IFPAB_RST	
C51_DAC_VREF	5mil/10mil
+1.2V_PLLPE	+1.2V_PLLIFP
+2.5V_PLLIFP	+1.2V_PLLCORE
+2.5V_PLLCORE	+1.2V_PLLGPU
+2.5V_PLLGPU	

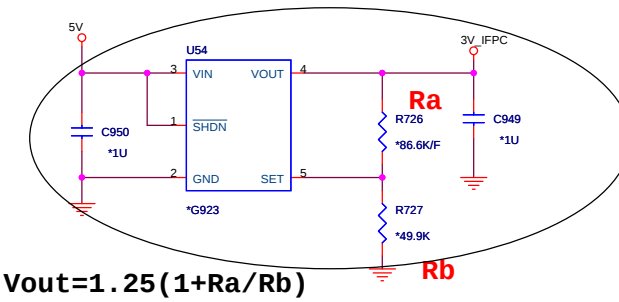
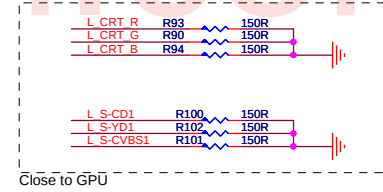
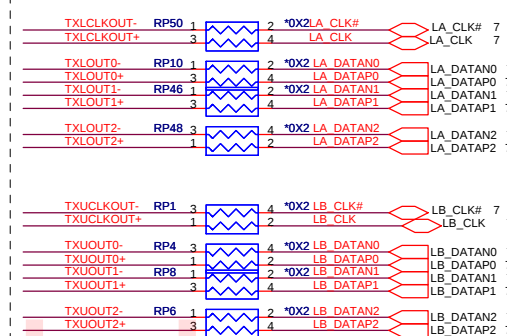


PROJECT : AT8
Quanta Computer Inc.

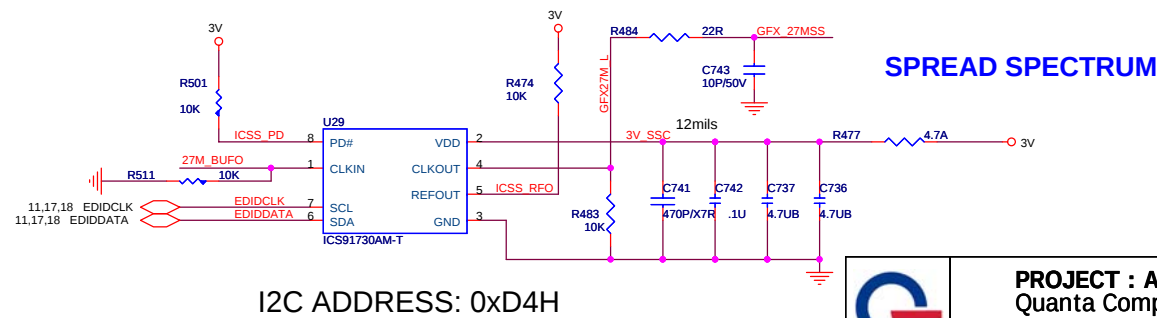
C51M/C51D POWER PLANE/GND & BYPASS







For HDMI
Nvidia's
PUN
issue

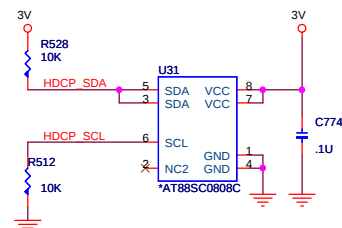
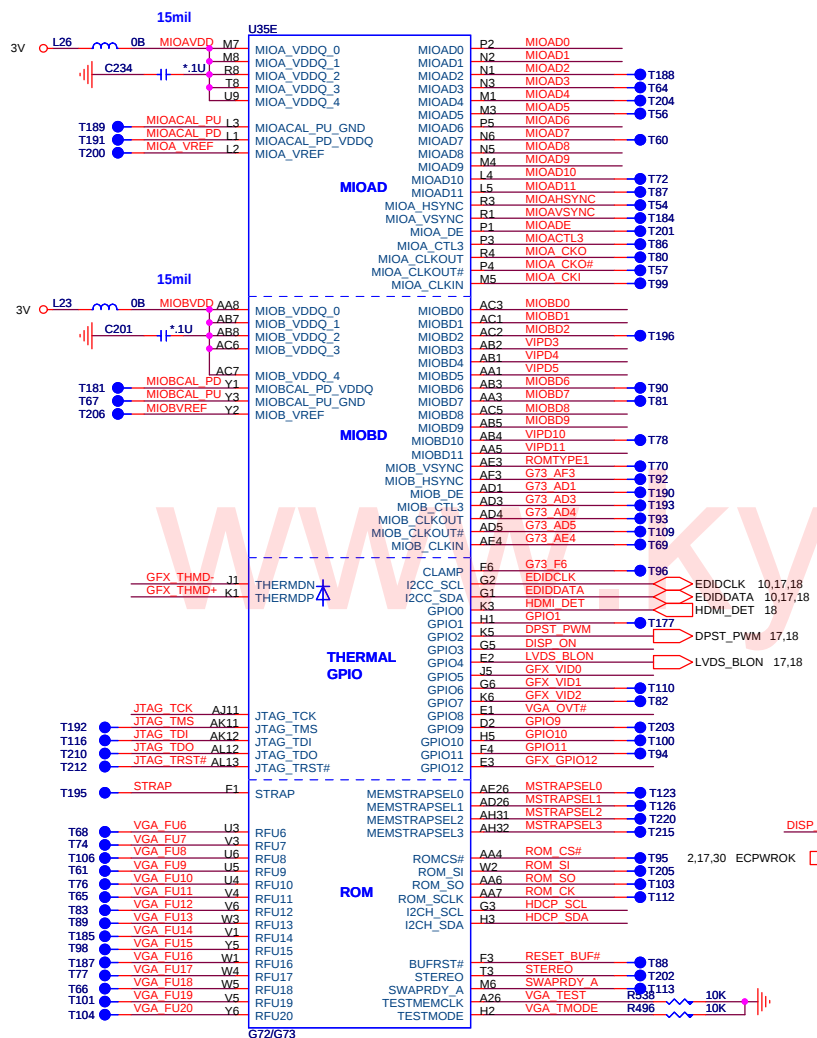


I2C ADDRESS: 0xD4H



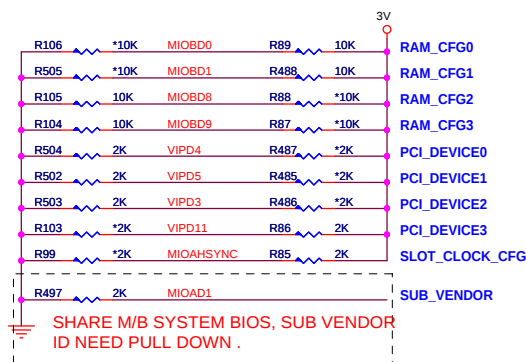
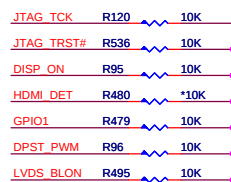
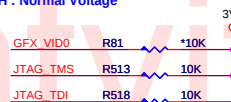
PROJECT : AT8
Quanta Computer Inc.

Size Custom	Document Number GFX(LVDS, CRT, TV)	Rev 2A
Date: Wednesday, June 14, 2006		Sheet 10 of 39



PCI_DEVICE[3:0]	DESCRIPTION
1000	G72M/G73M
0111	G72M-V/G73M-V
others	Reserved

GFX_VID0
L : Low Voltage
H : Normal Voltage

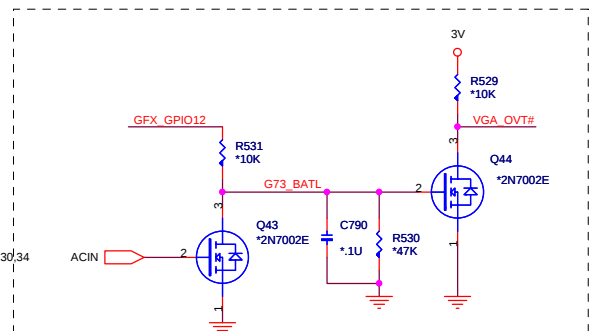


G72M VRAM Configuration Table

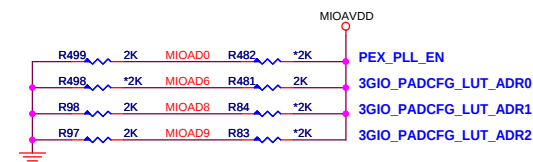
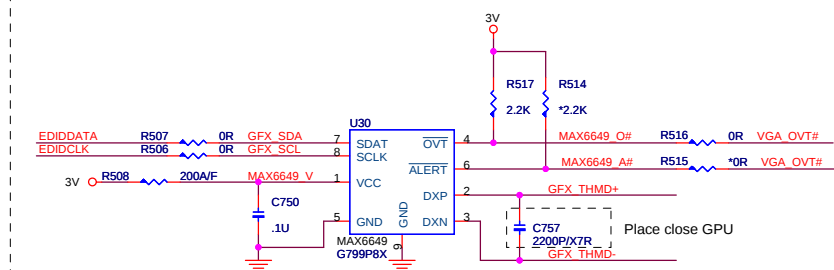
RAM_CFG[3:0]	DESCRIPTION	Vendor
0000	DDR2 16Mx16x4, 64bit, 128MB	Elpida
0001	DDR2 16Mx16x4, 64bit, 128MB	Samsung
0010	DDR2 16Mx16x4, 64bit, 128MB	Infineon
0011	DDR2 16Mx16x4, 64bit, 128MB	Hynix
0100	Reserved	
0101	DDR2 32Mx16x4, 64bit, 256MB	Samsung
0110	DDR2 32Mx16x4, 64bit, 256MB	Infineon
0111	DDR2 32Mx16x4, 64bit, 256MB	Hynix
1000	DDR2 16Mx16x2, 32bit, 64MB	Elpida
1001	DDR2 16Mx16x2, 32bit, 64MB	Samsung
1010	DDR2 16Mx16x2, 32bit, 64MB	Infineon
1011	DDR2 16Mx16x2, 32bit, 64MB	Hynix
others	Reserved	

G73M VRAM Configuration Table

RAM_CFG[3:0]	DESCRIPTION	Vendor
0000	DDR2 16Mx16x8, 128bit, 256MB	Elpida
0001	DDR2 16Mx16x8, 128bit, 256MB	Samsung
0010	DDR2 16Mx16x8, 128bit, 256MB	Infineon
0011	DDR2 16Mx16x8, 128bit, 256MB	Hynix
0100	Reserved	
0101	DDR2 32Mx16x8, 128bit, 512MB	Samsung
0110	DDR2 32Mx16x8, 128bit, 512MB	Infineon
0111	DDR2 32Mx16x8, 128bit, 512MB	Hynix
1000	DDR2 16Mx16x4, 64bit, 128MB	Elpida
1001	DDR2 16Mx16x4, 64bit, 128MB	Samsung
1010	DDR2 16Mx16x4, 64bit, 128MB	Infineon
1011	DDR2 16Mx16x4, 64bit, 128MB	Hynix
1100	Reserved	
1101	DDR2 32Mx16x4, 64bit, 256MB	Samsung
1110	DDR2 32Mx16x4, 64bit, 256MB	Infineon
1111	DDR2 32Mx16x4, 64bit, 256MB	Hynix

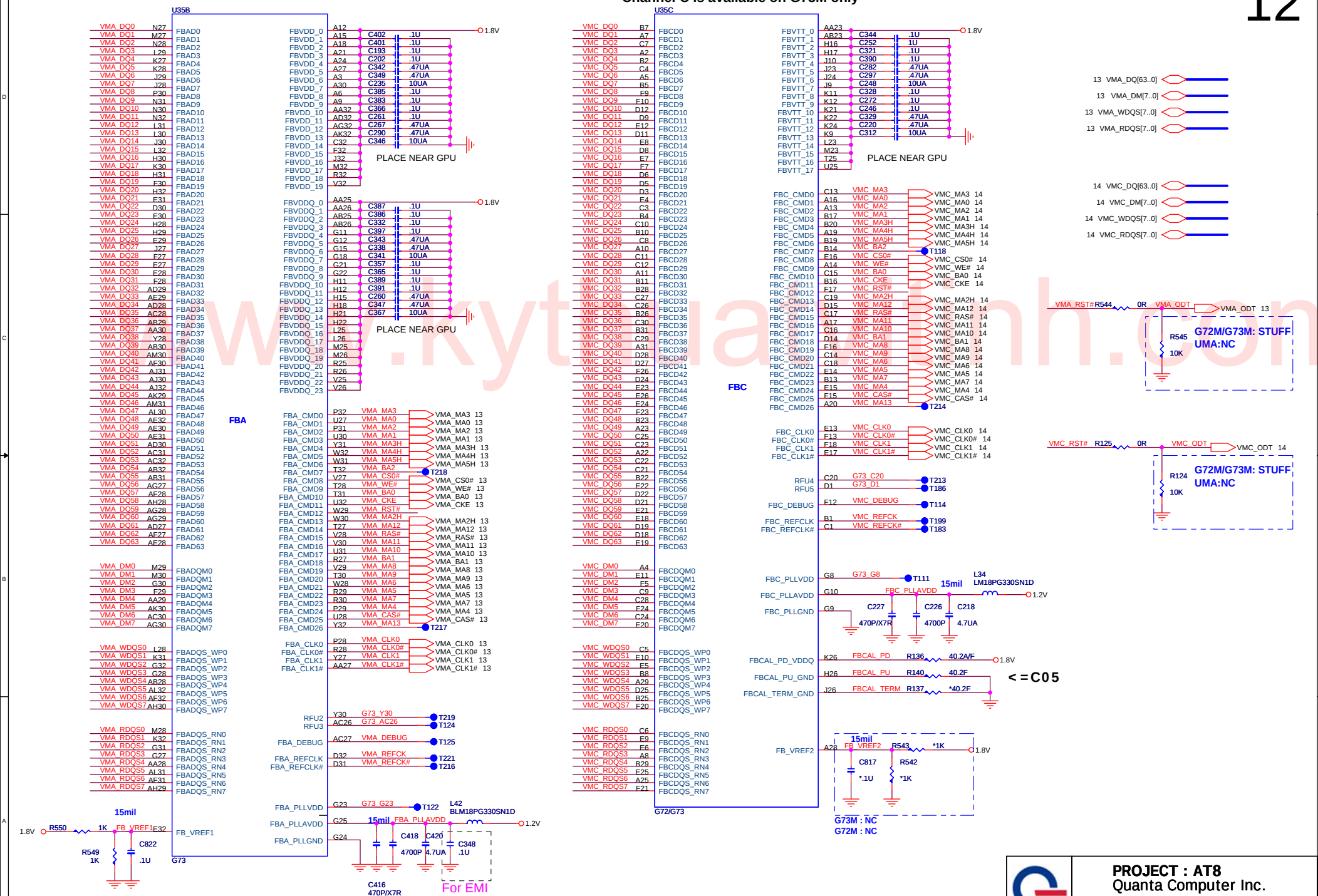


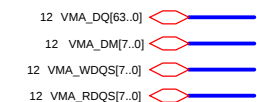
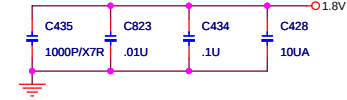
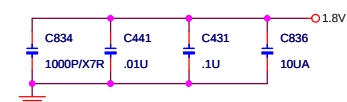
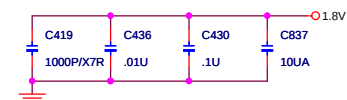
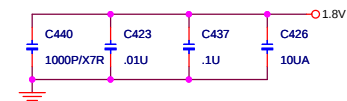
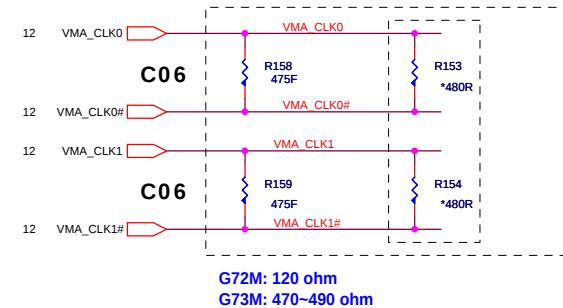
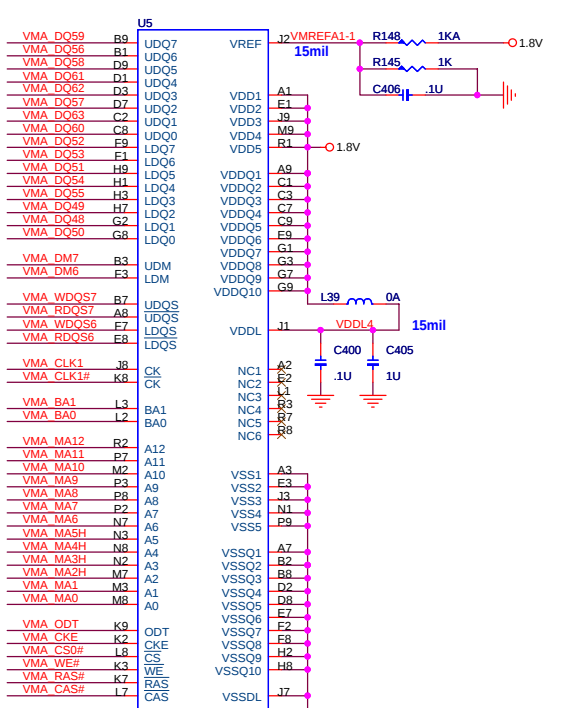
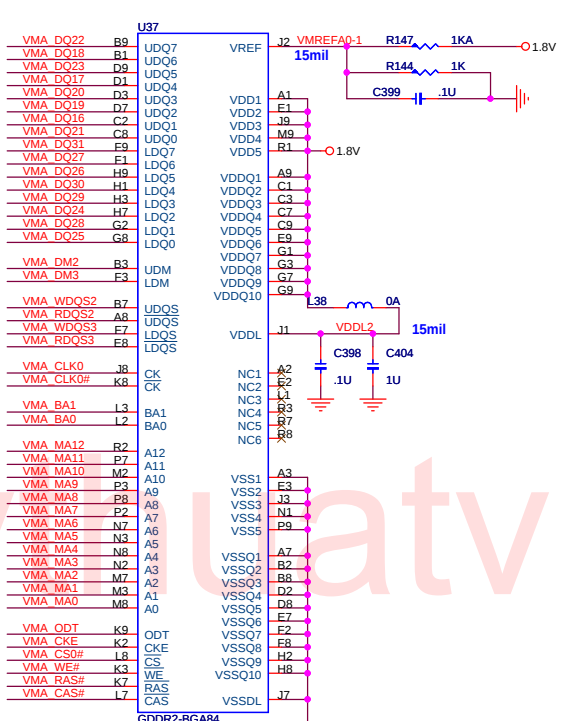
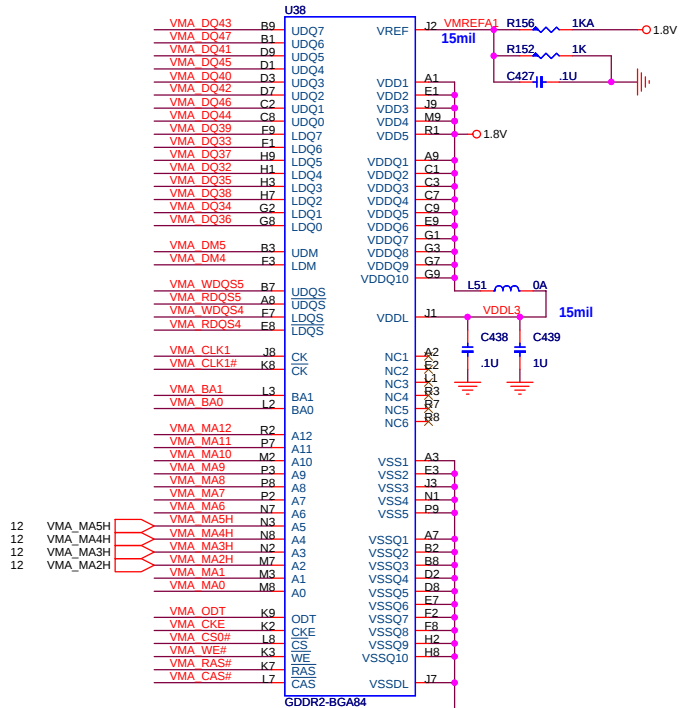
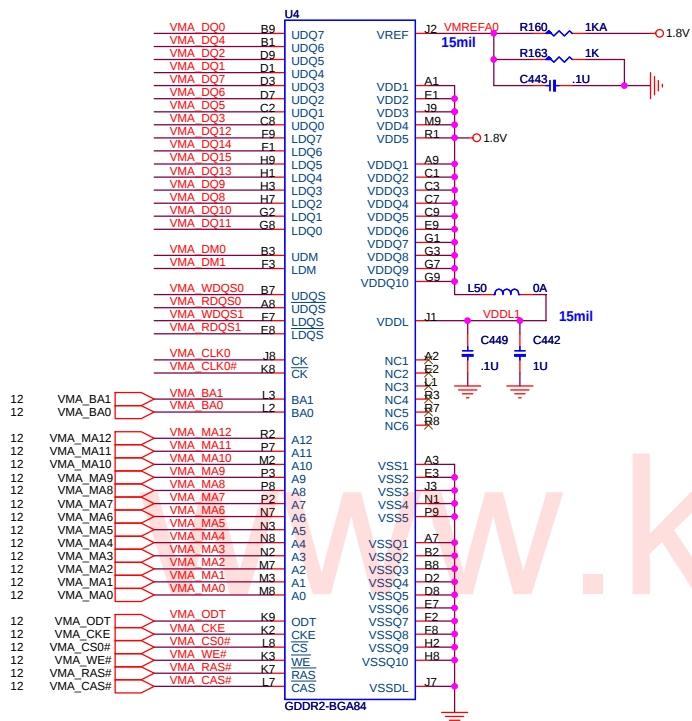
VGA THERMAIL CIRCUIT



PROJECT : AT8
Quanta Computer Inc.

Size Custom	Document Number GFX(ROM, GPIO, STRAP)	Re 2
Date: Wednesday, June 14, 2006	Sheet 11 of 39	


$$V_{REF} = F_{BVDDQ} * R_{bot} / (R_{top} + R_{bot})$$

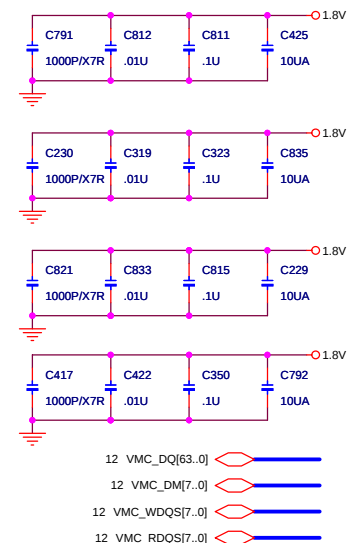
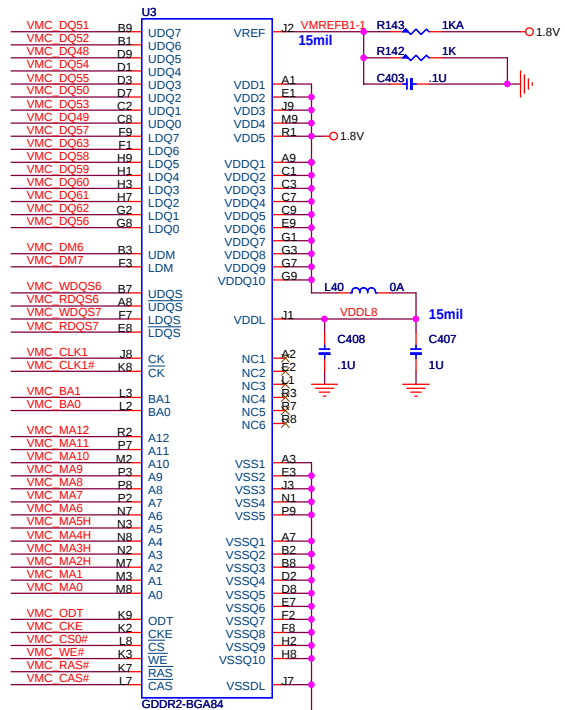
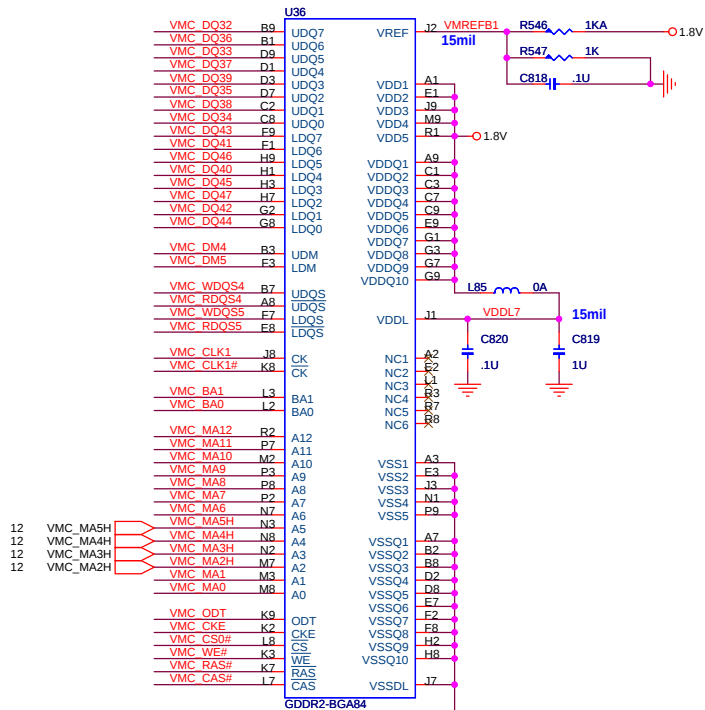
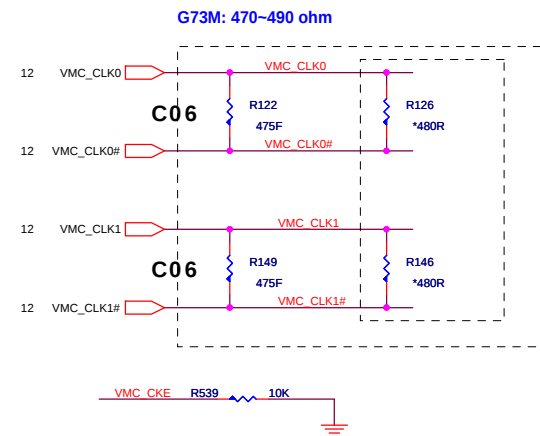
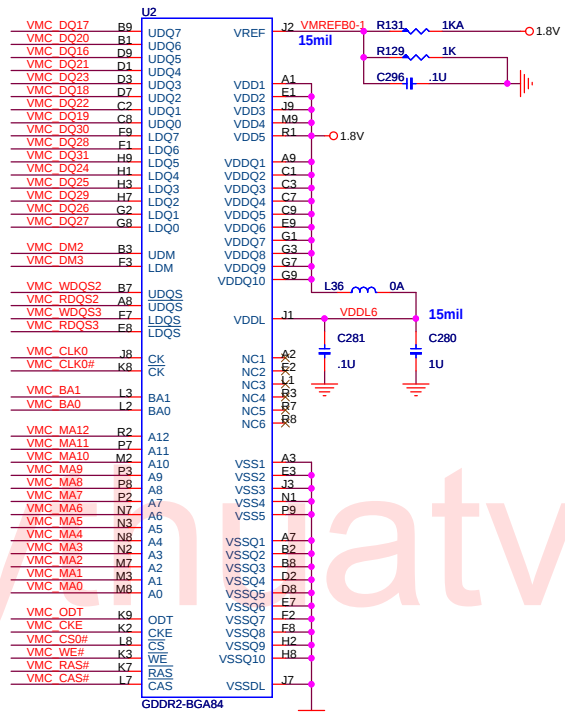
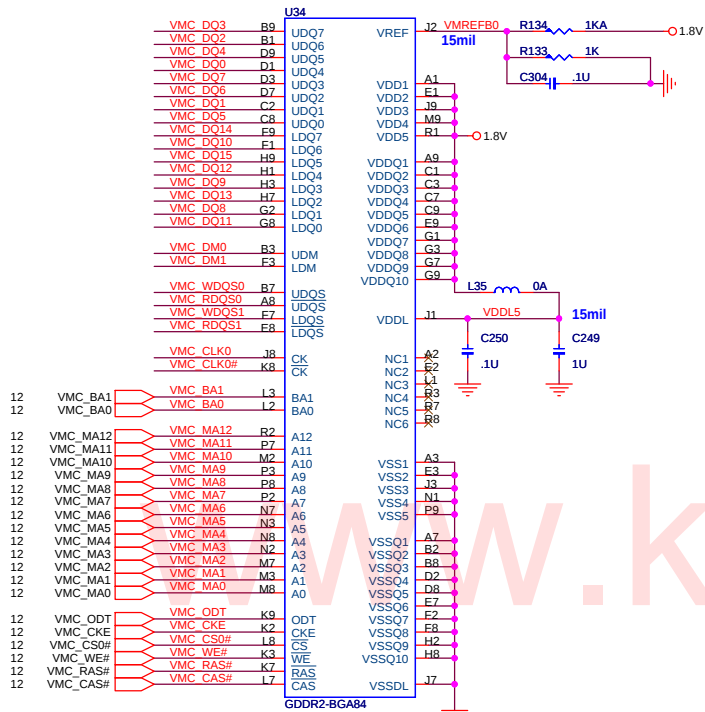


256Mb : AKD5JGAT*05
512Mb : AKD59G-T*01

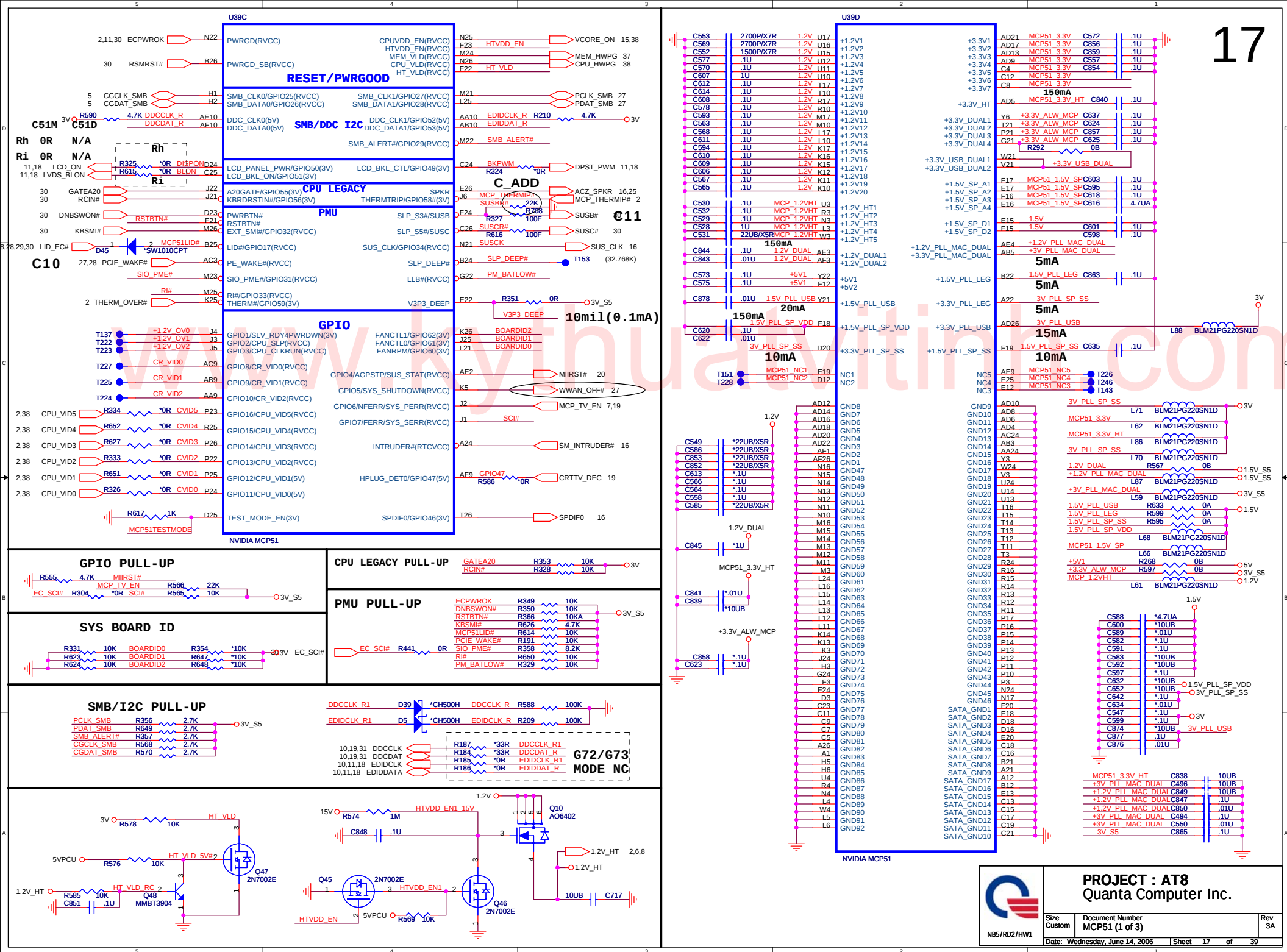


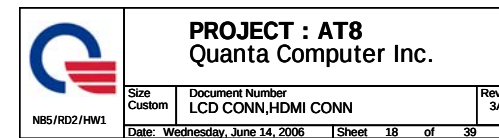
PROJECT : AT8
Quanta Computer Inc.

Size Custom	Document Number VRAM-1 (GDDR2)	Rev 1A
Date: Wednesday, June 14, 2006	Sheet 13 of 39	

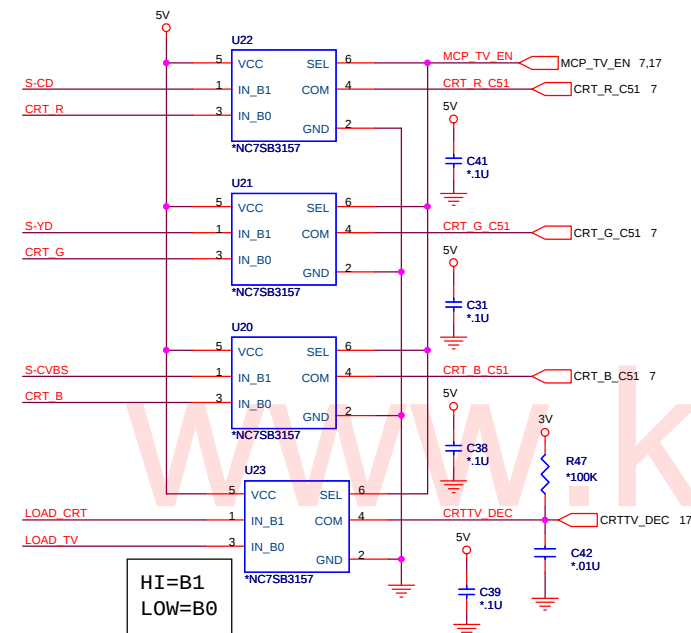


256Mb : AKD5JGAT*05
 512Mb : AKD59G-T*01

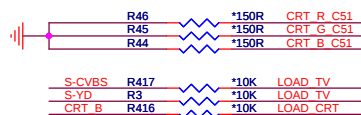




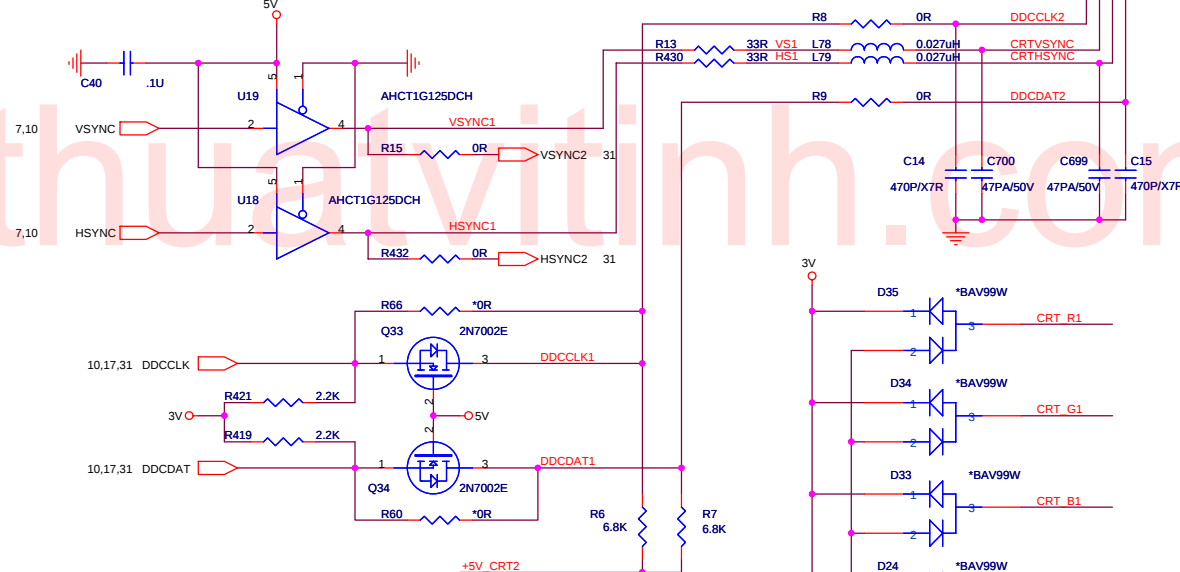
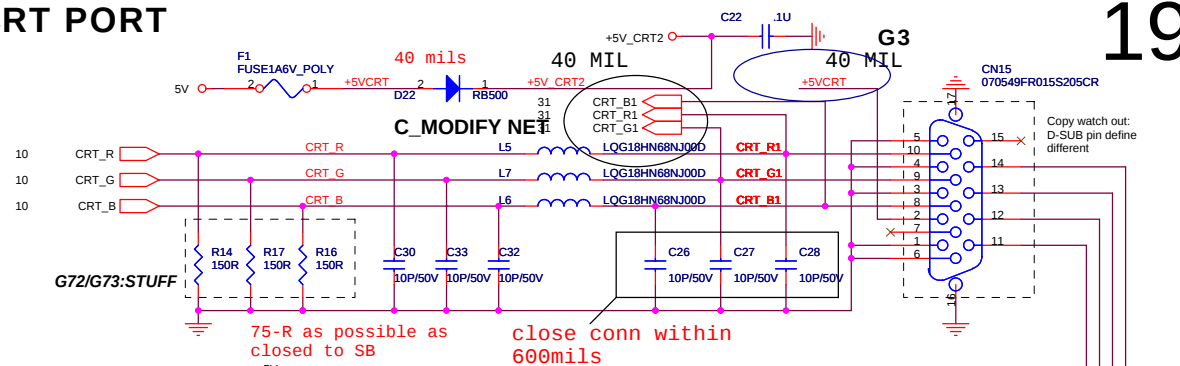
For UMA only



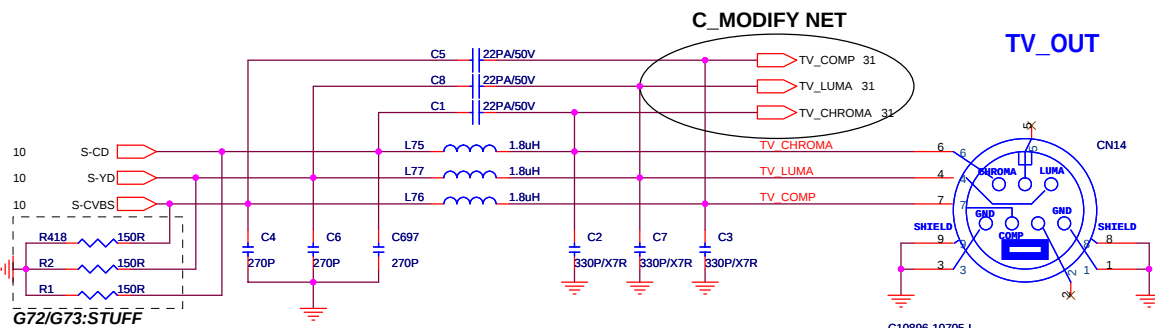
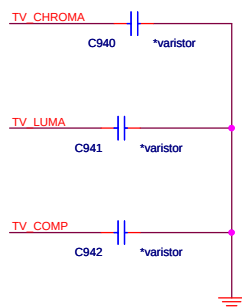
close within 600mils



CRT PORT



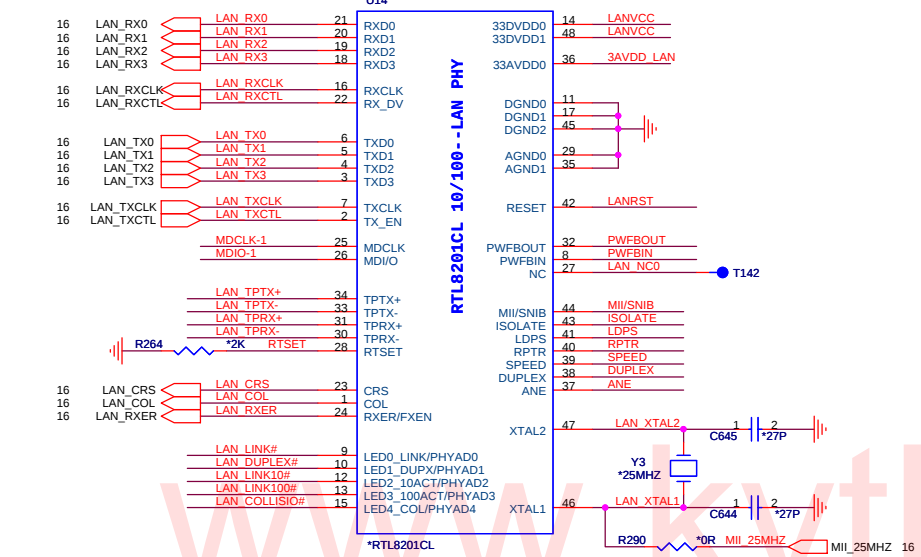
C13



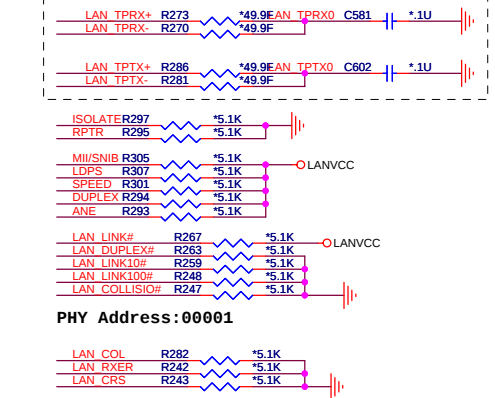
PROJECT : AT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CRT_TV_OUT	2A
Date: Thursday, June 15, 2006	Sheet 19 of 39	

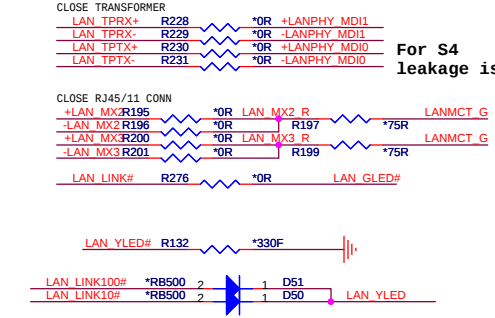
10/100M



Close To RTL8201CL

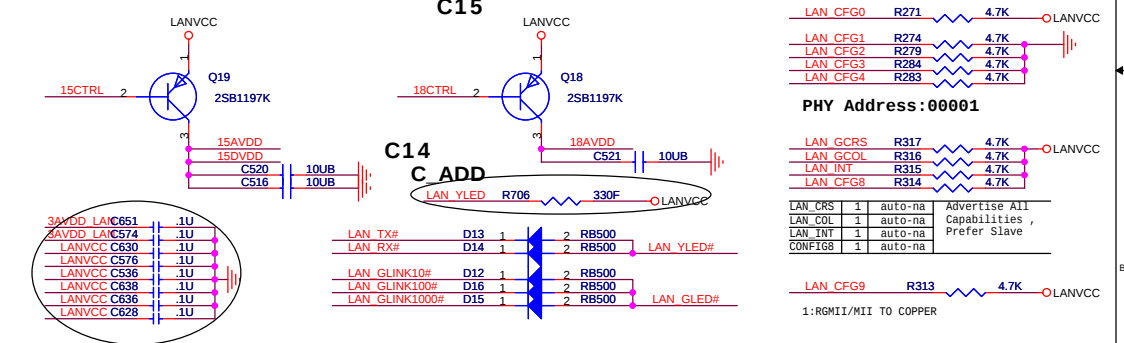
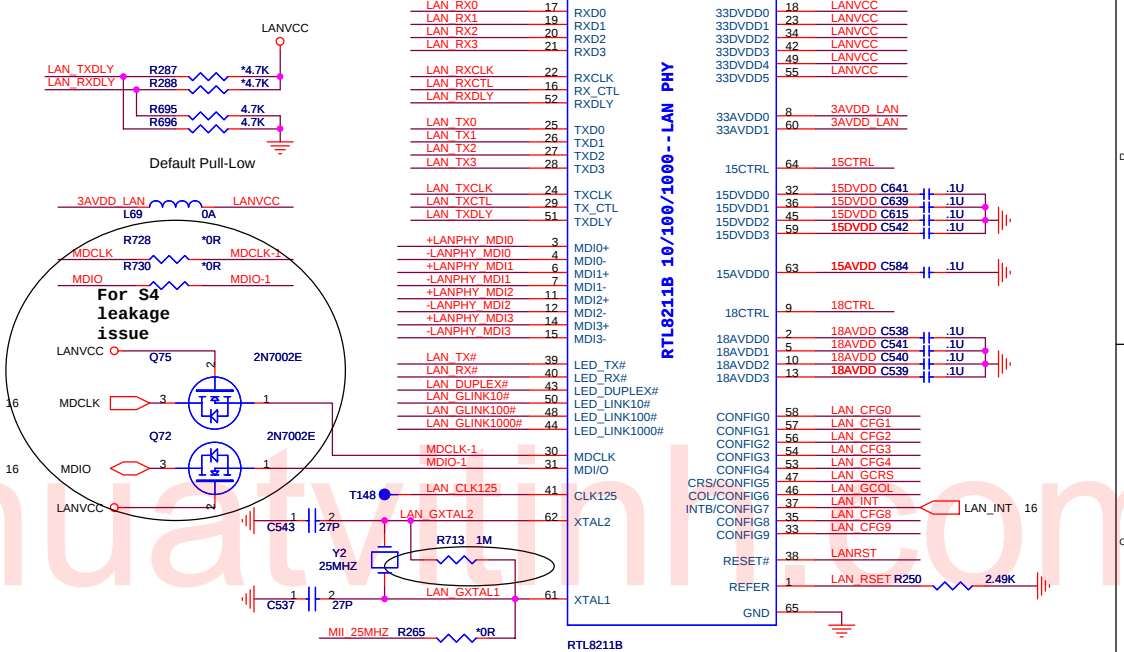


LAN_COL	1	Default	RTL8201B LED
LAN_RXER_R	1	Default	Fiber Mode
LAN_CRS	0	Default	Ensure operating at normal mode

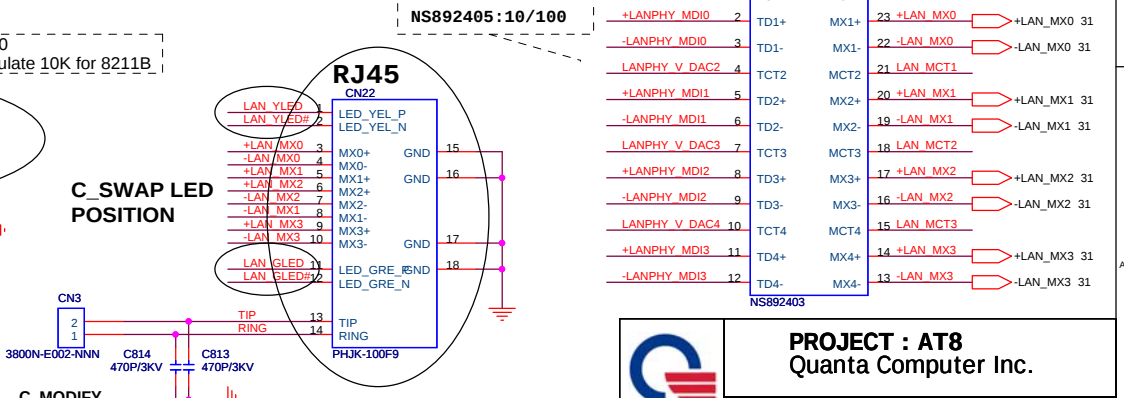


LINK10/100# assert high while system power up.

10/100/1000M



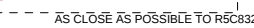
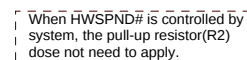
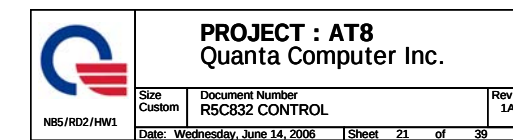
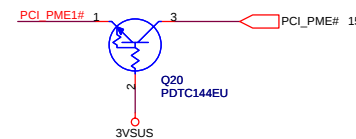
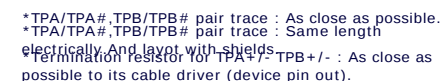
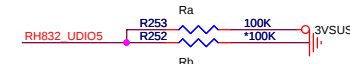
LAYOUT REPLACE_C FOR EMI



C MODIFY TIP/RING: 20/20

PROJECT : AT8
Quanta Computer Inc.

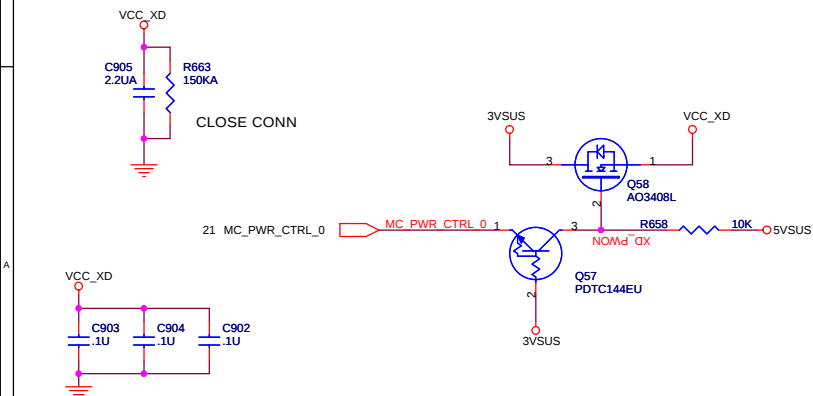
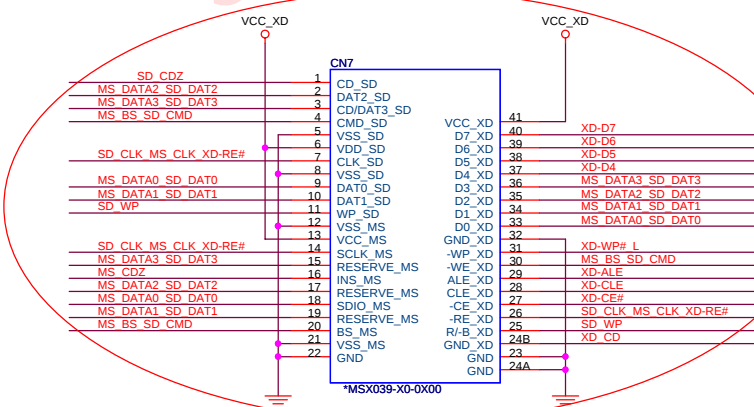
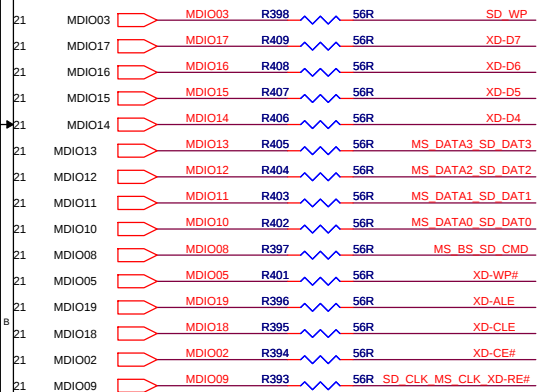
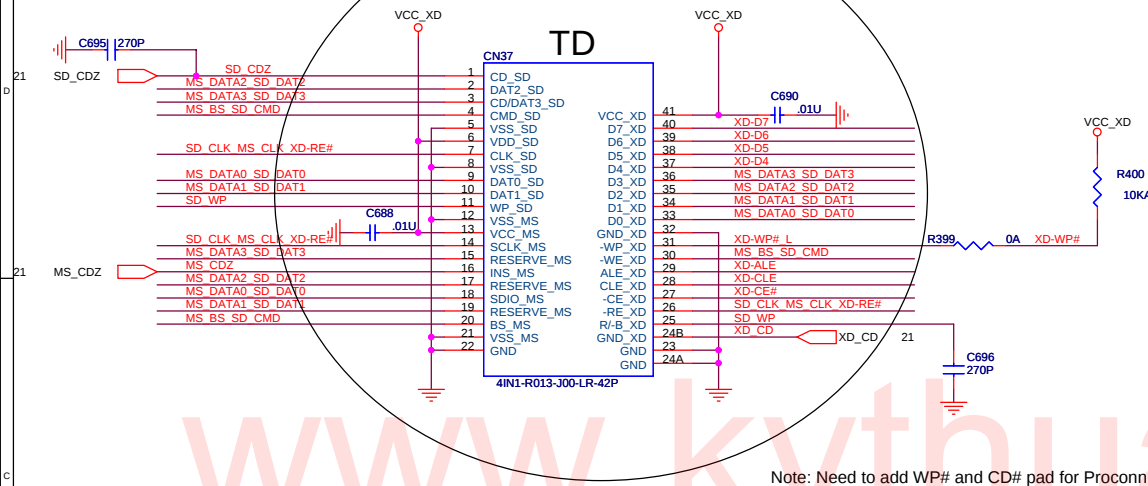
Size Custom	Document Number LAN PHY RTL8211B/8201CL_RJ45	Rev 3A
Date: Wednesday, June 14, 2006	Sheet 20	of 39



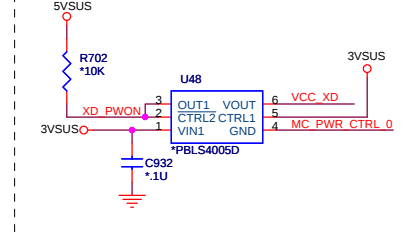
4 IN1 CARD READER

XD, MMC/SD, MS/MSP

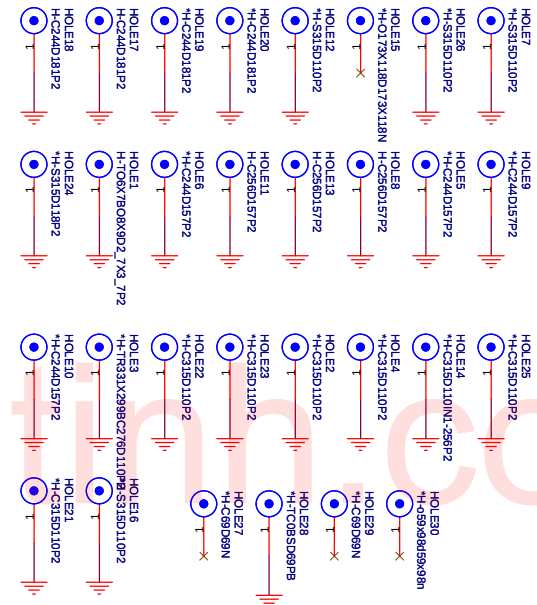
CHECK CONN.



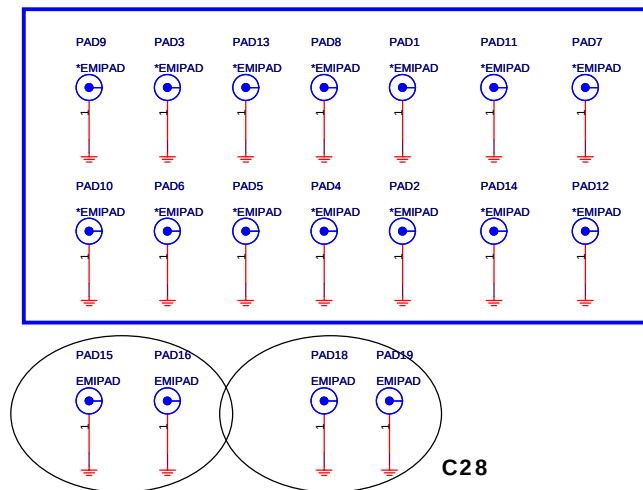
Reserve



SCREW HOLE



EMI PAD

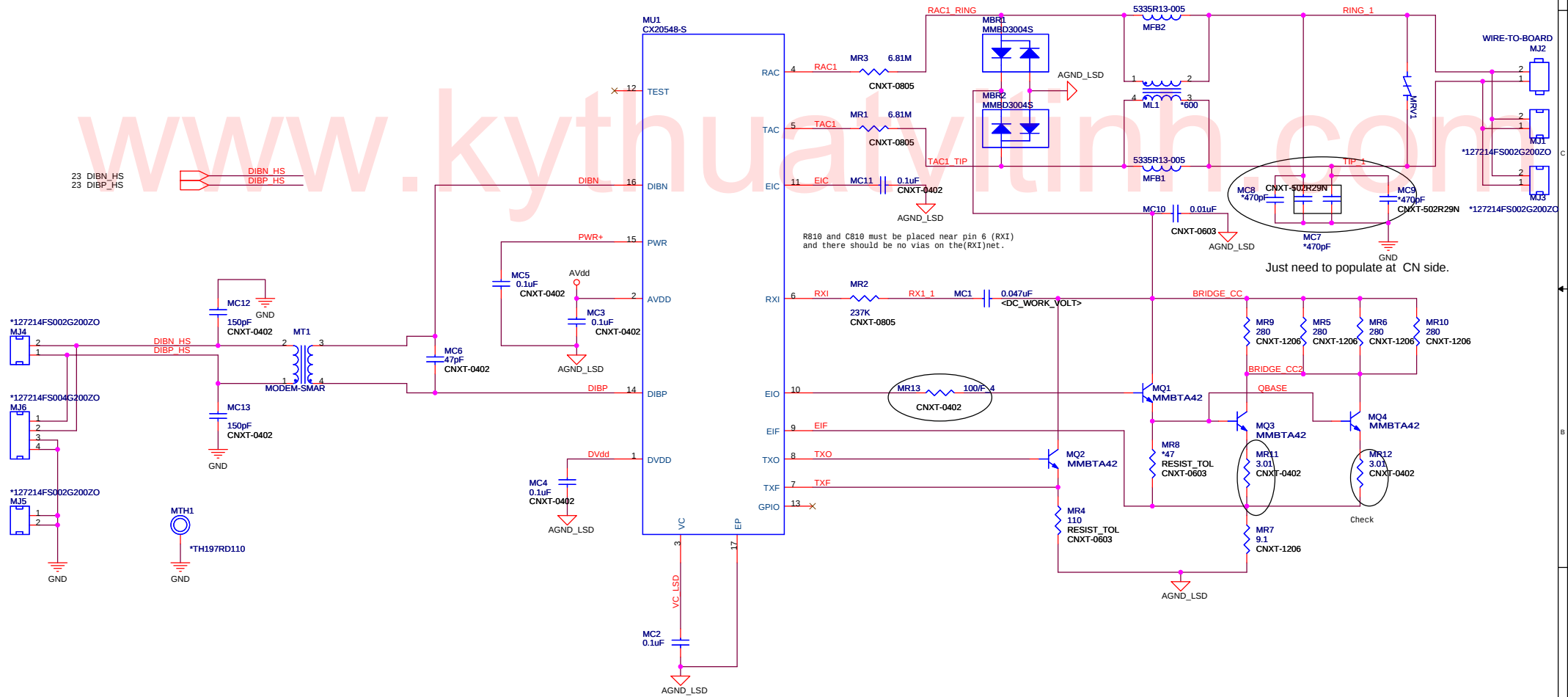


C_ADD

		PROJECT : AT8 Quanta Computer Inc.		Rev 3A
		Size Custom	Document Number CARD READER CONN	
Date: Wednesday, June 14, 2006		Sheet 22	of 39	

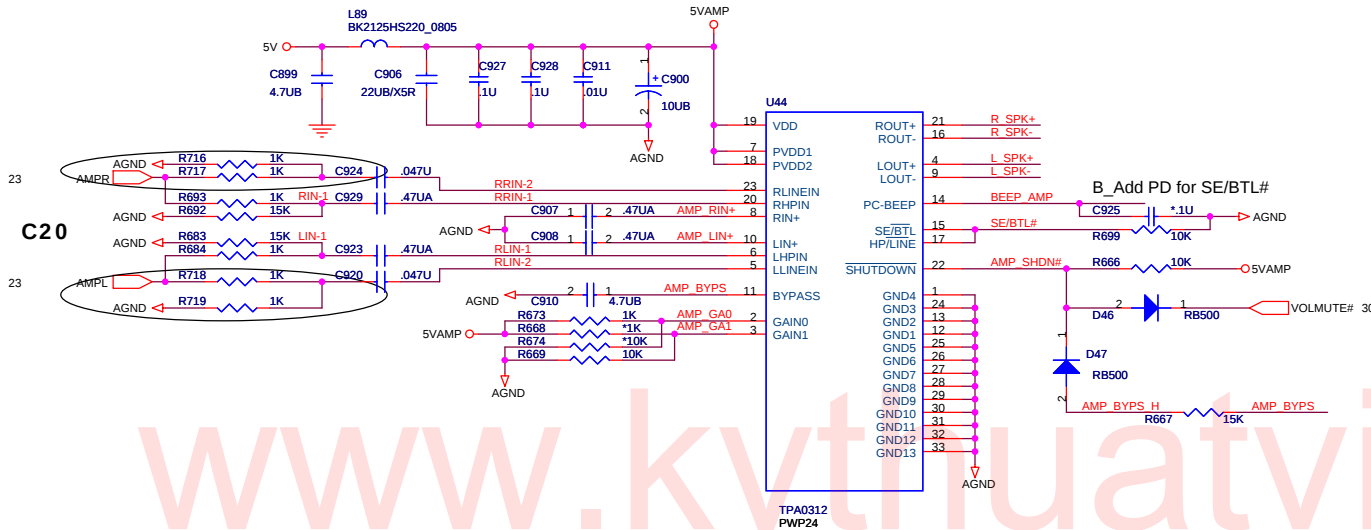
Revision History

REV	Description	Date
0	Initial Release	April 26, 2005
4		



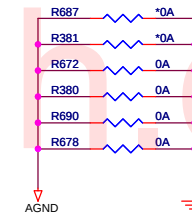
PROJECT : AT8
Quanta Computer Inc.

Size Custom	Document Number MODEM (DAA)	Rev 2A
Date: Wednesday, June 14, 2006	Sheet 24 of 39	

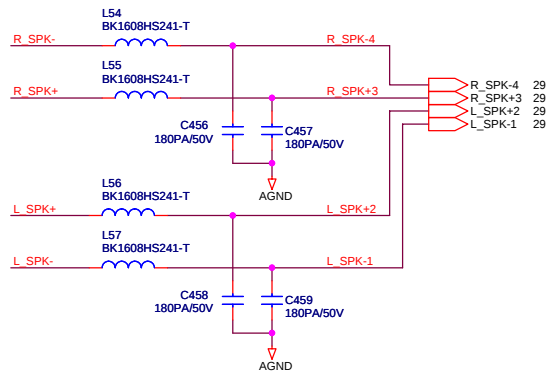


0312 Gain Table

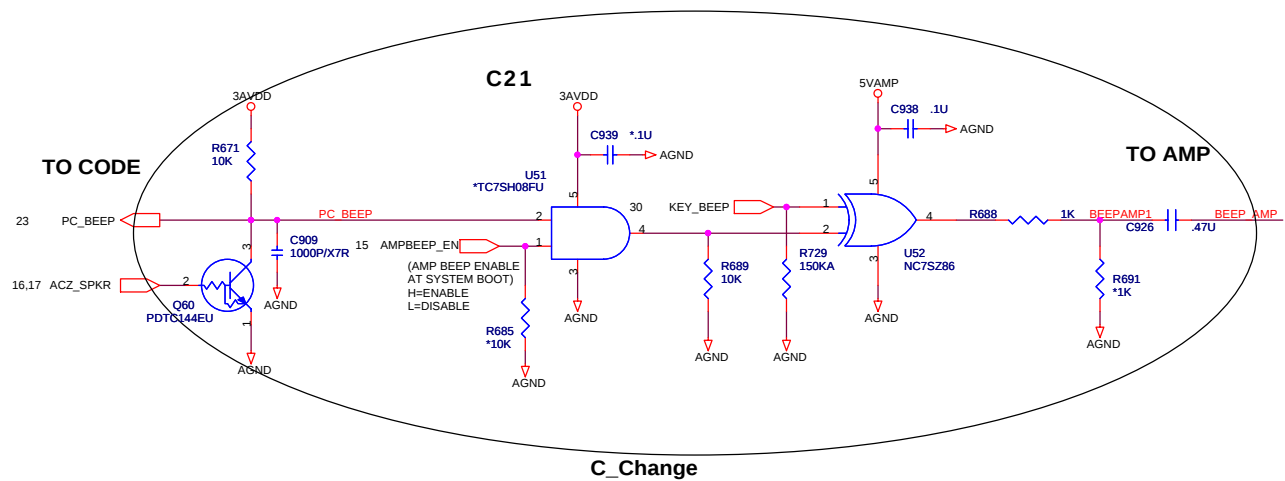
GAIN0	GAIN1	SE/BTL	AV(INV)
0	0	0	6dB
0	1	0	10dB
1	0	0	15.6dB
1	1	0	21.6dB
x	x	1	4.1dB



INT. SPEAKER

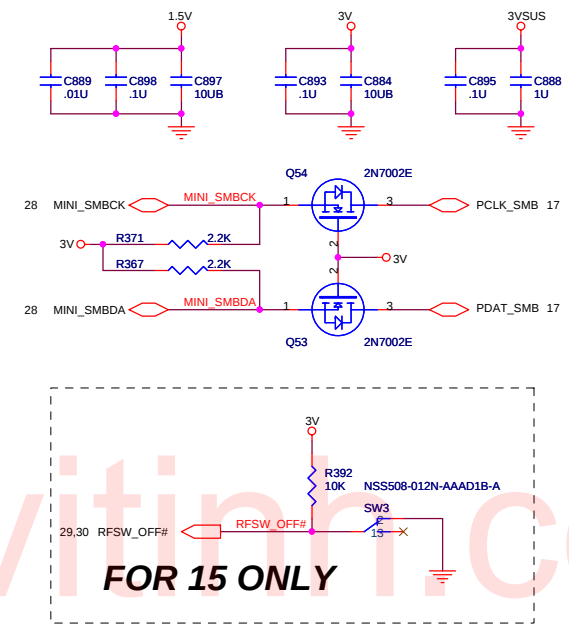


PCSPK BEEP





27



WWAN_ON

2

3

Q73

*PDTIC144EU

WWAN_ON

WWAN_OFF

2

1

RB500

RB500

WWAN_OFF# 17

WWAN_ON

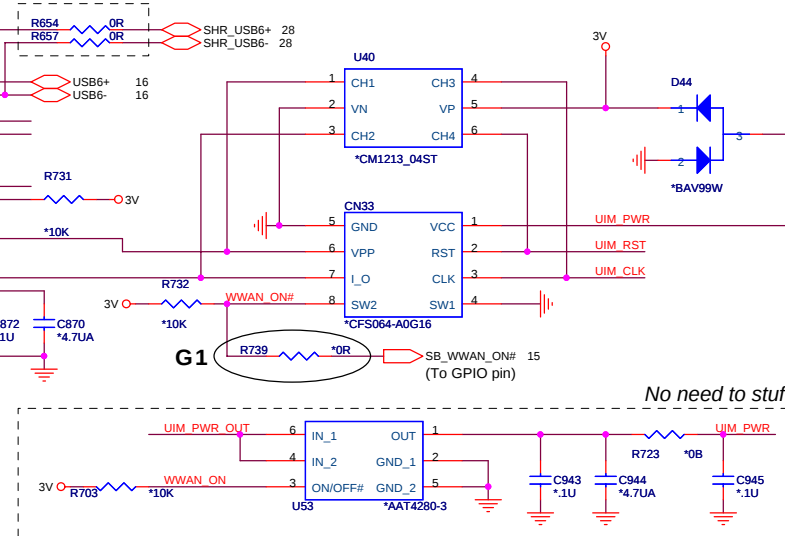
2

1

G1

UIM DATA R740 *10K UIM PWR

UIM PWR OUT R7722 *10K UIM PWR

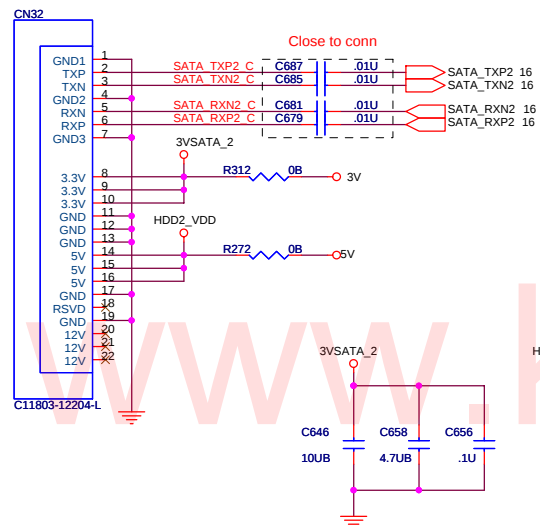


NB5/RD2/HWJ

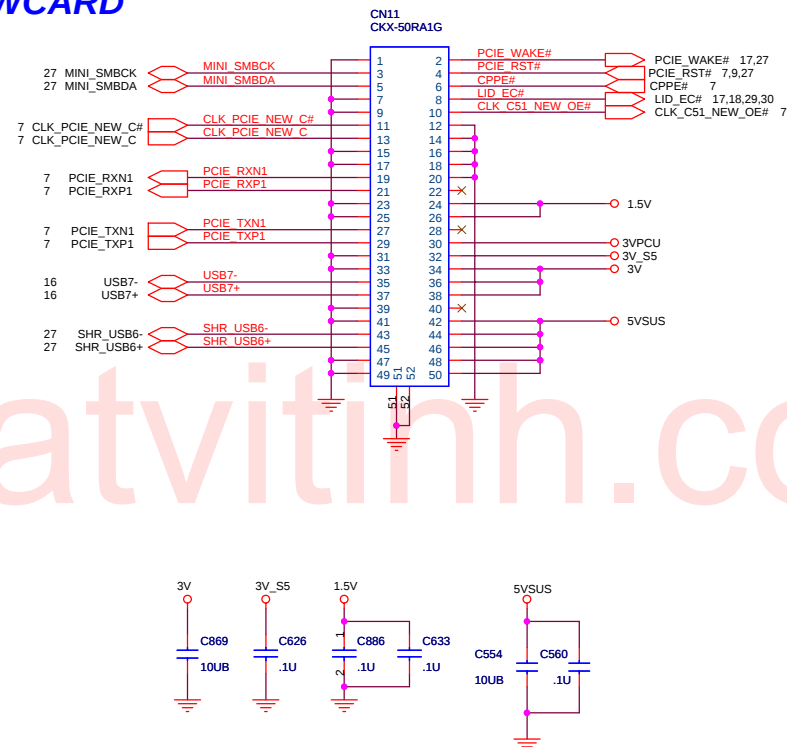
PROJECT : AT8
Quanta Computer Inc.

Size Custom	Document Number MINI CARD	Rev 3A
Date: Friday, June 16, 2006	Sheet 27 of 39	

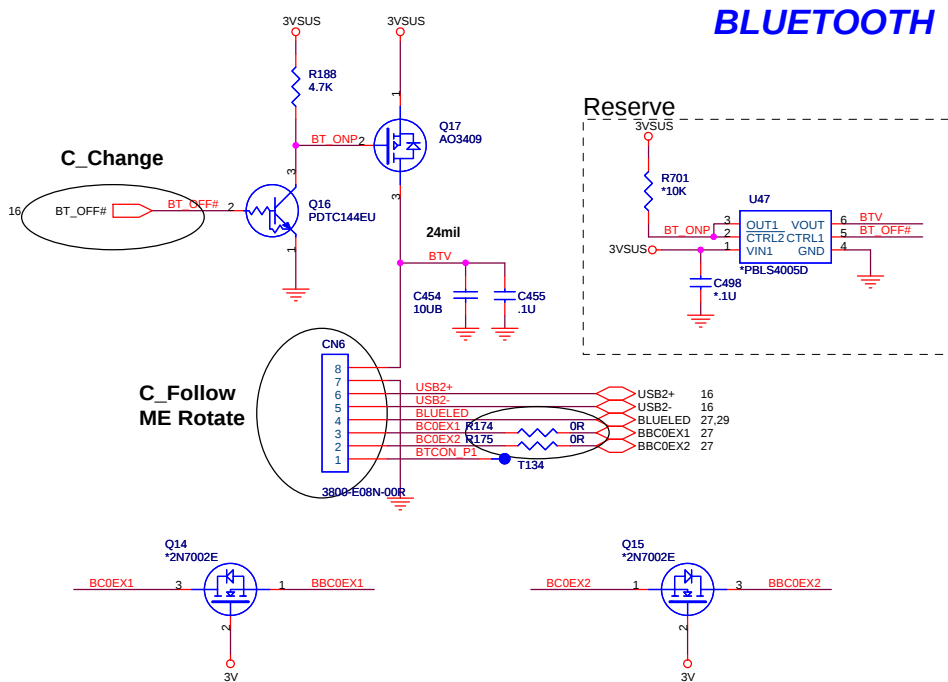
SATA_2 CONNECTOR For 17"W Second HDD



NEWCARD



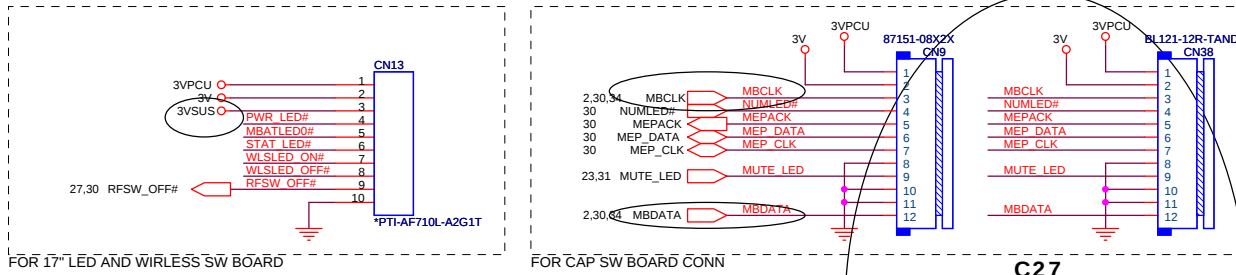
BLUETOOTH



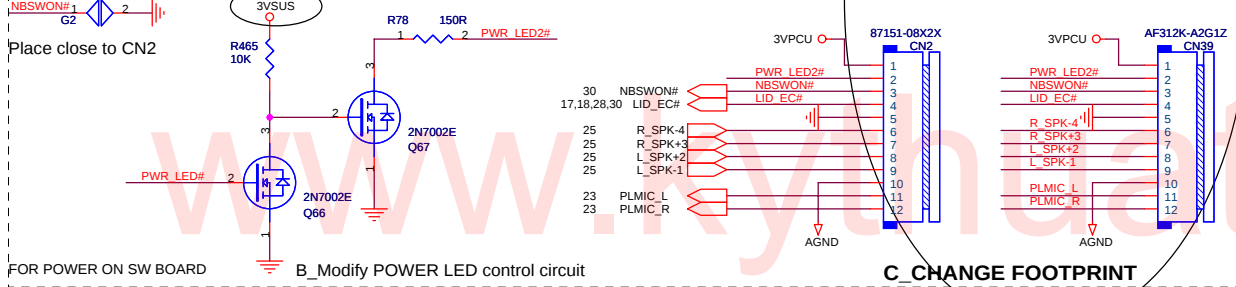
PROJECT : AT8
Quanta Computer Inc.

Size Custom	Document Number NEW CARD/BT	Rev 3A
Date: Wednesday, June 14, 2006	Sheet 28 of 39	

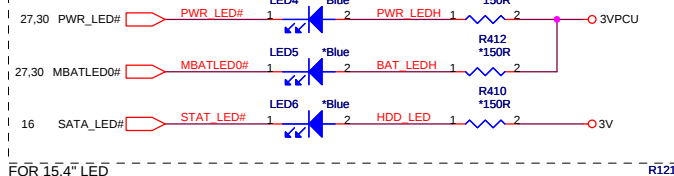
C_RESERVE FOR 2'ND SOURCE
C_CHANGE FOOTPRINT



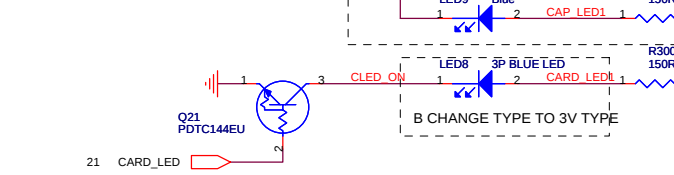
IB_ADD *ST_PAD1 C_MODIFY



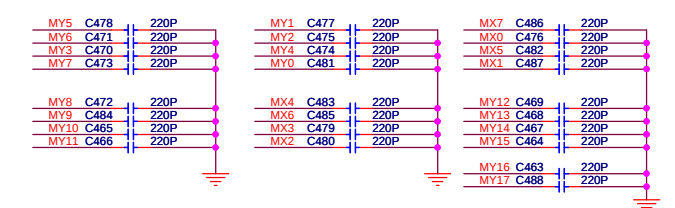
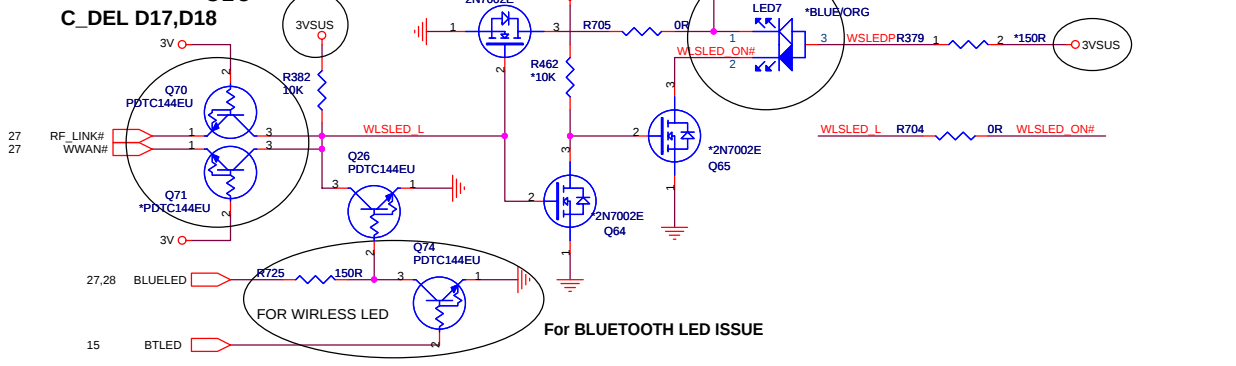
LED	*Blue	R411 *150P
-----	-------	---------------



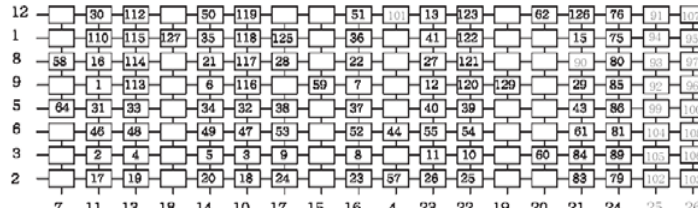
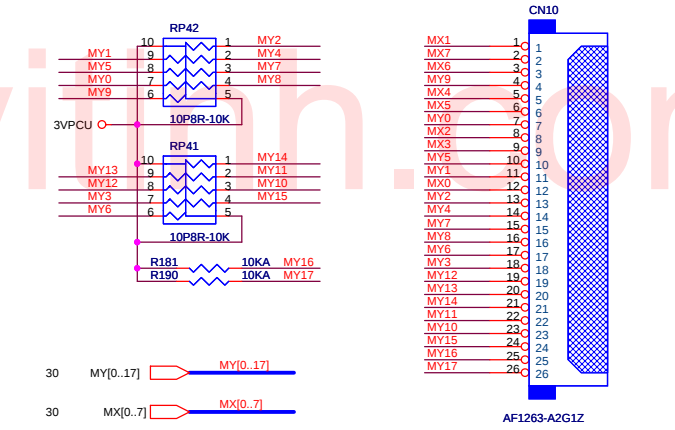
30 CAPSLED# CAPSLED# 1 2 CAP_LED 1 R442 1506

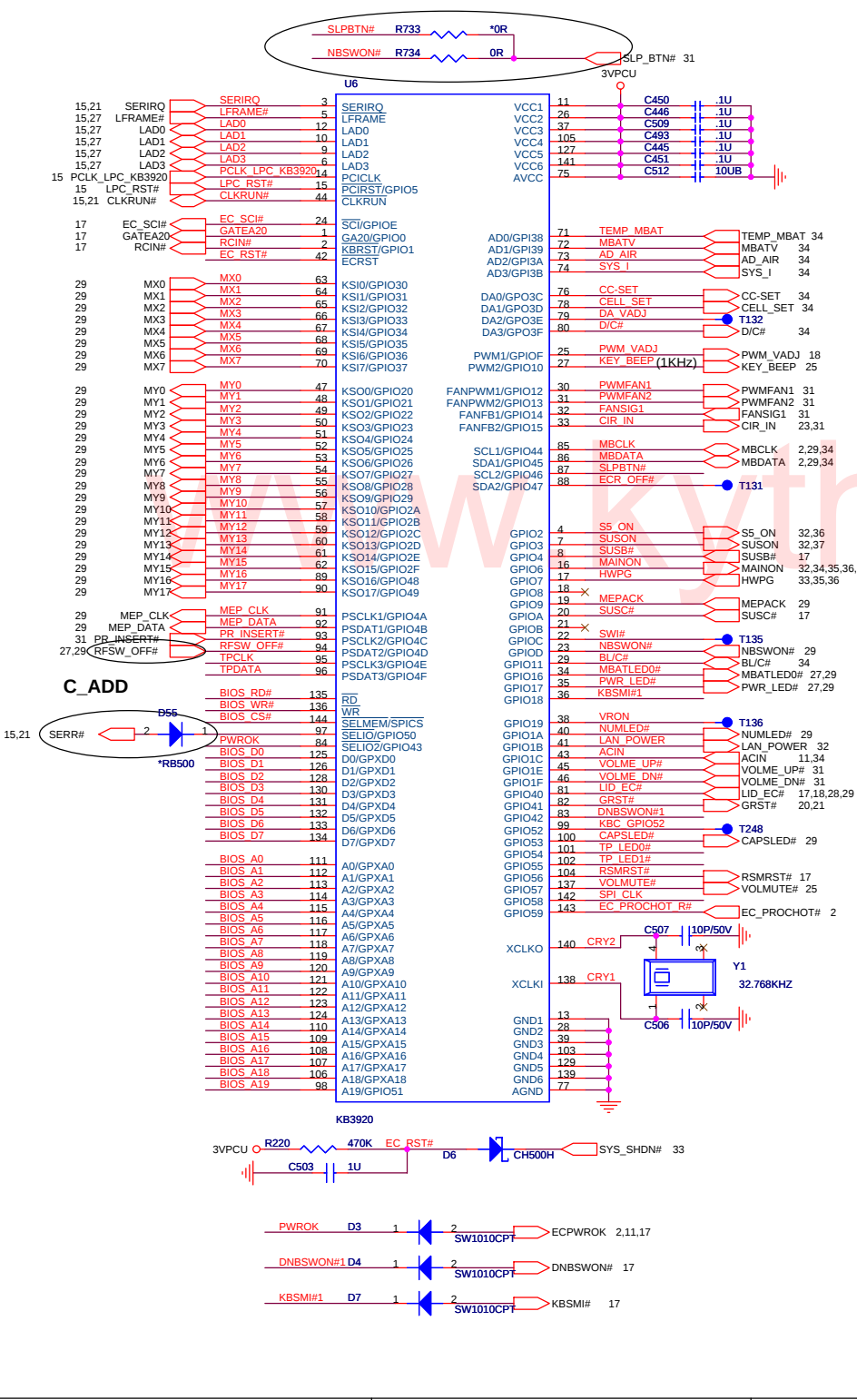


C23 Q28 3V



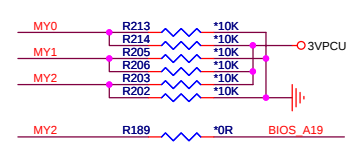
KEYBOARD PULL-UP





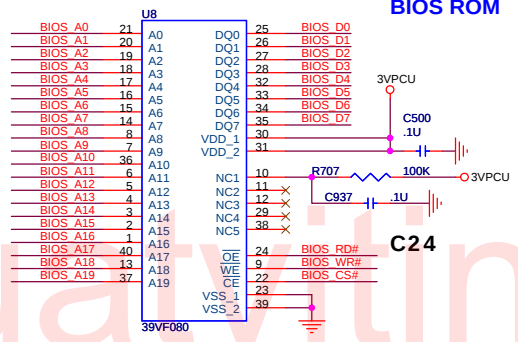
STRAP PIN

MY0	47	TP_TEST: Clock Test Mode Low: Test Mode. HIGH: 32kHz clock in normal running
MY1	48	TP_PLL: DPLL Test Mode Low: Test Mode. HIGH: Normal operation
MY2	49	TP_SPI: Default flash access Low: Boot from SPI flash part HIGH: Boot from ISA flash part
MY3	50	TP_ISP: In System Programming Mode Low: ISP mode HIGH: Normal Mode

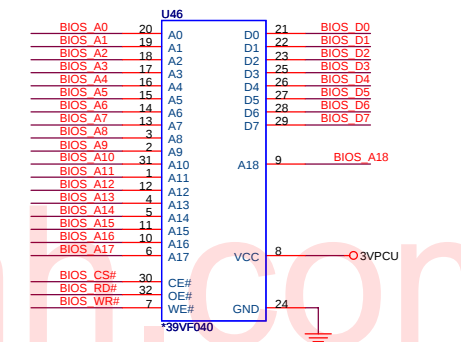


30

8Mbit (1M Byte), TSSOP40



4Mbit (512k Byte), TSSOP32

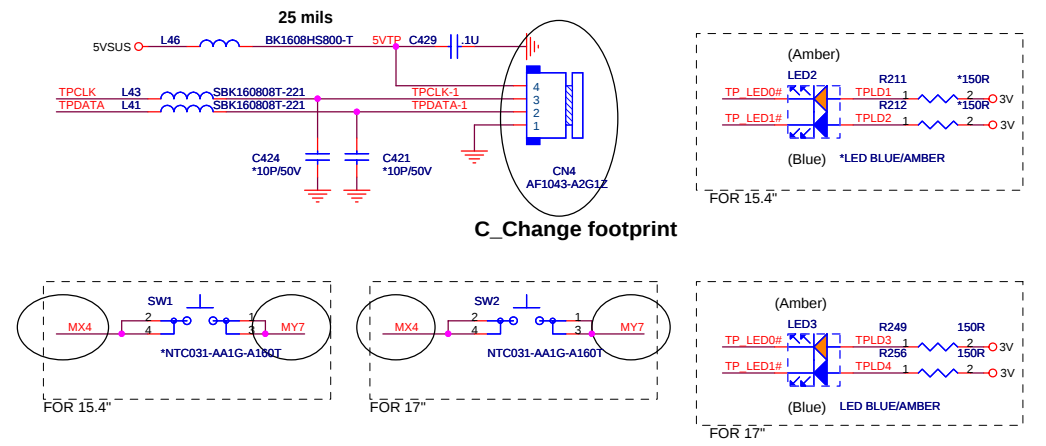


BIOS ROM

C24

B_Use SSOP32 to replace PLCC32

TOUCH PAD CONNECTOR

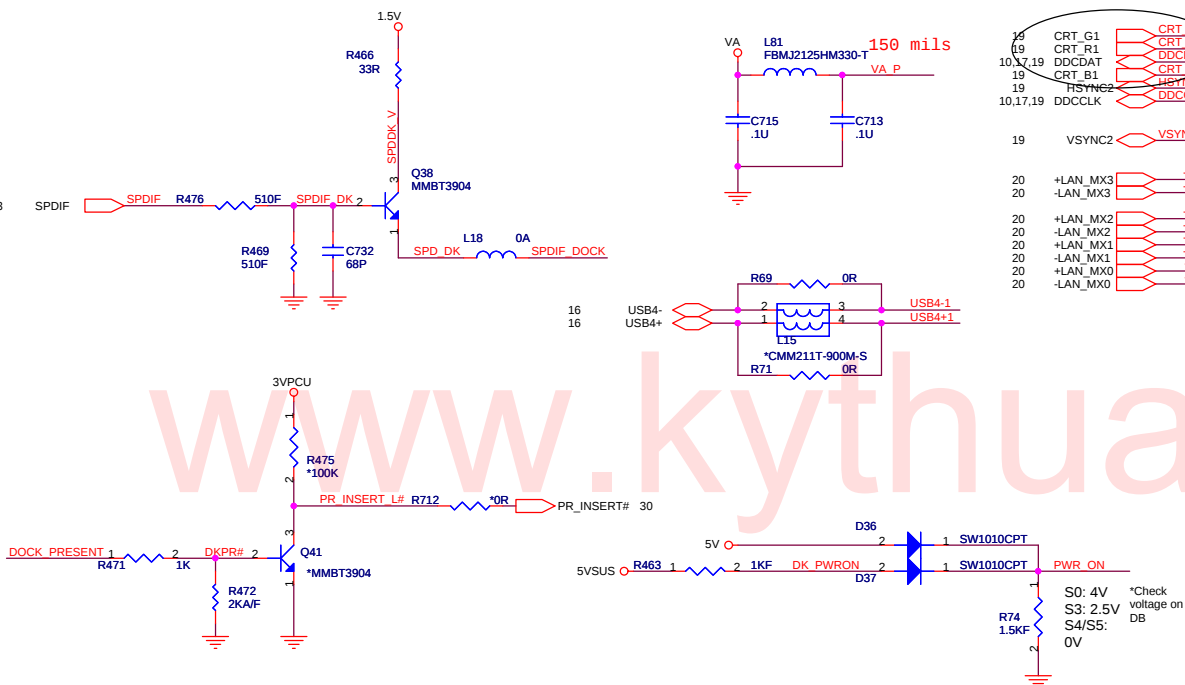


C_Change footprint

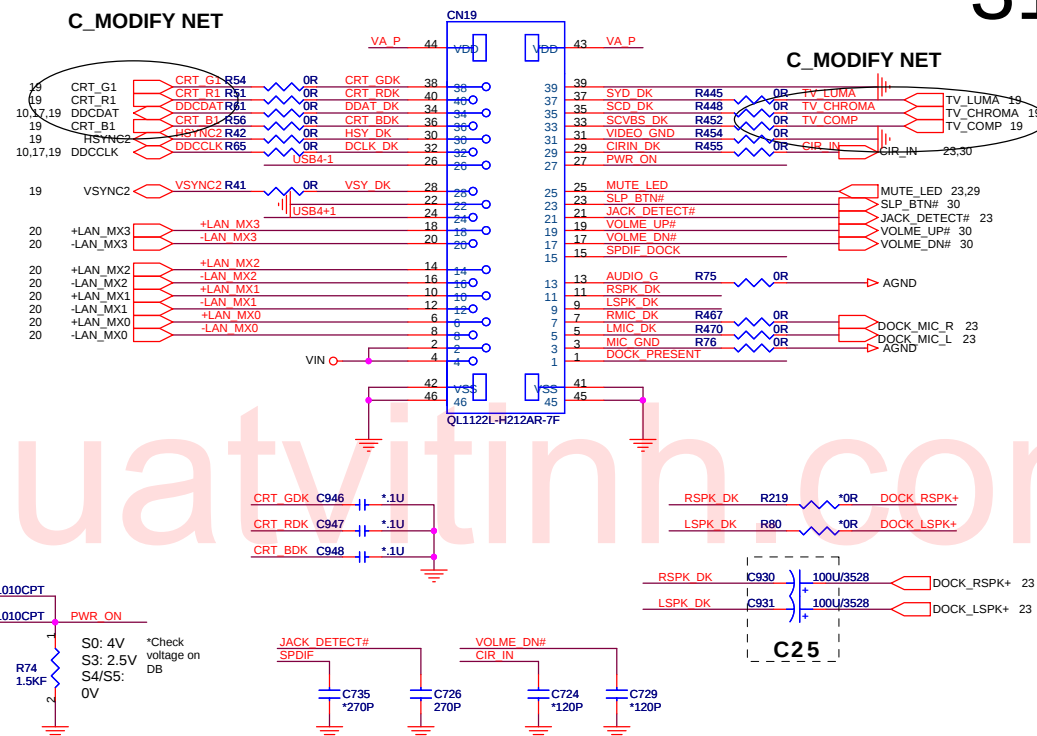
PROJECT : AT8
Quanta Computer Inc.

Size Custom	Document Number KB3920	Rev 3A
Date: Wednesday, June 14, 2006		Sheet 30 of 39

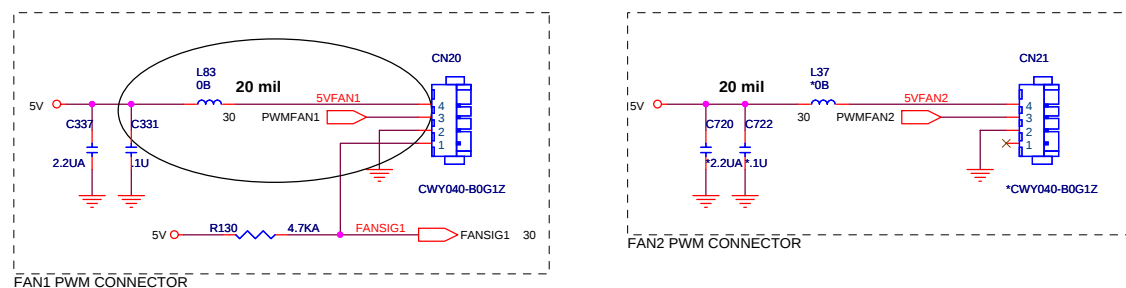
CABLE DOCK



C_MODIFY NET

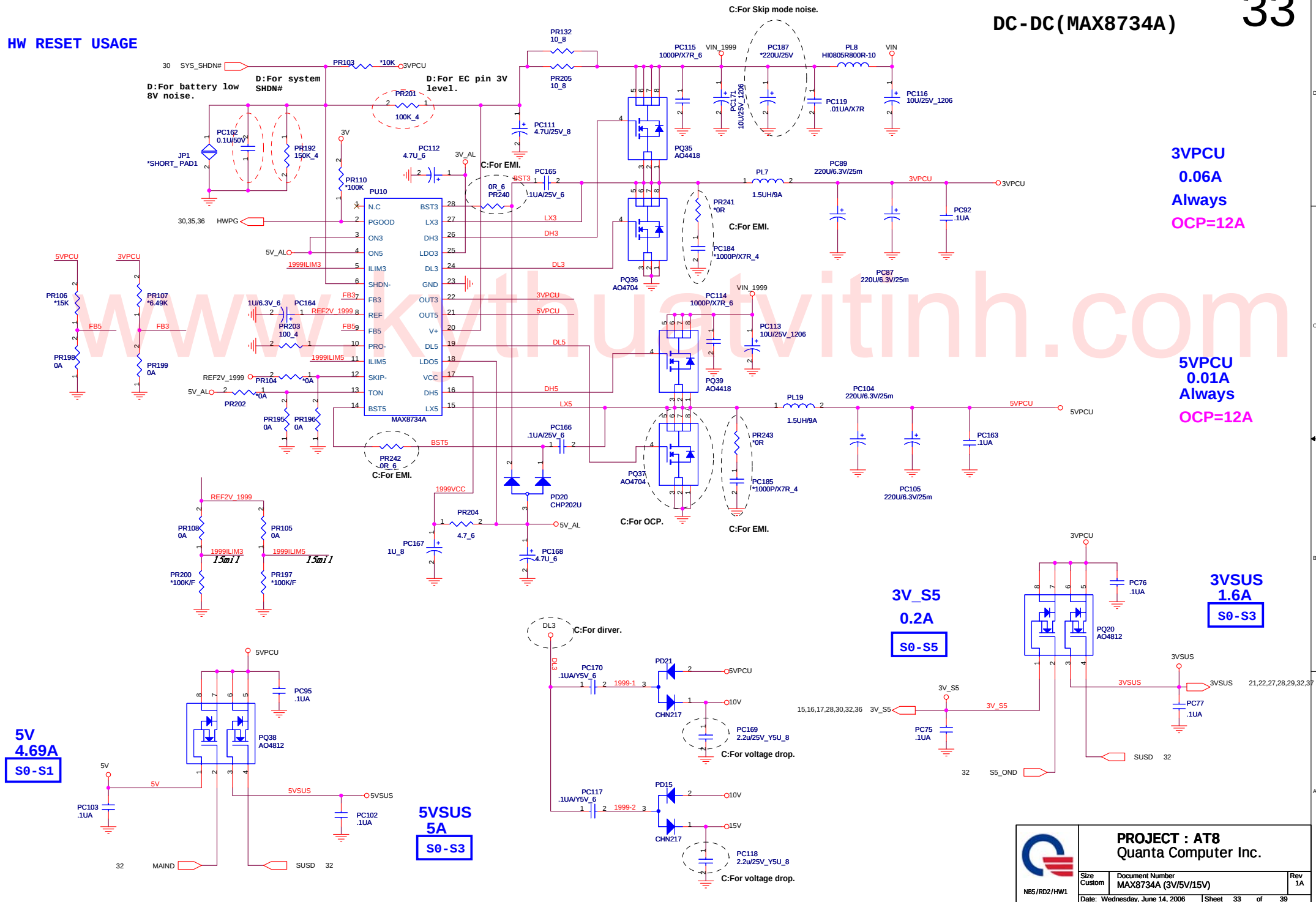


FAN



DC-DC (MAX8734A)

HW RESET USAGE



Adapter
19V/3.4A/65W
4.75A/90W

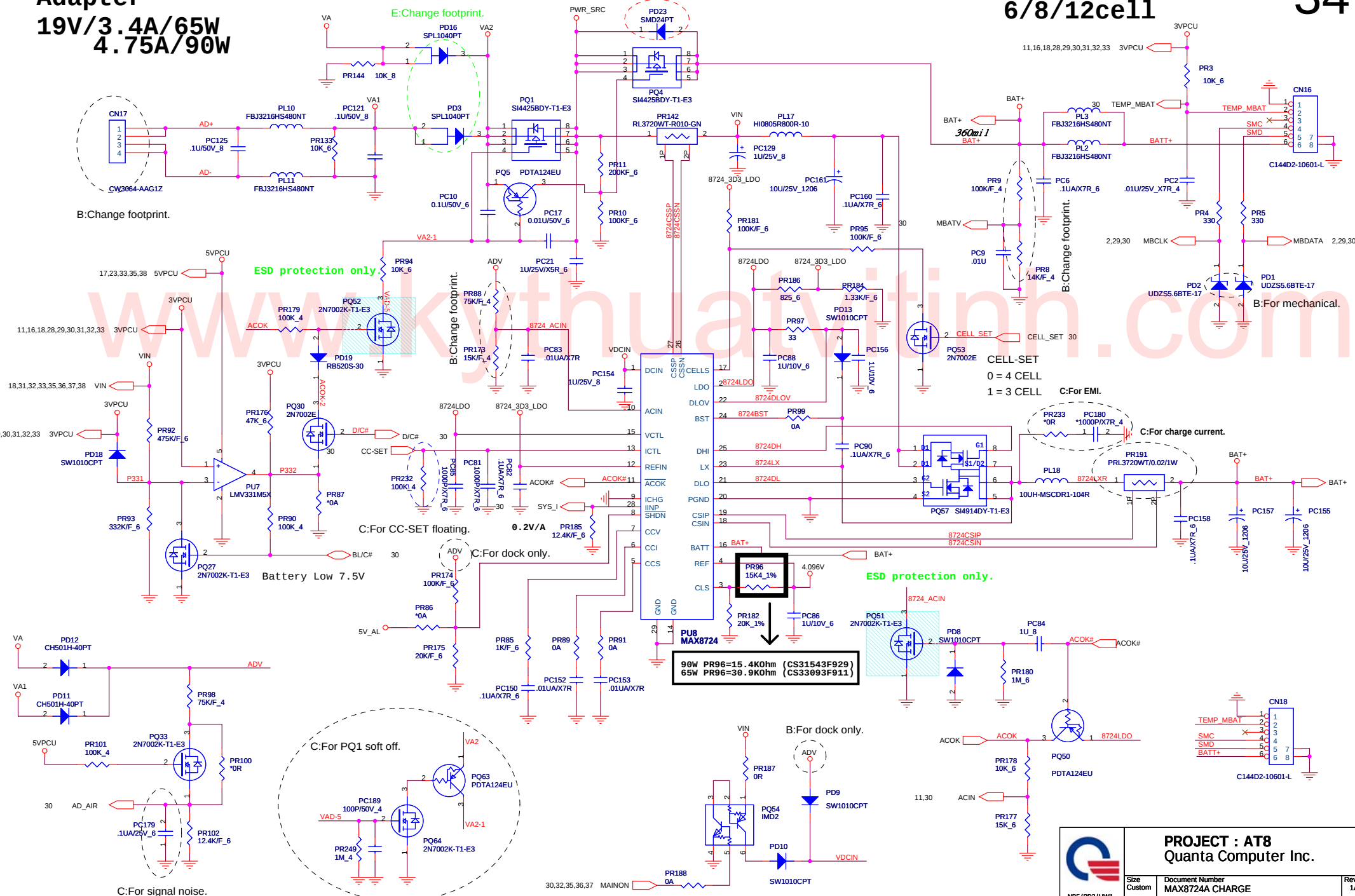
From Docking CNN

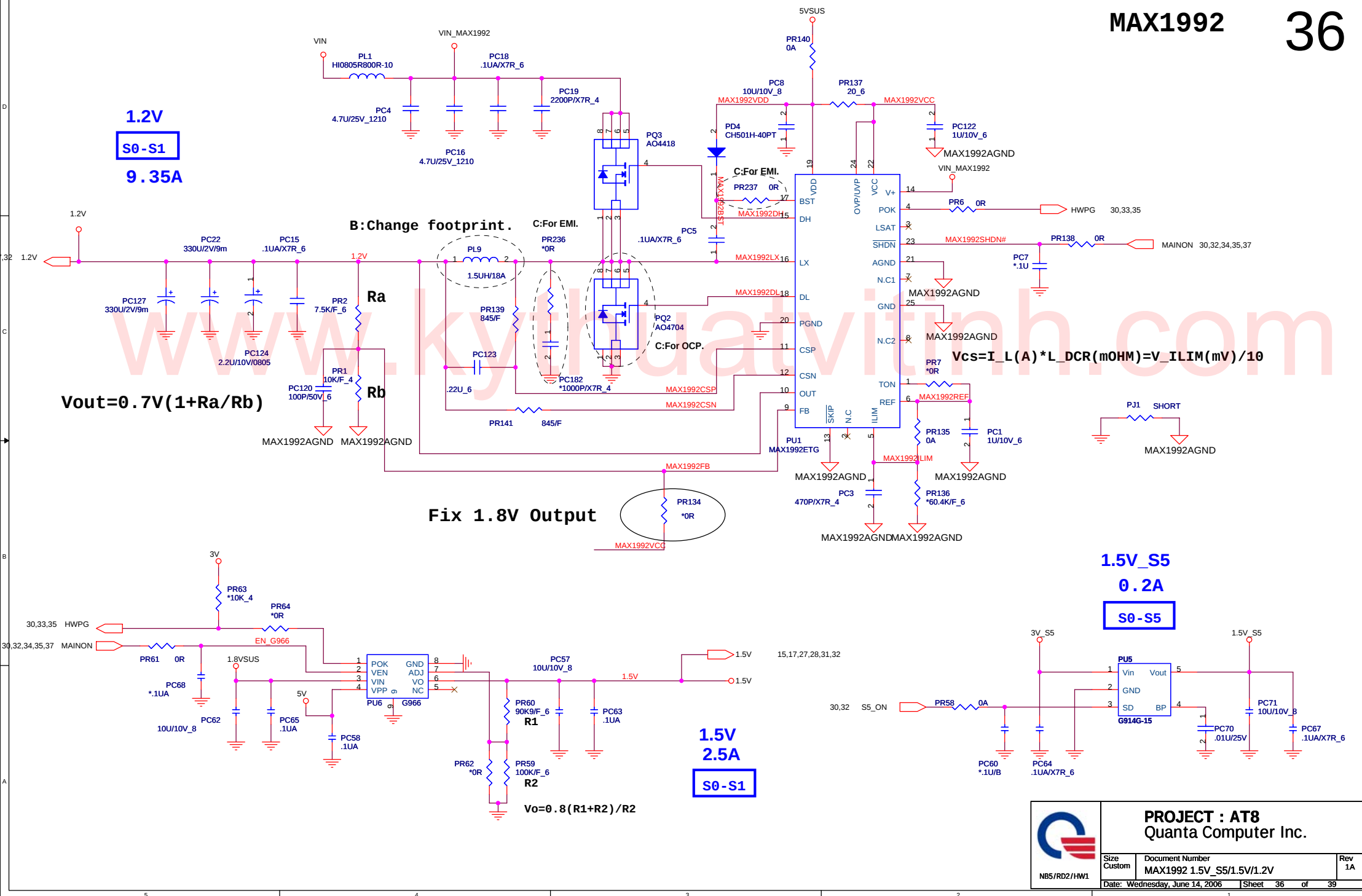
D:For discharge current.

MAX8724A

Battery
6/8/12cell

34





1.8VSUS

9.1A

S0-S3

1.8 Volt +/-5%
Design Current:15.0A
OCP: Max. 18.0A

C:For voltage drop.

D:For power switch.

B:For OCP set.

SMDDR_VTERM

1.53A / 0.9V

S0-S3

DCR 1.1m Ohms+-10%

C:For EMI.

C:For EMI.

0.9 Volt +/-5%
Design Current:1.5A
Maximum Current: 1.8A

SMDDR_VTERM

0.9V

?A

S0-S3

0.9V/1.2A

C:For 1.8V power sequence.

1.8V
4.75A

S0-S1



PROJECT : AT8
Quanta Computer Inc.

Size Custom	Document Number SC480 1.8VSUS/1.8V/SMDDR	Rev 1A
Date: Wednesday, June 14, 2006 Sheet 37 of 39		

