

Compal confidential

Schematics Document

Mobile Arrandale rPGA989 with
Intel PCH(Ibex Peak-M) core logic

2009-10-23 Rev 1.0

機 密	等級	硬體二部
	產出人員	
	產出日期	
	解密日期	

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Issued Date	2007/08/28	Deciphered Date	2006/03/10	Cover Sheet		
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O MEANS ON X MEANS OFF

power plane State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +0.75VS +VCCP +CPU_CORE +1.05VS +1.8VS
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

 : means Digital Ground
 : means Analog Ground

[illegible]

USB-0	Right side
USB-1	Right side
USB-2	Left side(with ESATA)
USB-3	Docking
USB-4	Camera
USB-5	WLAN
USB-6	X
USB-7	X
USB-8	MiniCard(WWAN/TV)
USB-9	New card
USB-10	Cardreader
USB-11	Finger Printer
USB-12	BT

PCle-1	WWAN
PCle-2	WLAN
PCle-3	LAN
PCle-4	New card
PCle-5	X
PCle-6	X

SATA0	HDD
SATA1	ODD
SATA2	X
SATA3	X
SATA4	ESATA
SATA5	Mult-Bay

	SOURCE	XDP	BATT	Thermal Sensor	SODIMM	CLK CHIP	WLAN WWAN	M93 Thermal Sensor	NB10M-GE	Cap sensor board	NEW CARD	G sensor
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	X	X	X	X	X	X	V	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	X	X	X	X	X	X	X	X
SMBCLK SMBDATA	PCH	V	X	X	V	V	V	X	X	X	V	V
SML0CLK SML0DATA	PCH	X	X	X	X	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH	X	X	X	X	X	X	X	X	X	X	X
		+3VS	+5VL		+3VS	+3VS	+3VALW			+5VL	+3VALW	+3VS

	SOURCE	LVDS	CRT	HDMI
D_EDID_DATA D_EDID_CLK	M93	V	X	X
D_CRT_DDC_DATA D_CRT_DDC_DATA	M93	X	V	X
HDMIDAT_VGA HDMICLK_VGA	M93	X	X	V

PA: PJP1, PJP903, PJP301, PJP302, PJP303, PJP304, PJP401,
PJP601, PJP602, PJP603, PJP501, PJP901, PJP902

OPP: PJP1, PJP301, PJP302, PJP303, PJP304, PJP401,
PJP601, PJP602, PJP603, PJP501, PJP901, PJP902, JP303

Stand-off Location: H12, H14

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0
G sensor	1D	0 0 0 1 1 1 0 1

NAL70 SKUs

PCB part number

PCB DA80000GL00

PA DAZ0BI00200

OPP DAZ0BI00300

PCH version

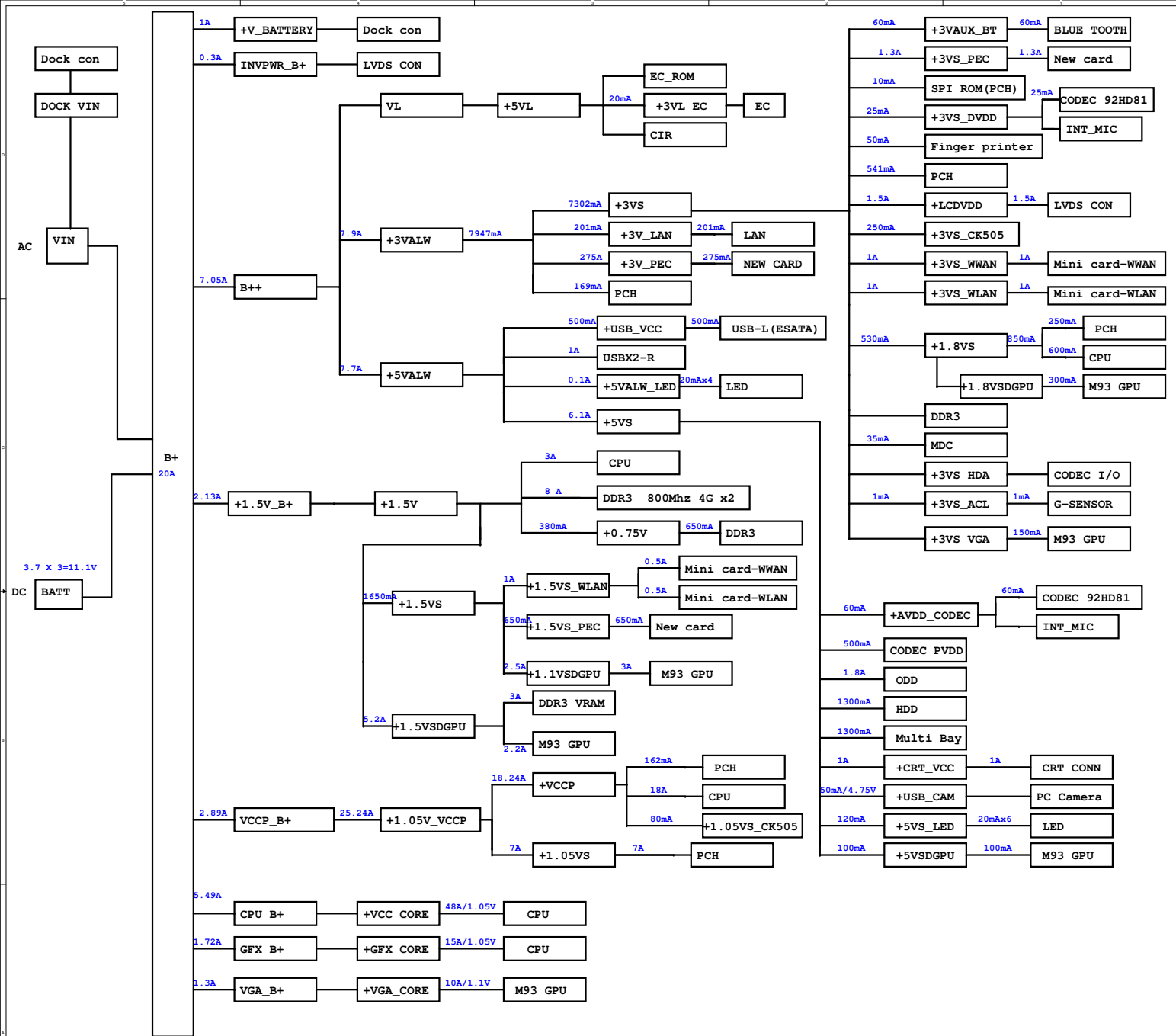
A1 QV73 SA00002KV10

B0 QLLT SA00002KV30

B1 QMGS SA00002KV60

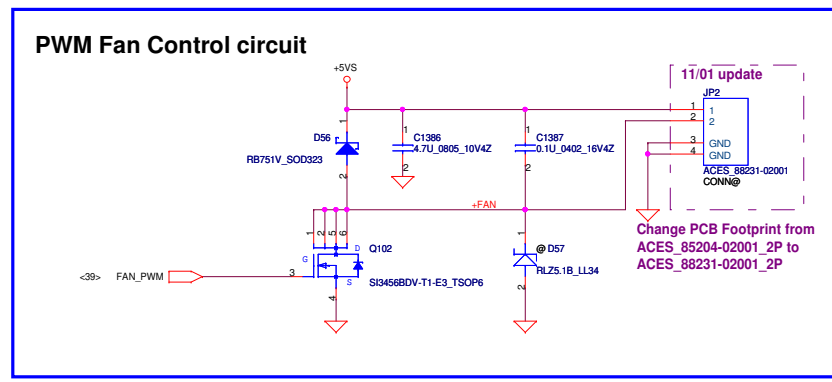
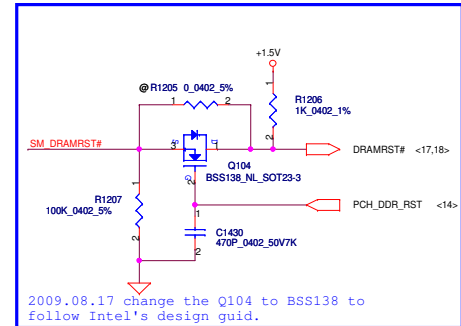
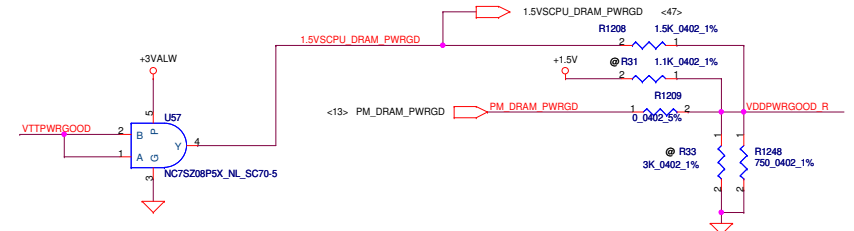
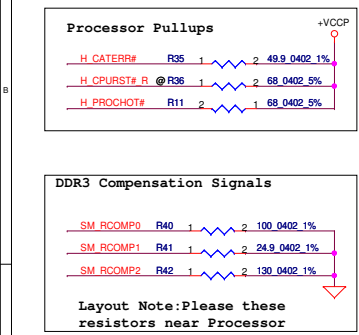
B3 QMNT SA00003N730

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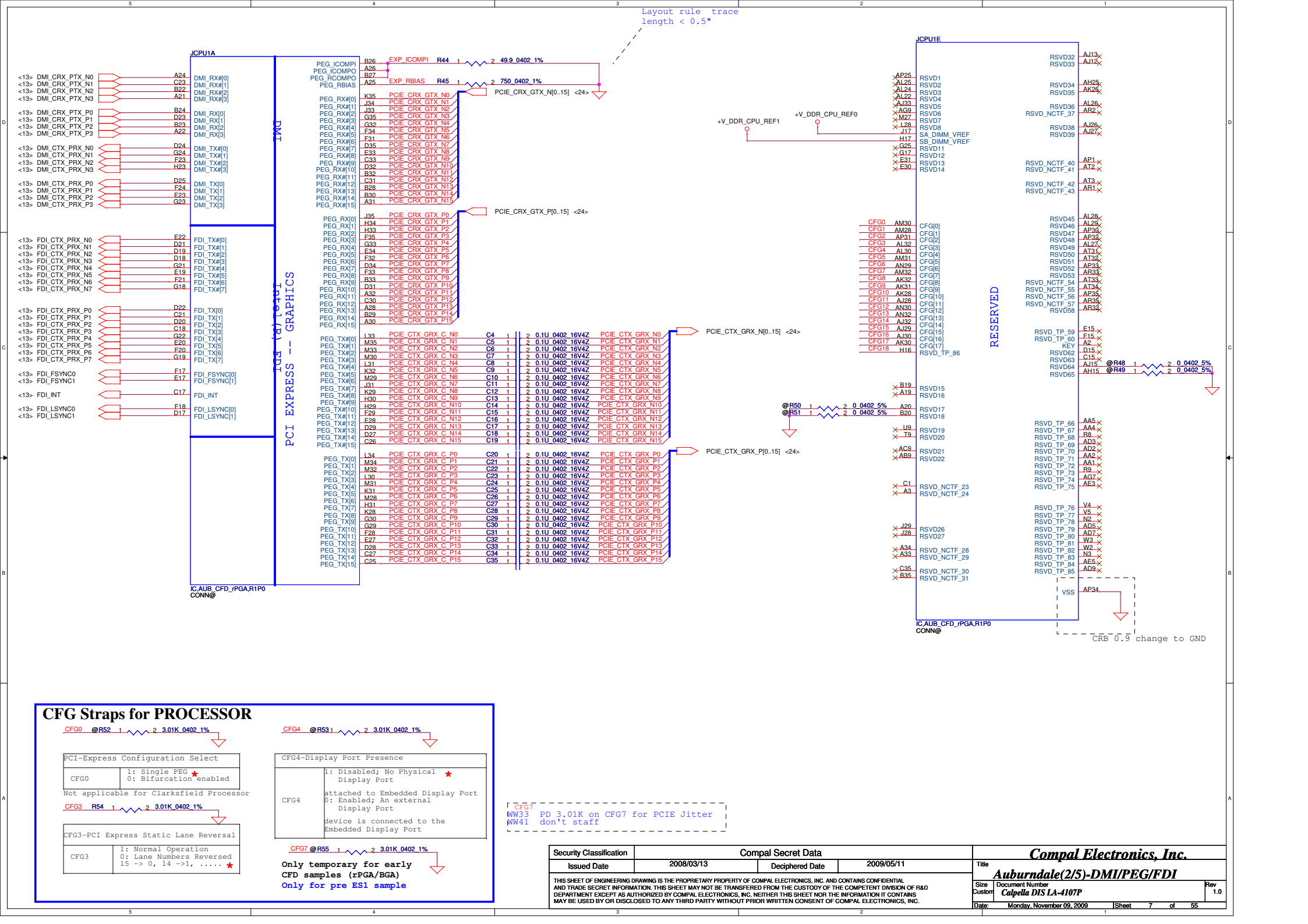


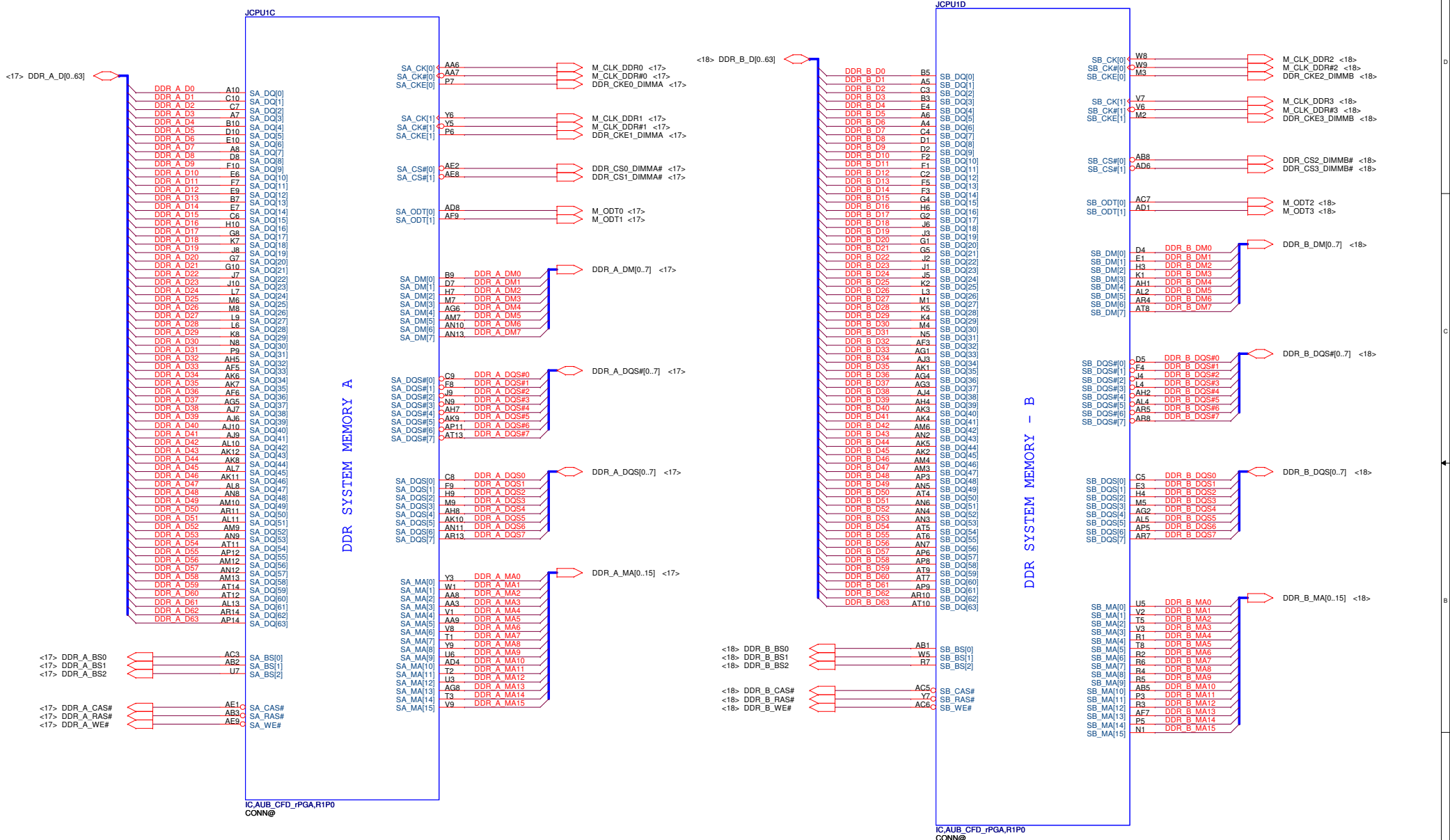
Calpella Discrete power on sequence				97.09.16.	Spec	define	min	Max
	Vin							
	B+							
	+3VL							
	+5VALW/+3VALW							
EC->PCH	RSMRST#	→ T1 ←			T1, >10ms, +3VALW to RSMRST#	T03	10 ms	-
	ON/OFF#	→ T2 ←			T2, User define			
EC->PCH	PWRBTN_OUT#	→ T3 ←			T3, 150ms, T4, 100ms			
PCH->EC	SLP_S5#	→ T5 ←			T5, >100ms, RSMRST# to SLP_S5#	T07	100 ms	-
PCH->EC	SLP_S4#	→ T6 ←			T6, >30us, SLP_S5# to SLP_S4#	T08	30 us	-
EC->PWR	SYSON	→ T7 ←			T7, 10ms, SLP_S3# to SYSON			
	+1.5V							
PCH->EC	SLP_S3#	→ T8 ←			T8, >30us, SLP_S4# to SLP_S3#	T09	30 us	-
EC->PWR	SUSP#	→ T9 ←			T9, 20ms, SLP_S3# to SUSP#			
	+5VS/+3VS/+1.8VS/+1.5VS/+1.05VS/+VCCP							
PWR->CPU	VTT_PWRGOOD	→ T10 ←			T10, VCCP stable to VTT_PWRGOOD assertion to the processor	T13	0.0001 ms	500 ms
EC->PWR	VR_ON	→ T11 ←			T11, >130ms, SLP_S3# to VR_ON	T16	99 ms	-
	+CPU_CORE	→ T12 ←			T12, Intel MVP soft start ramp-up time of +VOC_CORE	T17	-	3 ms
PWR->Clock	IMVP_CLK_EN#	→ T13 ←			T13, Duration Intel MVP V-boot, timing set by IMVP6.5	T18	10 us	100 us
	CLKIN_BCLK			Stable				
PWR->PCH or(EC->PCH)	VGATE or(PWROK)	→ T14 ←			T14, CLKIN_BCLK stable to VGATE assertion	T19	1 ms	-
PWR->PCH	PWROK	→ T15 ←			T15, IMVP_CLK_EN# to VGATE assert, Timing set by MVP6.5	T20	3 ms	20 ms
PWR->PCH	SYS_PWROK							
	MEPWROK				MEPWROK connect to PWROK (iAMT disable)			
	DRAMPWROK	→ T16 ←			T16, +1.5V stable to DRAMPWROK assertion. Timing set by PCH	T22	100 ns	-
	CLKOUT_BCLK	→ T17 ←			T17, VGATE assertion to DRAMPWROK assertion, Timing set by PCH	T23	1 ms	-
PCH->CPU	PROCPWRGD	→ T18 ←			T18, CLKOUT_BCLK stable to VCCPWRGOOD_0 - VCCPWRGOOD_1 assertion to Processor. Timing set by	T24	10 BCKS	-
	VCCPWRGOOD_0	→ T19 ←			T19, VTT_PWRGD to VCCPWRGOOD assertion, Timing set by PCH	T25	1 ms	-
	VCCPWRGOOD_1	→ T20 ←			T20, VGATE assertion to VCCPWRGOOD assertion, Timing by PCH	T26	1 ms	100 ms
		→ T21 ←			T21, VCORE stable to VCCPWRGOOD assertion	T27	0.05 ms	-
PCH->N.C.	SUS_STAT#	→ T22 ←			T22, VCCPWRGOOD to SUS_STAT#, timing default is 1ms	T28	0.03 ms	-
PCH->Device	PLT_RST#	→ T23 ←			T23, SUS_STAT# to PLT_RST#, timing set by PCH	T29	60 us	-

Design guide
1.11update, PLTRST series R28
resistor 1.5K, PL 750_0402_1%
resistor 750 ohm

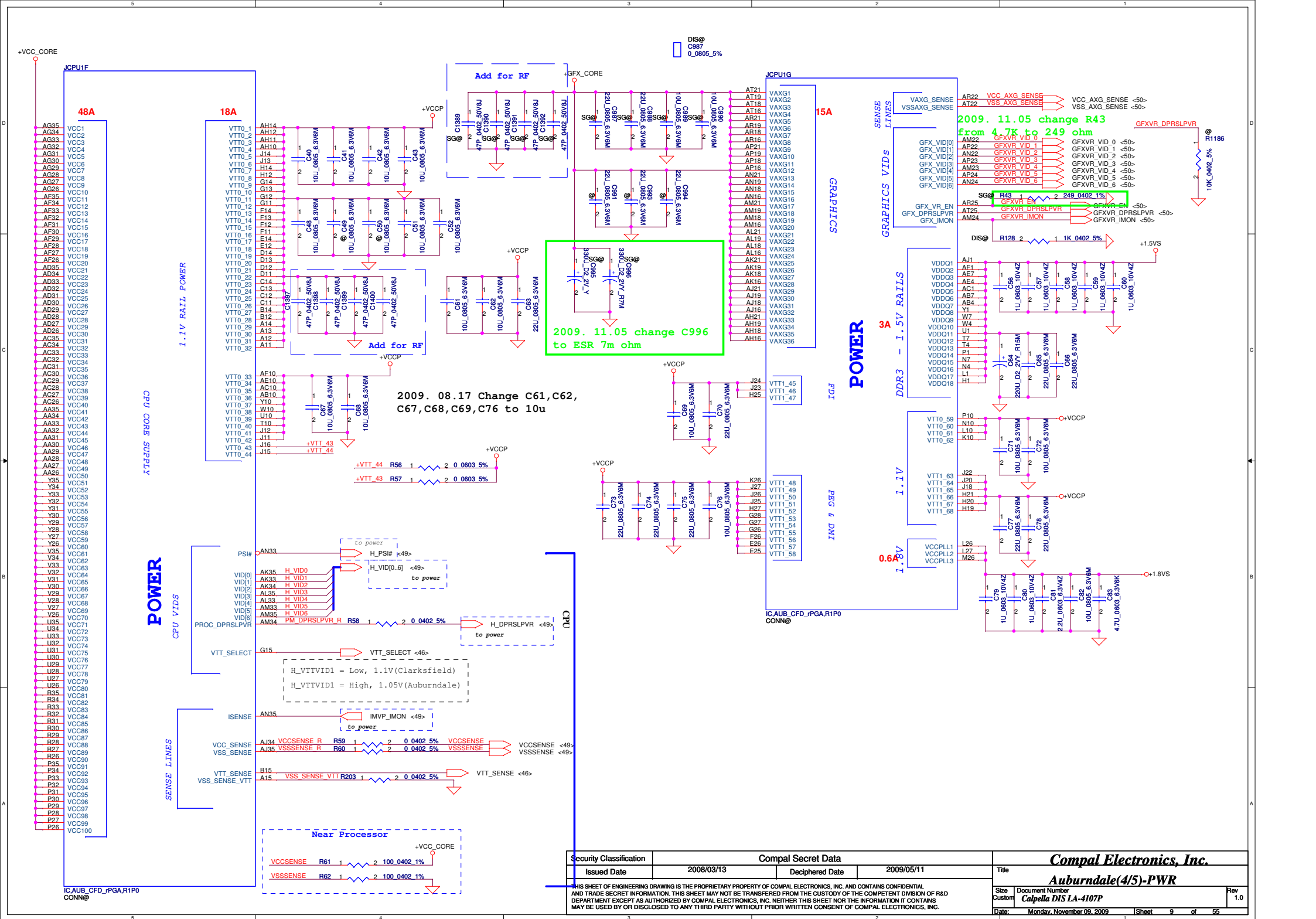


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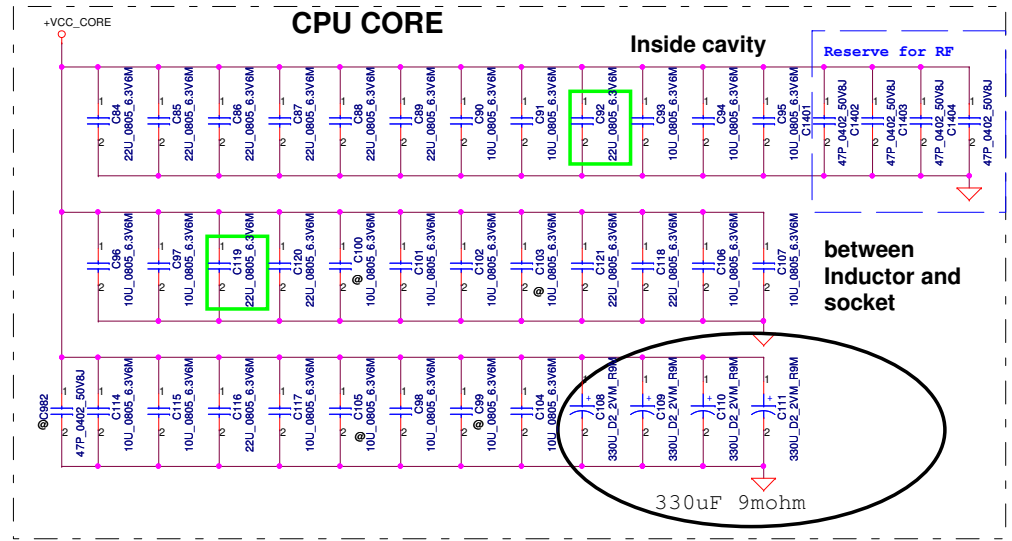
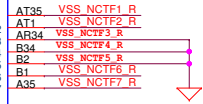
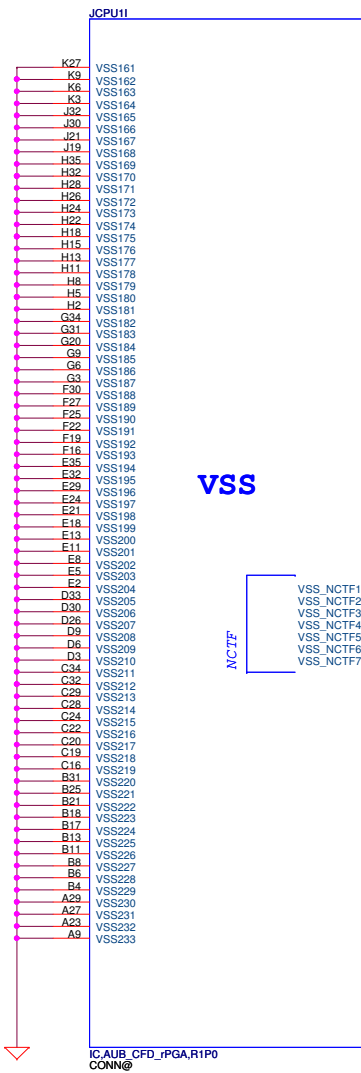
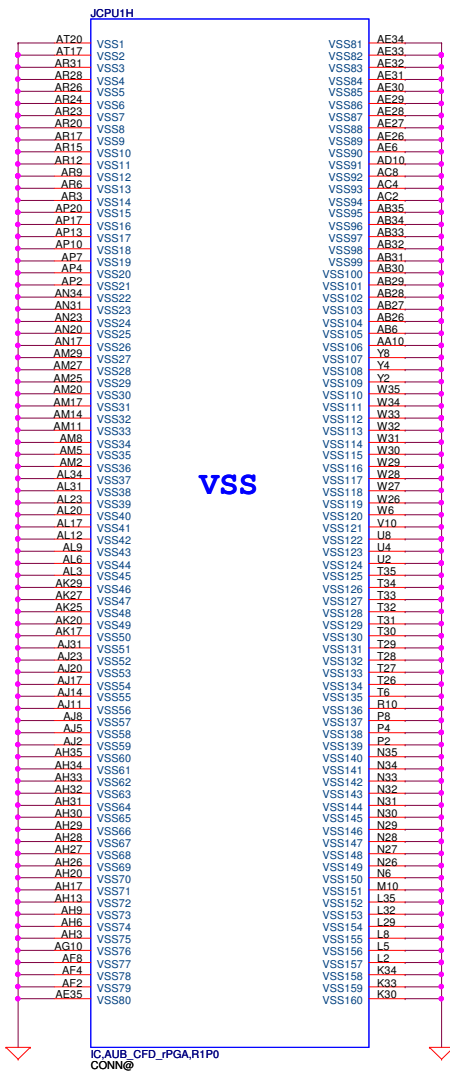




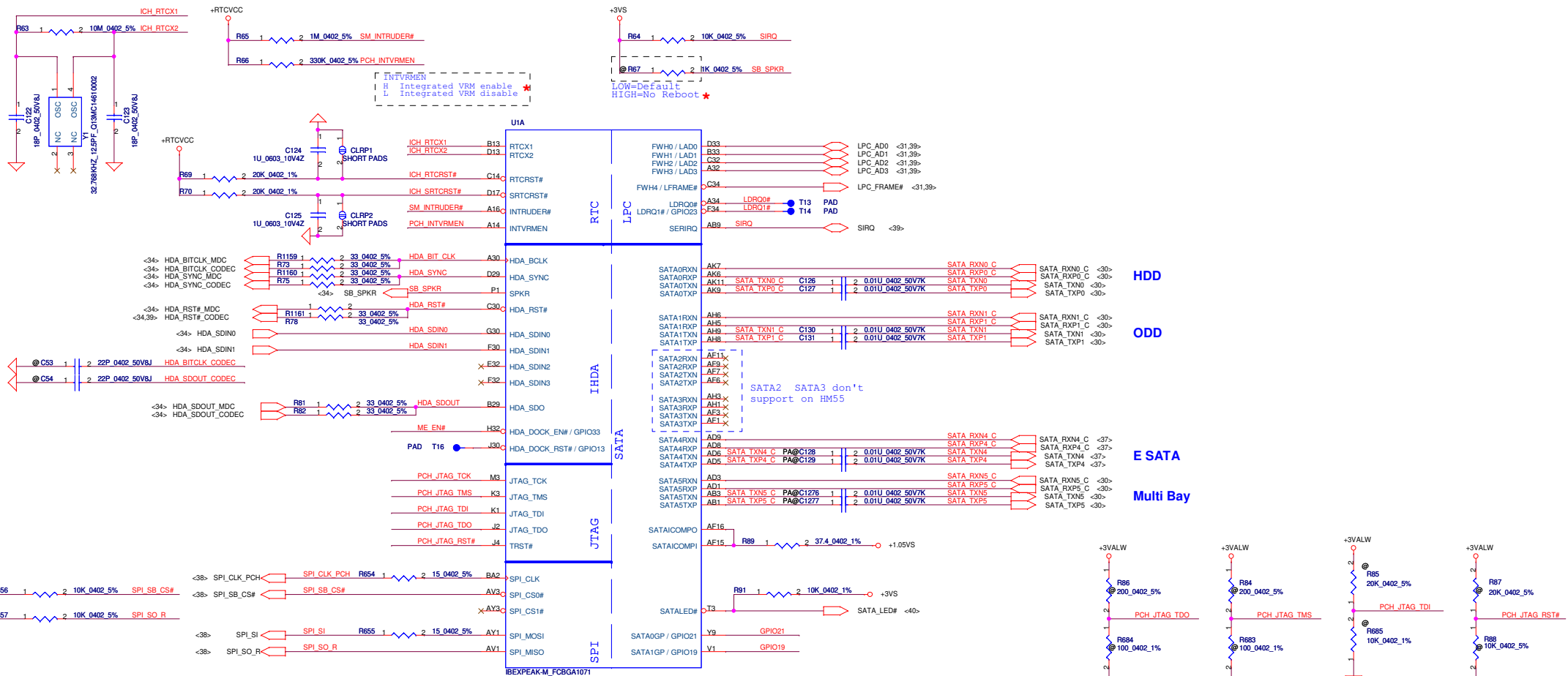
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HDA_SYNC

This signal has a weak internal pull down.
H=>On Die PLL is supplied by 1.5V
L=>On Die PLL is supplied by 1.8V

HDA_DOCK_EN#

ME debug mode, this signal has a weak internal PU
H=>Security measures defined in the Flash Descriptor will be in effect (default)
L=>Flash Descriptor Security will be overridden

SPI_MOSI

This signal has a weak internal pull down.

★ Disable iTPM=No Stuff
Enable iTPM=Stuff

iTPM ENABLE/DISABLE

SI Reserve GPIO19 21 PD for LPM enable power saving

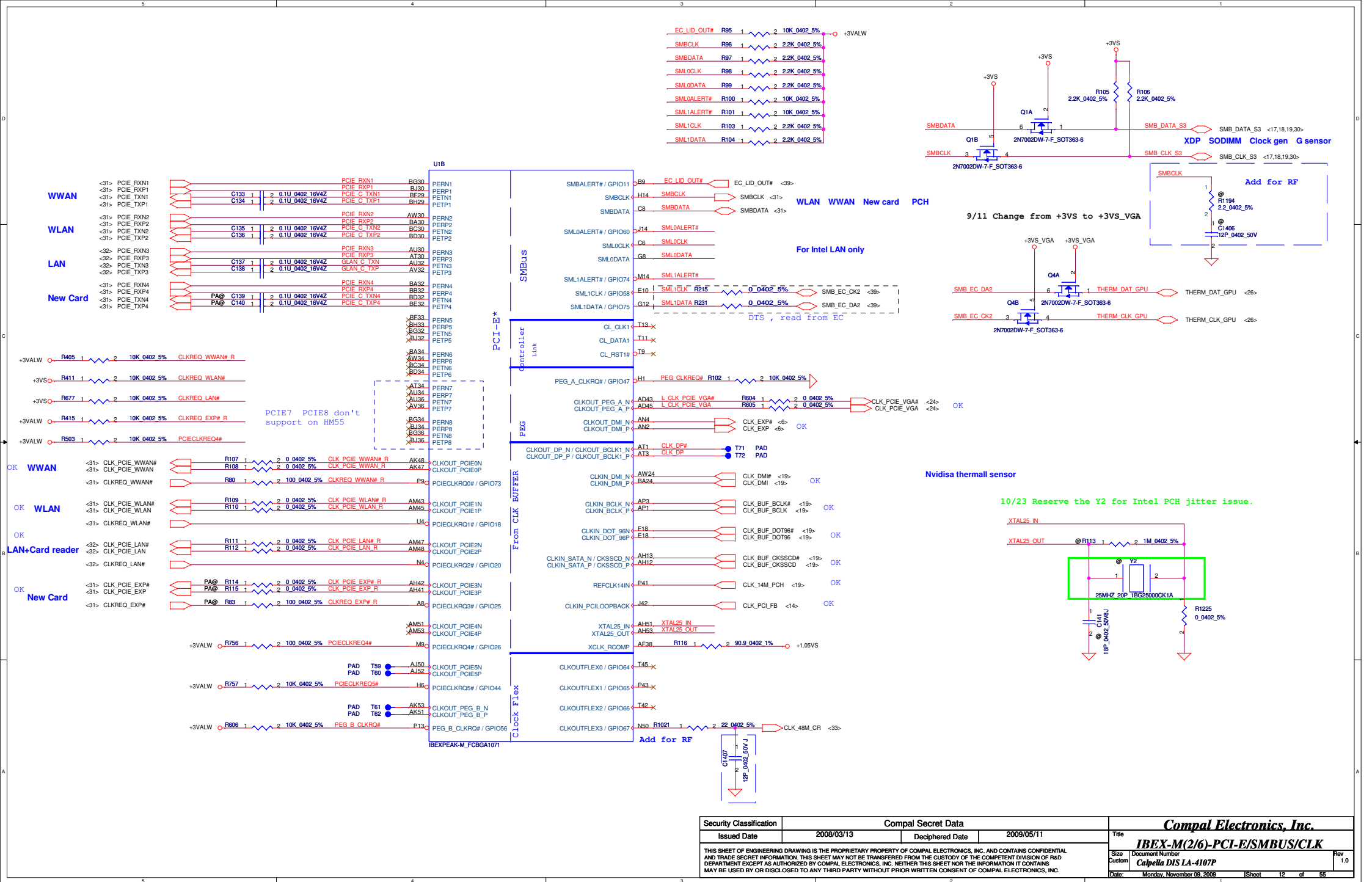
HDA_SDO

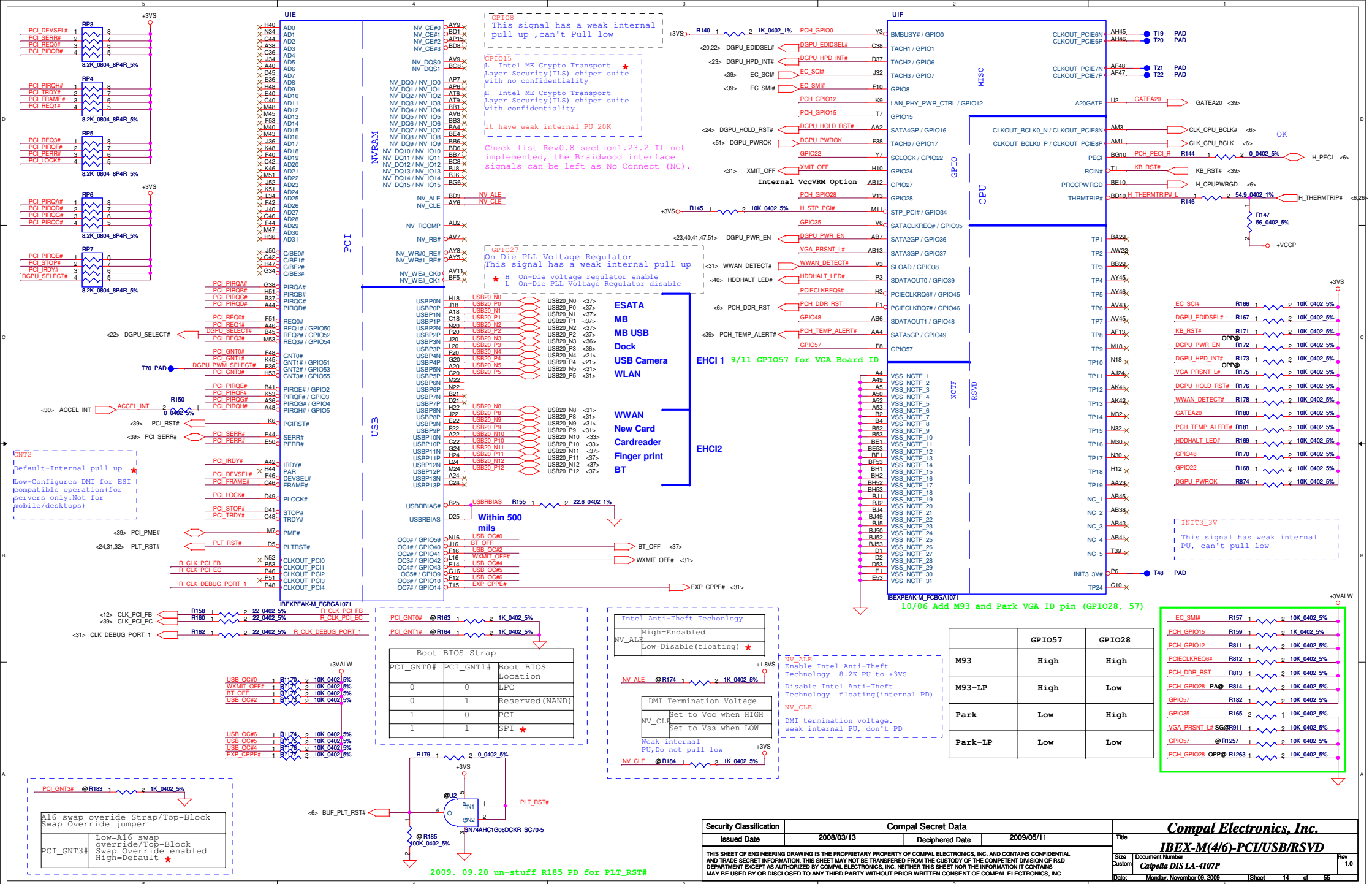
This signal has a weak internal pull down.
This signal can't PU

★ Disable iTPM=No Stuff
Enable iTPM=Stuff

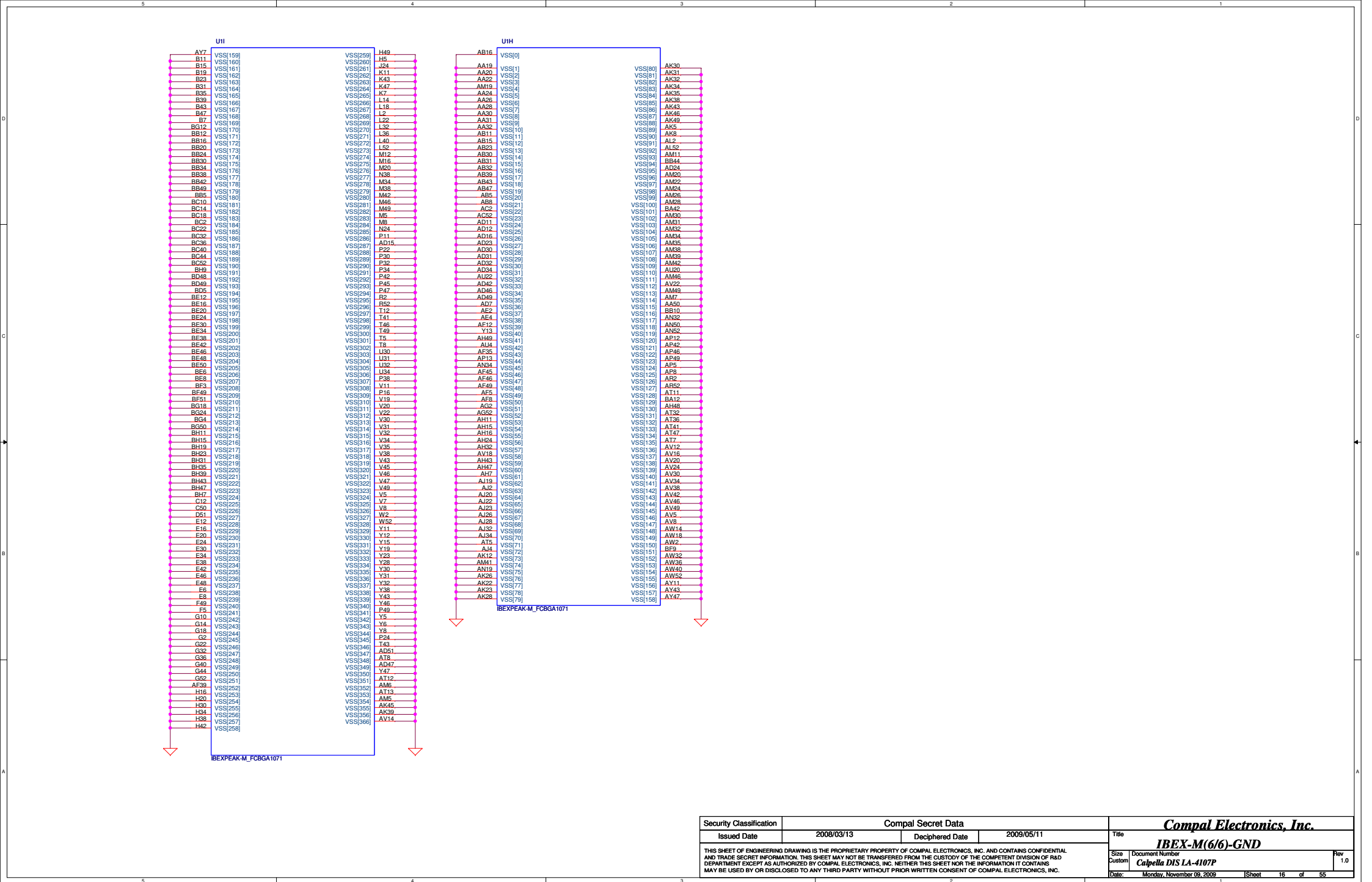
PCH Pin	RefDes	PCH JTAG Enable		PCH JTAG Disable	
		ES1	ES2	ES1	ES2
PCH_JTAG_TDO	R86	No Install	200ohm	No Install	No Install
PCH_JTAG_TMS	R84	No Install	100ohm	No Install	No Install
PCH_JTAG_TDI	R85	200ohm	200ohm	No Install	No Install
PCH_JTAG_TCK	R87	100ohm	100ohm	No Install	No Install
PCH_JTAG_RST#	R88	10Kohm	10Kohm	No Install	No Install

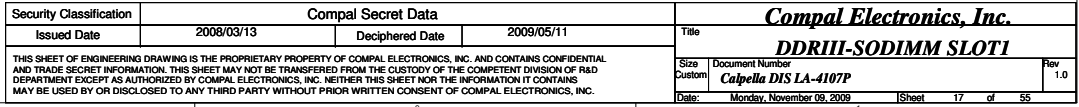
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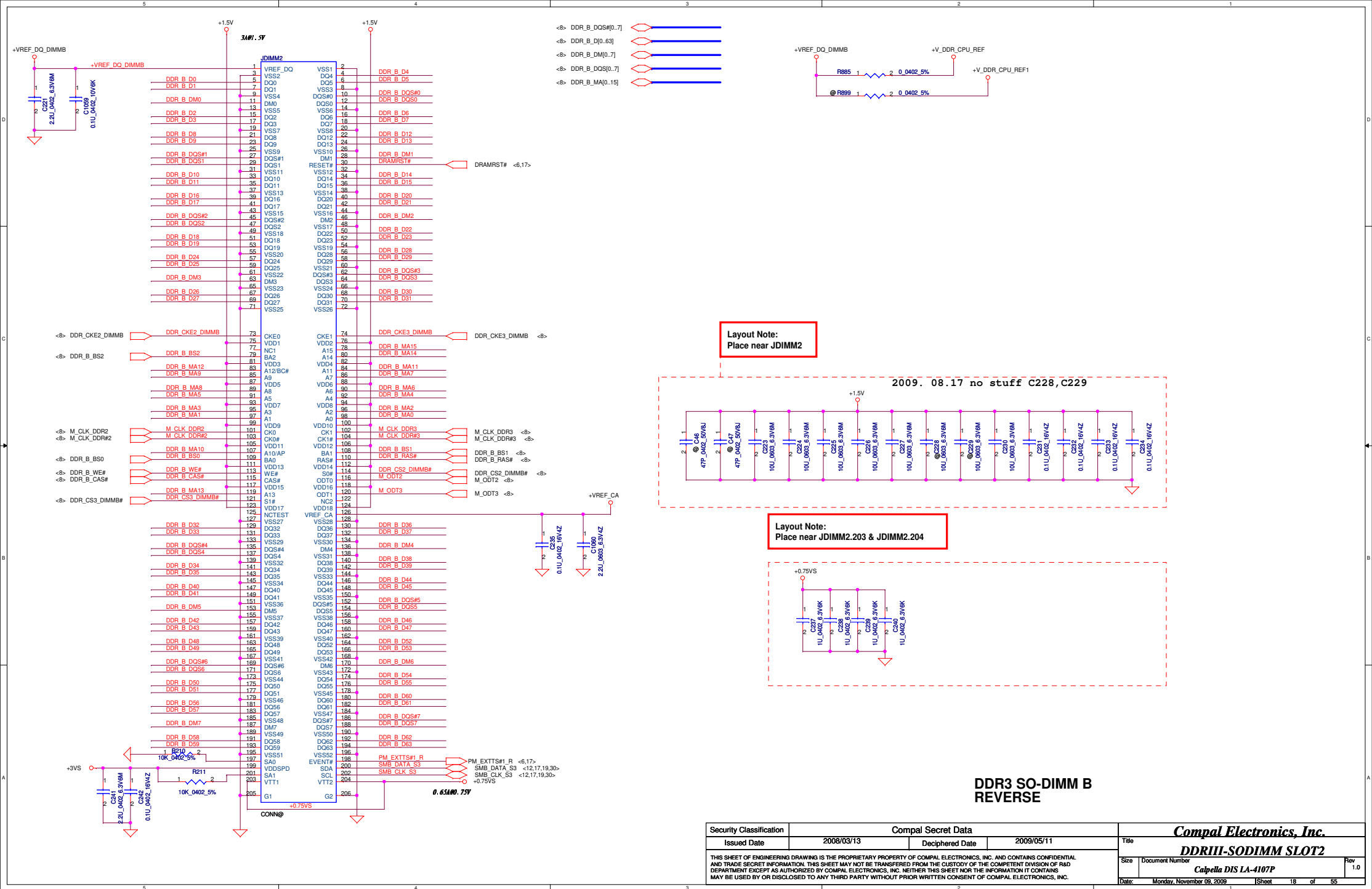




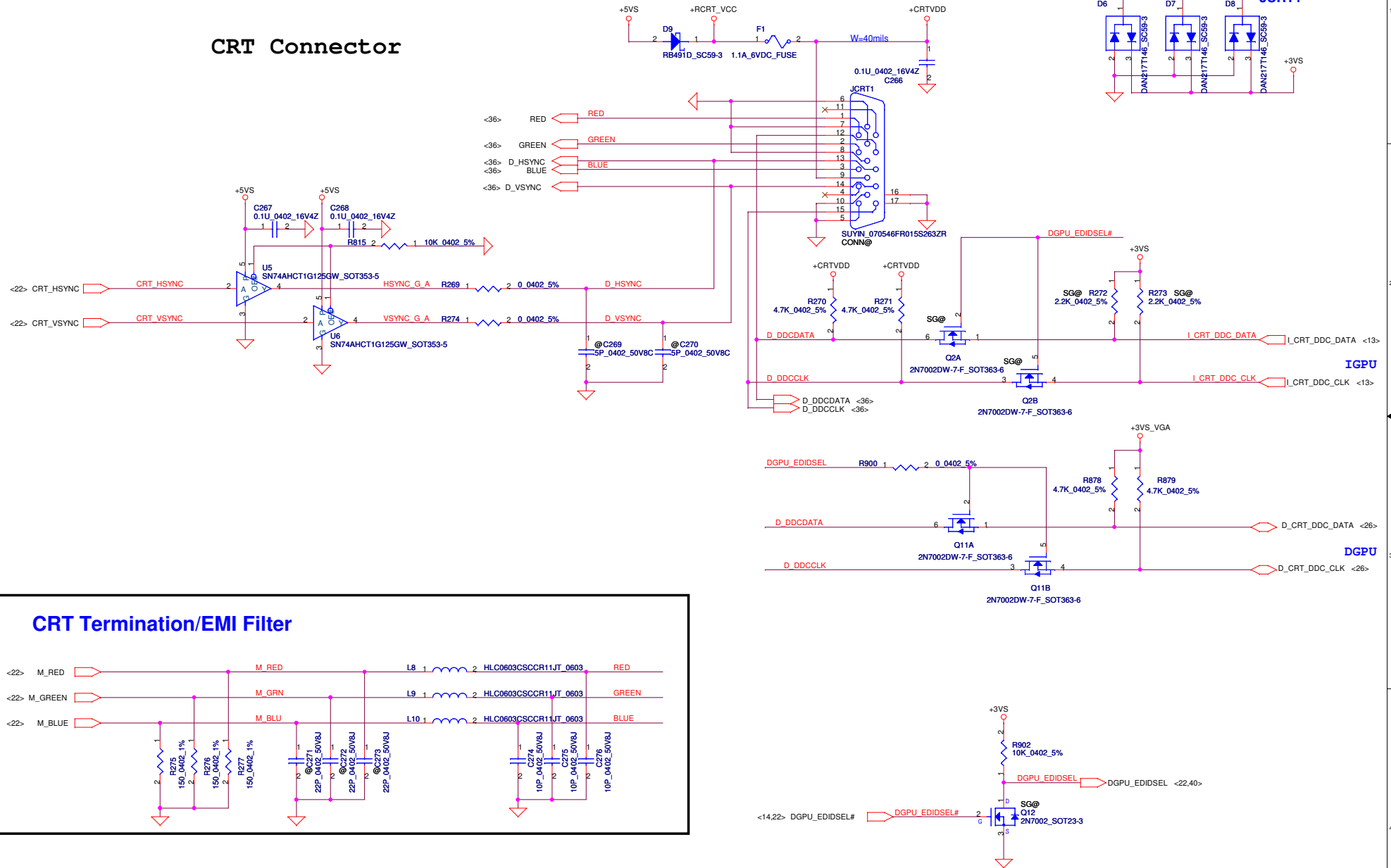
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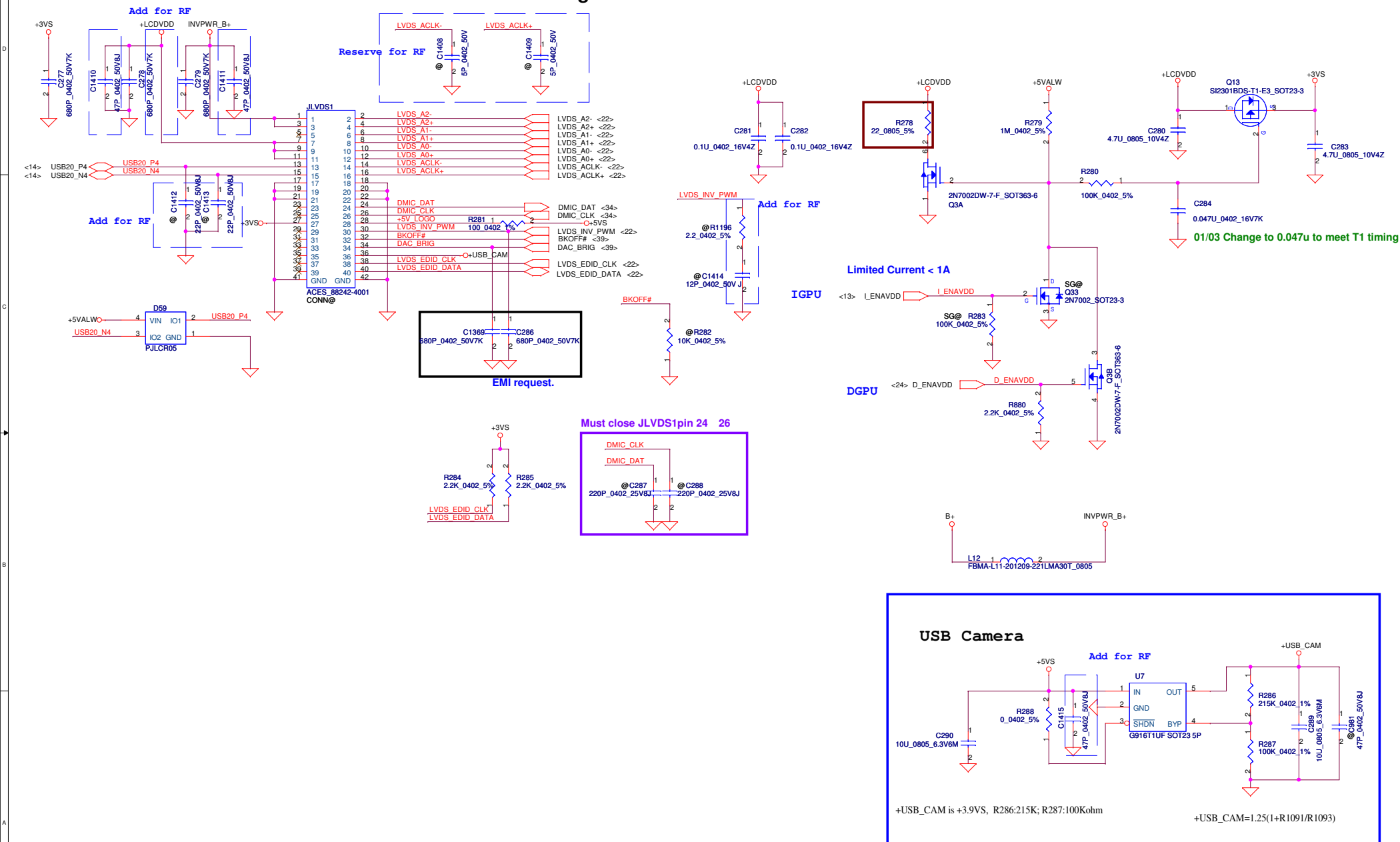


CRT Connector

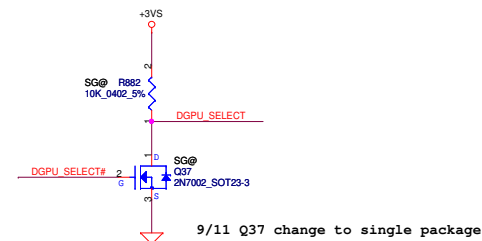
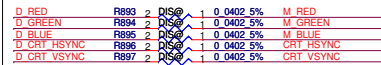
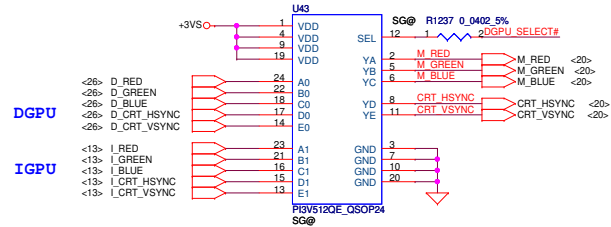
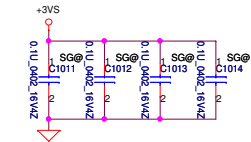
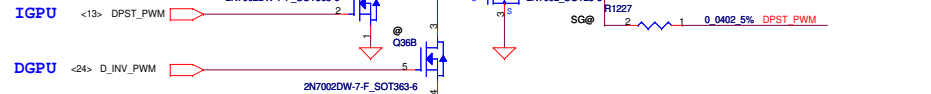
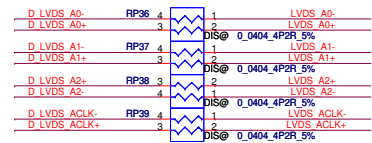
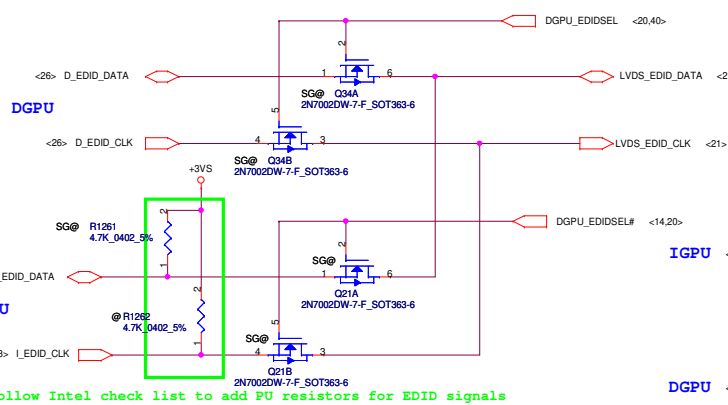
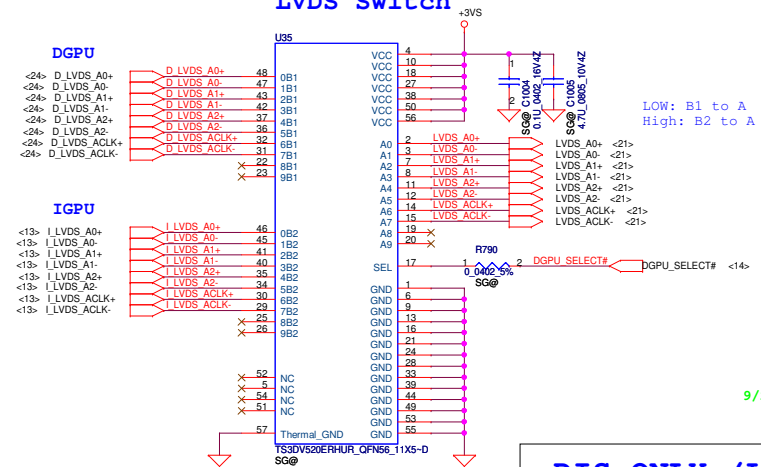


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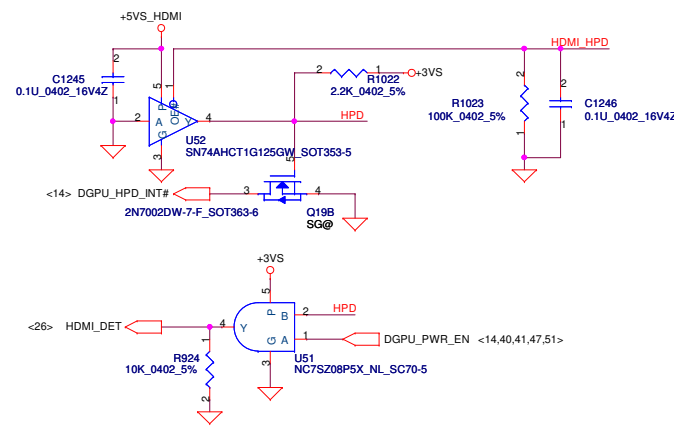
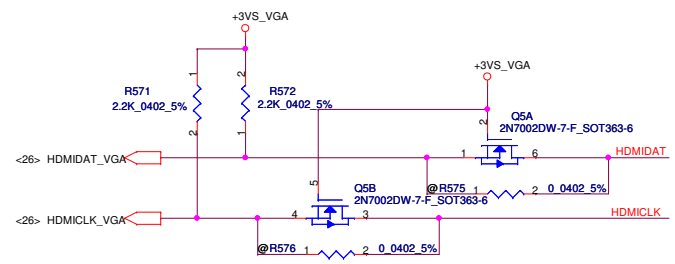
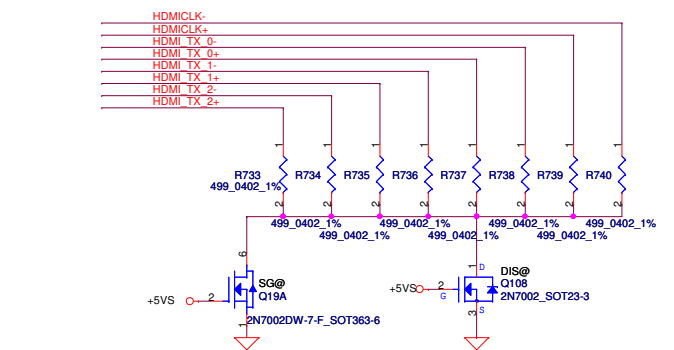
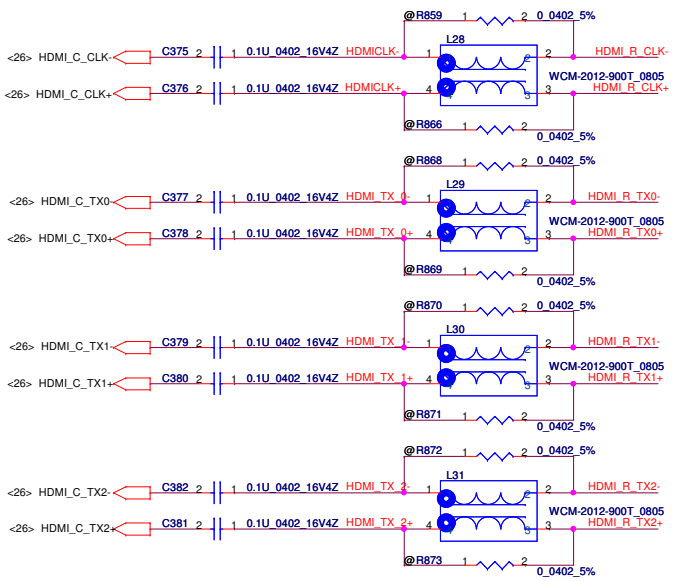
LVDS CONN & USB Camera + Dig Mic



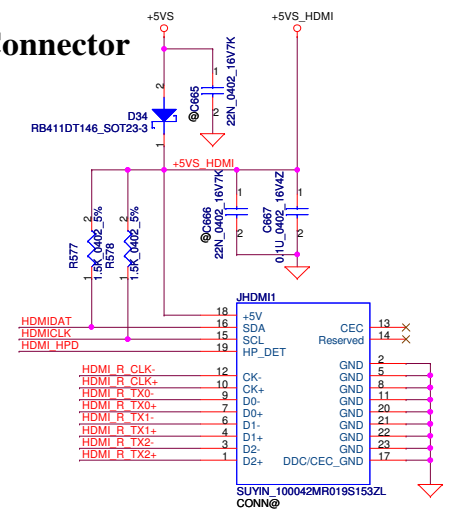
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										Capella DIS LA-4107P		1.0	
						Date:				Monday, November 05, 2009		Sheet 21 of 55	



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Issued Date	2007/09/29	Deciphered Date	2007/09/29	Title	
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				Custom	1.0
				Document Number Calpella DIS LA-4107P	
Date:	Monday, November 05, 2009	Sheet	22	of	55



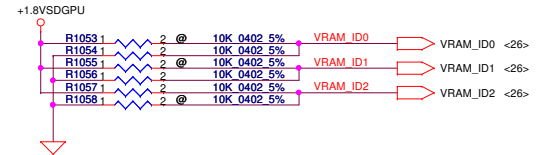
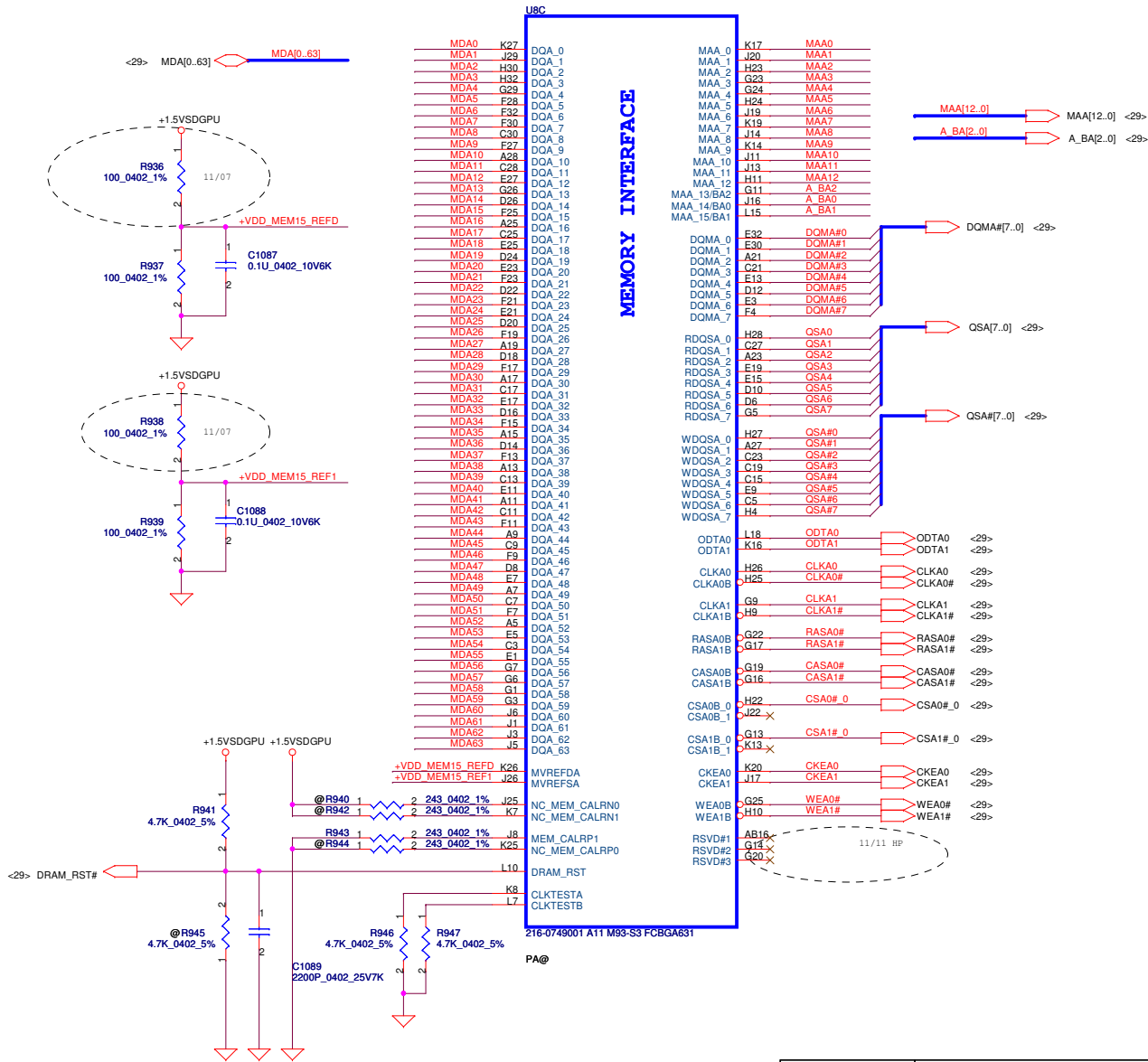
HDMI Connector



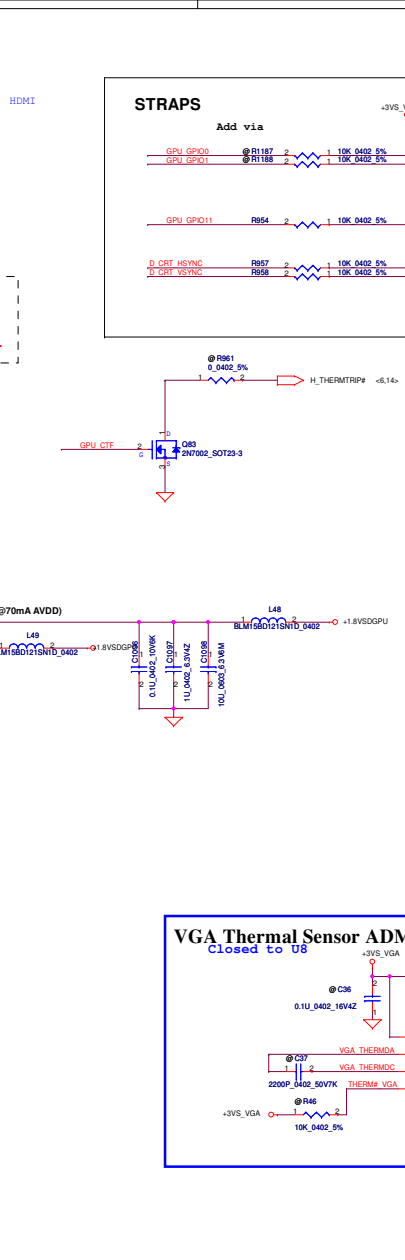
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Issued Date				2007/08/28				Deciphered Date			
								2006/03/10			
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Size				Document Number				Rev			
Custort				Calpella DIS LA-4107P				1.0			
Date:				Monday, November 09, 2009				Sheet 23 of 55			

[illegible][illegible]

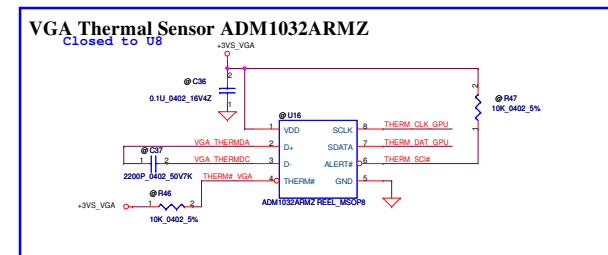
Security Classification	Compal Secret Data		Title	Compal Electronics, Inc.	
Issued Date	2006/03/31	Deciphered Date	2010/03/31		
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			A4	Compal DES LA-107P	1.0
			Date:	March 22, 2008	ISCAN 34 42 85



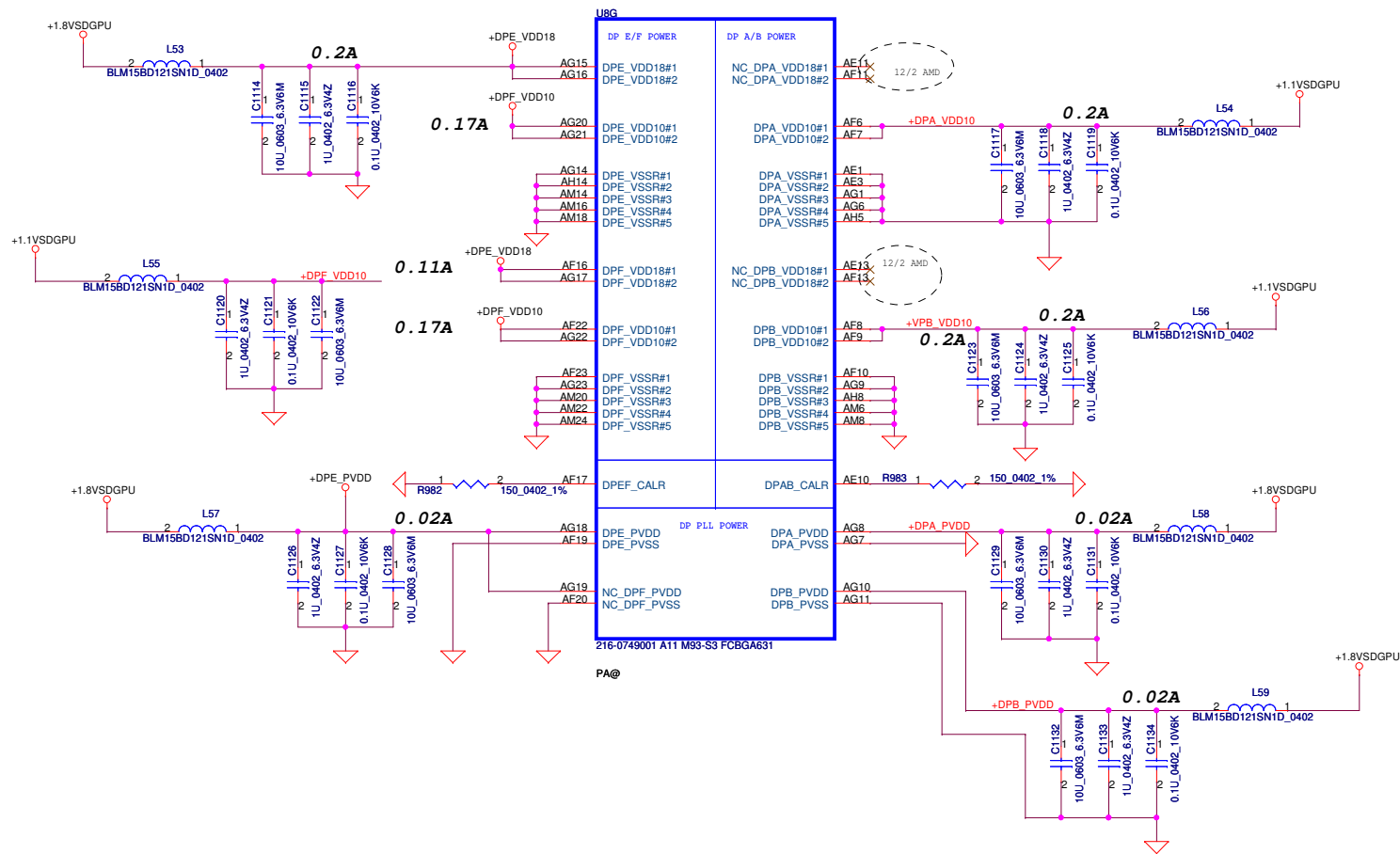
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Hynix Orion die H5TQ1G63BFR-12C SA000032400	0	0	0
Samsung E die K4W1G1646E-HC12 SA000035700	0	0	1
Qimonda IDGH1G-04A1F1C-16X SA000030800	0	1	0
TBD	0	1	1
TBD	1	0	0
TBD	1	0	1
TBD	1	1	0
TBD	1	1	1



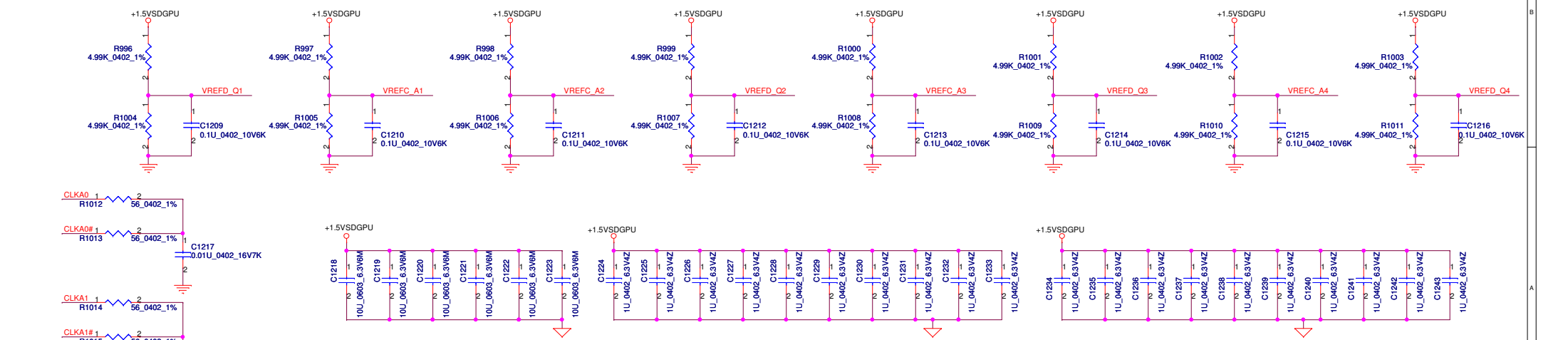
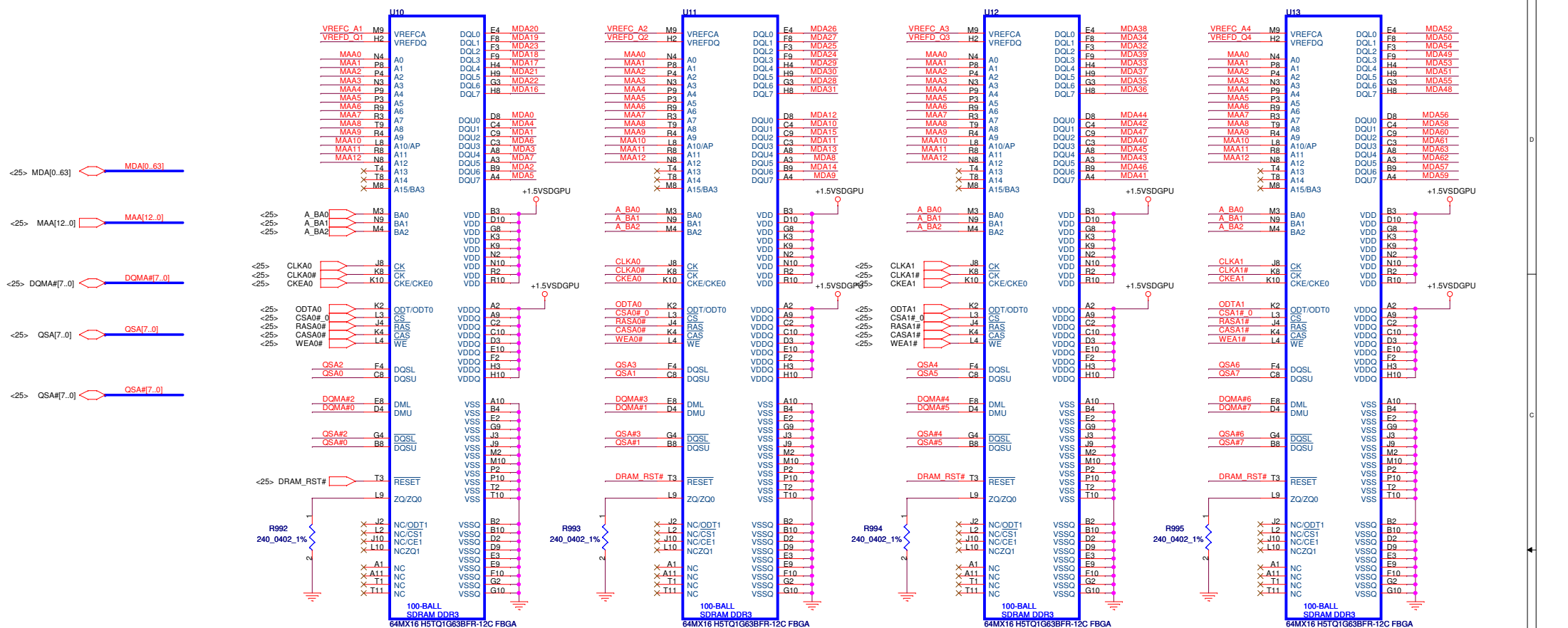
AMD RESERVED CONFIGURATION STRAPS	
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET	
H2SYN0	GENERIC0
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET	
GPIO21_BB_EN	



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			Scale	1:0	
			Material	Aluminum DIE LA-1047	
			Lot	0909	
			Rev	1.0	



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				Date	Monday, November 09, 2009
				Sheet	27 of 55
				Rev	1.0

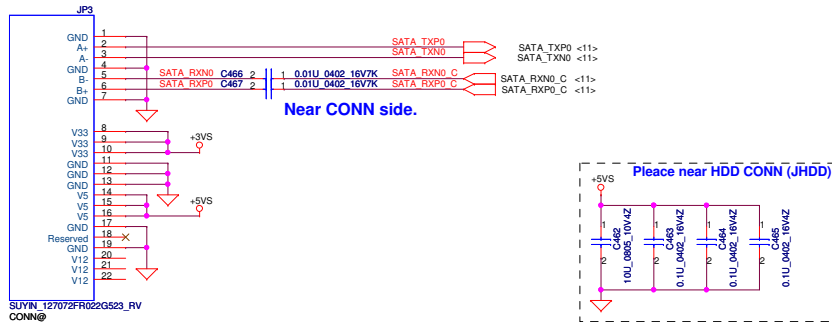


Security Classification				Compal Secret Data				Title			
Issued Date				2009/03/31				2010/03/31			
Deciphered Date											
Rev				1.0				1.0			

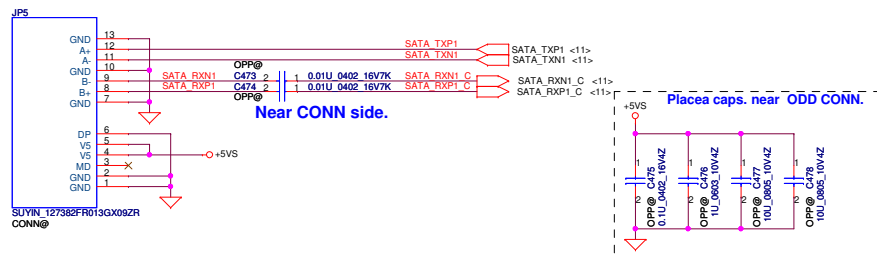
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Compal Electronics, Inc.
M92-S VRAM

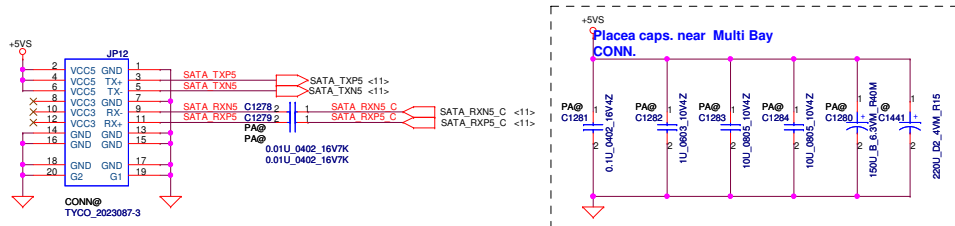
HDD Connector



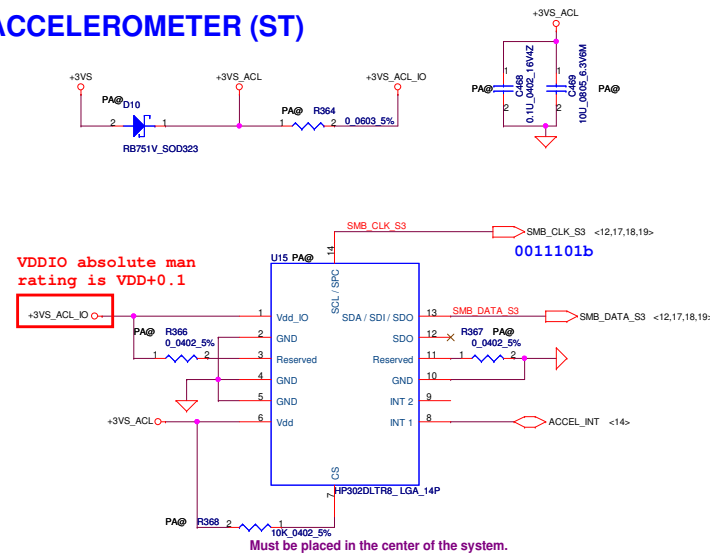
CD-ROM Connector



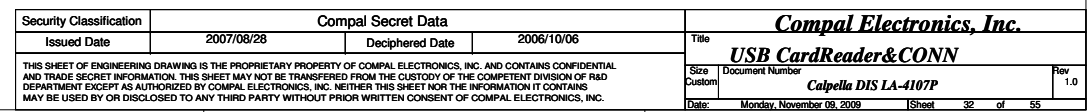
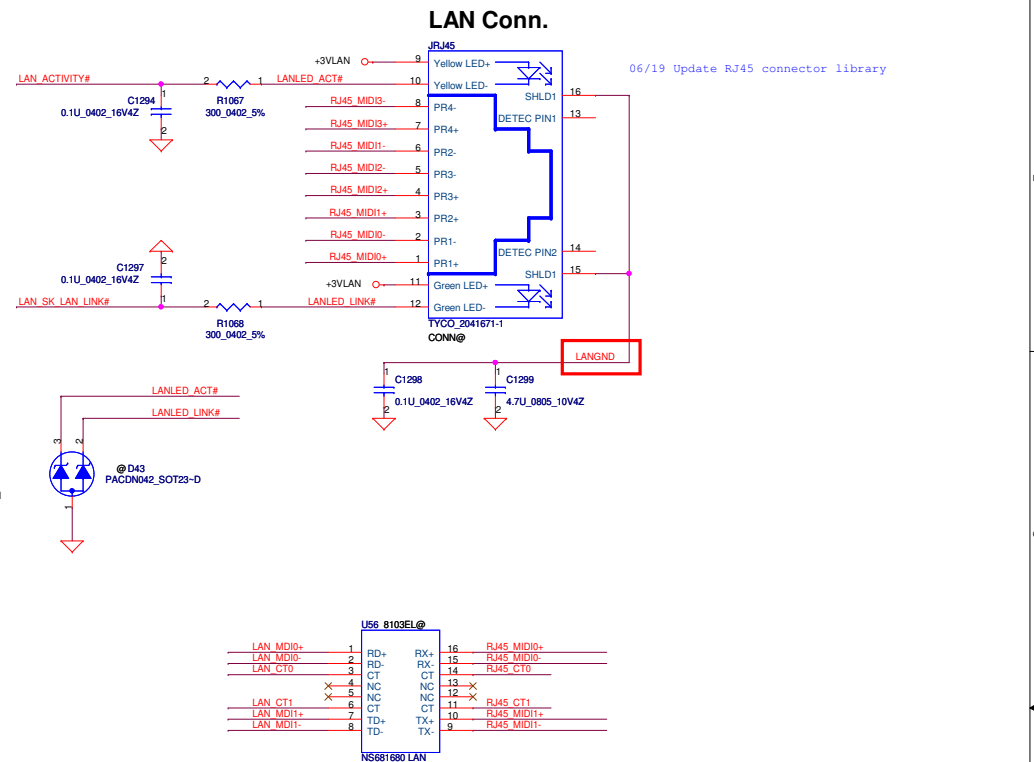
Multi Bay

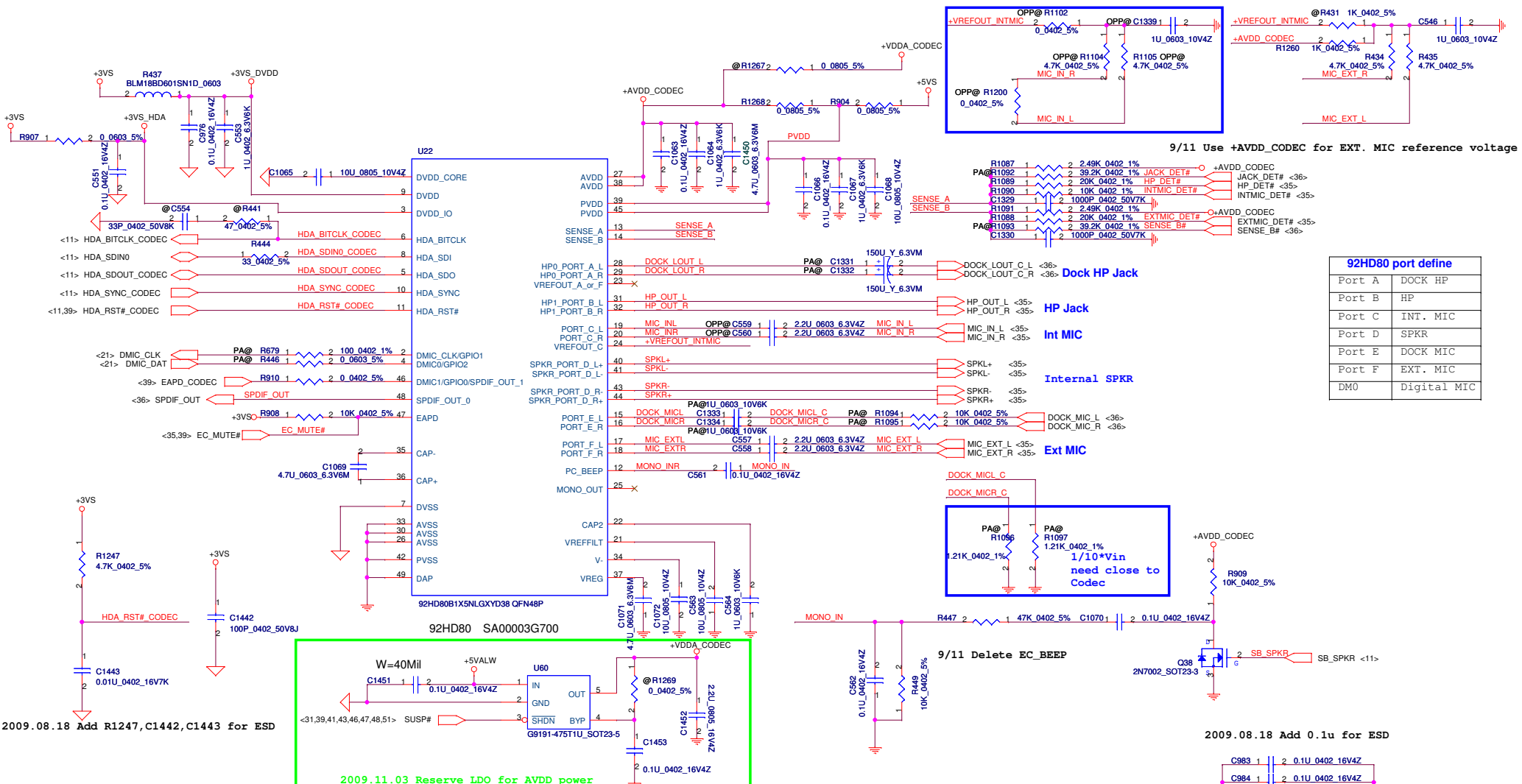


ACCELEROMETER (ST)

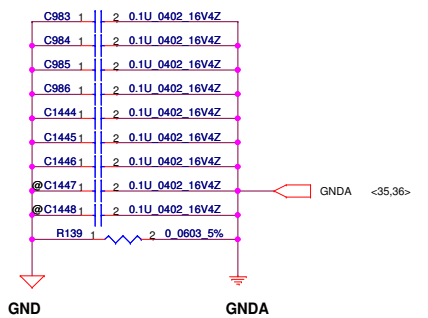
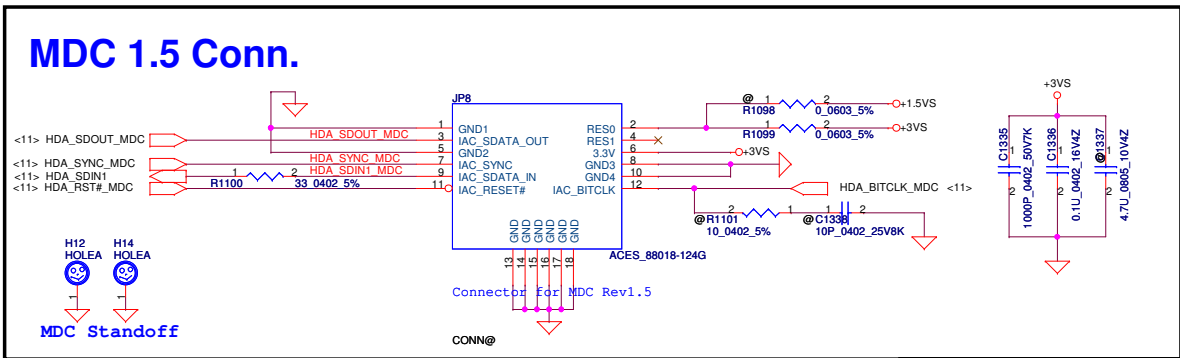


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Issued Date	2007/08/28	Deciphered Date	2006/03/10	Title	HDD & CDROM
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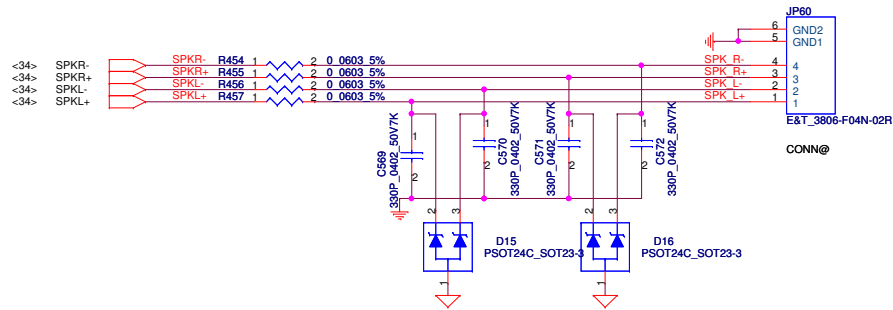


92HD80 port define	
Port A	DOCK HP
Port B	HP
Port C	INT. MIC
Port D	SPKR
Port E	DOCK MIC
Port F	EXT. MIC
DM0	Digital MIC

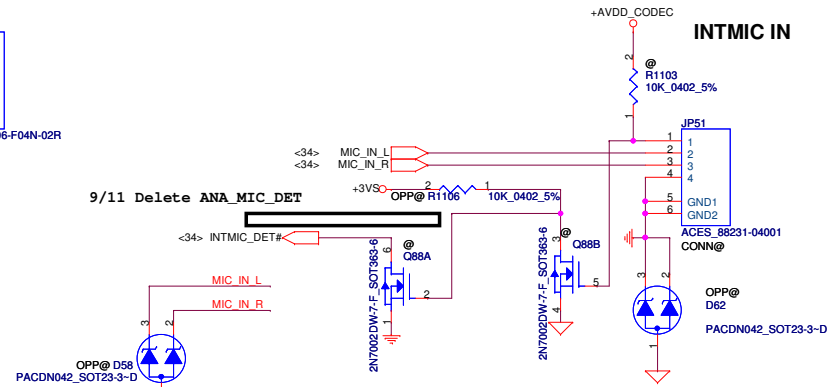


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				Custom	Calpella DIS LA-4107P
				Date	Monday, November 09, 2009
				Sheet	34 of 55
				Rev	1.0

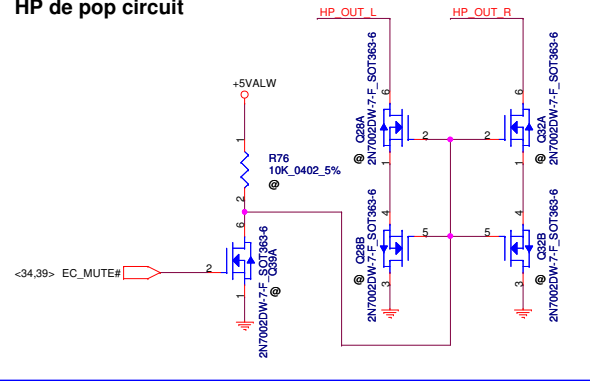
SPEAKER



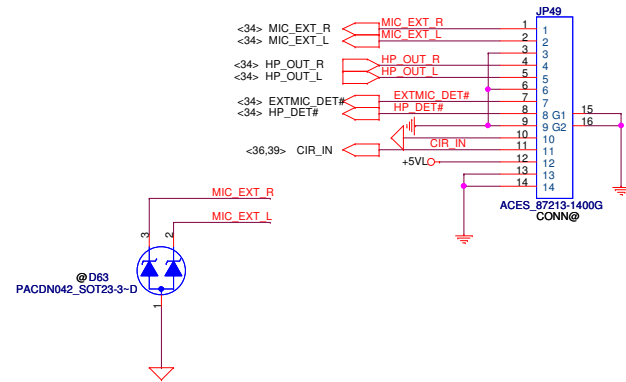
INTMIC IN



HP de pop circuit



Audio/B & CIR



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				Custom	Calpella DIS LA-4107P	1.0
				Date:	Monday, November 09, 2009	Sheet 35 of 55

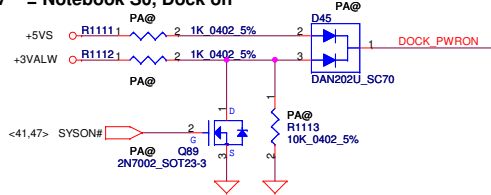
Atlas/ Saturn Dock

DOCK_PWR_ON Spec

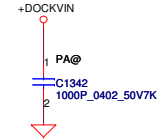
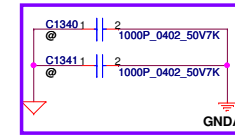
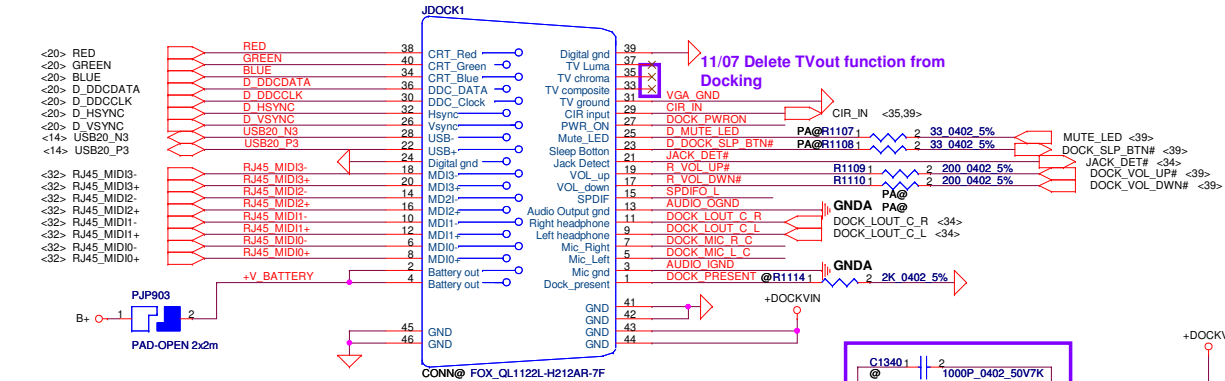
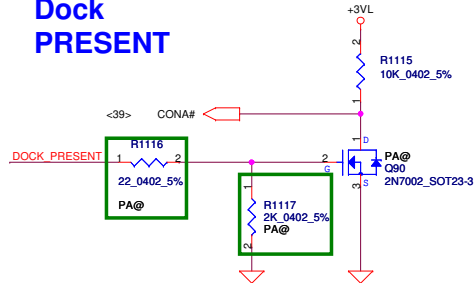
0V = Notebook S4/S5, Dock off

2.5V = Notebook S3, Dock on

4V = Notebook S0, Dock on

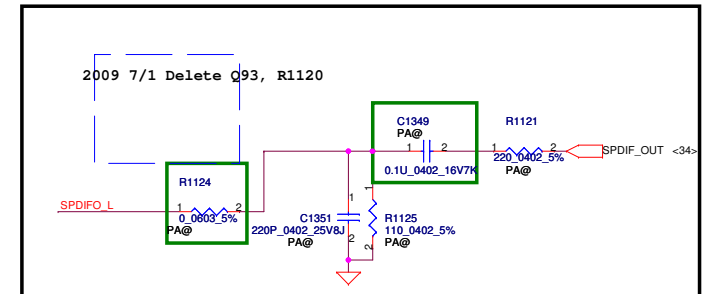
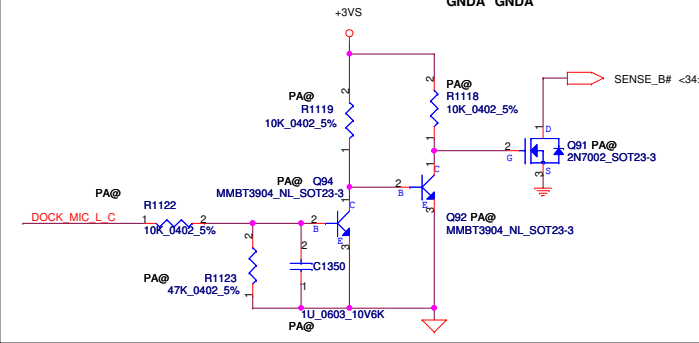
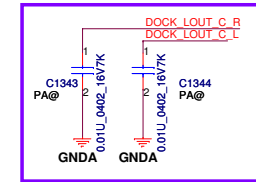
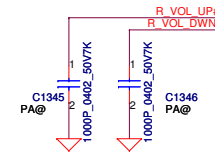
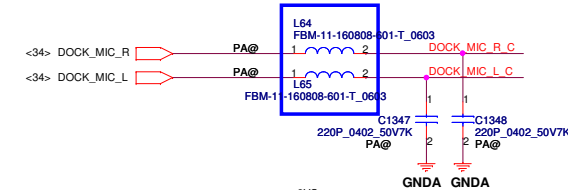


Dock PRESENT



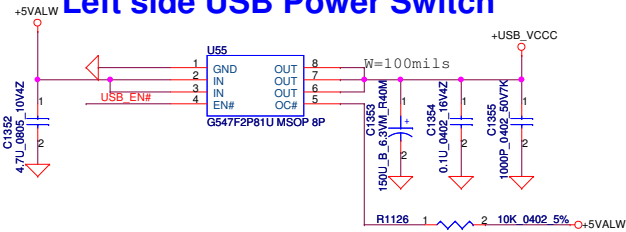
MIC_Dock

Need 600 Ohm 500 mA



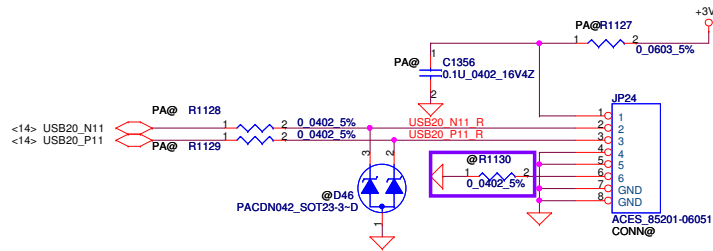
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				Customer	Calpella DIS LA-4107P
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Left side USB Power Switch

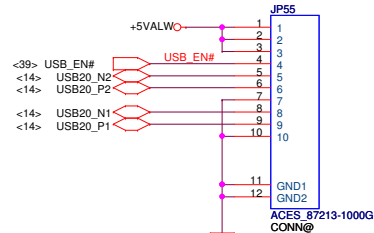


Finger printer

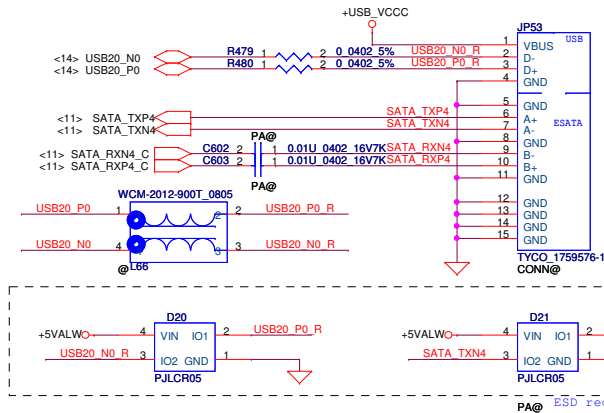
Change Finger printer from USB port7 to USB port 11



USB cable connector for Right side

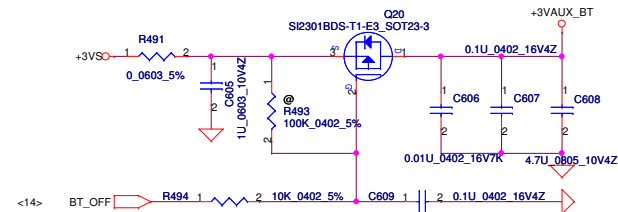
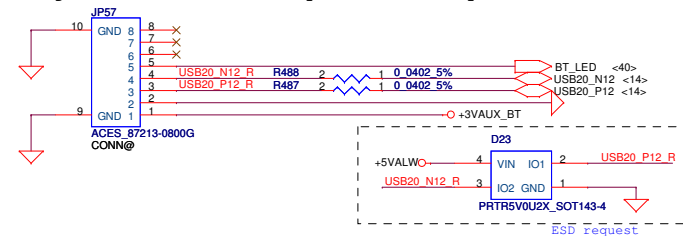


Left side ESATA/USB combination Connector



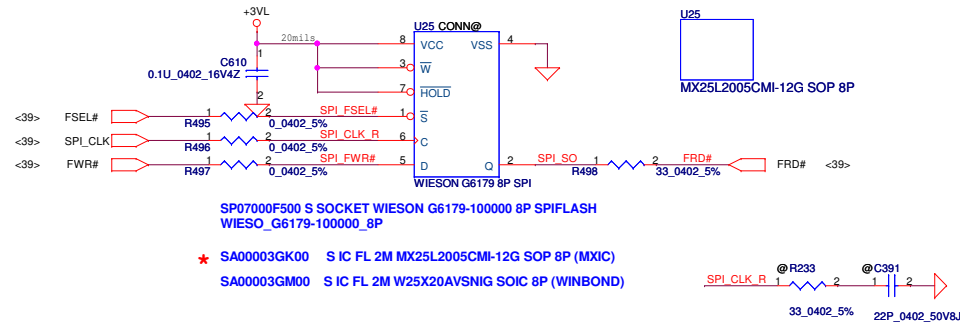
BT Connector (SoftBreeze) Need change to New version

Change Bluetooth from USB port 6 to USB port 12

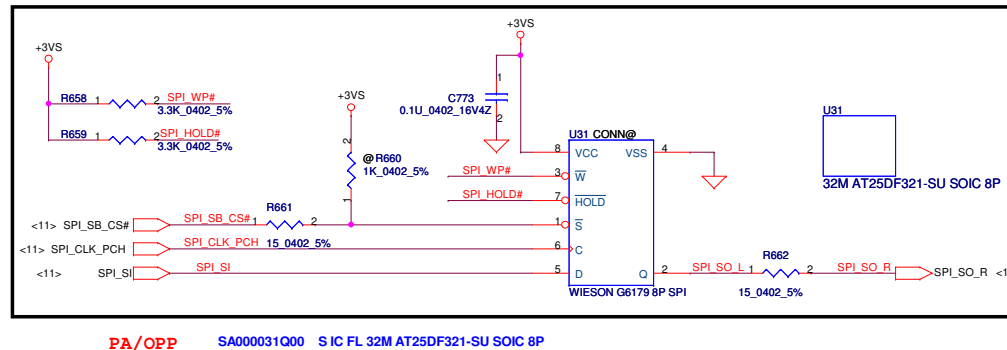


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					Calpella DIS LA-4107P	1.0
				Date:	Monday, November 09, 2009	Sheet 37 of 55

SPI ROM => 256K (EC code)

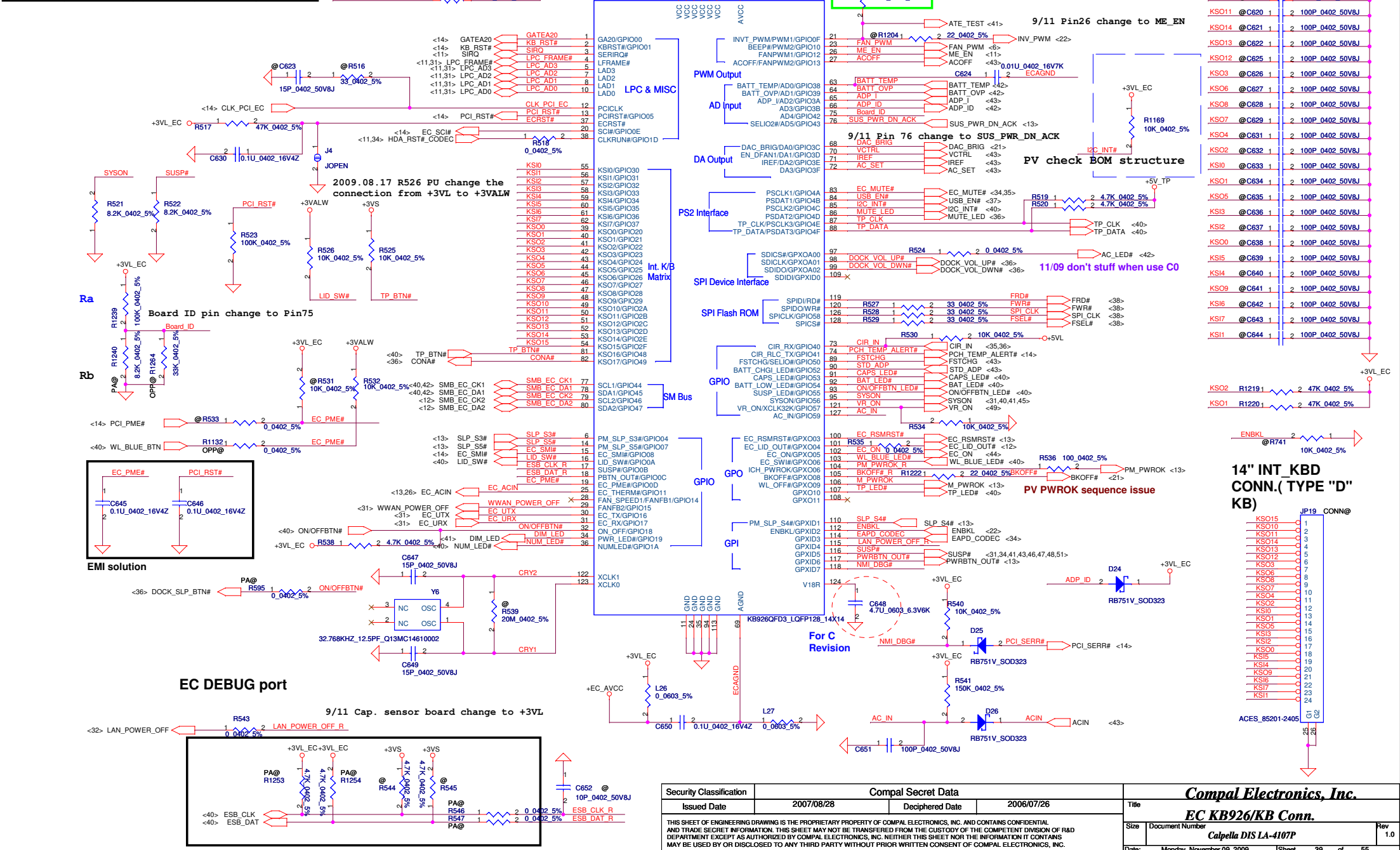


SPI ROM on PCH => 4M (ME code + System BIOS)



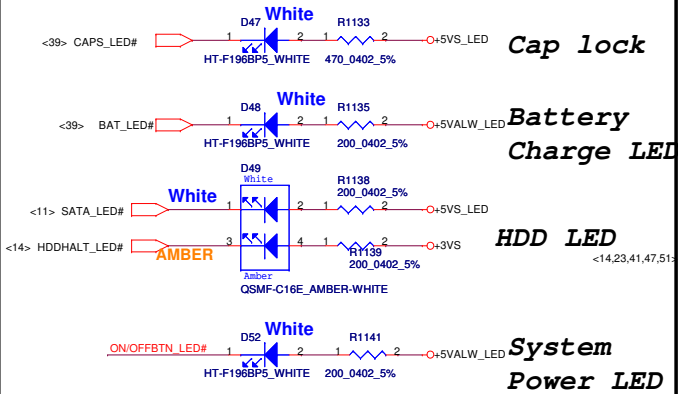
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				BIOS ROM	
				Calpella DIS LA-4107P	
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VCC	3.3V+/-5%			
Ra	100K+/-5%			
Board ID	Rb	V _{AD_RID} min	V _{AD_RID} typ	V _{AD_RID} max
Blade UMA	0	0V	0V	0V
Blade SG	8.2K+/-5%	0.216V	0.250V	0.289V
Bee UMA	18K+/-5%	0.436V	0.503V	0.538V
Bee DIS	33K+/-5%	0.712V	0.819V	0.875V

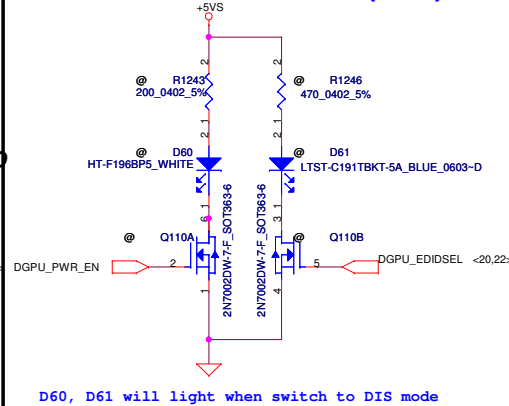


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2007/08/28		2006/07/26		EC KB926/KB Conn.	
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System & Caps-Lock LED

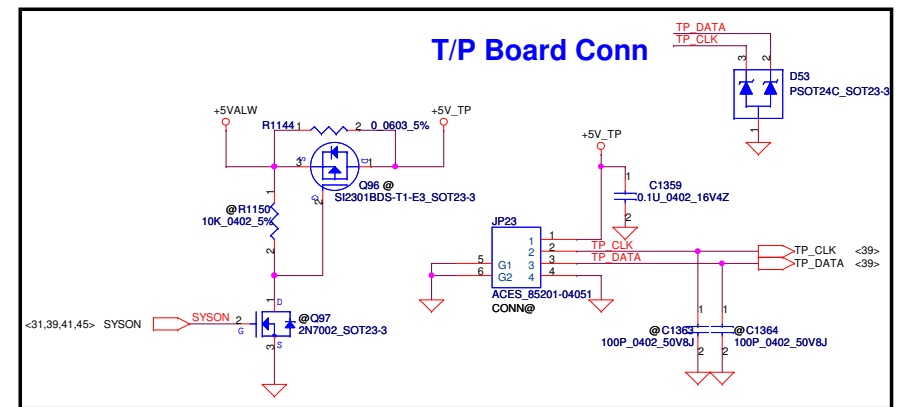
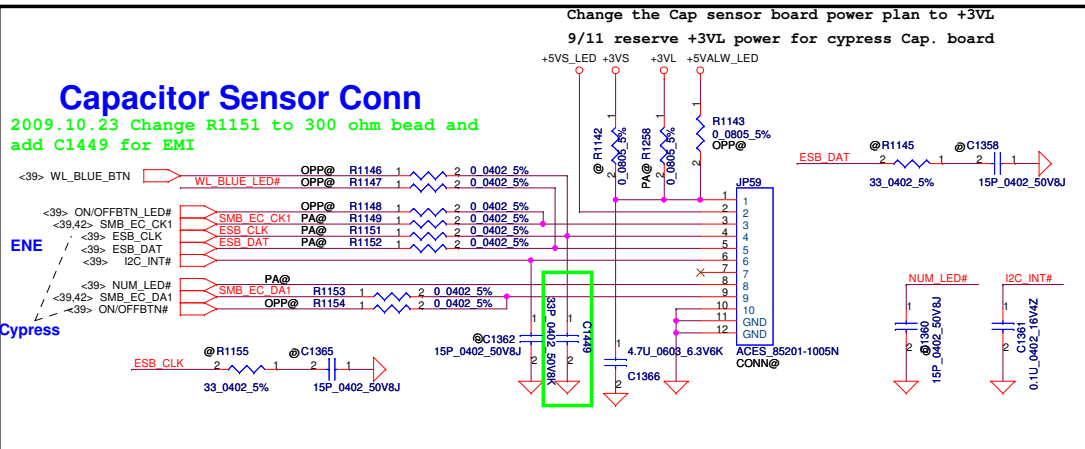
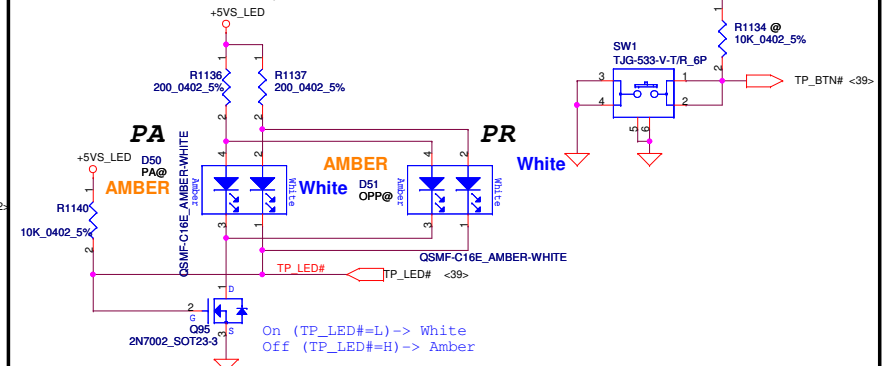


Switch function LED(test)

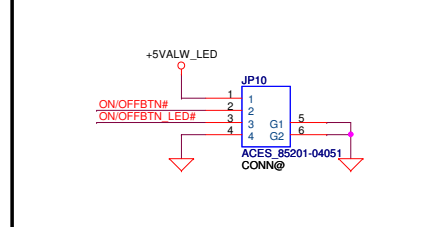


T/P Board (Include T/P_ON/OFF)

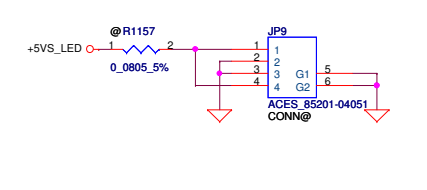
TouchPAD ON/OFF LED



ON/OFF Button Connector

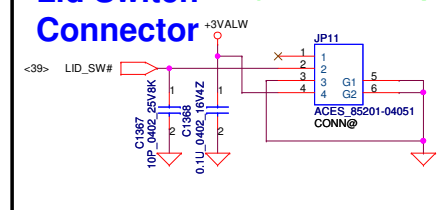


Keyboard backlight Conn

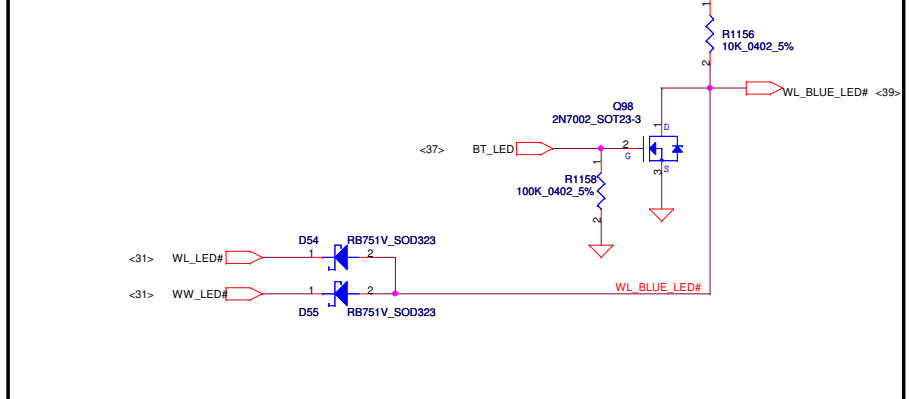


Lid Switch Connector

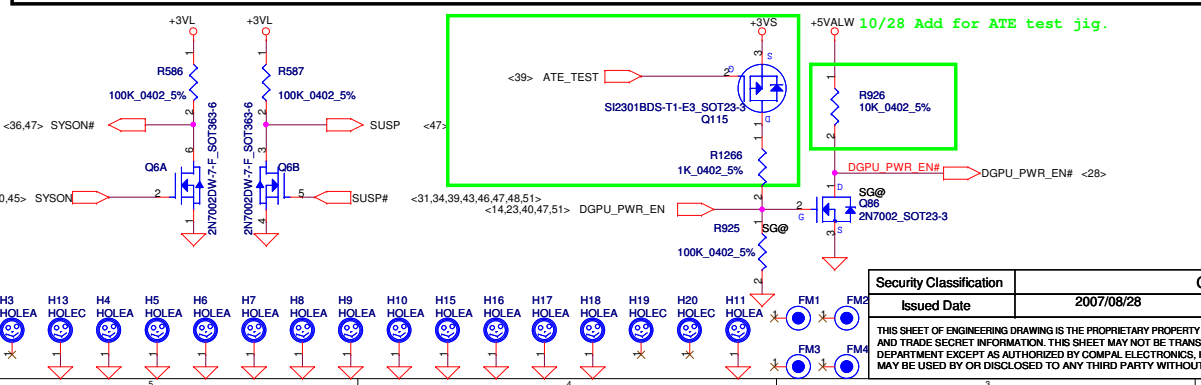
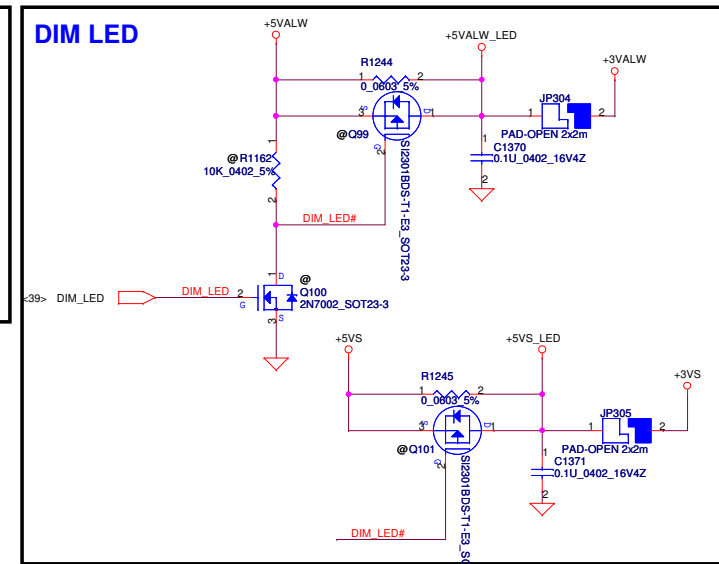
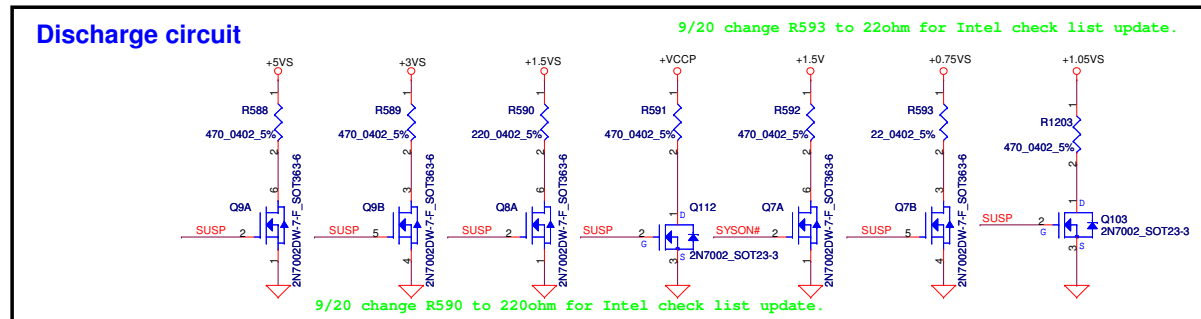
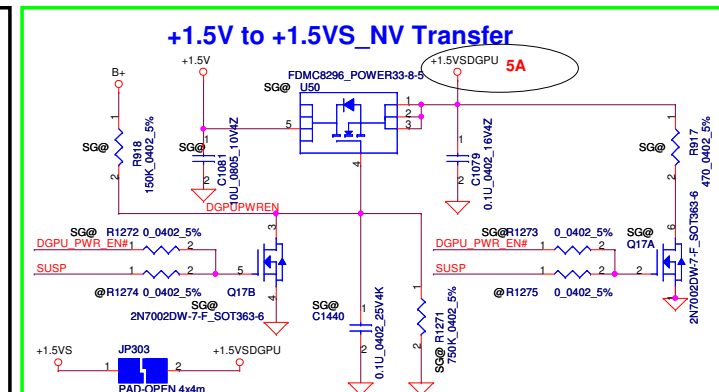
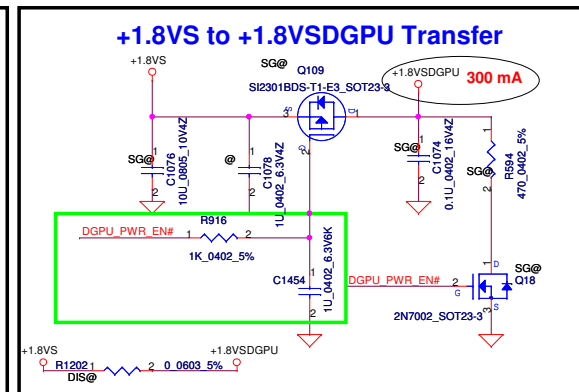
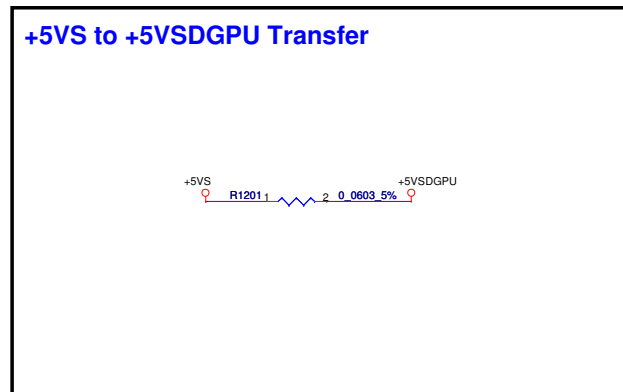
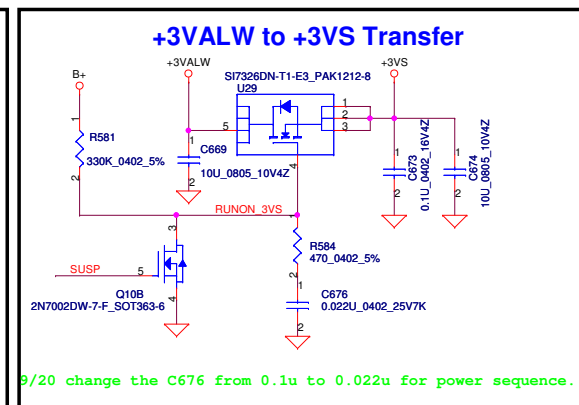
Change the Lid switch power plan to +3VALW



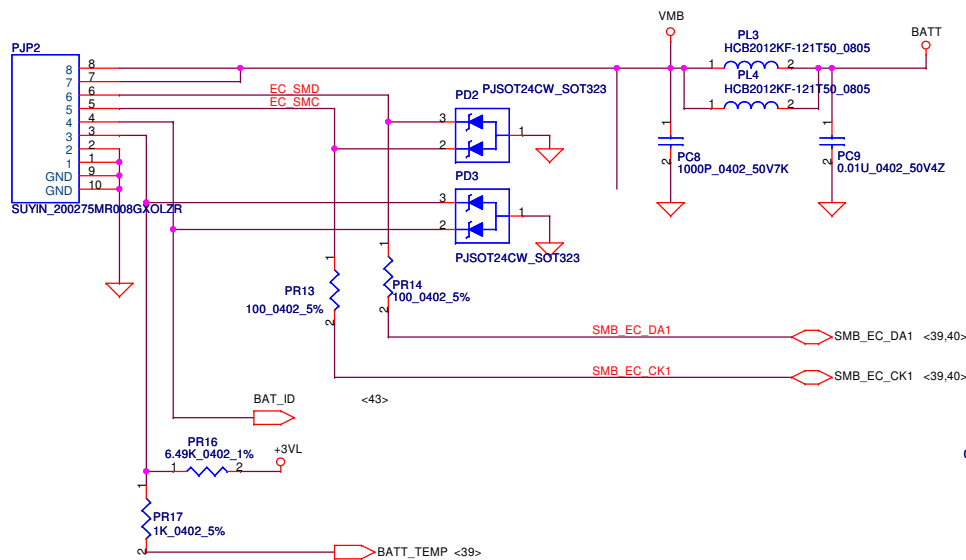
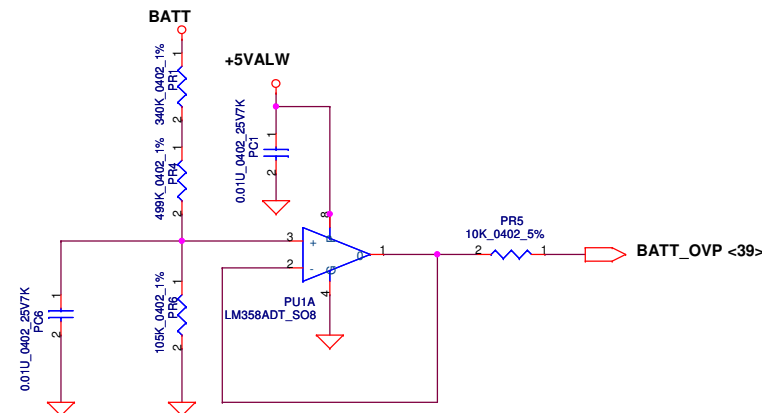
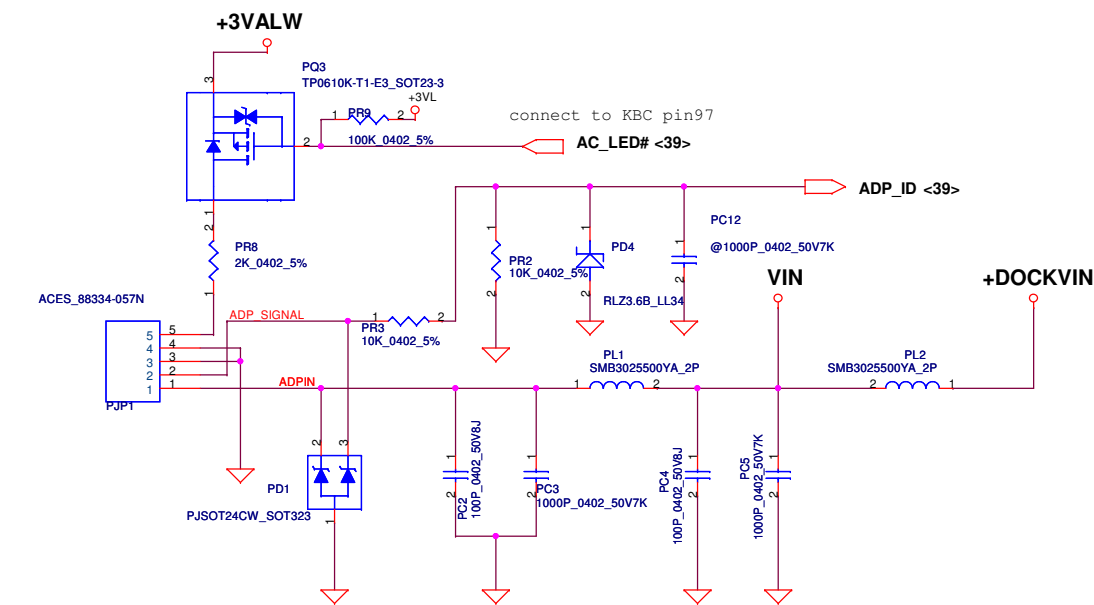
Mini card LED



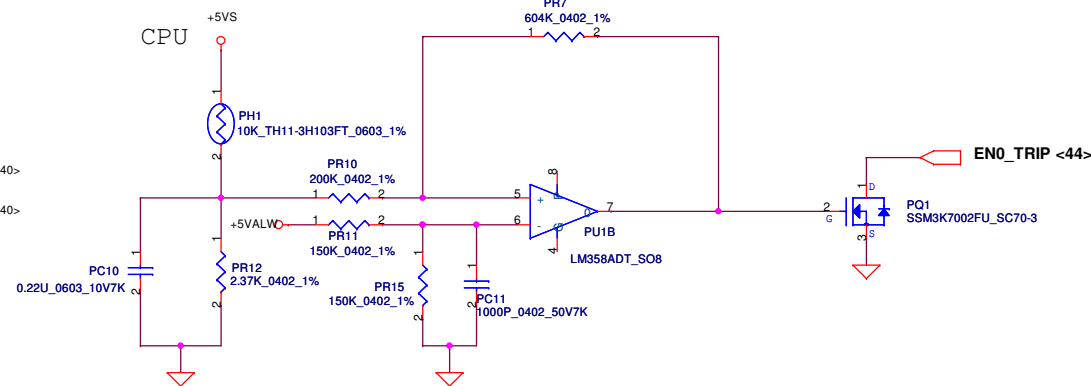
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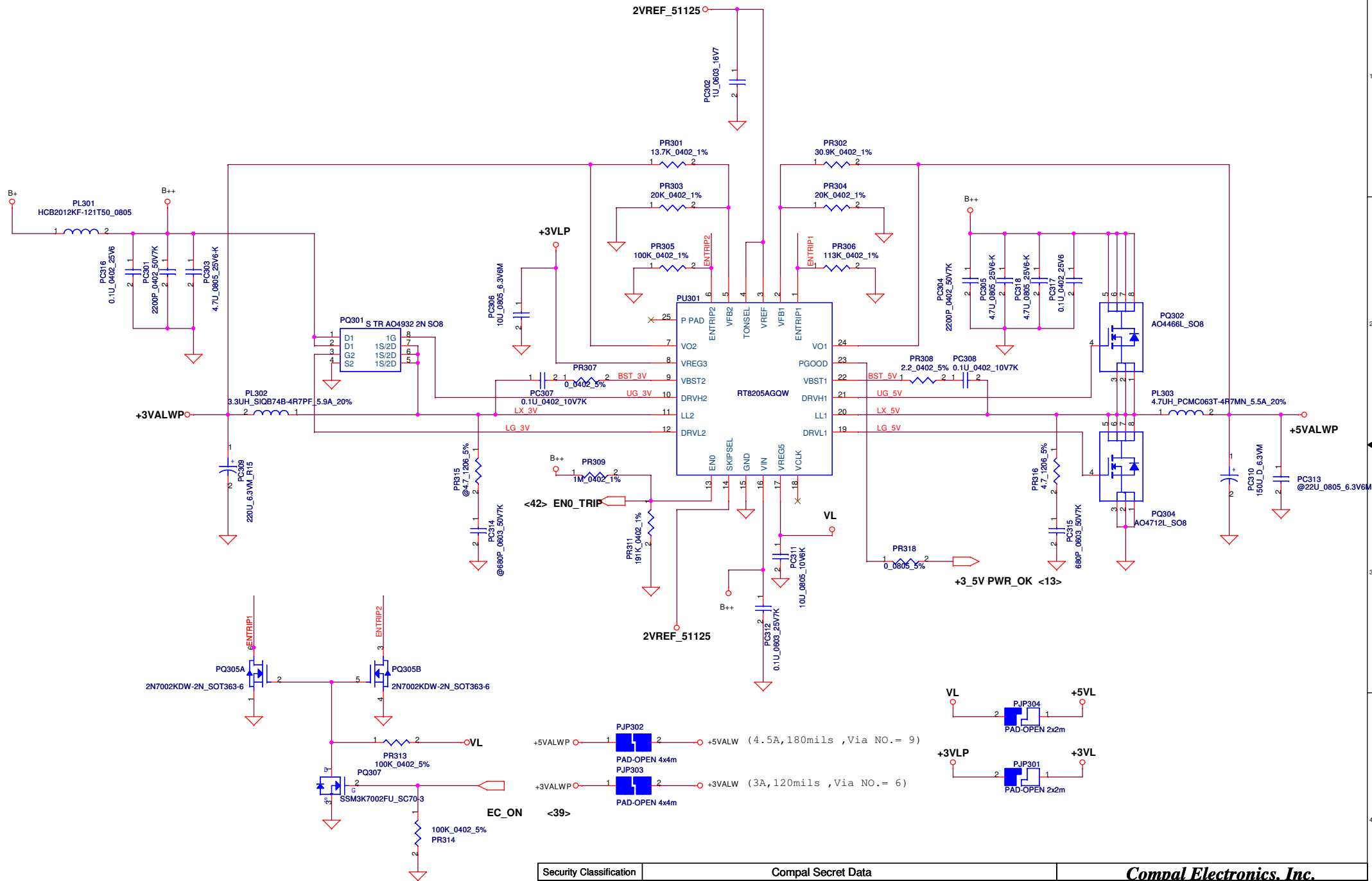
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PH1 under CPU bottom side :
CPU thermal protection at 90 +/-3 degree C



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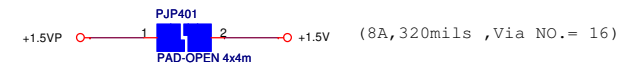
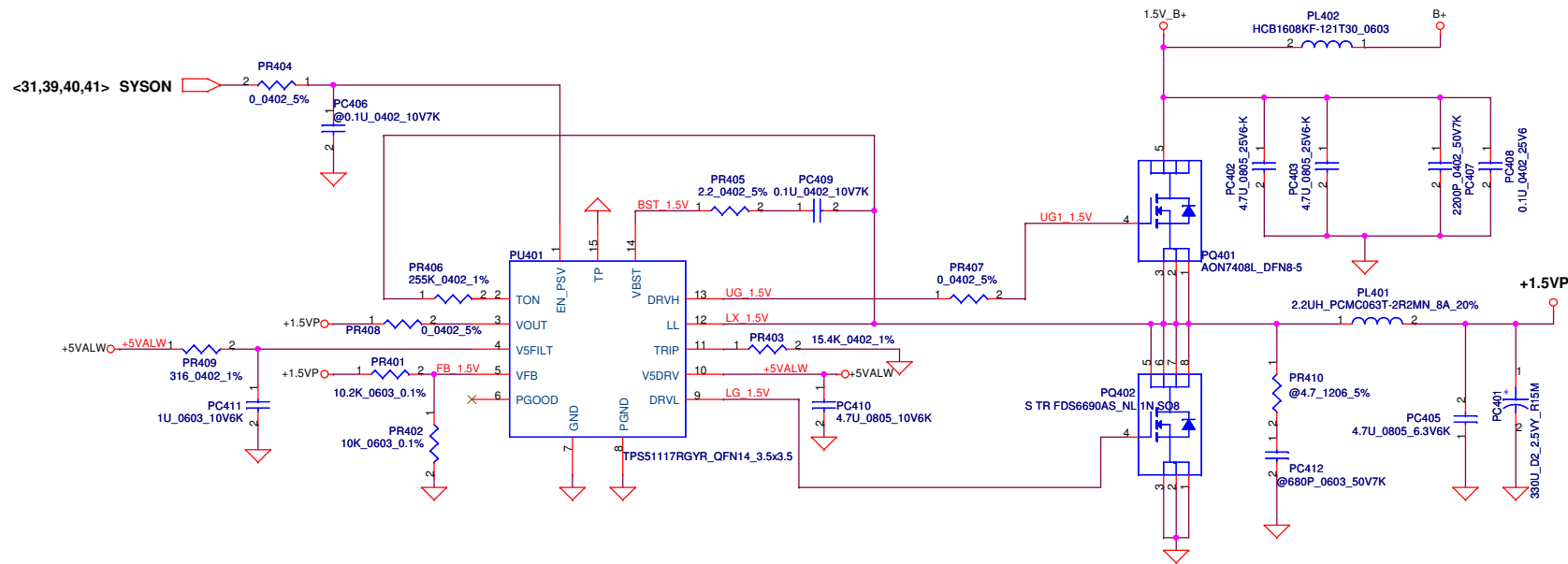
3.3VALWP/5VALWP

Calpella DIS LA-4107P

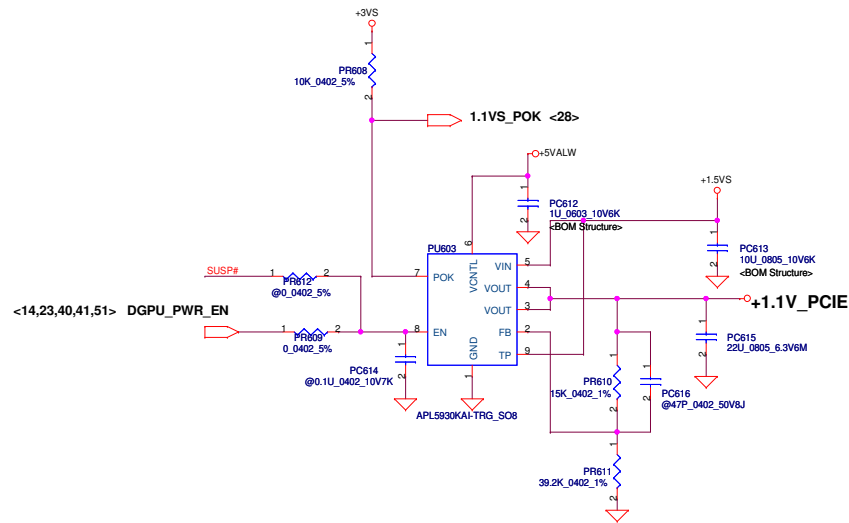
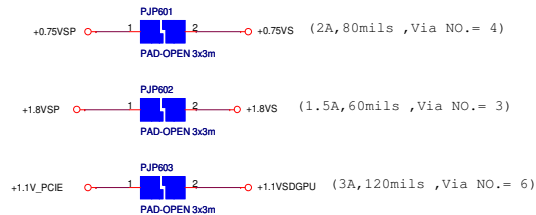
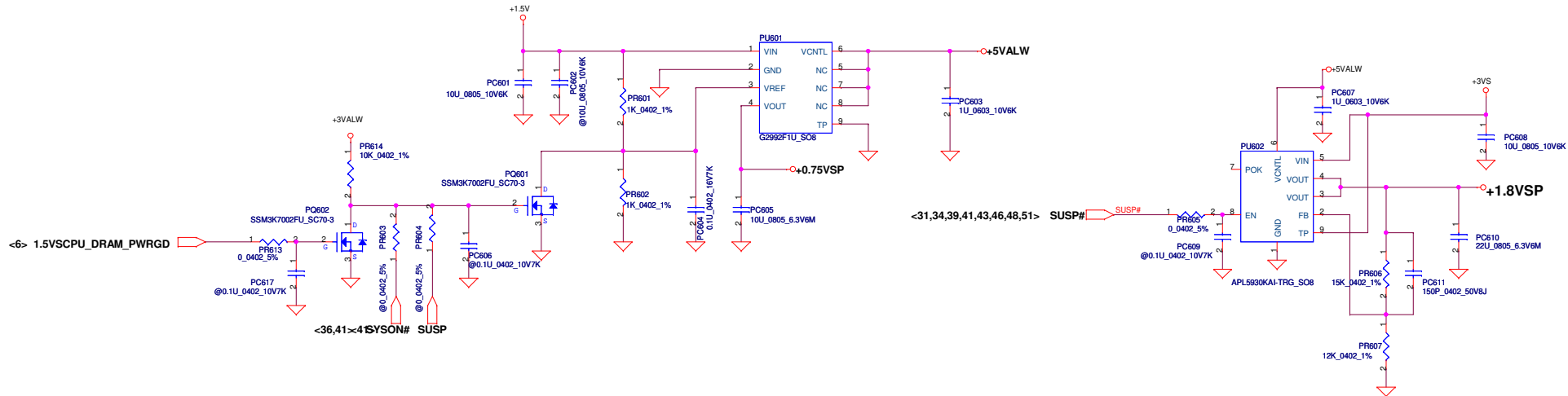
Monday, November 09, 2009

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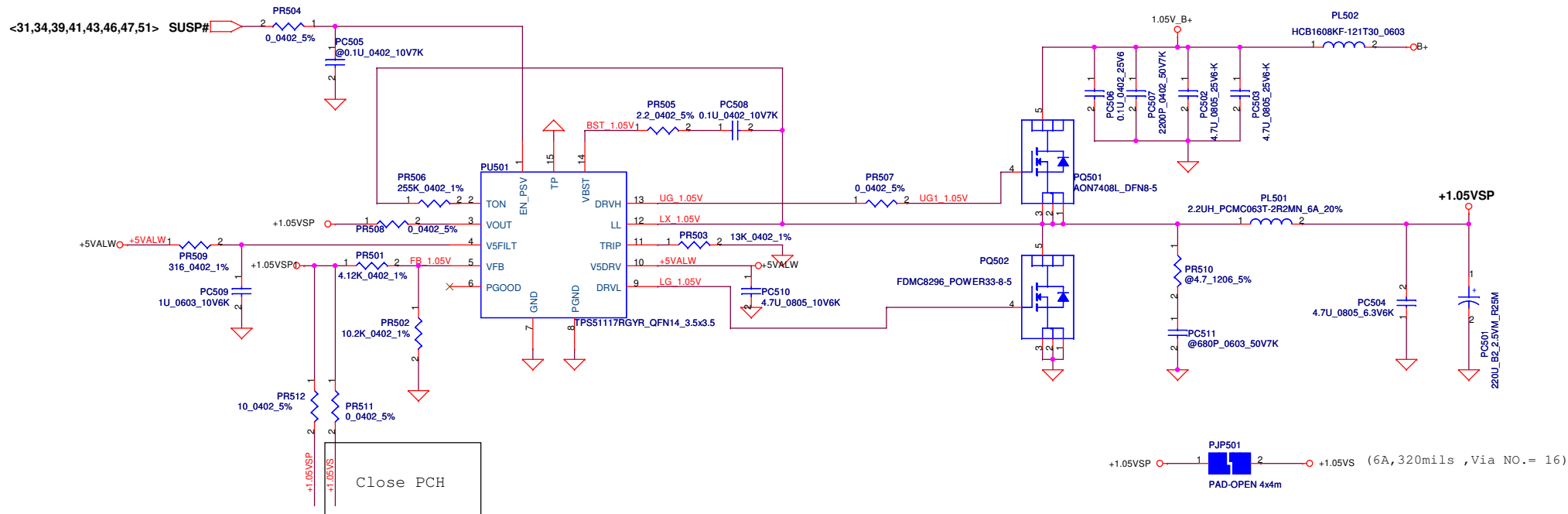
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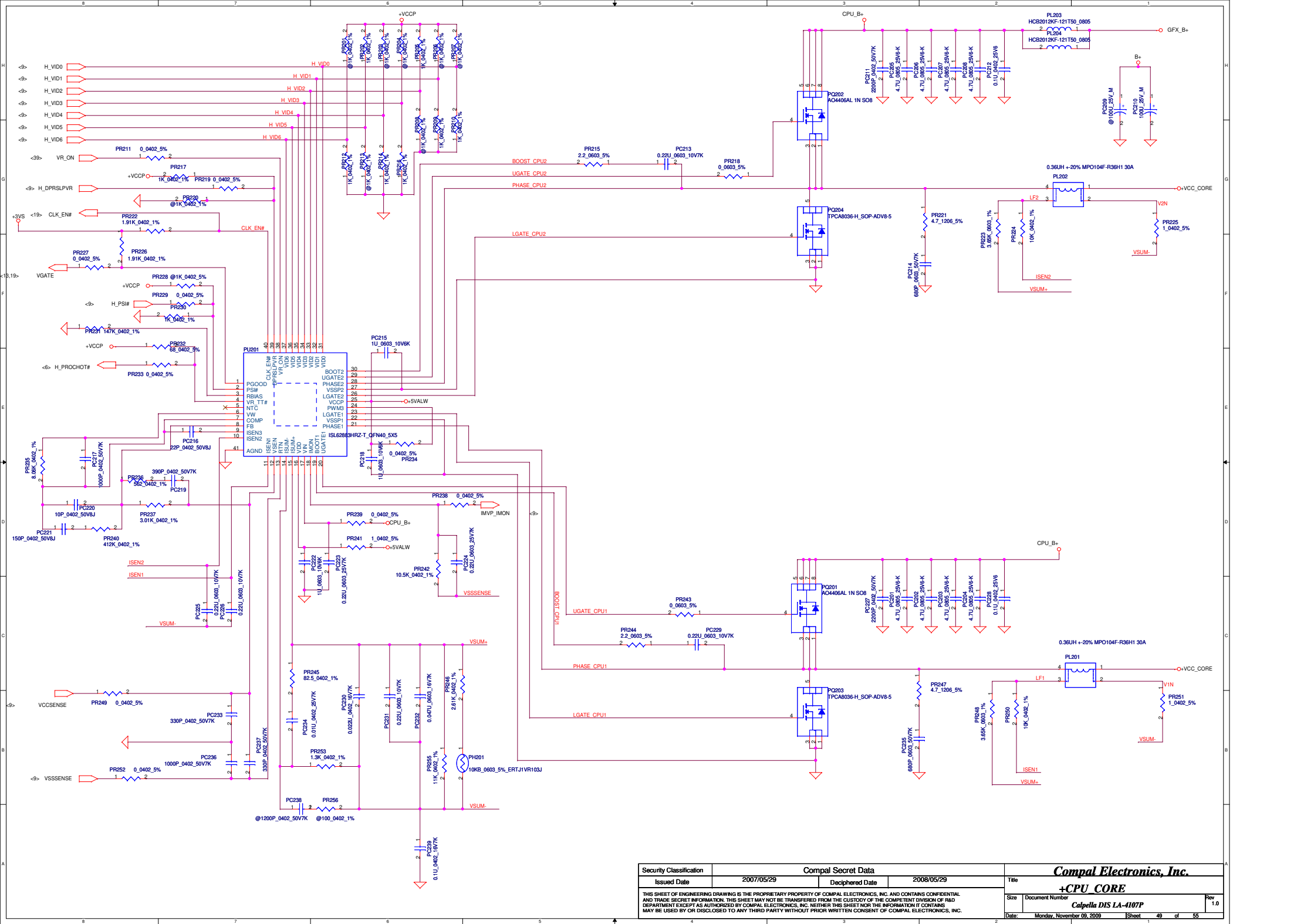
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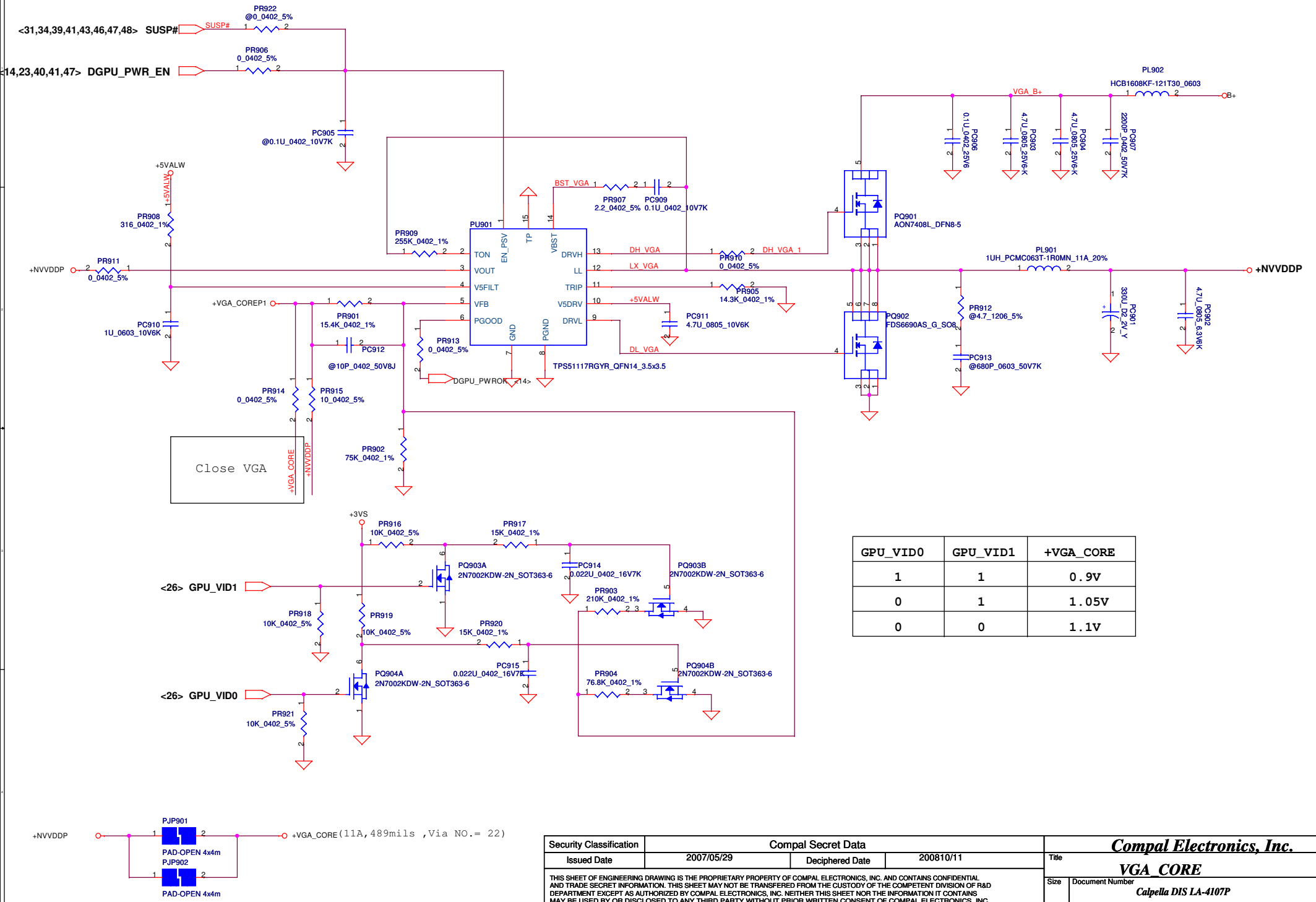
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Item	Fixed Issue (Reason for change)	PAGE	Modify List	Date	Phase
1	PLT_RST# need a PD resistor	14	Add R185 PD for PLT_RST#	08/6	PV
2	Remove MUX in CRT DDC circuit of SG design	20	Change to MOS design	08/6	PV
3	Remove MUX in LVDS ENAVDD circuit of SG design	21	Change to MOS design	08/6	PV
4	LCD panel will fail in OPP SKU	21	Add one 0 ohm resistor (R1238) for OPP SKU	08/6	PV
5	Remove MUX in LVDS I2C circuit of SG design	22	Change to MOS design	08/6	PV
6	OPP SKU: M93 and VRAM may have leakage in S3 mode	41	Change the power plan to +1.5VS of JP303	08/6	PV
7	8111VB power on timing issue	32	Add R1083 and C1319 to fine tune the power on timing	08/10	PV
8	Blade 2.0 need Board ID	39	Use EC GPIO48 for ID pin(Add R1239, R1240)	08/12	PV
9	EC GPIO17 will be used for debug card	39	LAN_POWER_OFF signal change to EC GPXID4(Pin 115)	08/12	PV
10	Cap. sensor board need to change the power source.	40	Change the power source of Cap. sensor board to +3VS	08/13	PV
11	Lid switch need to change the power source.	40	Change the power source of Lid switch to +3VALW and R526 PU to +3VALW.	08/13	PV
12	Change +1.8VS to +1.8VSDGPU Transfer design for cost down	41	Change the power MOS(U49) to 2301 PMOS(Q109).	08/13	PV
13	BIOS team doesn't need XDP connector	6	Remove the XDP connector	08/13	PV
14	Change +5VS to +5VSDGPU Transfer design for cost down	41	Use 0 ohm to contact +5VS and +5VSDGPU	08/13	PV
15	PCH_DDR_RST need use PCH GPIO46 to control	6	PCH_DDR_RST MOS gate control signal change from EC to PCH GPIO46	08/13	PV
16	Remove the 27MHz crystal of VGA	26	Use clock gen 27MHz source and stuff R216	08/14	PV
17	Q104 need change to low Vgs type	6	Change the Q104 to BSS138 P/N:SB501380020	08/18	PV
18	Cost down plan	9	Change the C995,C996 330u to ESR=9m ohm	08/14	PV
19	Cost down plan	9	Change the C64 from 330u to 220u	08/14	PV
20	Cost down plan	9	Change the C61,C62,C67,C68,C69,C76,C82 from 22u to 10u	08/14	PV
21	Cost down plan	9	Change the C200 330u to ESR=9m ohm	08/14	PV
22	Cost down plan	9	Un-stuff C204,C228 and C229	08/14	PV
23	Docking no sound when play music	34	Need to stuff R910	08/14	PV
24	Audio new Mapping	34	Exchange the port A and port F	08/14	PV
25	We won't have DIM_LED function	41	Un-stuff Q99,Q101 and add two 0 ohm(R1244,R1245) resistors for LED power source.	08/14	PV
26	ESD issue	34	Add R1247,C1442,C1443 and change the C983~C986, C1444~C1446 to 0.1u	08/18	PV
27	Black light issue(will see the garbage when boot)	22	Change the black light enable schematic design.	08/18	PV
28	CPU leakage issue	6	Change the design for Intel's power leakage issue when go into S3 mode	08/19	PV

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Item	Fixed Issue (Reason for change)	PAGE	Modify List	Date	Phase
29	INT.MIC ESD issue	35	Add D58 and D62 for ESD issue	08/18	PV
30	EXT.MIC ESD issue	35	Reserve D63 for Ext. MIC	08/18	PV
31	Reserve PU resistors to +3VL for ESB BUS	39	Reserve R1253,R1254 for ESB bus	08/21	PV
32	Make sure power sequence is correct	6,47	Use 1.5VSCPU_DRAM_PWRGD to enable 0.75VS power	09/11	PV2
33	Add ME_EN# for PCH GPIO33	11	Add inverter circuit for ME_EN signal	09/11	PV2
34	+3VS_VGA will have leakage when switch to IGPU mode	12	Change Q4 pin2 and pin5 to +3VS_VGA	09/11	PV2
35	Need contact SUS_PWR_DN_ACK between EC and PCH	13	Use PCH GPIO30 and EC pin76 for SUS_PWR_DN_ACK	09/11	PV2
36	Need add VGA ID pin for M93 and M93 LP	14	Use PCH GPIO57 for VGA ID pin	09/11	PV2
37	Change 27MHz clock source of VGA to Y7	19,26	non-stuff R216	09/11	PV2
38	Q37 dual package will have floating isse	22	Change Q37 to single package	09/11	PV2
39	Fix 8103 BOM isse	32	Add R1259 for 8103EL LAN chip	09/11	PV2
40	Fix EXT. MIC reference voltage issue	34	Change the reference voltage to +AVDD_CODEC	09/11	PV2
41	Remove EC_BEEP function	34	Delete EC_BEEP function	09/11	PV2
42	Remove Analog MIC detect function	35,39	Delete ANA_MIC_DET signal from EC and codec	09/11	PV2
43	EMI need to add chock for ESATA/USB port	37	Add L66 for ESATA/USB port	09/11	PV2
44	HM55 PCH will disable USB port6 and port7	37	Change Finger printer from USB port7 to USB port 11	09/11	PV2
45	HM55 PCH will disable USB port6 and port7	37	Change Bluetooth from USB port 6 to USB port 12	09/11	PV2
45	Remove EC_BEEP function	39	Change Pin 26 from EC_BEEP to ME_EN	09/11	PV2
46	Fix PV phase Board ID issue	39	Exchange TP_BTN# and Board_ID pin	09/11	PV2
47	Cypress Cap. sensor board need use +3VL power	40	Change Cap. sensor board power to +3VL	09/11	PV2
48	Adjust +3VS / +1.5VS power sequence	41	Change C676,C770 from 0.1u to 0.022u	09/12	PV2
49	PLT_RST# don't need PD resistor	14	Un-stuff R185	09/20	MV
50	Follow Intel to adjust +0.75VS discharge timing	41	Change R593 from 470ohm to 22ohm	09/20	MV
51	Follow Intel to adjust +1.5VS discharge timing	41	Change R590 from 470ohm to 220ohm	09/20	MV
52	Follow Intel Check list 2.0	15	Un-stuff C187 and C192	09/20	MV
53	EDID signal need to add PU resistor	22	Add R1261 for EDID DATA	09/20	MV
54	VCCADAC dosen't need LC filter when DIS only	15	Change L45 to 0 ohm resistor for OPP SKU	10/01	MV
55	GFX core power transient fail	9	Change C996 to 330u 7m ohm	10/21	MV

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Version Change List (P. I. R. List) for Power Circuit

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Note
1	44	PWR-3.3VALWP/5VALWP	8/12	PWR	all cap no more than 0805	Add PC318,PC305 from 1206 to 0805 and parallel with PC318	DB to PV1
2	49	PWR-CPU_CORE	8/13	PWR	OCP & IMON ajustment and Fixed LL to match INTEL Spec	Change PR253 from 1.1K to 1.3K,Change PR242 from 8.25K to 10.5K Change PR237 from 2.43K to 3.01K	DB to PV1
3	49	PWR-CPU_CORE	8/17	PWR	RF Solution	Change PQ201 PQ202 from AO4474L to AO4406AL,PR215 PR244 from 0 to 2.2	DB to PV1
4	47	PWR-0.75VP/1.8VSP	8/20	PWR	Cost Down plan	Change PU602 from APL5915 to APL5930	DB to PV1
5	43	PWR-Charger	8/20	PWR	Smart Charger	Change PR113 from 143K to 140K, Change PC117 from 1u to 0.1u, Add PR114	DB to PV1
6	49	PWR-CPU_CORE	8/20	PWR	Avoide DFX interfere	Delete PC209 and add PC210	DB to PV1
7	46	PWR-1.05V_VCCP	8/24	PWR	Follow HW Suggestion Pull-up resistor connect to 3VS	Add PR705 connect to 3VS, remove PR706	DB to PV1
8	45	PWR-1.5VP	8/24	PWR	PU401 second source solution	PR403 from 13.7K to 15.4K	DB to PV1
9	46	PWR-1.05V_VCCP	8/24	PWR	PU701 second source solution	PR703 from 8.06K to 6.98K	DB to PV1
10	49	PWR-CPU-CORE	8/28	PWR	Improve transient response	Add PC230	DB to PV1
11	46	PWR-1.05V_VCCP	9/2	PWR	Cost down plan	Change PC701 PC702 PC703 from 330u 6m ohm to 330u 9m ohm	DB to PV1
12	46	PWR-1.05V_VCCP	9/3	PWR	Improve VCCP Ripple	Del PC717	DB to PV1
13	50	GFX_CORE	9/11	PWR	Let GFX IMON measure easily	Add PR833 connect to GFRXVR_IMON and PU801 pin 13	PV1 to PV2
14	47	PWR-0.75VP/1.8VSP	9/11	PWR	For HW requirement add 1.5VSCPU_DRAM_PWRGD	Add 1.5VSCPU_DRAM_PWRGD add PR613 connect to PQ601 pin 2 and Delet PR604	PV1 to PV2