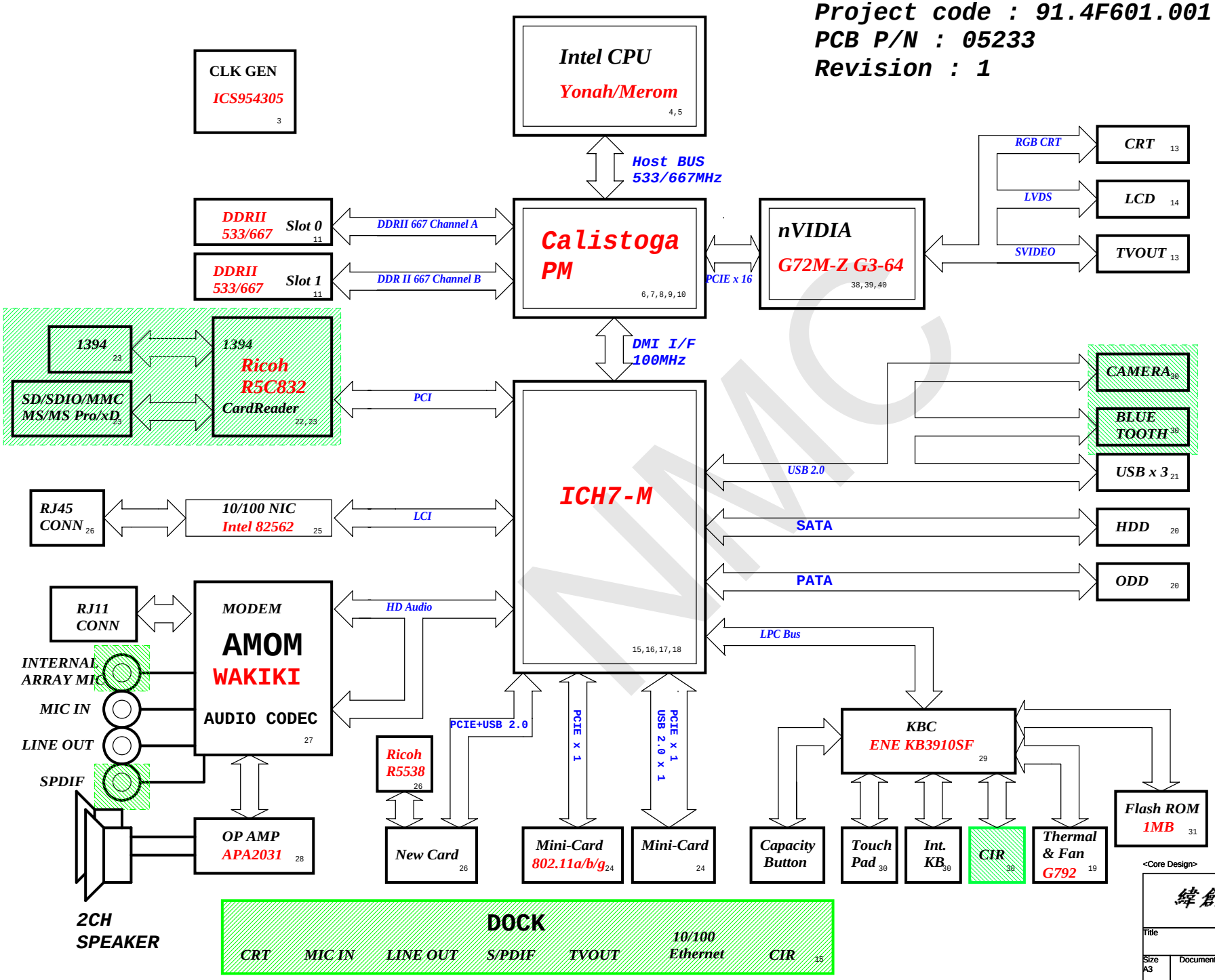
KAI Block Diagram

Project code : 91.4F601.001
PCB P/N : 05233
Revision : 1



SYSTEM DC/DC TPS51120	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3V_S5

SYSTEM DC/DC MAX8743	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3

MAXIM CHARGER MAX8725	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 3.0A 5V 100mA

CPU DC/DC MAX8736ETL	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 44A

PCB LAYER

L1:	Signal 1
L2:	GND
L3:	Signal 2
L4:	Signal 3
L5:	VCC
L6:	Signal 4
L7:	GND
L8:	Signal 5

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Block Diagram		
Size: A3	Document Number: KAI	Rev: 1
Date: Wednesday, April 19, 2006	Sheet 1 of 44	

Calistoga Strapping Signals and Configuration

page 7

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4** (Default)
CFG6		0=Moby Dick 1=Calistoga
CFG7	CPU Strap	0 = Reserved **1 =Mobile CPU(Default)**
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG[11:10]	Reserved	
CFG[13:12]	Reserved	
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG17	Global R-comp Disable (All R-comps)	0 = All R-comp Disable **1 = Normal Operation (Default)**
CFG18	VCC Select	**0 = 1.05V** (Default) 1 = 1.5V
CFG19	DMI Lane Reversal	**0 = Normal operation (Default):lane Numbered in order** 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	**0 = Only SDVO or PCIE x1 is operational (Default)** 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCRTL_DATA	SDVO Present	**0 = No SDVO device present** (Default) 1= SDVO device present

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORK In signal.

ICS954305 Spread Spectrum Select

page 3

SS3	SS2	SS1	SS0	Spread Amount%
0	0	0	0	-0.5
0	0	0	1	-1.0
0	0	1	0	-1.5
0	0	1	1	-2.0
0	1	0	0	-0.75
0	1	0	1	-1.25
0	1	1	0	-1.75
0	1	1	1	-2.25
1	0	0	0	+/-0.25
1	0	0	1	+/-0.5
1	0	1	0	+/-0.75
1	0	1	1	+/-1.0
1	1	0	0	+/-0.25
1	1	0	1	+/-0.5
1	1	1	0	+/-0.75
1	1	1	1	+/-1.0

PCI Routing

	IDSEL	IRQ	REQ/GNT
R5C832	25		0

ICH7M Integrated Pull-up and Pull-down Resistors

ICH6-M EDS 14308 0.8V1

ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, GNT[5]#/GPO[17], GNT[6]#/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]#/FB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
LAN_RXD[2:0]	ICH6 internal 10K pull-ups
ACZ_RST#, ACZ_SDIN[2:0], ACZ_SYNC, ACZ_SDOUT, ACZ_BITCLK, DPRSLPVR, SPKR, EE_CS,	ICH6 internal 20K pull-downs
USB[7:0][P,N]	ICH6 internal 15K pull-downs
DD[7], SDDREQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

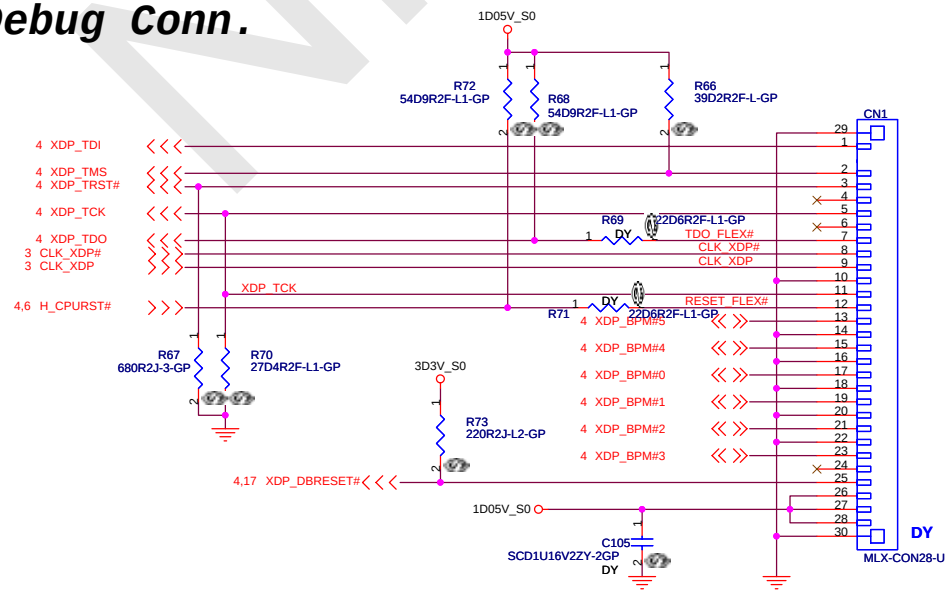
ICH7M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

History

11.18.2004: mini card not ready

ITP Debug Conn.



<Core Design>

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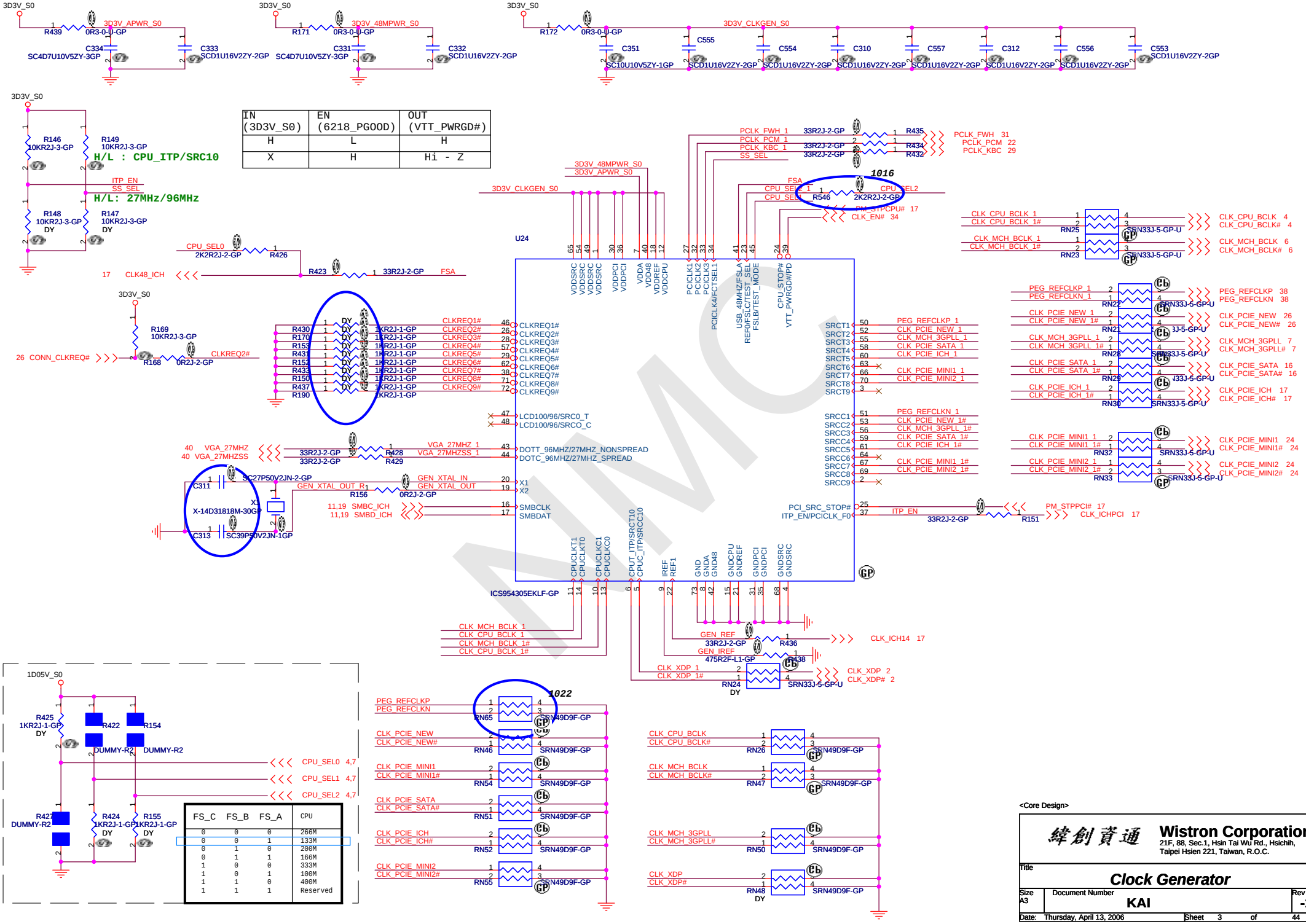
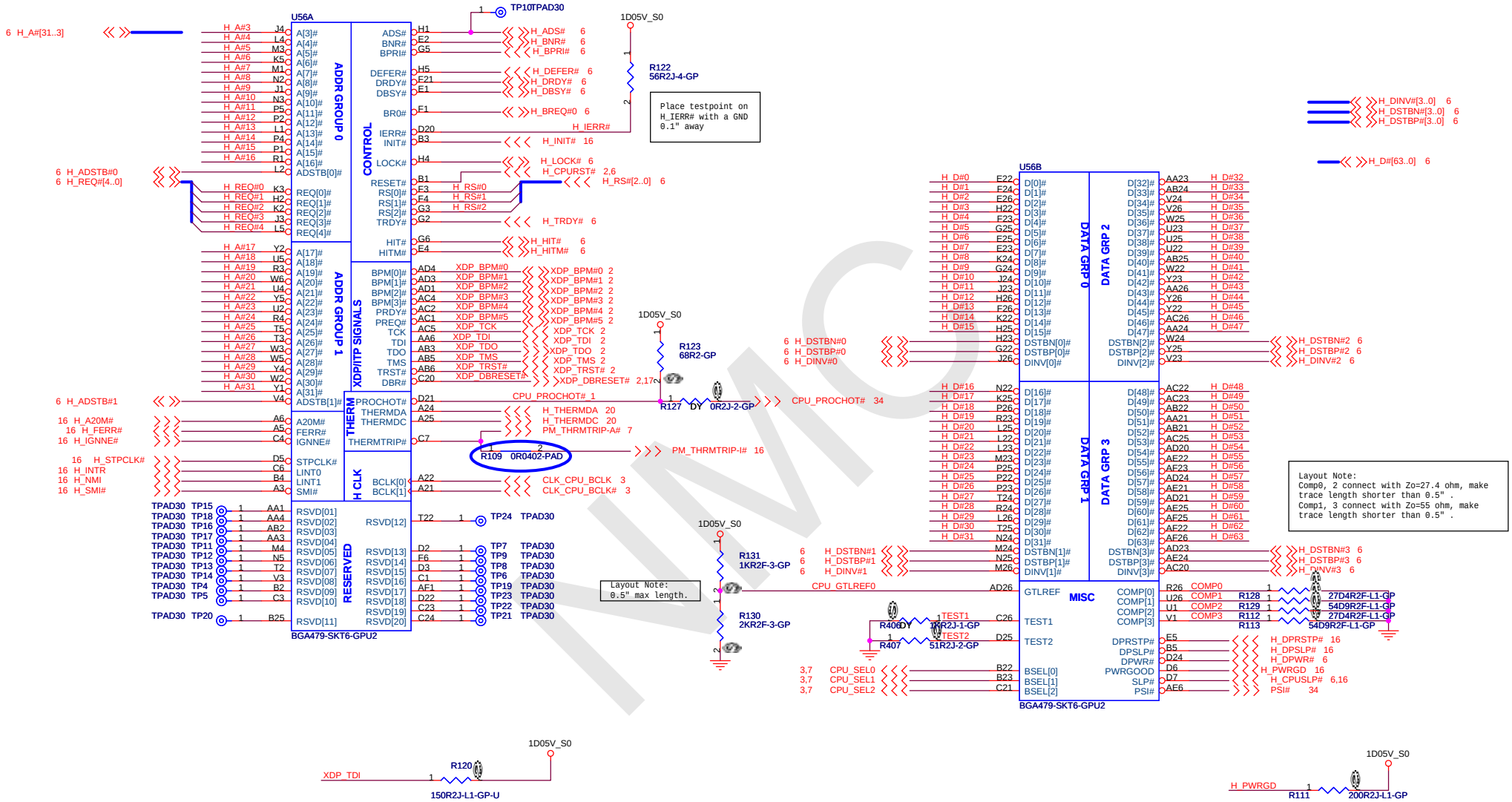
Title	ITP	
Size A3	Document Number KAI	Rev -1
Date: Thursday, April 13, 2006	Sheet 2 of 44	


3D3V_S0
R439 0R3-0-U-GP
3D3V_APWR_S0
C334 SC4D7U10V5ZY-3GP
C333 SCD1U16V2ZY-2GP
R171 0R3-0-U-GP
3D3V_48MPWR_S0
C331 SC4D7U10V5ZY-3GP
C332 SCD1U16V2ZY-2GP
R172 0R3-0-U-GP
3D3V_CLKGEN_S0
C351 SC10U10V5ZY-1GP
C555 SCD1U16V2ZY-2GP
C554 SCD1U16V2ZY-2GP
C310 SCD1U16V2ZY-2GP
C557 SCD1U16V2ZY-2GP
C312 SCD1U16V2ZY-2GP
C556 SCD1U16V2ZY-2GP
C553 SCD1U16V2ZY-2GP
R146 10KR2J-3-GP
R149 10KR2J-3-GP
H/L : CPU_ITP/SRC10
ITP_EN
SS_SEL
H/L: 27MHz/96MHz
R148 10KR2J-3-GP DY
R147 10KR2J-3-GP DY
IN (3D3V_S0) | EN (6218_PGOOD) | OUT (VTT_PWRGD#)
H | L | H
X | H | Hi - Z
CPU_SEL0
2K2R2J-2-GP R426
17 CLK48_ICH
R423 33R2J-2-GP FSA
U24
PCLK_FWH_1
PCLK_PCM_1
PCLK_KBC_1
SS_SEL
33R2J-2-GP
R435
R434
R432
PCLK_FWH 31
PCLK_PCM 22
PCLK_KBC 29
1016
FSA
CPU_SEL1
CPU_SEL2
R546 2K2R2J-2-GP
PM_STPCPU# 17
CLK_EN# 34
CLK_CPU_BCLK_1
CLK_CPU_BCLK_1#
RN25 SRN33J-5-GP-U
CLK_CPU_BCLK 4
CLK_CPU_BCLK# 4
CLK_MCH_BCLK_1
CLK_MCH_BCLK_1#
RN23 SRN33J-5-GP-U
CLK_MCH_BCLK 6
CLK_MCH_BCLK# 6
VDDSRC VDDSRC VDDSRC VDDSRC VDDPCI VDDPCI VDDA VDD48 VDDREF VDDCPU
PCICLK1 PCICLK2 PCICLK3 PCICLK4/FCTSEL1
USB_48MHZ/FSLA REF0/FSLC/TEST_SEL FSLB/TEST_MODE
CPU_STOP# VTT_PWRGD#/PD
R169 10KR2J-3-GP
26 CONN_CLKREQ#
R168 0R2J-2-GP
CLKREQ2#
R430 R170 R153 R431 R152 R433 R150 R437 R190
1KR2J-1-GP
CLKREQ1# CLKREQ2# CLKREQ3# CLKREQ4# CLKREQ5# CLKREQ6# CLKREQ7# CLKREQ8# CLKREQ9#
PEG_REFCLKP_1
PEG_REFCLKN_1
RN22 SRN33J-5-GP-U
PEG_REFCLKP 38
PEG_REFCLKN 38
CLK_PCIE_NEW_1
CLK_PCIE_NEW_1#
RN27 SRN33J-5-GP-U
CLK_PCIE_NEW 26
CLK_PCIE_NEW# 26
CLK_MCH_3GPLL_1
CLK_MCH_3GPLL_1#
RN28 SRN33J-5-GP-U
CLK_MCH_3GPLL 7
CLK_MCH_3GPLL# 7
CLK_PCIE_SATA_1
CLK_PCIE_SATA_1#
RN29 SRN33J-5-GP-U
CLK_PCIE_SATA 16
CLK_PCIE_SATA# 16
CLK_PCIE_ICH_1
CLK_PCIE_ICH_1#
RN30 SRN33J-5-GP-U
CLK_PCIE_ICH 17
CLK_PCIE_ICH# 17
SRCT1 SRCT2 SRCT3 SRCT4 SRCT5 SRCT6 SRCT7 SRCT8 SRCT9
PEG_REFCLKP_1
CLK_PCIE_NEW_1
CLK_MCH_3GPLL_1
CLK_PCIE_SATA_1
CLK_PCIE_ICH_1
CLK_PCIE_MINI1_1
CLK_PCIE_MINI2_1
SRCC1 SRCC2 SRCC3 SRCC4 SRCC5 SRCC6 SRCC7 SRCC8 SRCC9
PEG_REFCLKN_1
CLK_PCIE_NEW_1#
CLK_MCH_3GPLL_1#
CLK_PCIE_SATA_1#
CLK_PCIE_ICH_1#
CLK_PCIE_MINI1_1#
CLK_PCIE_MINI2_1#
CLK_PCIE_MINI1_1
CLK_PCIE_MINI1_1#
RN32 SRN33J-5-GP-U
CLK_PCIE_MINI1 24
CLK_PCIE_MINI1# 24
CLK_PCIE_MINI2_1
CLK_PCIE_MINI2_1#
RN33 SRN33J-5-GP-U
CLK_PCIE_MINI2 24
CLK_PCIE_MINI2# 24
LCD100/96/SRC0_T
LCD100/96/SRCO_C
40 VGA_27MHZ
40 VGA_27MHZSS
33R2J-2-GP R428
33R2J-2-GP R429
VGA_27MHZ_1
VGA_27MHZSS_1
DOTT_96MHZ/27MHZ_NONSPREAD
DOTC_96MHZ/27MHZ_SPREAD
C311 SC27P50V2JN-2GP
X1 X-14D31818M-30GP
C313 SC39P50V2JN-1GP
GEN_XTAL_OUT_R1
R156 0R2J-2-GP
GEN_XTAL_IN
GEN_XTAL_OUT
X1
X2
11,19 SMBC_ICH
11,19 SMBD_ICH
SMBCLK
SMBDAT
PCI_SRC_STOP#
ITP_EN/PCICLK_F0
ITP_EN
33R2J-2-GP R151
PM_STPPCI# 17
CLK_ICHPCI 17
CPUCLKT1 CPUCLKT0 CPUCLKC1 CPUCLKC0
CPUT_ITP/SRCT10 CPUC_ITP/SRCC10
IREF REF1
GND GNDA GND48 GNDCPU GNDREF GNDPCI GNDPCI GNDSRC GNDSRC
ICS954305EKLF-GP
CLK_MCH_BCLK_1
CLK_CPU_BCLK_1
CLK_MCH_BCLK_1#
CLK_CPU_BCLK_1#
GEN_REF
33R2J-2-GP R436
CLK_ICH14 17
GEN_IREF
475R2F-L1-GP R438
CLK_XDP_1
CLK_XDP_1#
RN24 SRN33J-5-GP-U DY
CLK_XDP_2
CLK_XDP# 2
1D05V_S0
R425 1KR2J-1-GP DY
R422 DUMMY-R2
R154 DUMMY-R2
CPU_SEL0 4,7
CPU_SEL1 4,7
CPU_SEL2 4,7
R427 DUMMY-R2
R424 1KR2J-1-GP DY
R155 1KR2J-1-GP DY
FS_C FS_B FS_A | CPU
0 0 0 | 266M
0 0 1 | 133M
0 1 0 | 200M
0 1 1 | 166M
1 0 0 | 333M
1 0 1 | 100M
1 1 0 | 400M
1 1 1 | Reserved
1022
PEG_REFCLKP
PEG_REFCLKN
RN65 SRN49D9F-GP
CLK_PCIE_NEW
CLK_PCIE_NEW#
RN46 SRN49D9F-GP
CLK_PCIE_MINI1
CLK_PCIE_MINI1#
RN54 SRN49D9F-GP
CLK_PCIE_SATA
CLK_PCIE_SATA#
RN51 SRN49D9F-GP
CLK_PCIE_ICH
CLK_PCIE_ICH#
RN52 SRN49D9F-GP
CLK_PCIE_MINI2
CLK_PCIE_MINI2#
RN55 SRN49D9F-GP
CLK_CPU_BCLK
CLK_CPU_BCLK#
RN26 SRN49D9F-GP
CLK_MCH_BCLK
CLK_MCH_BCLK#
RN47 SRN49D9F-GP
CLK_MCH_3GPLL
CLK_MCH_3GPLL#
RN50 SRN49D9F-GP
CLK_XDP
CLK_XDP#
RN48 SRN49D9F-GP DY
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Clock Generator
Size A3
Document Number KAI
Rev -1
Date: Thursday, April 13, 2006
Sheet 3 of 44



<Core Design>

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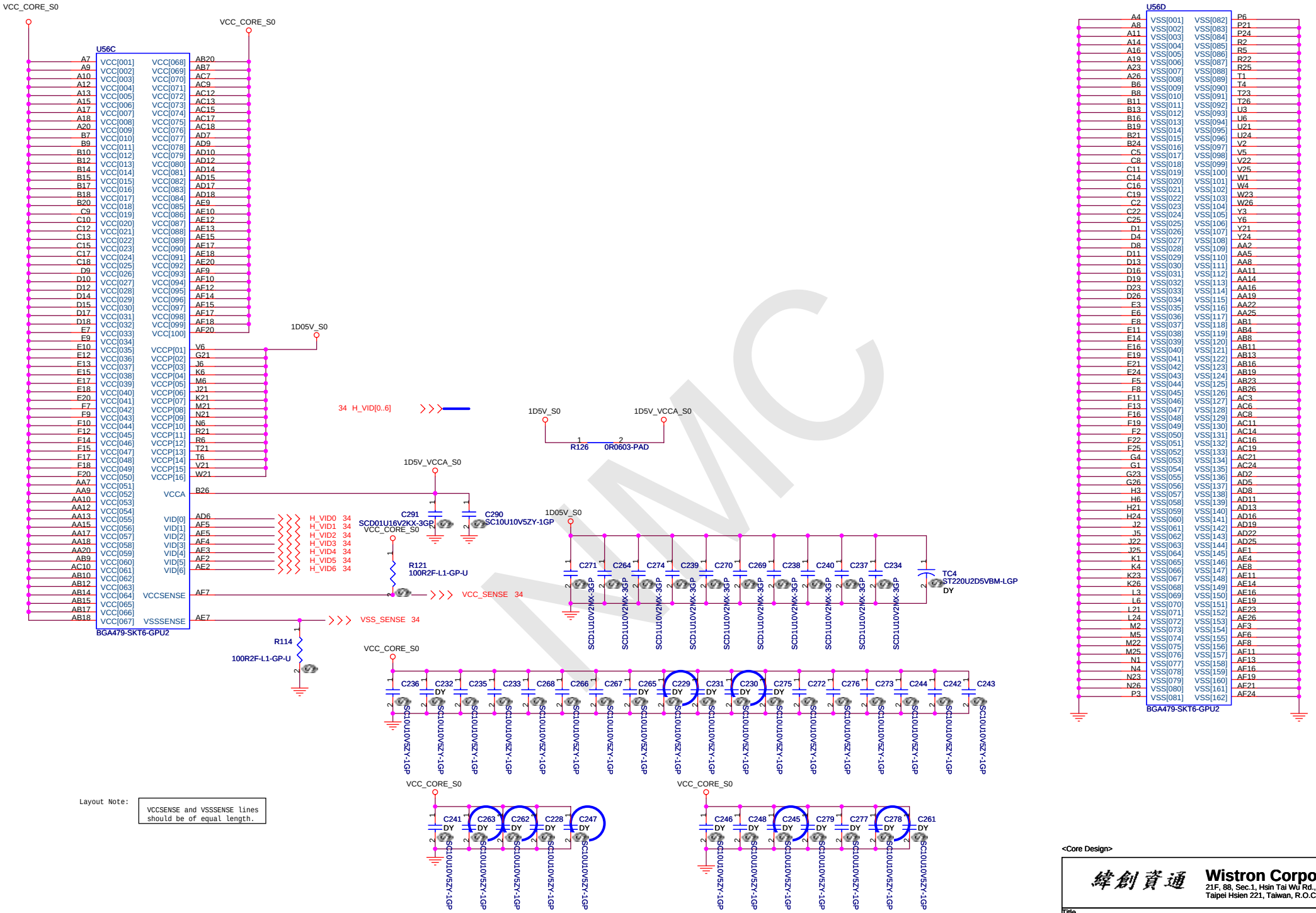
Title: CPU (1 of 2)

Size	Document Number	Rev
A3	KAI	-1

Date: Thursday, April 13, 2006 Sheet 4 of 44


VCC_CORE_S0
U56C
BGA479-SKT6-GPU2
1D05V_S0
34 H_VID[0..6]
1D05V_VCCA_S0
R126 0R0603-PAD
C291 SCD01U16V2KX-3GP
C290 SC10U10V5ZY-1GP
R121 100R2F-L1-GP-U
VCC_SENSE 34
VSS_SENSE 34
R114 100R2F-L1-GP-U
TC4 ST220U2D5VBM-LGP DY
SCD1U10V2MX-3GP
SC10U10V5ZY-1GP
SC10U10V6ZY-1GP
U56D
BGA479-SKT6-GPU2
Layout Note:
VCCSENSE and VSSSENSE lines should be of equal length.
<Core Design>
Wistron Corporation
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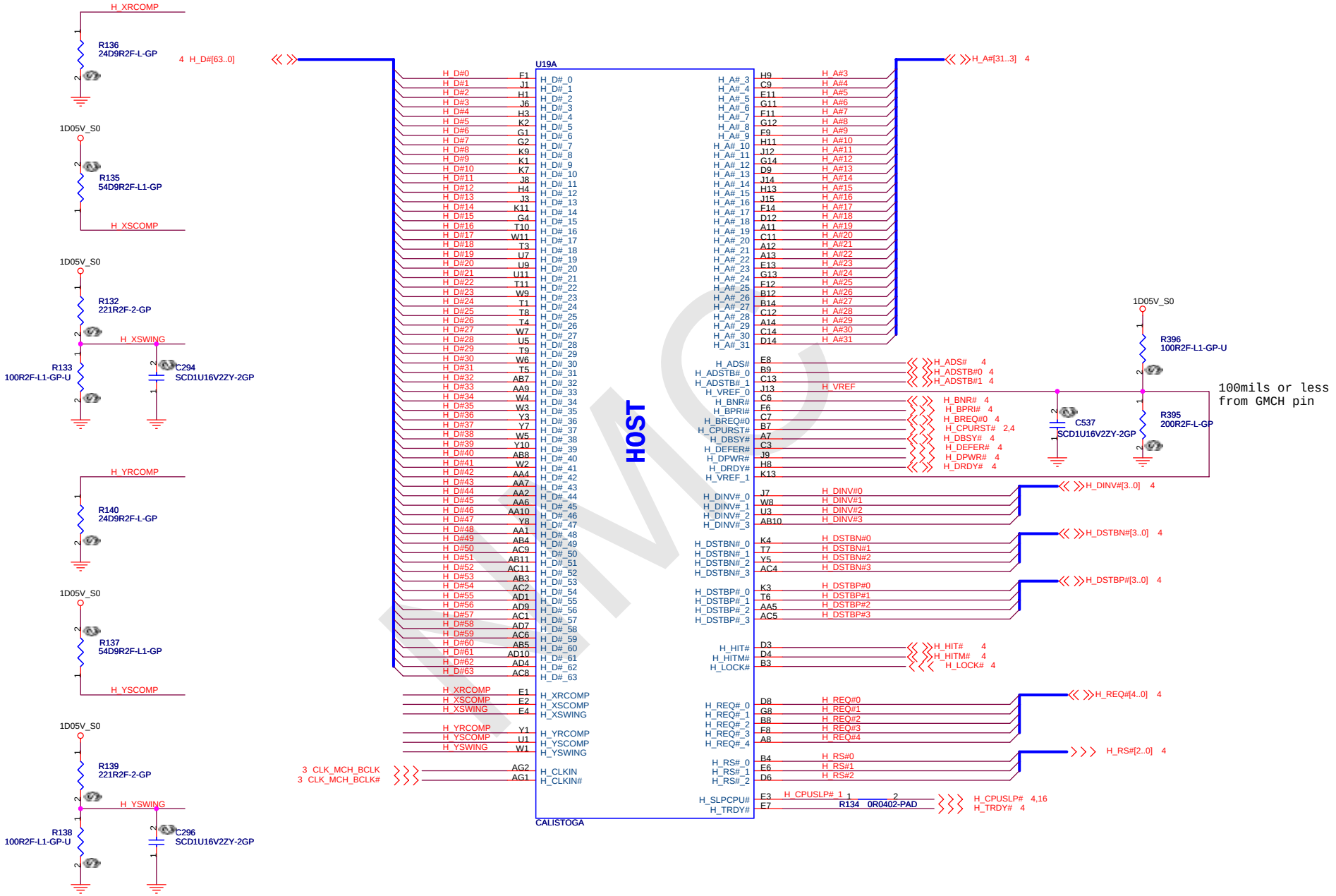
Title
CPU (2 of 2)
Size A3
Document Number KAI
Rev -1
Date: Thursday, April 13, 2006
Sheet 5 of 44



Place them near to the chip

<Core Design>

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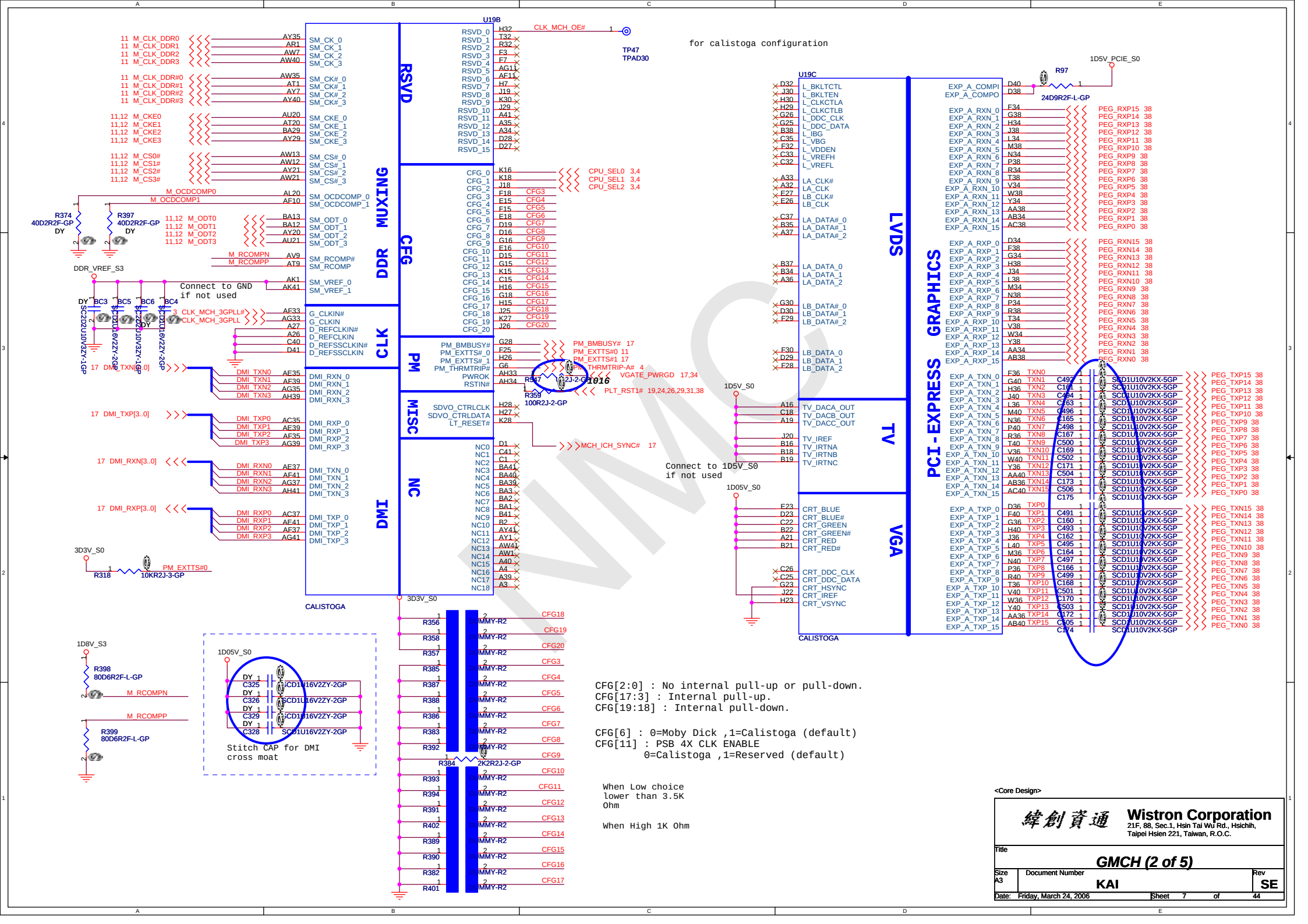
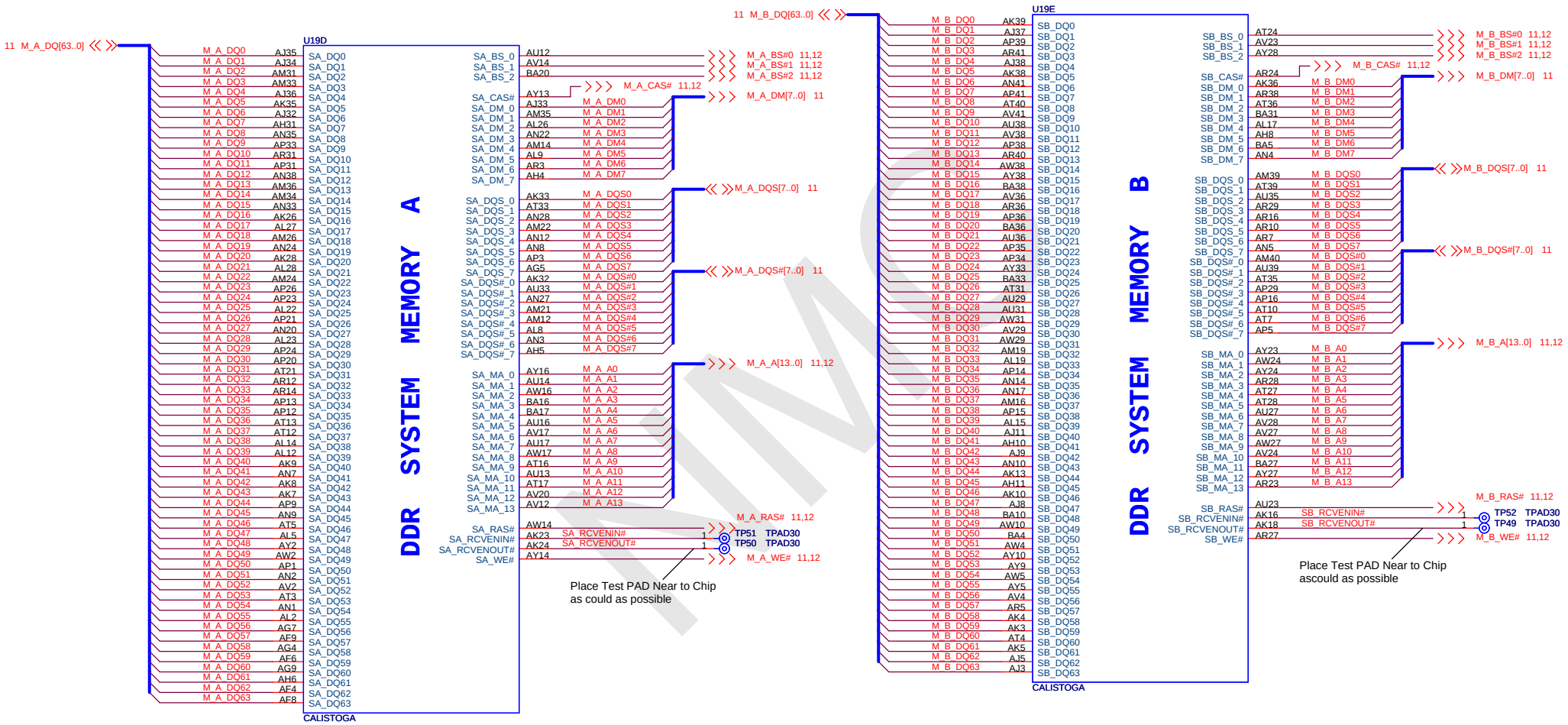
Title: GMCH (1 of 5)

Size: A3 | Document Number: KAI | Rev: -1

Date: Thursday, April 13, 2006 | Sheet 6 of 44


U19B
RSVD
CFG
PM
MISC
NC
DMI
DDR MUXING
CLK
CALISTOGA
for calistoga configuration
U19C
LVDS
TV
VGA
PCI-EXPRESS GRAPHICS
CALISTOGA
CLK_MCH_OE#
TP47
TPAD30
R97
24D9R2F-L-GP
1D5V_PCIE_S0
M_OCDCOMP0
M_OCDCOMP1
R374
40D2R2F-GP
R397
40D2R2F-GP
DDR_VREF_S3
Connect to GND
if not used
CLK_MCH_3GPLL#
CLK_MCH_3GPLL
PM_BMBUSY#
PM_EXTTS#0
PM_EXTTS#1
PM_THRMTRIP#
PWROK
RSTIN#
R347
2K2R2J-2-GP
R359
100R2J-2-GP
VGATE_PWRGD
PLT_RST1#
MCH_ICH_SYNC#
SDVO_CTRLCLK
SDVO_CTRLDATA
LT_RESET#
R318
10KR2J-3-GP
3D3V_S0
1D8V_S3
R398
80D6R2F-L-GP
R399
80D6R2F-L-GP
M_RCOMPN
M_RCOMPP
1D05V_S0
Stitch CAP for DMI
cross moat
R384
2K2R2J-2-GP
DUMMY-R2
Connect to 1D5V_S0
if not used
CFG[2:0] : No internal pull-up or pull-down.
CFG[17:3] : Internal pull-up.
CFG[19:18] : Internal pull-down.
CFG[6] : 0=Moby Dick ,1=Calistoga (default)
CFG[11] : PSB 4X CLK ENABLE
0=Calistoga ,1=Reserved (default)
When Low choice
lower than 3.5K
Ohm
When High 1K Ohm
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
GMCH (2 of 5)
Size A3
Document Number
KAI
Rev
SE
Date: Friday, March 24, 2006
Sheet 7 of 44



<Core Design>

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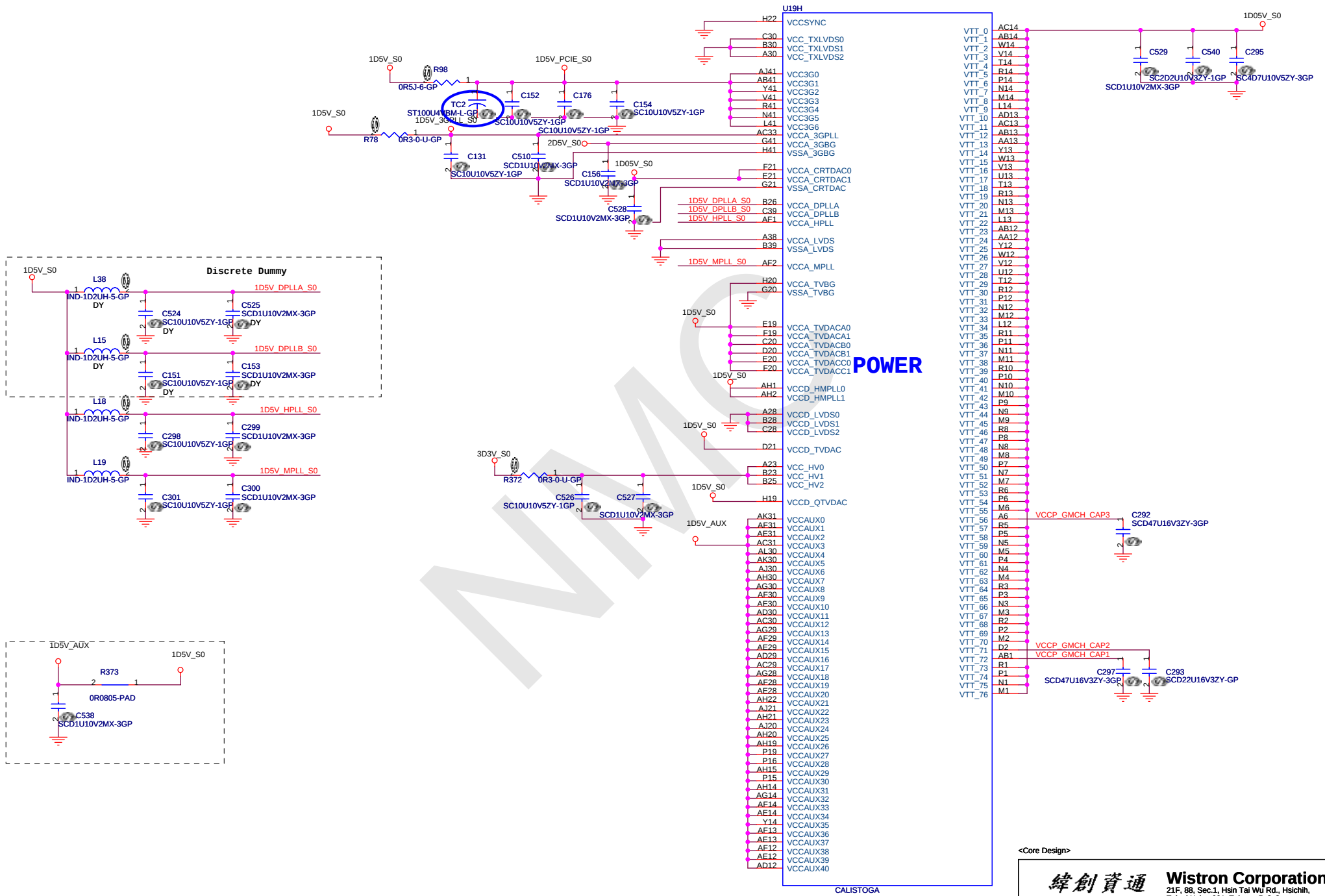
Title: GMCH (3 of 5)

Size	Document Number	Rev
A3	KAI	SE

Date: Friday, March 24, 2006 Sheet 8 of 44



<Core Design>

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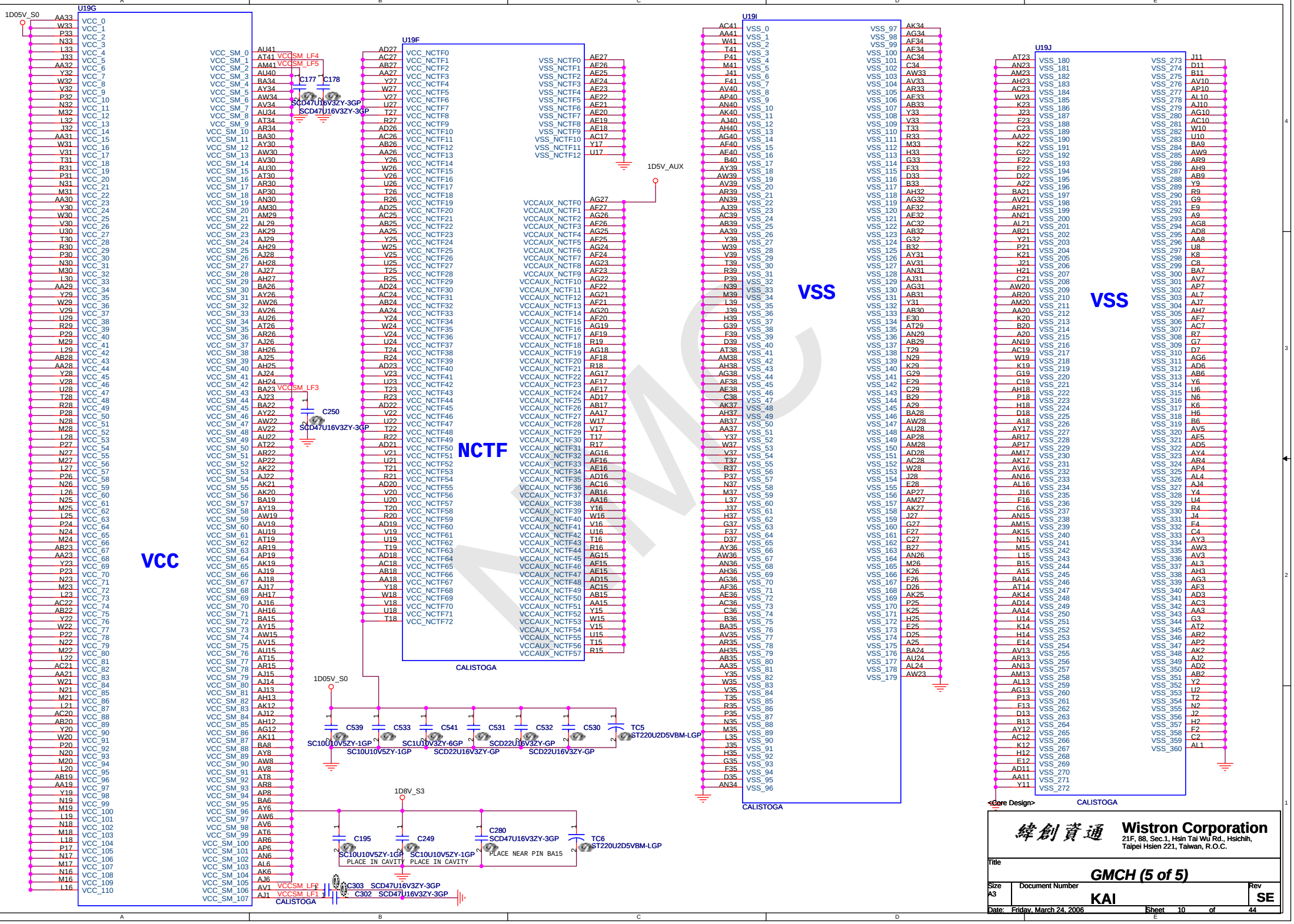
Title: GMCH (4 of 5)

Size: A3 | Document Number: KAI | Rev: SE

Date: Friday, March 24, 2006 | Sheet 9 of 44



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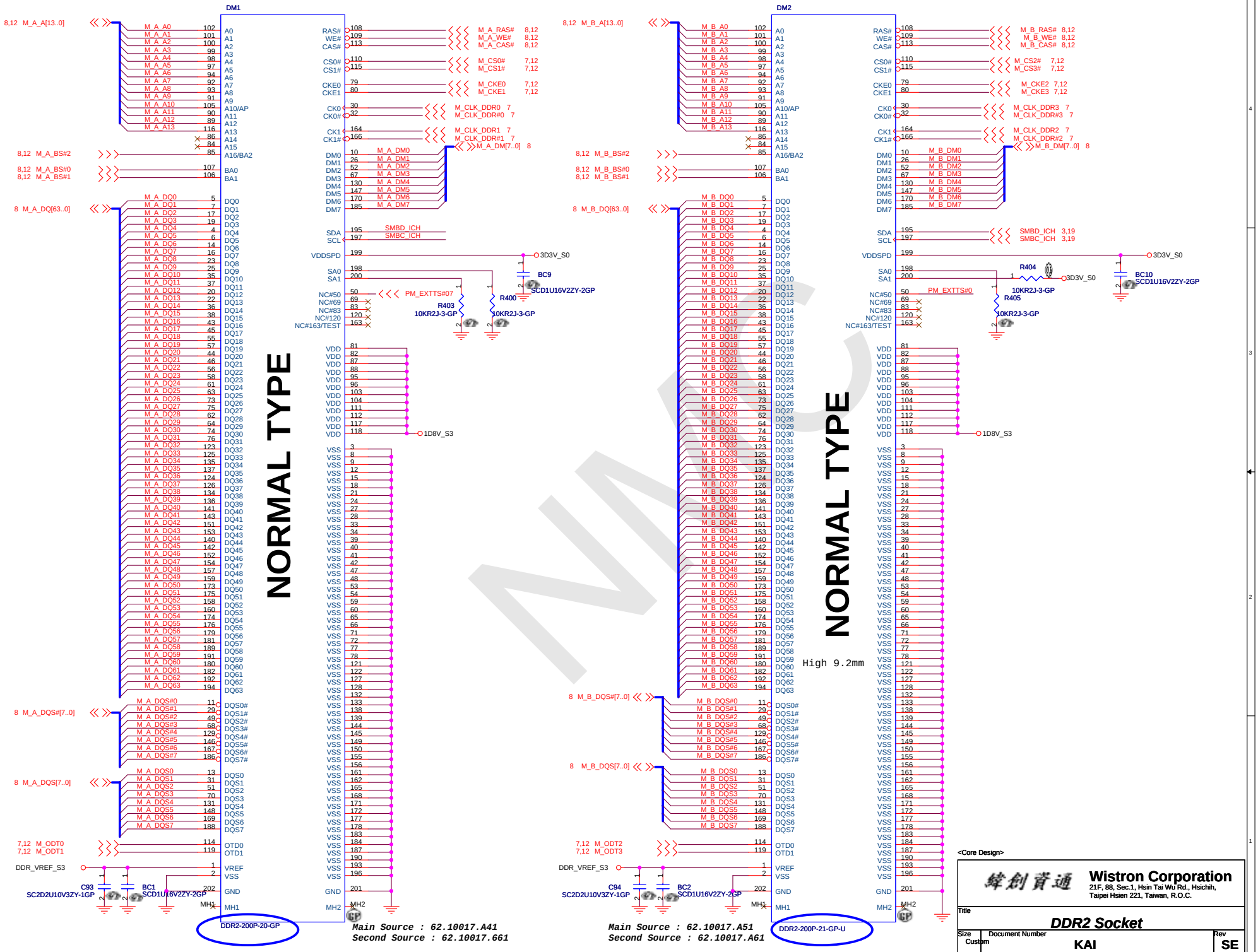
Title: GMCH (5 of 5)

Size	Document Number	Rev
A3	KAI	SE

Date: Friday, March 24, 2006 Sheet 10 of 44



<Core Design>

Wistron Corporation
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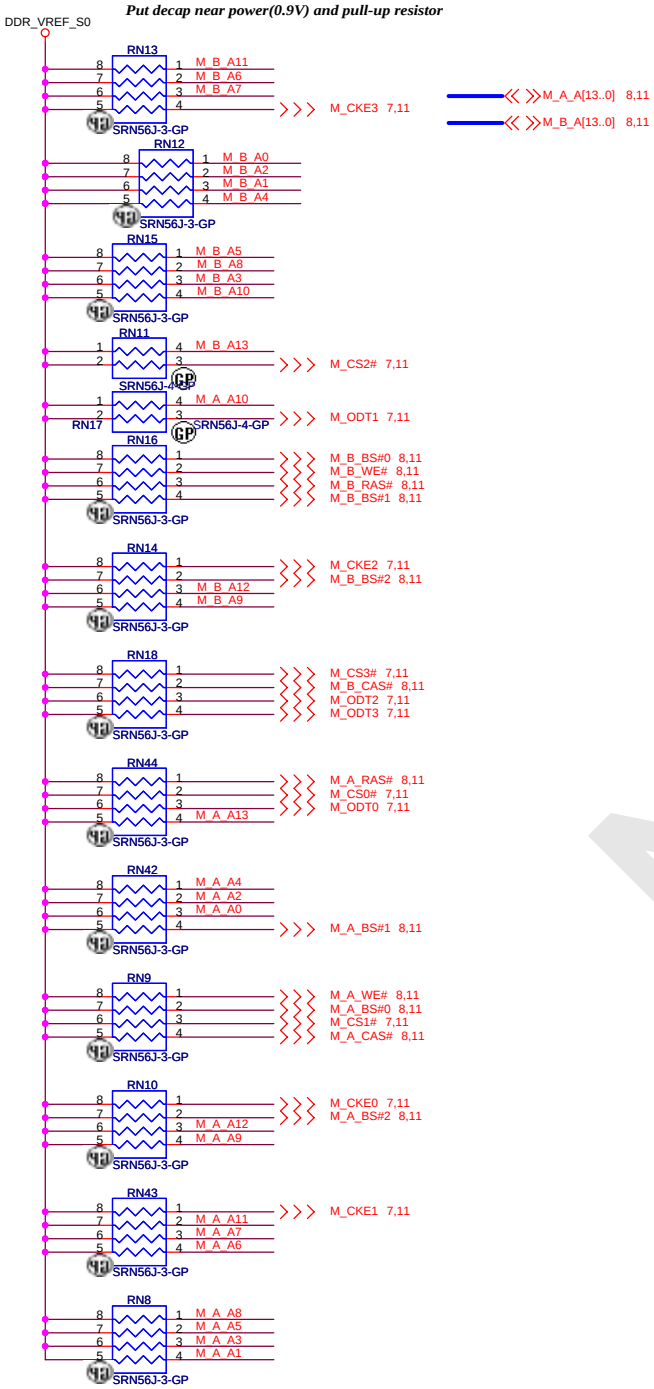
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR2 Socket

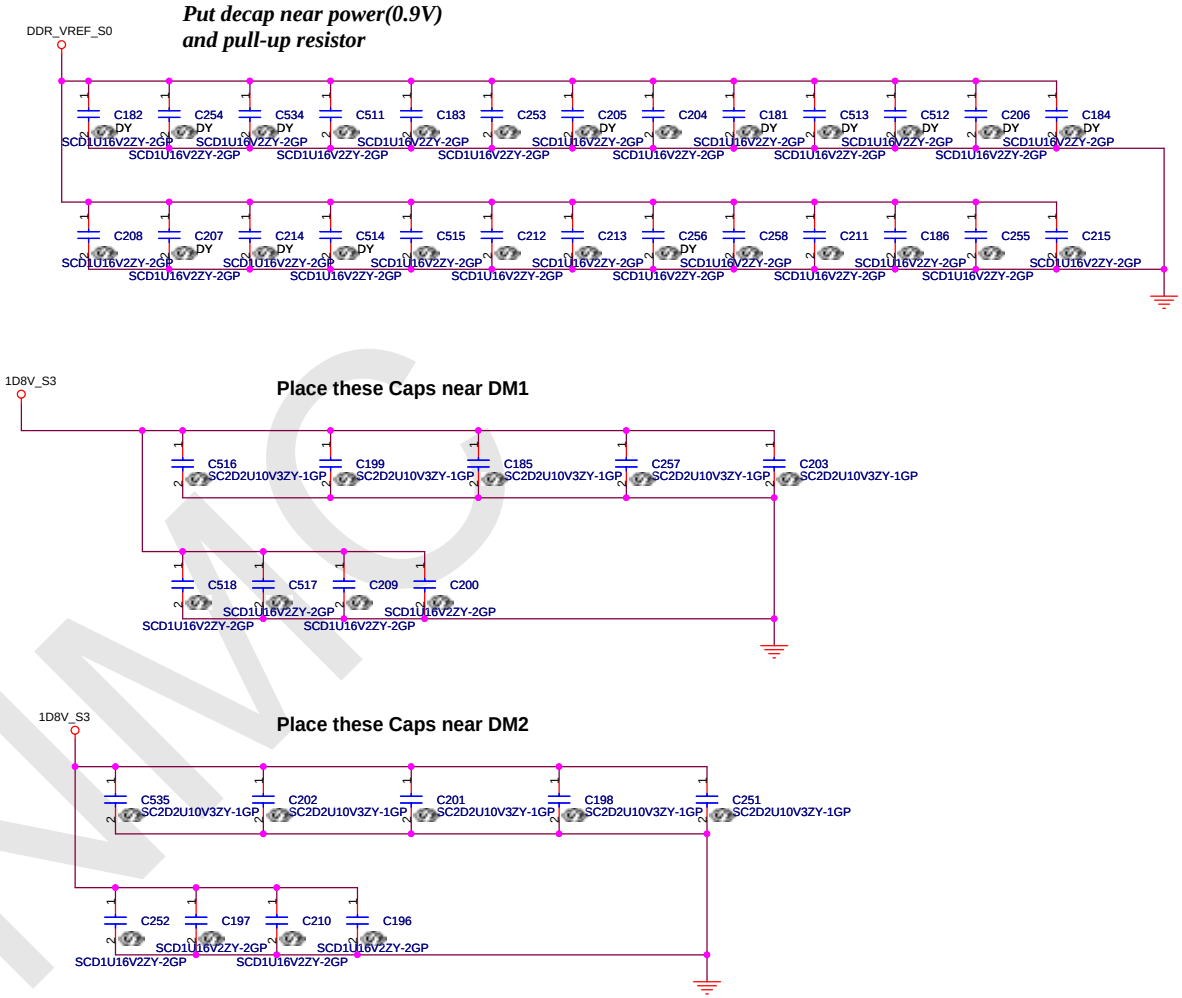
Size: Custom | Document Number: KAI | Rev: SE

Date: Thursday, April 13, 2006 | Sheet 11 of 44

PARALLEL TERMINATION



Decoupling Capacitor



<Core Design>

緯創資通 **Wistron Corporation**
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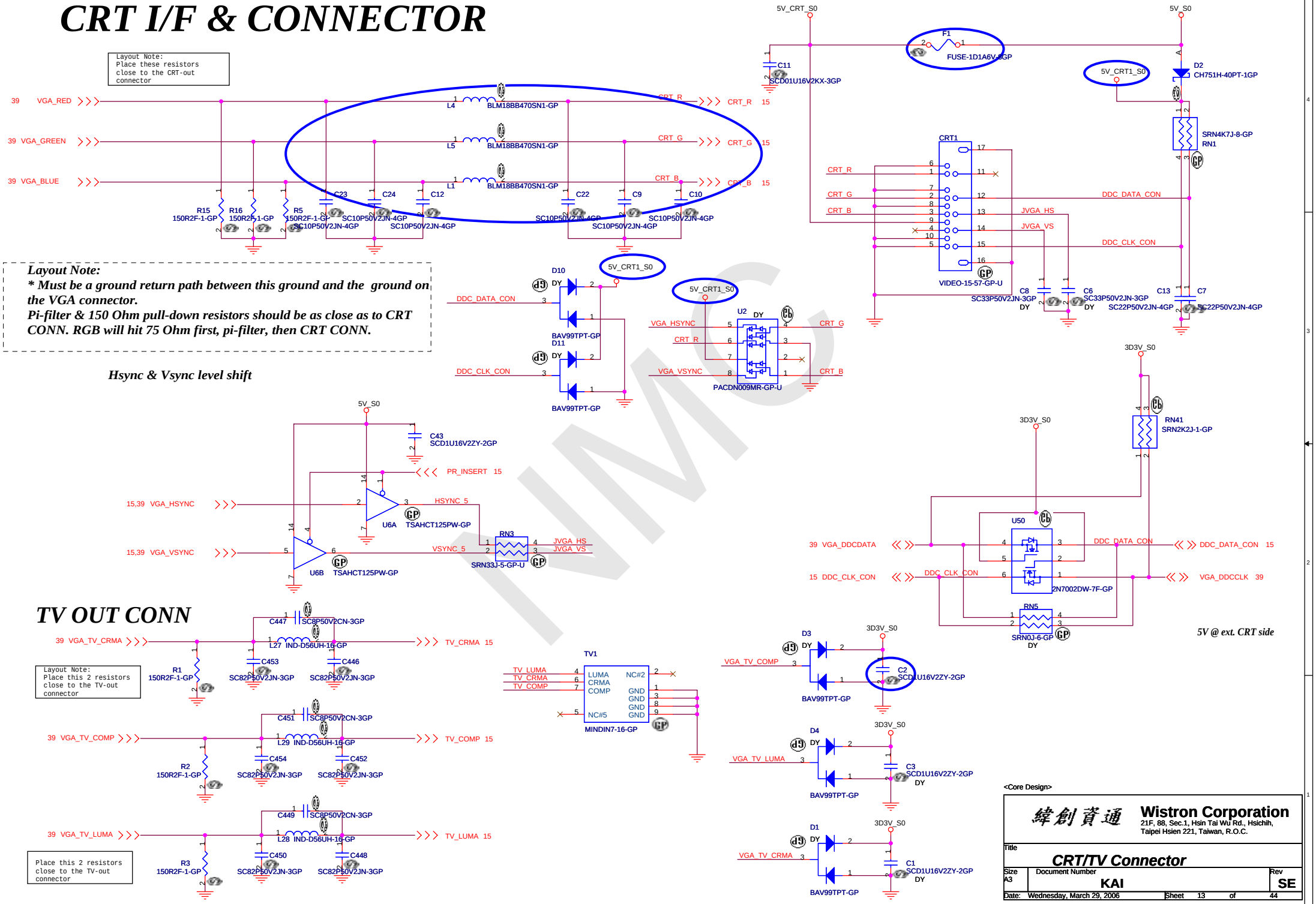
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR2 Termination Resistor***

Size	Document Number	Rev
A3	KAI	SE

Date: Friday, March 24, 2006 Sheet 12 of 44

CRT I/F & CONNECTOR



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

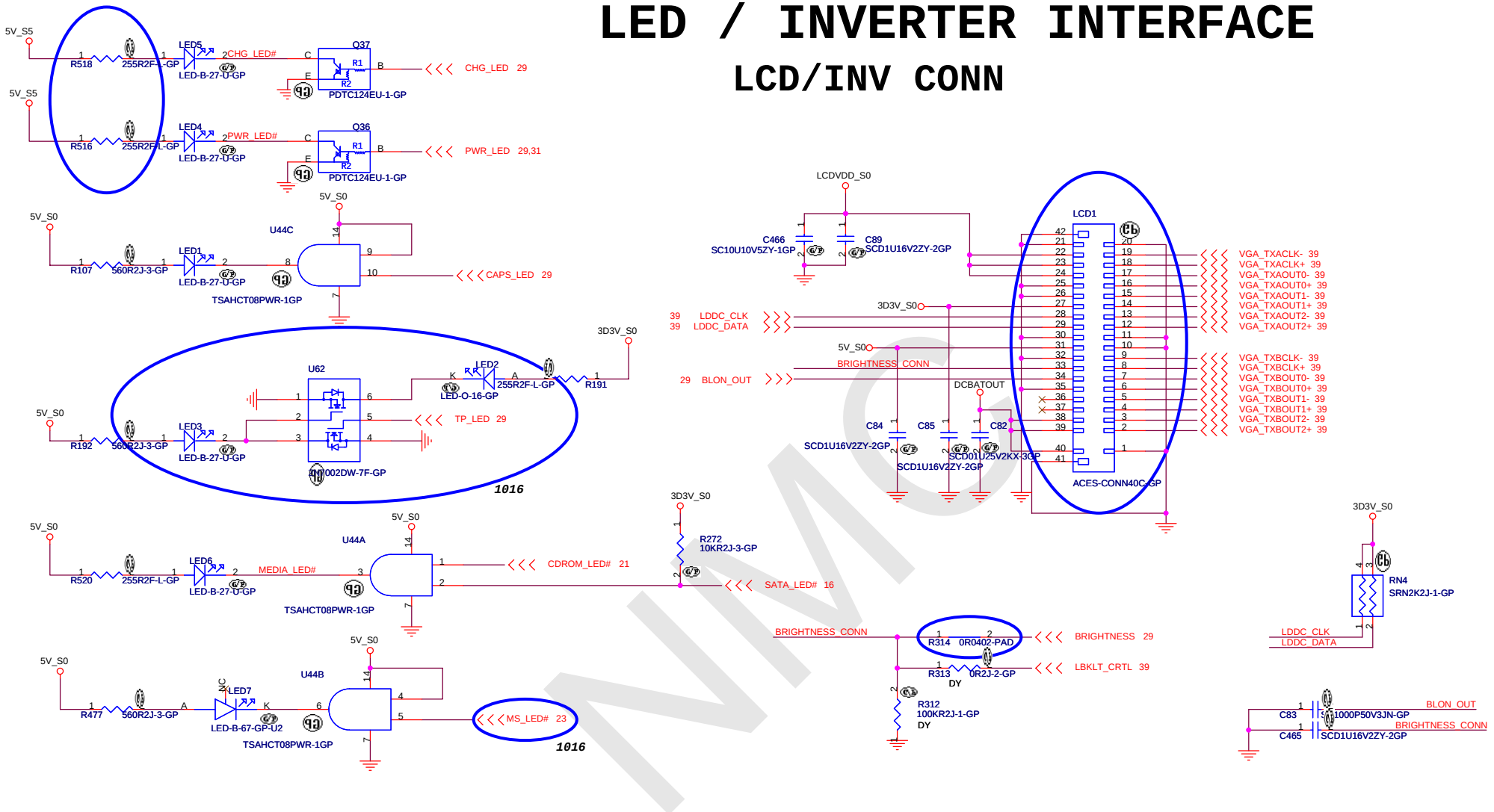
Title: CRT/TV Connector

Size	Document Number	Rev
A3	KAI	SE

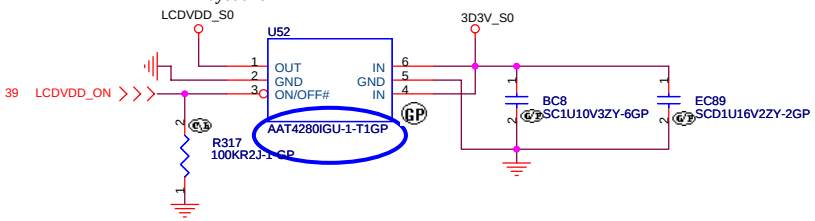
Date: Wednesday, March 29, 2006 Sheet 13 of 44

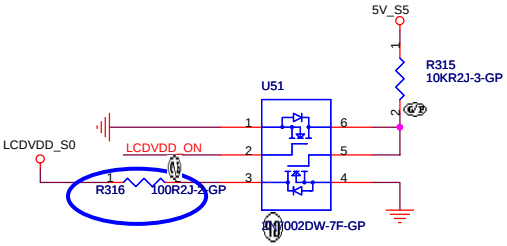
LED / INVERTER INTERFACE

LCD/INV CONN



Layout 40 mil





Discharge circuit

<Core Design>

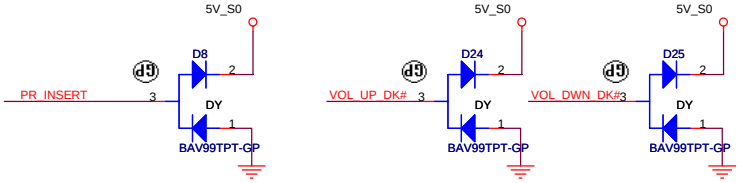
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LCD/Inverter Connector**

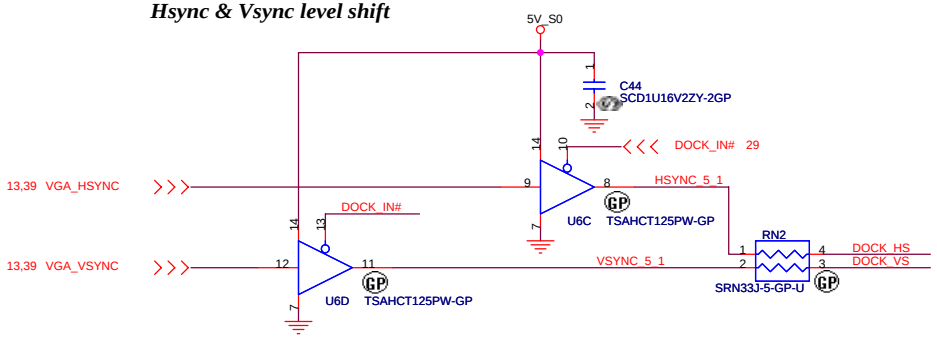
Size	Document Number	Rev
Custom	KAI	SE

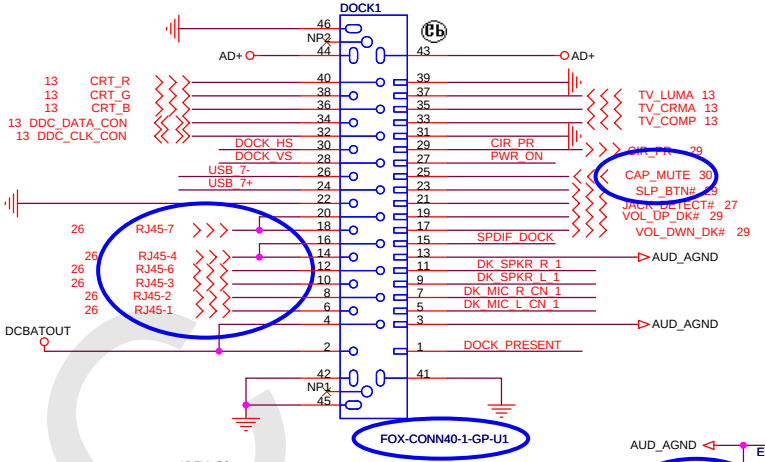
Date: Thursday, April 13, 2006 Sheet 14 of 44

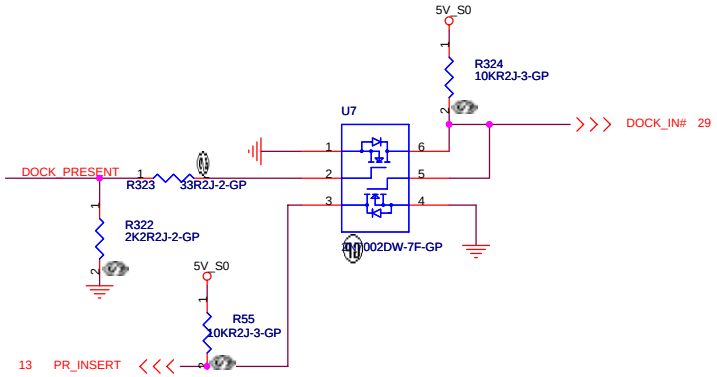
Docking Connector

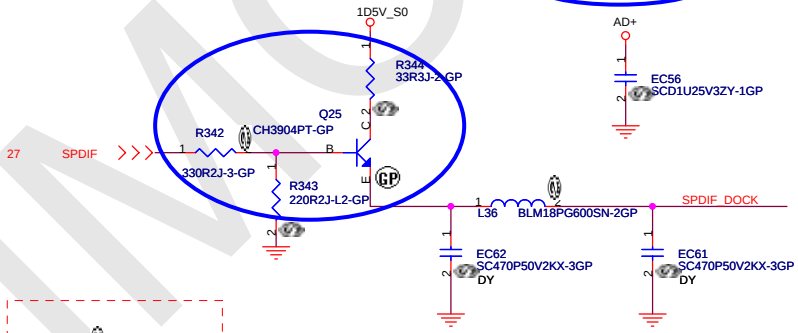


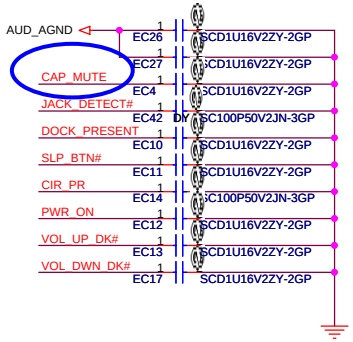
Hsync & Vsync level shift

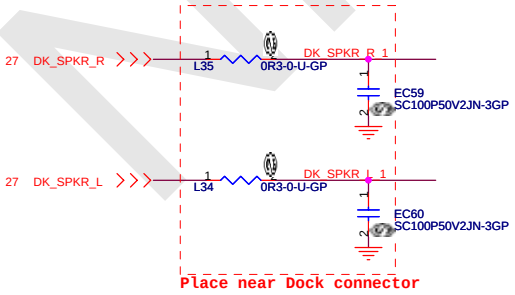


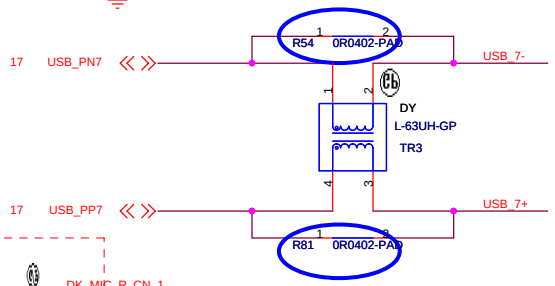


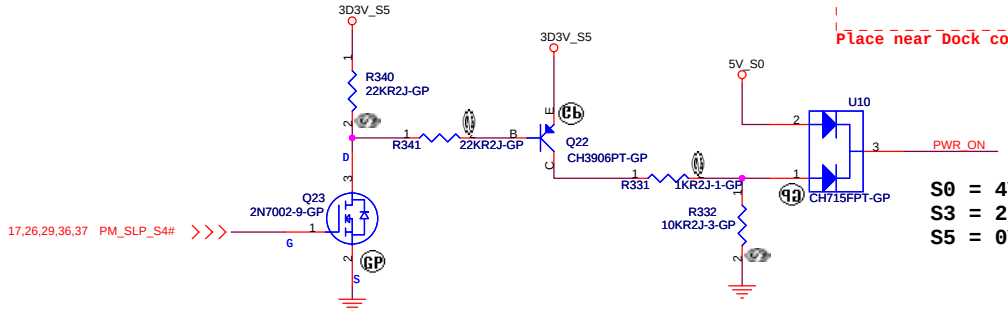


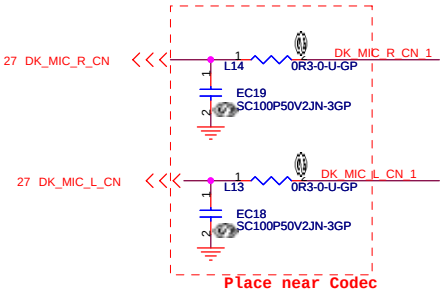












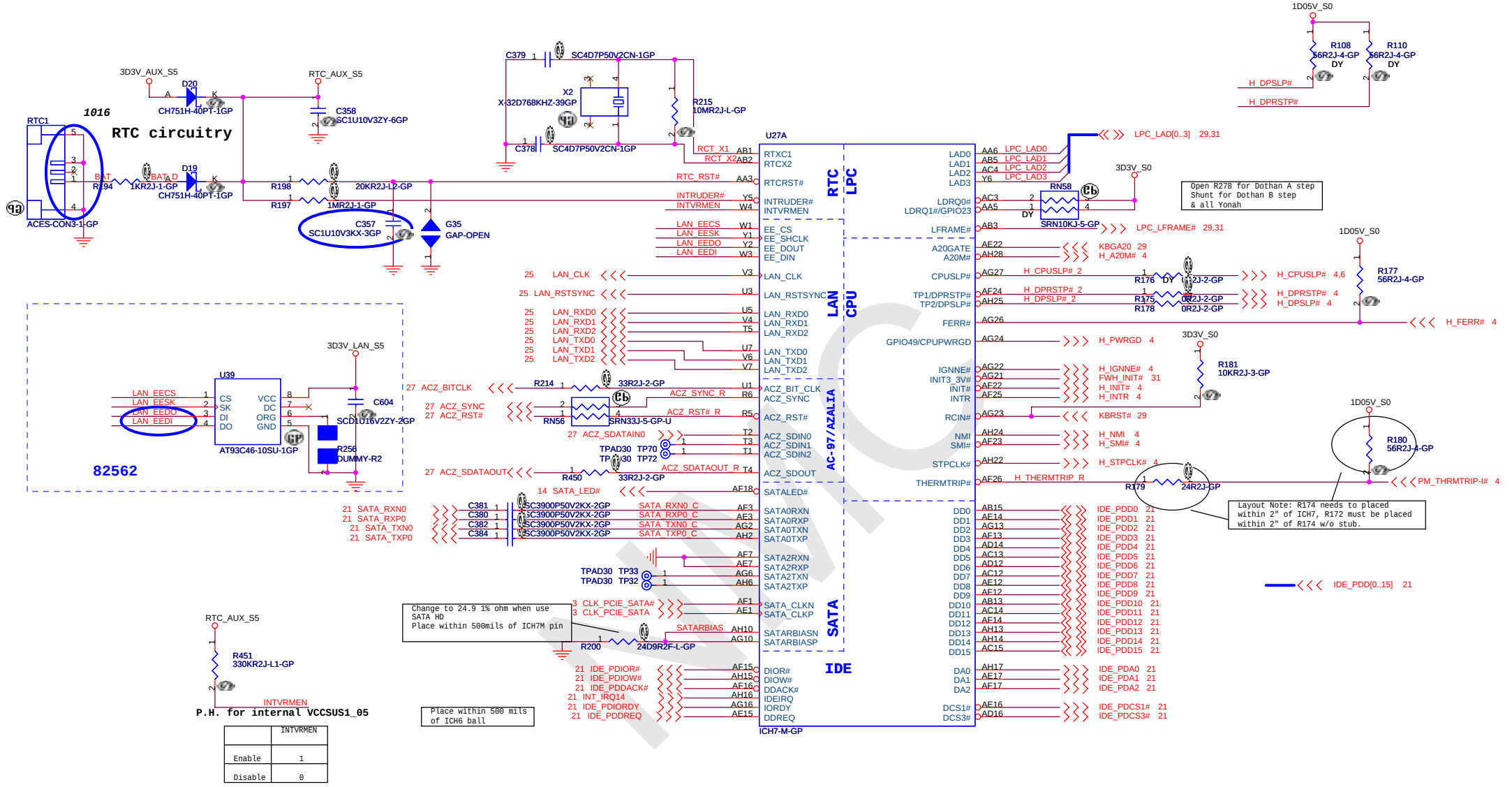
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Board to board conn/ Docking**

Size	Document Number	Rev
A3	KAI	SE

Date: Sunday, May 28, 2006 Sheet 15 of 44



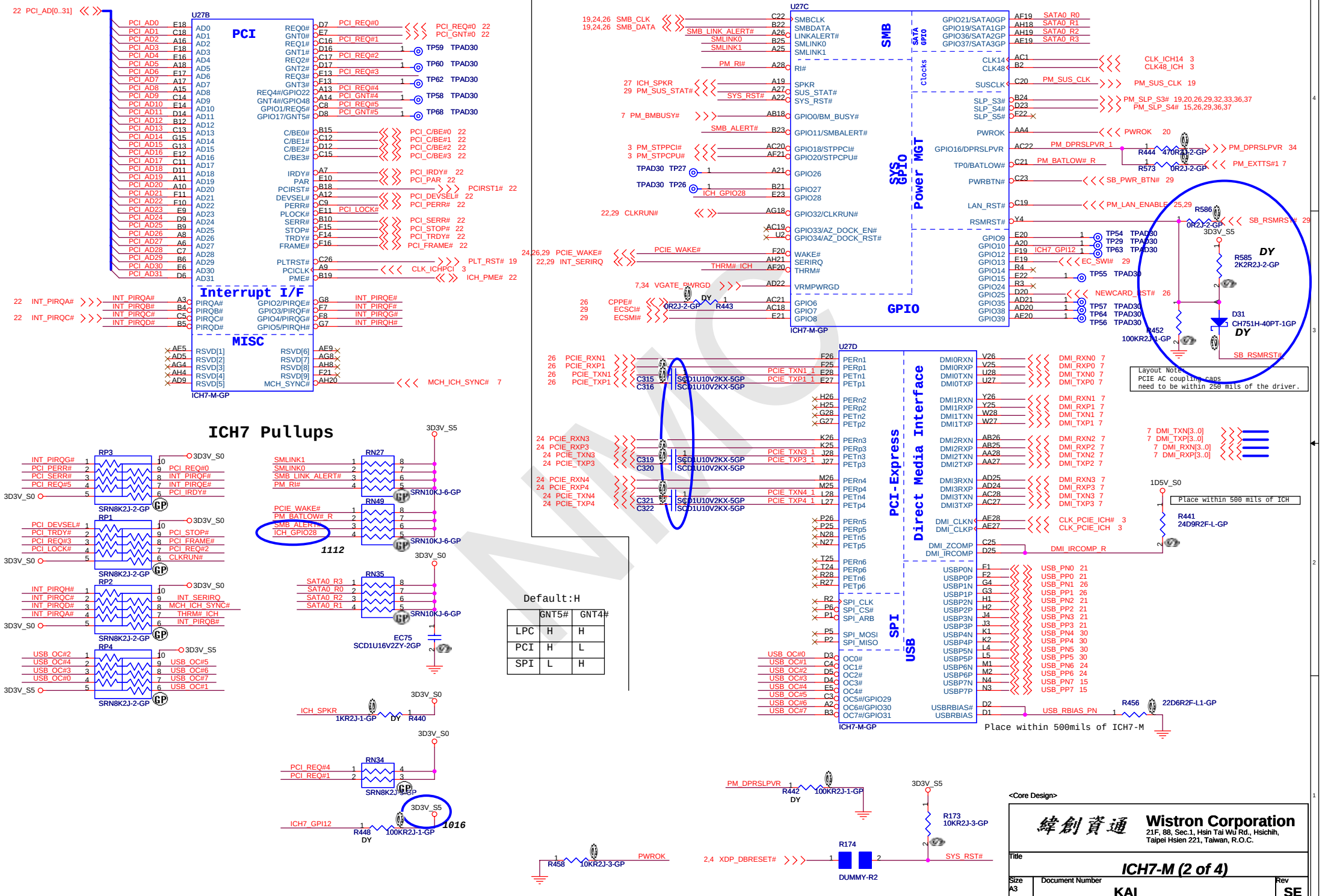
<Core Design>

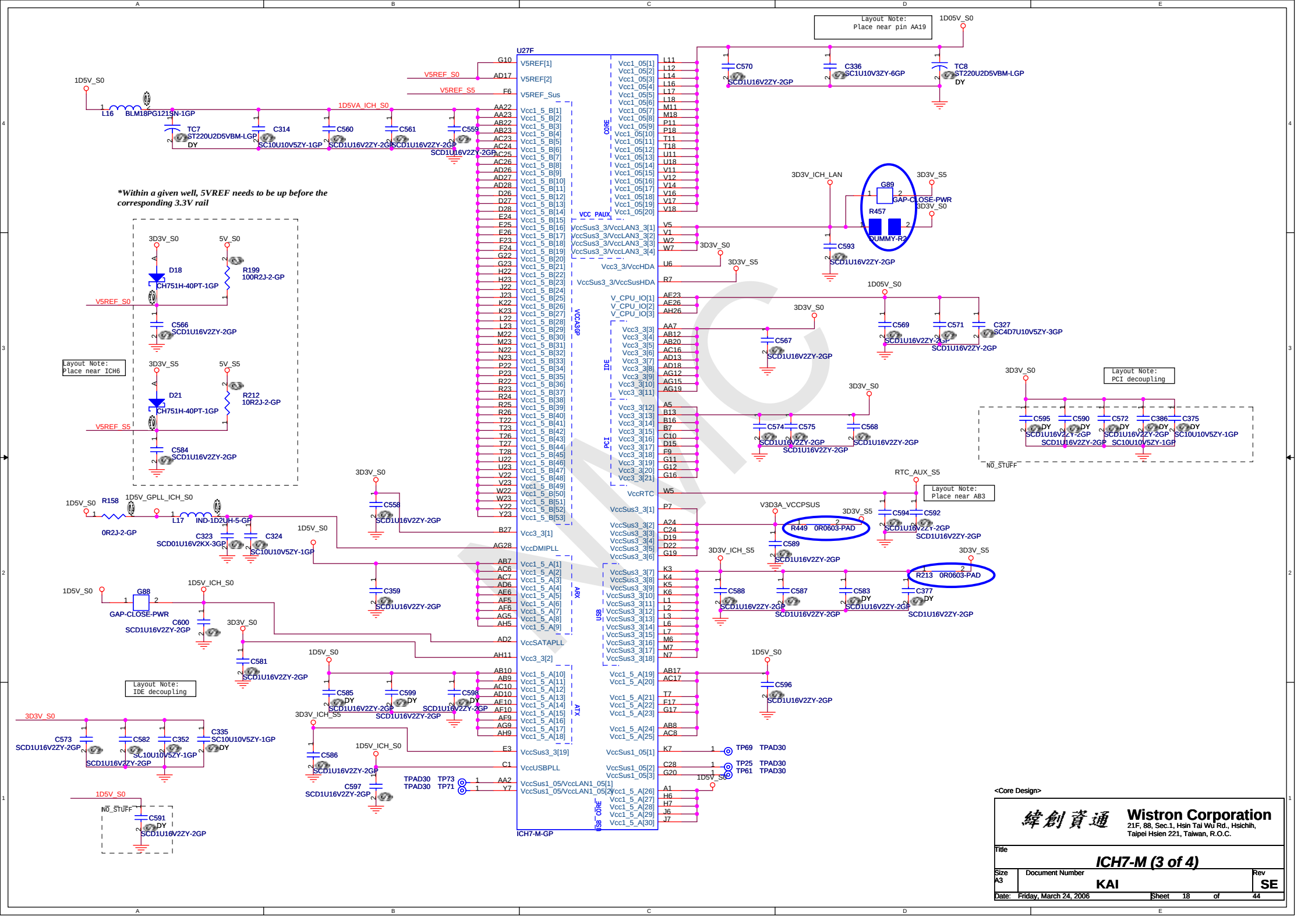
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH7-M (1 of 4)

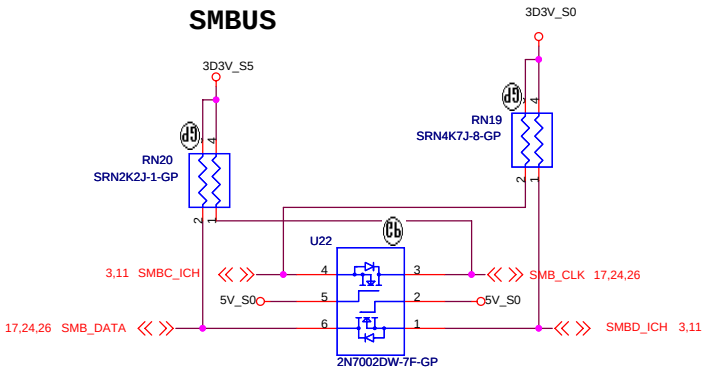
Size: A3 | Document Number: KAI | Rev: SE

Date: Tuesday, April 25, 2006 | Sheet 16 of 44

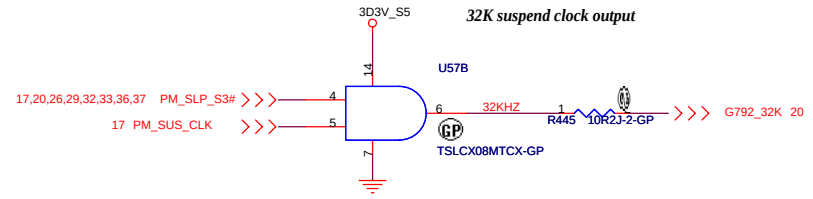

U27B
PCI
Interrupt I/F
MISC
ICH7-M-GP
U27C
SMB
SYS GPIO
Power MGT
GPIO
Clocks
SATA GPIO
ICH7-M-GP
U27D
PCI-Express
Direct Media Interface
SPI
USB
ICH7-M-GP
ICH7 Pullups
Default:H
GNT5# GNT4#
LPC H H
PCI H L
SPI L H
Layout Note:
PCIE AC coupling caps
need to be within 250 mils of the driver.
Place within 500 mils of ICH
Place within 500mils of ICH7-M
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH7-M (2 of 4)
Size A3
Document Number KAI
Rev SE
Date: Thursday, April 13, 2006
Sheet 17 of 44

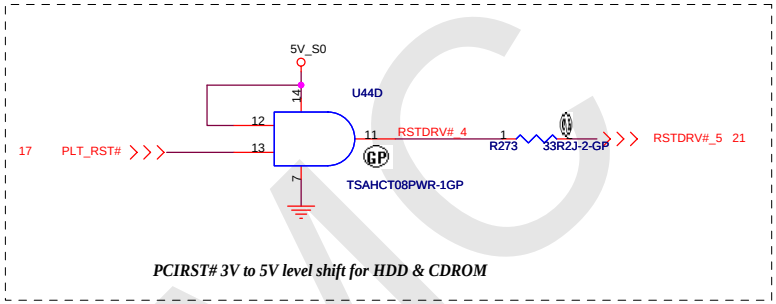

U27F
ICH7-M-GP
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Layout Note: Place near pin AA19
Layout Note: Place near ICH6
Layout Note: IDE decoupling
Layout Note: PCI decoupling
Layout Note: Place near AB3
NO_STUFF
GAP-CLOSE-PWR
DUMMY-R3
0R2J-2-GP
0R0603-PAD
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH7-M (3 of 4)
Size A3
Document Number
KAI
Rev
SE
Date: Friday, March 24, 2006
Sheet 18 of 44

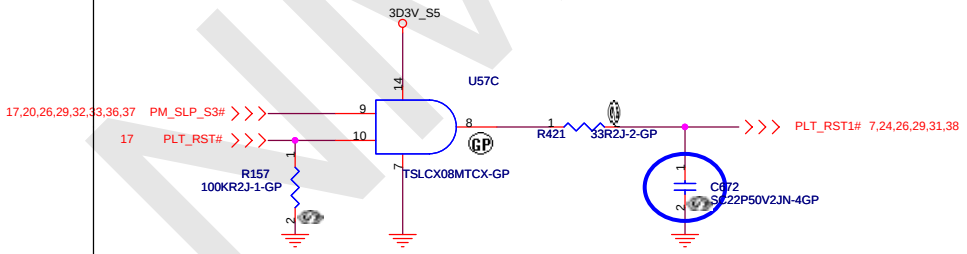
SMBUS

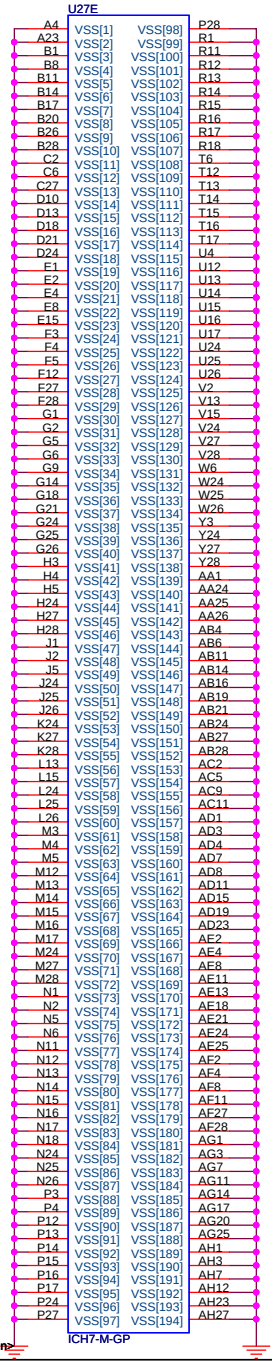


Q13 & Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance









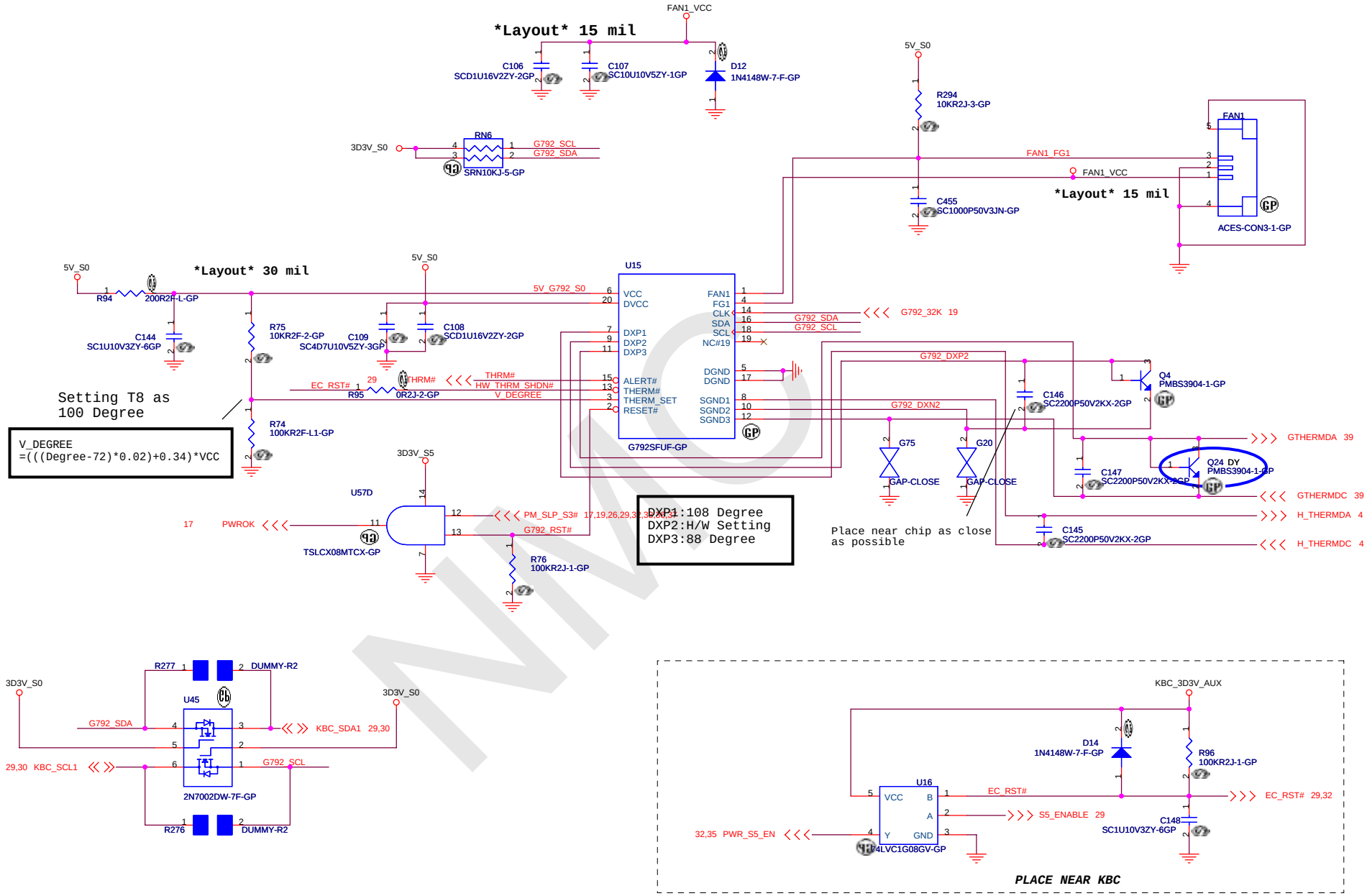
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ICH7-M (4 of 4)**

Size	Document Number	Rev
A3	KAI	SE

Date: Friday, March 24, 2006 Sheet 19 of 44



<Core Design>

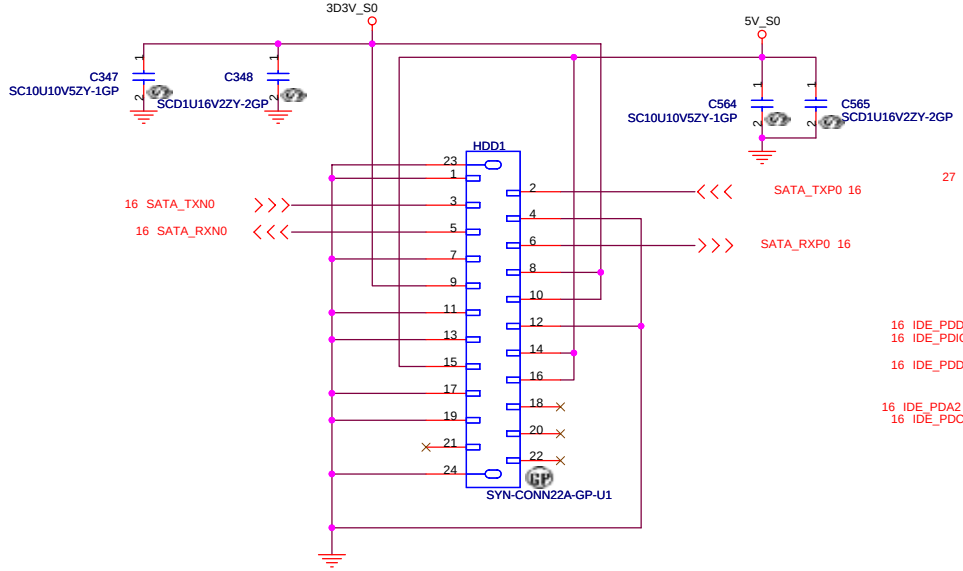
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Thermal/Fan Controllor***

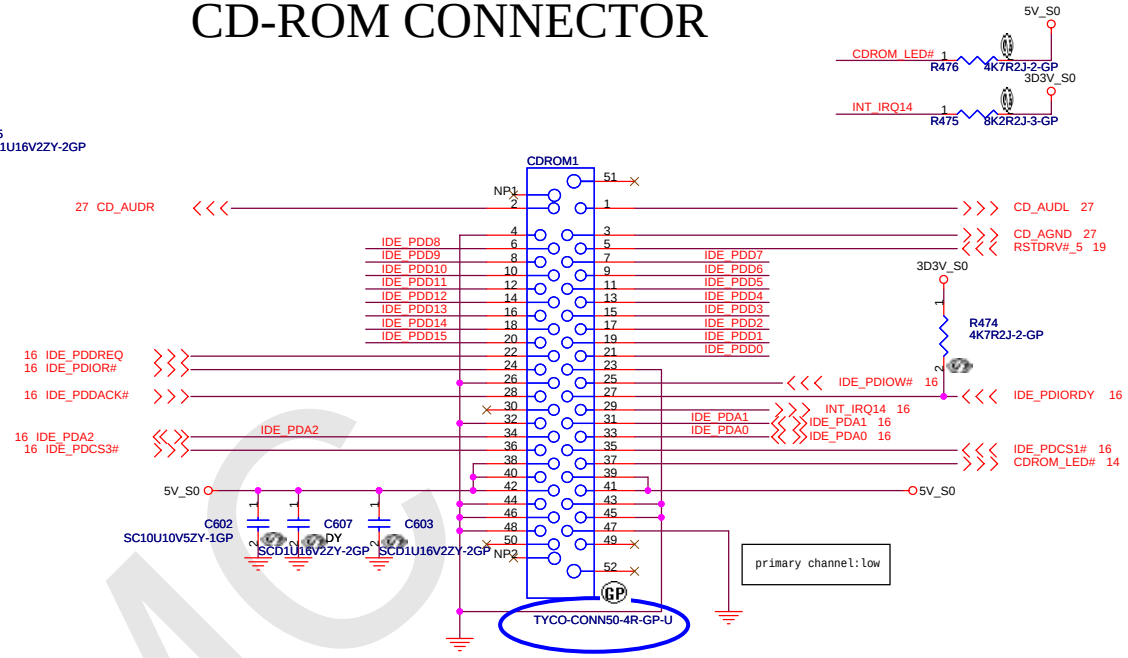
Size	Document Number	Rev
Custom	KAI	SE

Date: Monday, March 27, 2006 Sheet 20 of 44

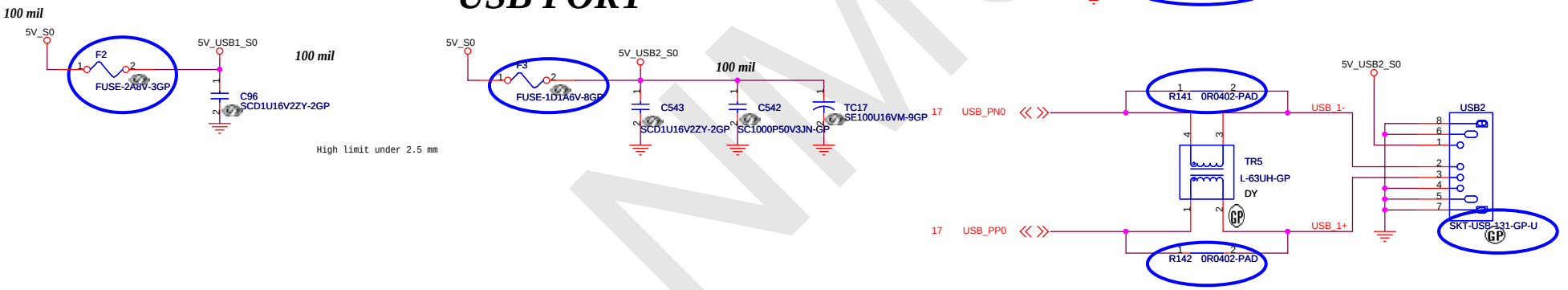
SATA HD Connector

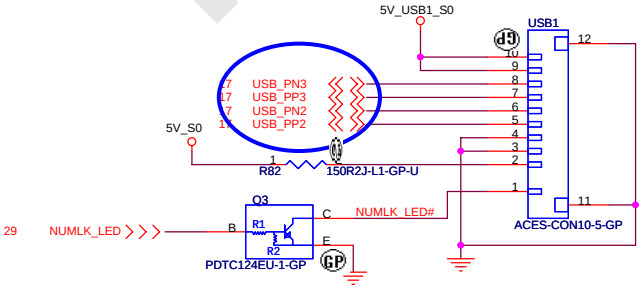


CD-ROM CONNECTOR



USB PORT

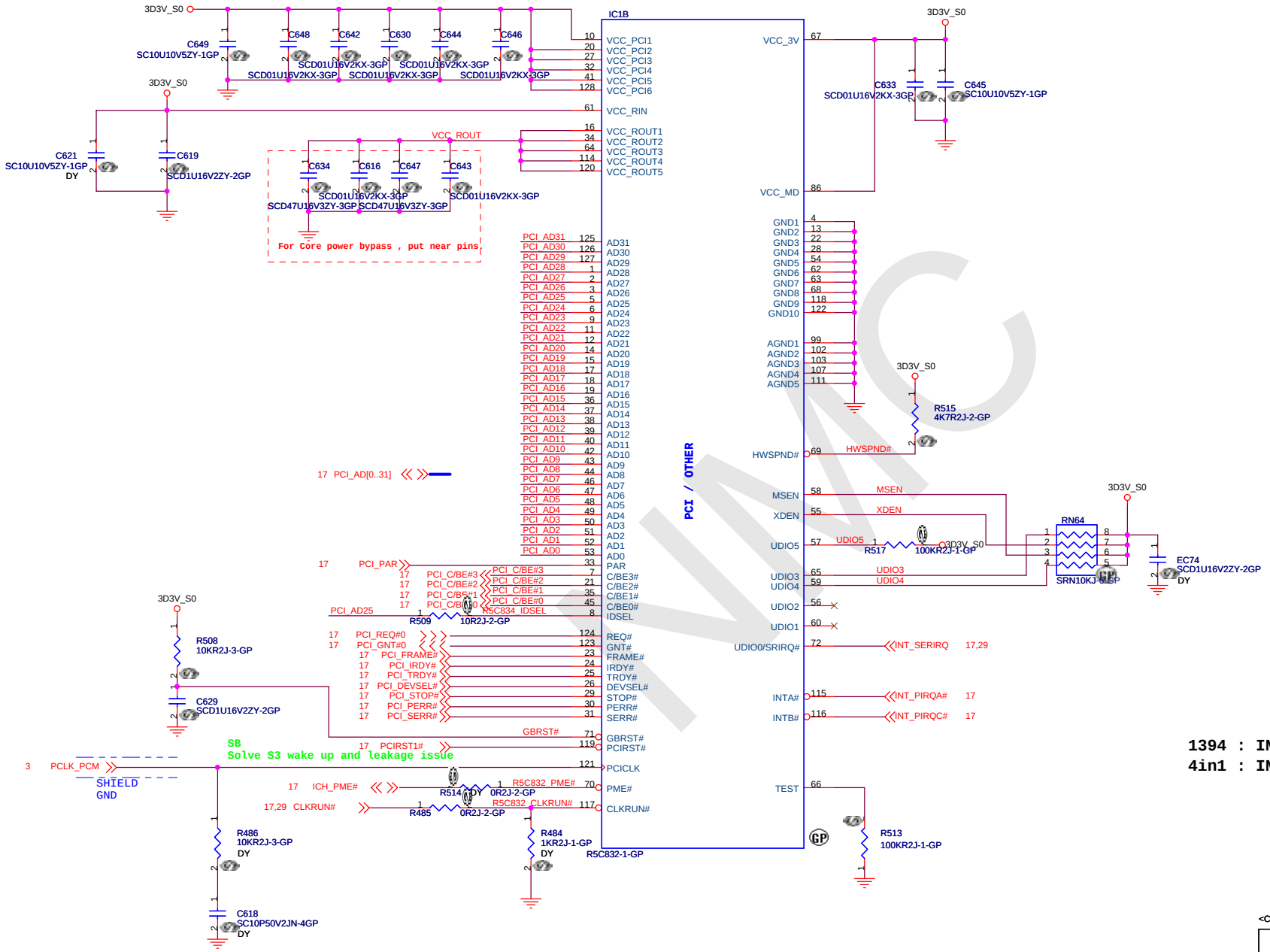




<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	HD/CDROM	
Size A3	Document Number KAI	Rev SE
Date: Friday, May 12, 2006	Sheet 21 of 44	



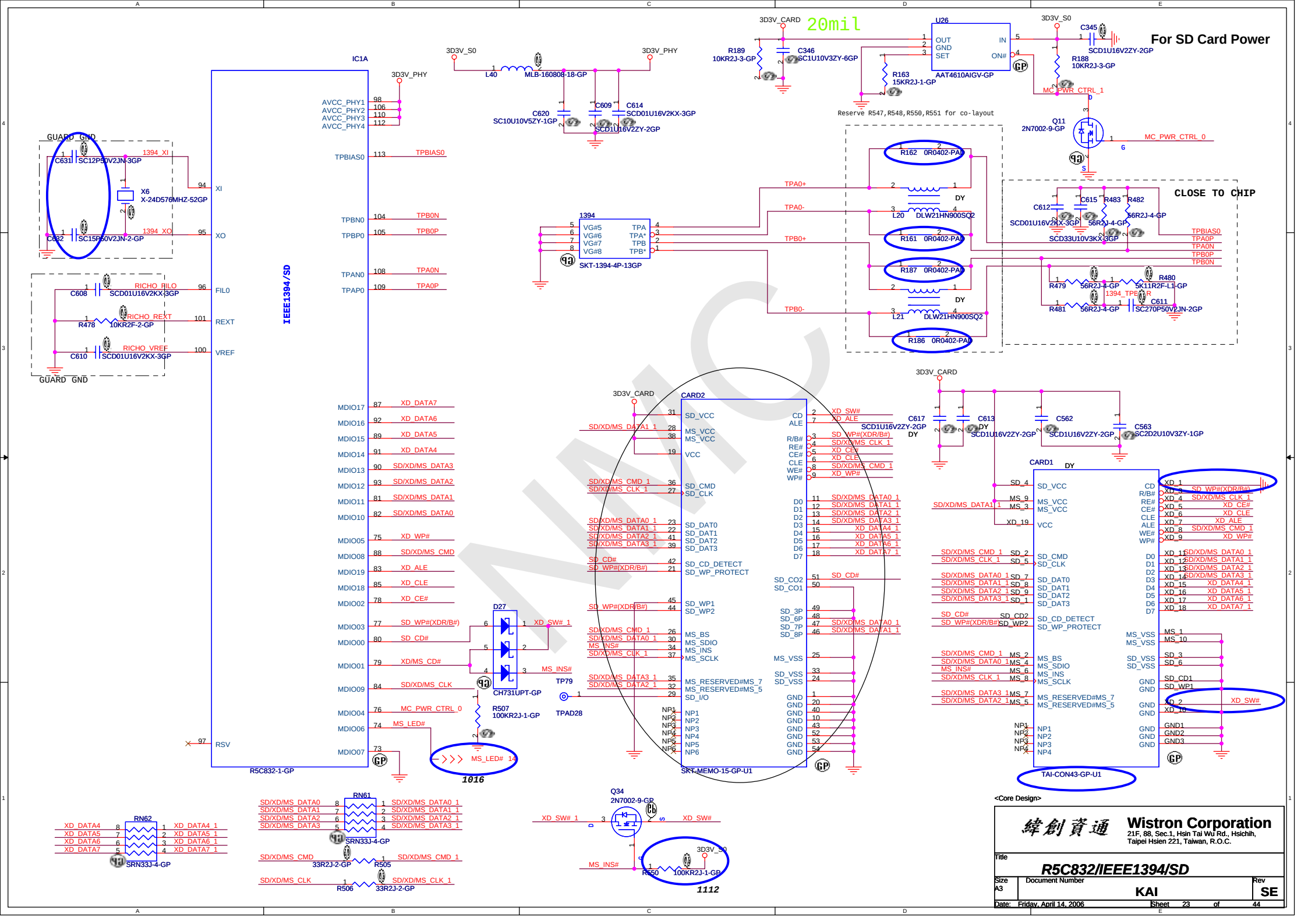
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: R5C832/PCI

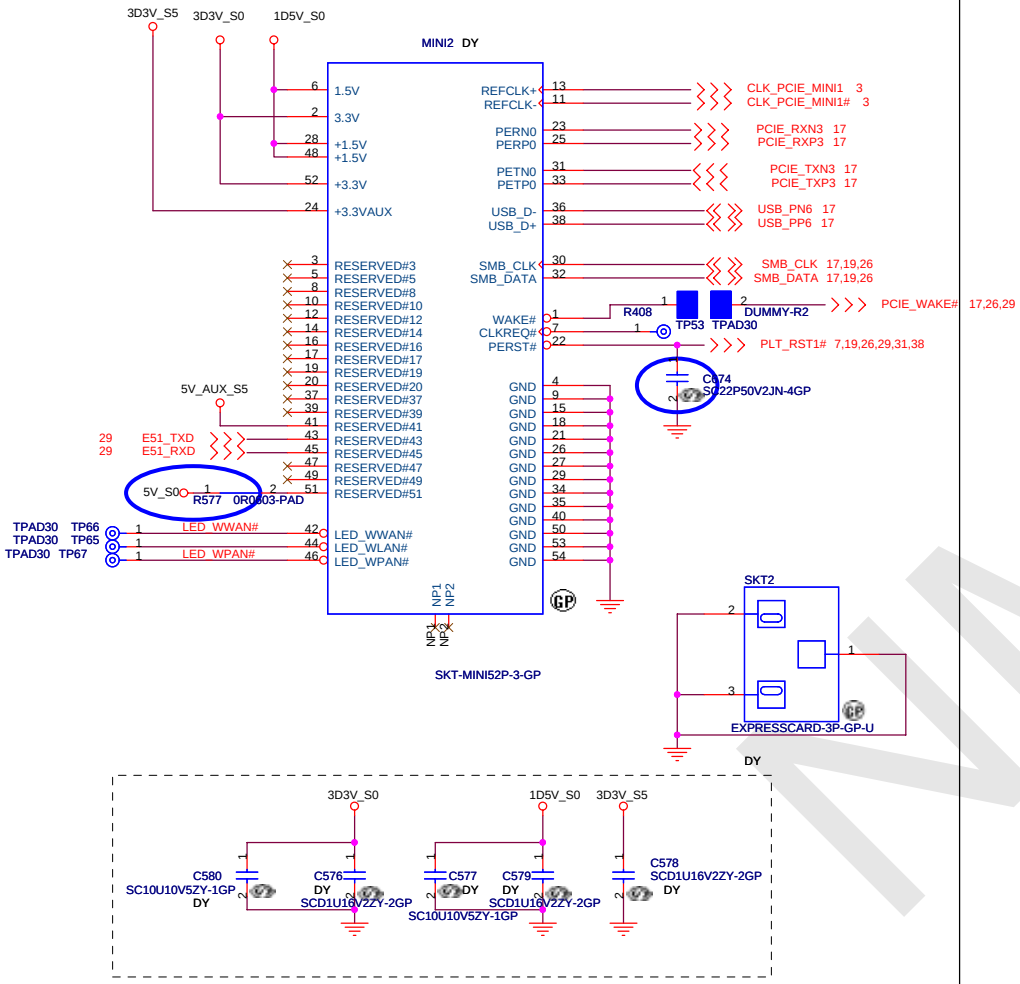
Size	Document Number	Rev
A3	KAI	SE

Date: Thursday, April 13, 2006 Sheet 22 of 44

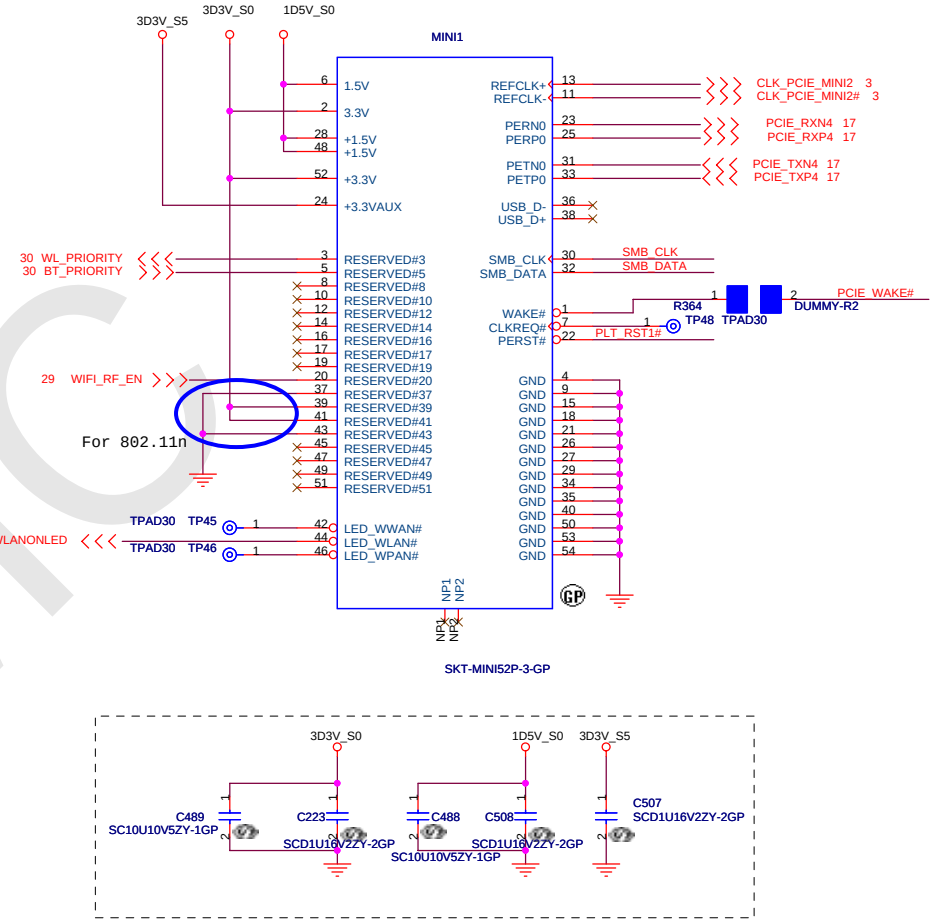

For SD Card Power
20mil
IC1A
IEEE1394/SD
R5C832-1-GP
CARD2
SKT-MEMO-15-GP-U1
CARD1
TAI-CON43-GP-U1
CLOSE TO CHIP
Reserve R547,R548,R550,R551 for co-layout
U26
AAT4610AIGV-GP
Q11
2N7002-9-GP
Q34
2N7002-9-GP
1394
SKT-1394-4P-13GP
D27
CH731UPT-GP
RN61
SRN33J-4-GP
RN62
SRN33J-4-GP
1016
1112
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
R5C832/IEEE1394/SD
Size A3
Document Number
KAI
Rev SE
Date: Friday, April 14, 2006
Sheet 23 of 44

Mini Card Connector

Mini Card Connector 2



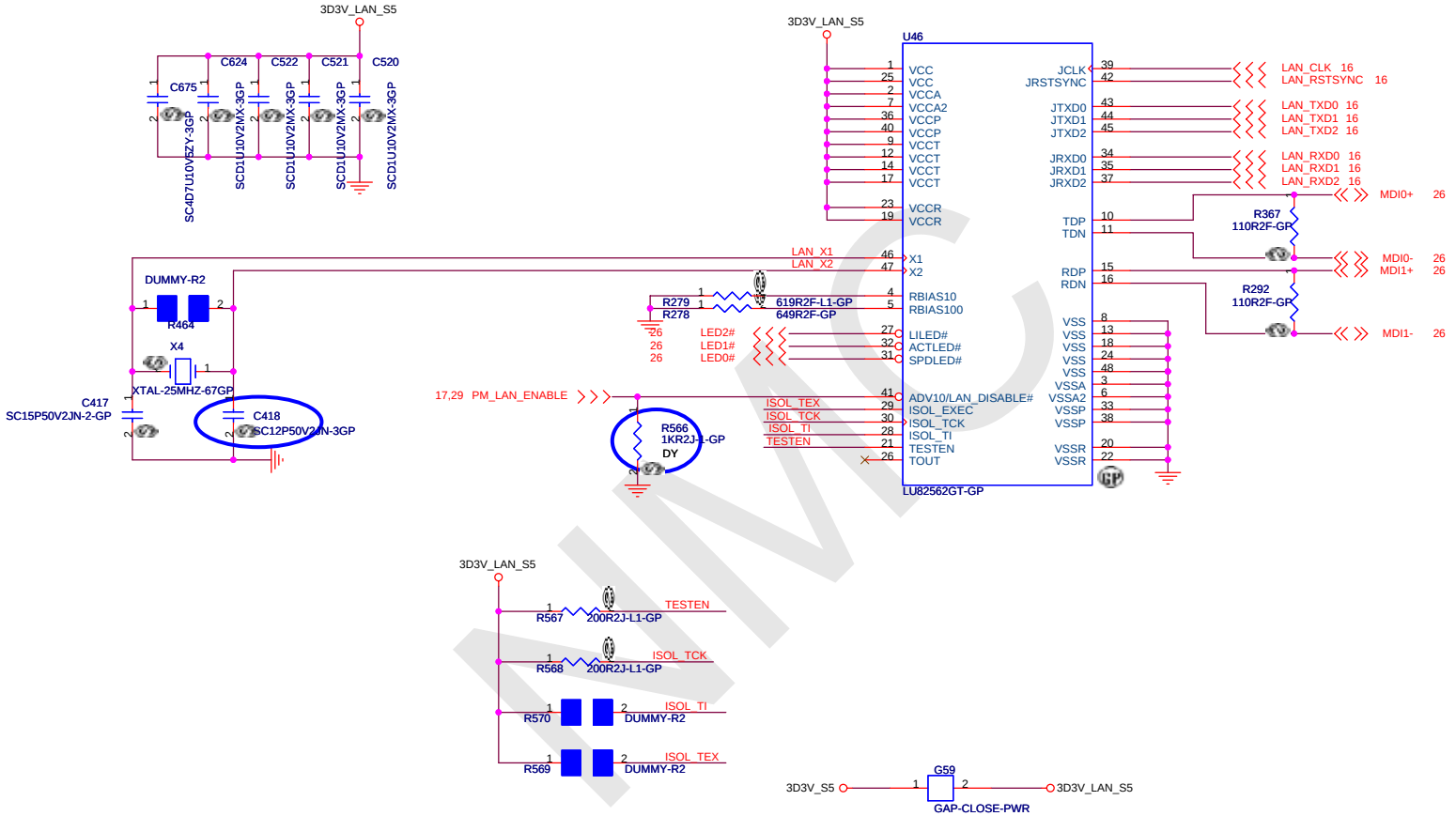
Mini Card Connector 1



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	MINI CARD CONN .	
Size A3	Document Number KAI	Rev SE
Date: Wednesday, May 24, 2006	Sheet 24 of 44	



TESTEN	ISOL_TCK	ISOL_TI	ISOL_TEK	
0	0	0	0	MODE0
0	0	1	1	MODE1
1	0	0	1	MODE2
1	0	1	1	MODE3
1	1	0	0	MODE4

<Core Design>

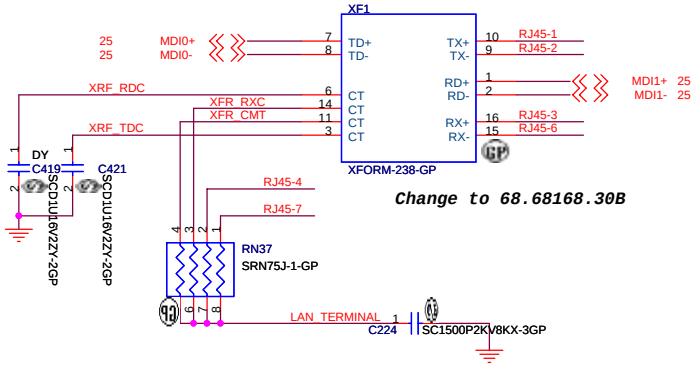
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN TEKOA**

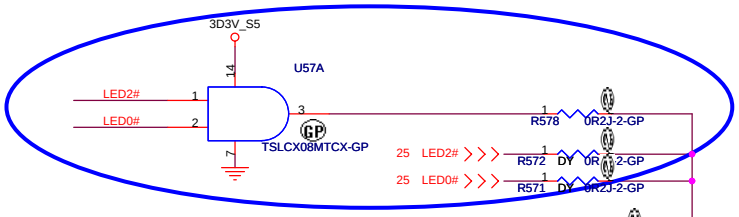
Size	Document Number	Rev
A3	KAI	SE

Date: Monday, March 27, 2006 Sheet 25 of 44

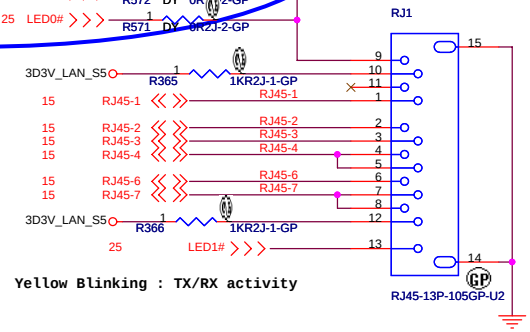
10/100M Lan Transformer



Change to 68.68168.30B



Green : Link 10/100 Mbps



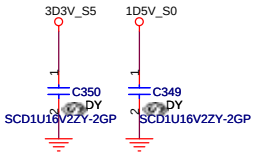
Yellow Blinking : TX/RX activity

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

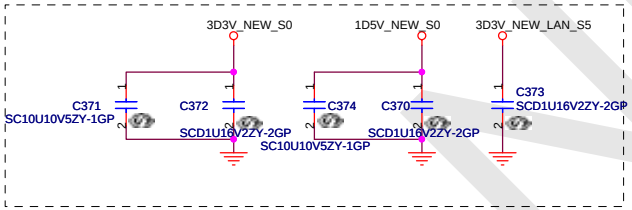
PIN09 : GREEN
PIN11 : ORANGE
PIN13 : YELLOW

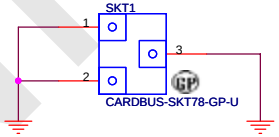
NEWCARD Connector

Place them Near to Chip

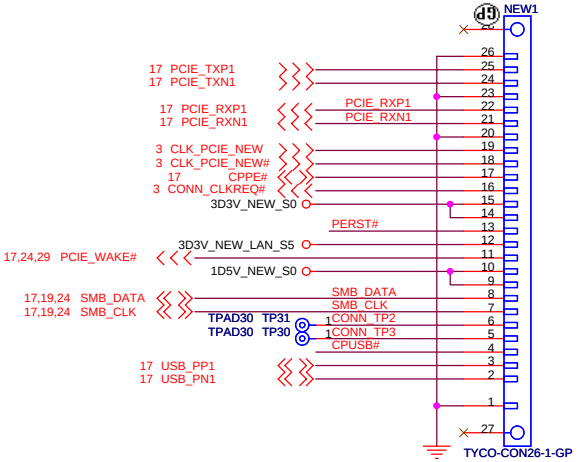


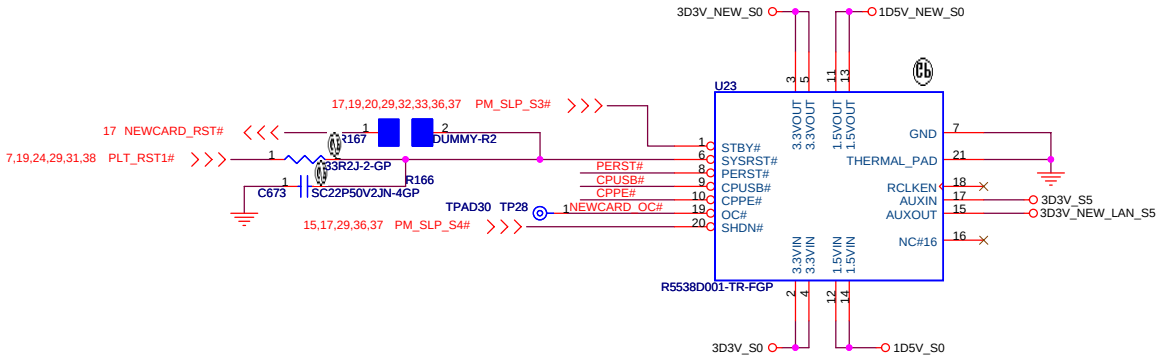
Place them Near to Connector





For Newcard socket





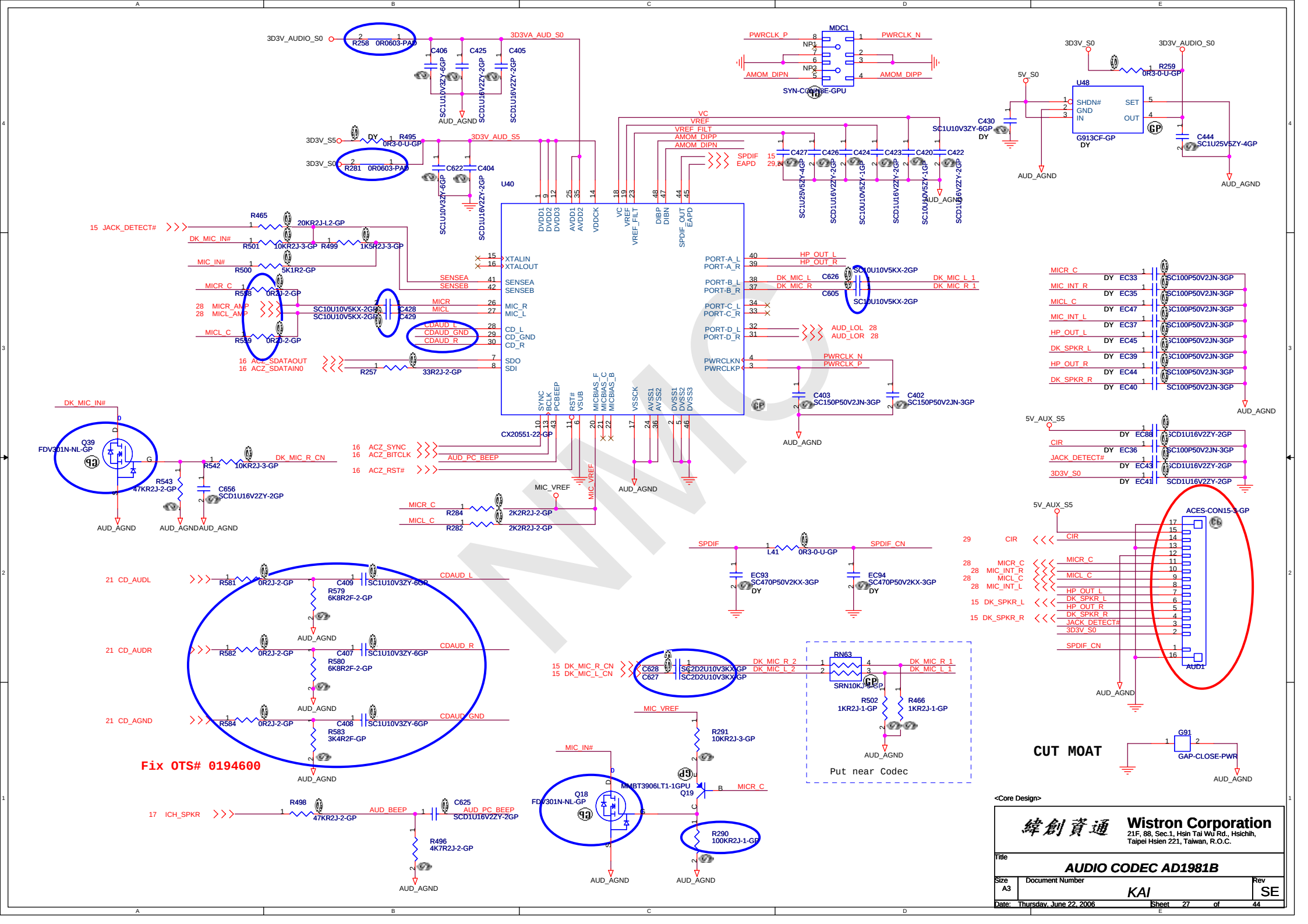
<Core Design>

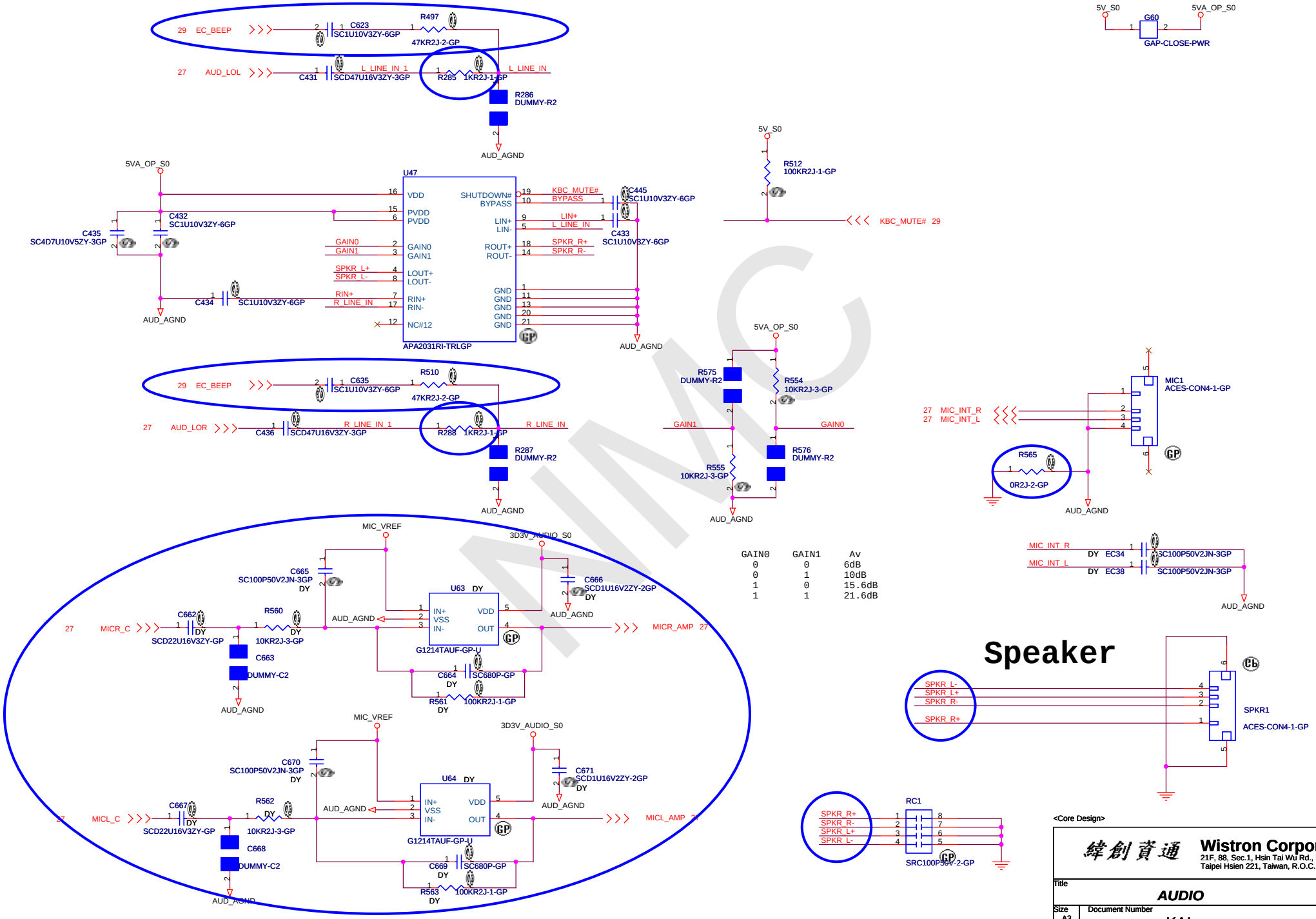
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **New Card**

Size	Document Number	Rev
A3	KAI	SE

Date: Thursday, April 13, 2006 Sheet 26 of 44

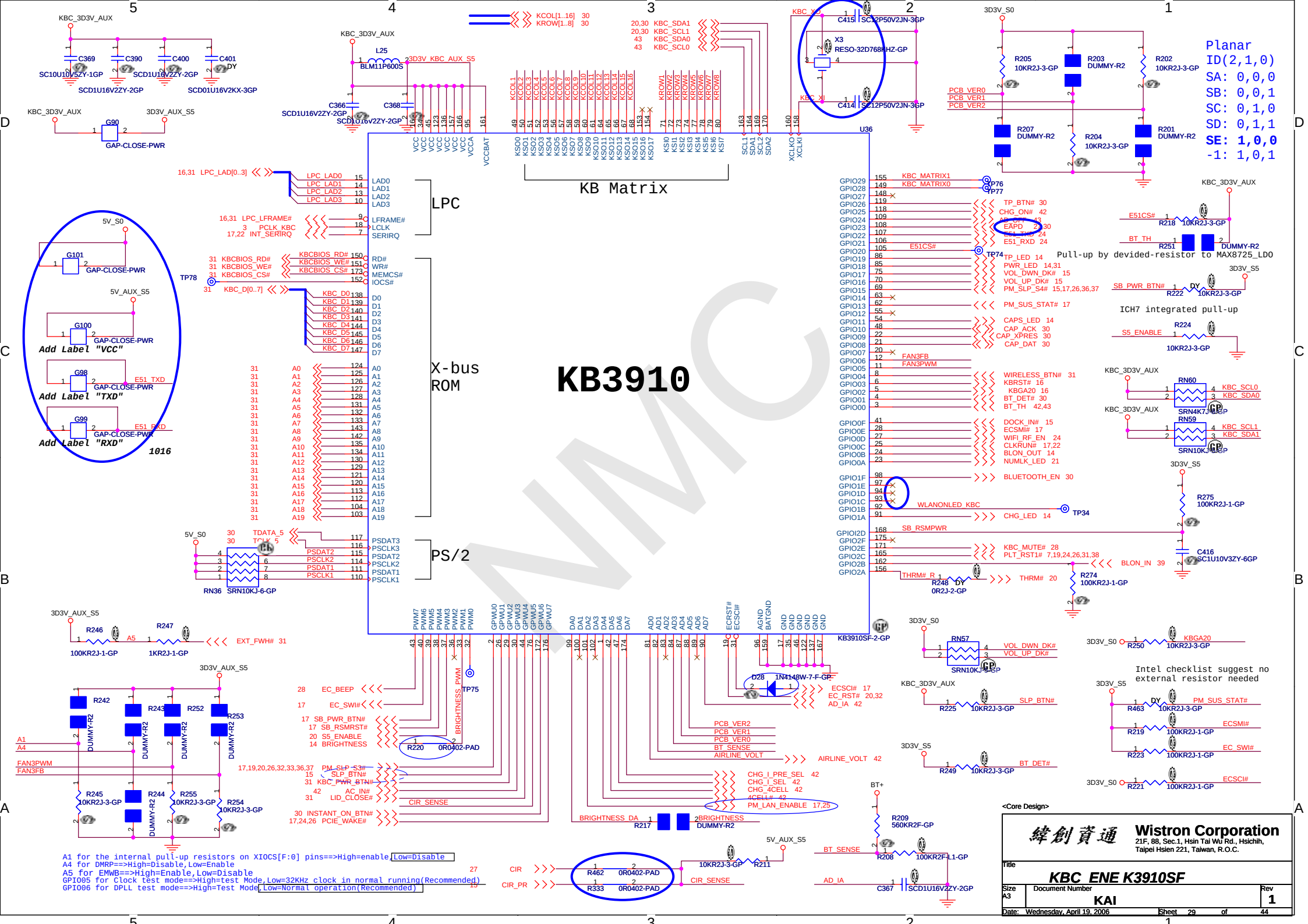

U40
MDC1
U48
3D3V_AUDIO_S0
3D3VA_AUD_S0
3D3V_AUD_S5
AUD_AGND
Fix OTS# 0194600
Put near Codec
CUT MOAT
ACES-CON15-3-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
AUDIO CODEC AD1981B
KAI
Thursday, June 22, 2006



<core_design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**AUDIO**	
Size A3	Document Number KAI	Rev SE
Date: Tuesday, May 23, 2006	Sheet 28 of 44	

</core_design>


KB3910
KB Matrix
LPC
X-bus ROM
PS/2
U36
KB3910SF-2-GP
Planar
ID(2,1,0)
SA: 0,0,0
SB: 0,0,1
SC: 0,1,0
SD: 0,1,1
SE: 1,0,0
-1: 1,0,1
Add Label "VCC"
Add Label "TXD"
Add Label "RXD"
1016
Pull-up by devided-resistor to MAX8725_LDO
ICH7 integrated pull-up
Intel checklist suggest no external resistor needed
A1 for the internal pull-up resistors on XIOCS[F:0] pins==>High=enable,Low=Disable
A4 for DMRP==>High=Disable,Low=Enable
A5 for EMWB==>High=Enable,Low=Disable
GPIO05 for Clock test mode==>High=test Mode,Low=32KHz clock in normal running(Recommended)
GPIO06 for DPLL test mode==>High=Test Mode,Low=Normal operation(Recommended)
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC_ENE K3910SF
KAI
Wednesday, April 19, 2006

CAMERA

Blue thumb

Internal KeyBoard Connector

29 KROW[1..8]
29 KCOL[1..16]

KB1
ACES-CON24-2-GP

Keyboard matrix (from vendor)

	US	Eur	Jap
MATRIXID1#	0	1	0
MATRIXID2#	0	0	1

TouchPad Connector

TPAD1
ACES-CON8-6-GP

CAM1
ACES-CON5-1GP

BT1
ACES-CON8-4-GP

Close to BT1

U61
G913CF-GP
MAX 150mA
FIXED MODE

TR4
TR6
L-63UH-GP

CAPACITY BUTTON

CAP1
ACES-CON12-4-GP

TOUCH-PAD SWITCH

SW1
SW-TACT-68-GP-U

RC6 RC5 RC4 RC7 RC2 RC3
SRC100P50V-2-GP
for EMI

Wistron Corporation
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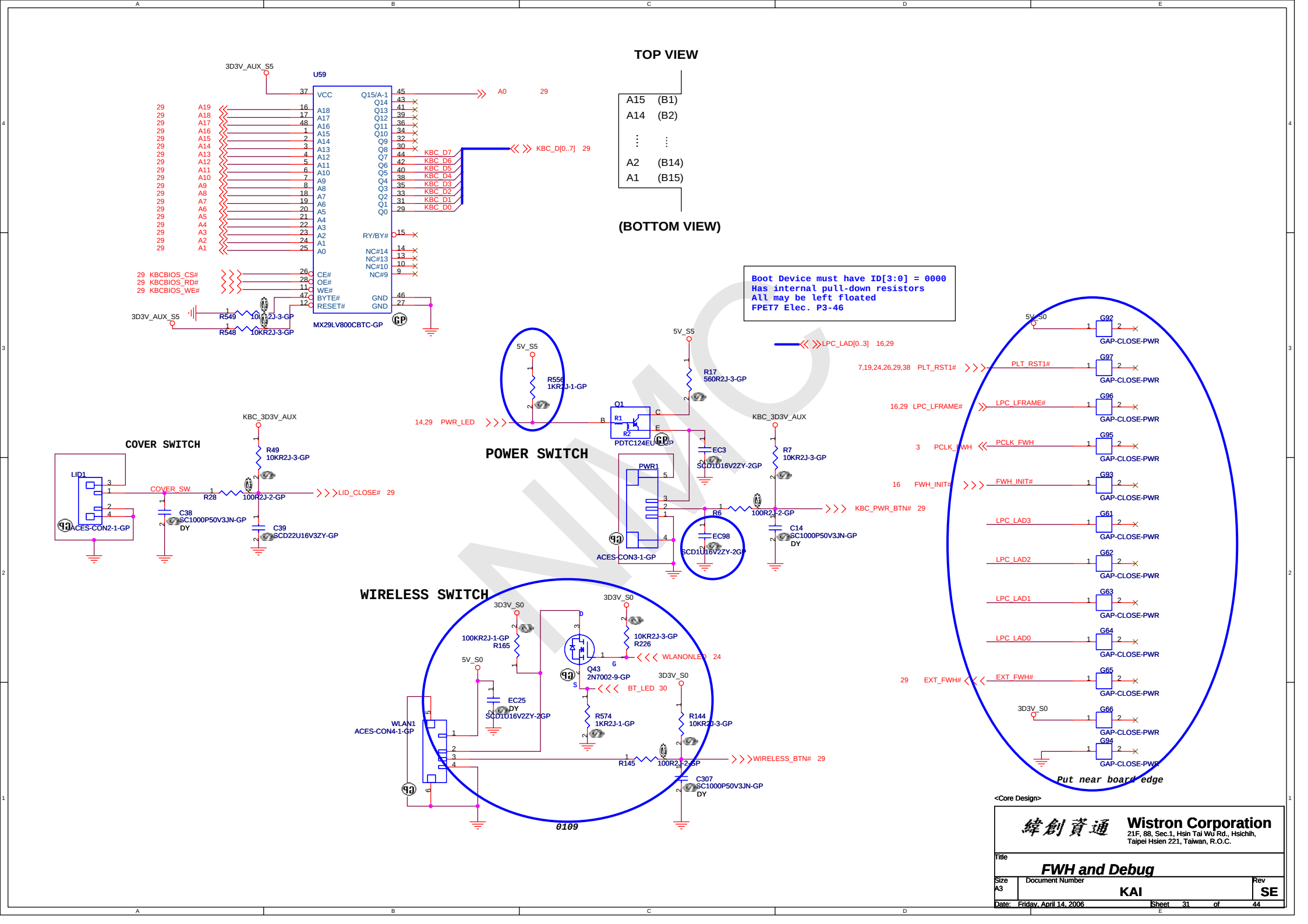
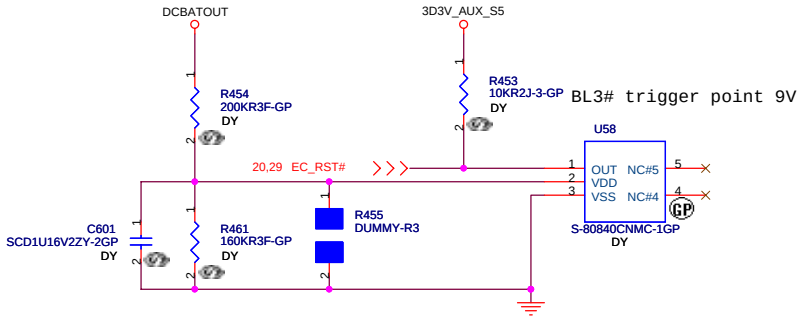
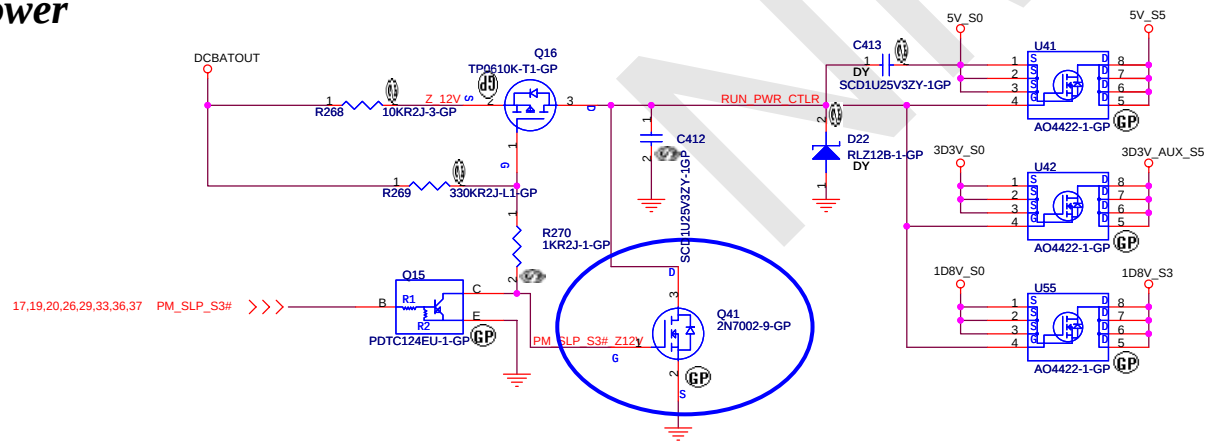
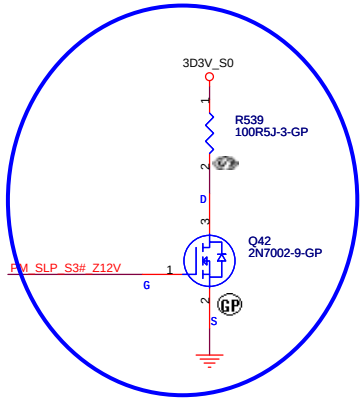
Title: KeyBoard-CONN
Size: A3
Document Number: KAI
Rev: SE
Date: Friday, April 14, 2006
Sheet 30 of 44

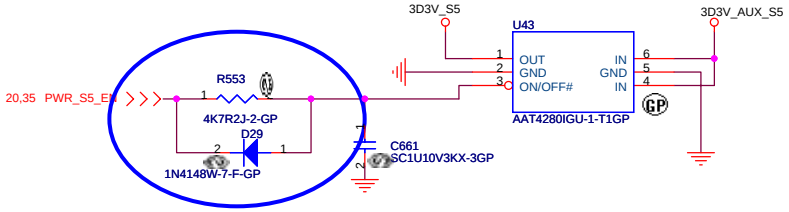

TOP VIEW
A15 (B1)
A14 (B2)
A2 (B14)
A1 (B15)
(BOTTOM VIEW)
U59
MX29LV800CBTC-GP
Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46
COVER SWITCH
POWER SWITCH
WIRELESS SWITCH
ACES-CON2-1-GP
ACES-CON3-1-GP
ACES-CON4-1-GP
PDTC124EU-2-GP
Q43 2N7002-9-GP
GAP-CLOSE-PWR
Put near board edge
0109
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
FWH and Debug
KAI
SE
Friday, April 14, 2006
31
44



Run Power



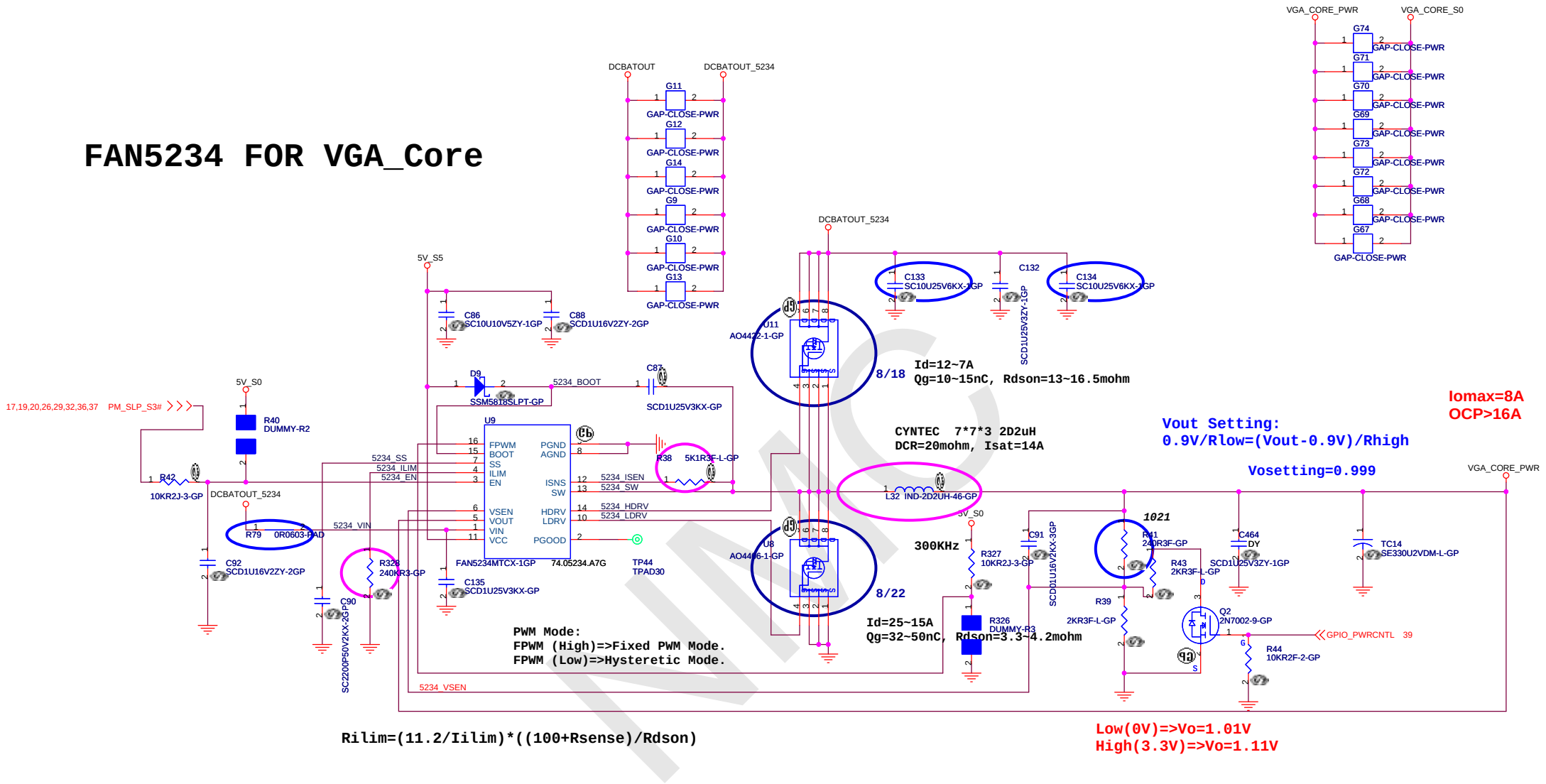




<Core Design>

緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	PWRPLANE&RESETLOGIC
Size A3 / Document Number	KAI / Rev SE
Date: Wednesday, May 17, 2006	Sheet 32 of 44

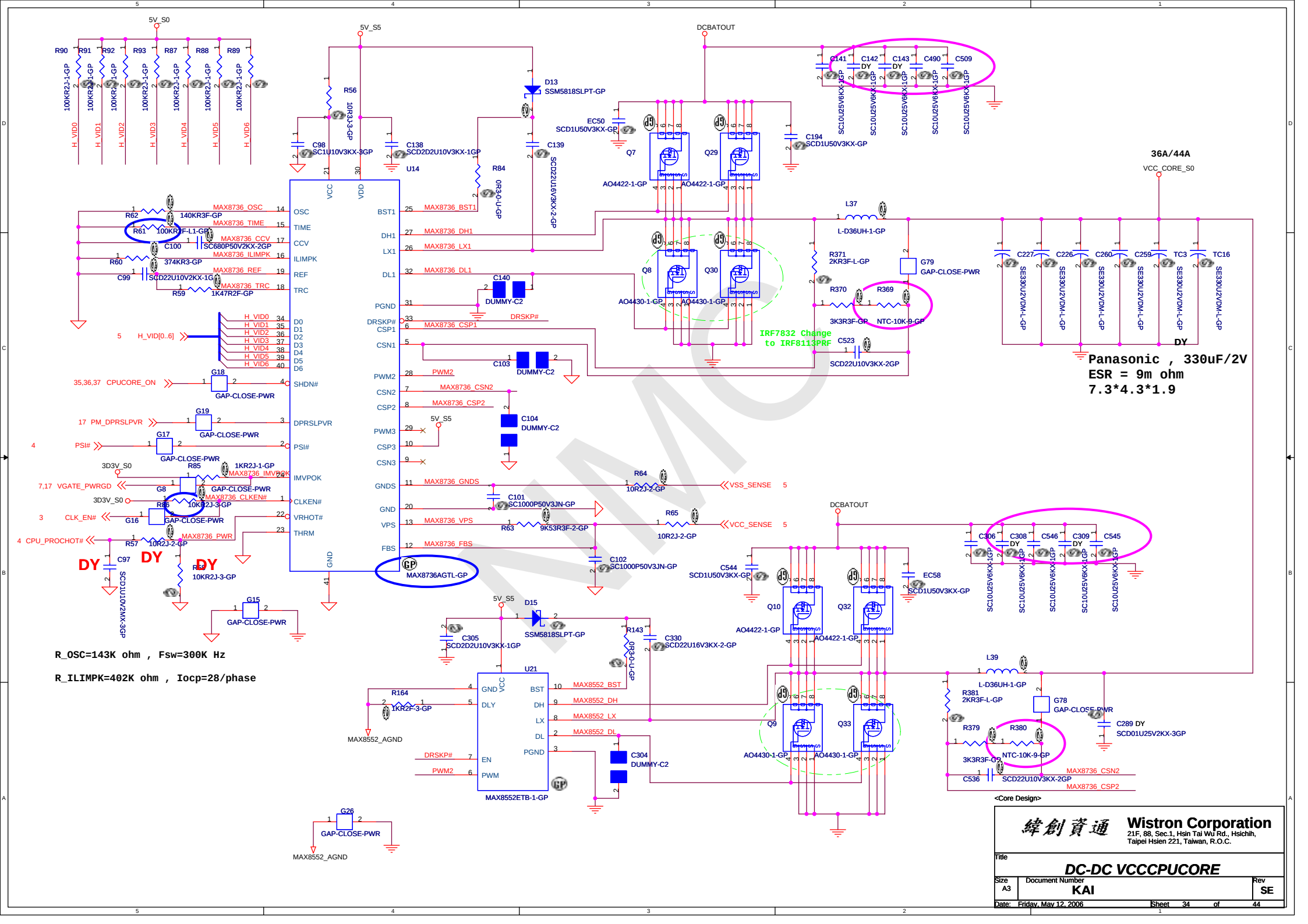
FAN5234 FOR VGA_Core



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	VGA CORE 1V	
Size A3	Document Number TACOMA	Rev SE
Date: Friday, April 14, 2006	Sheet 33 of 44	


5V_S0
5V_S5
DCBATOUT
36A/44A
VCC_CORE_S0
MAX8736AGTL-GP
MAX8552ETB-1-GP
Panasonic , 330uF/2V
ESR = 9m ohm
7.3*4.3*1.9
IRF7832 Change
to IRF8113PRF
R_OSC=143K ohm , Fsw=300K Hz
R_ILIMPK=402K ohm , Iocp=28/phase
DY
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DC-DC VCCCPUCORE
Size A3
Document Number KAI
Rev SE
Date: Friday, May 12, 2006
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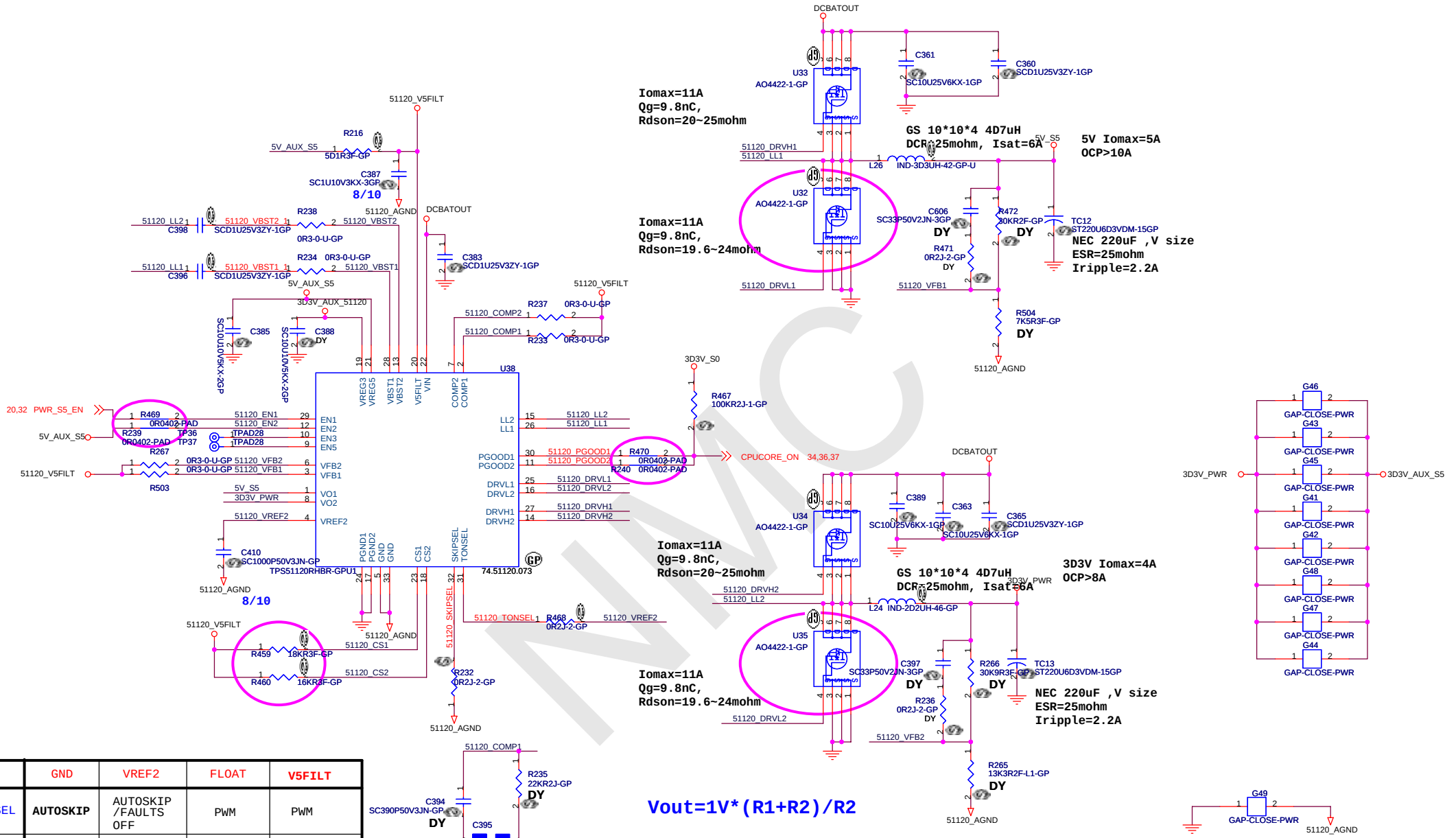

	GND	VREF2	FLOAT	V5FILT
SKIPSEL	**AUTOSKIP**	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	**D-Cap MODE**
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	**220k/CH1 330k/CH2**	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	**5V Fixed Output**
VFB2	N/A	not use	ADJ.	**3.3V Fixed Output**
EN1,EN2	Switcher OFF	not use	Swithchr ON	**Switcher ON**
EN3,EN5	LDO OFF	not use	**LDO ON**	VREG3 on

For TPS51120,
Vout=5V
1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.

Vout=3.3V
1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

<Core Design>

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Title: **5V_S5/3D3V_S5**

Size: A3 | Document Number: **KAI** | Rev: SE

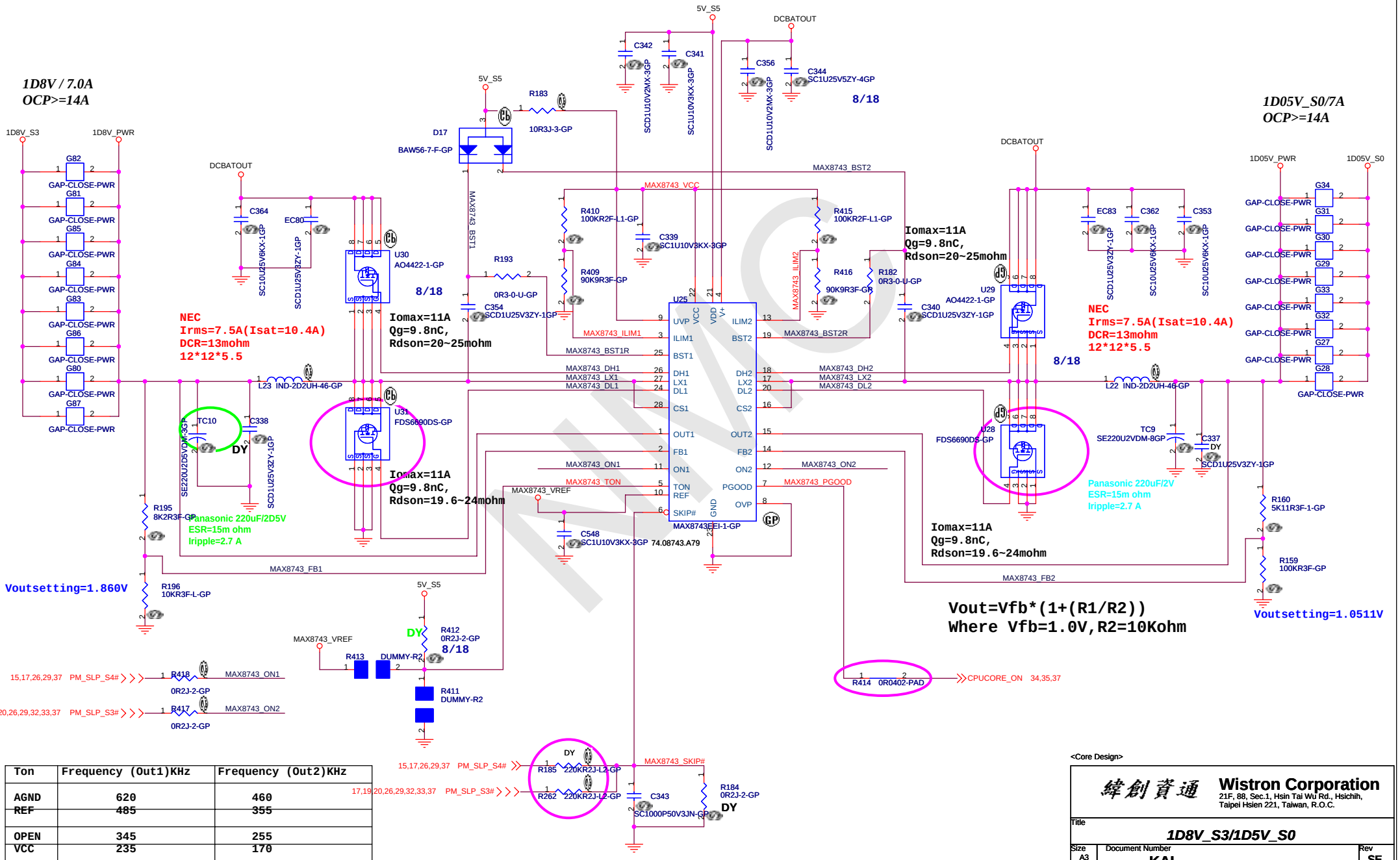
Date: Thursday, April 13, 2006 | Sheet 35 of 44

Iocp=7.0 2 = 14A*
Rds,on=17m ohm
*Vcs1=Iocp*Rds,on=238mV*
VILIM=Vcs1/0.1=2.38V

*Iocp=7.0*2 = 14A*
Rds,on=17m ohm
*Vcs2=Iocp*Rds,on=28mV*
VILIM2=Vcs2/0.1=2.38V

1D8V / 7.0A
OCP>=14A

1D05V_S0/7A
OCP>=14A



Ton	Frequency (Out1)KHz	Frequency (Out2)KHz
AGND	620	460
REF	485	355
OPEN	345	255
VCC	235	170

<Core Design>

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Title: *1D8V_S3/1D5V_S0*

Size: A3 | Document Number: KAI | Rev: SE

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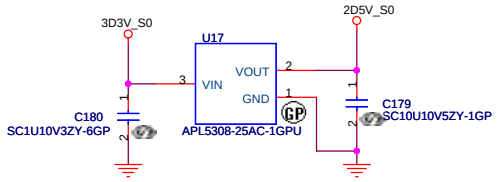
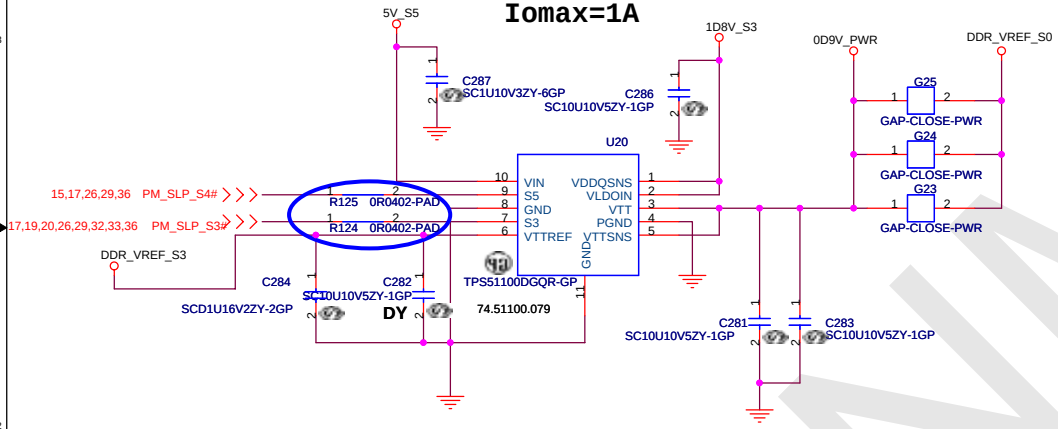
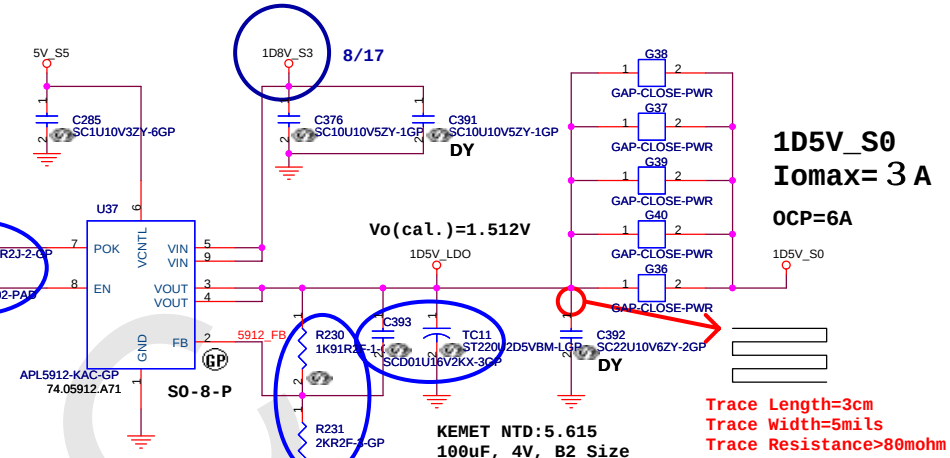
2D5V_S0
Iomax=300mA



0D9V
Iomax=1A





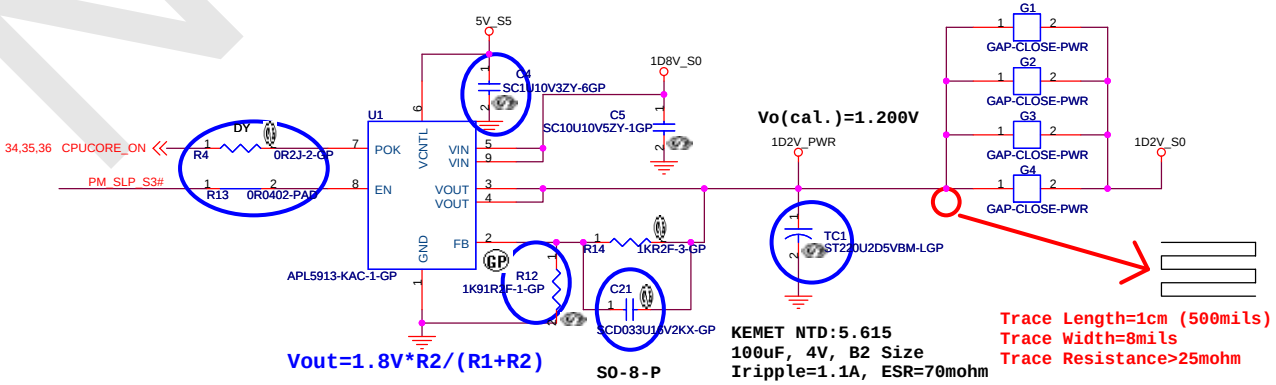
1D5V_S0
Iomax= 3 A
OCP=6A

Vo=0.8*(1+(R1/R2))

KEMET NTD:5.615
100uF, 4V, B2 Size
Iripple=1.1A, ESR=70mohm

Trace Length=3cm
Trace Width=5mils
Trace Resistance>80mohm

1D2V_S0
Iomax=3A



KEMET NTD:5.615
100uF, 4V, B2 Size
Iripple=1.1A, ESR=70mohm

Trace Length=1cm (500mils)
Trace Width=8mils
Trace Resistance>25mohm

<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: 0D9V_LDO/1D2V_LDO/1D5V_LDO/2D5V_LDO

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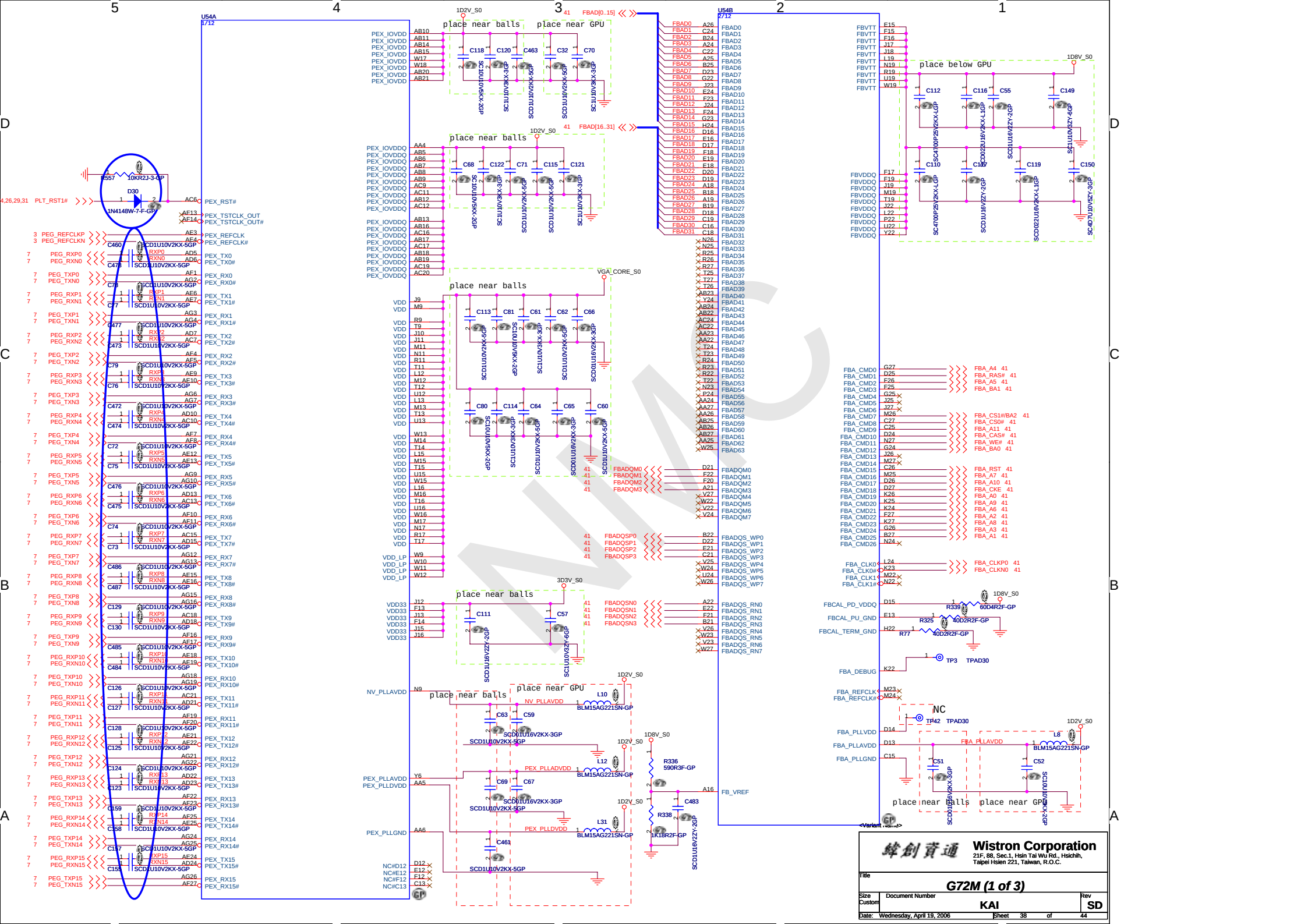
U54A
1/12
U54B
2/12
place near balls
place near GPU
place below GPU
VGA_CORE_S0
1D2V_S0
1D8V_S0
3D3V_S0
PEX_RST#
PEX_TSTCLK_OUT
PEX_TSTCLK_OUT#
PEX_REFCLK
PEX_REFCLK#
PLT_RST1#
R557 10KR2J-3-GP
D30 1N4148W-7-F-GP
FBAD[0..15]
FBAD[16..31]
FBADQM0
FBADQM1
FBADQM2
FBADQM3
FBADQSP0
FBADQSP1
FBADQSP2
FBADQSP3
FBADQSN0
FBADQSN1
FBADQSN2
FBADQSN3
FB_VREF
FBA_CMD0
FBA_CMD1
FBA_CMD2
FBA_CMD3
FBA_CMD4
FBA_CMD5
FBA_CMD6
FBA_CMD7
FBA_CMD8
FBA_CMD9
FBA_CMD10
FBA_CMD11
FBA_CMD12
FBA_CMD13
FBA_CMD14
FBA_CMD15
FBA_CMD16
FBA_CMD17
FBA_CMD18
FBA_CMD19
FBA_CMD20
FBA_CMD21
FBA_CMD22
FBA_CMD23
FBA_CMD24
FBA_CMD25
FBA_CMD26
FBA_A4
FBA_RAS#
FBA_A5
FBA_BA1
FBA_CS1#/BA2
FBA_CS0#
FBA_A11
FBA_CAS#
FBA_WE#
FBA_BA0
FBA_RST
FBA_A7
FBA_A10
FBA_CKE
FBA_A0
FBA_A9
FBA_A6
FBA_A2
FBA_A8
FBA_A3
FBA_A1
FBA_CLKP0
FBA_CLKN0
FBA_CLK0
FBA_CLK0#
FBA_CLK1
FBA_CLK1#
FBCAL_PD_VDDQ
FBCAL_PU_GND
FBCAL_TERM_GND
R339 60D4R2F-GP
R325 40D2R2F-GP
R77 40D2R2F-GP
TP3 TPAD30
FBA_DEBUG
FBA_REFCLK
FBA_REFCLK#
NC
TP42 TPAD30
FBA_PLLVDD
FBA_PLLAVDD
FBA_PLLGND
L8 BLM15AG221SN-GP
C51
C52
L10 BLM15AG221SN-GP
L12 BLM15AG221SN-GP
L31 BLM15AG221SN-GP
R336 590R3F-GP
R338 1K18R2F-GP
C483
C461
PEX_PLLAVDD
PEX_PLLDVDD
PEX_PLLGND
NV_PLLAVDD
PEX_PLLDVDD
NC#D12
NC#E12
NC#F12
NC#C13
Wistron Corporation
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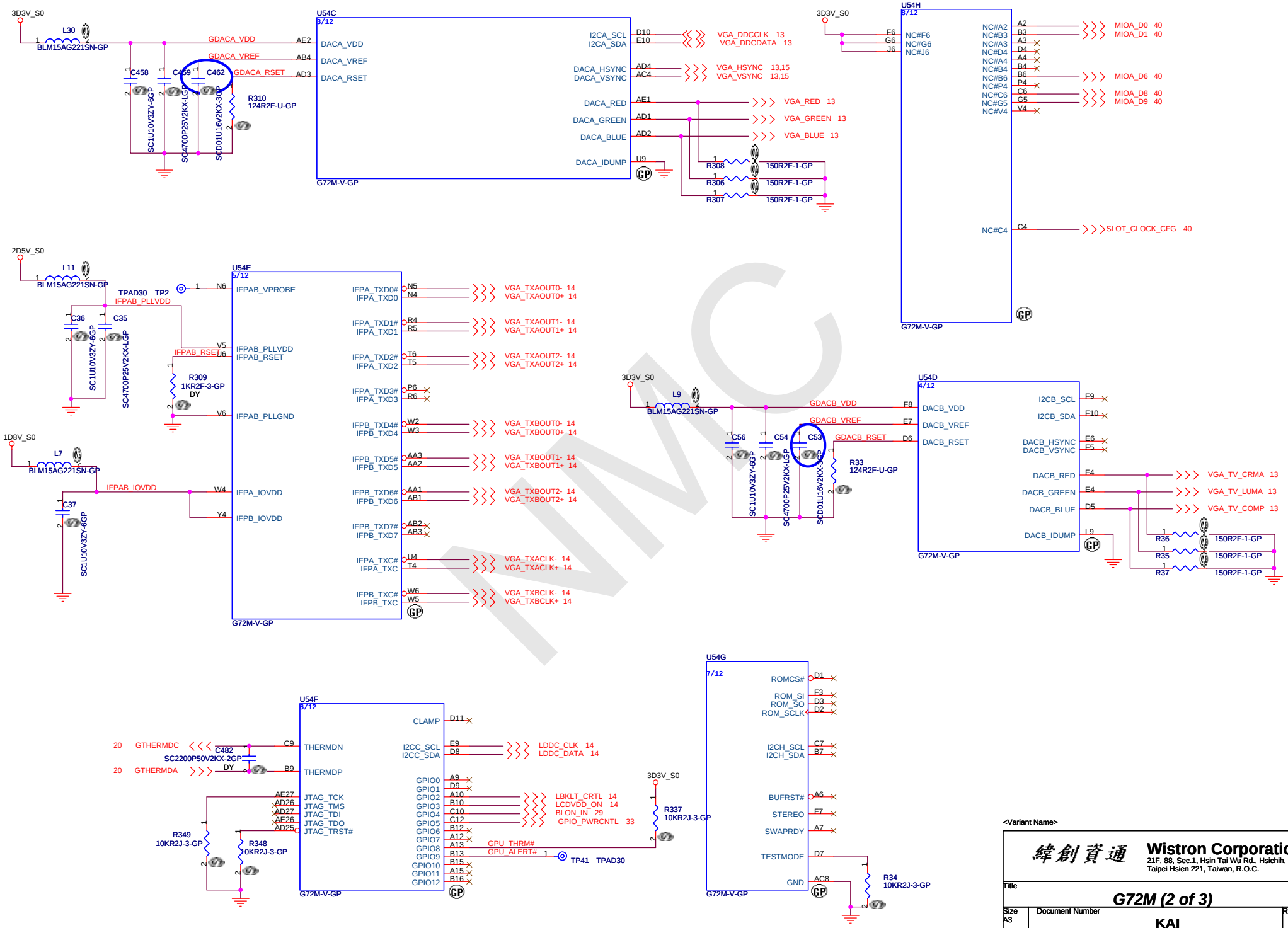
Taipei Hsien 221, Taiwan, R.O.C.
Title
G72M (1 of 3)
Size
Custom
Document Number
KAI
Rev
SD
Date: Wednesday, April 19, 2006
Sheet 38 of 44



<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***G72M (2 of 3)***	
Size A3	Document Number **KAI**	Rev **SE**
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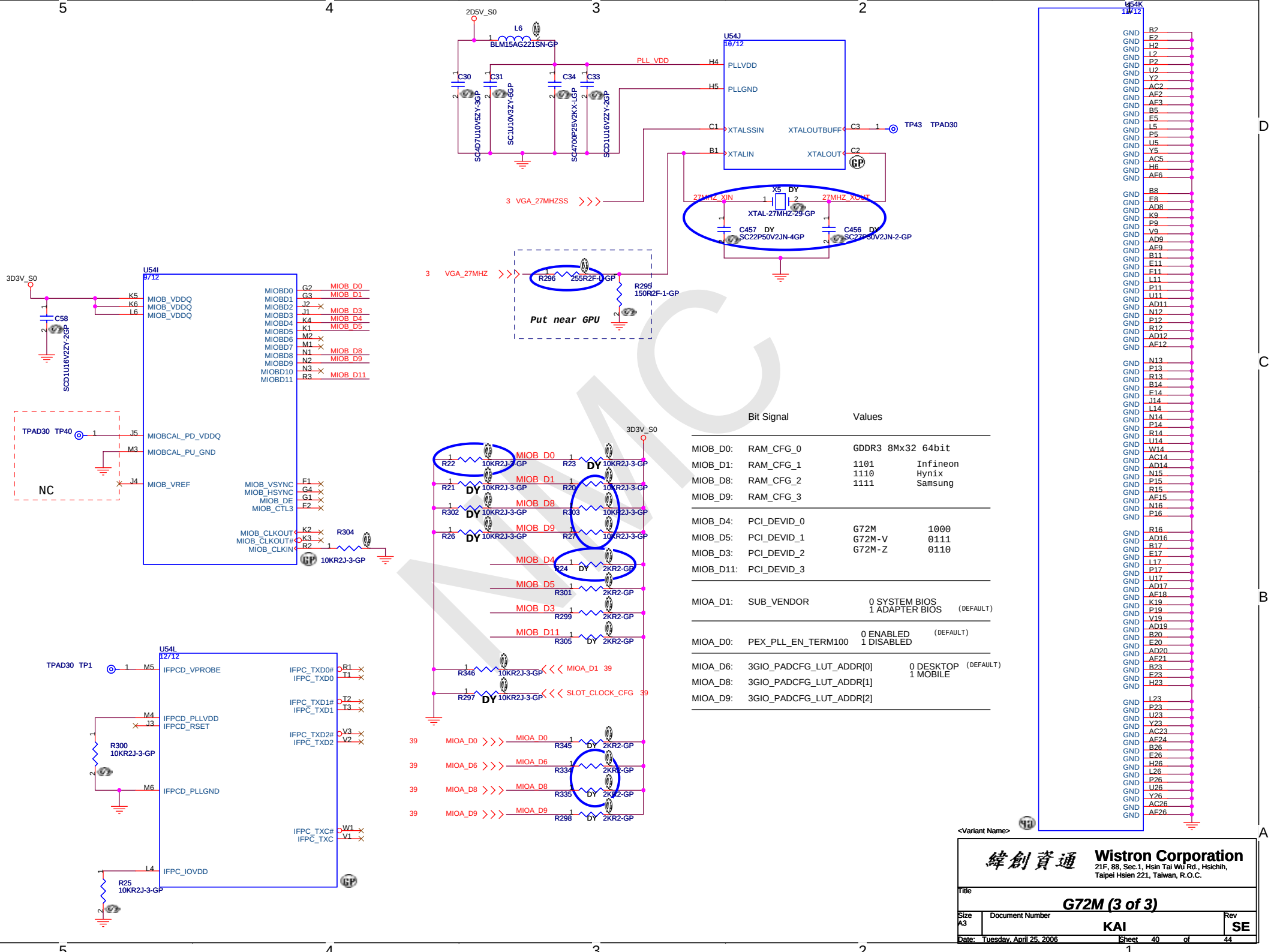

Bit	Signal	Values	
MIOB_D0:	RAM_CFG_0	GDDR3 8Mx32 64bit	
MIOB_D1:	RAM_CFG_1	1101	Infineon
MIOB_D8:	RAM_CFG_2	1110	Hynix
MIOB_D9:	RAM_CFG_3	1111	Samsung
MIOB_D4:	PCI_DEVID_0	G72M	1000
MIOB_D5:	PCI_DEVID_1	G72M-V	0111
MIOB_D3:	PCI_DEVID_2	G72M-Z	0110
MIOB_D11:	PCI_DEVID_3		
MIOA_D1:	SUB_VENDOR	0 SYSTEM BIOS 1 ADAPTER BIOS	(DEFAULT)
MIOA_D0:	PEX_PLL_EN_TERM100	0 ENABLED 1 DISABLED	(DEFAULT)
MIOA_D6:	3GIO_PADCFG_LUT_ADDR[0]	0 DESKTOP 1 MOBILE	(DEFAULT)
MIOA_D8:	3GIO_PADCFG_LUT_ADDR[1]		
MIOA_D9:	3GIO_PADCFG_LUT_ADDR[2]		

<Variant Name>

緯創資通 Wistron Corporation
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Title: G72M (3 of 3)

Size: A3 | Document Number: KAI | Rev: SE

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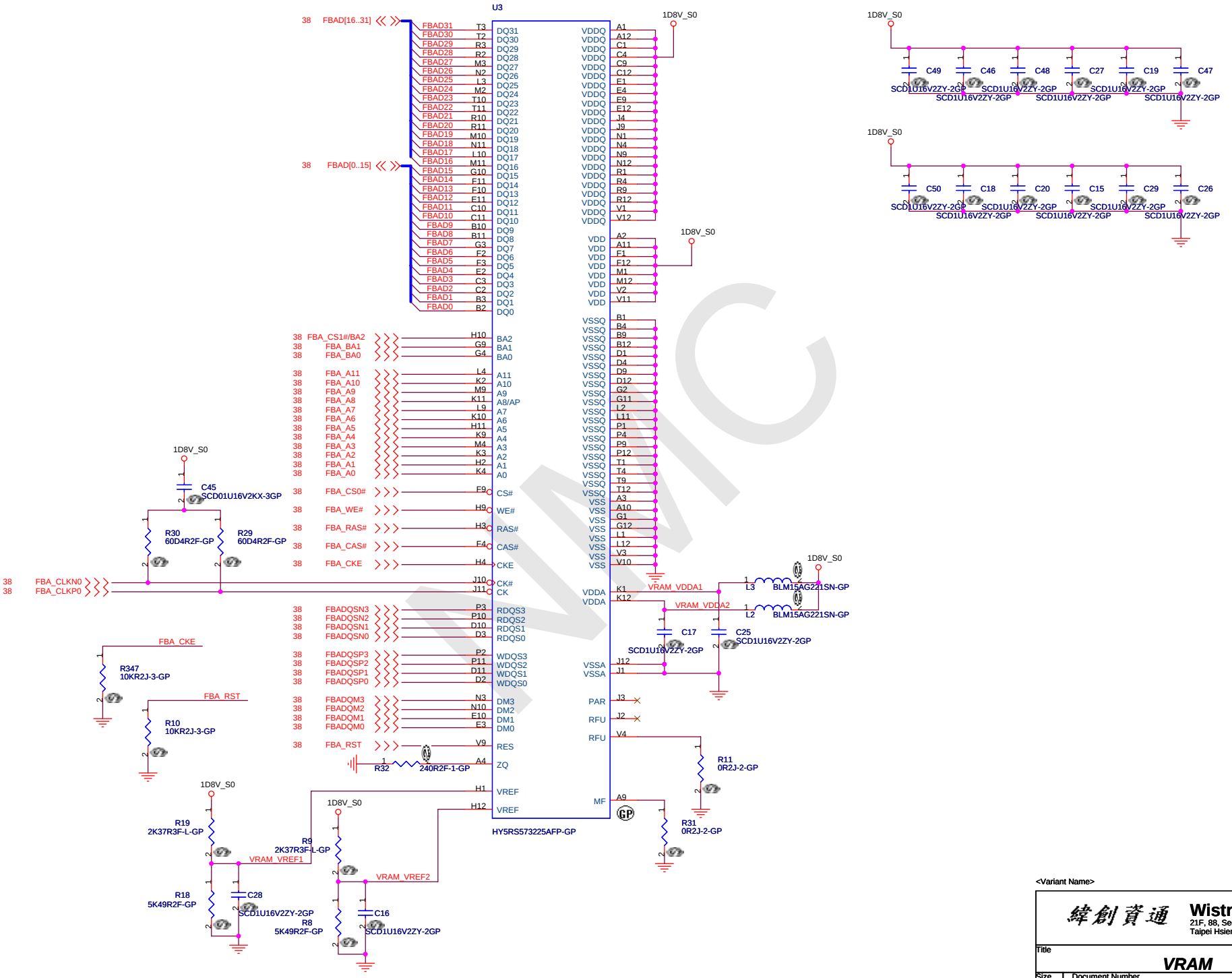
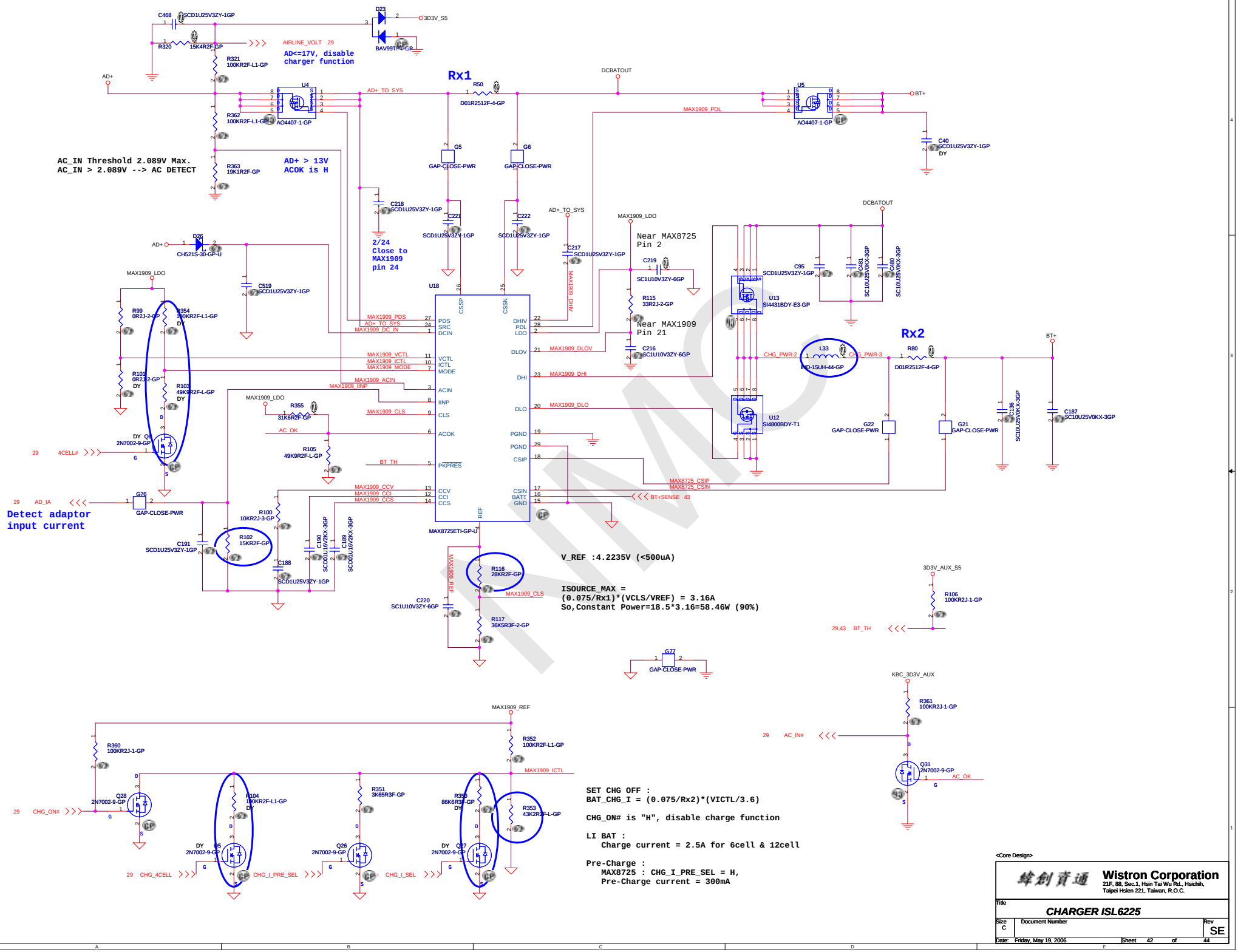


<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**VRAM**
Size A3	Document Number **KAI** Rev **SD**
Date: Wednesday, April 19, 2006	Sheet 41 of 44


AC_IN Threshold 2.089V Max.
AC_IN > 2.089V --> AC DETECT
AD+ > 13V
ACOK is H
AD<=17V, disable
charger function
Rx1
Rx2
2/24
Close to
MAX1909
pin 24
Near MAX8725
Pin 2
Near MAX1909
Pin 21
Detect adaptor
input current
V_REF :4.2235V (<500uA)
ISOURCE_MAX =
(0.075/Rx1)*(VCLS/VREF) = 3.16A
So,Constant Power=18.5*3.16=58.46W (90%)
SET CHG OFF :
BAT_CHG_I = (0.075/Rx2)*(VICTL/3.6)
CHG_ON# is "H", disable charge function
LI BAT :
Charge current = 2.5A for 6cell & 12cell
Pre-Charge :
MAX8725 : CHG_I_PRE_SEL = H,
Pre-Charge current = 300mA
MAX8725ETI-GP-U
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CHARGER ISL6225
Size C
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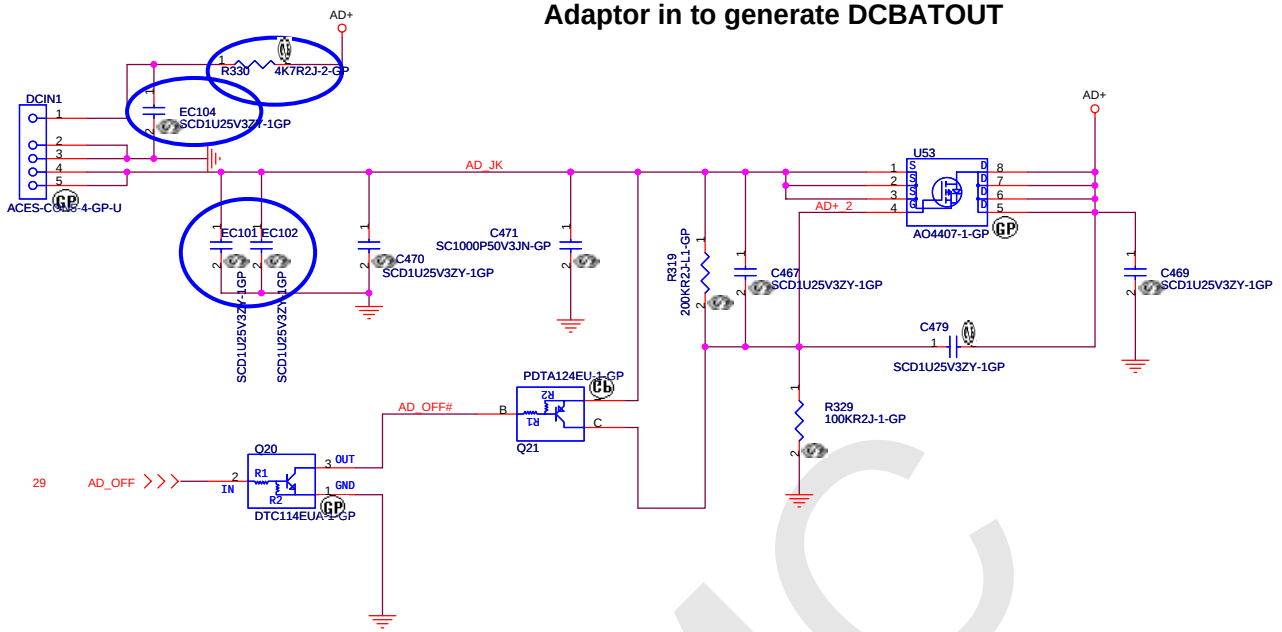
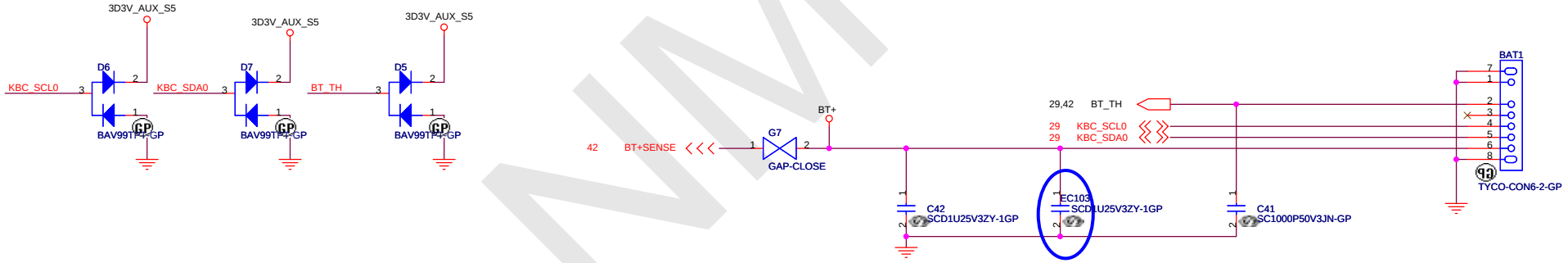
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AD/BATT CONN**

Size	Document Number	Rev
A3		SE

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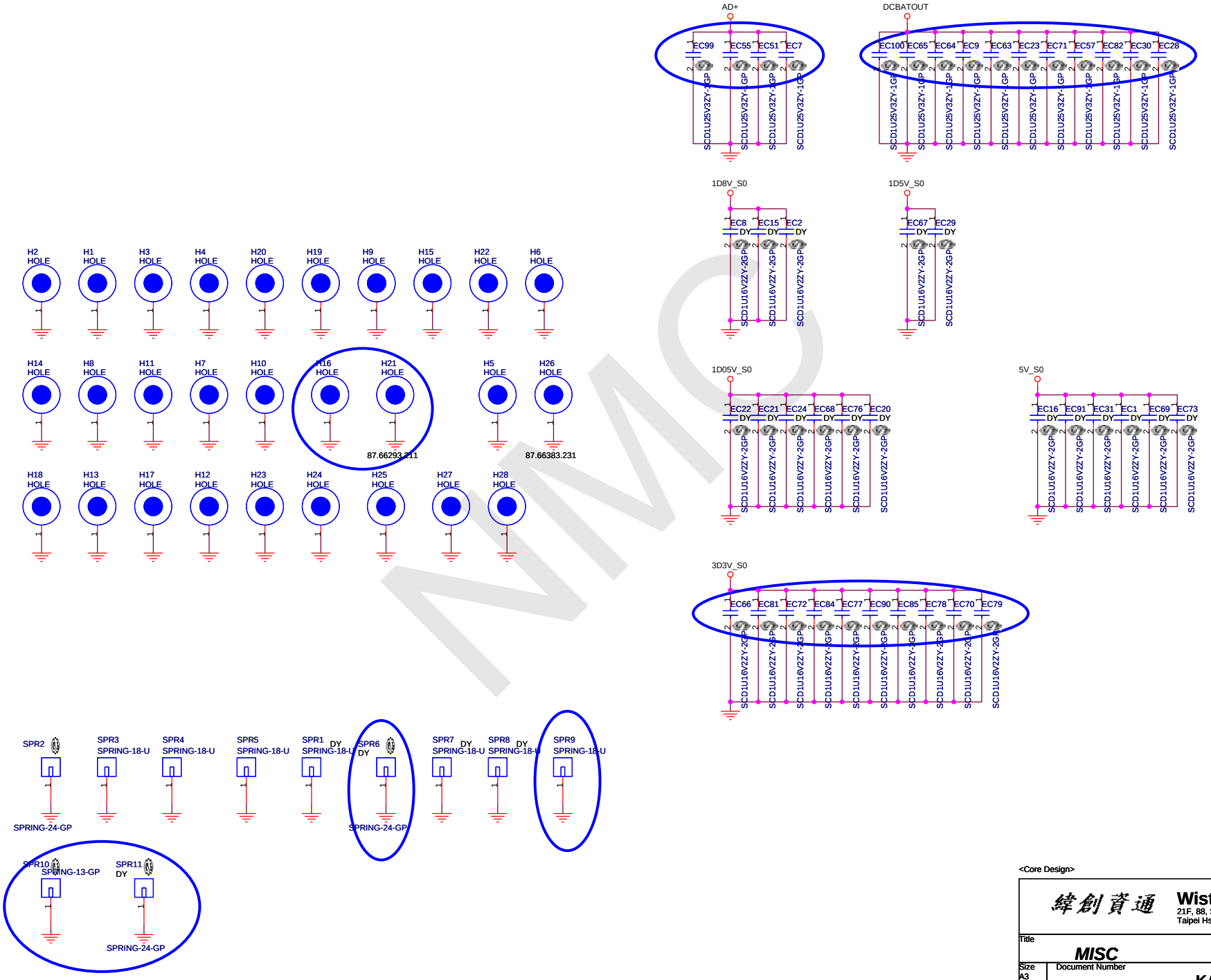

<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***MISC***

Size	Document Number	Rev
A3	KAI	SE

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