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Compal Confidential

NIWE2

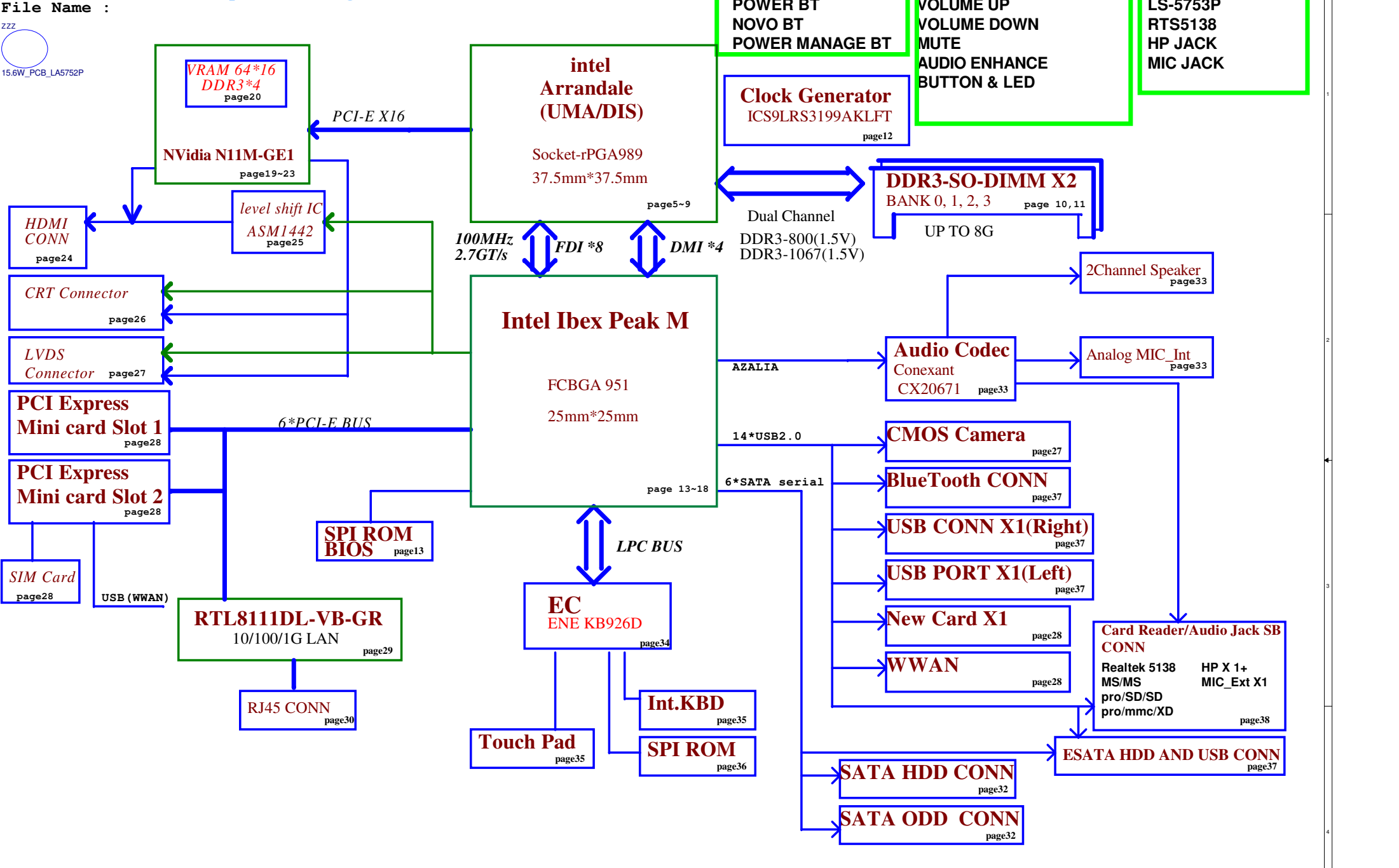
Schematics Document

Arrandale

with Intel IBEX PEAK-M core logic

REV:0.3

Security Classification	Compal Secret Data			Compal Electronics,Ltd.		
Issued Date	2008/03/25	Deciphered Date	2008/04/	Title Cover Sheet		
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				Date: Thursday, October 29, 2009Sheet 1 of 51		



power plane	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +1.8VS +0.75VS +1.05VS
				State
S0	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	○	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

	SOURCE	RAM M2	BATT	KE926	SODIMM	CLK CHIP	WLAN WWAN	N10x Thermal Sensor	N10x	Cap sensor board	NEW CARD	PCH
SMB_EC_CK1 SMB_EC_DA1	KB926 +3VALW	✗	V +3VALW	✗	✗	✗	✗	✗	✗	✗	✗	✗
SMB_EC_CK2 SMB_EC_DA2	KB926 +3VALW	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	V +3VALW
SMBCLK SMBDATA	PCH +3VALW	V +3VALW	✗	✗	V +3VS	V +3VS	✗	✗	✗	✗	V +3VS	✗
SML0CLK SML0DATA	PCH +3VALW	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗
SML1CLK SML1DATA	PCH +3VALW	✗	✗	V +3VALW	✗	✗	✗	V +3VS	✗	V +3VS	✗	✗

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

@ FUNCTION

	EVT	NON-USE
45@	(45 BOM)	
100@	10/100 LAN	
GIGA@	GIGA LAN	
UMA HDMI@	FOR UMA HDMI components	
HDMI@	FOR HDMI components	
3G@	3G(WWAN) function	
X76@	(X76 BOM)	
ESATA@	ESATA function	
CMOS@	Camera function	
BT@	Blue Tooth	
10M@	FOR 10M CHIP	
11M@	FOR 11M CHIP	
UMA@	UMA only (Arranddale)	
DIS@	DIS only (Arranddale)	
VGA@	FOR NVIDIA PART	
HYBRID@	FOR SWITCHABLE	
HU@	SWITCHABLE or UMA only	
HD@	SWITCHABLE or DIS only	

SKU

Arrandale (dGPU) DIS only	DIS@ / 100@ for EVT
Arrandale (iGPU) UMA only	UMA@ / 100@ for EVT
Arrandale (iGPU+dGPU) SWITCHABLE	VGA@+HD@+HU@+HYBRID@

PCIE PORT LIST	
PORT	DEVICE
1	
2	WLAN
3	LAN
4	3G
5	NEW CARD
6	
7	
8	

USB PORT LIST	
PORT	DEVICE
0	RIGHT SIDE
1	LEFT SIDE
2	CMOS
3	LEFT SIDE
4	RIGHT SIDE
5	CARD READER
6	
7	
8	WIRELESS
9	
10	NEW CARD
11	BT
12	
13	3G

GPIO	I/O	ACTIVE	Function Description
GPIO0	N/A	N/A	
GPIO1	IN	-	Hot plug detect for IFP link C
GPIO2	OUT	H	Panel Back-Light brightness(PWM capable)
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light On/Off (PWM)
GPIO5	OUT	-	GPU VID0
GPIO6	OUT	-	GPU VID1
GPIO7	OUT	-	GPU VID2
GPIO8	I/O	L	Thermal Catastrophic Overtemp
GPIO9	OUT	L	Thermal Alert
GPIO10	OUT		Memory VREF switch
GPIO11	I/O	L	SLI raster sync
GPIO12	IN	-	AC power detect pin
GPIO13	OUT	-	MEM_VID orPower supply control
GPIO14	OUT	-	Power supply control
GPIO15	IN	-	Hot plug detect for IFP Link E
GPIO16	OUT	-	Programmable Fan Control
GPIO17	IN	-	
GPIO18	IN	-	
GPIO19	IN	-	Hot plug detect for IFP Link D
GPIO20	IN	-	
GPIO21	IN	-	Hot plug detect for IFP link F
GPIO22	IN	-	SLI swap ready signal
GPIO23	I/O		

GPIO6 GPIO5 N10M-GS N10P-GS

GPU_VID1	GPU_VID0	VGA_CORE	P-State
0	0	0.8V	12
0	1	0.85V	12
1	0	0.9V	0, 10
1	1	1.0V (N10M-GS) 0.925V (N10P-GS)	

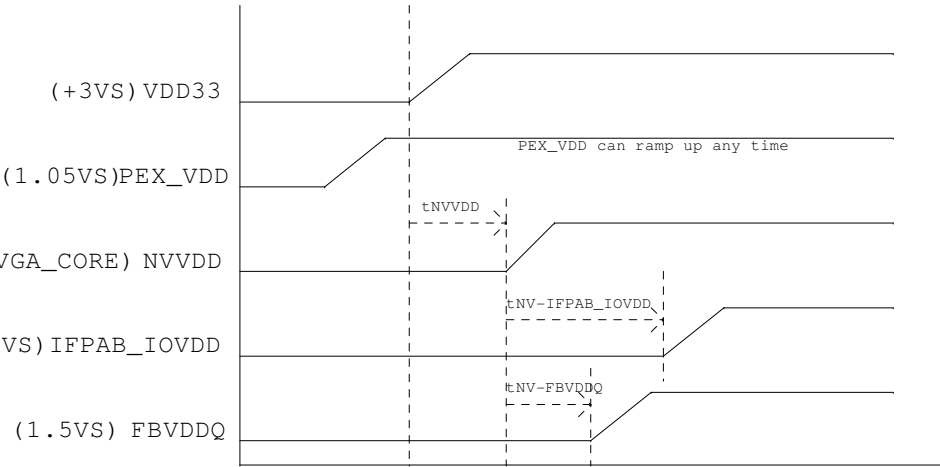
Products	GPU (4) (W)	Mem (1,5) (W)	NVCLK /MCLK (MHz)	NVVDD (V) (A) (W)			FBVDD (1.5V) (A) (W)		FBVDDQ (GPU+Mem) (1.5V) (A) (W)		PCI Express (1.05V) (6) (mA) (W)		I/O and PLLVDD (1.8V) (mA) (W)		I/O and PLLVDD (1.05V) (mA) (W)		Other (3.3V) (mA) (W)	
N10P-GS 128bit 1024MB DDR3	21.07	6.67	TBD	TBD	18.25	17.34	2.06	3.09	4.09	6.14	850	0.89	75	0.14	63	0.07	55	0.18
N10P-GE 128bit 1024MB DDR3	20.97	6.73	TBD	TBD	19.17	17.25	2.03	3.05	4.09	6.14	840	0.88	75	0.14	63	0.07	55	0.18
N10P-LP 128bit 1024MB DDR3	15.48	6.44	TBD	TBD	13.95	11.86	1.90	2.85	3.99	5.99	810	0.85	75	0.14	63	0.07	55	0.18

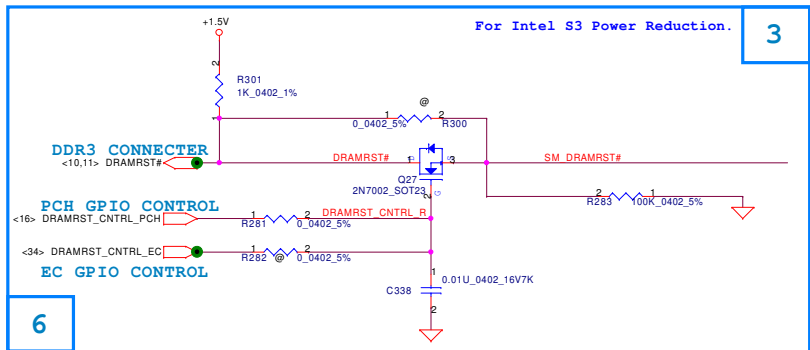
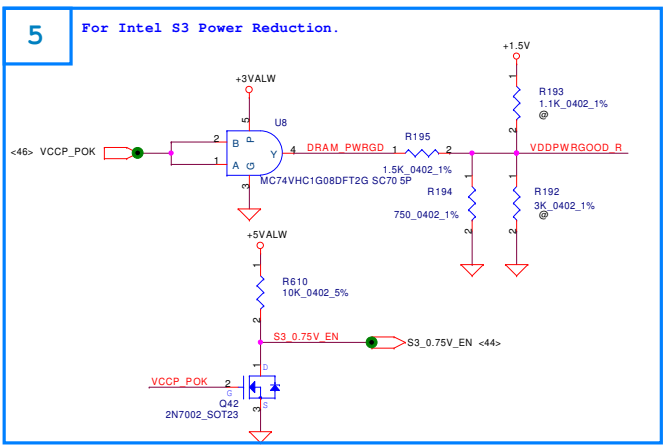
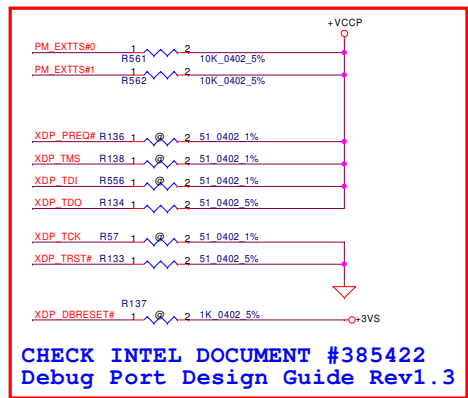
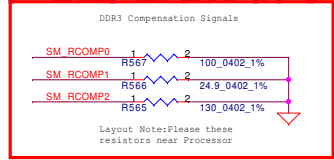
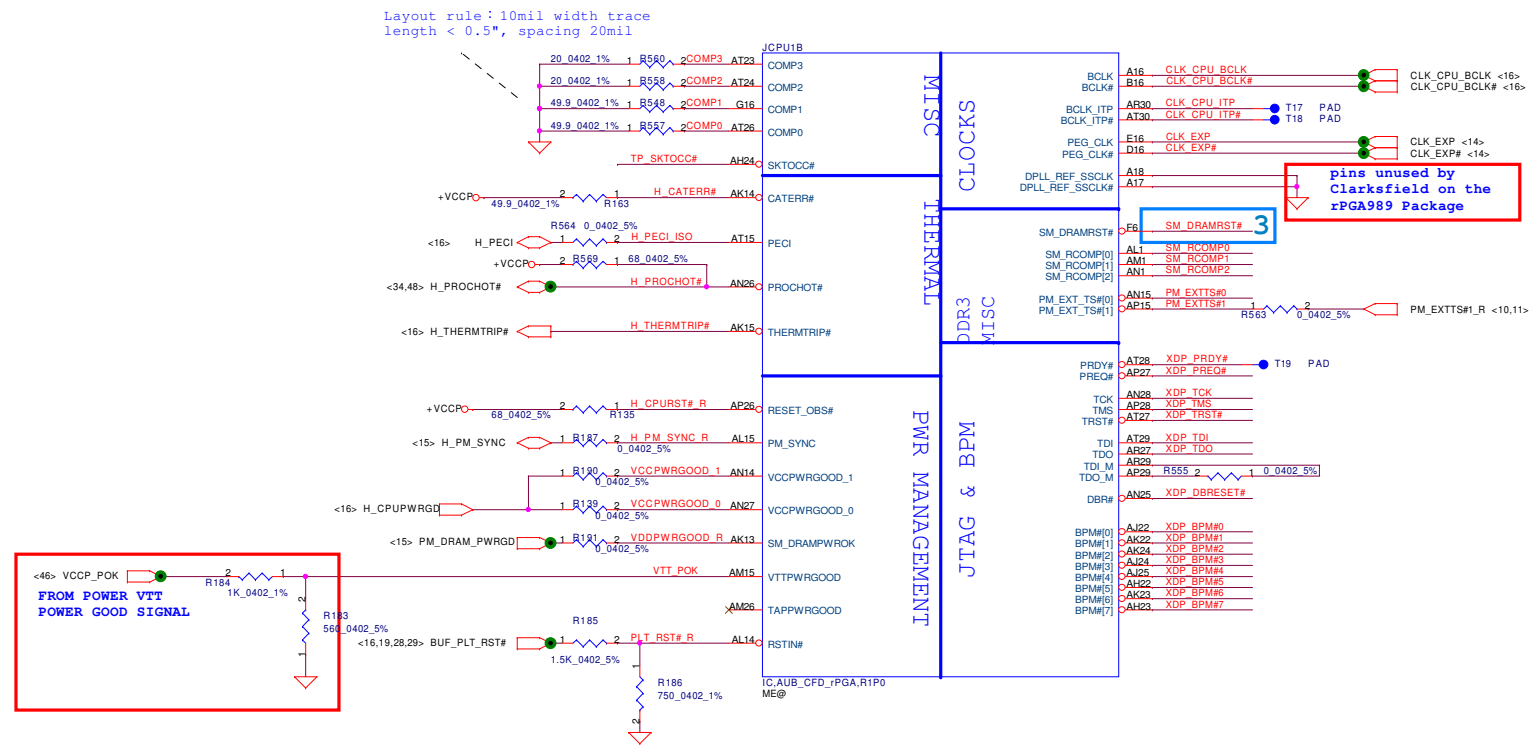
Performance Mode P0 TDP at Tj = 102 C* (DDR3)

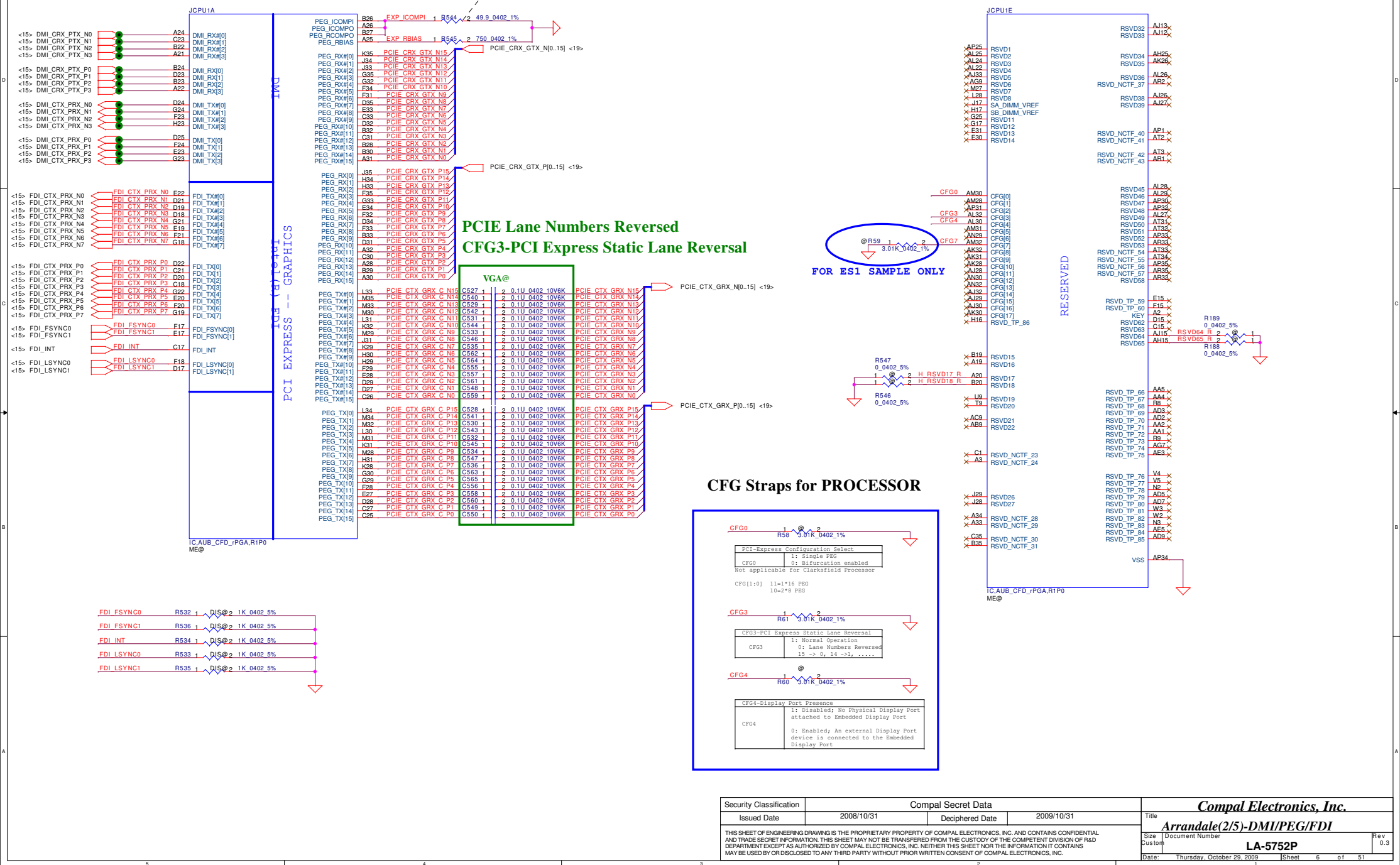
Products	GPU (4) (W)	Mem (1,5) (W)	NVCLK /MCLK (MHz)	NVVDD (V) (A) (W)			FBVDD (1.5V) (A) (W)		FBVDDQ (GPU+Mem) (1.5V) (A) (W)		PCI Express (1.05V) (6) (mA) (W)		I/O and PLLVDD (1.8V) (mA) (W)		I/O and PLLVDD (1.05V) (mA) (W)		Other (3.3V) (mA) (W)	
N10M-GE 64bit 512MB DDR3	13.36	2.93	TBD	TBD	11.89	10.70	0.66	0.99	2.16	3.24	792	0.83	75	0.14	63	0.07	100	0.33
N10M-GS 64bit 512MB DDR3	14.29	3.10	TBD	TBD	11.53	11.53	0.70	1.05	2.28	3.42	817	0.86	75	0.14	63	0.07	100	0.33
N10M-LP 64bit 512MB DDR3	8.28	2.91	TBD	TBD	6.60	5.61	0.62	0.93	2.20	3.3	782	0.82	75	0.14	63	0.07	100	0.33

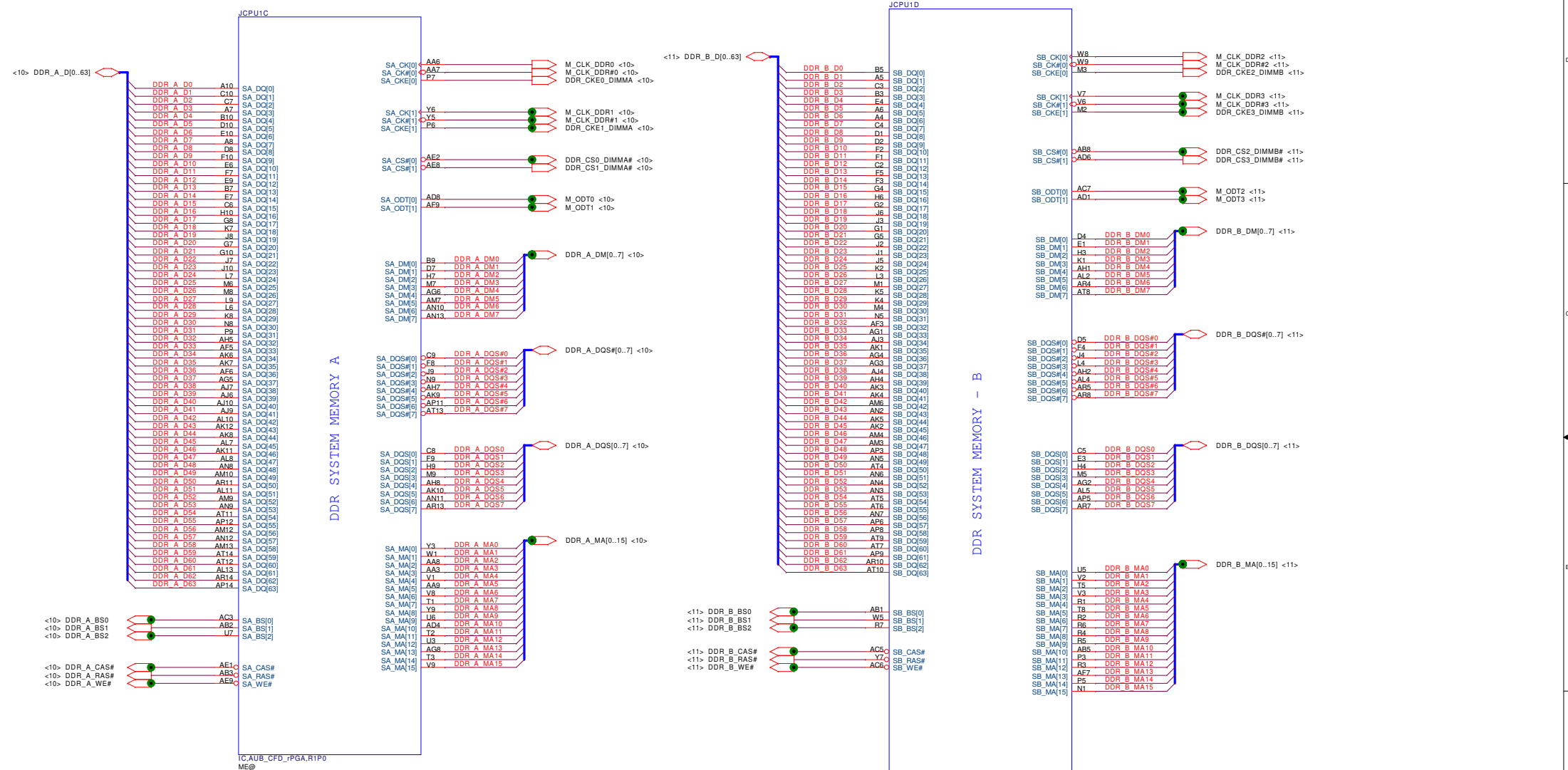
Power Sequence

The ramp time for any rail must be more than 40us

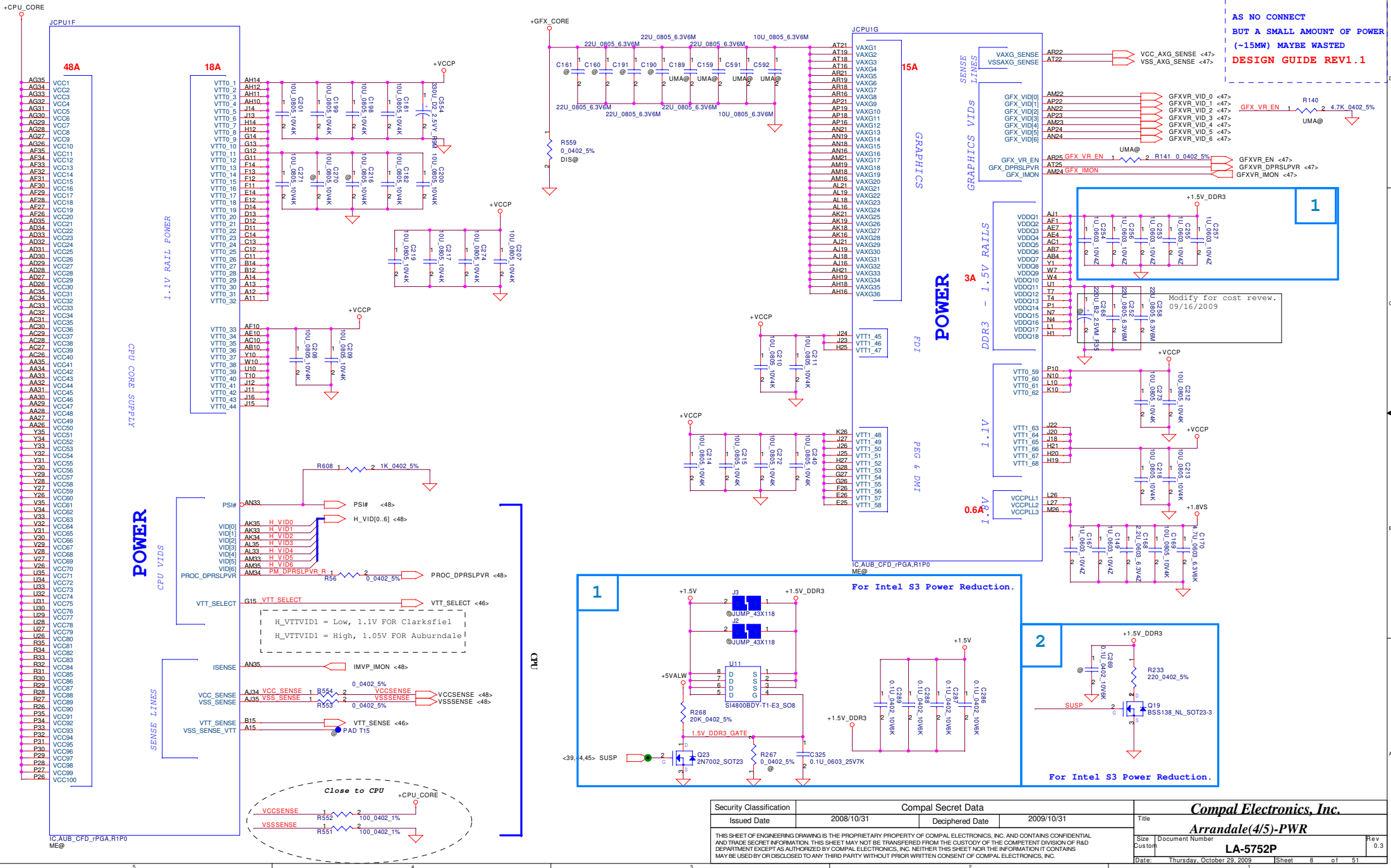




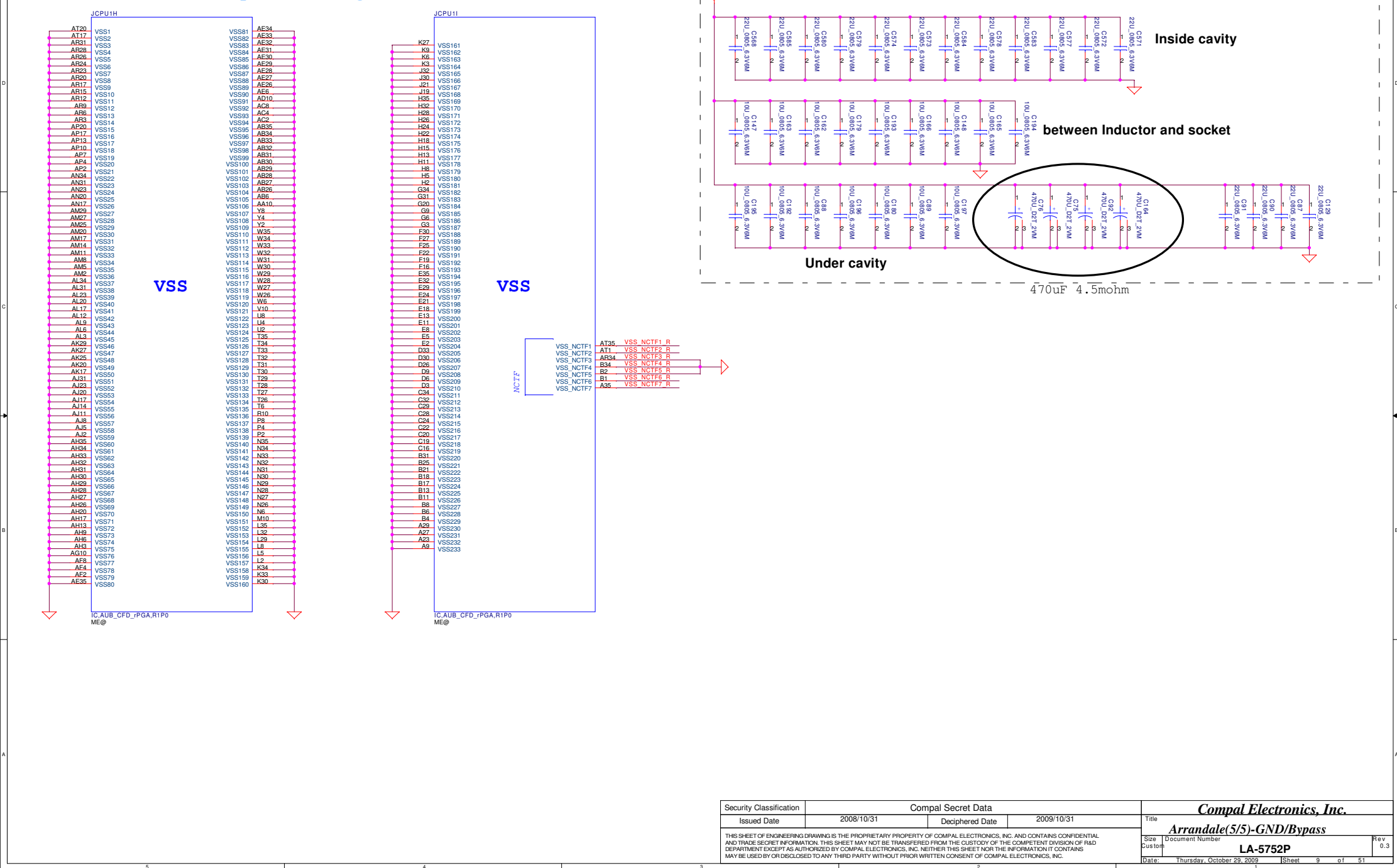


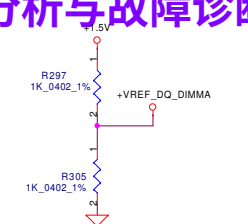
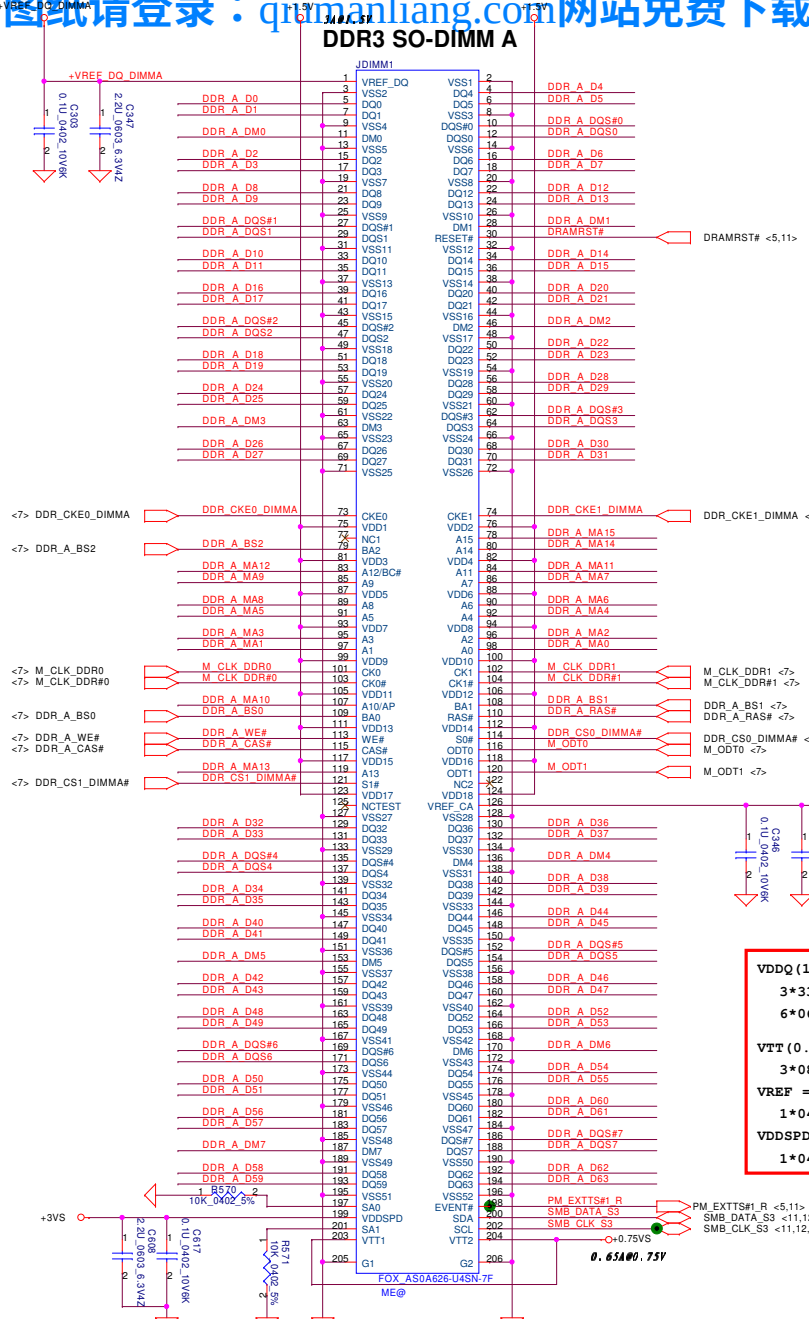


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Issued Date	2008/10/31	Deciphered Date	2009/10/31	Arrandale(3/5)-DDR III	
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Issued Date		Deciphered Date		Arrandale(4/5)-PWR	
2008/10/31		2009/10/31		LA-5752P	
Size		Document Number		Rev	
Custion		LA-5752P		0.3	
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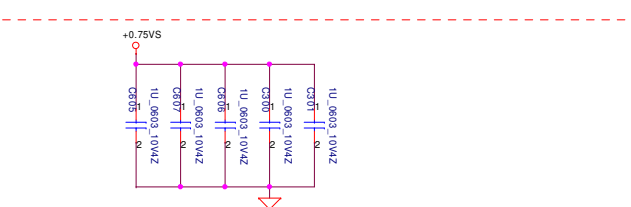
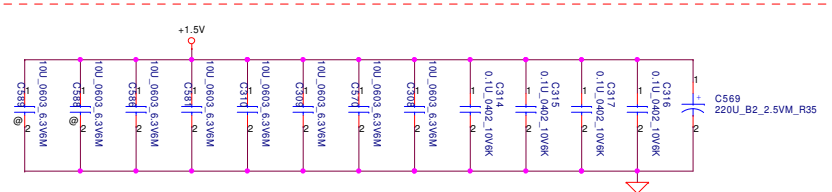




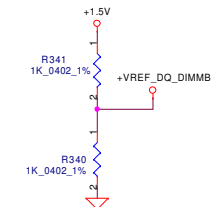
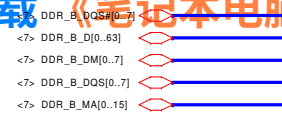
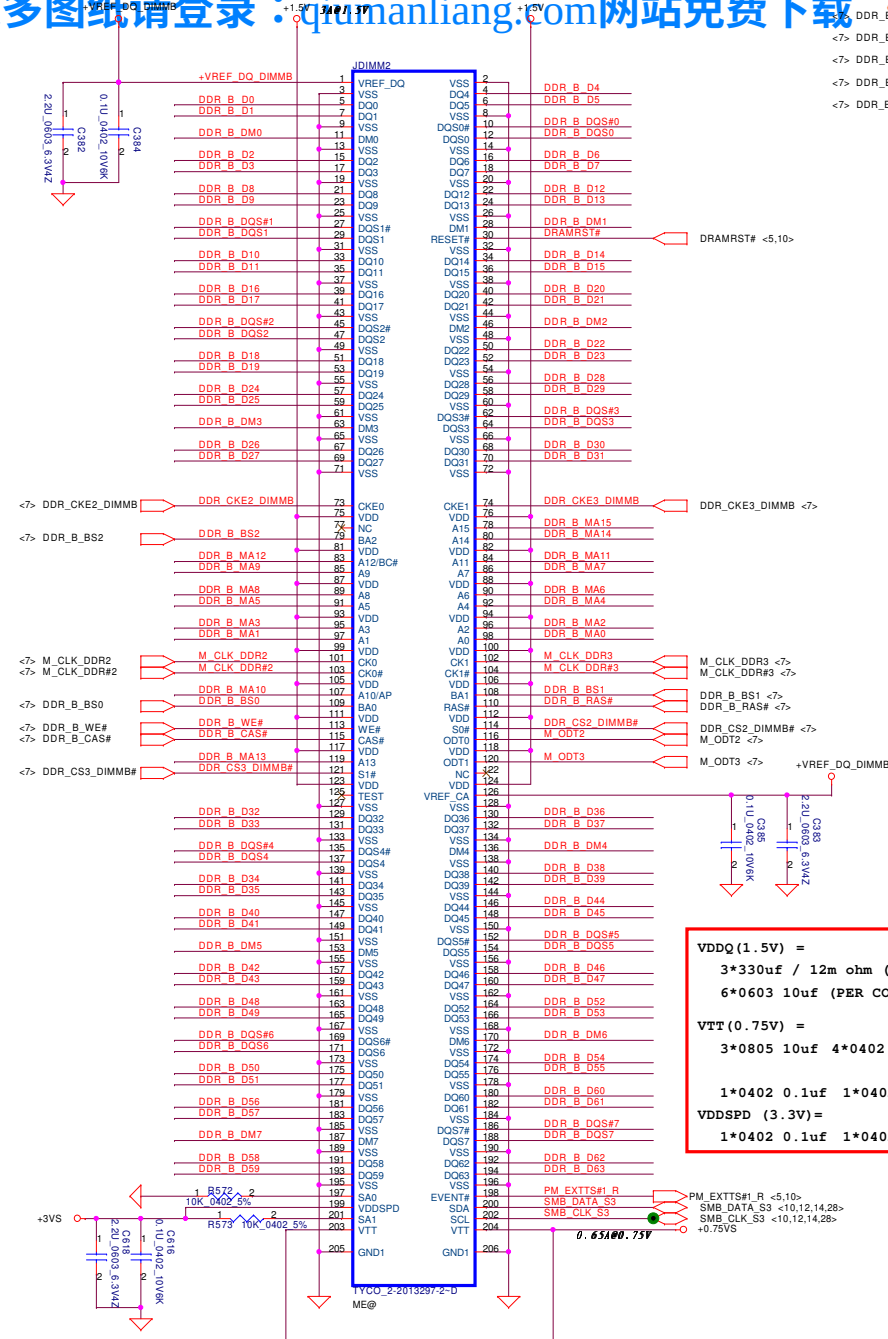
For Arranale only +VREF_DQ_DIMMA supply from a external 1.5V voltage divide circuit.
07/17/2009

Layout Note:
Place near DIMM

VDDQ(1.5V) =
3*330uf / 12m ohm (TOTAL FOR 2 SO-DIMMs)
6*0603 10uf (PER CONNECTOR)
VTT(0.75V) =
3*0805 10uf 4*0402 1uf
VREF =
1*0402 0.1uf 1*0402 2.2uf
VDDSPD (3.3V) =
1*0402 0.1uf 1*0402 2.2uf



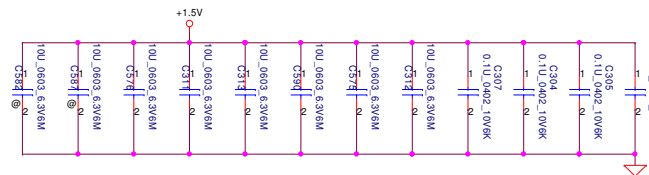
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Issued Date		Deciphered Date		Title	
2008/10/31		2009/10/31		DDRIII-SODIMM SLOT1	
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For Arranale only +VREF_DQ_DIMMB supply from a external 1.5V voltage divide circuit.

07/17/2009

Layout Note:
Place near DIMM

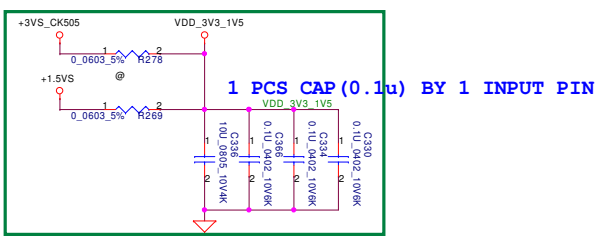


Layout Note:
Place near DIMM



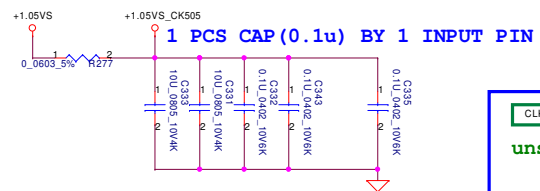
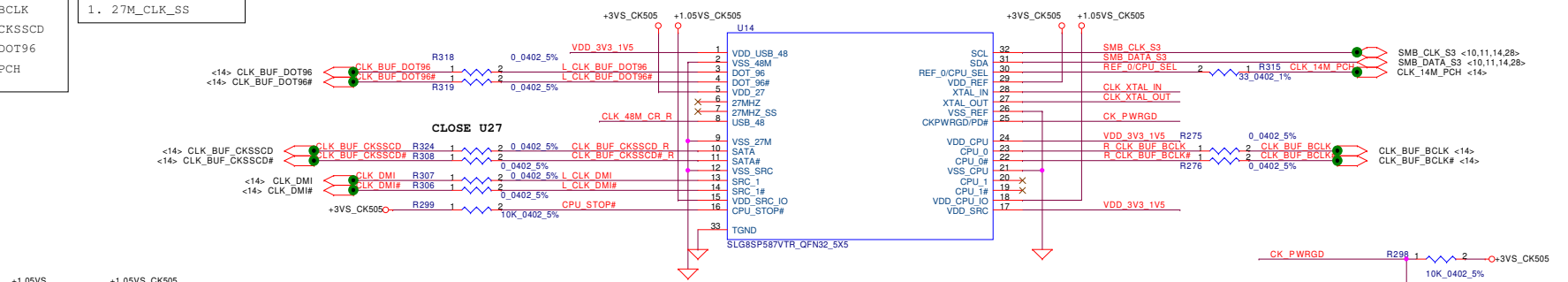
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Issued Date		2008/10/31	Deciphered Date	2009/10/31	Title		DDRIII-SODIMM SLOT2
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					LA-5752P		

Reserve for Low Power CLK GEN
RTM890N-632
SLG8LV597VTR



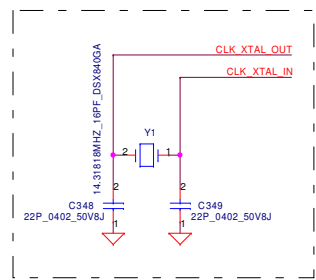
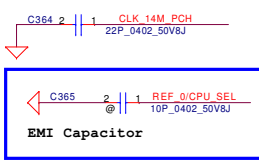
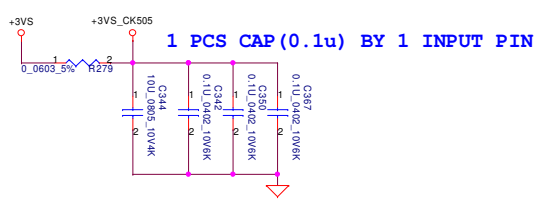
CLK GEN TO PCH
1. CLK_DMI
2. CLK_BUF_BCLK
3. CLK_BUF_CKSSCD
4. CLK_BUF_DOT96
5. CLK_14M_PCH

CLK GEN TO VGA
1. 27M_CLK
1. 27M_CLK_SS

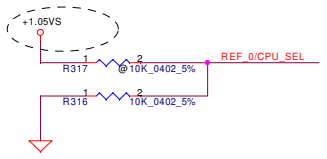


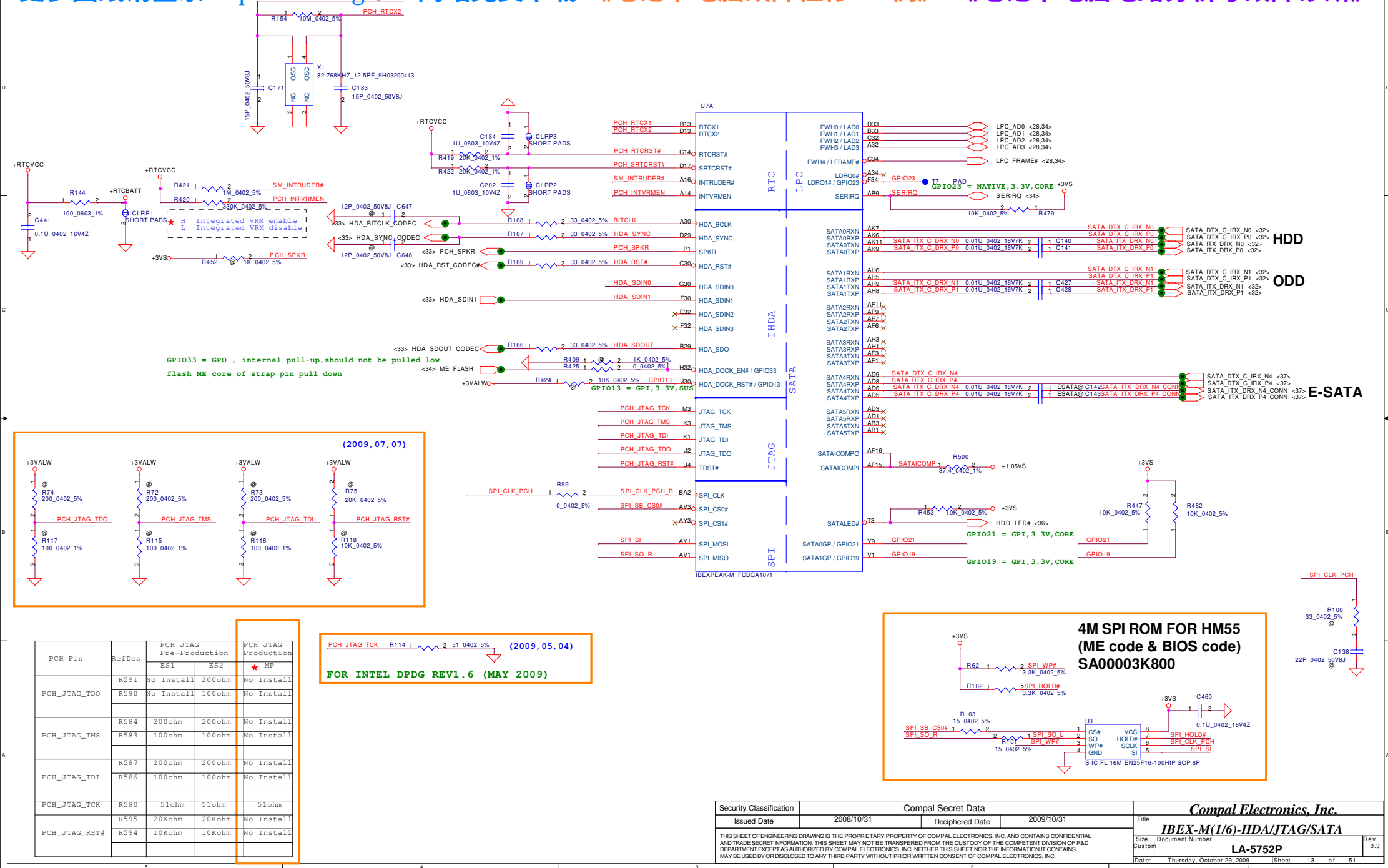
RTM890N-631-GRT QFN 32P CLK GEN (SA00003HQ00)
ICS9LV53199AKLFT MLF 32P CLK GEN (SA00003HR00)

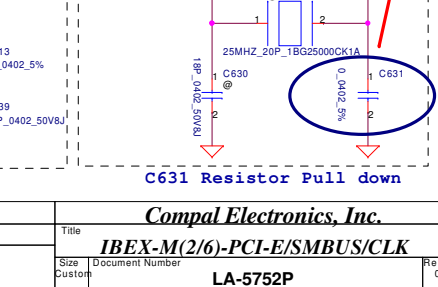
CLK_48M_CR
unstuff 09.09.08
PIN8 IS GND FOR ICS3197
PIN8 IS 48MHz FOR ICS3199



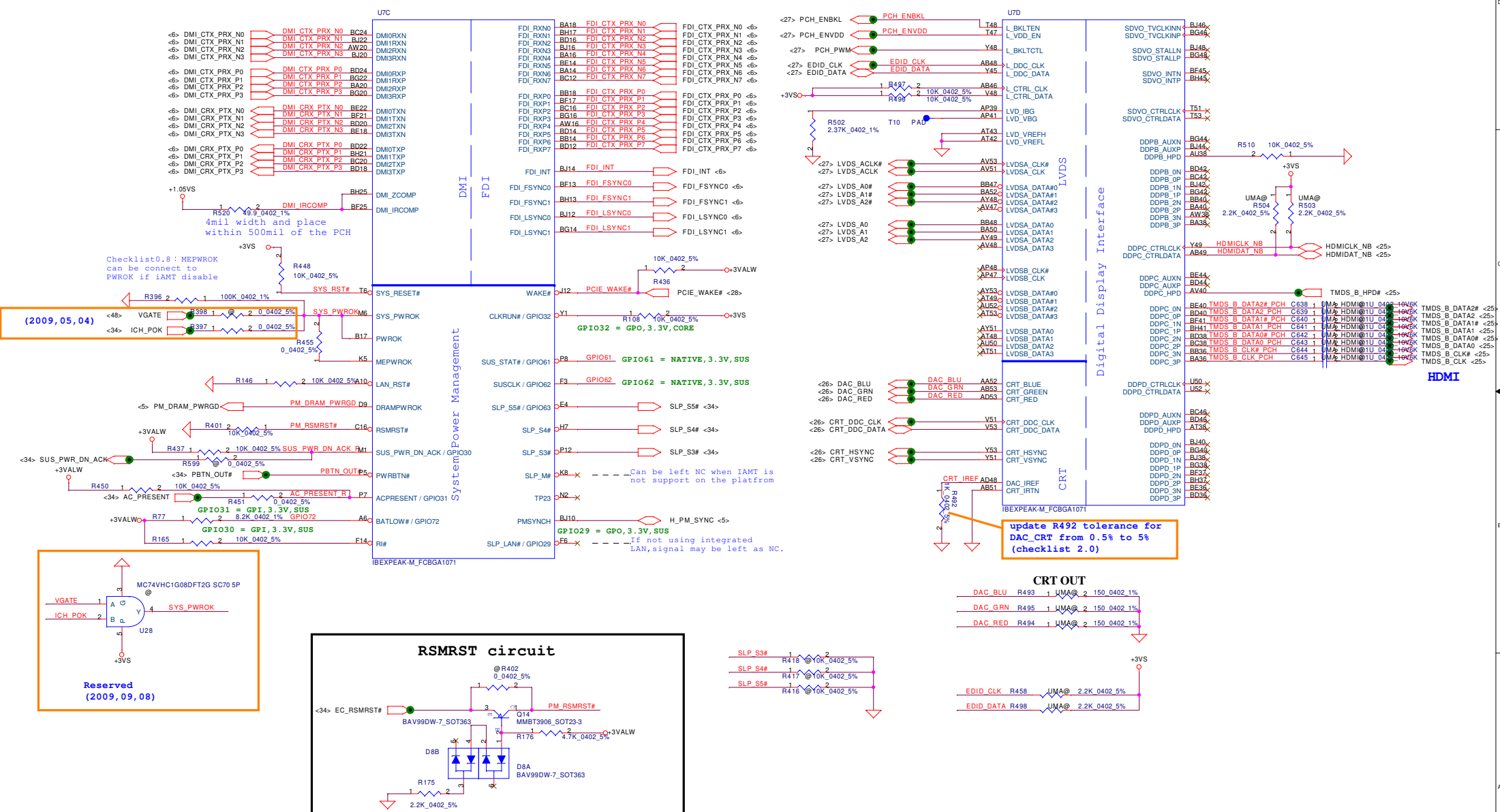
PIN	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

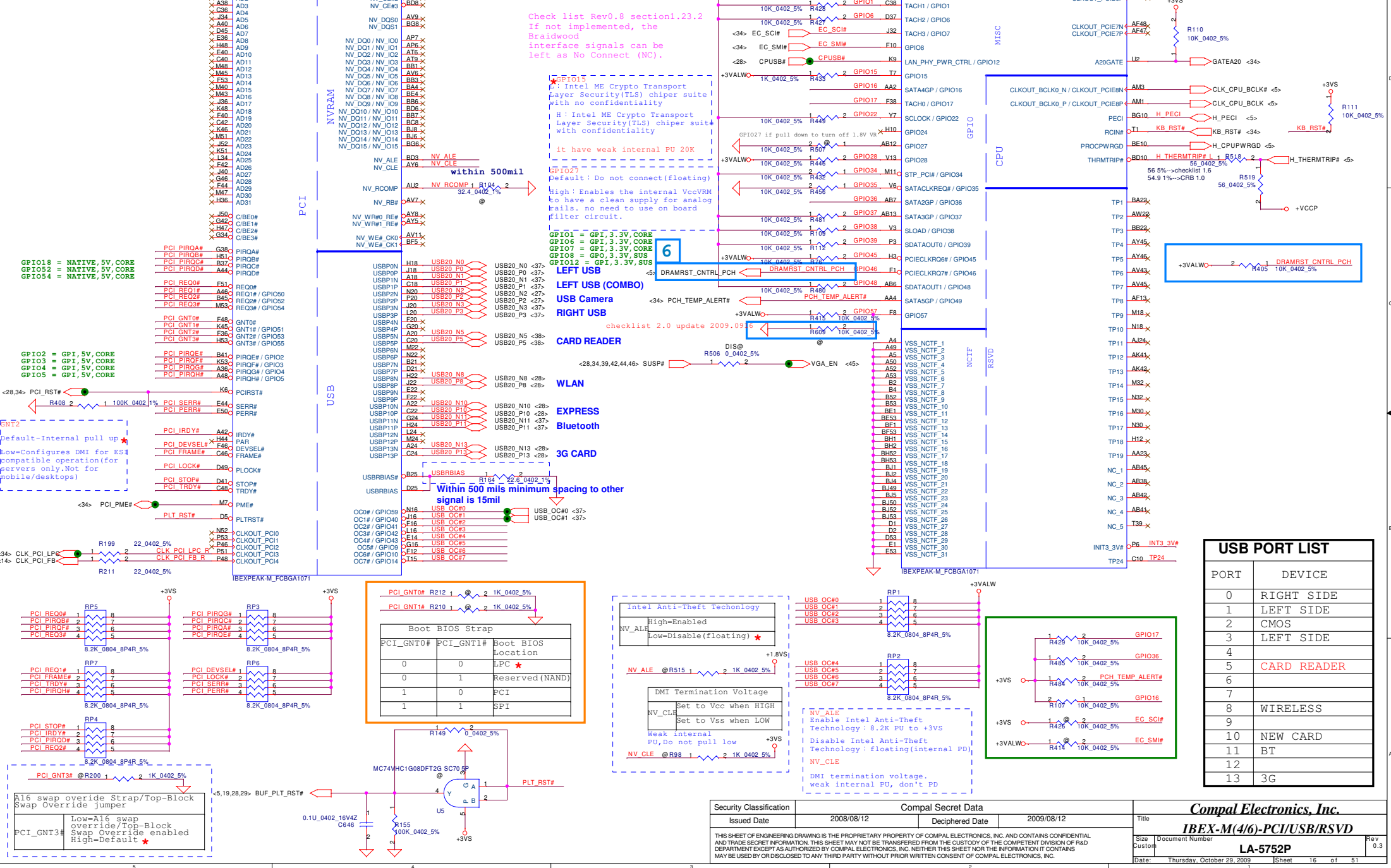


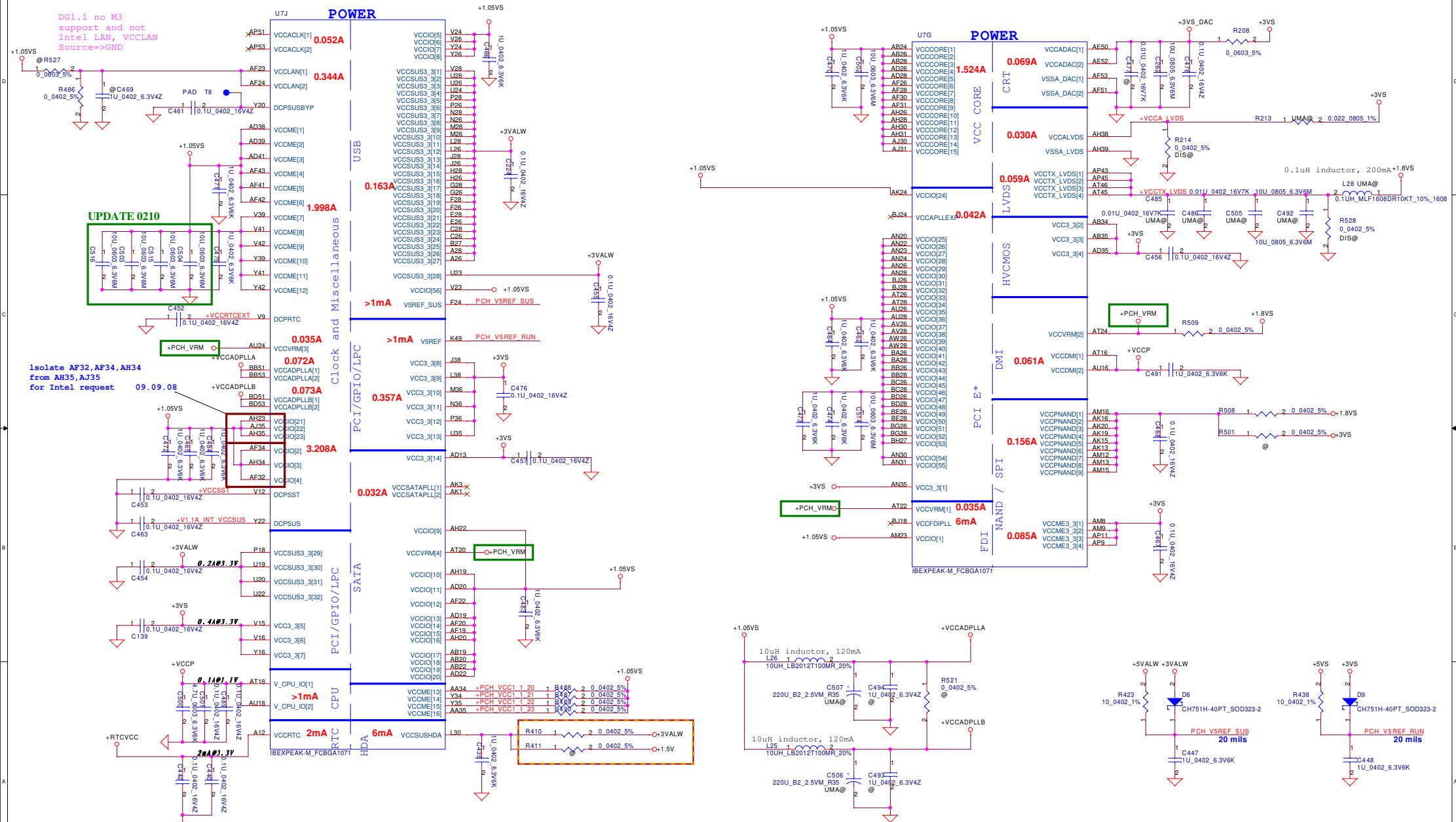




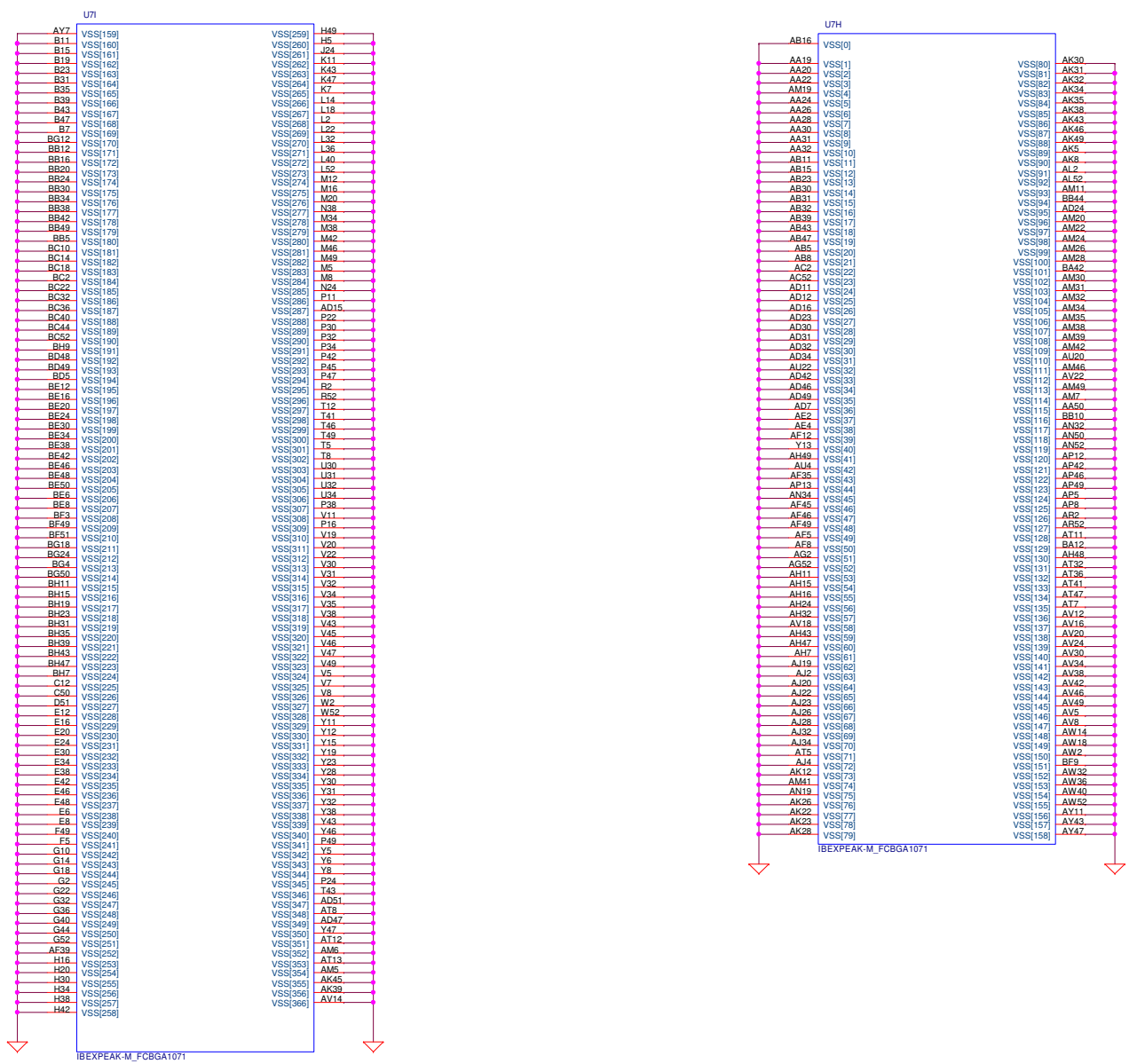
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		Date: Thursday, October 29, 2009		Sheet 14 of 51



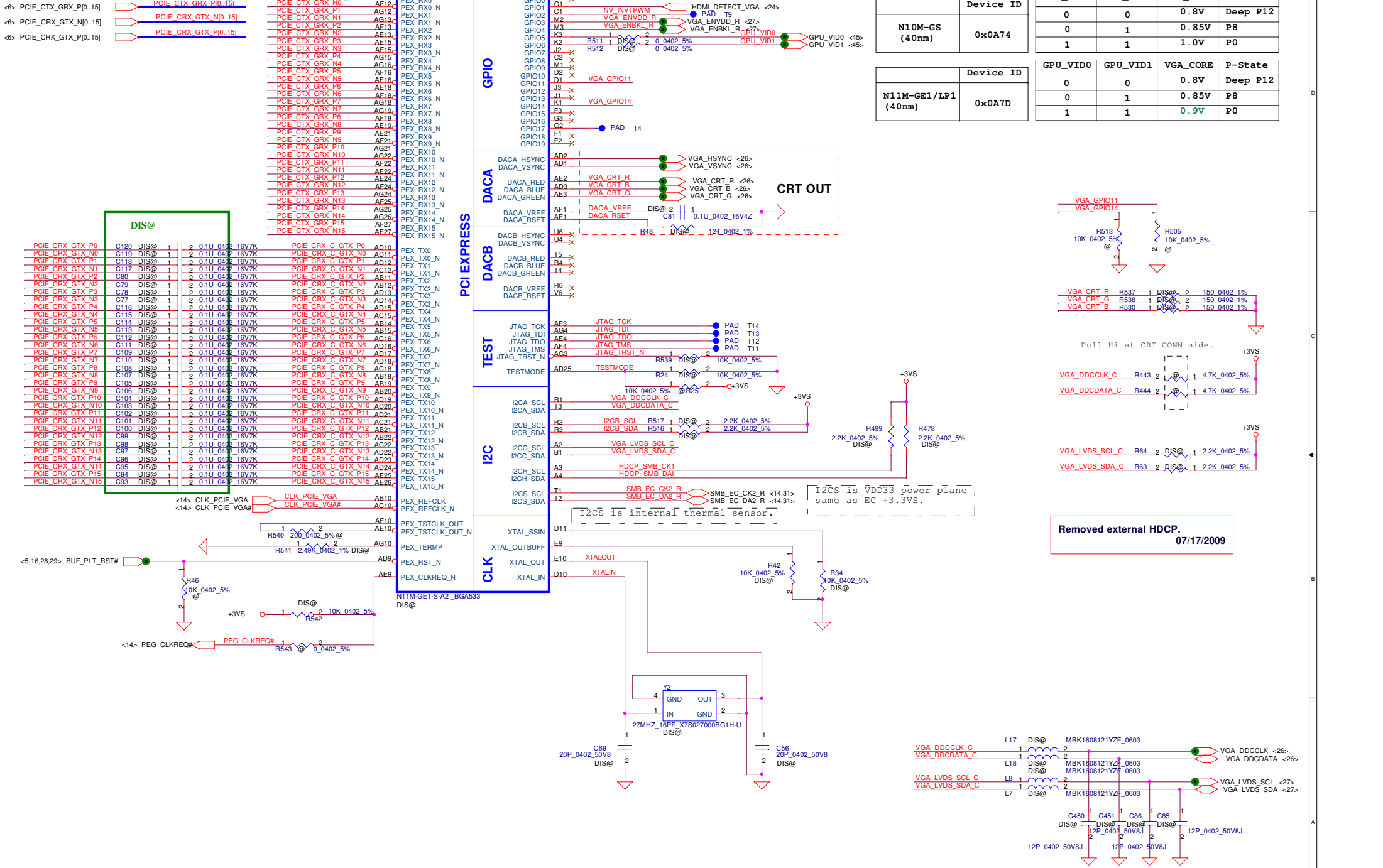


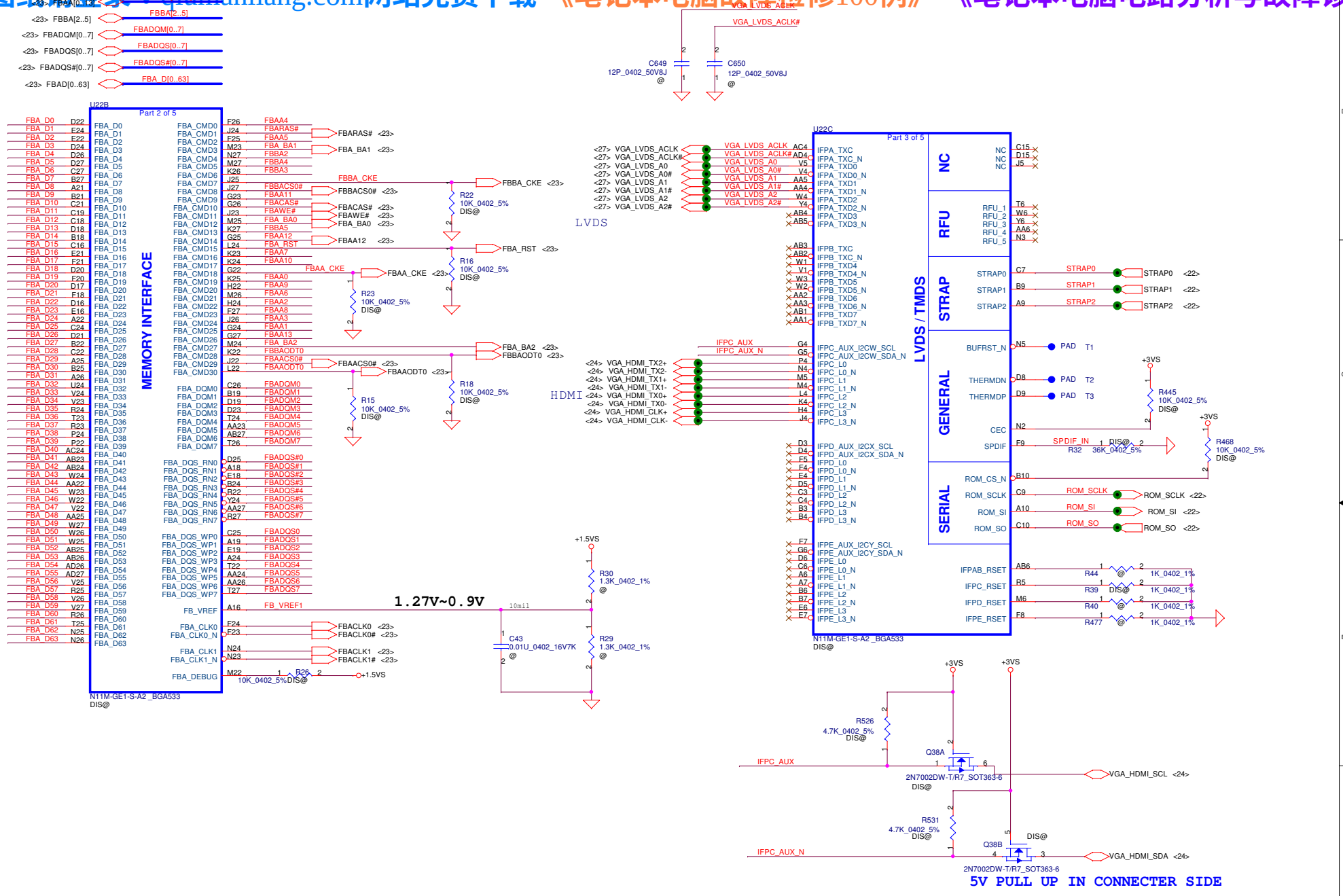


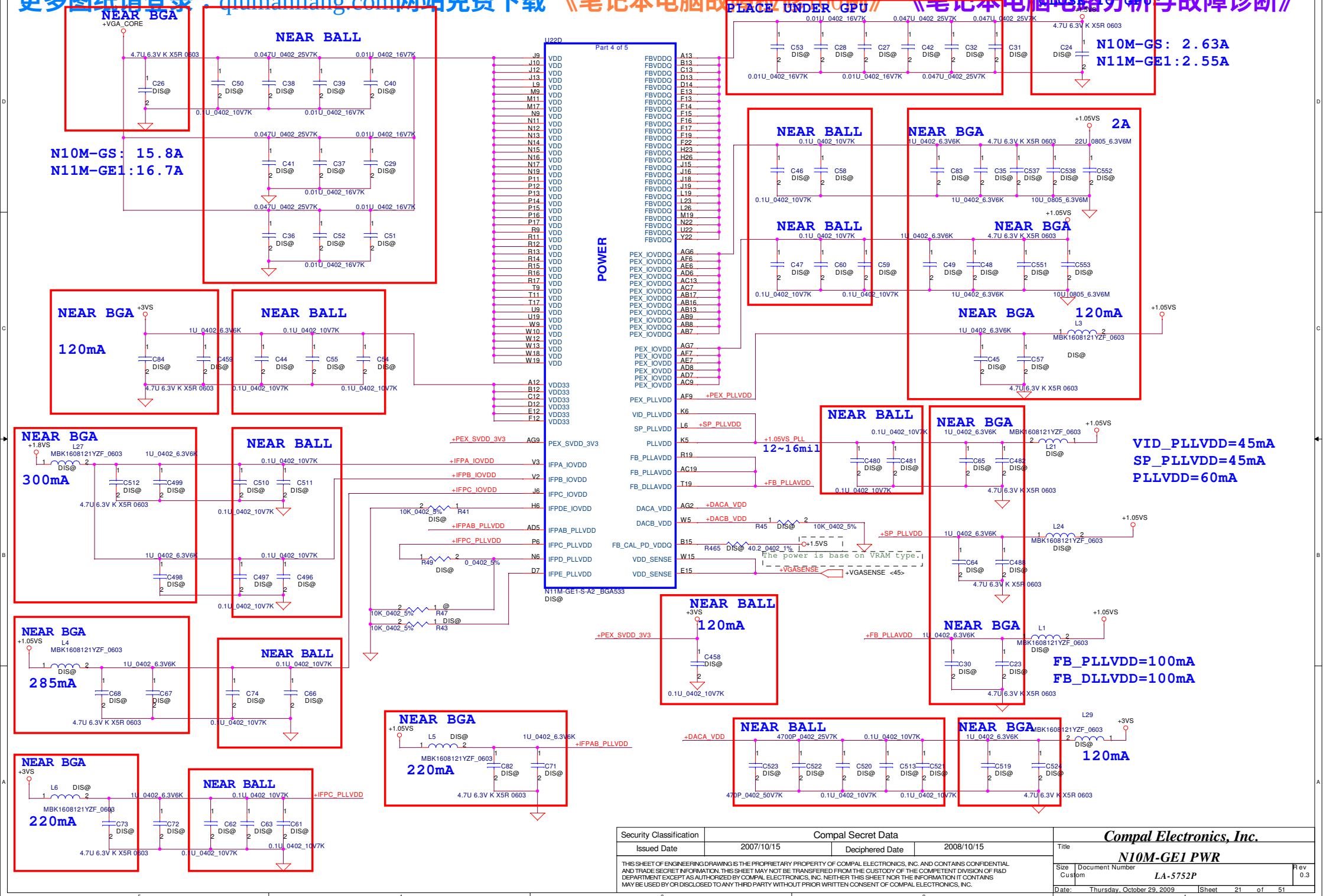
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Issued Date	2008/08/12	Deciphered Date	2009/08/12	IBEX-M(5/6)-PWR
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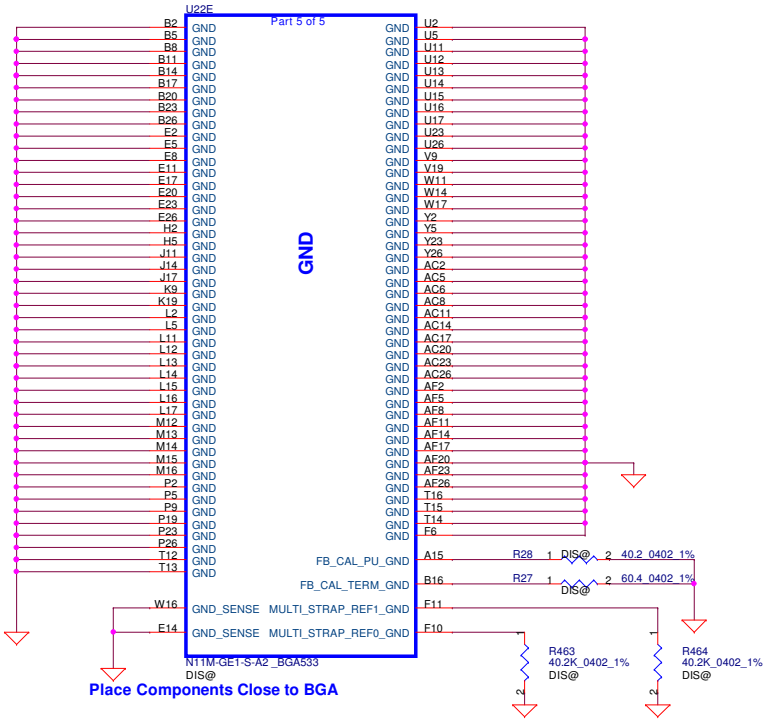
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Size		Document Number				Rev
Custome		LA-5752P				0.3
Date:		Thursday, October 29, 2009		Sheet	18	of 51







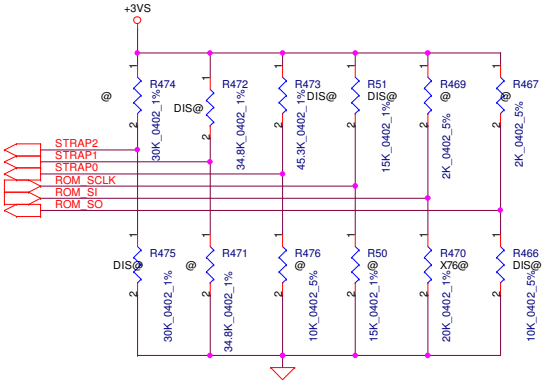
A total of 8 signals are required for GBL strapping (this includes:
2 reference signals
6 physical strapping pins
4 logical strapping bits
A total of 24 logical strapping bits are available



Place Components Close to BGA

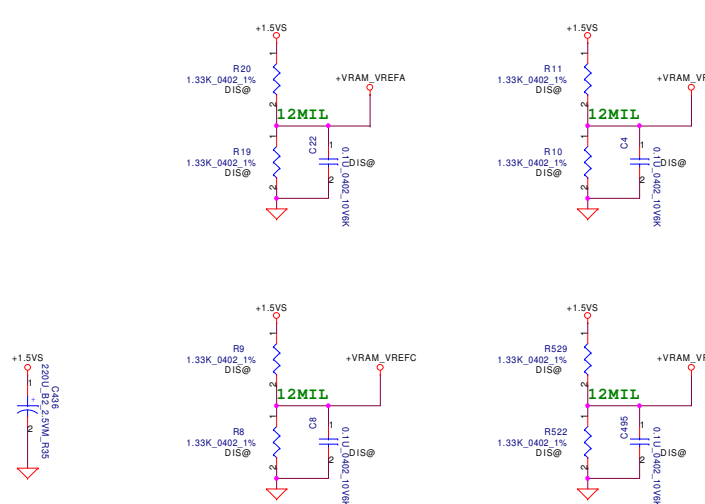
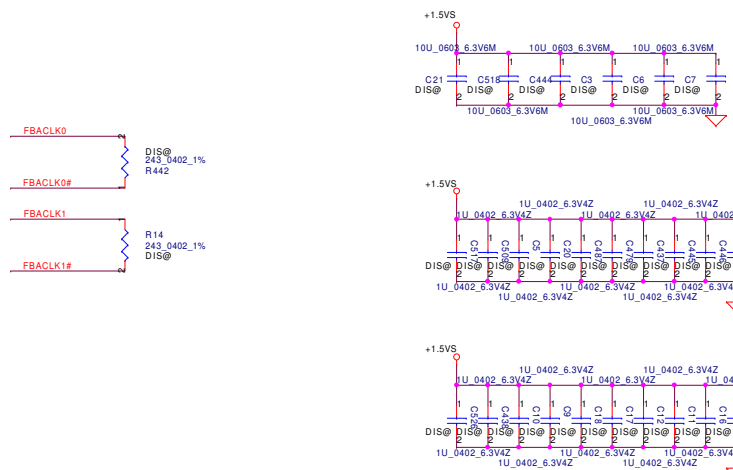
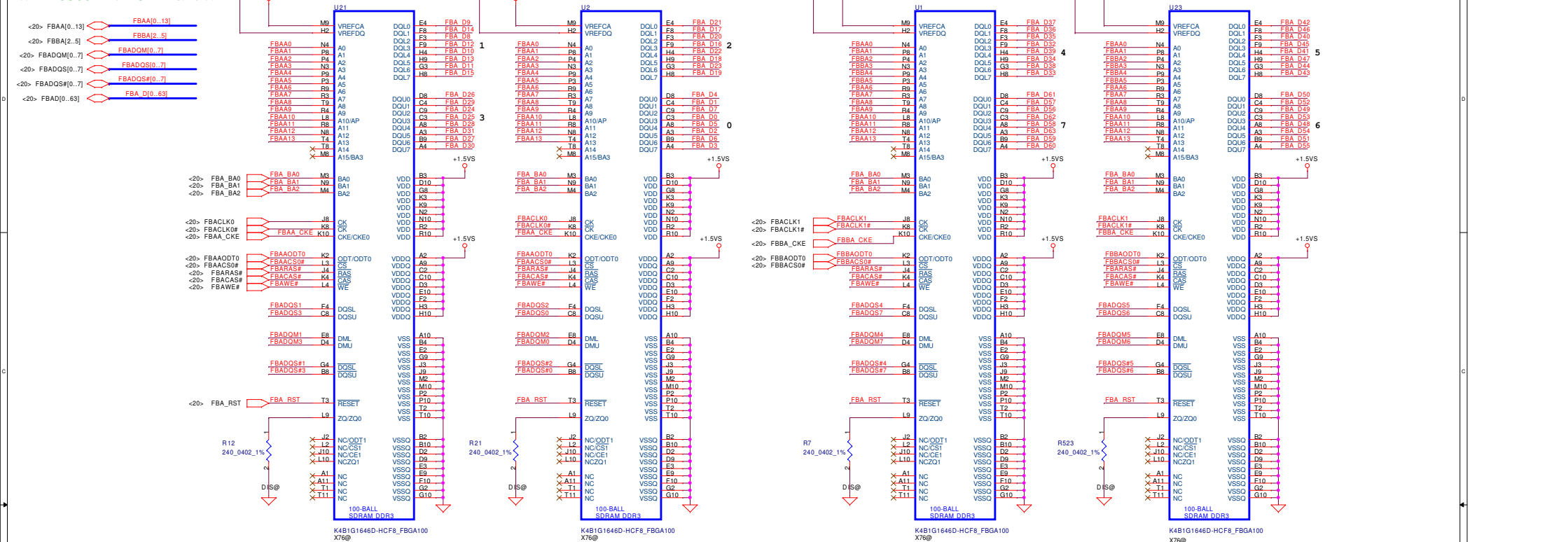
N11M-GE1 LP1	Memory/PKG	FBVDDQ	FB_CAL_PU_GND	FBCAL_PD_VDDQ	FBCAL_TERM_GND
	DDR3	+1.5VS	40.2 ohm	40.2 ohm	40.2/60.4 ohm

Must be used 1% resistor for driver calibration DG-04642-001-V01(May 22, 2009)

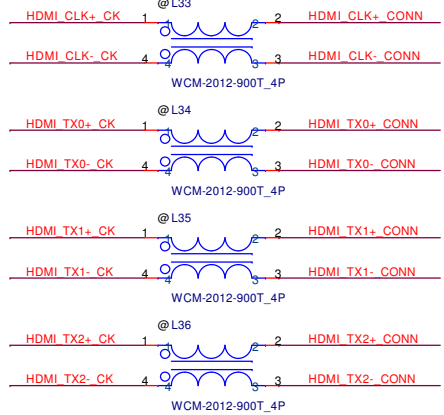
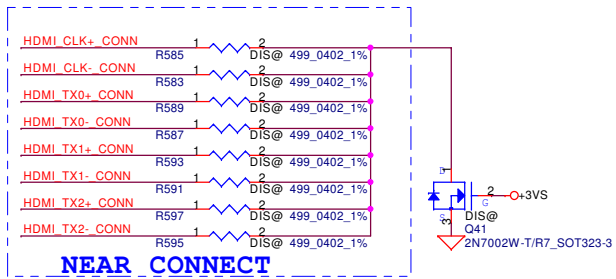
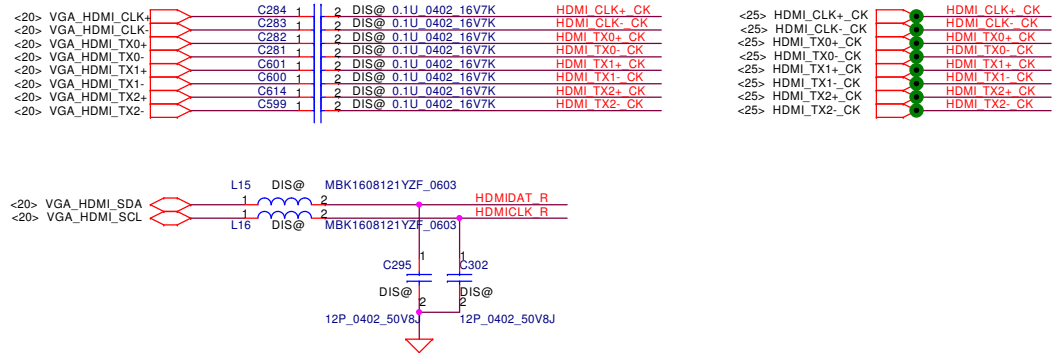


STRAP1 use for 3GIO_PADCFG to set 35K pull up.
(PUN-04335-001_V10 HW9 update)

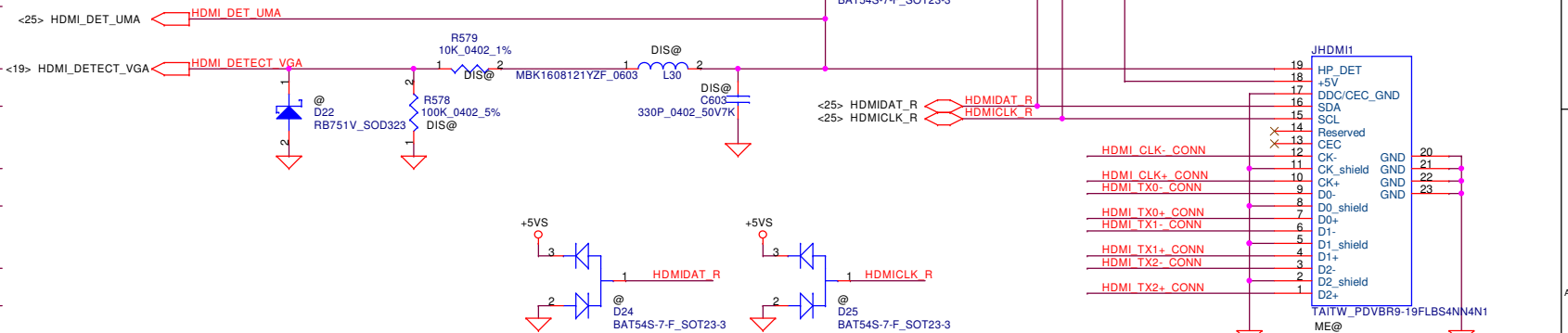
GPU	FB Memory (DDR3)		ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
N11M-GE1 LP1 (0x0A7D) 40nm	Samsung 800MHz (default)	K4W1G1646E-HC12						
		64Mx16	PD 10K	PD 15K	PD 20K	PU 30K	PU 35K	PU 45K
	Hynix 800MHz	H5TQ1G63BFR-12C						
		64Mx16	PD 10K	PD 15K	PD 15K	PU 30K	PU 35K	PU 45K
					X76			



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HDMI CLK*_ CK	S584	1	HDMI@ 2	0	0.0402	5%	HDMI CLK*_ CONN
HDMI CLK*_ CK	S582	1	HDMI@ 2	0	0.0402	5%	HDMI CLK*_ CONN
HDMI TX0*_ CK	S588	1	HDMI@ 2	0	0.0402	5%	HDMI TX0*_ CONN
HDMI TX0*_ CK	S586	1	HDMI@ 2	0	0.0402	5%	HDMI TX0*_ CONN
HDMI TX1*_ CK	S592	1	HDMI@ 2	0	0.0402	5%	HDMI TX1*_ CONN
HDMI TX1*_ CK	S590	1	HDMI@ 2	0	0.0402	5%	HDMI TX1*_ CONN
HDMI TX2*_ CK	S596	1	HDMI@ 2	0	0.0402	5%	HDMI TX2*_ CONN
HDMI TX2*_ CK	S594	1	HDMI@ 2	0	0.0402	5%	HDMI TX2*_ CONN



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				Date: Thursday, October 29, 2009	Sheet	24	of 51

FOR asmedia R428 STUFF

RESERVE THE R668 PULL UP TO 3VS

RESERVE THE R670 PULL DOWN TO GND

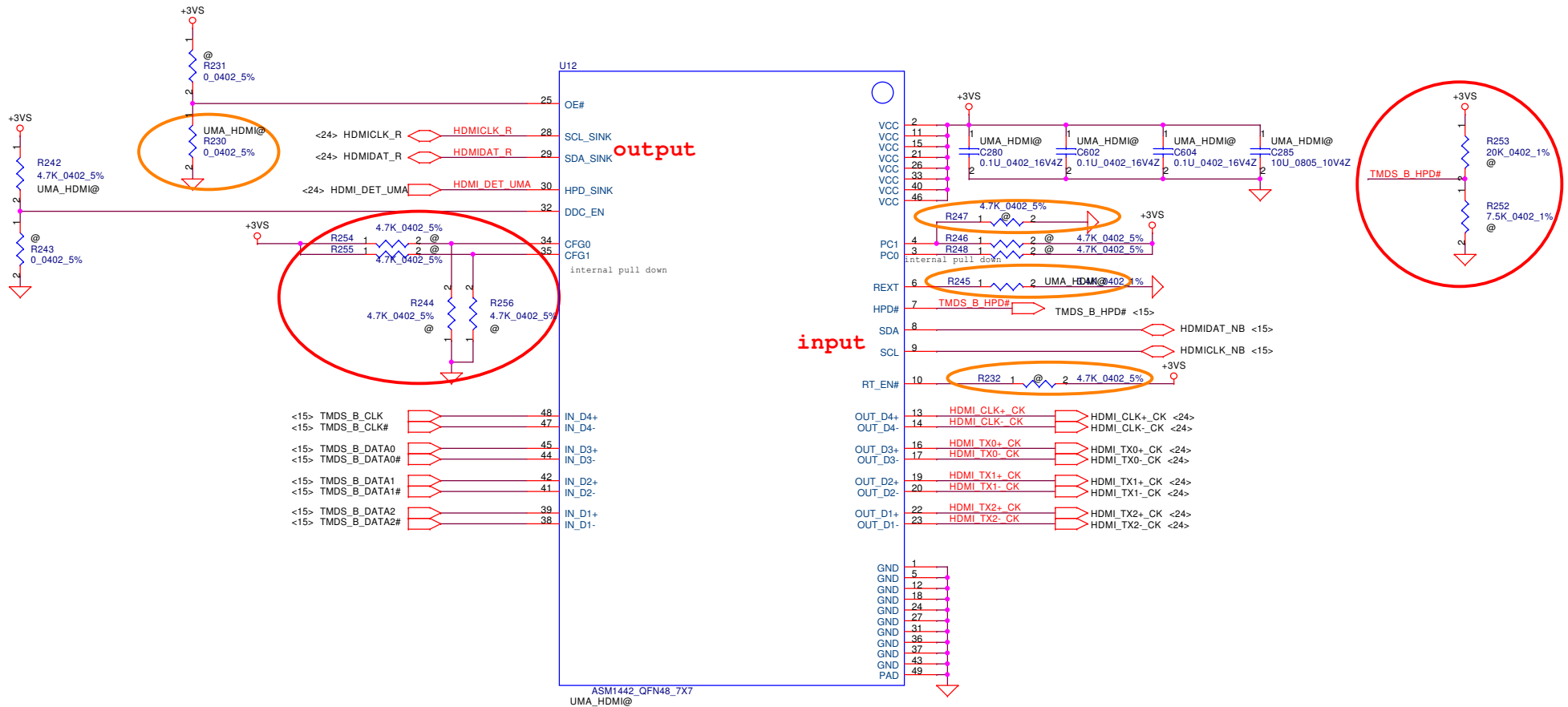
CHANGE R483 FROM 499 TO 3.4K OHM

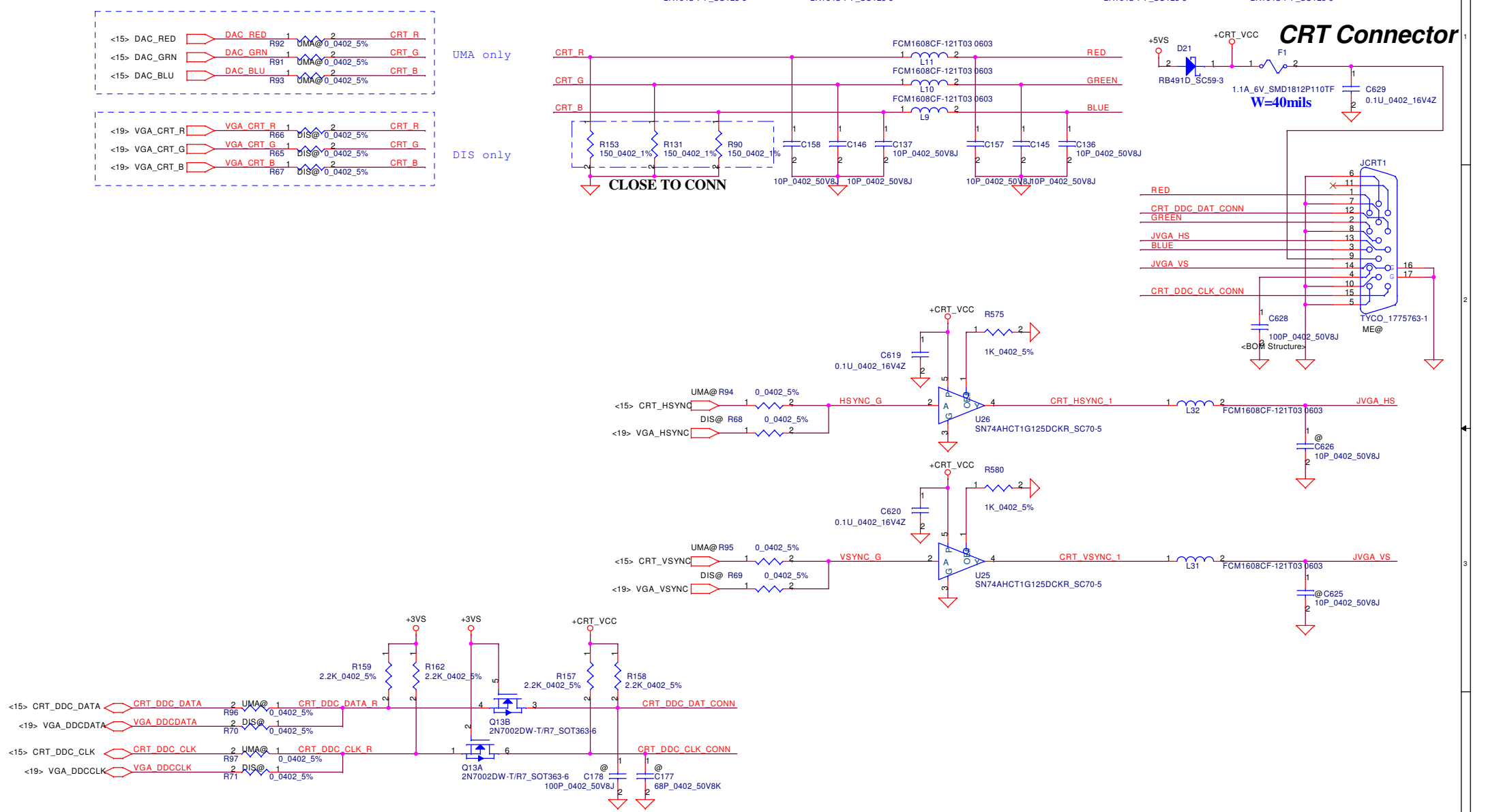
FOR 7318C

PIN6 PULL DOWN 1.2Kohm

PIN7 PULL DOWN 7.5Kohm

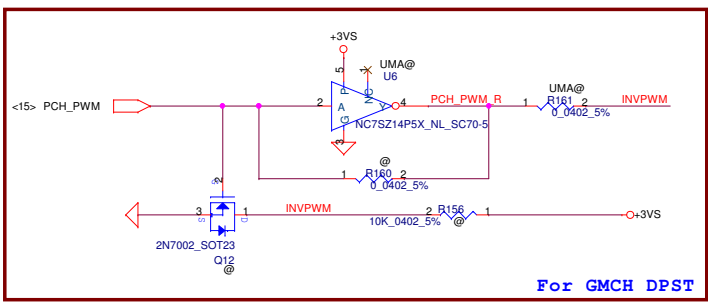
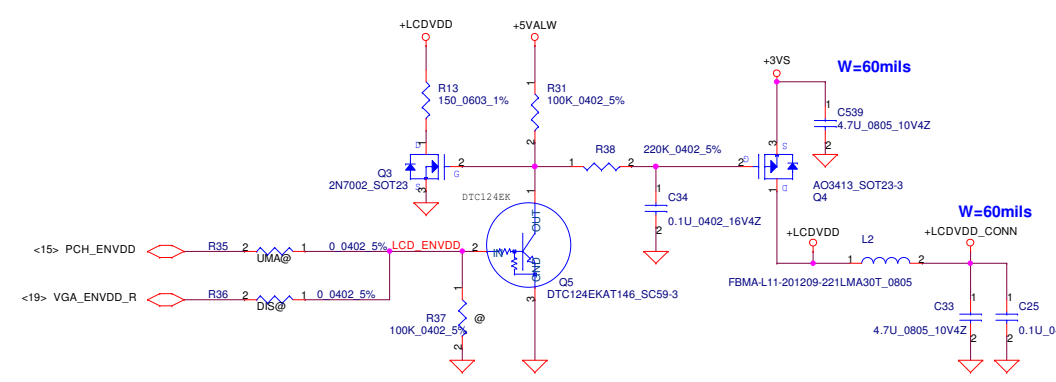
PIN7 PULL UP 20Kohm



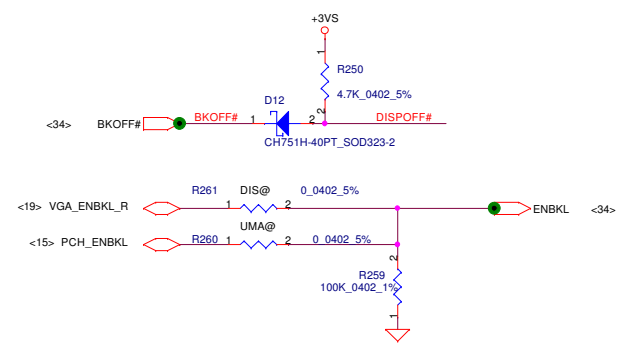
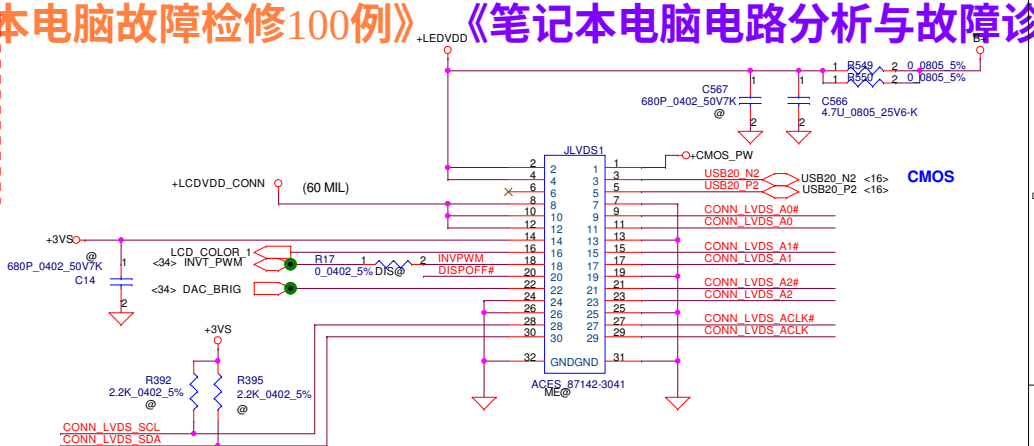
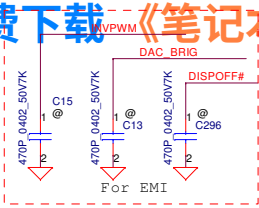


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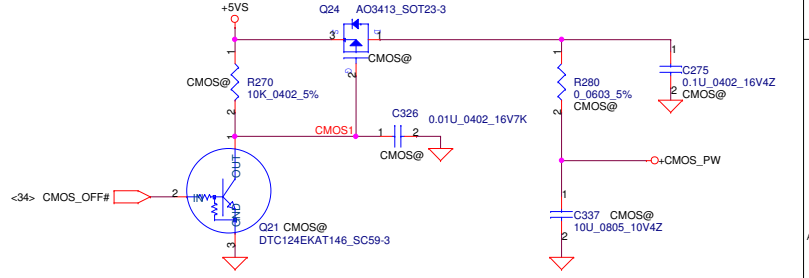
LCD POWER CIRCUIT



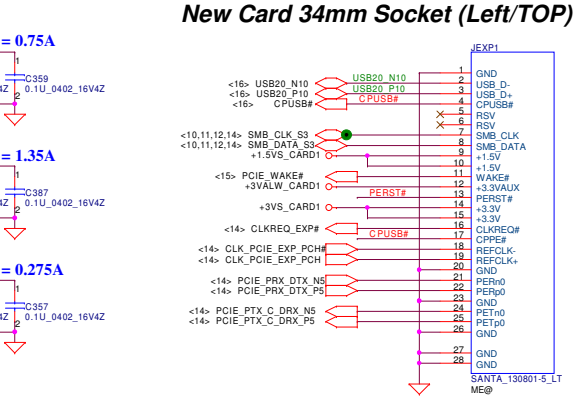
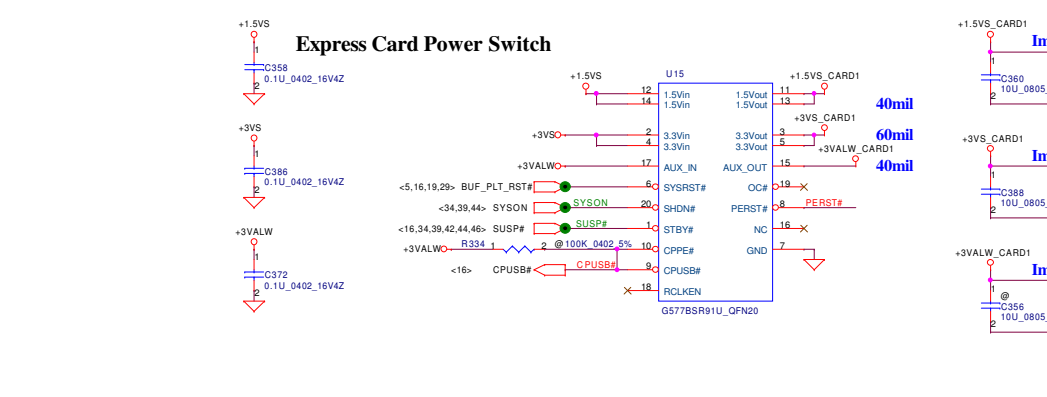
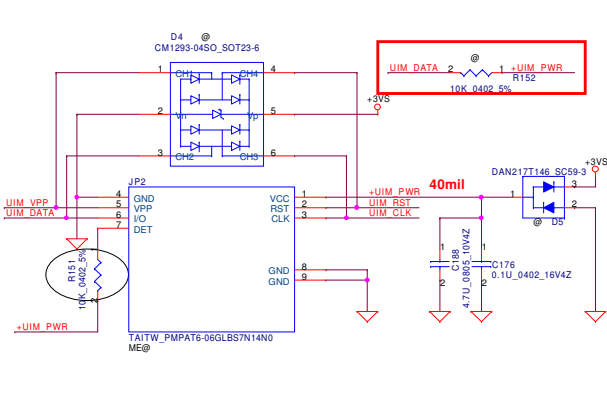
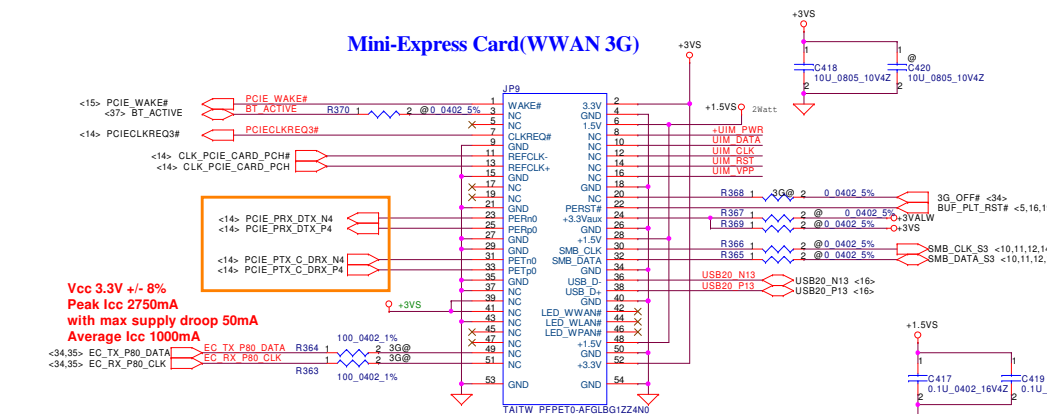
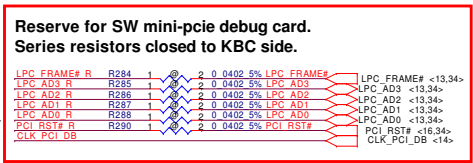
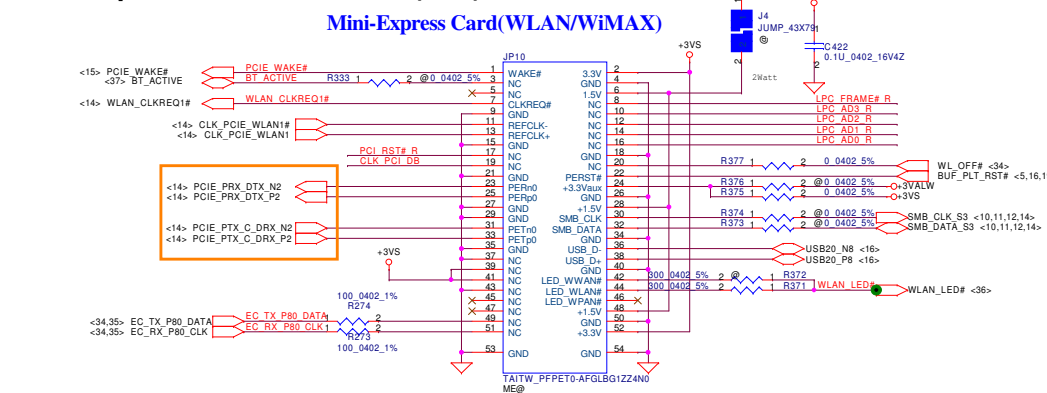
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<15> LVDS_A0	LVDS_A0	0.0402_5%	2	UMA@	1	R383	CONN_LVDS_A0
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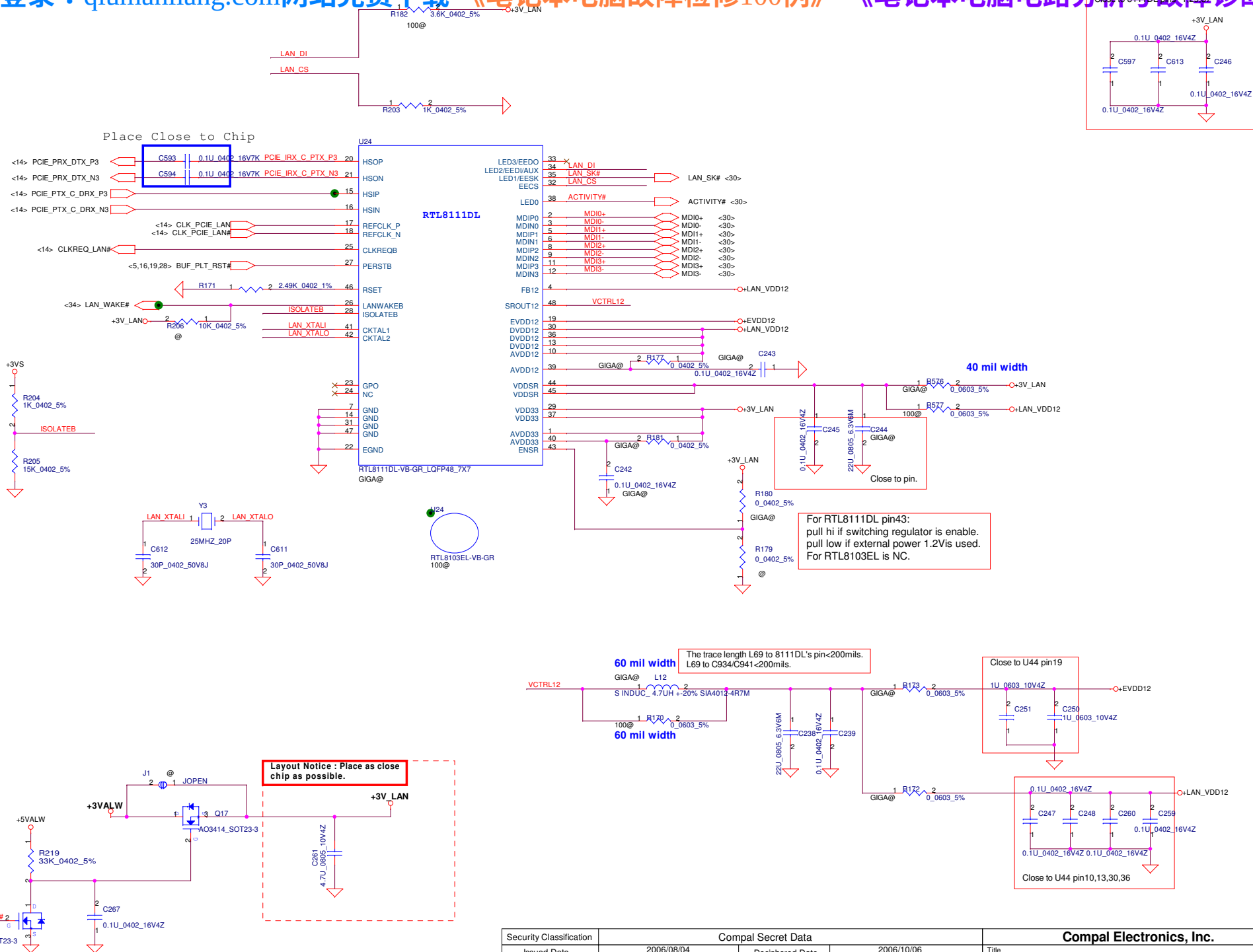


CMOS Camera

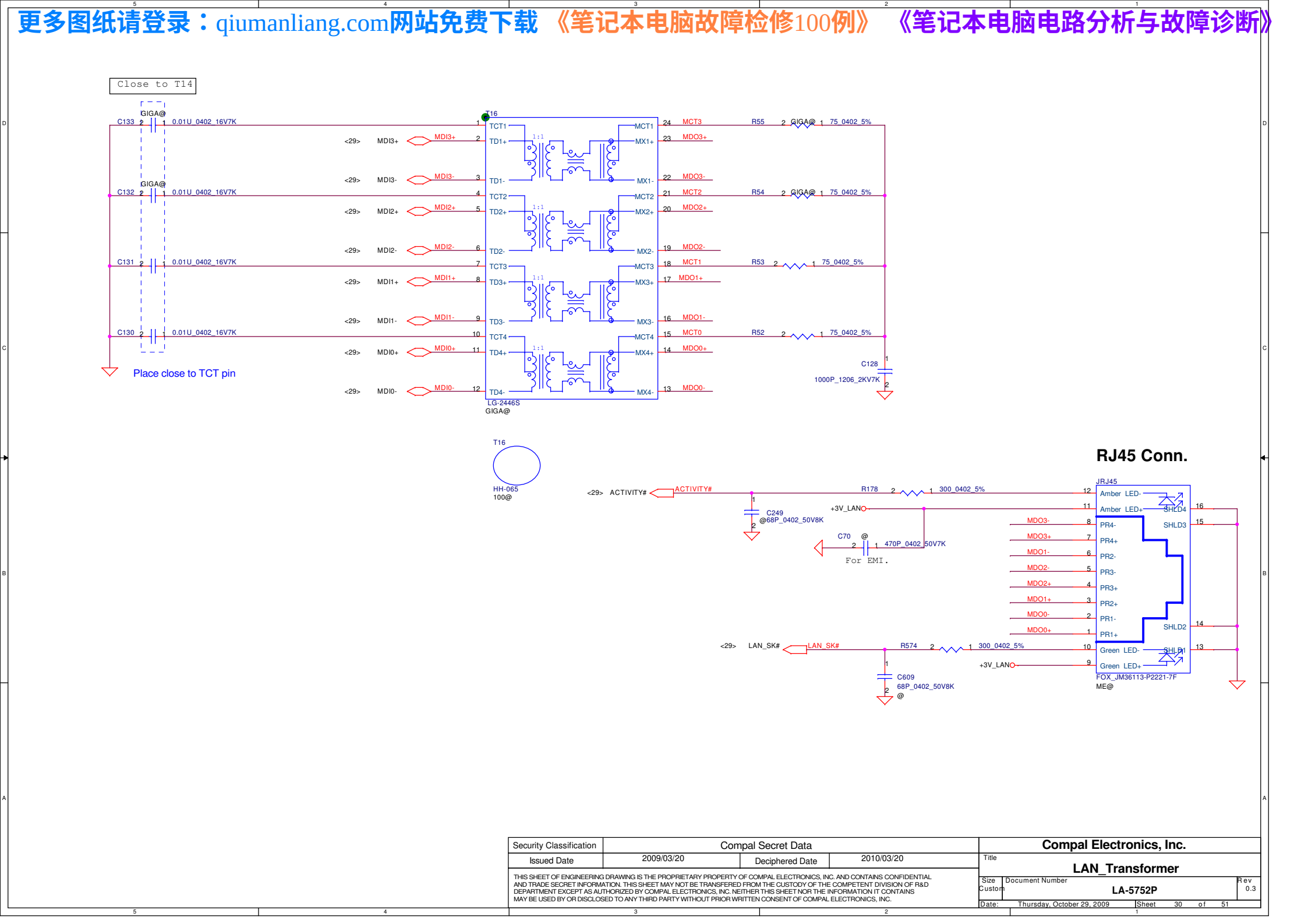


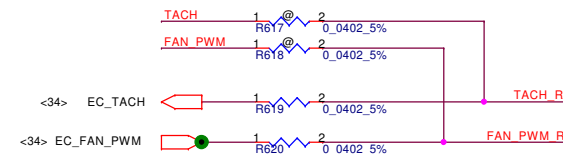
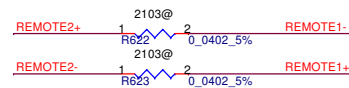
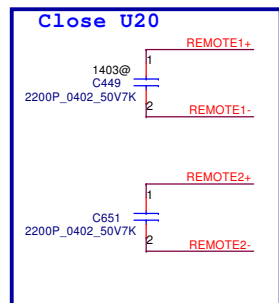
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		Document Number	
		LA-5752P	
		Rev 0.3	
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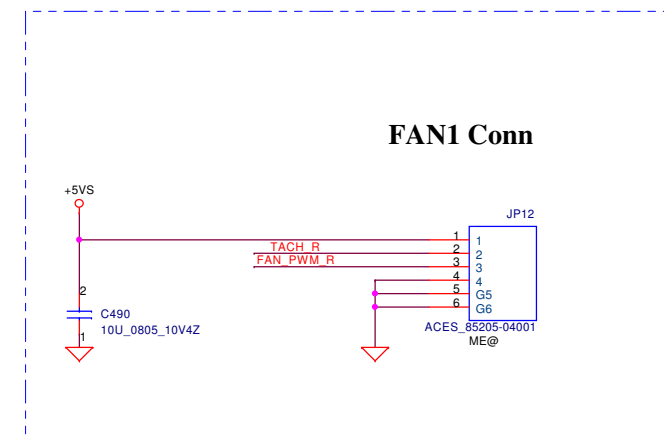
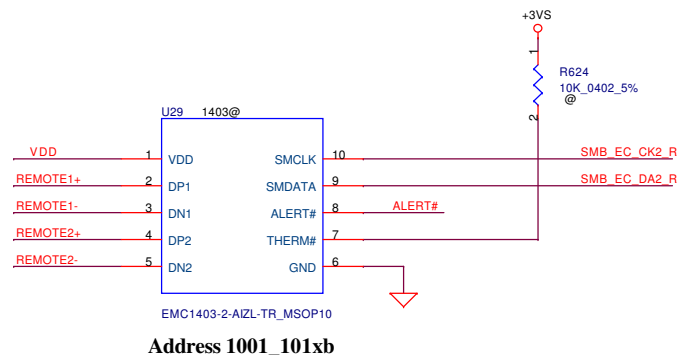


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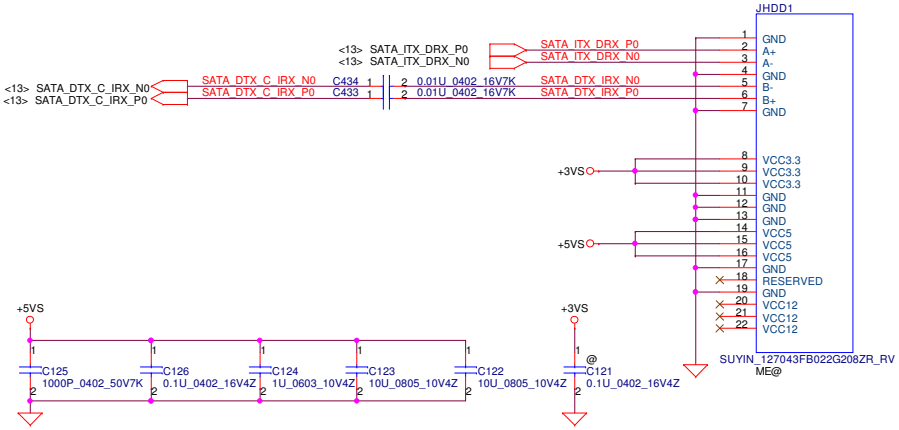


Shutdown Temp	TRIP_SET R439 (1%)
93	953ohm
94	1020ohm
95	1100ohm
96	1150ohm
97	1240ohm
98	1330ohm
99	1400ohm
100	1500ohm
101	1580ohm
102	1690ohm
103	1820ohm
104	1960ohm
105	2050ohm

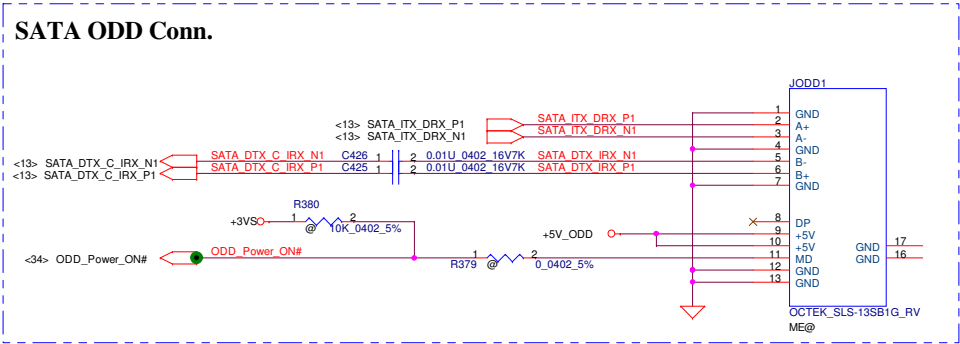


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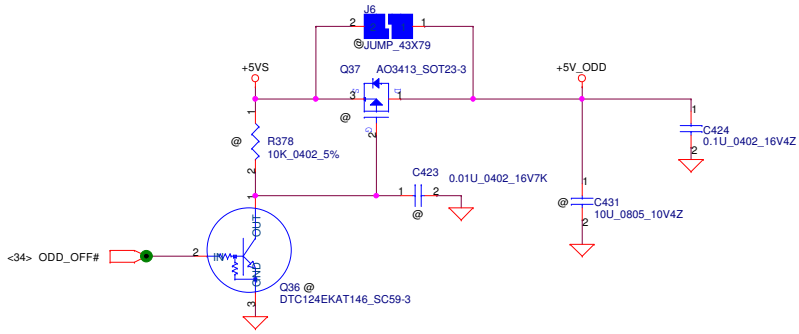
SATA HDD Conn.



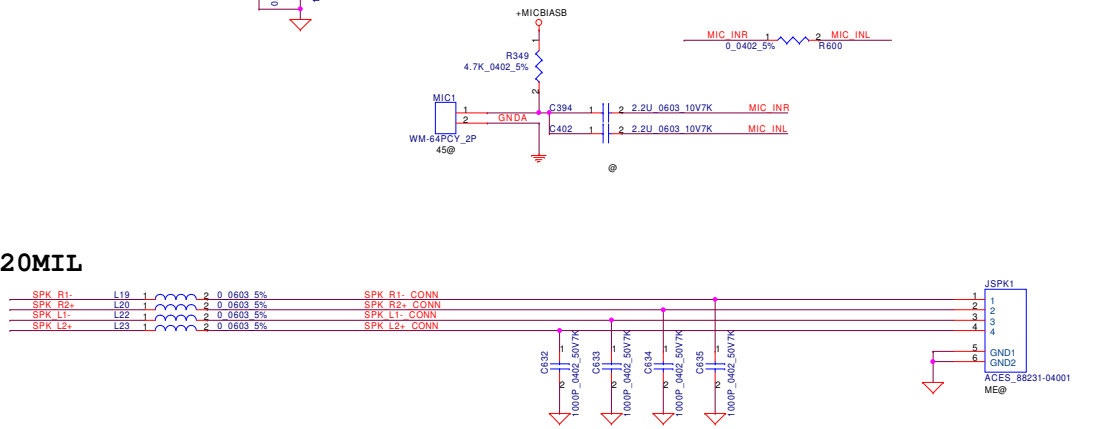
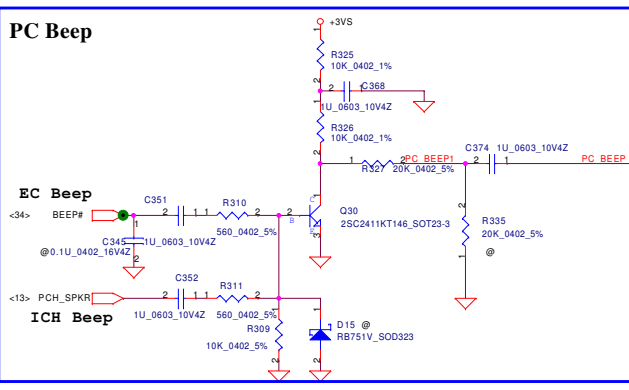
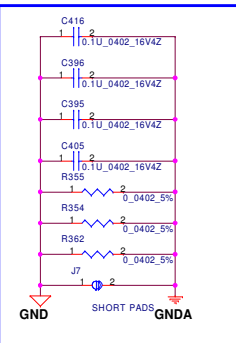
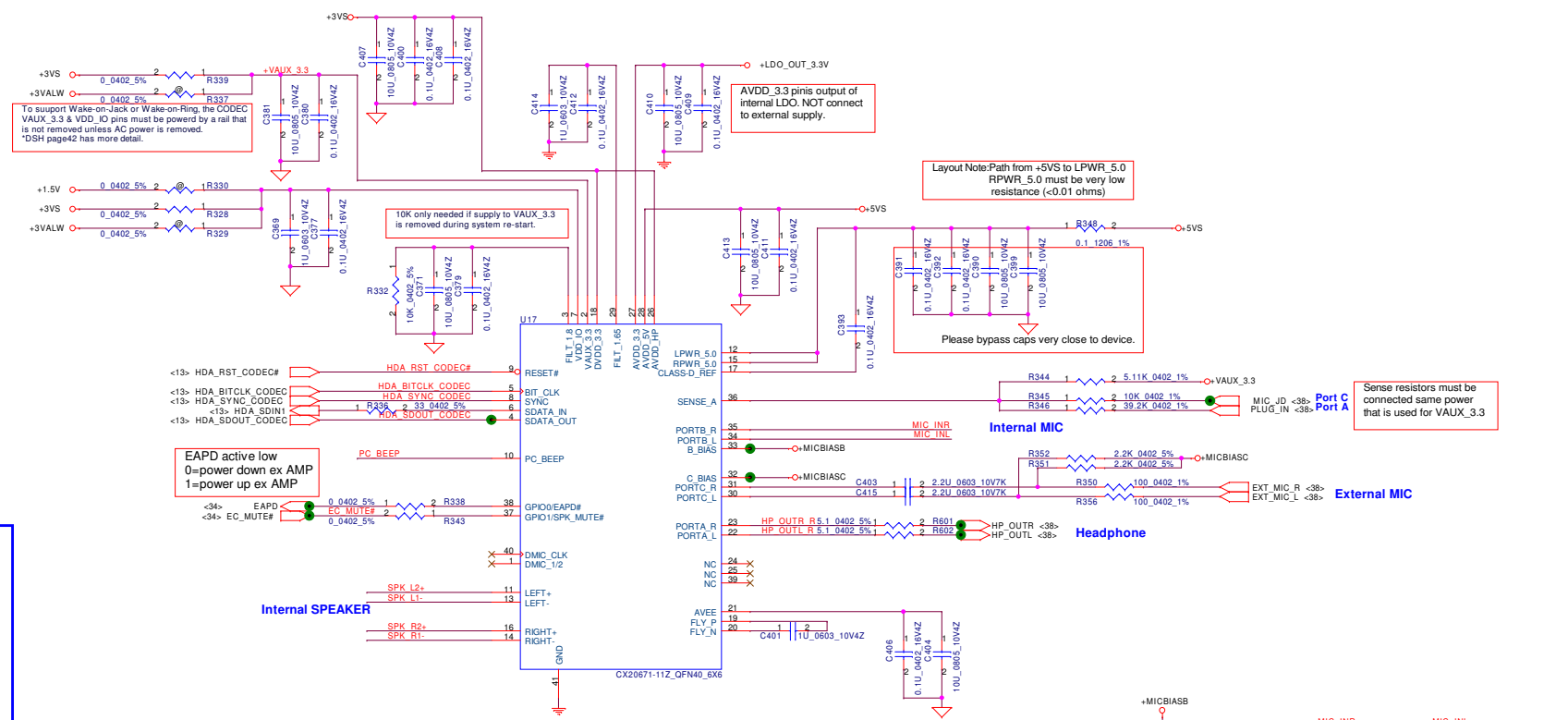
SATA ODD Conn.



ODD Power Control



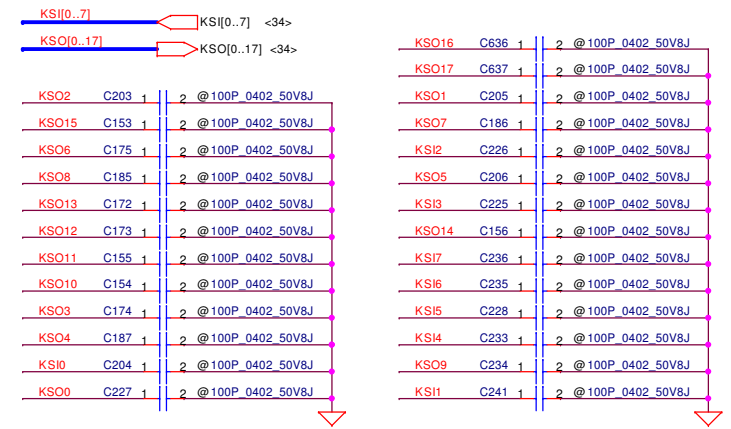
CX20671
 High Definition Audio Codec SoC
 With Integrated Class-D Stereo
 Amplifier.
 An integrated 5 V to 3.3 V Low-dropout
 voltage regulator (LDO).
 An integrated 3.3 V to 1.8V Low-dropout
 voltage regulator (LDO).



wide 20MIL

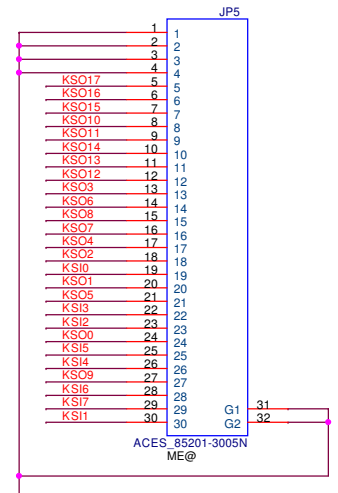
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INT_KBD Conn.

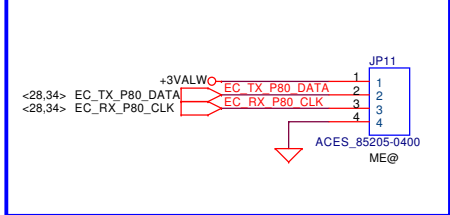


CONN PIN define need double check

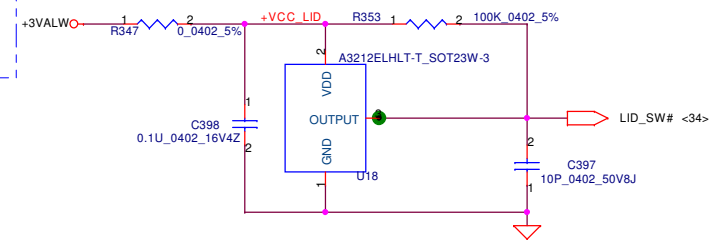
reversal of NIWE1



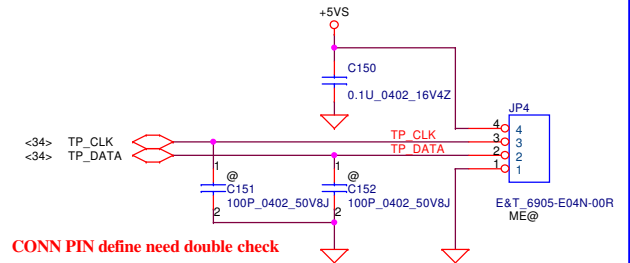
EC DEBUG PORT



Lid Switch

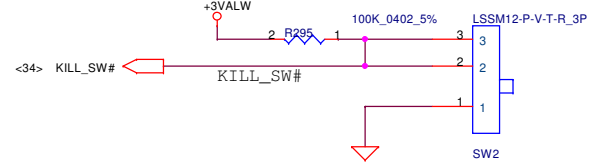


To TP/B Conn.



CONN PIN define need double check

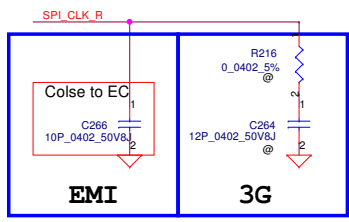
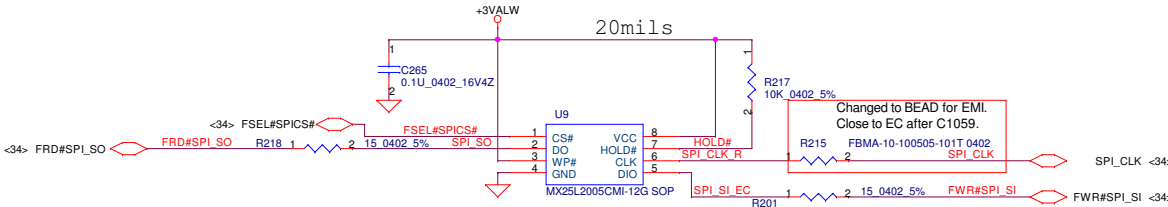
Kill Switch



Kill

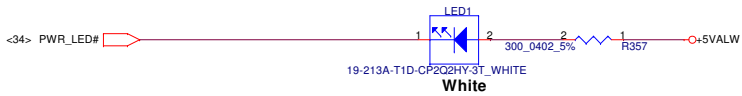
STATUS	
1, 2 (LOW)	OFF
2, 3 (HI)	ON

FOR EC-256KB SPI ROM
(150mil PACKAGE)
P/N : SA00003GK00

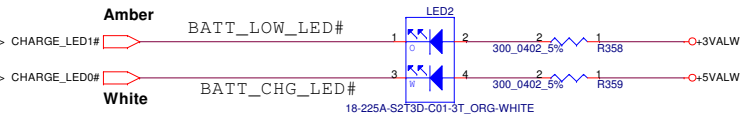


LED

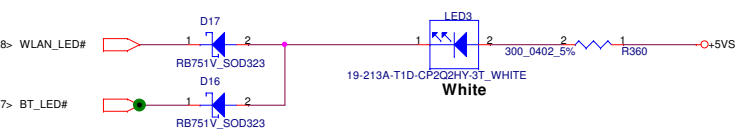
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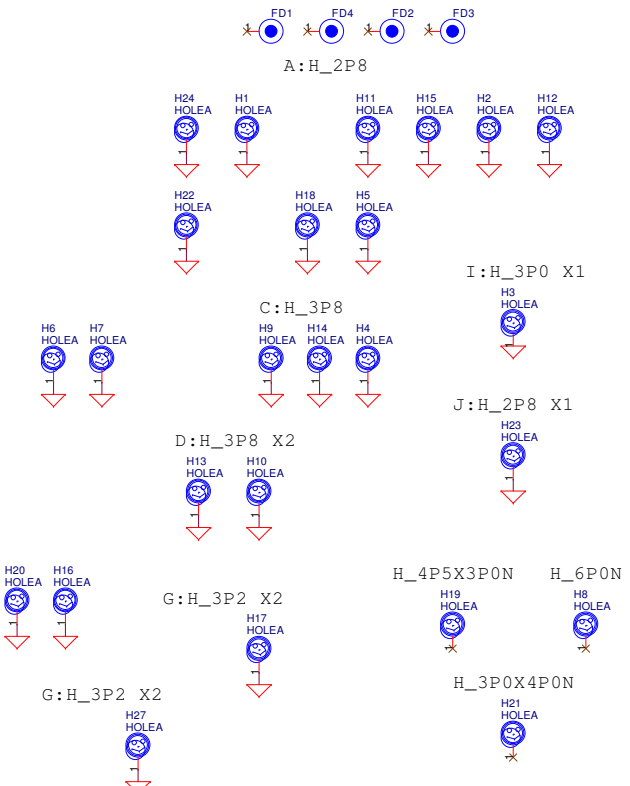
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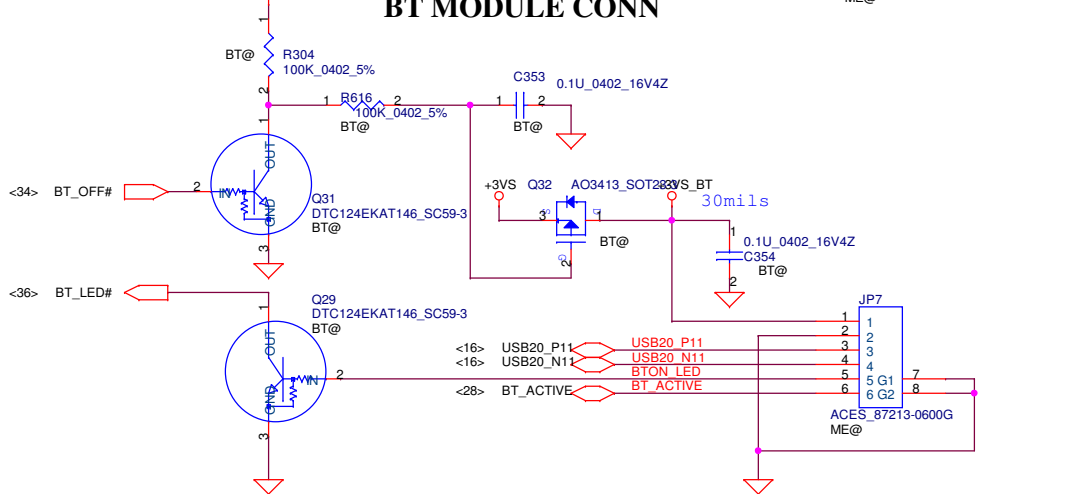
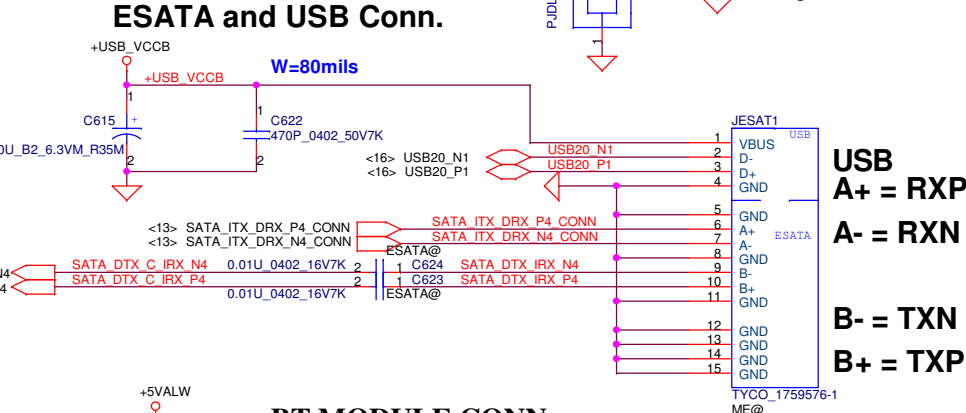
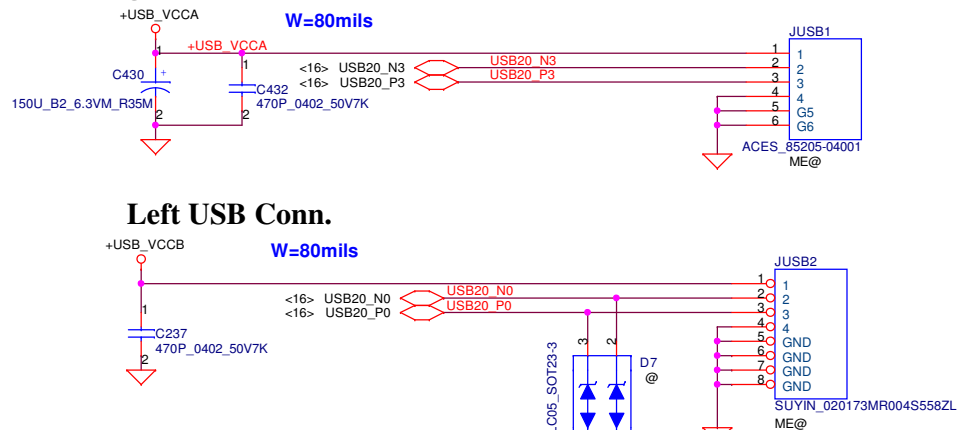
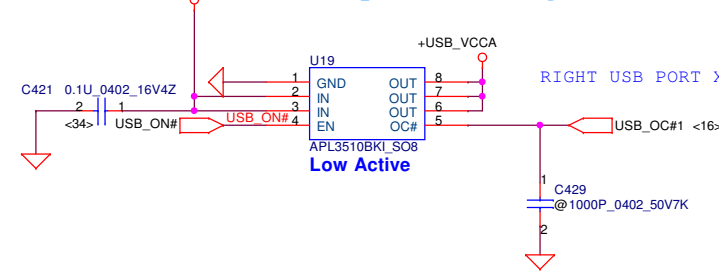
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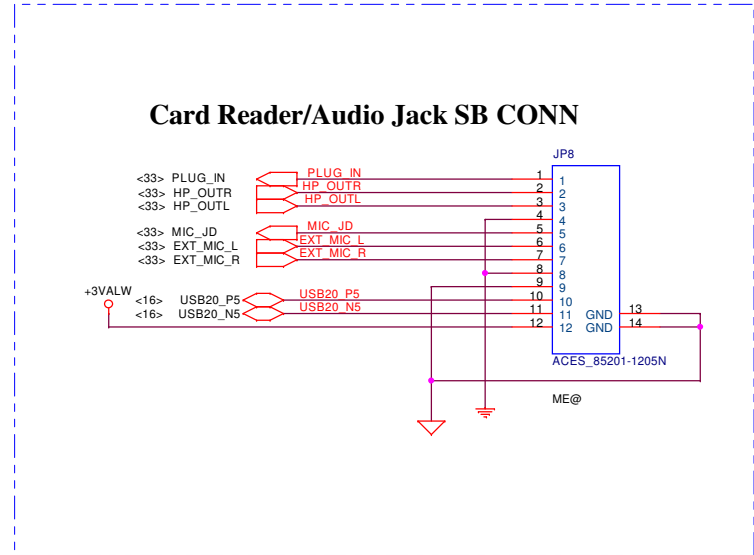
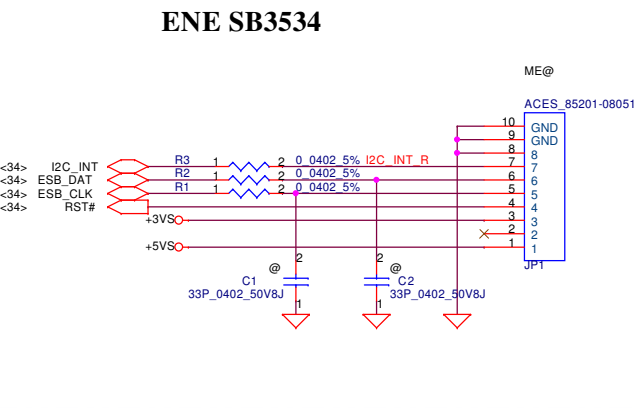
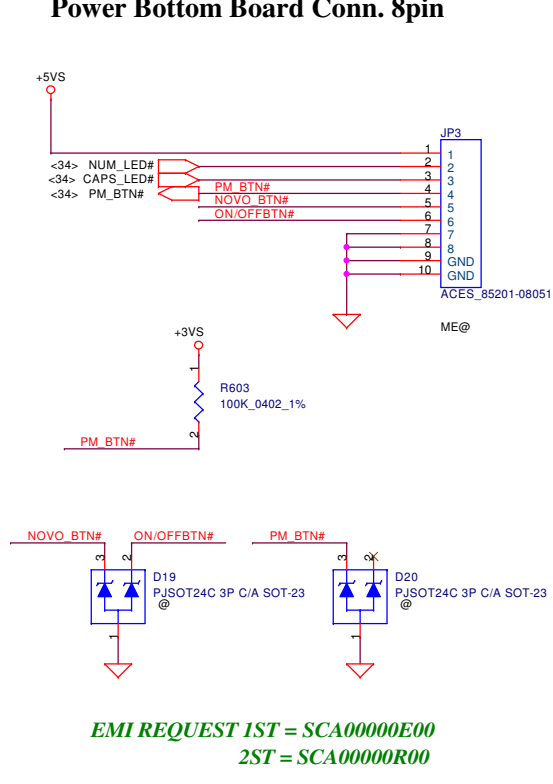
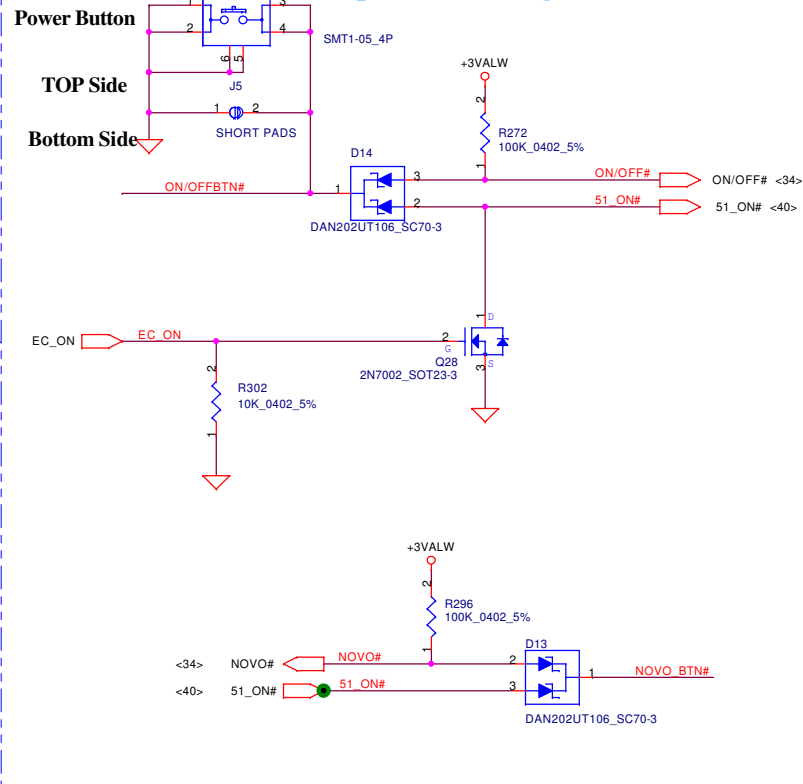
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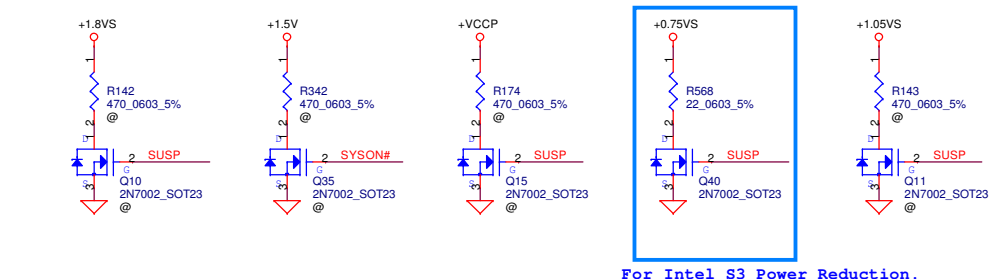
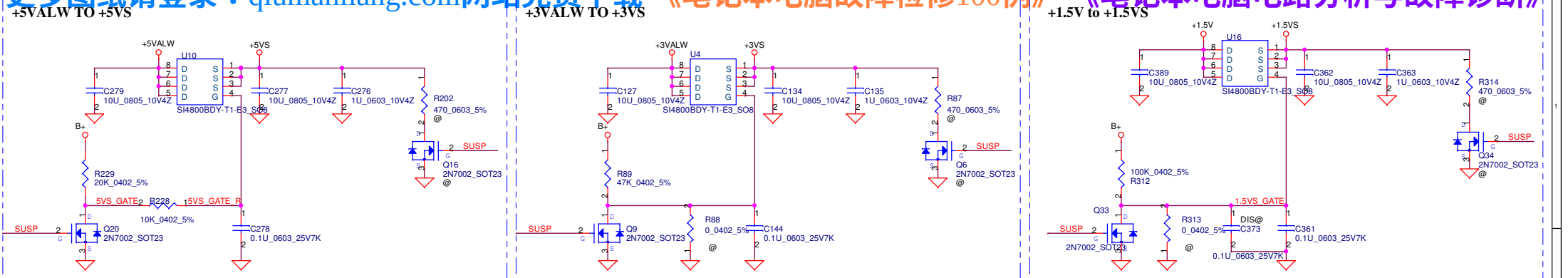
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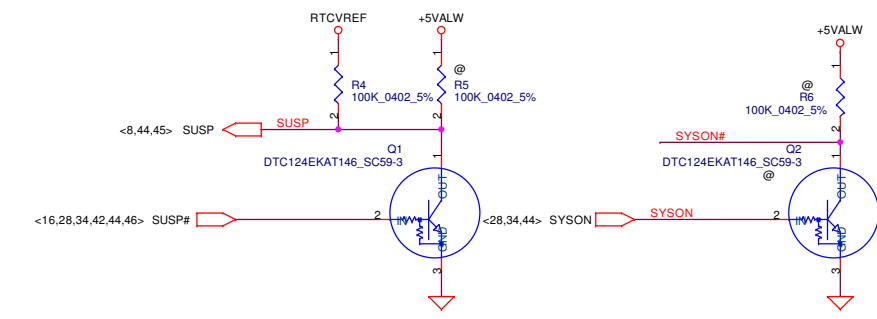
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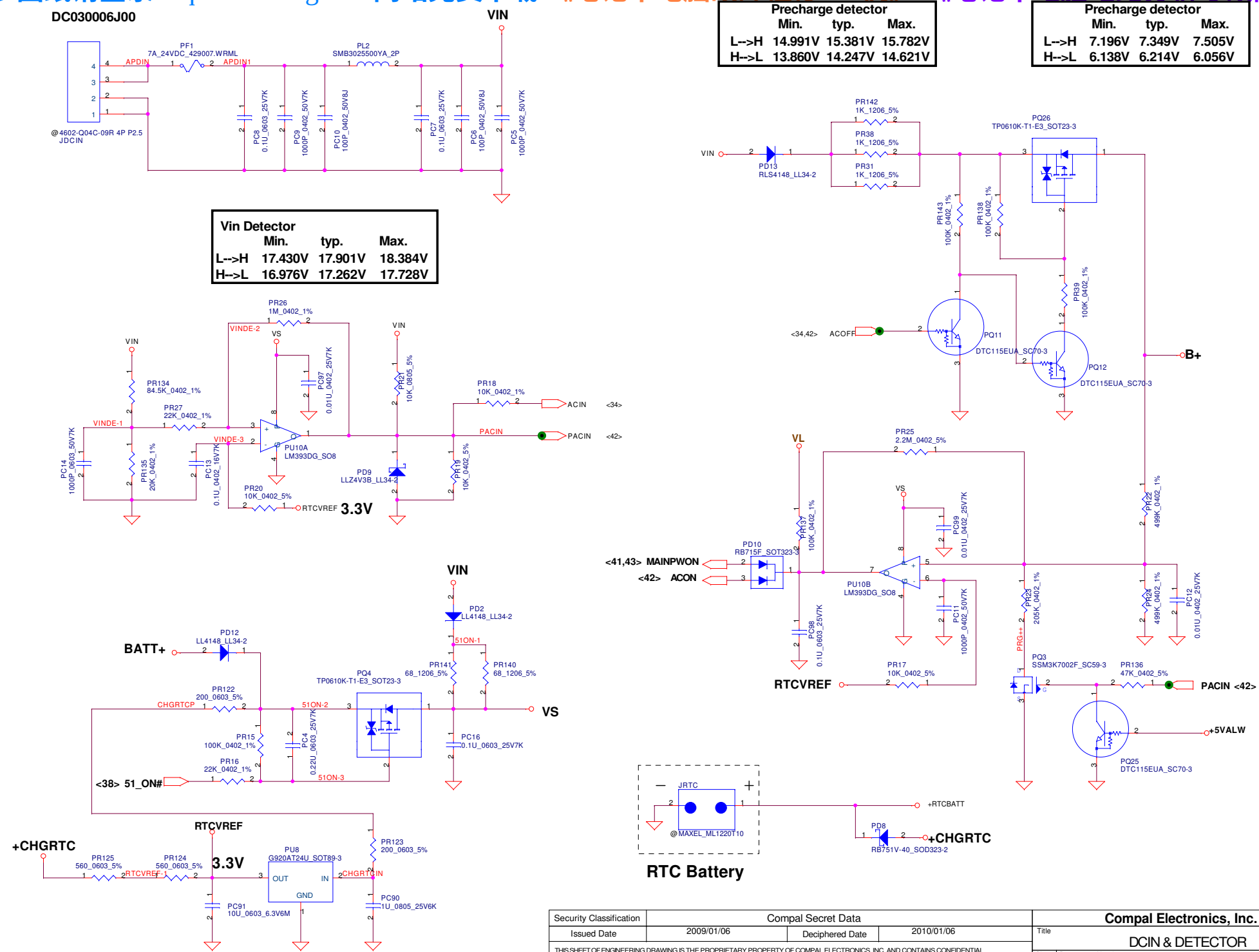
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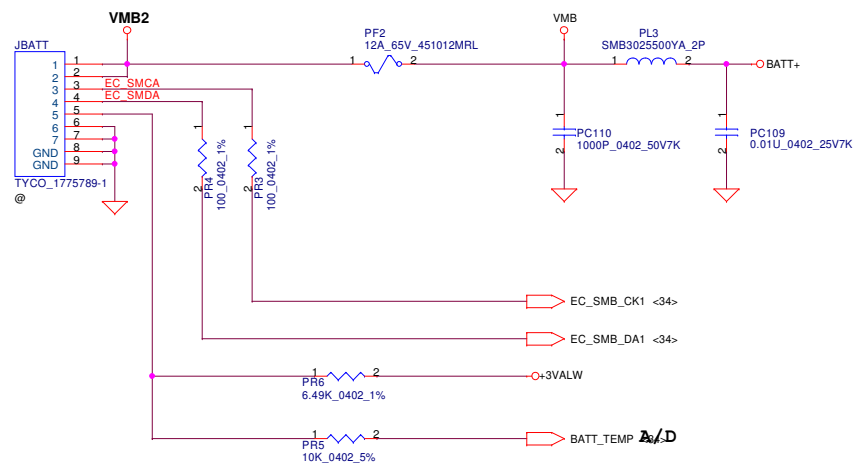


For Intel S3 Power Reduction.

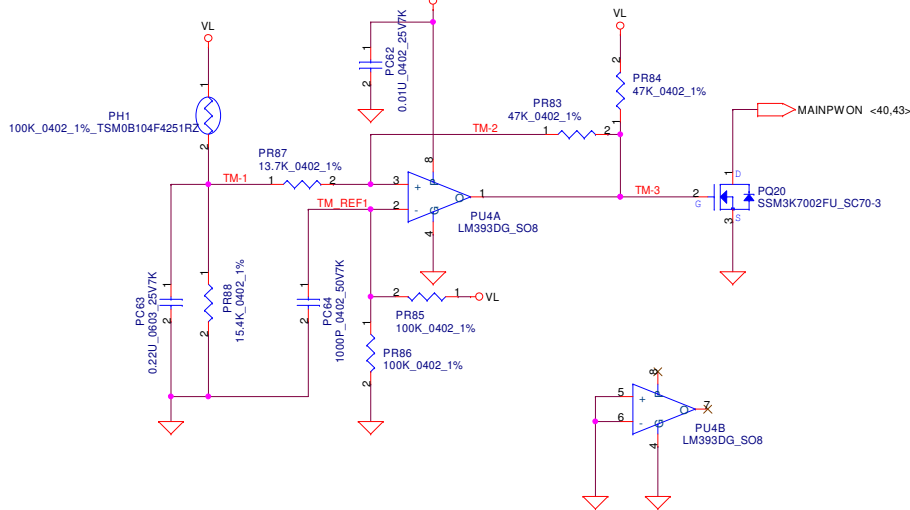


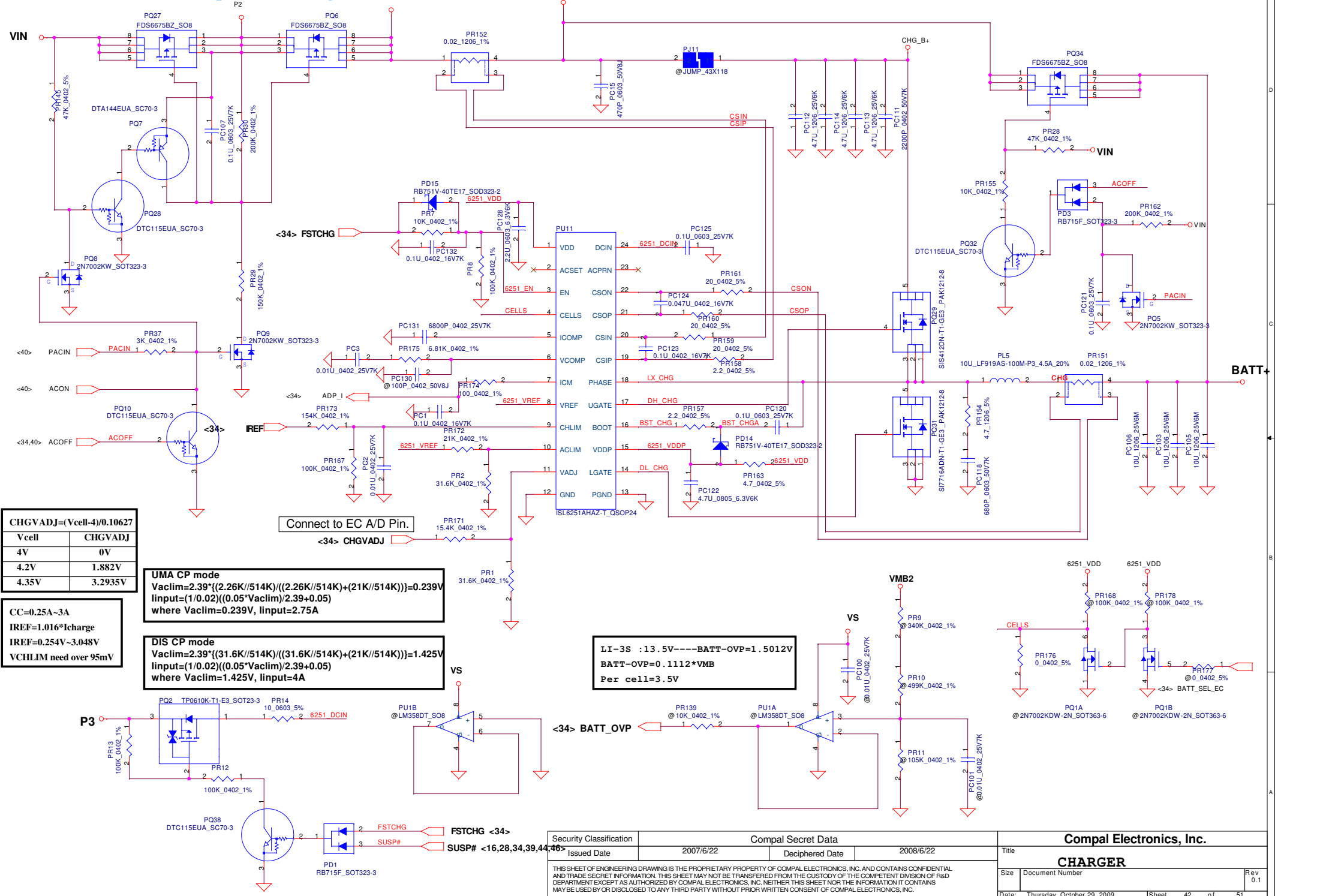
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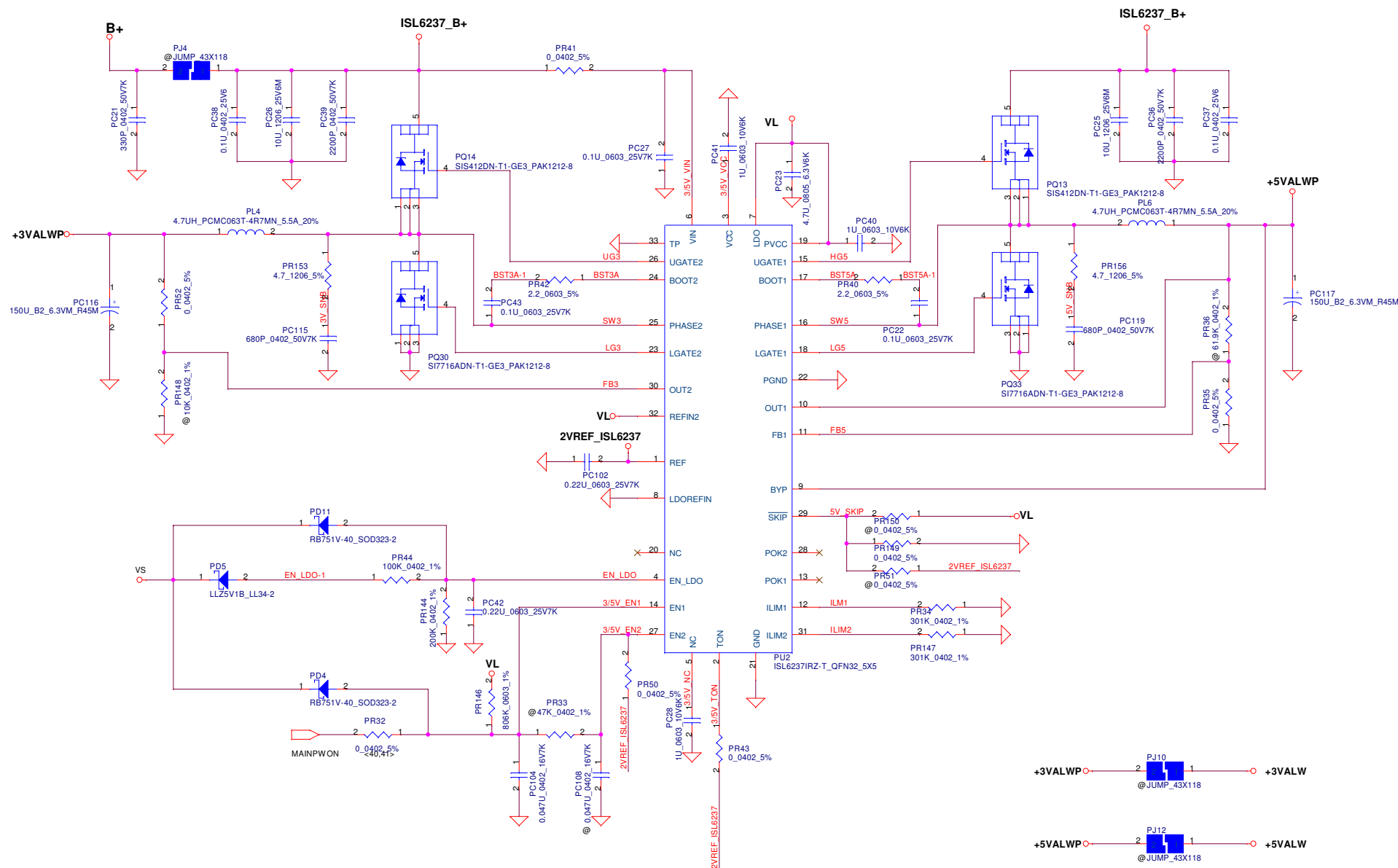




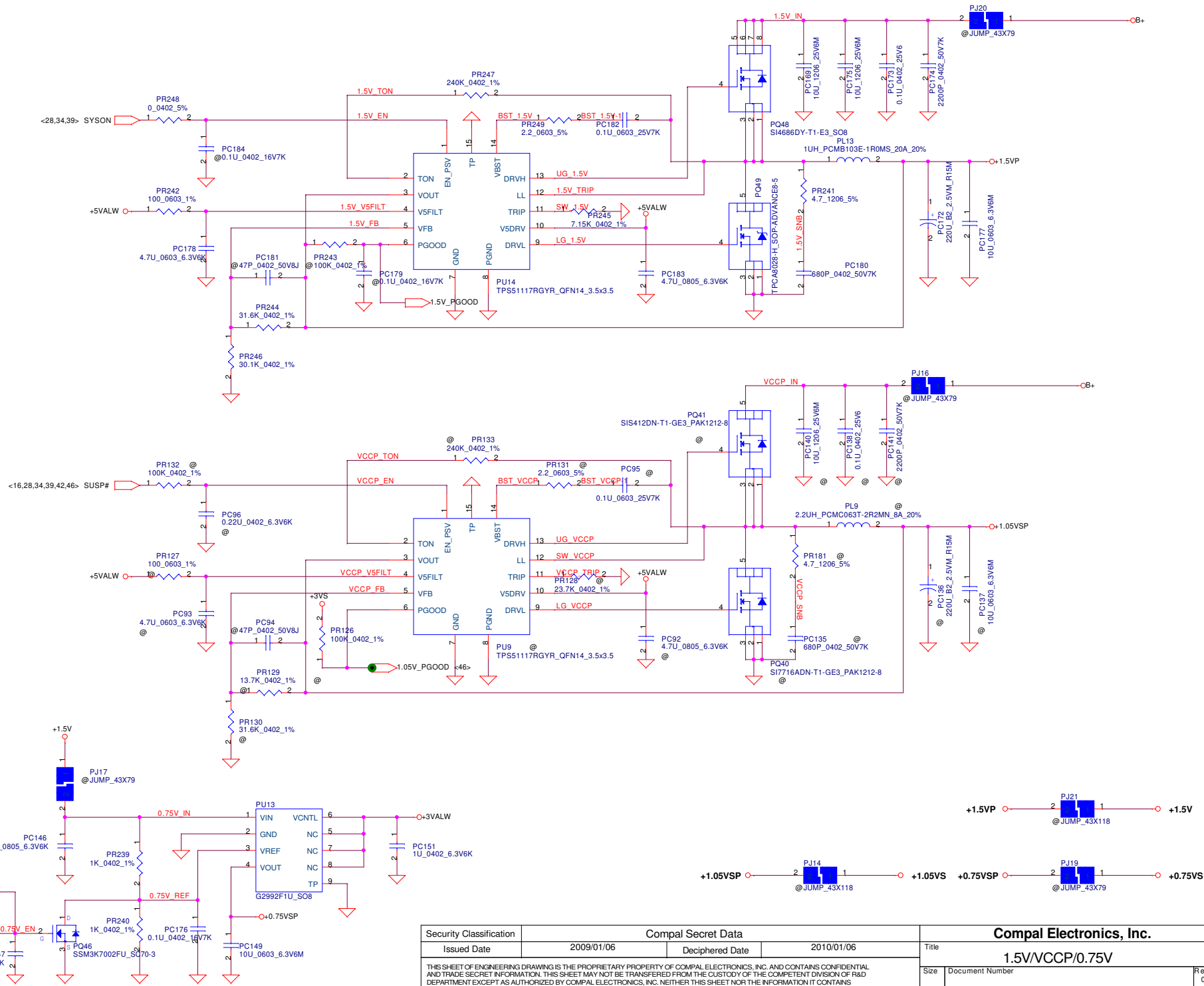
PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C



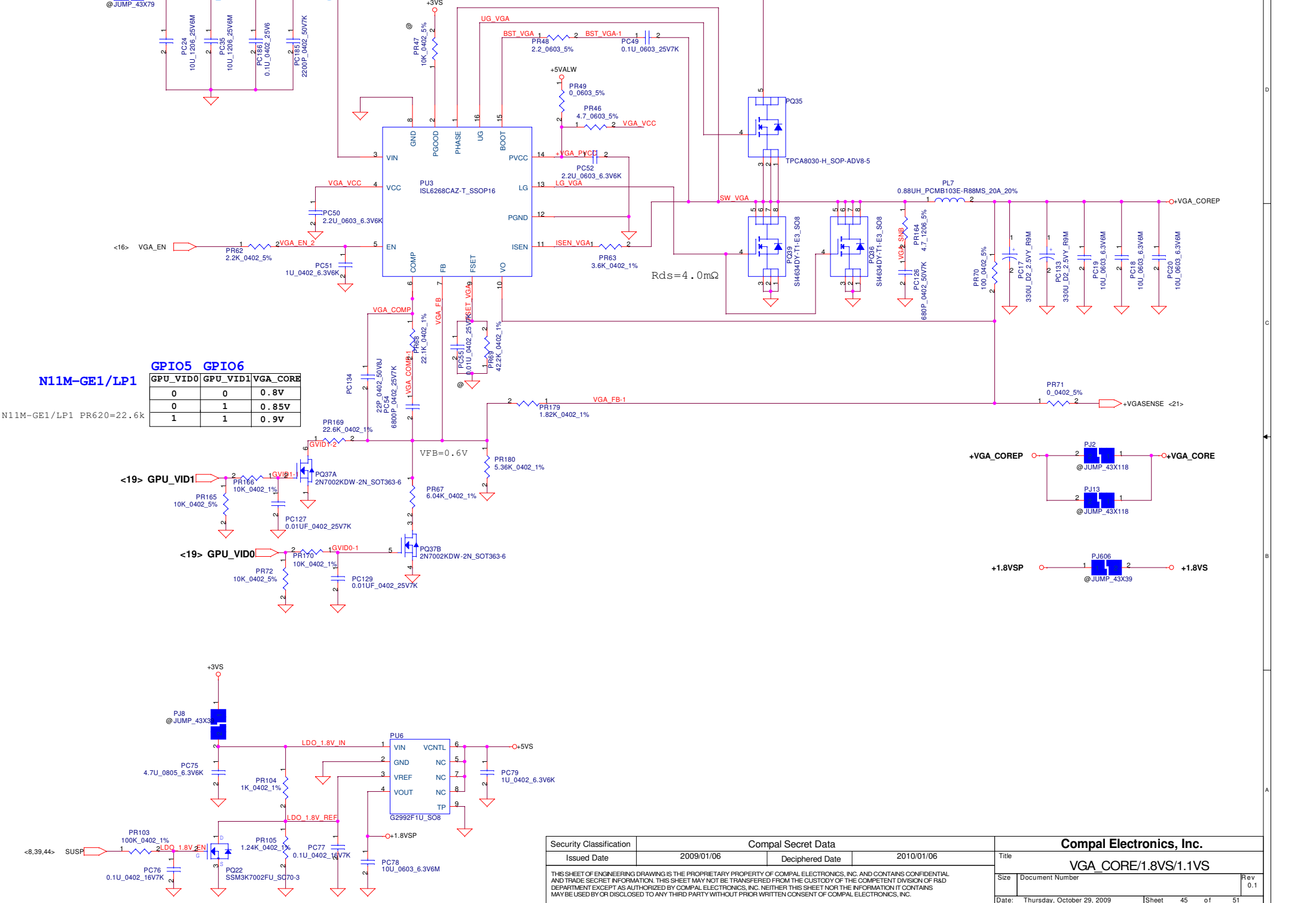


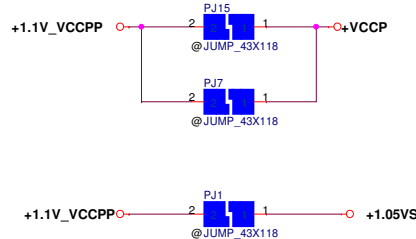
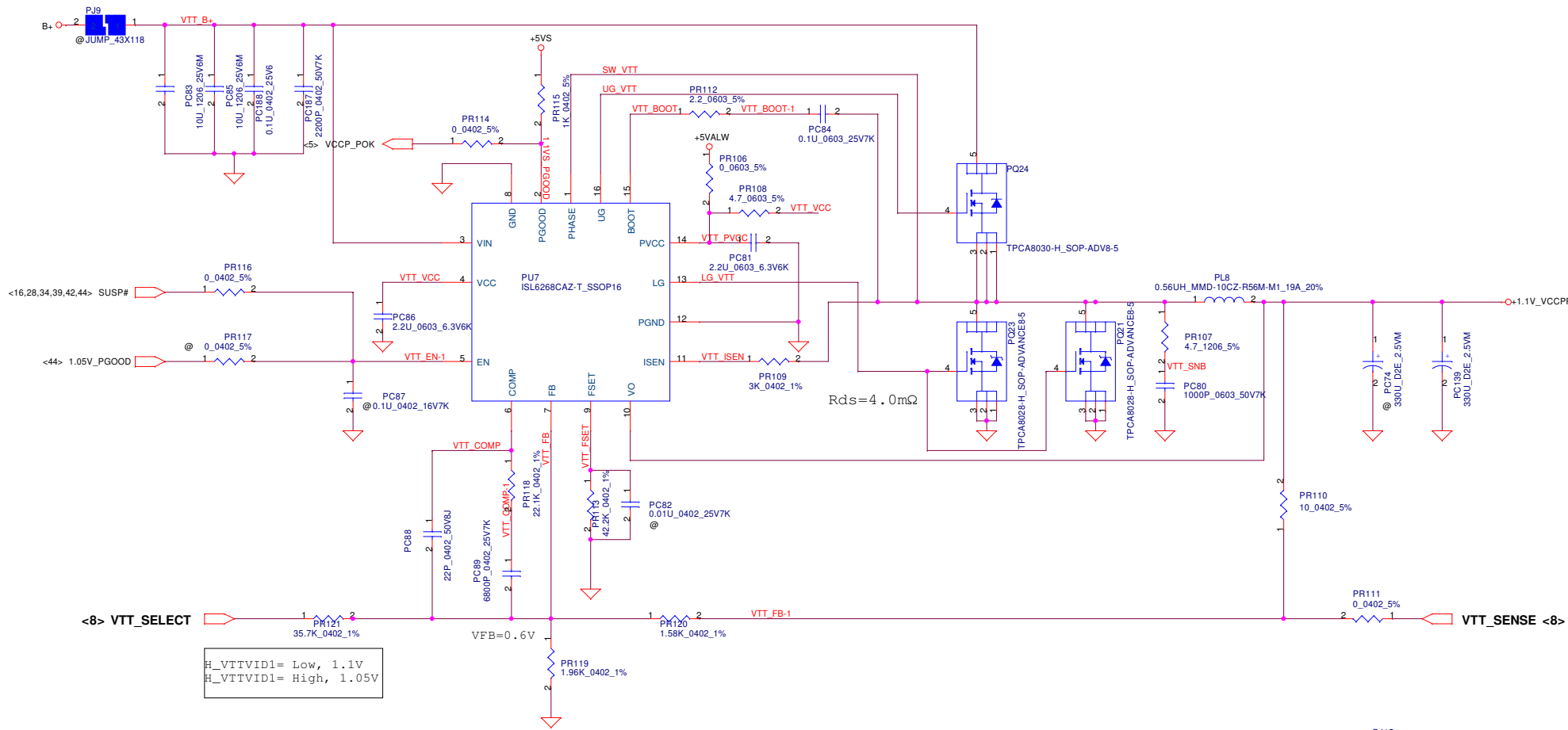


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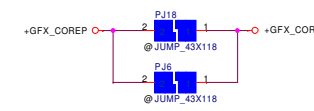
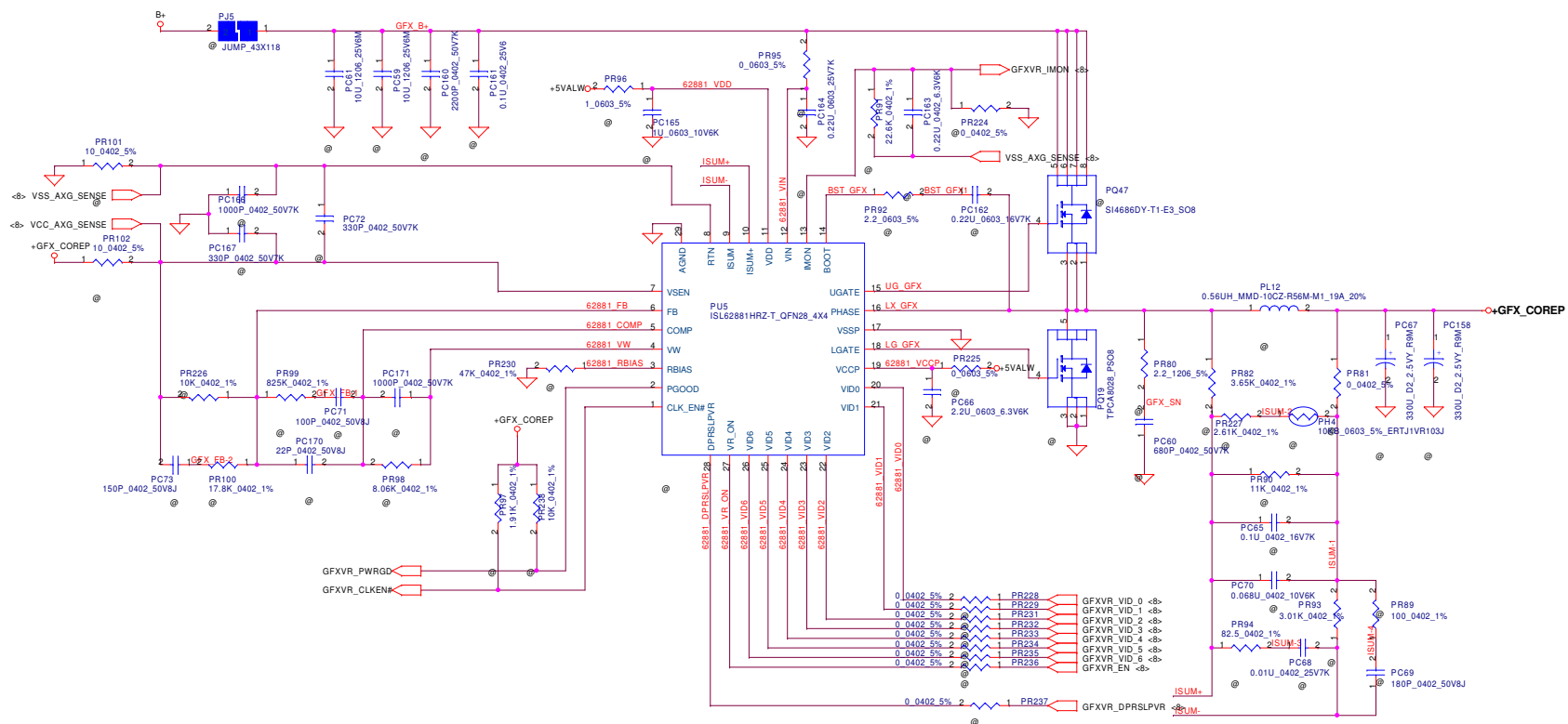


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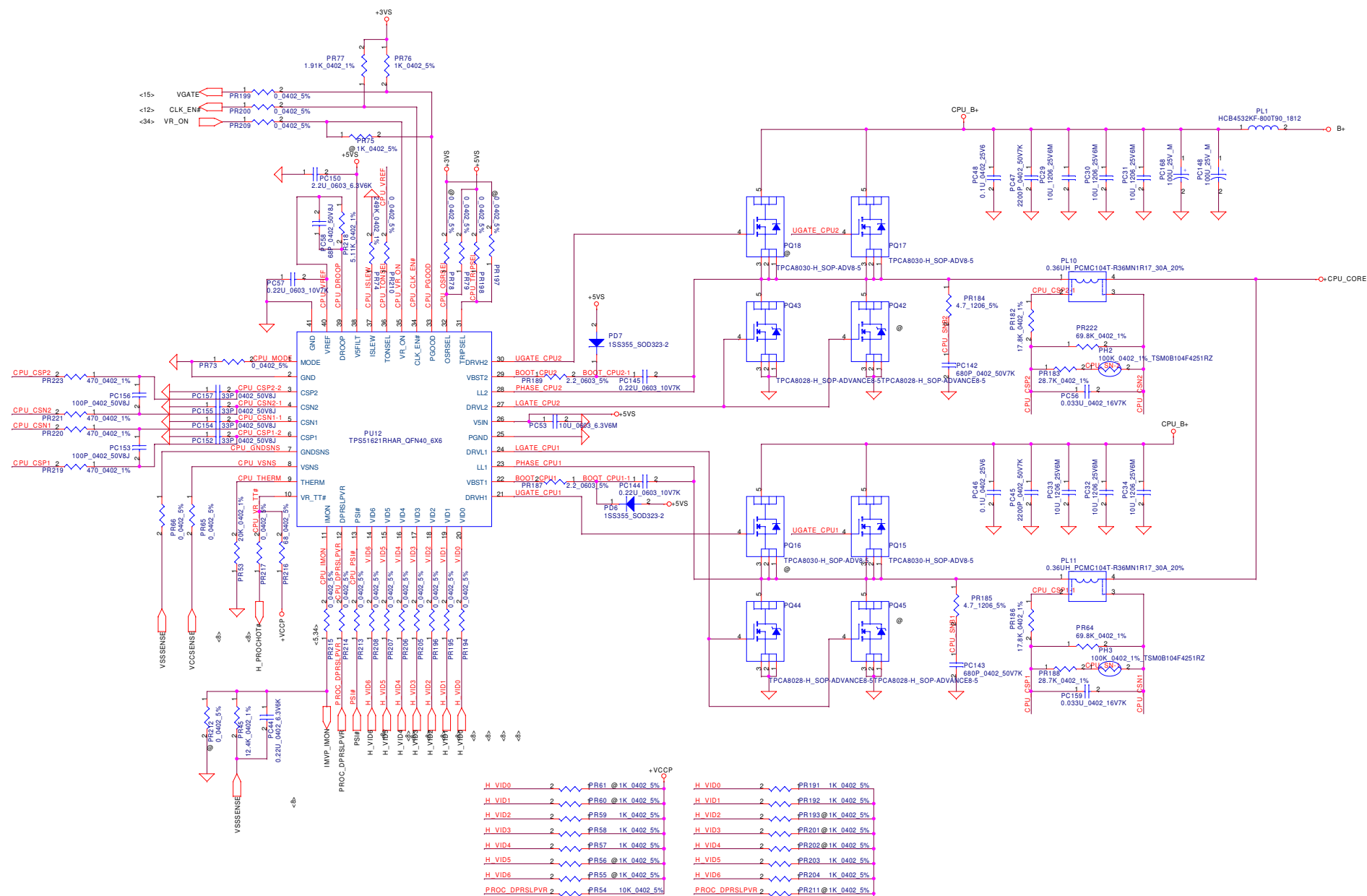


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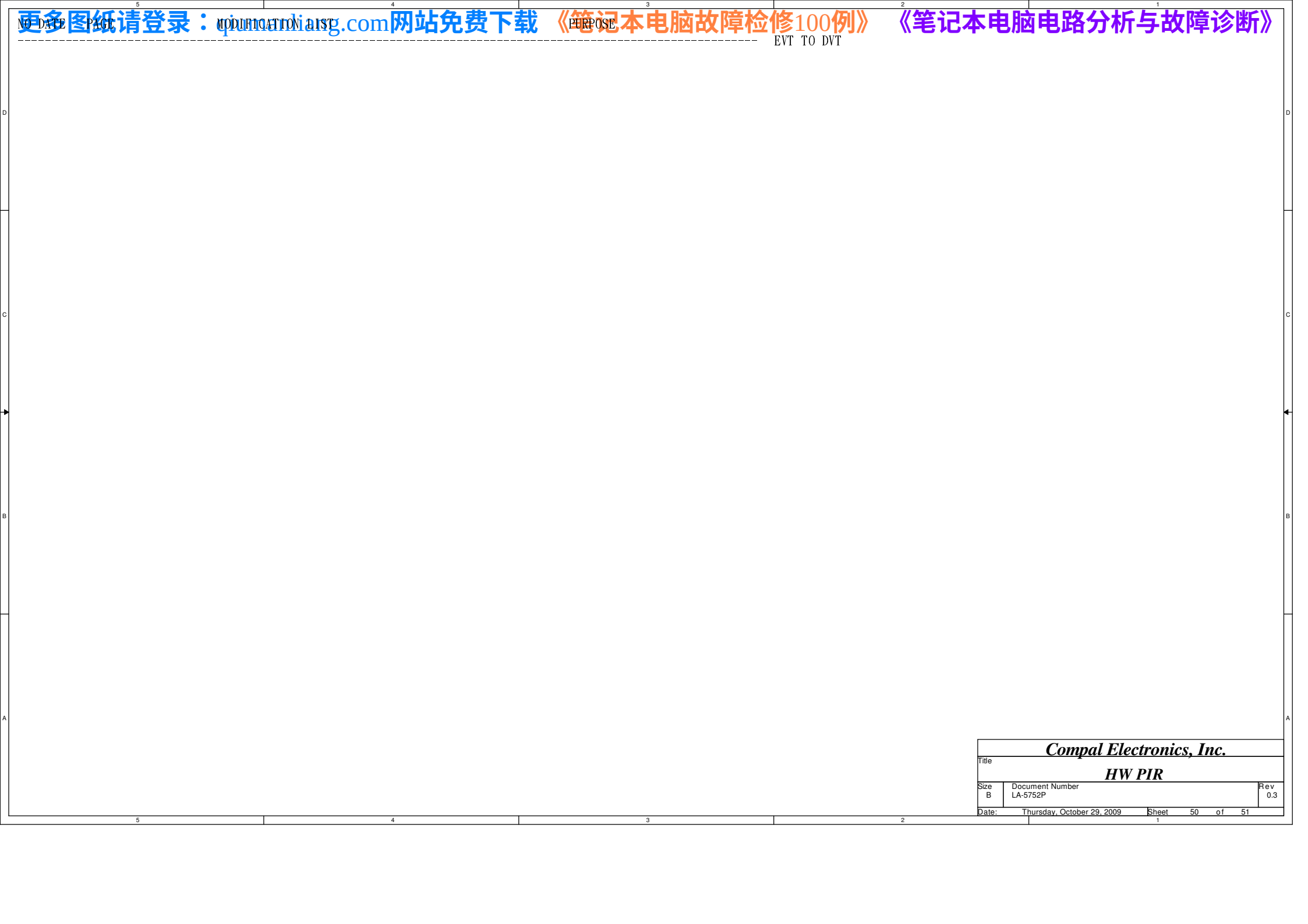
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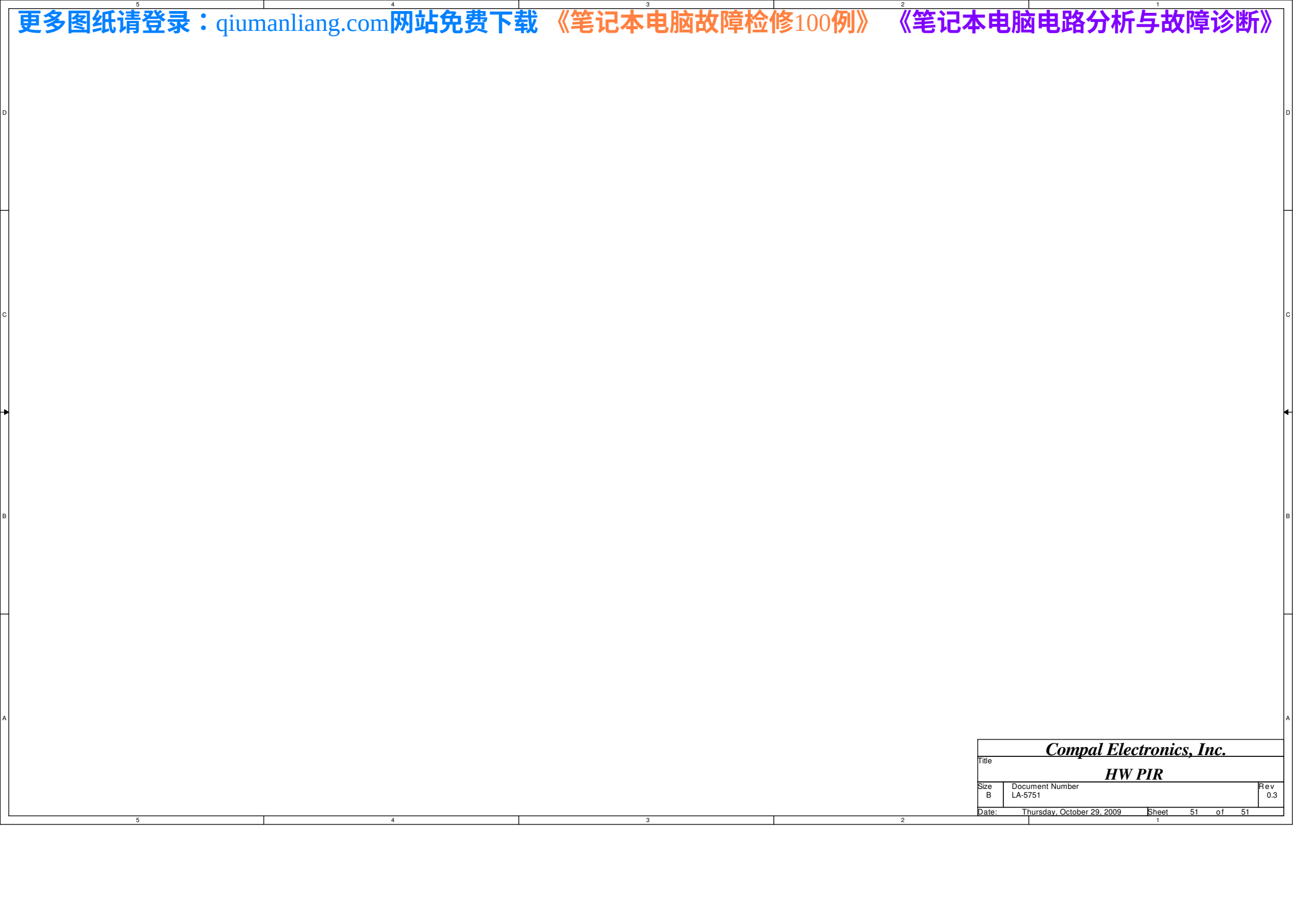
Version change list (P.I.R. List)

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