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S-SERIES 2009

INVICTA (Intel-Discrete)

MV Build (A03) - Final

2009.03.18

DATE	CHANGE NO.	REV

	EE	DATE	POWER	DATE
DRAWER				
DESIGN				
CHECK				
RESPONSIBLE				

SIZE = 3 VER :

FILE NAME : XXXX-XXXXXX-XX

P/N XXXXXXXXXXXX

INVENTEC

TITLE *INVICTA Cycle1*

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22527-0-MTR*	*A03*

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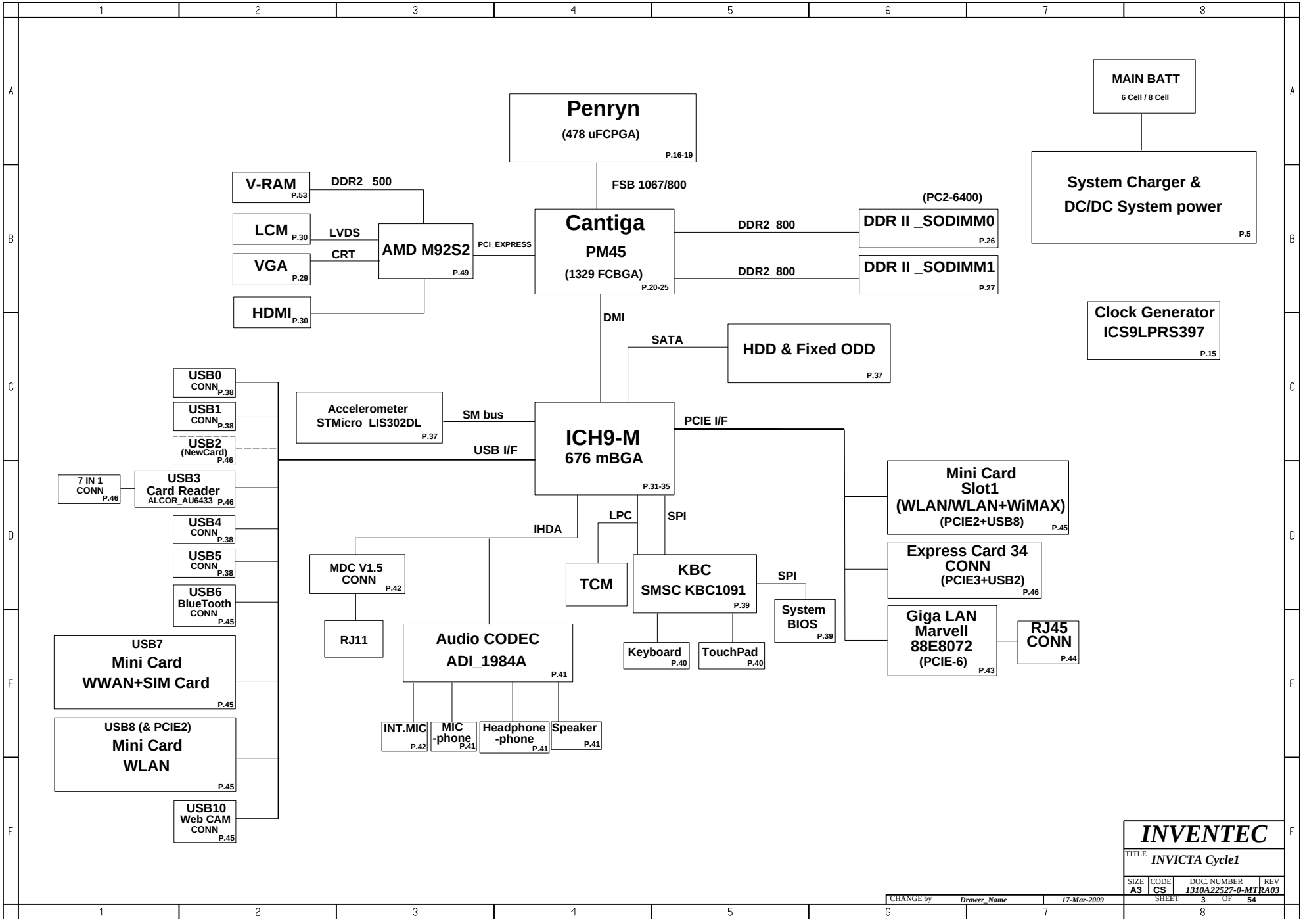

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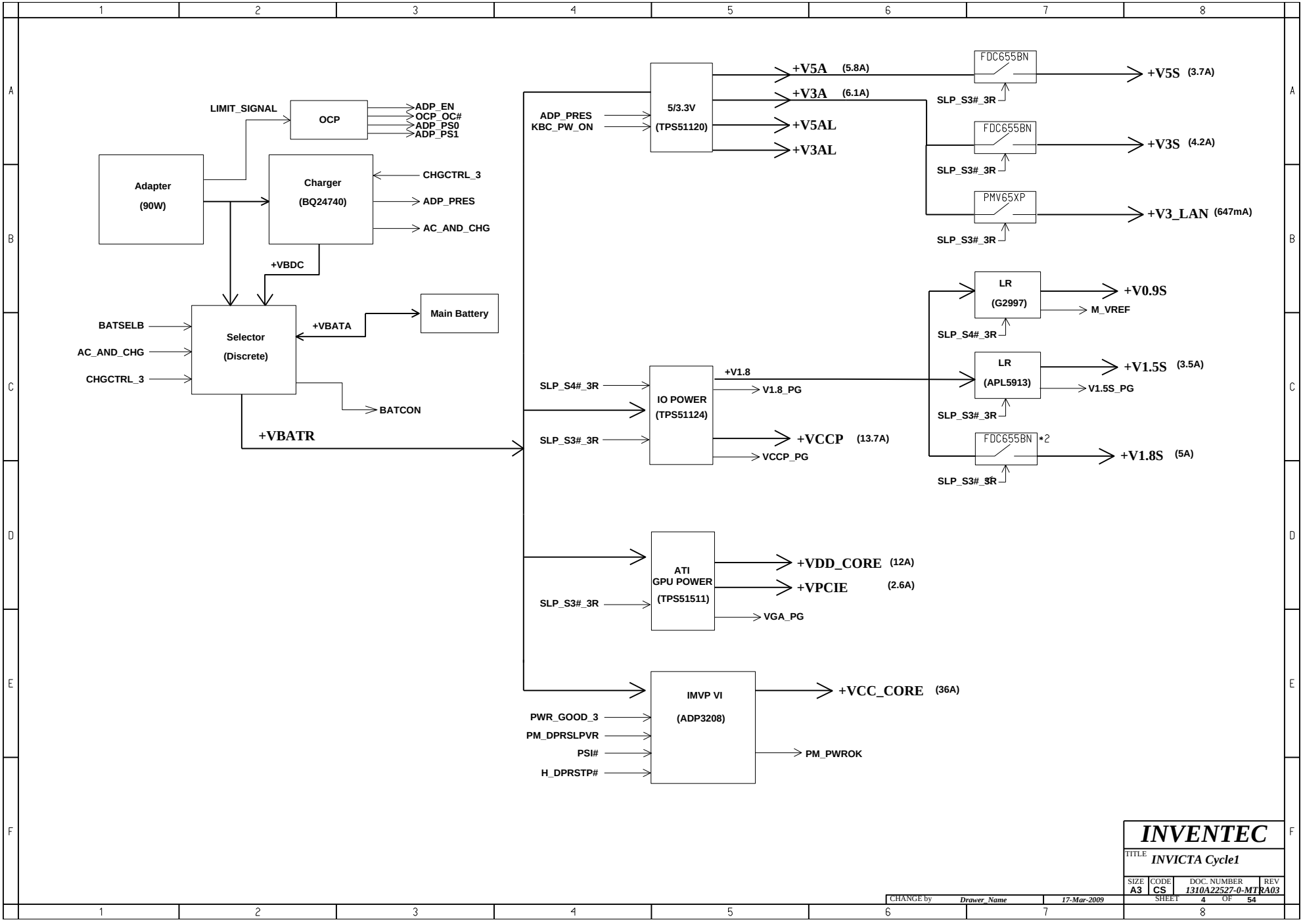

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TITLE: INVICTA Cycle1			
SIZE: A3	CODE: CS	DOC. NUMBER: 1310A22527-0-MTRA03	REV: 03
CHANGE by: Drawer_Name	17-Mar-2009	SHEET 4 OF 54	

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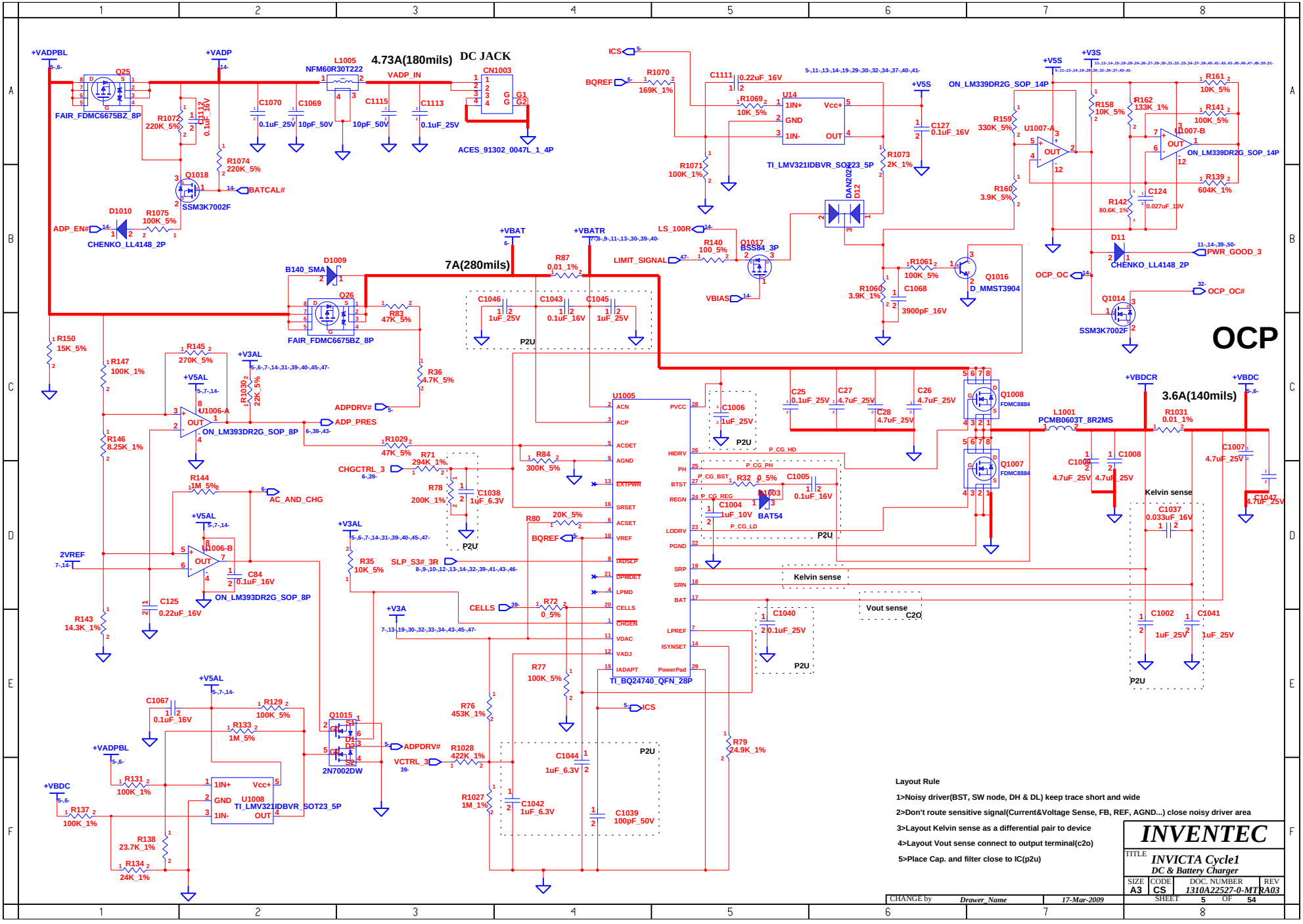

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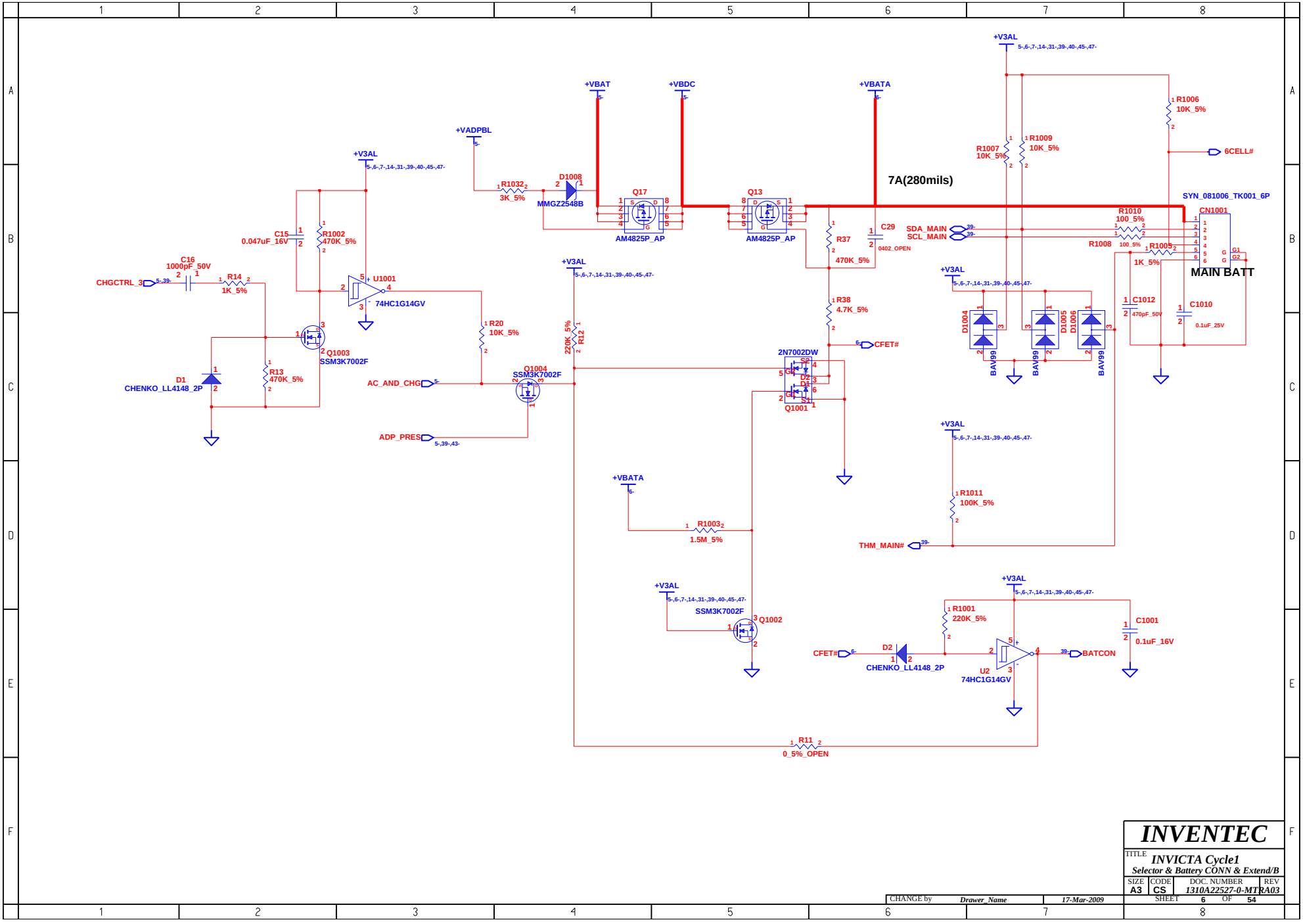

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SIZE: A3	CODE: CS	DOC. NUMBER: 1310A22527-0-MTRA03	REV:
CHANGE by: Drawer_Name	17-Mar-2009	SHEET 6 OF 54	

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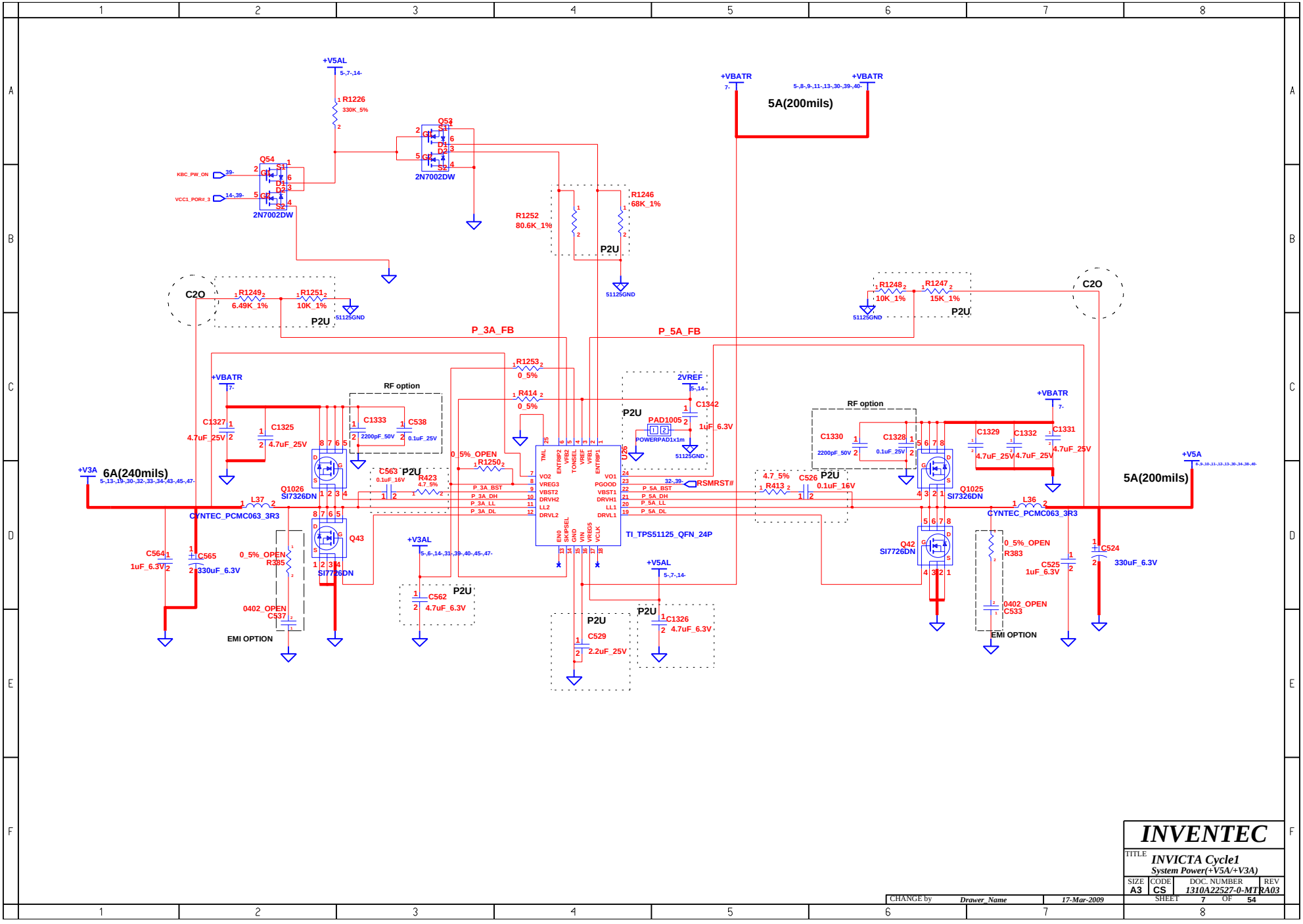

INVENTEC

TITLE: INVICTA Cycle1
System Power(+V5A/+V3A)

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22527-0-MTRA03	

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CHANGE by Drawer_Name 17-Mar-2009

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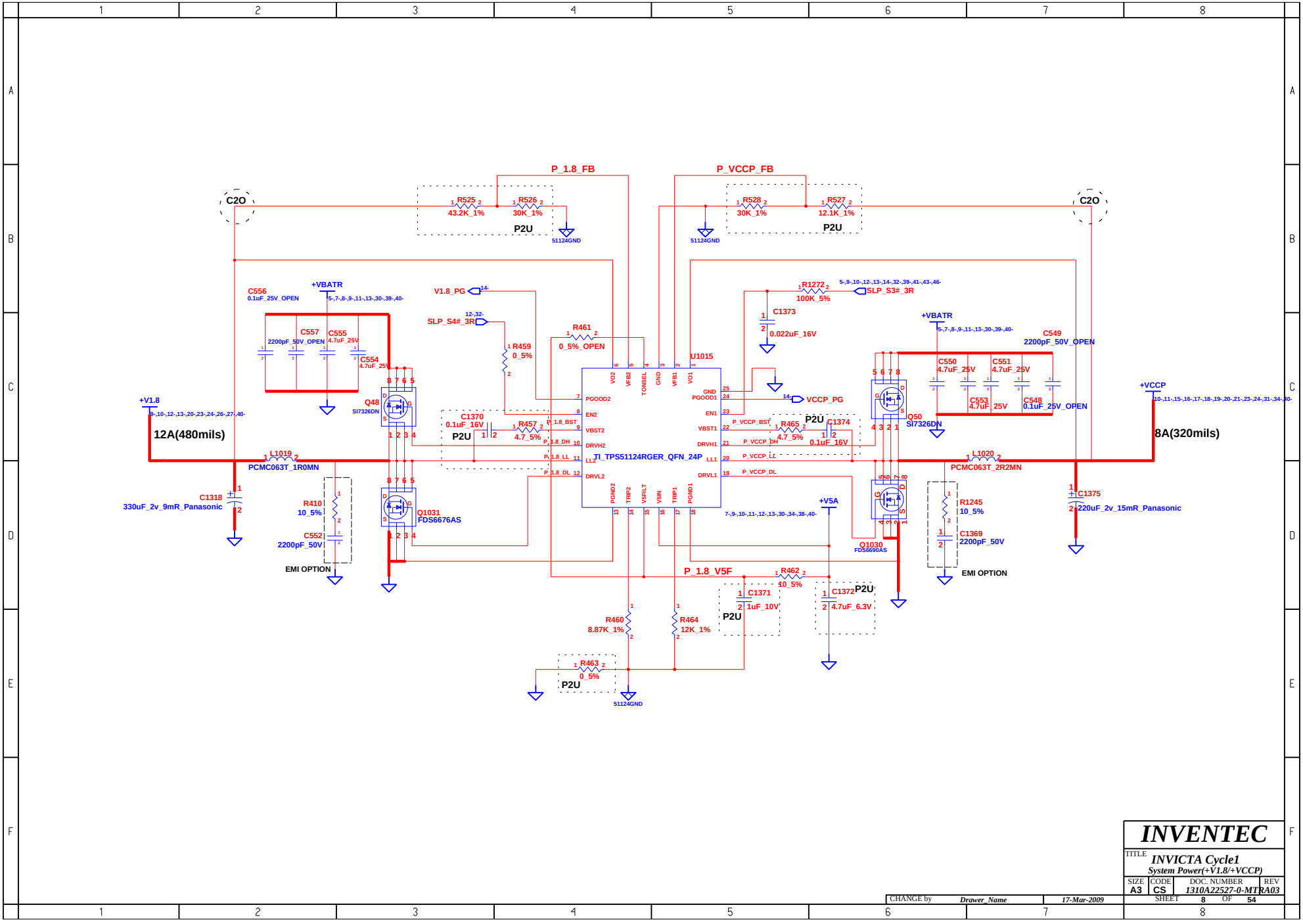

INVENTEC			
TITLE: INVICTA Cycle1 System Power(+V1.8/+VCCP)			
SIZE A3	CODE CS	DOC. NUMBER 1310A22527-0-MTRA03	REV
CHANGE by Drawer_Name	17-Mar-2009	SHEET 8 OF 54	

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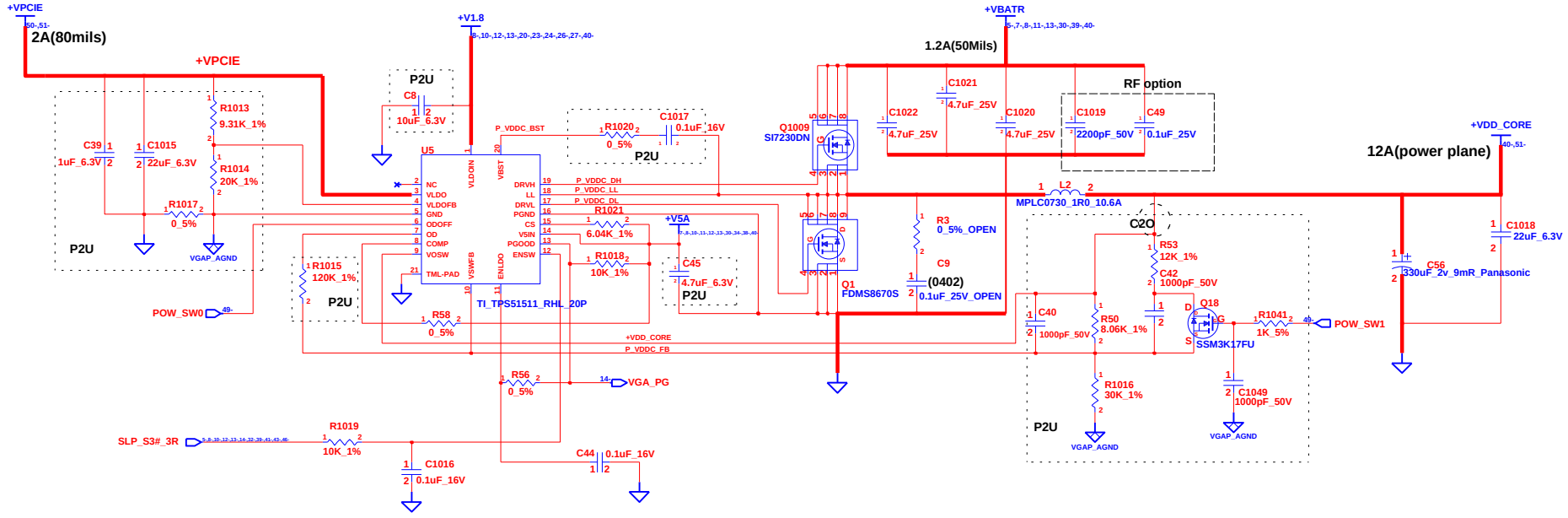
POW_SW1	POW_SW0	+VDD_CORE
0	0	1.0V
0	1	0.95V
1	0	0.9V



INVENTEC

TITLE
INVICTA Cycle1
Graphic Power (+VDD_CORE & +VPCIE)

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22527-0-MTRA03*	

CHANGE by *Drawer_Name* *17-Mar-2009*

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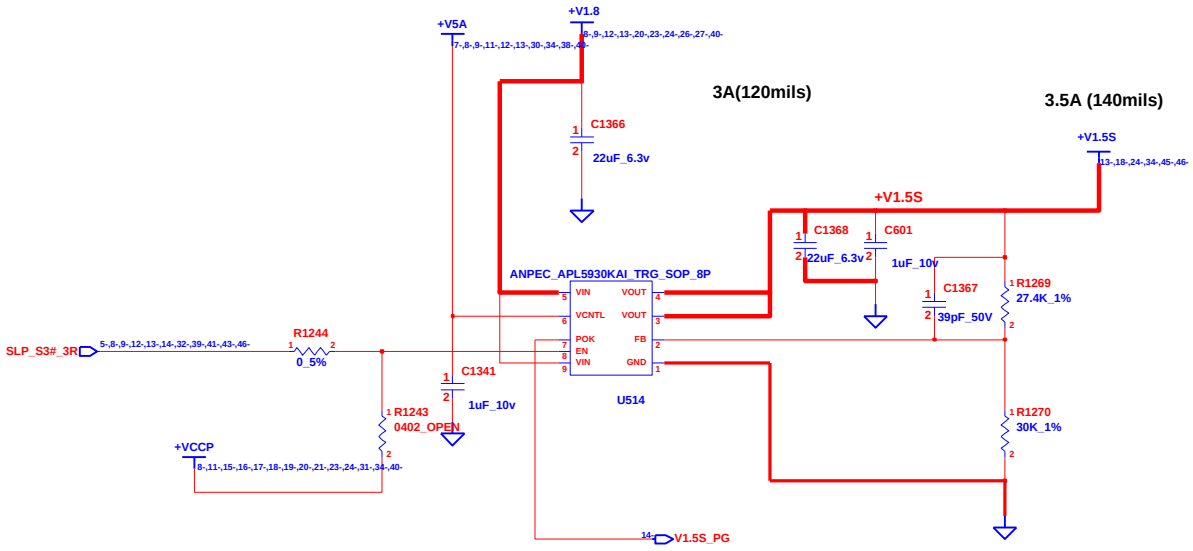

CHANGE by	Drawer_Name	17-Mar-2009	

INVENTEC

TITLE *INVICTA Cycle1*
System Power (+V1.5S)

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22527-0-MTRA03	

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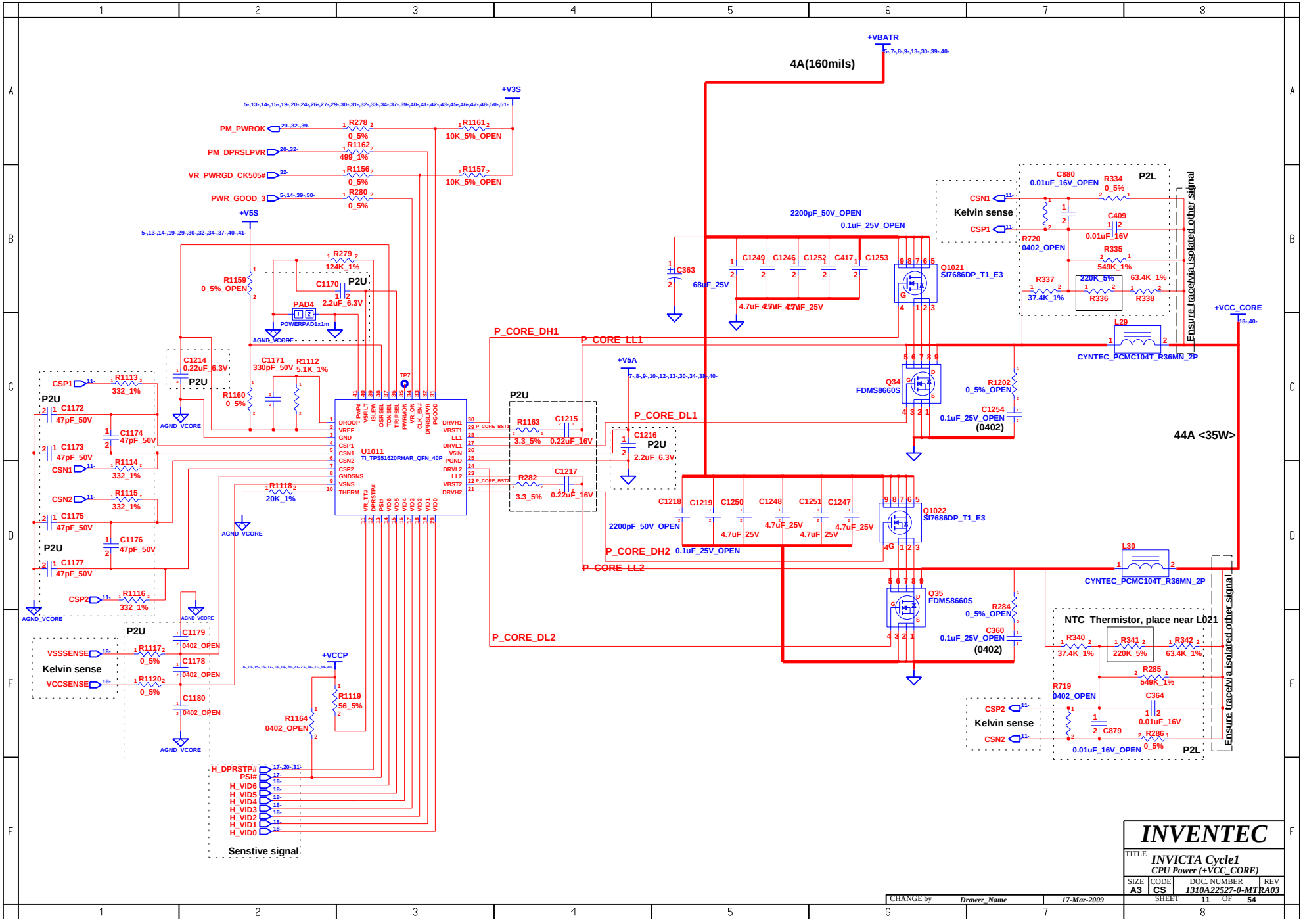

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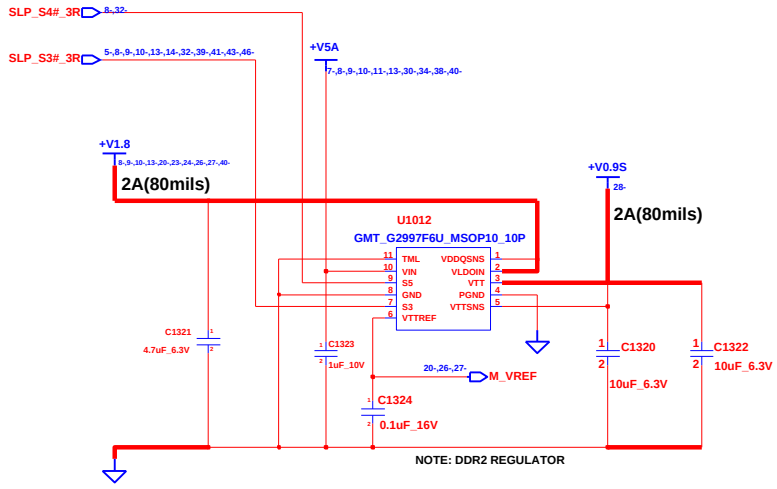

CHANGE by	Drawer_Name	17-Mar-2009	

INVENTEC

TITLE
INVICTA Cycle1
DDR Termination Voltage (+V0.9S)

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22527-0-MTRA03	

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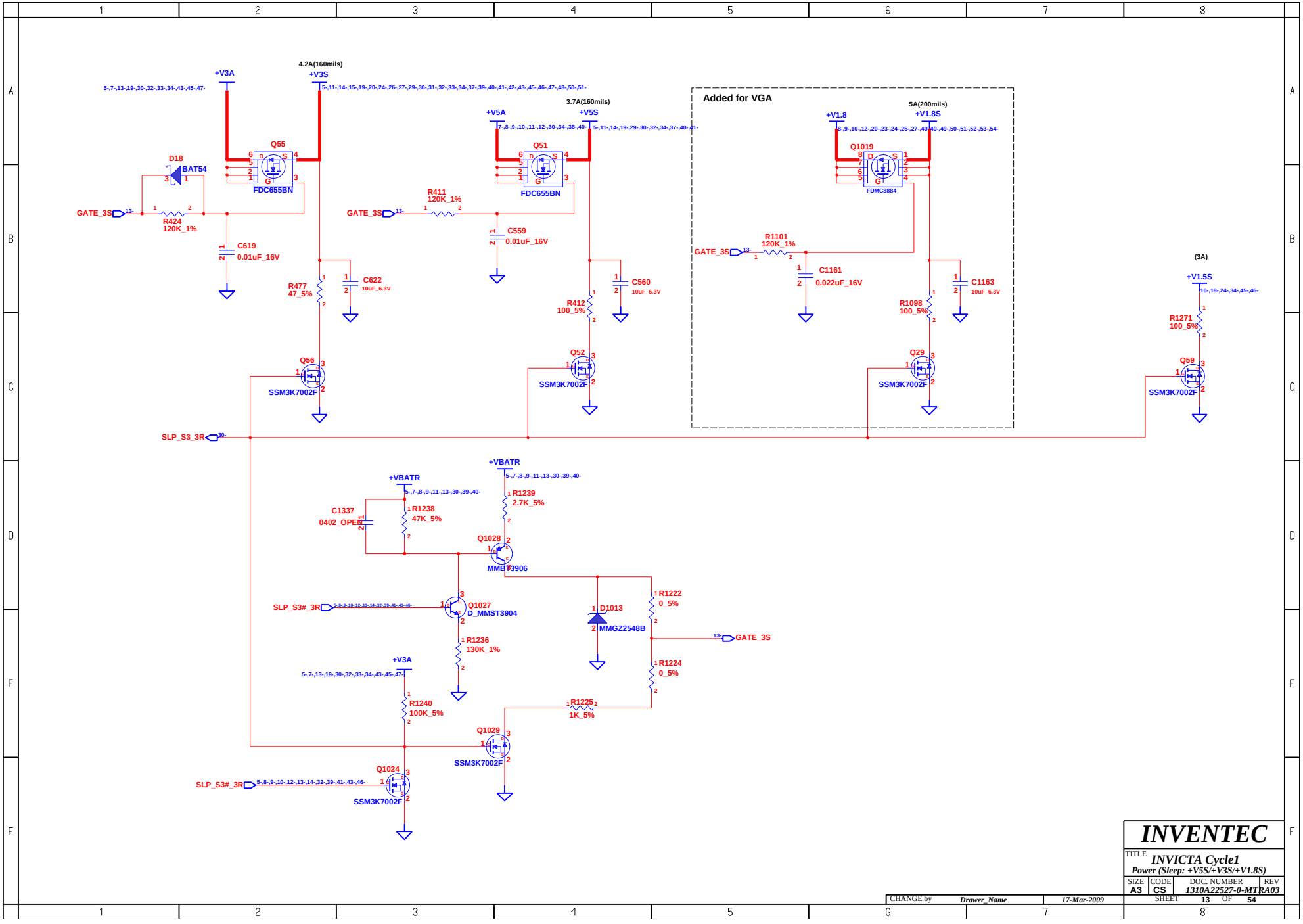

INVENTEC			
TITLE: INVICTA Cycle1 — Power (Sleep: +V5S/+V3S/+V1.8S)			
SIZE: A3	CODE: CS	DOC. NUMBER: 1310A22527-0-MTRA03	REV
CHANGE by: Drawer_Name	17-Mar-2009	SHEET 13 OF 54	

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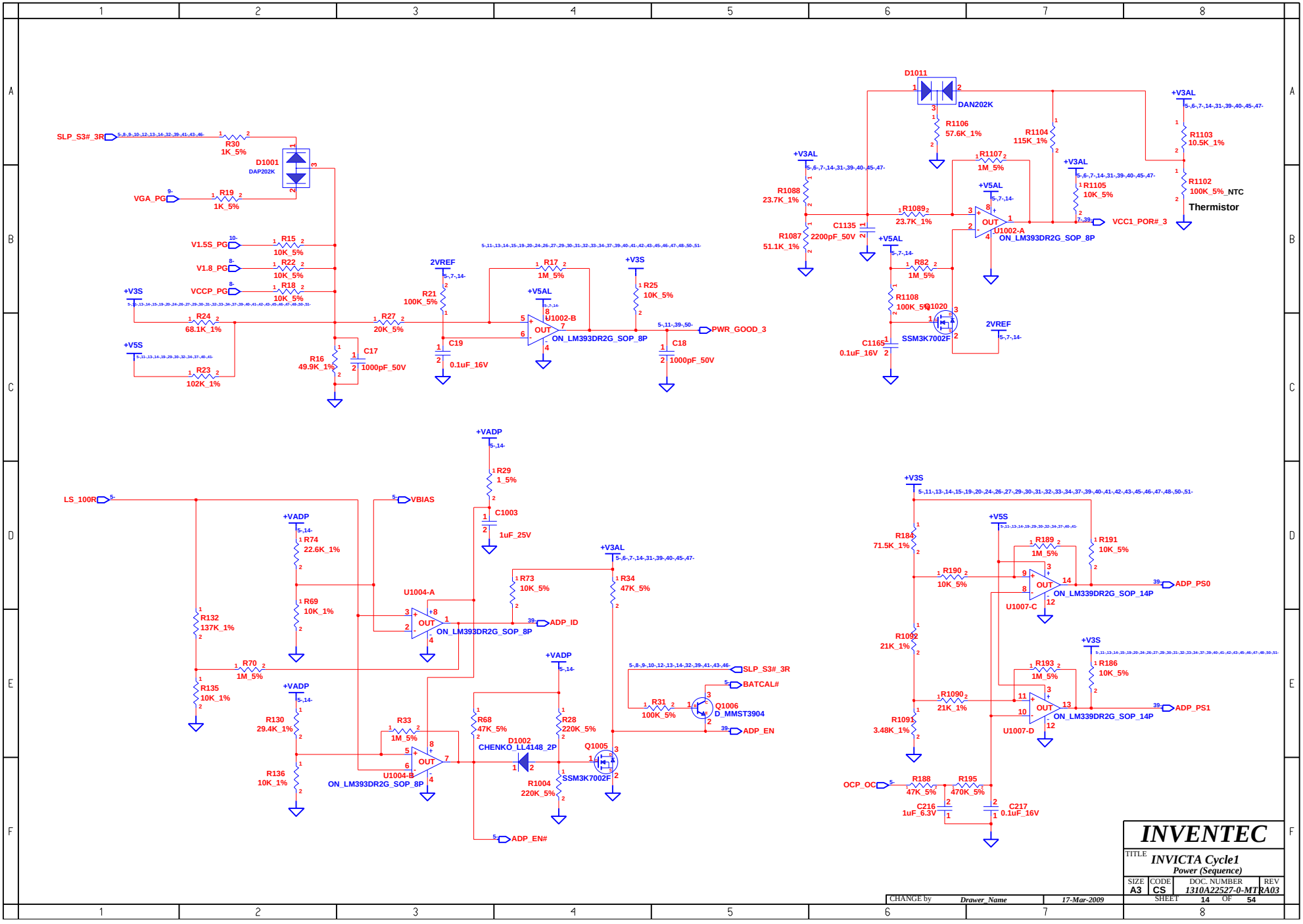

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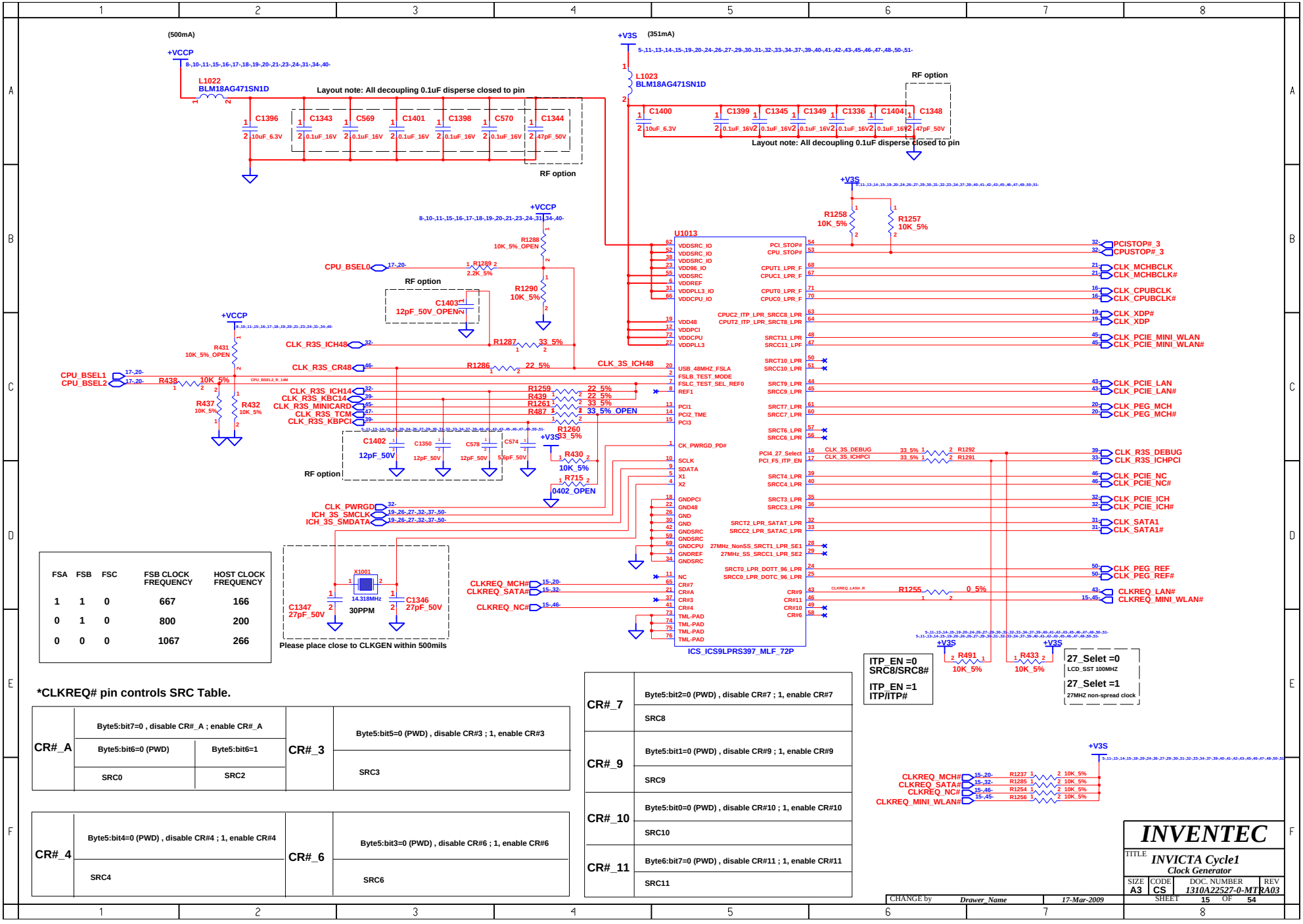

FSA	FSB	FSC	FSB CLOCK FREQUENCY	HOST CLOCK FREQUENCY
1	1	0	667	166
0	1	0	800	200
0	0	0	1067	266

***CLKREQ# pin controls SRC Table.**

CR#_A	Byte5:bit7=0 , disable CR#_A ; enable CR#_A		CR#_3	Byte5:bit5=0 (PWD) , disable CR#3 ; 1, enable CR#3
	Byte5:bit6=0 (PWD)	Byte5:bit6=1		SRC3
	SRC0	SRC2		

CR#_4	Byte5:bit4=0 (PWD) , disable CR#4 ; 1, enable CR#4	CR#_6	Byte5:bit3=0 (PWD) , disable CR#6 ; 1, enable CR#6
	SRC4		SRC6

CR#_7	Byte5:bit2=0 (PWD) , disable CR#7 ; 1, enable CR#7
	SRC8
CR#_9	Byte5:bit1=0 (PWD) , disable CR#9 ; 1, enable CR#9
	SRC9
CR#_10	Byte5:bit0=0 (PWD) , disable CR#10 ; 1, enable CR#10
	SRC10
CR#_11	Byte6:bit7=0 (PWD) , disable CR#11 ; 1, enable CR#11
	SRC11

INVENTEC

TITLE *INVICTA Cycle1*
Clock Generator

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22527-0-MTRA03	

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CHANGE by *Drawer_Name* *17-Mar-2009*

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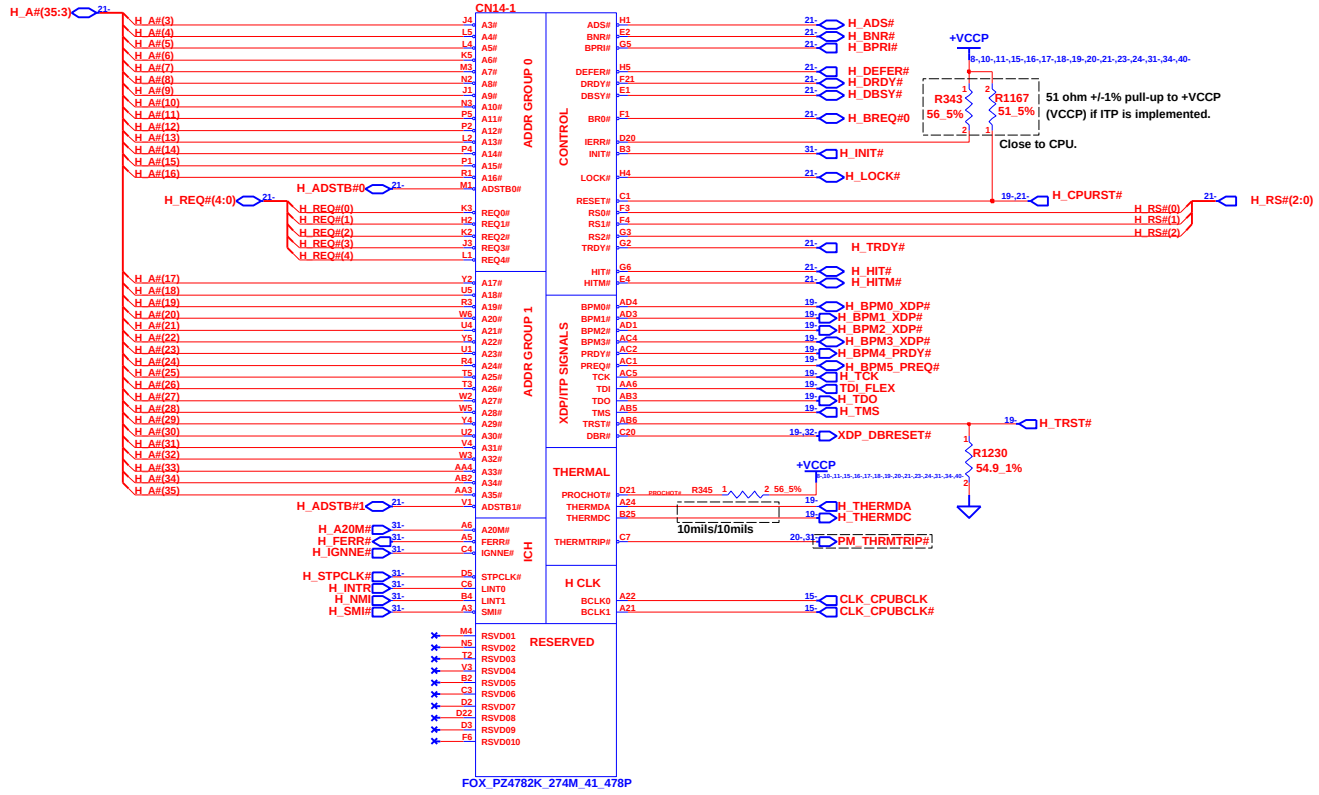

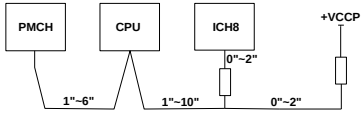

PM_THRMTRIP# should be T at CPU

CHANGE by	Drawer_Name	17-Mar-2009	

INVENTEC

TITLE *INVICTA Cycle1*
CPU Penryn-1

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22527-0-MTRA03	

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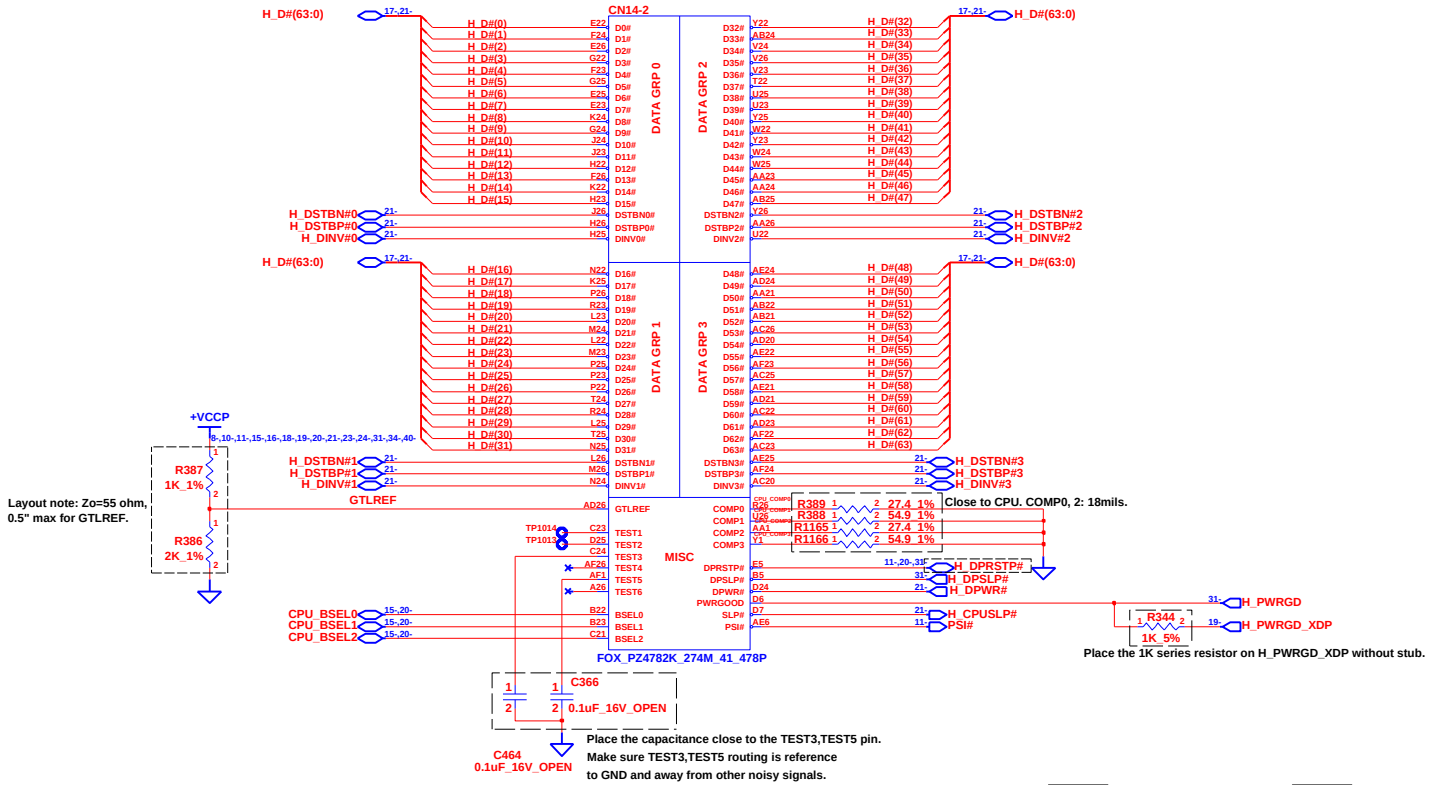

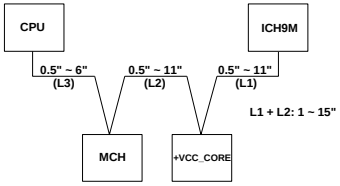

H_DPRSTP# topology

CHANGE by	Drawer_Name	17-Mar-2009	

INVENTEC

TITLE: *INVICTA Cycle1*
CPU Penryn-2

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22527-0-MTRA03	

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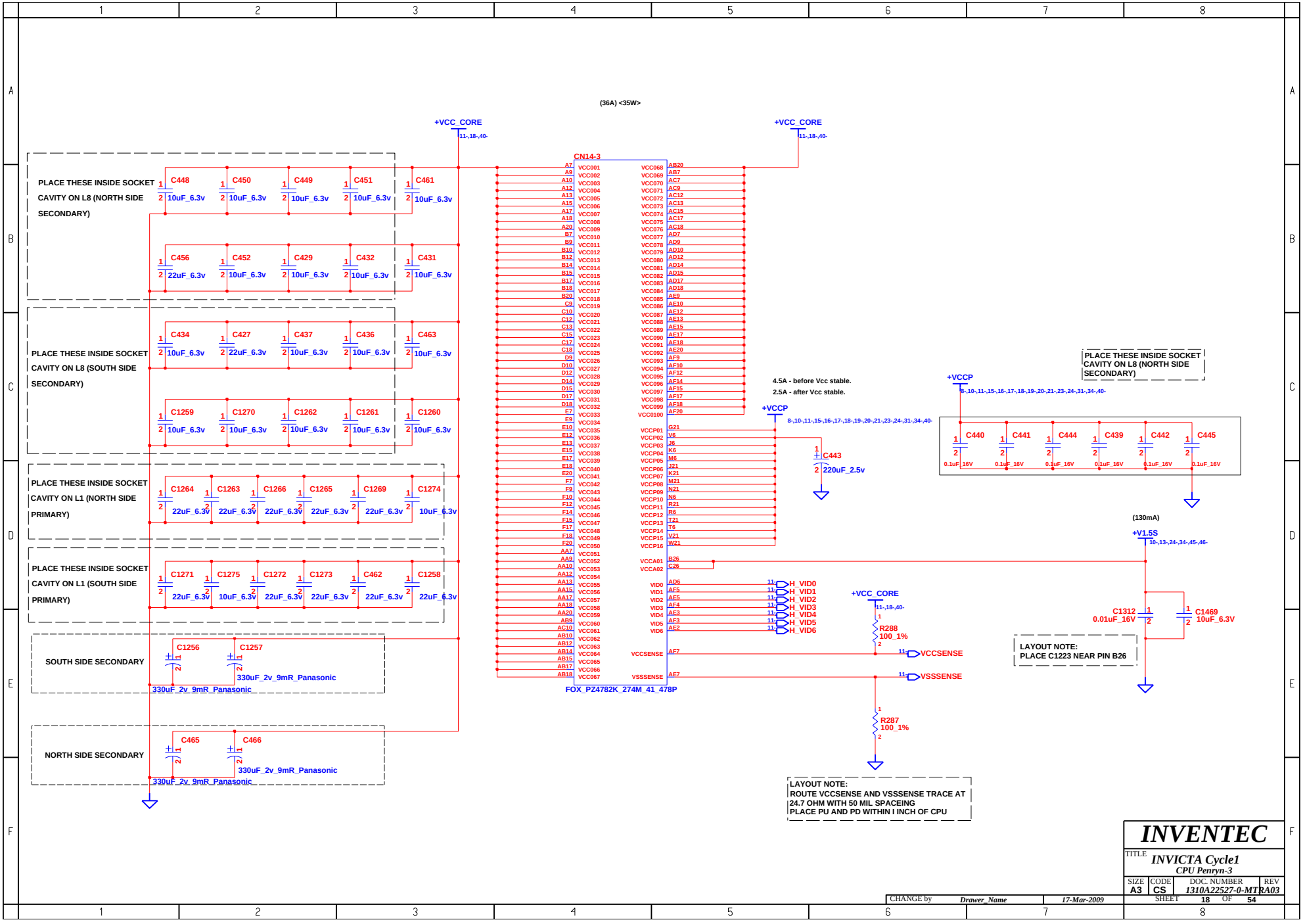

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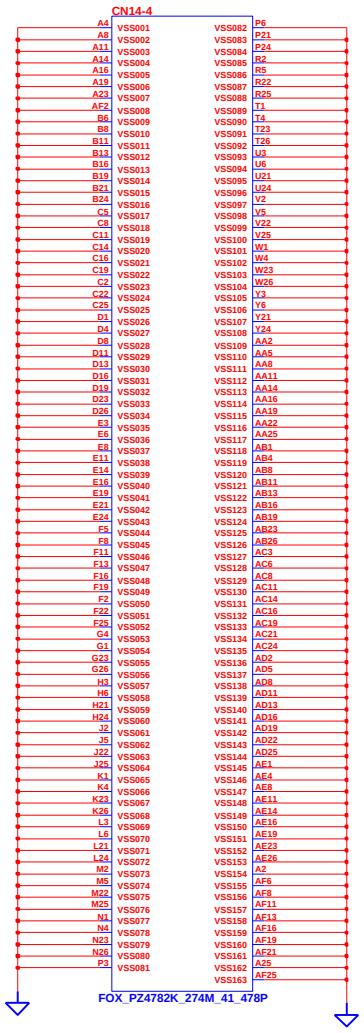
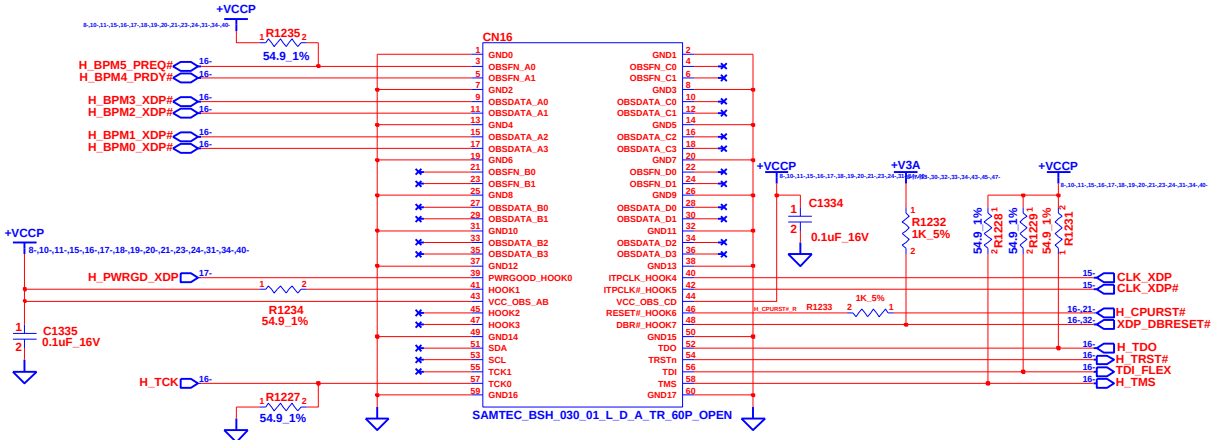
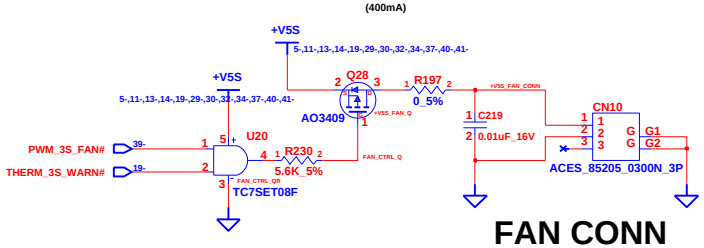
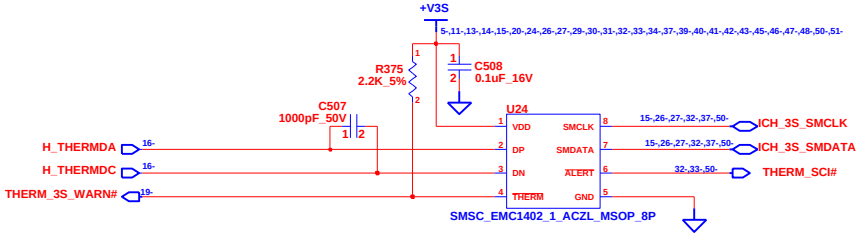




XDP CONNECTOR



FAN CONN



CHANGE by	Drawer_Name	17-Mar-2009	

INVENTEC

TITLE: *INVICTA Cycle1*
XDP & Thermal & Fan

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22527-0-MTRA03	

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MCH_CFG(5)	LOW=DMIx2 HIGH=DMIx4

MCH_CFG(7) (CPU Strap)	LOW=RSVD HIGH=Mobile CPU

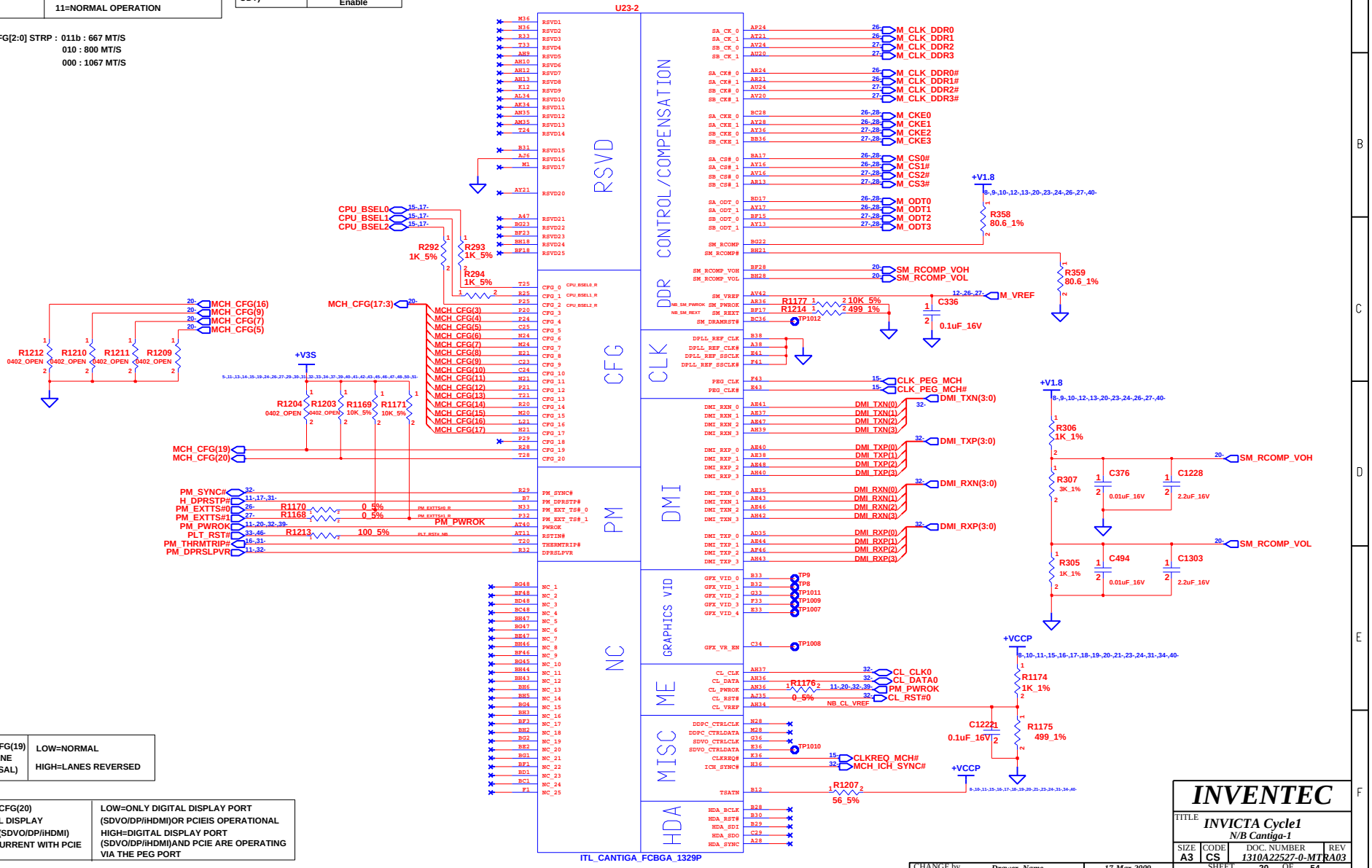
MCH_CFG(9) PCIE Graphics Lane	LOW=Reverse Lane HIGH=Normal operation

NOTE : USE 4K-OHM RESISTOR WHEN INSTALLING PULL-UP/PULL-DOWN RESISTOR ON ANY MCH-CFG CONNECTION/PINS.

MCH_CFG(13:12) XOR/ALLZ	00=PARTIAL CLOCK GATING DISABLE 01=XOR MODE ENABLE 10=ALL-Z MODE ENABLE 11=NORMAL OPERATION

MCH_CFG(16) (FSB Dynamic ODT)	LOW=Dynamic ODT Disable HIGH=Dynamic ODT Enable

NOTE: CFG[2:0] STRP : 011b : 667 MT/S
010 : 800 MT/S
000 : 1067 MT/S



MCH_CFG(19) (DMI LANE REVERSAL)	LOW=NORMAL HIGH=LANES REVERSED

MCH_CFG(20) DIGIAL DISPLAY PORT(SDVO/DP/iHDMI) CONCURRENT WITH PCIE	LOW=ONLY DIGITAL DISPLAY PORT (SDVO/DP/iHDMI)OR PCIEIS OPERATIONAL HIGH=DIGITAL DISPLAY PORT (SDVO/DP/iHDMI)AND PCIE ARE OPERATING VIA THE PEG PORT

CHANGE by	Drawer_Name	17-Mar-2009	

INVENTEC

TITLE *INVICTA Cycle1*
N/B Cantiga-1

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22527-0-MTRA03	

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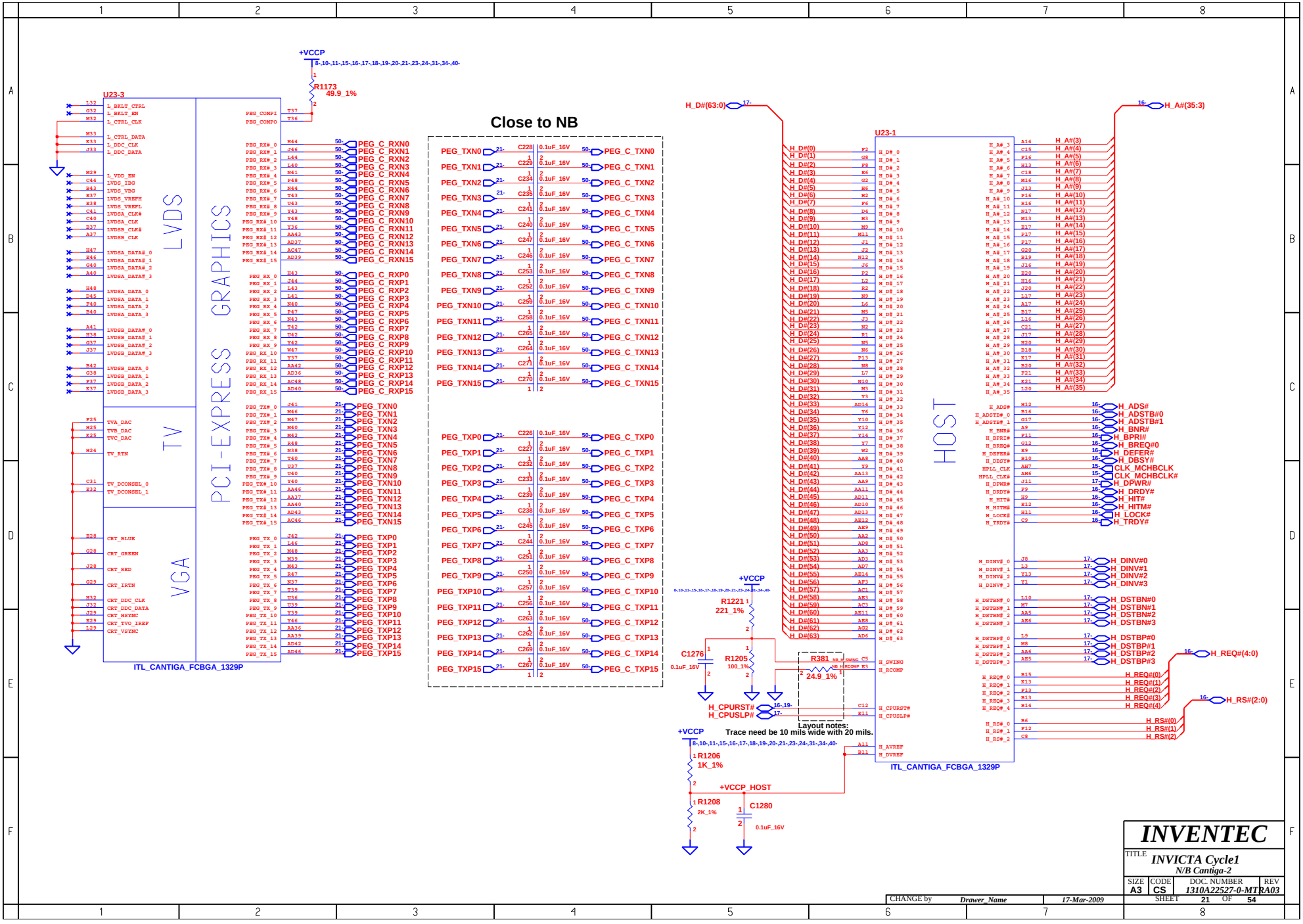

CHANGE by	Drawer_Name	17-Mar-2009	

INVENTEC

TITLE: *INVICTA Cycle1*
N/B Cantiga-2

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22527-0-MTRA03	

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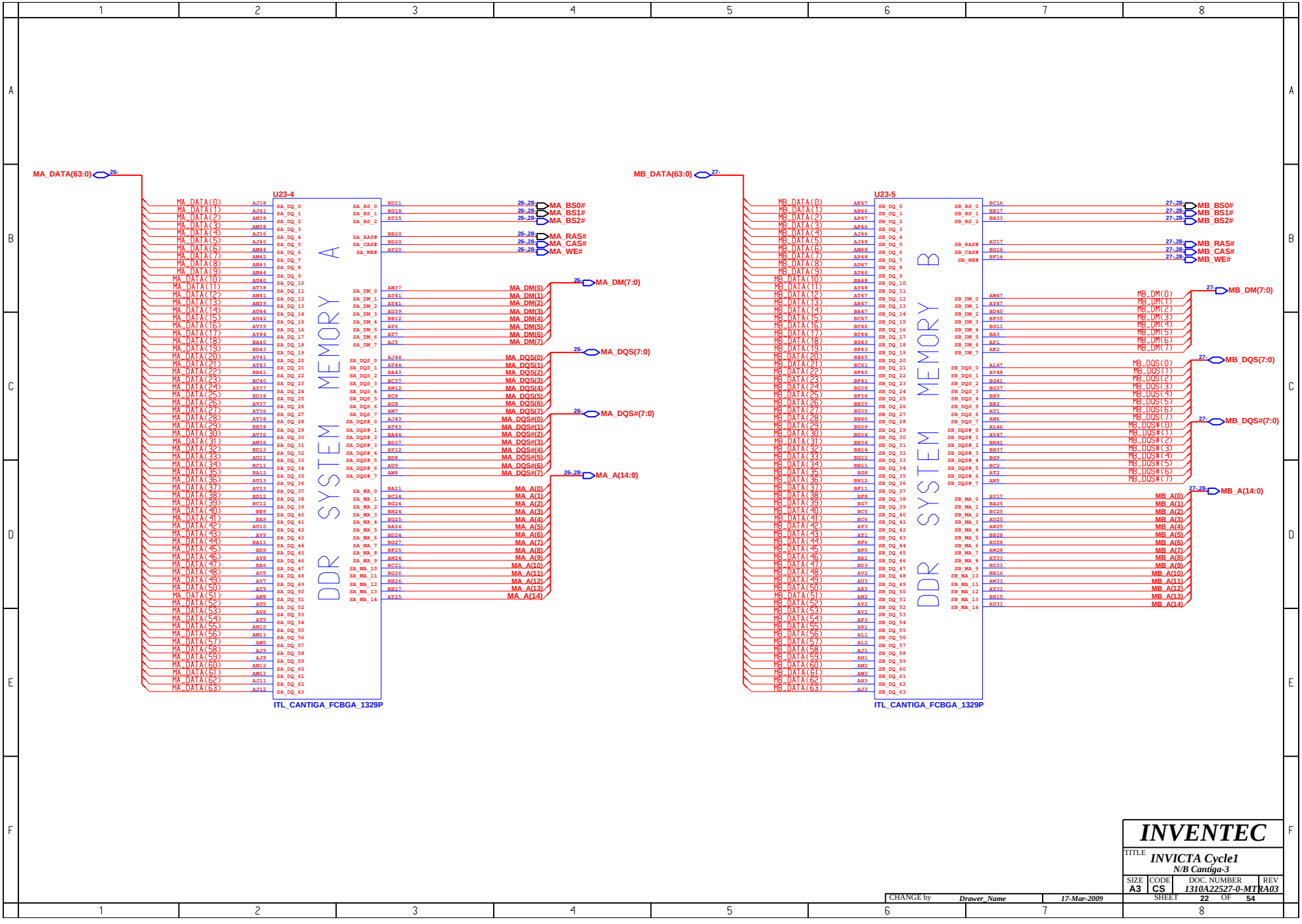

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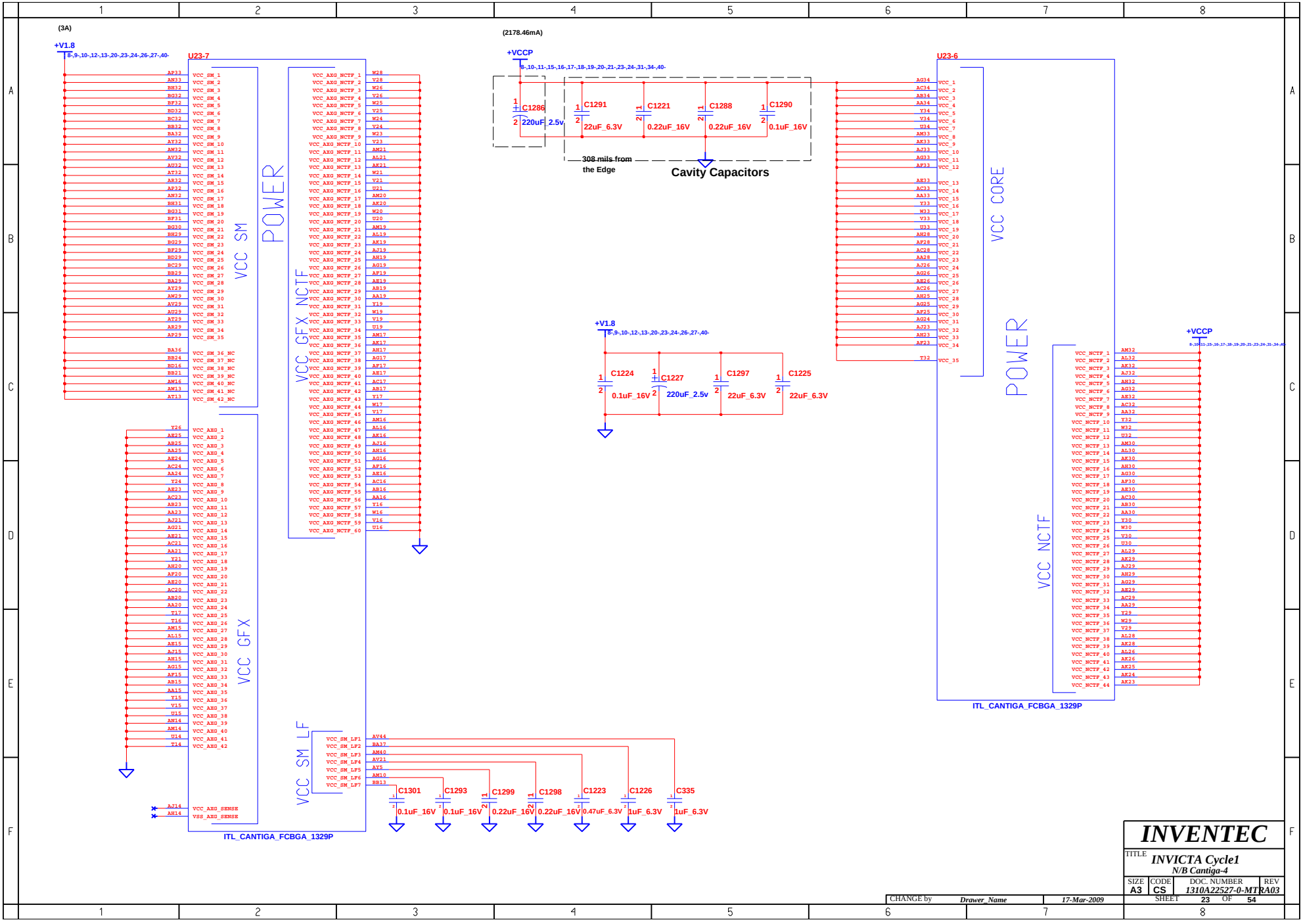

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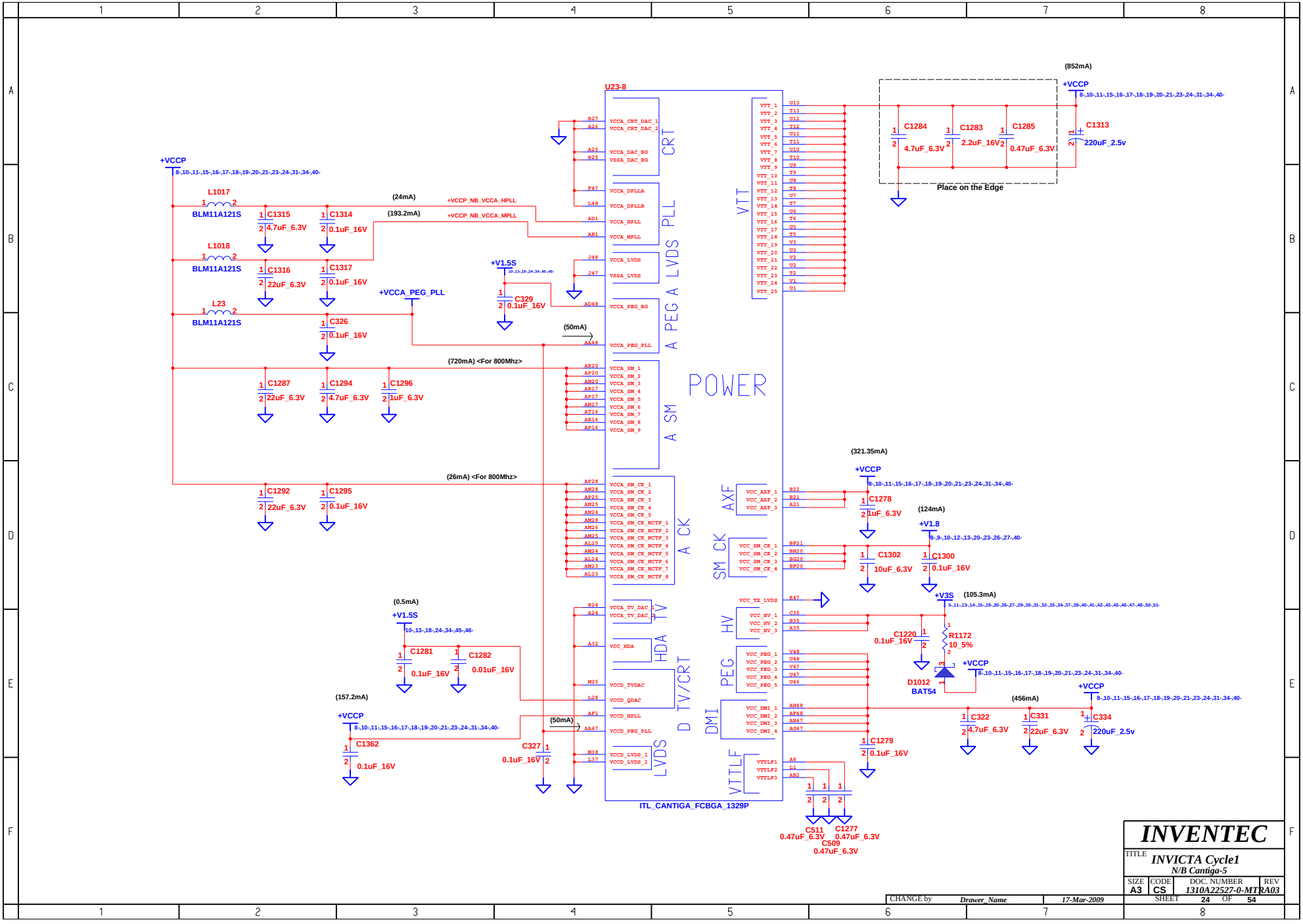

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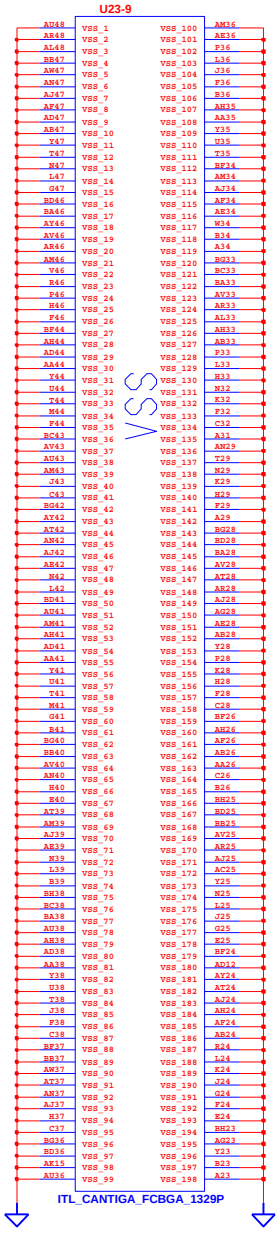

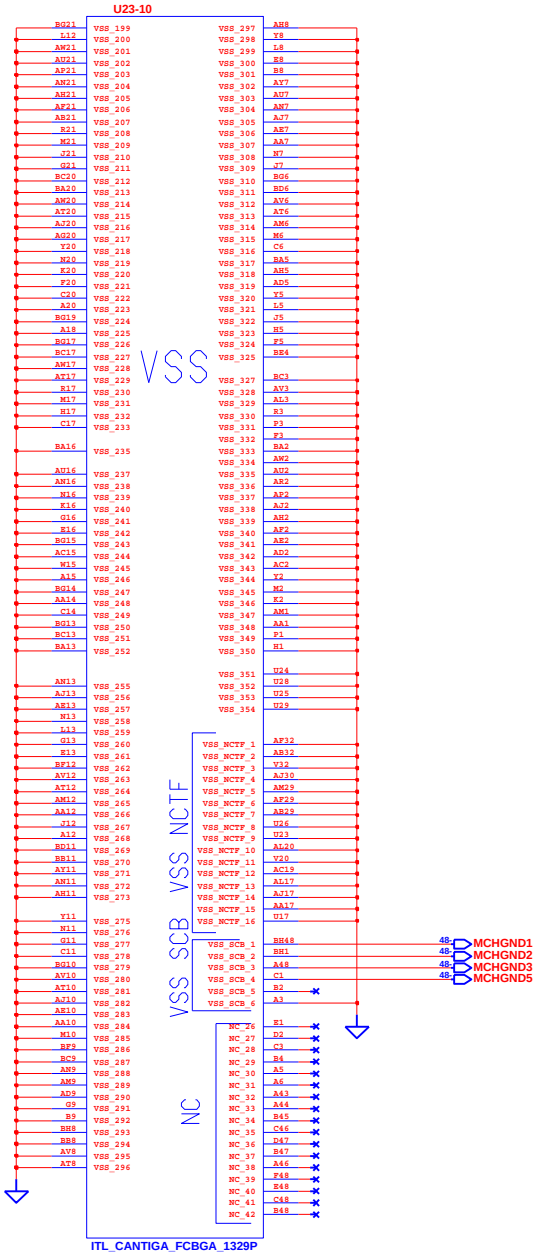

INVENTEC			
TITLE	INVICTA Cycle1 N/B Cantiga-6		
SIZE A3	CODE CS	DOC. NUMBER 1310A22527-0-MTRA03	REV
CHANGE by Drawer_Name	17-Mar-2009	SHEET 25 OF 54	

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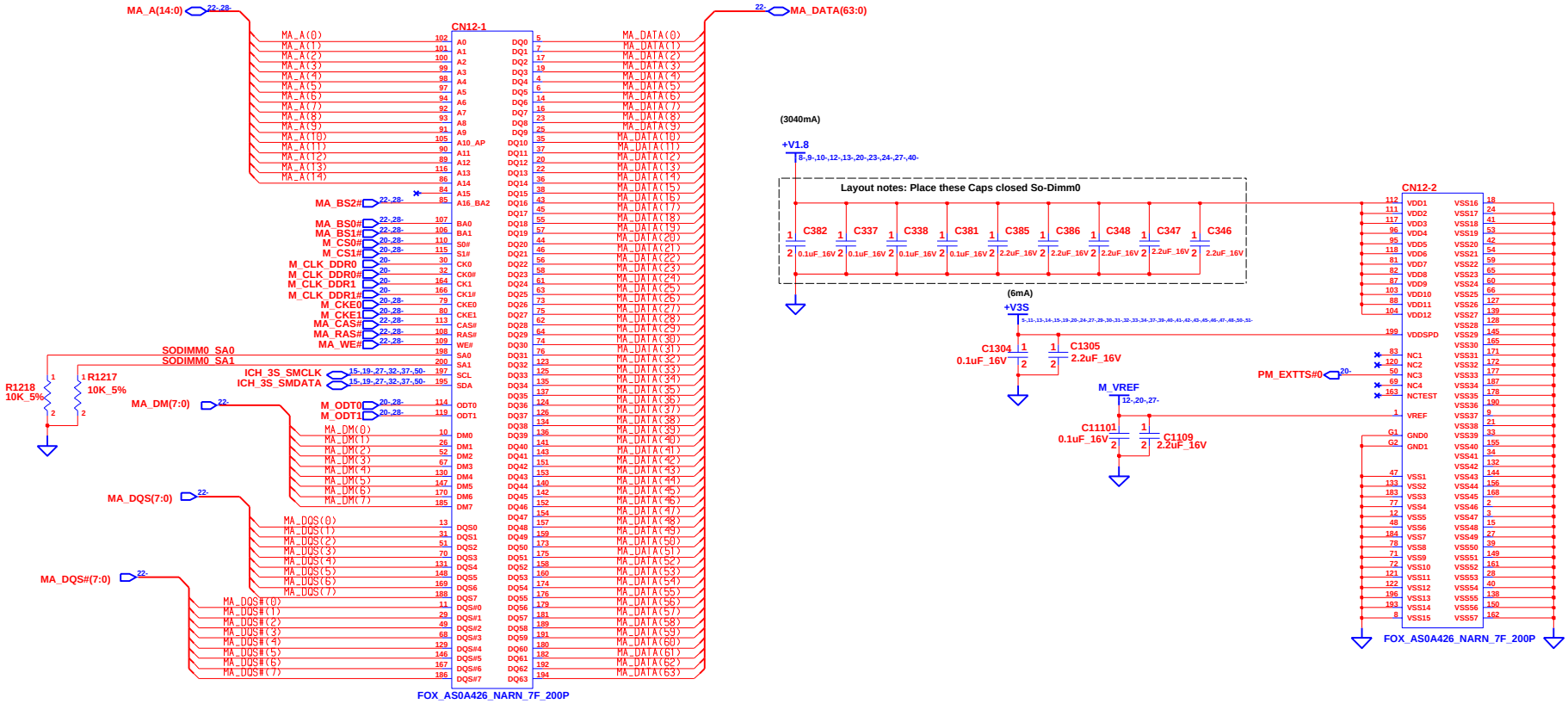

SO DIMM0_9.2mm

INVENTEC			
TITLE: INVICTA Cycle1 DDR2 DIMM0			
SIZE A3	CODE CS	DOC. NUMBER 1310A22527-0-MTRA03	REV 03
CHANGE by Drawer_Name	17-Mar-2009	SHEET 26 OF 54	

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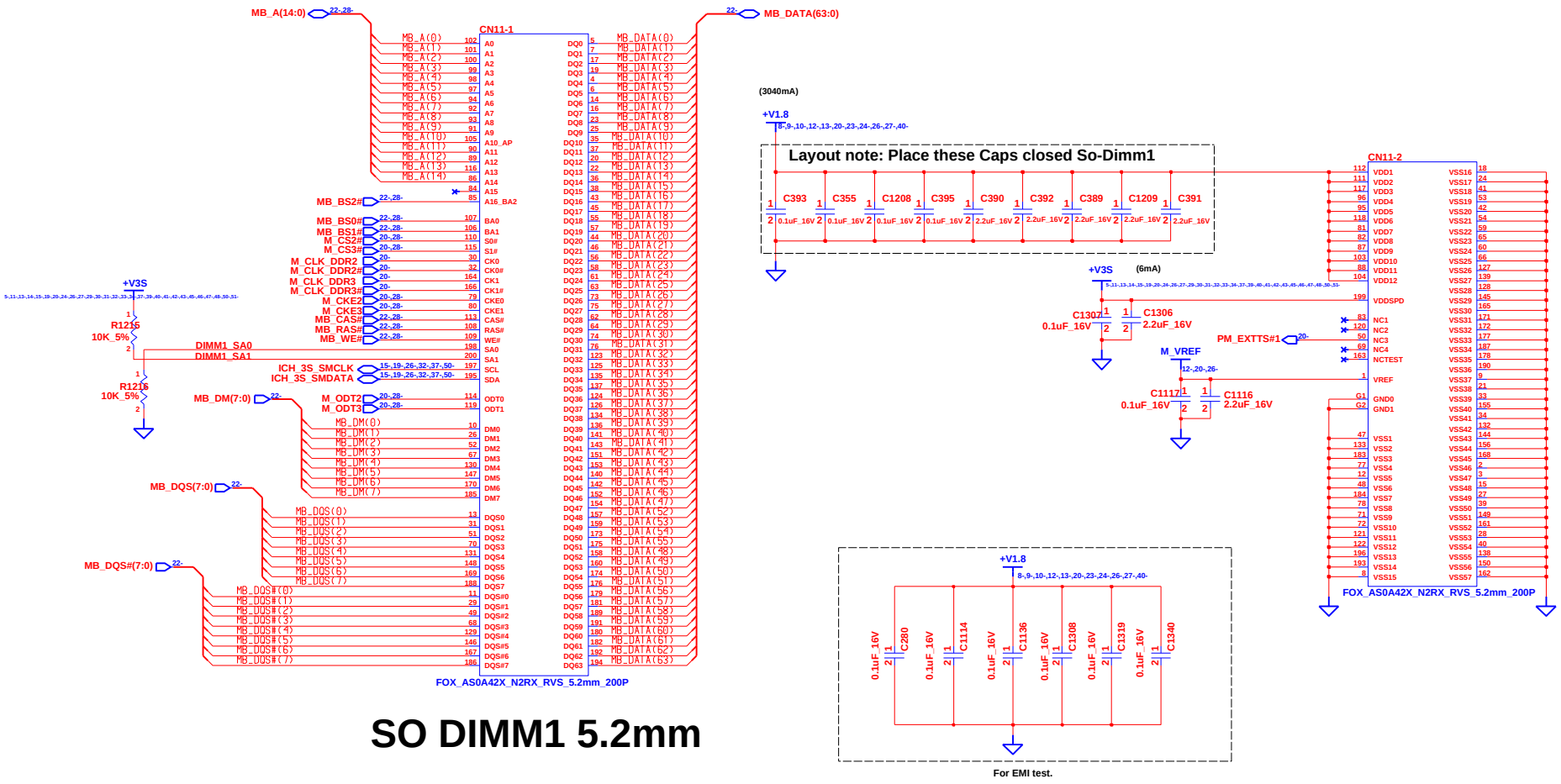

SO DIMM1 5.2mm

CHANGE by	Drawer_Name	17-Mar-2009	

INVENTEC

TITLE: *INVICTA Cycle1*
DDR2 DIMM1

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22527-0-MTRA	03

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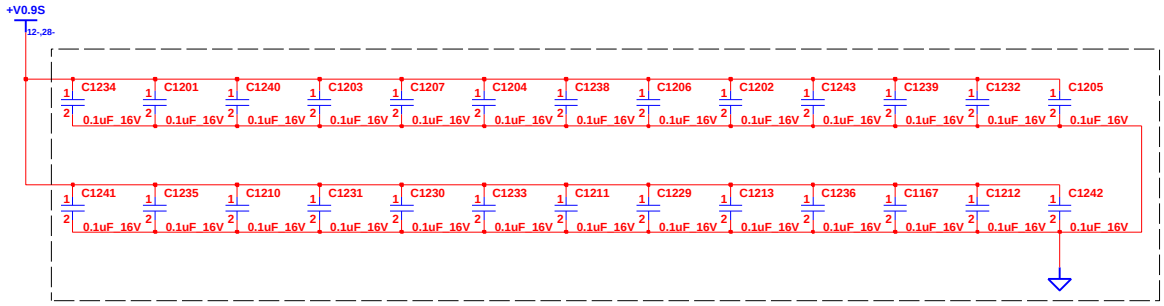
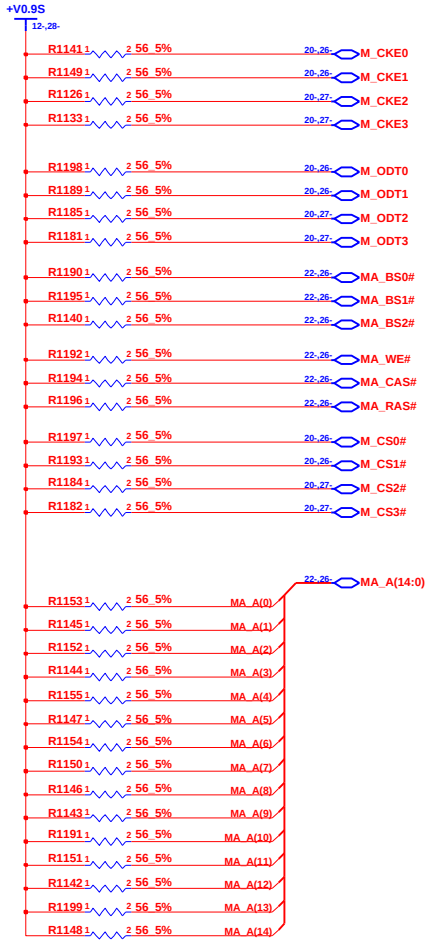
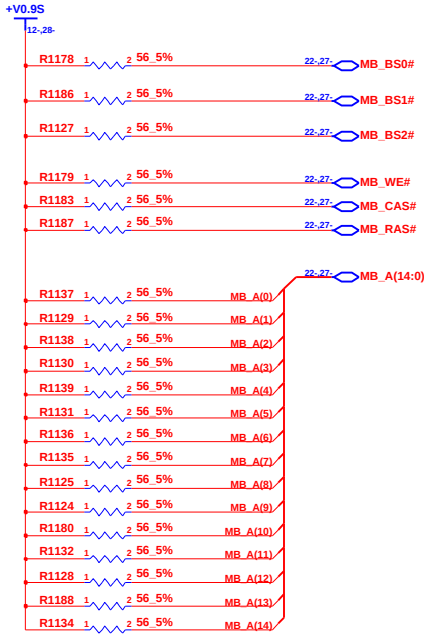


Layout notes : Place one Cap close to every 2 pull up resistor terminated to +V0.9S.





CHANGE by	Drawer_Name	27-Sep-2003	

INVENTEC

TITLE: *INVICTA Cycle1*
DDR2 termination

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22527-0-MTRA03	

SHEET 28 OF 54

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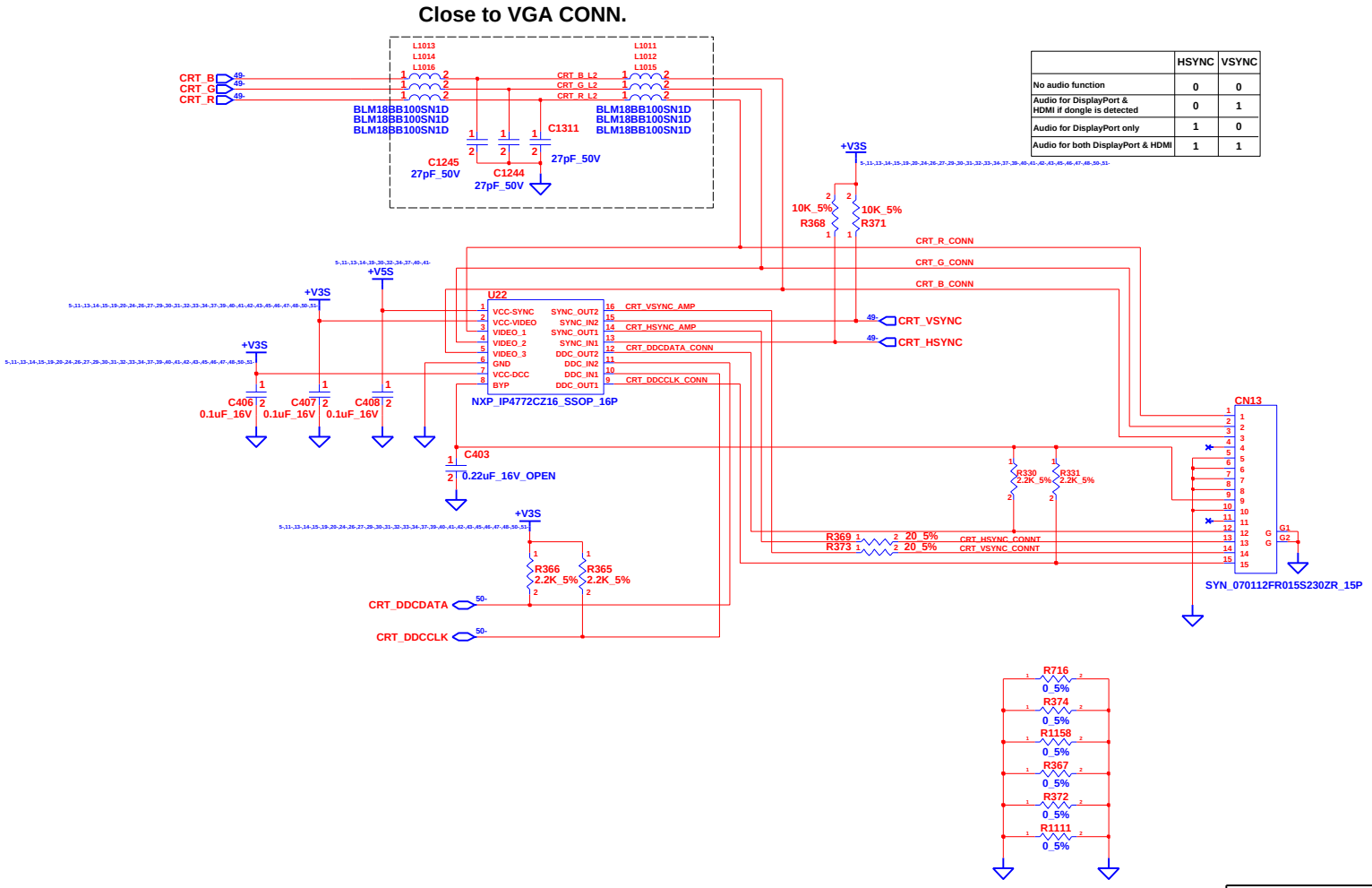

	HSYNC	VSYNC
No audio function	0	0
Audio for DisplayPort & HDMI if dongle is detected	0	1
Audio for DisplayPort only	1	0
Audio for both DisplayPort & HDMI	1	1

INVENTEC

TITLE *INVICTA Cycle1*
VGA CONN

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22527-0-MTRA03	

CHANGE by *Drawer_Name* *17-Mar-2009*

SHEET 29 OF 54

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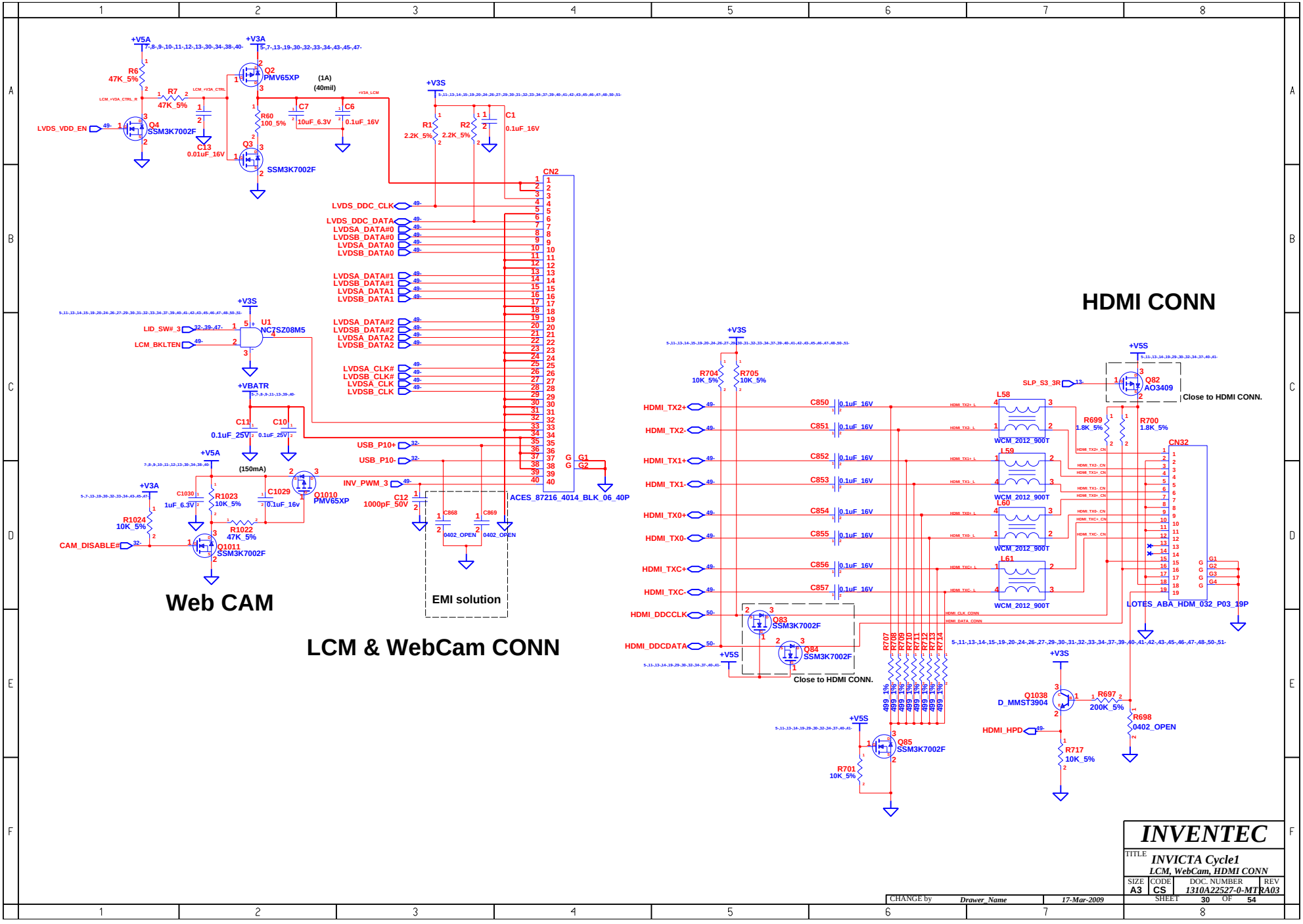

INVENTEC			
TITLE	INVICTA Cycle1 LCM, WebCam, HDMI CONN		
SIZE A3	CODE CS	DOC. NUMBER 1310A22527-0-MTRA03	REV
CHANGE by Drawer_Name	17-Mar-2009	SHEET 30 OF 54	

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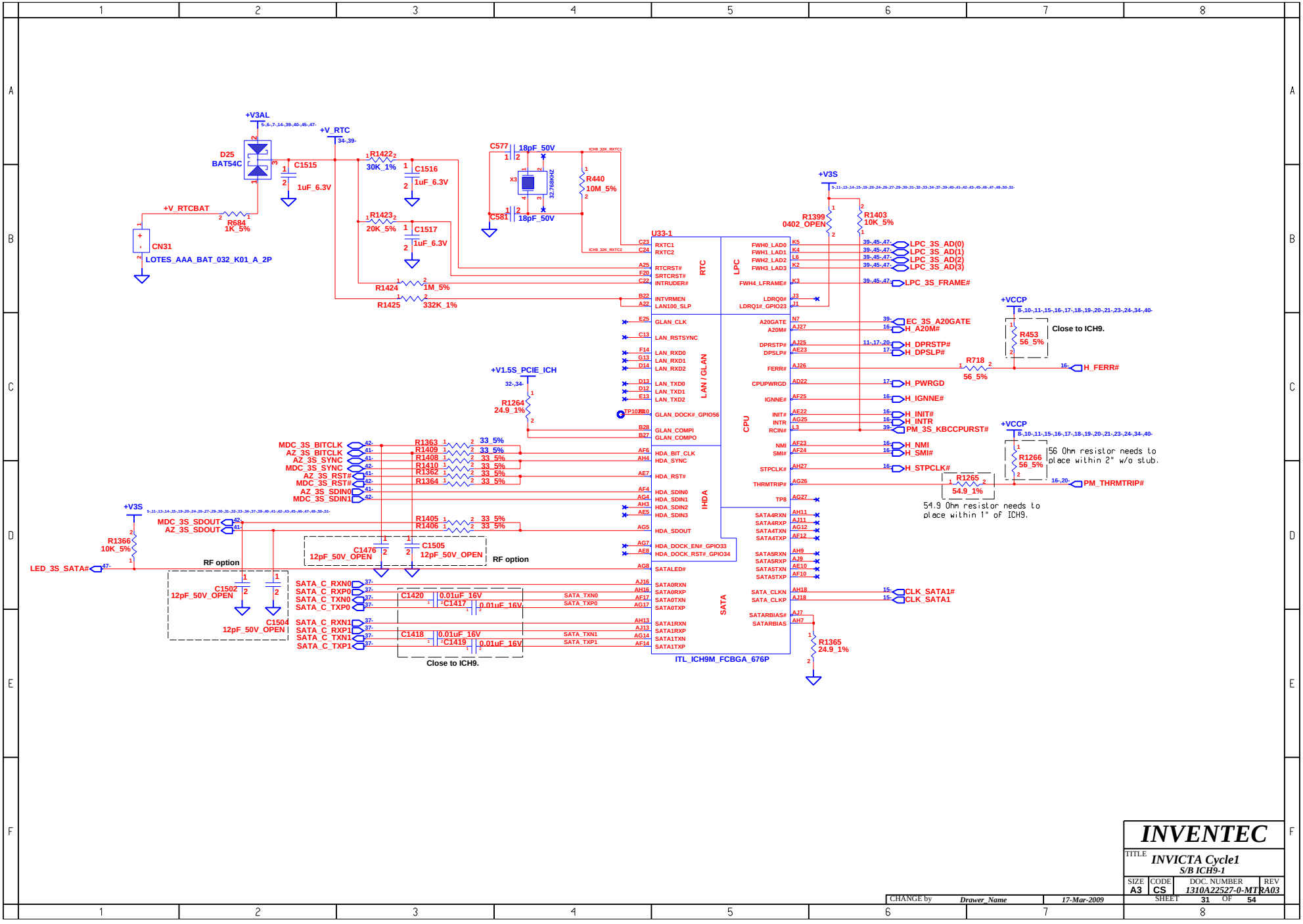

INVENTEC			
TITLE: INVICTA Cycle1 S/B ICH9-1			
SIZE: A3	CODE: CS	DOC. NUMBER: 1310A22527-0-MTRA03	REV: 03
CHANGE by: Drawer_Name	17-Mar-2009	SHEET 31 OF 54	

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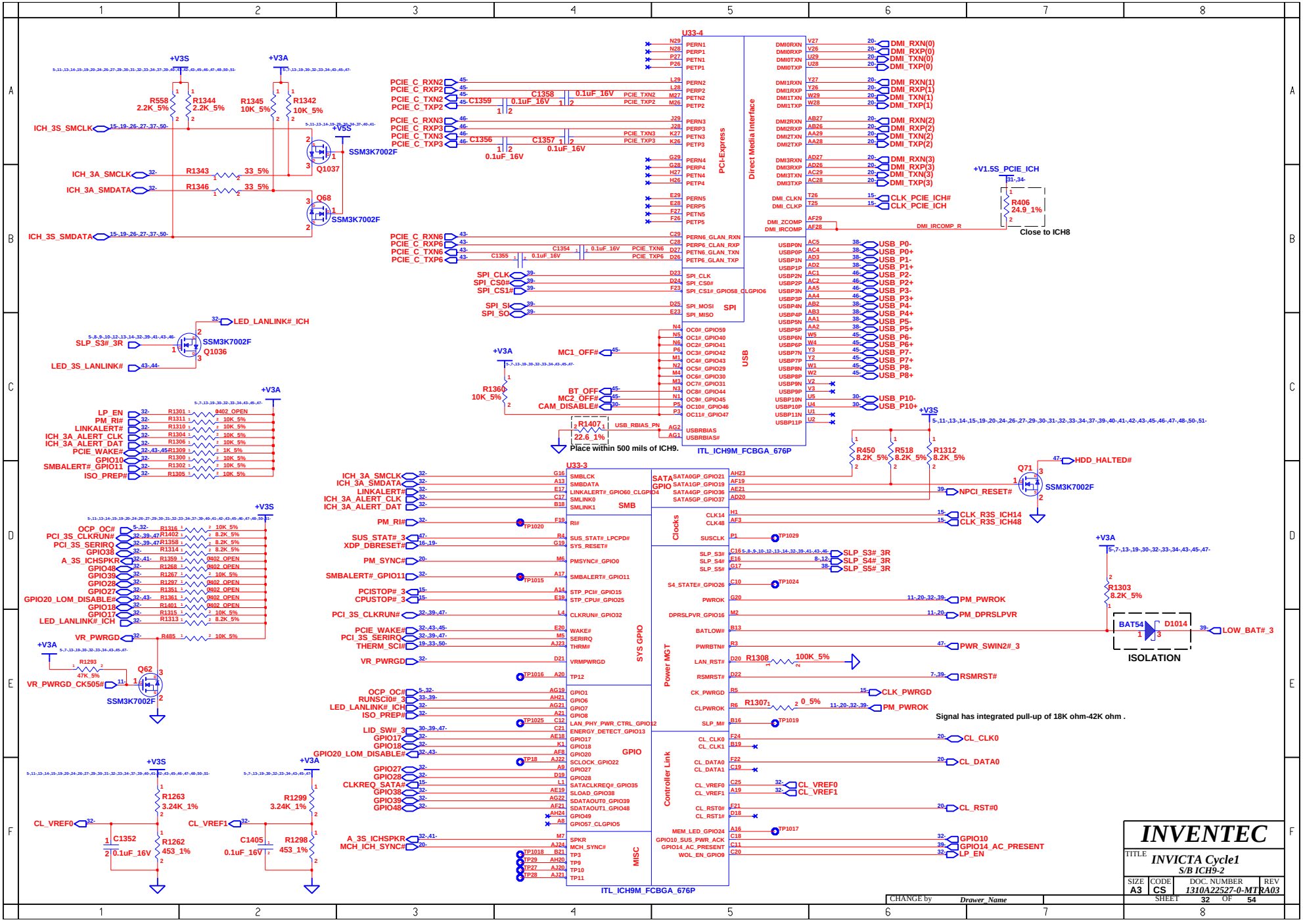

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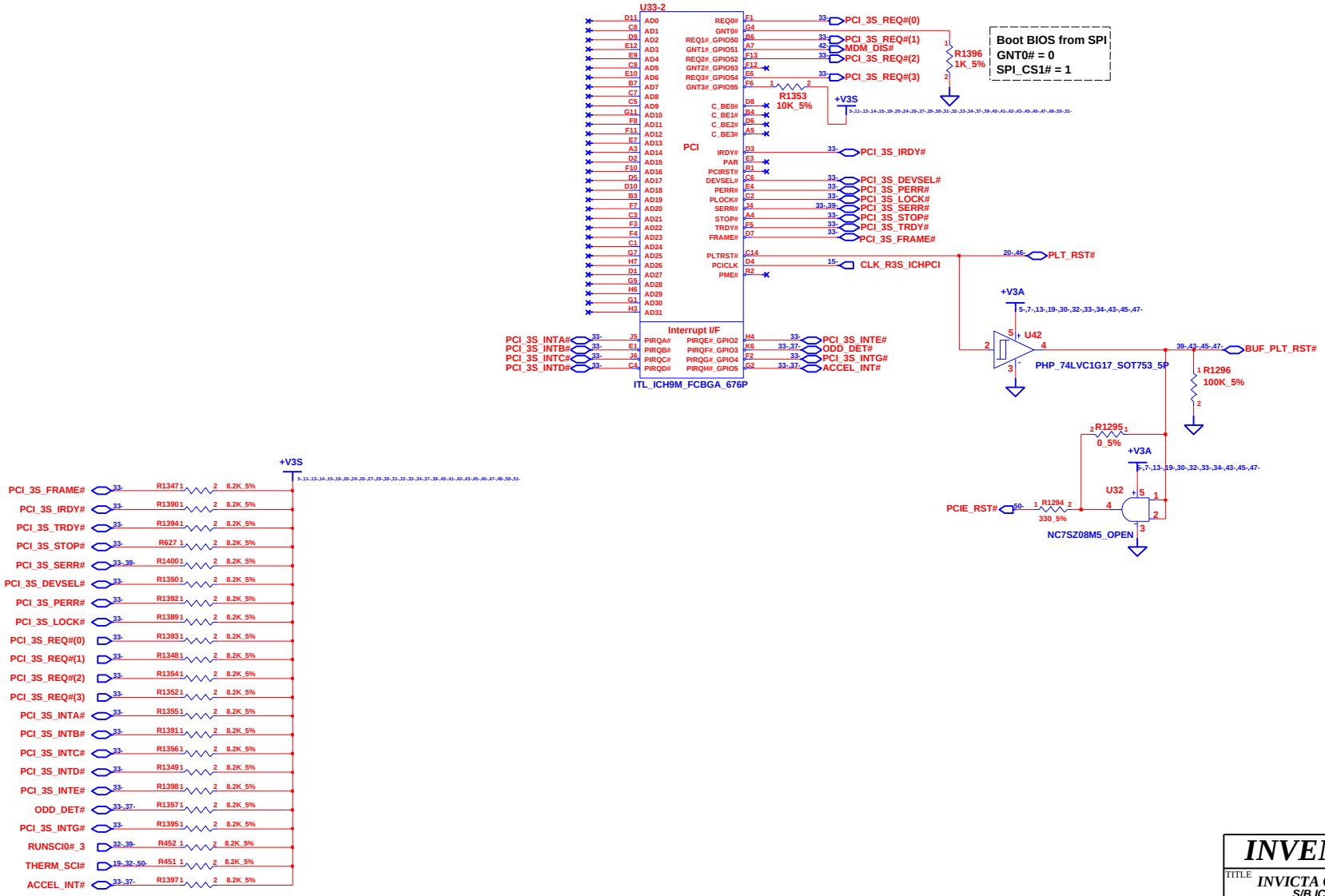

INVENTEC

TITLE *INVICTA Cycle1*
S/B ICH9-3

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22527-0-MTRA03	

SHEET 33 OF 54

CHANGE by *Drawer_Name* *17-Mar-2009*

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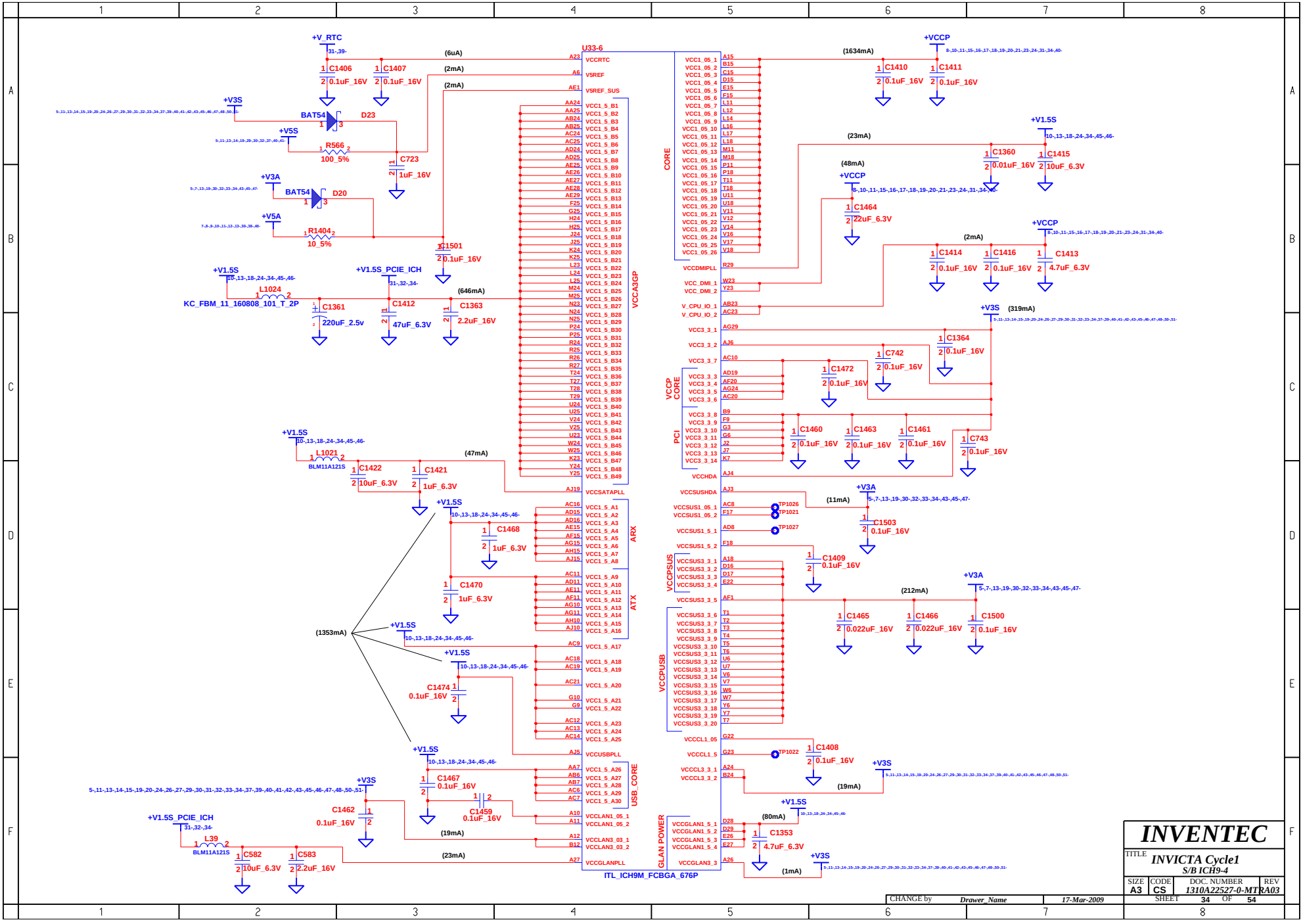
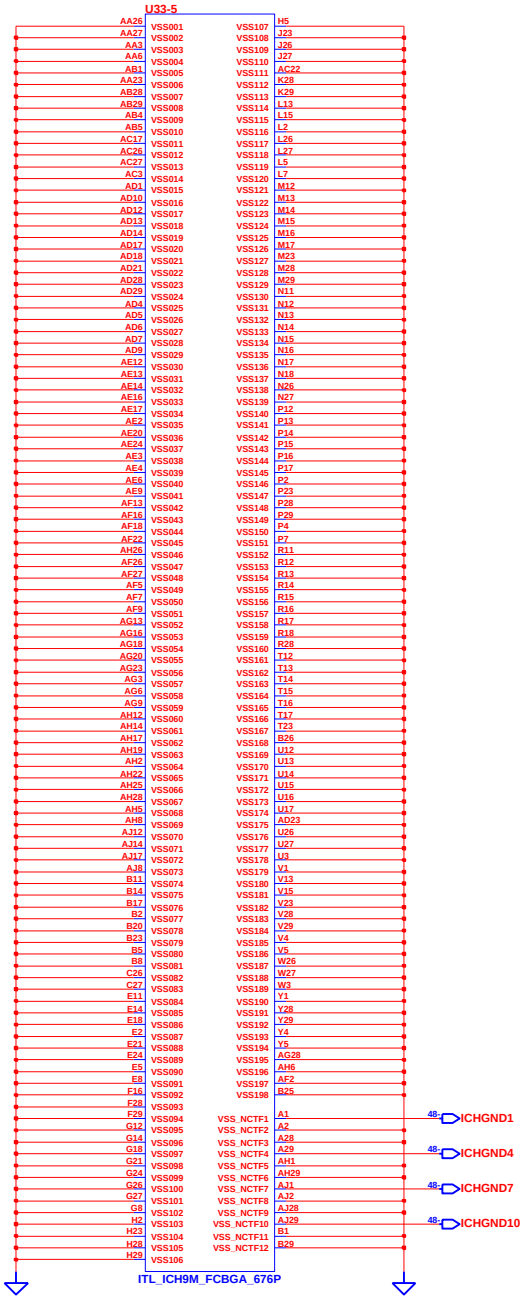


www.bufanxiu.com



CHANGE by	Drawer_Name	17-Mar-2009	

INVENTEC

TITLE: *INVICTA Cycle1*
S/B ICH9-5

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22527-0-MTRA03	

SHEET 35 OF 54

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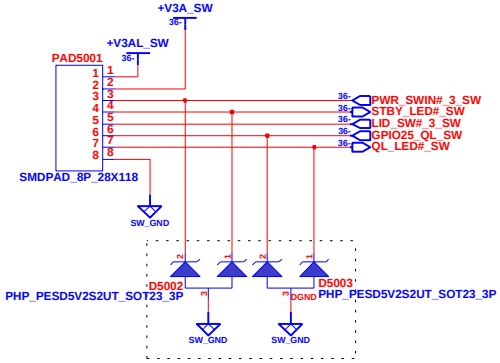
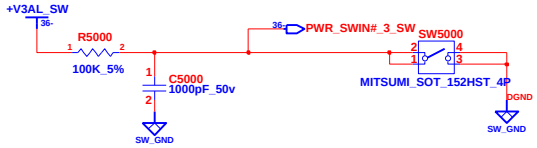
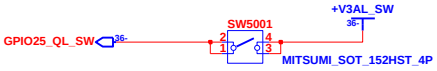
PWR SW B/B CONN



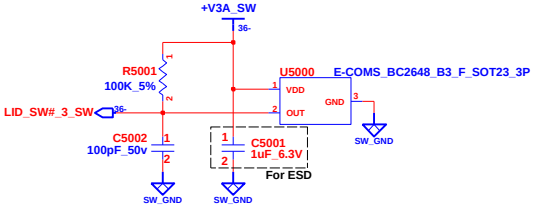
Power Button



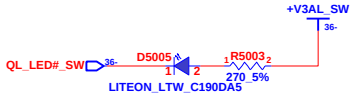
Quick Look Button



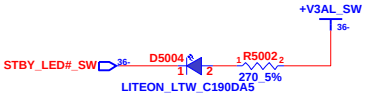
LID Switch



Quick Look LED



Power / Standby LED



Power & LID Switch Board

INVENTEC			
TITLE	INVICTA Cycle1 PWR, LID, APP SW/Bs		
SIZE A3	CODE CS	DOC. NUMBER 1310A22527-0-MTRA03	REV
CHANGE by Drawer_Name	17-Mar-2009	SHEET 36 OF 54	

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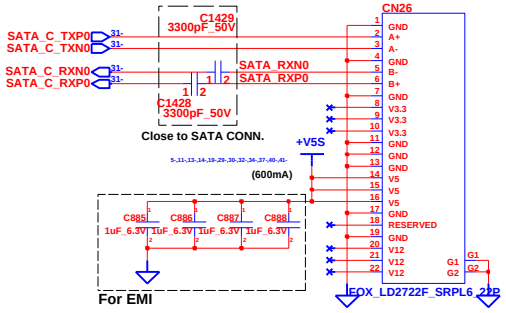
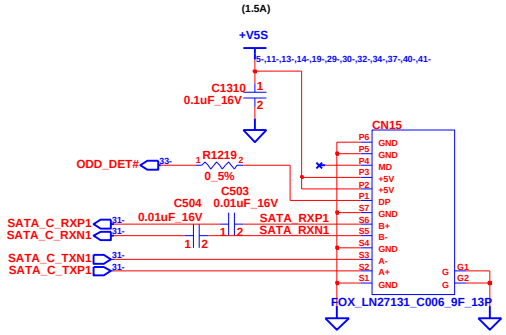
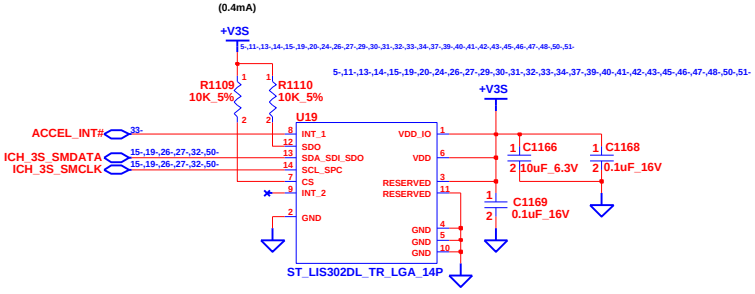


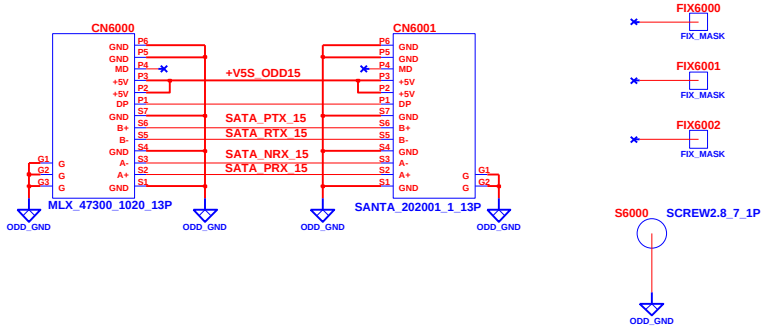
SATA HDD



SATA ODD



Accelerometer



15" ODD Extend Board

CHANGE by	Drawer_Name	17-Mar-2009	

INVENTEC

TITLE: *INVICTA Cycle1*

HDD & ODD CONN & Accelerometer & 15"ODD EXT/B

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22527-0-MTRA03	

SHEET 37 OF 54

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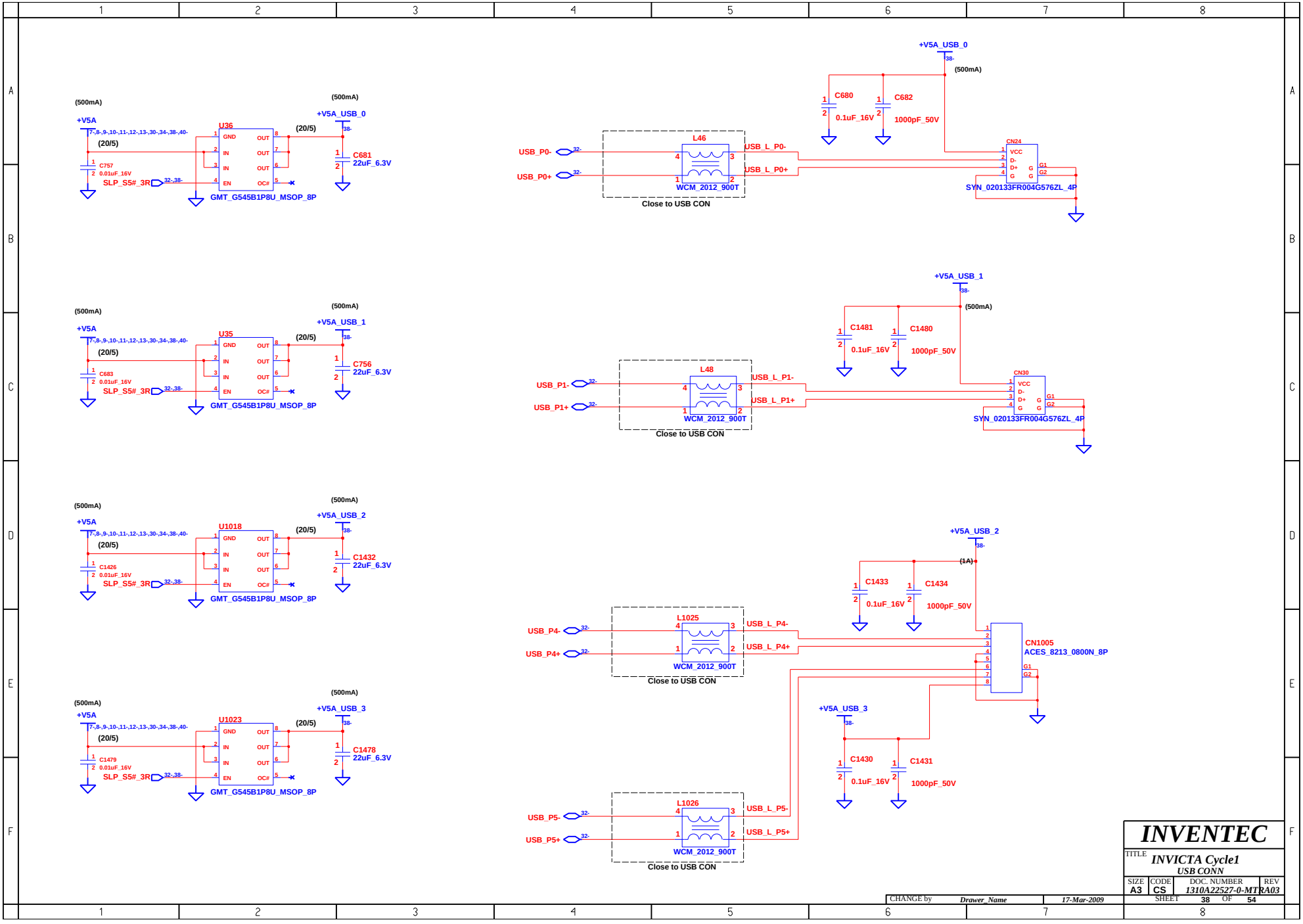
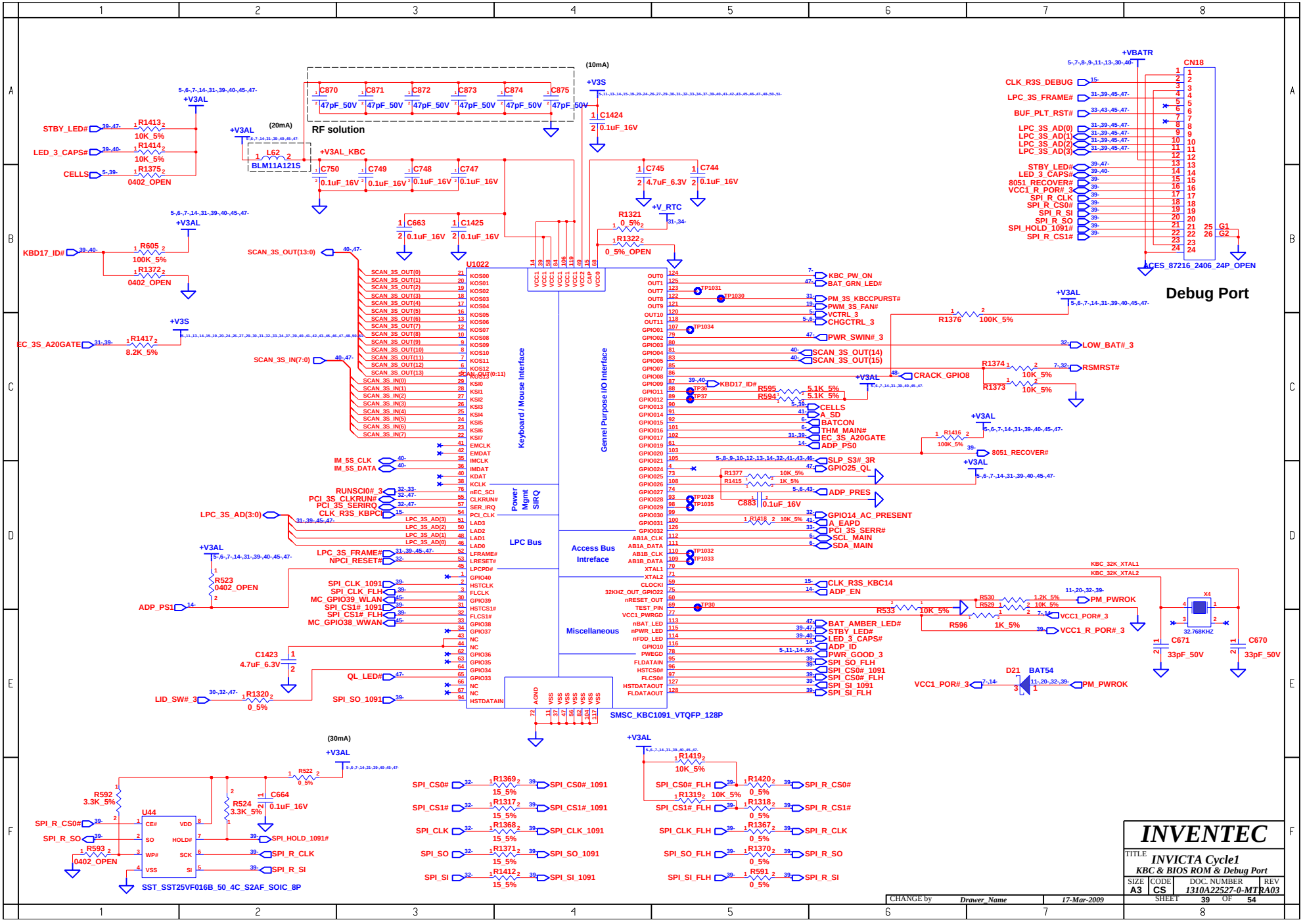
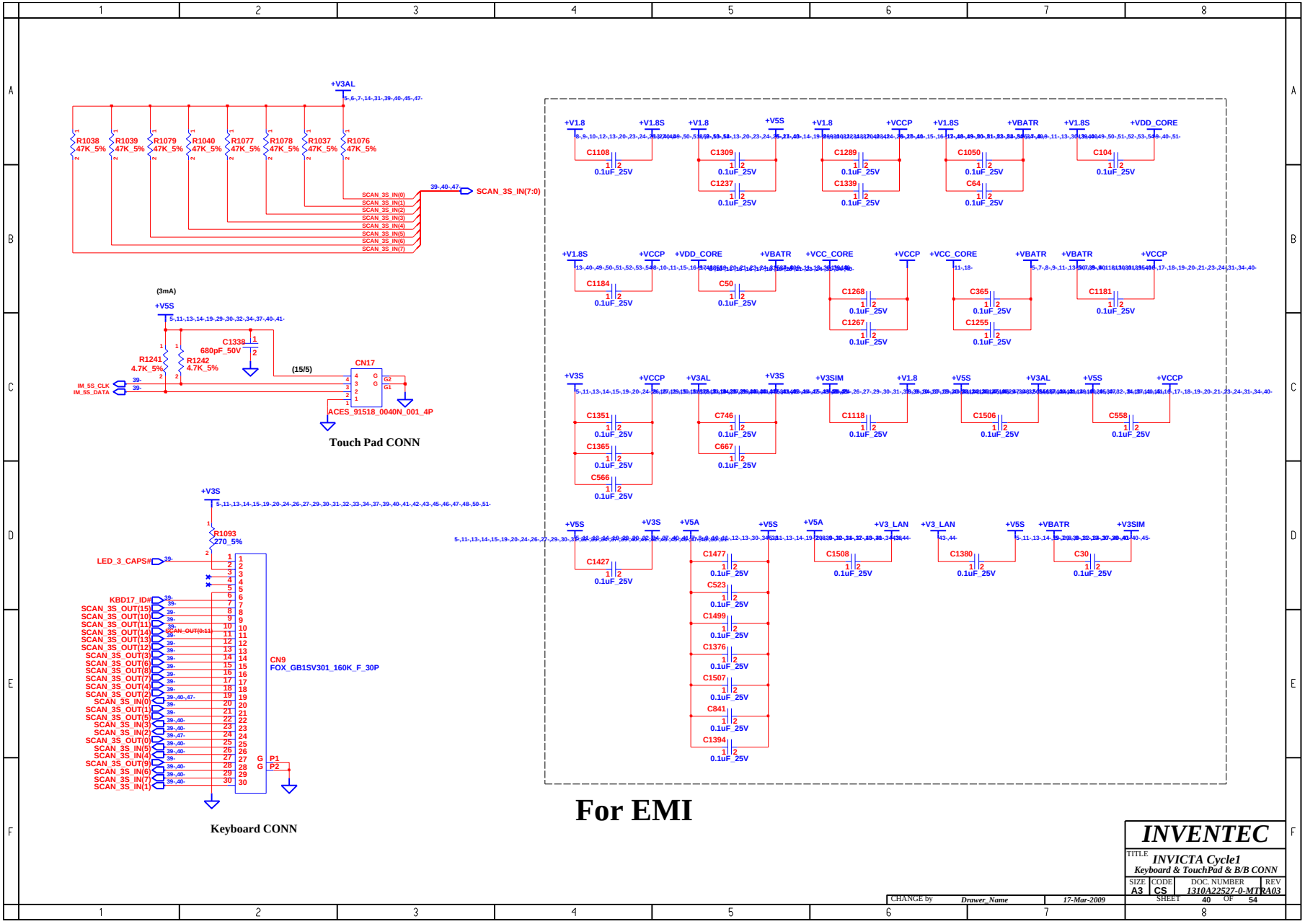


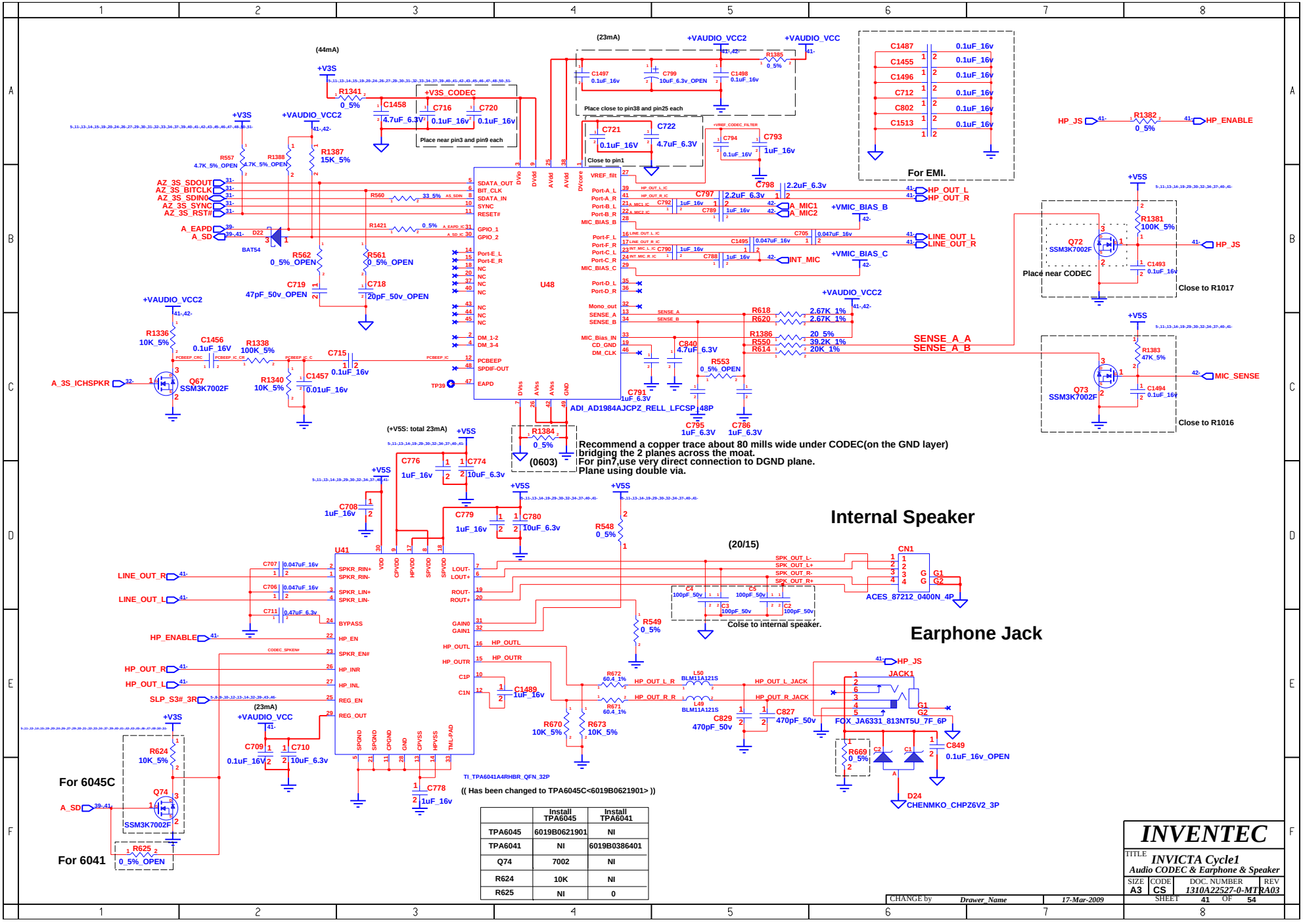
www.bufanxiu.com



www.bufanxiu.com



www.bufanxiu.com



	Install TPA6045	Install TPA6041
TPA6045	6019B0621901	NI
TPA6041	NI	6019B0386401
Q74	7002	NI
R624	10K	NI
R625	NI	0

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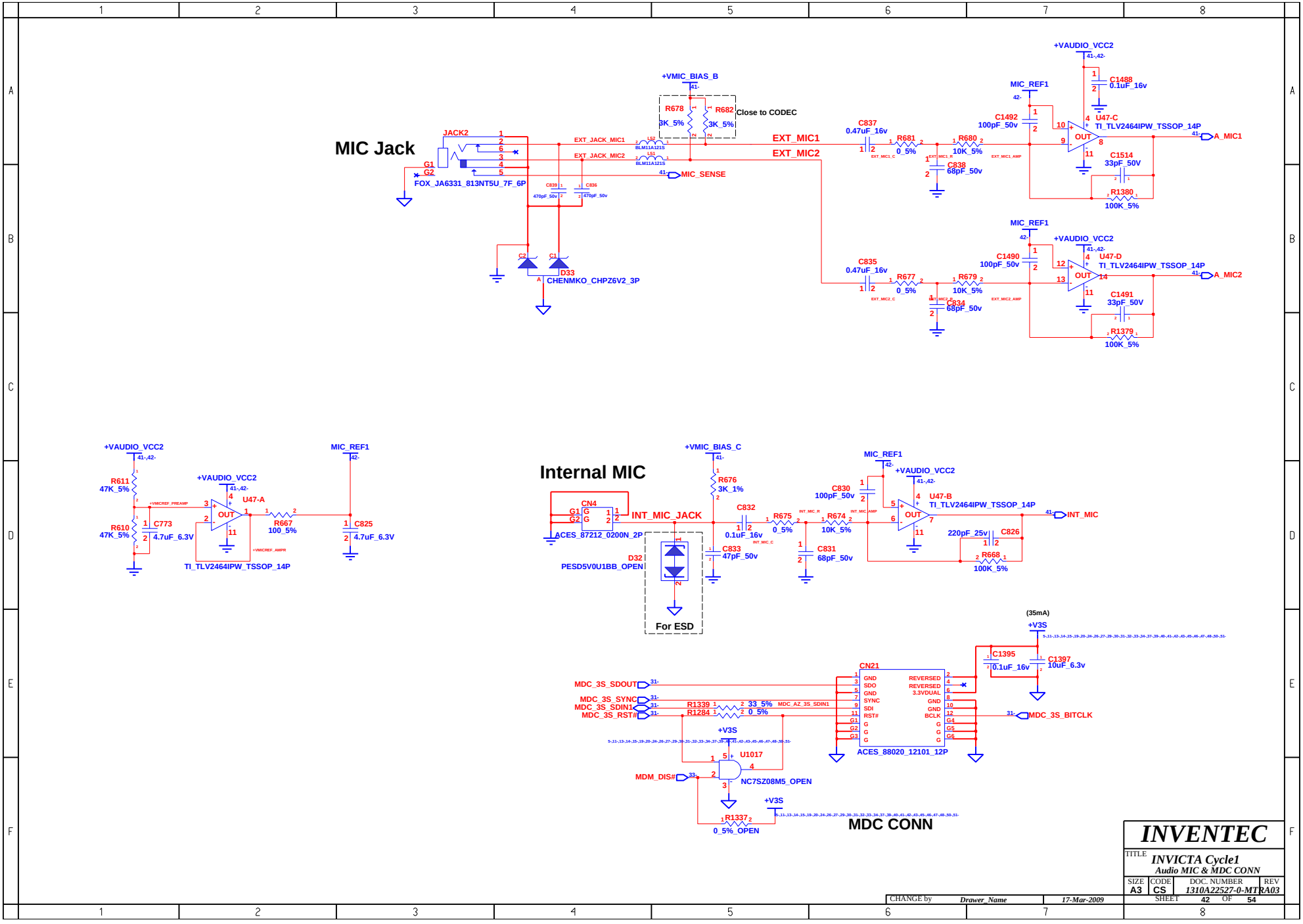
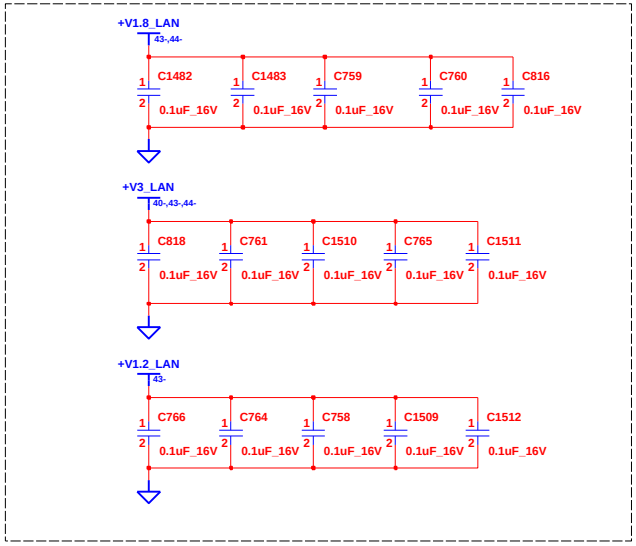
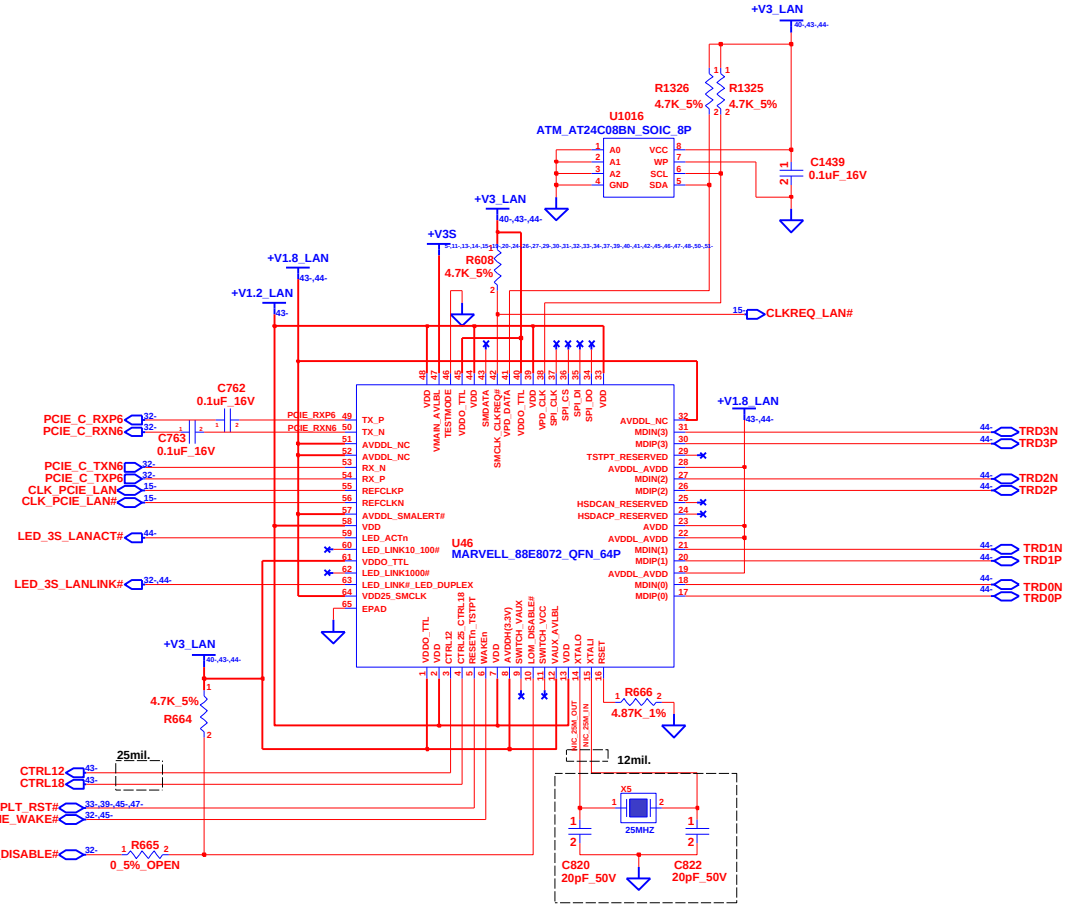
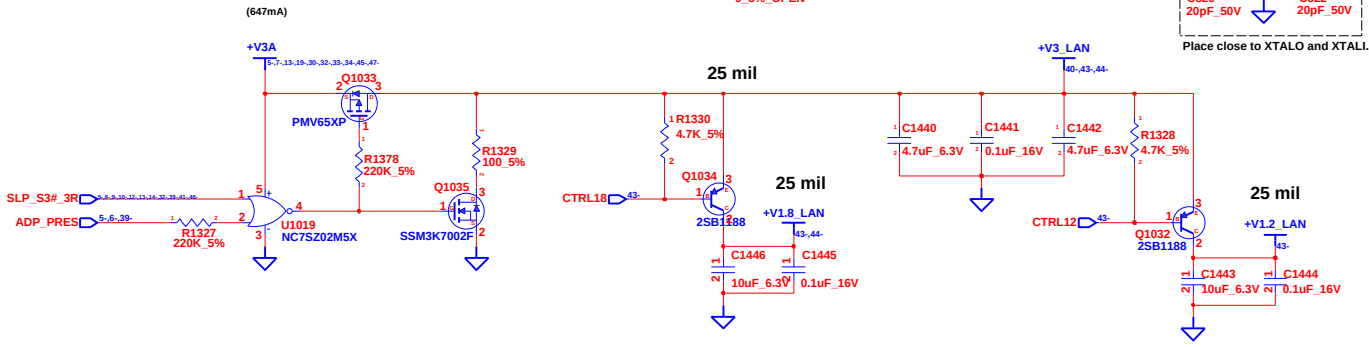


www.bufanxiu.com



Place bypass cap as close as possible with every power pin.





INVENTEC			
TITLE: INVICTA Cycle1 — Giga LAN Controller			
SIZE A3	CODE CS	DOC. NUMBER 1310A22527-0-MTRA03	REV
CHANGE by Drawer_Name	17-Mar-2009	SHEET 43 OF 54	

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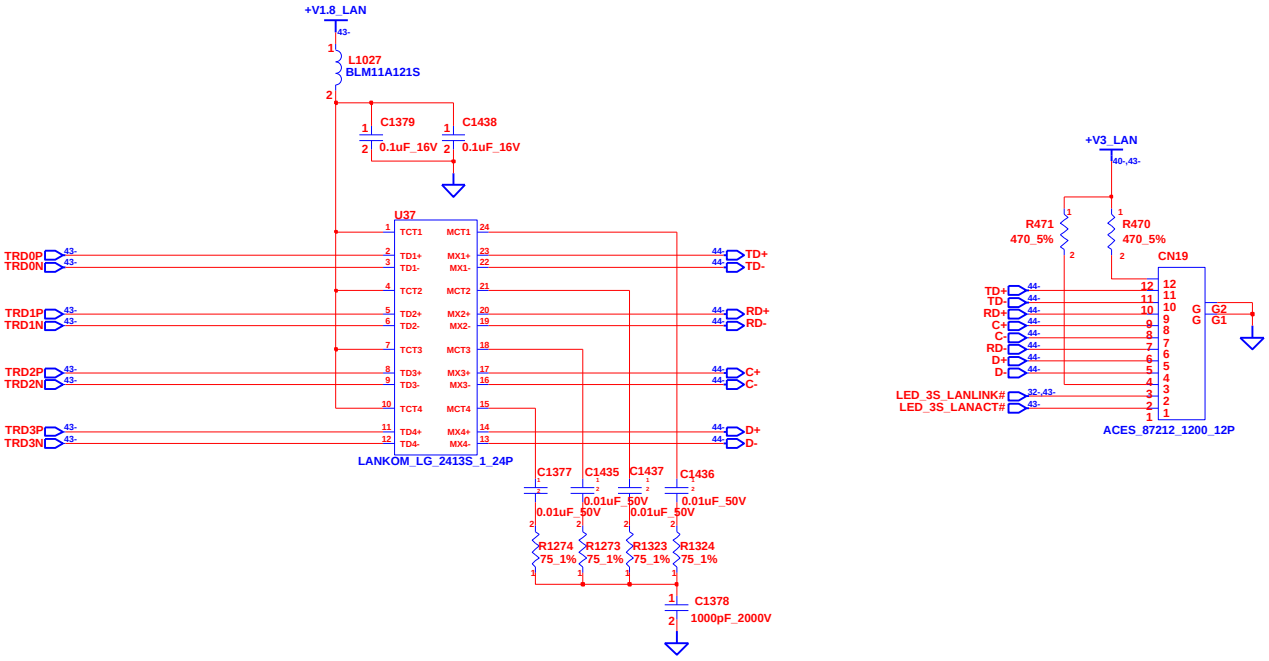

INVENTEC

TITLE
INVICTA Cycle1
Magnetic & RJ45 CONN

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22527-0-MTRA03	

SHEET 44 OF 54

CHANGE by Drawer_Name 17-Mar-2009

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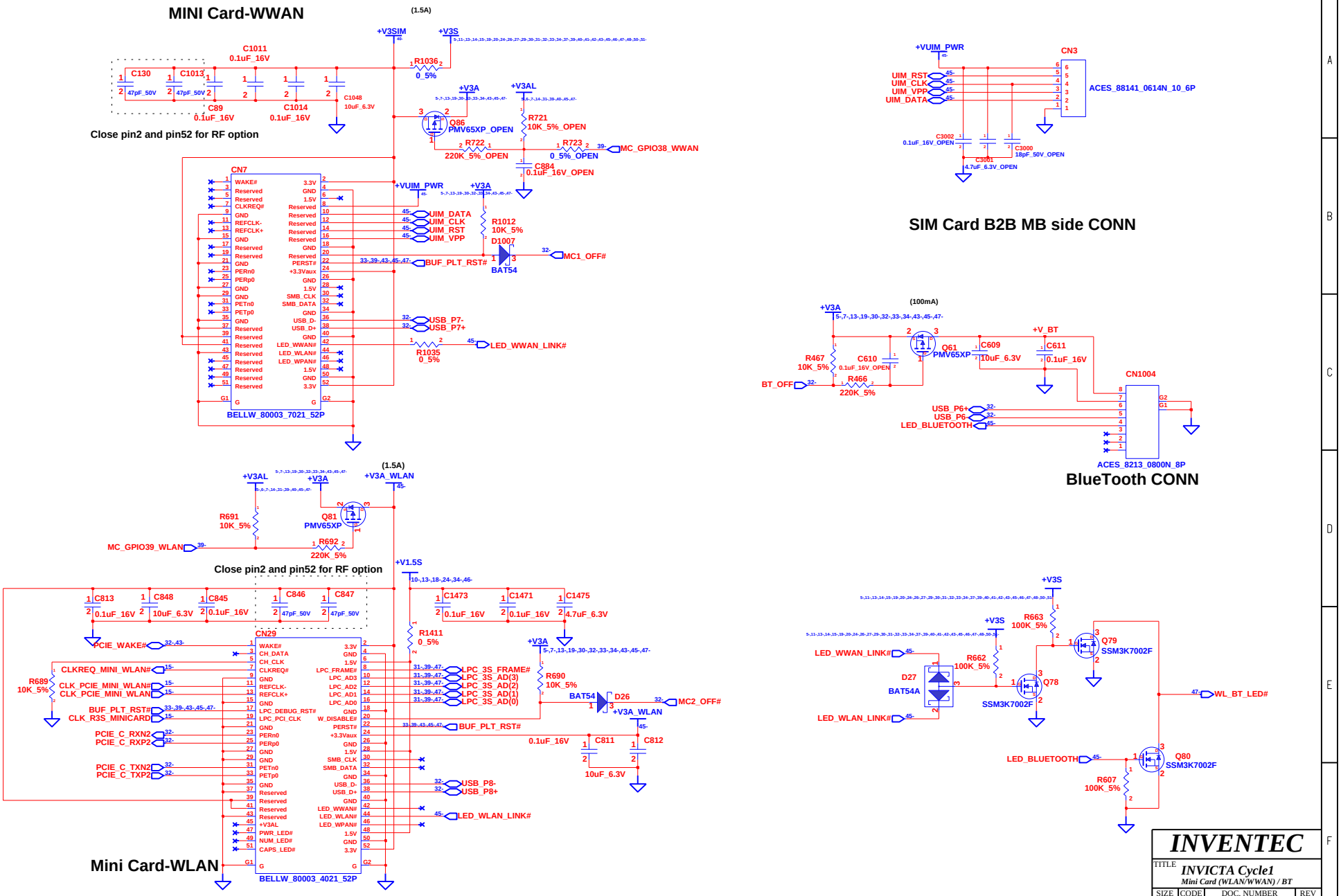
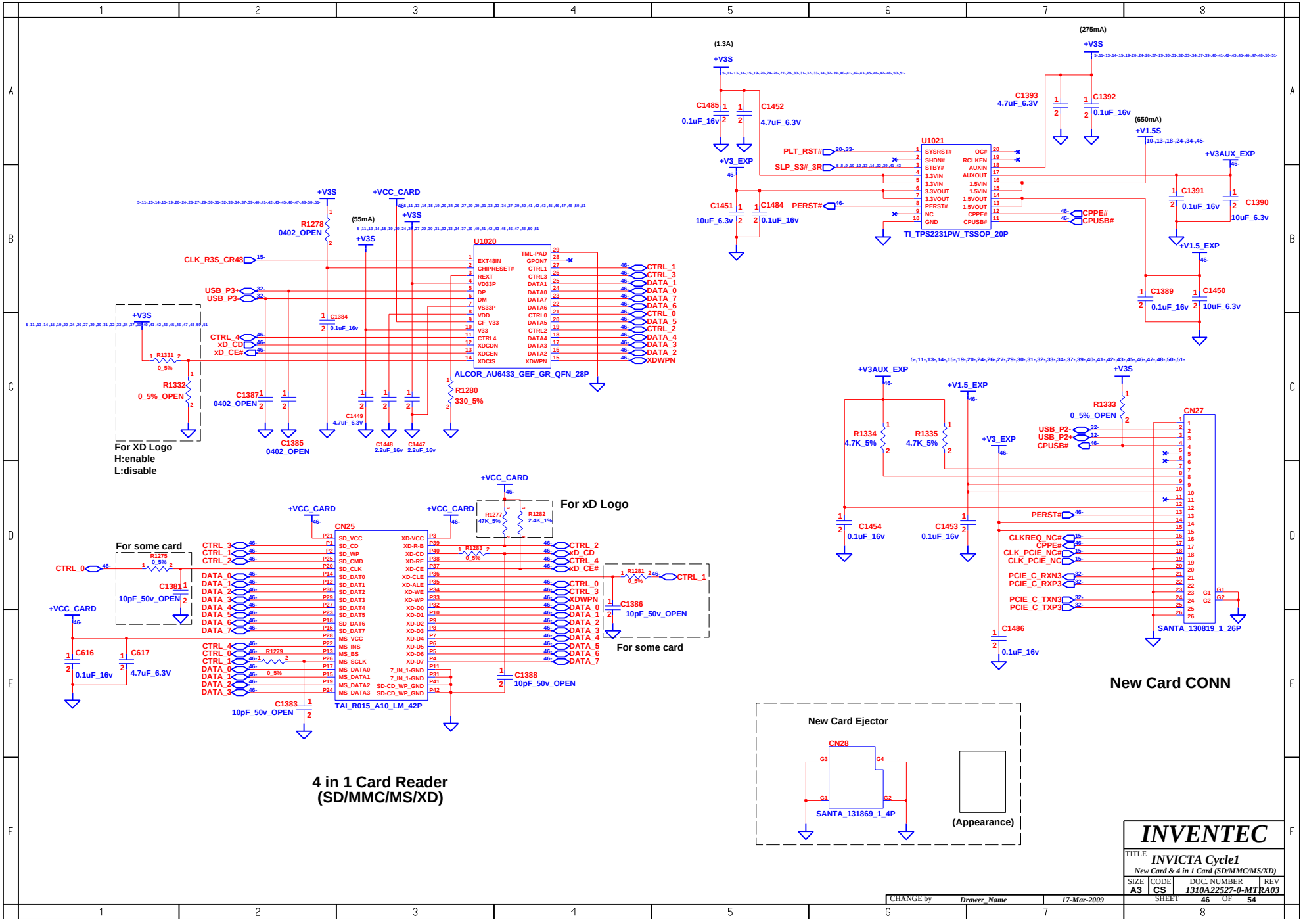


www.bufanxiu.com



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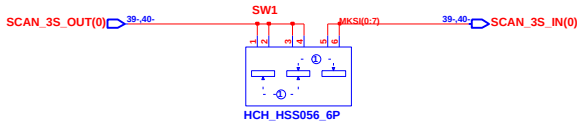
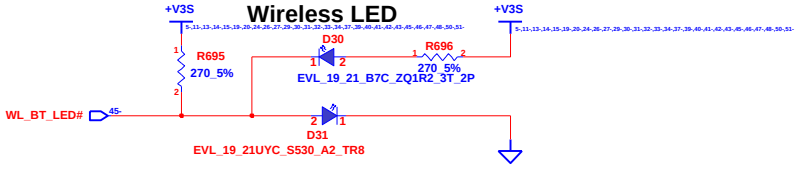
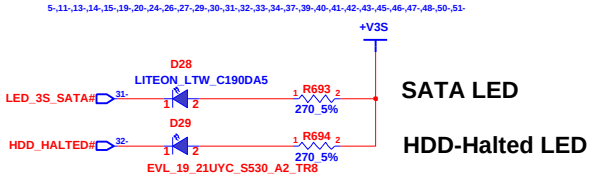
Wireless Button



Wireless LED

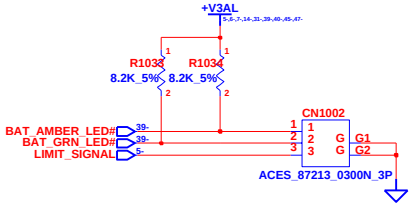


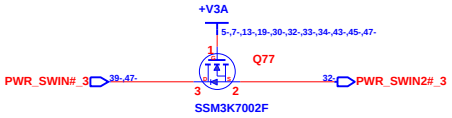


SATA LED

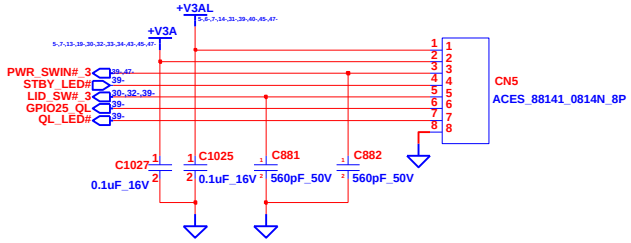
HDD-Halted LED

Battery Charge LED CONN

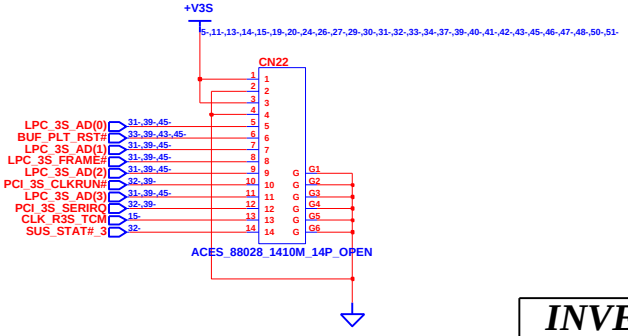




LED & SW B/B CONN



TCM CONN



CHANGE by	Drawer_Name	17-Mar-2009	

INVENTEC

TITLE: *INVICTA Cycle1*
LEDs & TCM CONN

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22527-0-MTRA03	

SHEET 47 OF 54

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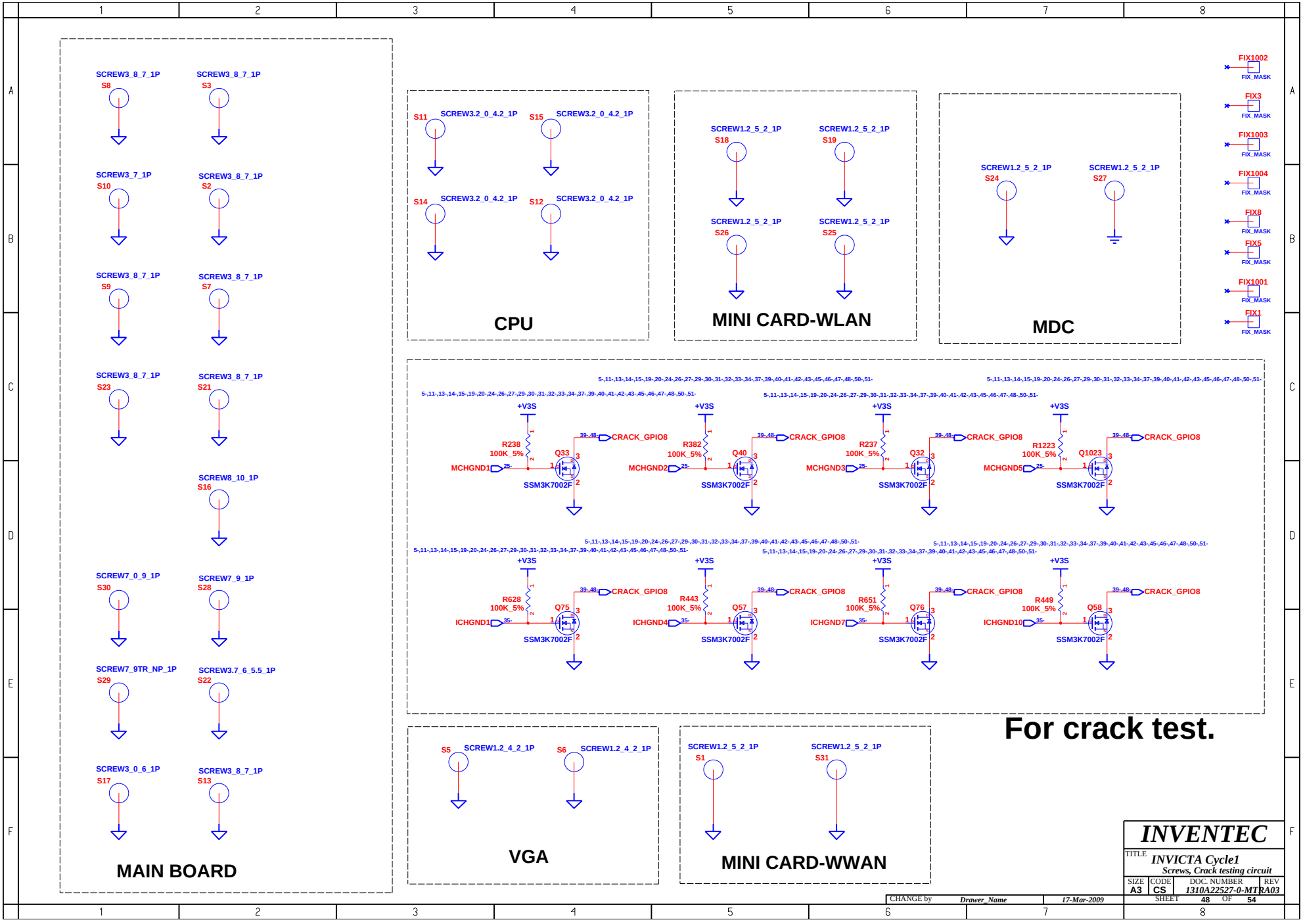

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STRAPS	PIN	Description of default settings	
TX_PWRS_ENB	GPIO0	PCIE full TX output swing.	1
TX_DEEMPH_EN	GPIO1	PCIE transmitter de-emphasis enabled.	1
BIF_DEBUG_ACCESS	GPIO4	Debug signals muxed out.	0
ROMIDCFG(0:3)	GPIO[11:13,9]	Memory aperture type	X X X X

X = DESIGN DEPENDANT

0 = DO NOT INSTALL RESISTOR

1 = INSTALL 10K RESISTOR

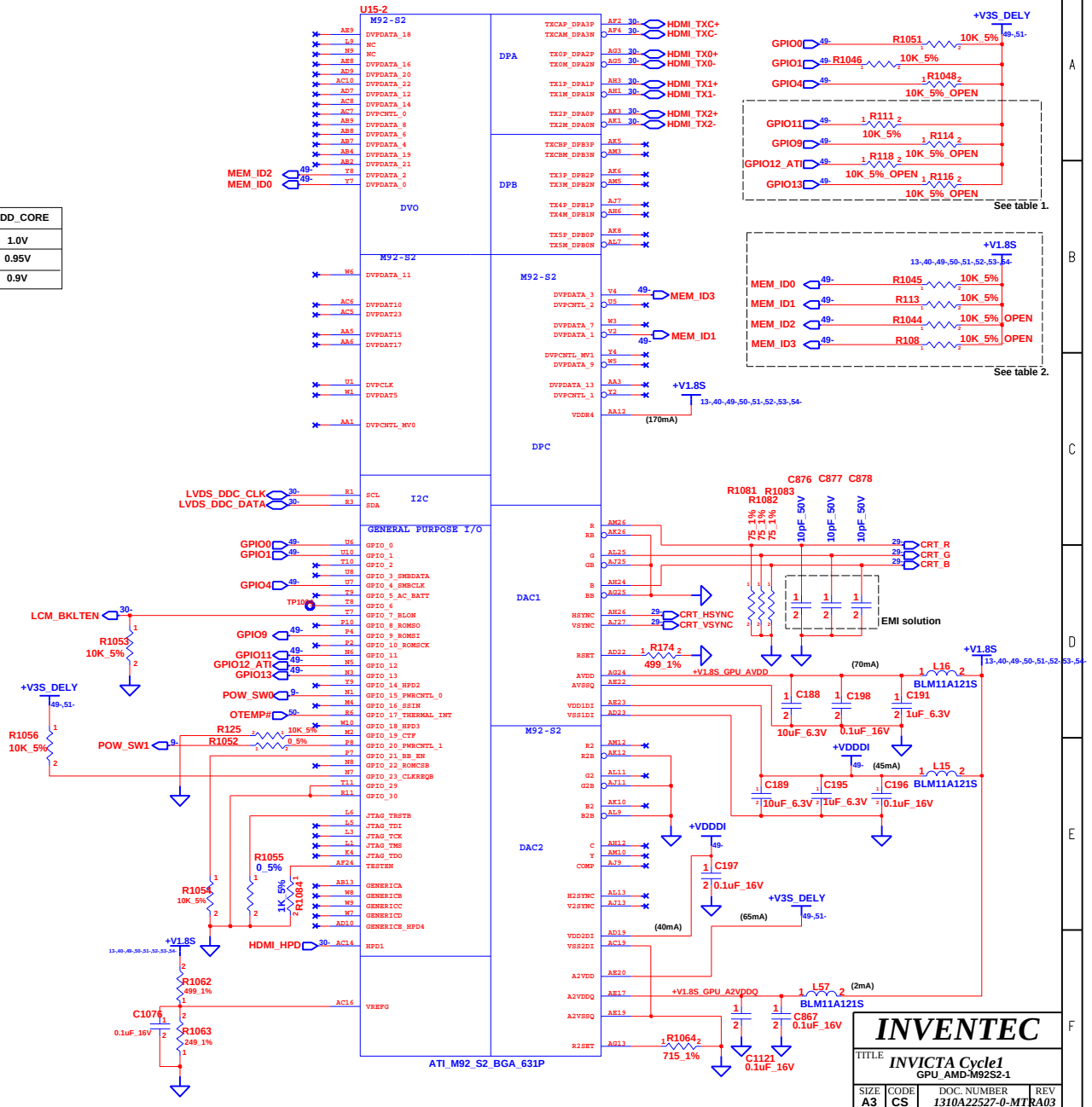
Table 1

GPIO_13	GPIO_12	GPIO_11	For DIS-GDDR2	
0	0	1	512MB/256MB memory aperture	(Default)
1	1	0	reserved	

POW_SW1	POW_SW0	+VDD_CORE
0	0	1.0V
0	1	0.95V
1	0	0.9V

Table 2

For DIS-VRAM DDR2					
MEM_ID3	MEM_ID2	MEM_ID1	MEM_ID0	vendor	
0	0	0	1	Samsung (512MB)	
0	0	1	0	Qimonda (512MB)	
0	0	1	1	Hynix (512MB)	(Default)



INVENTEC

TITLE INVICTA Cycle1
GPU_AMD-M92S2-1

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22527-0-MTRA03	

SHEET 49 OF 54

CHANGE by Drawer_Name 17-Mar-2009

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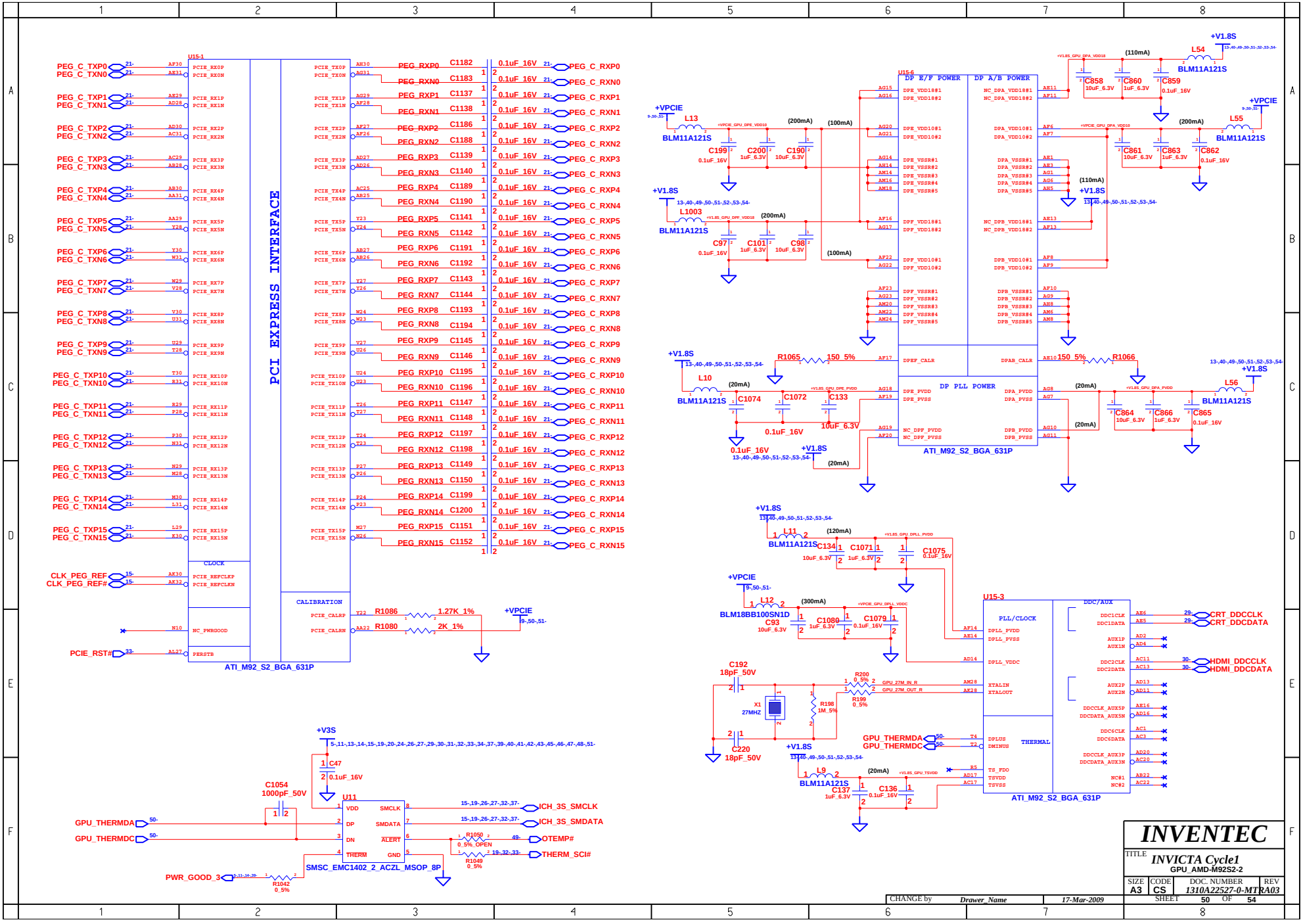
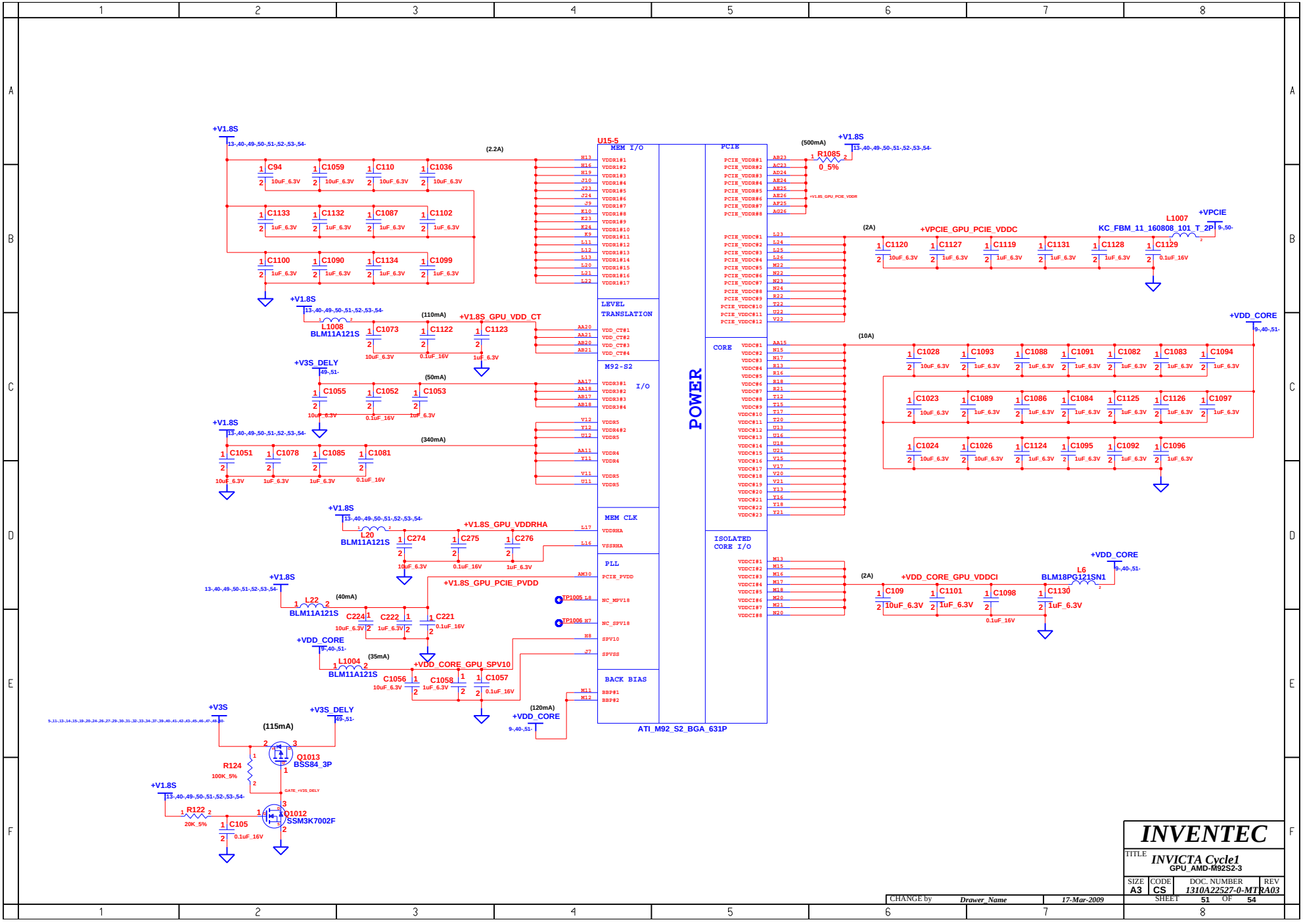
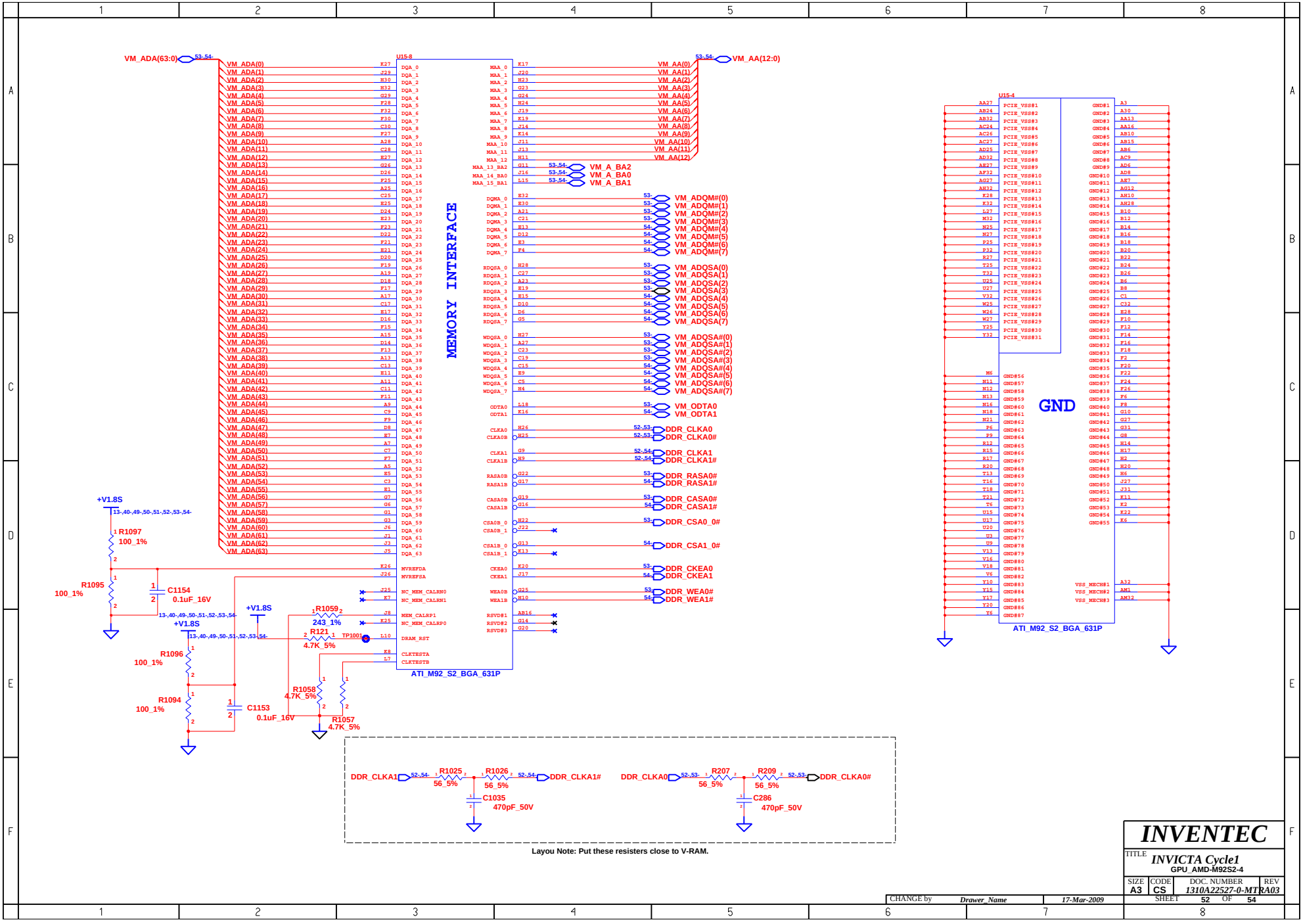


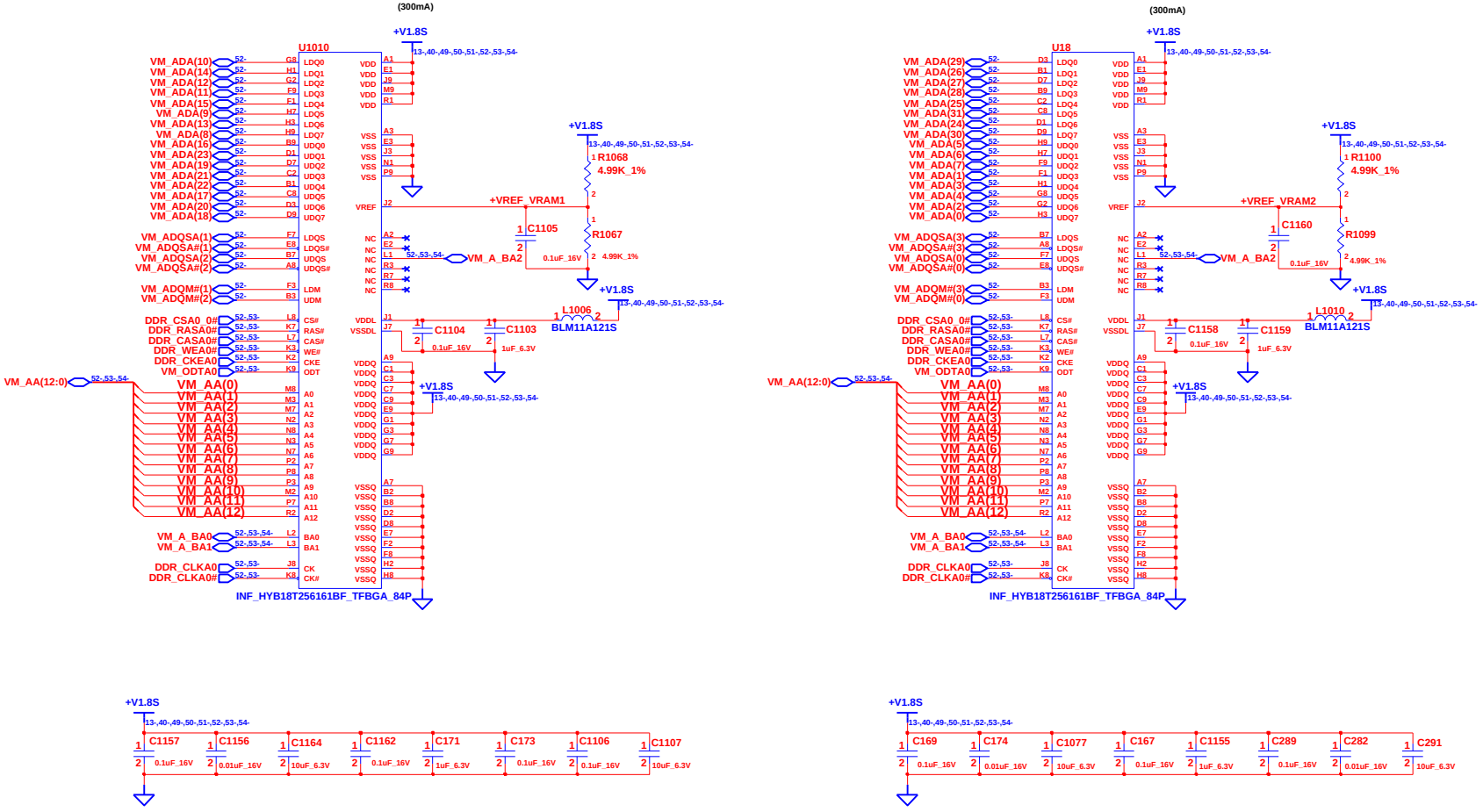
www.bufanxiu.com



www.bufanxiu.com



www.bufanxiu.com



INVENTEC

TITLE
INVICTA Cycle1
Video RAM (DDR2) -1

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22527-0-MTRA03	

SHEET 53 OF 54

CHANGE by	Drawer_Name	17-Mar-2009

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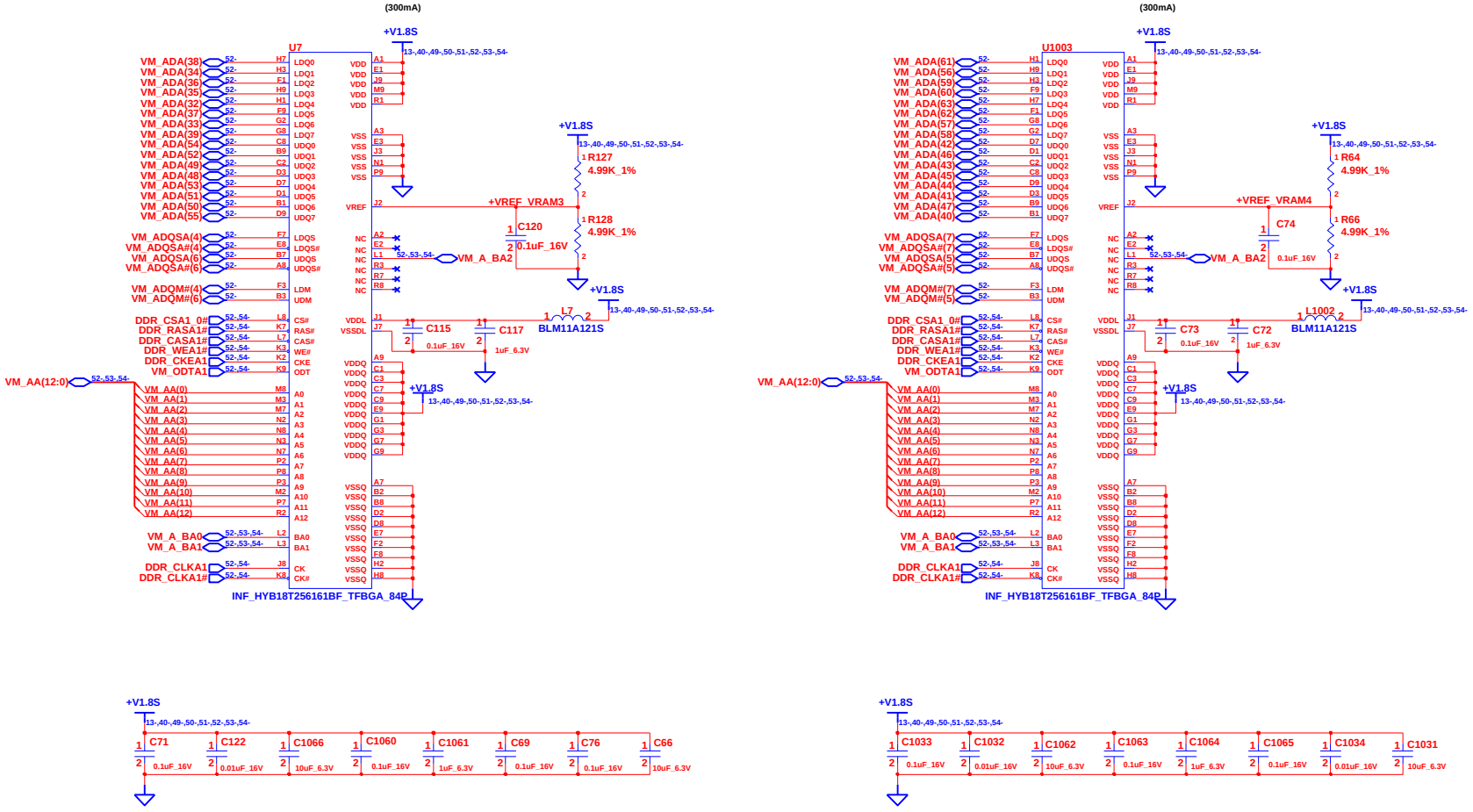

CHANGE by	Drawer_Name	17-Mar-2009	

INVENTEC

TITLE *INVICTA Cycle1*
Video RAM (DDR2) -2

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22527-0-MTRA03	

SHEET 54 OF 54