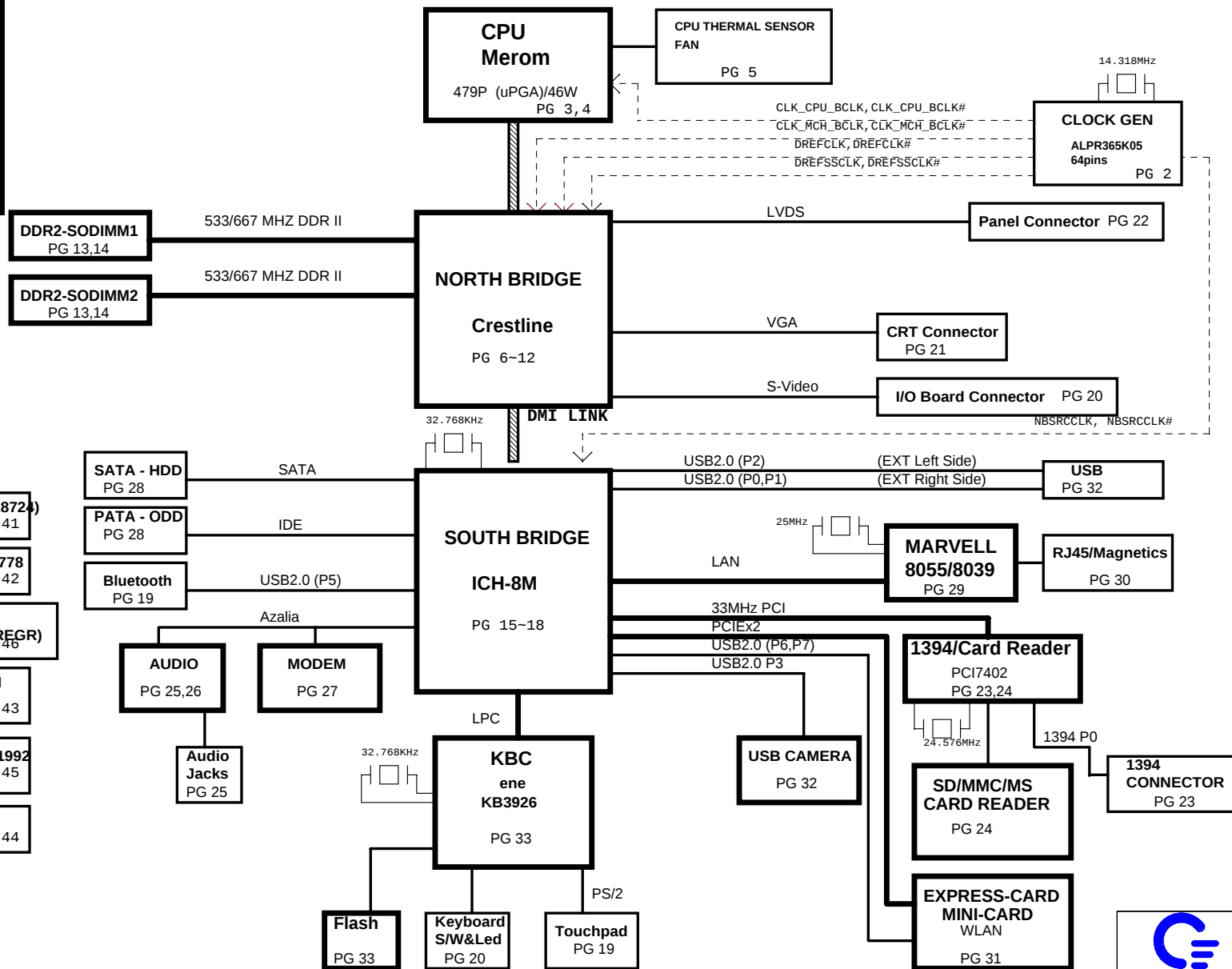


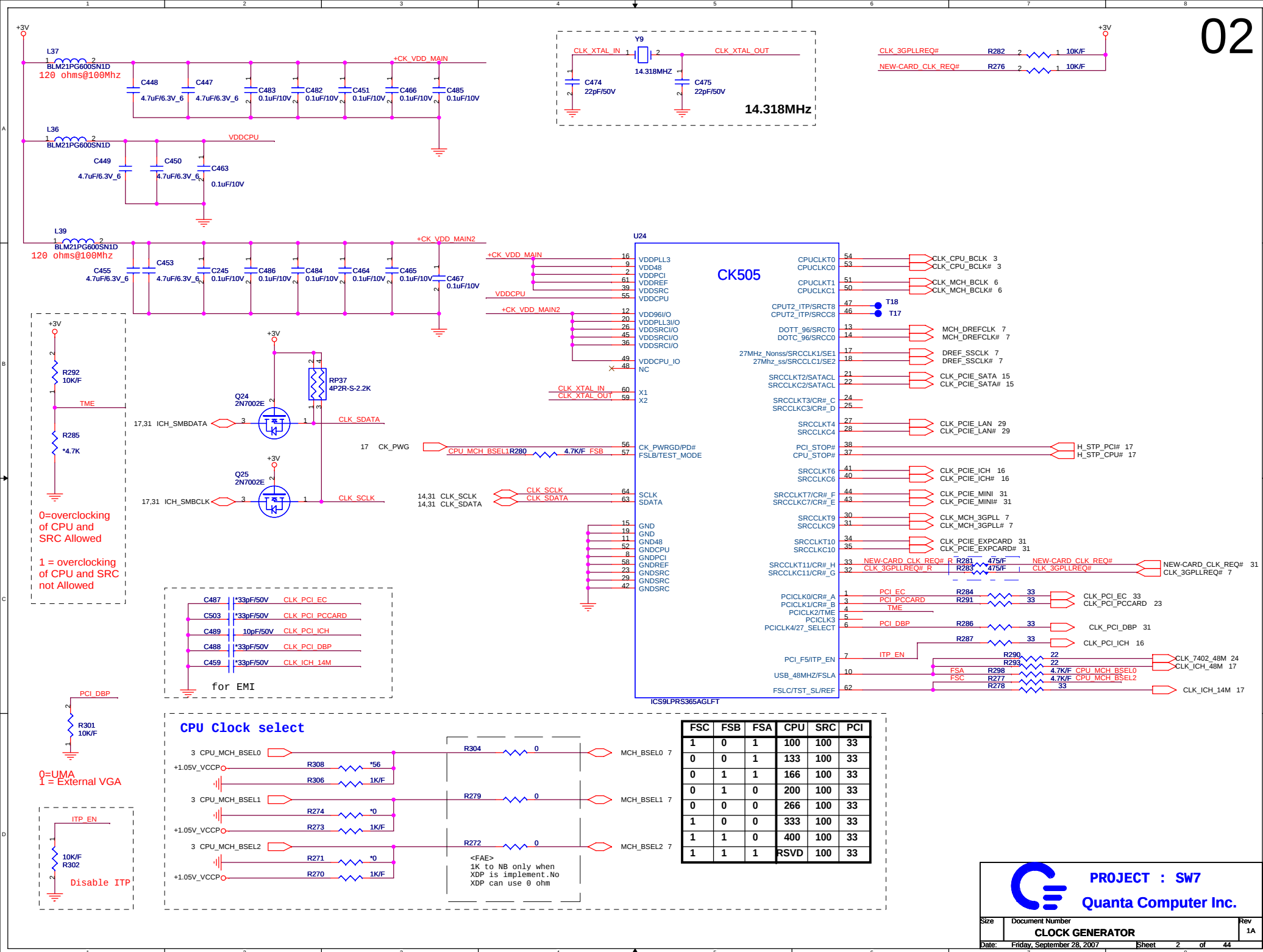
SW7 BLOCK DIAGRAM

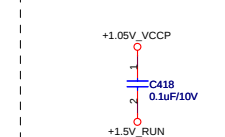
01

PCB STACK UP

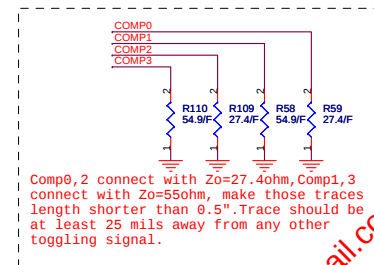
LAYER 1 : TOP
LAYER 2 : SGND1
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : IN3
LAYER 7 : SGND2
LAYER 8 : BOT







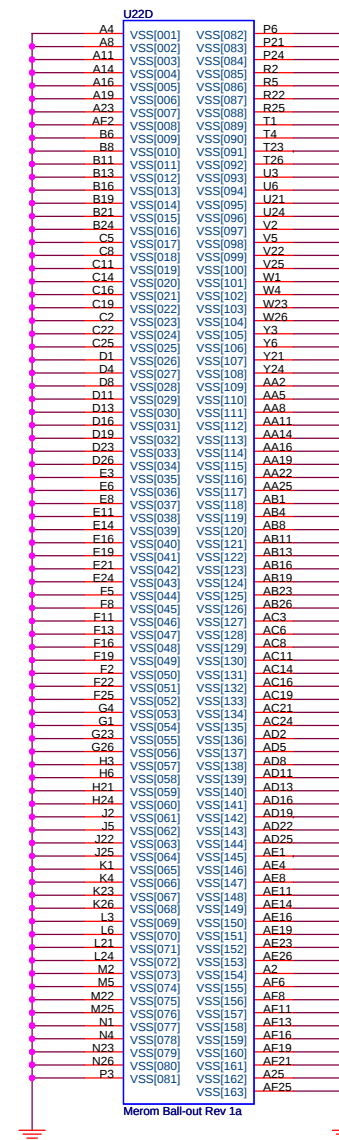
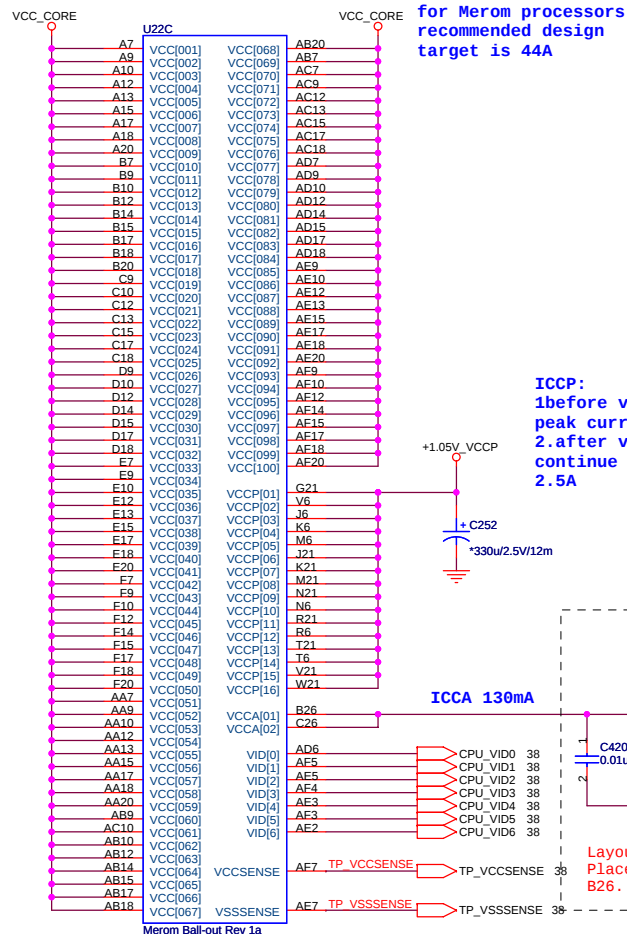
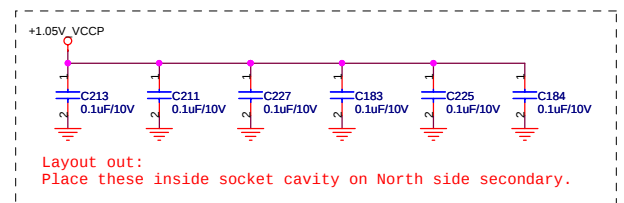
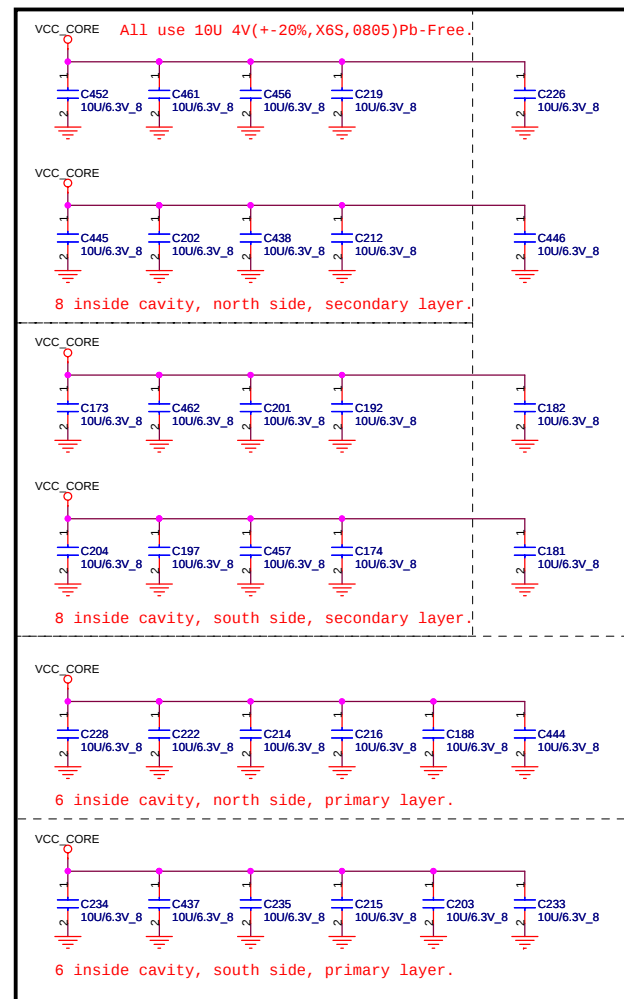
For the purpose of testability, route these signals through a ground referenced Z0 = 55ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

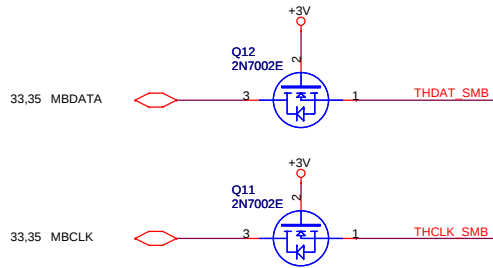
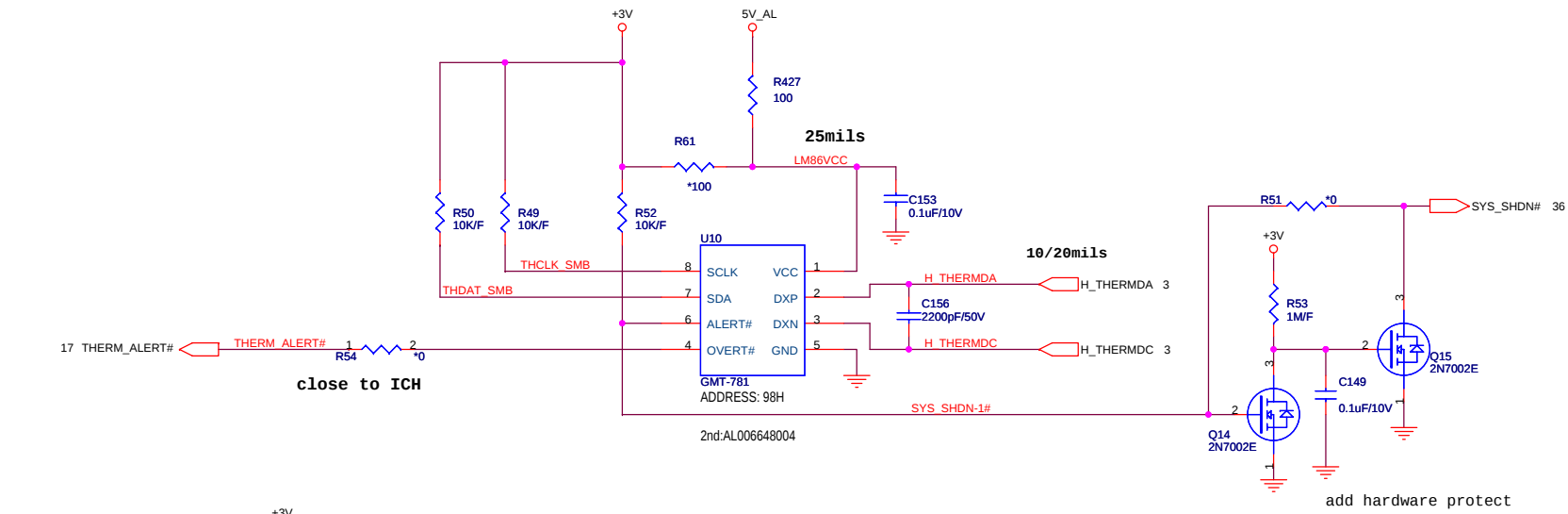


ITP disable guidelines			
Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 2.0" of the ITP
TMS	39 ohm +/- 1%	VTT	Within 2.0" of the ITP
TRST#	500-680ohm +/- 5%	GND	Within 2.0" of the ITP
TCK	27 ohm +/- 1%	GND	Within 2.0" of the ITP
TDO	150 ohm +/- 5%	VTT	Within 2.0" of the ITP

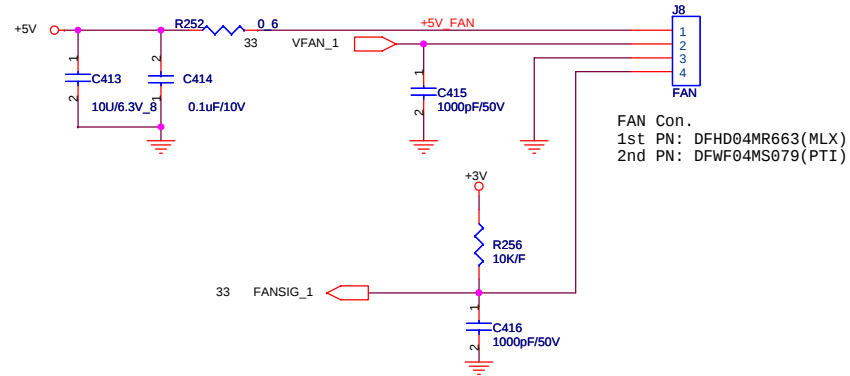
Note: Populate R5, R8, C372 & R430 when ITP connector is populated.

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0

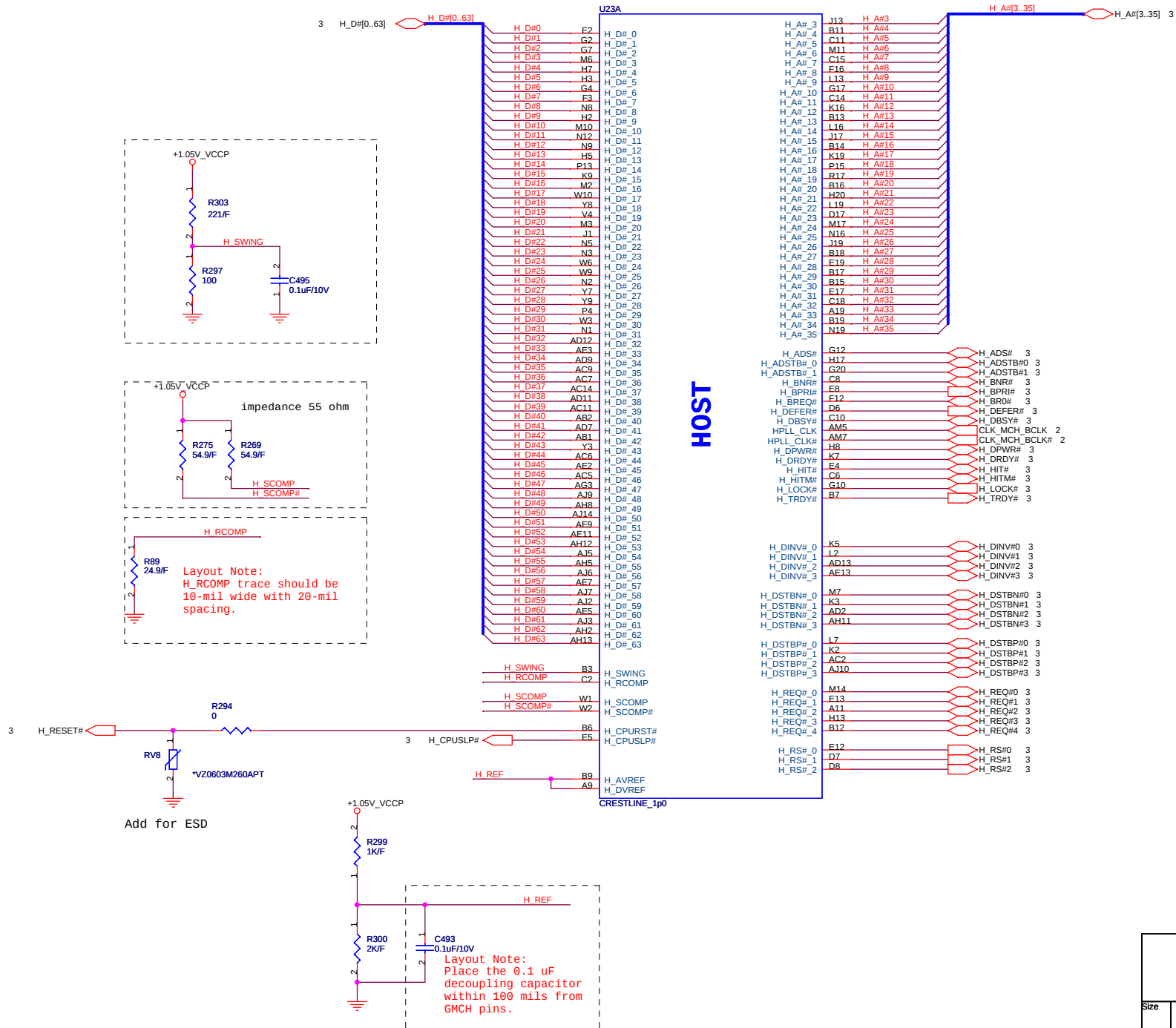




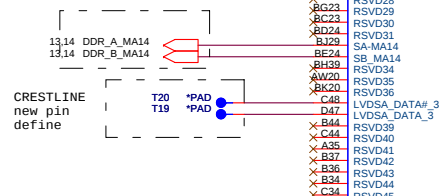
1st FAN OUT CONNECTOR



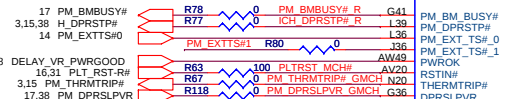
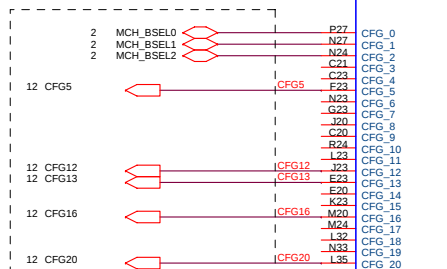
		PROJECT : SW7 Quanta Computer Inc.	
Size	Document Number		Rev
	THERMAL LM86 & FAN		1A
Date:	Friday, September 28, 2007	Sheet	5 of 44



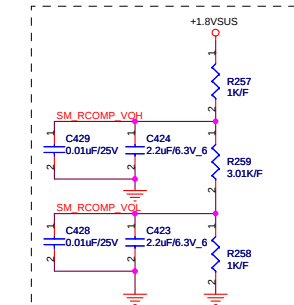
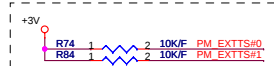
W22 update
--- MA14 needs
to be routed if
customers are
planning on
using 2Gb
technology and
width=8 (by 8)
DIMMs



Layout Note:
Location of all MCH_CFG strap
resistors needs to be close to
minimize stub.



GMCH pwrok is 3.3v
tolerant



DDR_MUXING

CLK

DMI

VID

ME

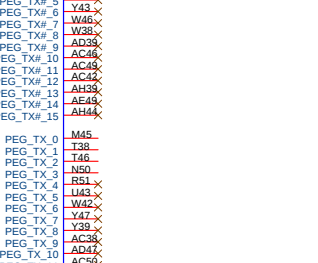
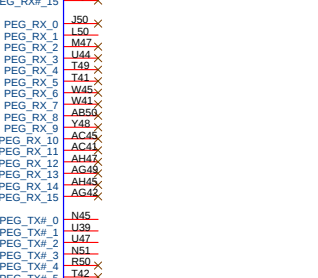
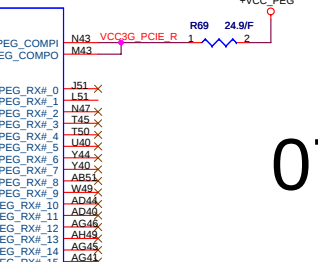
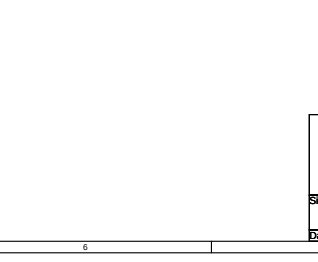
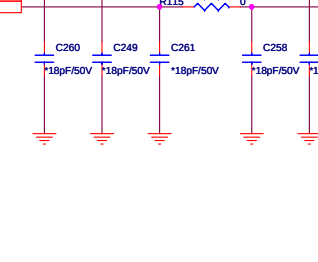
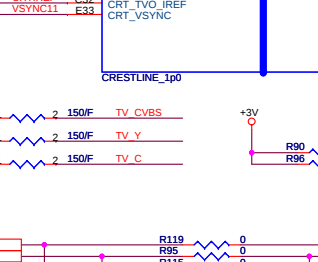
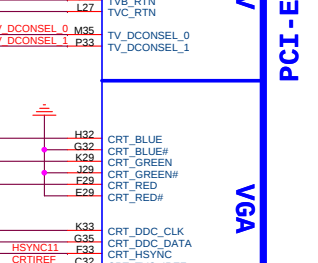
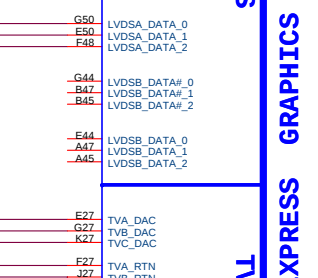
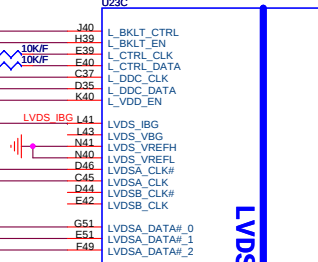
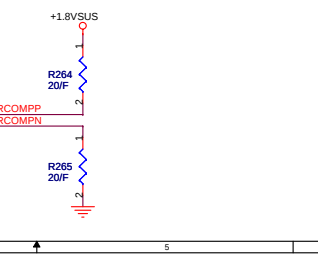
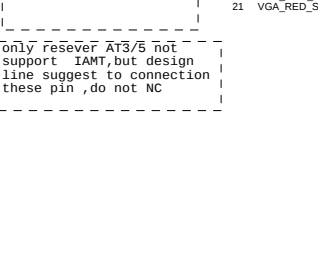
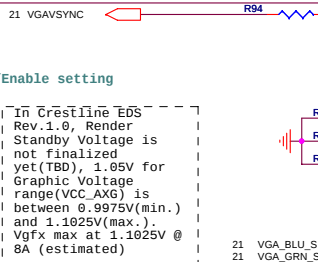
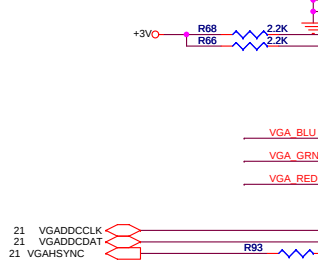
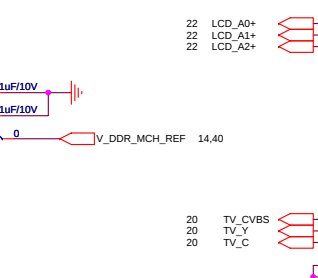
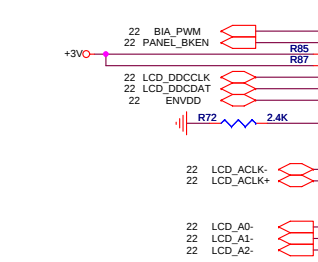
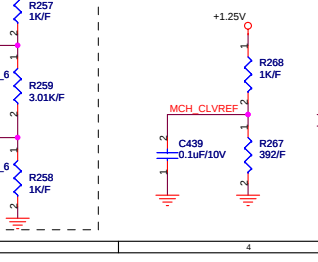
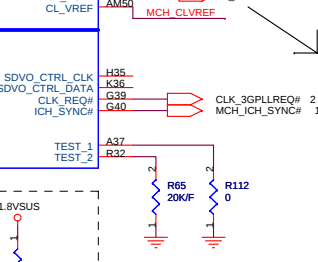
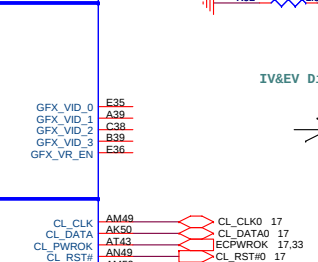
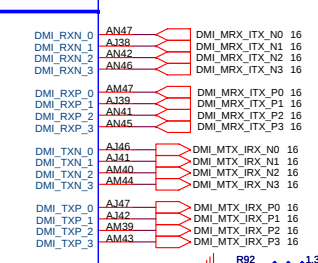
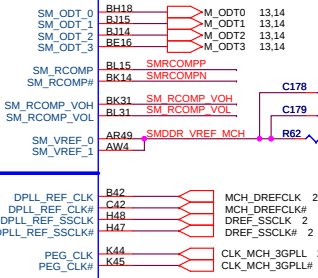
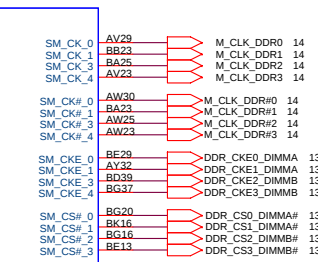
MISC

ON

TEST

TEST

TEST



14 DDR_A_D[63:0]

DDR A D0 AR43 SA_DQ_0
 DDR A D1 AW44 SA_DQ_1
 DDR A D2 BA45 SA_DQ_2
 DDR A D3 AY46 SA_DQ_3
 DDR A D4 AR41 SA_DQ_4
 DDR A D5 AR45 SA_DQ_5
 DDR A D6 AT42 SA_DQ_6
 DDR A D7 BB45 SA_DQ_7
 DDR A D8 AW47 SA_DQ_8
 DDR A D9 BF48 SA_DQ_9
 DDR A D10 BG47 SA_DQ_10
 DDR A D11 BJ45 SA_DQ_11
 DDR A D12 BB47 SA_DQ_12
 DDR A D13 BG50 SA_DQ_13
 DDR A D14 BH49 SA_DQ_14
 DDR A D15 BE45 SA_DQ_15
 DDR A D16 AW43 SA_DQ_16
 DDR A D17 BE44 SA_DQ_17
 DDR A D18 BG42 SA_DQ_18
 DDR A D19 BE40 SA_DQ_19
 DDR A D20 BE44 SA_DQ_20
 DDR A D21 BH45 SA_DQ_21
 DDR A D22 BG40 SA_DQ_22
 DDR A D23 BF40 SA_DQ_23
 DDR A D24 AR40 SA_DQ_24
 DDR A D25 AW40 SA_DQ_25
 DDR A D26 AT39 SA_DQ_26
 DDR A D27 AW36 SA_DQ_27
 DDR A D28 AW41 SA_DQ_28
 DDR A D29 AY41 SA_DQ_29
 DDR A D30 AY38 SA_DQ_30
 DDR A D31 AT38 SA_DQ_31
 DDR A D32 AV13 SA_DQ_32
 DDR A D33 AT13 SA_DQ_33
 DDR A D34 AW11 SA_DQ_34
 DDR A D35 AV11 SA_DQ_35
 DDR A D36 AU15 SA_DQ_36
 DDR A D37 AT11 SA_DQ_37
 DDR A D38 BA13 SA_DQ_38
 DDR A D39 BA11 SA_DQ_39
 DDR A D40 BE10 SA_DQ_40
 DDR A D41 BD10 SA_DQ_41
 DDR A D42 BD8 SA_DQ_42
 DDR A D43 AY9 SA_DQ_43
 DDR A D44 BG10 SA_DQ_44
 DDR A D45 AW9 SA_DQ_45
 DDR A D46 BD7 SA_DQ_46
 DDR A D47 BB9 SA_DQ_47
 DDR A D48 BB5 SA_DQ_48
 DDR A D49 AY7 SA_DQ_49
 DDR A D50 AT5 SA_DQ_50
 DDR A D51 AT7 SA_DQ_51
 DDR A D52 AY6 SA_DQ_52
 DDR A D53 BB7 SA_DQ_53
 DDR A D54 AR5 SA_DQ_54
 DDR A D55 AR8 SA_DQ_55
 DDR A D56 AR9 SA_DQ_56
 DDR A D57 AN3 SA_DQ_57
 DDR A D58 AM8 SA_DQ_58
 DDR A D59 AN10 SA_DQ_59
 DDR A D60 AT9 SA_DQ_60
 DDR A D61 AN9 SA_DQ_61
 DDR A D62 AM9 SA_DQ_62
 DDR A D63 AN11 SA_DQ_63

CRESTLINE_1p0

DDR SYSTEM MEMORY A

SA_BS_0 BB19
 SA_BS_1 BK19
 SA_BS_2 BF29
 SA_CAS# BL17
 SA_DM_0 AT45
 SA_DM_1 BD44
 SA_DM_2 BD42
 SA_DM_3 AW38
 SA_DM_4 AW13
 SA_DM_5 BG8
 SA_DM_6 AY5
 SA_DM_7 AN6
 SA_DQS_0 AT46
 SA_DQS_1 BE48
 SA_DQS_2 BB43
 SA_DQS_3 BG37
 SA_DQS_4 BB16
 SA_DQS_5 BH6
 SA_DQS_6 BB2
 SA_DQS_7 AP3
 SA_DQS#_0 AT47
 SA_DQS#_1 AR40
 SA_DQS#_2 BC41
 SA_DQS#_3 BA37
 SA_DQS#_4 BA16
 SA_DQS#_5 BH7
 SA_DQS#_6 BC1
 SA_DQS#_7 AP2
 SA_MA_0 BJ19
 SA_MA_1 BD20
 SA_MA_2 BK27
 SA_MA_3 BH28
 SA_MA_4 BL24
 SA_MA_5 BK28
 SA_MA_6 BJ27
 SA_MA_7 BJ25
 SA_MA_8 BL28
 SA_MA_9 BA28
 SA_MA_10 BC19
 SA_MA_11 BE28
 SA_MA_12 BG30
 SA_MA_13 BJ16

SA_RAS# BE18
 SA_RCVEN# AY20
 SA_WE# BA19

DDR_A_BS0 13.14
 DDR_A_BS1 13.14
 DDR_A_CAS# 13.14
 DDR_A_DM[0..7] 14
 DDR_A_DQS[7:0] 14
 DDR_A_DQS#[7:0] 14
 DDR_A_MA[13:0] 13.14
 DDR_A_RAS# 13.14
 DDR_A_WE# 13.14

14 DDR_B_D[63:0]

DDR B D0 AP49 SB_DQ_0
 DDR B D1 AR51 SB_DQ_1
 DDR B D2 AW50 SB_DQ_2
 DDR B D3 AW51 SB_DQ_3
 DDR B D4 AN51 SB_DQ_4
 DDR B D5 AN50 SB_DQ_5
 DDR B D6 AV50 SB_DQ_6
 DDR B D7 AV49 SB_DQ_7
 DDR B D8 BA50 SB_DQ_8
 DDR B D9 BB50 SB_DQ_9
 DDR B D10 BA49 SB_DQ_10
 DDR B D11 BE50 SB_DQ_11
 DDR B D12 BA51 SB_DQ_12
 DDR B D13 AY49 SB_DQ_13
 DDR B D14 BE50 SB_DQ_14
 DDR B D15 BE49 SB_DQ_15
 DDR B D16 BJ50 SB_DQ_16
 DDR B D17 BJ43 SB_DQ_17
 DDR B D18 BJ43 SB_DQ_18
 DDR B D19 BL43 SB_DQ_19
 DDR B D20 BK47 SB_DQ_20
 DDR B D21 BK49 SB_DQ_21
 DDR B D22 BK43 SB_DQ_22
 DDR B D23 BK42 SB_DQ_23
 DDR B D24 BJ41 SB_DQ_24
 DDR B D25 BL41 SB_DQ_25
 DDR B D26 BJ37 SB_DQ_26
 DDR B D27 BJ36 SB_DQ_27
 DDR B D28 BK41 SB_DQ_28
 DDR B D29 BJ40 SB_DQ_29
 DDR B D30 BL35 SB_DQ_30
 DDR B D31 BK37 SB_DQ_31
 DDR B D32 BK13 SB_DQ_32
 DDR B D33 BK11 SB_DQ_33
 DDR B D34 BK11 SB_DQ_34
 DDR B D35 BC11 SB_DQ_35
 DDR B D36 BC13 SB_DQ_36
 DDR B D37 BE12 SB_DQ_37
 DDR B D38 BC12 SB_DQ_38
 DDR B D39 BG12 SB_DQ_39
 DDR B D40 BJ10 SB_DQ_40
 DDR B D41 BL9 SB_DQ_41
 DDR B D42 BK5 SB_DQ_42
 DDR B D43 BL5 SB_DQ_43
 DDR B D44 BK9 SB_DQ_44
 DDR B D45 BK10 SB_DQ_45
 DDR B D46 BJ8 SB_DQ_46
 DDR B D47 BJ6 SB_DQ_47
 DDR B D48 BE4 SB_DQ_48
 DDR B D49 BH5 SB_DQ_49
 DDR B D50 BC1 SB_DQ_50
 DDR B D51 BC2 SB_DQ_51
 DDR B D52 BK3 SB_DQ_52
 DDR B D53 BE4 SB_DQ_53
 DDR B D54 BD3 SB_DQ_54
 DDR B D55 BA3 SB_DQ_55
 DDR B D56 BB3 SB_DQ_56
 DDR B D57 AR1 SB_DQ_57
 DDR B D58 AT3 SB_DQ_58
 DDR B D59 AY2 SB_DQ_59
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 DDR B D61 AU2 SB_DQ_61
 DDR B D62 AU2 SB_DQ_62
 DDR B D63 AT2 SB_DQ_63

CRESTLINE_1p0

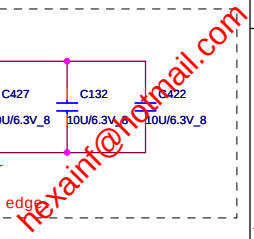
DDR SYSTEM MEMORY B

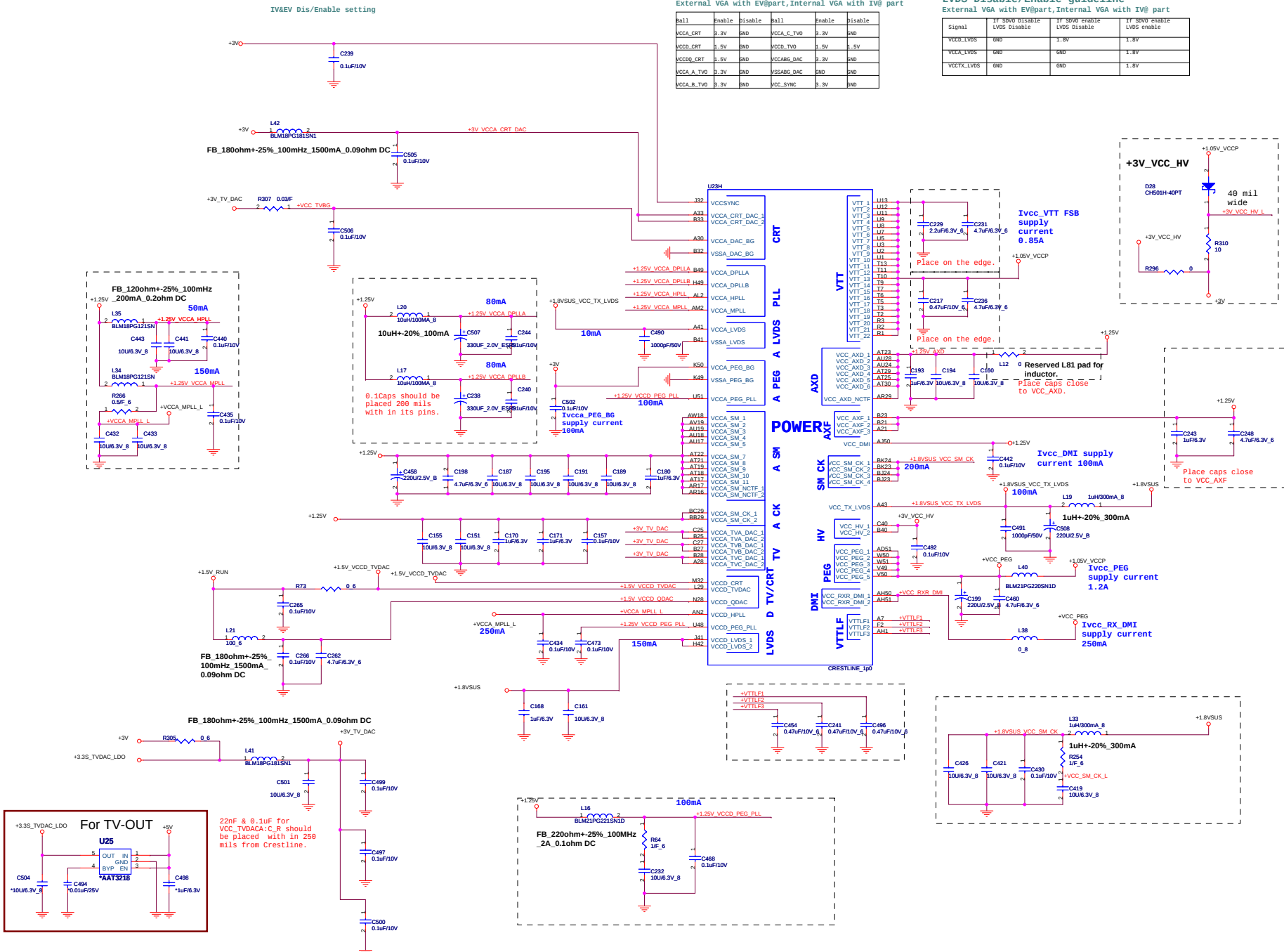
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 SB_BS_1 BG18
 SB_BS_2 BG36
 SB_CAS# BE17
 SB_DM_0 AR50
 SB_DM_1 BD49
 SB_DM_2 BK45
 SB_DM_3 BL39
 SB_DM_4 BH12
 SB_DM_5 BE3
 SB_DM_6 AW2
 SB_DM_7
 SB_DQS_0 AT50
 SB_DQS_1 BD50
 SB_DQS_2 BK46
 SB_DQS_3 BK39
 SB_DQS_4 BJ12
 SB_DQS_5 BE2
 SB_DQS_6 AV2
 SB_DQS_7 AU50
 SB_DQS#_0 RC50
 SB_DQS#_1 BL45
 SB_DQS#_2 BK38
 SB_DQS#_3 BK12
 SB_DQS#_4 BK7
 SB_DQS#_5 BE2
 SB_DQS#_6 AV3

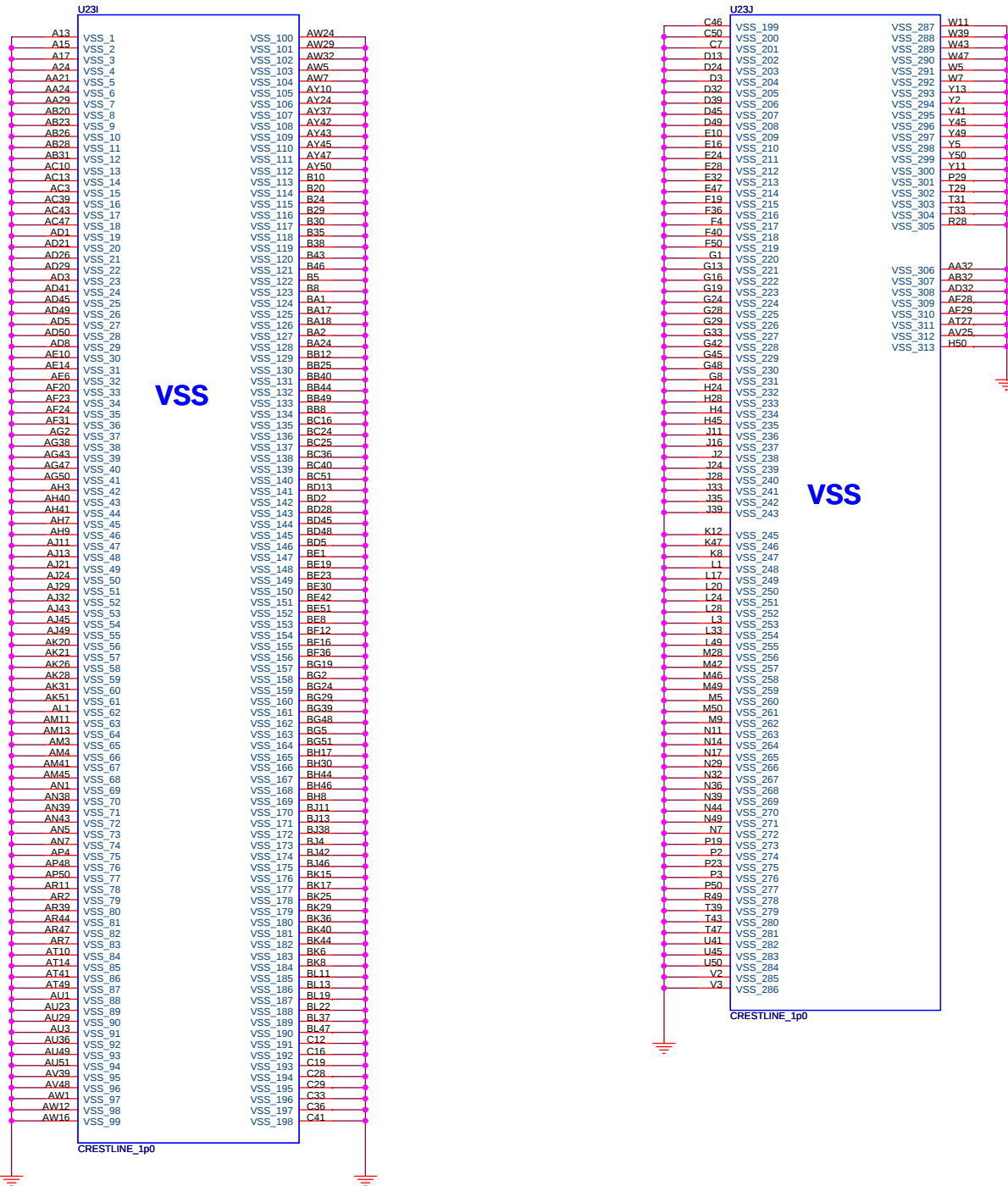
DDR_B_BS0 13.14
 DDR_B_BS1 13.14
 DDR_B_BS2 13.14
 DDR_B_CAS# 13.14
 DDR_B_DM[0..7] 14
 DDR_B_DQS[7:0] 14
 DDR_B_DQS#[7:0] 14
 DDR_B_MA[13:0] 13.14
 DDR_B_RAS# 13.14
 DDR_B_WE# 13.14



PROJECT : SW7
 Quanta Computer Inc.

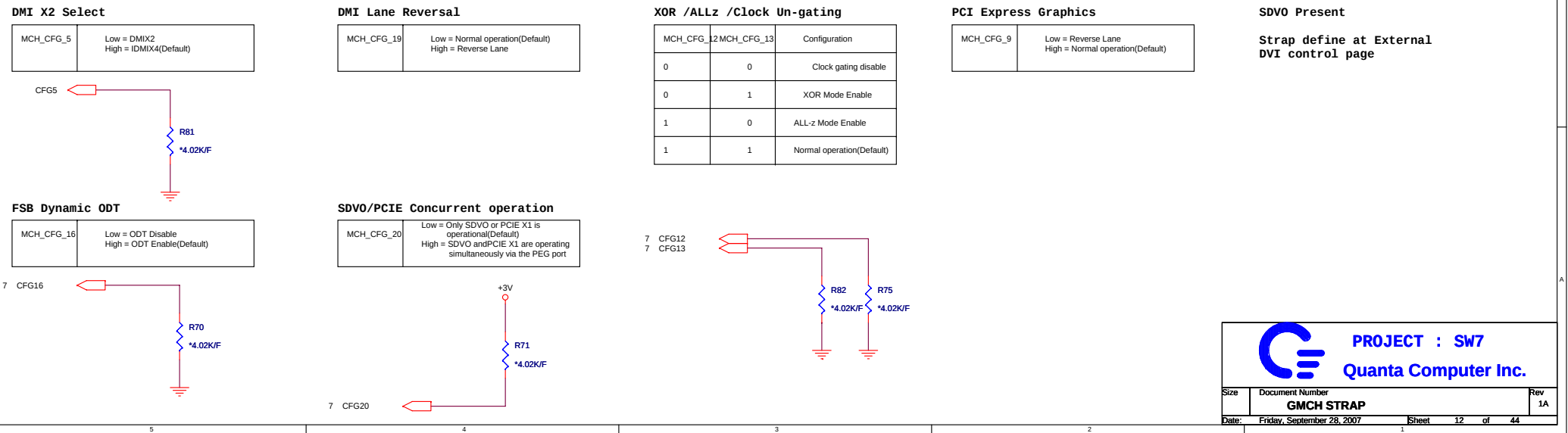






All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal
CFG[17:3] Have internal Pull-up
CFG[18:19] Have internal Pull-down
Any CFG signal strapping option not list below should be left NC Pin

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU(Default)
CFG8	Low power PCI Express	0 = Normal mode 1 = Low Power mode
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIE concurrent	0 = Only SDVO or PCIE x1 is operation(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

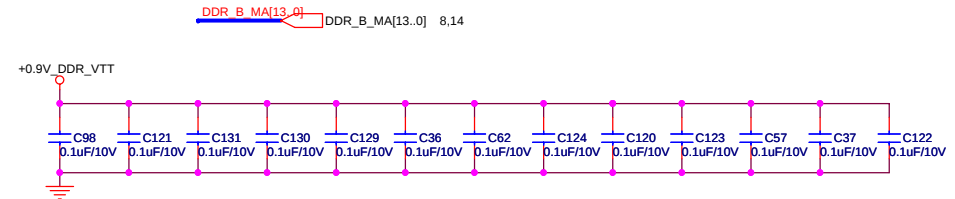
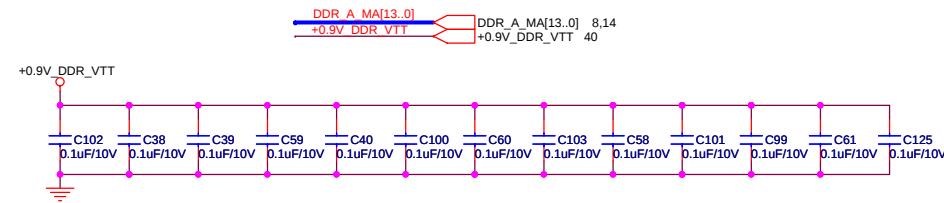


DDRII DUAL CHANNEL A, B.

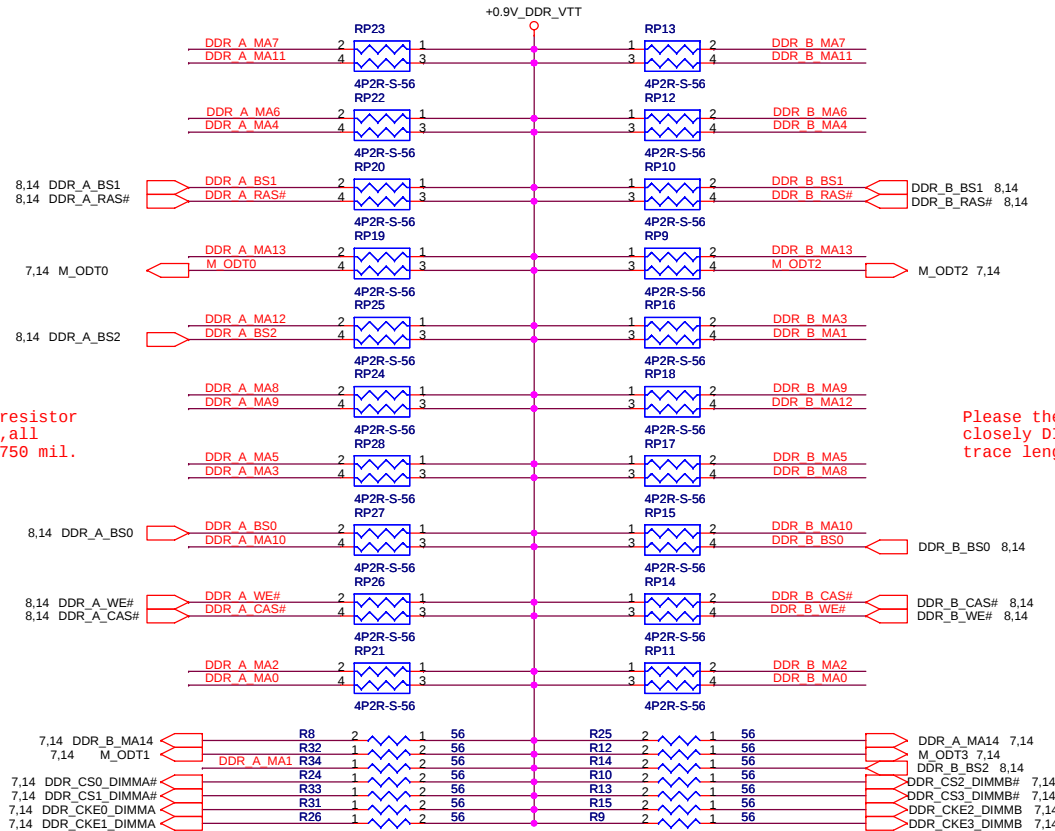
13

DDRII A CHANNEL

DDRII B CHANNEL



Layout note: Place one cap close to every 2 pullup resistors terminated to SMDR_VTERM

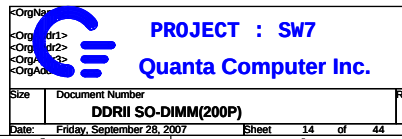


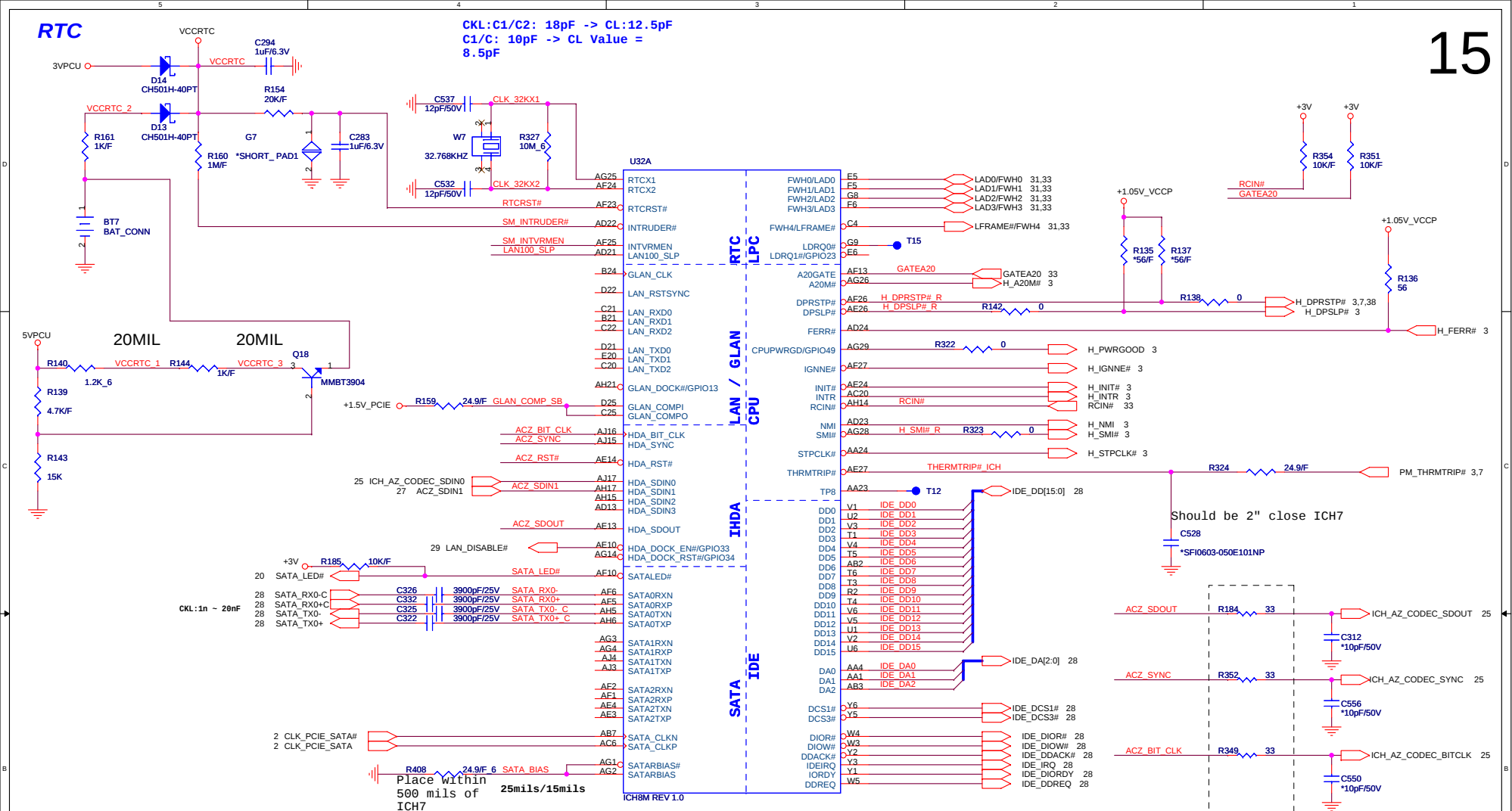
		PROJECT : SW7	
		Quanta Computer Inc.	
Size	Document Number	Rev	
	DDRII RES.ARRAY	1A	
Date:	Friday, September 28, 2007	Sheet	13 of 44

hex@inf@hmail.com



PROJECT :
Quanta Com





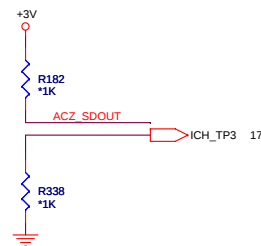
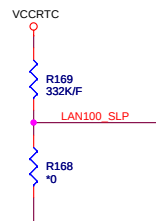
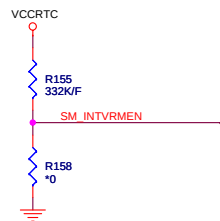
SB Strap

ICH8-M Internal VR Enable strap
(Internal VR for Vccsus1_05, VccSus1_5 and VccCL1_5)

INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)
----------	---

**ICH8-M LAN100_SLP Strap
(Internal VR for VccLAN1_05 and
VccCL1.05)**

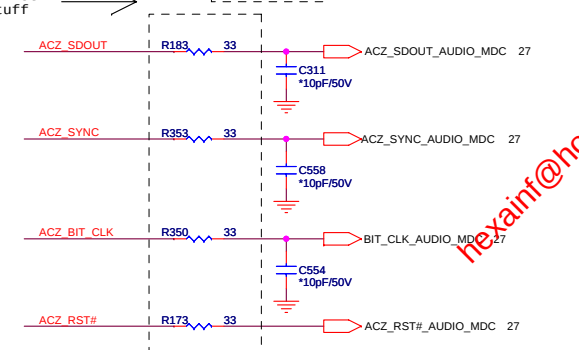
LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)
------------	---



XOR Chain Entrance Strap

ICH_RSV0	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal operation(Default)
1	1	Set PCIe port config bit 1

```
intel check list
define to stuff
33ohm
```



PROJECT : SW7
Quanta Computer Inc.

Size	Document Number	Rev
	ICH8-M HOST(1/4)	1
Date:	Friday, September 28, 2007	Sheet 15 of 44

UDIO_MDC 27

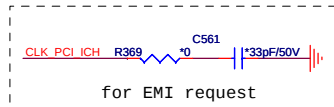
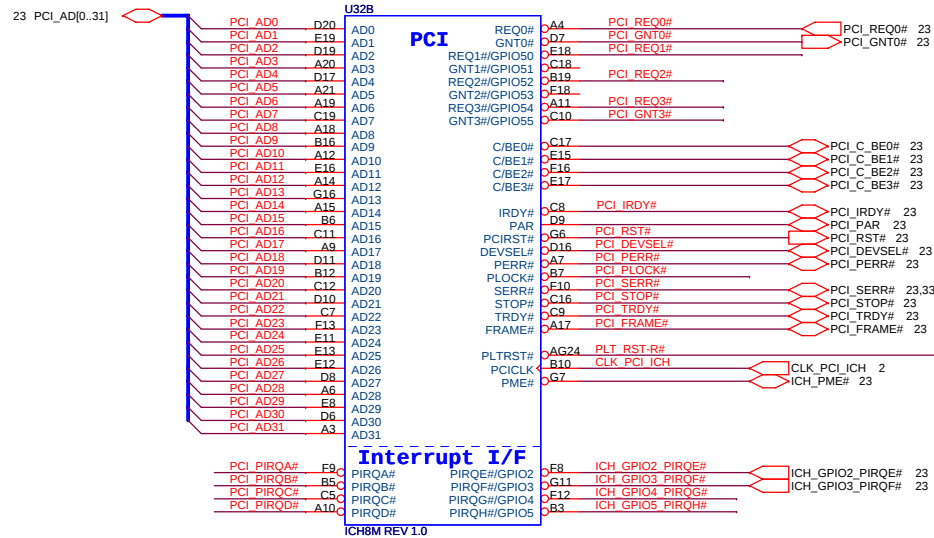
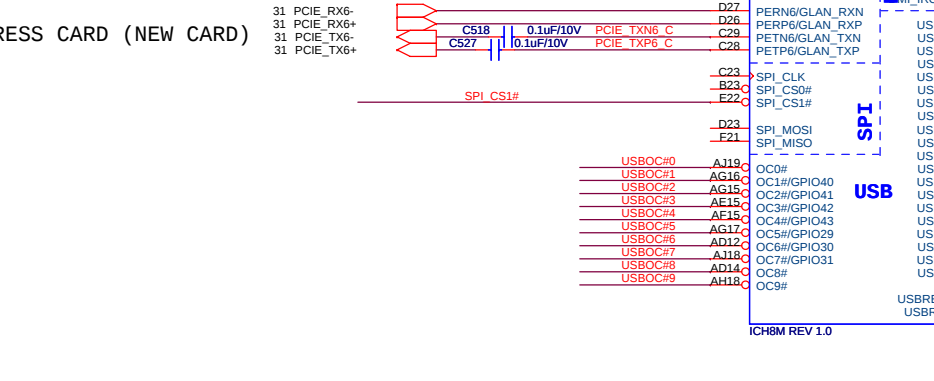
DIO_MDC 27

9_MDC 27

MINI CARD WLAN PCI-E

PCI-E-LAN

EXPRESS CARD (NEW CARD)



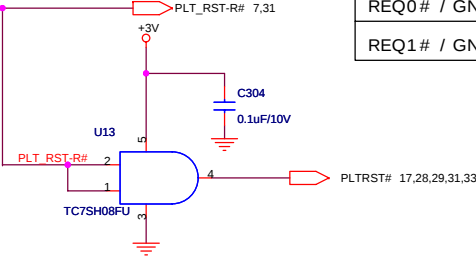
Direct Media Interface

SPI

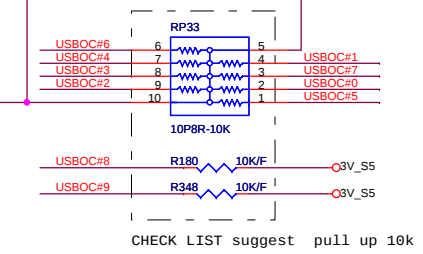
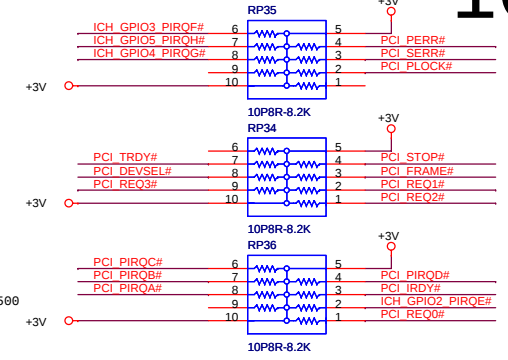
USB

ICH8M REV 1.0

25mils/15mils
Place within 500
mils of ICH7

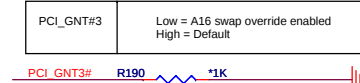


PCI Pullups



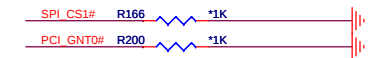
CHECK LIST suggest pull up 10k

A16 SWAP Override strap



ICH8 Boot BIOS select

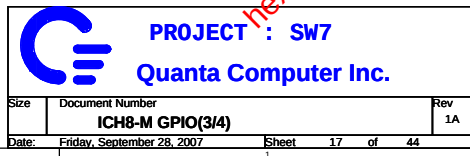
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC

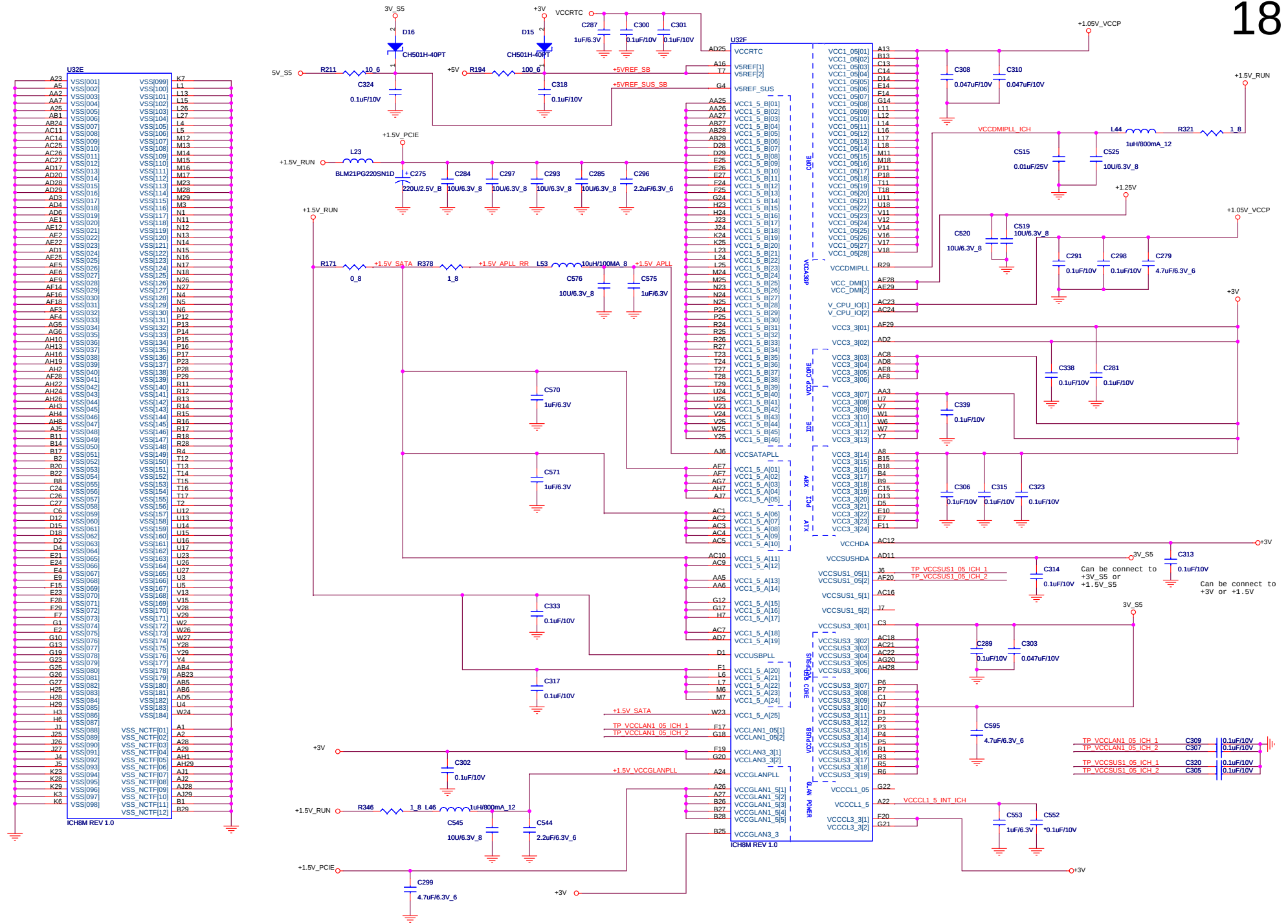


PCI ROUTING TABLE	IDSEL	INTERRUPT	DEVICE
REQ0# / GNT0#	AD25	INTE#,INTF#	PCI17402
REQ1# / GNT1#	AD22	INTC#,INTD#	MINI PCI for debug

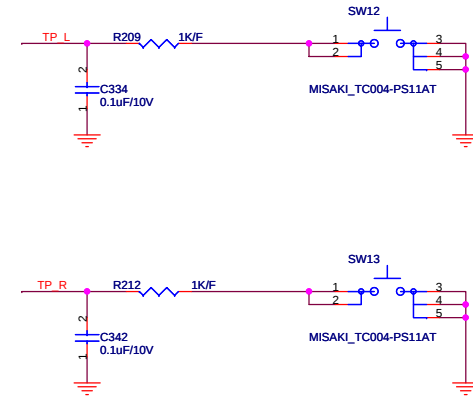
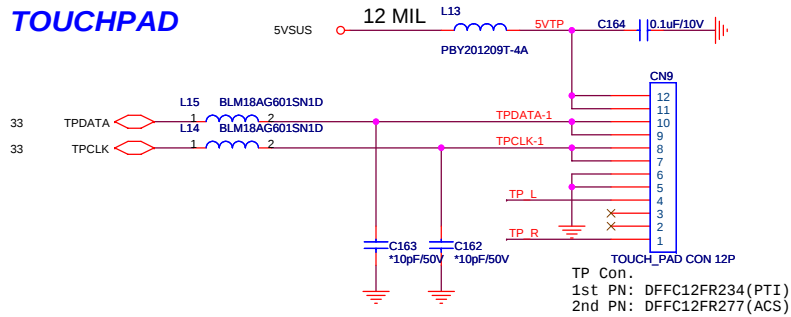
PROJECT : SW7
Quanta Computer Inc.

Size	Document Number	Rev
	ICH8-M M PCI E(2/4)	1A
Date:	Friday, September 28, 2007	Sheet 16 of 44

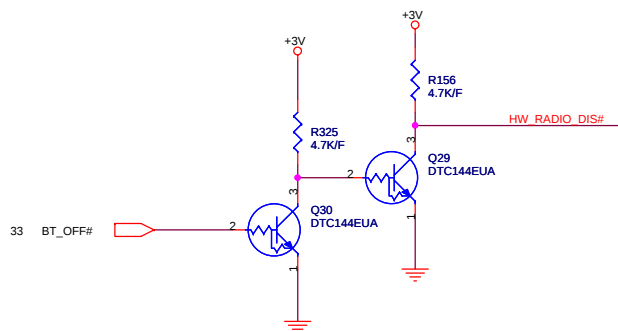
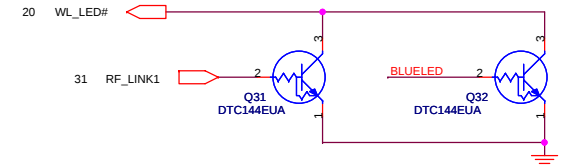
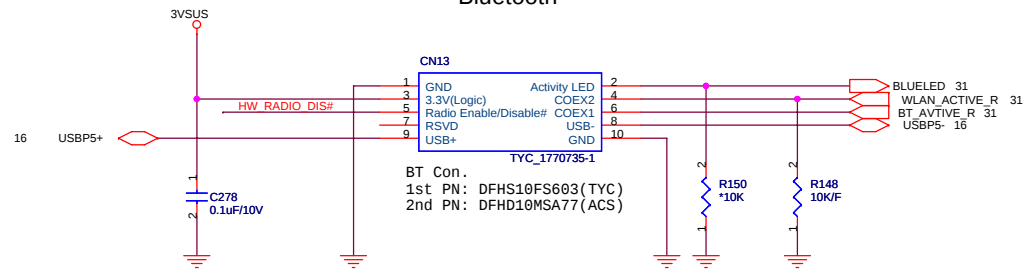




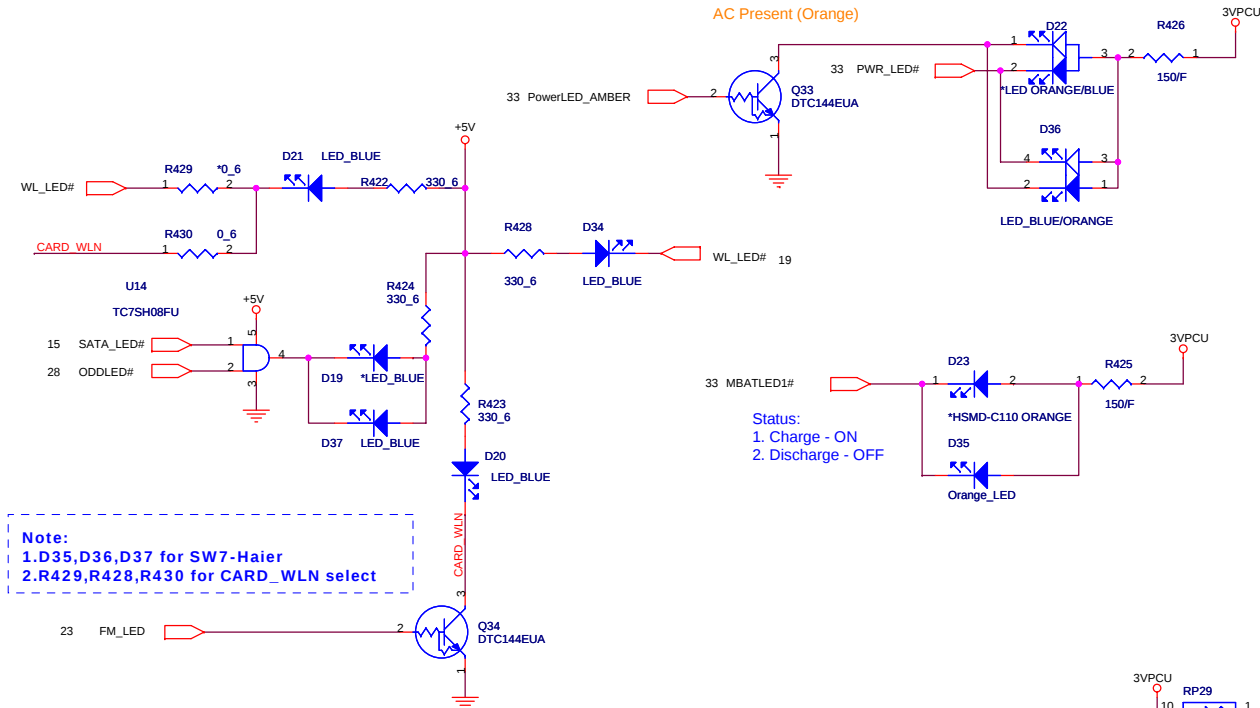
TOUCHPAD



Bluetooth



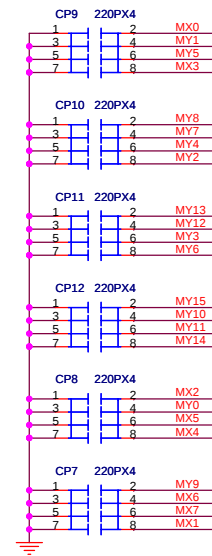
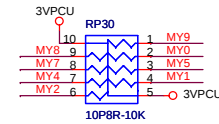
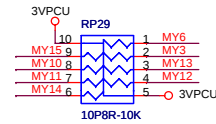
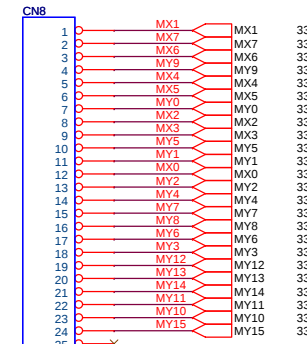
hexainf@hotmail.com



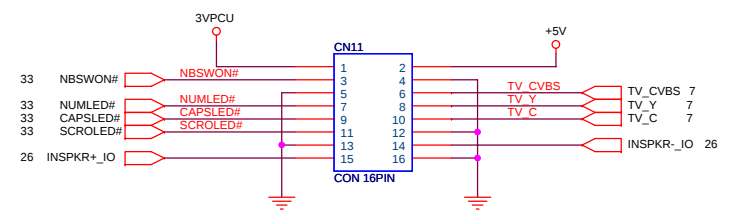
Note:
 1.D35,D36,D37 for SW7-Haier
 2.R429,R428,R430 for CARD_WLN select

Status:
 1. Charge - ON
 2. Discharge - OFF

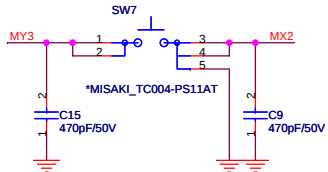
KEYBOARD



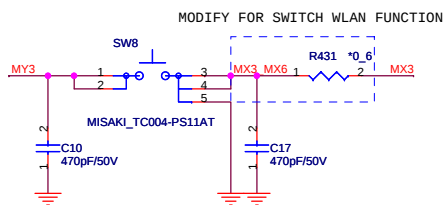
I/O Board CONN



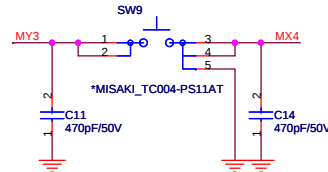
IE



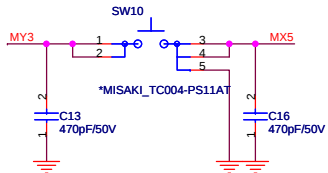
E-Mail



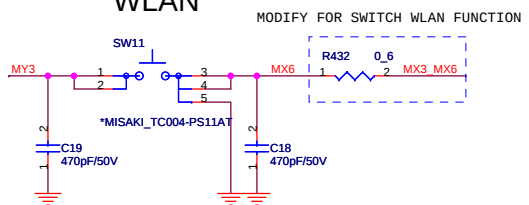
FAN

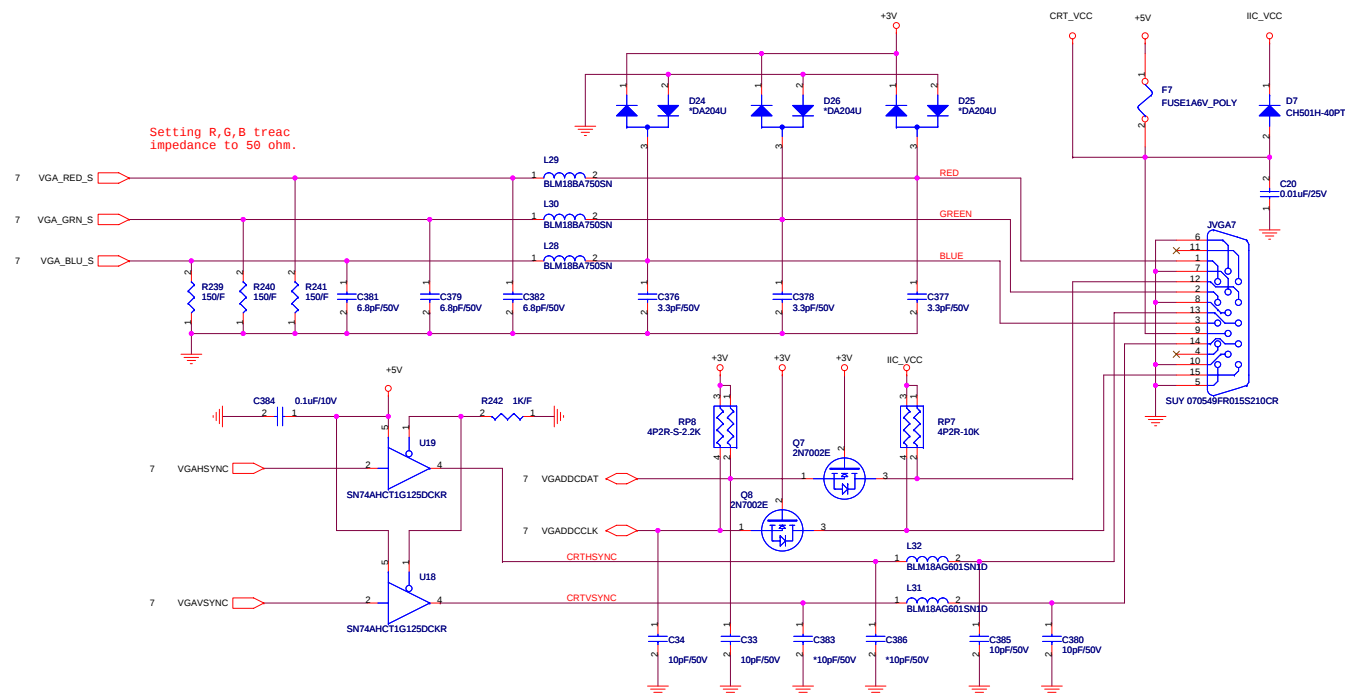


MUTE



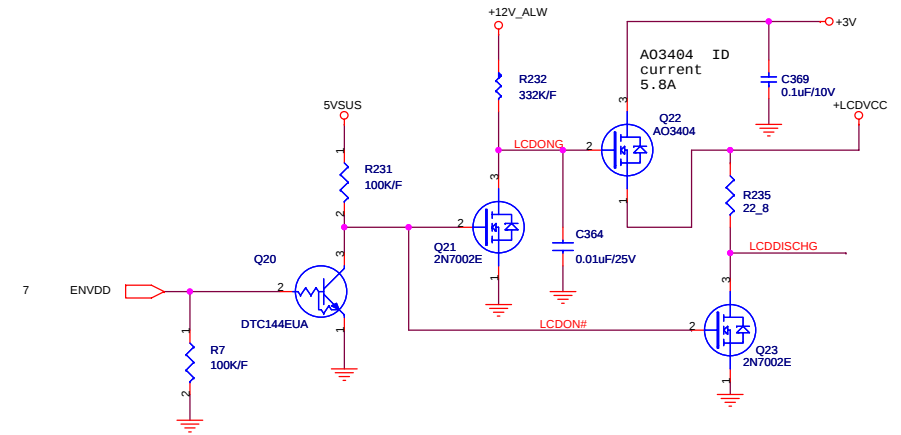
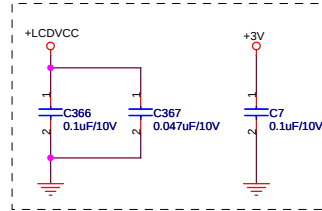
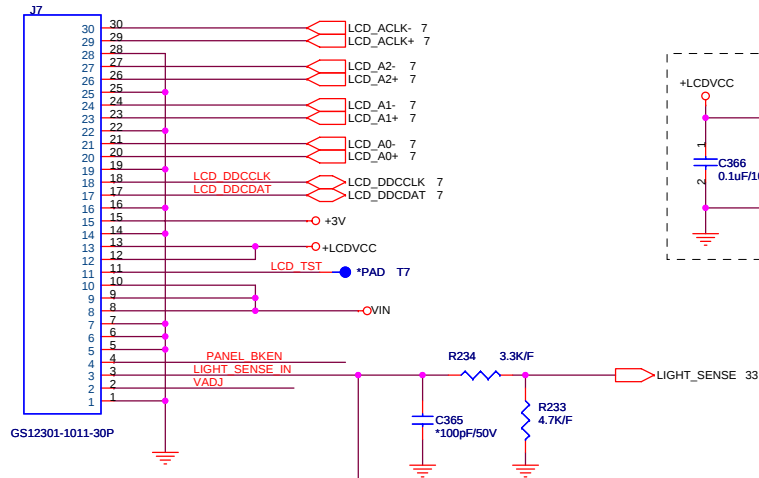
WLAN



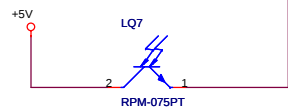


hexainf@hotmail.com

LCD CONNECTOR

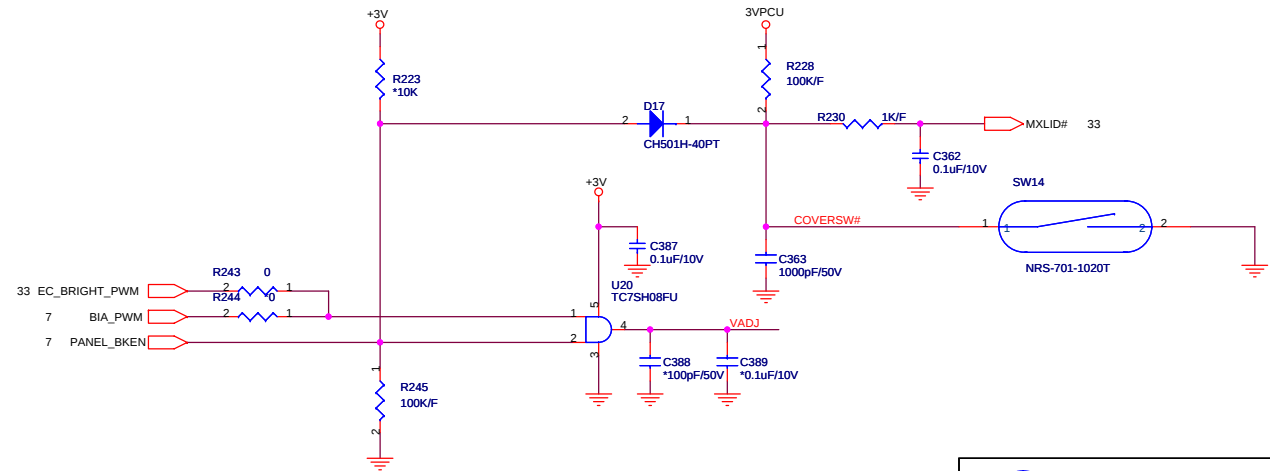
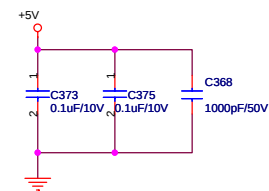


Light sensor



Pin 1: Emitter

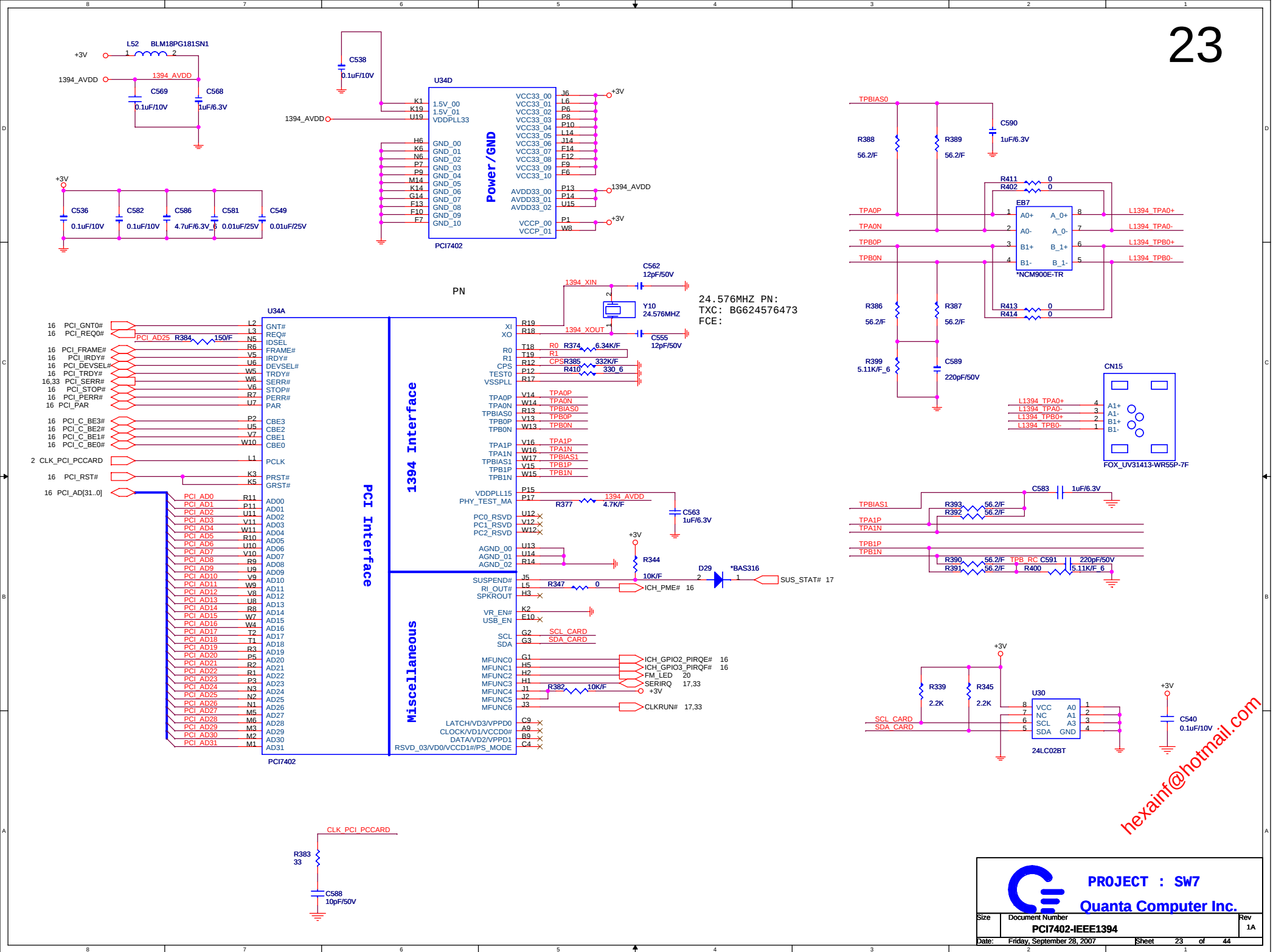
Pin 2: Collector

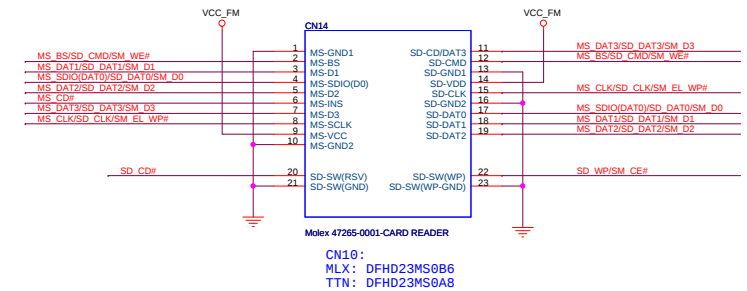
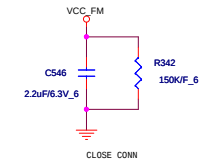
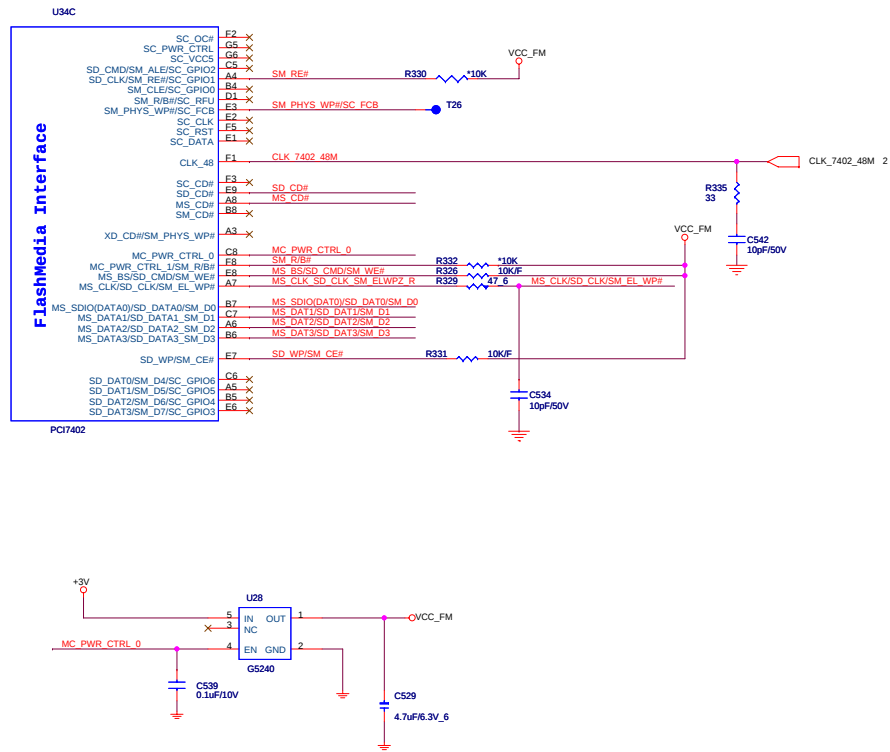
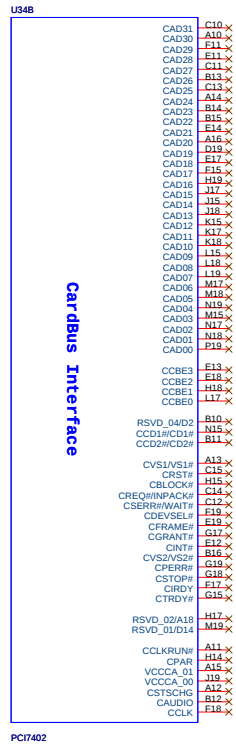


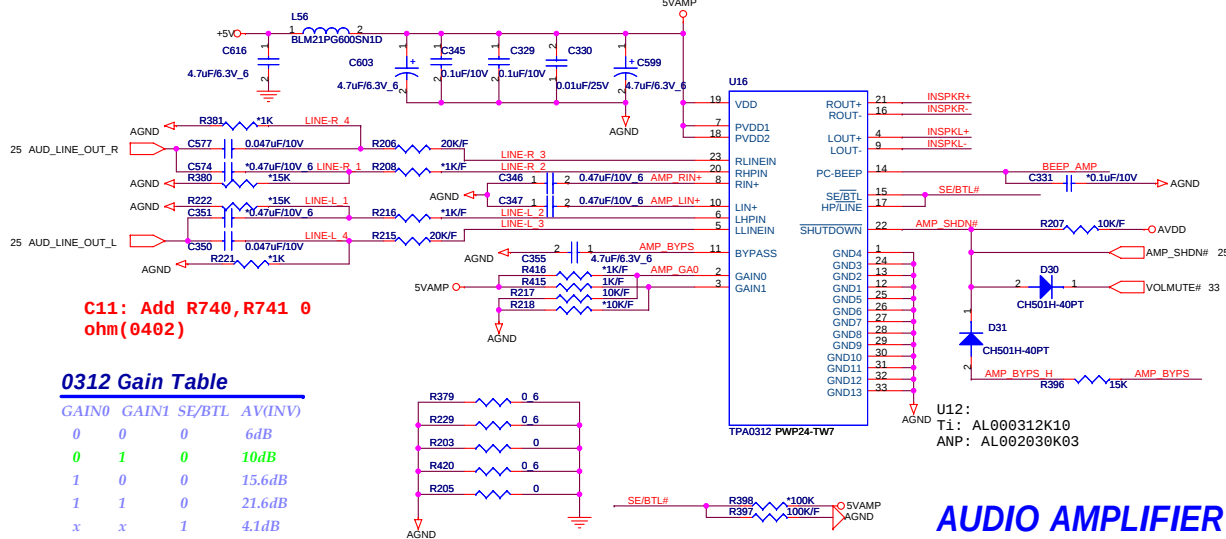
PROJECT : SW7
Quanta Computer Inc.

Size	Document Number	Rev
	LCD CONN	1A

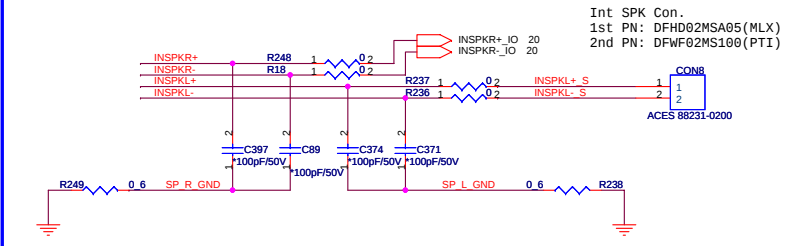
Date: Friday, September 28, 2007 Sheet 22 of 44



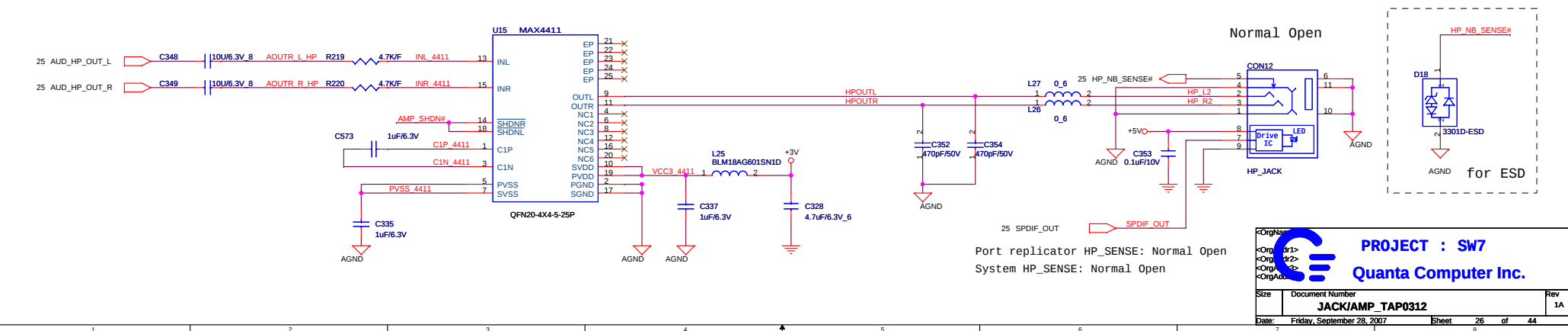
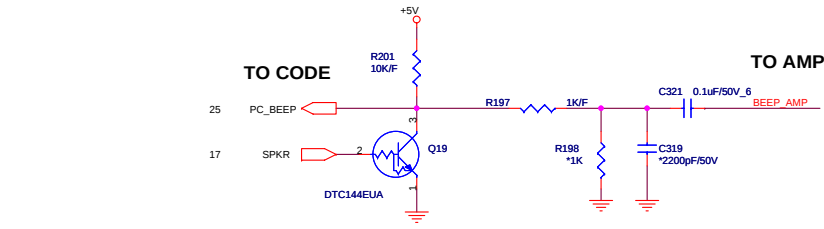




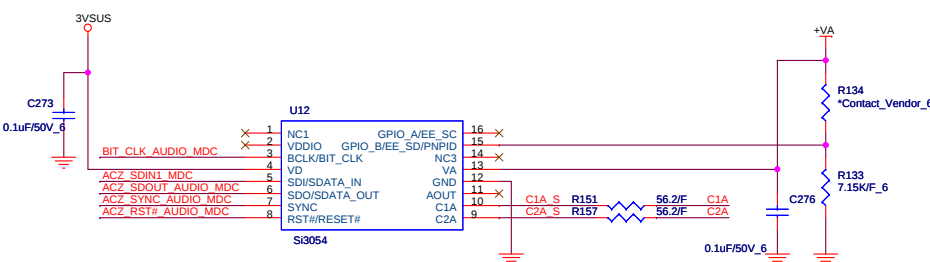
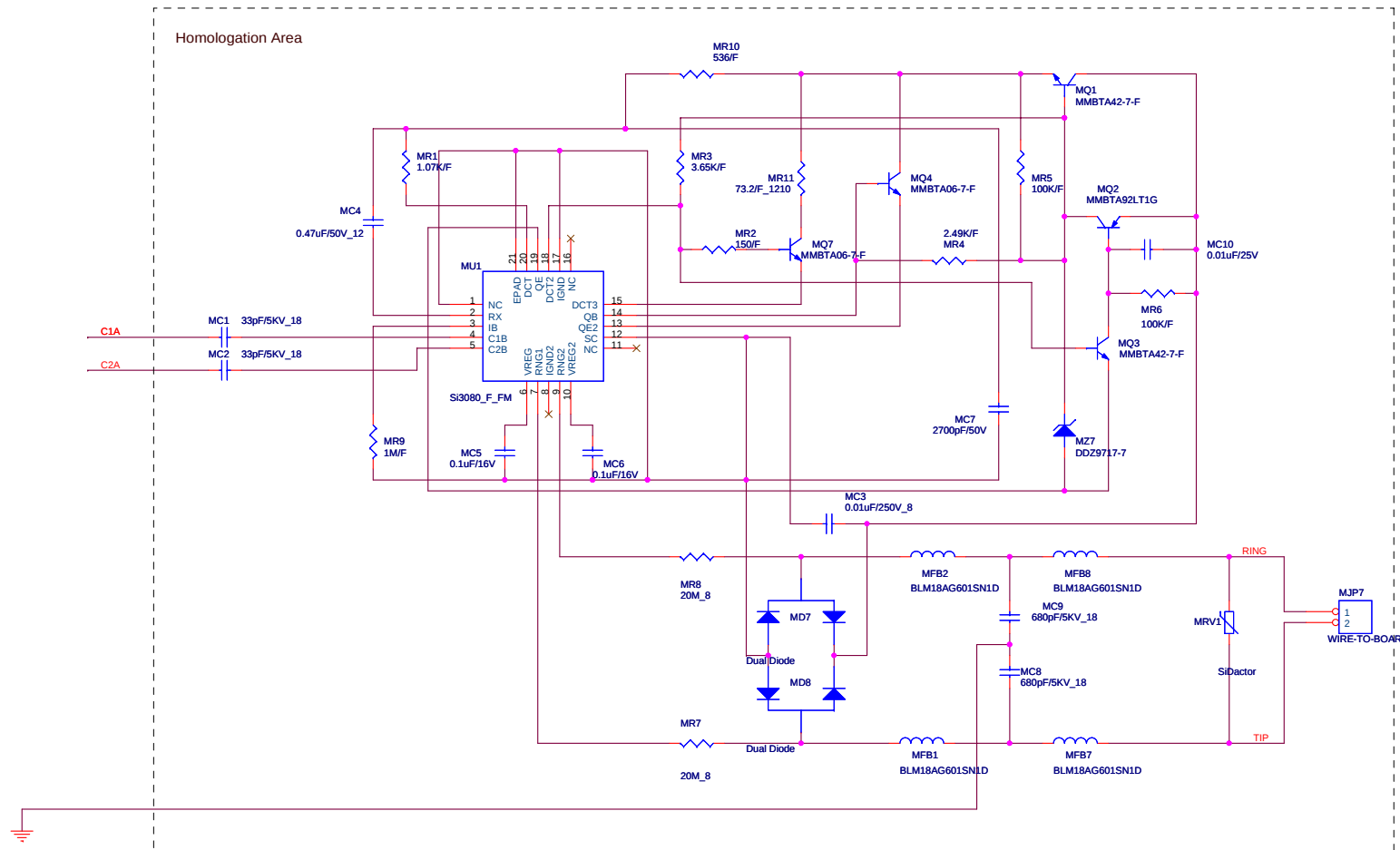
INT. SPEAKER



PCSPK BEEP



No Ground Plane In DAA Section



ACZ_RST# AUDIO_MDC 15
ACZ_SYNC AUDIO_MDC 15
BIT_CLK AUDIO_MDC 15
ACZ_SDOUT AUDIO_MDC 15
ACZ_SDIN1 MDC R147 33
ACZ_SDIN1 15

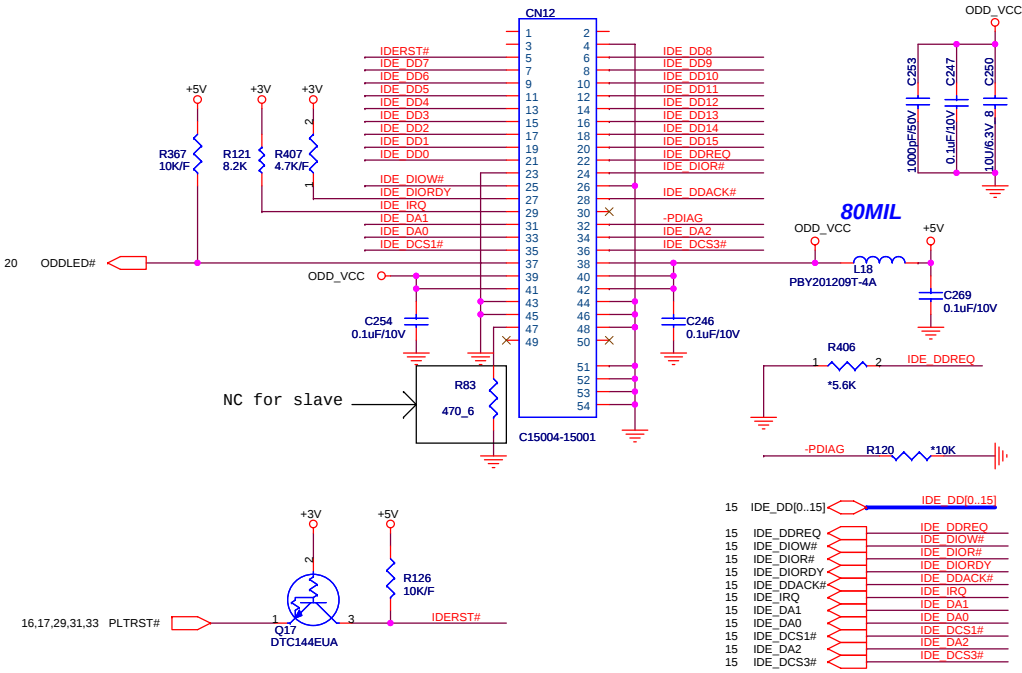
SILICON LABORATORIES CONFIDENTIAL

PROJECT : SW7

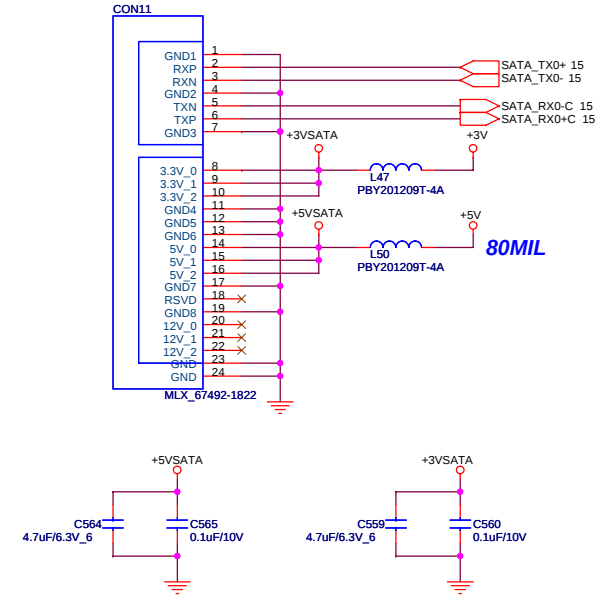
Quantia Computer Inc.

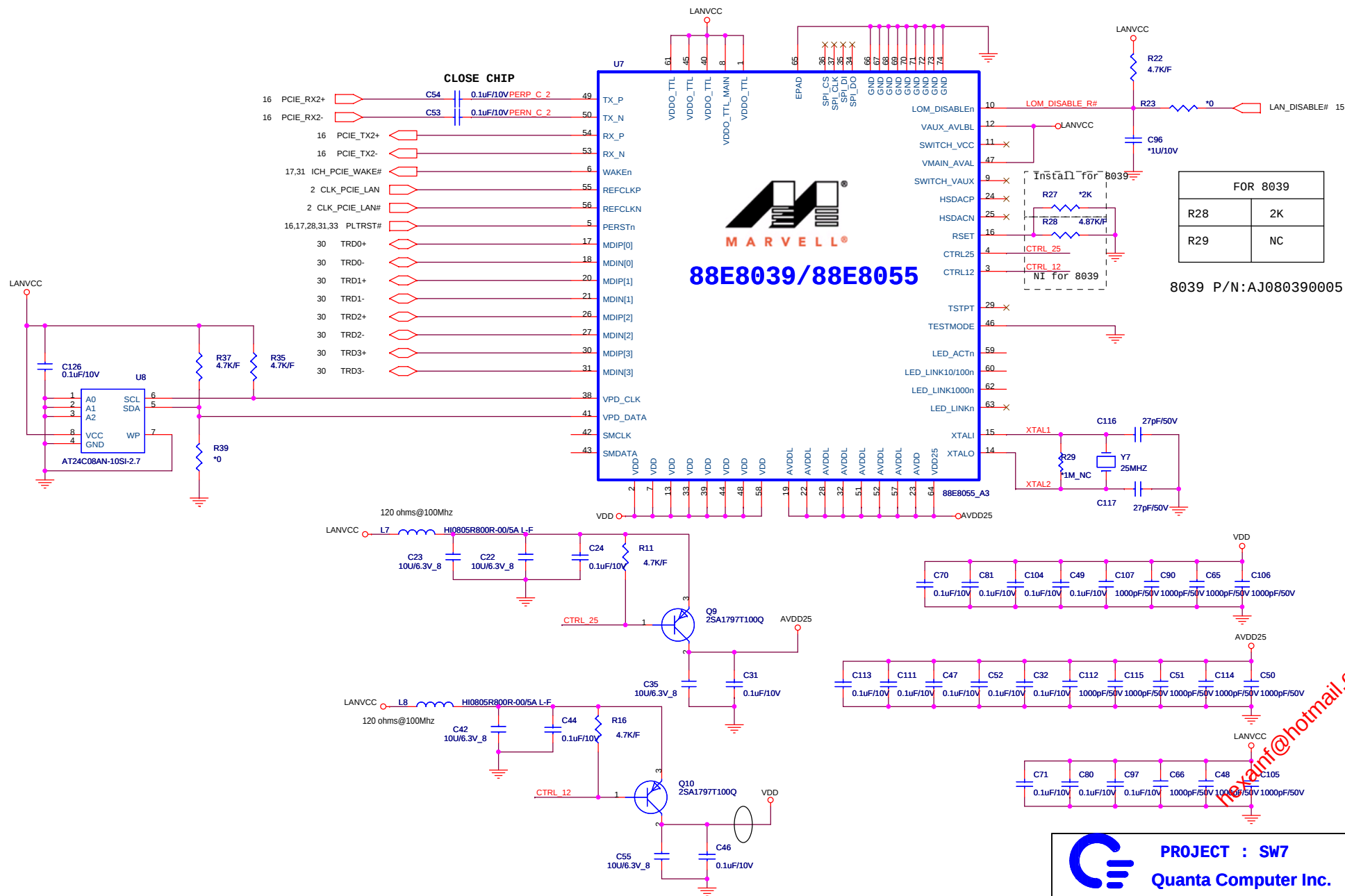
Size	Document Number	Rev	1A
MODEM(DAA)			
Date:	Friday, September 28, 2007	Sheet	27 of 44

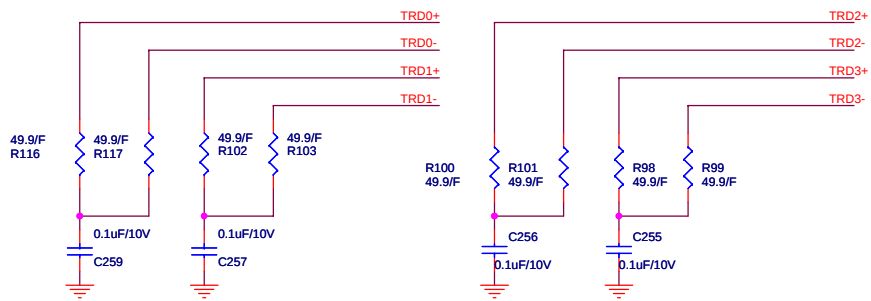
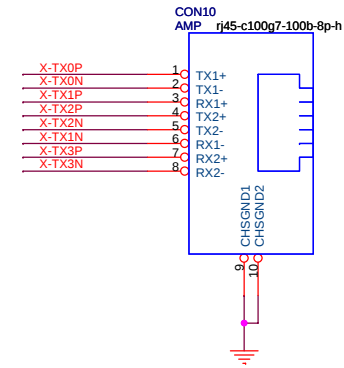
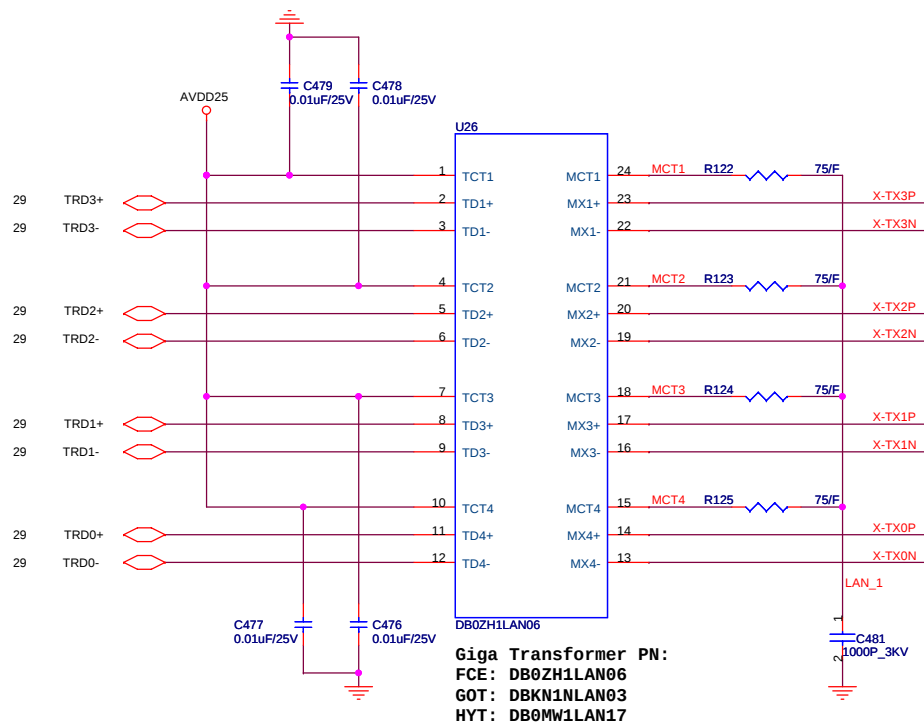
ODD CONNECTOR

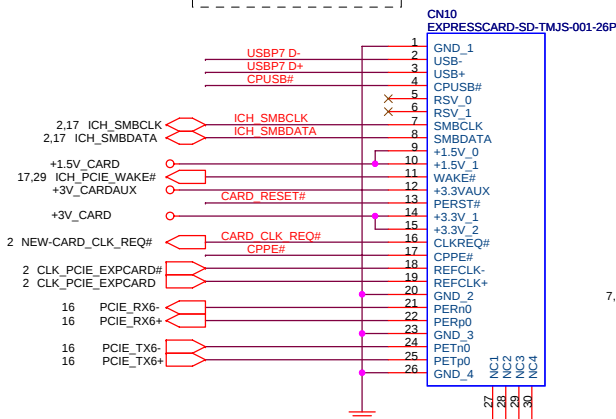
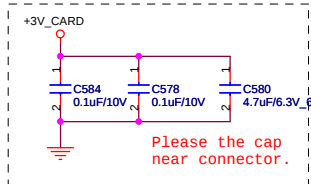
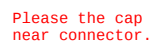


SATA Connector.

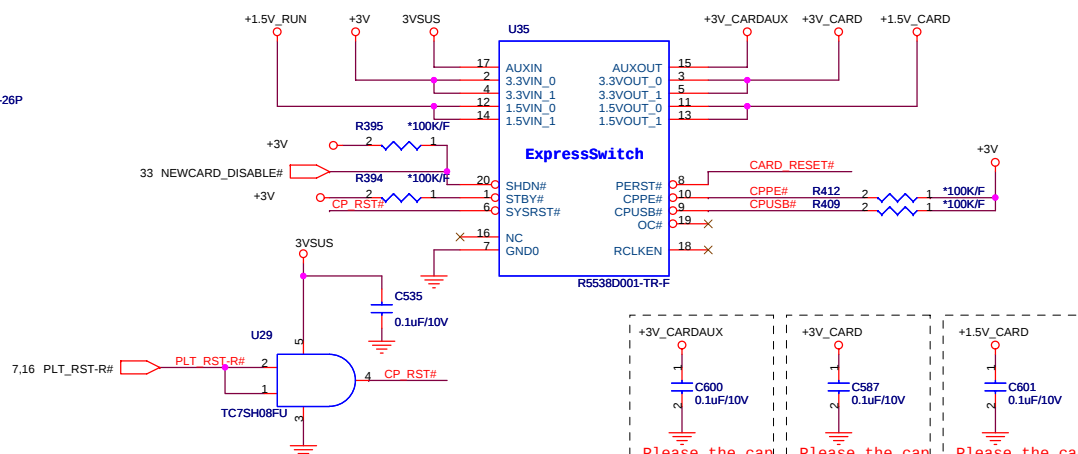








PCI-Express TX and RX direct to connector.



Please the cap
near pin 15
(AUXOUT).

Please the cap
near pin 3 & 5
(3.3VOUT).

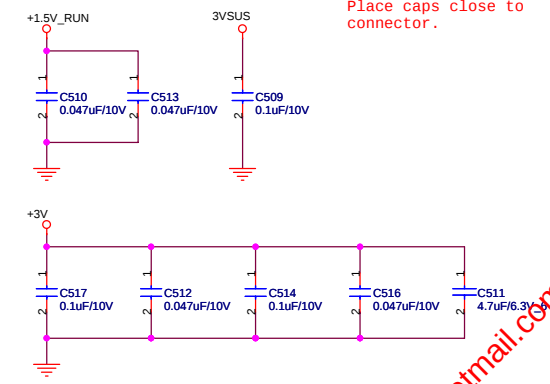
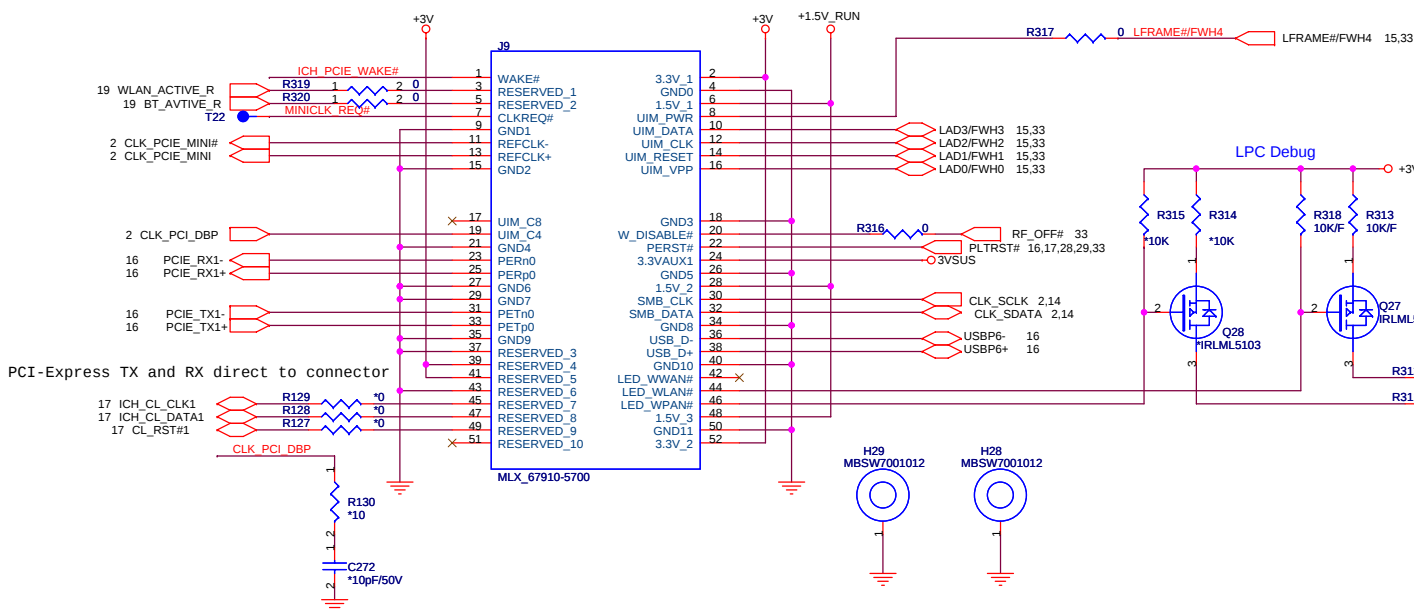
Please the cap near pin 11 & 13(1.5VOUT).

Please the cap
near pin 12 &
14(1.5VIN).

Please the cap
near pin 2 & 4
(3.3VIN).

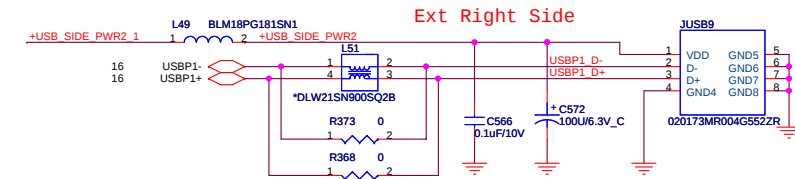
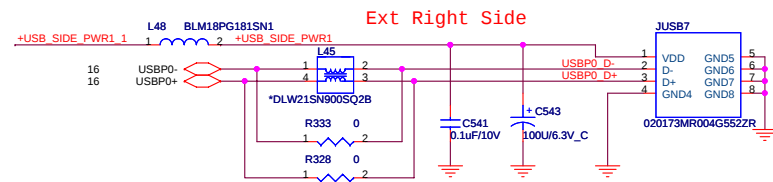
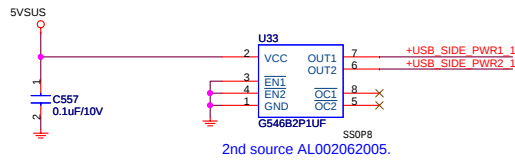
Please the cap
near pin 17
(AUXIN).

Place caps close to connector.

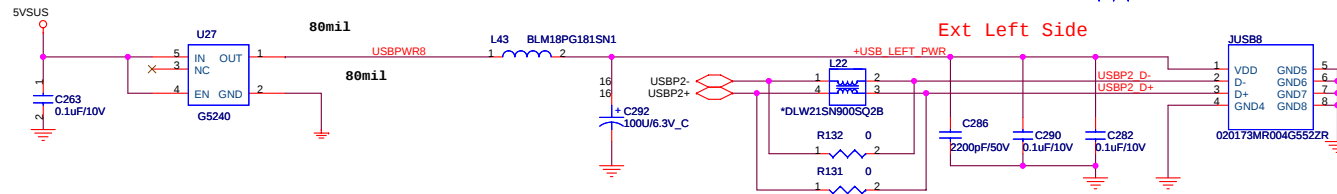


PROJECT : SW7
Quanta Computer Inc.

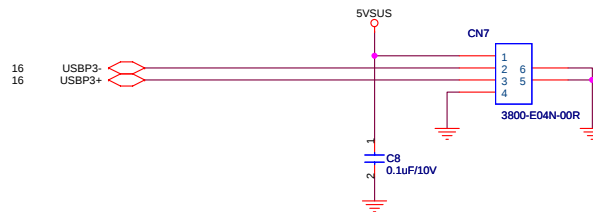
Size	Document Number	Rev
	Express card & Mini Card	1A
Date:	Friday, September 28, 2007	Sheet 31 of 44

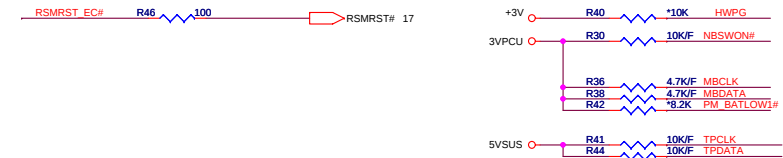
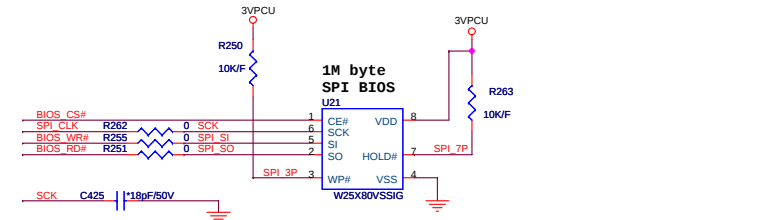
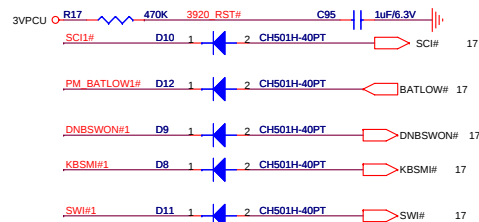
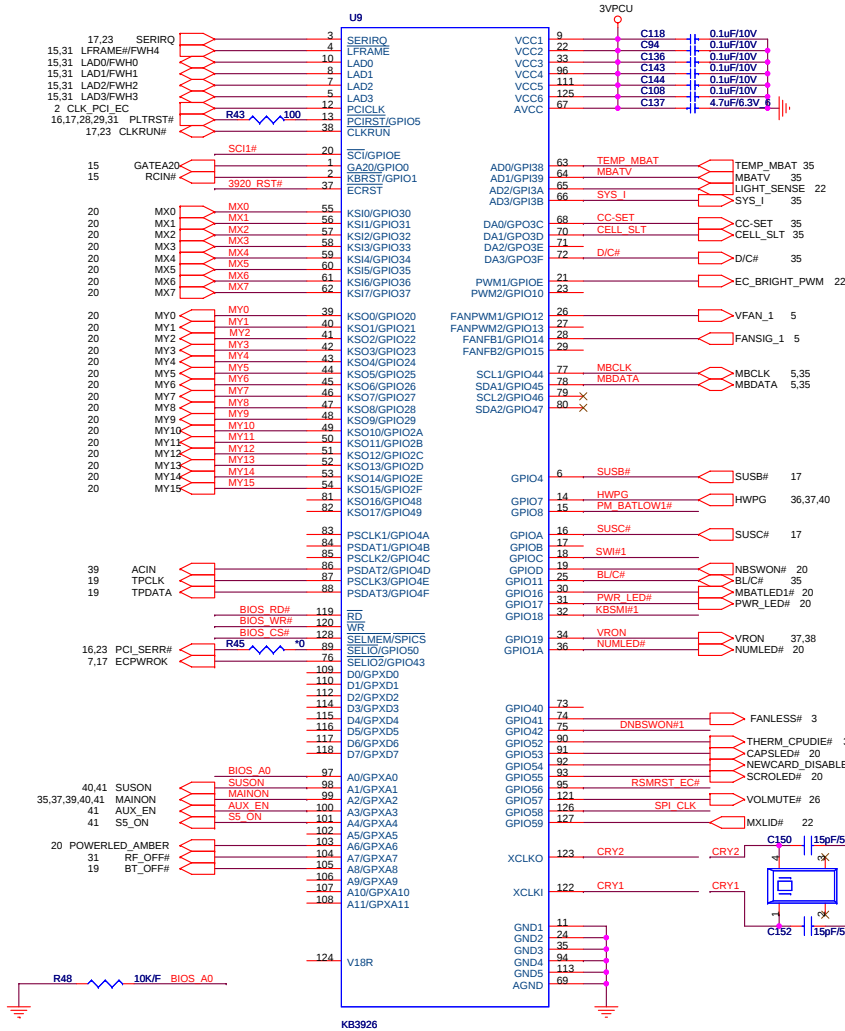


USB Con.
1st PN: DFHS04FR920(SUY)
2nd PN: DFHS04FRB11(A0P)



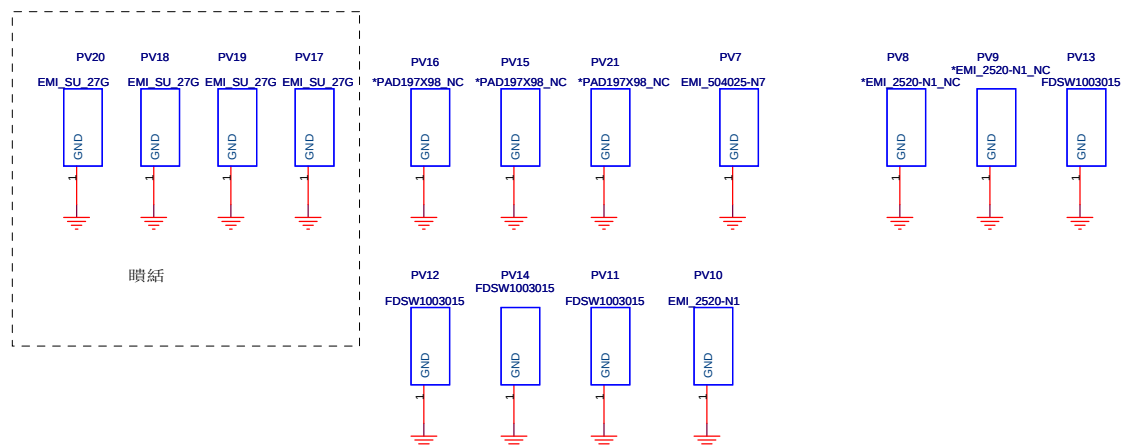
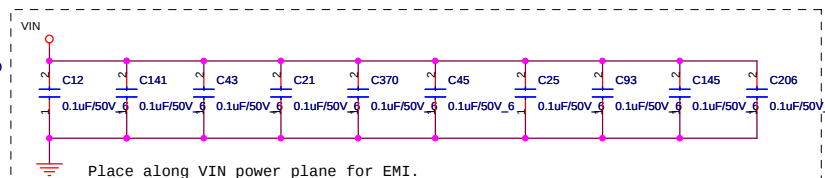
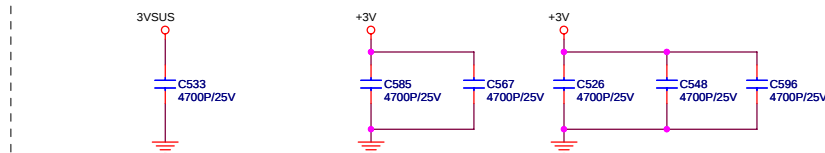
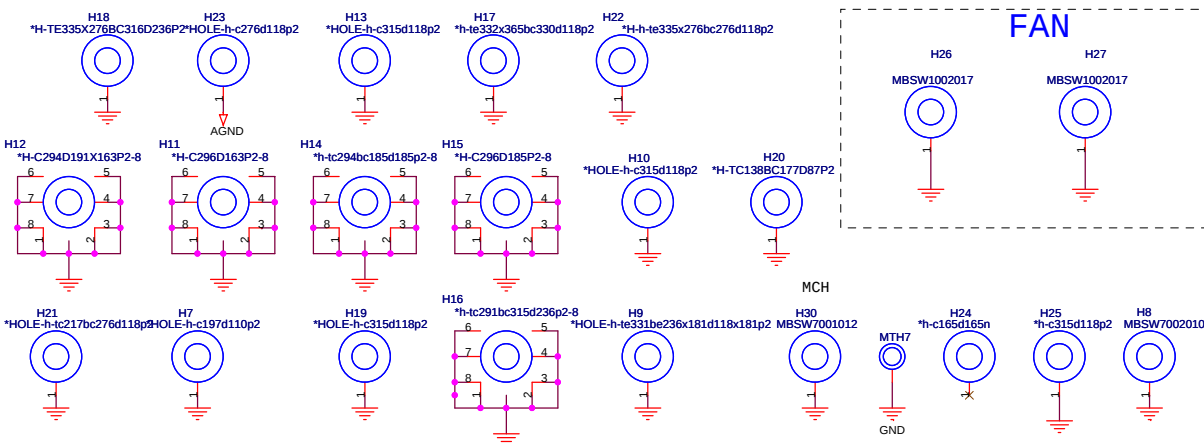
Int USB Con.
1st PN: DFHD04MR876(EIC)
2nd PN: DFHD04MR981(PTI)



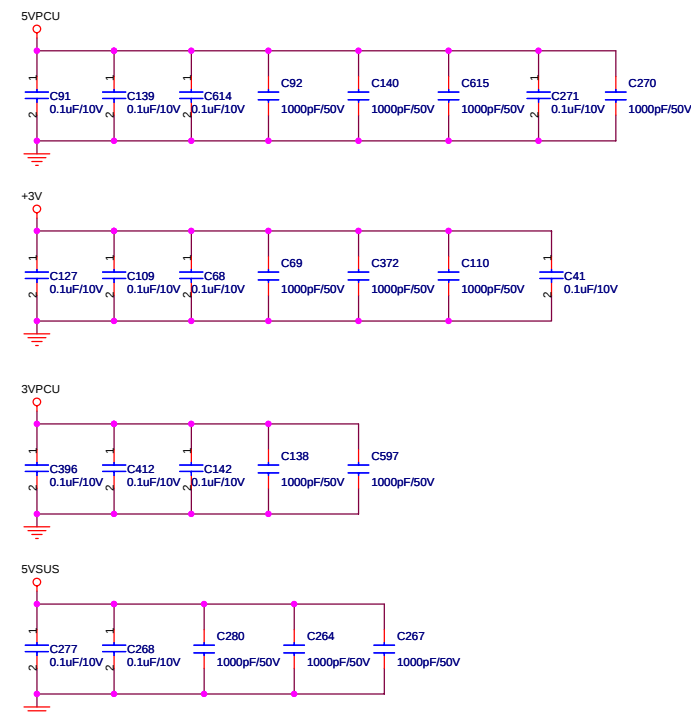


PROJECT : SW
Quanta Computer Inc.

Size	Document Number	Rev
	KB3926/ROM	1A
Date:	Friday, September 28, 2007	Sheet 33 of 44



EMI

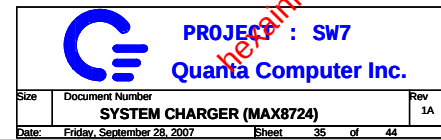


PROJECT : SW7
Quanta Computer Inc.

Size	Document Number	Rev
	Screw Holes & EMI	1A

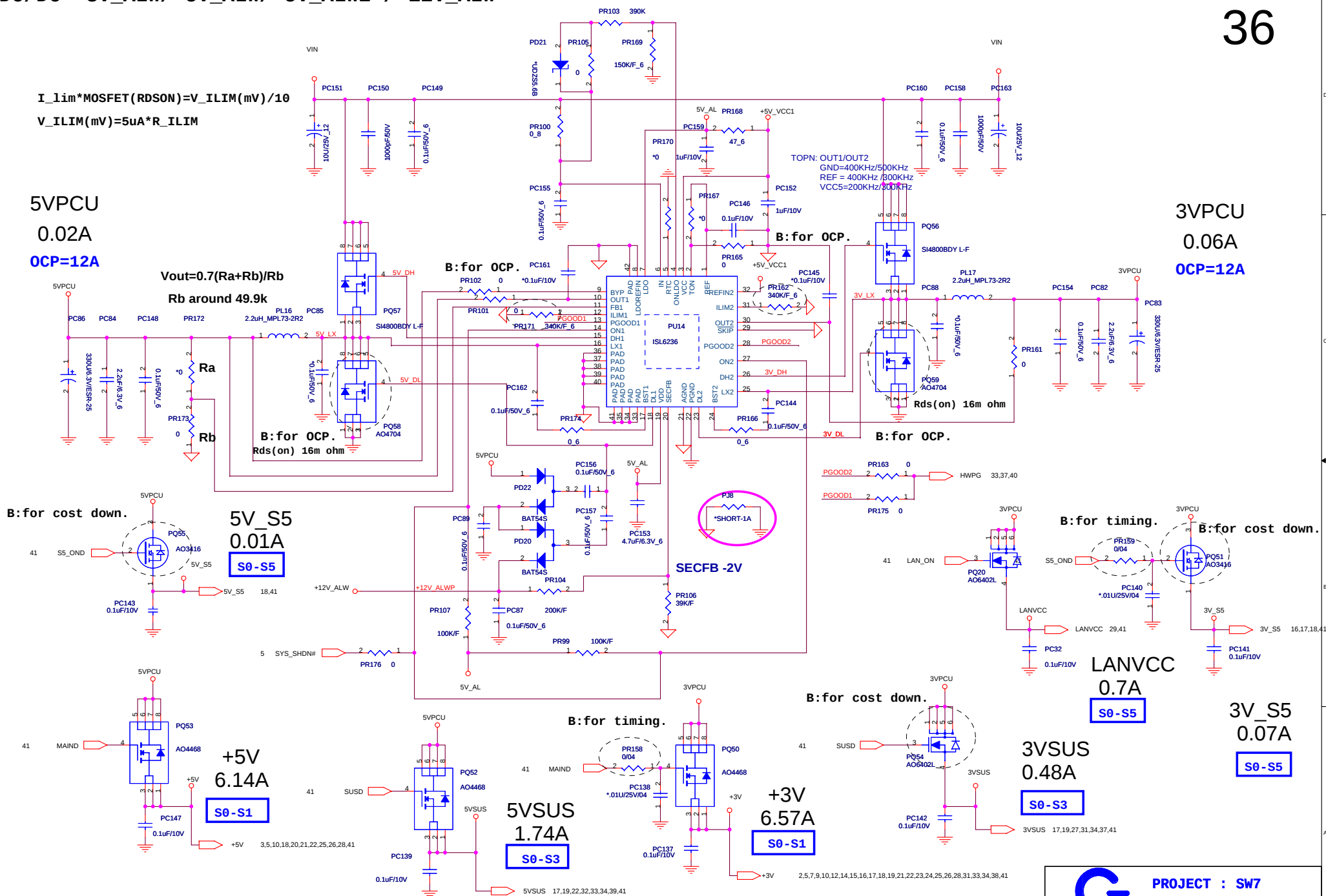
Date: Friday, September 28, 2007 Sheet 34 of 44

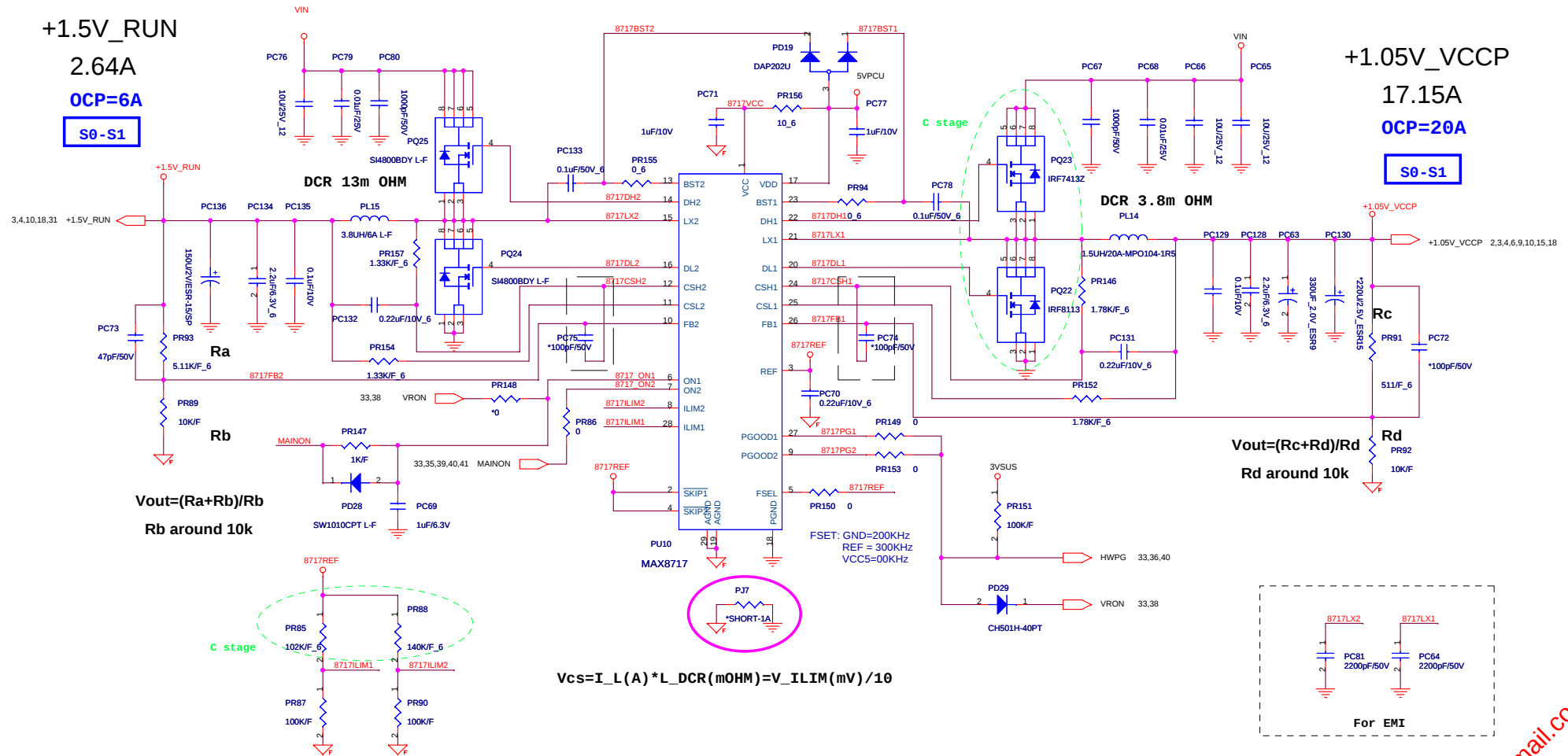
35



5VPCU
0.02A
0CP=12A

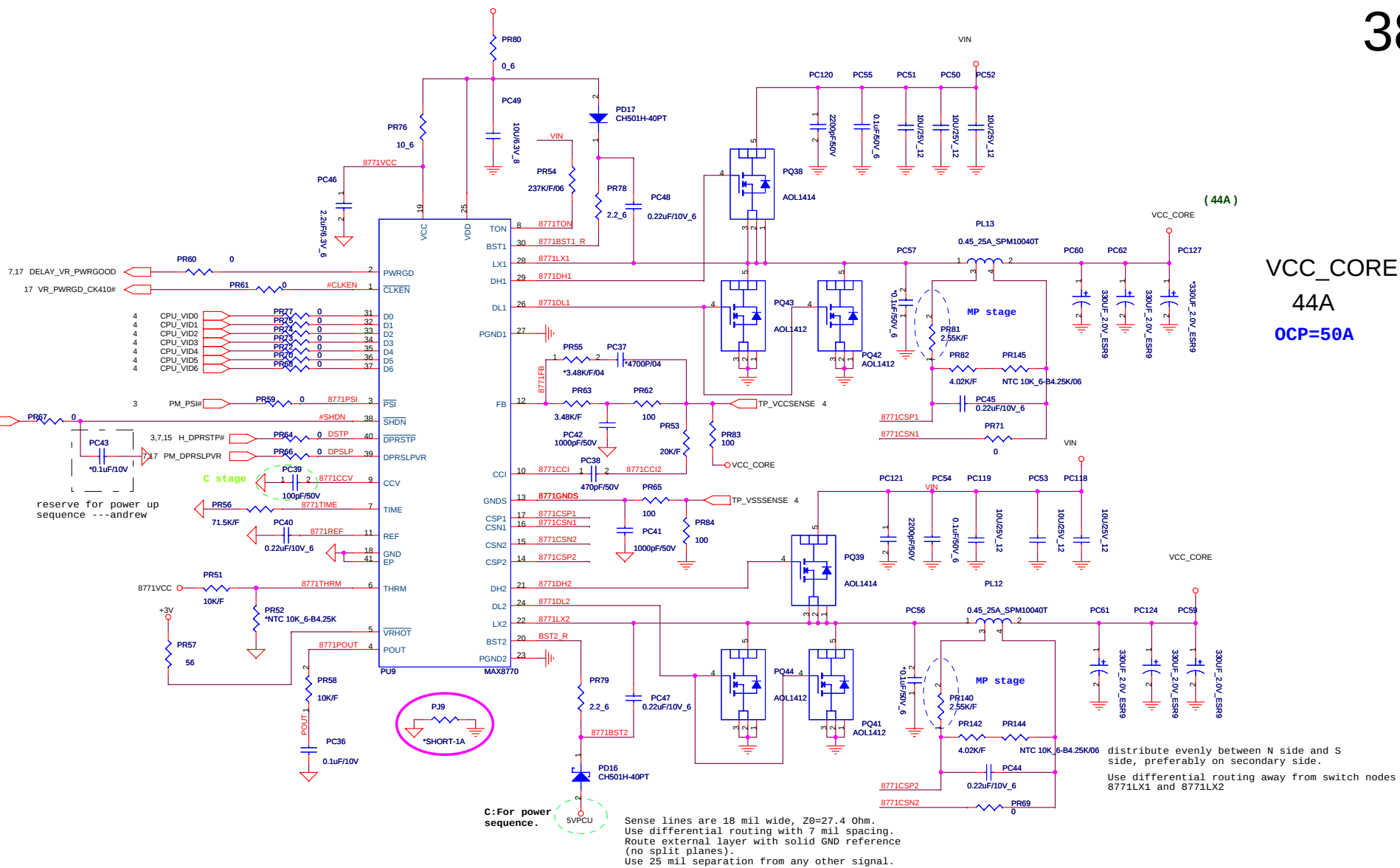
3VPCU
0.06A
OCP=12A



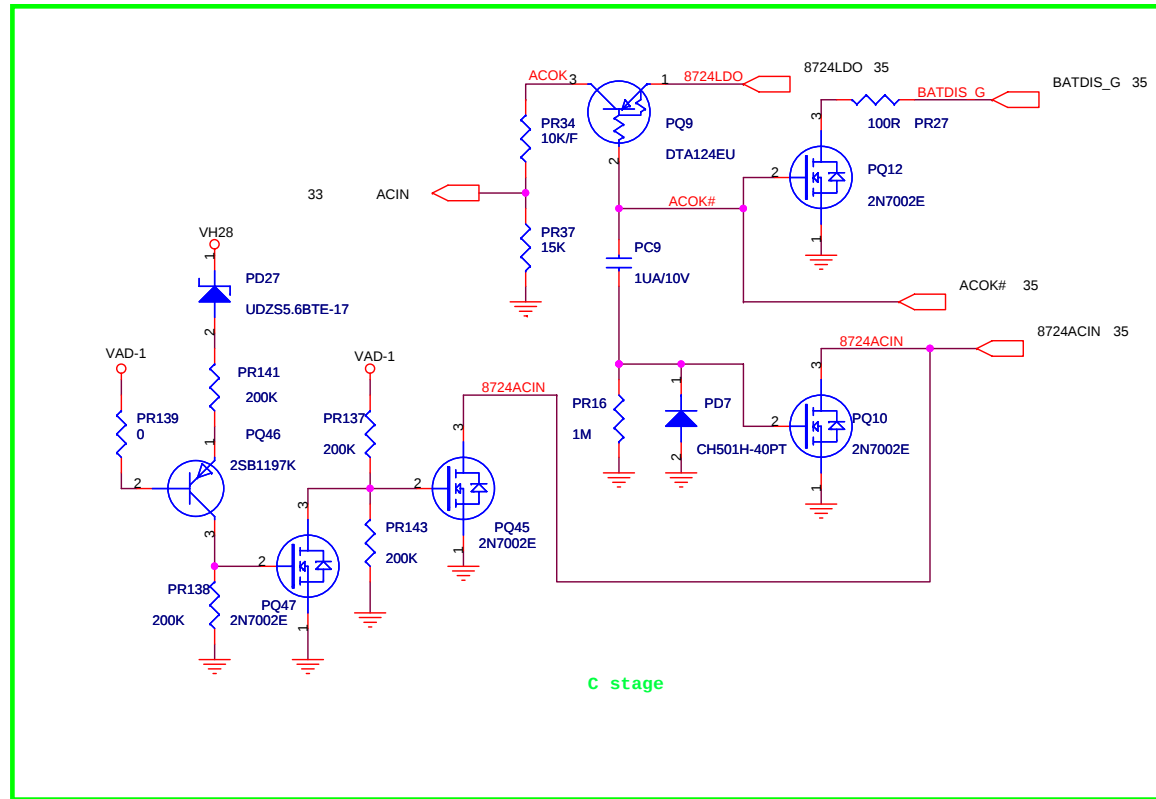


PROJECT SW7
Quantum Computer Inc.

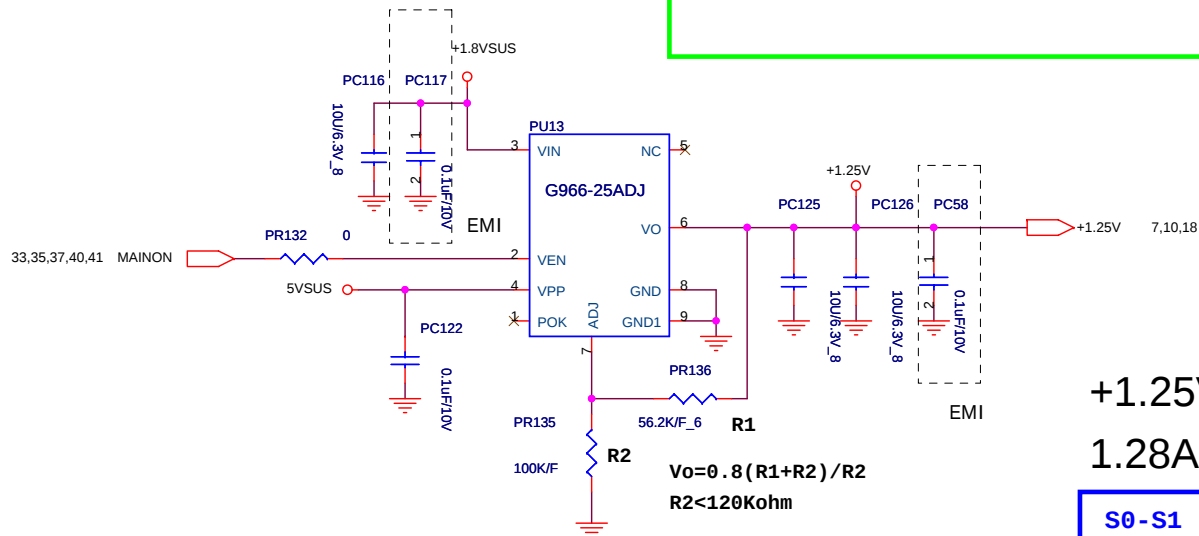
Size	Document Number	Rev
	+1.5V_RUN/+1.05V_VCCP (MAX8717)	1A
Date:	Friday, September 26, 2007	Sheet 37 of 44



Add layout note on pins 22 and 28 of MAX8771 controller. These nets have large voltage swings. Need to route them away from the sensitive areas that are trying to detect small changes in voltage, such as the voltage sense VccSense VssSense lines.



C stage



+1.25V
1.28A

S0-S1

$$V_o = 0.8 (R_1 + R_2) / R_2$$

$$R_2 < 120Kohm$$

PROJECT : SW7

Quanta Computer Inc.

Size	Document Number	Rev
	+1.25V&+2.5V	1A
Date:	Friday, September 28, 2007	Sheet 39 of 44

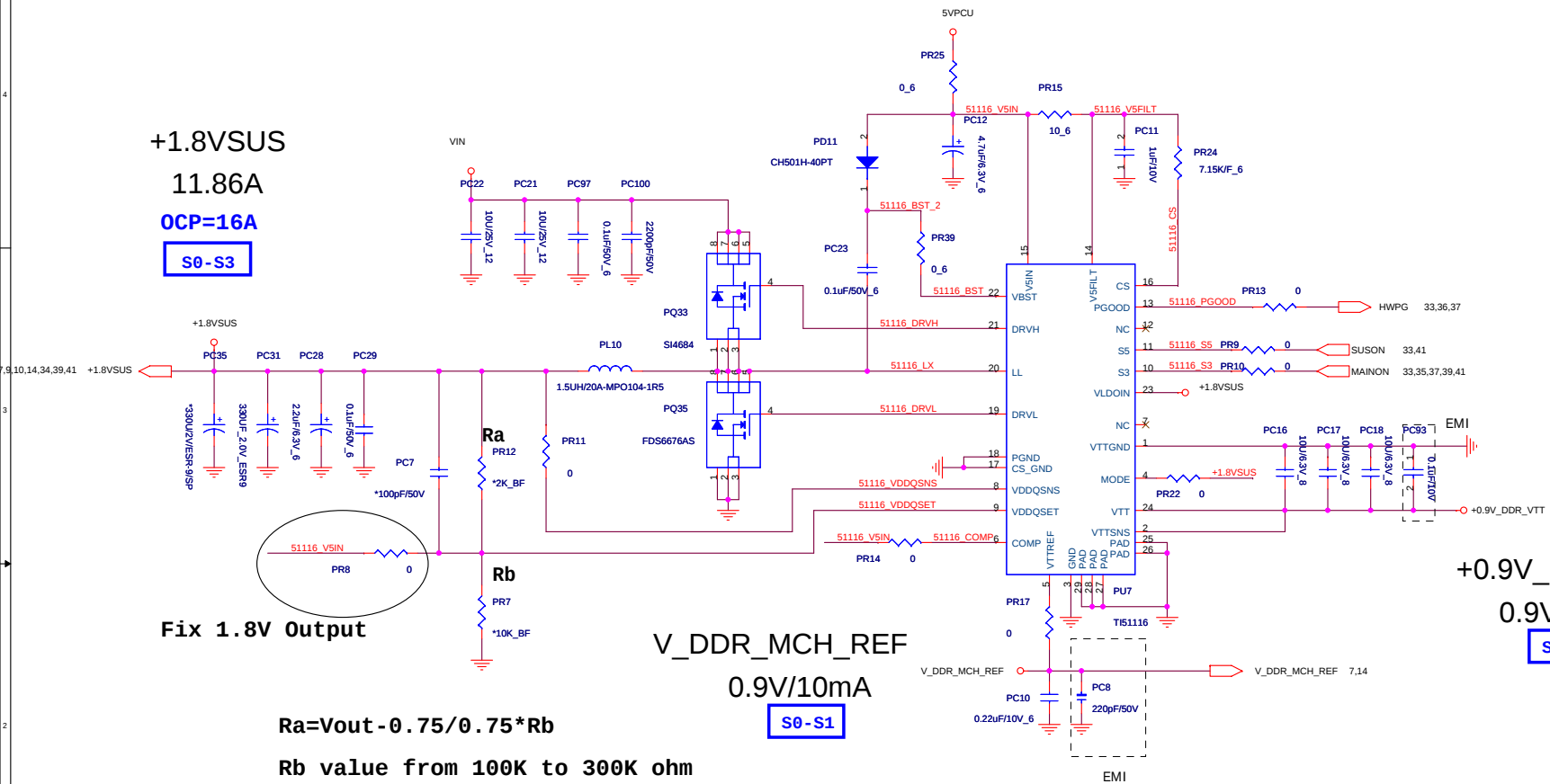
hexainf@hotmail.com

+1.8VSUS

11.86A

OCP=16A

S0-S3



Fix 1.8V Output

V_DDR_MCH_REF

0.9V/10mA

S0-S1

$$R_a = V_{out} - 0.75 / 0.75 \cdot R_b$$

Rb value from 100K to 300K ohm

Mode	Discharge Mode
V5IN	No discharge
VDDQ	Tracking discharge
Gnd	Non-tracking discharge

$$V_{TRIP}(mV) = R_{TRIP}(Kohm) \cdot 10(uA)$$

$$I_{OCP} = V_{trip} / R_{ds_on} + I_{Ripple} / 2$$

VDDQSET	VDDQ(V)	VTTREF and Vtt	Note
GND	2.5	V_vddqsns/2	DDR
V5IN	1.8	V_vddqsns/2	DDR2
FB	adjustable	V_VDDQSNS/2	1.5V < VDDQ < 3V

+0.9V_DDR_VTT

0.9V/10mA

S0-S1



PROJECT : SW7
Quanta Computer Inc.

Size	Document Number	Rev
	DDR2 +1.8VSUS/+0.9V_DDR_VTT	1A
Date	Friday, September 28, 2007	Sheet 40 of 44

