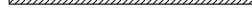


Model Name: GA-8VM800M-775

Revision :1.0

SHEET	TITLE
1	BOM & PCB MODIFY HISTORY
2	COVER SHEET
3	BLOCK DIAGRAM
4,5,6,7	INTEL P4_LGA775 CPU
8,9,10,11	P4M800 (NORTH BRIDGE)
12	CLOCK GENERATOR (RTM 862520)
13,14,15	VT8237R/CD (SOUTH BIRDGE)
16,17	DDR SDRAM DIMMS 1,2 DDR TERMINATION
18	AGP SLOT
19	PCI SLOT 1,2,3
20	BIOS , VGA Connect
21	IDE,USB
22	LPC I/O_W83627EHF
23	COM,PRT,FDD,KB/MS, IR
24	AC 97 CODEC
25	AUDIO JACK,GAME PORT
26	PANEL,STR LED,FANS
27	LAN 8100C & USB CONNECTOR
28	DDR POWER
29	ATX CONN,3VDUAL,VDDQ DC POWER
30	VCORE PHASE PWM FAIRCHILD ISL6556B

		COMPONENT SIDE (1 oz. Copper)
		GND SIDE (1 oz. Copper)
		VCC SIDE (1 oz. Copper)
		SOLDER SIDE (1 oz. Copper)

GIGABYTE		
Title COVER SHEET		
Size Custom	Document Number GA-8VM800M-775	Rev 1.0
Date: Tuesday, August 16, 2005	Sheet 1 of 30	1

Model Name: GA-8VM800M-775

Version:1.0

Component value change history

2005/06/29

[illegible]

Circuit or PCB layout change for next version

[illegible]

GA-8VM800M-775 BLOCK DIAGRAM

CLOCK GEN

VCC25 = 2.5V(I/O, MEMORY/I, VLINK/I)
VCC3 = 3.3V

PAGE 12

INTEL 775 SOCKET

VCORE = 1.75V (650-1100MHZ) / SLEEP : 1.3V
VCCA = 2.5V ; 2.5V = 2.5V

PAGE 4, 5, 6, 7

VID0~4

PWM/OTHER POWER

VCORE = 1.75V (650-1100MHZ) / SLEEP : 1.3V
5VSB, -12V, +12V, VCC, VCC3, 3VDUAL
DDRVT, DDR25V, 3VSTR, VCC25

PAGE 28, 29, 30

AGP SLOT 4X/8X

VDDQ = 1.5V (AGP POWER 4X)
VCC3 = 3.3V
+12V = 12V
3VDUAL = 3.3V
VCC = 5V

PAGE 18

VIA P4M800 NORTH BRIDGE

VCORE = 1.75V (650-1100MHZ) / SLEEP : 1.3V
DDR25V = 2.5V(SUSPEND POWER)
VDDQ = 1.5V (AGP POWER 4X)
VCC25 = 2.5V(I/O, MEMORY/I, VLINK/I)

PAGE 8, 9, 10, 11

MAA0~15
MDD0~63
-DQSD0~7

DDR SDRAM DIMM X 2

DDR25V = 2.5V(SUSPEND POWER)
DDRVT = 1.25V

PAGE 16, 17

DQM0~7

USB PORTS 0~5

VCC = 5V
5VSB = 5V
5VUSB = 5V

PAGE 21

VLAD0~7
CONTROL BUS

V LINK

VIA VT8237R SOUTH BRIDGE

VCC25 = 2.5V(I/O, MEMORY/I, VLINK/I)
3VDUAL = 3.3V(SUSPEND POWER)
VCC3 = 3.3V
RTCVDD = 3.3V

PAGE 13, 14, 15

USB CON

PAGE 21

IDE Primary and Secondary

VCC = 5V

PAGE 21

AC97 CODEC ALC 655 "D"

+12V = 12V
VCC3 = 3.3V
VCC = 5V
AVDD = 5V

PAGE 24

AUDIO PORTS :

LIN_OUT LINE_IN MIC FRONT AUDIO
CD_IN AUX_IN GAME PORT

PAGE 25

PCI BUS

PCI SLOT 1, 2, 3

+12 = 12V
-12 = -12V
VCC = 5V
VCC3 = 3V
3VDUAL = 3V

PAGE 19

LAN 8100C

VDDTXRX = 3.3V
VDDC = 3.3V

PAGE 27

PCI BUS

FRONT PANEL /FANS

VCC = 5V 5VSB = 5V
+12 = 12V PVCC = 5V

PAGE 26

LPC BUS

BIOS & VGA

VCC = 5V
VCC3 = 3V

PAGE 20

LPC I/O W83627EHF

VCC = 5V 5VSB = 5V VBAT = 3V

IR

PAGE 22

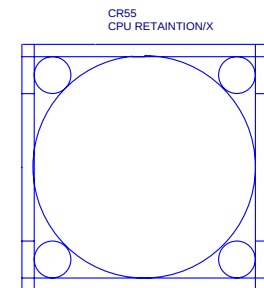
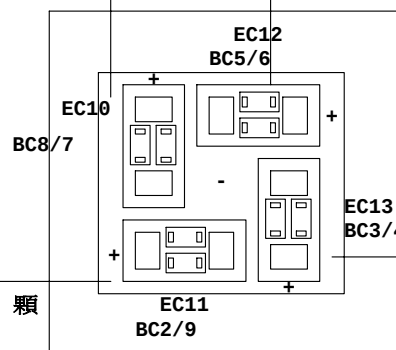
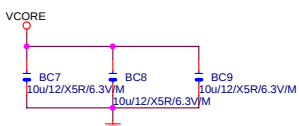
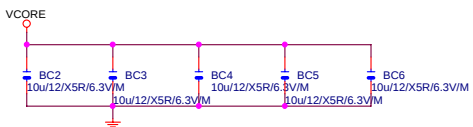
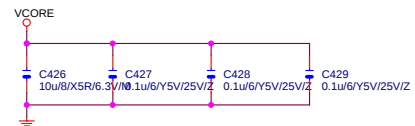
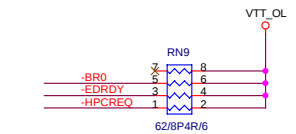
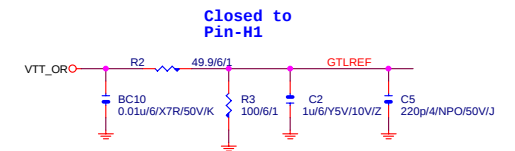
I/O PORTS :

COMA COMB LPT PS2 FDD

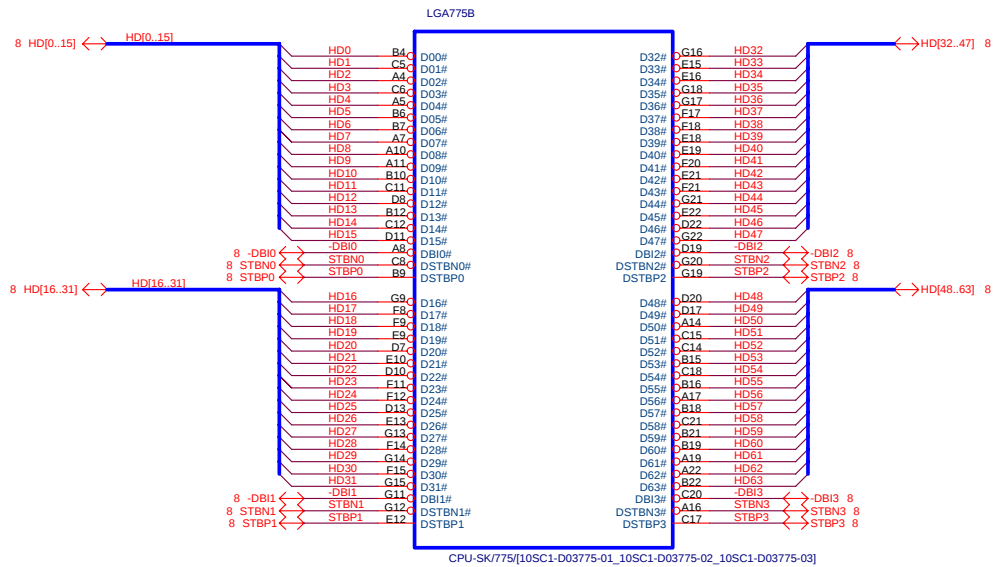
PAGE 23

GIGABYTE

BLOCK DIAGRAM			Rev
Size	Document Number	GA-8VM800M-775	1.0
Custom			
Date:	Tuesday, August 16, 2005	Sheet 3 of 30	



GIGABYTE			
Title			
P4_LGA775-A			
Size Custom	Document Number	GA-8VM800M-775	Rev 1.0
Date:	Tuesday, August 16, 2005	Sheet	4 of 30



Note:
VCCA & VCOREPLL
define doesn't same as
old P4 design kit

As close as possible to
CPU socket

Trace width doesn't
less than 12 Mil

Place outside of CPU socket

Locate at ICH6 Side

CPU

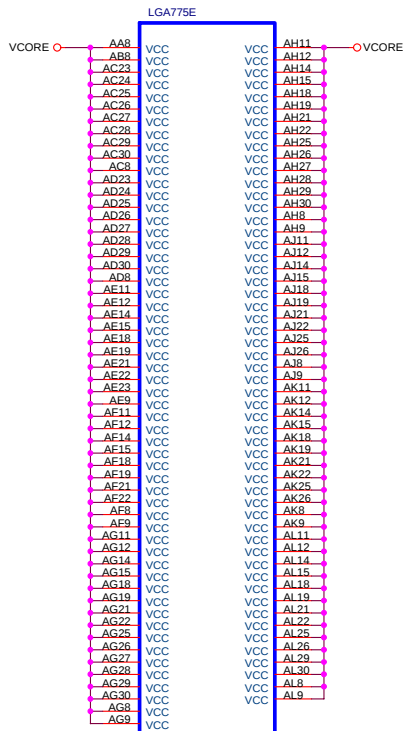
NA	FSB	FSA	
FSBSEL3	FSBSEL1	FSBSEL0	Clock
1	0	1	100MHZ
0	0	1	133MHZ
0	1	1	166MHZ
0	1	0	200MHZ
0	0	0	266MHZ

X

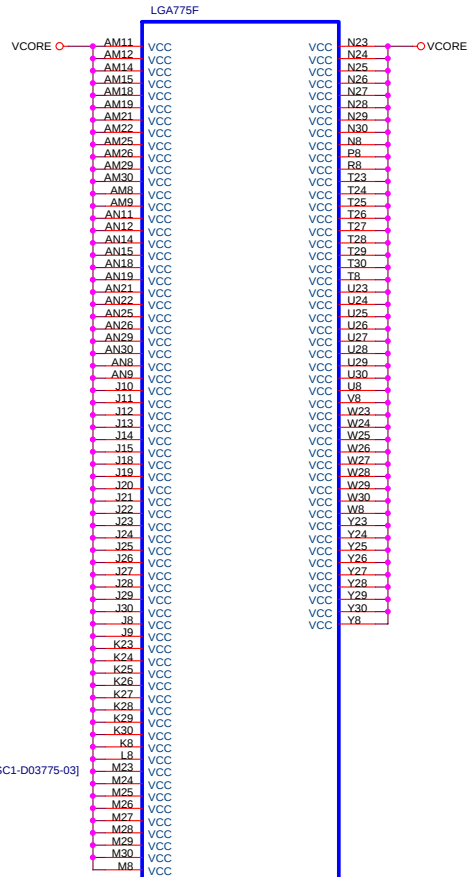
PROCESSOR HOT

asserted at 130 degree (RS2=720 ohm)
deasserted at 115 degree (RS2=1270 ohm)

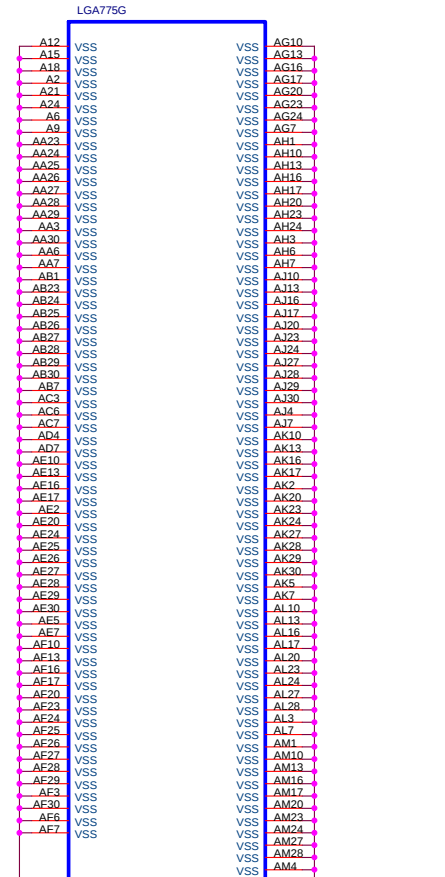
Plase at PH4 copper



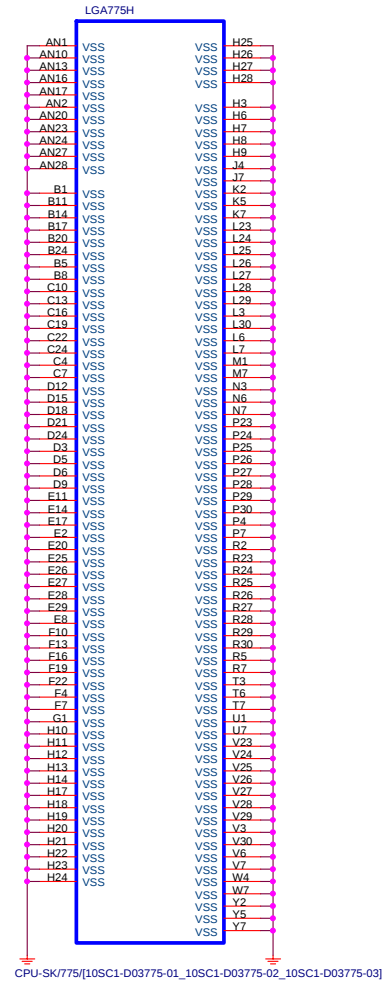
CPU-SK/775/[10SC1-D03775-01_10SC1-D03775-02_10SC1-D03775-03]



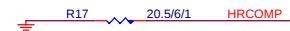
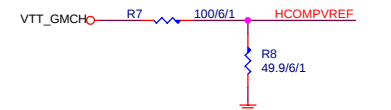
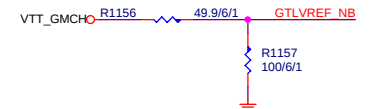
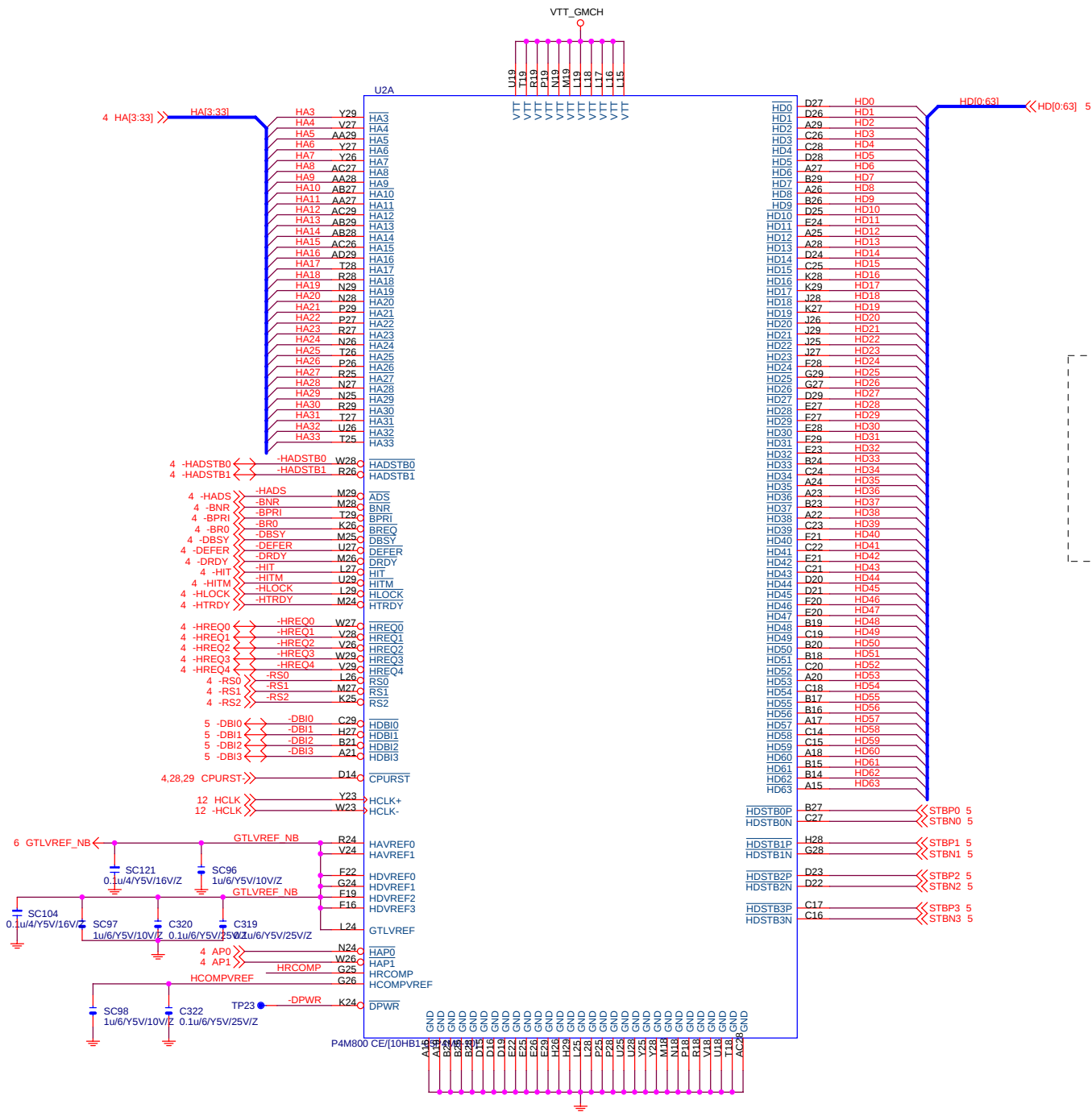
CPU-SK/775/[10SC1-D03775-01_10SC1-D03775-02_10SC1-D03775-03]



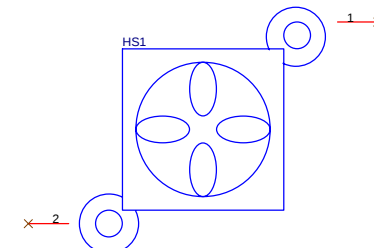
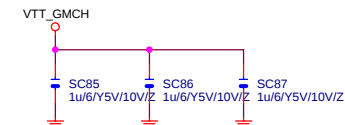
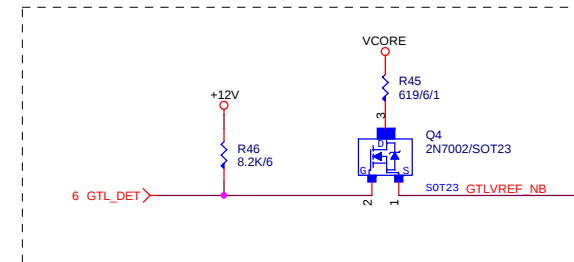
CPU-SK/775/[10SC1-D03775-01_10SC1-D03775-02_10SC1-D03775-03]



CPU-SK/775/[10SC1-D03775-01_10SC1-D03775-02_10SC1-D03775-03]



Please Close to P4M800

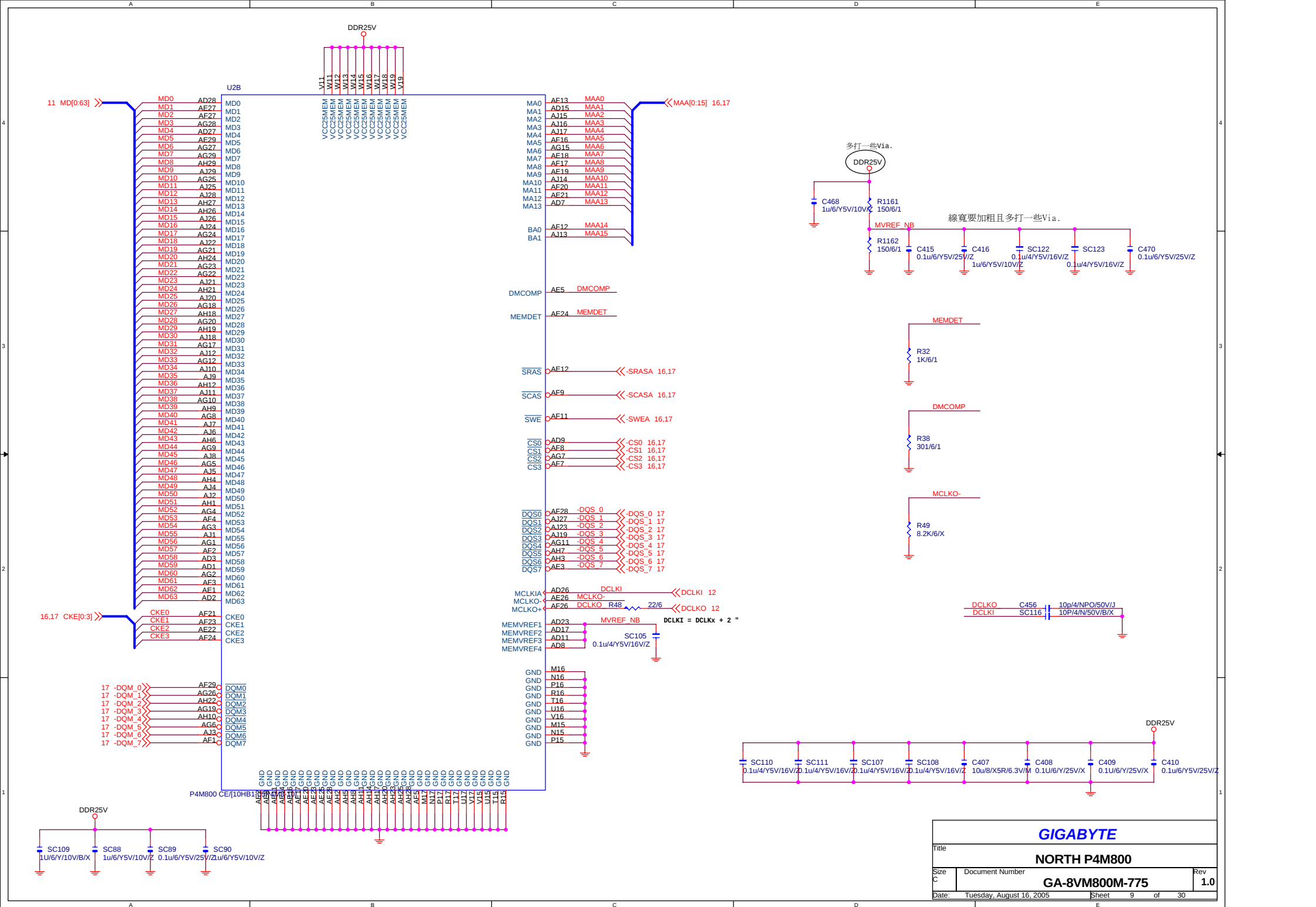


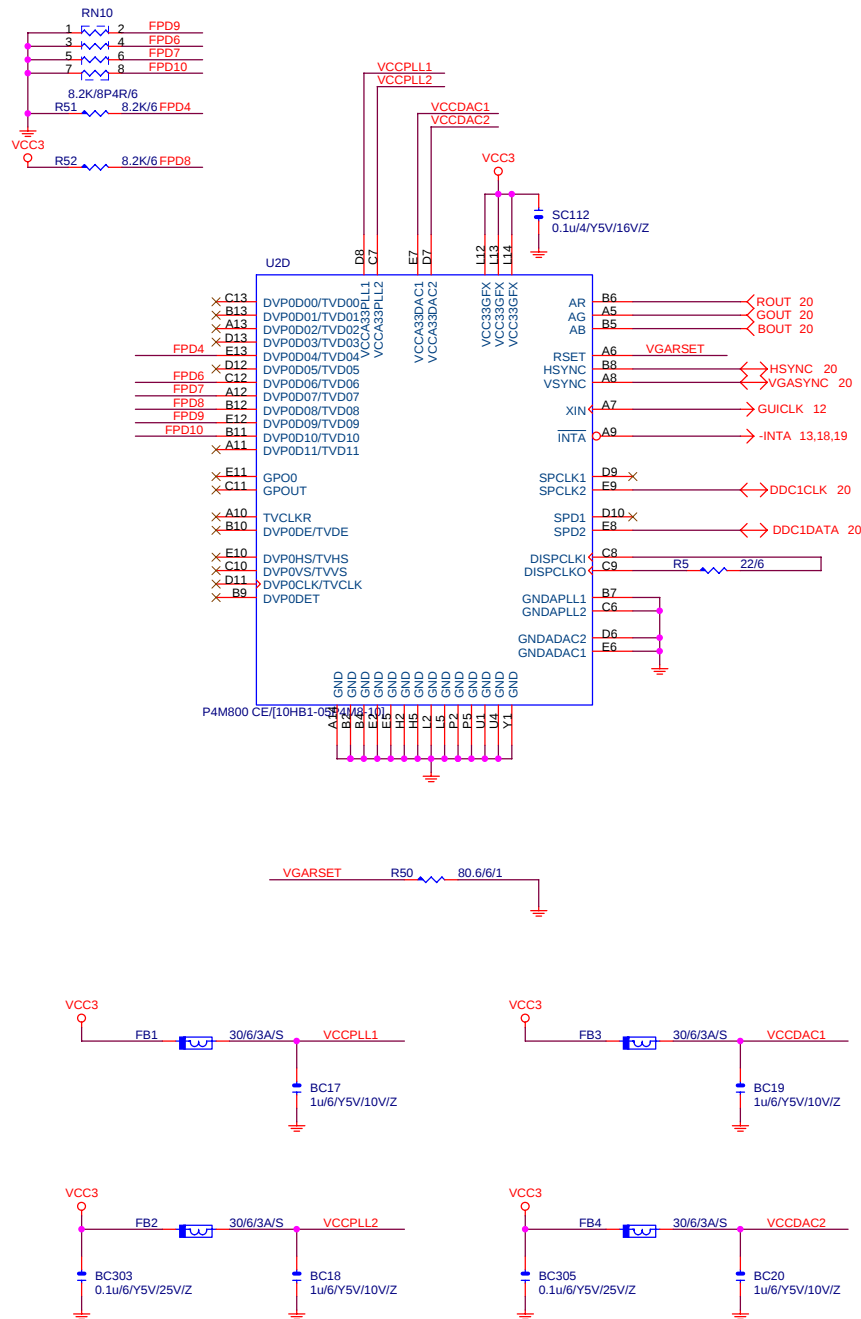
HEAT SINK/GIGABYTE/[12SP2-04E004-01_12SP2-04E004-02_12SP2-04E004-03_12SP2-04E004-04]

NB Heatsink

GIGABYTE

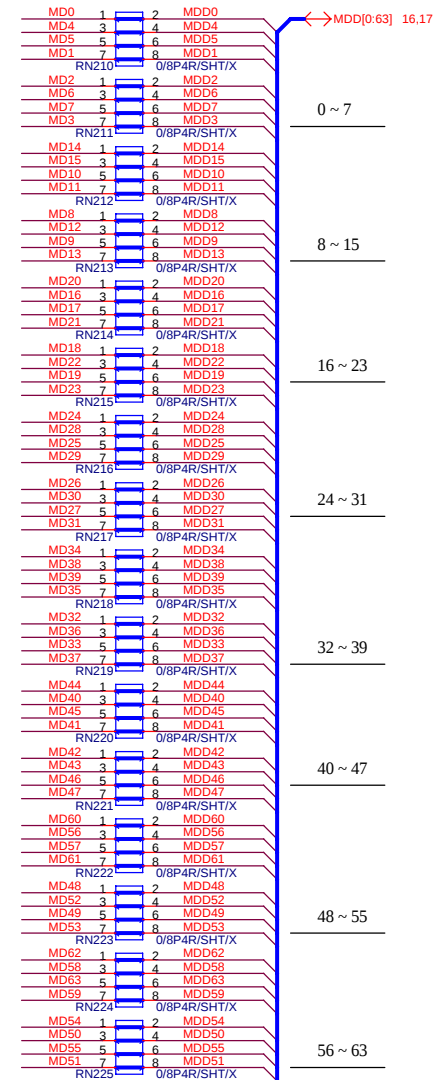
Title		
NORTH P4M800		
Size C	Document Number	Rev
	GA-8VM800M-775	1.0
Date: Tuesday, August 16, 2005		
Sheet 8 of 30		





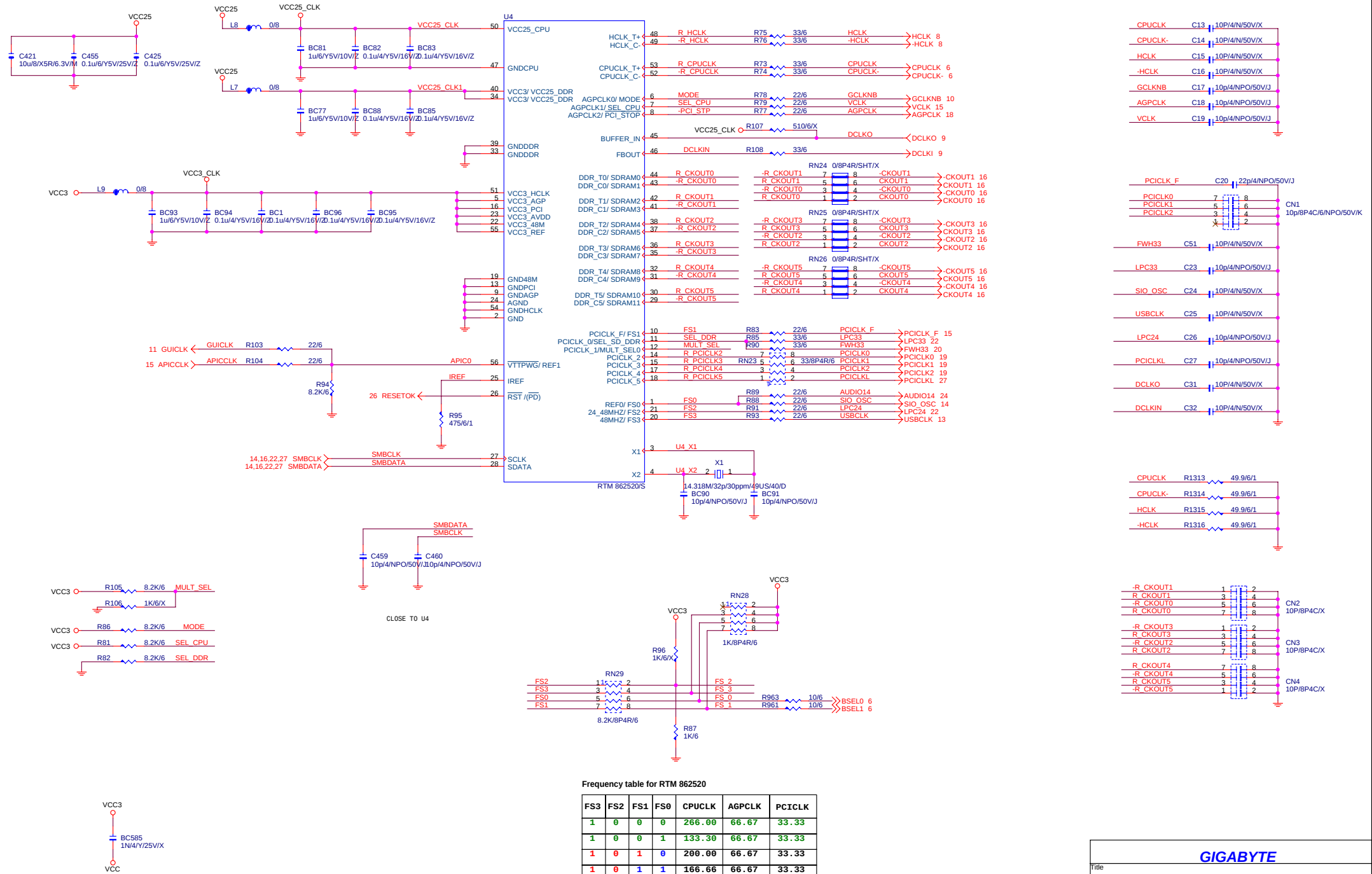
9 MD[0:63] >> MD[0:63]

DDR MD DAMPING Near DIMM 1

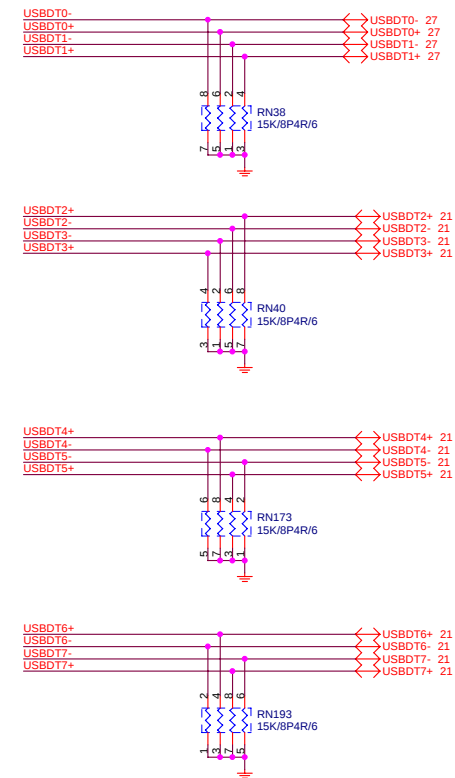
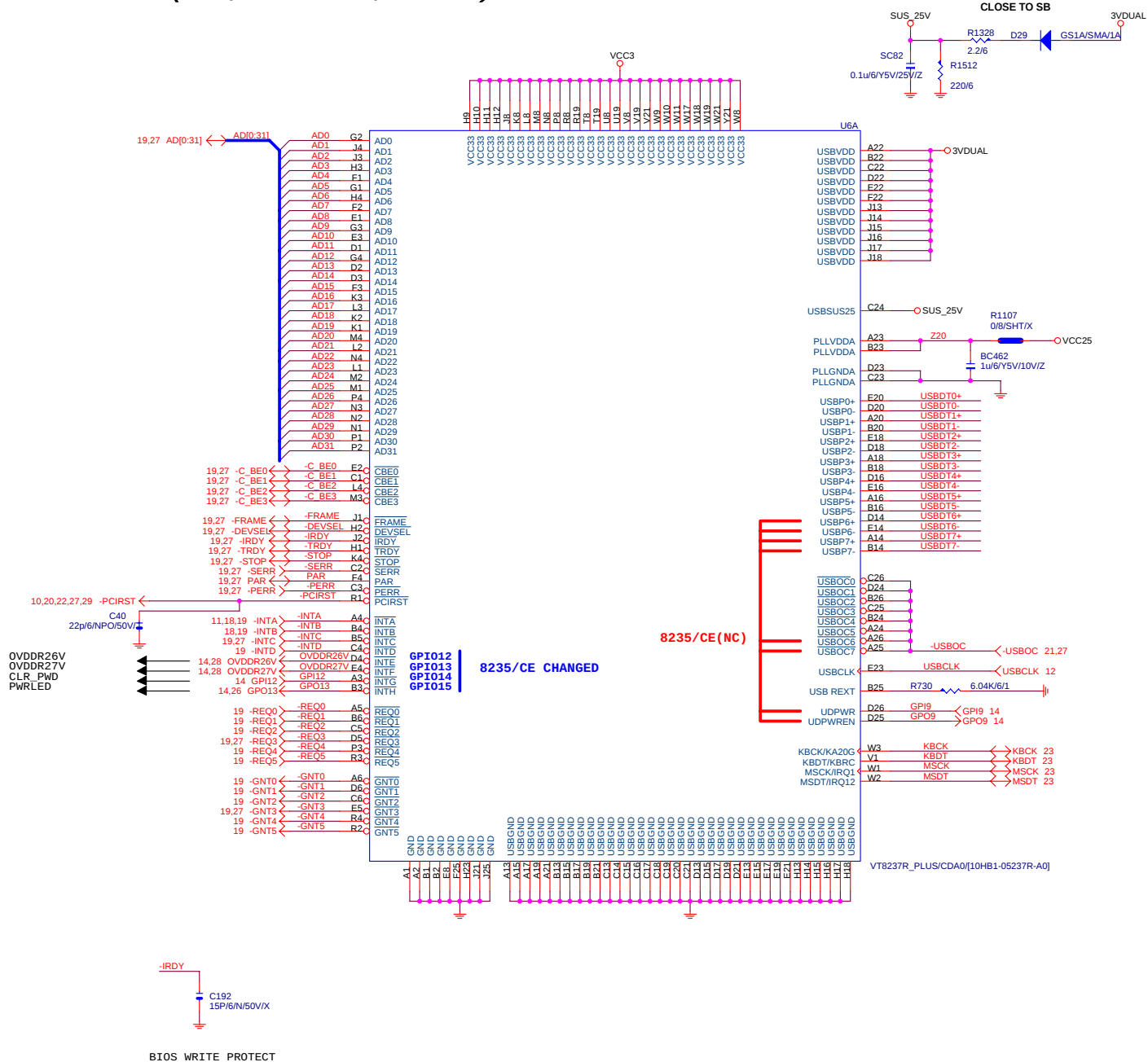


GIGABYTE			
Title			
NORTH P4M800			
Size	Document Number	Rev	
C	GA-8VM800M-775	1.0	
Date:	Tuesday, August 16, 2005	Sheet	11 of 30

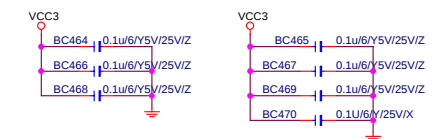
CLOCK GENERATOR



SB VT8237 (PCI, USB BUS, KB/MS)

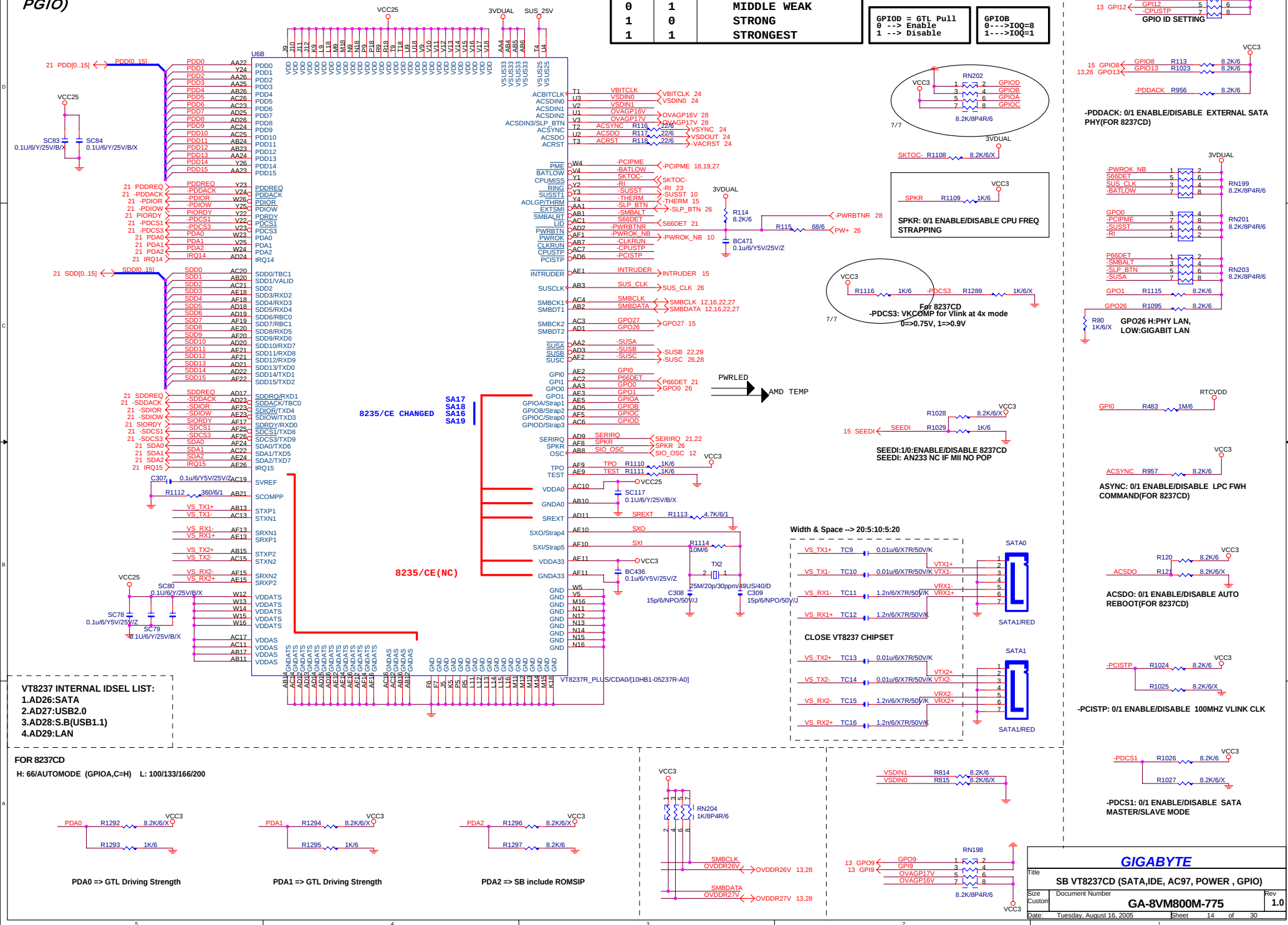


UDPWR/UDPWREN時, UDPWR必須PULL-DOWN

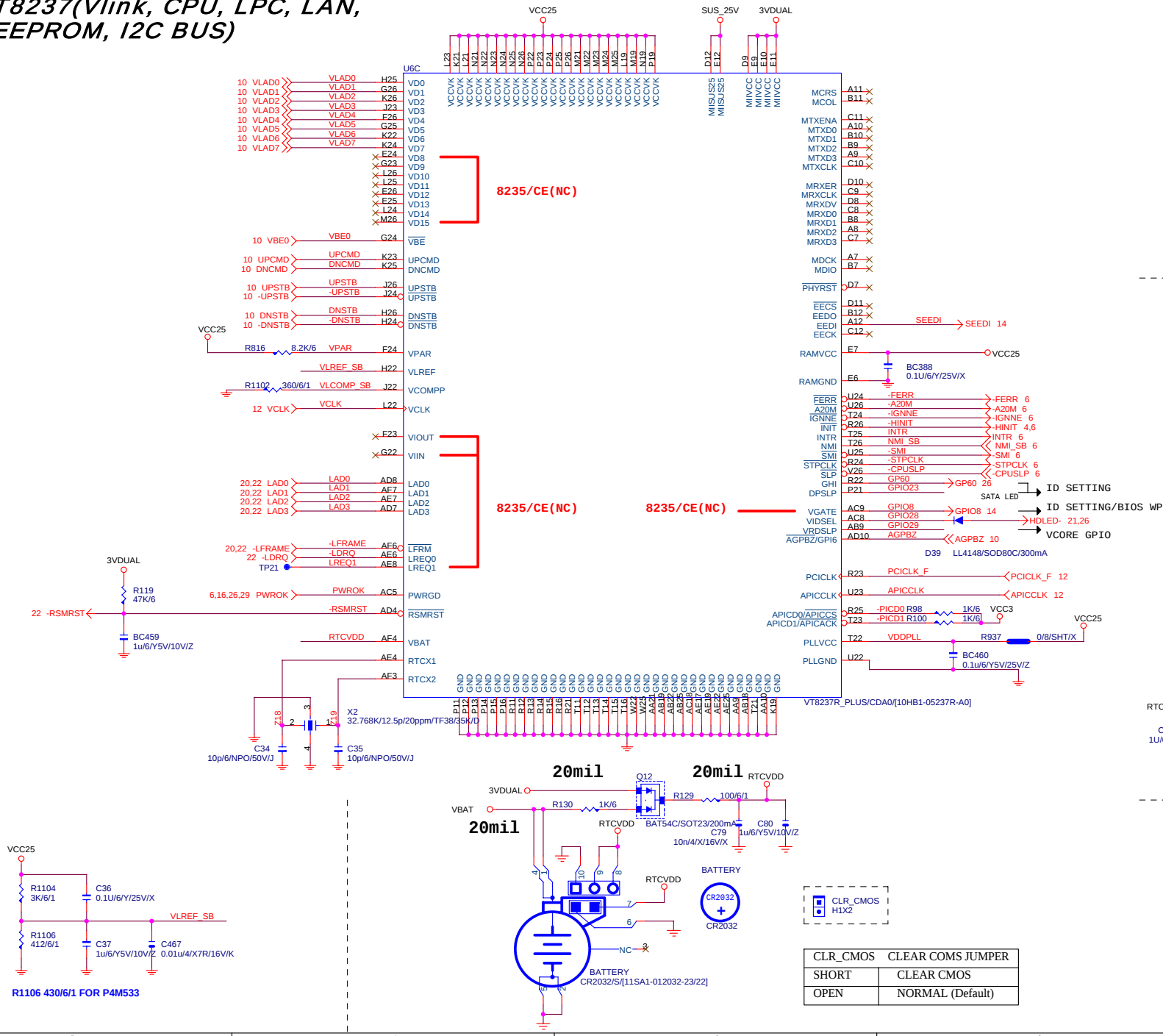


Decoupling capacitors

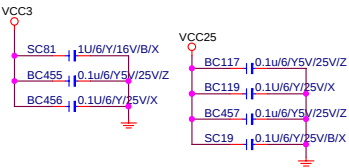
P/SDA1	P/SDA0	GTL Driving Strength
0	0	WEAK
0	1	MIDDLE WEAK
1	0	STRONG
1	1	STRONGEST



SB VT8237(Vlink, CPU, LPC, LAN,
LAN EEPROM, I2C BUS)



Decoupling capacitors

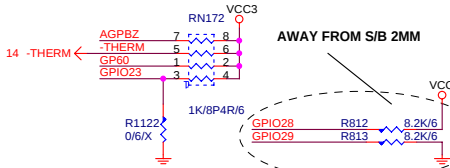
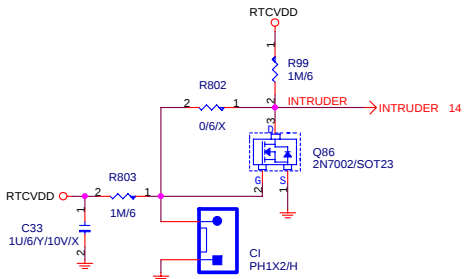


Internal MAC P.U

AN233 REMOVE Sep.8



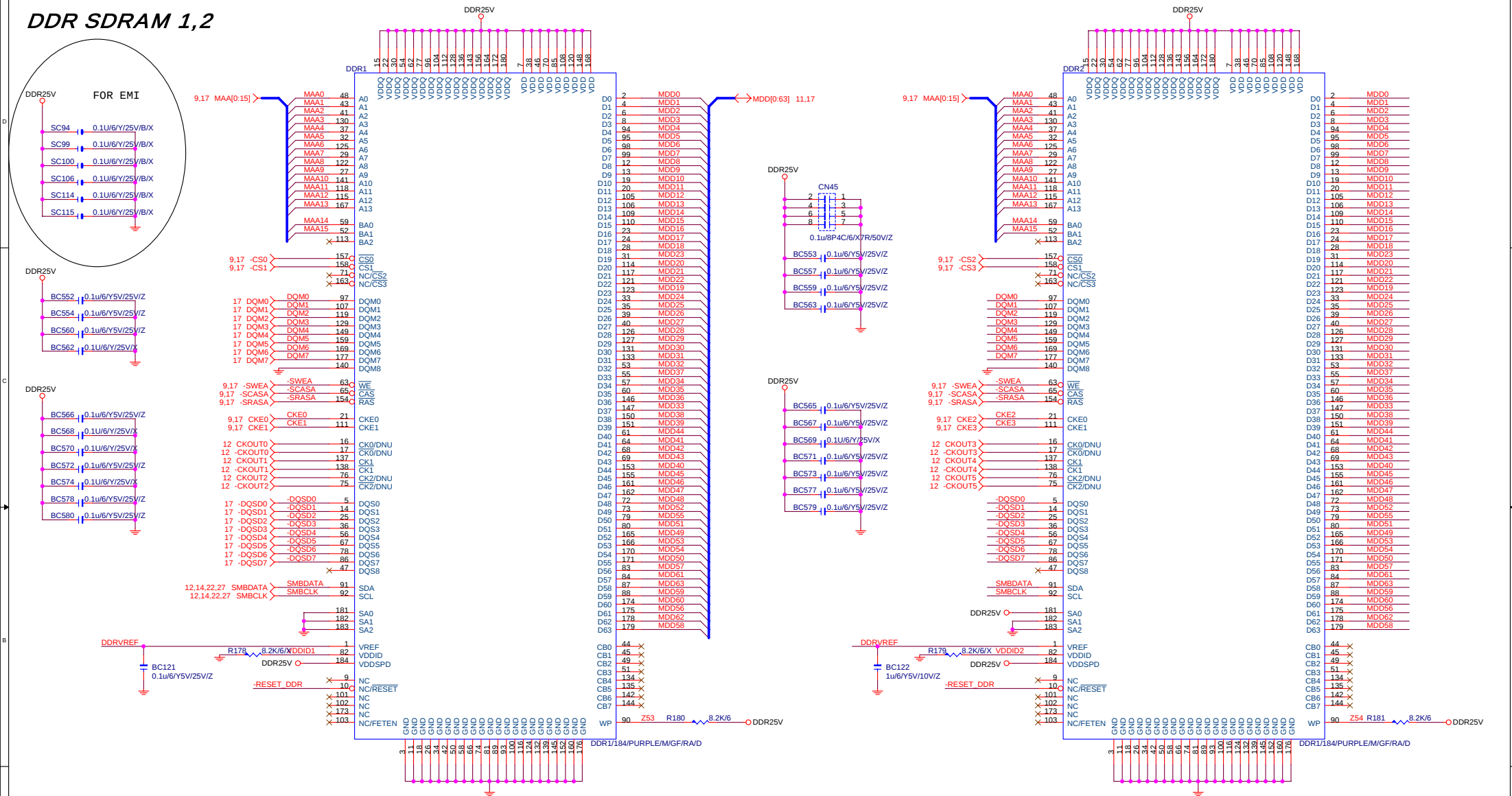
Case Open Circuits



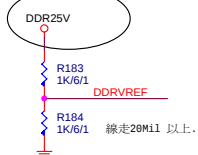
CLR_CMOS	CLEAR COMS JUMPER
SHORT	CLEAR CMOS
OPEN	NORMAL (Default)

GIGABYTE		
Title SB VT8237CD(Vlink, CPU, LPC, LAN, I2C)		
Size Custom	Document Number	Rev 1.0
Date: Tuesday, August 16, 2005 Sheet 15 of 30		

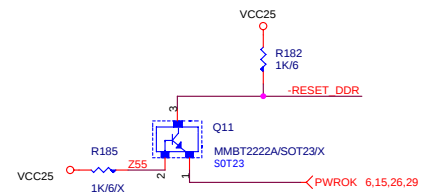
DDR SDRAM 1,2



補銅柏打VIA.



For Register DDR Support



GIGABYTE			
DDR UNBUFFERED 1,2			
Size Custom	Document Number	Rev	
	GA-8VM800M-775		1.0
Date:	Tuesday, August 16, 2005	Sheet	16 of 30



3

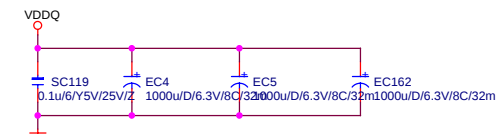
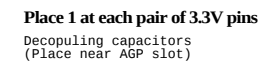
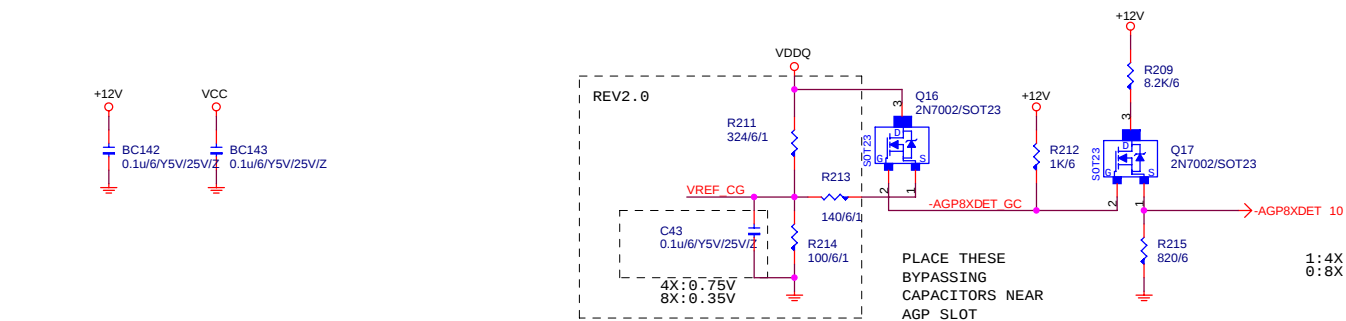


3



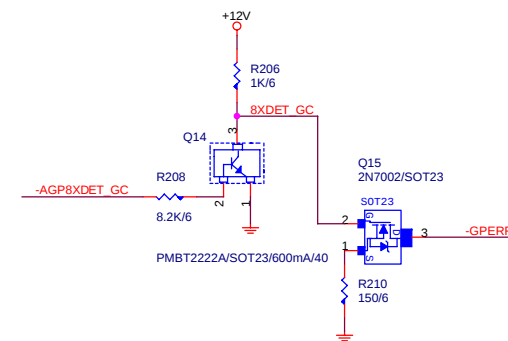
2

A

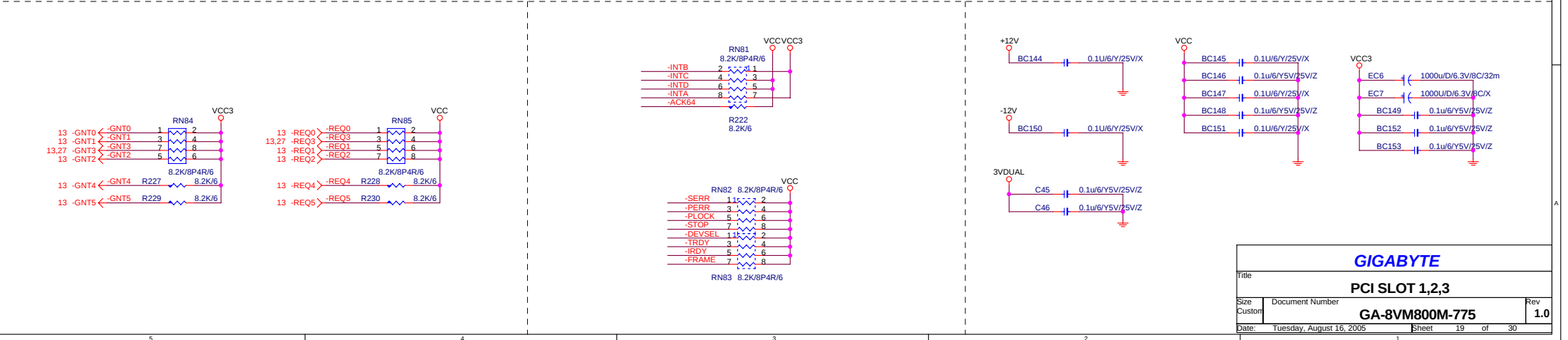
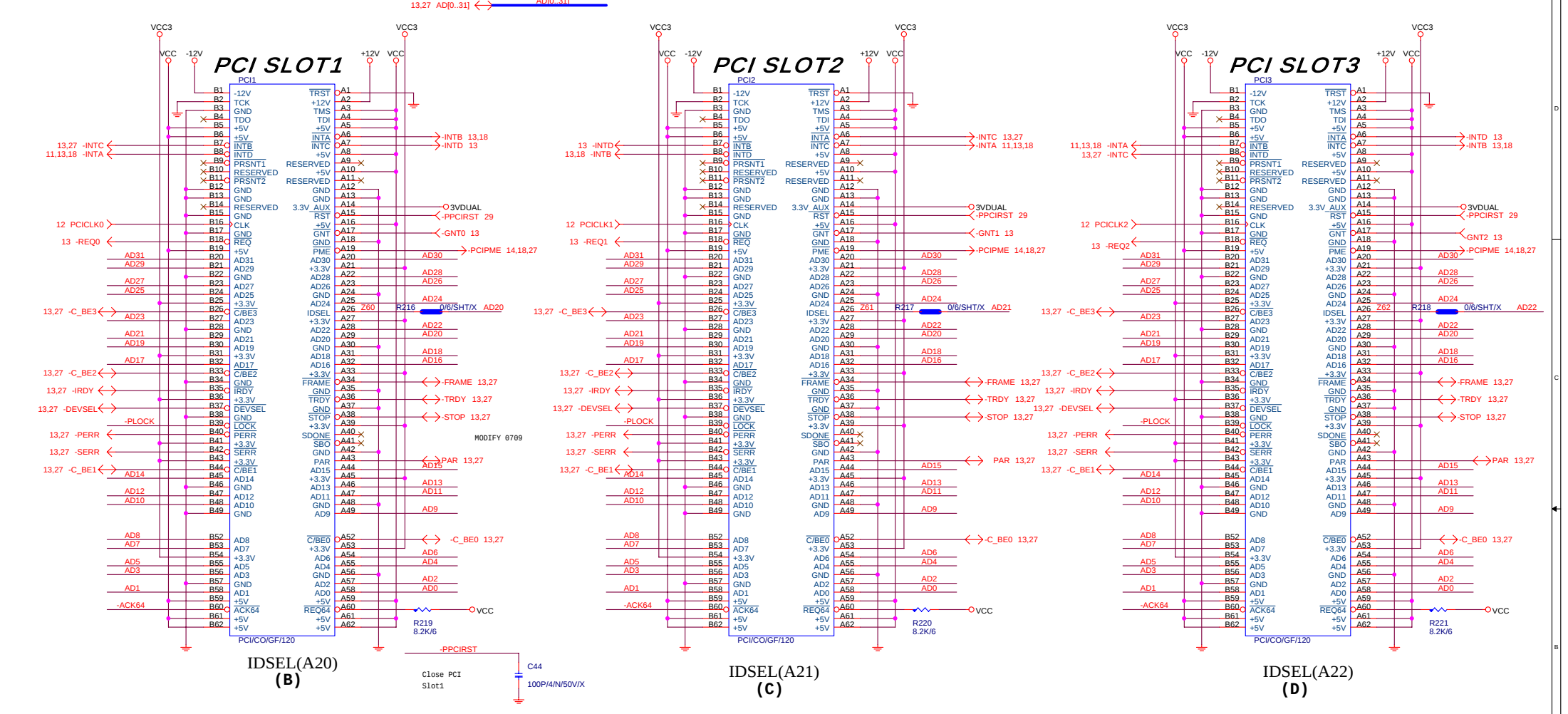


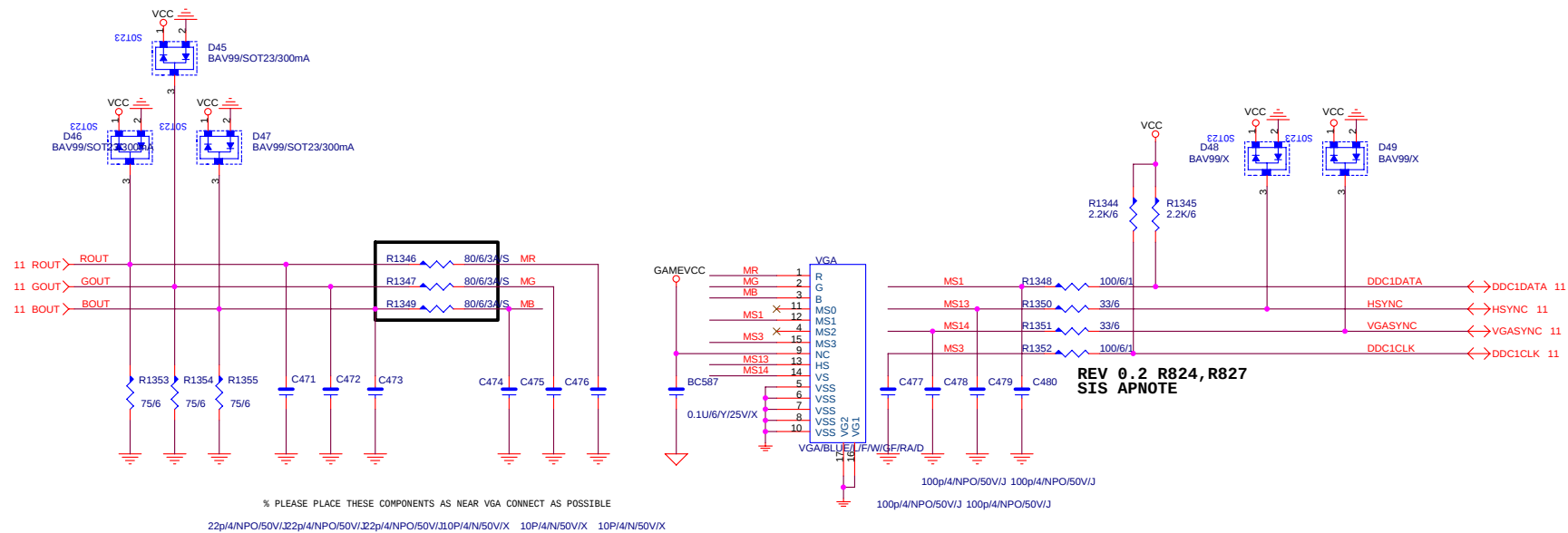
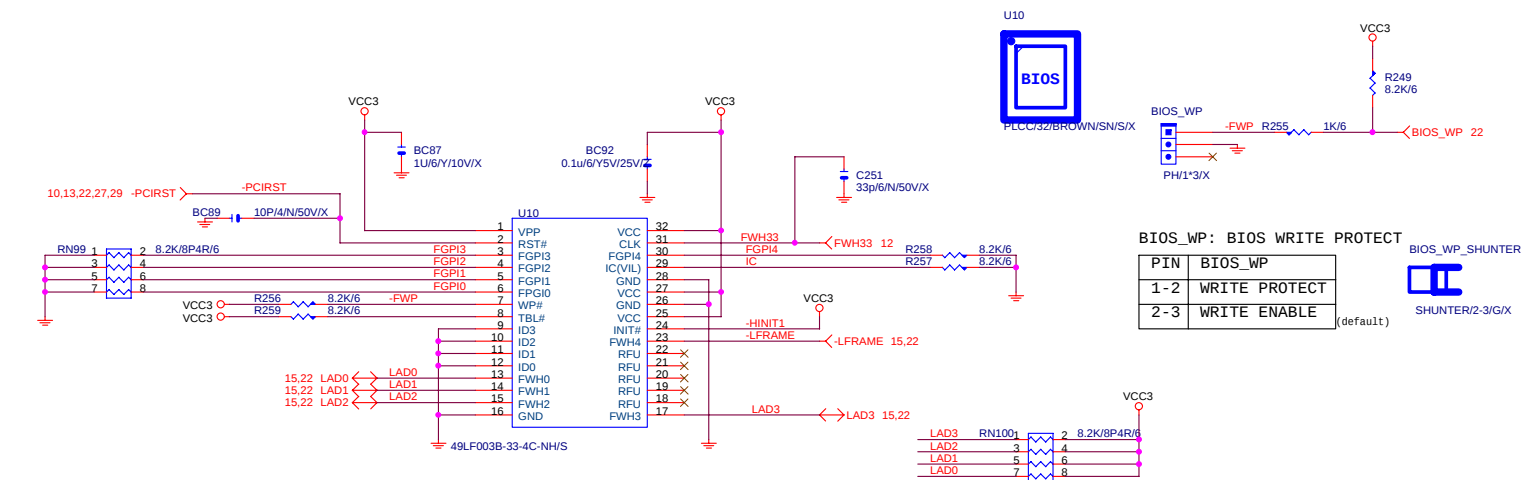
Place 1 at each pair of VDDQ pins

Place an additional for spread from A14 - A33

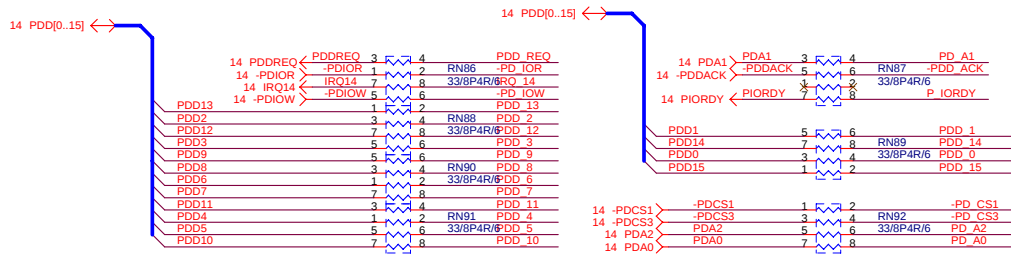


GIGABYTE				
Title				
AGP SLOT				
Size	Document Number			Rev
Custom	GA-8VM800M-775			1.
Date:	Tuesday, August 16, 2005	Sheet	18	of 30



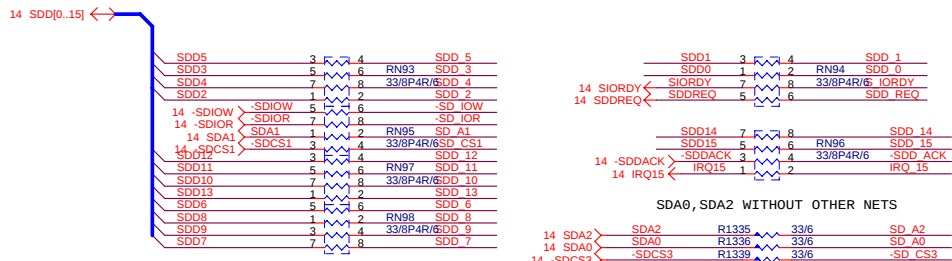


PRIMARY IDE

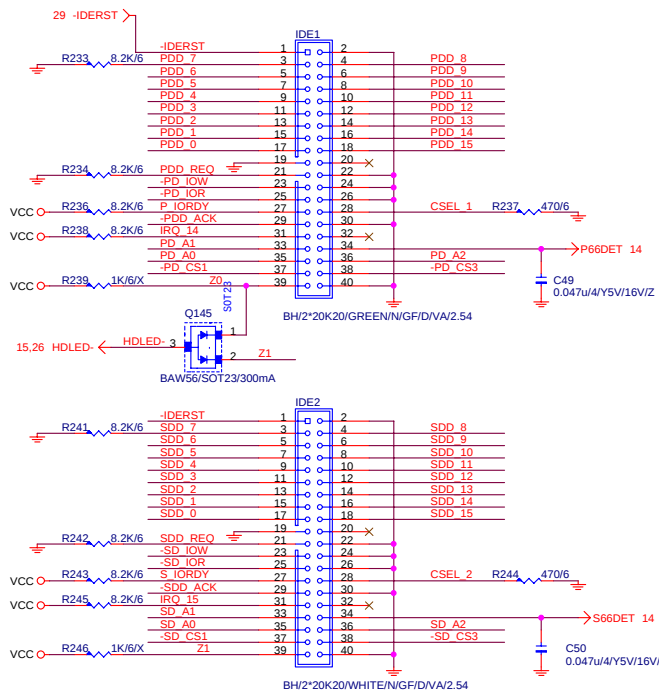


These resistor should placed near South Bridge

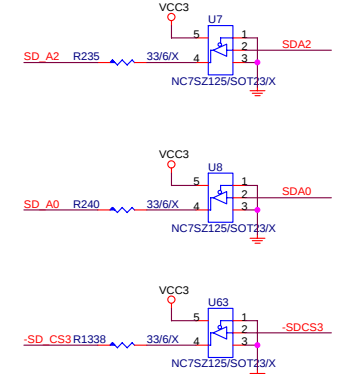
SECONDARY IDE



These resistor should placed near South Bridge



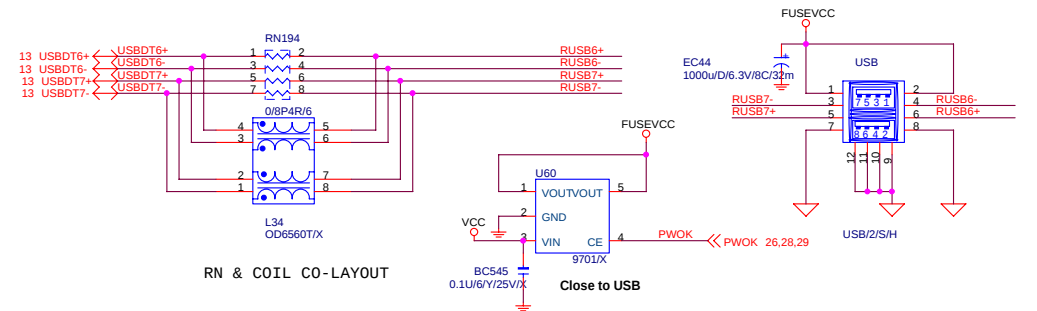
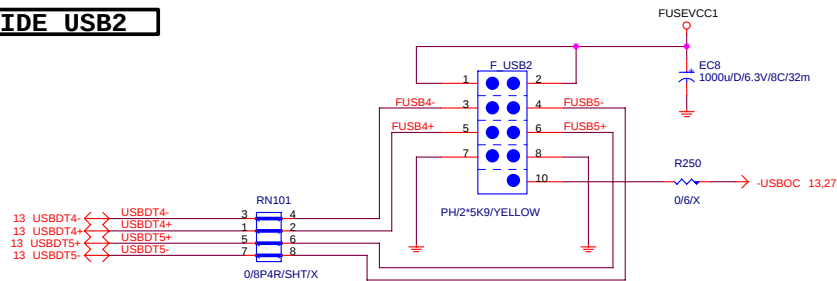
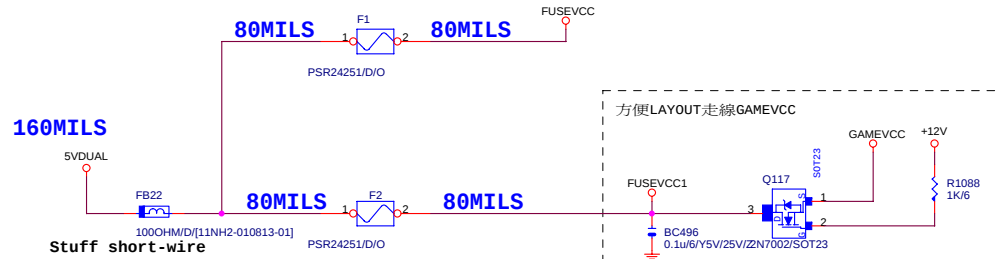
CD, DVD ROM STRAPPING ISSUE



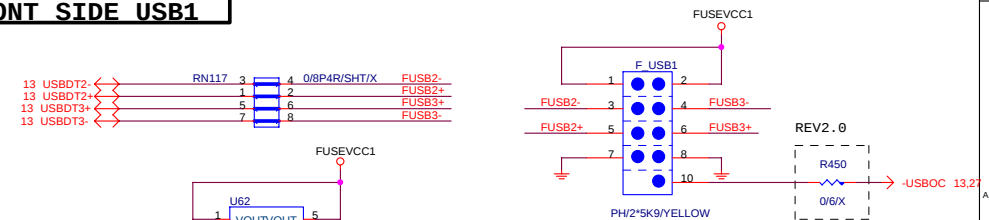
SIRQ



FRONT SIDE USB2

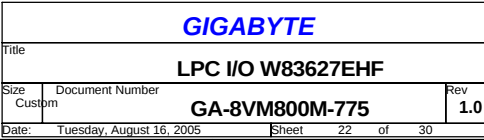
**FUSEVCC, GAMEVCC**

FRONT SIDE USB1

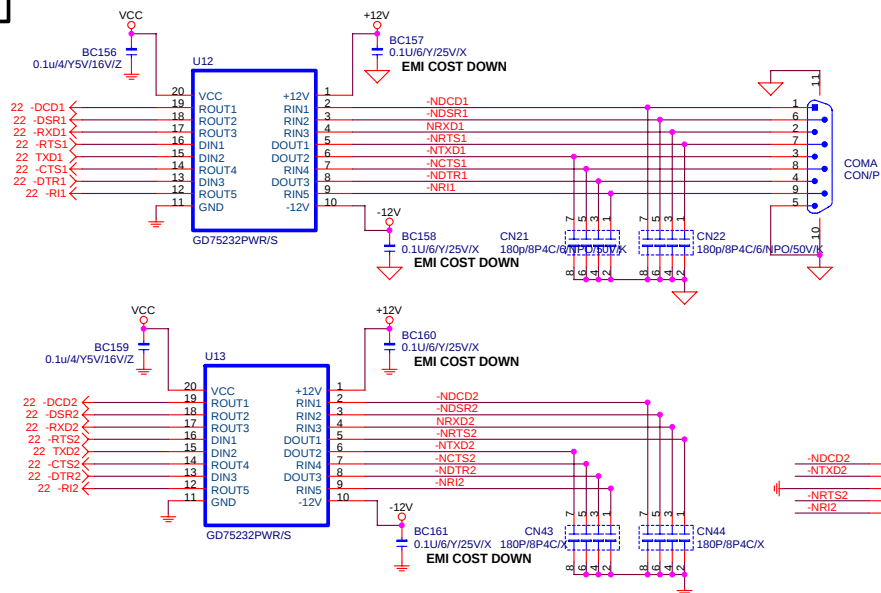
**GIGABYTE**

IDE, USB

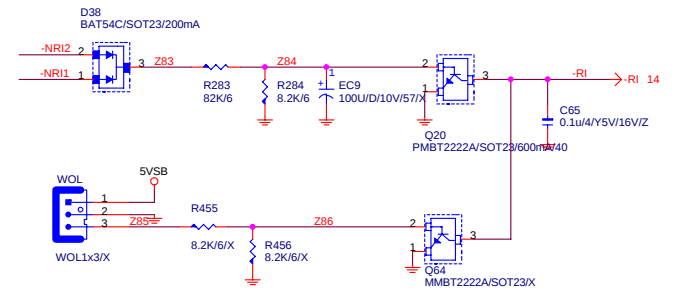
Size	Document Number	Rev
Custom	GA-8VM800M-775	1.0
Date:	Tuesday, August 16, 2005	Sheet 21 of 30



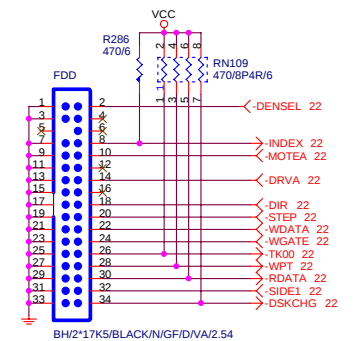
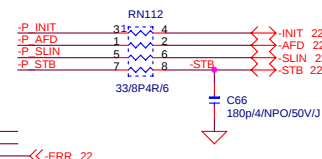
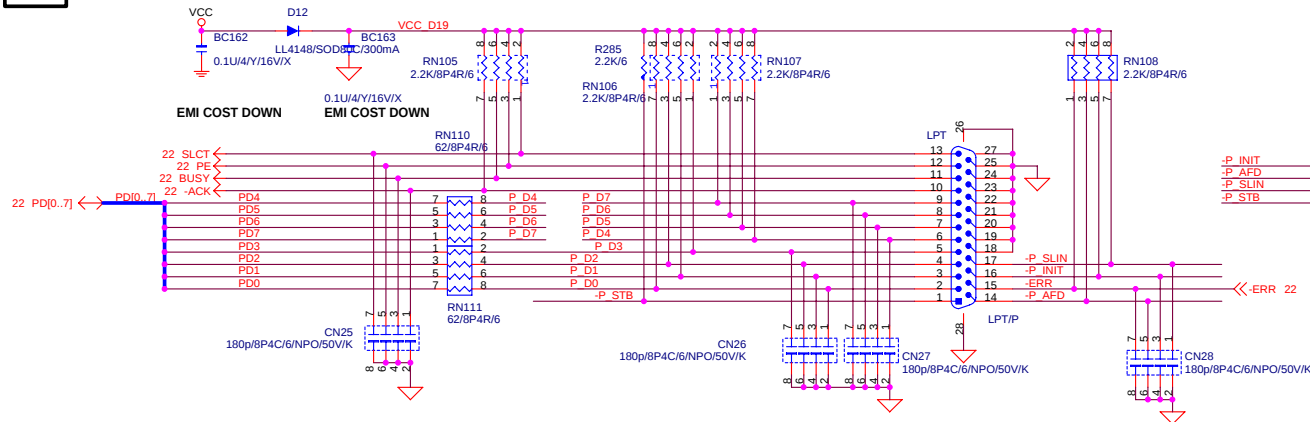
COM A, B



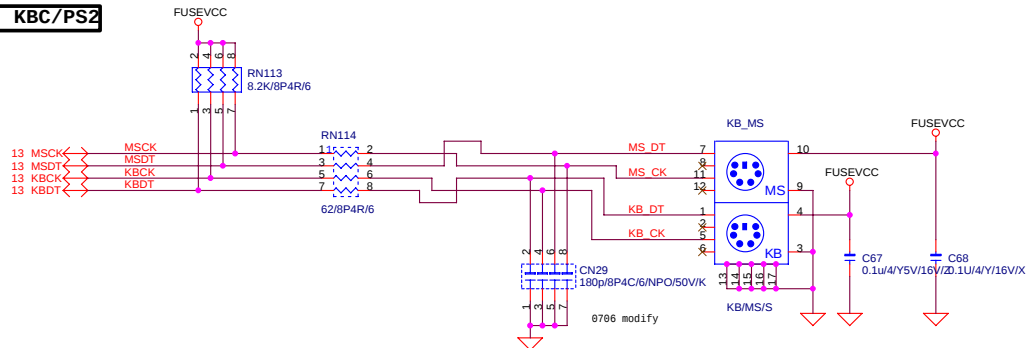
WAKE UP



LPT



KBC/PS2



GIGABYTE

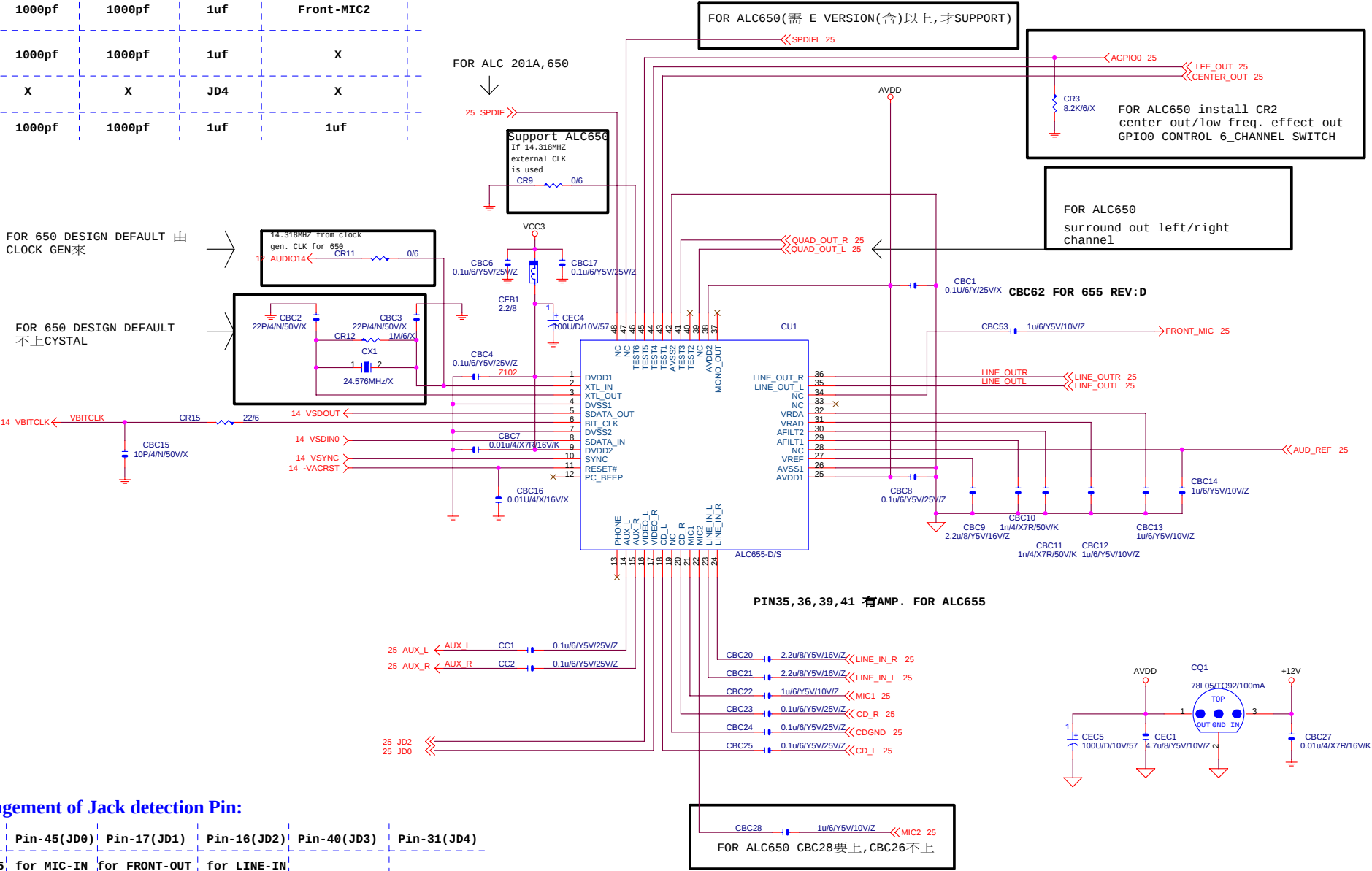
Title			
COM,PRT,FDD,KB,IR			
Size	Document Number		Rev
Custom	GA-8VM800M-775		1.0
Date:	Tuesday, August 16, 2005	Sheet	23 of 30

Filter Cap design:

	Pin-29	Pin-30	Pin-31	Pin-32
ALC655 Rev D	1000pf	1000pf	1uf	Front-MIC2
ALC655 Rev C	1000pf	1000pf	1uf	X
ALC658	X	X	JD4	X
ALC650	1000pf	1000pf	1uf	1uf

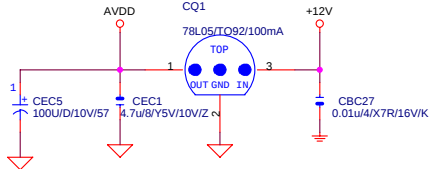
FOR 650 DESIGN DEFAULT 由CLOCK GEN來

FOR 650 DESIGN DEFAULT 不上CRYSTAL



Arrangement of Jack detection Pin:

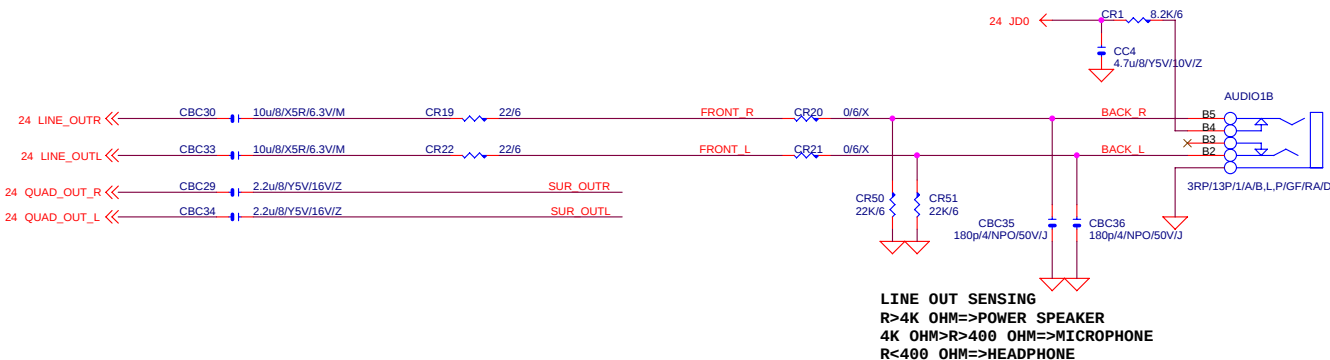
	Pin-45(JD0)	Pin-17(JD1)	Pin-16(JD2)	Pin-40(JD3)	Pin-31(JD4)
ALC655	for MIC-IN	for FRONT-OUT	for LINE-IN		
ALC658	for MIC-IN	for UAJ1	for UAJ2	for FRONT-OUT	for LINE-IN
				External pull high is needed	External pull high is needed



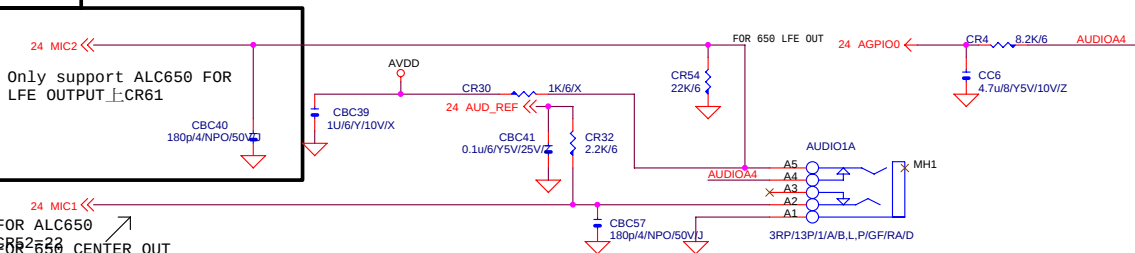
LINE OUT

JDO, JD2, GPIO0 爲偵測 DEVICE INPUT 時由 LOW TO HIGH Edge trigger (pop manual)

1/2(3.14)RC=1/2(3.14)8.2K*4.7U=4.3HZ 以上 AC 信號全部衰減 TO 0V 不會造成 JDO 誤動作 (無 device 時 play wav)



MIC

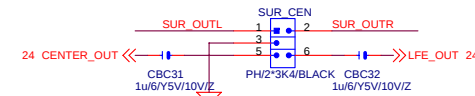


MICROPHONE IN SENSING (當 INPUT) (利用 vref 偏壓與 CR43, CR32 並聯求出阻抗)
 $7.1k \text{ ohm} > R > 2.3k \text{ ohm} \Rightarrow \text{microphone in}$
 $R < 2.3k \text{ ohm}$ or $R > 7.1k \text{ ohm} \Rightarrow \text{unknown device}$

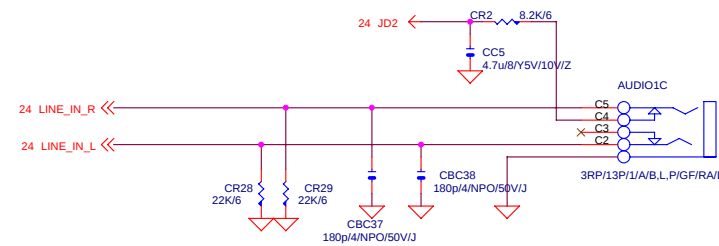
MICROPHONE IN SENSING (當 OUTPUT)
 $R > 4K \text{ OHM} \Rightarrow \text{POWER SPEAKER}$
 $4K \text{ OHM} > R > 400 \text{ OHM} \Rightarrow \text{MICROPHONE}$
 $R < 400 \text{ OHM} \Rightarrow \text{HEADPHONE}$

FOR SUPPORT 6 CHANNEL,
SURROUND OUT

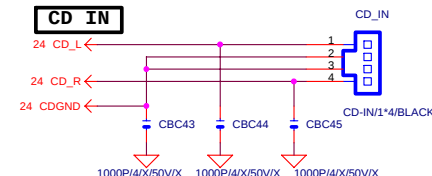
CENTER OUT, LOW
FREQUENCY EFFECT OUT



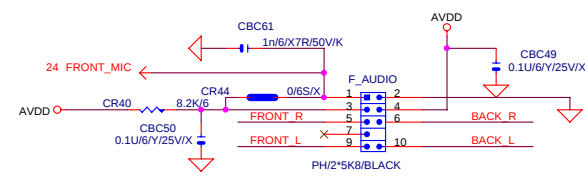
LINE-IN



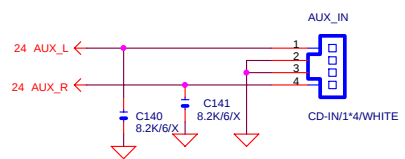
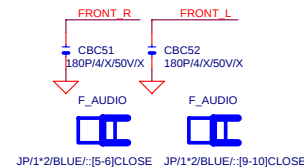
CD IN



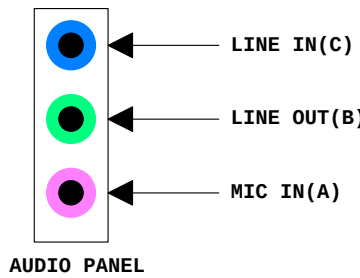
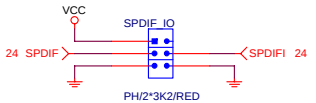
INTEL FRONT AUDIO



For EMI



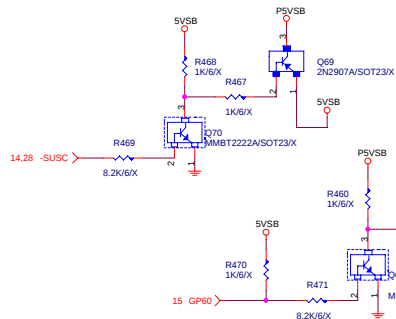
SPDIF_IO



GIGABYTE CORP.

Audio Output, Game Port

Title	GA-8VM800M-775	Rev	1.0
Size	Custom	Document Number	
Date:	Tuesday, August 16, 2005	Sheet	25 of 30



(GP060 DEFAULT HIGH, RESUME WELL)

States for green LED

LED States	ACPI States	GP60
ON	S1,S3	0
OFF	S0,S5	1

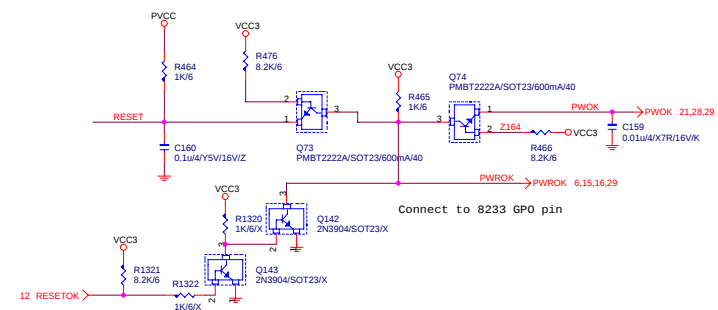
States for a single-color power LED

LED States	ACPI States			
OFF	S1,S3,S5			
Steady Green	S0			
Blinking Green	S0(message waiting)			
Blinking Green	S0(message waiting)			

States for a dual-color power LED

LED States	ACPI States				
OFF	S5				
Steady Green	S0				
Blinking Green	S0(message waiting)				
Steady Yellow	S1,S3				
Blinking Yellow	S1,S3(message waiting)				

RESET

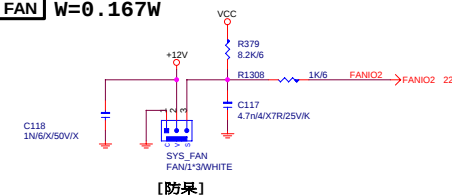


Connect to 8293 GPO pin

3 PIN POWER LED
LAYOUT PLACE CLOSE
TO F_PANEL

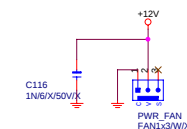
PWR_LED
1 MPD+
2 MPD-
3 MPD-
PH1X3H[11NH2-000103-0501]

SYSTEM FAN W=0.167W



[防噪]

POWER FAN



[防噪]

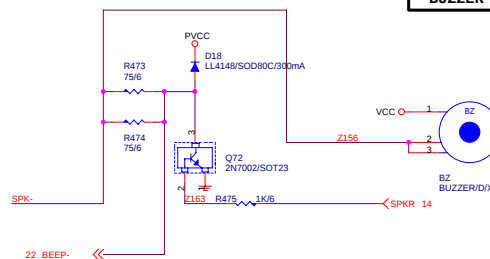
PVCC 在VCC PLANE 切割互連

NOTE:ALLEGRO use NET connect.

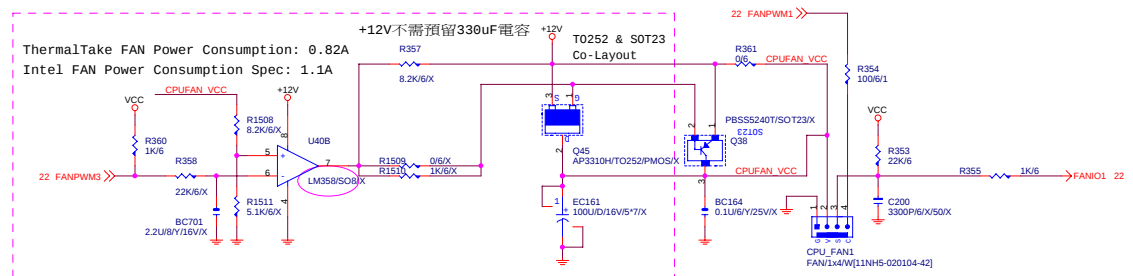


Note 115

BUZZER



CPU FAN



GIGABYTE

File	PANEL, STR LED & FANS		
Size	Document Number	GA-8VM800M-775	Rev 1.0
Custom			
Date:	Tuesday, August 16, 2005	Sheet 26 of 30	

	10/100	Giga	Giga
	8100C	8110S	8110SB
AVDDH	N/A	3.3V	3.3V
V_12P	2.5V	N/A	3.3V
AVDDL	3.3V	2.5V	2.5V
V_DAC	N/A	2.5V	2.5V
DVDD	2.5V	1.8V	1.3V
DVDD_A	2.5V	1.8V	1.3V

	Yellow	Green	Orange
10Mb	---	OFF	OFF
100Mb	---	ON	OFF
1Gb	---	OFF	ON
Link	ON	---	---
Active	Blink	---	---



FOR EMI



FOR EMI



FOR EMI



FOR EMI



FOR EMI



FOR EMI



FOR EMI



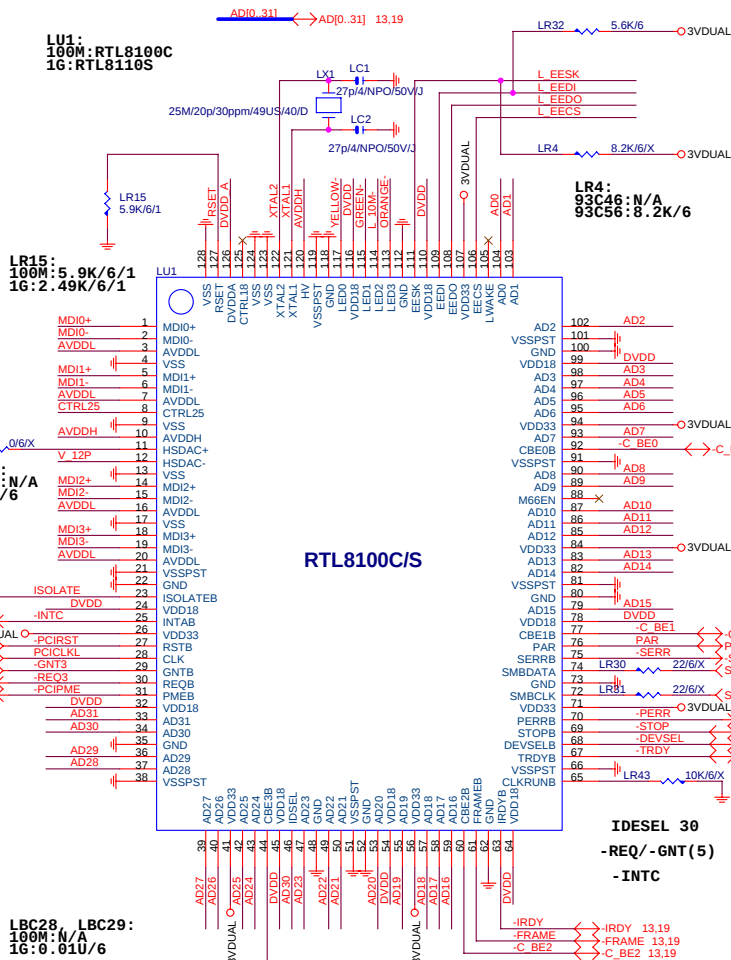
FOR EMI



FOR EMI



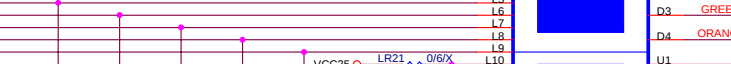
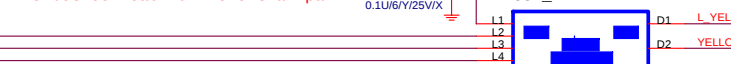
FOR EMI



RTL8100C/S



Spacing : at least 50 mils between each differential pair

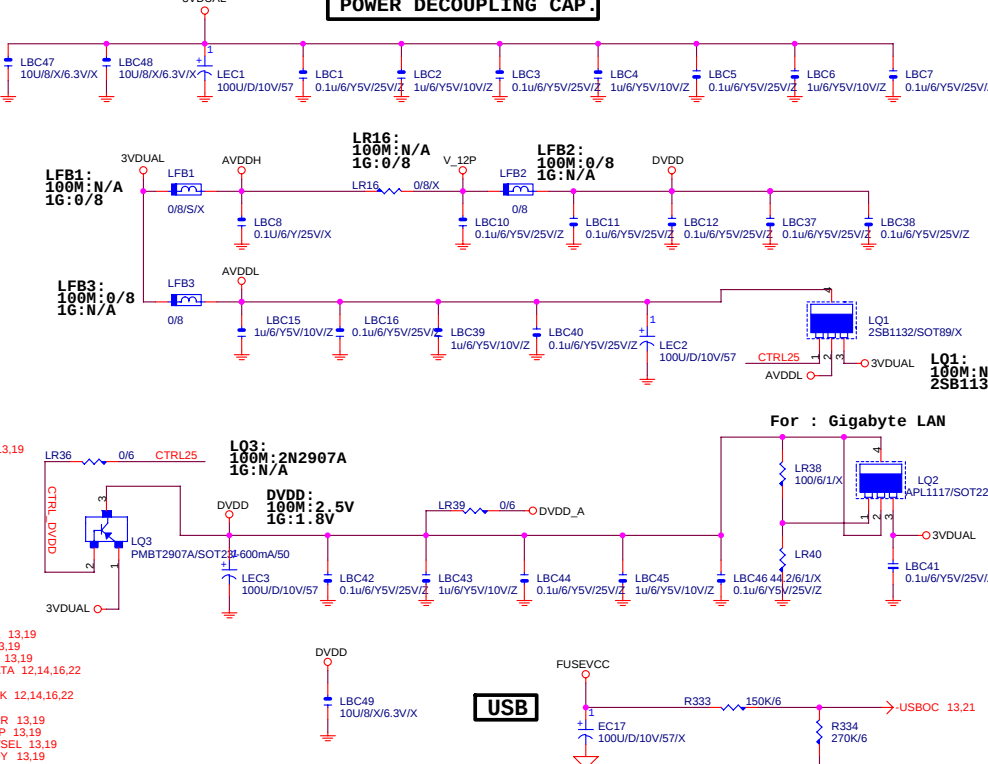


LR22, LR23, LBC26 Close to Lan Chip

Realtek suggestion (TX+, TX-).

LR24, LR25, LBC27 Close to Lan Chip

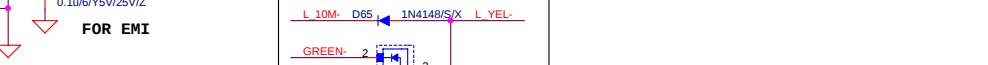
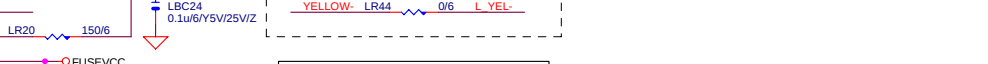
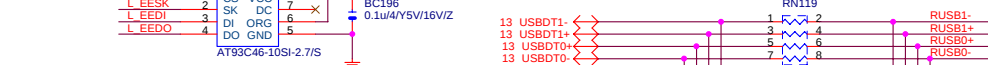
Realtek Suggestion (RX+, RX-).



POWER DECOUPLING CAP.



LAN EEPROM



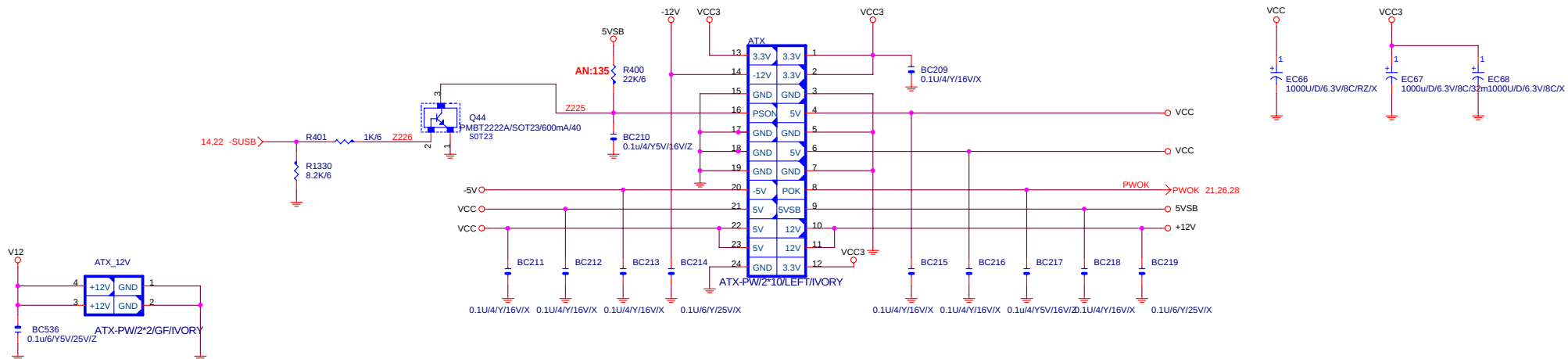
FOR 8100C

FOR 8110S

Title			GIGABYTE
Document Number			LAN RTL8110C
Date			Tuesday, August 16, 2005
Sheet			27 of 30
Rev			1.0

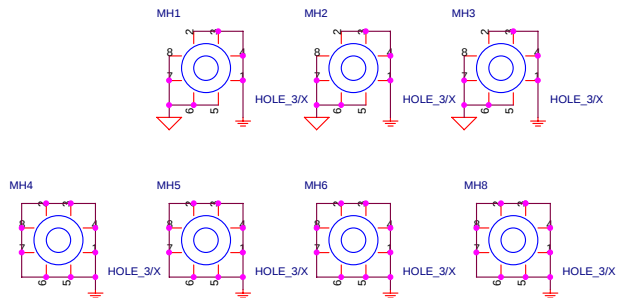
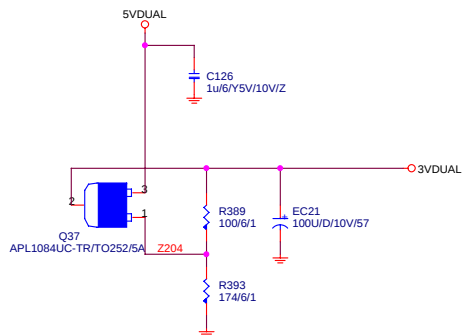
ATX CONN, DC POWER

ATX POWER CONNECTOR

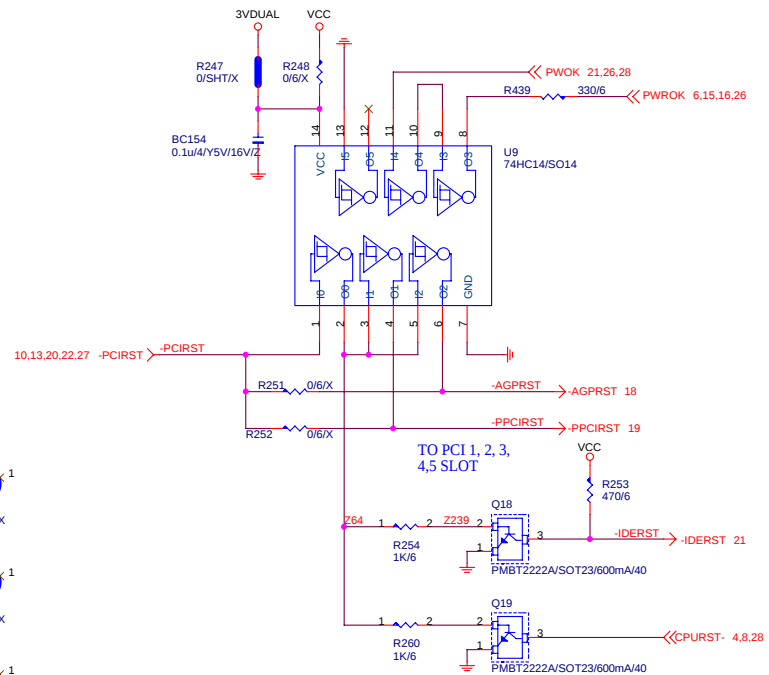
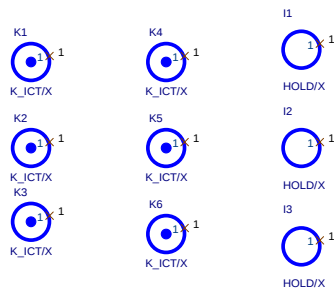


PCI+IDE RESET

5VDUAL TRANS TO 3VDUAL(3.3V)



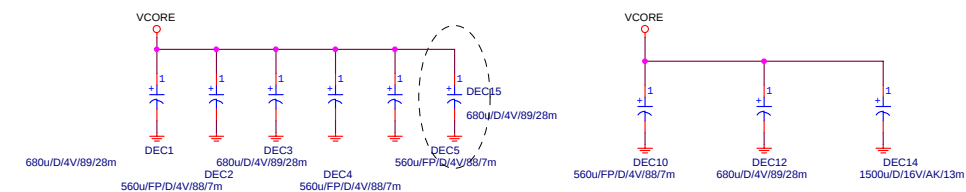
(08/12) HOLE_3-2



GIGABYTE

ATX, DC POWER

Size Custom	Document Number GA-8VM800M-775	Rev 1.0
Date: Tuesday, August 16, 2005	Sheet 29 of 30	



DD1 :在HIGH SIDE 發生S-D SHORT 時(OVP), LOW SIDE MOSFET TURN ON ,讓Vcore 降壓,同時V12 也會下降6-7V以下時,造成PWM 無法提供POWER TO LOW SIDE TURN ON,所以加DD1 延長PWM POWER 提供給LOW SIDE MOSFET TURN ON 保護CPU VOLTAGE 過高.

DR9,DC5 FOR V12 OVER 19V 以上,SPEC (18V)

DR12 為一個 CYCLE的DUTY(50%) DELAY :讓限流時間DELAY (DR35,DC13) 才啟動. DR39:240K 工作頻率=720KHZ / 4PHASE=180K(1 PHASE)

