8S651MP-RZ Schematics

Revision 1.0

Dte:93/07/21

SHEET	TITLE
1	COVER SHEET
2	BOM & PCB MODIFY HISTORY
3	BLOCK DIAGRAM
4,5,6	INTEL CPU_WMT_478
7-10	SIS651/645DX (NORTH BRIDGE) HOST; DDR; AGP,HYPER ZIP
11-14	962 (SOUTH BIRDGE)
15	CKG(ICS952004) + CKBF (ICS93722)
16,17	DDR SDRAM DIMMS 1,2 & DDR TERMINATION
18	AGP SLOT
19	VGA Connector
20	PCI SLOT 1-3
21	IDE,USB
22	Winbond W83697HF
23	BIOS
24	COM,PRT,FDD,KB/MS,IR
25	CNR SLOT
26	AUDIO AC 97 CODEC
27	AUDIO JACK,GAME PORT
28	RTL8100B & USB CONNECTOR
29	PANEL,STR LED,FANS ,CPU GN
30	VCORE PHASE PWM HIP 6301 + 6601
31	ALL POWER CIRCUIT
32	ATX & ATX12V CONN
33	GPIO Connecttion
34	TEST POINT

GIGABYTE

Title: COVER SHEET

Size: Custom | Document Number: 8S651MP-RZ | Rev: 1.0

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Model Name: 8S651MP-RZ

Version: 1.0

Component value change history

AUTOBOM
2003/09/08

Date	Change Item	Reason
09/08	RELAYOUT REV:1.01	FOR PRESCOTT CPU
09/10	BOM	R467 1.05k/6/1 change to 931/6/1
09/17	BOM	CHANG U14 TO ISA FLASH ROM
09/18	BOM	CHANG PCB FROM 1.01 TO 1.02
04/01/05	BOM	SUPPORT PRESCOTT CPU'S NEW RATIO REGISTER
04/02/19	BOM	TURN P-BOM
04/03/15	BOM	FOR D STEPPING ISSUE
04/04/07	BOM	651 C1 EVALUATION
04/05/21	BOM	TURN P-BOM,N/B heatsink add tape,FB42 from short wire to 100
04/06/03	BOM	CHANGE COMP (R11,R12) from 51.1 to 61.9
04/06/14	BOM	CHANGE CPU RM from Black to Yellow
04/07/13	BOM	FOR CKD BOM
04/07/15	BOM	Change R639 from 100 to 80.6
04/07/15	BOM	FOR CKD BOM

Circuit or PCB layout change for next version

Date	Change Item	Reason
09/18	RELAYOUT REV:1.02	FOR FACTORY MANUFACTURE
09/23	RELAYOUT REV:1.03	ONE NET INSIDE CPU SOCKET
12/23	RELAYOUT REV:4.1	FIX PRESCOTT CPU RATIO FAIL ISSUE
12/29	RELAYOUT REV:4.1	ADD PROCESSOR HOT FUNCTION
04/04/02	RELAYOUT REV:1.0	CHANGE CHIPSET TO C1 VERSION

GIGABYTE

Title: BOM & PCB MODIFY HISTORY

Size: Custom | Document Number: 8S651MP-RZ | Rev: 1.0

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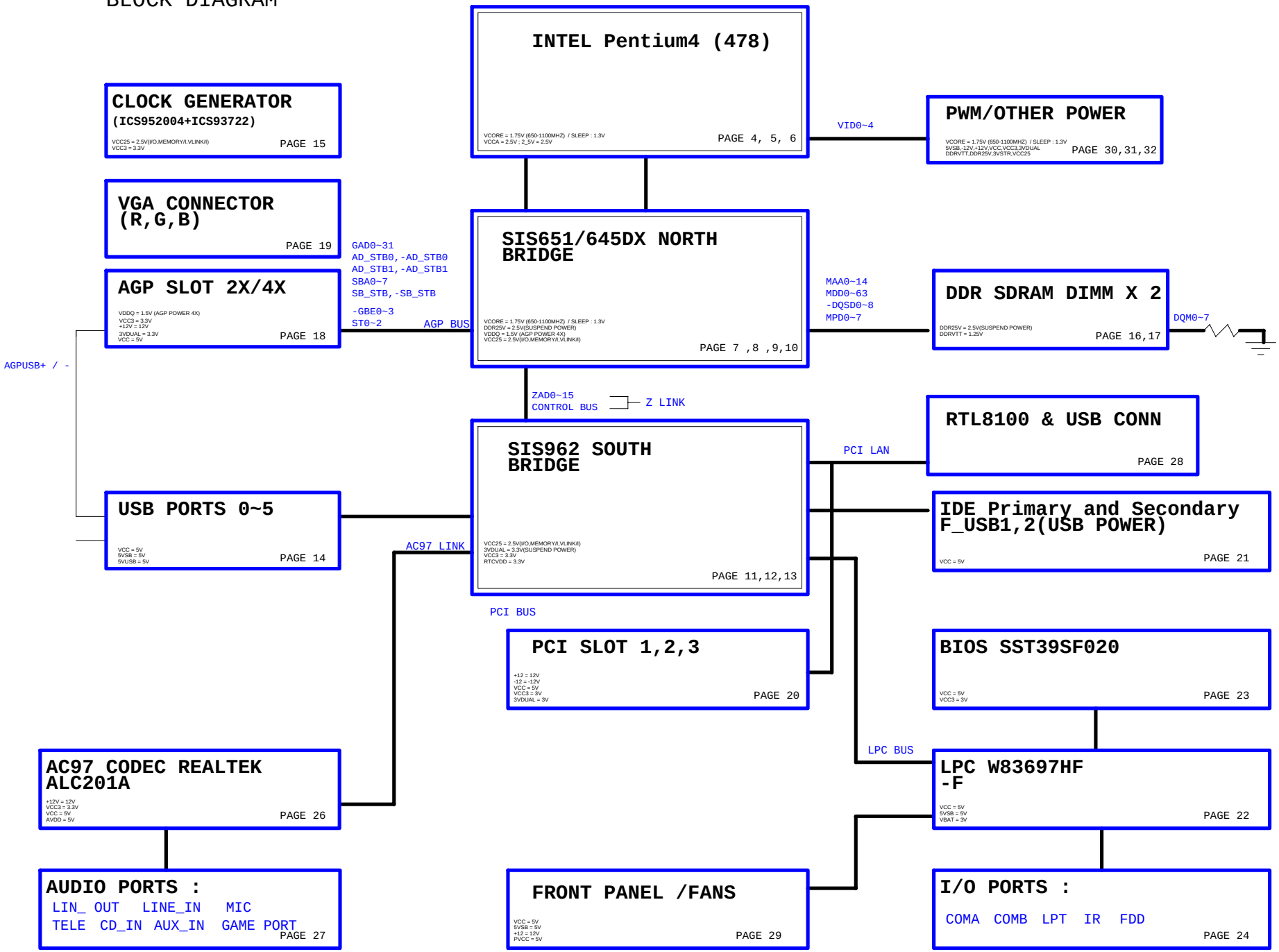
BLOCK DIAGRAM



GIAGBYTE

Title	BLOCK DIAGRAM	
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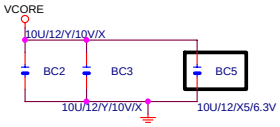
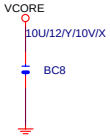
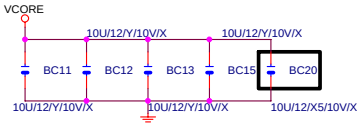
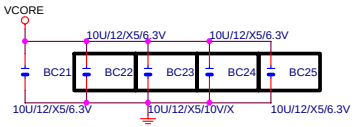
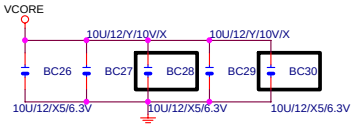
(X5R) X11 1206(10U) NOTE:GIGA

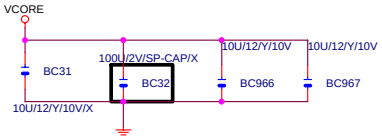


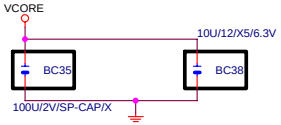


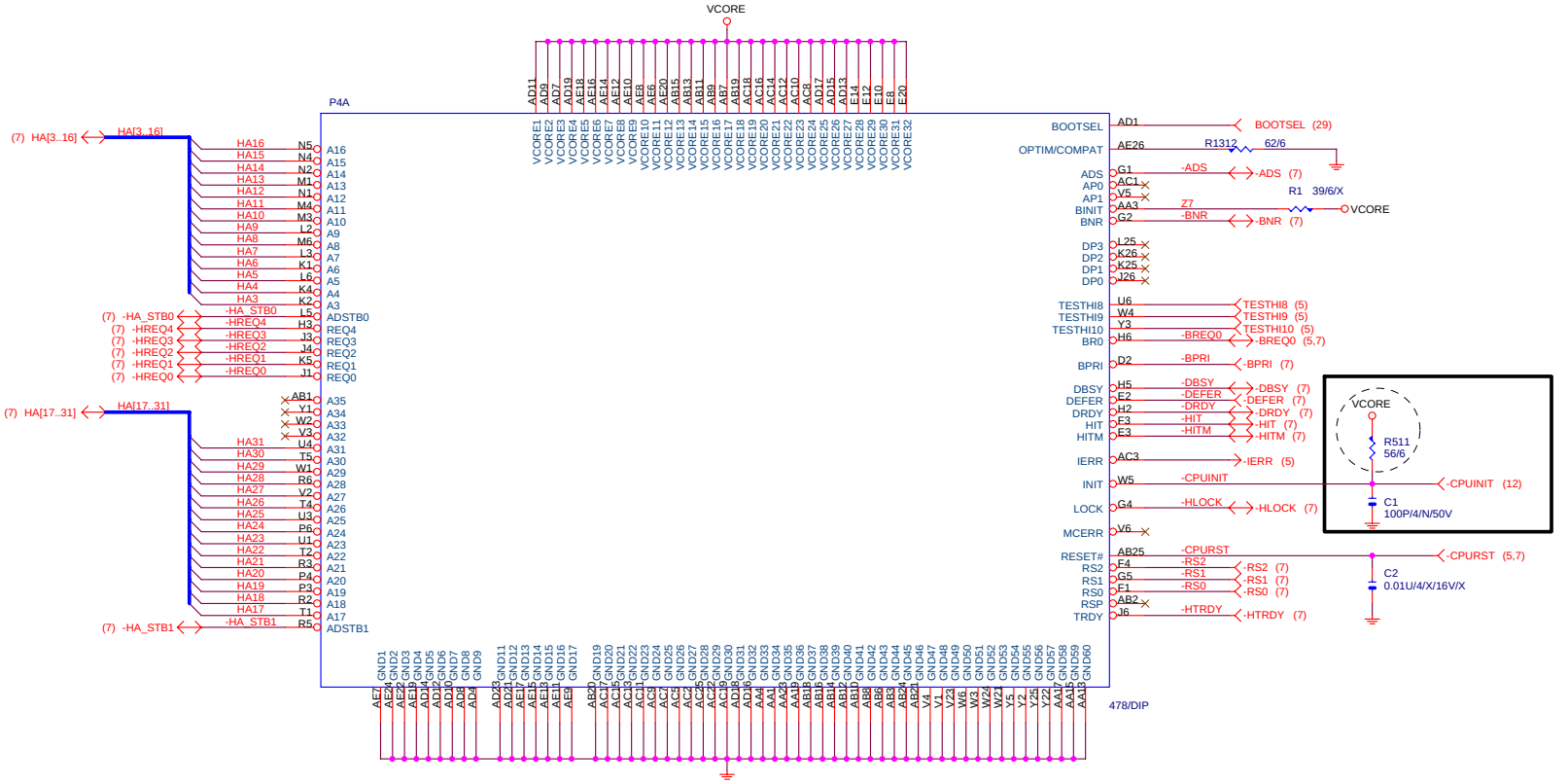












GIGABYTE		
Title	WILLIAMATE 478A	
Size: Custom	Document Number: 8S651MP-RZ	Rev: 1.0
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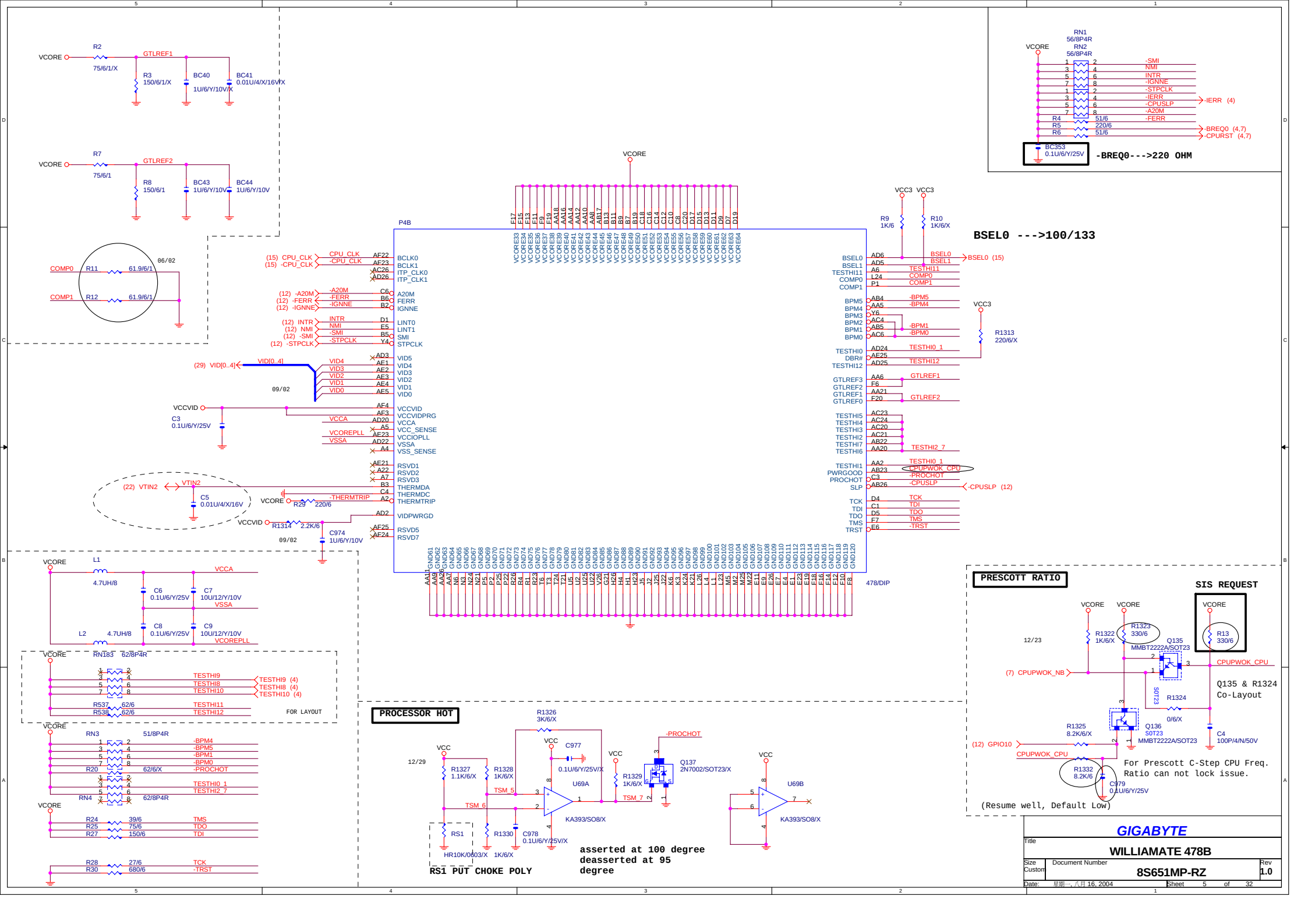
P4B
BCLK0
BCLK1
ITP_CLK0
ITP_CLK1
A20M
FERR
IGNNE
LINT0
LINT1
SMI
STPCLK
VID5
VID4
VID3
VID2
VID1
VID0
VCCVID
VCCVIDPRG
VCCA
VCC_SENSE
VCCIOPLL
VSSA
VSS_SENSE
RSVD1
RSVD2
RSVD3
THERMDA
THERMDC
THERMTRIP
VIDPWRGD
RSVD5
RSVD7
BSEL0
BSEL1
TESTHI11
COMP0
COMP1
BPM5
BPM4
BPM3
BPM2
BPM1
BPM0
TESTHI0
DBR#
TESTHI12
GTLREF3
GTLREF2
GTLREF1
GTLREF0
TESTHI5
TESTHI4
TESTHI3
TESTHI2
TESTHI7
TESTHI6
TESTHI1
PWRGOOD
PROCHOT
SLP
TCK
TDI
TDO
TMS
TRST
478/DIP
BSEL0 --->100/133
PRESCOTT RATIO
SIS REQUEST
Q135 & R1324
Co-Layout
For Prescott C-Step CPU Freq.
Ratio can not lock issue.
(Resume well, Default Low)
PROCESSOR HOT
asserted at 100 degree
deasserted at 95
degree
RS1 PUT CHOKE POLY
-BREQ0--->220 OHM
FOR LAYOUT
GIGABYTE
WILLIAMATE 478B
8S651MP-RZ
1.0
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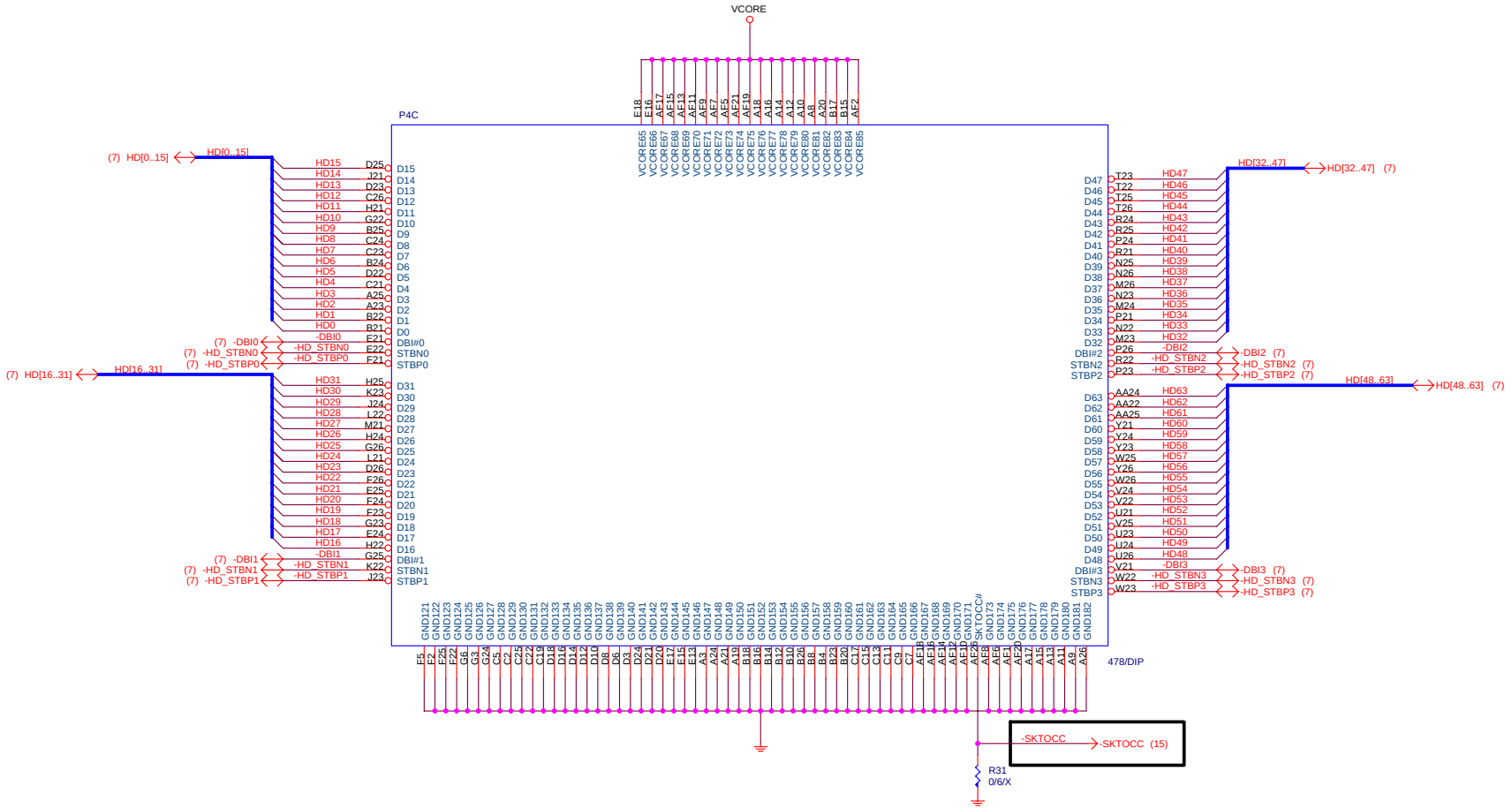

GIGABYTE			
Title	WILLIAMATE 478C		
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-DBI[0..3] <-> -DBI[0..3] (6)
HD[0..63] <-> HD[0..63] (6)
HA[3..31] <-> HA[3..31] (4)
GD[0..31] -> GD[0..31] (18)
SBA[0..7] -> SBA[0..7] (18)
ST[0..2] -> ST[0..2] (18)

651/645DX-1

AGP

HOST

U38A

SIS651/C1

(15) HCLK
(15) -HCLK
(4) -HLOCK
(4) -DEFER
(4) -HTRDY
(4,5) -CPURST
(5) CPUPWOK_NB
(4) -BPRI
(4,5) -BREQ0
(4) -RS2
(4) -RS1
(4) -RS0
(4) -ADS
(4) -HITM
(4) -HIT
(4) -DRDY
(4) -DBSY
(4) -BNR
(4) -HREQ4
(4) -HREQ3
(4) -HREQ2
(4) -HREQ1
(4) -HREQ0
(4) -HA_STB1
(4) -HA_STB0

AC/BE#3 AC/BE#2 AC/BE#1 AC/BE#0 -> -GBE3 -GBE2 -GBE1 -GBE0 (18)
AREQ# -> -GREQ (18)
AGNT# -> -GGNT (18)
AFRAME# -> -GFRAME (18)
AIRDY# -> -GIRDY (18)
ATRDY# -> -GTRDY (18)
ADEVSEL# -> -GDEVSEL (18)
ASERR# -> -GSERR (18)
ASTOP# -> -GSTOP (18)
APAR -> GPAR (18)
RBF# -> -RBF (18)
WBF# -> -WBF (18)
PIPE# -> -PIPE (18)
AGP8XDET
ADBIH
ADBIL
SB_STB -> SB_STB (18)
SB_STB# -> -SB_STB (18)
AD_STB0 -> AD_STB0 (18)
AD_STB0# -> -AD_STB0 (18)
AD_STB1 -> AD_STB1 (18)
AD_STB1# -> -AD_STB1 (18)
AGPCLK -> GCLK_NB (15)
AGPRCOMP
A1XAVDD
A1XAVSS
A4XAVDD
A4XAVSS
AGPVREF -> AGPVREF (18)
AGPVSSREF
HDSTBN#3 -> -HD_STBN3 (6)
HDSTBN#2 -> -HD_STBN2 (6)
HDSTBN#1 -> -HD_STBN1 (6)
HDSTBN#0 -> -HD_STBN0 (6)
HDSTBP#3 -> -HD_STBP3 (6)
HDSTBP#2 -> -HD_STBP2 (6)
HDSTBP#1 -> -HD_STBP1 (6)
HDSTBP#0 -> -HD_STBP0 (6)

TP8
TP9
TP10

10mil AGPRCOMP R631 VDDQ 60.4/6/1/X 11/19

20mil A1XAVDD R632 0/6/SHT/X C784 1U/6/Y/10V C785 C786 0.1U/6/Y/25V/X A1XAVSS 1U/6/Y/10V/X VCC3

20mil A4XAVDD R633 0/6/SHT/X C787 1U/6/Y/10V C788 C789 0.1U/6/Y/25V/X A4XAVSS 1U/6/Y/10V/X VCC3

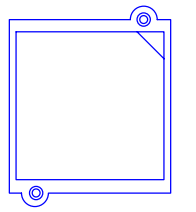
20mil C1XAVDD R634 0/6/SHT/X C790 1U/6/X/10V C791 C792 1U/6/X/10V C1XAVSS 1U/6/X/10V VCC3

20mil C4XAVDD R635 0/6/SHT/X C793 1U/6/X/10V C794 C795 1U/6/X/10V C4XAVSS 1U/6/X/10V VCC3
C953 1U/6/X/10V

C954 22U/12/Y/10V VCC3
C955 1U/6/X/10V C958 22U/12/Y/10V/X
C956 22U/12/Y/10V
C957 22U/12/Y/10V/X

N.B HEATSINK

NB_HEATSINK1



NB_HEATSINK

0402
VCORE
10mil R636 14/6/1 HNCOMP
Rds-on(n) = 10 ohm
HNCVERF = 1/3 VCORE
10mil R639 80.6/6/1 HPCOMP
Rds-on(p) = 56 ohm
HPCVERF = 2/3 VCORE
07/15

VCORE NOISE ISSUE
R638 75/6/1 C797 1U/6/Y/10V
10mil HVREF
R640 100/6/1 C798 SC38 0.01U/6/X/50V
1U/6/Y/10V
11/12 BOM

VCORE NOISE ISSUE
R637 150/6/1 C796 1U/6/Y/10V
10mil HNCVREF
R641 75/6/1 C799 0.01U/6/X/50V

place this capacitor under 650 solder side

VREF C-CAP PULL-UP MEASURE NOISE WORST.

GIGABYTE	
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DDR MD DAMPPING

Near DIMM 1

11/19
short pad

11/19
short pad

11/19
short pad

REV 0.2

MDD[0:63] <> MDD[0:63] (16,17)
DQM[0..7] > DQM[0..7] (16,17)
MAA[0..14] > MAA[0..14] (16,17)
-CS[0..3] > -CS[0..3] (16,17)
CKE[0..5] > CKE[0..5] (16)
-DQSD[0..7] > -DQSD[0..7] (16,17)

U38B

651
645DX-2

SIS651/C1

NO USE NO POP

20mil
SDAVDD
SDAVSS
R650 0/6/SHT/X
C800 1U/6/Y/10V
C801
C802 0.1U/6/Y/25V
1U/6/Y/10V/X
VCC3

20mil
DDRAVDD
DDRAVSS
R651 0/6/SHT/X
C803 1U/6/Y/10V
C804
C805 0.1U/6/Y/25V/X
1U/6/Y/10V/X
VCC3

NOISE ISSUE
10mil
DDRVREFB
C806 1U/6/Y/10V
R656 150/6/1
C808 0.01U/6/X/50V
R658 150/6/1
DDR25V

NOISE ISSUE
10mil
DDRVREFA
C809 1U/6/Y/10V
R659 150/6/1
C810 0.01U/6/X/50V
R661 150/6/1
DDR25V

VREF C-CAP PULL-UP MEASURE NOISE WORST.

Title	SIS651/645DX(DDR)
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GIGABYTE

NOTE: This page is for universal PCB design(suitable for both 645 or 650)

NB Hardware Trap Table

	0	1	Default	embedded pull-low (30~50K Ohm)
DLLEN#	enable PLL	disable PLL	0	yes
DRAM_SEL	SDR	DDR	1(DDR)	yes
TRAP0	normal	NB debug mode	0	yes
TRAP1	TV selection, NTSC/PAL(0/1)		0	
CSYNC	enable VB		0	
RSYNC	enable VGA interrupt		1	
LSYNC	enable panel link		0	

650
645DX-3

HyperZip

U38C

SIS651/C1

REV 0.2 EMI

NOISE ISSUE

SIS 645DX NO POP

SIS REQUEST
NO POP

DACAVDD1(VSS)---->DACAVDD2(VSS)
(SIS AP-02)

REV 0.2 SIS CHECK

11/17 MEM0131

20mil
10mil
10mil
20mil

Title	SIS651/645DX(HYPER ZIP)
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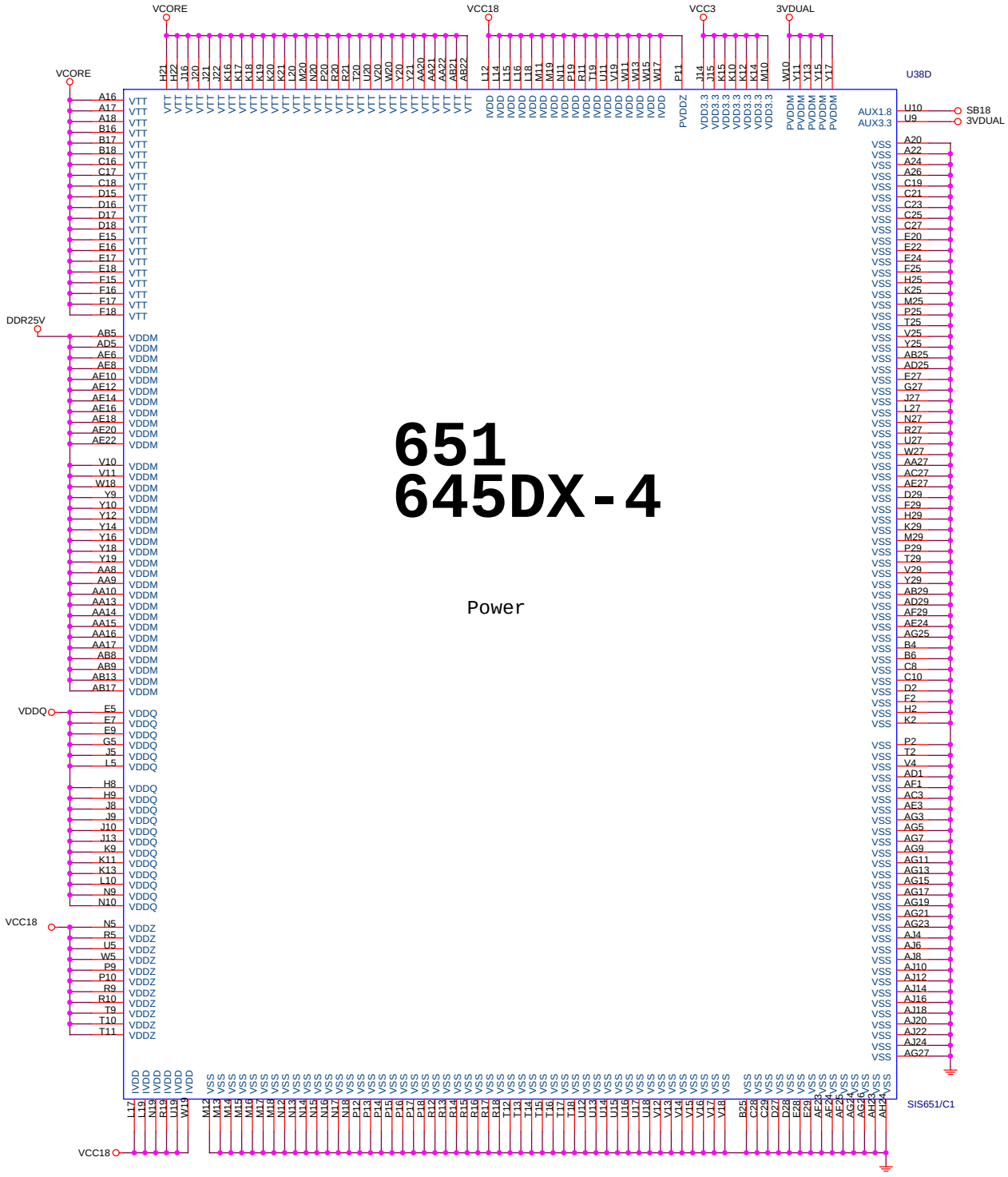
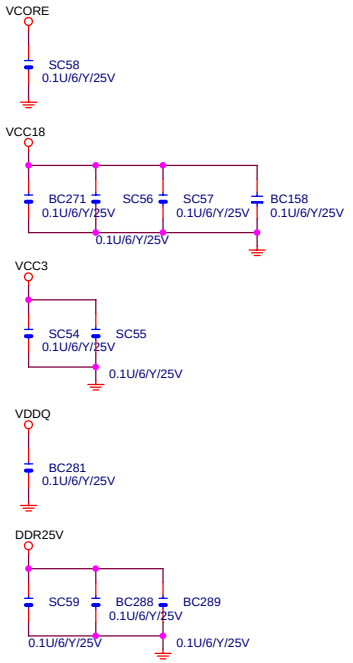
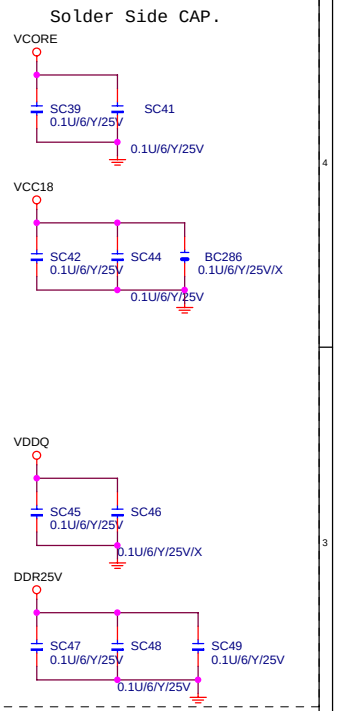
GIGABYTE







GIGABYTE		
Title: SIS651/645DX(PWR)		
Size: Custom	Document Number: 8S651MP-RZ	Rev: 1.0
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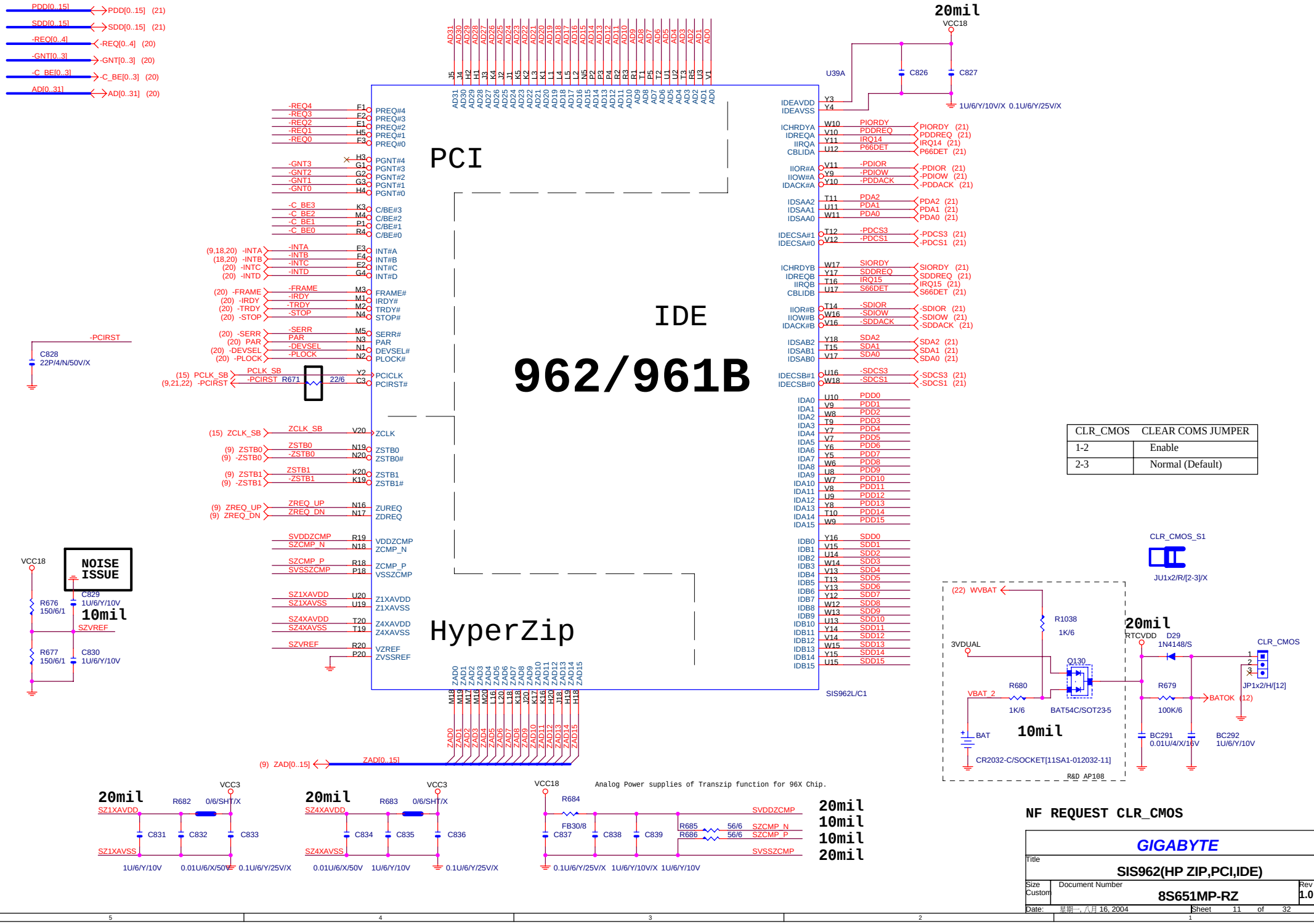
PDD[0..15] PDD[0..15] (21)
SDD[0..15] SDD[0..15] (21)
-REQ[0..4] -REQ[0..4] (20)
-GNT[0..3] -GNT[0..3] (20)
-C_BE[0..3] -C_BE[0..3] (20)
AD[0..31] AD[0..31] (20)
PCI
IDE
962/961B
HyperZip
SIS962L/C1
20mil
VCC18
U39A
C826
C827
1U/6/Y/10V/X 0.1U/6/Y/25V/X
IDEAVDD
IDEAVSS
-PCIRST
C828
22P/4/N/50V/X
NOISE ISSUE
VCC18
R676 150/6/1
R677 150/6/1
C829 1U/6/Y/10V
C830 1U/6/Y/10V
10mil
SZVREF
CLR_CMOS_S1
JU1x2/R/[2-3]/X
(22) WVBAT
R1038 1K/6
3VDUAL
Q130
R680 1K/6
BAT54C/SOT23-5
VBAT_2
BAT
CR2032-C/SOCKET[11SA1-012032-11]
10mil
R&D AP108
20mil
RTCVDD
D29 1N4148/S
R679 100K/6
BATOK (12)
BC291 0.01U/4/X/16V
BC292 1U/6/Y/10V
CLR_CMOS
JP1x2/H/[12]
CLR_CMOS | CLEAR COMS JUMPER
1-2 | Enable
2-3 | Normal (Default)
NF REQUEST CLR_CMOS
20mil
SZ1XAVDD
R682 0/6/SHT/X
C831 C832 C833
SZ1XAVSS
1U/6/Y/10V 0.01U/6/X/50V 0.1U/6/Y/25V/X
VCC3
20mil
SZ4XAVDD
R683 0/6/SHT/X
C834 C835 C836
SZ4XAVSS
0.01U/6/X/50V 1U/6/Y/10V 0.1U/6/Y/25V/X
VCC3
VCC18
Analog Power supplies of Transzip function for 96X Chip.
R684
FB30/8
C837 C838 C839
R685 56/6 SZCMP_N
R686 56/6 SZCMP_P
SVDDZCMP
SVSSZCMP
0.1U/6/Y/25V/X 1U/6/Y/10V/X 1U/6/Y/10V
20mil
10mil
10mil
20mil
GIGABYTE
Title
SIS962(HP ZIP,PCI,IDE)
Size Custom
Document Number
8S651MP-RZ
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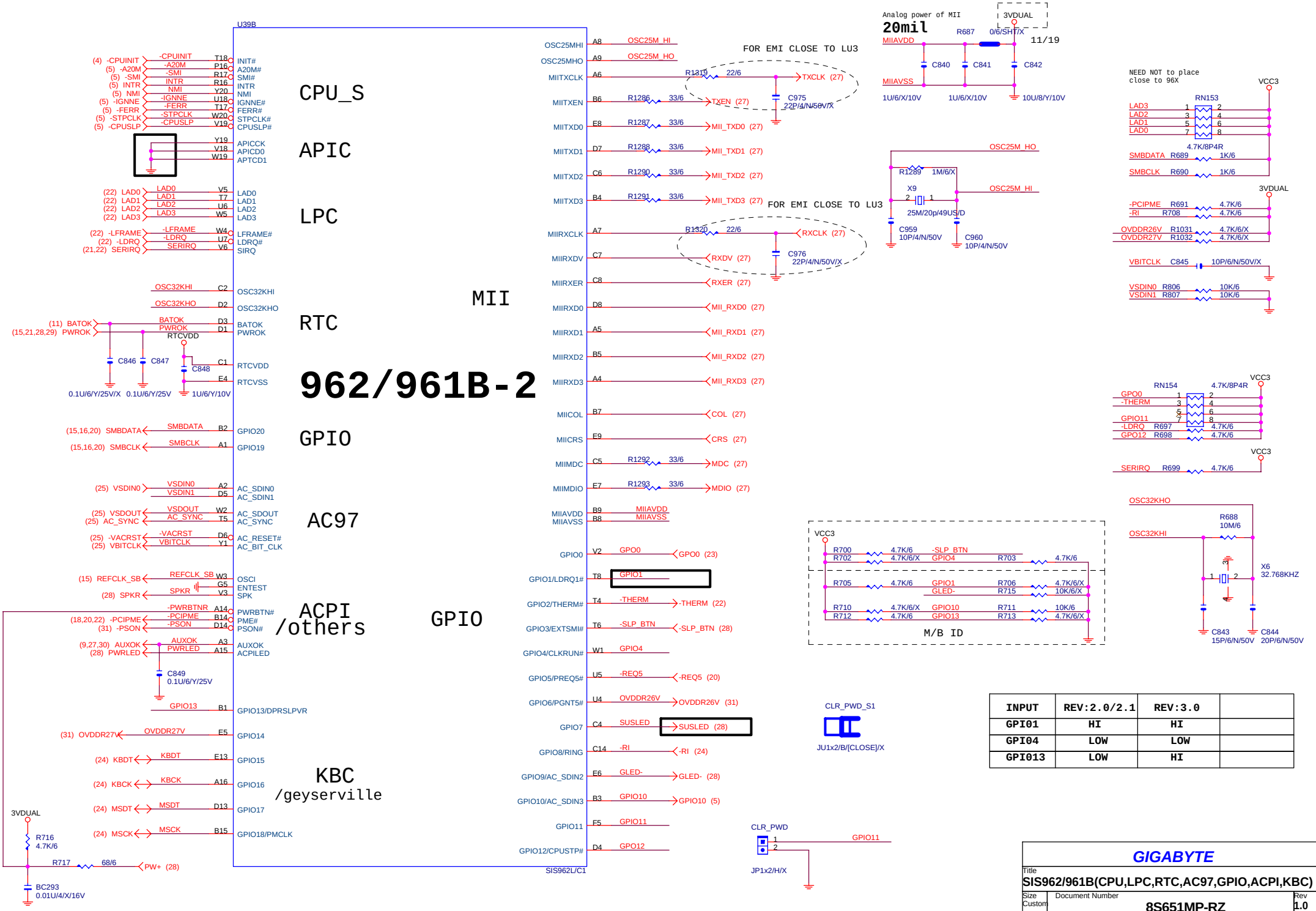
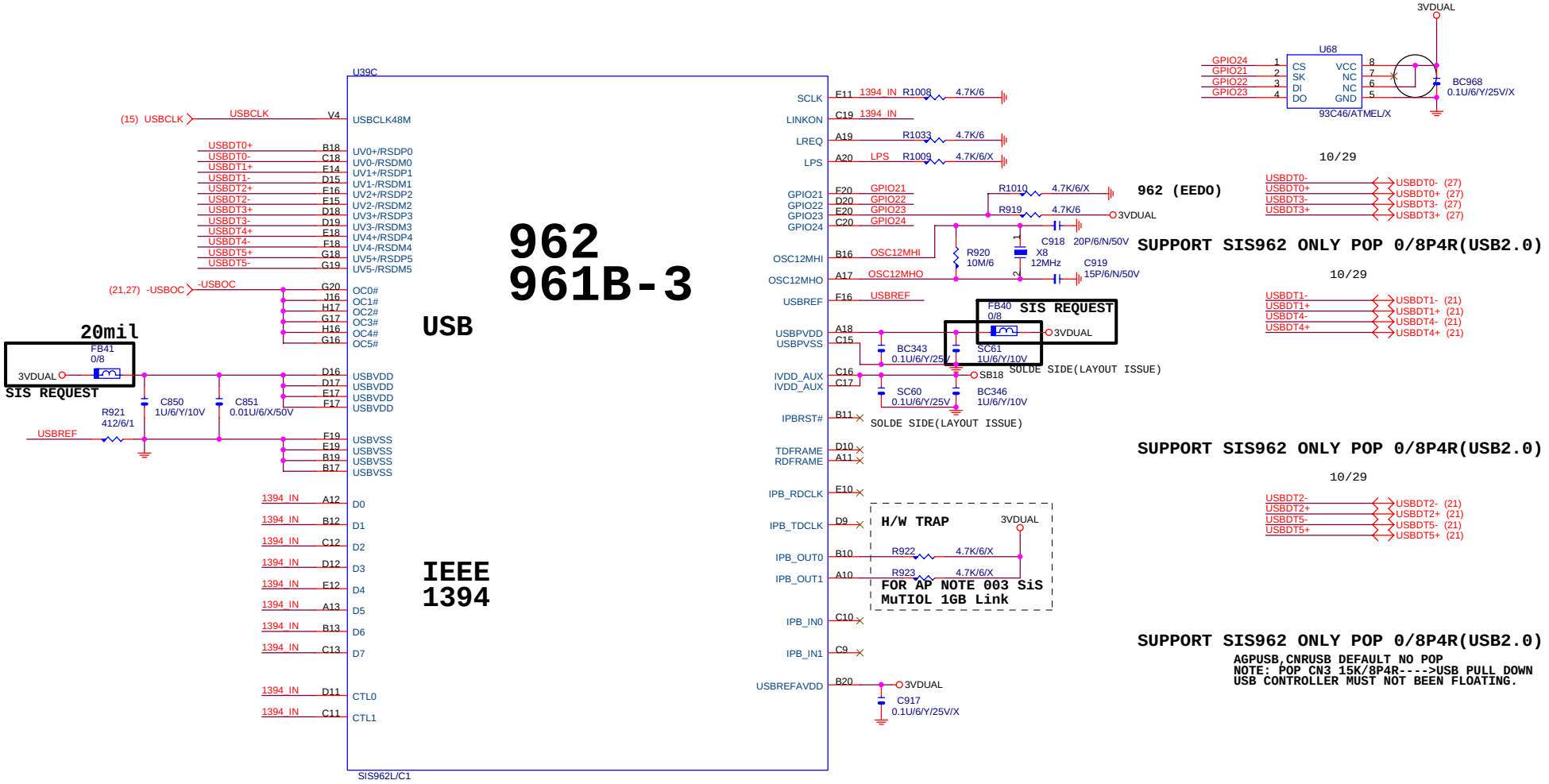


INPUT	REV:2.0/2.1	REV:3.0	
GPI01	HI	HI	
GPI04	LOW	LOW	
GPI013	LOW	HI	



GIGABYTE			
Title	SIS962/961B(USB20,1394)		
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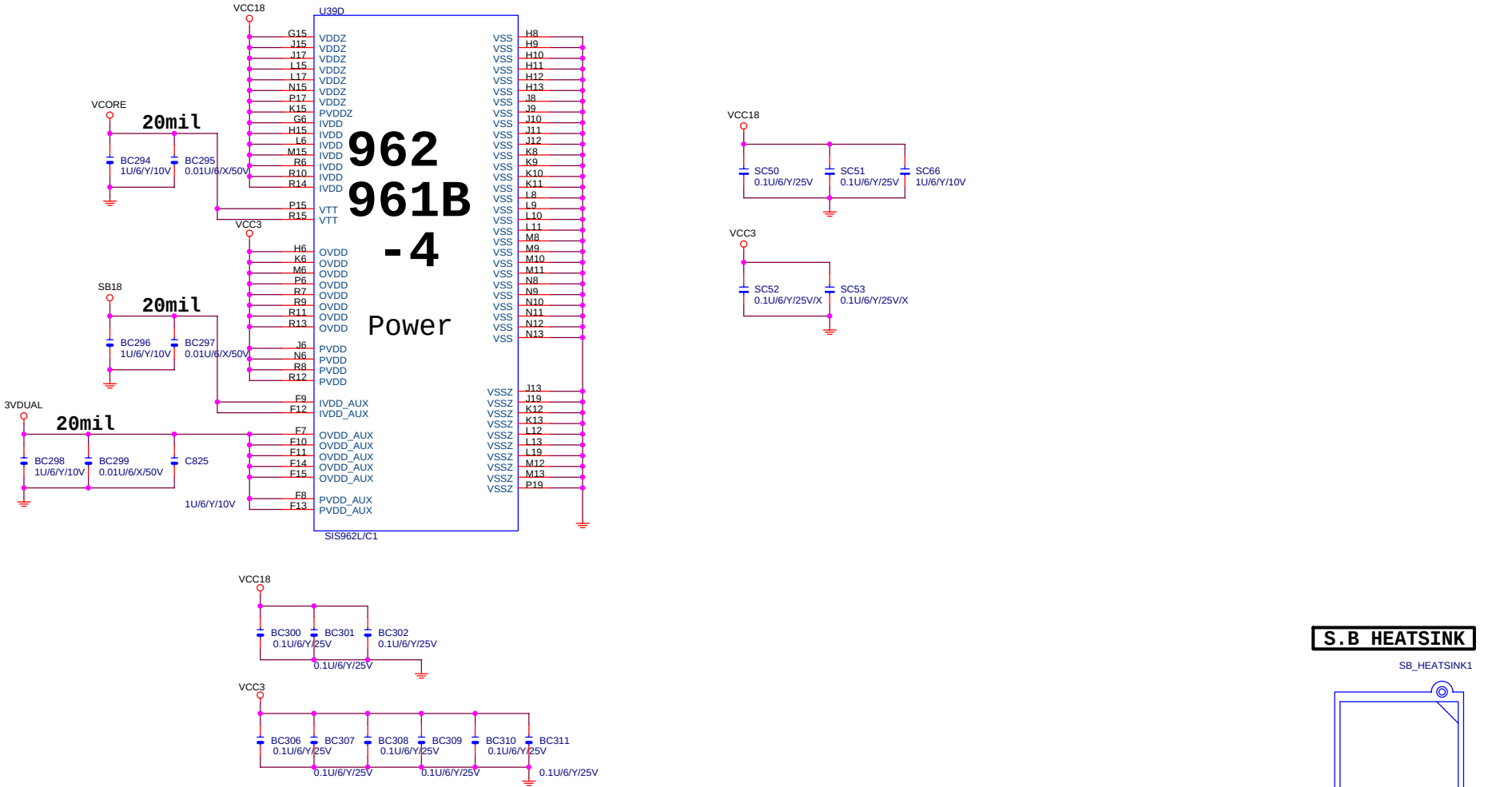

S.B HEATSINK

SB_HEATSINK1

SB_HEATSINK/X

GIGABYTE		
Title: SIS962/961B(PWR)		
Size: Custom	Document Number: 8S651MP-RZ	Rev: 1.0
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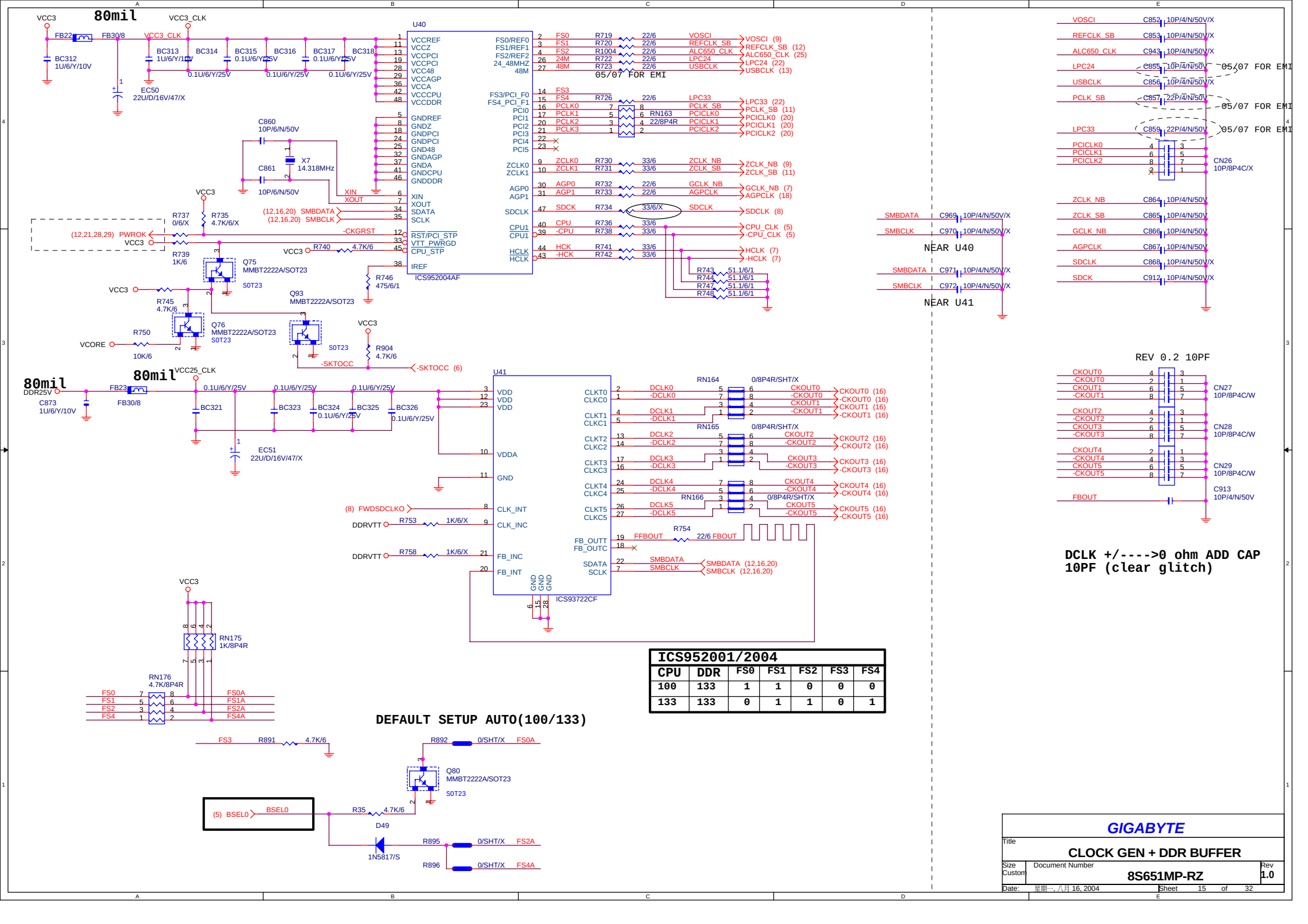
80mil
U40
ICS952004AF
05/07 FOR EMI
NEAR U40
NEAR U41
REV 0.2 10PF
DCLK +/---->0 ohm ADD CAP 10PF (clear glitch)
U41
ICS93722CF
ICS952001/2004
CPU DDR FS0 FS1 FS2 FS3 FS4
100 133 1 1 0 0 0
133 133 0 1 1 0 1
DEFAULT SETUP AUTO(100/133)
GIGABYTE
Title
CLOCK GEN + DDR BUFFER
Size Custom
Document Number
8S651MP-RZ
Rev 1.0
Date: 星期一, 八月 16, 2004
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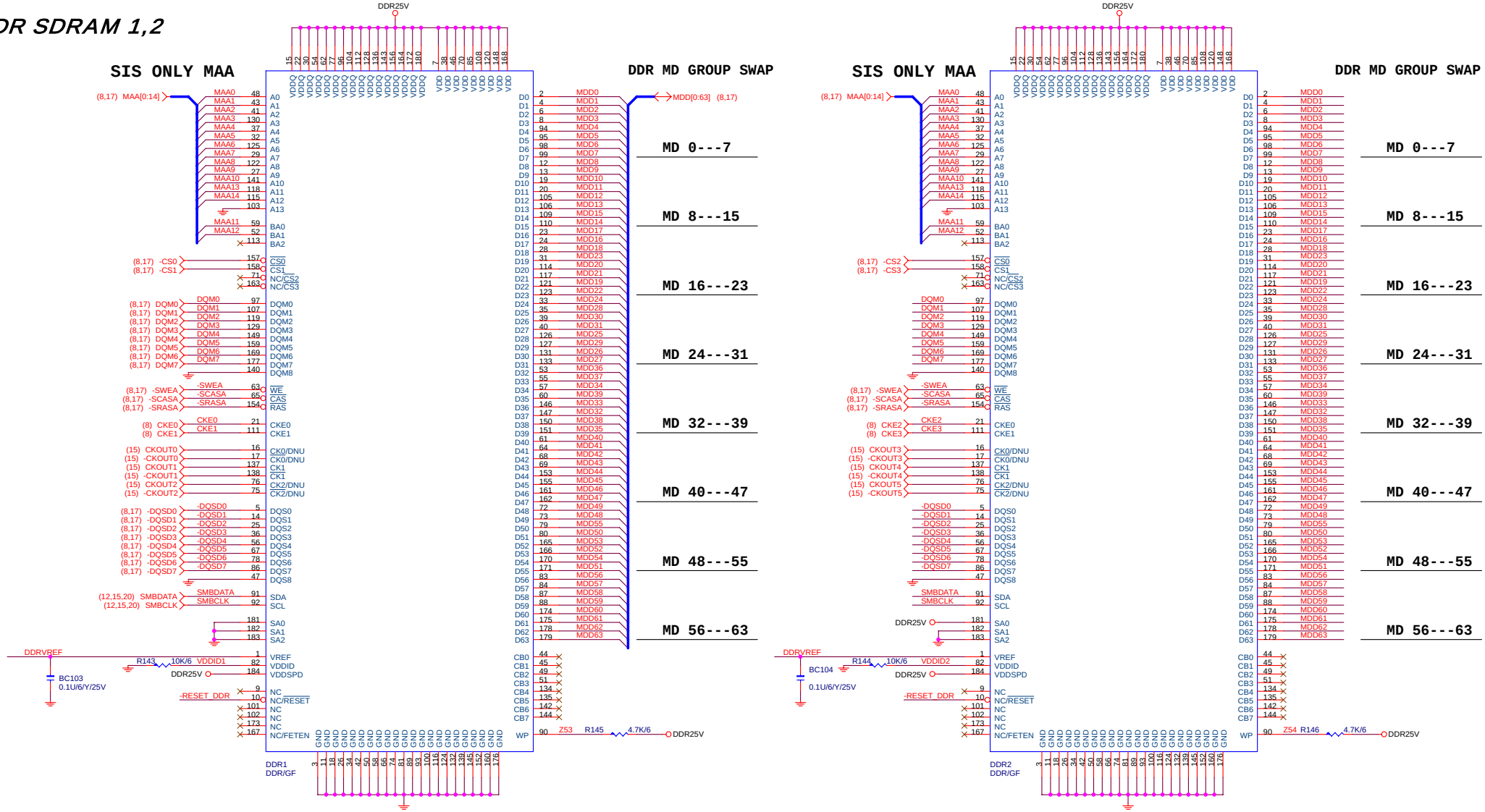
DDR SDRAM 1,2

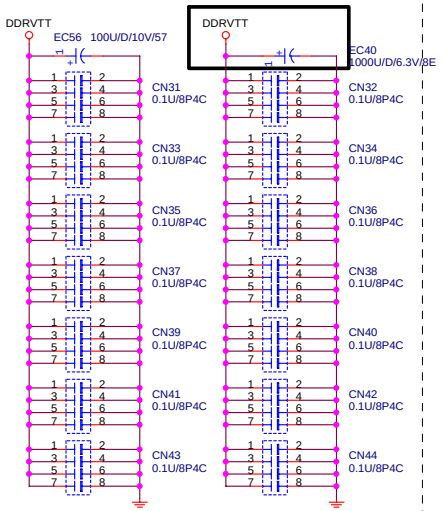


GIGABYTE

Title	DDR UNBUFFERED 1,2	
Size: Custom	Document Number: 8S651MP-RZ	Rev: 1.0
Date: 星期一, 八月 16, 2004	Sheet 16 of 32	

DDRVTT Decouple

NF REQUEST 10X12

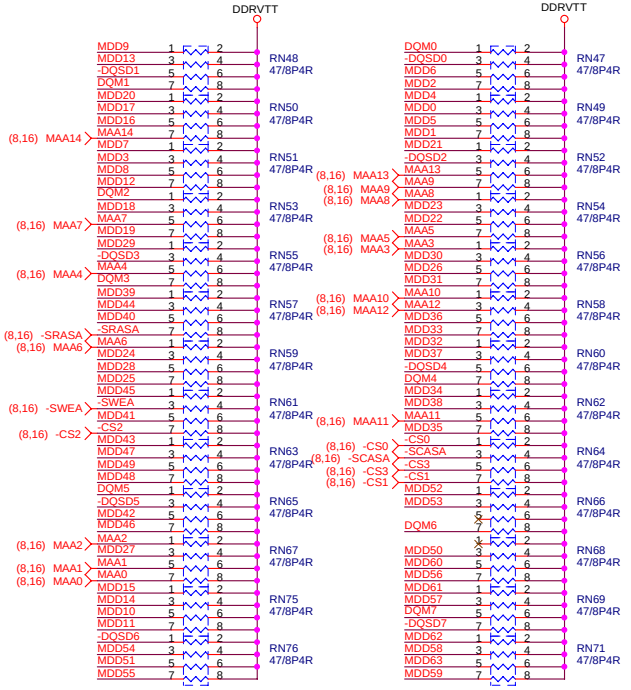


R&D NOTE 109 (0.1U/8P4C X9PCS)

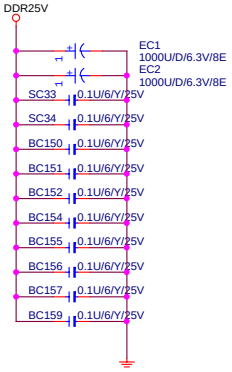
NOTE: Place these decoupling capacitors close to VTT_MEM termination resistors. (one decoupling coapcitor for each two R-packs)

DDR TERMINATION

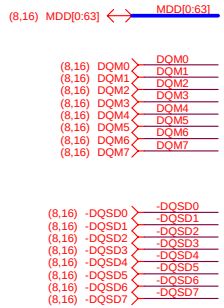
REV 0.2 DDR DIMM ISSUE
33-->47 OHM



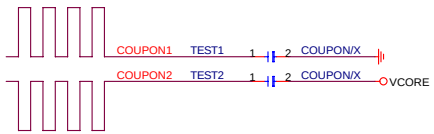
DDR25V Decouple



NOTE: Place Detribute 4 pcs per DDR module.



IMPEDENCE TESTING COUPON

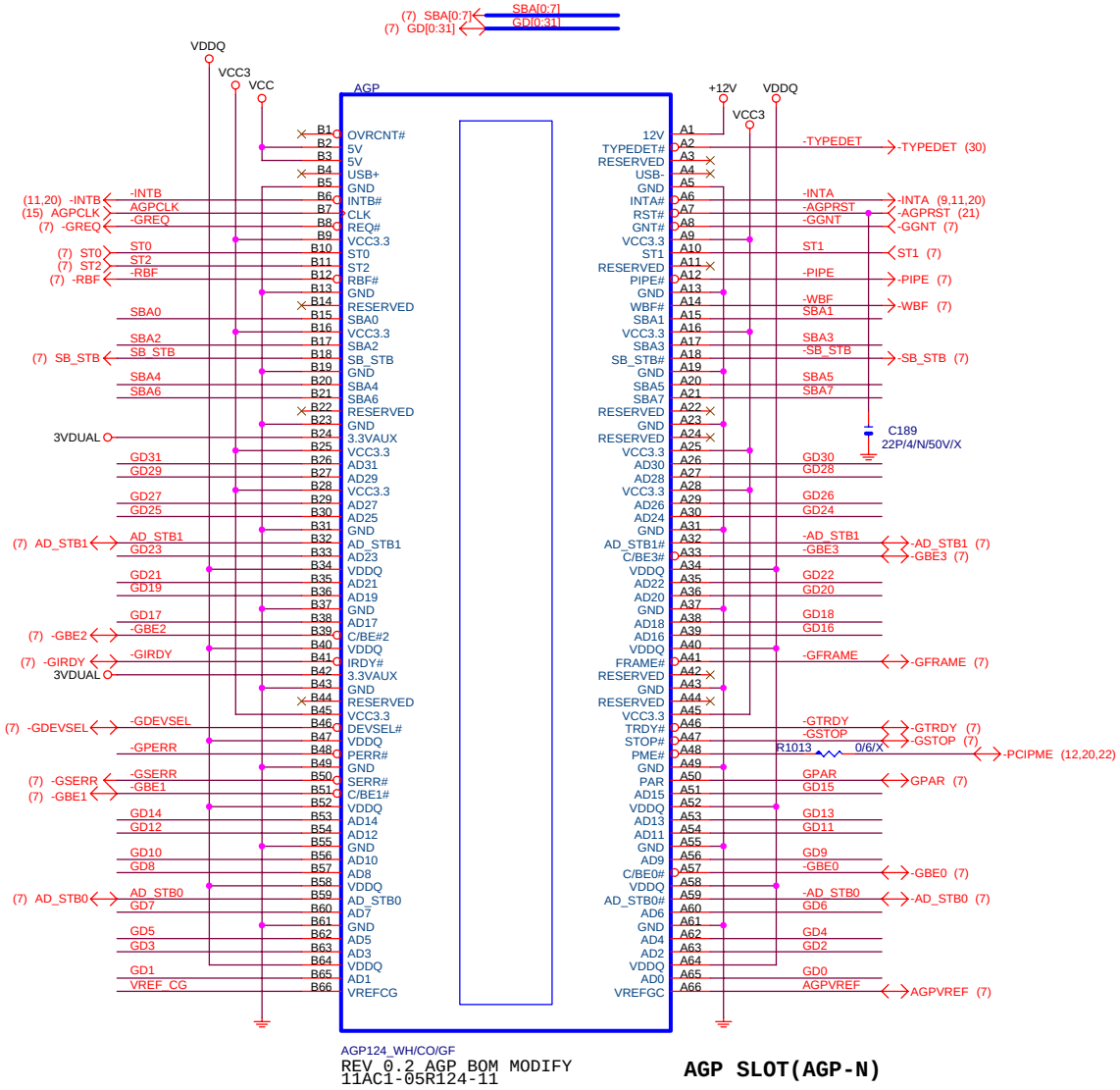


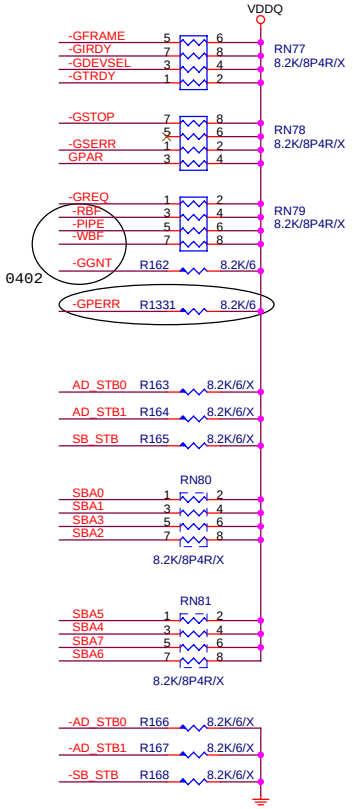
GIGABYTE

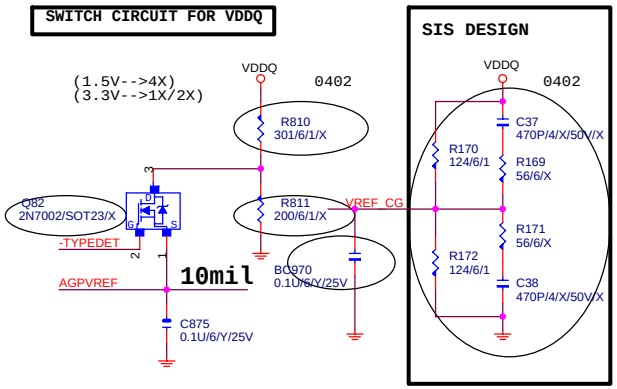
Title: DDR UNBUFFERED 3

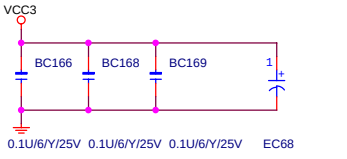
Size: Custom | Document Number: 8S651MP-RZ | Rev: 1.0

Date: 星期一, 八月 16, 2004 | Sheet 17 of 32



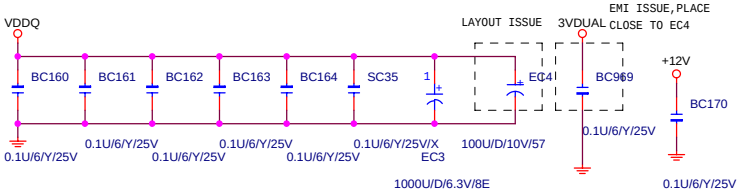






Place 1 at each pair of 3.3V pins

Decoupling capacitors
(Place near AGP slot)



Place 1 at each pair of VDDQ pins

Place an additional for spread from A14 - A33

GIGABYTE		
Title: AGP SLOT		
Size: Custom	Document Number: 8S651MP-RZ	Rev: 1.0
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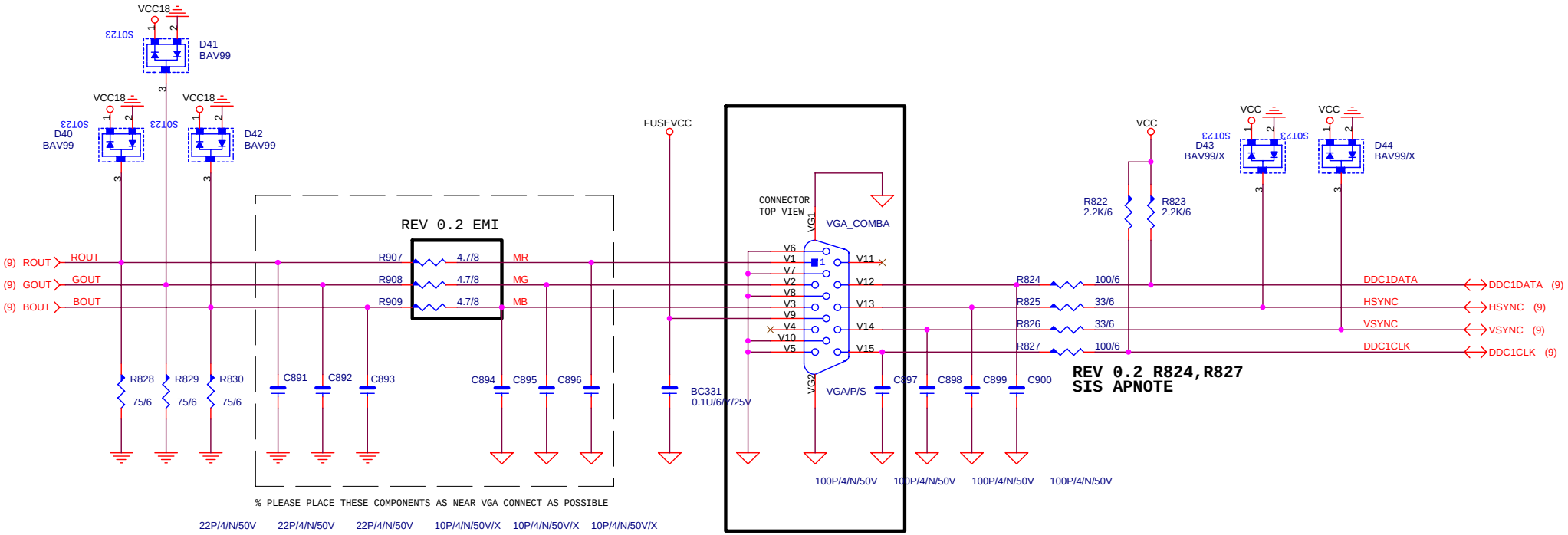
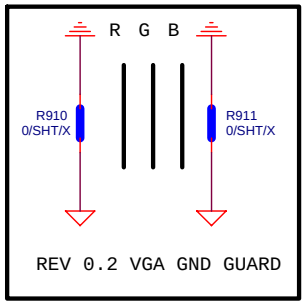
VGA CONNECTOR 1

SIS 645DX NO POP



DUAL LAYOUT(VGA/COM)

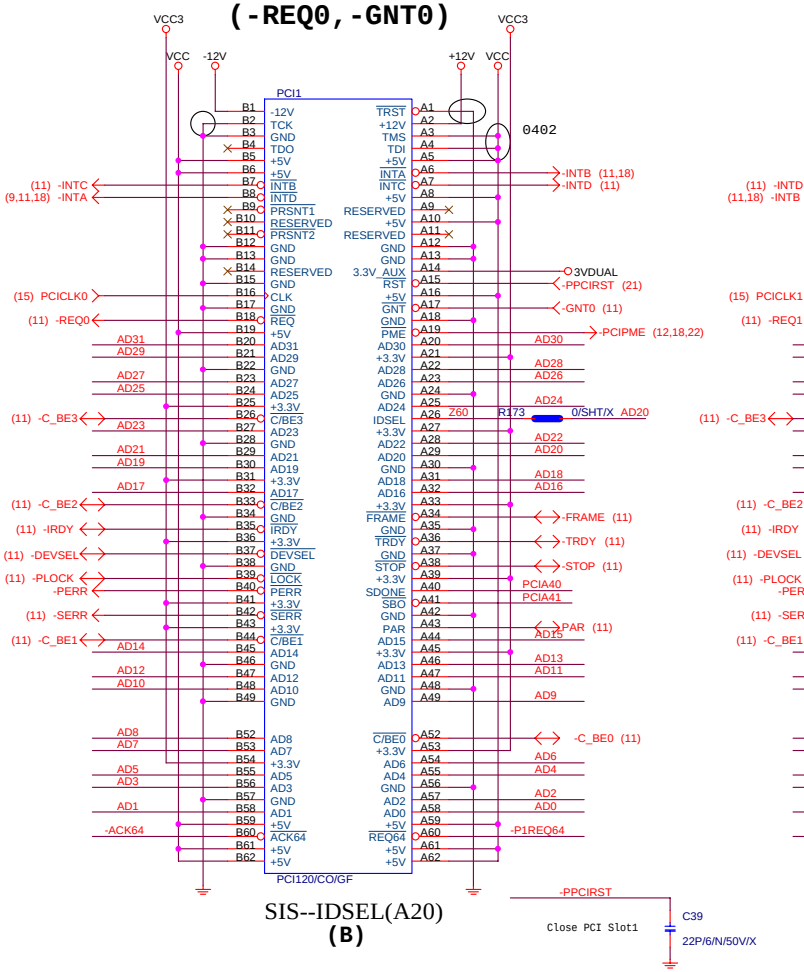
REV 0.2 R824,R827 SIS APNOTE



GIGABYTE		
Title: VGA CONNECTOR		
Size: B	Document Number: 8S651MP-RZ	Rev: 1.0
Date: 星期一, 八月 16, 2004	Sheet 19 of 32	

PCI SLOT 1,2,3

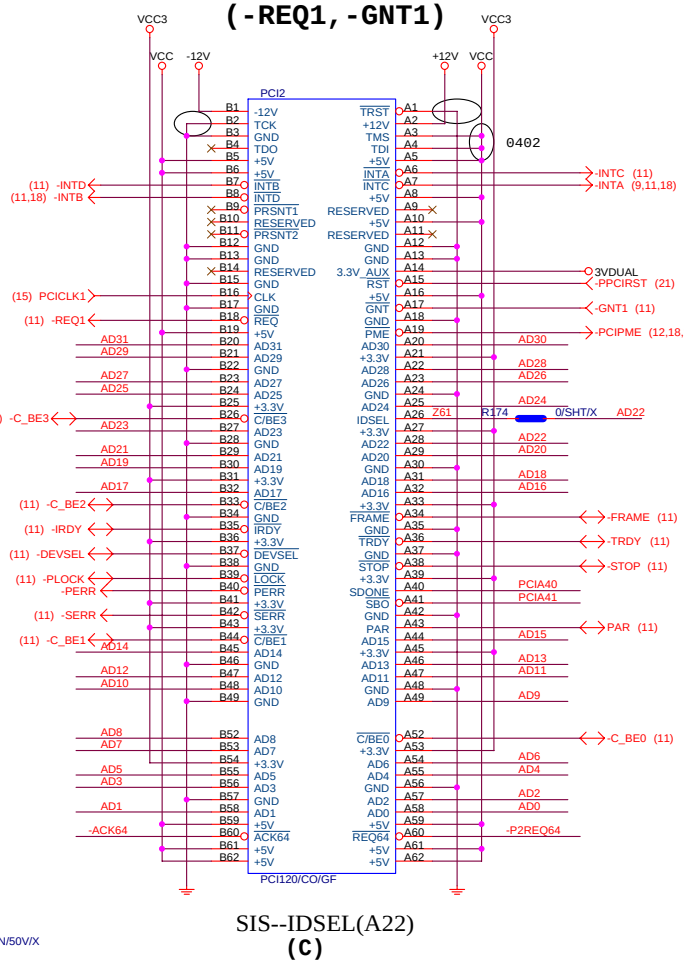
PCI SLOT1 (-REQ0,-GNT0)



SIS--IDSEL(A20)

(B)

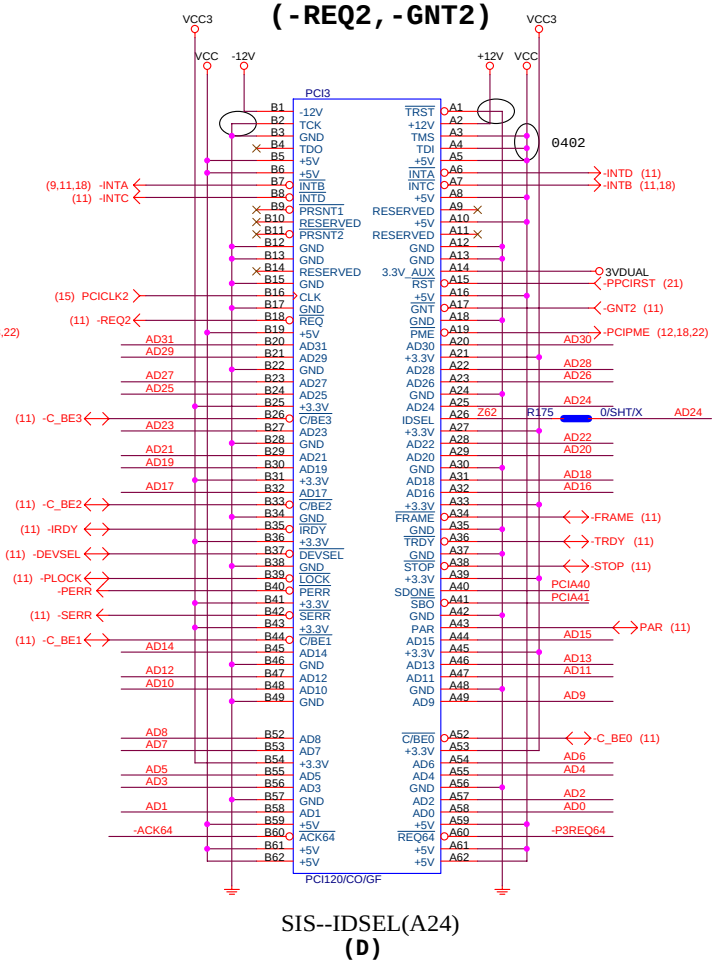
PCI SLOT2 (-REQ1,-GNT1)



SIS--IDSEL(A22)

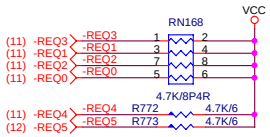
(C)

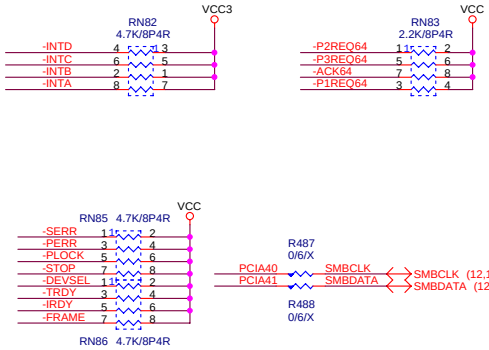
PCI SLOT3 (-REQ2,-GNT2)

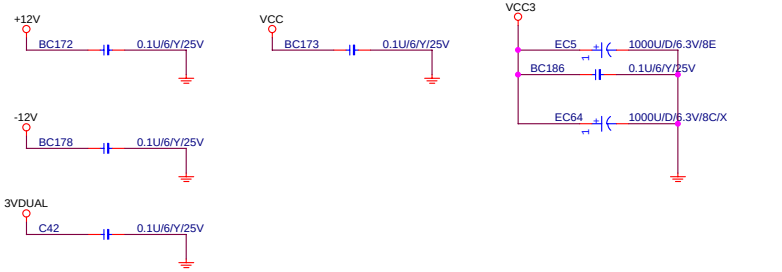


SIS--IDSEL(A24)

(D)







GIGABYTE		
Title	PCI SLOT 1,2,3	
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PRIMARY IDE

10/29

(11) PDD[0..15]

PDD14 PDD1 PDD15 PDD13 PDD2 PDD0 PDD4 PDD5 PDD7 PDD9 PDD10 PDD11 PDD8 PDD12 PDD3 PDD6

(11) PDDREQ → PDDREQ
(11) -PDIOW → -PDIOW
(11) -PDIOR → -PDIOR
(11) PIORDY → PIORDY
(11) -PDDACK → -PDDACK
(11) IRQ14 → IRQ14

(11) PDA0 → PDA0
(11) PDA1 → PDA1
(11) PDA2 → PDA2
(11) -PDCS1 → -PDCS1
(11) -PDCS3 → -PDCS3

IDE1

R191 1K/6 -IDERST
R192 5.6K/6 PDDREQ
R193 4.7K/6 -PDIOW
R195 10K/6/X -PDIOR
R784 10K/6 PIORDY
R196 1K/6 -PDDACK
IRQ14
PDA1
PDA0
-PDCS1
Z0
HDLED-
(28) HDLED-
D5 1N4148/S
BX2x20/20/B

PDD8 PDD9 PDD10 PDD11 PDD12 PDD13 PDD14 PDD15
PDA2
-PDCS3
CSEL_1
R194 470/6
P66DET (11)
C46 0.047U/4/X/10V

NF --REV 0.2 IDE1-->BLUE

11/17 MEMO131

Dual Layout with Q12,Q13,...

VCC VCC3
R1250 0/6/X
R1251 0/6/SHT/X
BC462 0.1U/6

U60
-PCIRST
R1252 0/6/X
Z64
-PPCIRST
R1253 0/6/X
-AGPRST
VCC
GND
74HC14
-PWOK
PWOK
R1254 330/6
(12,15,28,29) PWROK

PWOK PWOK (23,28,29,31)
-AGPRST -AGPRST (18)
-PWOK -PWOK
PWROK R1255 0/6/X PWROK_NB

SECONDARY IDE

10/29

(11) SDD[0..15]

SDD0 SDD15 SDD1 SDD14 SDD8 SDD2 SDD4 SDD7 SDD6 SDD9 SDD10 SDD11 SDD12 SDD3 SDD5 SDD13

(11) SDDREQ → SDDREQ
(11) -SDIOW → -SDIOW
(11) -SDIOR → -SDIOR
(11) SIORDY → SIORDY
(11) -SDDACK → -SDDACK
(11) IRQ15 → IRQ15

(11) SDA0 → SDA0
(11) SDA1 → SDA1
(11) SDA2 → SDA2
(11) -SDCS1 → -SDCS1
(11) -SDCS3 → -SDCS3

IDE2

R199 1K/6 -IDERST
R201 5.6K/6 SDDREQ
R202 4.7K/6 -SDIOW
R204 10K/6/X -SDIOR
R785 10K/6 SIORDY
R205 1K/6 -SDDACK
IRQ15
SDA1
SDA0
-SDCS1
Z1
HDLED-
D6 1N4148/S
BX2x20/20/B

SDD8 SDD9 SDD10 SDD11 SDD12 SDD13 SDD14 SDD15
SDA2
-SDCS3
CSEL_2
R203 470/6
S66DET (11)
C47 0.047U/4/X/10V

SIRQ

S_IRQ
(12,22) SERIRQ
SERIRQ
SIRQ1x2/O/X

FRONT SIDE USB1

EGND FOR EMI

USB2.0

INTEL CONN F_USB

10/29

FUSEVCC
EC7 100U/D/10V/57
EGND
F_USB1
L8
USBDT1- USBDT1+ FUSB1- FUSB1+
USBDT4- USBDT4+ FUSB4- FUSB4+
OD6560T/X
FUSB1- FUSB1+ FUSB4- FUSB4+ -USBOC1
EGND
PHX2x5/9/BLACK

(13) USBDT1- (13) USBDT1+ (13) USBDT4- (13) USBDT4+
RN181
0/8P4R/SHT/X

-USBOC1 R1022 0/6/X -USBOC (13,27)

FRONT SIDE USB2

EGND FOR EMI

USB2.0

INTEL CONN F_USB

10/29

FUSEVCC
EC55 100U/D/10V/57
EGND
F_USB2
L9
USBDT2- USBDT2+ FUSB2- FUSB2+
USBDT5- USBDT5+ FUSB5- FUSB5+
OD6560T/X
FUSB2- FUSB2+ FUSB5- FUSB5+ -USBOC1
EGND
PHX2x5/9/BLACK

(13) USBDT2- (13) USBDT2+ (13) USBDT5- (13) USBDT5+
RN180
0/8P4R/SHT/X

FUSEVCC,GAMEVCC

5VDUAL
80mil
F1 24251/D 2.5A/16V
FUSEVCC
FB42 100/12.5/D
80mil
GAMEVCC +12V
20mil
R963 1K/6
Q100 S0T23
2N7002/SOT23
BC351 0.1U/6/Y/25V
BC350 0.1U/6/Y/25V
EMI

PCI+IDE RESET

R179 0/6/X
VCC
R176 1K/6/X
R177 470/6/X
R178 10K/6/X
(9,11,22) -PCIRST
Z63
S0T23
Q12 MMBT2222A/SOT23/X
Z64
R506 220/6/X
Z238
Q13 MMBT2222A/SOT23/X
-PPCIRST
(20) -PPCIRST

11/17 MEMO131

TO PCI 1, 2, 3 SLOT

R178, R179 close source side

11/17 MEMO131

VCC3
R1256 1K/6
PWROK_NB (9)
R1257 8.2K/6/X
R1258 8.2K/6
-PWOK
Q118 MMBT2222A/SOT23
C300 0.01U/6/Y/50V/X

For Samsung DDR333 Reset several times can't boot issue.

11/19
R206 1K/6
Q14 MMBT2222A/SOT23
Z239
R208 8.2K/6
-IDERST

GIGABYTE

Title: IDE, USB

Size: Custom | Document Number: 8S651MP-RZ | Rev: 1.0

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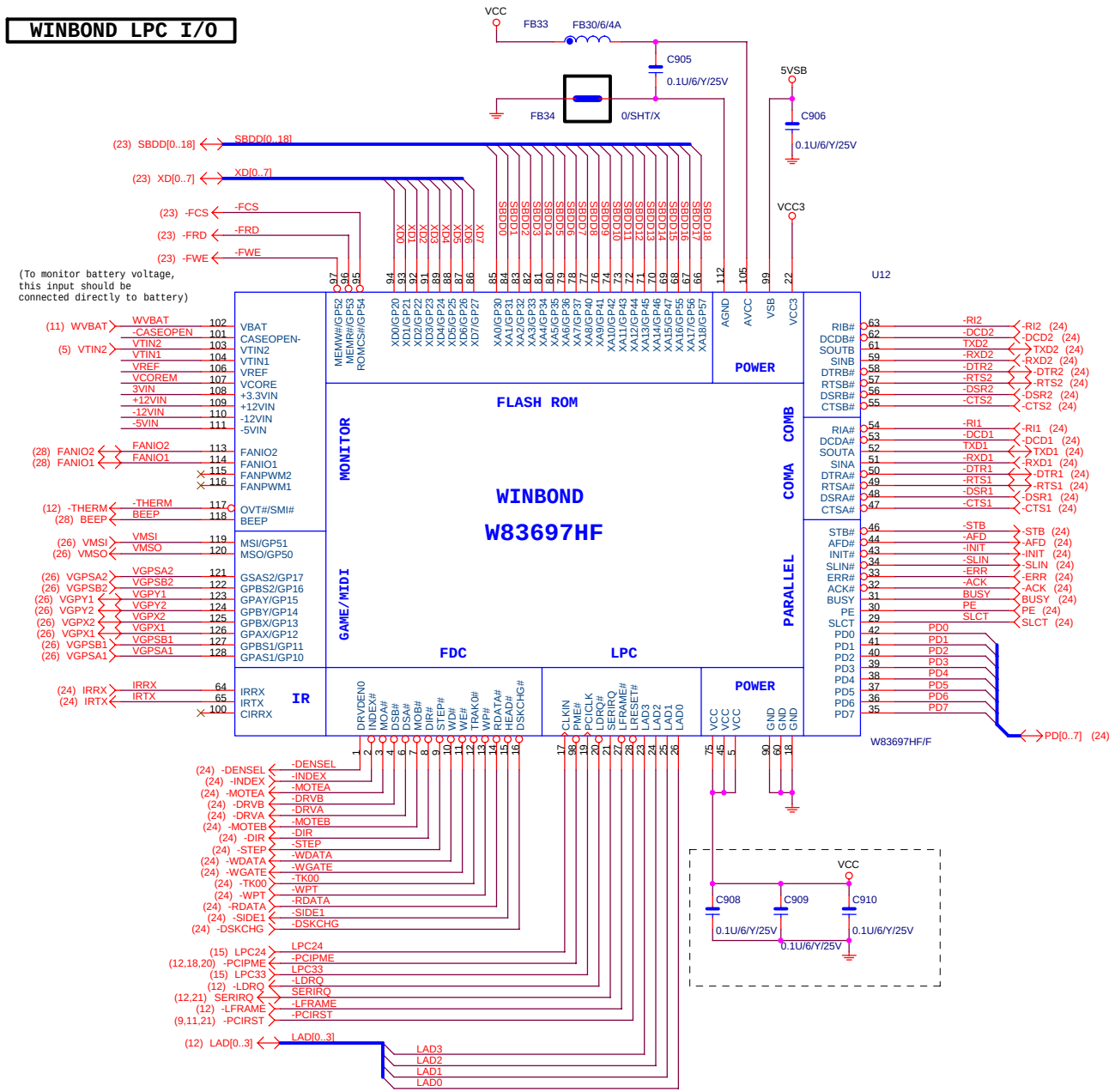
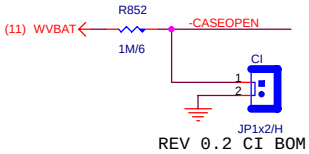
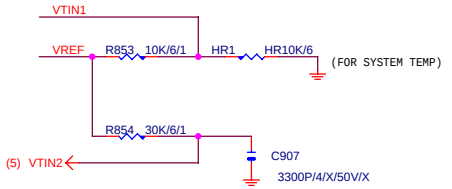
WINBOND LPC I/O



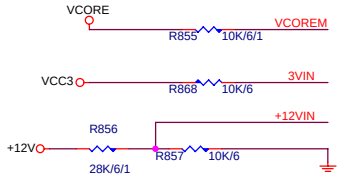


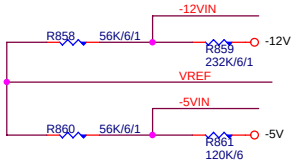
REV 0.2 CI BOM MODIFY

Case Open Circuits



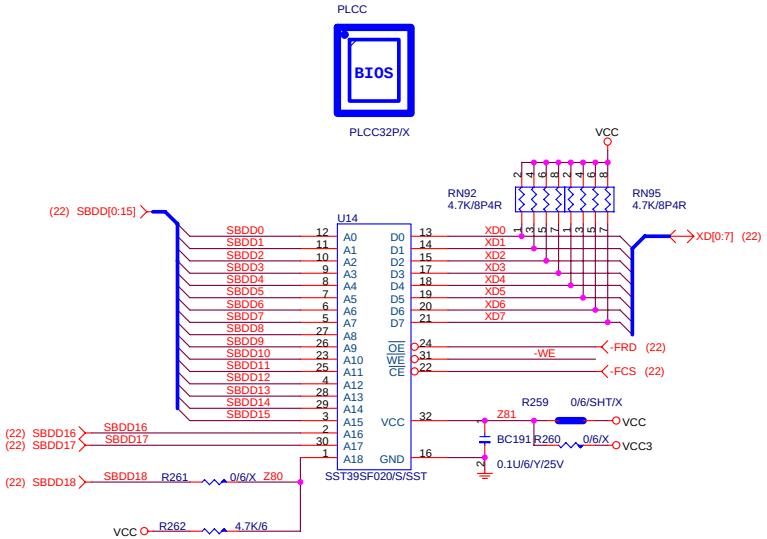
Thermal Monitoring

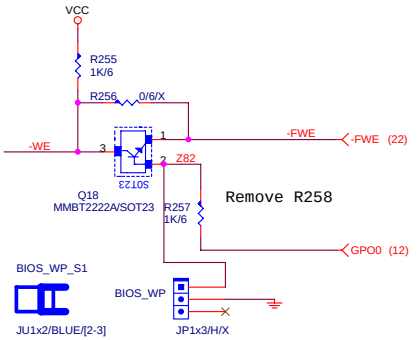




Voltage Monitoring

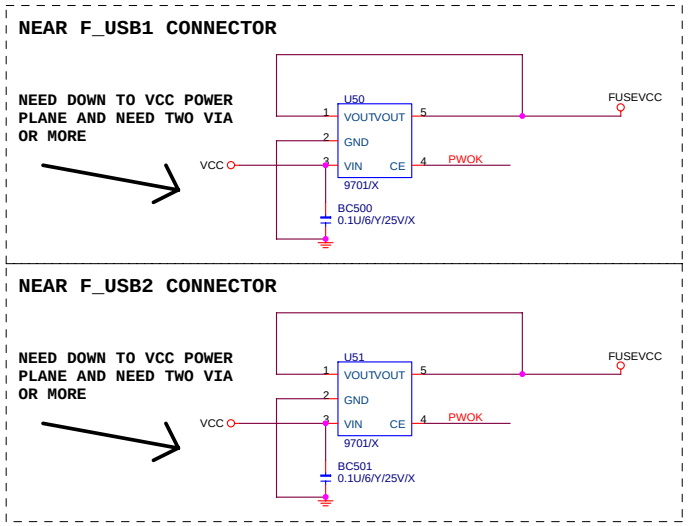
GIGABYTE		
Title: LPC W83697		
Size: Custom	Document Number: 8S651MP-RZ	Rev: 1.0
Date: 星期一, 八月 16, 2004	Sheet 22 of 32	

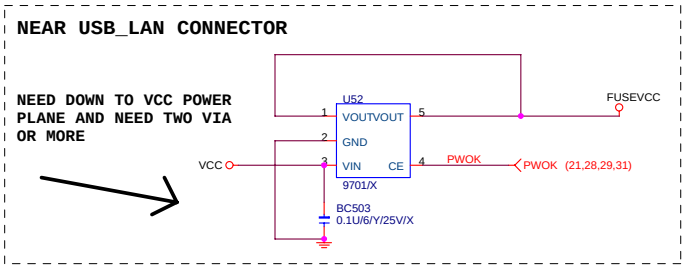




BIOS_WP: BIOS WRITE PROTECT

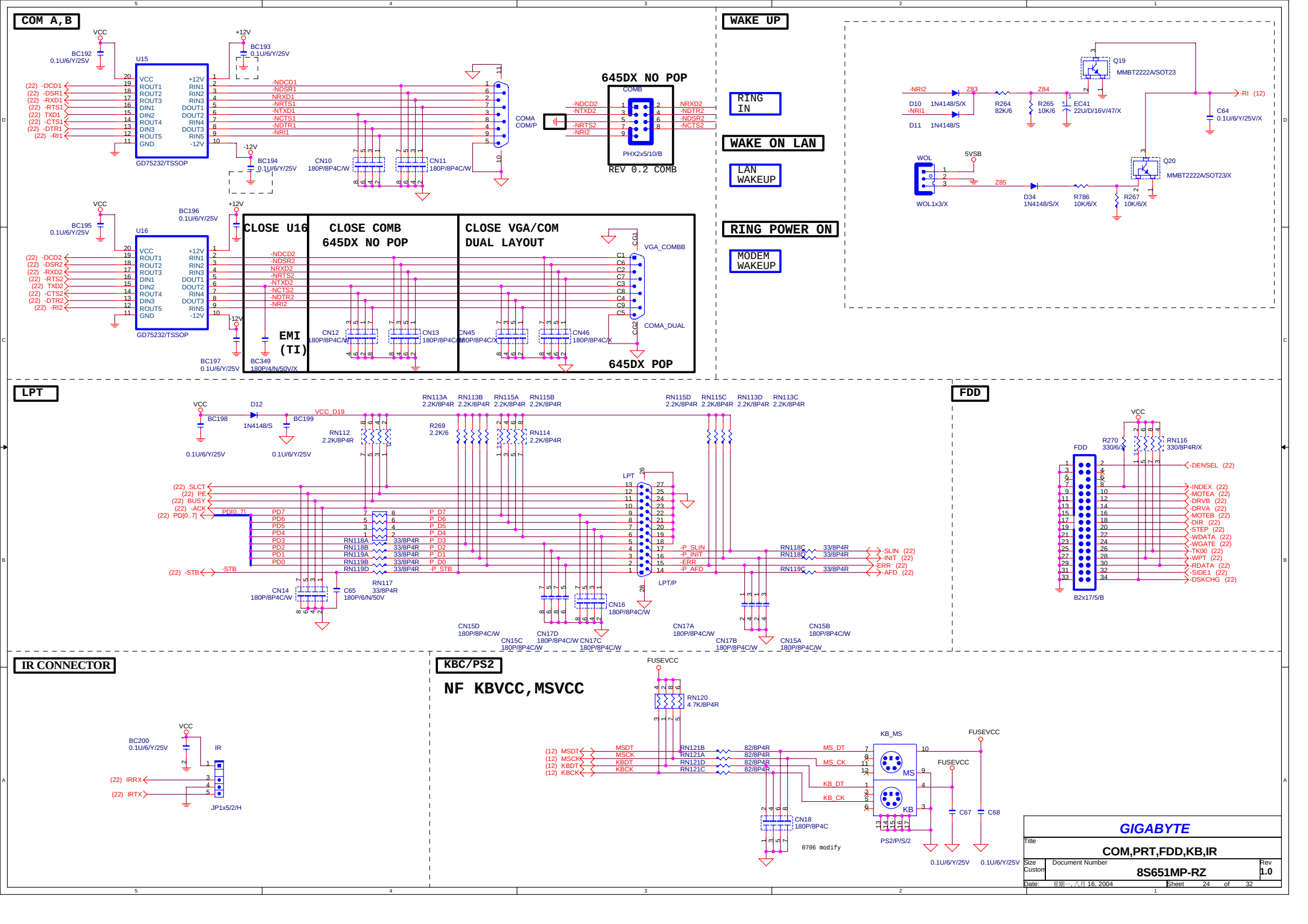
PIN	BIOS_WP
1-2	WRITE PROTECT
2-3	WRITE ENABLE (default)





GIGABYTE

Title: Flash ROM		
Size: Custom	Document Number: 8S651MP-RZ	Rev: 1.0
Date: 星期一, 八月 16, 2004	Sheet 23 of 32	


COM A,B
U15
GD75232/TSSOP
BC192 0.1U/6/Y/25V
BC193 0.1U/6/Y/25V
BC194 0.1U/6/Y/25V
CN10 180P/8P4C/W
CN11 180P/8P4C/W
COMA
COM/P
645DX NO POP
COMB
PHX2x5/10/B
REV 0.2 COMB
U16
BC195 0.1U/6/Y/25V
BC196 0.1U/6/Y/25V
BC197 0.1U/6/Y/25V
BC349 180P/4/N/50V/X
EMI (TI)
CLOSE U16
CLOSE COMB 645DX NO POP
CLOSE VGA/COM DUAL LAYOUT
CN12 180P/8P4C/W
CN13 180P/8P4C/W
CN45 180P/8P4C/X
CN46 180P/8P4C/X
VGA_COMBB
COMA_DUAL
645DX POP
WAKE UP
RING IN
WAKE ON LAN
LAN WAKEUP
RING POWER ON
MODEM WAKEUP
Q19 MMBT2222A/SOT23
Q20 MMBT2222A/SOT23/X
D10 1N4148/S/X
D11 1N4148/S
D34 1N4148/S/X
R264 82K/6
R265 10K/6
R786 10K/6/X
R267 10K/6/X
EC41 22U/D/16V/47/X
C64 0.1U/6/Y/25V/X
WOL1x3/X
LPT
RN112 2.2K/8P4R
RN113A 2.2K/8P4R
RN113B 2.2K/8P4R
RN115A 2.2K/8P4R
RN115B 2.2K/8P4R
RN114 2.2K/8P4R
RN115D 2.2K/8P4R
RN115C 2.2K/8P4R
RN113D 2.2K/8P4R
RN113C 2.2K/8P4R
R269 2.2K/6
RN117 33/8P4R
RN118A 33/8P4R
RN118B 33/8P4R
RN119A 33/8P4R
RN119B 33/8P4R
RN119D 33/8P4R
RN118C 33/8P4R
RN118D 33/8P4R
RN119C 33/8P4R
CN14 180P/8P4C/W
C65 180P/6/N/50V
CN16 180P/8P4C/W
CN15D 180P/8P4C/W
CN15C 180P/8P4C/W
CN17D 180P/8P4C/W
CN17C 180P/8P4C/W
CN17A 180P/8P4C/W
CN17B 180P/8P4C/W
CN15A 180P/8P4C/W
CN15B 180P/8P4C/W
LPT/P
FDD
R270 330/6/X
RN116 330/8P4R/X
B2x17/5/B
IR CONNECTOR
BC200 0.1U/6/Y/25V
JP1x5/2/H
KBC/PS2
NF KBVCC,MSVCC
RN120 4.7K/8P4R
RN121B 82/8P4R
RN121A 82/8P4R
RN121D 82/8P4R
RN121C 82/8P4R
CN18 180P/8P4C
0706 modify
KB_MS
MS
KB
PS2/P/S/2
C67
C68
GIGABYTE
Title
COM,PRT,FDD,KB,IR
Size Custom
Document Number
8S651MP-RZ
Rev 1.0
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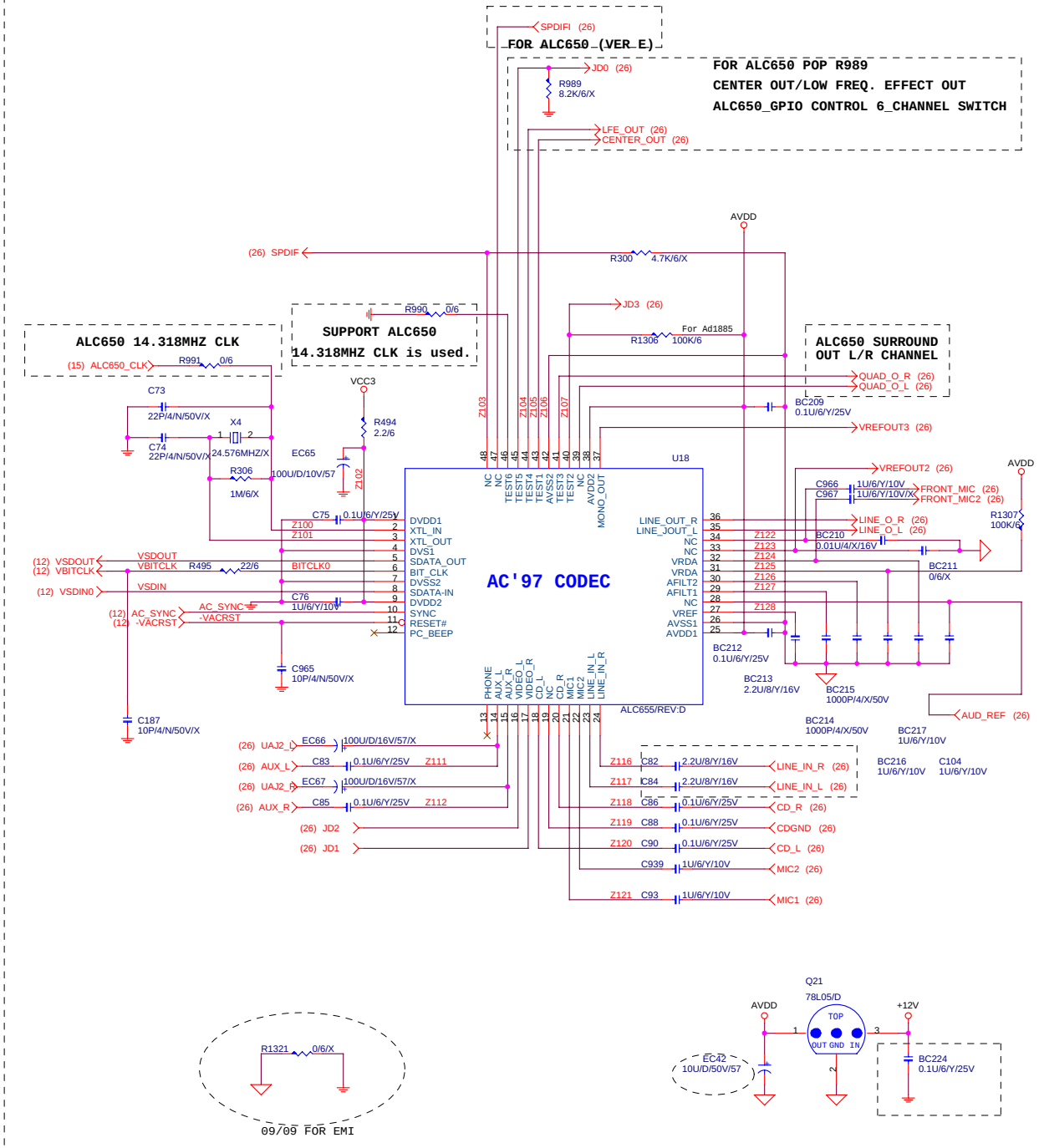

NF	SIGMATEL9756
Disti	ALC201A

GIGABYTE

Title: AUDIO (AC97 CODEC)

Size: Custom | Document Number: 8S651MP-RZ | Rev: 1.0

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SPDIF

SPDIF_IO

FUSEVCC
SPDIF_IO
(25) SPDIF
SPDIFI (25)
PIN2X3-CUT2/BLACK

LINE OUT

EC8,9,10,11不可DUAL LAYOUT

FLOR
SUR_OUTR R992 0/6
(25) JD1
R1294 8.2K/6/X
C961
4.7U/8/Y/10V/X
EC8 100U/D/10V/57
(25) QUAD_O_R R993 0/6/X
LNR
LNL
EC9 100U/D/10V/57
(25) LINE_O_R R994 0/6 R914 0/6/X
EC10 100U/D/10V/57
(25) LINE_O_L R995 0/6 R917 0/6/X
EC11 100U/D/10V/57
(25) QUAD_O_L R996 0/6/X
SUR_OUTL R997 0/6
AUDIO_1A
R1295 22K/6/X
R1296 22K/6/X
C97
C98
1000P/4/X/50V
1000P/4/X/50V
3RJ+15FEMALE
LINE OUT
FLOL
(25) VREFOUT3
D64 1N4148/S/X

LINE-IN

(25) JD2
R1297 8.2K/6/X
C962
4.7U/8/Y/10V/X
(25) UAJ2_R
(25) LINE_IN_R R327 0/6
(25) LINE_IN_L R330 0/6
AUDIO_1B
(25) UAJ2_L
(25) VREFOUT2
R529 22K/6/X
R530 22K/6/X
C102 1000P/4/X/50V
C103 1000P/4/X/50V
3RJ+15FEMALE
LINE-IN
D65 1N4148/S/X

SUR_CEN
SUR_OUTL
SUR_OUTR
(25) CENTER_OUT
LFE_OUT (25)
C940 1U/6/Y/10V
H2X3/4/H
C941 1U/6/Y/10V

INTEL FRONT AUDIO

(25) FRONT_MIC
CR44 0/6S/X
MIC CR45 0/6/X
CR60 0/6/X
AVDD
CBC49 0.1U/6/Y/25V/X
F_AUDIO
AVDD
CR40 8.2K/6
CBC50 0.1U/6/Y/25V/X
FLOR
FLOL
KEY
LNR
LNL
VREFOUT3 (25)
(25) JD3
CR57 0/6/X
(25) VREFOUT2
CR47 22/SHT/X
CR46 22/SHT/X
H2X5/-8/Black
R1308 0/6/X
(25) UAJ2_L
(25) JD2
CR58 0/6/X
(25) UAJ2_R
C968 1000P/4/X/50V/X
R1310 22K/6/X
Not Drill on pin8
(25) FRONT_MIC2

F_AUDIO_S1
F_AUDIO_S2
JU1x2/B/[5-6]
JU1x2/B/[9-10]

MIC

ONLY ALC650 FOR LFE OUTPUT POP R

(25) MIC2
C942 1000P/4/X/50V/X
R1309 22K/6/X
AVDD
R335 1K/6/X
(25) JD0
R1300 8.2K/6/X
C963
4.7U/8/Y/10V/X
C105 1U/6/Y/10V
R1301 4.7K/6/X
(25) AUD_REF
C964 0.1U/6/Y/25V
R336 10K/6/X
R337 2.2K/6
AUDIO_1C
Z137
(25) MIC1
R339 0/6
C181 0.01U/4/X/16V
MIC
C944 1000P/4/X/50V
EMI
0703 MODIFY
R1311 22K/6/X
3RJ+15FEMALE
MIC

AUX IN

DISTI DEFAULT NO POP

AUX_IN
(25) AUX_L
(25) AUX_R
C108 1000P/4/X/50V/X
C109 1000P/4/X/50V/X
WF1x4/W/X

CD IN

CD_IN
(25) CD_L
(25) CD_R
(25) CDGND
C182
C110
C111
WF1x4/B
1000P/4/X/50V
1000P/4/X/50V
1000P/4/X/50V

GAME PORT

FOR I/O W83697HF

GAMEVCC
R344 4.7K/6/X
R345 4.7K/6/X
RN126 2.2K/8P4R
GAME-1
(22) VGPSA1 VGPSA1
(22) VGPSB1 VGPSB1
(22) VGPX1 VGPX1
(22) VGPX2 VGPX2
(22) VMSO VMSO
(22) VGPY2 VGPY2
(22) VGPY1 VGPY1
(22) VGPSB2 VGPSB2
(22) VGPSA2 VGPSA2
(22) VMSI VMSI
RN129C 0/8P4R/SHT/X
RN129D 0/8P4R/SHT/X
RN130A 2.2K/8P4R
RN130C 2.2K/8P4R
R346 2.2K/6
RN130D 2.2K/8P4R
RN130B 2.2K/8P4R
RN129B 0/8P4R/SHT/X
RN129A 0/8P4R/SHT/X
R347 2.2K/6
GP_SA1
GP_SB1
GP_X1
GP_X2
MS_0
GP_Y2
GP_Y1
GP_SB2
GP_SA2
MS_I
RN174 1M/8P4R
C114 0.01U/6/X/50V
C116 100P/6/N/50V/X
C118 0.01U/6/X/50V
C115 0.01U/6/X/50V
C117 0.01U/6/X/50V
C121 1000P/6/X/50V
C122 180P/6/N/50V
C123 180P/6/N/50V
CN19 180P/8P4C
CN20 0.01U/8P4C
BC230 0.1U/6/Y/25V
AD/GM
BC228 0.1U/6/Y/25V
BC229 0.1U/6/Y/25V

GIGABYTE		
Title	AUDIO OUTPUT,GAME PORT	
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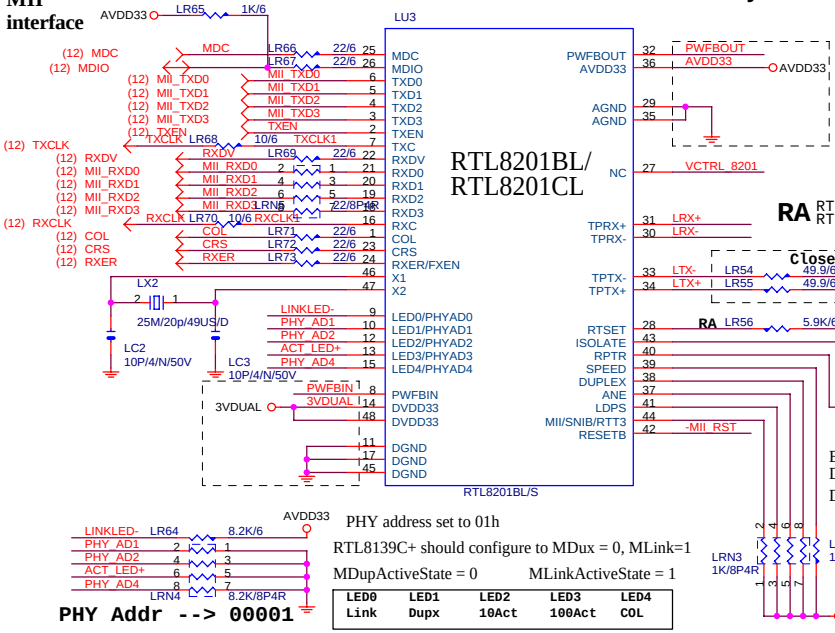
Connect to MII interface

RTL8201BL/ RTL8201CL Co-Layout



RA RTL8201BL:5.9K/6/1
RTL8201CL:2.0K/6/1

Close to RTL8201

Enable: N-way, Full duplex, 100Mbps, Link Down Power Saving

Disable: Isolate, Repeater Mode

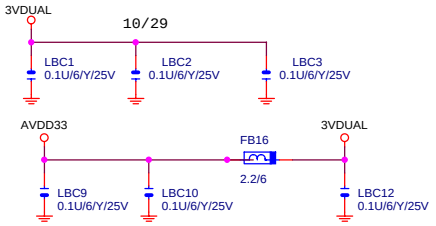
PHY address set to 01h

RTL8139C+ should configure to MDux = 0, MLink=1

MDupActiveState = 0 MLinkActiveState = 1

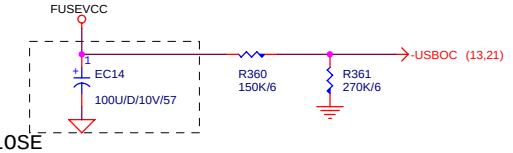
LED0	LED1	LED2	LED3	LED4
Link	Dupx	10Act	100Act	COL

PHY Addr --> 00001

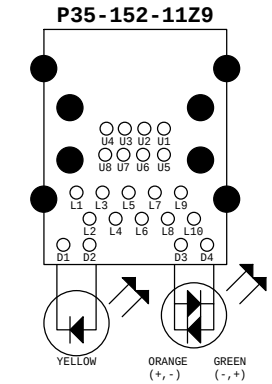


USB2.0

REAR USBX2

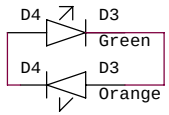


EC CLOSE
USB_PORT(FUSEVCC)

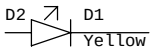


	Link(Speed) (Link to Hub)	Active (Data Transmit)
10Mb	Green(ON)	Yellow(Blink)
100Mb	Green(ON)	Yellow(Blink)
1Gb	--	--

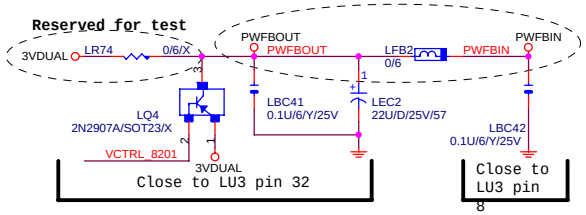
Dual Color LED

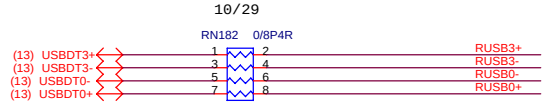


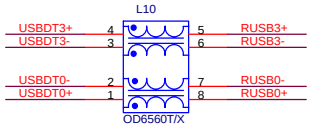
Single Color LED

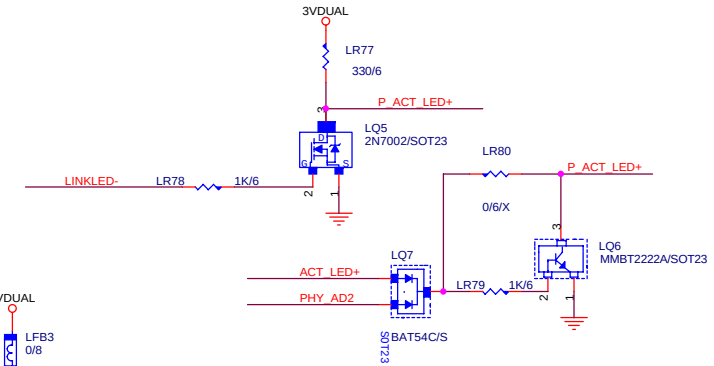


Reserved for test

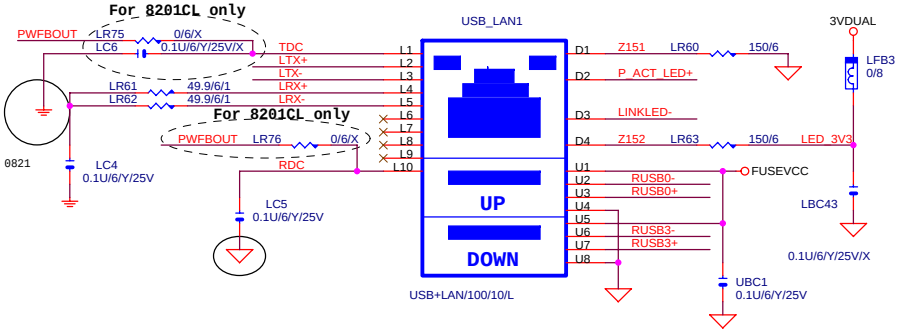








For 8201CL only



Place decoupling capacitor DC1~DC5 as close as possible to each power pin

BLOCK A : The components inside BLOCK A are reserved for RTL8201B(.25u version). In RTL8201B, DVDD0 and AVDD0 will be fed 2.5V produced by BLOCK A which is functional as linear regulator and L3, R6 will be removed. In order to be layout-compatible between RTL8201 and RTL8201B, please reserve the component space and pads in your layout for future extension.

GIGABYTE

Title	LAN RTL8101L	
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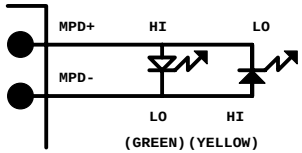
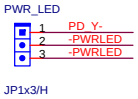
FRONT PANEL



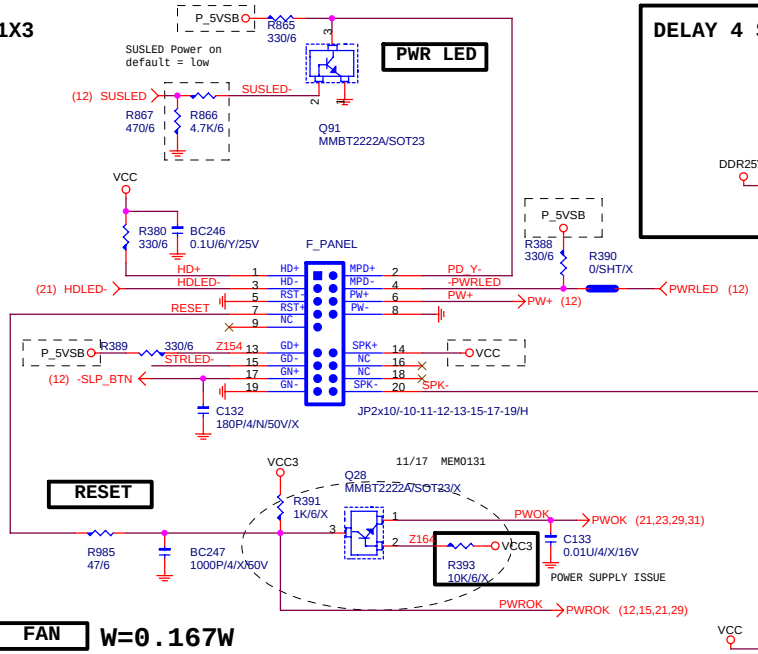
PWR_LED FOR DISTI PIN 1X3 LED USED

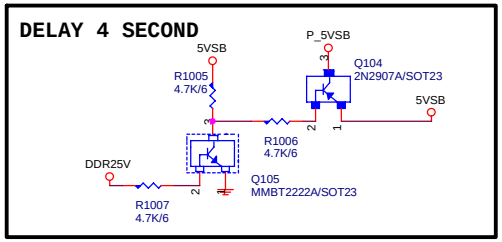


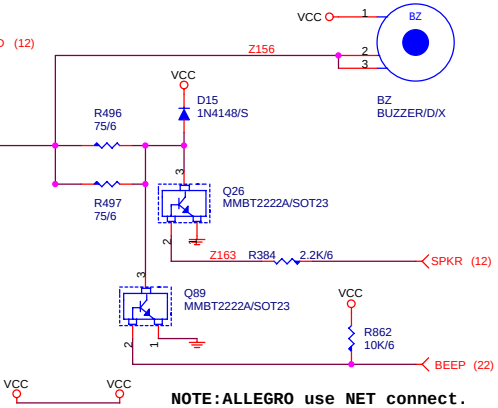
LED States	ACPI States	MPD+	MPD-
OFF	S1,S3,S5	HI	HI
Steady Green	S0	HI	LO
Blinking Green	S0(message waiting)	HI	BLINKING

States for a dual-color power LED

LED States	ACPI States	MPD+	MPD-
OFF	S5	HI	HI
Steady Green	S0	HI	LO
Blinking Green	S0(message waiting)	HI	BLINKING
Steady Yellow	S1,S3	LO	HI
Blinking Yellow	S1,S3(message waiting)	LO	BLINKING

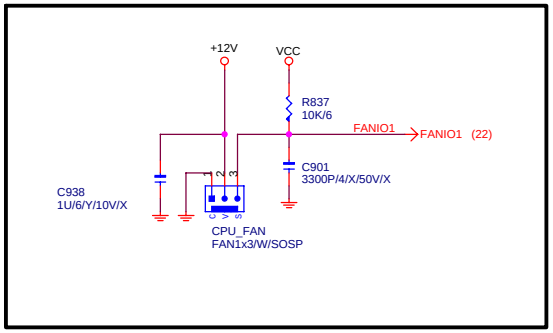


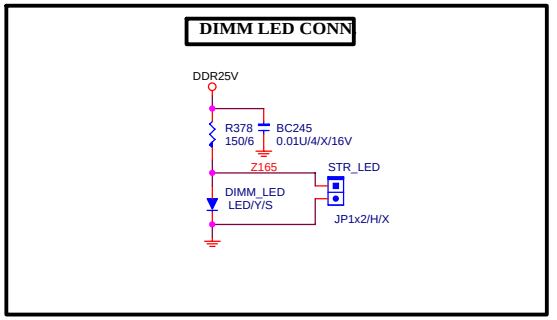


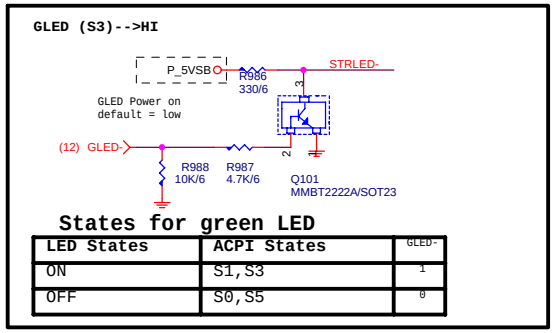


NOTE:ALLEGRO use NET connect.

CPU FAN W=0.167W



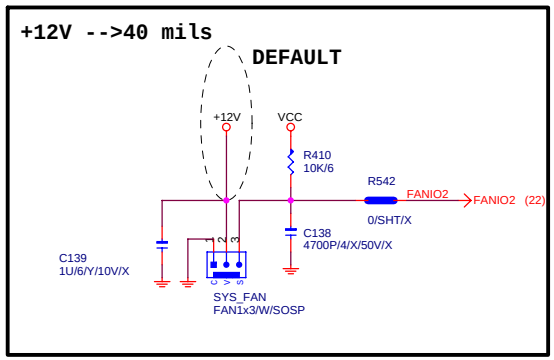




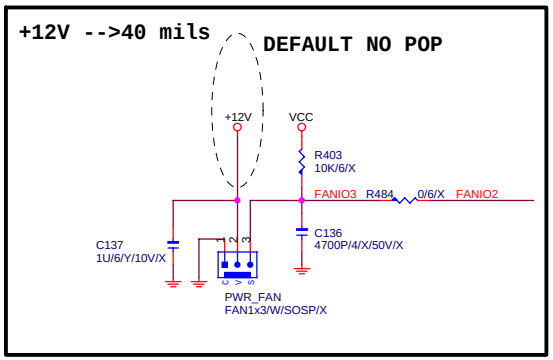
States for green LED

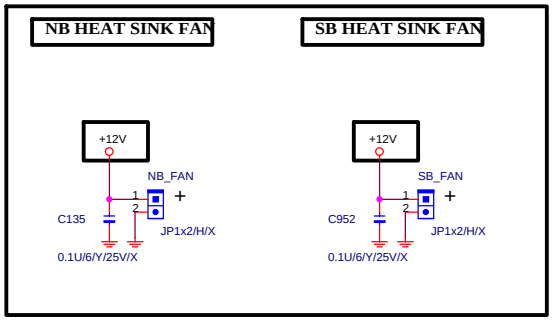
LED States	ACPI States	GLED-
ON	S1,S3	1
OFF	S0,S5	0

SYSTEM FAN W=0.167W



POWER FAN W=0.167W





GIGABYTE

Title: PANEL, STR LED & FANS

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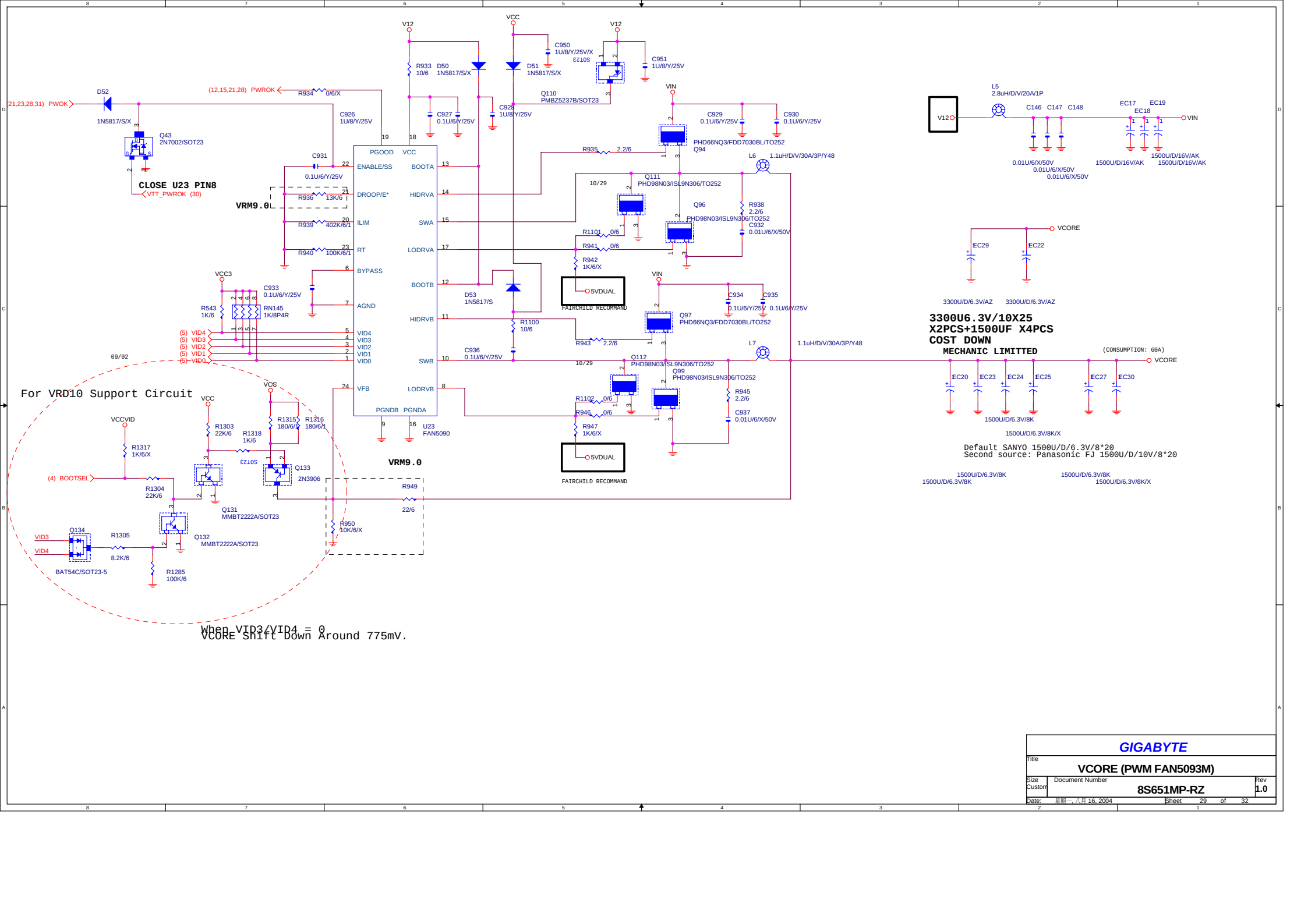

GIGABYTE

Title: VCORE (PWM FAN5093M)

Size: Custom | Document Number: 8S651MP-RZ | Rev: 1.0

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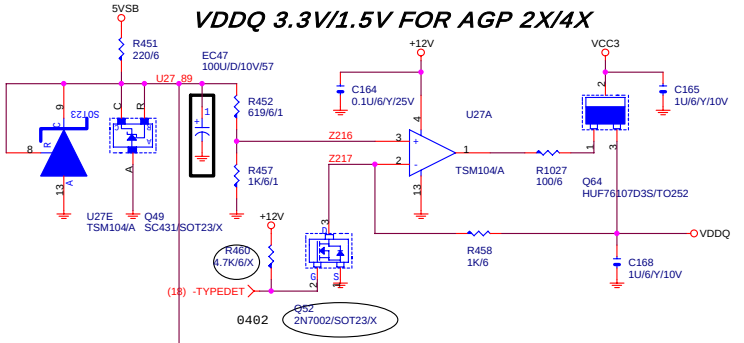
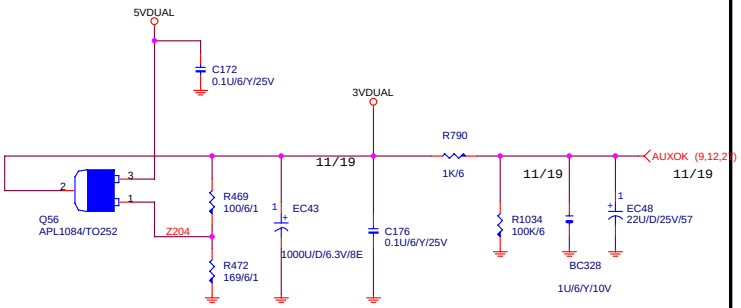
VDDQ 3.3V/1.5V FOR AGP 2X/4X

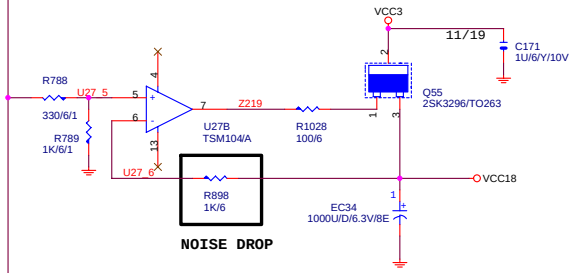


5VDUAL TRANS TO 3VDUAL(3.3V)

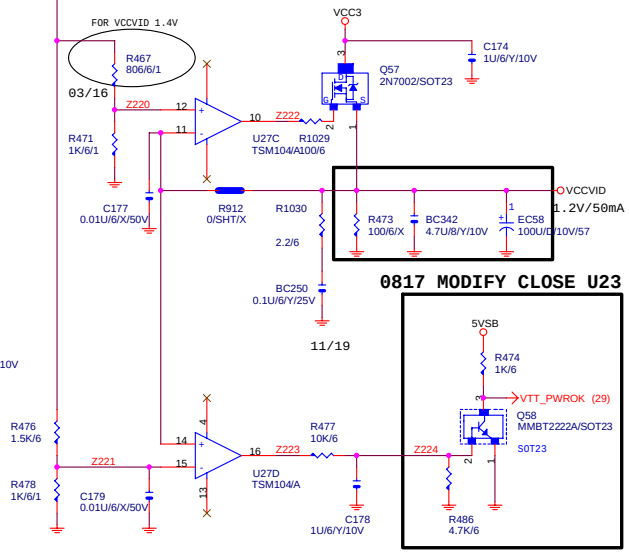
5VDUAL 80 mils ABOVE



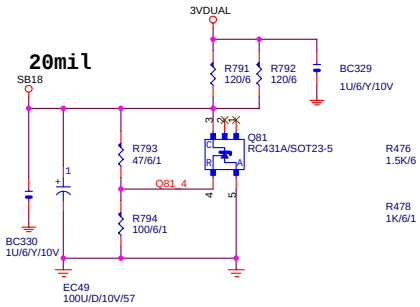
VCC18 FOR NB,SB



VCCVID FOR NORTHWOOD CPU



SB18 FOR SB



GIGABYTE		
Title	DC POWER	
Size: Custom	Document Number: 8S651MP-RZ	Rev: 1.0
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ATX CON, DDR POWER

Default應該由3VDUAL轉DDR25V,因改舊版無法把5VDUAL及3VDUAL的MOS靠近DDR，故另加兩個DIODE作出3VDUAL1。

VCC3 VCC3 3VDUAL
6 VIA
D61 1N5820/S/X D20 1N5820/S RN137 4.7/8P4R D21 1N5817/S
Z214

10/29

3VDUAL1
BC952 0.1U/6/Y/25V/X
DDR25V with over-current protect.
DDR25V
6 VIA
DIP Cap. at other page
Q119 APM3055/TO252
R1273 100/6/SHT/X
BC961 0.01U/4/Y25V/X

5VSB
BC959 1U/6/Y/10V

VCC
BC956 0.1U/6/Y/25V
Q121 HUF76107D3S/TO252
R1274 100/SHT/X
R1275 100/SHT/X

5VSB
Q120 HUF76107D3S/TO252
BC957 0.1U/6/Y/25V

U67 W83301GR
VCC 6
5V_DRV 16
5V_DLSB 15
PWOK 17
5VDLEND# 10
S3# 12
S5# 11
C1 7
C2 8
SS 18
VSS 5
STR_DRV1 20
STR_SEN1 19
STR_DRV2 1
STR_SEN2 2
STR_DRV3 3
STR_SEN3 4
CHRPMP 9
V_SET0 14
V_SET1 13

5VDUAL
(21,23,28,29) PWOK
(8) -SUSB
SLP_S5EN
Add a pull-up R
R1035 1K/6/X
EC46 1000U/D/6.3V/8E
BC954 0.01U/4/Y/25V/X
BC955 0.01U/4/Y/25V/X
BC958 0.1U/6/Y/25V
BC965 0.1U/6/Y/25V

VCC3
BC962 0.1U/6/Y/25V
Q122 APM3055/TO252
R1276 100/6/SHT/X
DDRVTT
BC963 0.01U/4/Y25V/X
Q123 APM3055/TO252
R1277 100/6/SHT/X
BC964 0.01U/4/Y25V/X

BC960 0.1U/6/Y/25V
R1278 1K/6
5VSB
R1279 1K/6
R1280 1K/6/X

Over Voltage to 2.6V
R1283 1K/6

Q125 MMBT2222A/SOT23/X
(12) OVDDR27V
R1281 8.2K/6/X
Q124 MMBT2222A/SOT23/X
(12) OVDDR26V
R1282 8.2K/6/X

-SUSB: S3=Low
-SUSB: S0,S1,S5=Hi
11/19
5VSB
R475 47K/6/X
R802
(8) -SUSB
Q60 2N7002/SOT23 8.2K/6
Z210
(21,23,28,29) PWOK
Z211
R479 47K/6
C194 1U/6/Y/10V/X
C876 1U/6/Y/10V/X
Q59 2N7002/SOT23

OVDDR267, OVDDR27V RESUME WELL DEFAULT HIGH

	GPIO13 OVDDR27V	GPIO1 OVDDR26V
2.5V	HIGH	HIGH
2.6V	LOW	HIGH
2.7V	LOW	LOW

K1 K_ICT/X
K2 K_ICT/X
K3 K_ICT/X
K4 K_ICT/X
K5 K_ICT/X
K6 K_ICT/X
I1 4MMH/X
I2 4MMH/X
I3 4MMH/X
I4 4MMH/X
MH1 MH2 MH3 MH4 MH5 MH7 HOLE_3
EGND

-12V VCC3 VCC3
5VSB
R482 22K/6
(12) -PSON
Z225
BC252 0.1U/6/Y/25V
ATX
3.3V 3.3V
-12V 3.3V
GND GND
PSON 5V
GND GND
GND 5V
GND GND
-5V POK
5V 5VSB
5V 12V
PWR2x10/CL1
BC251 0.1U/6/Y/25V
VCC
VCC
PWOK
PWOK (21,23,28,29)
5VSB
+12V
-5V
VCC
VCC
BC253 BC254 BC255 BC256 BC257 BC258 BC259 BC260 BC261
0.1U/6/Y/25V

V12
ATX_12V
+12V GND
+12V GND
BC262 0.1U/6/Y/25V
PWR2x2/CL1/SOSP

PB REQUEST V12

+12V TRACE 250MIL

ATX POWER CONNECTOR

GIGABYTE

Title	ATX, DDR POWER	
Size: Custom	Document Number: 8S651MP-RZ	Rev: 1.0
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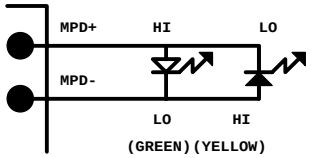
LO:Normal

RTL8100L ON-BOARD		
	-REQ0 PCI1	**IDSEL(A20)--B**
	-REQ1 PCI2	**IDSEL(A22)--C**
	-REQ2 PCI3	**IDSEL(A24)--D**
	-REQ3 RTL8100L	**IDSEL(A27)--B**



8SRXL South Bridge GPIO LIST				
ITEM	DESCRIPTION	I/O	STATUS	Default
GPIO0	Bios Write Protect	O	Hi:Write Enable, Lo:Write Protect	Hi
GPIO1	N/A		PULL-UP	Hi
GPIO2	THERM#			Hi
GPIO3	Green Button	O	Hi:Normal, Lo:Into Green mode	Hi
GPIO4	CLKRUN#		PULL-DOWN	Lo
GPIO5	N/A		PULL-UP	Hi
GPIO6	DDR OVER VOLTAGE	O		Hi
GPIO7	SUSLED	O	**AS LIKE DEFINED...**	Lo
GPIO8	Wake On Ring	I	Hi:Normal, Lo:Ring Power On	Hi
GPIO9	GLED	I	**AS LIKE DEFINED...**	Lo
GPIO10	Mother Board ID	I	SIS DEMO B/D PULL-DOWN	Lo
GPIO11	N/A		PULL-UP	Hi
GPIO12	N/A		PULL-UP	Hi
GPIO13	Mother Board ID	I	SIS DEMO B/D PULL-DOWN	Lo
GPIO14	DDR OVER VOLTAGE	I		Lo
GPIO15	KB Data	I/OD		
GPIO16	KB Clk	I/OD		
GPIO17	MS Data	I/OD		
GPIO18	MS Clk	I/OD		

States for a single-color power LED

				BIOS	
LED States	**ACPI States**	MPD+	MPD-	GPIO7	ACPILED
OFF	S5	HI	HI	**LO**	**HI/NC**
Steady Green	S0	HI	LO	**LO**	**LO**
Blinking Green	S0(message waiting)	HI	BLINKING	**LO**	**BLINKING**

States for a dual-color power LED

				BIOS	
LED States	**ACPI States**	MPD+	MPD-	GPIO7	ACPILED
OFF	S5	HI	HI	**LO**	**HI/NC**
Steady Green	S0	HI	LO	**LO**	**LO**
Blinking Green	S0(message waiting)	HI	BLINKING	**LO**	**BLINKING**
Steady Yellow	S1,S3	LO	HI	**HI**	**HI**
Blinking Yellow	S1,S3(message waiting)	LO	BLINKING	**HI**	**BLINKING**

States for green LED

			BIOS
LED States	**ACPI States**	GLED-	GPIO9
ON	S1,S3	HI	**HI**
OFF	S0,S5	LO	**LO**

BIOS REQUEST

		INTEL LED DEFINED				GIGABYTE LED DEFINED					
SINGLE	**DUAL**		**GPIO7**	**ACPILED**	**GPIO9**		**GPIO7**	**ACPILED**	**GPIO9**	**SINGLE**	**DUAL**
GREEN	**GREEN**	**S0**	**LO**	**LO**	**LO**	**S0**	**LO**	**LO**	**LO**	**GREEN**	**GREEN**
OFF	**YELLOW**	**S1**	**HI**	**HI**	**HI**	**S1**	**LO**	**BLINKING**	**HI**	**G(BLINK)**	**G(BLINK)**
OFF	**YELLOW**	**S3**	**HI**	**HI**	**HI**	**S3**	**HI**	**HI**	**HI**	**OFF**	**YELLOW**
OFF	**OFF**	**S4/S5**	**LO**	**HI/NC**	**LO**	**S4/S5**	**LO**	**HI/NC**	**LO**	**OFF**	**OFF**

GIGABYTE

Title: **GPIO, REQ/GNT Table**

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Date: 星期一, 八月 16, 2004 | Sheet 32 of 32