

GA-M61VME-S2

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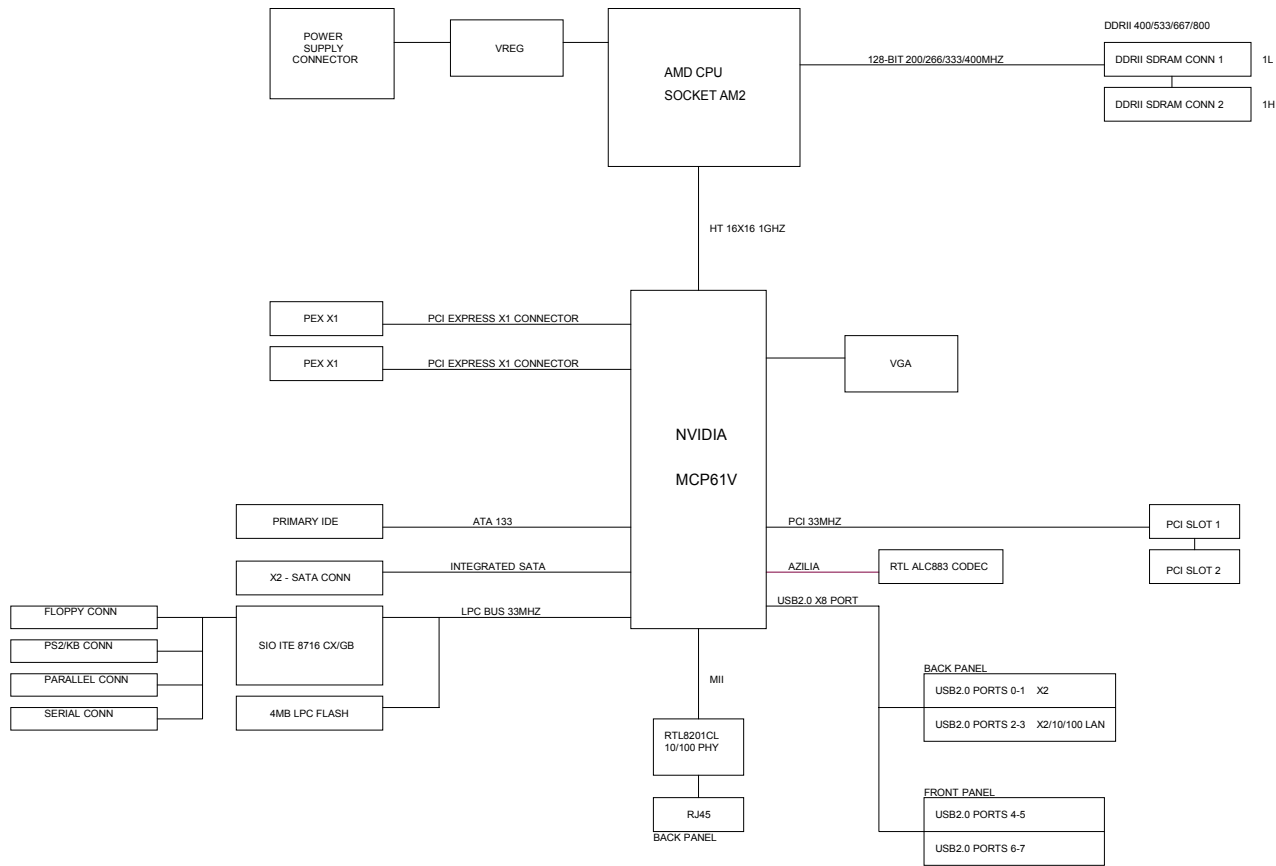
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GIGABYTE			
Title			
BLOCK DIAGRAM			
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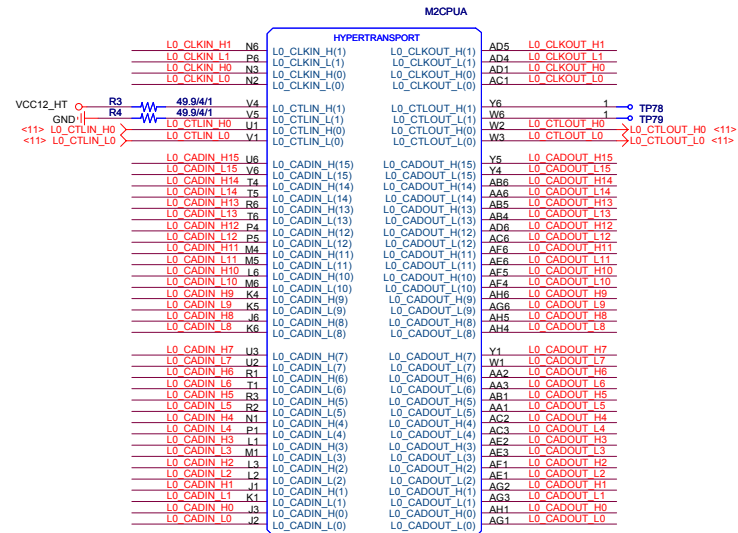
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BLOCK DIAGRAM

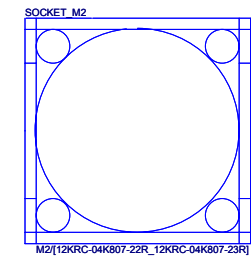


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L0_CADIN_H[0..15] <L0_CADIN_H[0..15] <11>
L0_CLKIN_L[0..1] <L0_CLKIN_L[0..1] <11>
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L0_CADOUT_L[0..15] <L0_CADOUT_L[0..15] <11>
L0_CADOUT_H[0..15] <L0_CADOUT_H[0..15] <11>
L0_CLKOUT_L[0..1] <L0_CLKOUT_L[0..1] <11>
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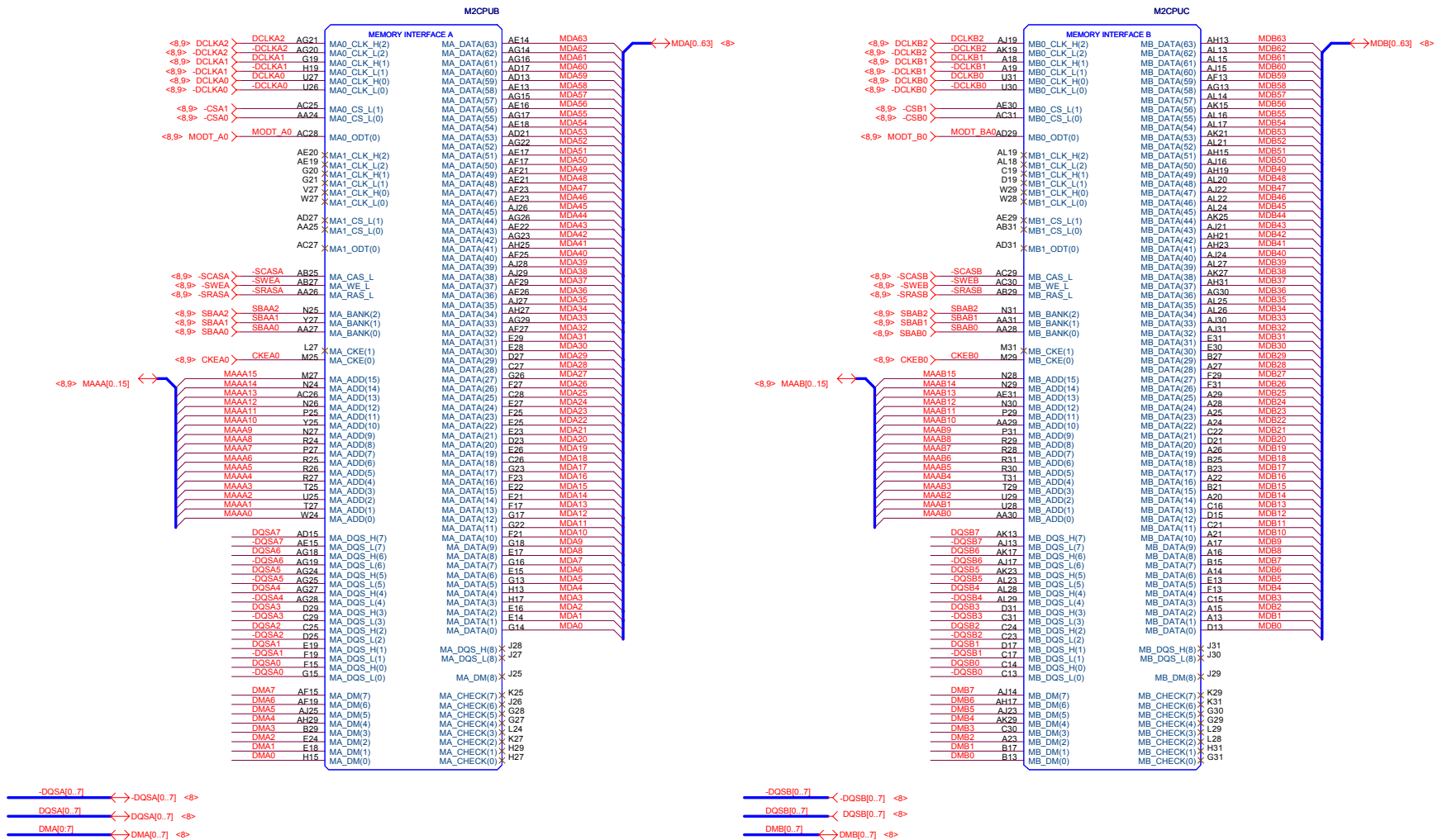
CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR18V
CPU_VTT_SUS = DDRVTT

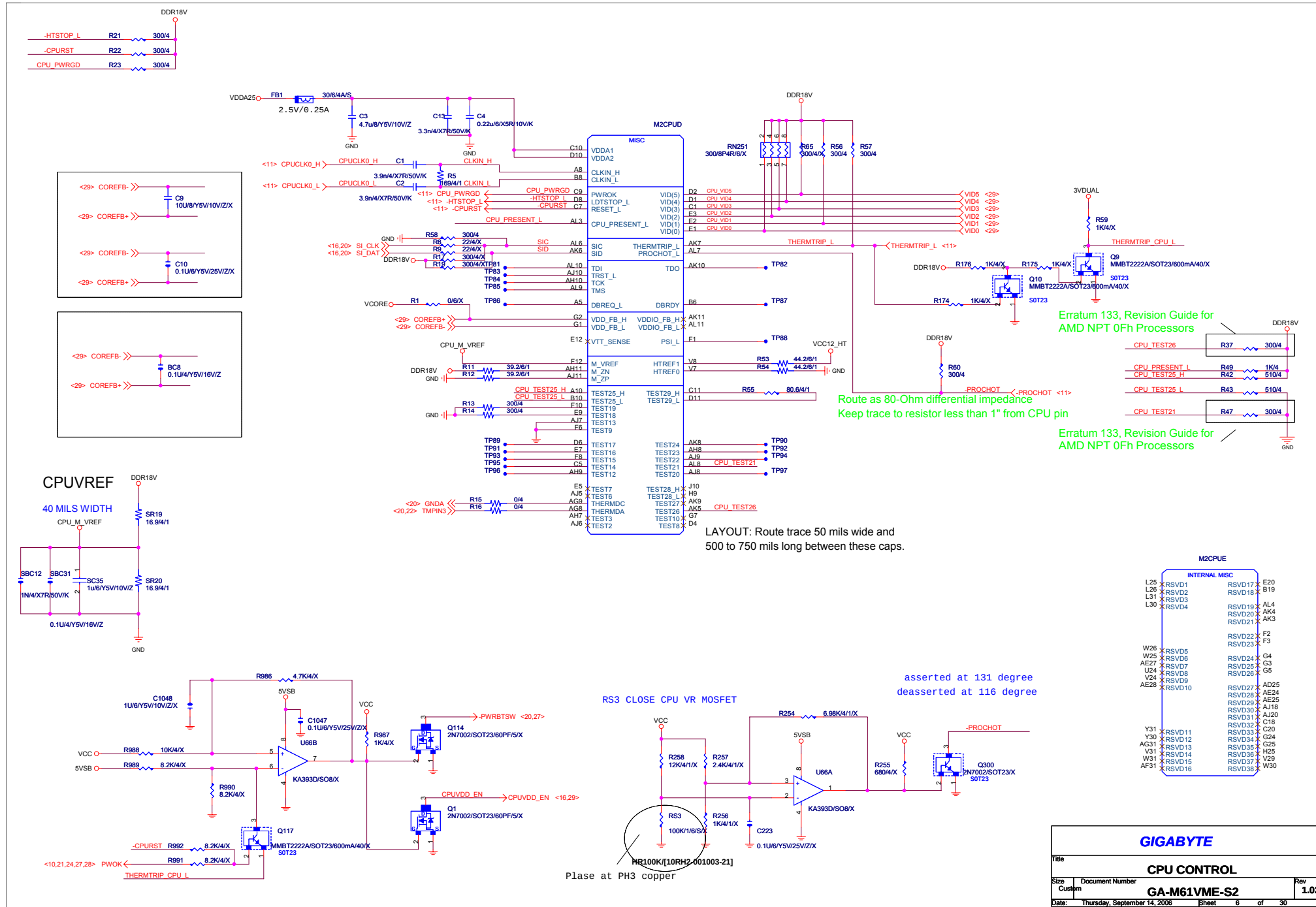
VLDT_A = VCC12_HT
VLDT_B = HT12B

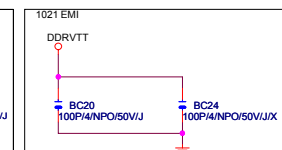
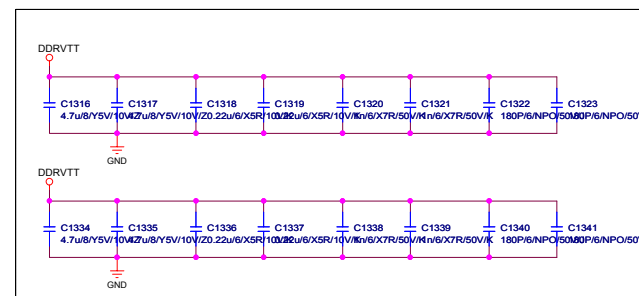
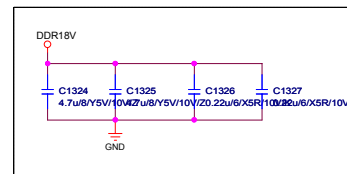
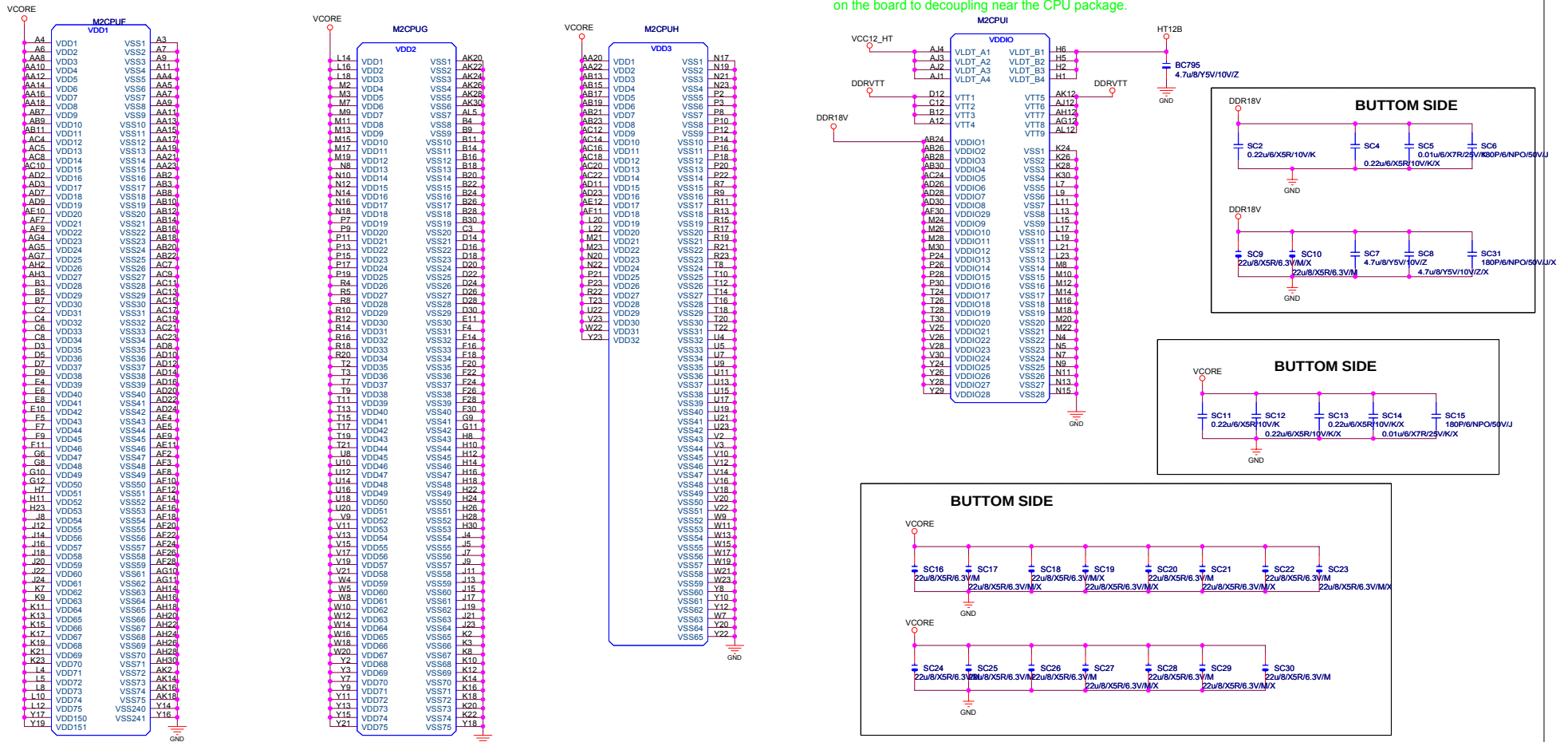


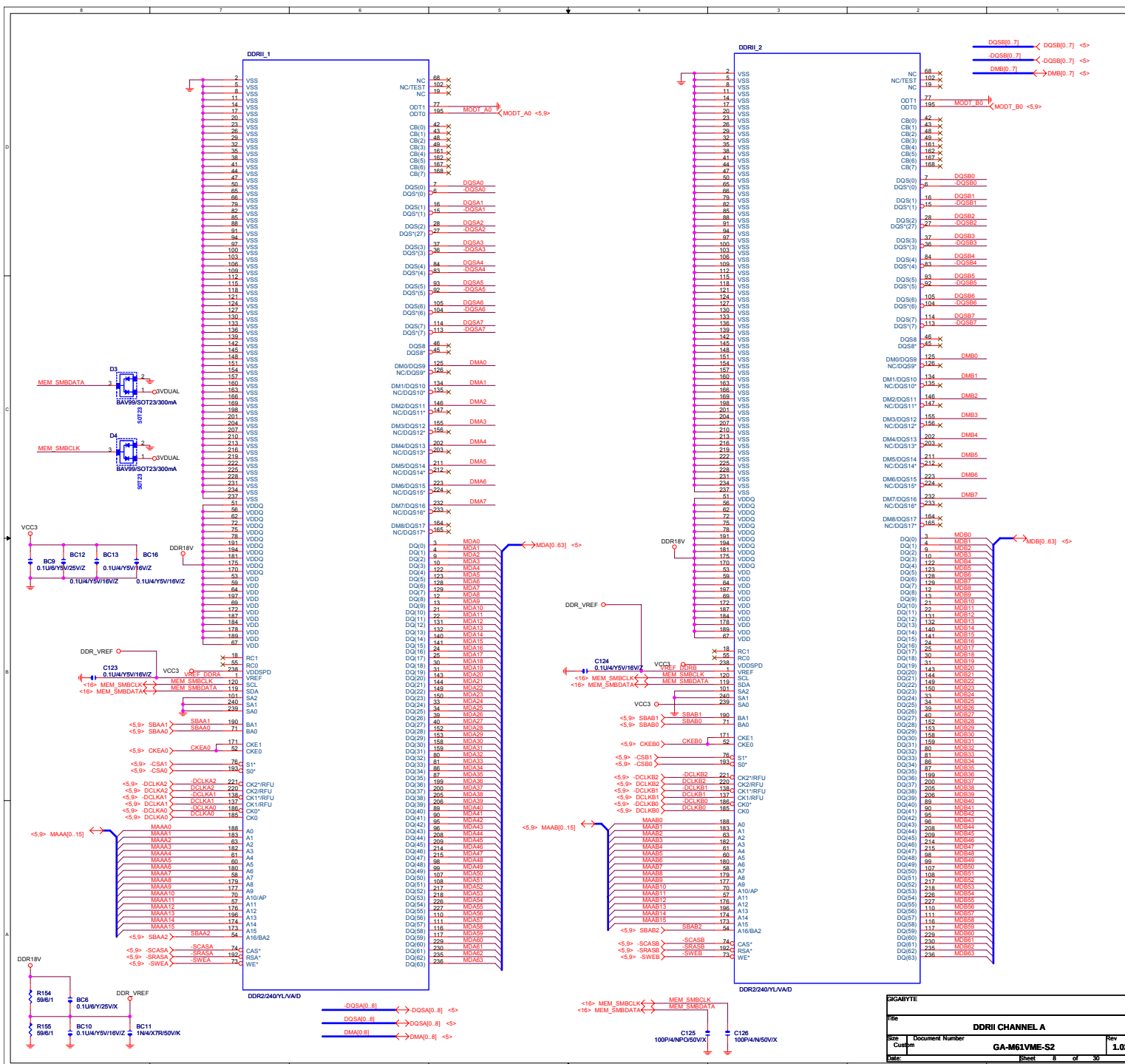
GIGABYTE

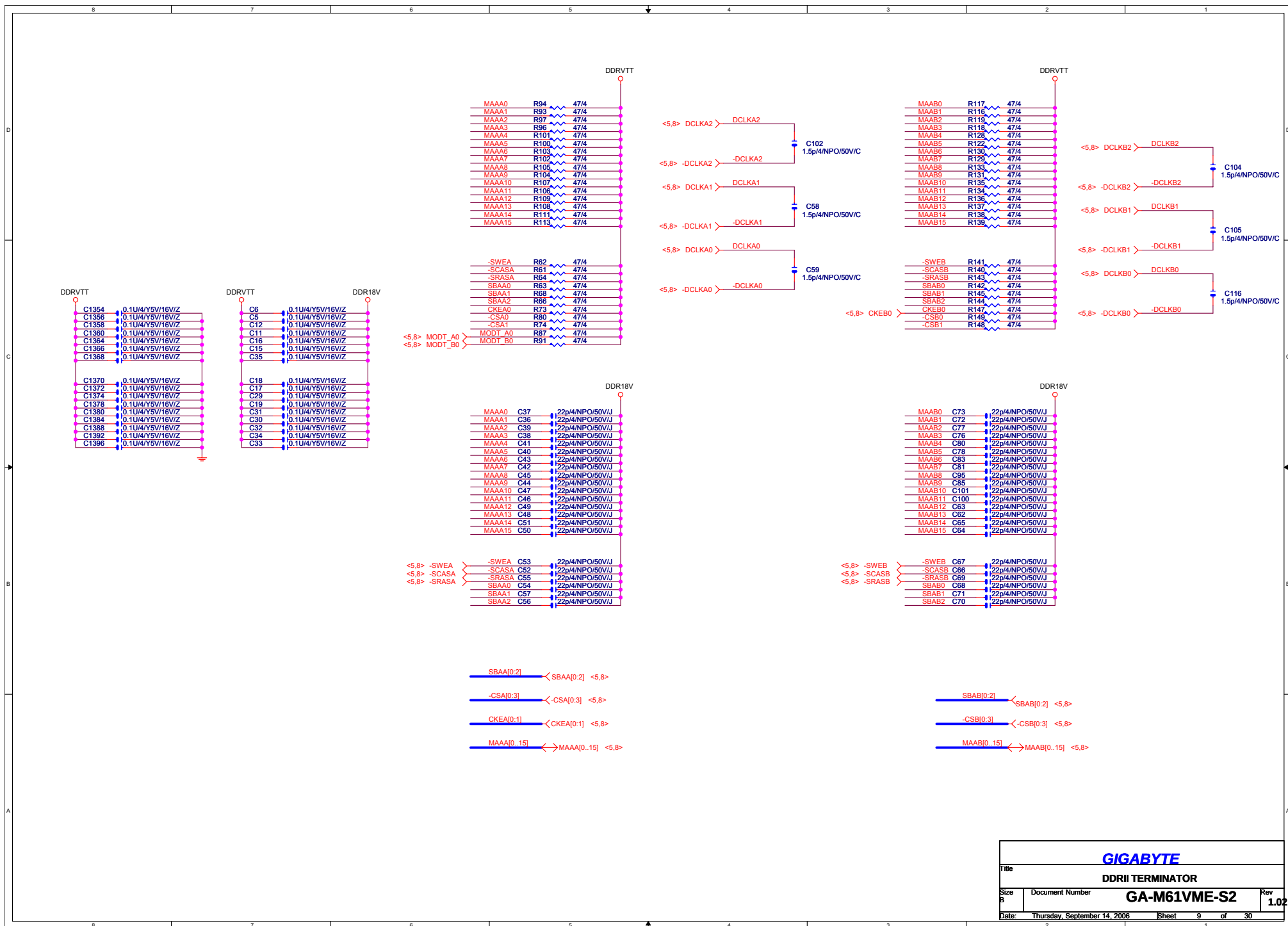
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CPU HYPER TRANSPORT			
Size	Document Number	Document Number	Rev
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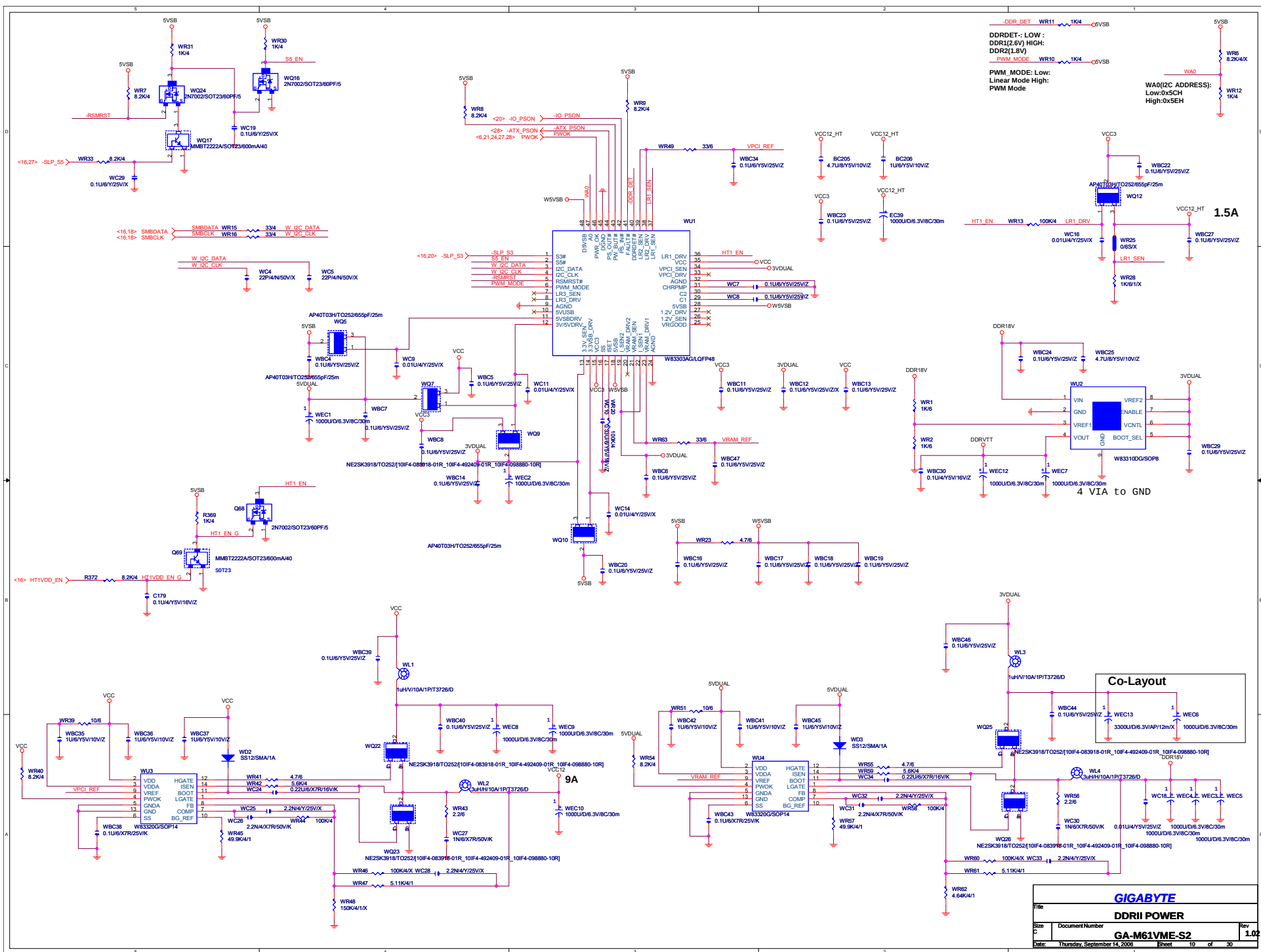


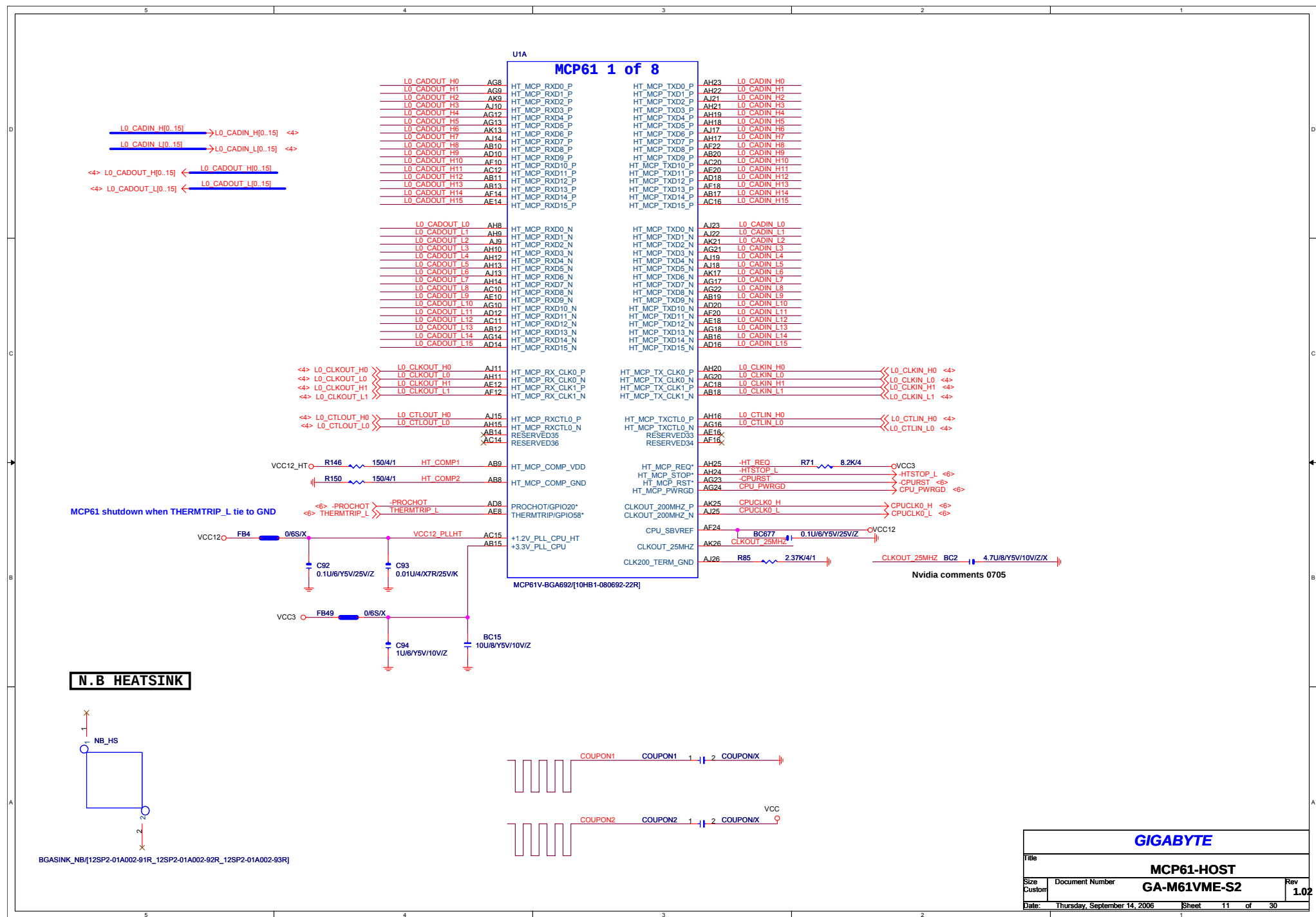


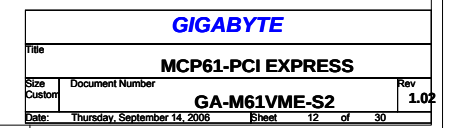


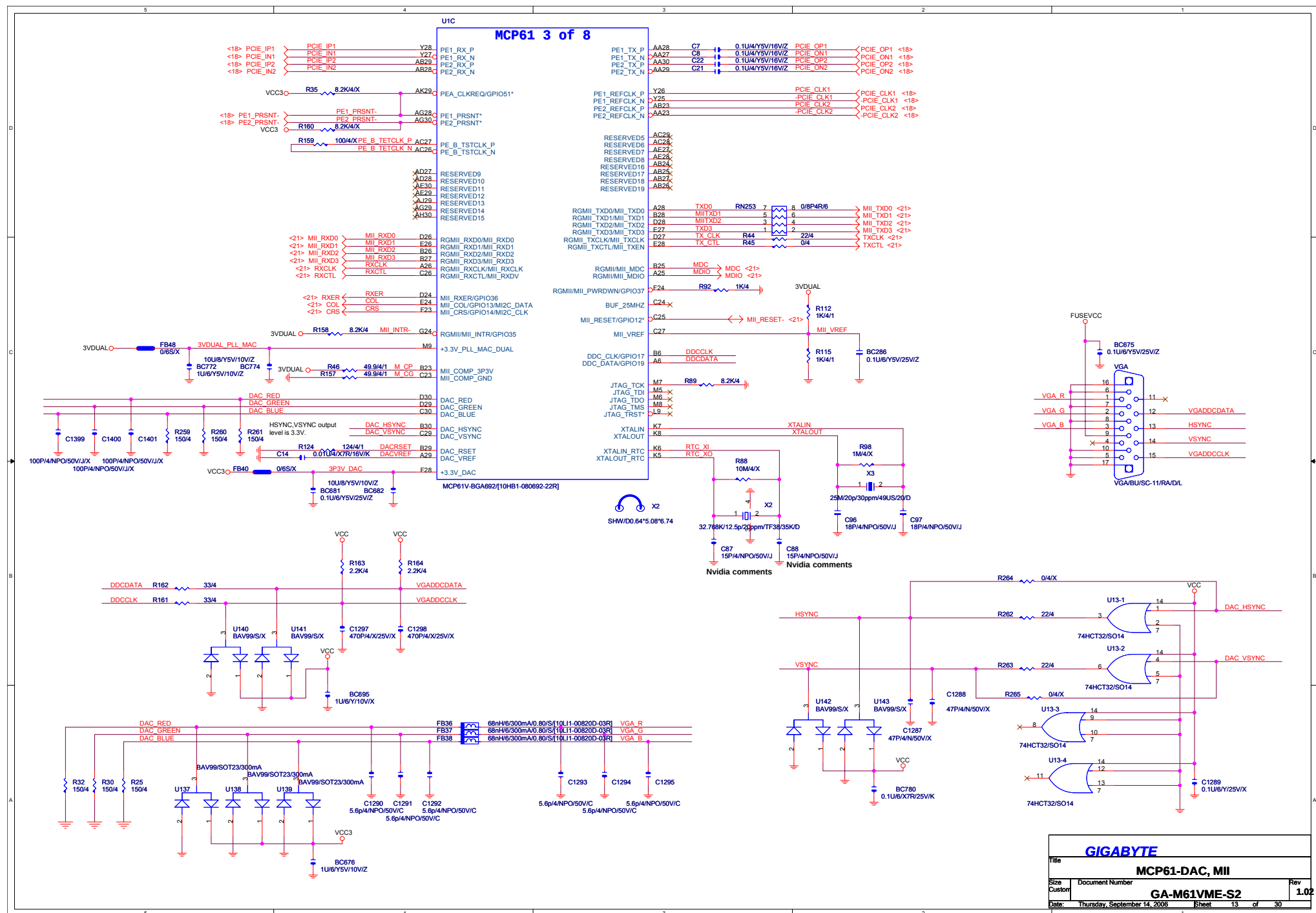


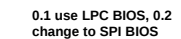


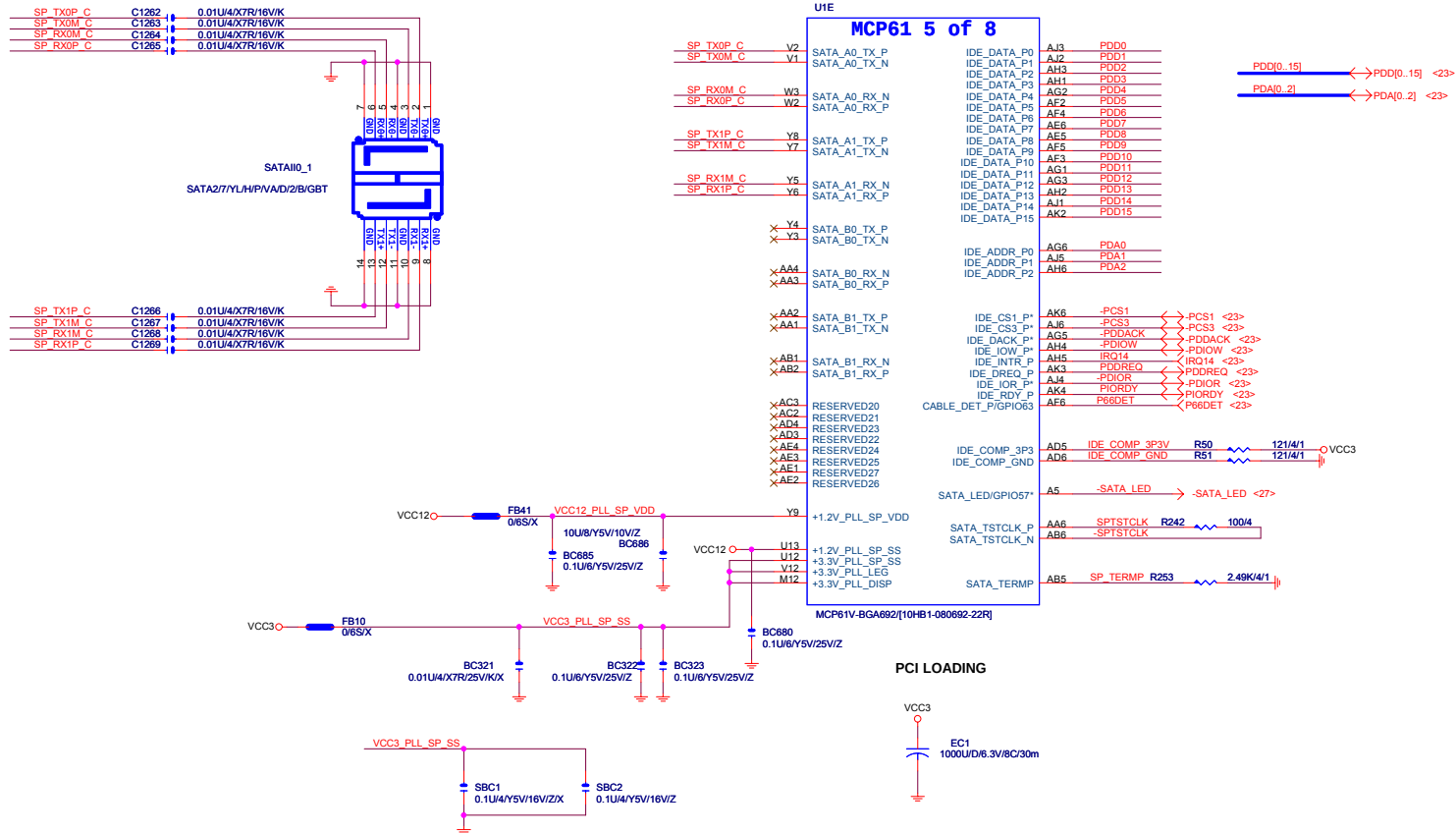


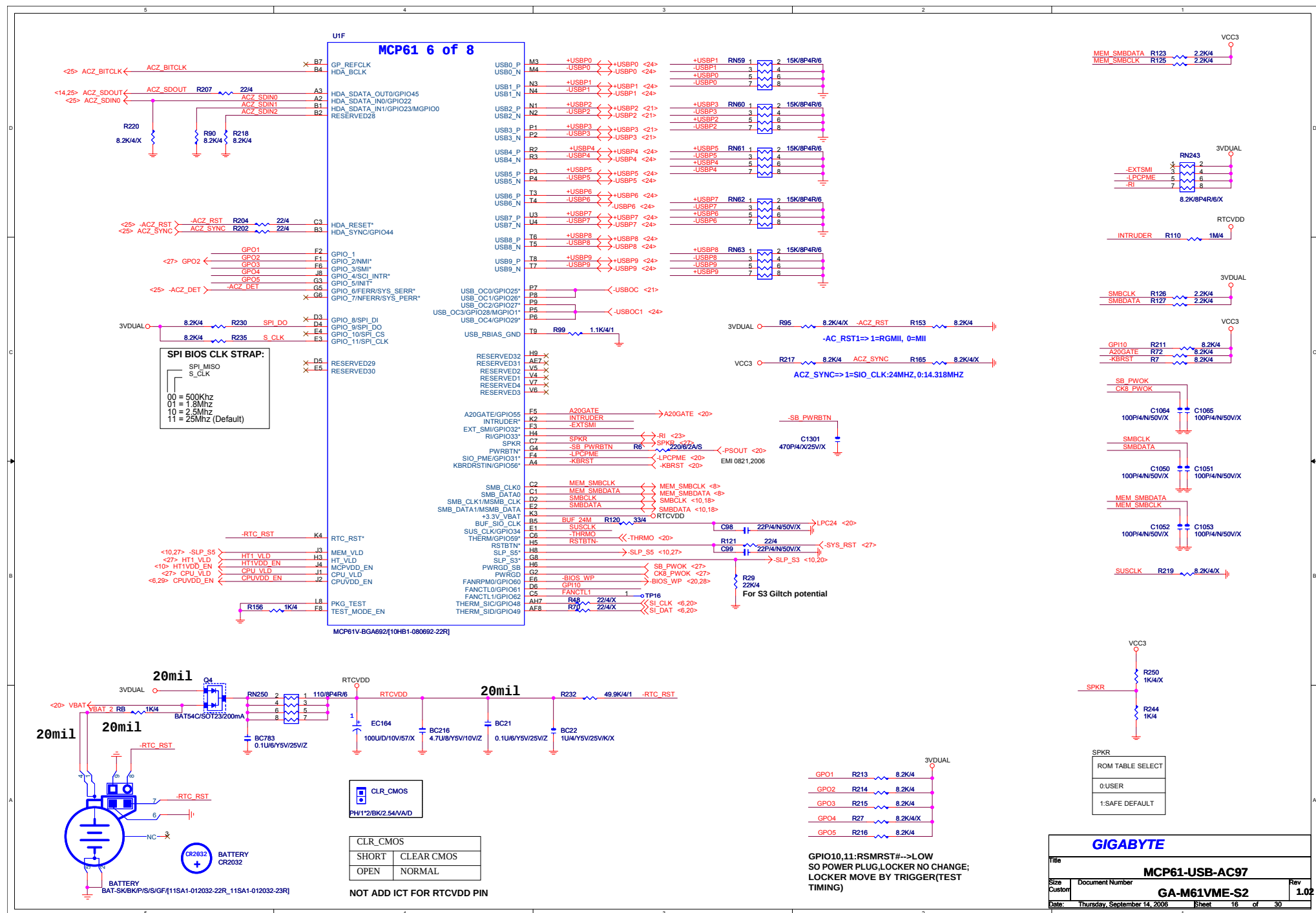


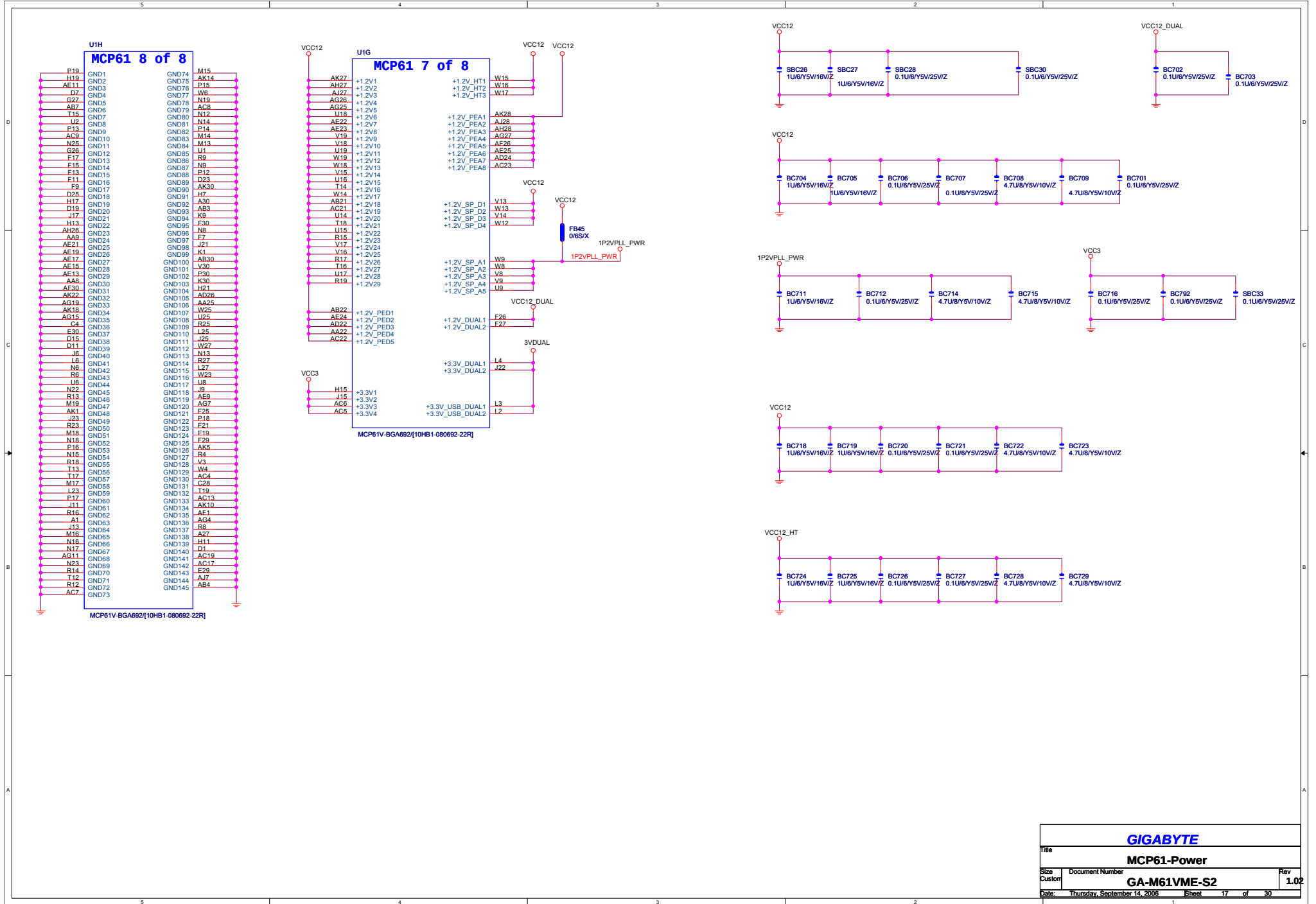


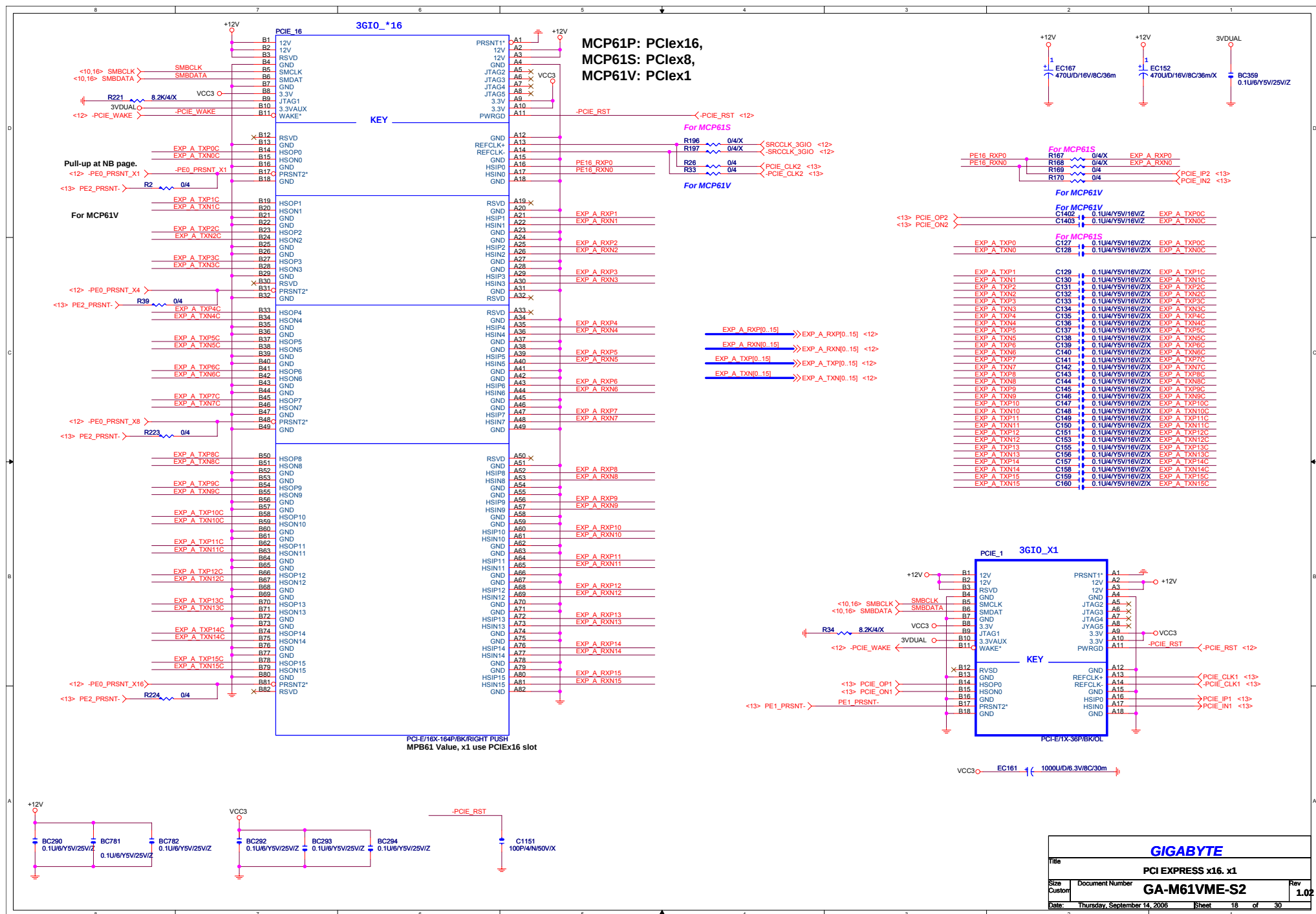




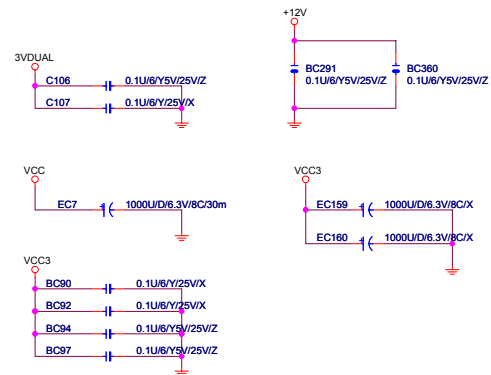
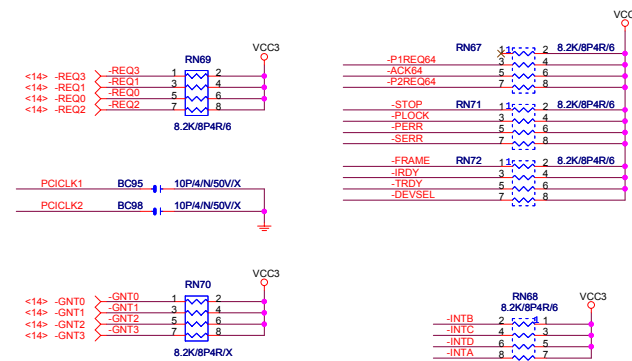
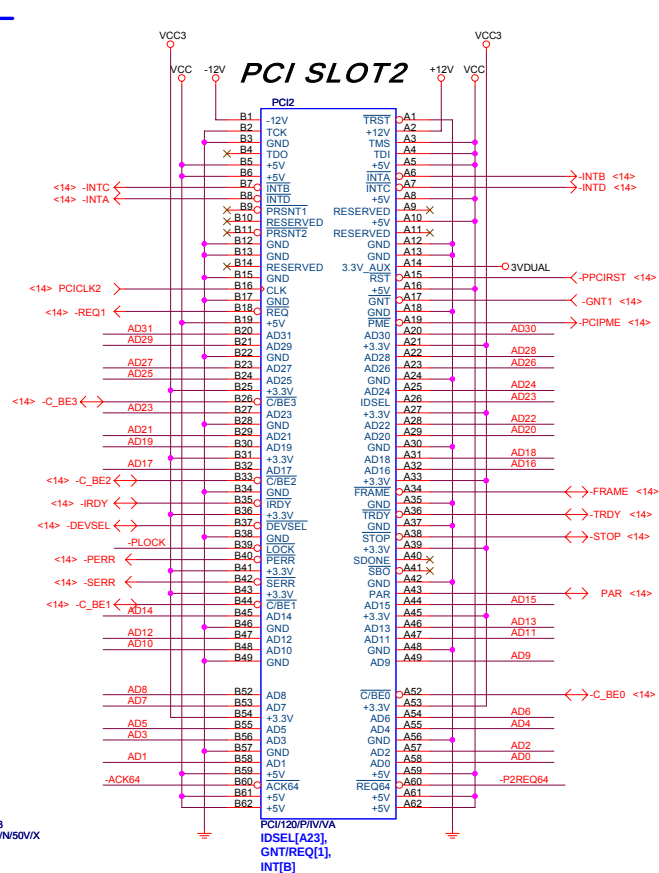
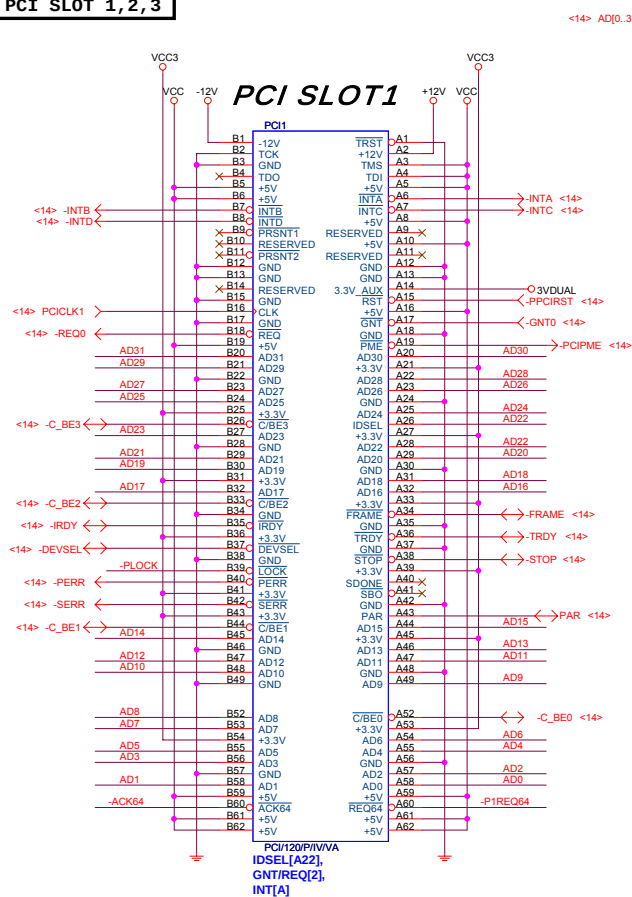


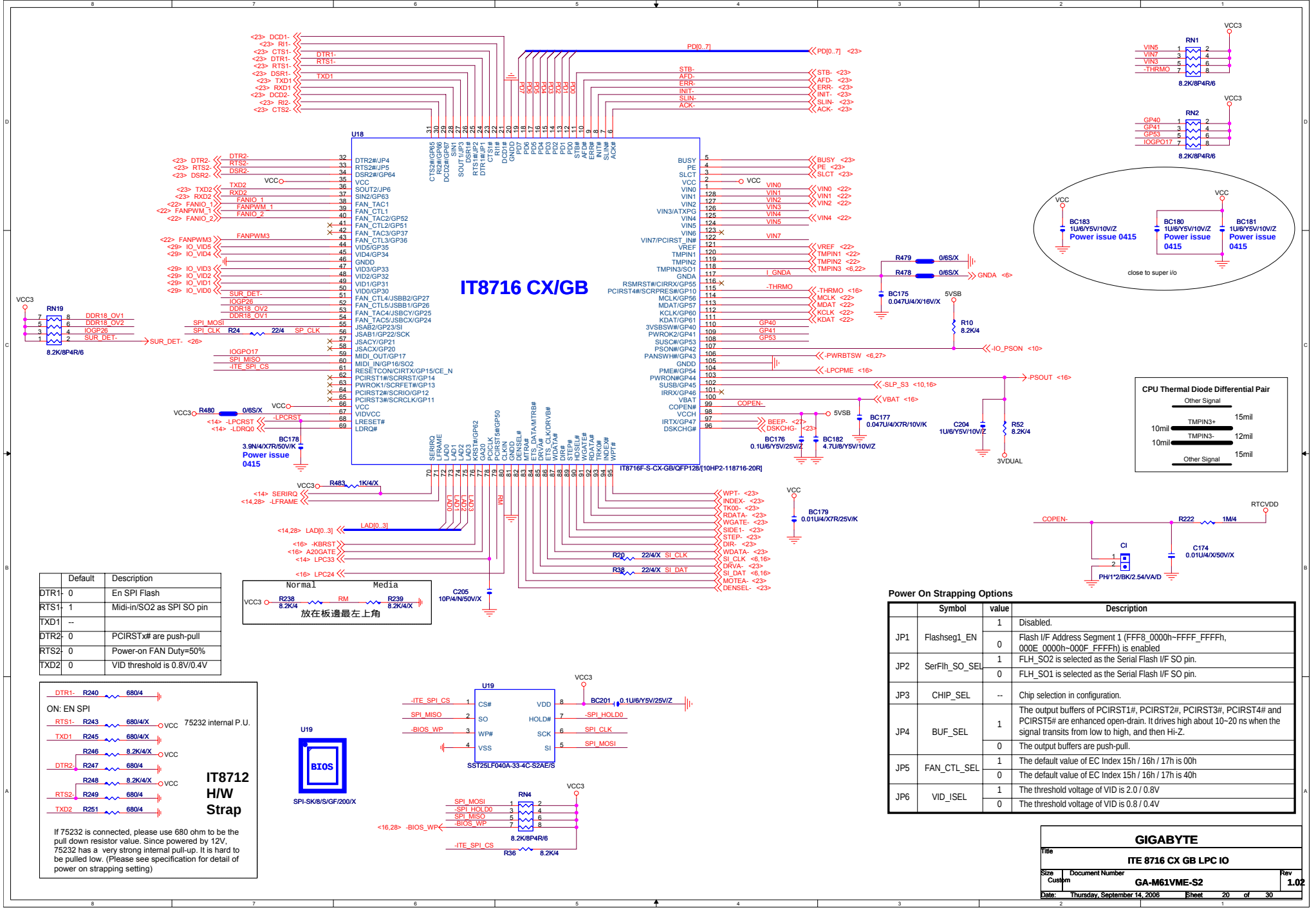






PCI SLOT 1,2,3





	Default	Description
DTR1-	0	En SPI Flash
RTS1-	1	Mid-in/SO2 as SPI SO pin
TXD1	--	
DTR2-	0	PCIRSTx# are push-pull
RTS2-	0	Power-on FAN Duty=50%
TXD2	0	VID threshold is 0.8V/0.4V

DTR1-

R240

680/4

RTS1-

R243

680/4/X

VCC

TXD1

R245

680/4/X

DTR2-

R247

680/4

VCC

RTS2-

R249

680/4

VCC

TXD2

R251

680/4

ON: EN SPI

75232 internal P.U.

IT8712

H/W

Strap

If 75232 is connected, please use 680 ohm to be the pull down resistor value. Since powered by 12V, 75232 has a very strong internal pull-up. It is hard to be pulled low. (Please see specification for detail of power on strapping setting)

Power On Strapping Options

	Symbol	value	Description
JP1	Flashseg1_EN	1	Disabled.
		0	Flash I/F Address Segment 1 (FFF8_0000h~FFFF_FFFFh, 000E_0000h~000F_FFFFh) is enabled
JP2	SerFlh_SO_SEL	1	FLH_SO2 is selected as the Serial Flash I/F SO pin.
		0	FLH_SO1 is selected as the Serial Flash I/F SO pin.
JP3	CHIP_SEL	--	Chip selection in configuration.
JP4	BUF_SEL	1	The output buffers of PCIRST1#, PCIRST2#, PCIRST3#, PCIRST4# and PCIRST5# are enhanced open-drain. It drives high about 10~20 ns when the signal transits from low to high, and then Hi-Z.
		0	The output buffers are push-pull.
JP5	FAN_CTL_SEL	1	The default value of EC Index 15h / 16h / 17h is 00h
		0	The default value of EC Index 15h / 16h / 17h is 40h
JP6	VID_ISEL	1	The threshold voltage of VID is 2.0 / 0.8V
		0	The threshold voltage of VID is 0.8 / 0.4V

GIGABYTE

ITE 8716 CX GB LPC IO

Size Custom Document Number

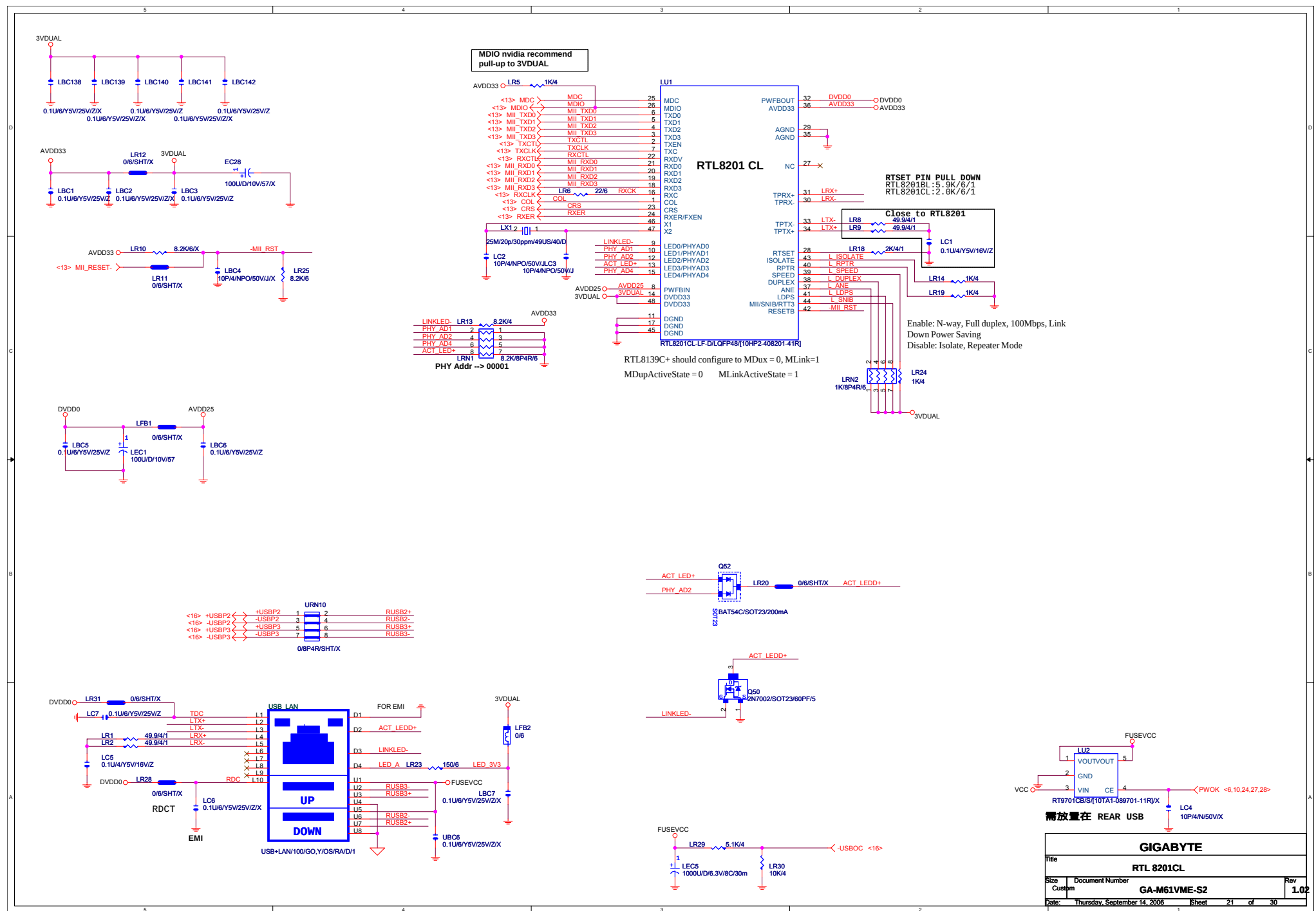
GA-M61VME-S2

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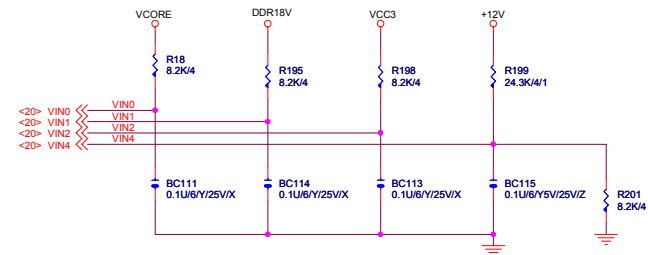
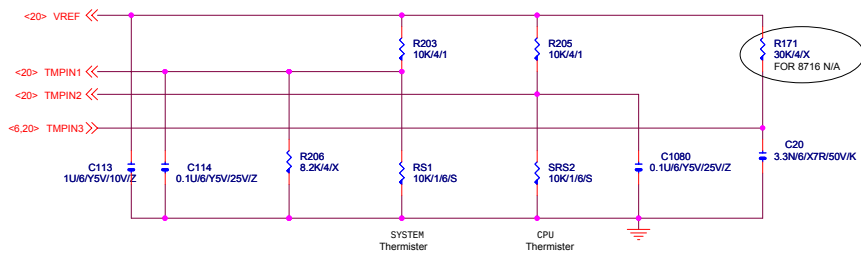
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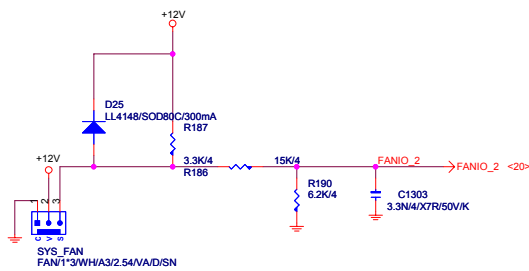
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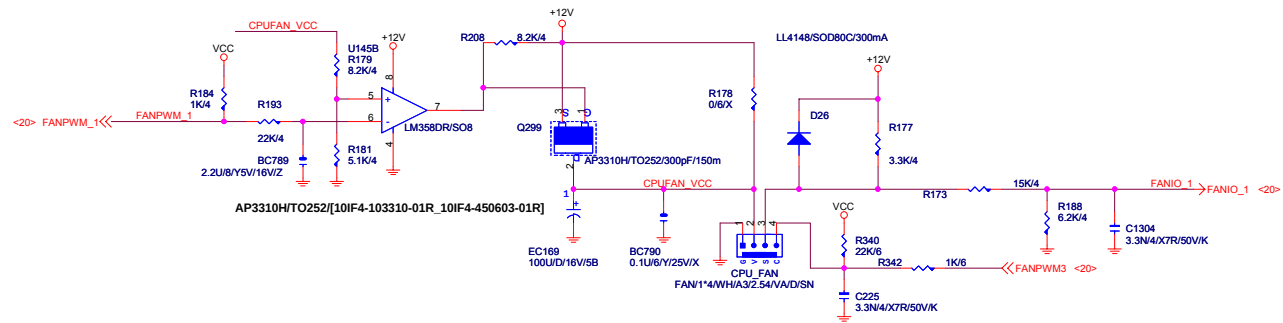
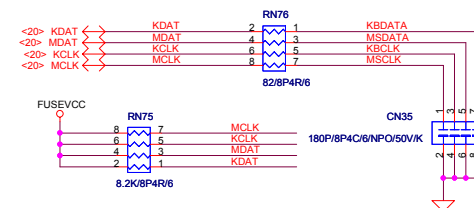
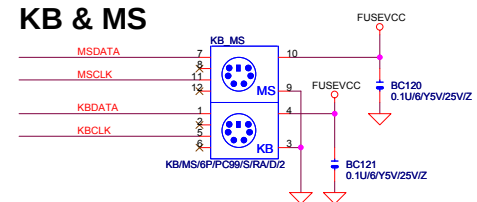
Hardware Monitor circuits

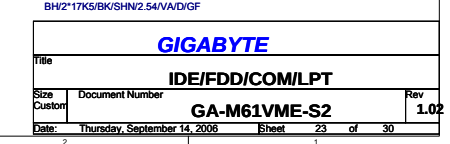


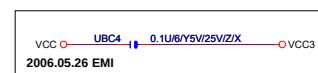
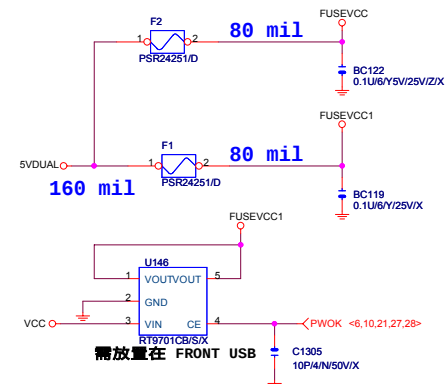
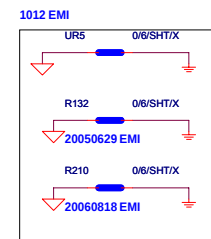
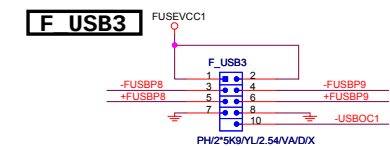
SYSTEM FAN

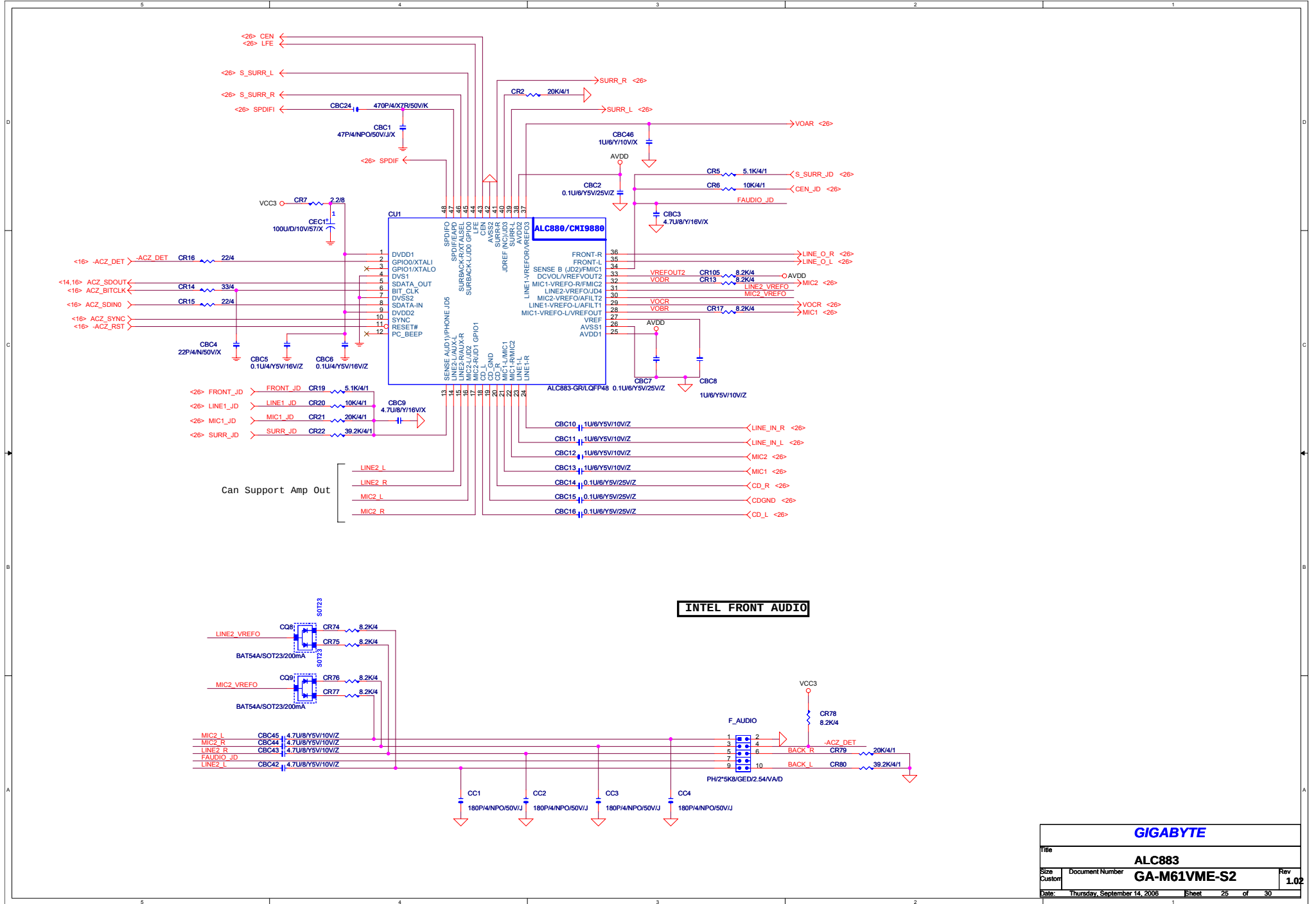


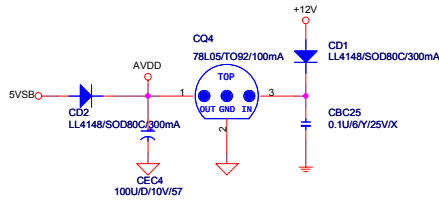
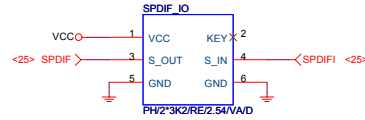
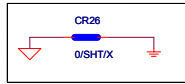
CPU FAN

**KB & MS**

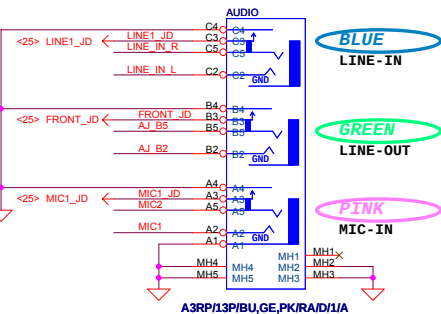
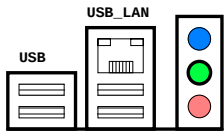
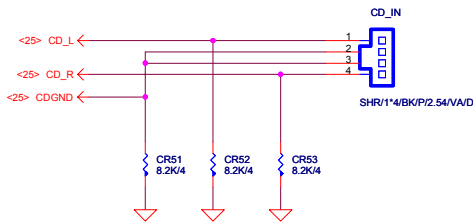




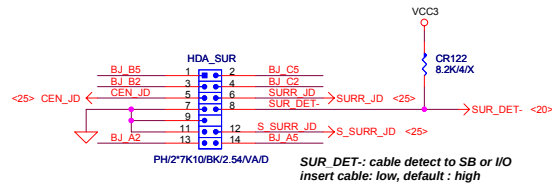




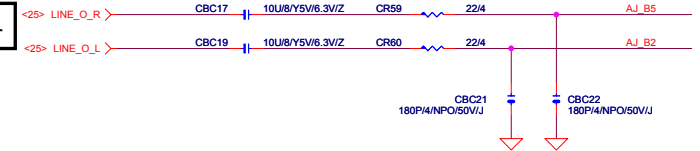
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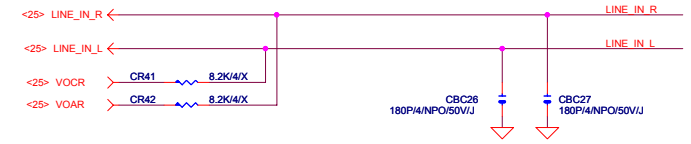
A3RJ13P/B[11NR6-403006-01_11NR6-403006-02]
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LINE OUT FRONT OUT



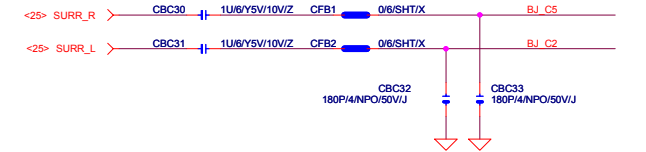
LINE-IN



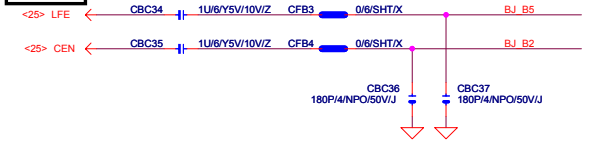
MIC



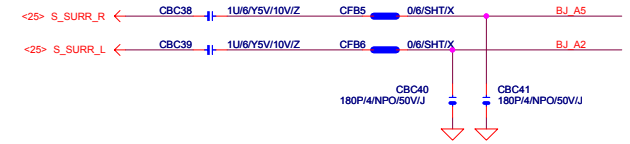
SURROUND



CEN/LFE



SURR BACK



GIGABYTE

Title		
AUDIO JACK		
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