GA-M61PM-S2

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SHEET	TITLE
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27	FRONT PANEL POWER SEQUENCE
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29	PWM ISL6566
30	VCC12_DUAL,VCC12_HT,VDDA25 POWER
31	DDRII POWER
32	TI TSB43AB23 1394

Revision:1.0

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Title: BLOCK DIAGRAM

Size: Custom | Document Number: GA-M61PM-S2 | Rev: 1.0

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Model Name:GA-M61PM-S2 *Revision:1.0*

Component value change history

P-Code: A95096-0

Date	Change Item		Reason
2006.06.06	0.1 BOM release	PCB:0.1	
2006.08.02	1.0A D_BOM release	PCB:1.0	SPI change to ITE8716. Clear CMOS change to RTCRST Heat sink change to 92R
			Add EMI solution
2006.08.11	1.0A P_BOM release	PCB:1.0	Add packing list.

Circuit or PCB layout change for next version

Date	Change Item	Reason
2006.06.23	0.1 Gerber Out	
2006.08.01	1.0 Gerber Out 1394 VCC-->VCC3	

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Title: BOM & PCB MODIFY HISTORY

Size: Custom | Document Number: GA-M61PM-S2 | Rev: 1.0

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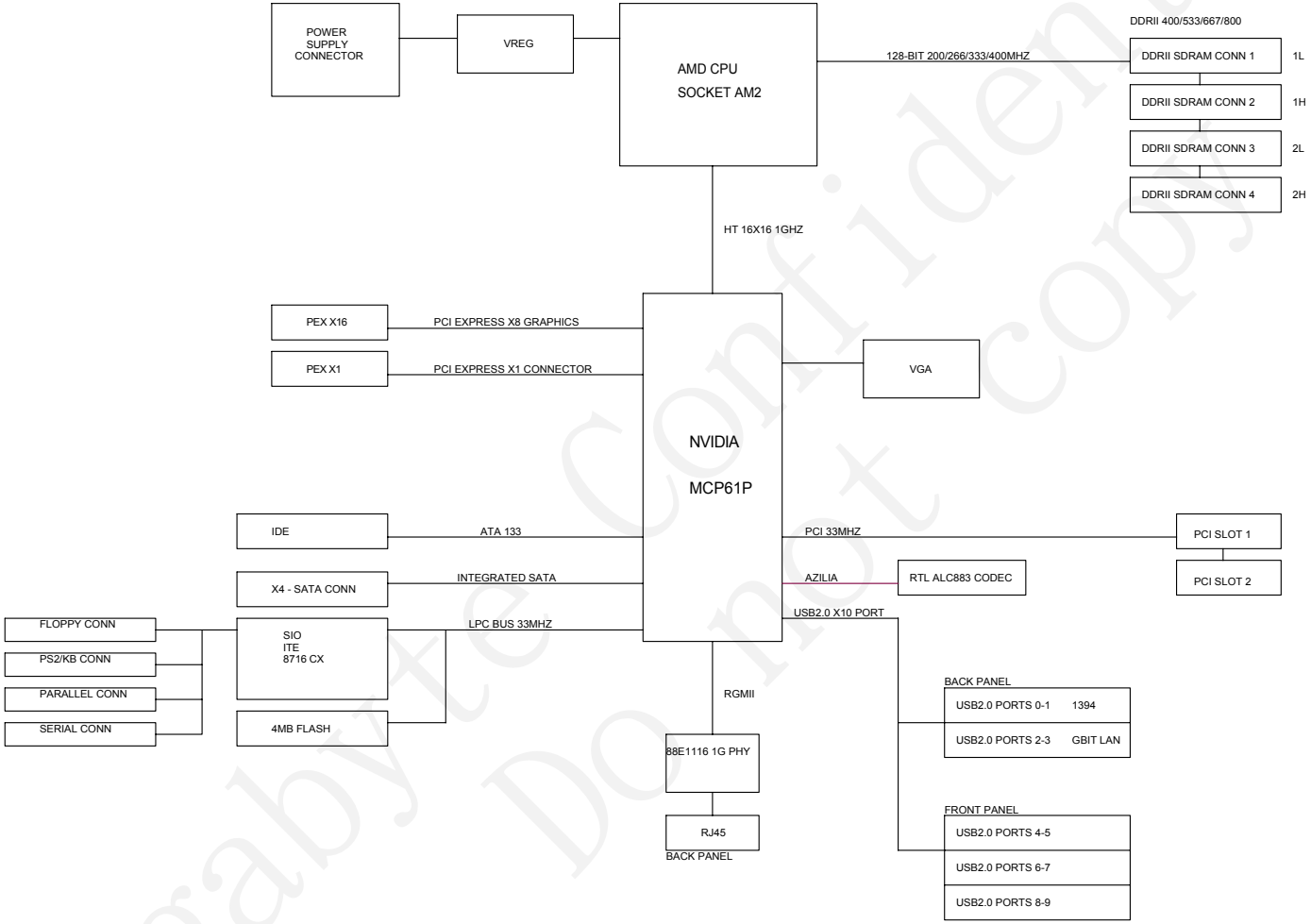
BLOCK DIAGRAM



GIGABYTE		
Title: BLOCK DIAGRAM		
Size: Custom	Document Number: GA-M61PM-S2	Rev: 1.0
Date: Tuesday, August 15, 2006	Sheet 3 of 32	

L0_CADIN_L[0..15] L0_CADIN_L[0..15] <11>
L0_CADIN_H[0..15] L0_CADIN_H[0..15] <11>
L0_CLKIN_L[0..1] L0_CLKIN_L[0..1] <11>
L0_CLKIN_H[0..1] L0_CLKIN_H[0..1] <11>
L0_CADOUT_L[0..15] L0_CADOUT_L[0..15] <11>
L0_CADOUT_H[0..15] L0_CADOUT_H[0..15] <11>
L0_CLKOUT_L[0..1] L0_CLKOUT_L[0..1] <11>
L0_CLKOUT_H[0..1] L0_CLKOUT_H[0..1] <11>

CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR18V
CPU_VTT_SUS = DDRVTT

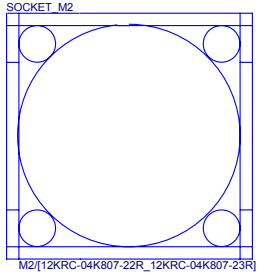
VLDT_A = VCC12_HT
VLDT_B = HT12B

M2CPUA

HYPERTRANSPORT

		L0_CLKIN_H1	N6	L0_CLKIN_H(1)	L0_CLKOUT_H(1)	AD5	L0_CLKOUT_H1
		L0_CLKIN_L1	P6	L0_CLKIN_L(1)	L0_CLKOUT_L(1)	AD4	L0_CLKOUT_L1
		L0_CLKIN_H0	N3	L0_CLKIN_H(0)	L0_CLKOUT_H(0)	AD1	L0_CLKOUT_H0
		L0_CLKIN_L0	N2	L0_CLKIN_L(0)	L0_CLKOUT_L(0)	AC1	L0_CLKOUT_L0
VCC12_HT	R3	49.9/4/1	V4	L0_CTLIN_H(1)	L0_CTLOUT_H(1)	Y6	1 TP78
GND	R4	49.9/4/1	V5	L0_CTLIN_L(1)	L0_CTLOUT_L(1)	W6	1 TP79
<11> L0_CTLIN_H0		L0_CTLIN_H0	U1	L0_CTLIN_H(0)	L0_CTLOUT_H(0)	W2	L0_CTLOUT_H0 L0_CTLOUT_H0 <11>
<11> L0_CTLIN_L0		L0_CTLIN_L0	V1	L0_CTLIN_L(0)	L0_CTLOUT_L(0)	W3	L0_CTLOUT_L0 L0_CTLOUT_L0 <11>
		L0_CADIN_H15	U6	L0_CADIN_H(15)	L0_CADOUT_H(15)	Y5	L0_CADOUT_H15
		L0_CADIN_L15	V6	L0_CADIN_L(15)	L0_CADOUT_L(15)	Y4	L0_CADOUT_L15
		L0_CADIN_H14	T4	L0_CADIN_H(14)	L0_CADOUT_H(14)	AB6	L0_CADOUT_H14
		L0_CADIN_L14	T5	L0_CADIN_L(14)	L0_CADOUT_L(14)	AA6	L0_CADOUT_L14
		L0_CADIN_H13	R6	L0_CADIN_H(13)	L0_CADOUT_H(13)	AB5	L0_CADOUT_H13
		L0_CADIN_L13	T6	L0_CADIN_L(13)	L0_CADOUT_L(13)	AB4	L0_CADOUT_L13
		L0_CADIN_H12	P4	L0_CADIN_H(12)	L0_CADOUT_H(12)	AD6	L0_CADOUT_H12
		L0_CADIN_L12	P5	L0_CADIN_L(12)	L0_CADOUT_L(12)	AC6	L0_CADOUT_L12
		L0_CADIN_H11	M4	L0_CADIN_H(11)	L0_CADOUT_H(11)	AF6	L0_CADOUT_H11
		L0_CADIN_L11	M5	L0_CADIN_L(11)	L0_CADOUT_L(11)	AE6	L0_CADOUT_L11
		L0_CADIN_H10	L6	L0_CADIN_H(10)	L0_CADOUT_H(10)	AF5	L0_CADOUT_H10
		L0_CADIN_L10	M6	L0_CADIN_L(10)	L0_CADOUT_L(10)	AF4	L0_CADOUT_L10
		L0_CADIN_H9	K4	L0_CADIN_H(9)	L0_CADOUT_H(9)	AH6	L0_CADOUT_H9
		L0_CADIN_L9	K5	L0_CADIN_L(9)	L0_CADOUT_L(9)	AG6	L0_CADOUT_L9
		L0_CADIN_H8	J6	L0_CADIN_H(8)	L0_CADOUT_H(8)	AH5	L0_CADOUT_H8
		L0_CADIN_L8	K6	L0_CADIN_L(8)	L0_CADOUT_L(8)	AH4	L0_CADOUT_L8
		L0_CADIN_H7	U3	L0_CADIN_H(7)	L0_CADOUT_H(7)	Y1	L0_CADOUT_H7
		L0_CADIN_L7	U2	L0_CADIN_L(7)	L0_CADOUT_L(7)	W1	L0_CADOUT_L7
		L0_CADIN_H6	R1	L0_CADIN_H(6)	L0_CADOUT_H(6)	AA2	L0_CADOUT_H6
		L0_CADIN_L6	T1	L0_CADIN_L(6)	L0_CADOUT_L(6)	AA3	L0_CADOUT_L6
		L0_CADIN_H5	R3	L0_CADIN_H(5)	L0_CADOUT_H(5)	AB1	L0_CADOUT_H5
		L0_CADIN_L5	R2	L0_CADIN_L(5)	L0_CADOUT_L(5)	AA1	L0_CADOUT_L5
		L0_CADIN_H4	N1	L0_CADIN_H(4)	L0_CADOUT_H(4)	AC2	L0_CADOUT_H4
		L0_CADIN_L4	P1	L0_CADIN_L(4)	L0_CADOUT_L(4)	AC3	L0_CADOUT_L4
		L0_CADIN_H3	L1	L0_CADIN_H(3)	L0_CADOUT_H(3)	AE2	L0_CADOUT_H3
		L0_CADIN_L3	M1	L0_CADIN_L(3)	L0_CADOUT_L(3)	AE3	L0_CADOUT_L3
		L0_CADIN_H2	L3	L0_CADIN_H(2)	L0_CADOUT_H(2)	AF1	L0_CADOUT_H2
		L0_CADIN_L2	L2	L0_CADIN_L(2)	L0_CADOUT_L(2)	AE1	L0_CADOUT_L2
		L0_CADIN_H1	J1	L0_CADIN_H(1)	L0_CADOUT_H(1)	AG2	L0_CADOUT_H1
		L0_CADIN_L1	K1	L0_CADIN_L(1)	L0_CADOUT_L(1)	AG3	L0_CADOUT_L1
		L0_CADIN_H0	J3	L0_CADIN_H(0)	L0_CADOUT_H(0)	AH1	L0_CADOUT_H0
		L0_CADIN_L0	J2	L0_CADIN_L(0)	L0_CADOUT_L(0)	AG1	L0_CADOUT_L0

SOCKET_M2



M2/[12KRC-04K807-22R_12KRC-04K807-23R]

GIGABYTE

Title	CPU HYPER TRANSPORT		
Size: Custom	Document Number: GA-M61PM-S2		Rev: 1.0
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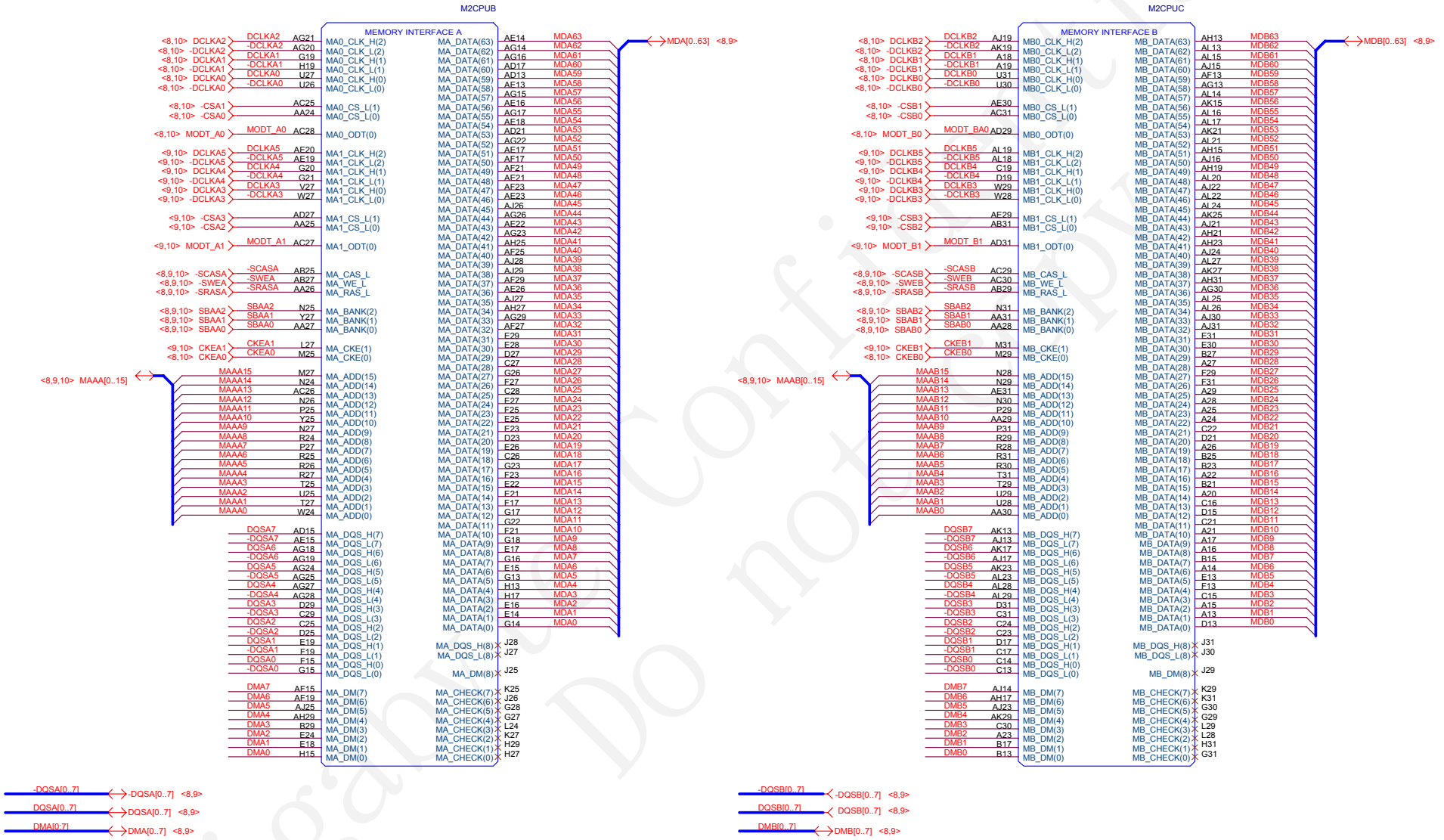

GIGABYTE

Title	CPU DDRII MEMORY
Size: Custom	Document Number: GA-M61PM-S2
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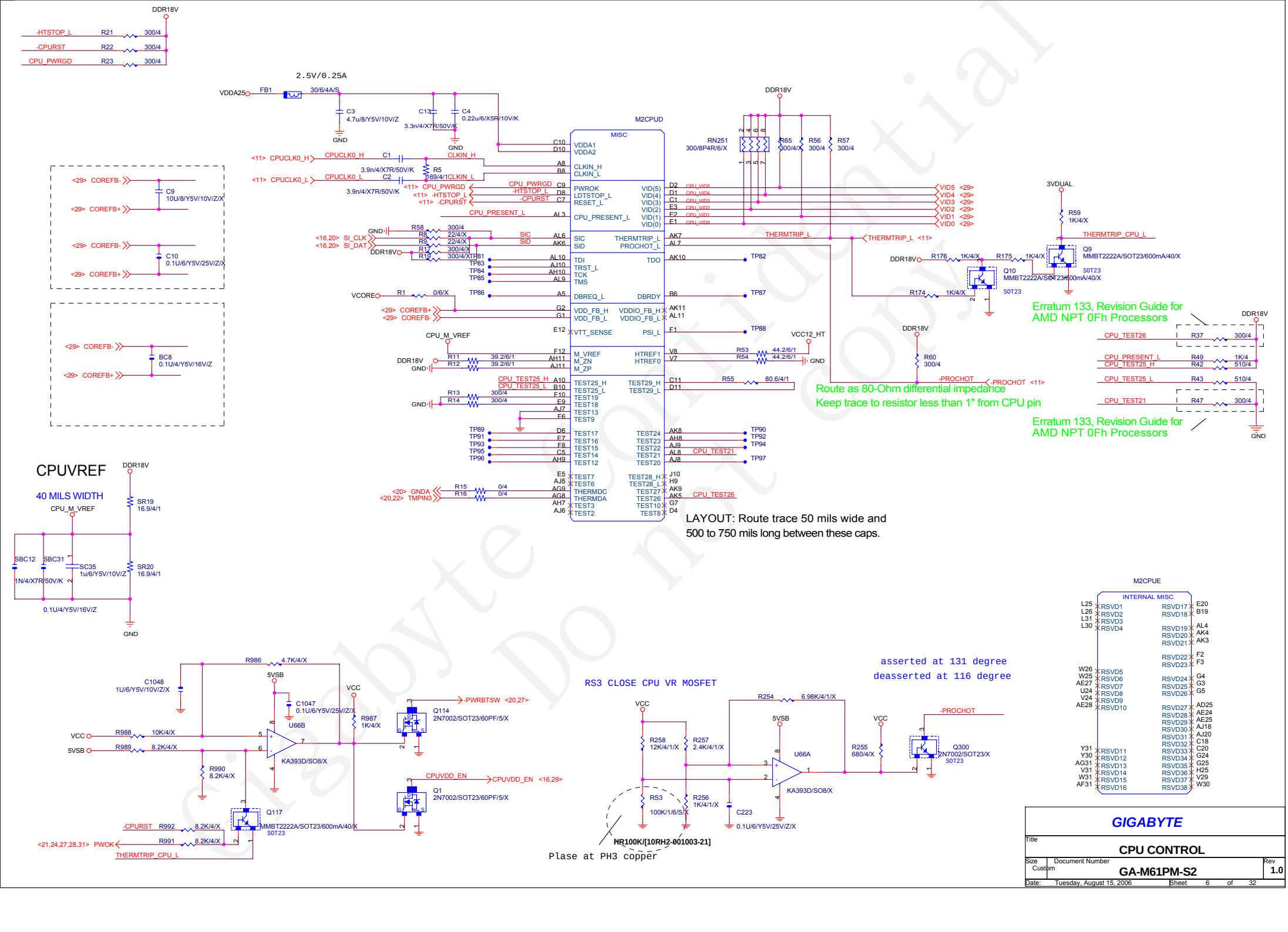
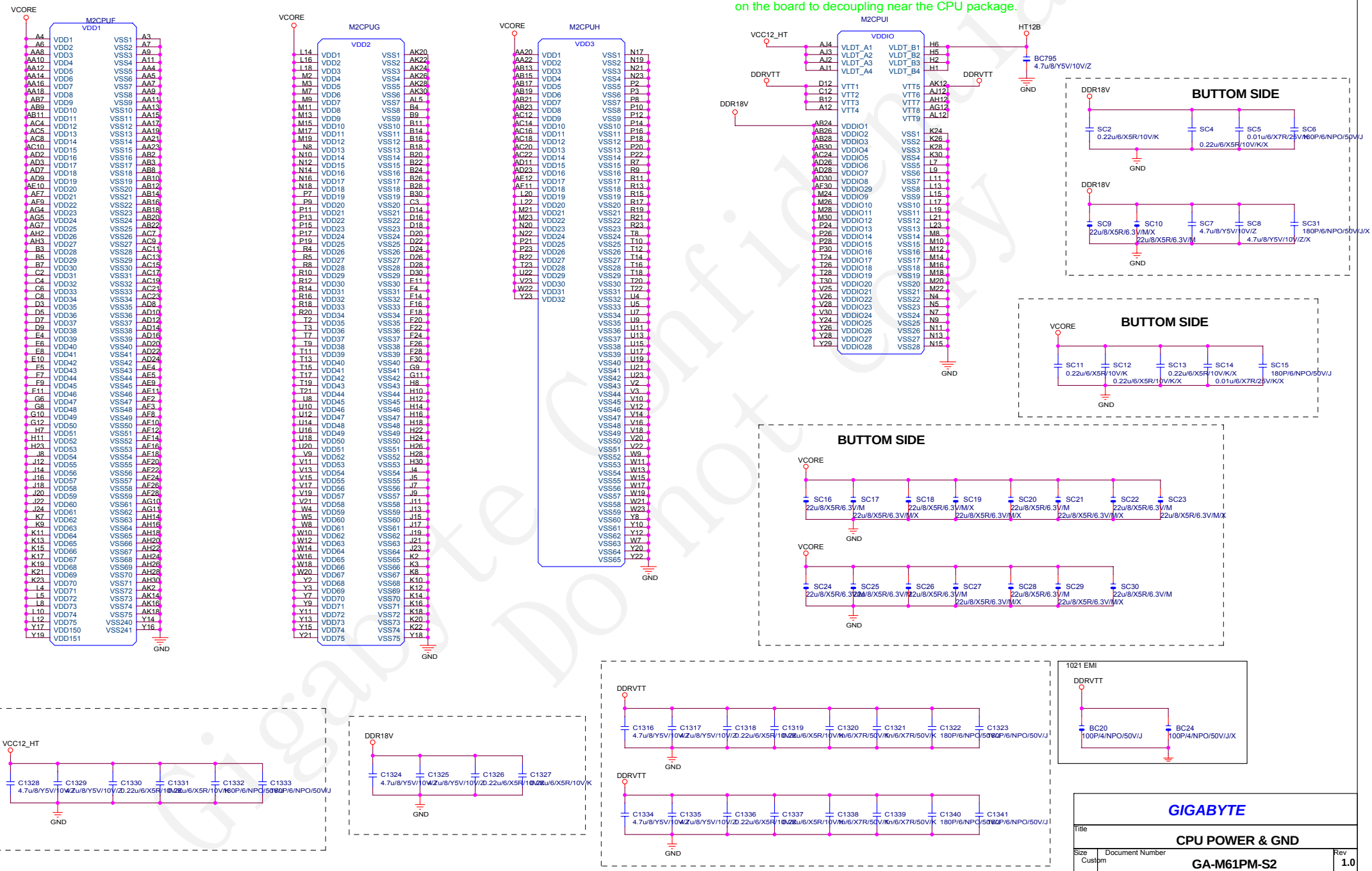


VLDT_RUN_B is connected to the VLDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.



GIGABYTE

Title: CPU POWER & GND

Size: Custom | Document Number: GA-M61PM-S2 | Rev: 1.0

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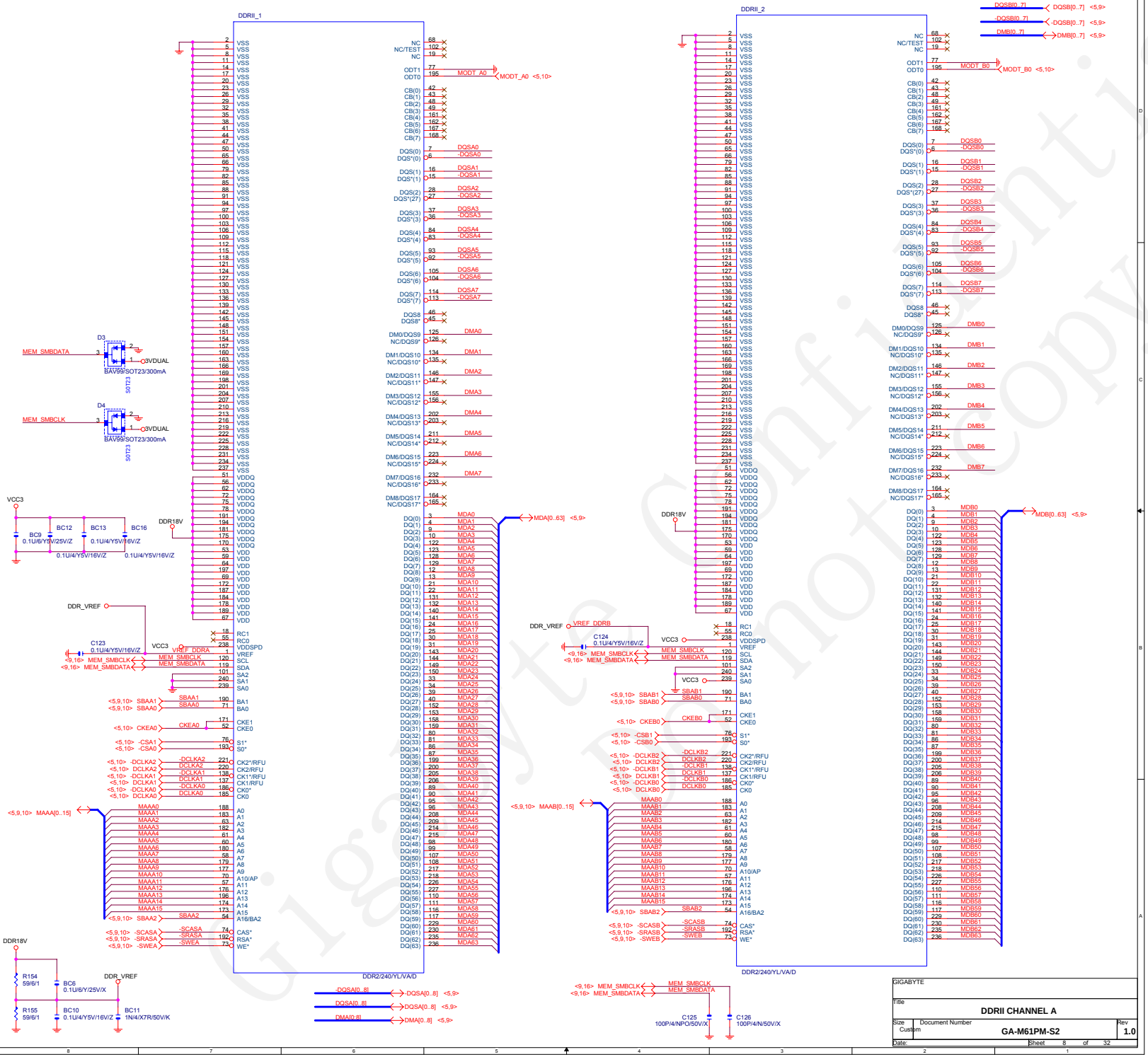

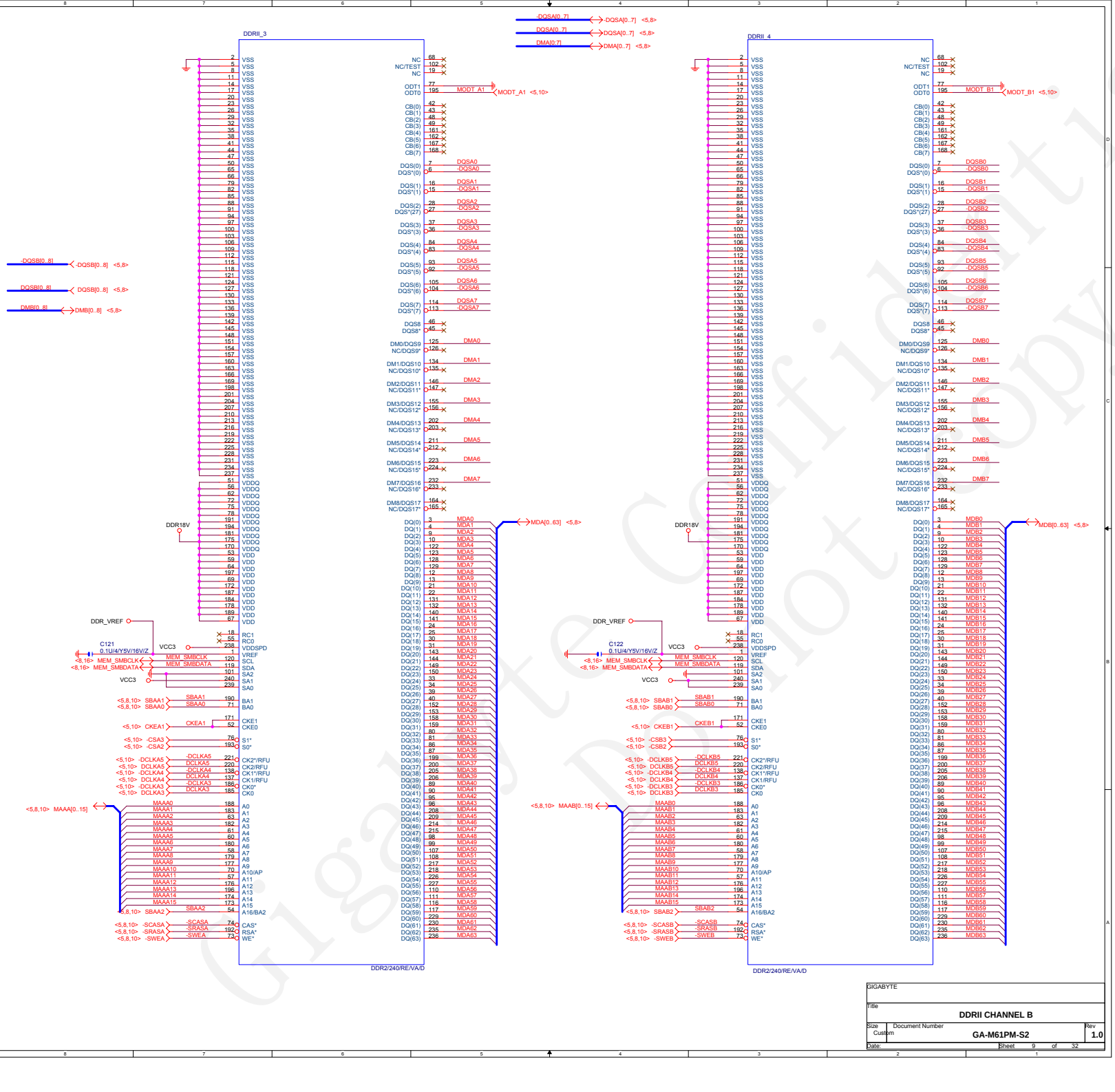

GIGABYTE

Title: DDRII CHANNEL B

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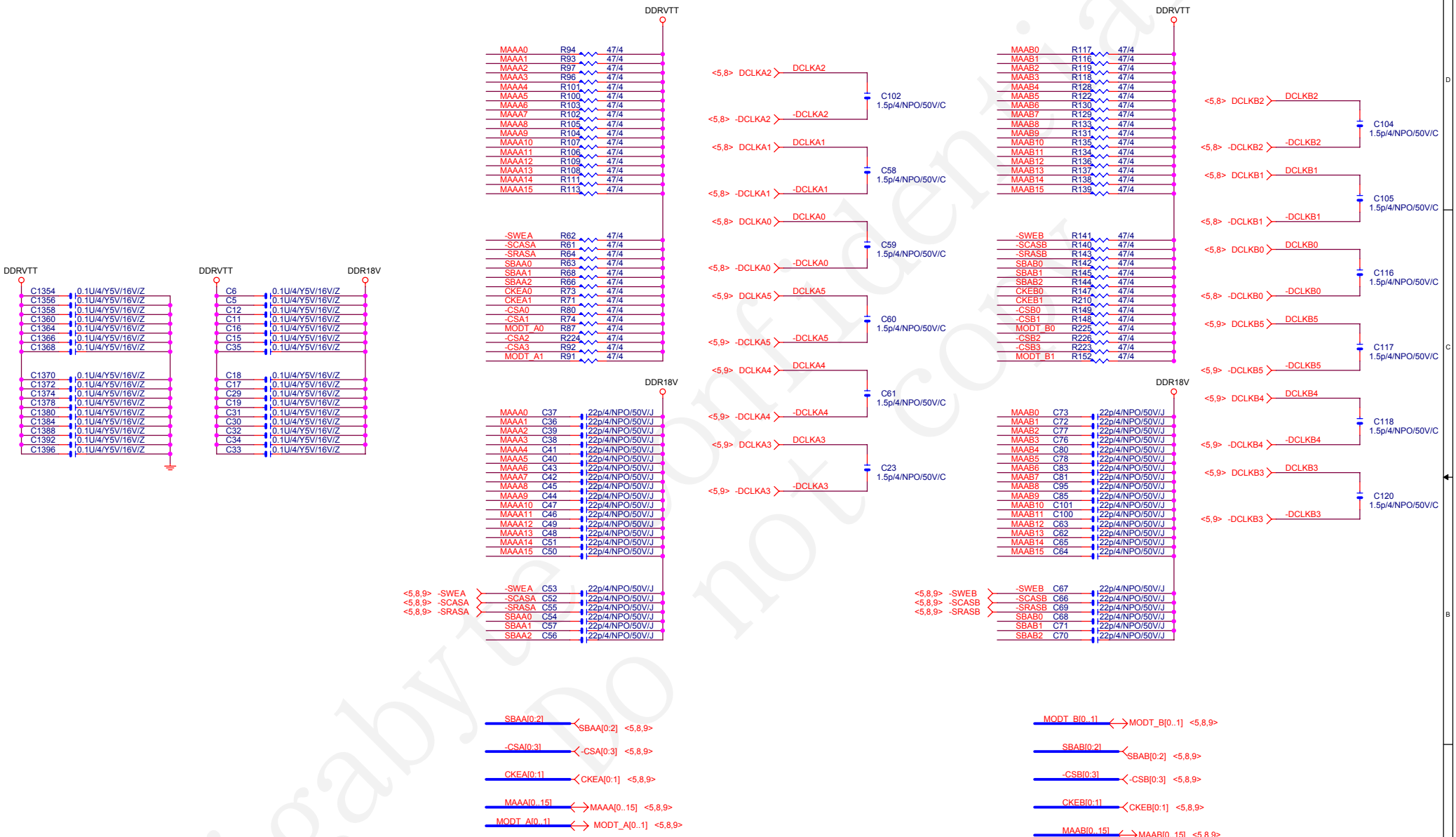

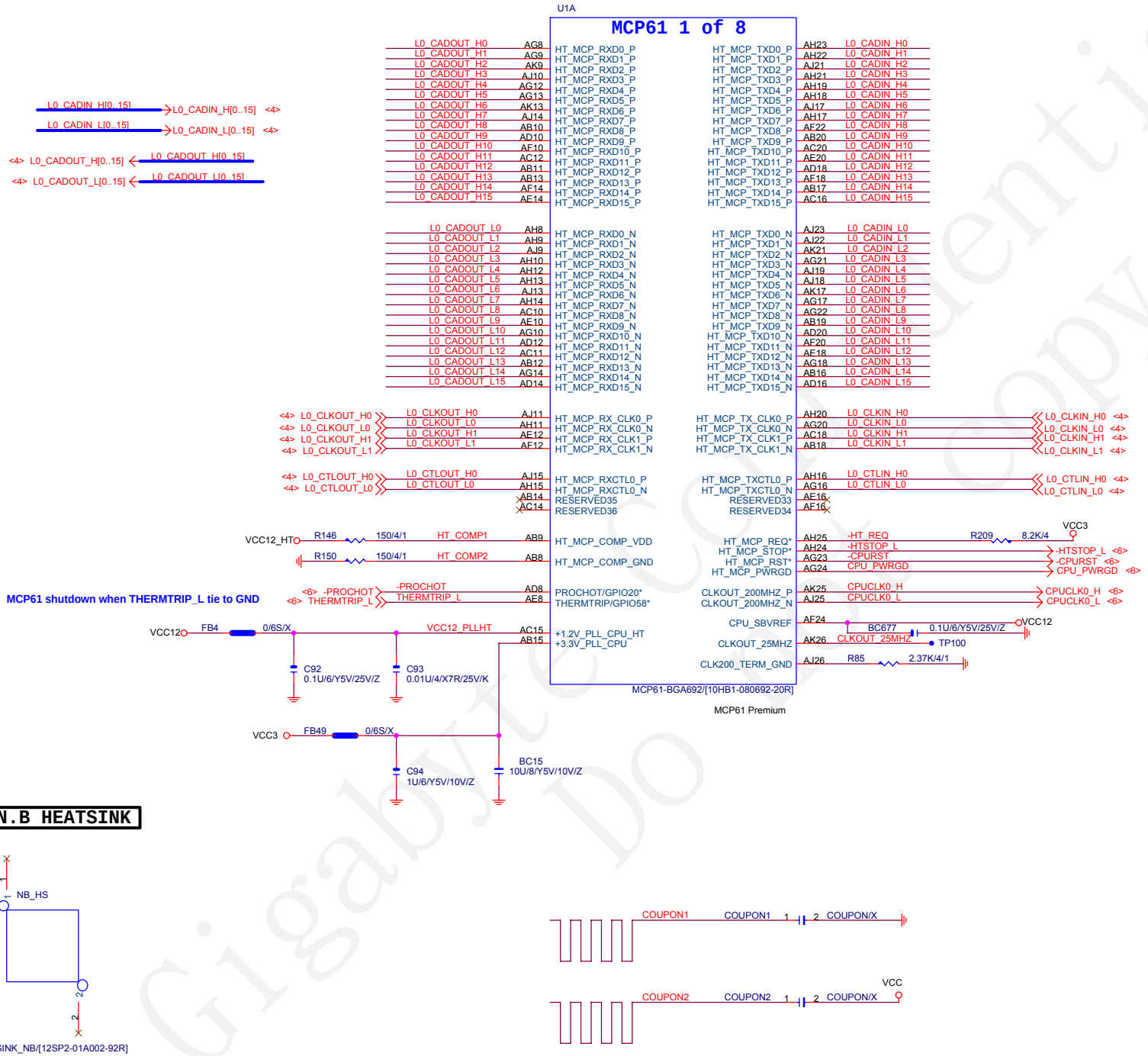

GIGABYTE			
Title	C51-HOST		
Size: Custom	Document Number: GA-M61PM-S2		Rev: 1.0
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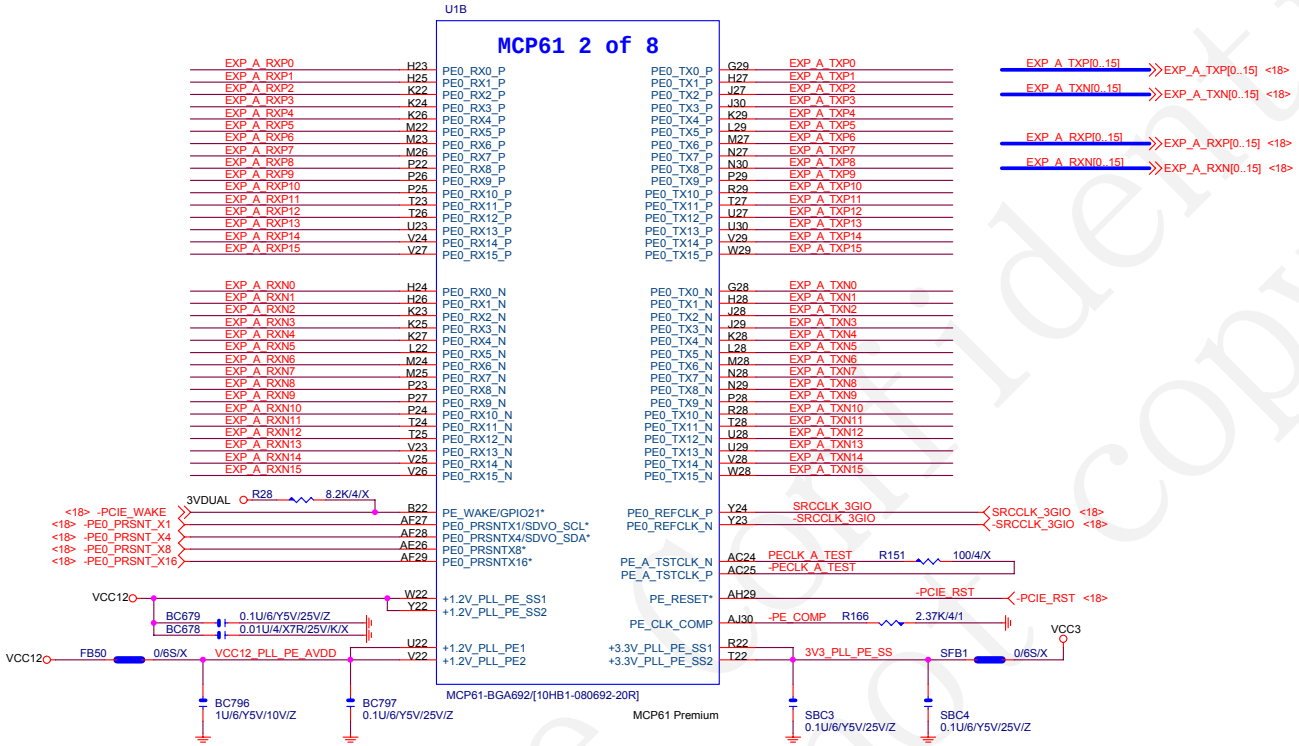

GIGABYTE

Title: C51-PCI EXPRESS

Size: Custom | Document Number: GA-M61PM-S2 | Rev: 1.0

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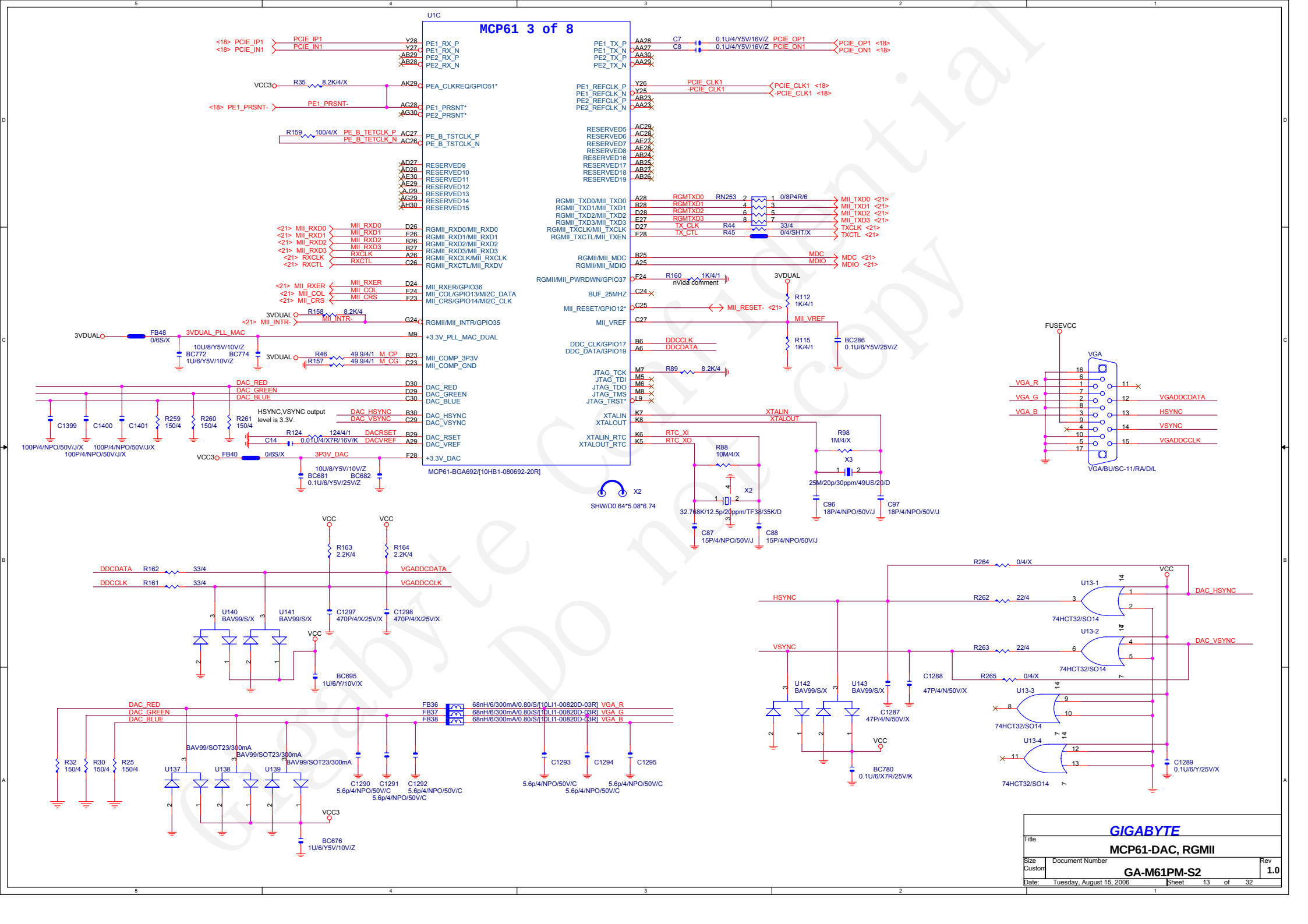
U1C
MCP61 3 of 8
MCP61-BGA692/[10HB1-080692-20R]
PCIE_IP1
PCIE_IN1
PE1_RX_P
PE1_RX_N
PE2_RX_P
PE2_RX_N
PE1_TX_P
PE1_TX_N
PE2_TX_P
PE2_TX_N
PCIE_OP1
PCIE_ON1
PE1_REFCLK_P
PE1_REFCLK_N
PE2_REFCLK_P
PE2_REFCLK_N
PCIE_CLK1
-PCIE_CLK1
PEA_CLKREQ/GPIO51*
PE1_PRSNT-
PE1_PRSNT*
PE2_PRSNT*
PE_B_TETCLK_P
PE_B_TETCLK_N
PE_B_TSTCLK_P
PE_B_TSTCLK_N
RESERVED5
RESERVED6
RESERVED7
RESERVED8
RESERVED16
RESERVED17
RESERVED18
RESERVED19
RESERVED9
RESERVED10
RESERVED11
RESERVED12
RESERVED13
RESERVED14
RESERVED15
RGMII_TXD0/MII_TXD0
RGMII_TXD1/MII_TXD1
RGMII_TXD2/MII_TXD2
RGMII_TXD3/MII_TXD3
RGMII_TXCLK/MII_TXCLK
RGMII_TXCTL/MII_TXEN
RGMII_RXD0/MII_RXD0
RGMII_RXD1/MII_RXD1
RGMII_RXD2/MII_RXD2
RGMII_RXD3/MII_RXD3
RGMII_RXCLK/MII_RXCLK
RGMII_RXCTL/MII_RXDV
RGMII/MII_MDC
RGMII/MII_MDIO
RGMII/MII_PWRDWN/GPIO37
MII_RXER/GPIO36
MII_COL/GPIO13/MI2C_DATA
MII_CRS/GPIO14/MI2C_CLK
RGMII/MII_INTR/GPIO35
BUF_25MHZ
MII_RESET/GPIO12*
MII_VREF
+3.3V_PLL_MAC_DUAL
MII_COMP_3P3V
MII_COMP_GND
DDC_CLK/GPIO17
DDC_DATA/GPIO19
JTAG_TCK
JTAG_TDI
JTAG_TDO
JTAG_TMS
JTAG_TRST*
XTALIN
XTALOUT
XTALIN_RTC
XTALOUT_RTC
RTC_XI
RTC_XO
DAC_RED
DAC_GREEN
DAC_BLUE
DAC_HSYNC
DAC_VSYNC
DAC_RSET
DAC_VREF
+3.3V_DAC
3VDUAL
3VDUAL_PLL_MAC
VCC3
VCC
FUSEVCC
VGA
VGA/BU/SC-11/RA/D/L
VGA_R
VGA_G
VGA_B
VGADDCDATA
VGADDCCLK
HSYNC
VSYNC
DDCDATA
DDCCLK
MII_TXD0
MII_TXD1
MII_TXD2
MII_TXD3
TXCLK
TXCTL
MDC
MDIO
MII_RXD0
MII_RXD1
MII_RXD2
MII_RXD3
RXCLK
RXCTL
MII_RXER
MII_COL
MII_CRS
MII_INTR-
MII_RESET-
MII_VREF
HSYNC,VSYNC output level is 3.3V.
SHW/D0.64*5.08*6.74
32.768K/12.5p/20ppm/TF38/35K/D
25M/20p/30ppm/49US/20/D
74HCT32/SO14
BAV99/SOT23/300mA
68nH/6/300mA/0.80/S/[10LI1-00820D-03R]
GIGABYTE
MCP61-DAC, RGMII
GA-M61PM-S2
1.0
Tuesday, August 15, 2006
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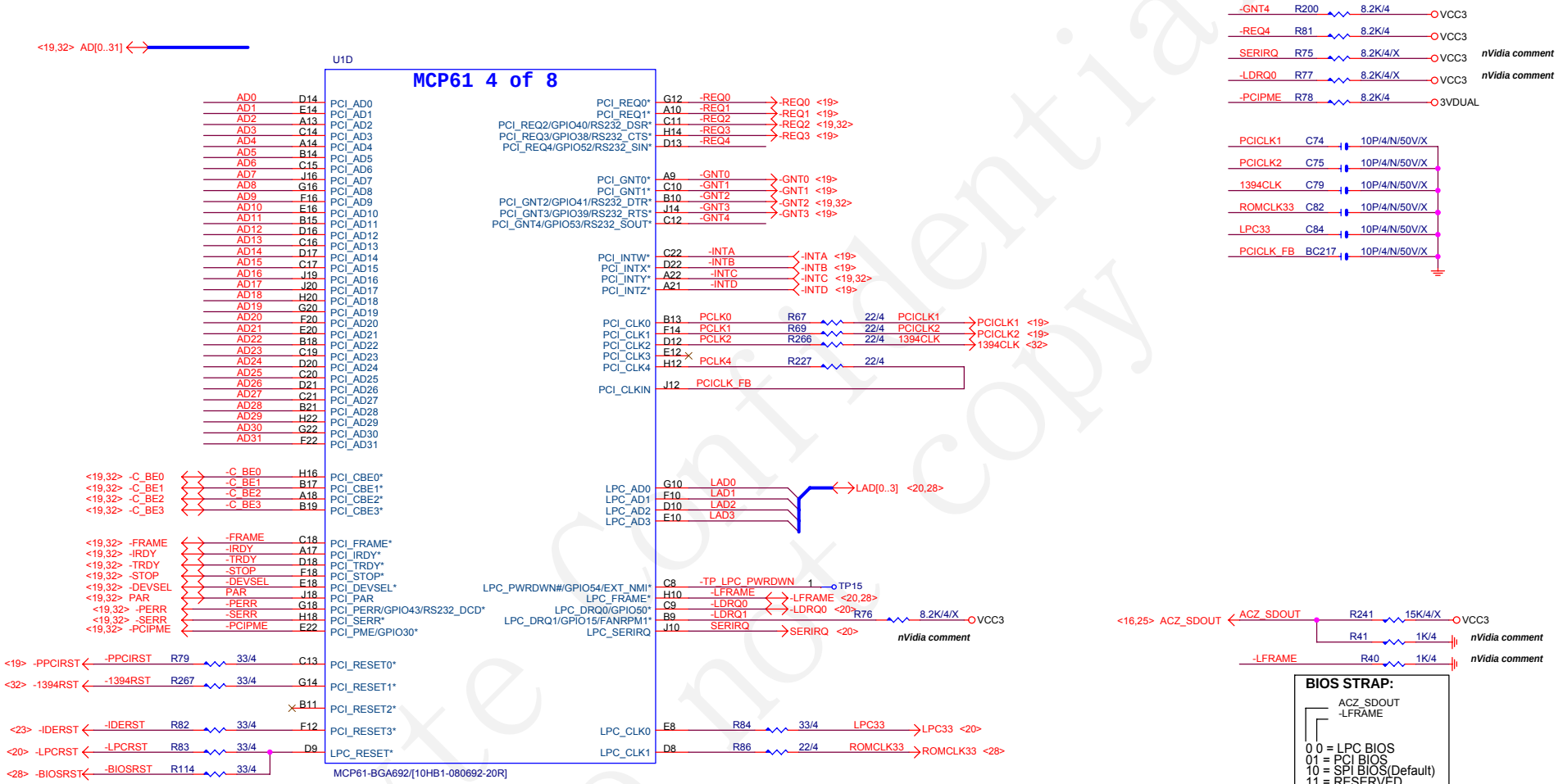

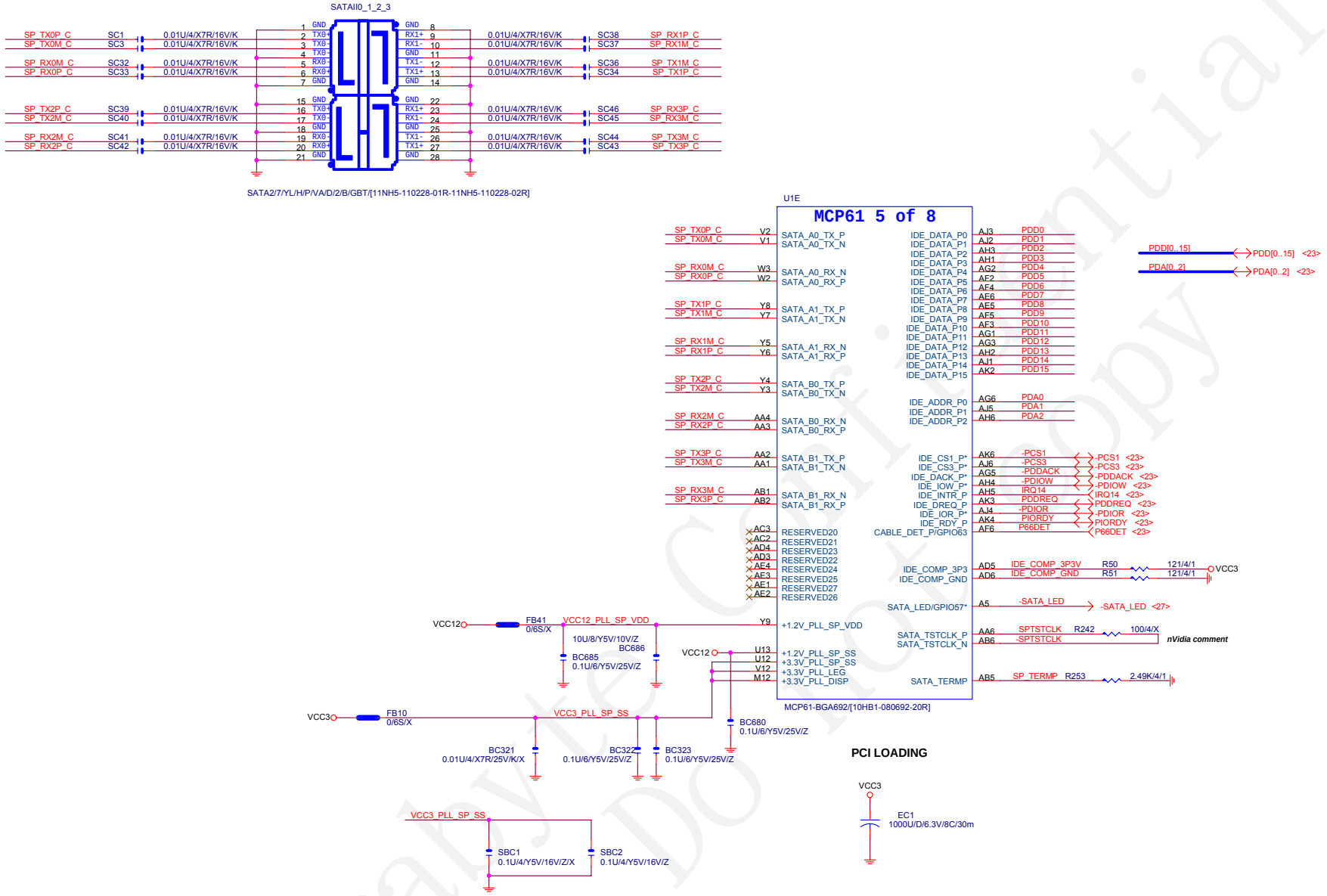

GIGABYTE			
Title	MCP51-SATA IDE		
Size: Custom	Document Number: GA-M61PM-S2		Rev: 1.0
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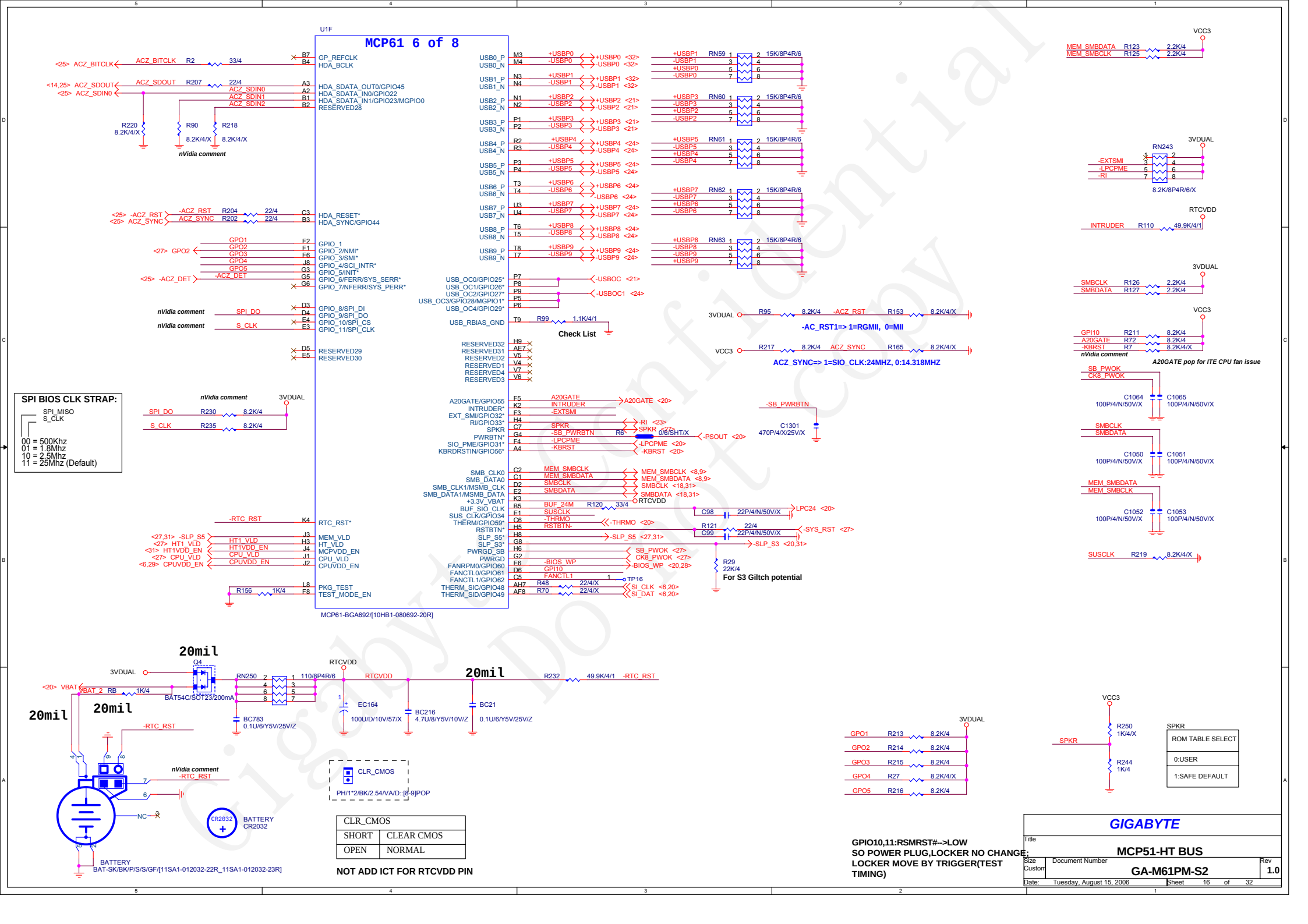
U1F
MCP61 6 of 8
MCP61-BGA692/[10HB1-080692-20R]
SPI BIOS CLK STRAP:
SPI_MISO
S_CLK
00 = 500Khz
01 = 1.8Mhz
10 = 2.5Mhz
11 = 25Mhz (Default)
Check List
-AC_RST1=> 1=RGMII, 0=MII
ACZ_SYNC=> 1=SIO_CLK:24MHZ, 0:14.318MHZ
A20GATE pop for ITE CPU fan issue
For S3 Giltch potential
20mil
BATTERY
BAT-SK/BK/P/S/GF/[11SA1-012032-22R_11SA1-012032-23R]
CLR_CMOS
PH/1*2/BK/2.54/VA/D::[8-9]POP
CLR_CMOS
SHORT CLEAR CMOS
OPEN NORMAL
NOT ADD ICT FOR RTCVDD PIN
GPIO10,11:RSMRST#-->LOW
SO POWER PLUG,LOCKER NO CHANGE;
LOCKER MOVE BY TRIGGER(TEST TIMING)
SPKR
ROM TABLE SELECT
0:USER
1:SAFE DEFAULT
GIGABYTE
MCP51-HT BUS
GA-M61PM-S2
Rev 1.0
Tuesday, August 15, 2006
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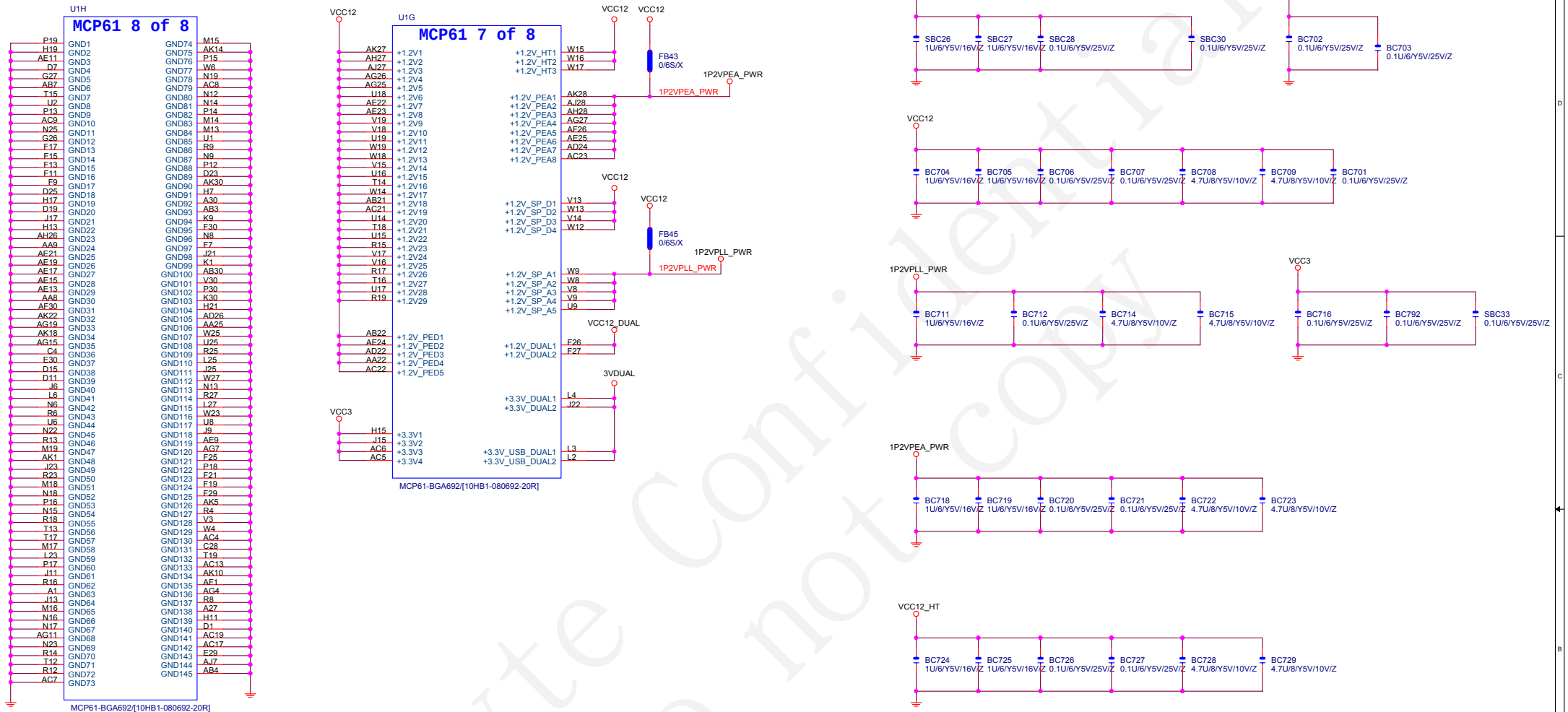

GIGABYTE

Title	MCP51-RGMII	
Size: Custom	Document Number: GA-M61PM-S2	Rev: 1.0
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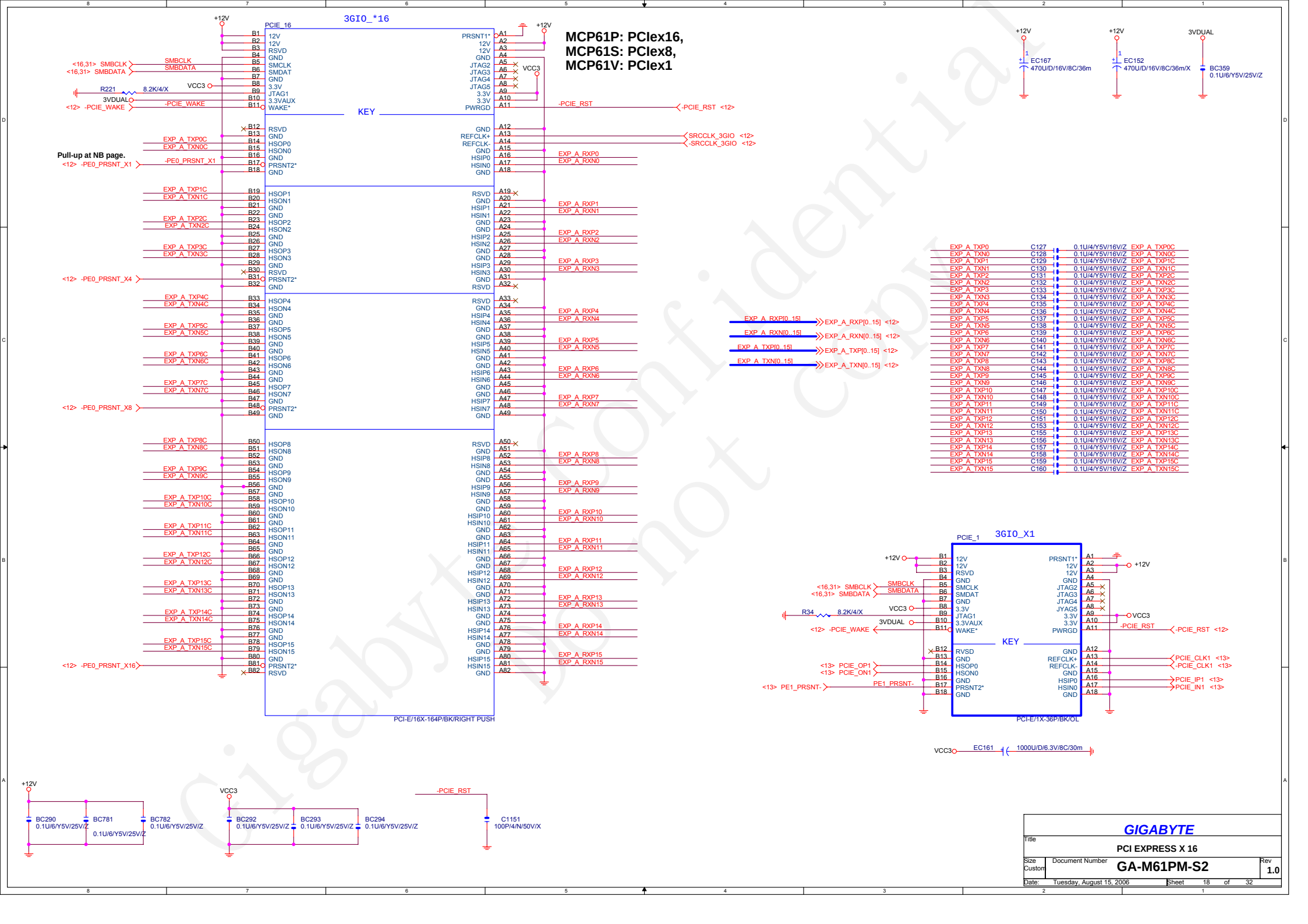
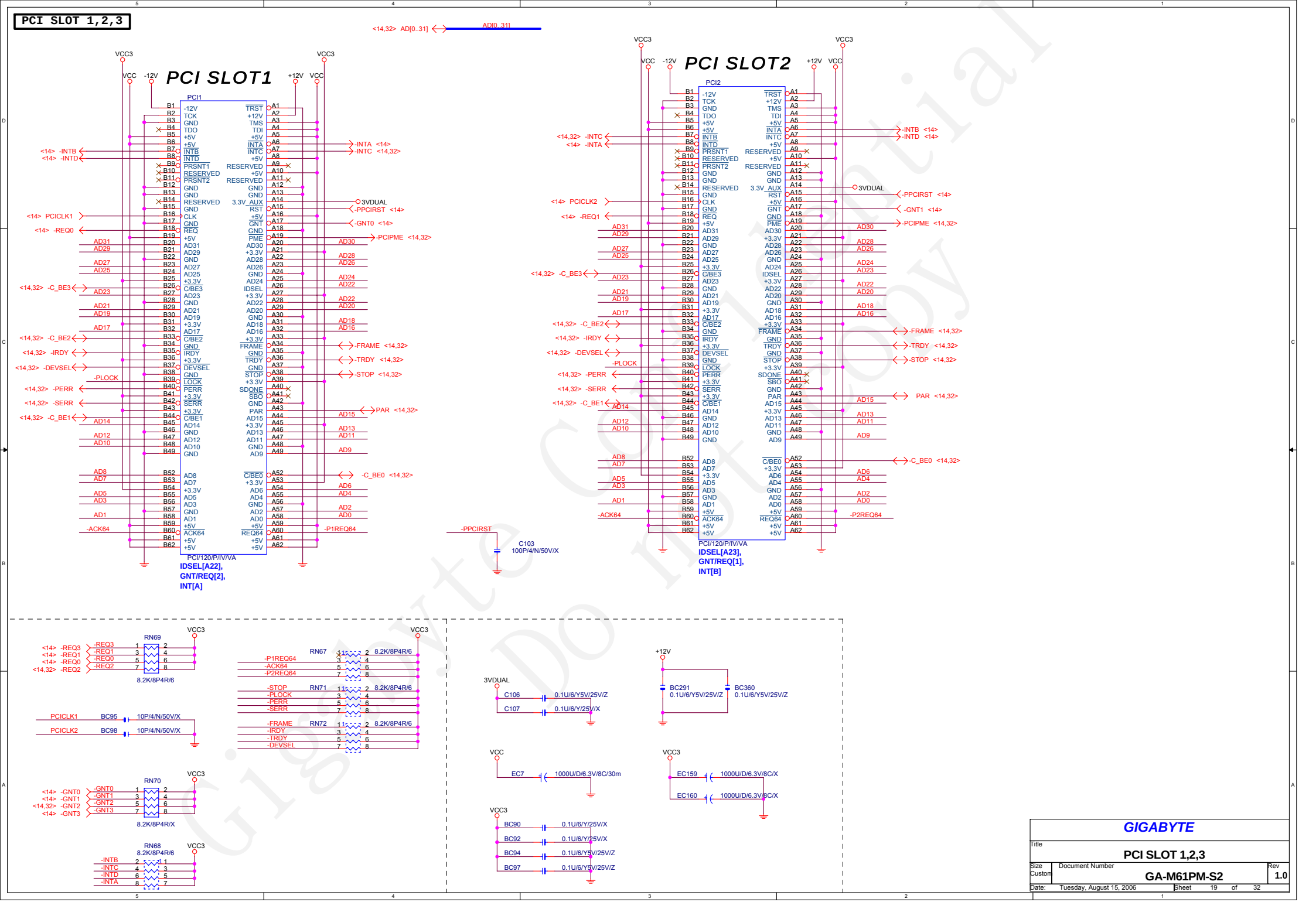


PCI SLOT 1,2,3



GIGABYTE		
Title	PCI SLOT 1,2,3	
Size: Custom	Document Number: GA-M61PM-S2	Rev: 1.0
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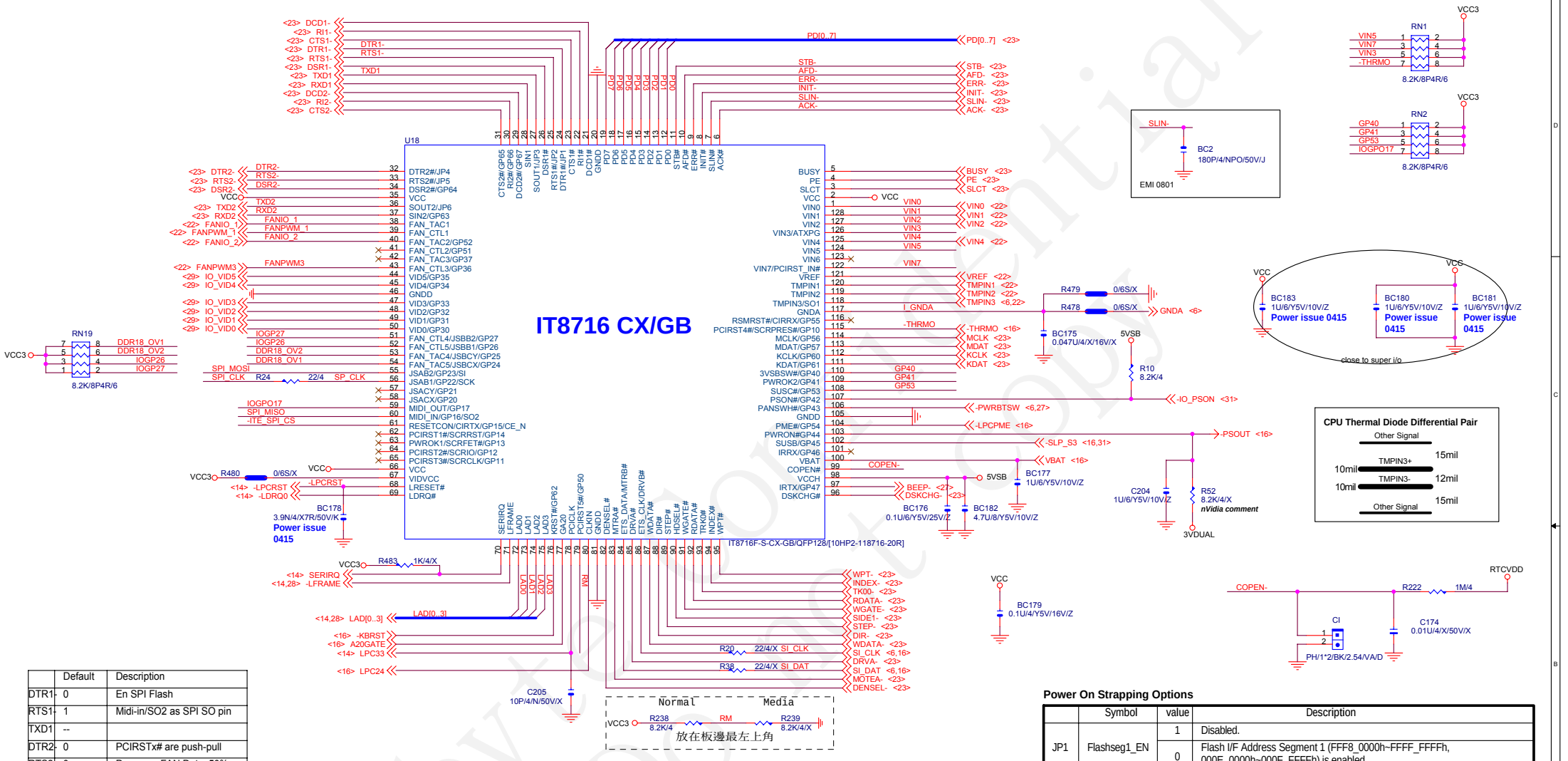

	Default	Description
DTR1-	0	En SPI Flash
RTS1-	1	Midi-in/SO2 as SPI SO pin
TXD1	--	
DTR2-	0	PCIRSTx# are push-pull
RTS2-	0	Power-on FAN Duty=50%
TXD2	0	VID threshold is 0.8V/0.4V

IT8712 H/W Strap

ON: EN SPI

DTR1- R240 680/4

RTS1- R243 680/4/X VCC 75232 internal P.U.

TXD1 R245 680/4/X

R246 8.2K/4/X VCC

DTR2- R247 680/4

R248 8.2K/4/X VCC

RTS2 R249 680/4

TXD2 R251 680/4

If 75232 is connected, please use 680 ohm to be the pull down resistor value. Since powered by 12V, 75232 has a very strong internal pull-up. It is hard to be pulled low. (Please see specification for detail of power on strapping setting)

Power On Strapping Options

	Symbol	value	Description
JP1	Flashseg1_EN	1	Disabled.
		0	Flash I/F Address Segment 1 (FFF8_0000h~FFFF_FFFFh, 000E_0000h~000F_FFFFh) is enabled
JP2	SerFlh_SO_SEL	1	FLH_SO2 is selected as the Serial Flash I/F SO pin.
		0	FLH_SO1 is selected as the Serial Flash I/F SO pin.
JP3	CHIP_SEL	--	Chip selection in configuration.
JP4	BUF_SEL	1	The output buffers of PCIRST1#, PCIRST2#, PCIRST3#, PCIRST4# and PCIRST5# are enhanced open-drain. It drives high about 10~20 ns when the signal transits from low to high, and then Hi-Z.
		0	The output buffers are push-pull.
JP5	FAN_CTL_SEL	1	The default value of EC Index 15h / 16h / 17h is 00h
		0	The default value of EC Index 15h / 16h / 17h is 40h
JP6	VID_ISEL	1	The threshold voltage of VID is 2.0 / 0.8V
		0	The threshold voltage of VID is 0.8 / 0.4V

GIGABYTE

Title: ITE 8712 LPC IO

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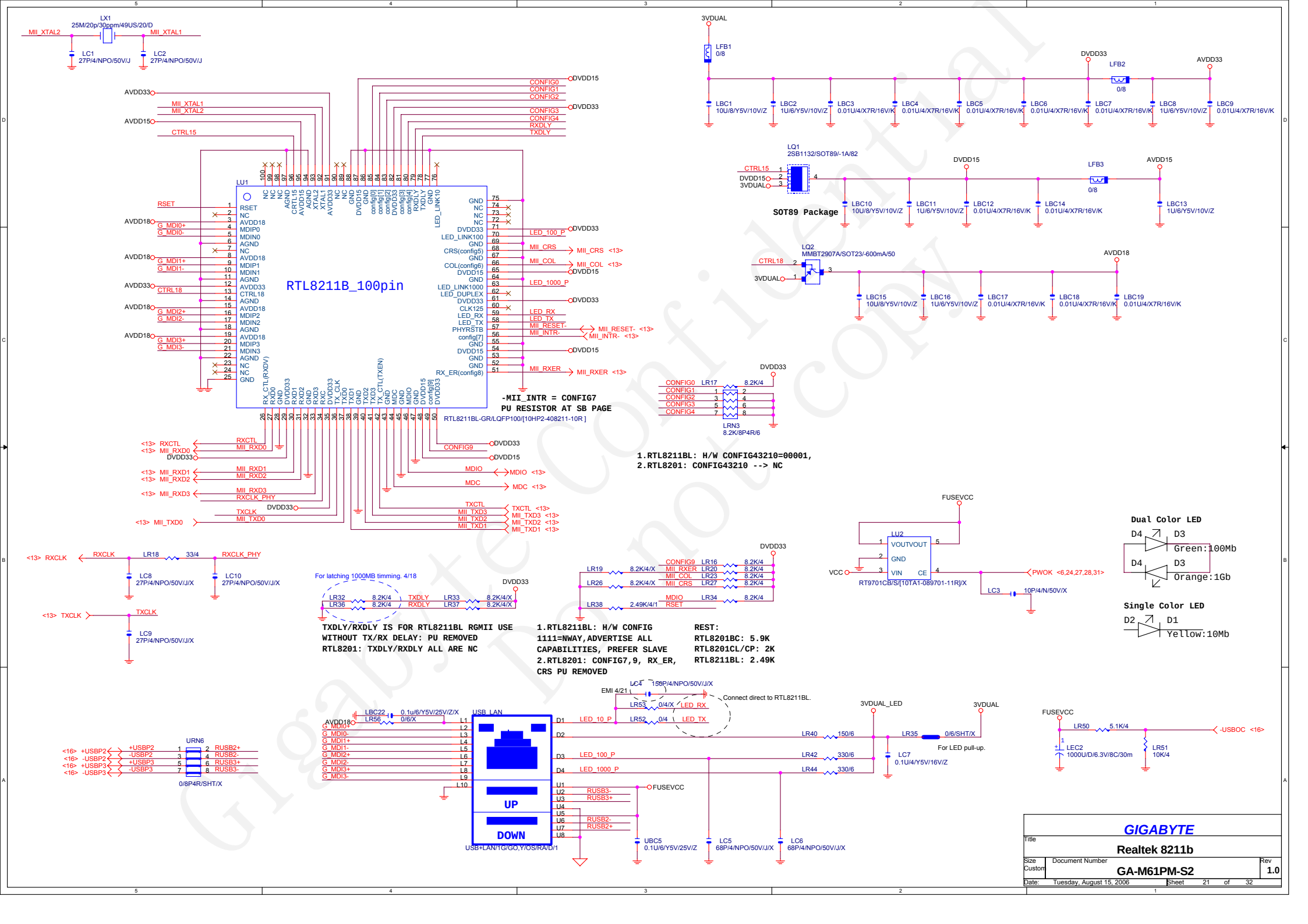
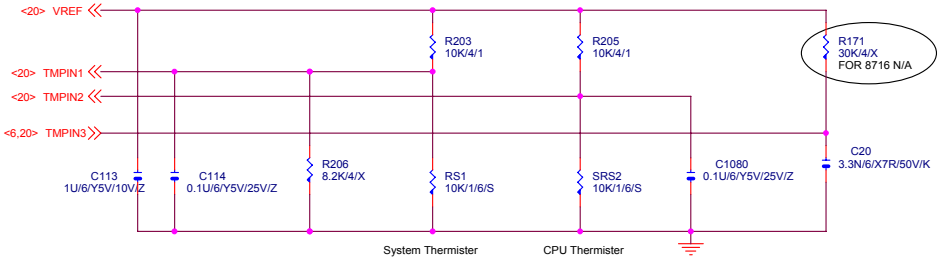
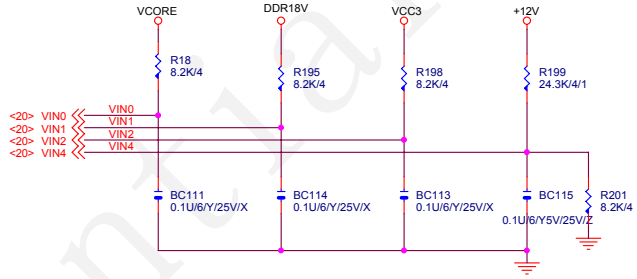
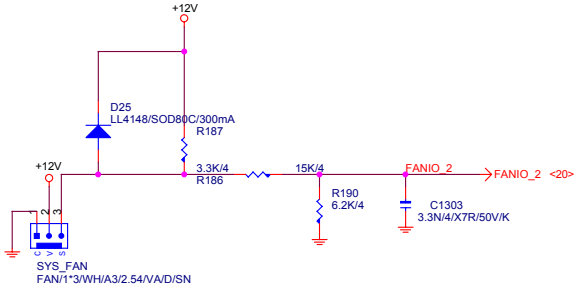


Hardware Monitor circuits

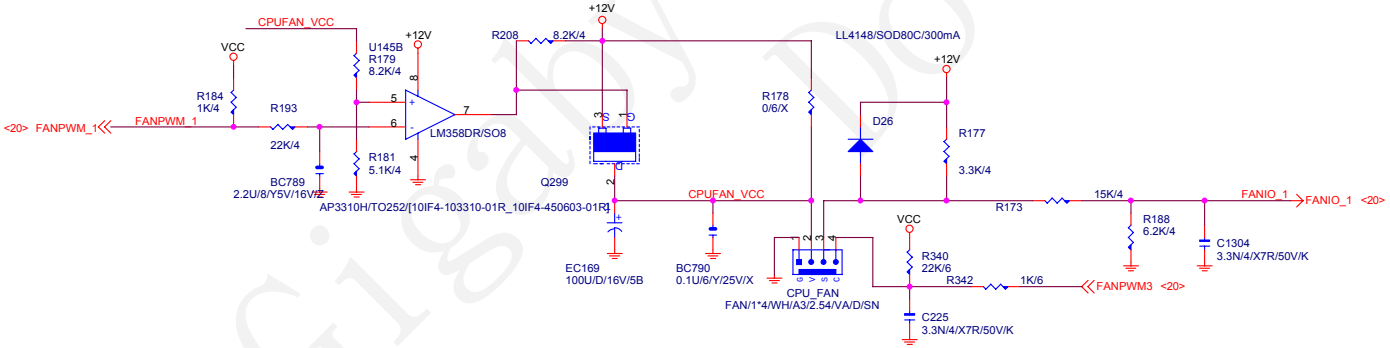




SYSTEM FAN



CPU FAN



GIGABYTE

Title: FAN/HWMO

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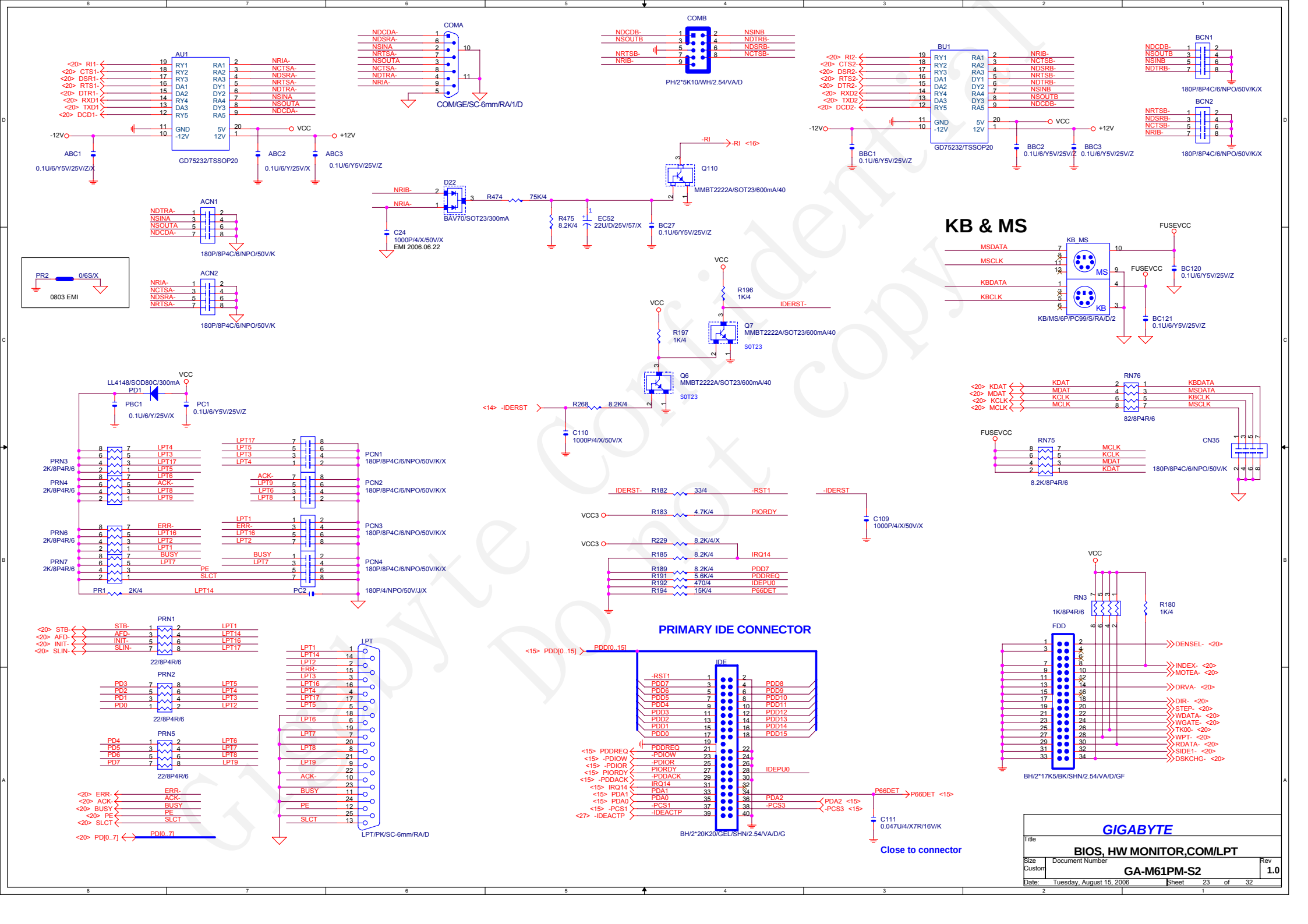

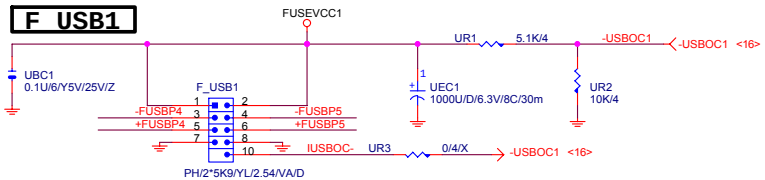

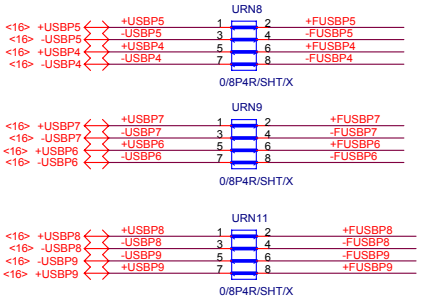

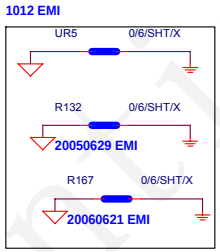

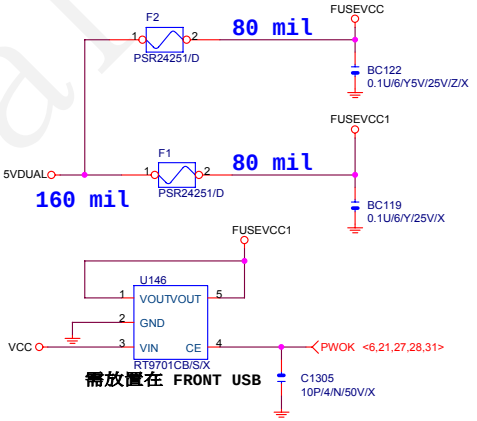

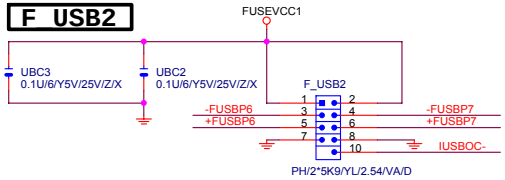

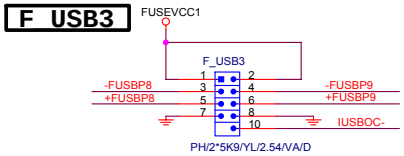

GIGABYTE

Title: USB PORT

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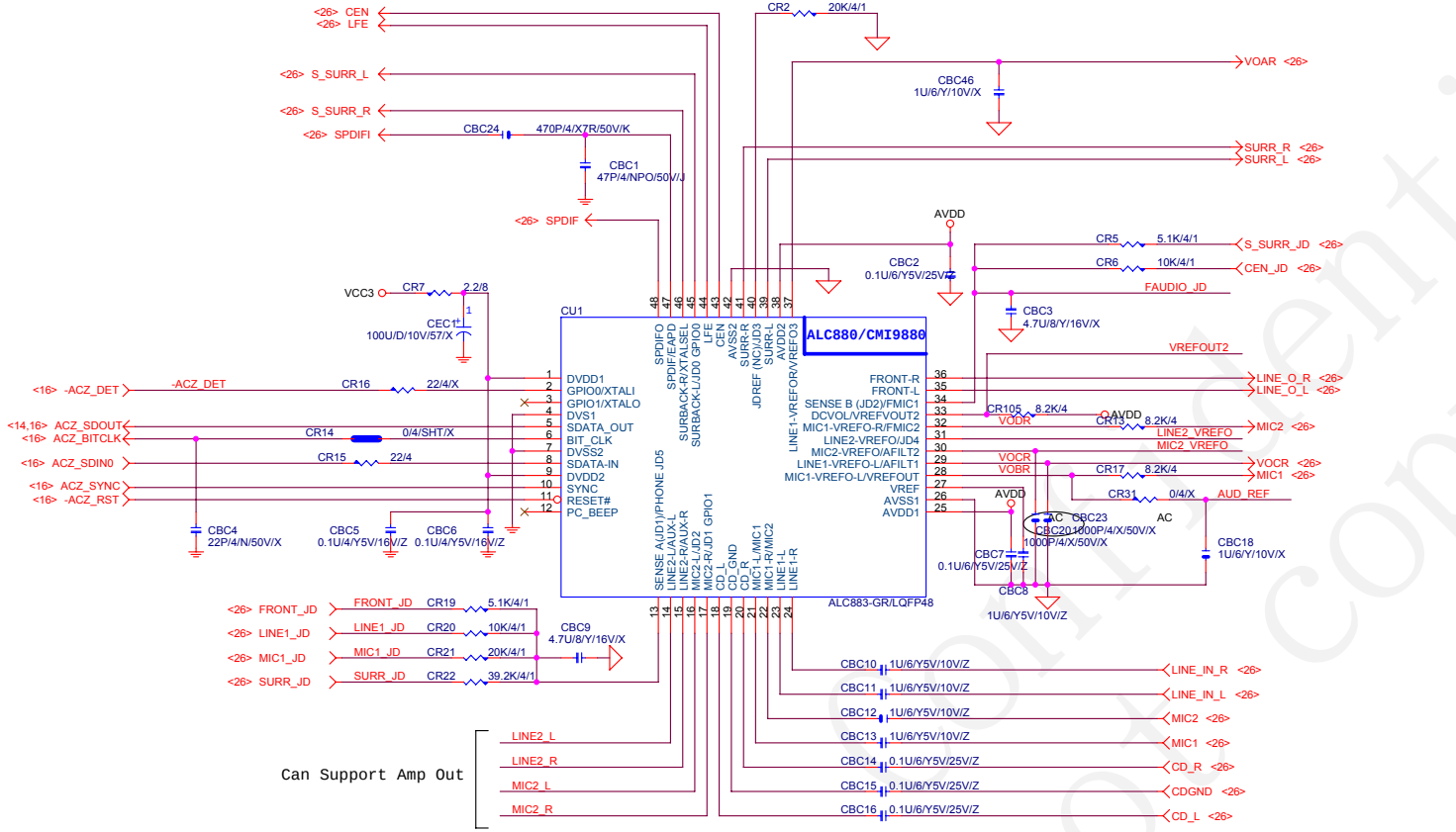

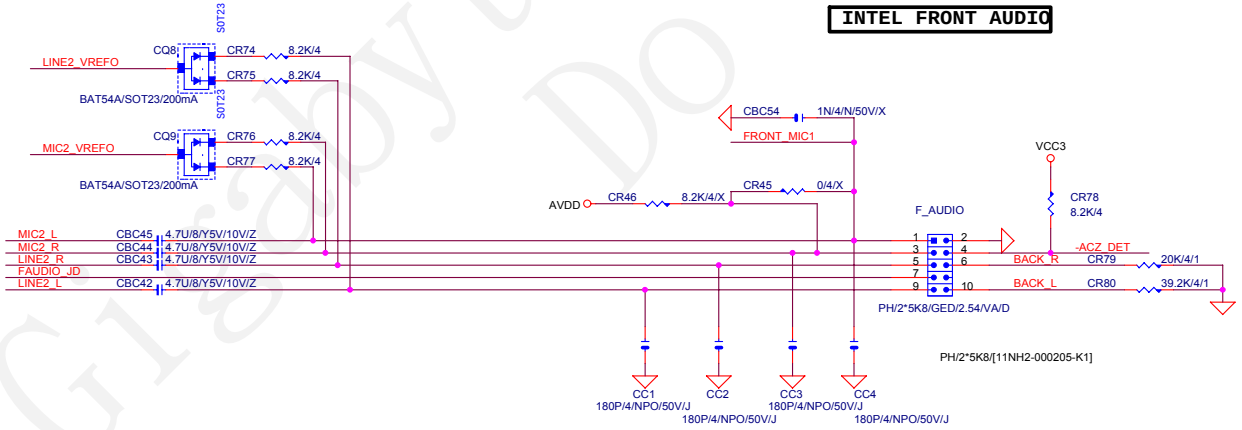

GIGABYTE		
Title	AC97 ALC658	
Size: Custom	Document Number: GA-M61PM-S2	Rev: 1.0
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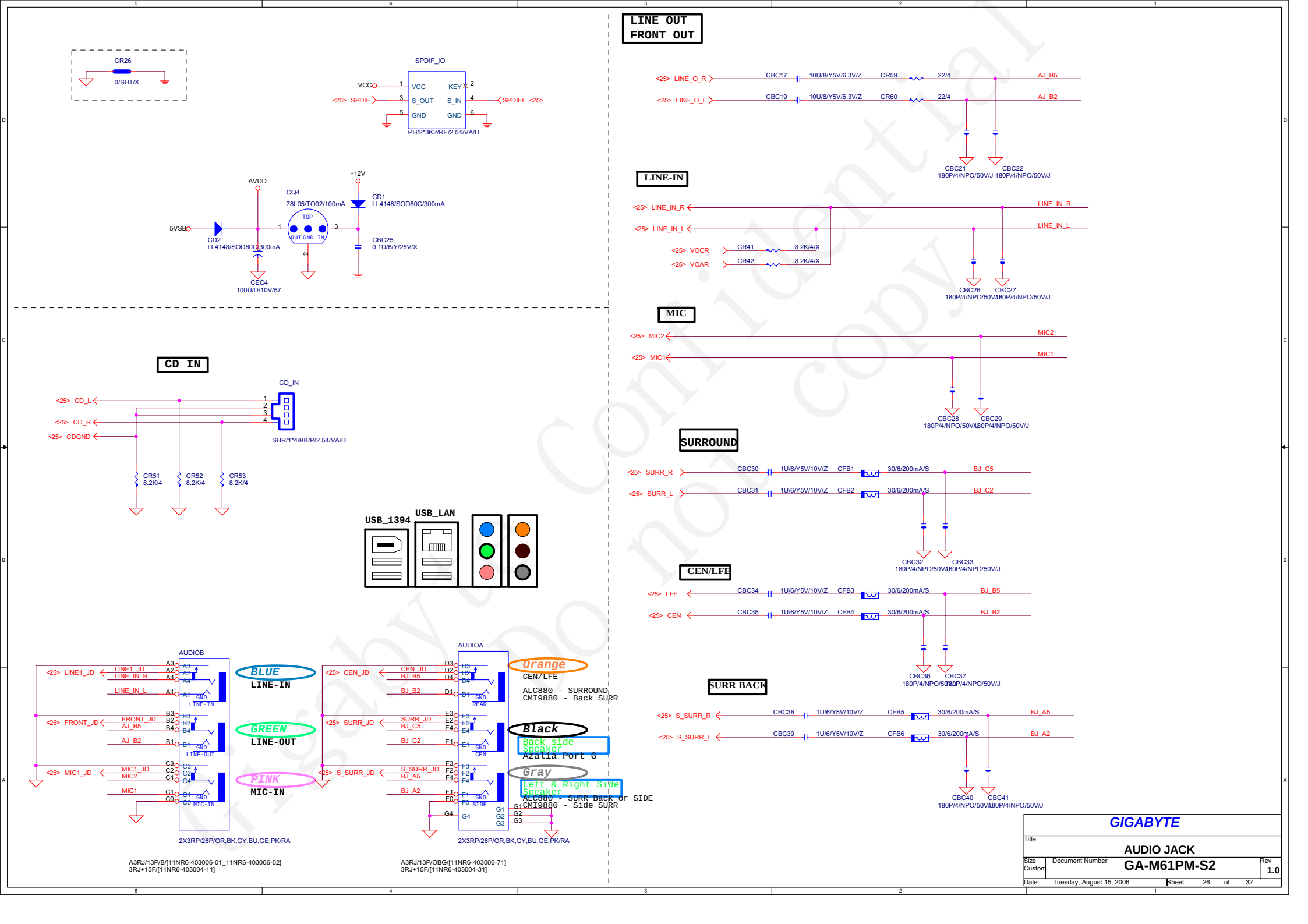

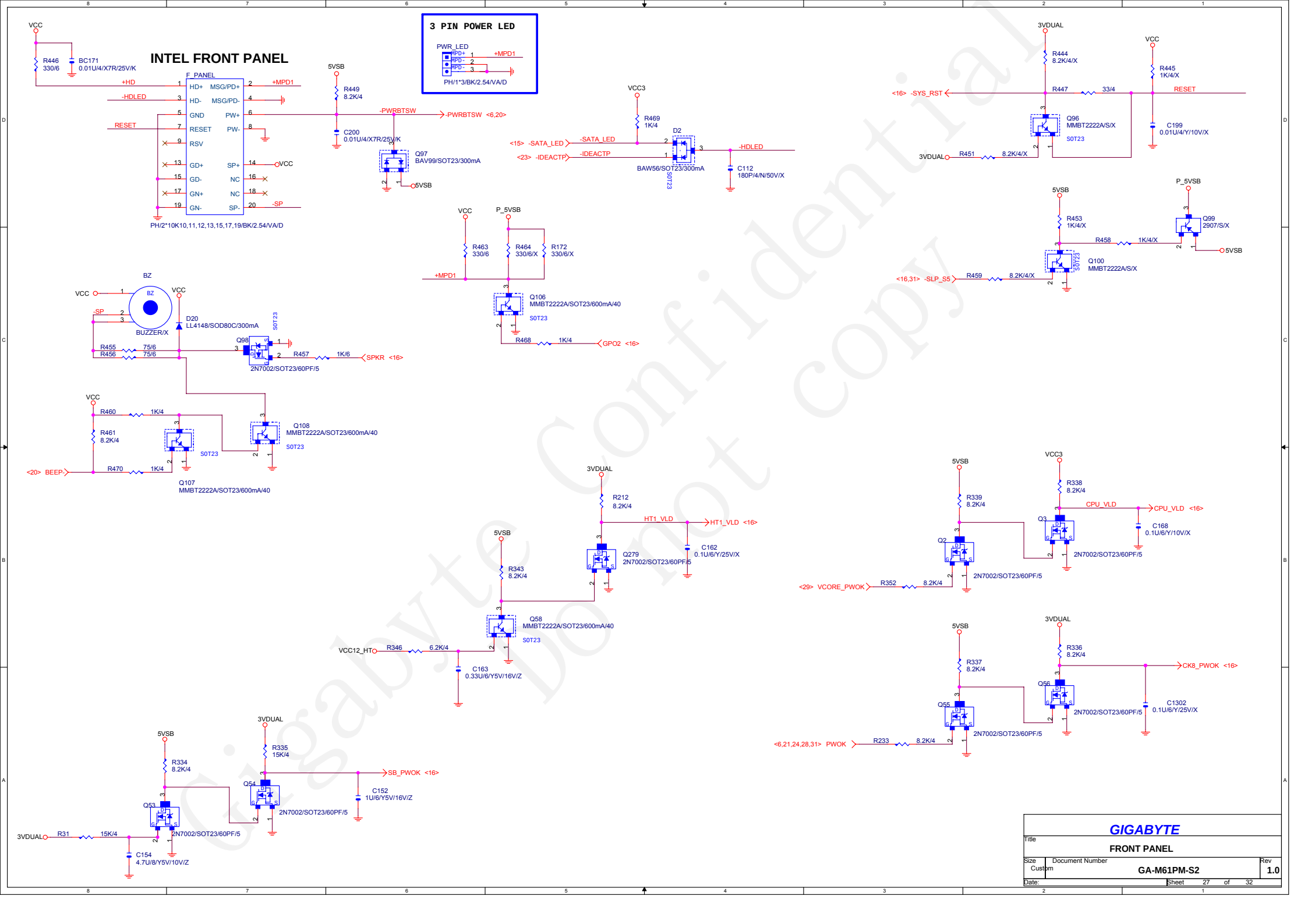
INTEL FRONT PANEL
3 PIN POWER LED
PWR_LED
PH/1*3/BK/2.54/VA/D
F_PANEL
PH/2*10K10,11,12,13,15,17,19/BK/2.54/VA/D
R446 330/6
BC171 0.01U/4/X7R/25V/K
R449 8.2K/4
C200 0.01U/4/X7R/25V/K
Q97 BAV99/SOT23/300mA
R469 1K/4
D2
BAW56/SOT23/300mA
C112 180P/4/N/50V/X
R444 8.2K/4/X
R445 1K/4/X
R447 33/4
Q96 MMBT2222A/S/X
C199 0.01U/4/Y/10V/X
R451 8.2K/4/X
R453 1K/4/X
R458 1K/4/X
Q99 2907/S/X
Q100 MMBT2222A/S/X
R459 8.2K/4/X
R463 330/6
R464 330/6/X
R172 330/6/X
Q106 MMBT2222A/SOT23/600mA/40
R468 1K/4
BUZZER/X
D20 LL4148/SOD80C/300mA
R455 75/6
R456 75/6
Q98 2N7002/SOT23/60PF/5
R457 1K/6
R460 1K/4
R461 8.2K/4
R470 1K/4
Q107 MMBT2222A/SOT23/600mA/40
Q108 MMBT2222A/SOT23/600mA/40
R212 8.2K/4
Q279 2N7002/SOT23/60PF/5
C162 0.1U/6/Y/25V/X
R343 8.2K/4
Q58 MMBT2222A/SOT23/600mA/40
R346 6.2K/4
C163 0.33U/6/Y5V/16V/Z
R338 8.2K/4
Q3 2N7002/SOT23/60PF/5
C168 0.1U/6/Y/10V/X
R339 8.2K/4
Q2 2N7002/SOT23/60PF/5
R352 8.2K/4
R336 8.2K/4
Q56 2N7002/SOT23/60PF/5
C1302 0.1U/6/Y/25V/X
R337 8.2K/4
Q55 2N7002/SOT23/60PF/5
R233 8.2K/4
R334 8.2K/4
Q53 2N7002/SOT23/60PF/5
R335 15K/4
Q54 2N7002/SOT23/60PF/5
C152 1U/6/Y5V/16V/Z
R31 15K/4
C154 4.7U/8/Y5V/10V/Z
-PWRBTSW -PWRBTSW <6,20>
-SATA_LED
-IDEACTP
-HDLED
-SYS_RST
RESET
SPKR <16>
GPO2 <16>
SLP_S5
CPU_VLD
HT1_VLD
VCORE_PWOK
PWOK
CK8_PWOK
SB_PWOK
BEEP
GIGABYTE
FRONT PANEL
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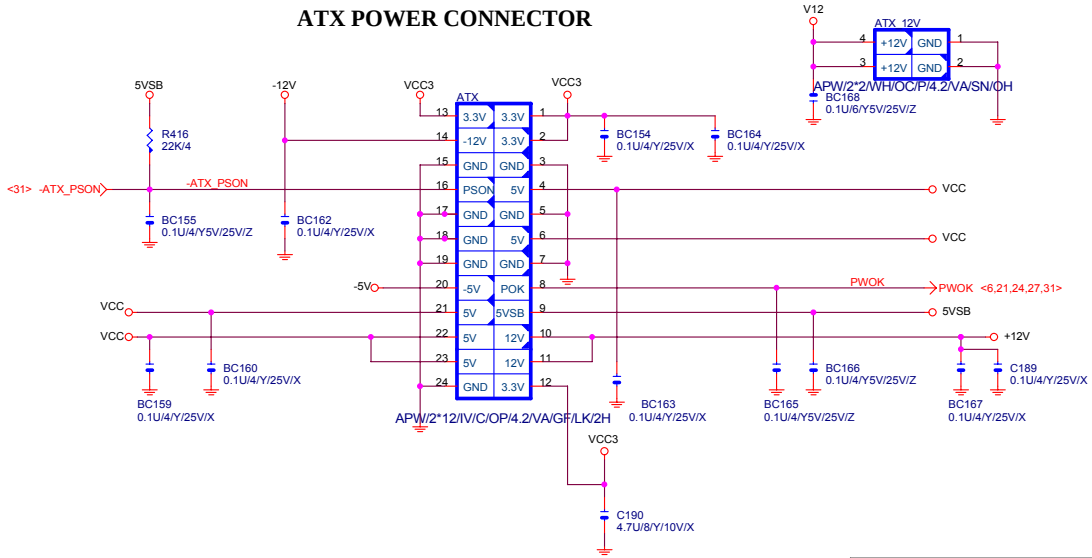
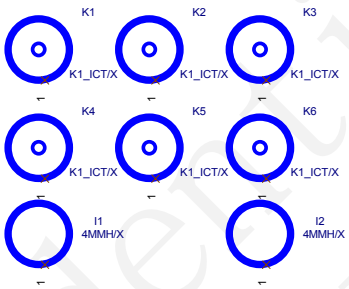
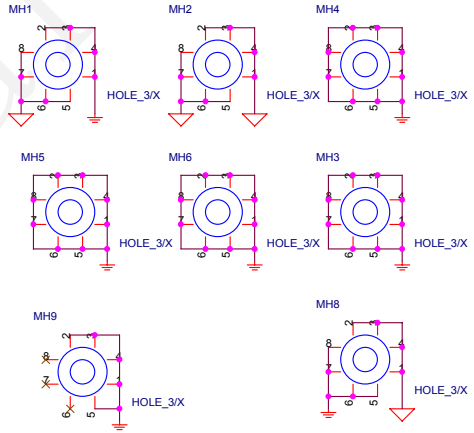
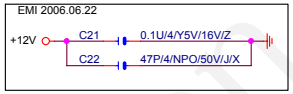
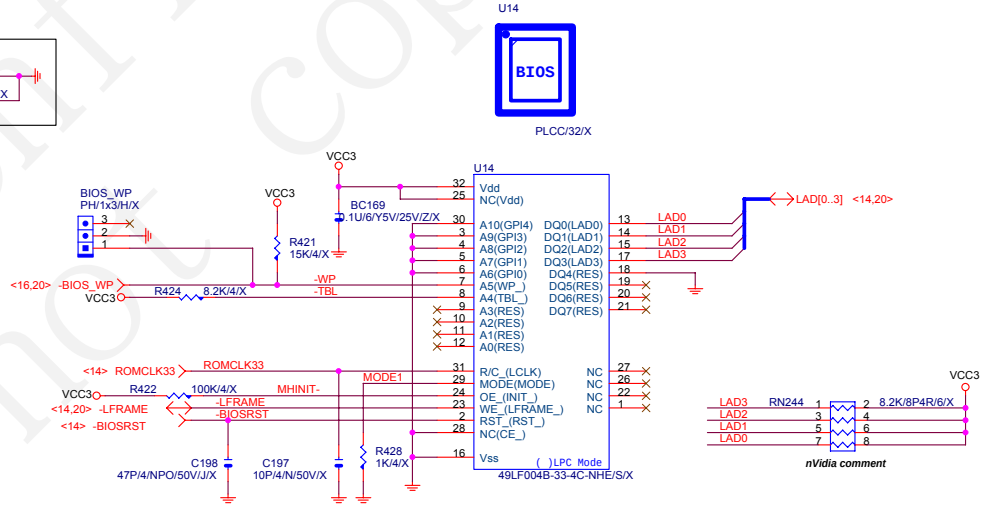
ATX POWER CONNECTOR











GIGABYTE

Title: Misc. PWR & ATX CONN

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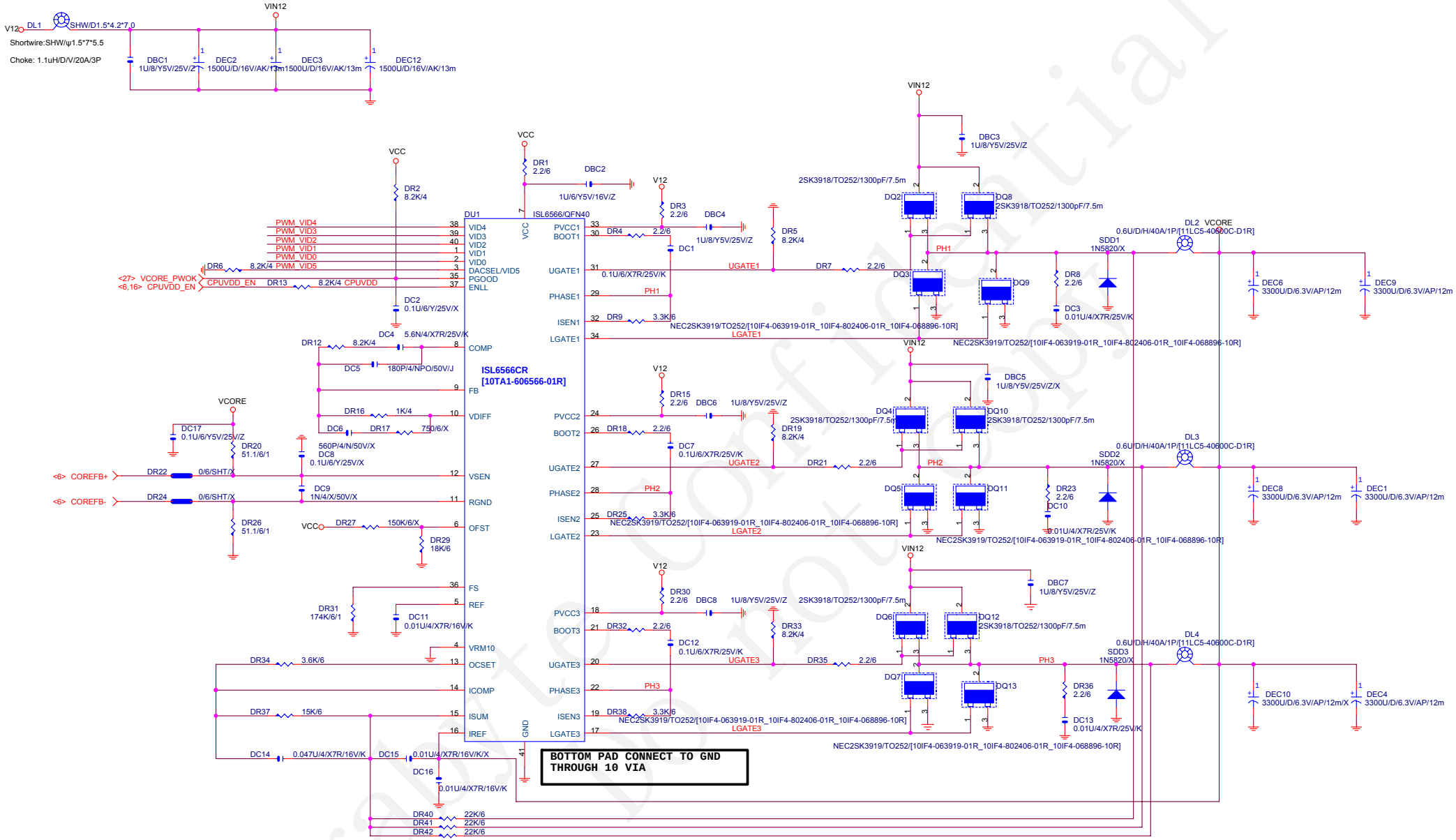

GIGABYTE

Title: VCORE (PWM ISL6559BC+6602B+6601B)

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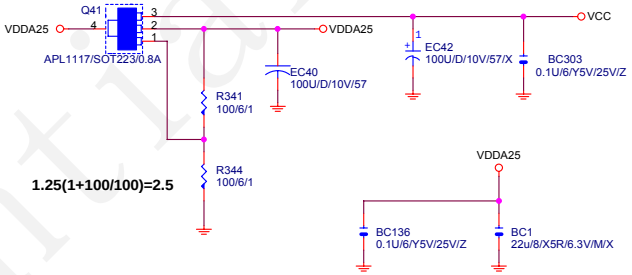

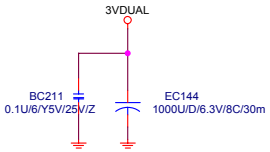

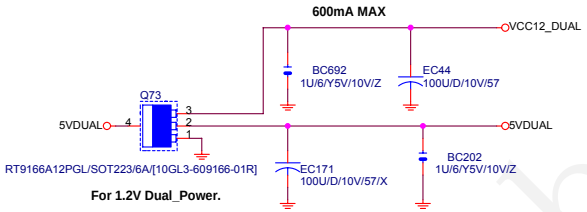

GIGABYTE		
Title: VCC12HT,VDDA25 POWER		
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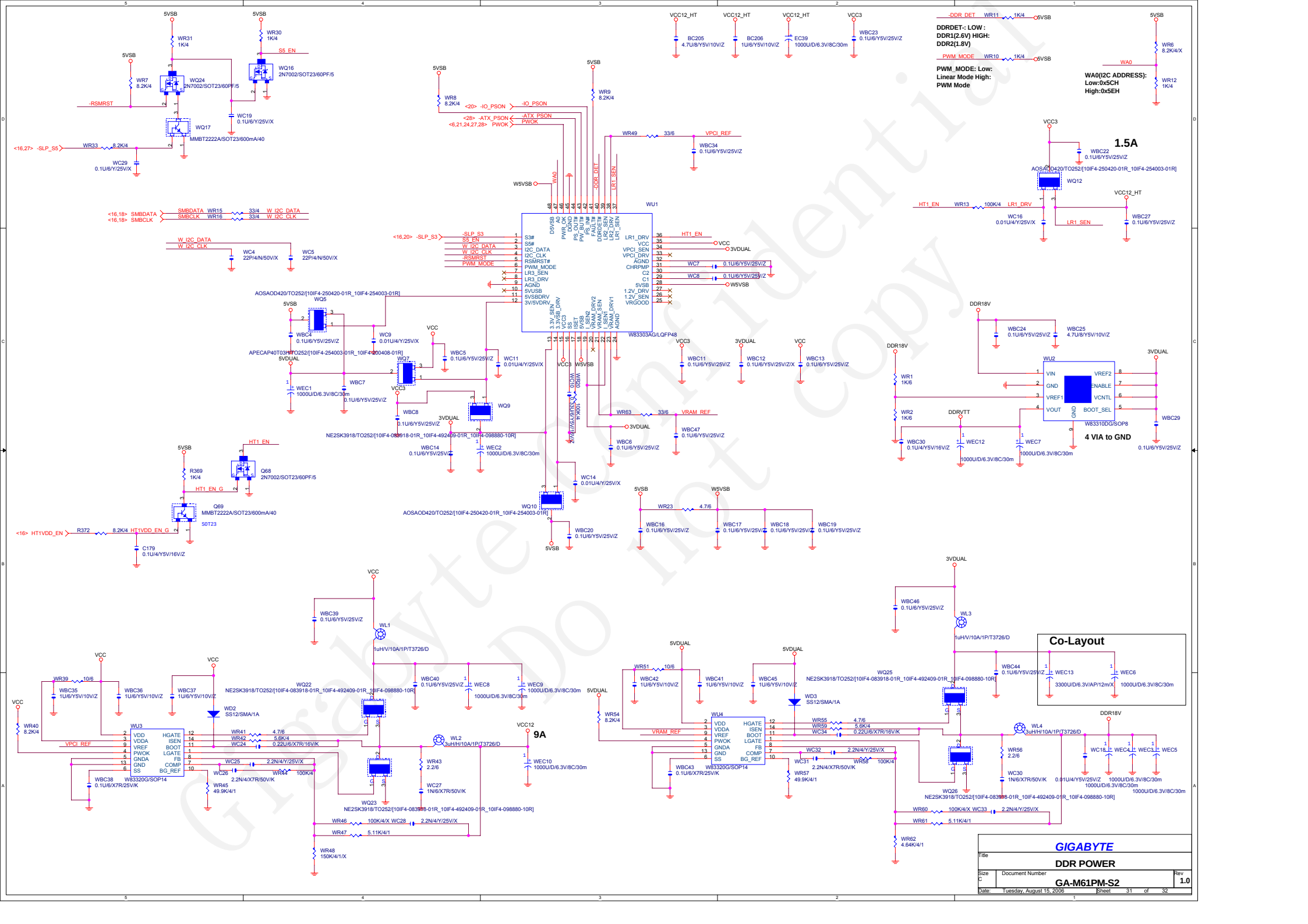
DDRDET-: LOW :
DDR1(2.6V) HIGH:
DDR2(1.8V)
PWM_MODE: Low:
Linear Mode High:
PWM Mode
WA0(I2C ADDRESS):
Low:0x5CH
High:0x5EH
1.5A
4 VIA to GND
9A
Co-Layout
GIGABYTE
DDR POWER
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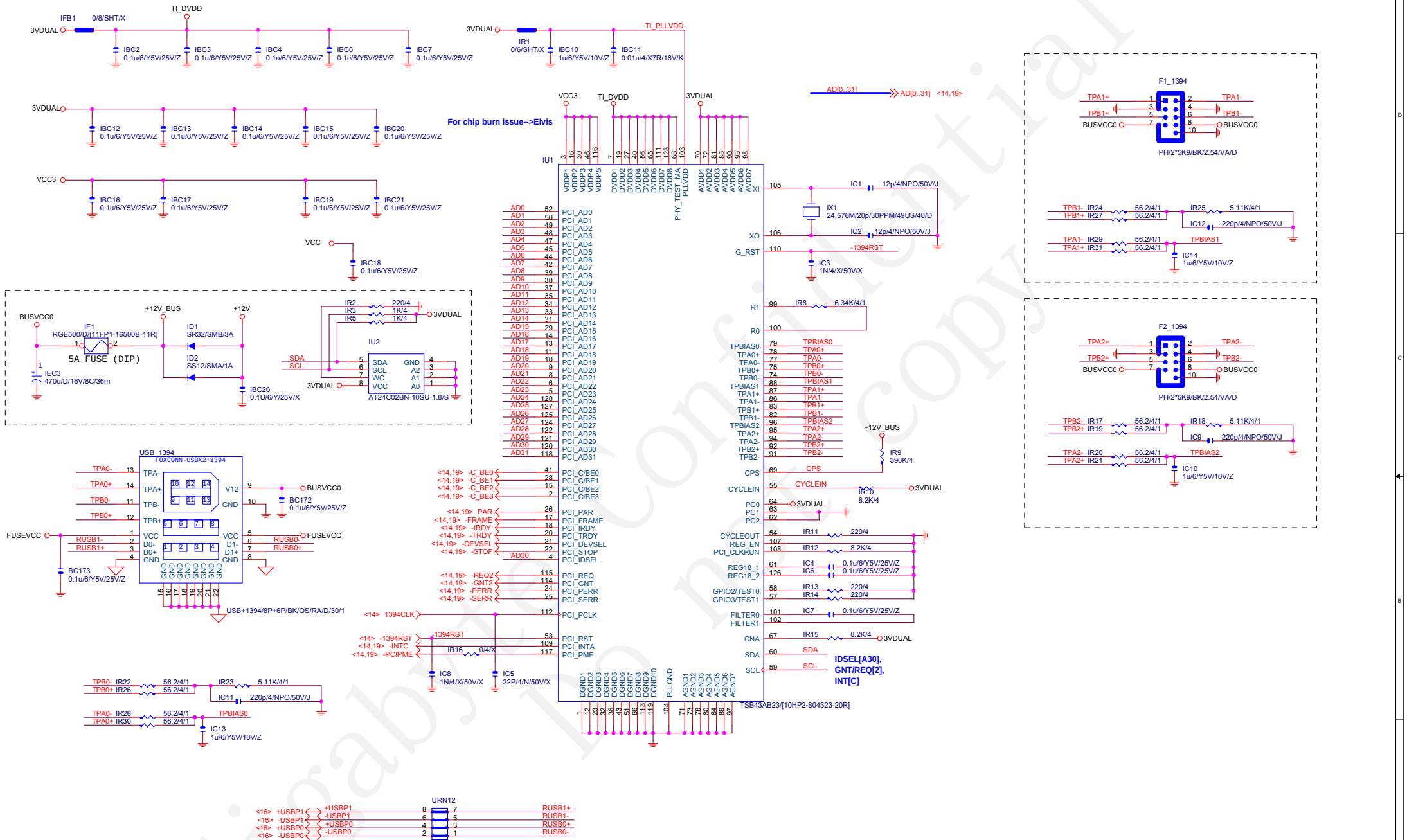

GIGABYTE		
Title	TSB43AB23A 1394A	
Size: Custom	Document Number: GA-M61PM-S2	Rev: 1.0
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