

1234

GIGABYTE GA-M59SLI-S4 Schematics

Revision:1.01

SHEET TITLE

SHEET TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	PROCESSOR HT INTERFACE
05	PROCESSOR DDR2 INTERFACE
06	PROCESSOR CONTROL & DEBUG
07	PROCESSOR POWER& GROUND
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09	DIMM A1,B1
10	DIMM TERMINATION
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12	C51XE(C51D) HT LINK
13	C51XE(C51D) PCI-E X16 (PE-A)
14	C51XE(C51D) PLL POWER
15	C51XE(C51D) POWER & GROUND
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23	MCP55P PCI
24	MCP55P PWR/GND
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26	PCI EXPRESS X16 SLOT 2

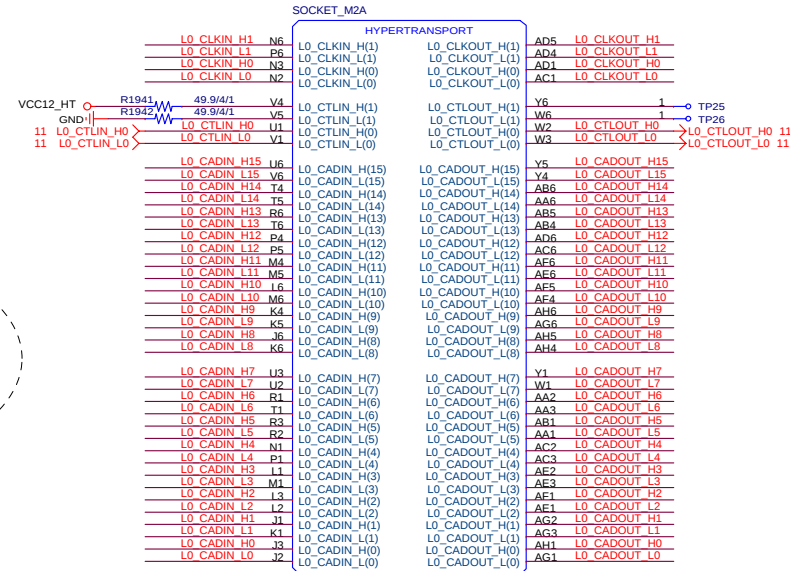
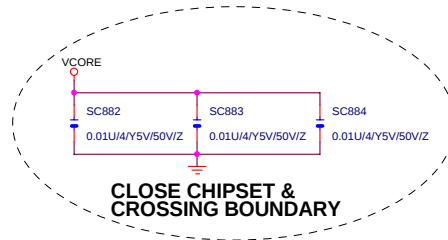
27	PCI EXPRESS X8
28	PCI EXPRESS X1 SLOT 1,2
29	PCI SLOT 1,2
30	FAN/HW MONITOR
31	IDE/FDD
32	KB_MS/FUSEVCC
33	VCORE POWER (ISL6559 4-Phase)
34	Dynamic O.C.
35	Dual Current Sourcing (F75383S)
36	VCC12_HT,VCCA25,PLL POWER
37	PWR SEQUENCE,3114,1394B PWR
38	DDR18 , DDRVTT , 5VDUAL
39	ATX POWER CONNCTOR,VCC15
40	DUAL BIOS
41	FRONT PANEL
42	ITE 8716
43	F_USB1/F_USB2/F_USB3 CONNECTOR
44	TI 1394A 1/2
45	COMA , LPT, TPM
46	AUDIO CODEC ALC883
47	AUDIO JACK, L_OUT, F_AUDIO
48	JMICRON 363
49	Marvell 88E1116 GbE Phy -A
50	Marvell 88E1116 GbE Phy -B
51	

GIGABYTE CORP.			
TitleCOVER SHEET			
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L0_CADIN_L[0..15] <L0_CADIN_L[0..15] 11
L0_CADIN_H[0..15] <L0_CADIN_H[0..15] 11
L0_CLKIN_L[0..1] <L0_CLKIN_L[0..1] 11
L0_CLKIN_H[0..1] <L0_CLKIN_H[0..1] 11
L0_CADOUT_L[0..15] <L0_CADOUT_L[0..15] 11
L0_CADOUT_H[0..15] <L0_CADOUT_H[0..15] 11
L0_CLKOUT_L[0..1] <L0_CLKOUT_L[0..1] 11
L0_CLKOUT_H[0..1] <L0_CLKOUT_H[0..1] 11

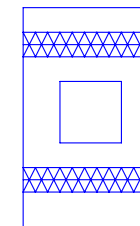
CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR18V
CPU_VTT_SUS = DDRVTT

VLDT_A = VCC12_HT
VLDT_B = HT12B



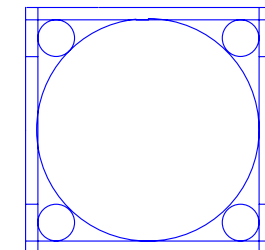
CPU-SK/940AM2/S/15u

SOCKET_M2



M2_RM/[12SP2-060110-01R]/X

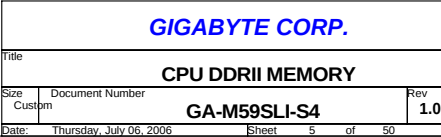
SOCKET_M2

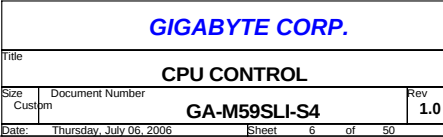


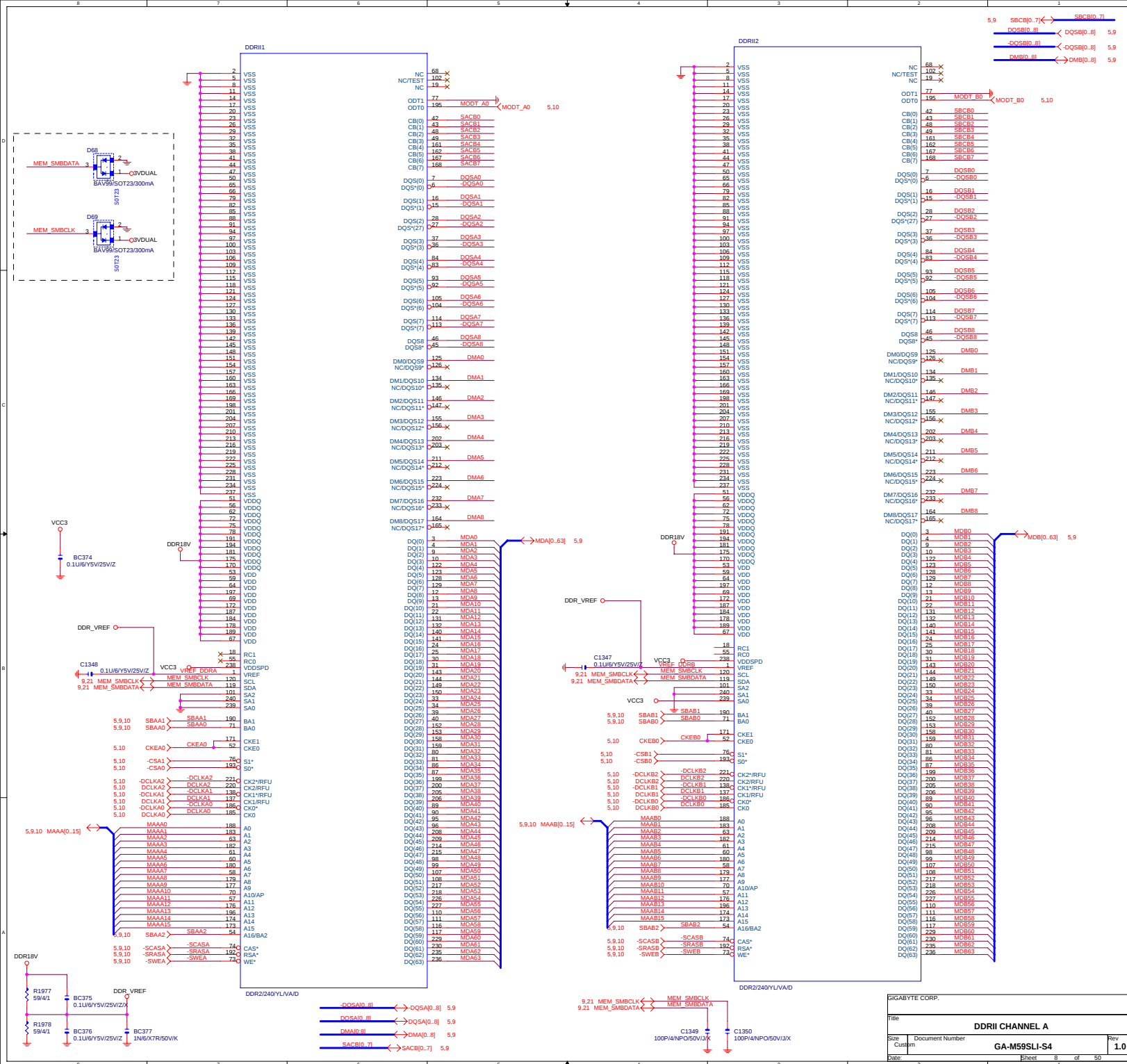
K8-940AM2/RM/BP-M/SC/BK/3M/[12KRC-04K807-41R]

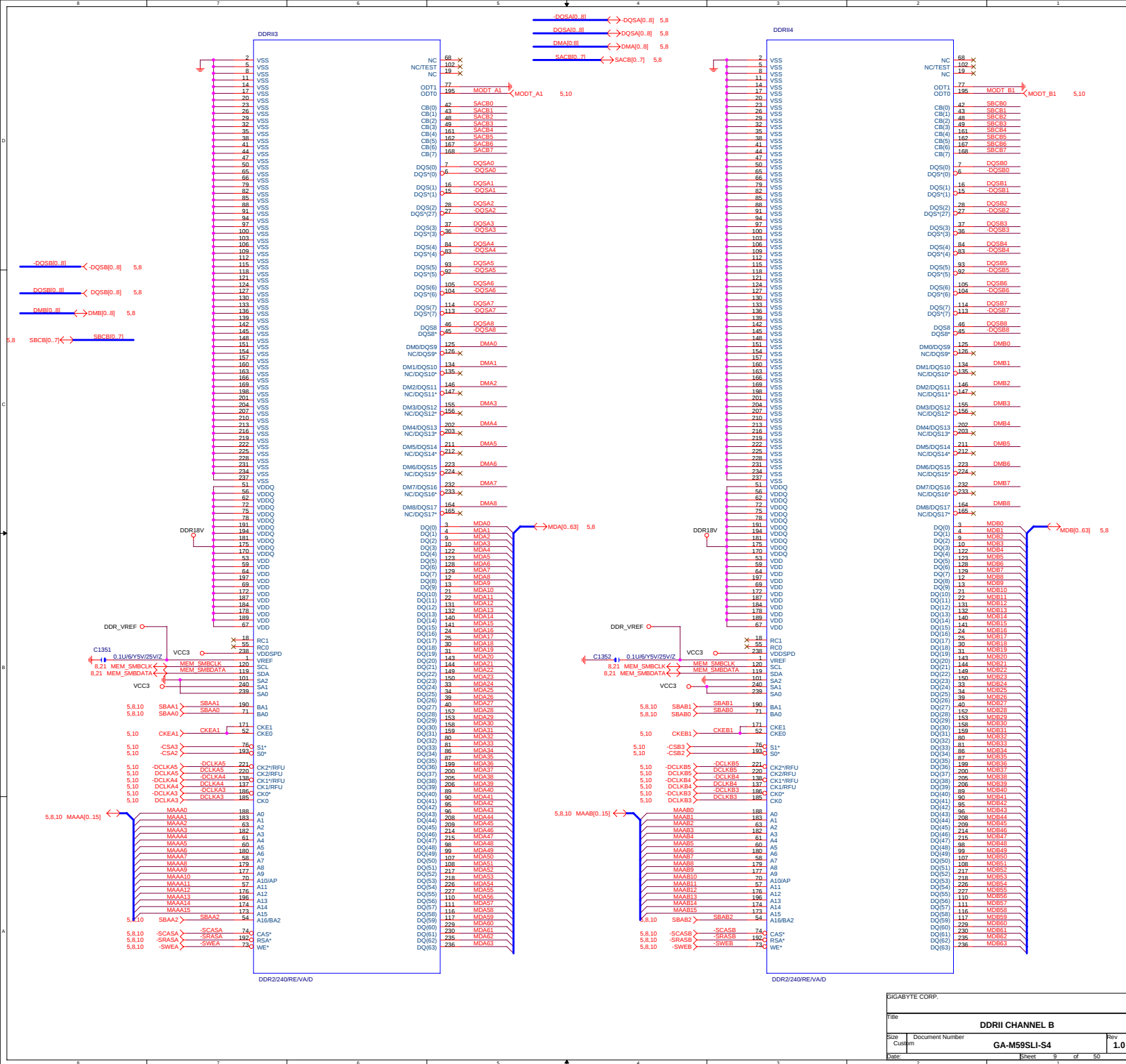
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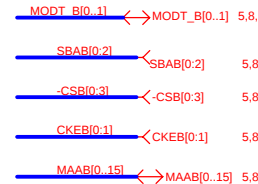
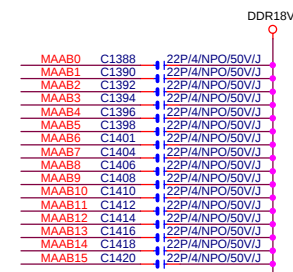
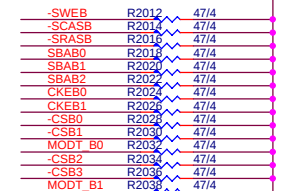
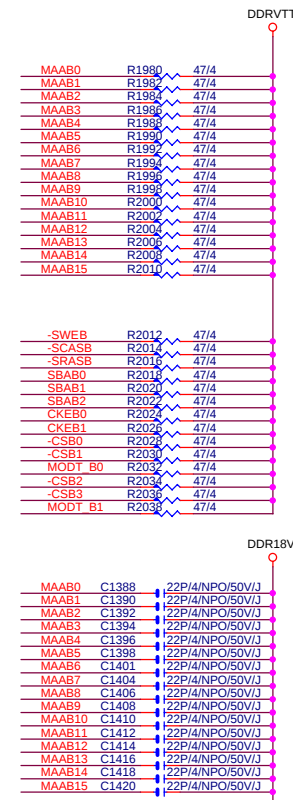
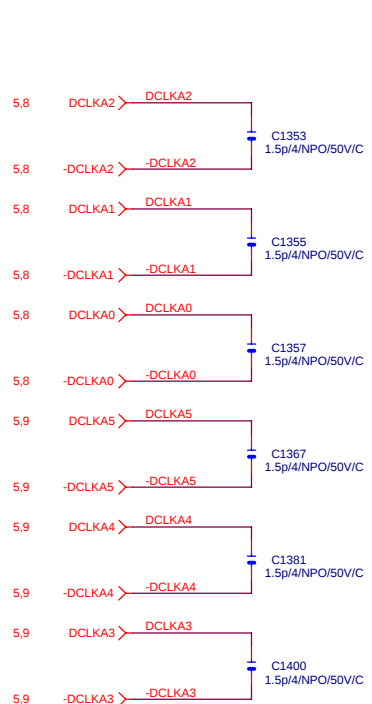
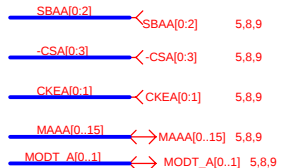
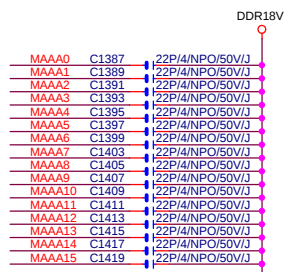
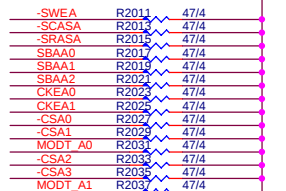
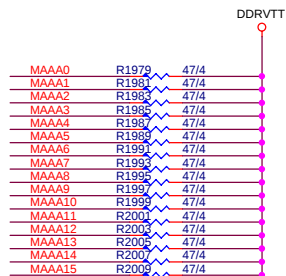
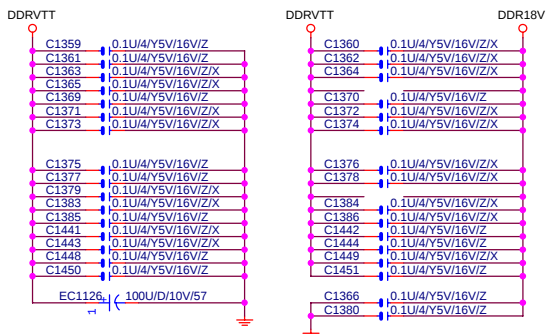
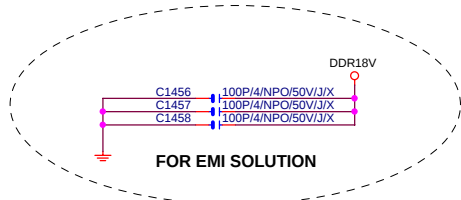
Title			Rev
CPU HYPER TRANSPORT			1.0
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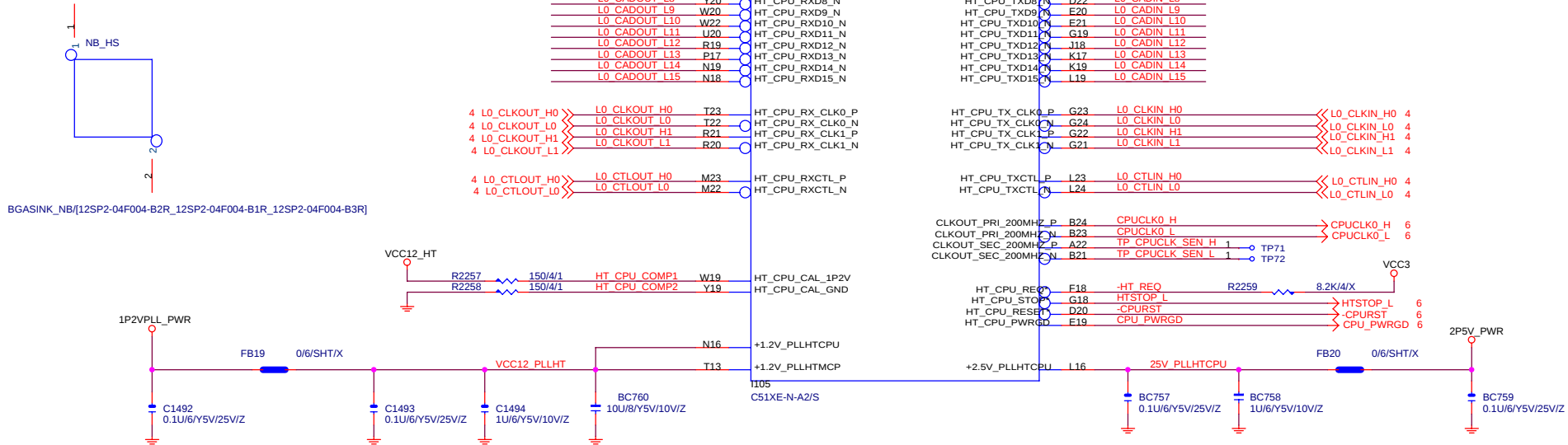






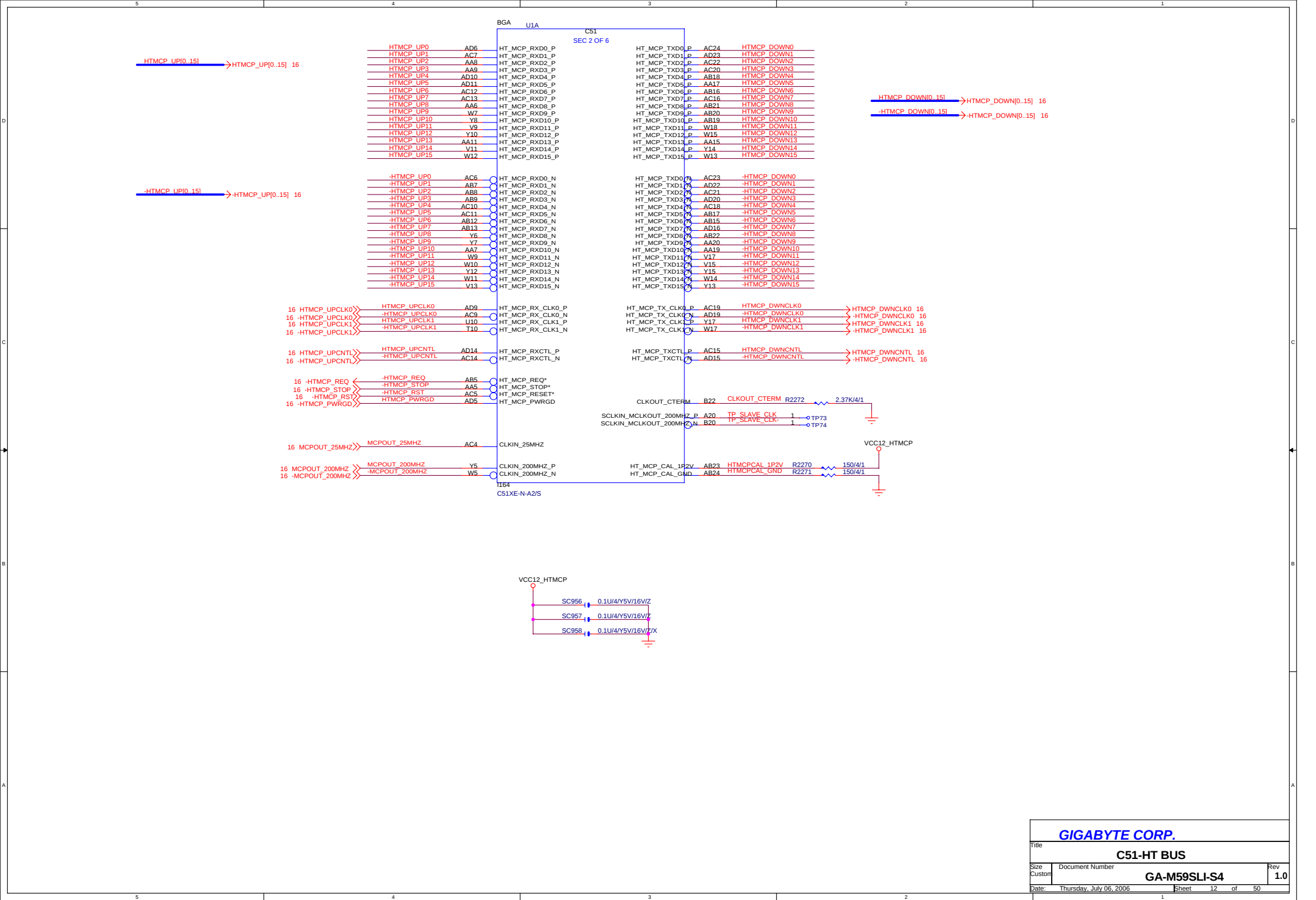


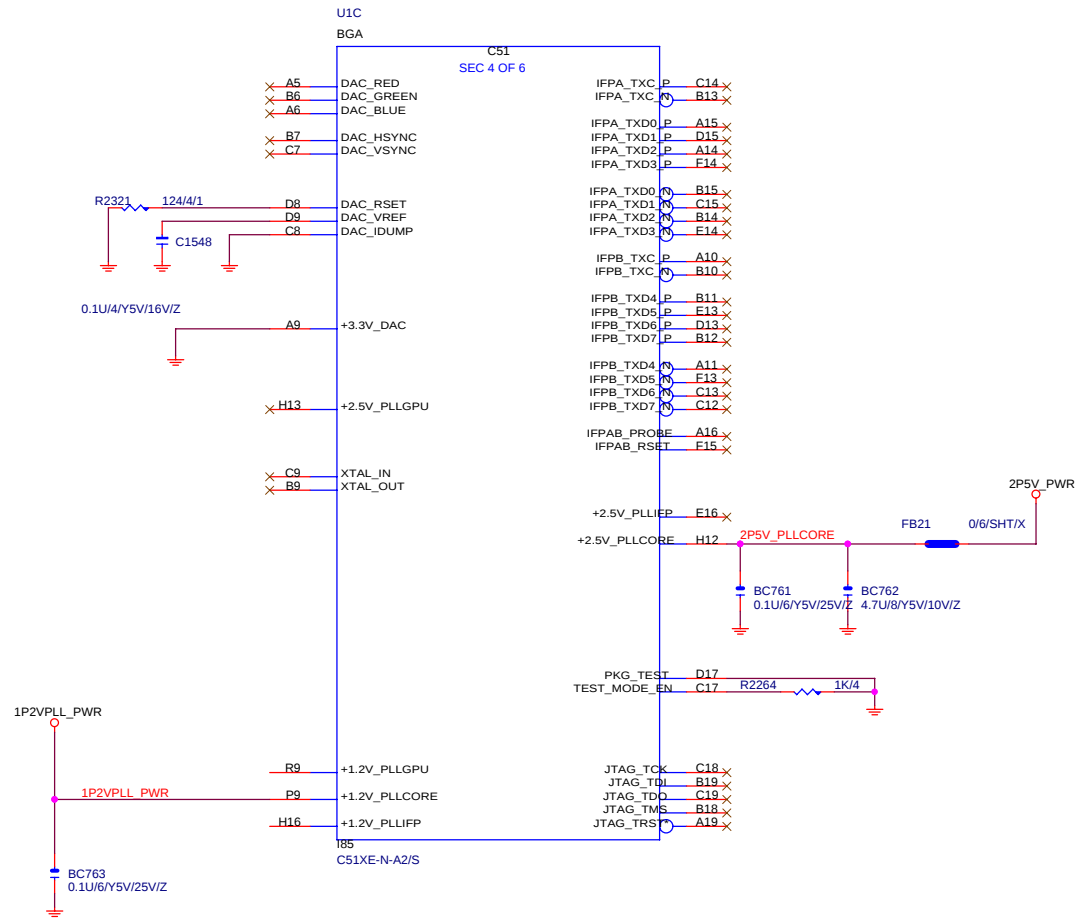
N.B HEATSINK



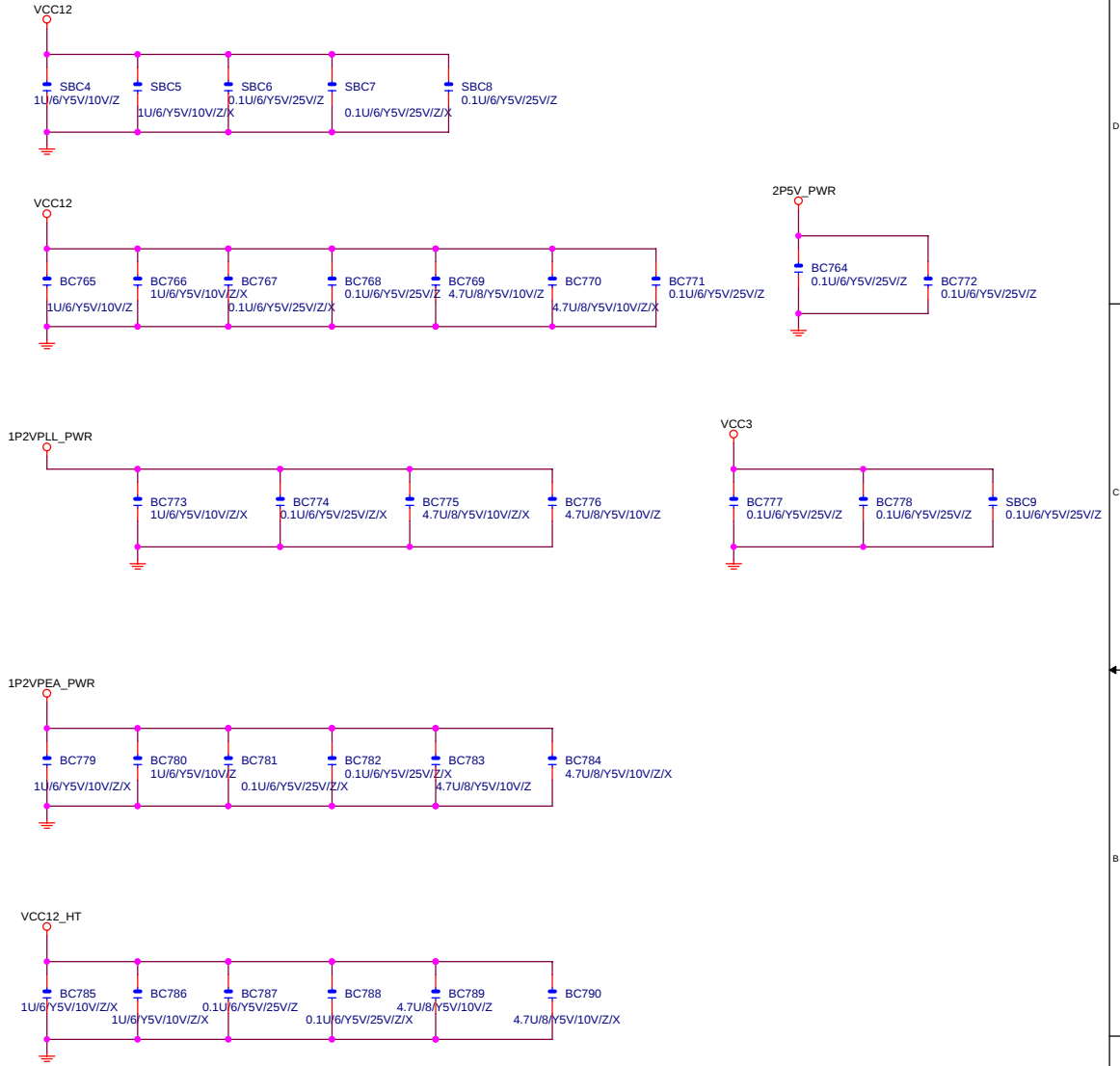
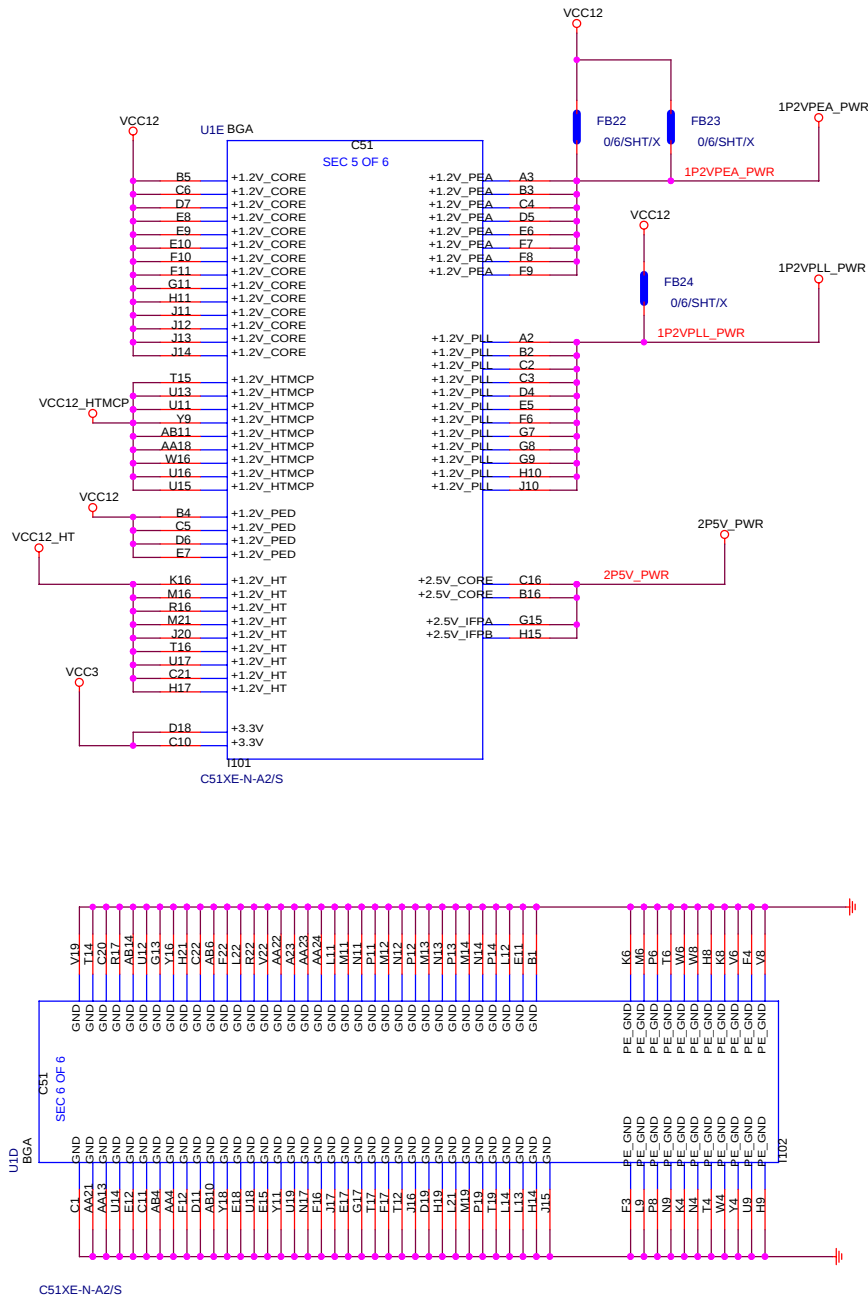
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C51-HOST			
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C51-PWR/GND			
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HTMCP_DOWN[0..15] → HTMCP_DOWN[0..15] 12

-HTMCP_DOWN[0..15] → -HTMCP_DOWN[0..15] 12

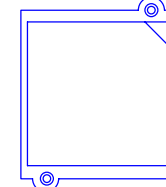
U5G1A PBGA776-NVIDIA-MCP55

MCP55
MCP55P-N-A1
SEC 1 OF 9

HTMCP_UP[0..15] → HTMCP_UP[0..15] 12

N.B FANSINK

HS1



FAN SINK(12SP2-01A002-32R_12SP2-01A002-33R_12SP2-01A002-34R)/X

-HTMCP_UP[0..15] → -HTMCP_UP[0..15] 12

HTMCP_DOWN0 AK32 HT_MCP_RXD0_P
HTMCP_DOWN1 AJ32 HT_MCP_RXD1_P
HTMCP_DOWN2 AH32 HT_MCP_RXD2_P
HTMCP_DOWN3 AH30 HT_MCP_RXD3_P
HTMCP_DOWN4 AE32 HT_MCP_RXD4_P
HTMCP_DOWN5 AE32 HT_MCP_RXD5_P
HTMCP_DOWN6 AD32 HT_MCP_RXD6_P
HTMCP_DOWN7 AD30 HT_MCP_RXD7_P
HTMCP_DOWN8 AG27 HT_MCP_RXD8_P
HTMCP_DOWN9 AE27 HT_MCP_RXD9_P
HTMCP_DOWN10 AD26 HT_MCP_RXD10_P
HTMCP_DOWN11 AE29 HT_MCP_RXD11_P
HTMCP_DOWN12 AB23 HT_MCP_RXD12_P
HTMCP_DOWN13 AB26 HT_MCP_RXD13_P
HTMCP_DOWN14 AB28 HT_MCP_RXD14_P
HTMCP_DOWN15 AA28 HT_MCP_RXD15_P

-HTMCP_DOWN0 AK31 HT_MCP_RXD0_N
-HTMCP_DOWN1 AJ31 HT_MCP_RXD1_N
-HTMCP_DOWN2 AH31 HT_MCP_RXD2_N
-HTMCP_DOWN3 AH29 HT_MCP_RXD3_N
-HTMCP_DOWN4 AE30 HT_MCP_RXD4_N
-HTMCP_DOWN5 AE31 HT_MCP_RXD5_N
-HTMCP_DOWN6 AD31 HT_MCP_RXD6_N
-HTMCP_DOWN7 AD29 HT_MCP_RXD7_N
-HTMCP_DOWN8 AG28 HT_MCP_RXD8_N
-HTMCP_DOWN9 AE28 HT_MCP_RXD9_N
-HTMCP_DOWN10 AD25 HT_MCP_RXD10_N
-HTMCP_DOWN11 AE28 HT_MCP_RXD11_N
-HTMCP_DOWN12 AB24 HT_MCP_RXD12_N
-HTMCP_DOWN13 AB25 HT_MCP_RXD13_N
-HTMCP_DOWN14 AB27 HT_MCP_RXD14_N
-HTMCP_DOWN15 AA29 HT_MCP_RXD15_N

HT_MCP_TXD0_P R29 HTMCP_UP0
HT_MCP_TXD1_P T29 HTMCP_UP1
HT_MCP_TXD2_P T31 HTMCP_UP2
HT_MCP_TXD3_P U31 HTMCP_UP3
HT_MCP_TXD4_P W29 HTMCP_UP4
HT_MCP_TXD5_P V29 HTMCP_UP5
HT_MCP_TXD6_P Y31 HTMCP_UP6
HT_MCP_TXD7_P AA31 HTMCP_UP7
HT_MCP_TXD8_P R24 HTMCP_UP8
HT_MCP_TXD9_P T28 HTMCP_UP9
HT_MCP_TXD10_P U28 HTMCP_UP10
HT_MCP_TXD11_P T25 HTMCP_UP11
HT_MCP_TXD12_P V27 HTMCP_UP12
HT_MCP_TXD13_P V26 HTMCP_UP13
HT_MCP_TXD14_P Y28 HTMCP_UP14
HT_MCP_TXD15_P Y26 HTMCP_UP15

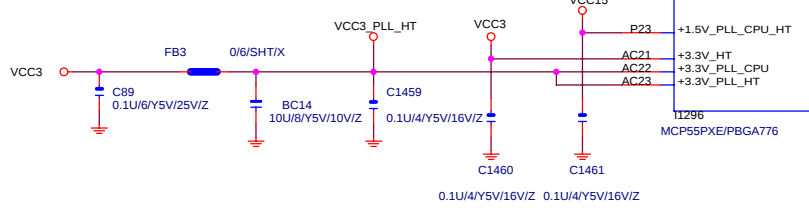
HT_MCP_TXD0_N R30 -HTMCP_UP0
HT_MCP_TXD1_N T30 -HTMCP_UP1
HT_MCP_TXD2_N T32 -HTMCP_UP2
HT_MCP_TXD3_N U32 -HTMCP_UP3
HT_MCP_TXD4_N W30 -HTMCP_UP4
HT_MCP_TXD5_N Y30 -HTMCP_UP5
HT_MCP_TXD6_N Y32 -HTMCP_UP6
HT_MCP_TXD7_N AA32 -HTMCP_UP7
HT_MCP_TXD8_N T24 -HTMCP_UP8
HT_MCP_TXD9_N T27 -HTMCP_UP9
HT_MCP_TXD10_N U29 -HTMCP_UP10
HT_MCP_TXD11_N T26 -HTMCP_UP11
HT_MCP_TXD12_N V28 -HTMCP_UP12
HT_MCP_TXD13_N V25 -HTMCP_UP13
HT_MCP_TXD14_N Y27 -HTMCP_UP14
HT_MCP_TXD15_N Y25 -HTMCP_UP15

12 HTMCP_DWNCCLK0 HTMCP_DWNCCLK0 AG30 HT_MCP_RX_CLK0_P
12 -HTMCP_DWNCCLK0 -HTMCP_DWNCCLK0 AG29 HT_MCP_RX_CLK0_N
12 HTMCP_DWNCCLK1 HTMCP_DWNCCLK1 AD27 HT_MCP_RX_CLK1_P
12 -HTMCP_DWNCCLK1 -HTMCP_DWNCCLK1 AD28 HT_MCP_RX_CLK1_N

12 HTMCP_DWNCNTL HTMCP_DWNCNTL AC30 HT_MCP_RXCTL_P
12 -HTMCP_DWNCNTL -HTMCP_DWNCNTL AC29 HT_MCP_RXCTL_N

R1797 150/4/1 HT_MCP_COMP1 AG26 HT_MCP_COMP_GND1
R1798 49.9/4/1 HT_MCP_COMP2 AG25 HT_MCP_COMP_GND2

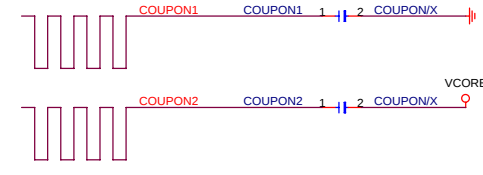
3VDUAL R2500 8.2K/4/X
6 THERMTRIP_CPU_L THERMTRIP_CPU_L R2508 0/4 AJ29 THERMTRIP/GPIO*



CLKOUT0_CLKIN_200MHZ FN32 SR18 0/6/SHT/X MCPOUT_200MHZ
CLKOUT0_CLKIN_200MHZ FN31 SR19 0/6/SHT/X MCPOUT_200MHZ
CLKOUT1_200MHZ M30 TP_CLKOUT1_P 1 TP47
CLKOUT1_200MHZ M29 TP_CLKOUT1_N 1 TP48
CLKOUT2_200MHZ L30 TP_CLKOUT2_P 1 TP49
CLKOUT2_200MHZ L29 TP_CLKOUT2_N 1 TP50

VCC12_HTMCP
HT_VREF U23
CLKOUT_25MHZ N26 R2269 22/4 MCPOUT_25MHZ
CLK200_TERM_GND M28 R2094 562/4/1

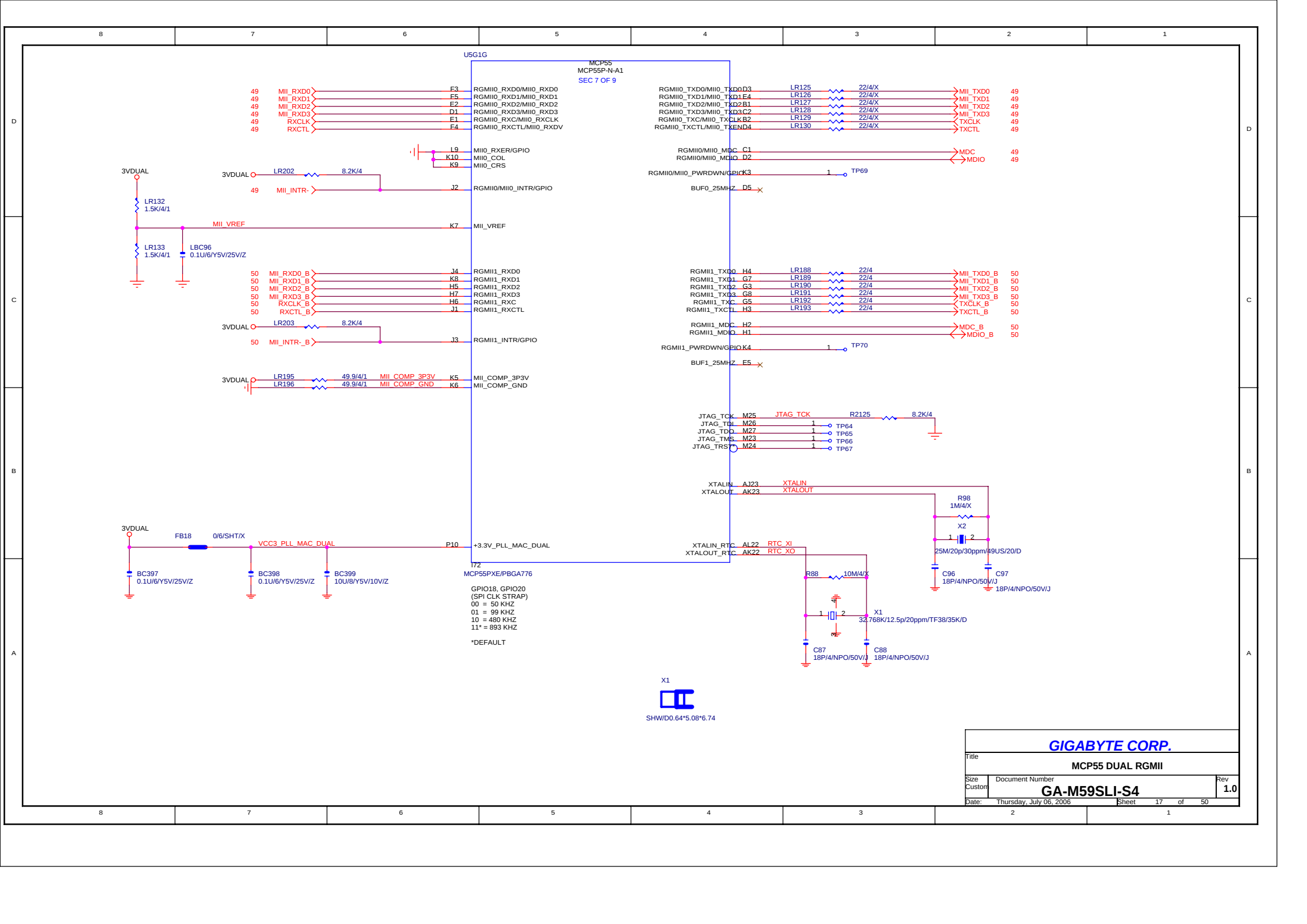
-HTMCP_REQ R2250 1K/4
-HTMCP_STOP R2251 1K/4
-HTMCP_RST R2252 1K/4
-HTMCP_PWRGD R2253 1K/4

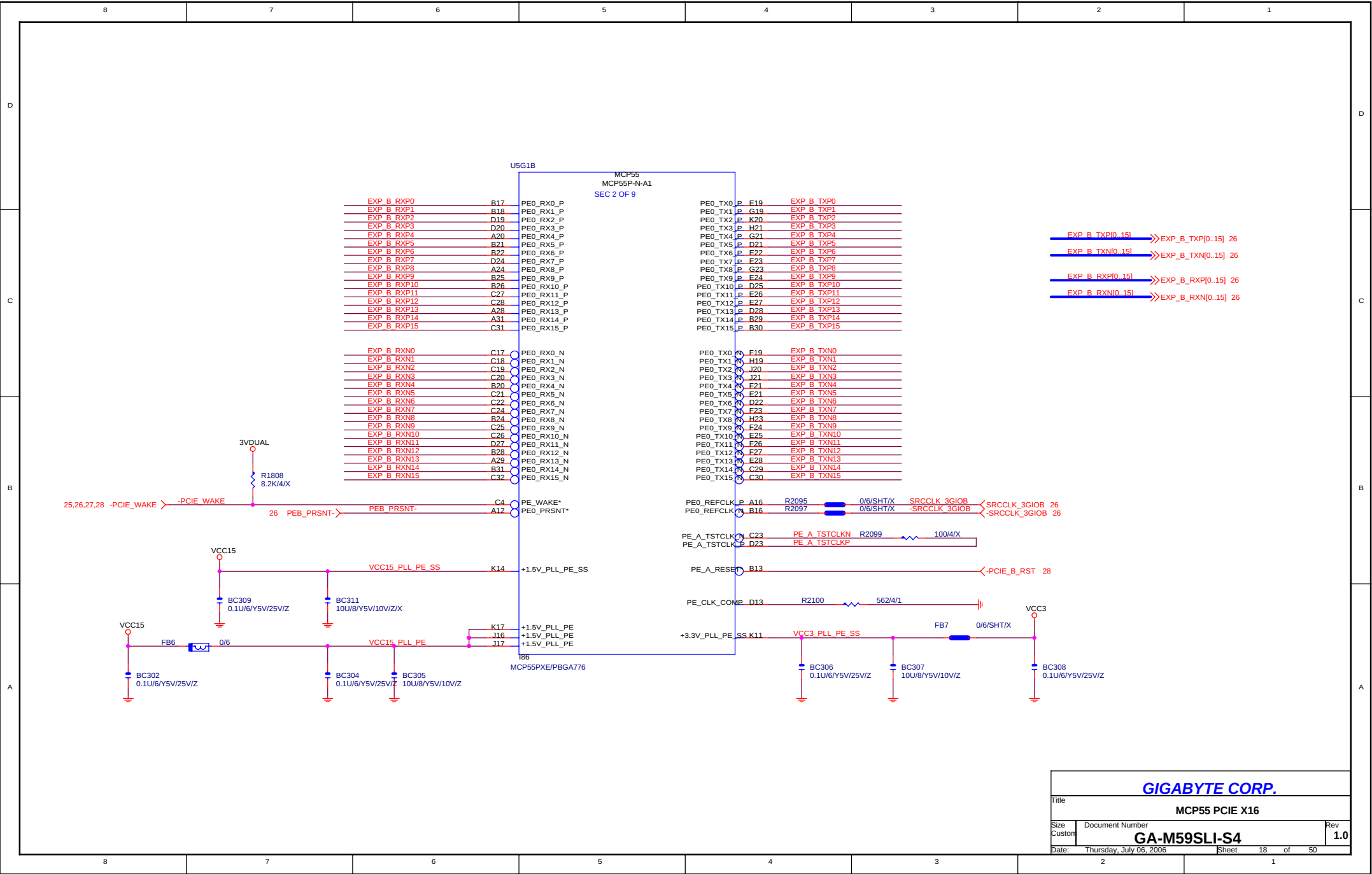


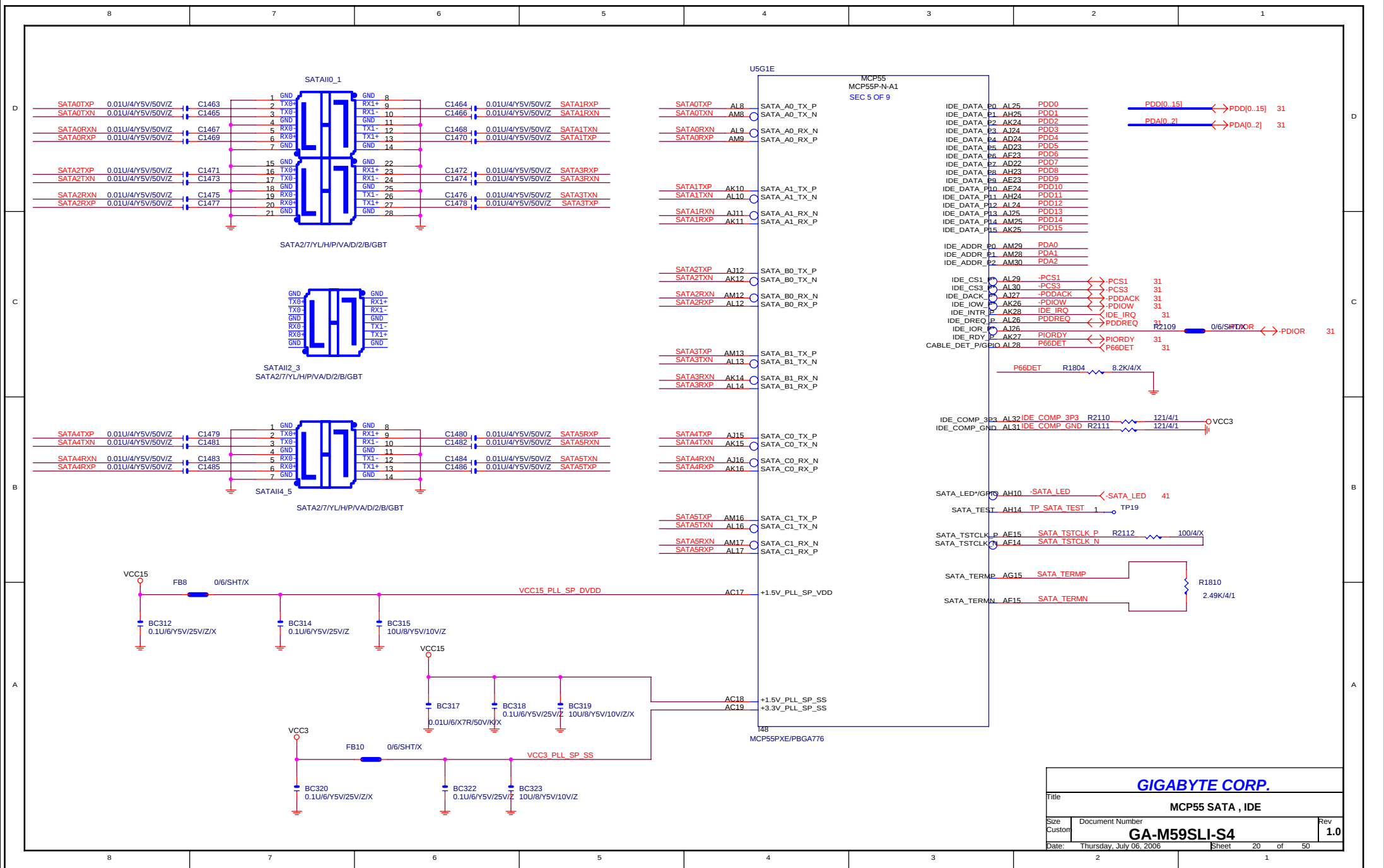
GIGABYTE CORP.

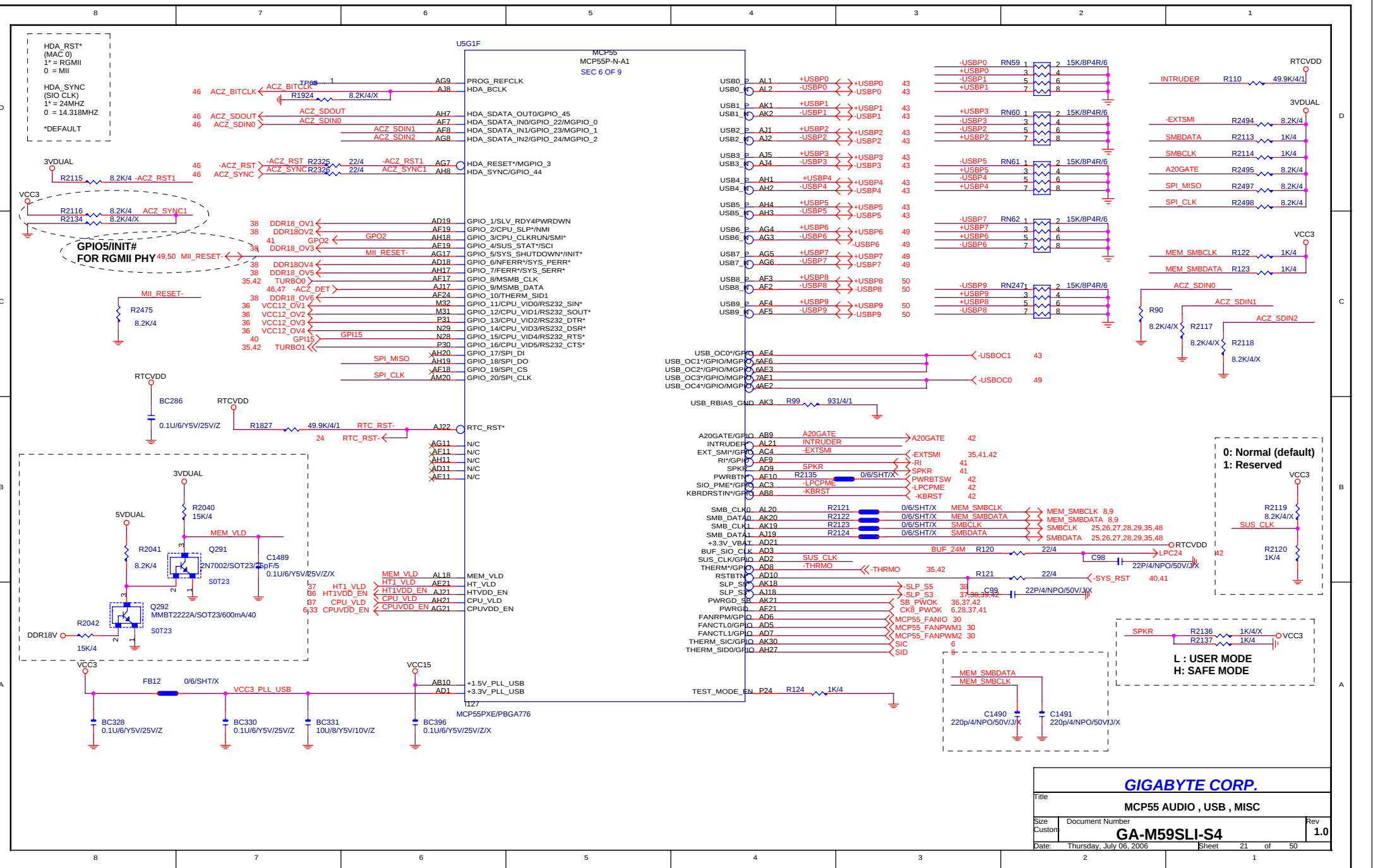
MCP55 HT/CLK

Title		
MCP55 HT/CLK		
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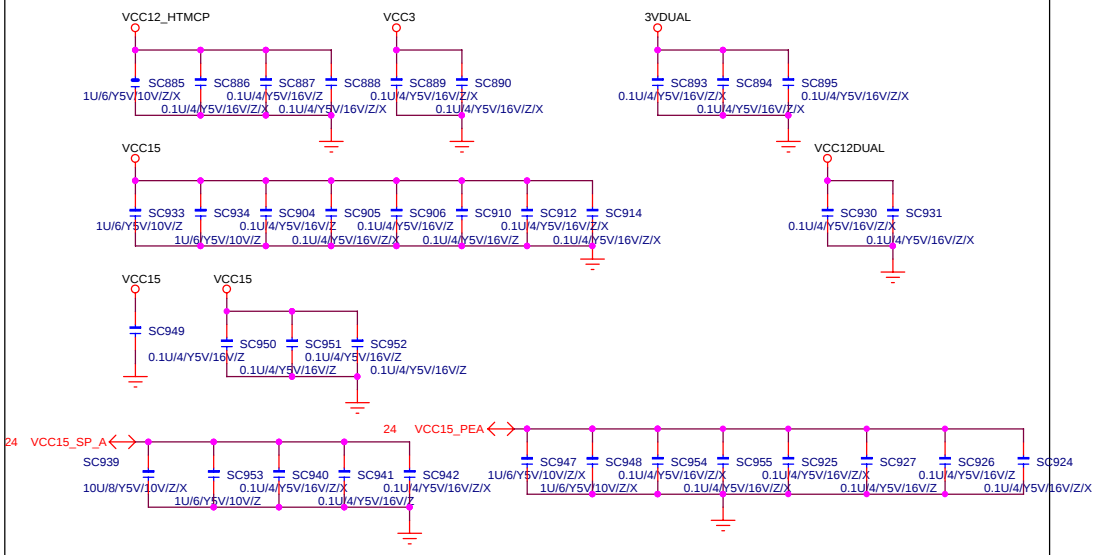






GIGABYTE CORP.			
MCP55 AUDIO , USB , MISC			
Title	Document Number	Rev	1.0
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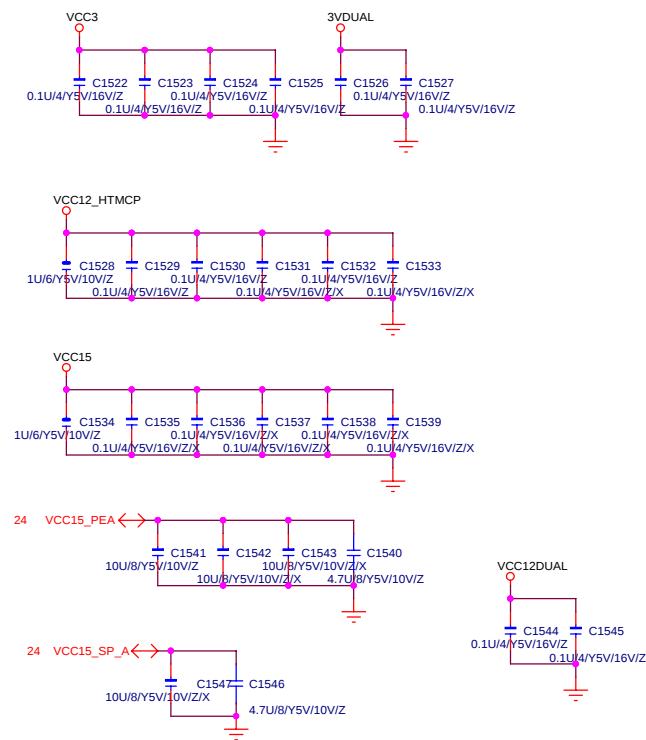
MCP55 BACK SIDE DECOUPLING



MCP55 INTERNAL PULL-UP/PULL-DOWN

PIN	VOLTAGE
A20GATE/GPIO	+3.3V
EXT_SM*/GPIO	+3.3V_DUAL
HDA_SDATA_IN0/GPIO_22/MGPIO_0	+3.3V_DUAL/GND
HDA_SDATA_IN1/GPIO_23/MGPIO_1	+3.3V_DUAL/GND
HDA_SDATA_IN2/GPIO_24/MGPIO_2	+3.3V_DUAL/GND
HDA_SDATA_OUT/GPIO_45	+3.3V_DUAL/GND
JTAG_TDI	+3.3V
JTAG_TMS	+3.3V
JTAG_TRST*	GND
KBRDRSTIN*/GPIO	+3.3V
PE_WAKE*	+3.3V_DUAL
SIO_PME*/GPIO	+3.3V_DUAL
THERM*/GPIO	+3.3V

MCP55 TOP SIDE DECOUPLING



GIGABYTE CORP.

Title

MCP55 DECOUPLING

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29,44 AD[0..31] <--

AD0	AA4	PCI_AD0
AD1	AB3	PCI_AD1
AD2	AB2	PCI_AD2
AD3	AA3	PCI_AD3
AD4	Y10	PCI_AD4
AD5	AA2	PCI_AD5
AD6	Y9	PCI_AD6
AD7	Y8	PCI_AD7
AD8	Y7	PCI_AD8
AD9	Y4	PCI_AD9
AD10	Y5	PCI_AD10
AD11	Y1	PCI_AD11
AD12	Y3	PCI_AD12
AD13	Y2	PCI_AD13
AD14	V9	PCI_AD14
AD15	V8	PCI_AD15
AD16	U2	PCI_AD16
AD17	U3	PCI_AD17
AD18	U8	PCI_AD18
AD19	T9	PCI_AD19
AD20	T7	PCI_AD20
AD21	T8	PCI_AD21
AD22	T6	PCI_AD22
AD23	T3	PCI_AD23
AD24	T1	PCI_AD24
AD25	T2	PCI_AD25
AD26	R3	PCI_AD26
AD27	R4	PCI_AD27
AD28	T5	PCI_AD28
AD29	P9	PCI_AD29
AD30	P7	PCI_AD30
AD31	P8	PCI_AD31

29,44 -C_BE0	<--	-C_BE0	Y6	PCI_CBE0*
29,44 -C_BE1	<--	-C_BE1	V9	PCI_CBE1*
29,44 -C_BE2	<--	-C_BE2	V2	PCI_CBE2*
29,44 -C_BE3	<--	-C_BE3	T4	PCI_CBE3*

29,44 -FRAME	<--	-FRAME	U4	PCI_FRAME*
29,44 -IRDY	<--	-IRDY	V3	PCI_IRDY*
29,44 -TRDY	<--	-TRDY	V4	PCI_TRDY*
29,44 -STOP	<--	-STOP	W4	PCI_STOP*
29,44 -DEVSEL	<--	-DEVSEL	W3	PCI_DEVSEL*
29,44 PAR	<--	PAR	V7	PCI_PAR
29,44 -PERR	<--	-PERR	V5	PCI_PERR*/GPIO
29,44 -SERR	<--	-SERR	V6	PCI_SERR*
29,44 -PCIPME	<--	-PCIPME	AB6	PCI_PME*/GPIO

29	-PPCIRST	<--	-PPCIRST	R79	33/4	AB5	PCI_RESET0*
45	-TPMRST	<--	-TPMRST	R2466	33/4	AA10	PCI_RESET1*
44	-1394RST	<--	-1394RST	R81	33/4	AB4	PCI_RESET2*
31	-IDERST	<--	-IDERST	R82	33/4	AB7	PCI_RESET3*
40	-LPCBIOSRST	<--	-LPCBIOSRST	R83	33/4	AH6	LPC_RESET*
42	-LPCSIORST	<--	-LPCSIORST	R85	33/4		

MCP55PXE/PBGA776

MCP55
MCP55P-N-A1
SEC 4 OF 9

PCI_REQ0*	N4	-REQ0
PCI_REQ1*	P3	-REQ1
PCI_REQ2*/GPIO	P4	-REQ2
PCI_REQ3*/GPIO	P5	-REQ3
PCI_REQ4*/FANRPM	P6	-REQ4
PCI_GNT0*	M1	-GNT0
PCI_GNT1*	M2	-GNT1
PCI_GNT2*/GPIO	N2	-GNT2
PCI_GNT3*/GPIO	N3	-GNT3
PCI_GNT4*/RS232_DTR	P2	-GNT4

PCI_INT0*	L7	-INTA	<--	-INTA	29
PCI_INT1*	L5	-INTB	<--	-INTB	29
PCI_INT2*	M3	-INTC	<--	-INTC	29,44
PCI_INT3*	L3	-INTD	<--	-INTD	29

PCI_CLK0	M6	PCLK0	R69	22/4	PCICLK1	>	PCICLK1	29
PCI_CLK1	M4	PCLK1	R74	22/4	PCICLK2	>	PCICLK2	29
PCI_CLK2	M5	PCLK2	R2465	22/4				45
PCI_CLK3	M7	PCLK3	R65	22/4	1394CLK	<<	TPMCLK33	44
PCI_CLK4	M8							
PCI_CLK5	N9	PCLK5	R72	22/4				
PCI_CLKIN	M9							

LPC_AD0	AL4							
LPC_AD1	AM4							
LPC_AD2	AL5							
LPC_AD3	AM5							

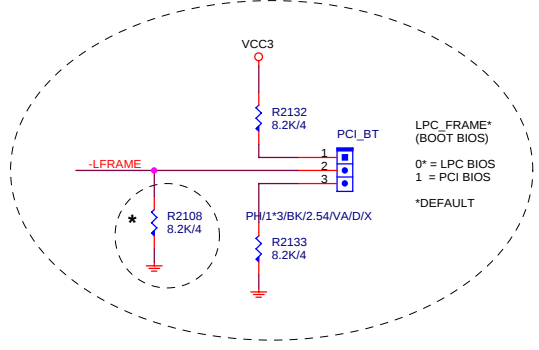
LPC_FRAME*	AK7	R2107	33/4	-LFRAME	<--	-LFRAME	40,42,45
LPC_DRQ0*	AL6			-LDRQ0	<--	-LDRQ0	42
LPC_DRQ1/LPC_RST	AK6			-LDRQ1	<--	-LDRQ1	
LPC_SERIRQ	AJ7			SERIRQ	>	SERIRQ	42,45

LPC_PWRDWN*/GPIO/EXT	AKA5	R2144	8.2K/4			VCC3	
LPC_CLK0	AL3	R86	22/4	LPC33	>	LPC33	42
LPC_CLK1	AM3	R84	22/4	ROMCLK33	>	ROMCLK33	40

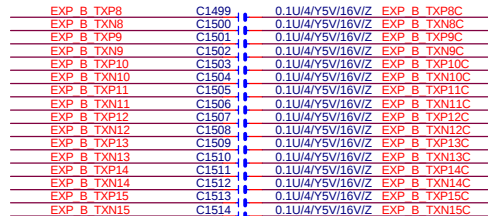
TPMCLK33	C1617	10P/4/NPO/50V/J/X
PCICLK1	C75	10P/4/NPO/50V/J/X
PCICLK2	C76	10P/4/NPO/50V/J/X
1394CLK	C79	10P/4/NPO/50V/J/X

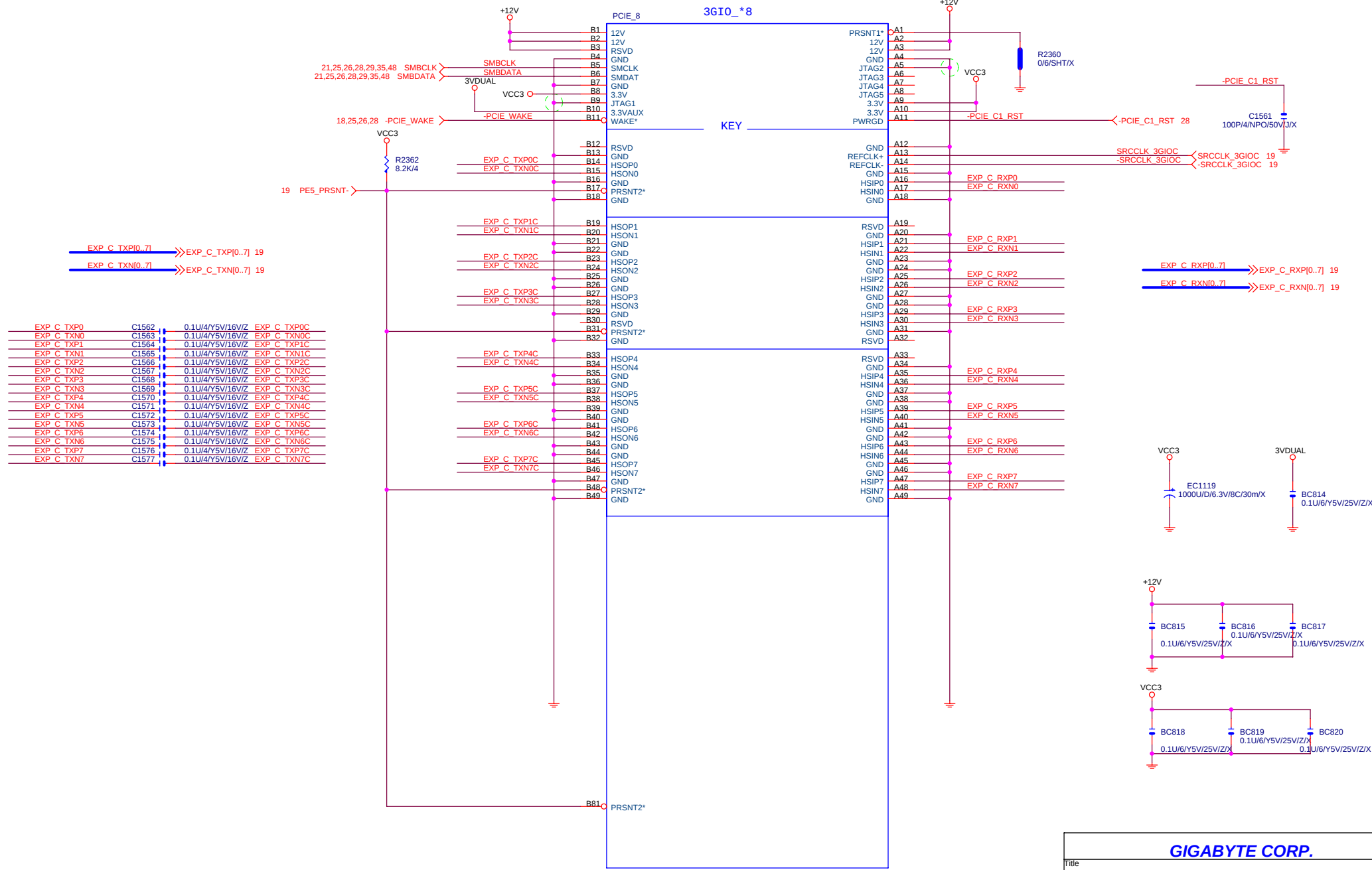
ROMCLK33	C82	10P/4/NPO/50V/J/X
LPC33	C84	10P/4/NPO/50V/J/X

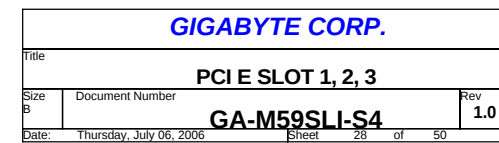
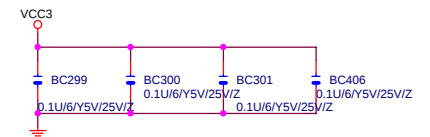
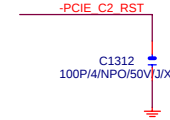
SERIRQ	R78	8.2K/4	VCC3
-LDRQ0	R77	8.2K/4	VCC3
-LDRQ1	R76	8.2K/4	VCC3



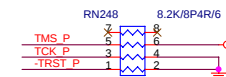
GIGABYTE CORP.			
Title			
MCP55 PCI			
Size	Document Number	Rev	
Custom	GA-M59SLI-S4	1.0	
Date:	Thursday, July 06, 2006	Sheet	23 of 50



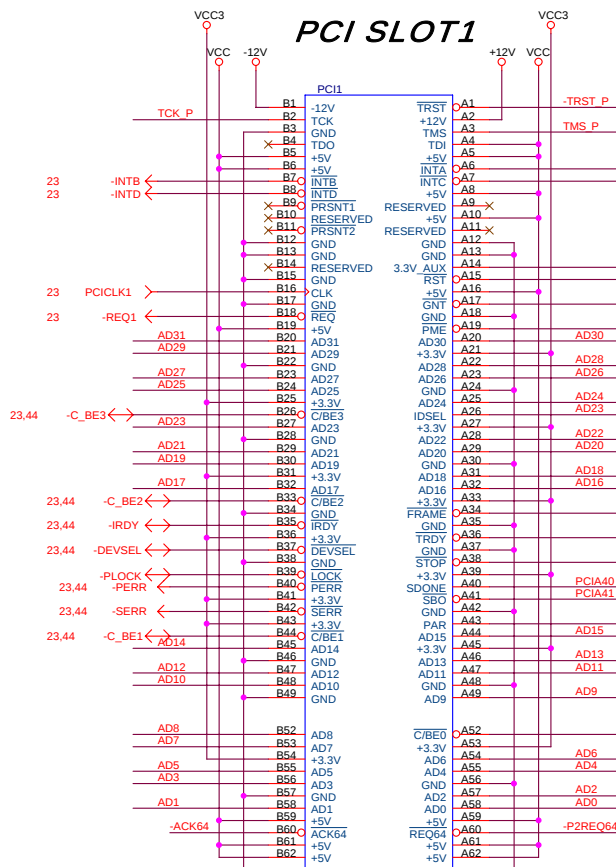




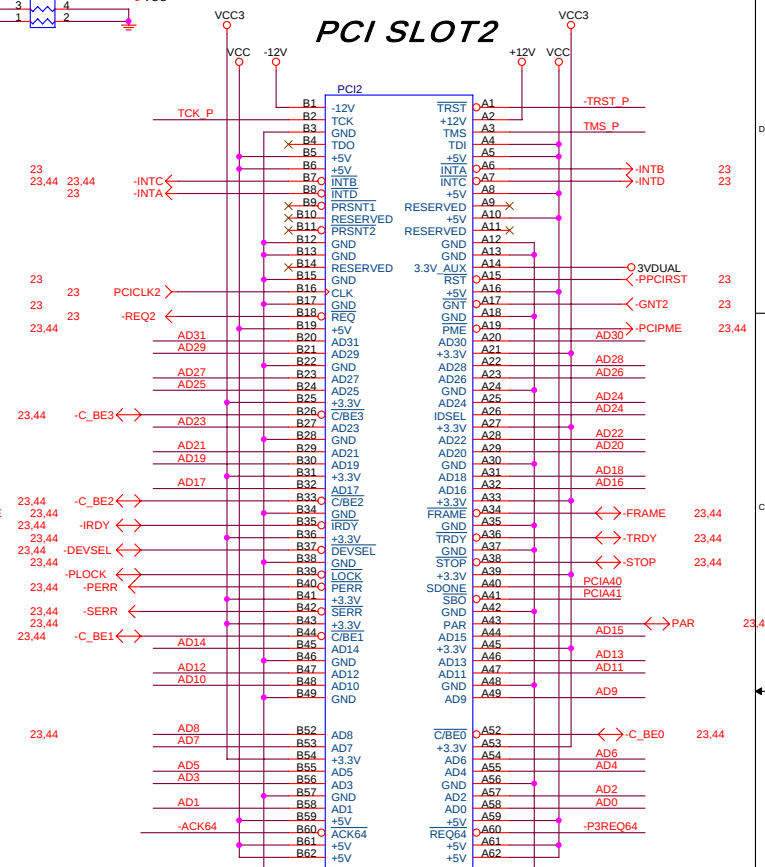
PCI SLOT 1,2



PCI SLOT1



PCI SLOT2

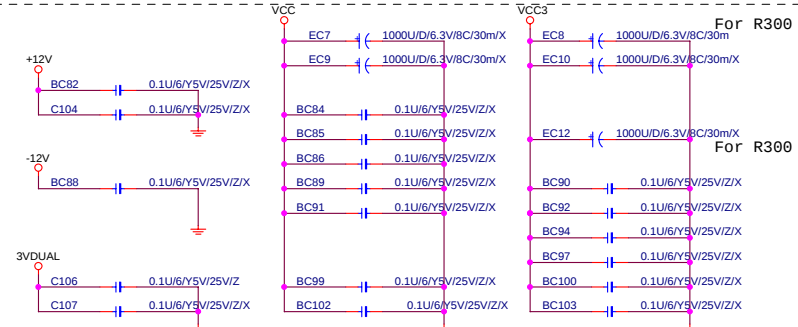
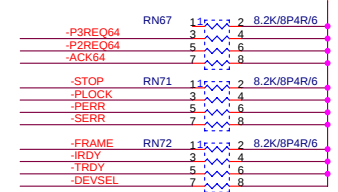
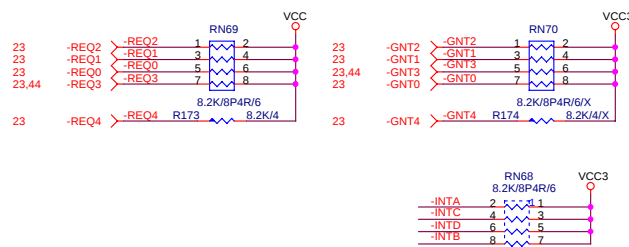


Close PCI Slot1

-PPCIRST

C103

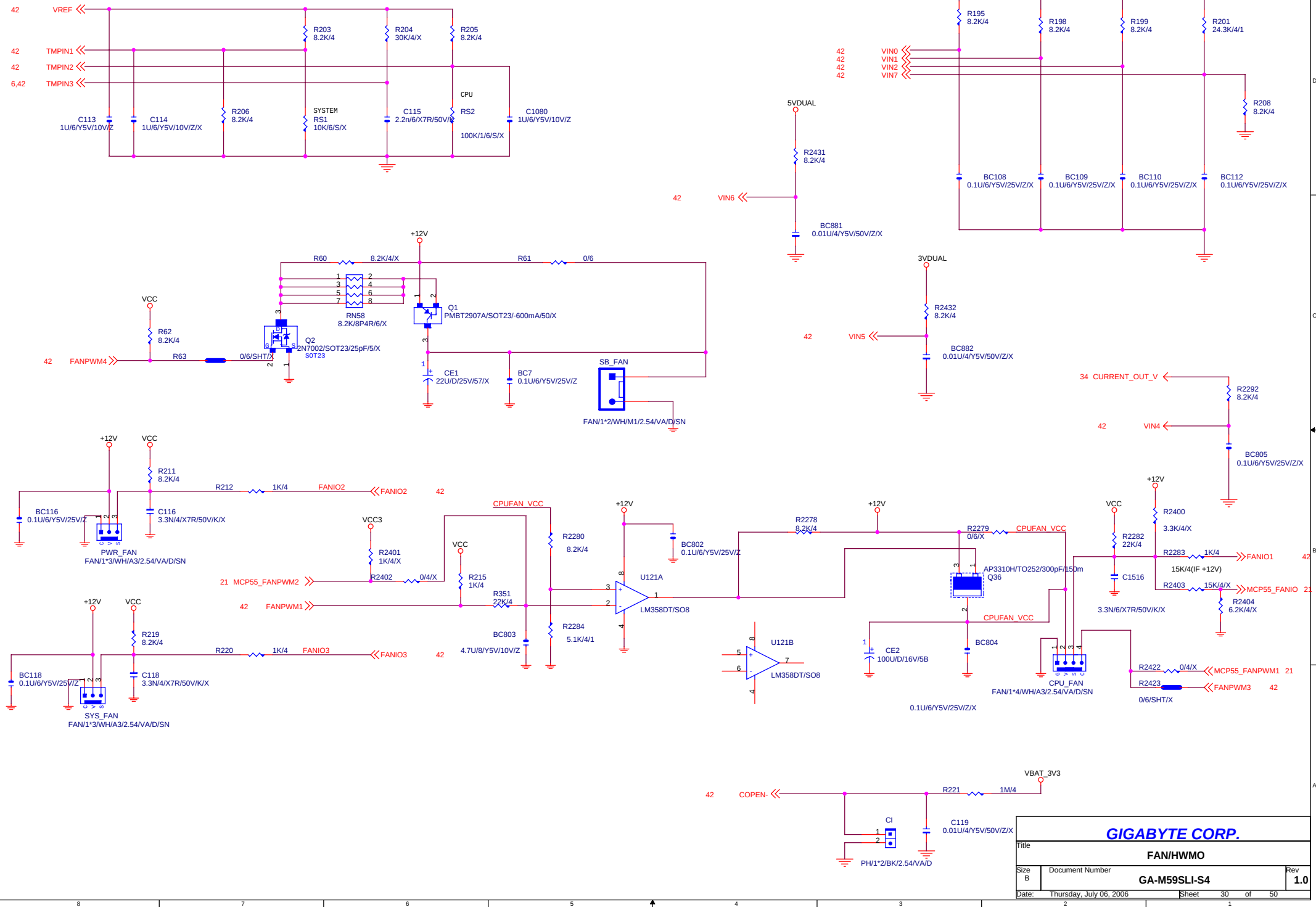
100P/4/NPO/50V/J/X

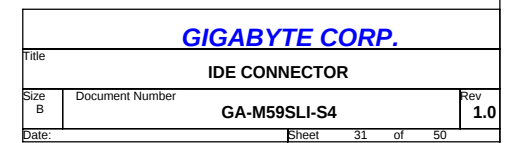
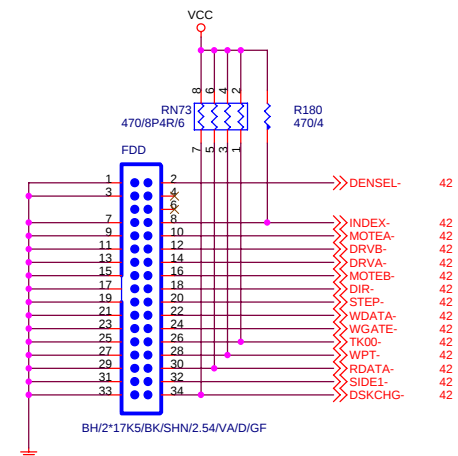
IDSEL(A23)
(D)IDSEL(A24)
(A)

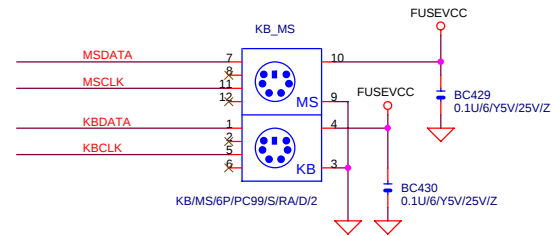
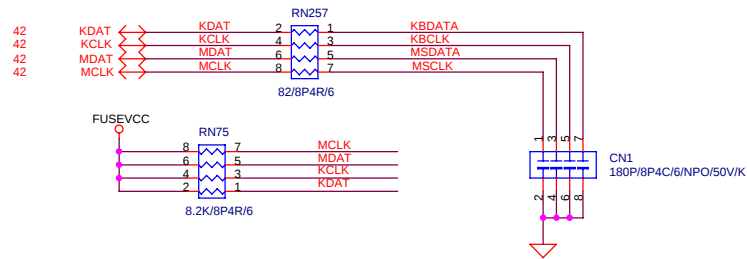
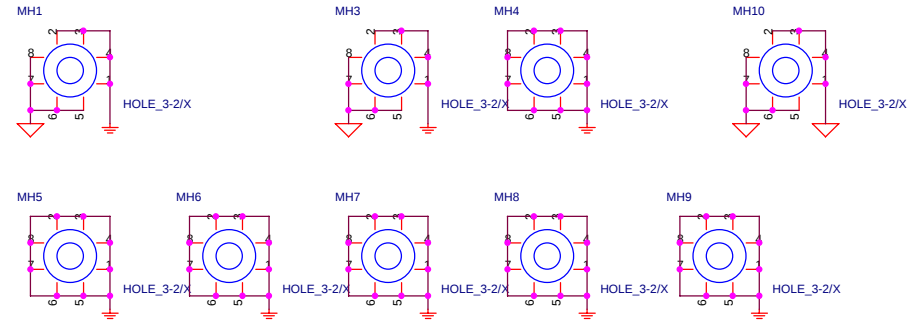
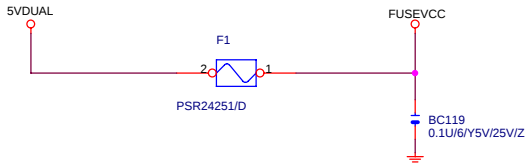
GIGABYTE CORP.

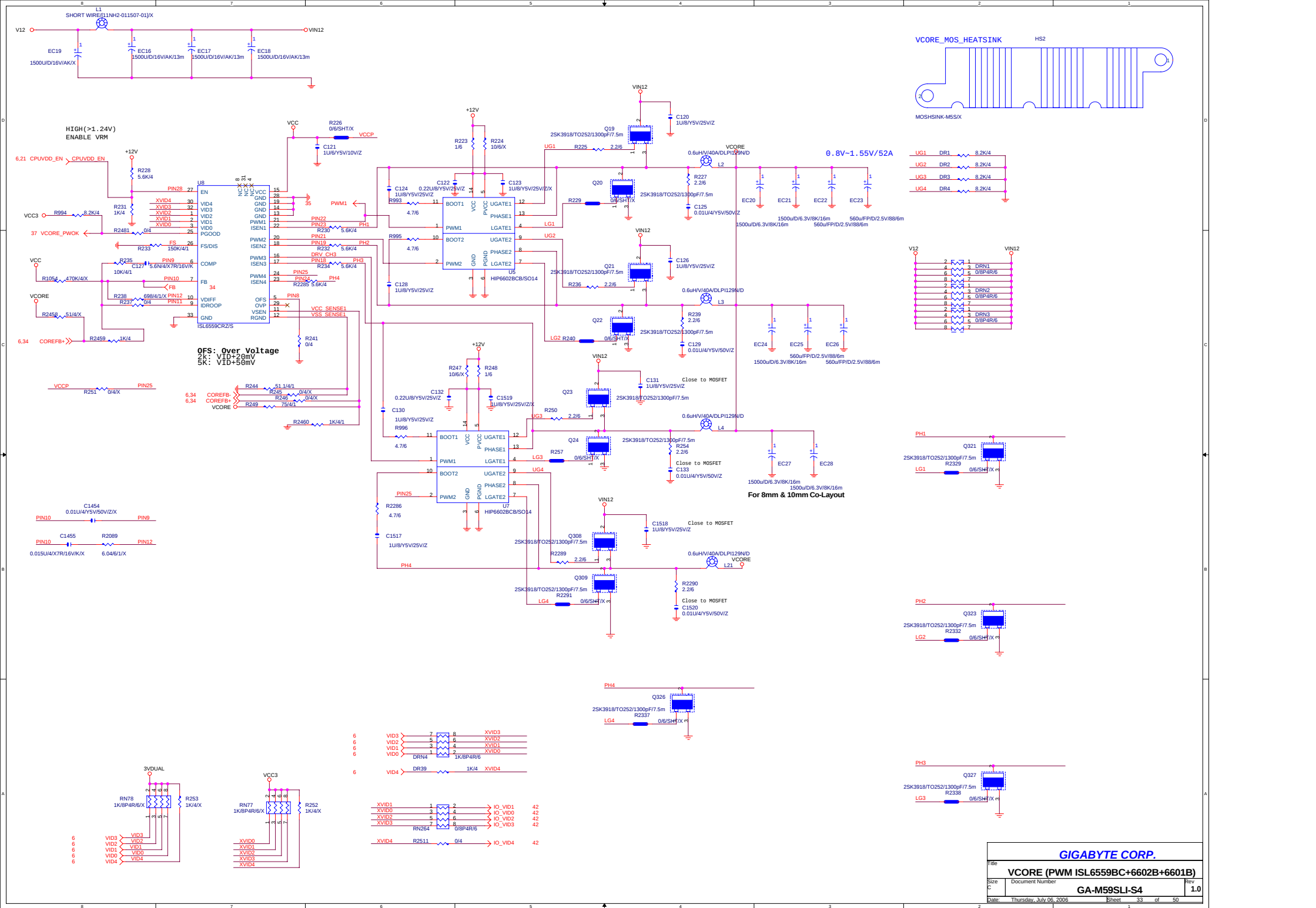
Title			
PCI SLOT 1,2			
Size Custom	Document Number		Rev
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Hardware Monitor circuits

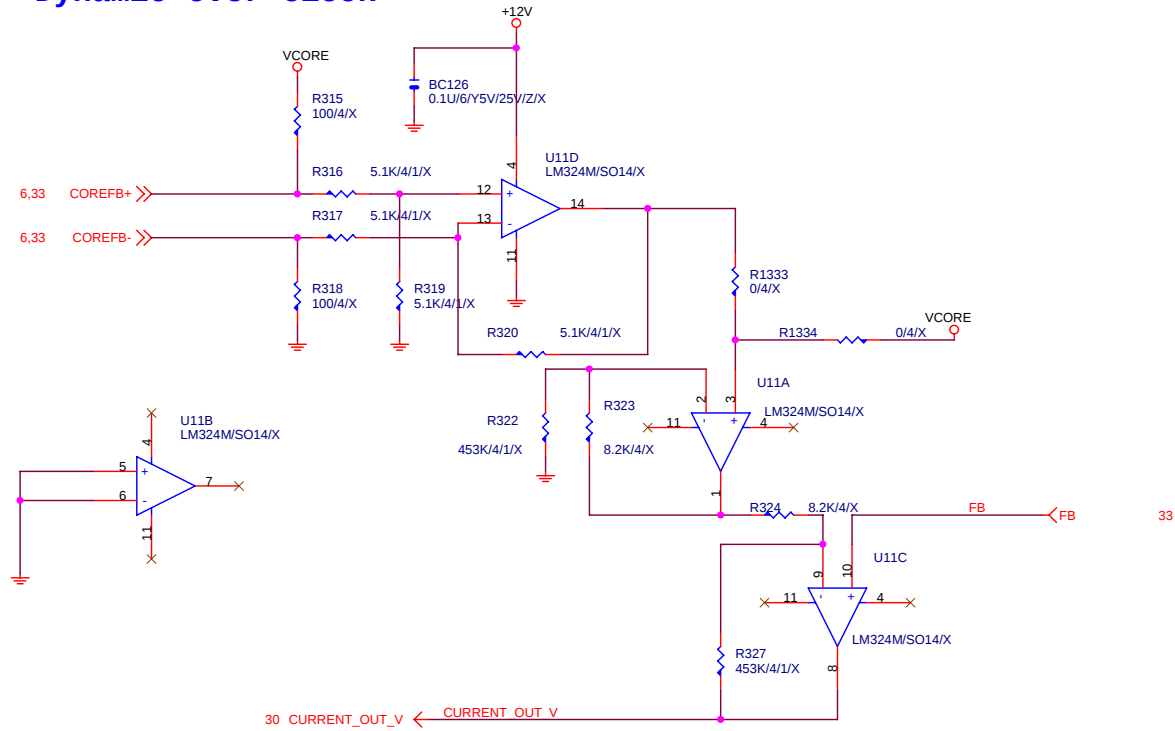






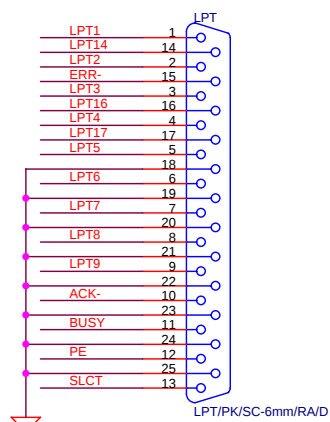
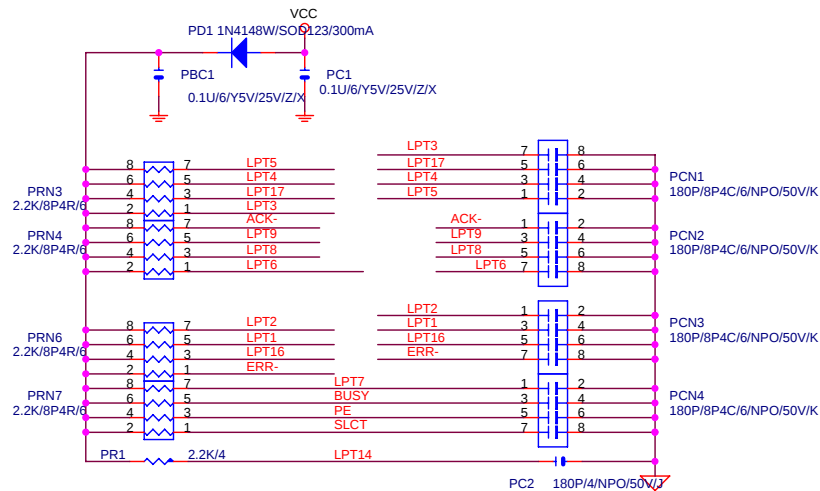
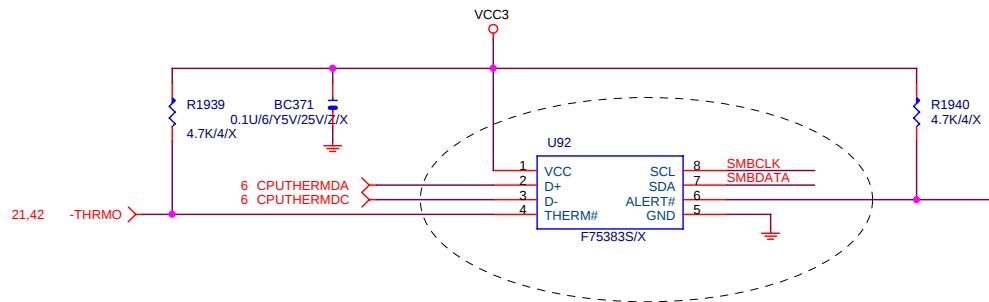


Dynamic Over-Clock

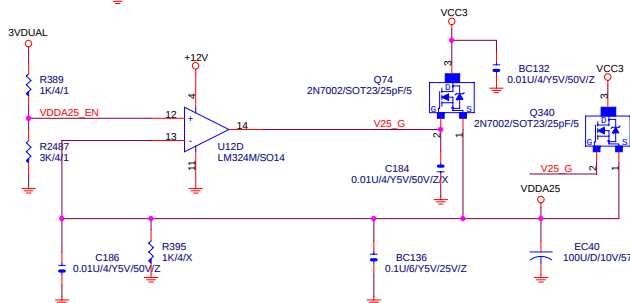
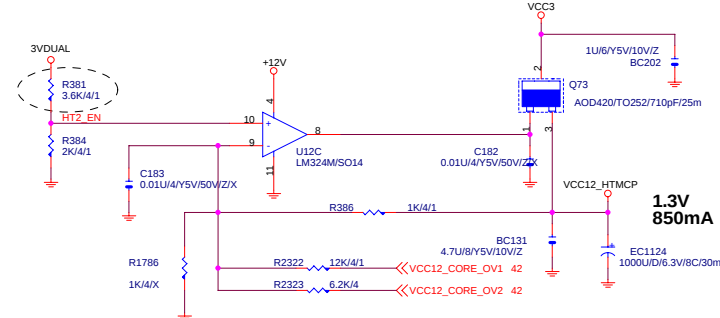
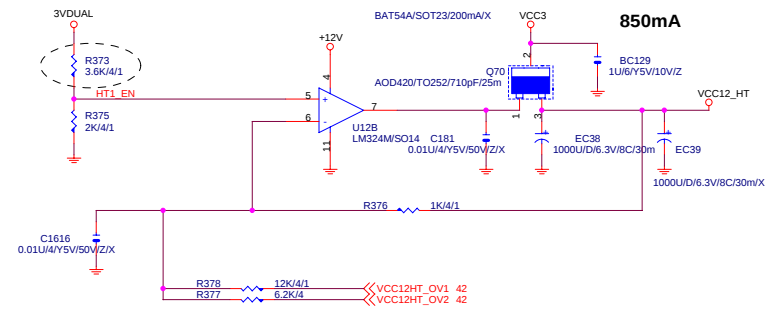
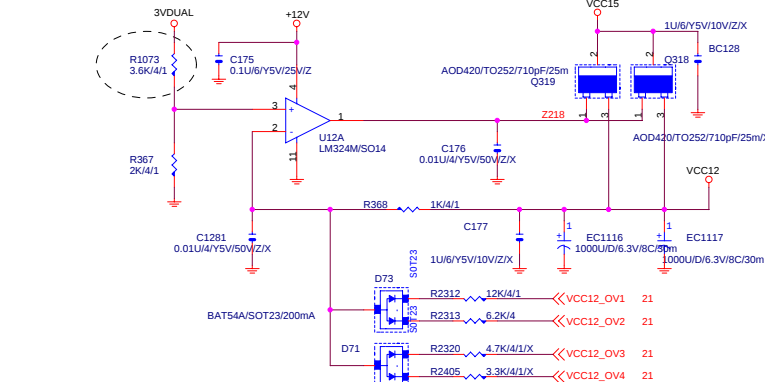
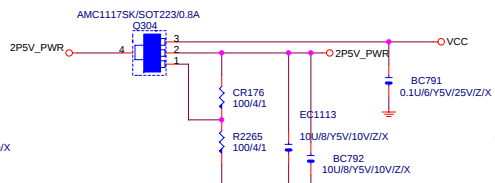
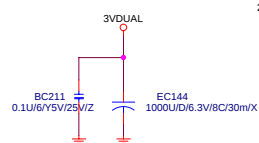
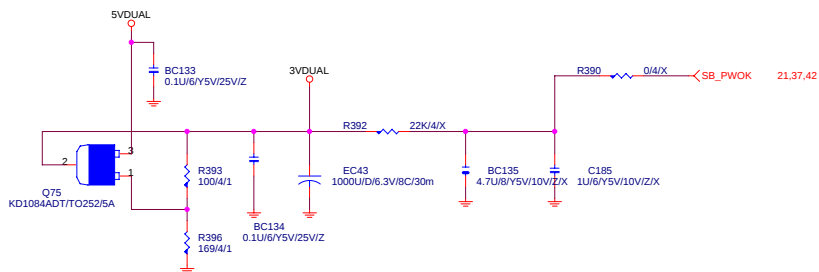
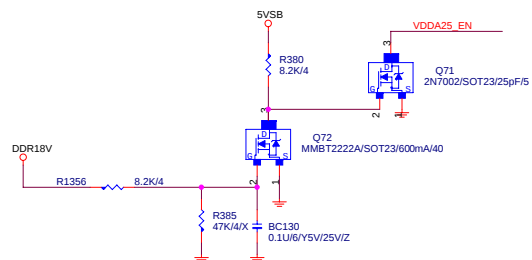
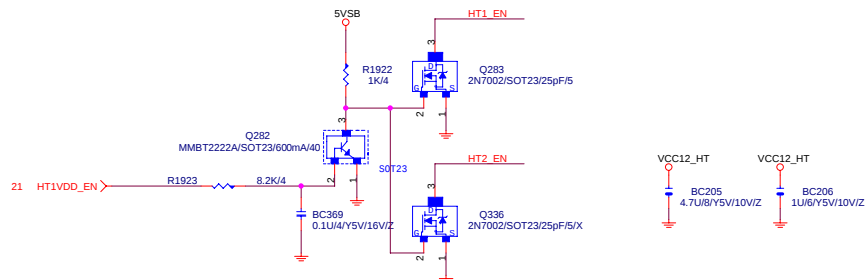
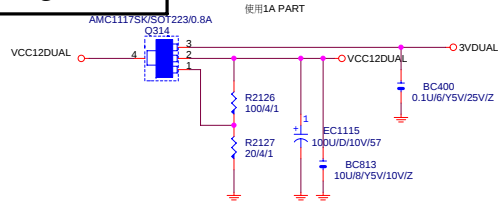


GIGABYTE CORP.

Title			
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Size B	Document Number		Rev
	GA-M59SLI-S4		1.0
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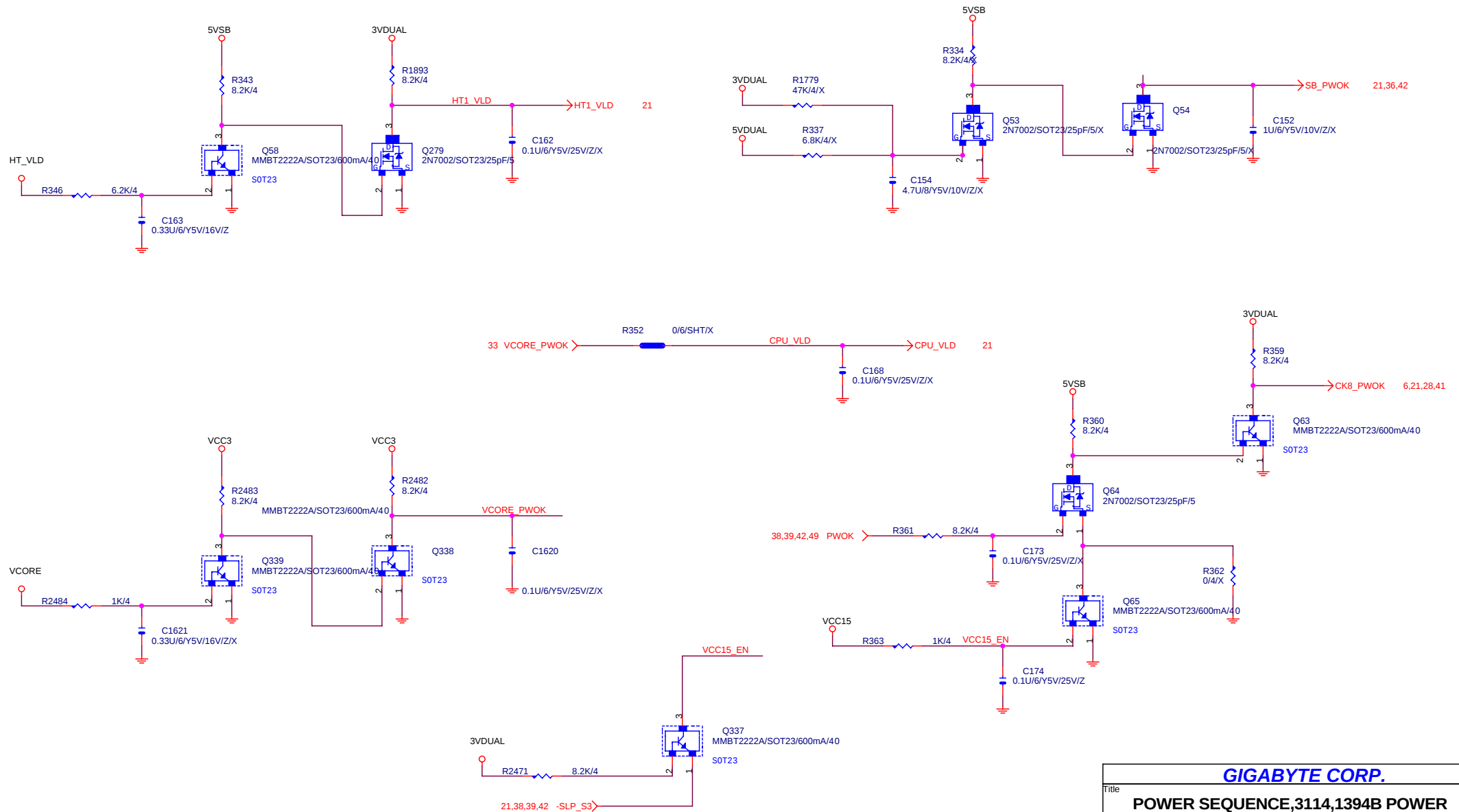


1.5V@850mA Max

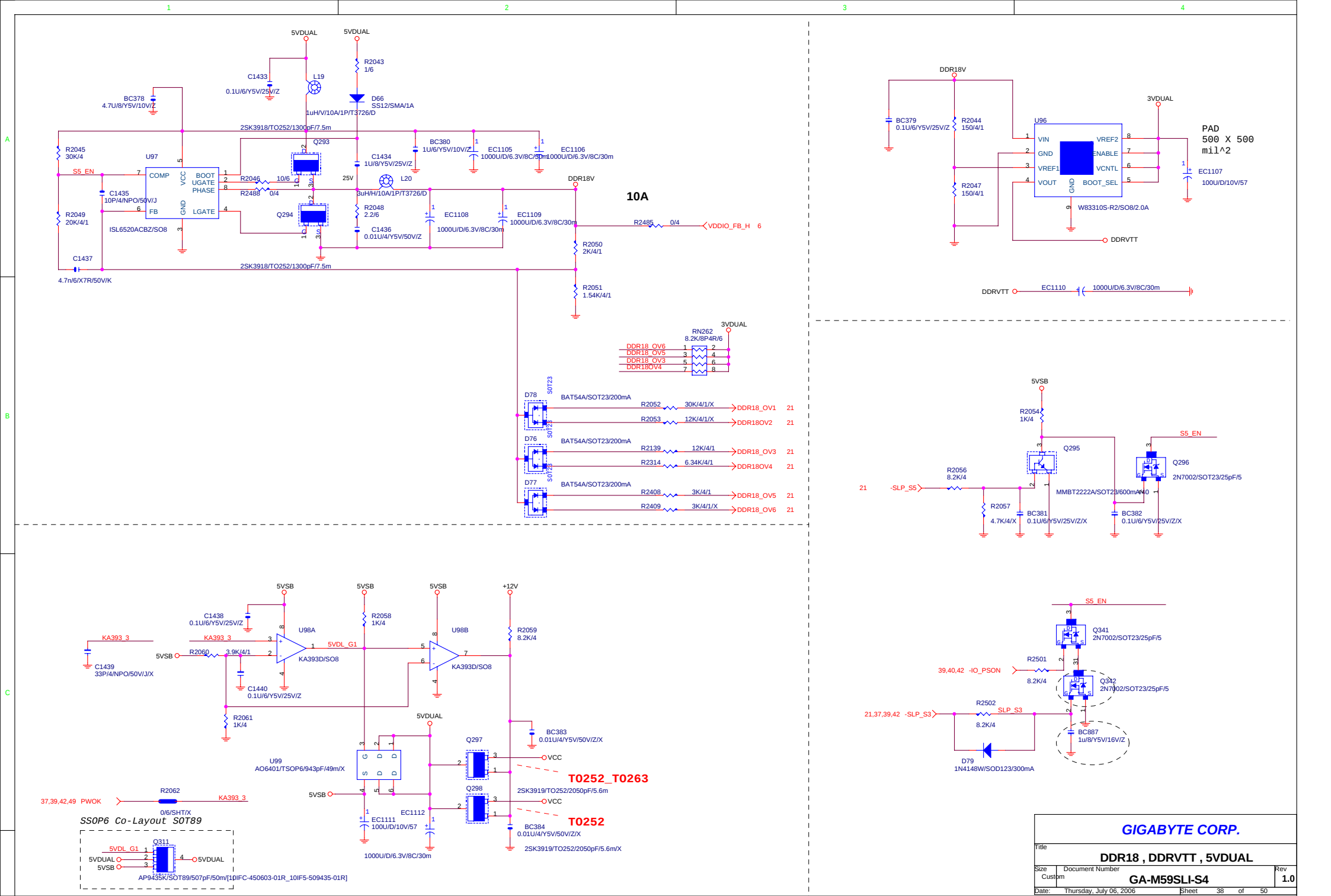


GIGABYTE CORP.			
Title			
VCC12 HT,VCCA25,PLL POWER			
Size	Document Number		Rev
	GA-M59SLI-S4		1.0
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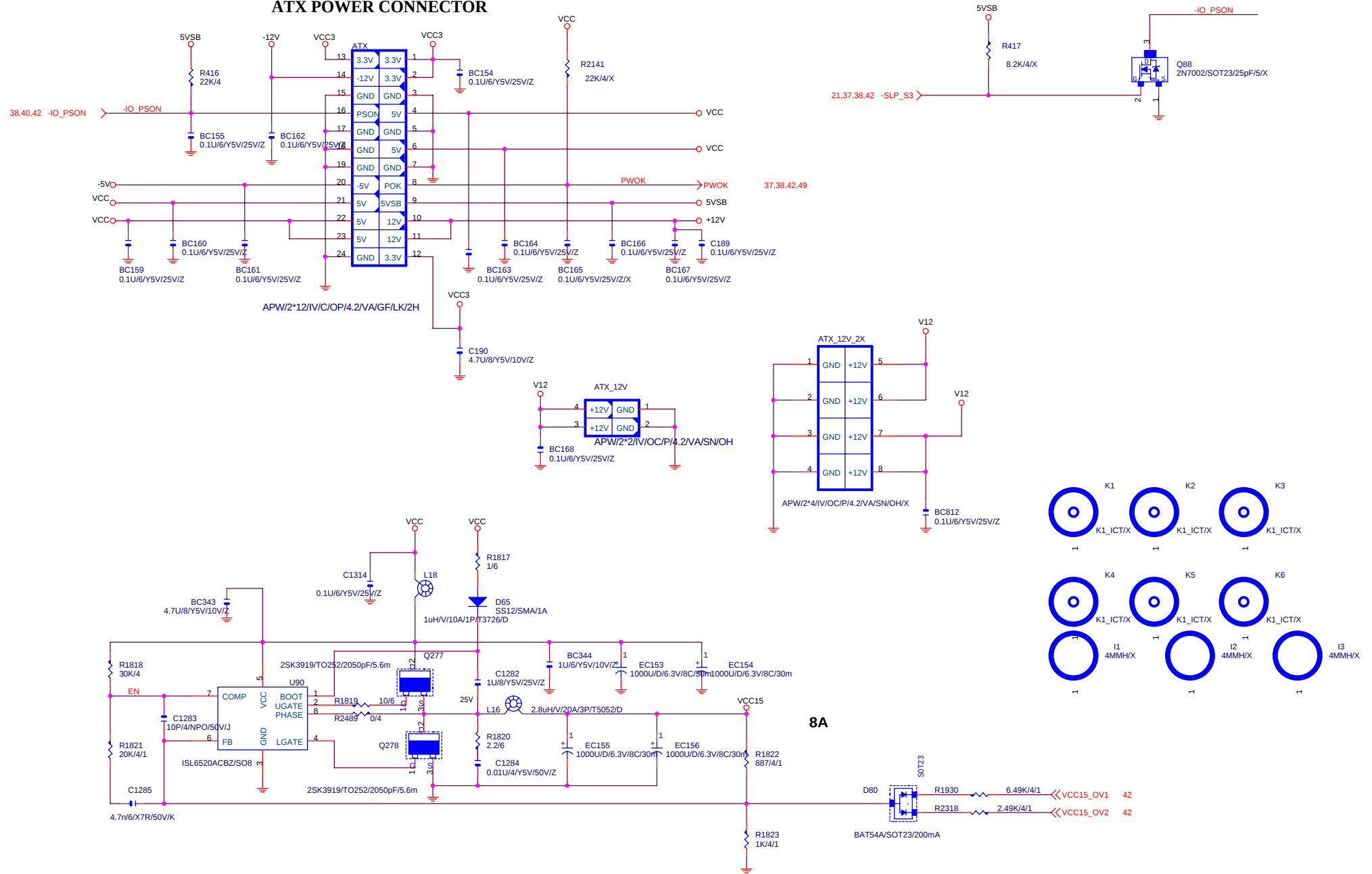
DDR25V FOR DDR DIMM & NB



GIGABYTE CORP.			
Title			
POWER SEQUENCE,3114,1394B POWER			
Size	Document Number		Rev
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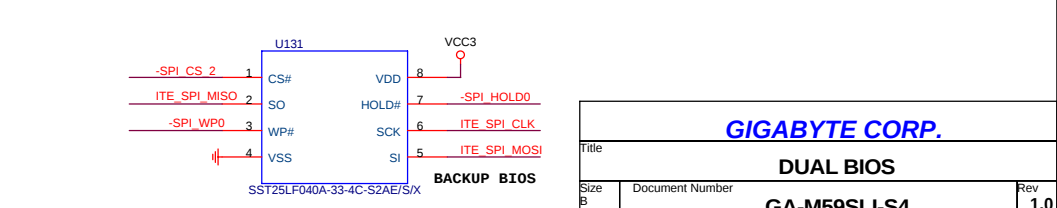
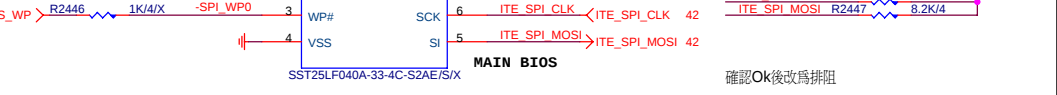
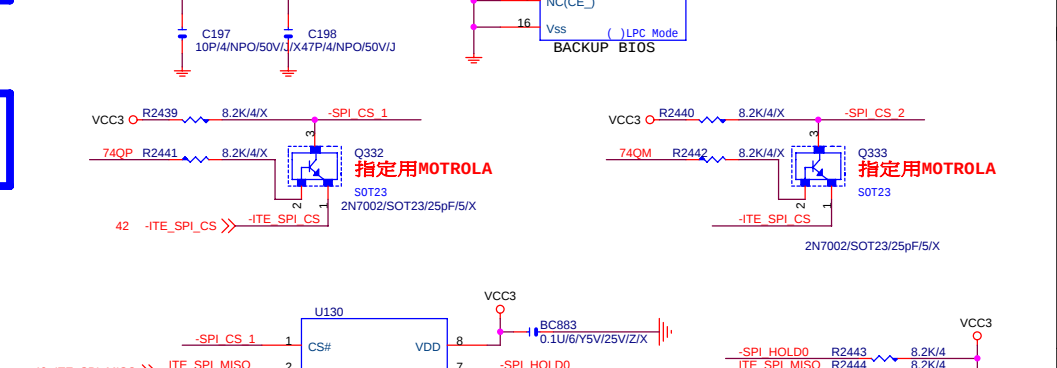
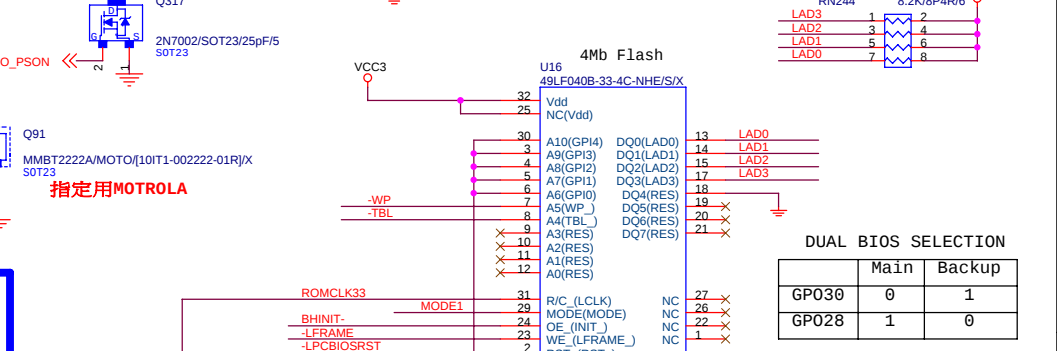
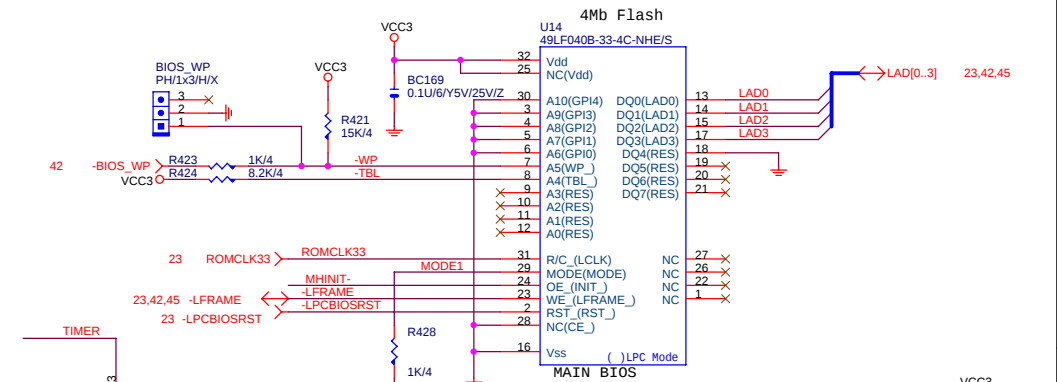
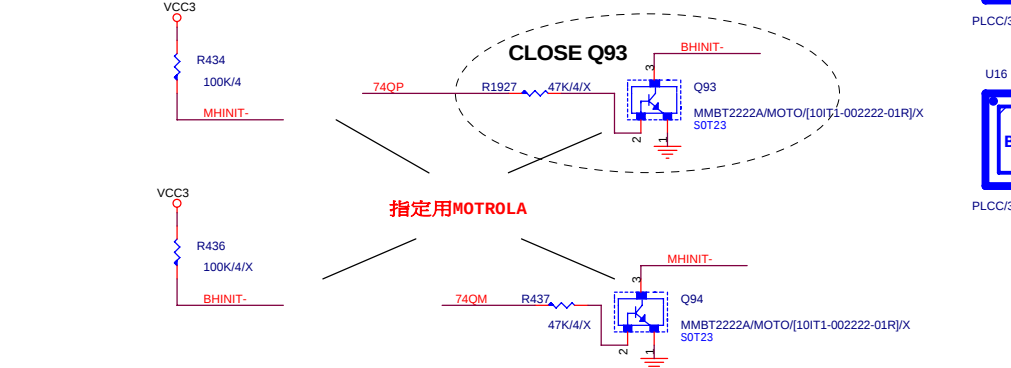
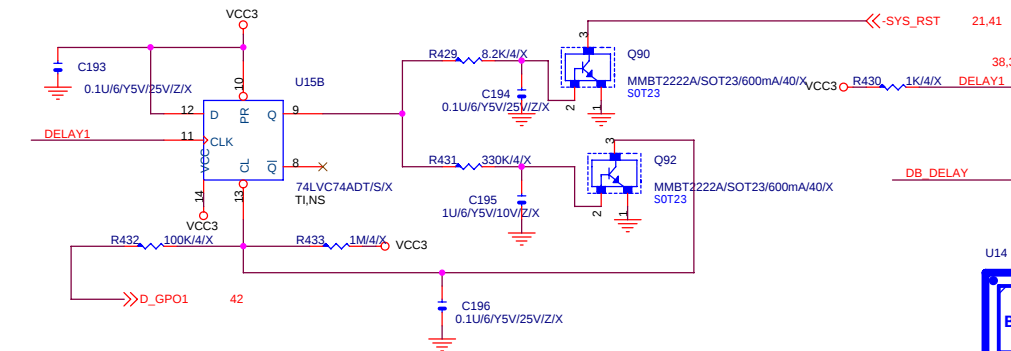
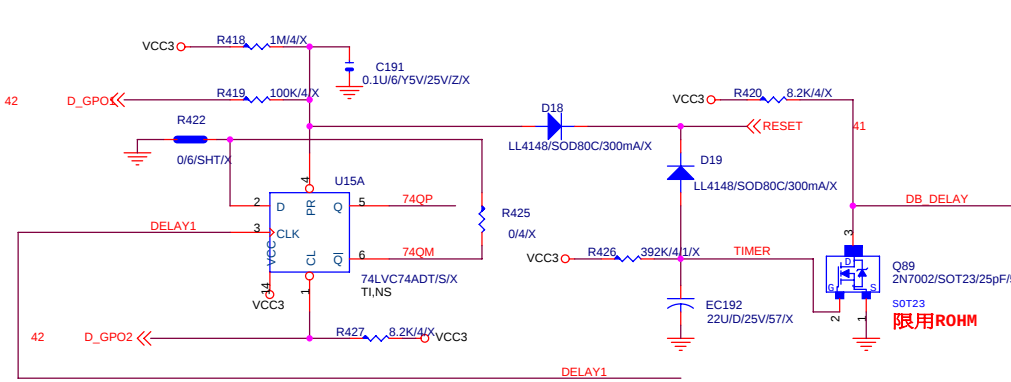


ATX POWER CONNECTOR

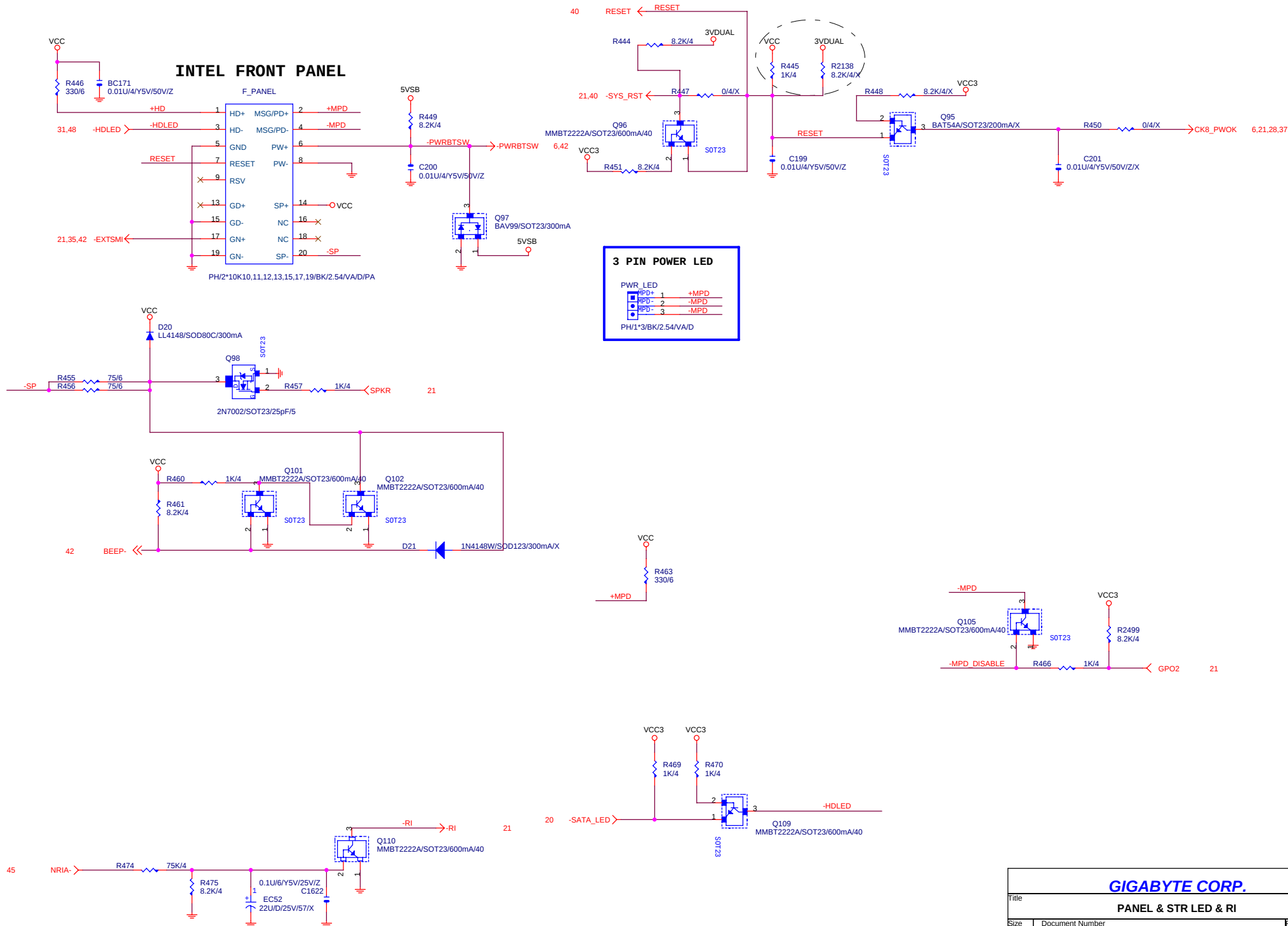


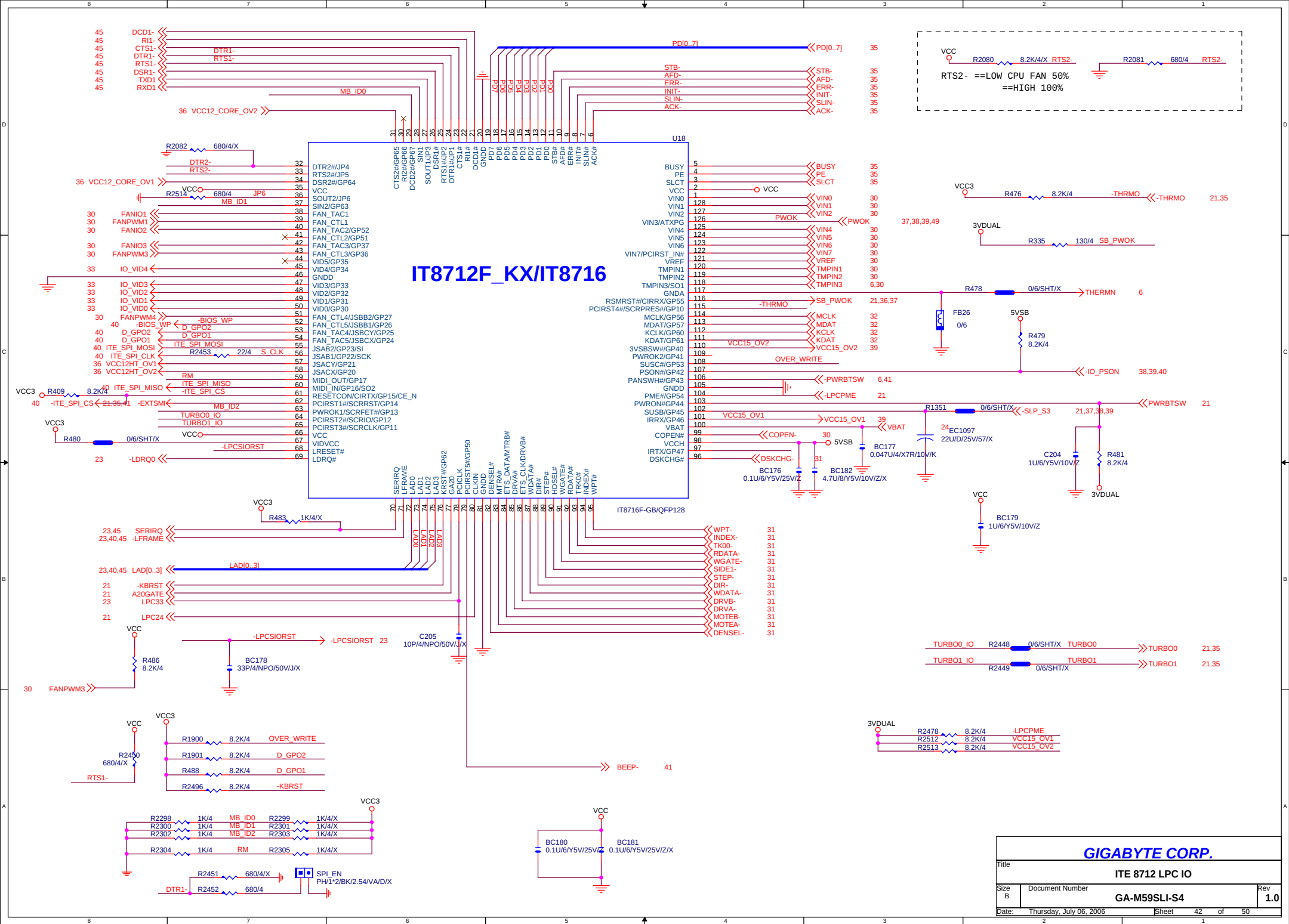
GIGABYTE CORP.

Title			
Misc. PWR & ATX CONN.			
Size B	Document Number		Rev
	GA-M59SLI-S4		1.0
Date:	Sheet	39	of 50

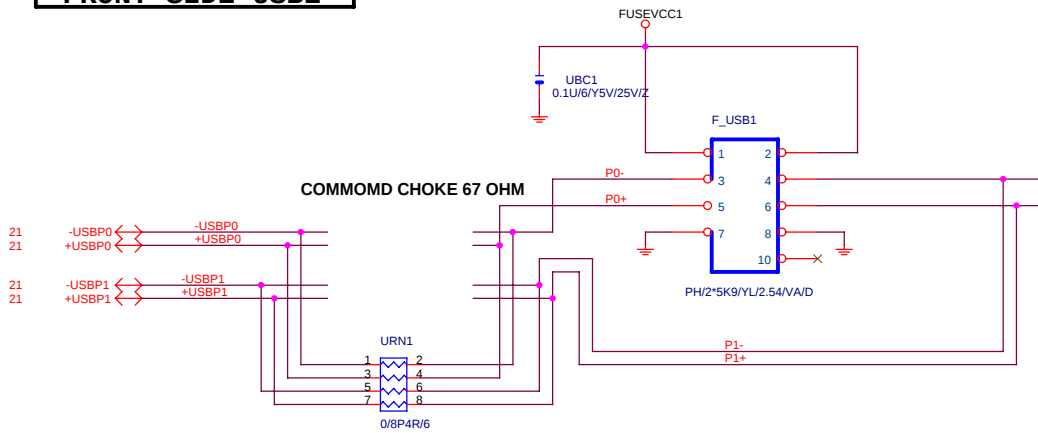


GIGABYTE CORP.			
DUAL BIOS			
Title	Document Number	Rev	1.0
GA-M59SLI-S4			
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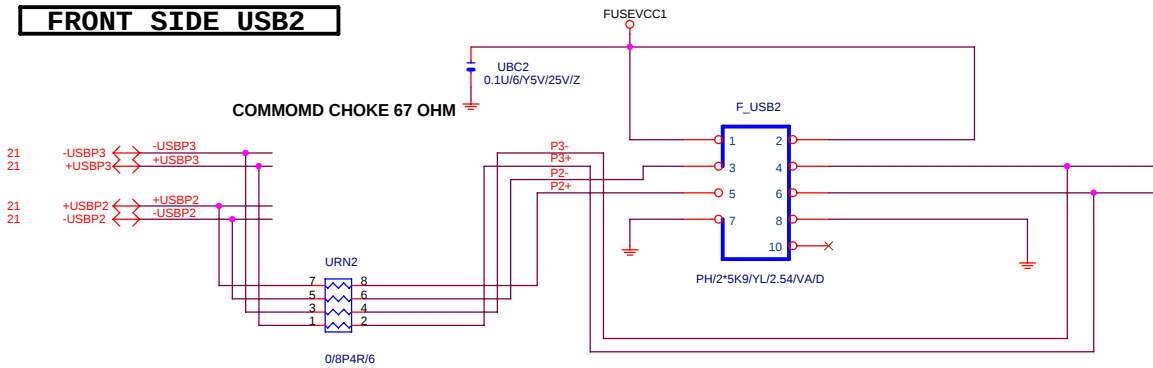




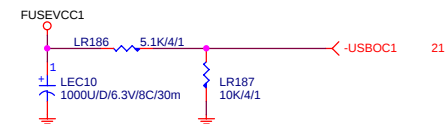
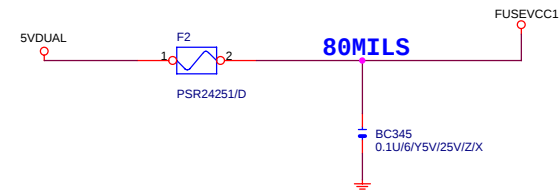
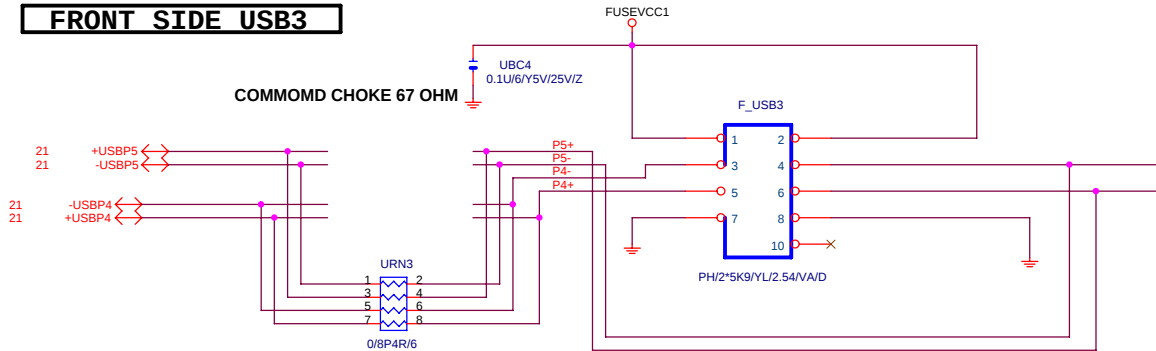
FRONT SIDE USB1

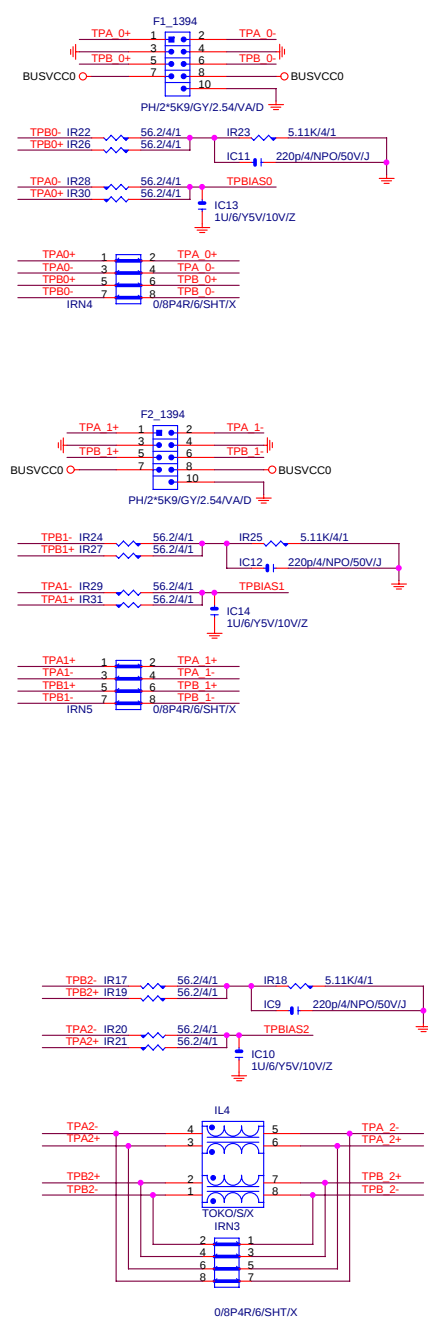
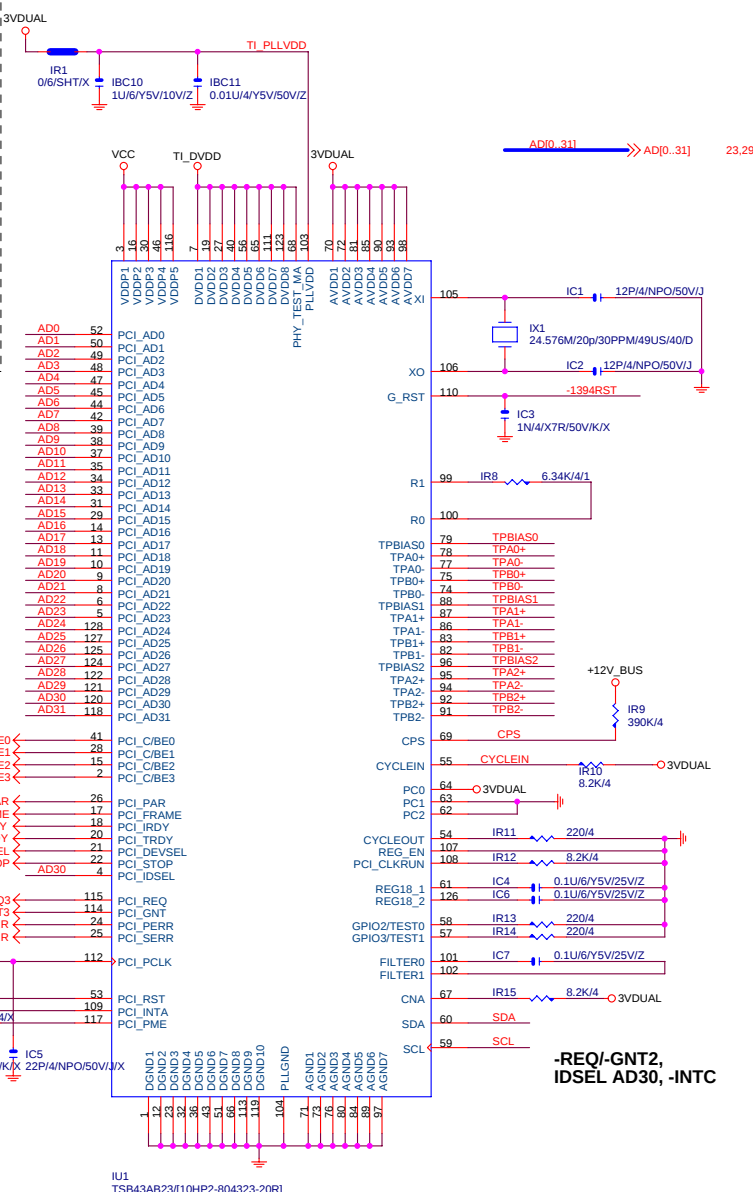
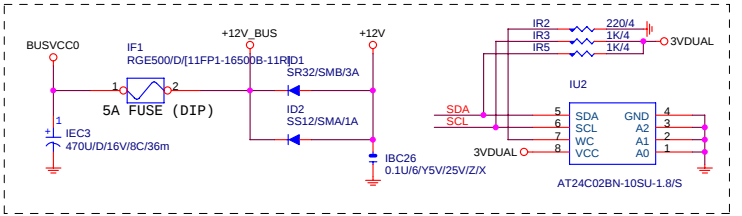
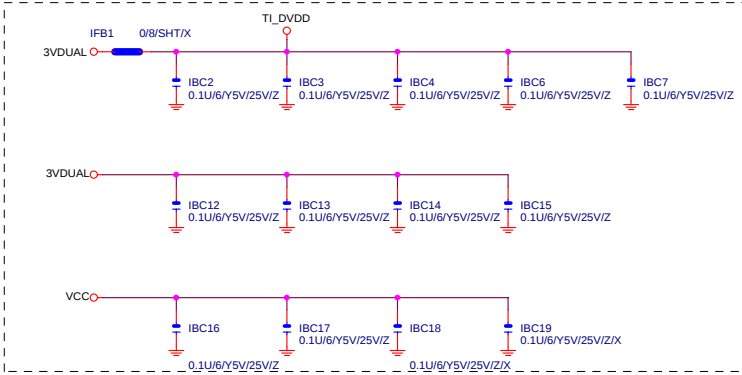


FRONT SIDE USB2

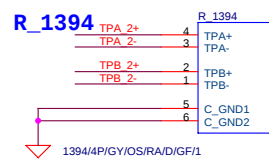


FRONT SIDE USB3

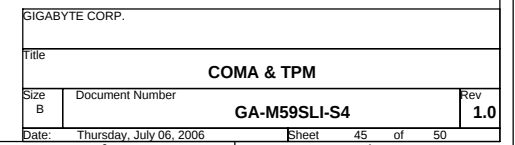
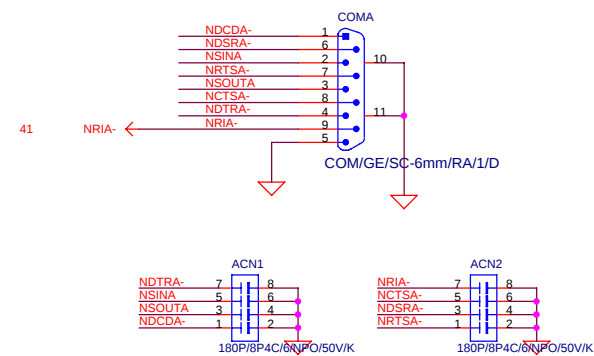




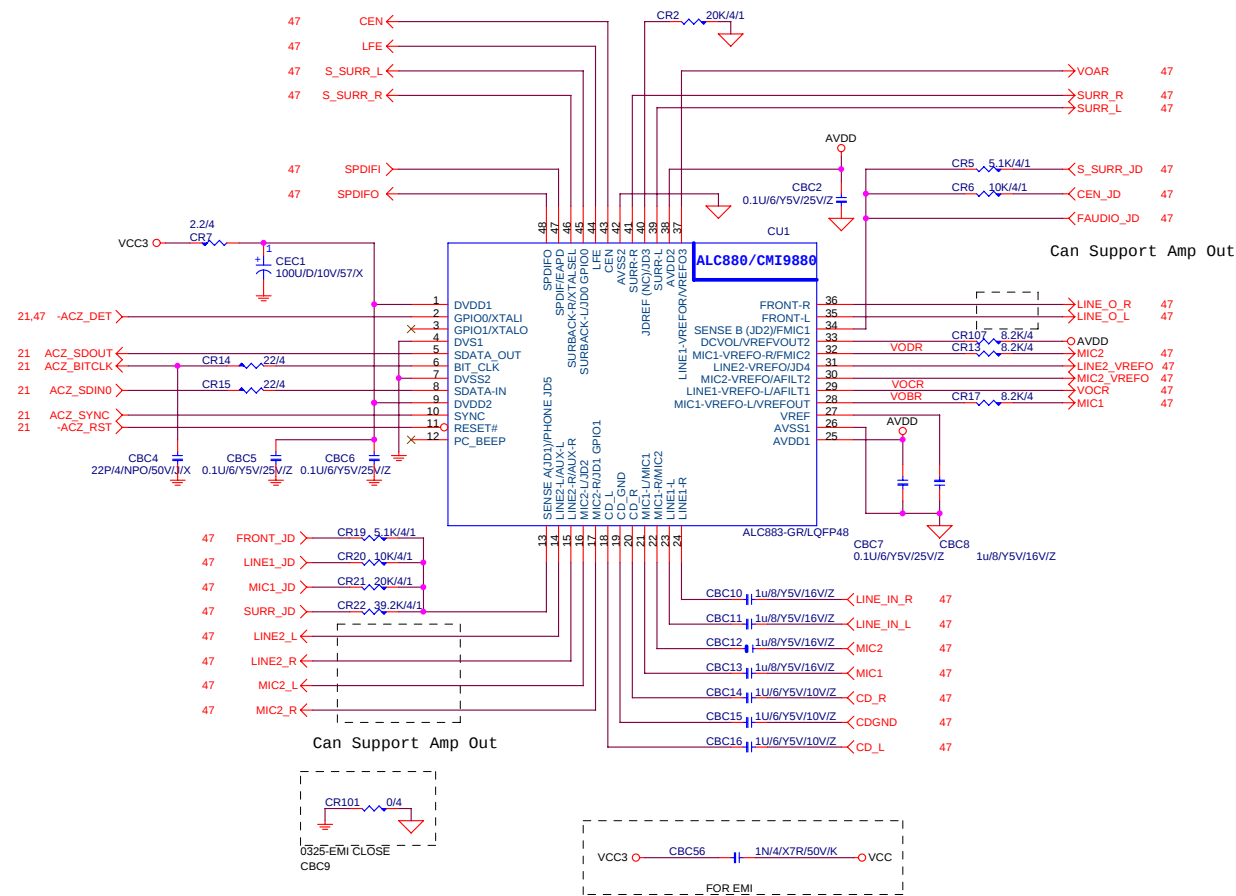
TPA 0-
TPA 0+
TPB 0-
TPB 0+



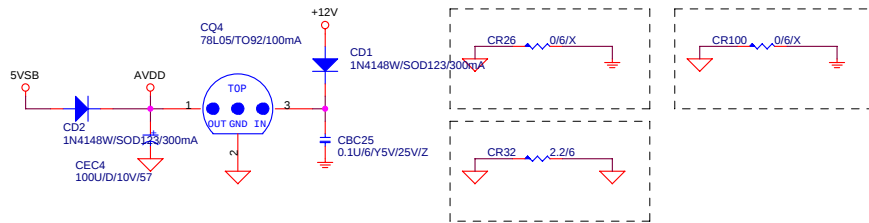
GIGABYTE CORP.			
Title			
TSB43AB23A 1394A			
Size	Document Number	Rev	
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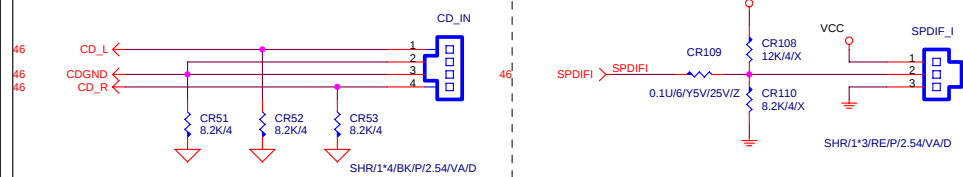
AZALIA CODEC



CODEC POWER/EMI PAD

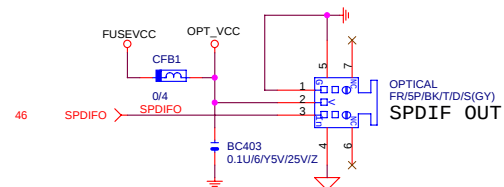
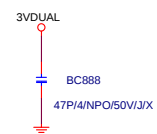


CD IN



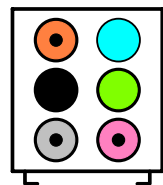
SPDIF

Remove COAXIAL

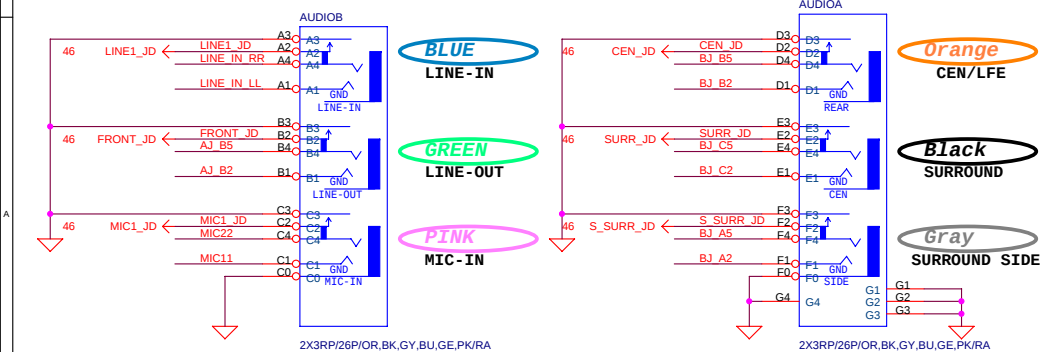


AZALIA JACK

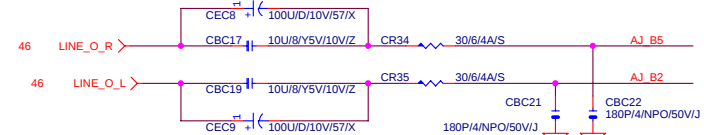
BTX AZALIA CONNECTOR



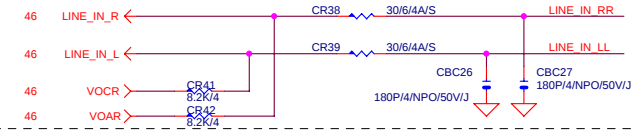
11NR6-403007-21



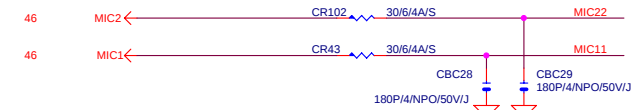
LINE-OUT



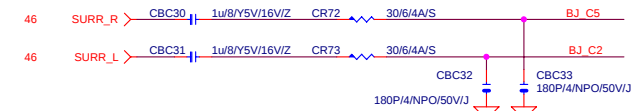
LINE-IN



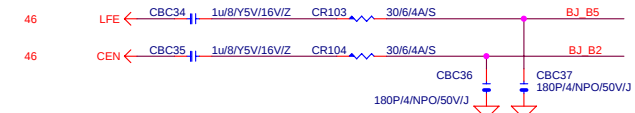
MIC-IN



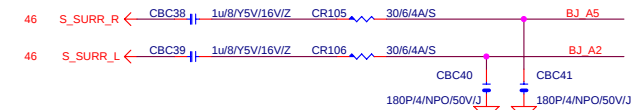
SURROUND



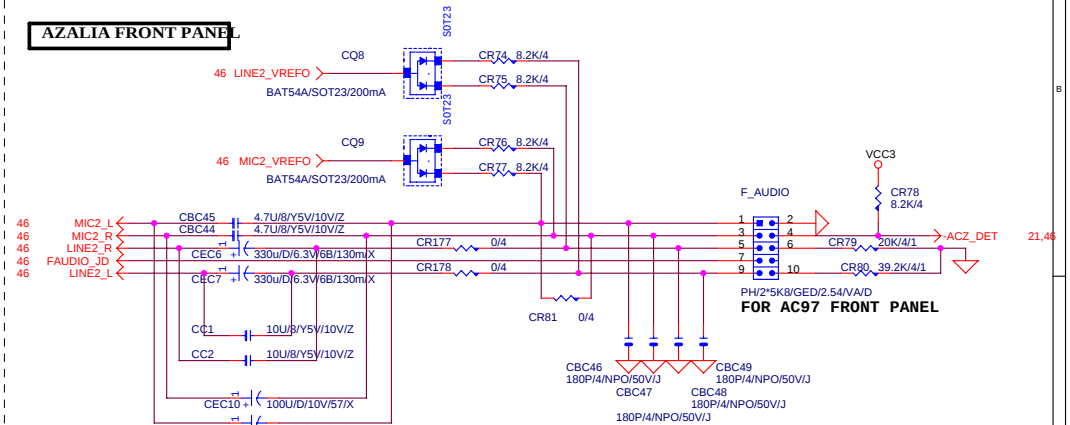
CEN/LFB



SURR BACK



AZALIA FRONT PANEL



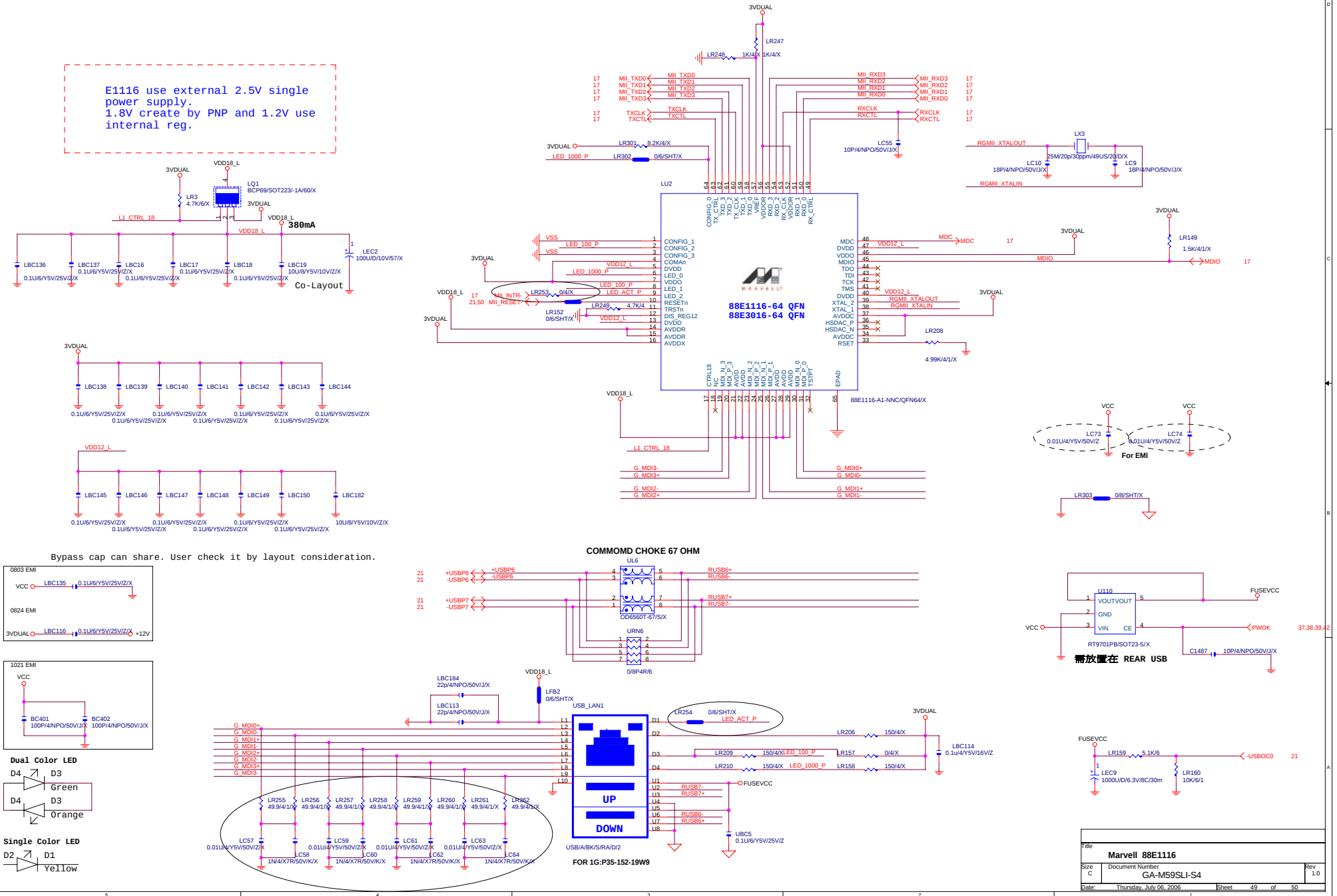
GIGABYTE CORP.

Title			
AUDIO JACK			
Size	Document Number		Rev
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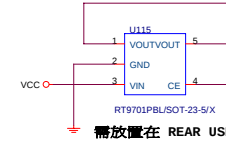
Hardware Configuration: See config_0:4

1. PHY address:00001
2. ENA_XC:Enable Auto-Crossover
3. RGMII_TX:Transmit clock not internally delayed
4. RGMII_RX:Receive clock transition when data transitions
5. Advertise all capabilities

E1116 use external 2.5V single power supply.
1.8V create by PNP and 1.2V use internal reg.



1. PHY address:00010
2. ENA_XC:Enable Auto-Crossover
3. RGMII_TX:Transmit clock not internally delayed
4. RGMII_RX:Receive clock transition when data transitions
5. Advertise all capabilities



File			
Marvell_88E1115_88E1116_88E3016			
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