GA-M55plus-S3G

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30	PWM ISL6566
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33	POWER SEQUENCE
34	BIOS ATX POWER CONNCTOR
35	FRONT PANEL
36	ITE 8716GB/CX
37	Marvell 88E1116
38	TI TSB43AB23 1394

Revision:1.2

Digitally signed by dd
DN: cn=dd, o=dd, ou=dd, email=dddd@yahoo.com, c=US
Date: 2009.12.17 19:06:51 +07'00'

GIGABYTE

Title: BLOCK DIAGRAM

Size: A1 | Custom | Document Number: GA-M55plus-S3G | Rev: 1.2

Date: Thursday, July 06, 2006 | Sheet 1 of 38

Model Name:GA-M55plus-S3G

Component value change history

Version:1.2
P-Code:

Date	Change Item	Reason
2006.03.22	0.1 New BOM Release. PCB:0.1	
2006.04.18	1.0A D_BOM Release. PCB:1.0	LAN_USB remove 11NR6-702010-A1R Remove BIOS socket
		TPM no POP, Remove BIOS socket RM use plastic, F_PANEL use color
		Remove Power LED dual color schematic Add AMD Validation circuit
2006.05.02	1.0B P_BOM Release. PCB:1.0	RM change to orange. PCIE x16 change to blue. 11AC1-021164-81R
		CPU fan speed. 15K-->8.2K Update new packing list BC7 for EMI
2006.05.08	1.0B ECN Release. PCB:1.0	Add VGA cap: 12PC1-V00001-01R, and Q74 2nd source.
2006.06.07	1.1A E_BOM Release. PCB:1.1	Modify DVI I2C PU ,74LVC08A change to SOIC
2006.06.12	1.2A E_BOM Release. PCB:1.2	Change VDDA25 generate method.
2006.06.28	1.2A P_BOM Release. PCB:1.2	For PVT use. Add packing list.
2006.07.06	1.2B P_BOM Release. PCB:1.2	Add ESD protect Diode. And combine repeat source.

Circuit or PCB layout change for next version

Date	Change Item	Reason
2006.03.17	0.1 Gerber Out	
2006.04.14	1.0 Gerber Out Rename to GA-M55plus-S3G	
2006.06.06	1.1 Gerber Out	Modify DVI I2C PU ,74LVC08A change to SOIC
2006.06.13	1.2 Gerber Out	Change VDDA25 generate method.

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Title: BOM & PCB MODIFY HISTORY

Size: Custom | Document Number: GA-M55plus-S3G | Rev: 1.2

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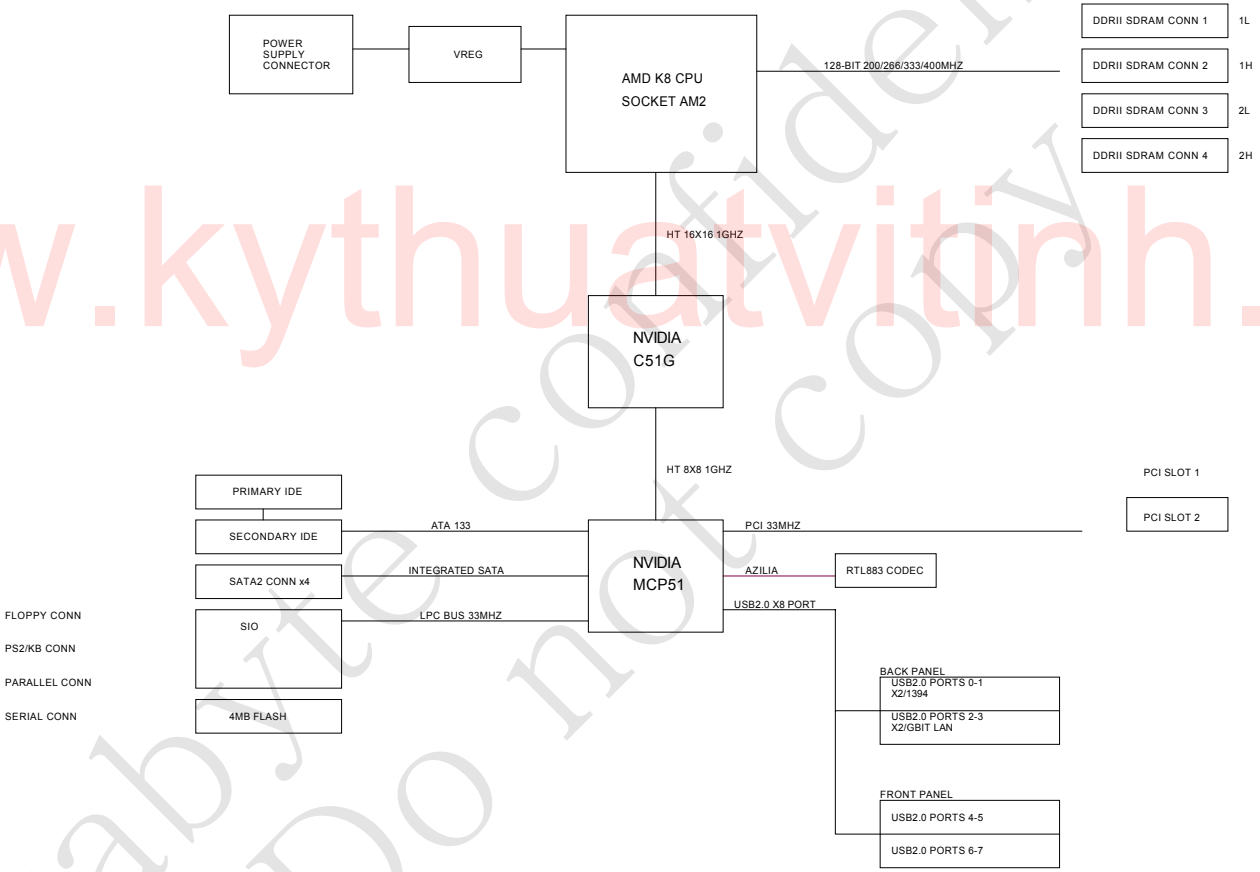
BLOCK DIAGRAM



GIGABYTE		
Title: BLOCK DIAGRAM		
Size: Custom	Document Number: GA-M55plus-S3G	Rev: 1.2
Date: Thursday, July 06, 2006	Sheet 3 of 38	

L0_CADIN_L[0..15] <11>
L0_CADIN_H[0..15] <11>
L0_CLKIN_L[0..1] <11>
L0_CLKIN_H[0..1] <11>
L0_CADOUT_L[0..15] <11>
L0_CADOUT_H[0..15] <11>
L0_CLKOUT_L[0..1] <11>
L0_CLKOUT_H[0..1] <11>

CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR18V
CPU_VTT_SUS = DDRVTT

VLDT_A = VCC12_HT
VLDT_B = HT12B

M2CPUA

HYPERTRANSPORT

VCC12_HT R3 49.9/4/1 V4
GND R4 49.9/4/1 V5
<11> L0_CTLIN_H0 L0_CTLIN_H0 U1
<11> L0_CTLIN_L0 L0_CTLIN_L0 V1

L0_CLKIN_H1 N6
L0_CLKIN_L1 P6
L0_CLKIN_H0 N3
L0_CLKIN_L0 N2

L0_CADIN_H15 U6
L0_CADIN_L15 V6
L0_CADIN_H14 T4
L0_CADIN_L14 T5
L0_CADIN_H13 R6
L0_CADIN_L13 T6
L0_CADIN_H12 P4
L0_CADIN_L12 P5
L0_CADIN_H11 M4
L0_CADIN_L11 M5
L0_CADIN_H10 L6
L0_CADIN_L10 M6
L0_CADIN_H9 K4
L0_CADIN_L9 K5
L0_CADIN_H8 J6
L0_CADIN_L8 K6

L0_CADIN_H7 U3
L0_CADIN_L7 U2
L0_CADIN_H6 R1
L0_CADIN_L6 T1
L0_CADIN_H5 R3
L0_CADIN_L5 R2
L0_CADIN_H4 N1
L0_CADIN_L4 P1
L0_CADIN_H3 L1
L0_CADIN_L3 M1
L0_CADIN_H2 L3
L0_CADIN_L2 L2
L0_CADIN_H1 J1
L0_CADIN_L1 K1
L0_CADIN_H0 J3
L0_CADIN_L0 J2

L0_CLKOUT_H1 AD5
L0_CLKOUT_L1 AD4
L0_CLKOUT_H0 AD1
L0_CLKOUT_L0 AC1

Y6 1 TP78
W6 1 TP79
L0_CTLOUT_H0 W2
L0_CTLOUT_L0 W3
L0_CTLOUT_H0 <11>
L0_CTLOUT_L0 <11>

L0_CADOUT_H15 Y5
L0_CADOUT_L15 Y4
L0_CADOUT_H14 AB6
L0_CADOUT_L14 AA6
L0_CADOUT_H13 AB5
L0_CADOUT_L13 AB4
L0_CADOUT_H12 AD6
L0_CADOUT_L12 AC6
L0_CADOUT_H11 AF6
L0_CADOUT_L11 AF6
L0_CADOUT_H10 AF5
L0_CADOUT_L10 AF4
L0_CADOUT_H9 AH6
L0_CADOUT_L9 AG6
L0_CADOUT_H8 AH5
L0_CADOUT_L8 AH4

L0_CADOUT_H7 Y1
L0_CADOUT_L7 W1
L0_CADOUT_H6 AA2
L0_CADOUT_L6 AA3
L0_CADOUT_H5 AB1
L0_CADOUT_L5 AA1
L0_CADOUT_H4 AC2
L0_CADOUT_L4 AC3
L0_CADOUT_H3 AE2
L0_CADOUT_L3 AE3
L0_CADOUT_H2 AF1
L0_CADOUT_L2 AE1
L0_CADOUT_H1 AG2
L0_CADOUT_L1 AG3
L0_CADOUT_H0 AH1
L0_CADOUT_L0 AG1

SOCKET_M2 M2/[12KRC-04K807-41R]

GIGABYTE

Title: CPU HYPER TRANSPORT

Size: Custom | Document Number: GA-M55plus-S3G | Rev: 1.2

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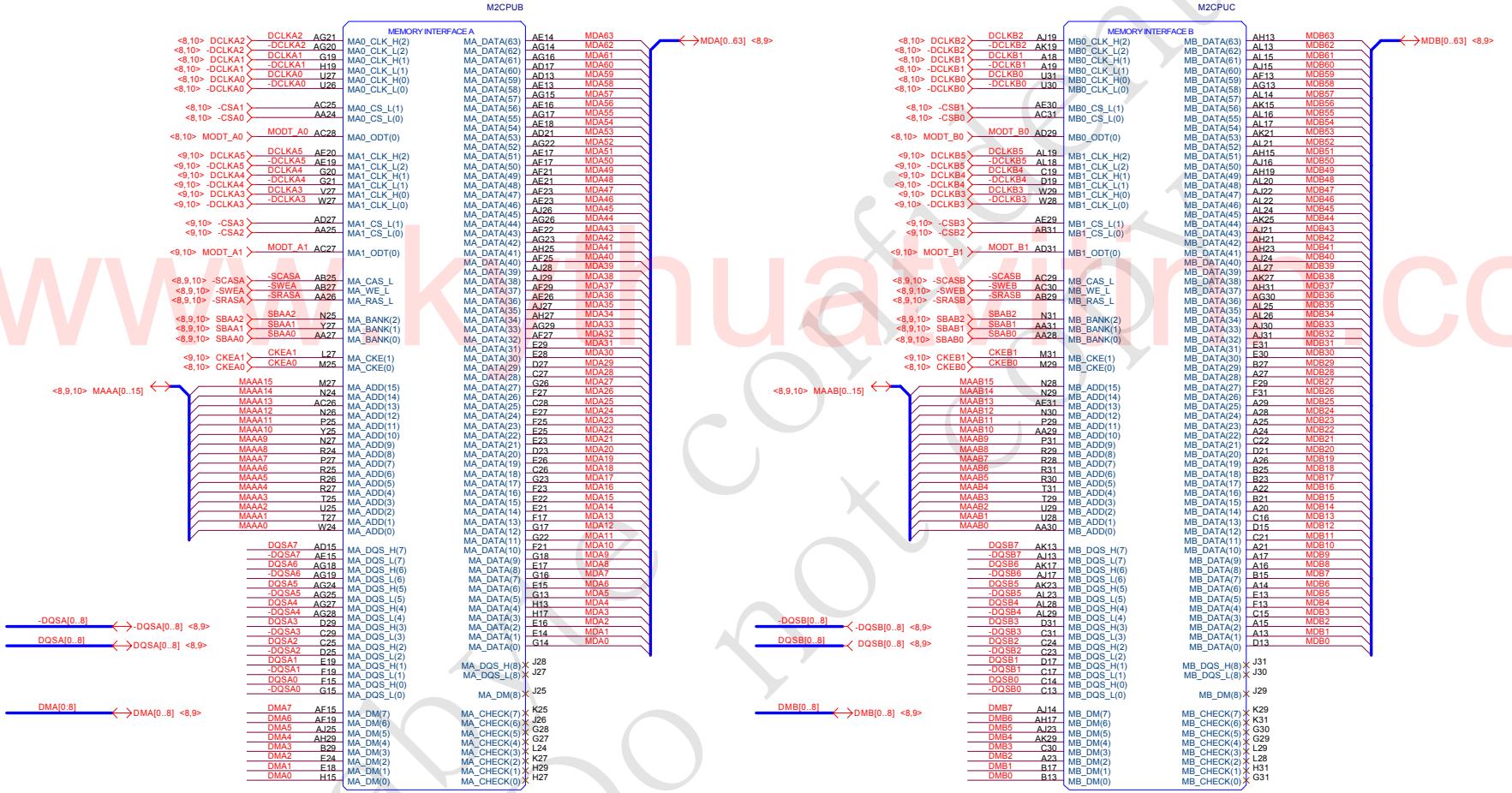
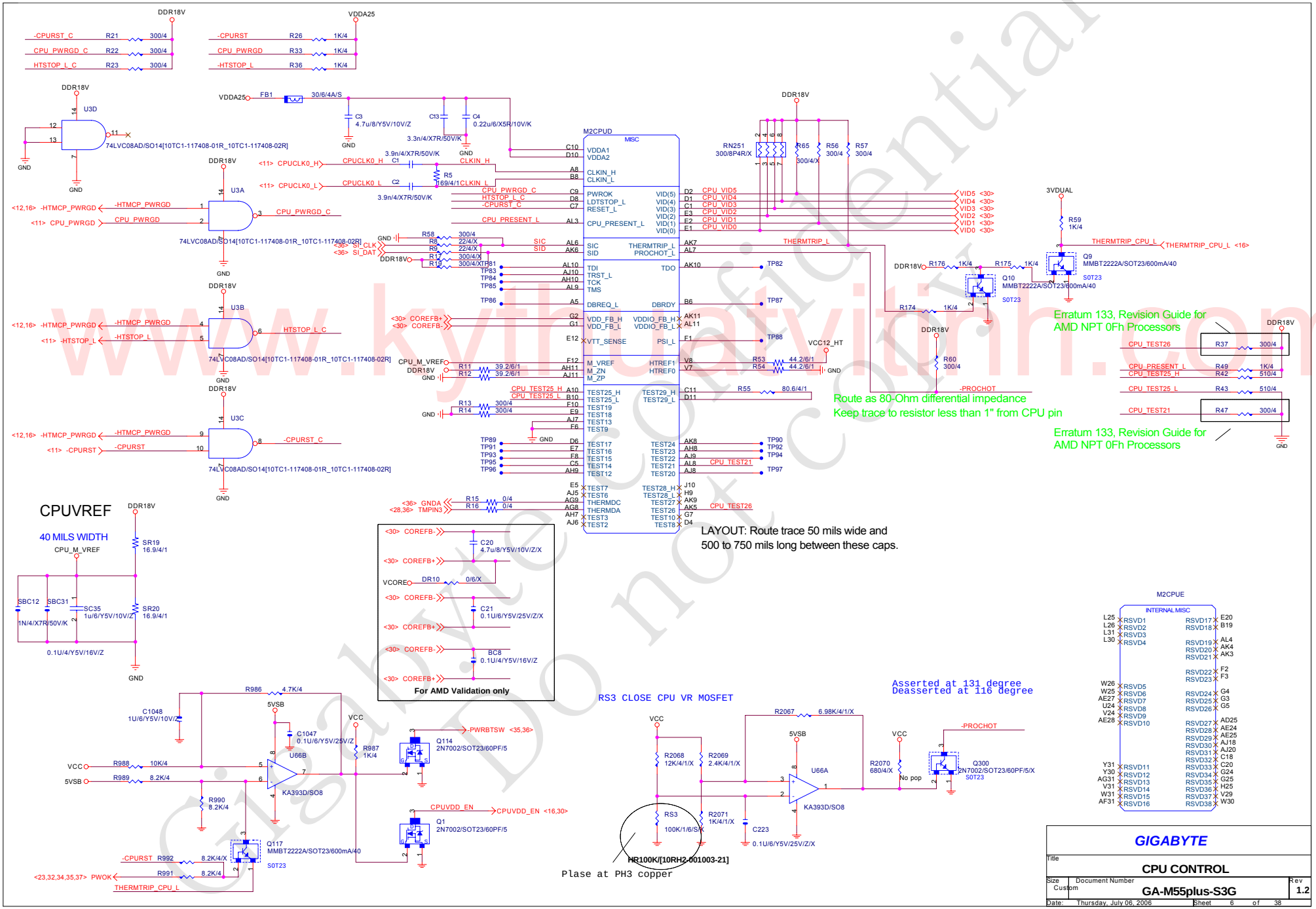


GIGABYTE

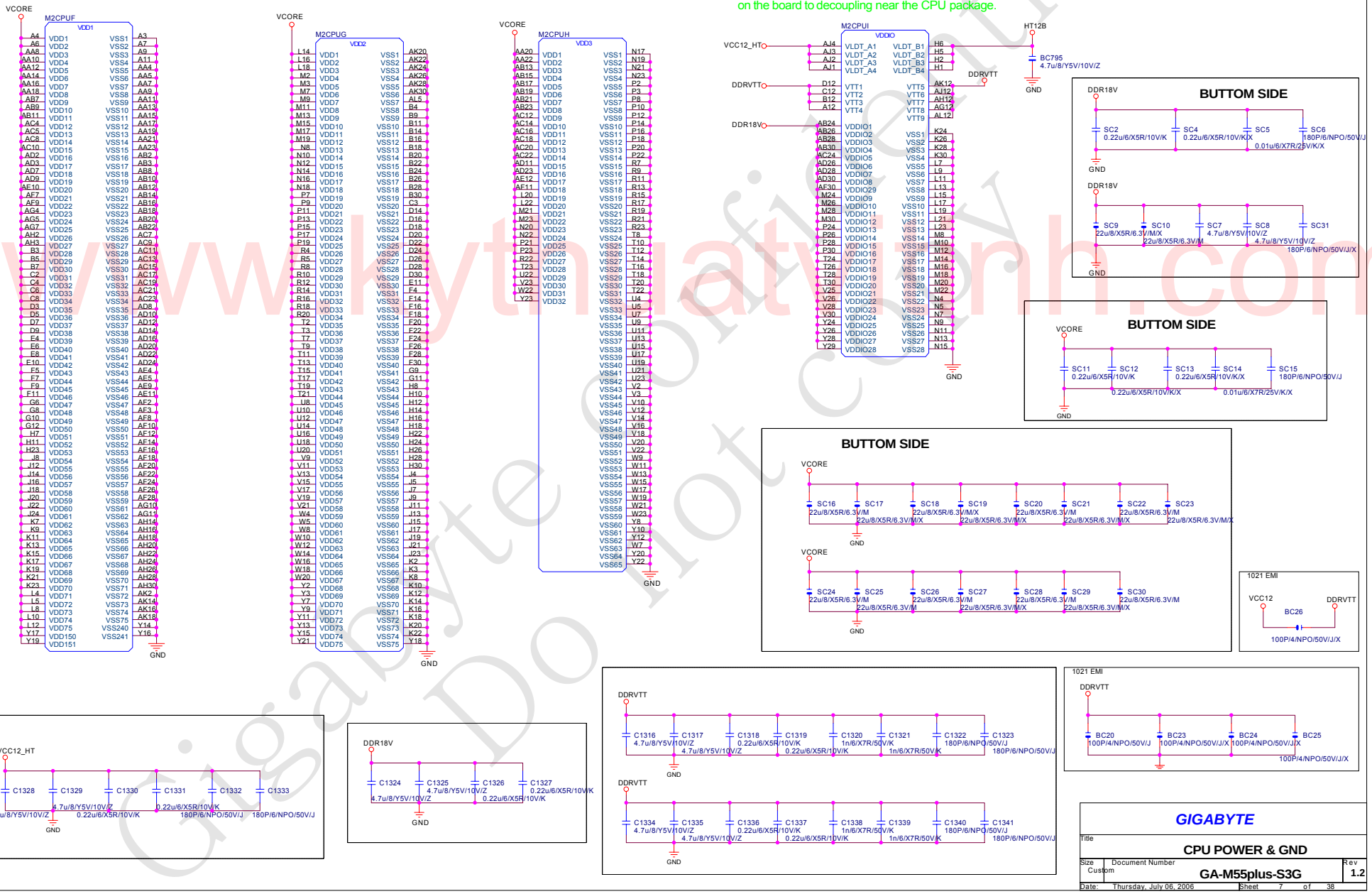
Title: CPU DDRII MEMORY

Size: Custom | Document Number: GA-M55plus-S3G | Rev: 1.2

Date: Thursday, July 06, 2006 | Sheet 5 of 38



VLDT_RUN_B is connected to the VLDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.



GIGABYTE

Title: CPU POWER & GND

Size: Custom | Document Number: GA-M55plus-S3G | Rev: 1.2

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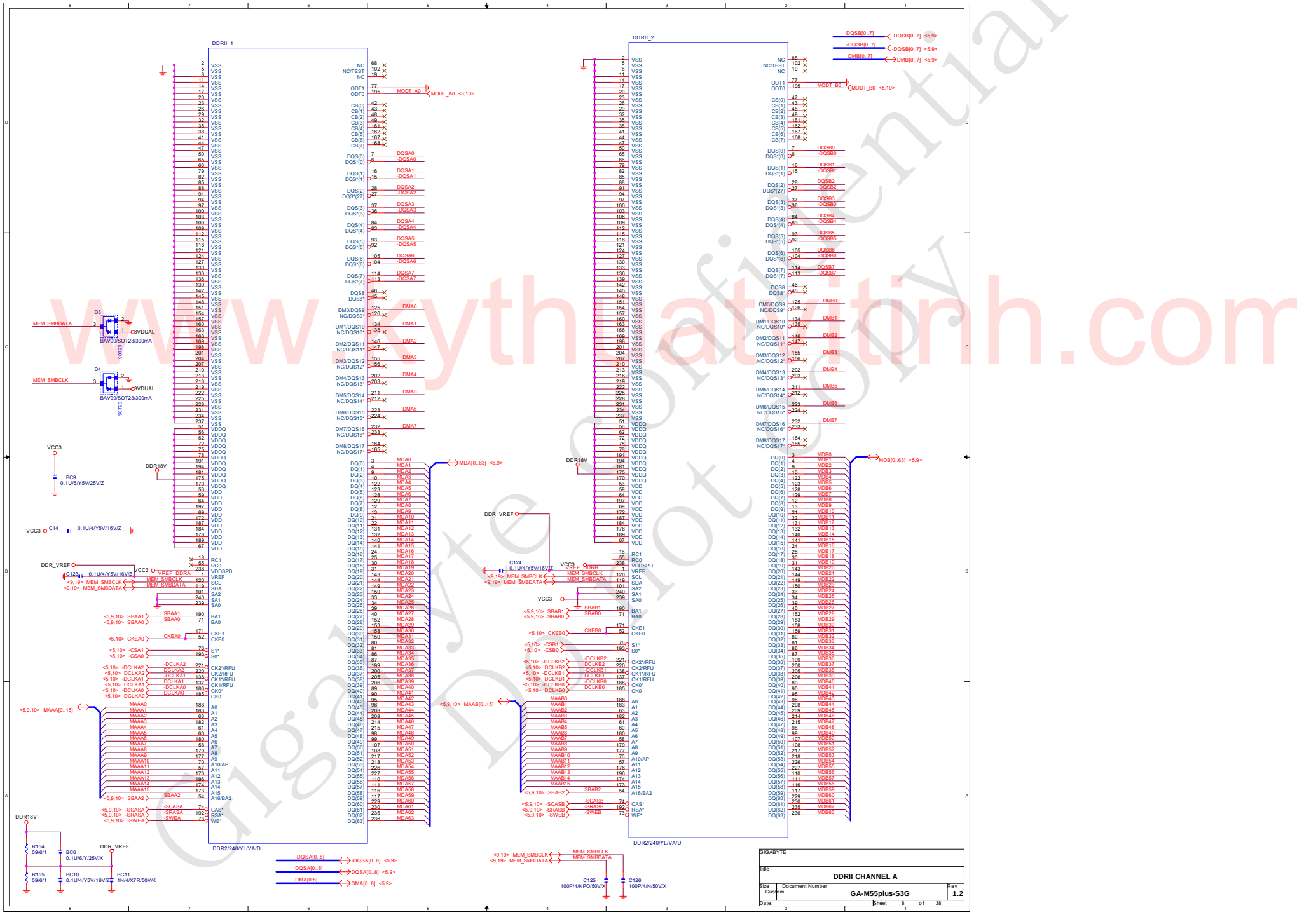

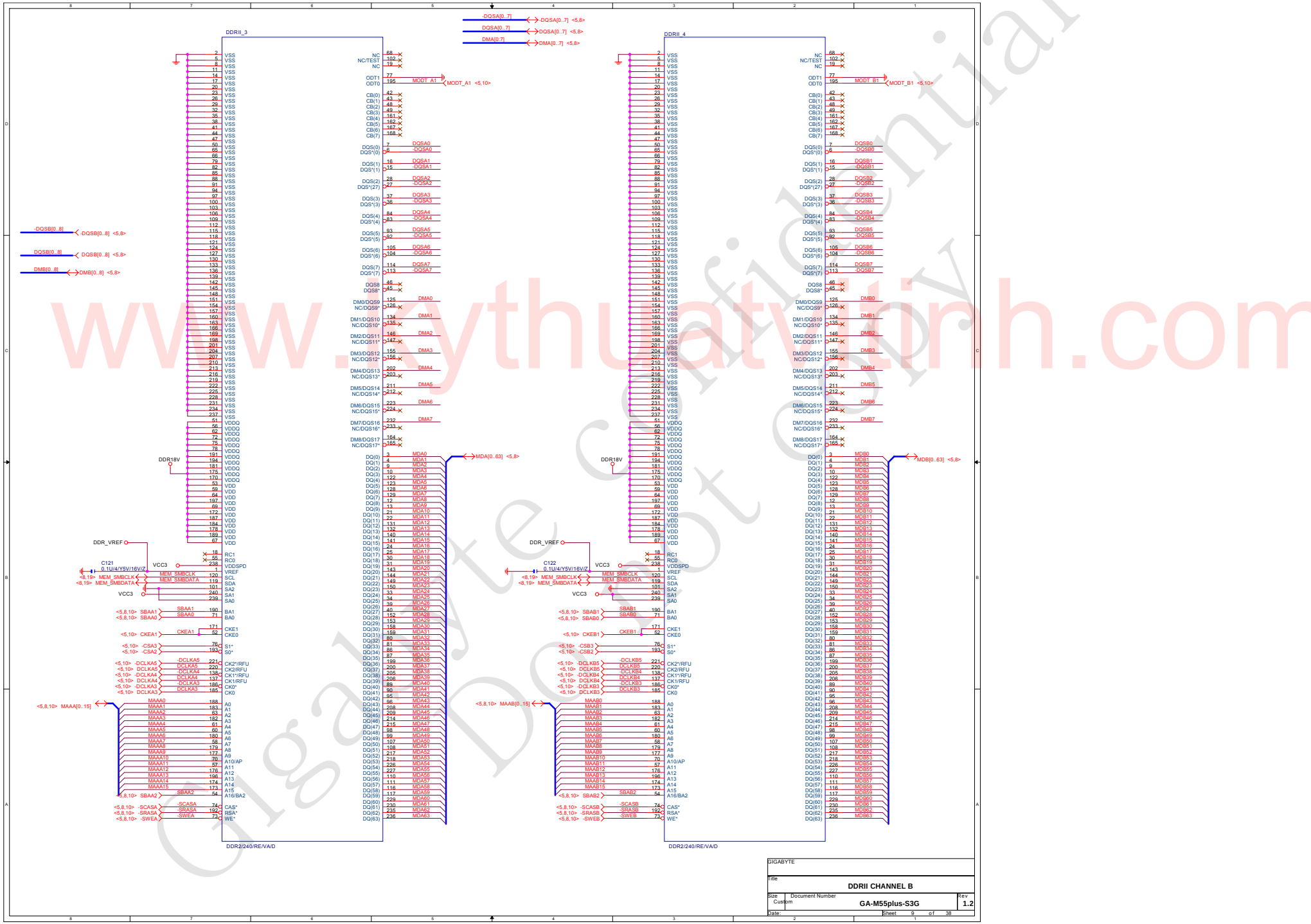

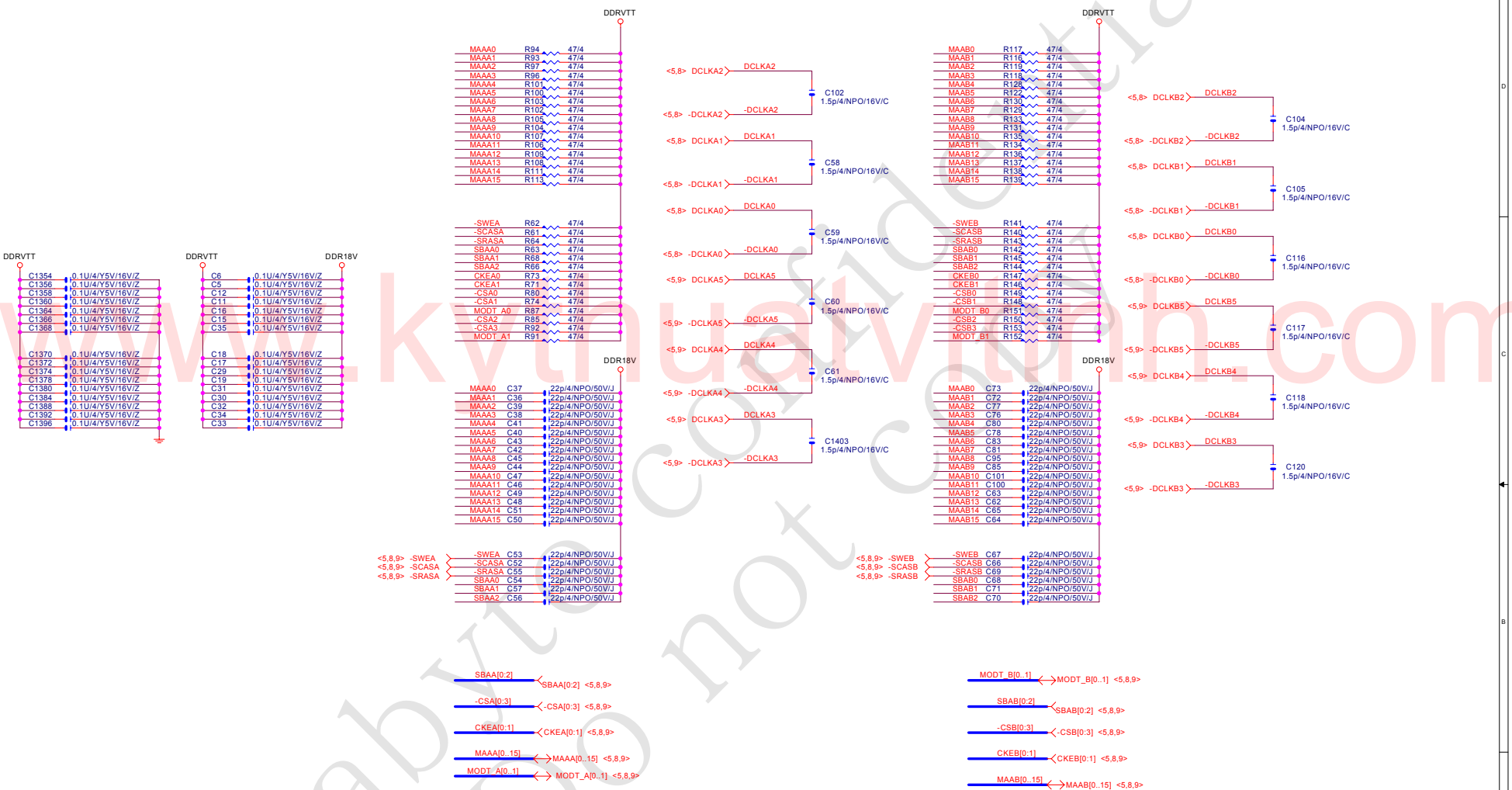

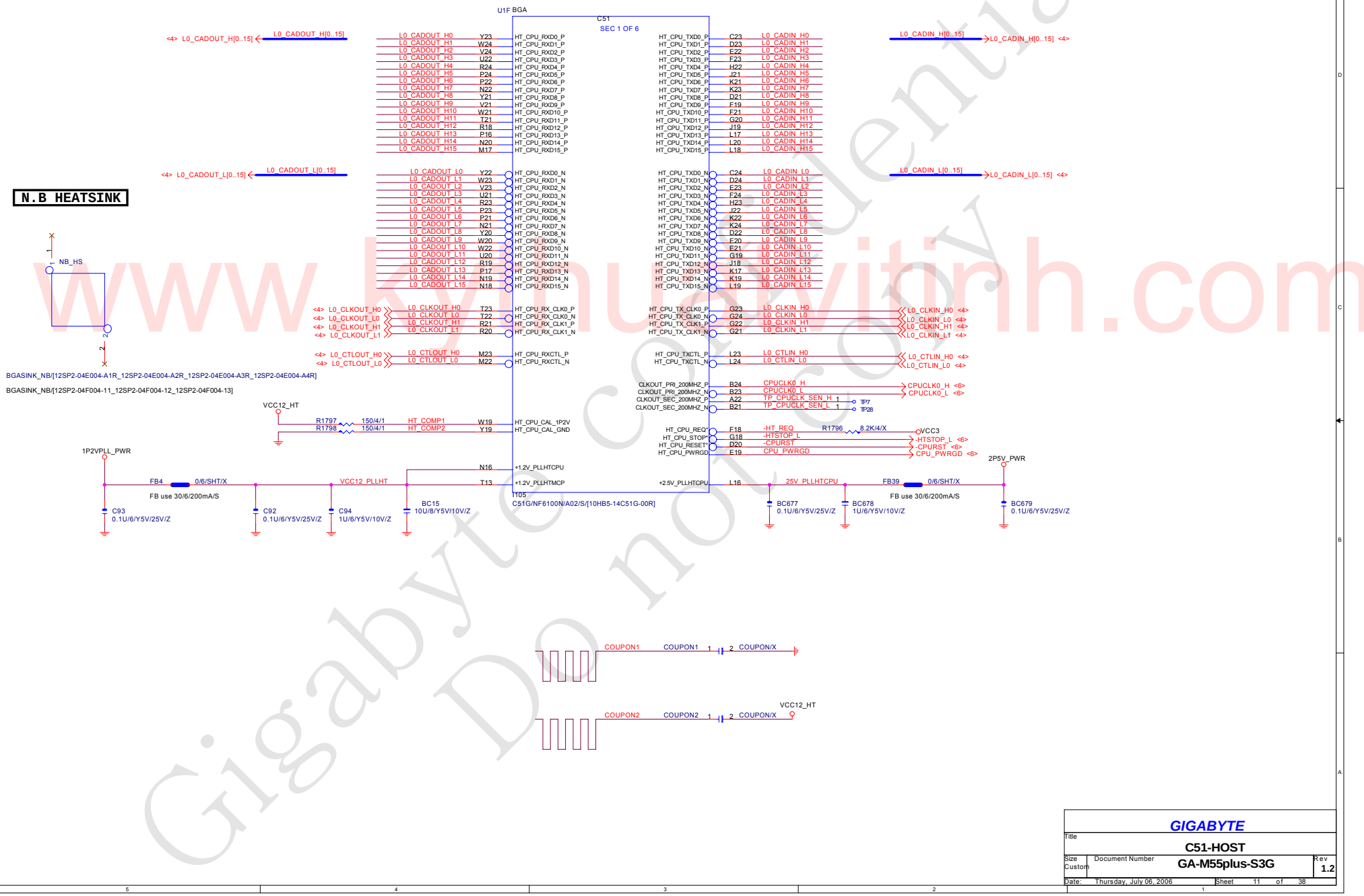

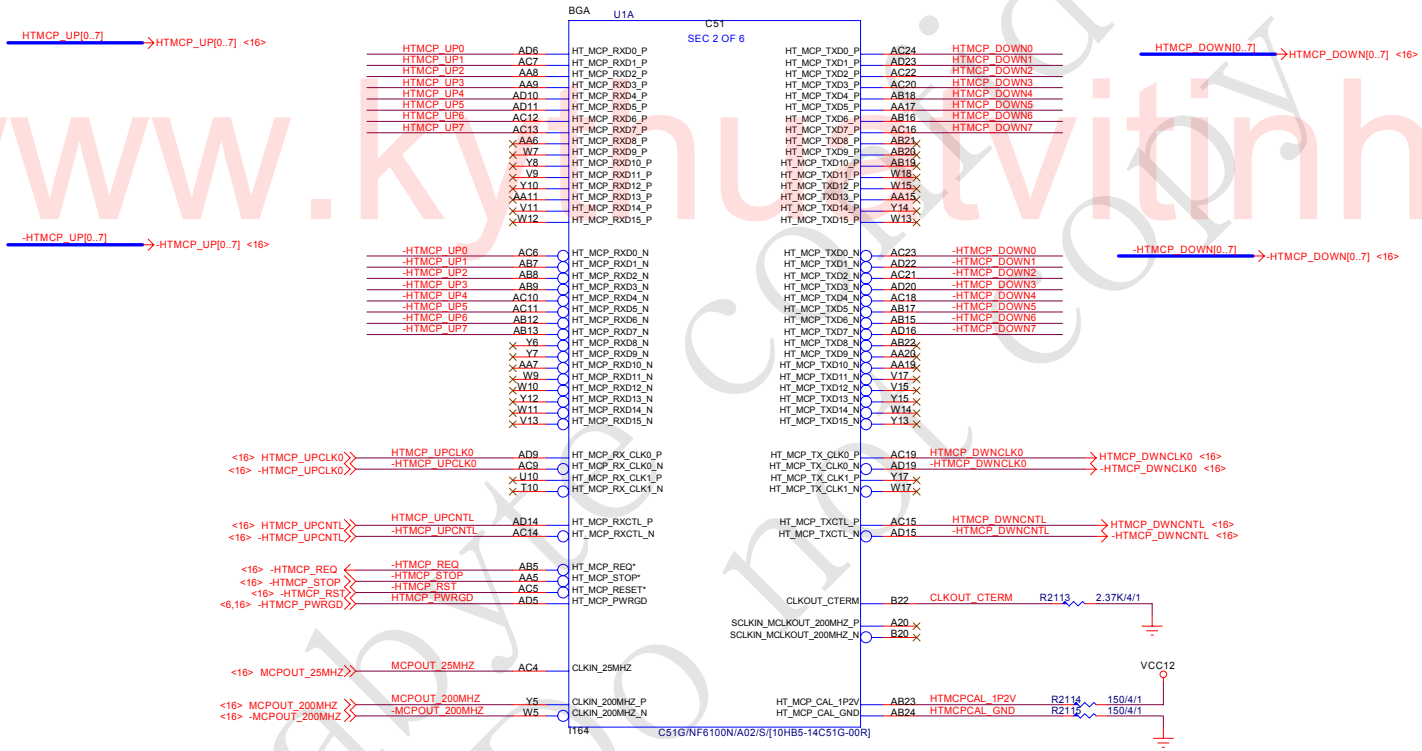

GIGABYTE		
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Size: Custom	Document Number: GA-M55plus-S3G	Rev: 1.2
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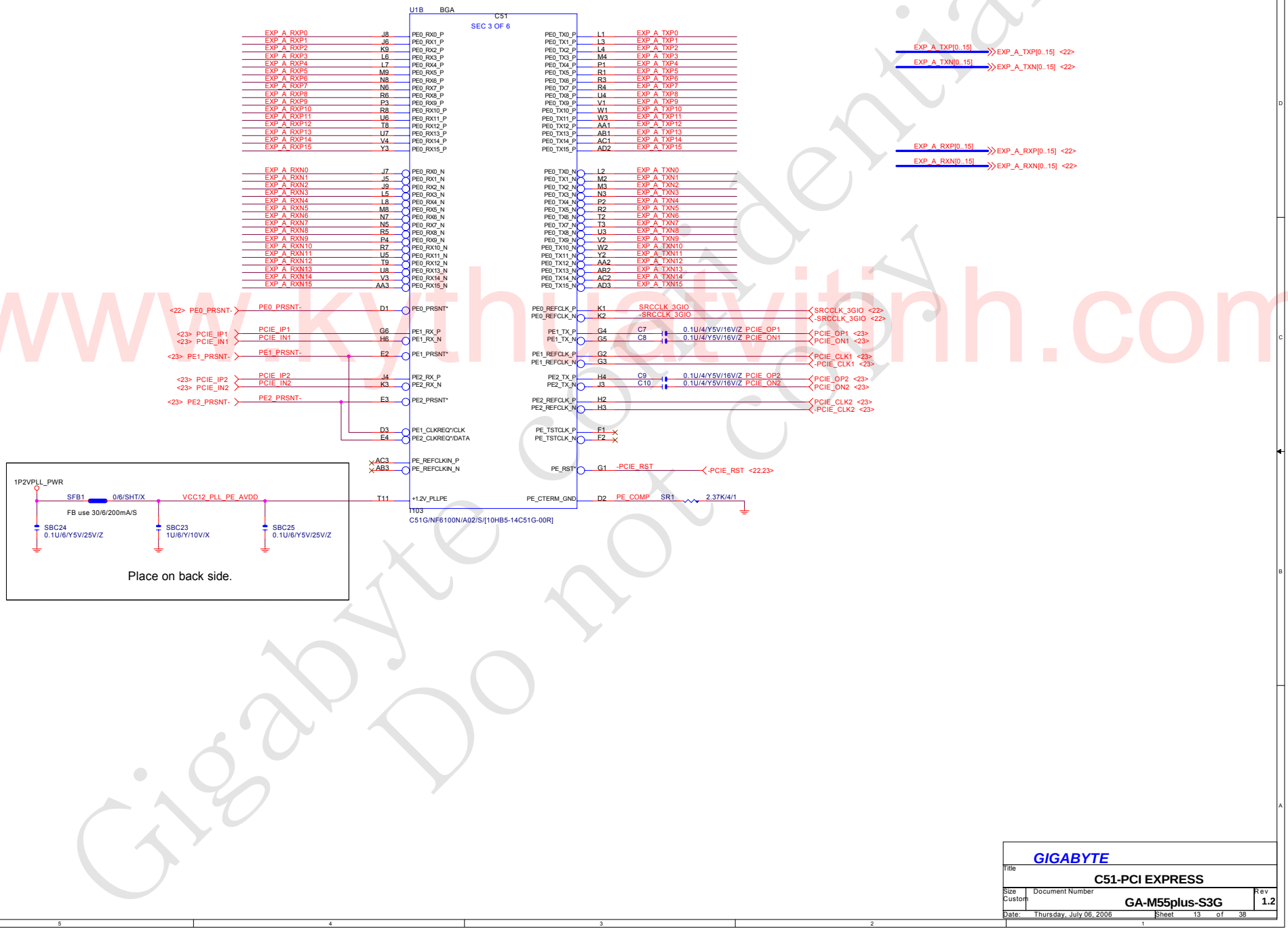

GIGABYTE

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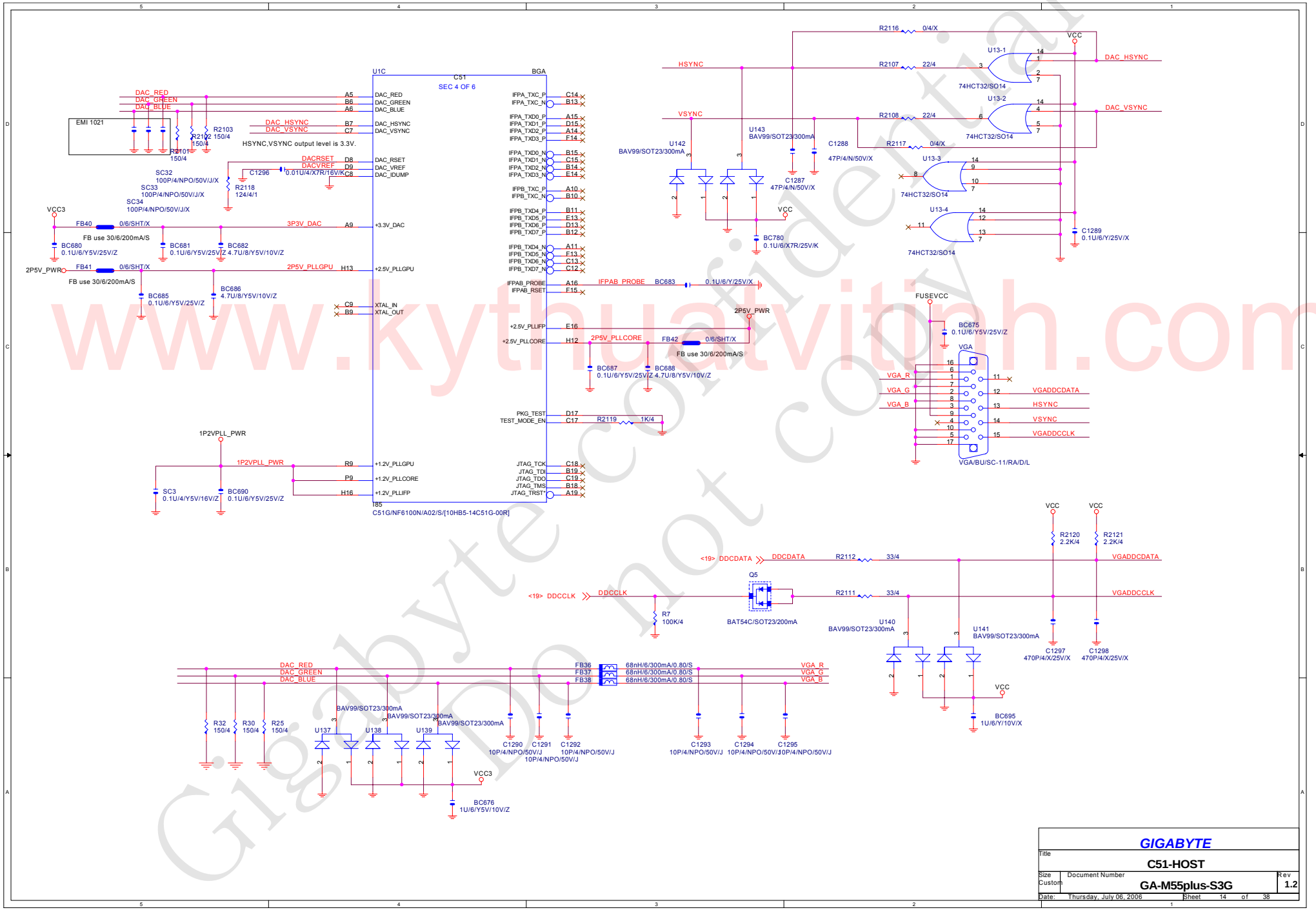
Size: Custom	Document Number: GA-M55plus-S3G	Rev: 1.2
Date: Thursday, July 06, 2006	Sheet 13 of 38	



GIGABYTE		
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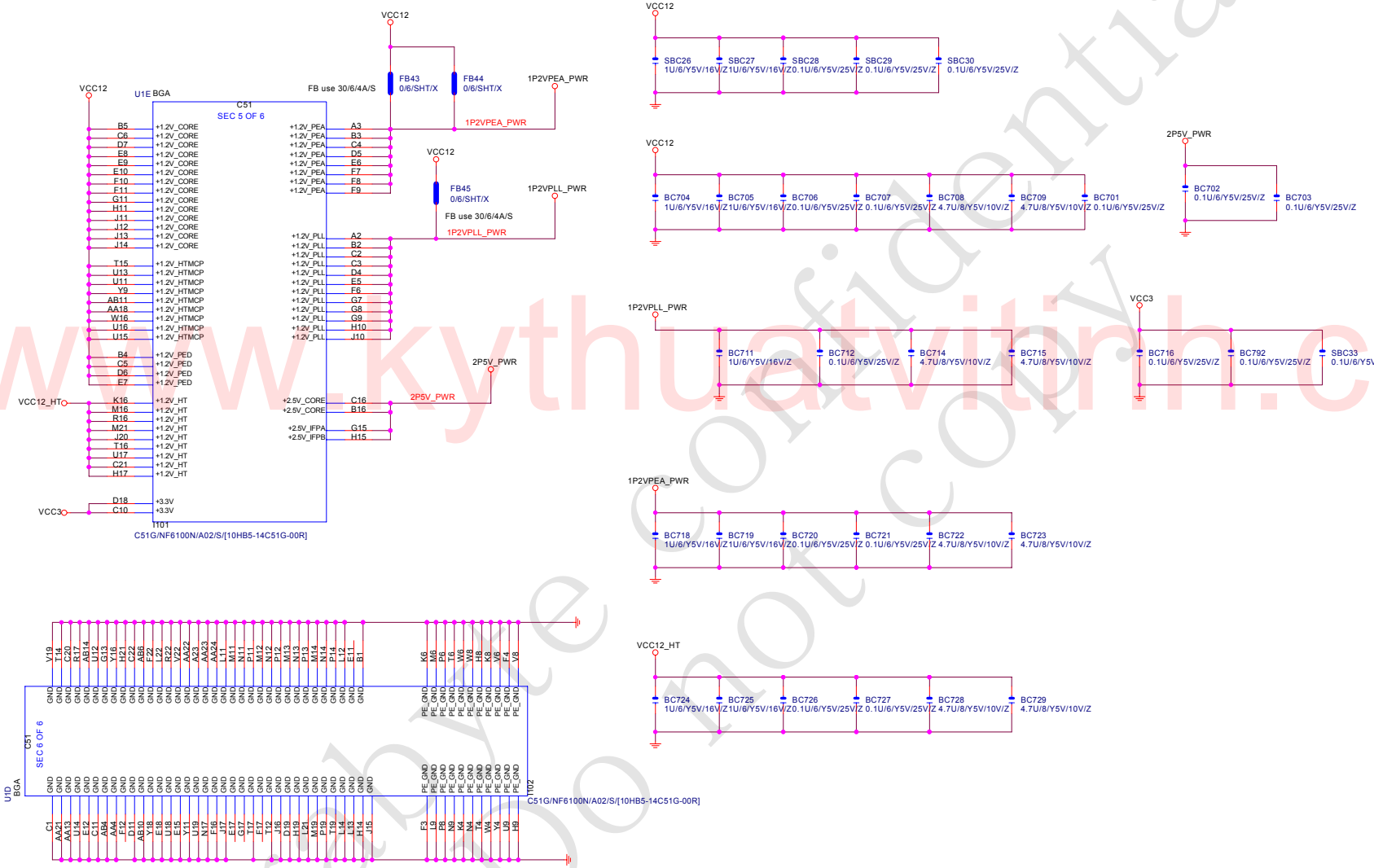
Size: Custom	Document Number: GA-M55plus-S3G	Rev: 1.2
Date: Thursday, July 06, 2006	Sheet 14 of 38	



F12, J17, G17, T17, E11 single pin only.

GIGABYTE		
Title: C51-PWR/GND		
Size: Custom	Document Number: GA-M55plus-S3G	Rev: 1.2
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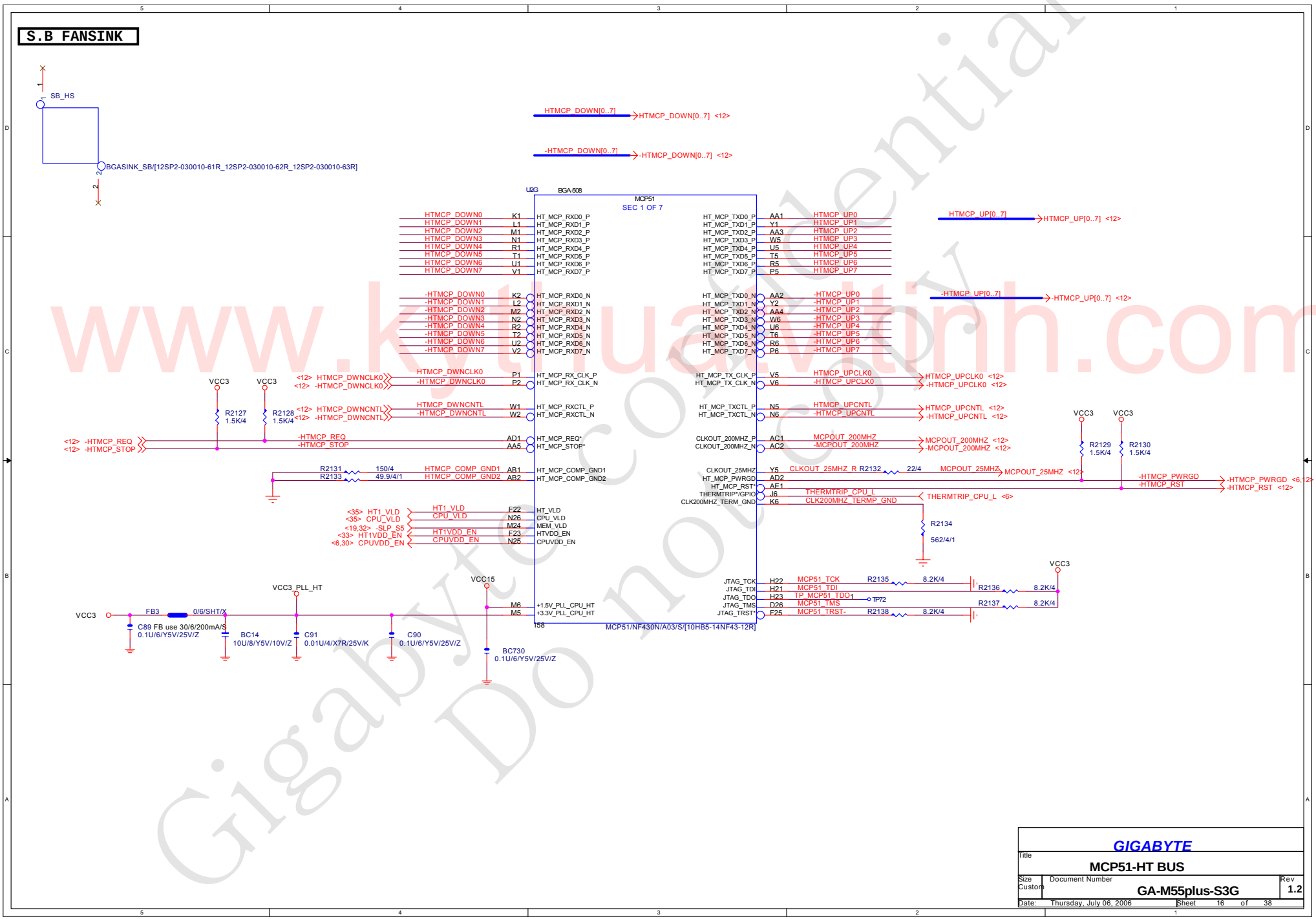

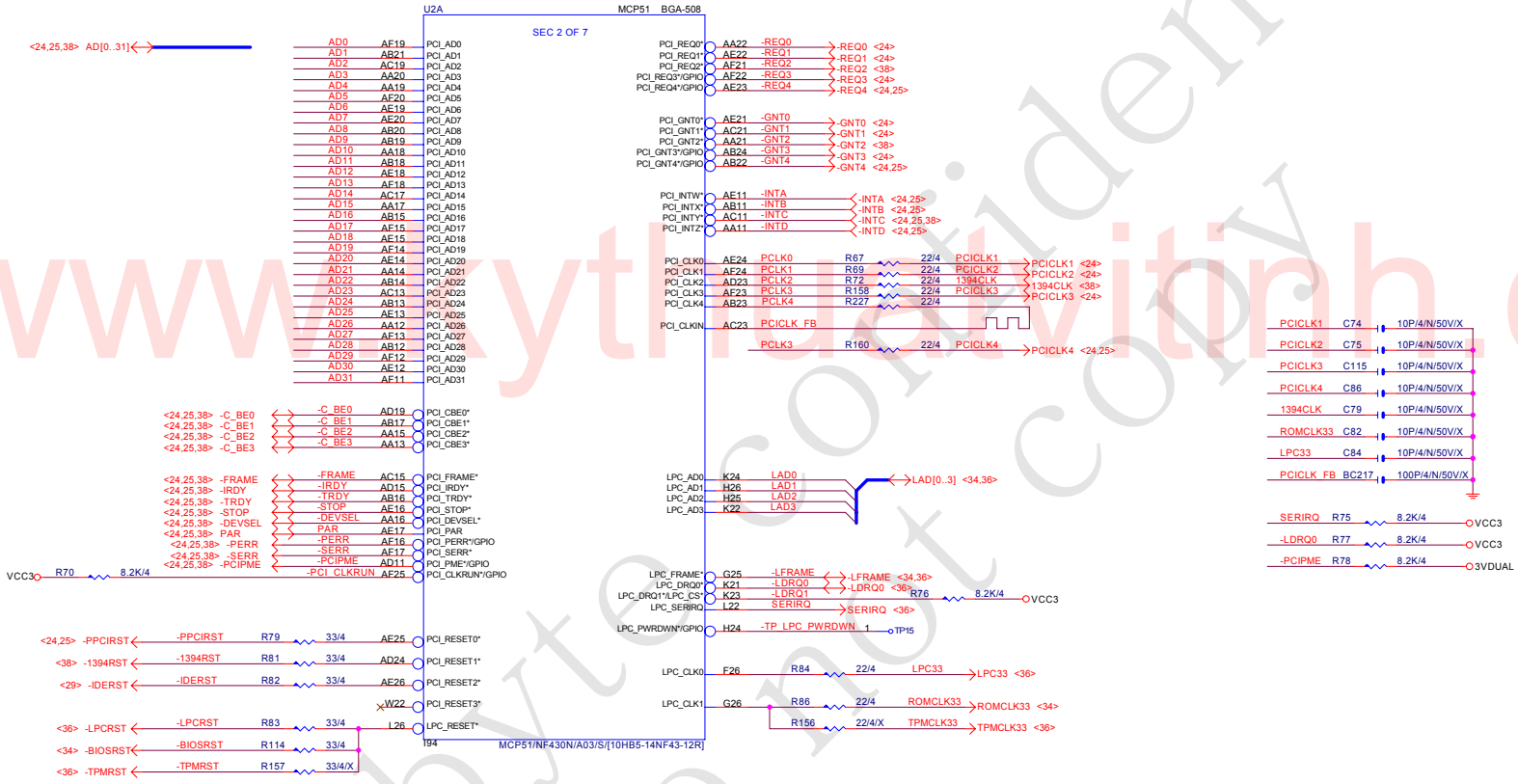

GIGABYTE

Title: MCP51-PCI BUS

Size: Custom | Document Number: GA-M55plus-S3G | Rev: 1.2

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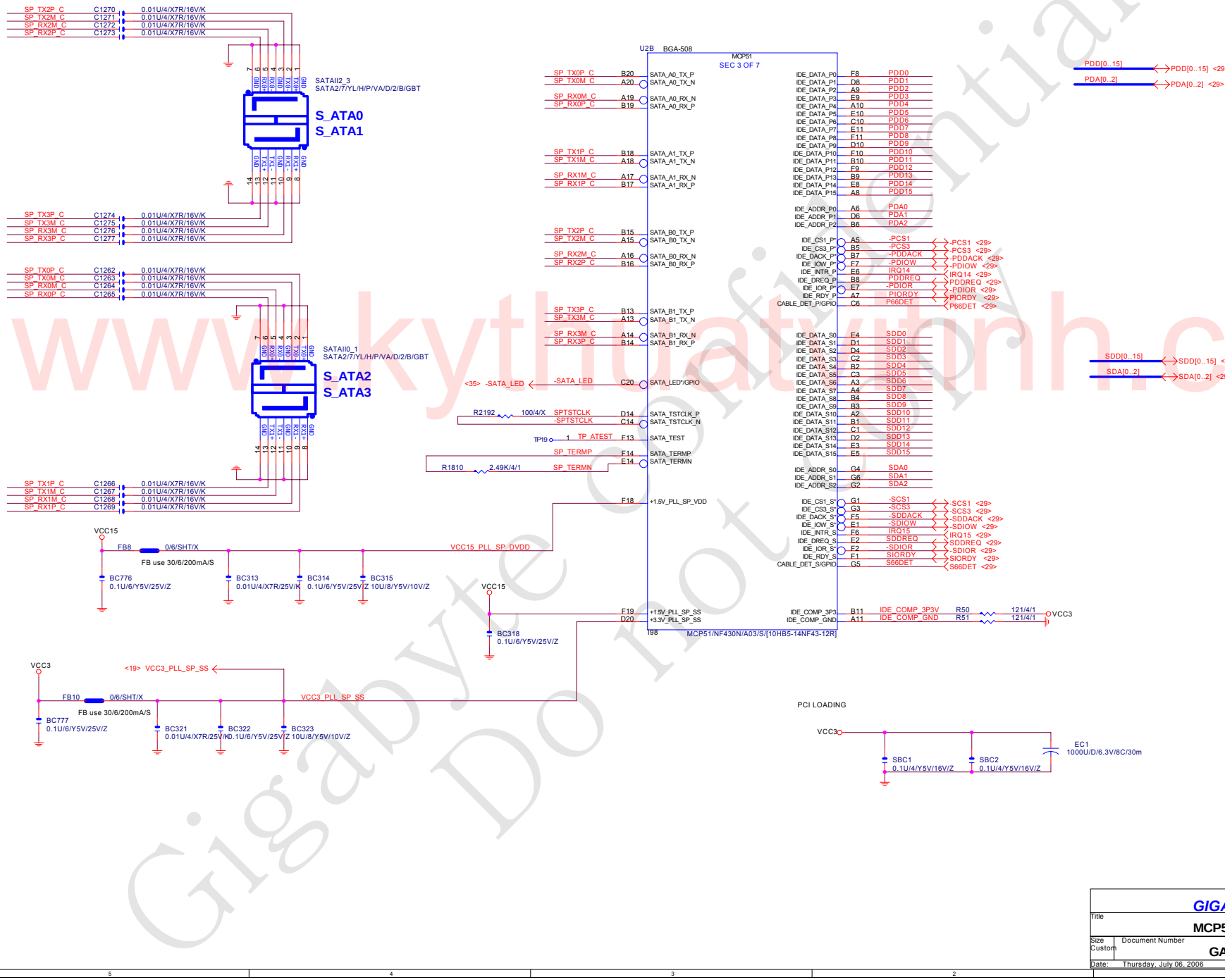

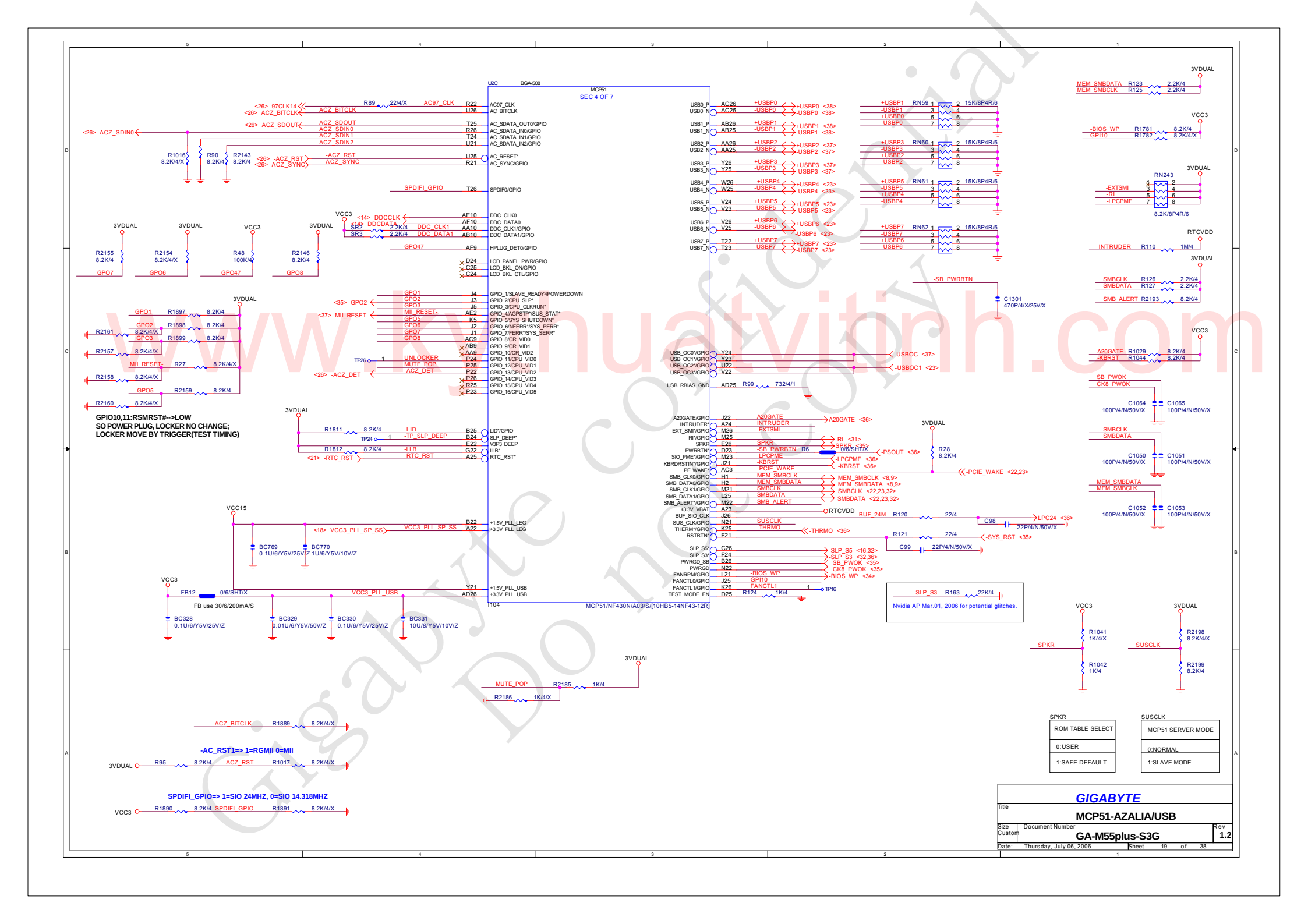

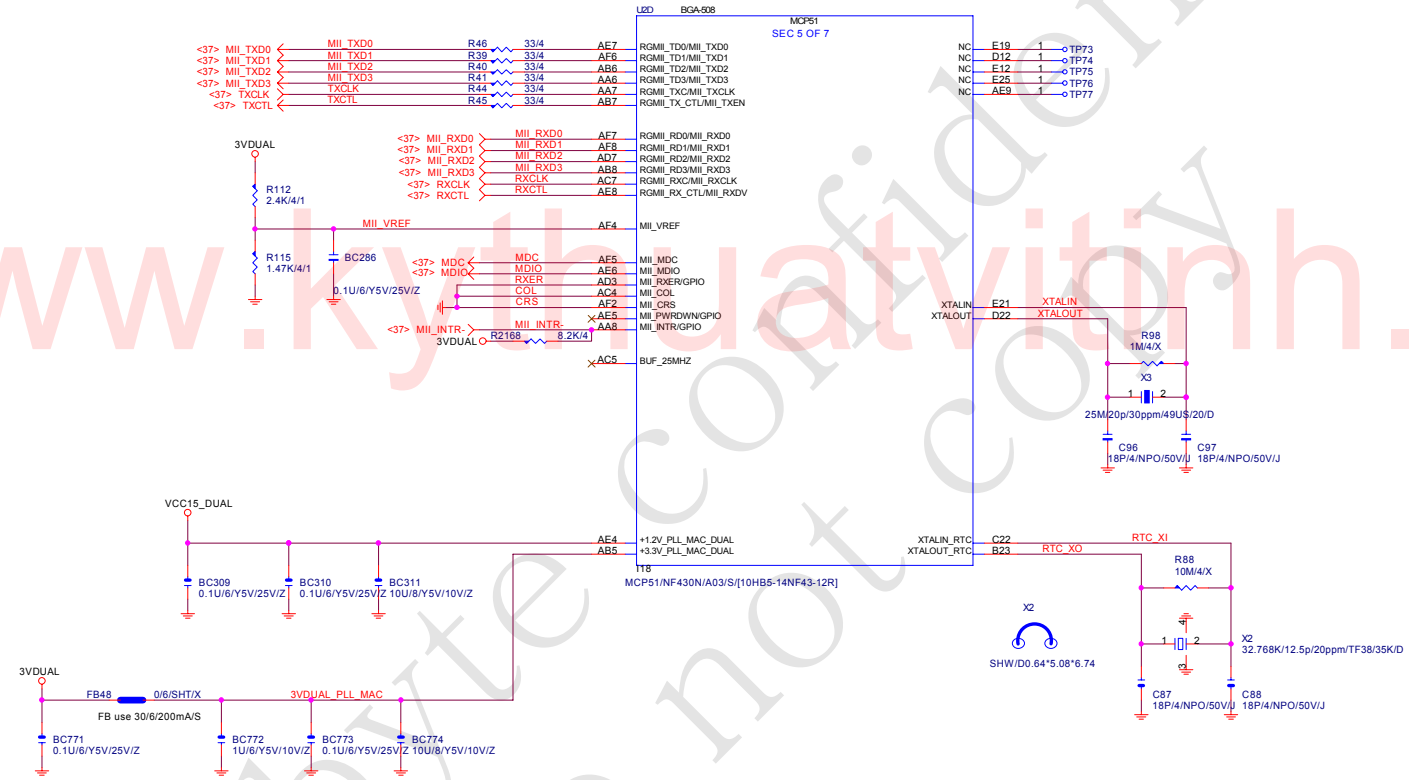

GIGABYTE

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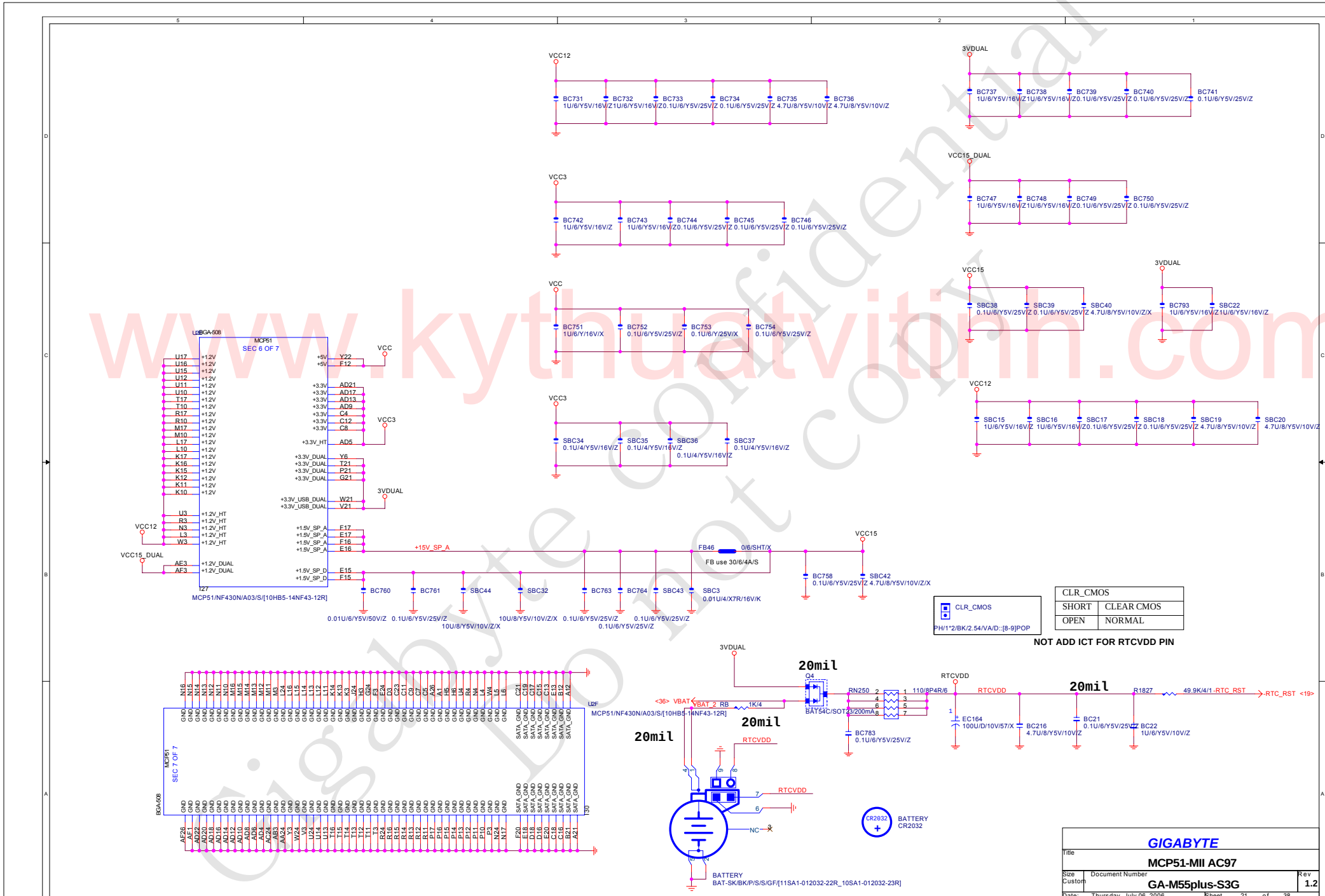

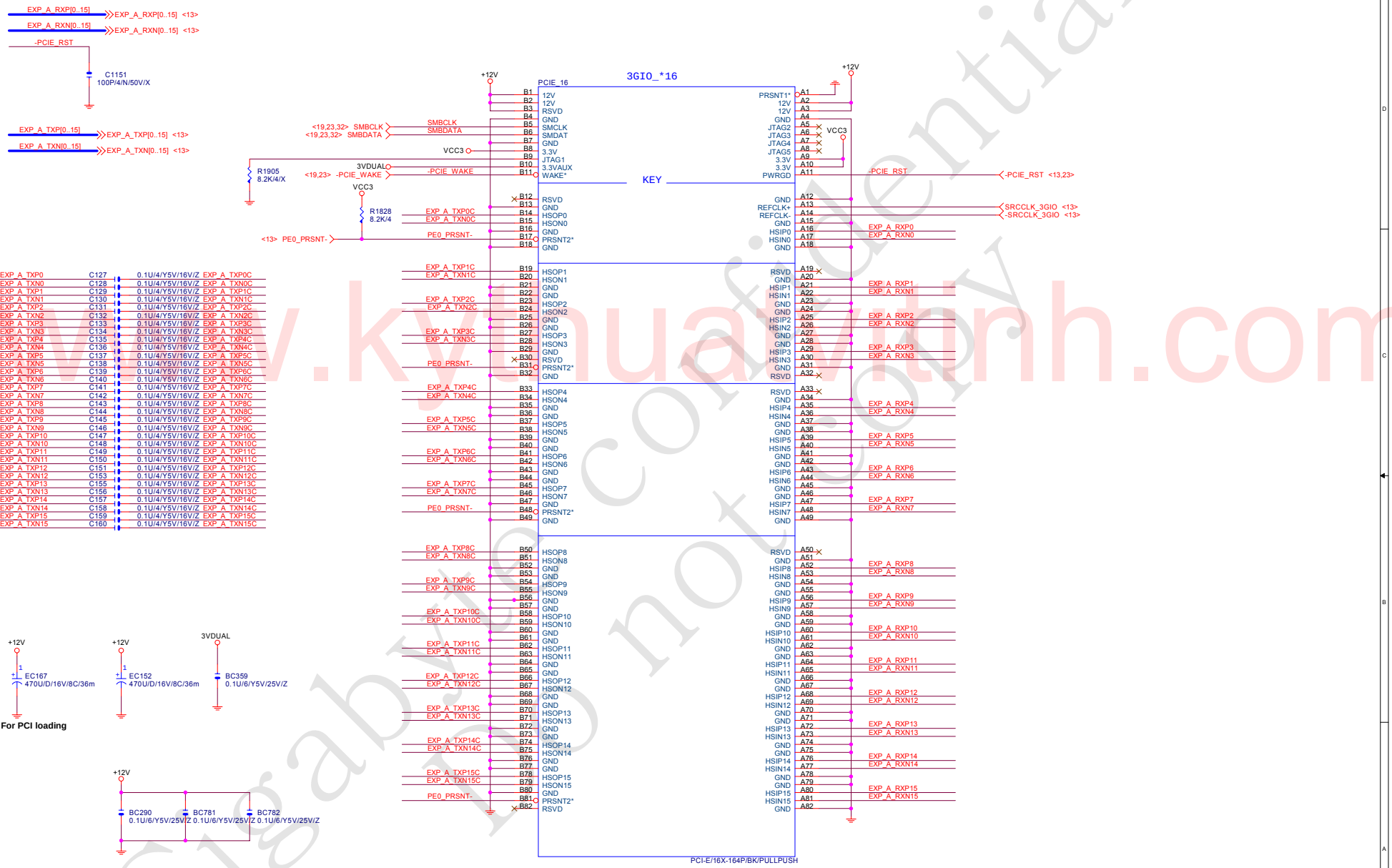

GIGABYTE		
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Size: Custom	Document Number: GA-M55plus-S3G	Rev: 1.2
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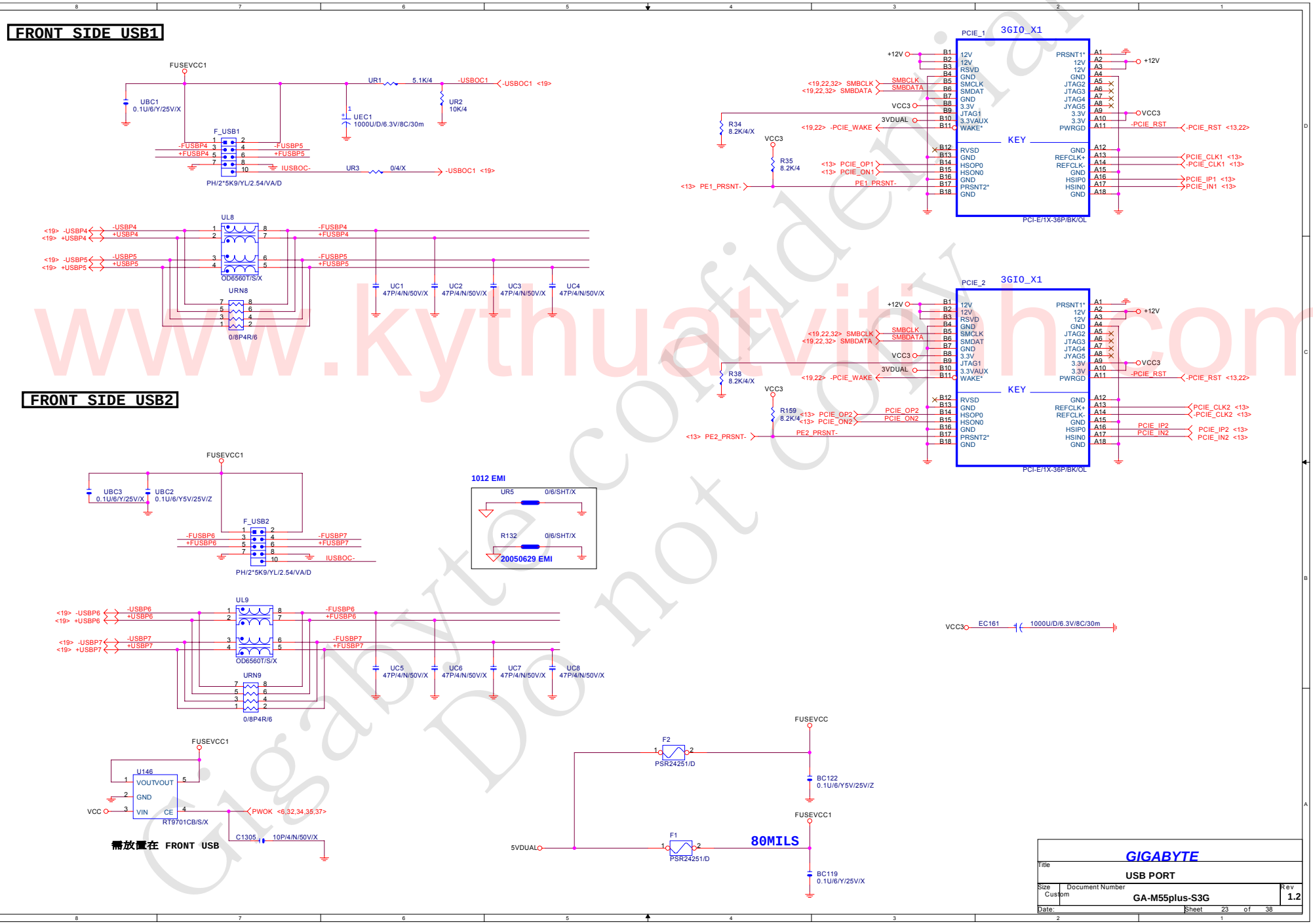

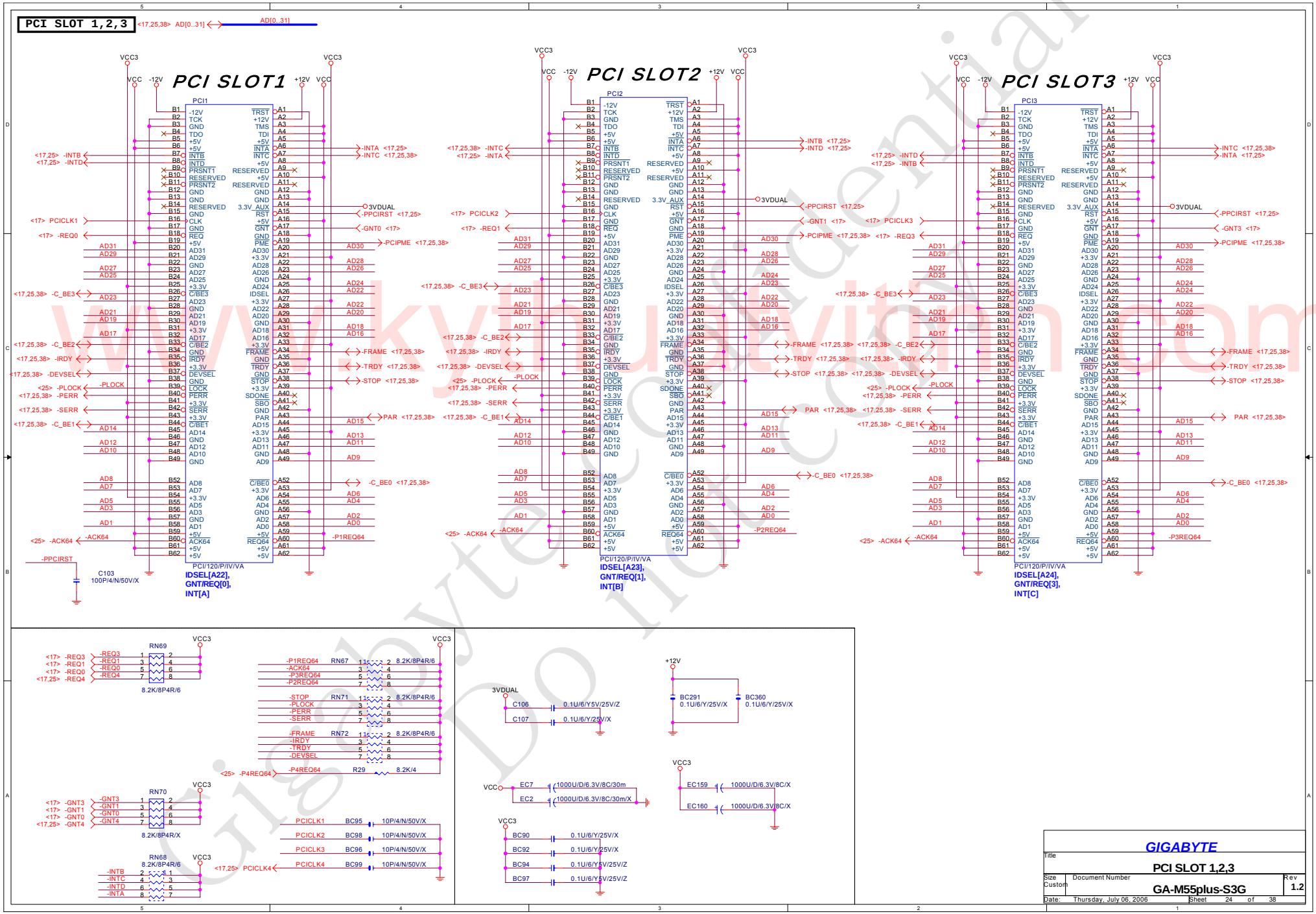

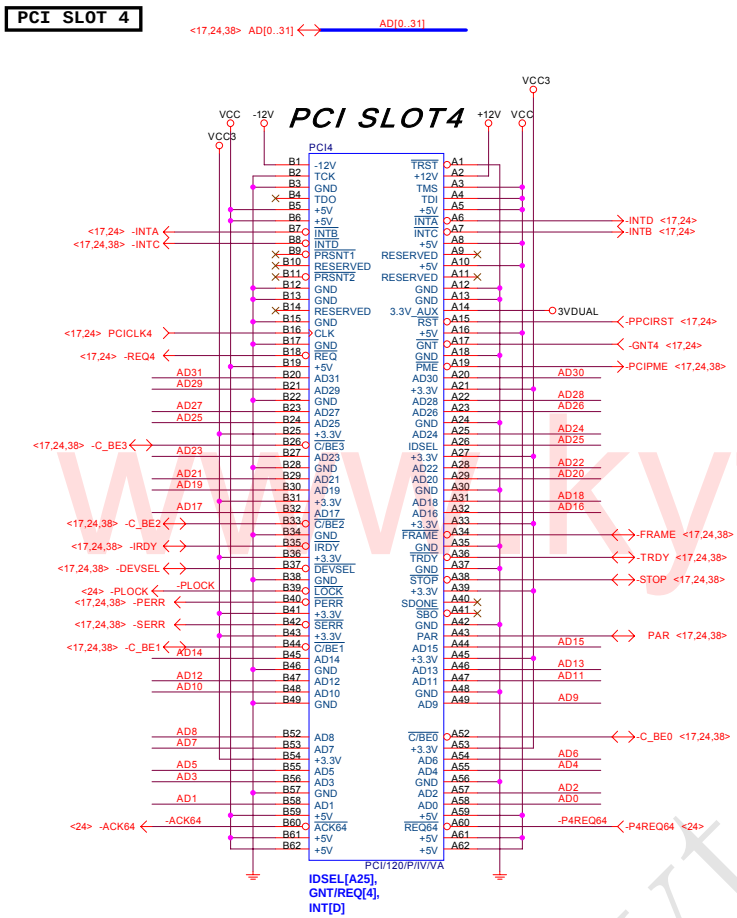

GIGABYTE		
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Size: Custom	Document Number: GA-M55plus-S3G	Rev: 1.2
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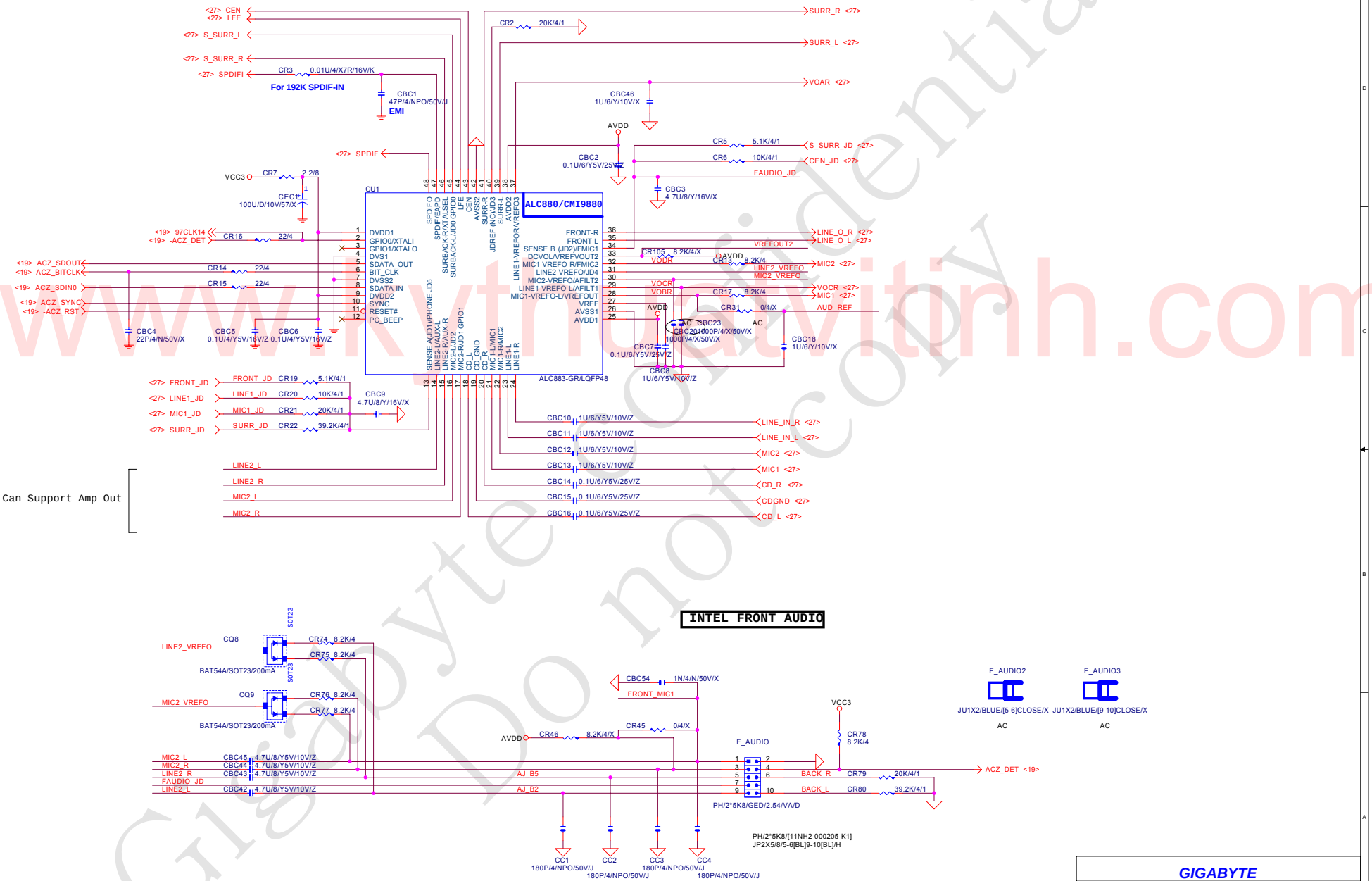
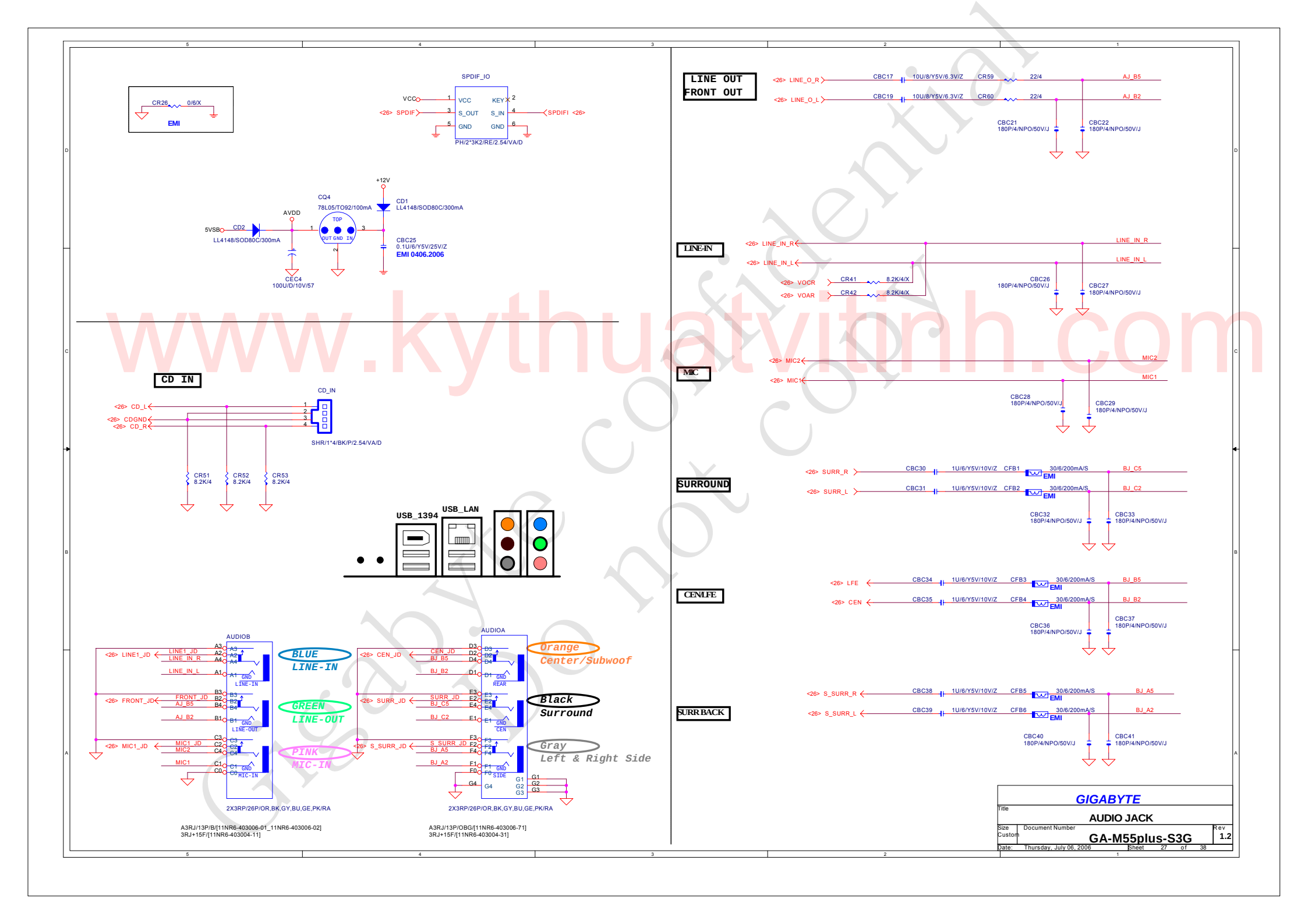
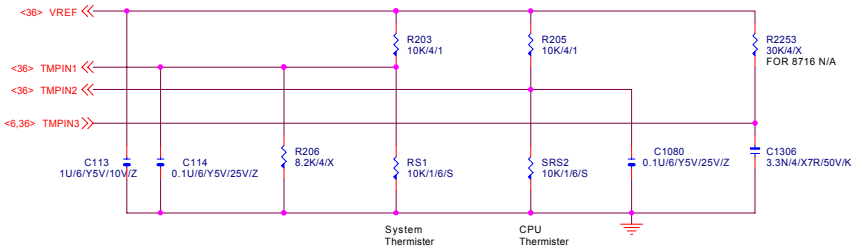
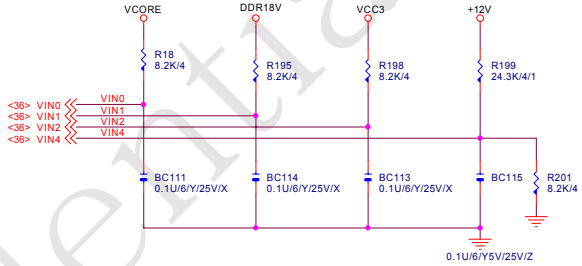


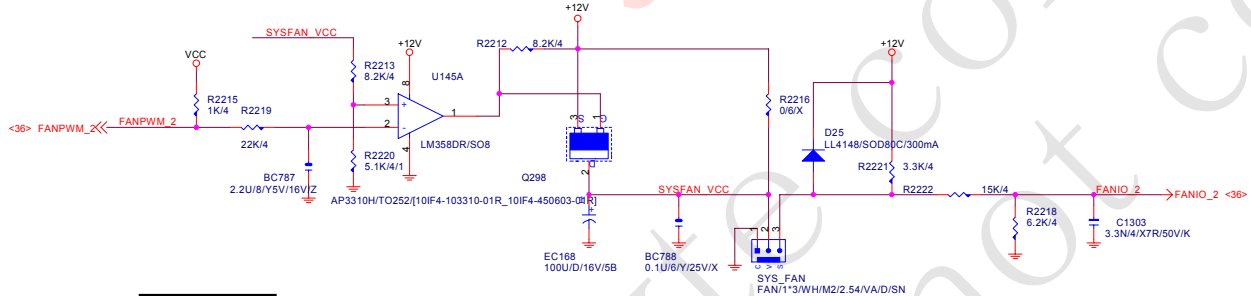


Hardware Monitor circuits

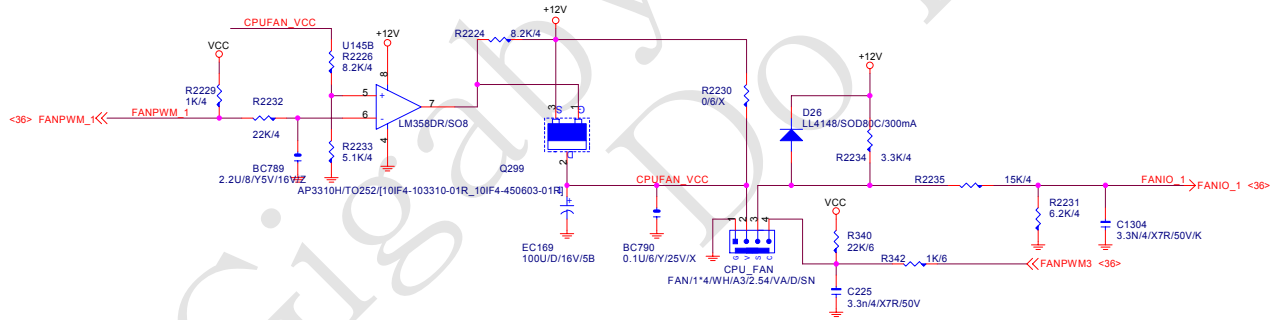




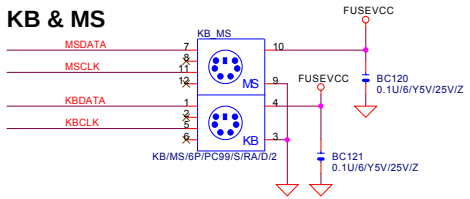
SYSTEM FAN

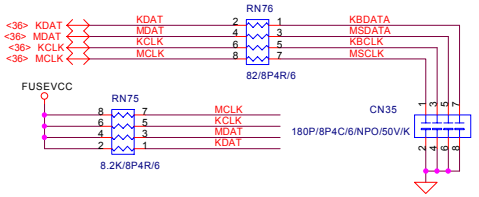


CPU FAN



KB & MS





GIGABYTE		
Title: FAN/HWMO		
Size: Custom	Document Number: GA-M55plus-S3G	Rev: 1.2
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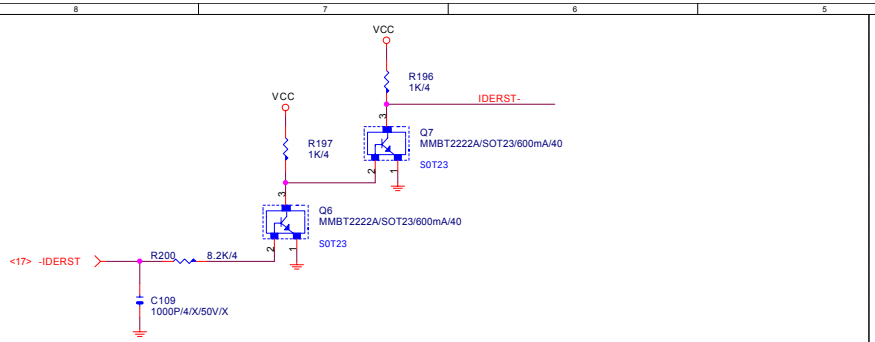
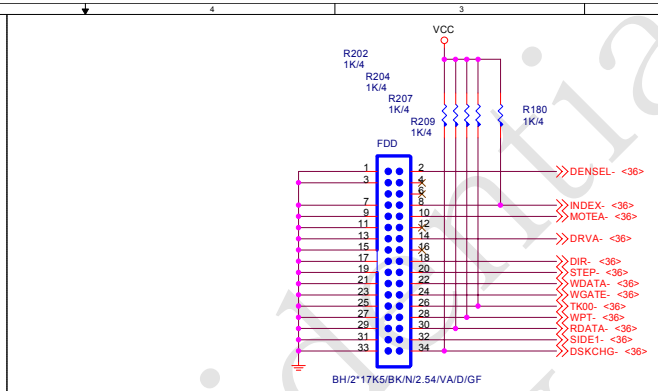
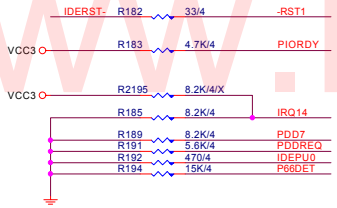
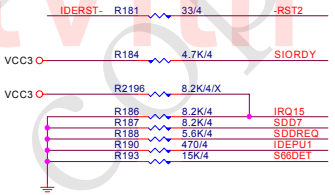
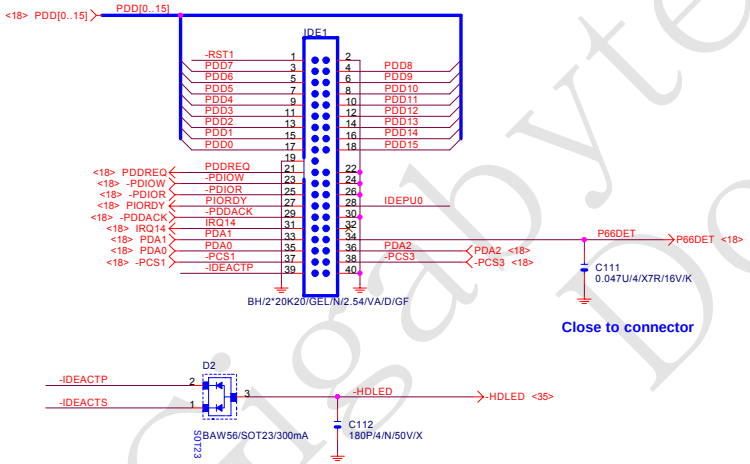




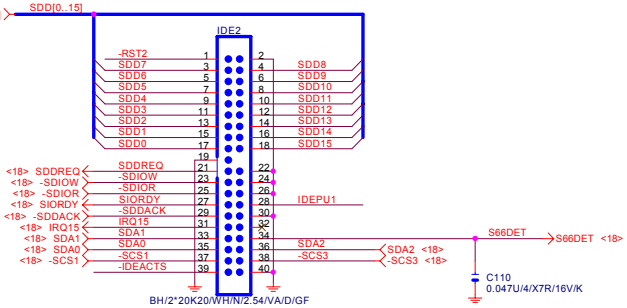




PRIMARY IDE CONNECTOR



SECONDARY IDE CONNECTOR



GIGABYTE		
Title	IDE CONNECTOR	
Size: Custom	Document Number: GA-M55plus-S3G	Rev: 1.2
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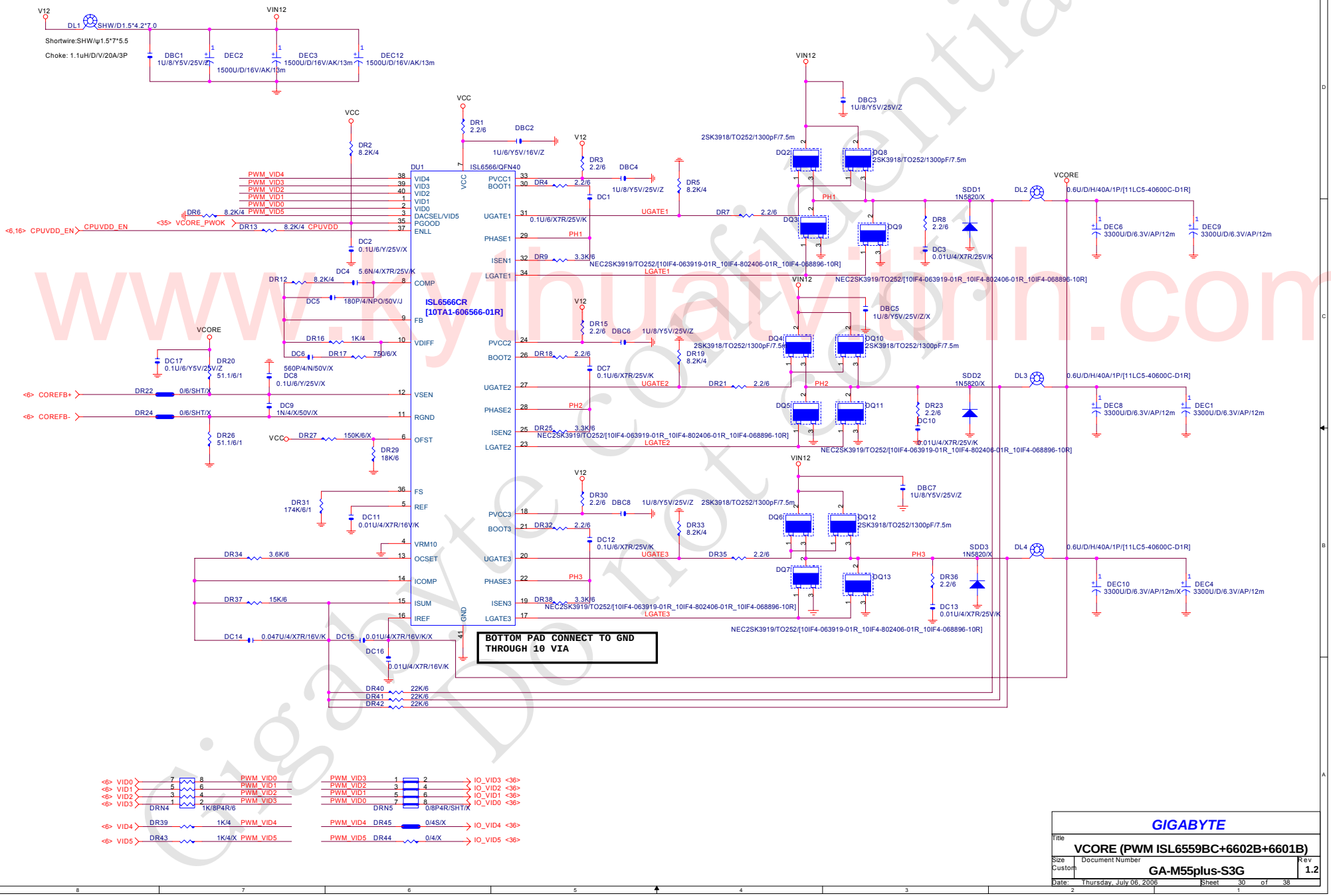

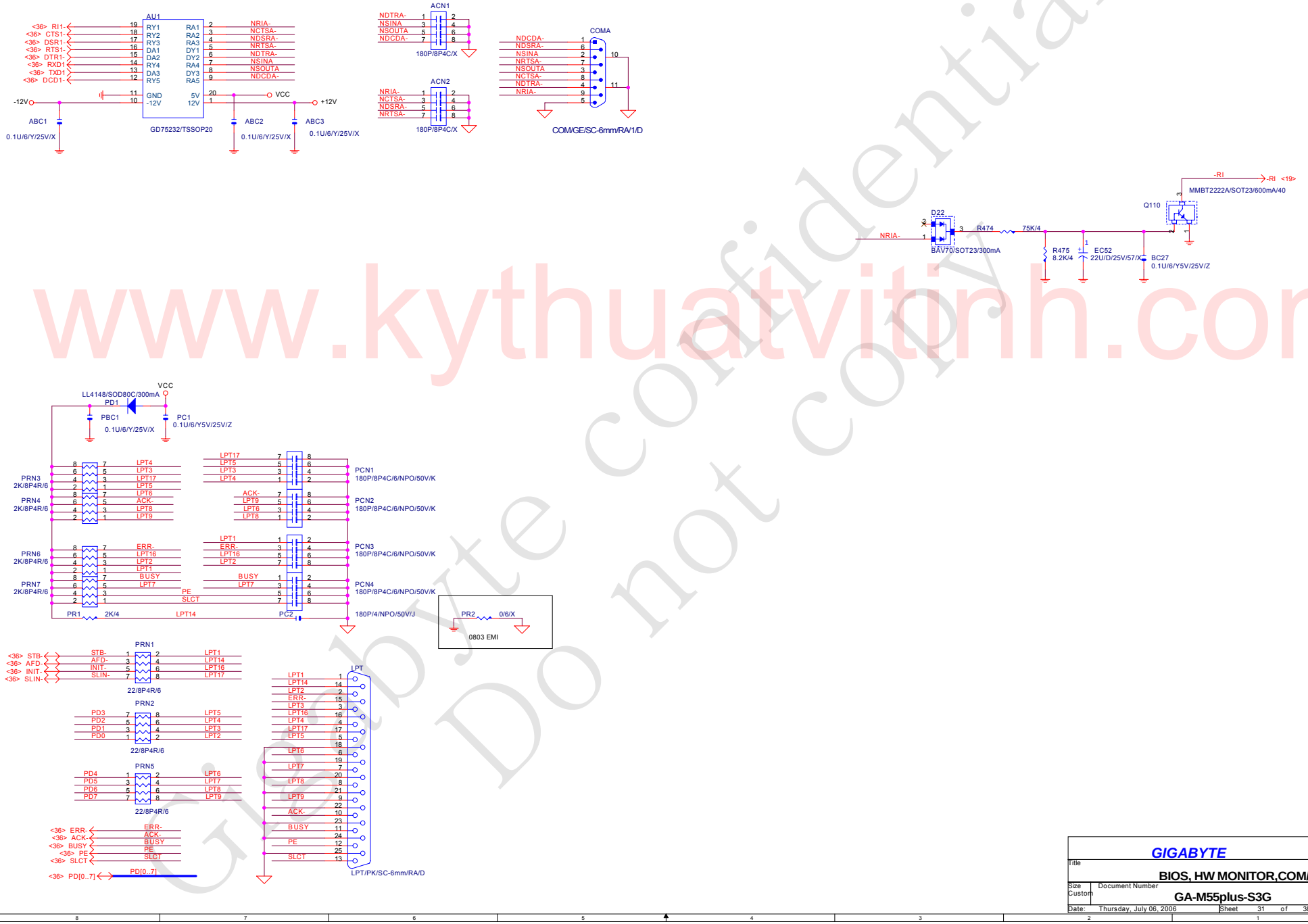

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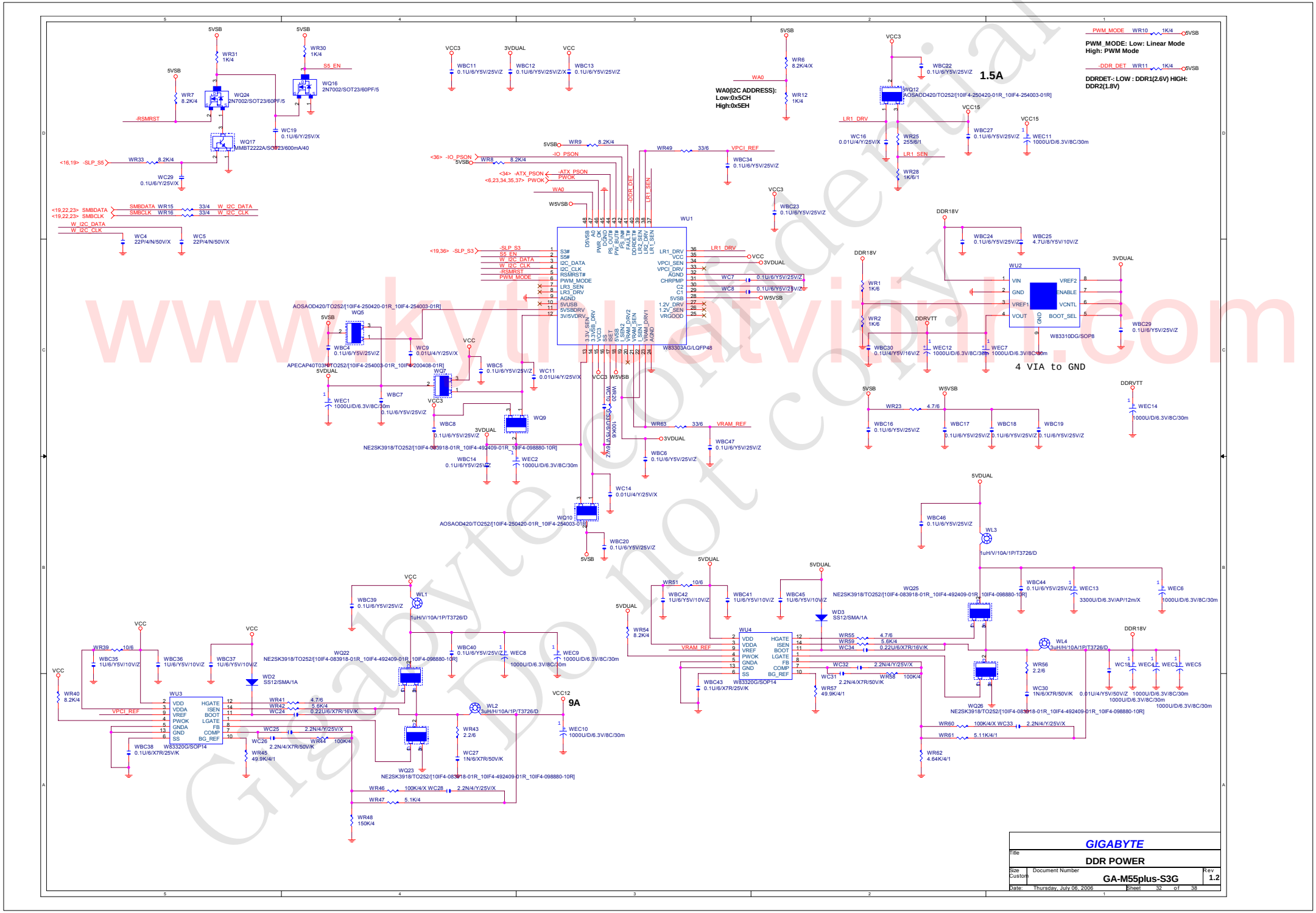

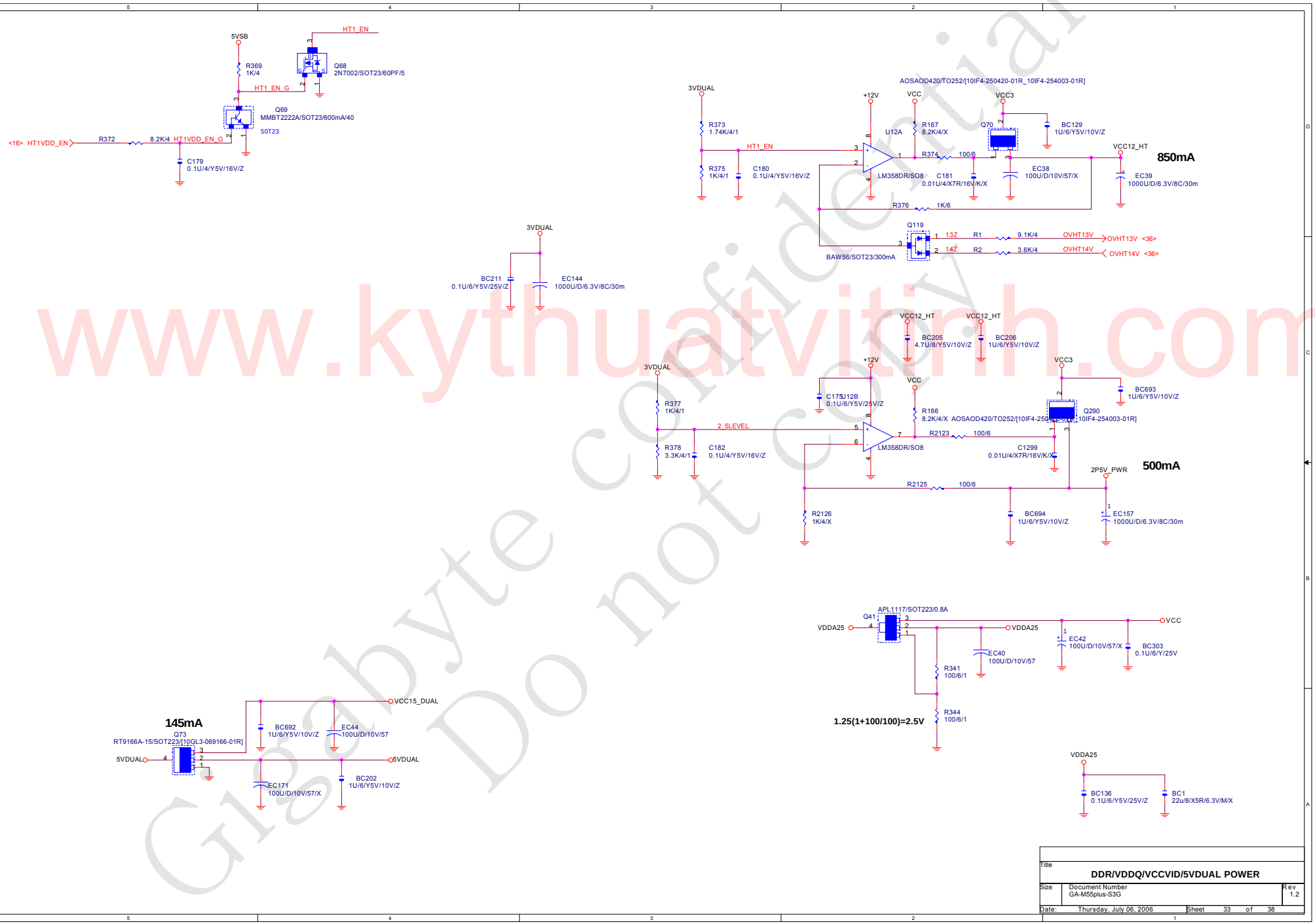

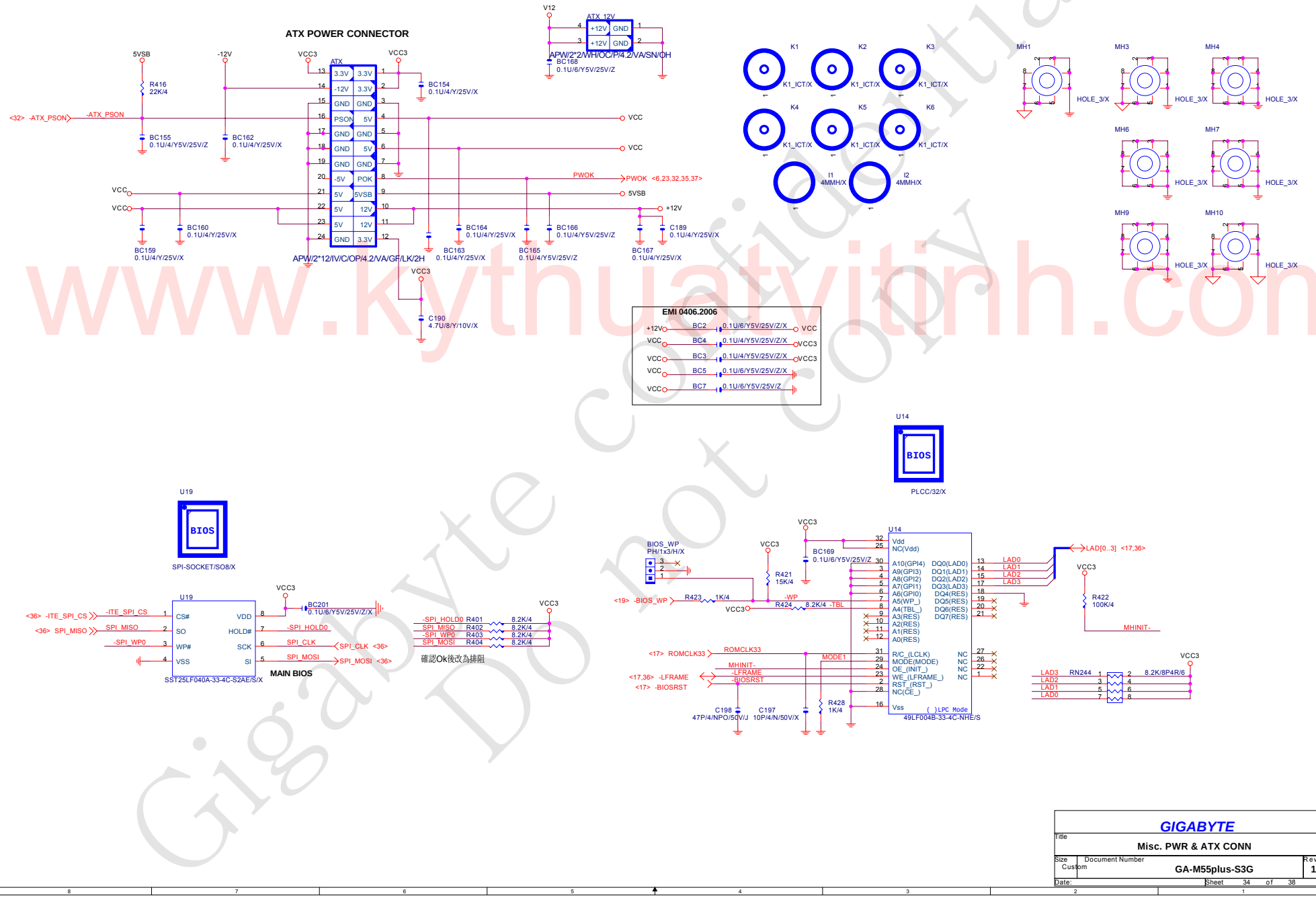

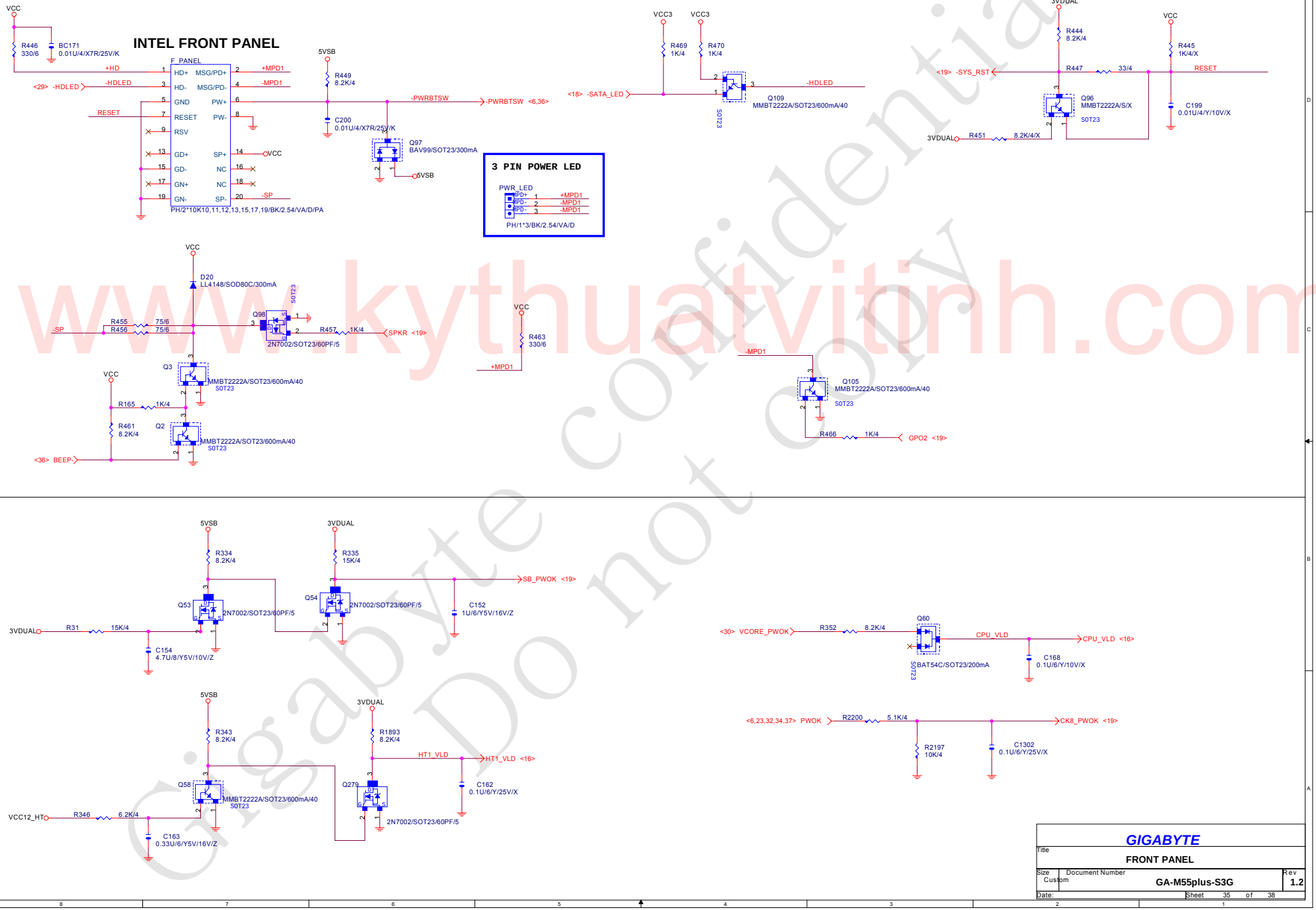

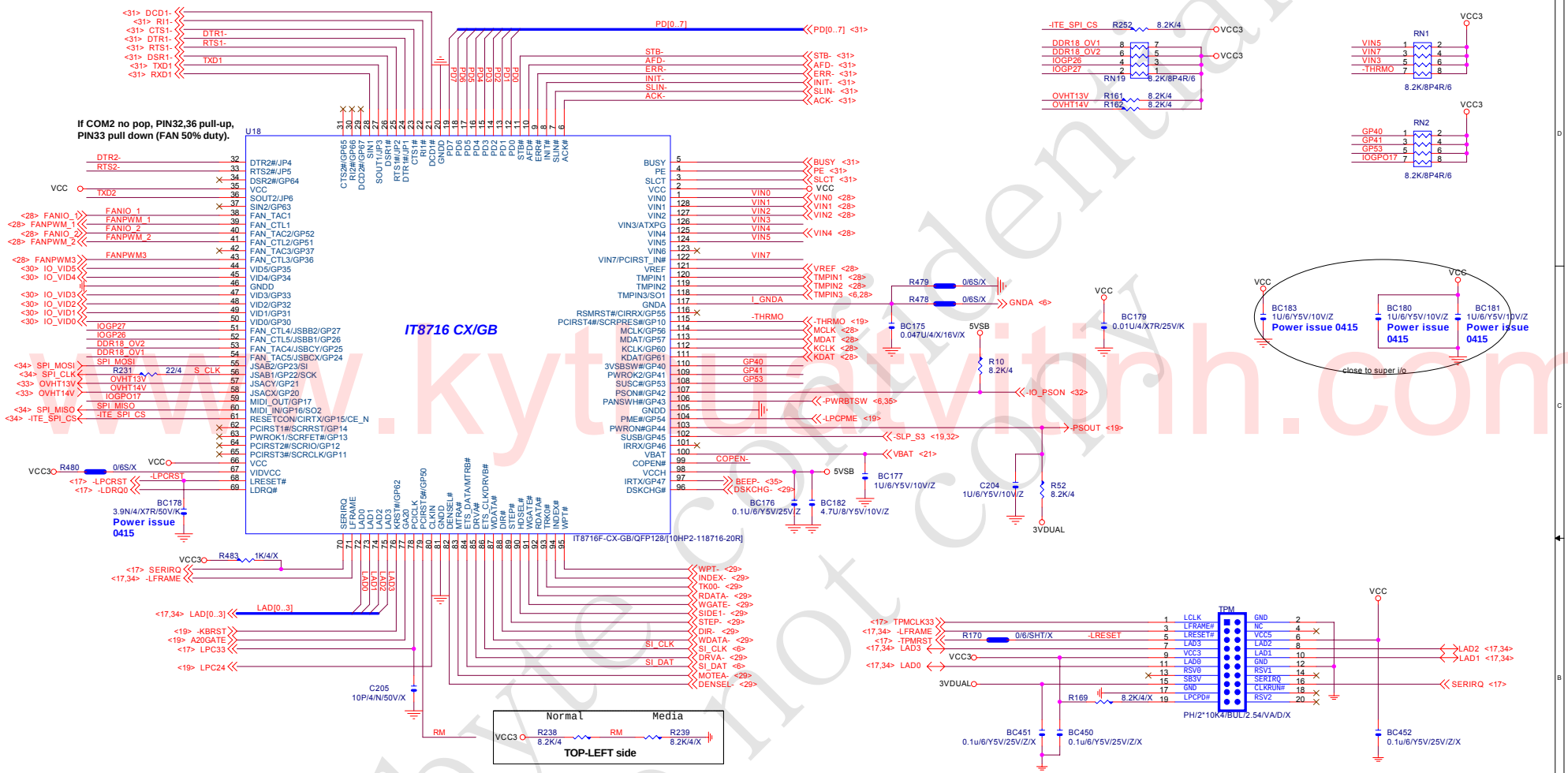

If COM2 no pop, PIN32,36 pull-up, PIN33 pull down (FAN 50% duty).

ON: EN SPI

75232 internal P.U.

IT8716 H/W Strap

If 75232 is connected, please use 680 ohm to be the pull down resistor value. Since powered by 12V, 75232 has a very strong internal pull-up. It is hard to be pulled low. (Please see specification for detail of power on strapping setting)

	Default	Description
DTR1-	0	En SPI Flash
RTS1-	1	Midi-in/SO2 as SPI SO pin
TXD1	--	
DTR2-	0	PCIRSTx# are push-pull
RTS2-	0	Power-on FAN Duty=50%
TXD2	0	VID threshold is 0.8V/0.4V

CPU Thermal Diode Differential Pair

Other Signal — 15mil — TMPIN3+ — 10mil — TMPIN3- — 12mil — 10mil — Other Signal — 15mil

Power On Strapping Options

	Symbol	value	Description
JP1	Flashseg1_EN	1	Disabled.
		0	Flash I/F Address Segment 1 (FFF8_0000h~FFFF_FFFFh, 000E_0000h~000F_FFFFh) is enabled
JP2	SerFlh_SO_SEL	1	FLH_SO2 is selected as the Serial Flash I/F SO pin.
		0	FLH_SO1 is selected as the Serial Flash I/F SO pin.
JP3	CHIP_SEL	--	Chip selection in configuration.
JP4	BUF_SEL	1	The output buffers of PCIRST1#, PCIRST2#, PCIRST3#, PCIRST4# and PCIRST5# are enhanced open-drain. It drives high about 10~20 ns when the signal transits from low to high, and then Hi-Z.
		0	The output buffers are push-pull.
JP5	FAN_CTL_SEL	1	The default value of EC Index 15h / 16h / 17h is 00h
		0	The default value of EC Index 15h / 16h / 17h is 40h
JP6	VID_ISEL	1	The threshold voltage of VID is 2.0 / 0.8V
		0	The threshold voltage of VID is 0.8 / 0.4V

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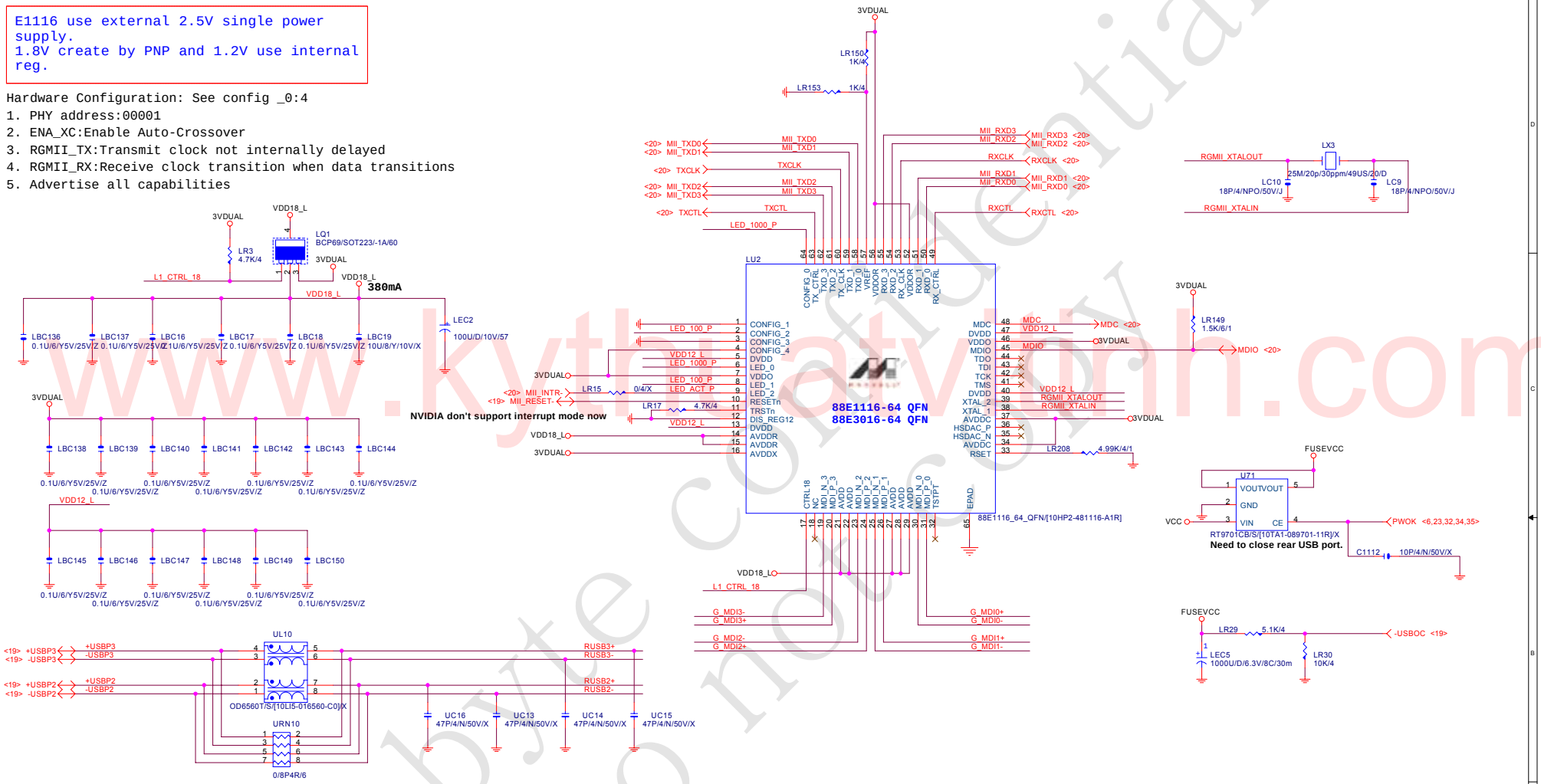
E1116 use external 2.5V single power supply.
1.8V create by PNP and 1.2V use internal reg.

Hardware Configuration: See config _0:4
1. PHY address:00001
2. ENA_XC:Enable Auto-Crossover
3. RGMII_TX:Transmit clock not internally delayed
4. RGMII_RX:Receive clock transition when data transitions
5. Advertise all capabilities



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