GIGABYTE GA-M55S-S3 Schematics

Revision: 2.02

SHEET	TITLE
01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	PROCESSOR HT INTERFACE
05	PROCESSOR DDR INTERFACE
06	PROCESSOR DDR INTERFACE
07	PROCESSOR CONTROL & DEBUG
08	DIMM A0,B0
09	DIMM A1,B1
10	DIMM TERMINATION
11	MCP55 HT/CLK
12	MCP55 PCIE X16
13	MCP55 PCIE X8 X1
14	MCP55 PCI
15	MCP55 SATA , IDE
16	MCP55 AUDIO , USB , MISC
17	MCP55 DUAL RGMII
18	MCP55 PWR/GND
19	MCP55 DECOUPLING
20	PCI EXPRESS X16 SLOT
21	PCI EXPRESS X8 SLOT
22	PCI EXPRESS X1 SLOT1,2,3
23	PCI 1,2 SLOT
24	CODEC 883
25	AUDIO JACK, L_OUT, F_AUDIO

SHEET	TITLE
26	IDE1/FDD
27	KB_MS/FUSEVCC
28	VCORE POWER
29	VCC12_HT,VCCA25,VCC15,PLL POWER
30	PWR SEQUENCE PWR
31	DDR18 , DDRVTT , 5VDUAL
32	ATX POWER CONNCTOR,VCC15
33	DUAL BIOS
34	FRONT PANEL
35	ITE 8716F (GB)
36	FAN/HW MONITOR
37	F_USB1/F_USB2/F_USB3 CONNECTOR
38	COMA , LPT , TPM , R_USB
39	MARVELL 1116 RGMII PHY -A
40	TI TSB43AB23 1394A
41	
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44	

GIGABYTE CORP.

Title: BLOCK DIAGRAM

Size: Custom | Document Number: GA-M55S-S3 | Rev: 2.02

Date: 星期二, 一月 09, 2007 | Sheet 1 of 41

Model Name: GA-M55S-S3

Version: 2.02

Component value change history

Date	Change Item	Reason
REV2.0 2006/03/27	First release.	
2006/11/16	REV2.01	
	change codec from ALC883 to ALC888	
	remove CR10,R42	
	change CR32 from 220ohm to 2.2ohm CR45 change to 470pf CBC17,CBC18,CBC21 change to 0.1uf	
	add R41 DEC12 ,DEC13 ,DEC14 ,DEC15 ,DEC16 ,DEC17	
	add U29,C341,DC14,SDC1	
	add input choke cover DL1	
	L1,L4 update library footprint "CHOKE2U-20A-SQ-1"機構改腳距	
	DL1 input choke "cover"	
	remove DRN3,DRN4,DRN5,DRN6,LR16,LR31,TP21	
2006/11/22	REV2.01	
	remove CR48 CR49 CQ4	
2006/12/05	REV2.01	
	remove C66 R85	
2006/12/12	REV2.02	
	DL1,DL2,DL3,DL4 footprint-->CHOCK06U-40A_1PDL-2	
	L1,L4, footprint-->CHOCK2U-20A_SQ-2	
	L2,L3, footprint-->CHOCK08U-15A_1P-1	
2006/12/26	REV2.02	
	CBC50,CBC51,CBC52,CBC53:4.7u/8/X5R/25V/K-->4.7u/8/X5R/10V/K	
2007/01/09	REV2.02	
	CBC50,CBC51,CBC52,CBC53:4.7u/8/X5R/10V/K-->4.7u/8/X5R/6.3V/K	

Circuit or PCB layout change for next version

Date	Change Item	Reason
REV0.1 2006/03/27		
2006/11/17	REV2.01	
	remove U6,U10,BC72 ,R131, R97,C236,C65,R367	
	remove NET-EOMCLK33	

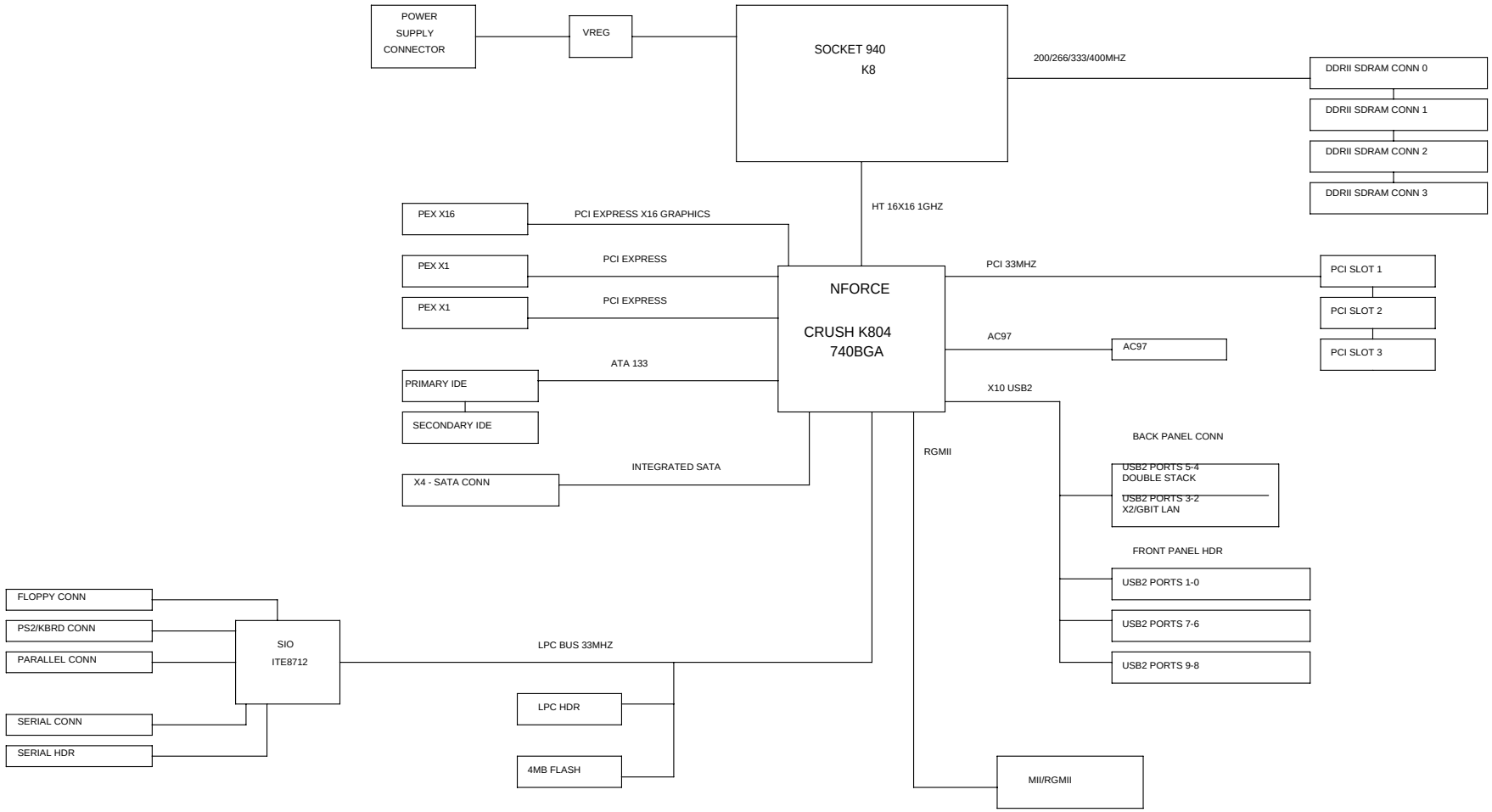
GIGABYTE CORP.

Title: BOM & PCB MODIFY HISTORY

Size: Custom | Document Number: GA-M55S-S3 | Rev: 2.02

Date: 星期二, 一月 09, 2007 | Sheet 2 of 41

BLOCK DIAGRAM



GIGABYTE CORP.		
Title: BLOCK DIAGRAM		
Size: Custom	Document Number: GA-M55S-S3	Rev: 2.02
Date: 星期二, 一月 09, 2007	Sheet 3 of 41	

L0_CADIN_L[0..15] L0_CADIN_L[0..15] [11]
L0_CADIN_H[0..15] L0_CADIN_H[0..15] [11]
L0_CLKIN_L[0..1] L0_CLKIN_L[0..1] [11]
L0_CLKIN_H[0..1] L0_CLKIN_H[0..1] [11]
L0_CADOUT_L[0..15] L0_CADOUT_L[0..15] [11]
L0_CADOUT_H[0..15] L0_CADOUT_H[0..15] [11]
L0_CLKOUT_L[0..1] L0_CLKOUT_L[0..1] [11]
L0_CLKOUT_H[0..1] L0_CLKOUT_H[0..1] [11]

CPU_VDDA_RUN = VDDA25
CPU_VDDIO_SUS = DDR18V
CPU_VTT_SUS = DDRVTT

CPU_VDD_RUN = VCORE

VLDT_RUN = VCC12_HT

VLDT_A = VCC12_HT
VLDT_B = HT12B

U12A

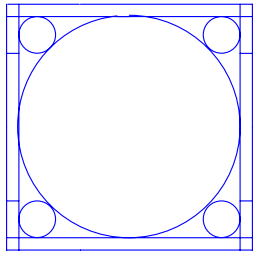
HYPERTRANSPORT

L0_CLKIN_H1	N6	L0_CLKIN_H(1)	L0_CLKOUT_H(1)	AD5	L0_CLKOUT_H1
L0_CLKIN_L1	P6	L0_CLKIN_L(1)	L0_CLKOUT_L(1)	AD4	L0_CLKOUT_L1
L0_CLKIN_H0	N3	L0_CLKIN_H(0)	L0_CLKOUT_H(0)	AD1	L0_CLKOUT_H0
L0_CLKIN_L0	N2	L0_CLKIN_L(0)	L0_CLKOUT_L(0)	AC1	L0_CLKOUT_L0
VCC12_HT — R156 49.9/6/1	V4	L0_CTLIN_H(1)	L0_CTLOUT_H(1)	Y6	1 — TP3
GND — R163 49.9/6/1	V5	L0_CTLIN_L(1)	L0_CTLOUT_L(1)	W6	1 — TP4
[11] L0_CTLIN_H0	U1	L0_CTLIN_H(0)	L0_CTLOUT_H(0)	W2	L0_CTLOUT_H0 [11]
[11] L0_CTLIN_L0	V1	L0_CTLIN_L(0)	L0_CTLOUT_L(0)	W3	L0_CTLOUT_L0 [11]
L0_CADIN_H15	U6	L0_CADIN_H(15)	L0_CADOUT_H(15)	Y5	L0_CADOUT_H15
L0_CADIN_L15	V6	L0_CADIN_L(15)	L0_CADOUT_L(15)	Y4	L0_CADOUT_L15
L0_CADIN_H14	T4	L0_CADIN_H(14)	L0_CADOUT_H(14)	AB6	L0_CADOUT_H14
L0_CADIN_L14	T5	L0_CADIN_L(14)	L0_CADOUT_L(14)	AA6	L0_CADOUT_L14
L0_CADIN_H13	R6	L0_CADIN_H(13)	L0_CADOUT_H(13)	AB5	L0_CADOUT_H13
L0_CADIN_L13	T6	L0_CADIN_L(13)	L0_CADOUT_L(13)	AB4	L0_CADOUT_L13
L0_CADIN_H12	P4	L0_CADIN_H(12)	L0_CADOUT_H(12)	AD6	L0_CADOUT_H12
L0_CADIN_L12	P5	L0_CADIN_L(12)	L0_CADOUT_L(12)	AC6	L0_CADOUT_L12
L0_CADIN_H11	M4	L0_CADIN_H(11)	L0_CADOUT_H(11)	AE6	L0_CADOUT_H11
L0_CADIN_L11	M5	L0_CADIN_L(11)	L0_CADOUT_L(11)	AE6	L0_CADOUT_L11
L0_CADIN_H10	L6	L0_CADIN_H(10)	L0_CADOUT_H(10)	AF5	L0_CADOUT_H10
L0_CADIN_L10	M6	L0_CADIN_L(10)	L0_CADOUT_L(10)	AF4	L0_CADOUT_L10
L0_CADIN_H9	K4	L0_CADIN_H(9)	L0_CADOUT_H(9)	AH6	L0_CADOUT_H9
L0_CADIN_L9	K5	L0_CADIN_L(9)	L0_CADOUT_L(9)	AG6	L0_CADOUT_L9
L0_CADIN_H8	J6	L0_CADIN_H(8)	L0_CADOUT_H(8)	AH5	L0_CADOUT_H8
L0_CADIN_L8	K6	L0_CADIN_L(8)	L0_CADOUT_L(8)	AH4	L0_CADOUT_L8
L0_CADIN_H7	U3	L0_CADIN_H(7)	L0_CADOUT_H(7)	Y1	L0_CADOUT_H7
L0_CADIN_L7	U2	L0_CADIN_L(7)	L0_CADOUT_L(7)	W1	L0_CADOUT_L7
L0_CADIN_H6	R1	L0_CADIN_H(6)	L0_CADOUT_H(6)	AA2	L0_CADOUT_H6
L0_CADIN_L6	T1	L0_CADIN_L(6)	L0_CADOUT_L(6)	AA3	L0_CADOUT_L6
L0_CADIN_H5	R3	L0_CADIN_H(5)	L0_CADOUT_H(5)	AB1	L0_CADOUT_H5
L0_CADIN_L5	R2	L0_CADIN_L(5)	L0_CADOUT_L(5)	AA1	L0_CADOUT_L5
L0_CADIN_H4	N1	L0_CADIN_H(4)	L0_CADOUT_H(4)	AC2	L0_CADOUT_H4
L0_CADIN_L4	P1	L0_CADIN_L(4)	L0_CADOUT_L(4)	AC3	L0_CADOUT_L4
L0_CADIN_H3	L1	L0_CADIN_H(3)	L0_CADOUT_H(3)	AE2	L0_CADOUT_H3
L0_CADIN_L3	M1	L0_CADIN_L(3)	L0_CADOUT_L(3)	AE3	L0_CADOUT_L3
L0_CADIN_H2	L3	L0_CADIN_H(2)	L0_CADOUT_H(2)	AF1	L0_CADOUT_H2
L0_CADIN_L2	L2	L0_CADIN_L(2)	L0_CADOUT_L(2)	AE1	L0_CADOUT_L2
L0_CADIN_H1	J1	L0_CADIN_H(1)	L0_CADOUT_H(1)	AG2	L0_CADOUT_H1
L0_CADIN_L1	K1	L0_CADIN_L(1)	L0_CADOUT_L(1)	AG3	L0_CADOUT_L1
L0_CADIN_H0	J3	L0_CADIN_H(0)	L0_CADOUT_H(0)	AH1	L0_CADOUT_H0
L0_CADIN_L0	J2	L0_CADIN_L(0)	L0_CADOUT_L(0)	AG1	L0_CADOUT_L0

VCORE
SC24 0.01U/4/Y5V/25V/Z
SC23 0.01U/4/Y5V/25V/Z
SC18 0.01U/4/Y5V/25V/Z

CLOSE CHIPSET & CROSSING BOUNDARY

SOCKET_M2
M2_RM/PLASTICS/[12KRC-04K807-42R_12KRC-04K807-43R]

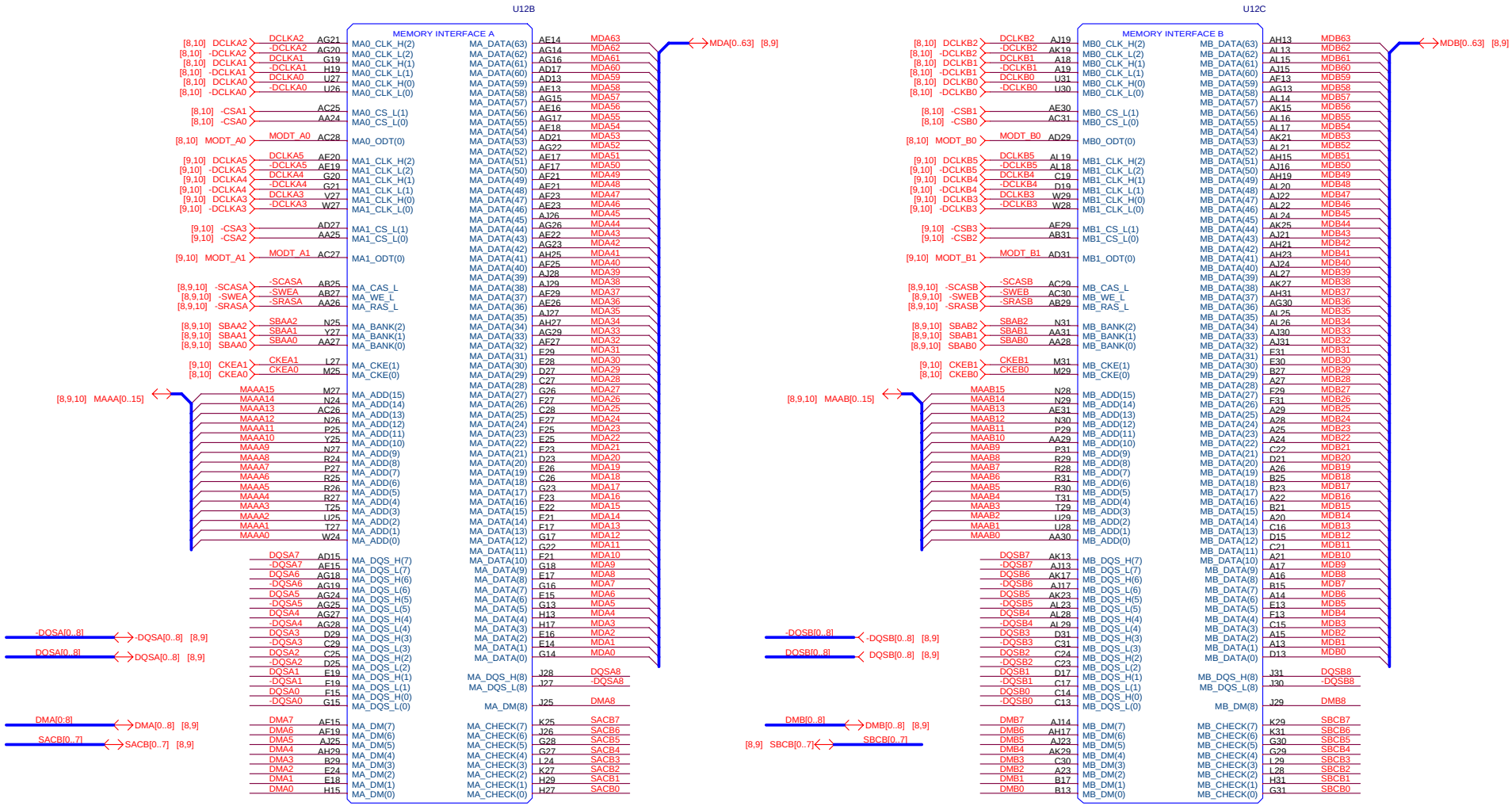


GIGABYTE CORP.

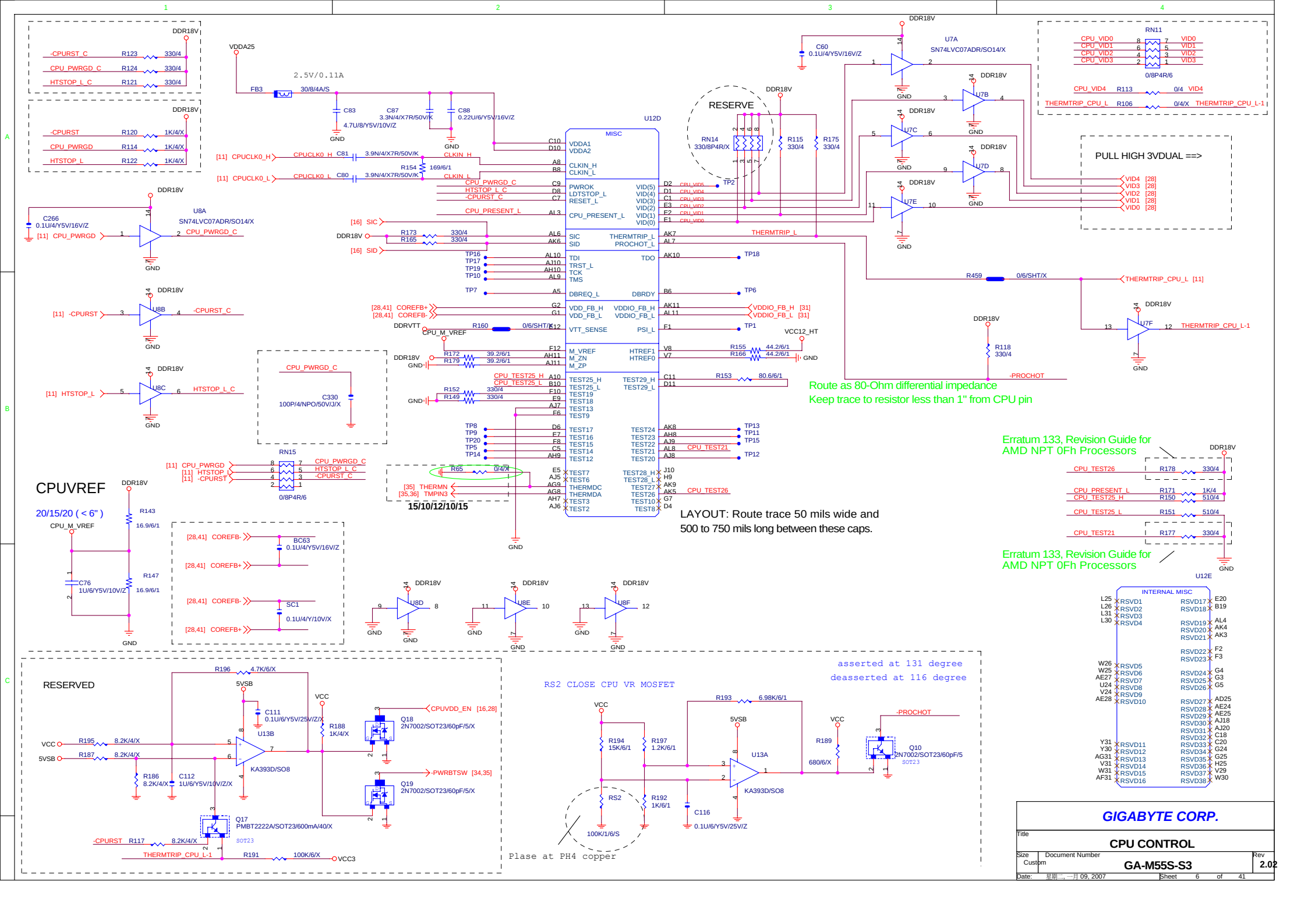
Title: CPU HYPER TRANSPORT

Size: Custom | Document Number: GA-M55S-S3 | Rev: 2.02

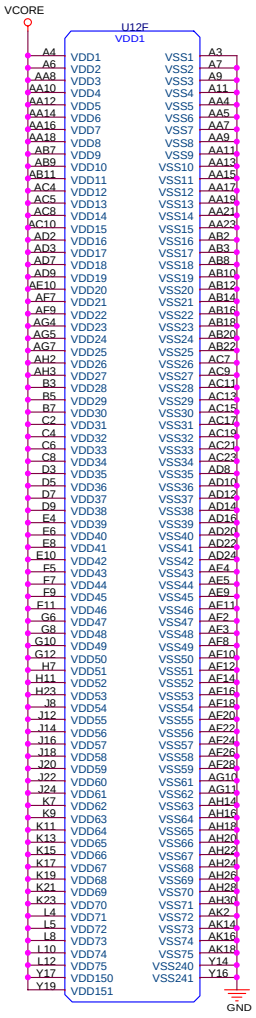
Date: 星期二, 一月 09, 2007 | Sheet 4 of 41

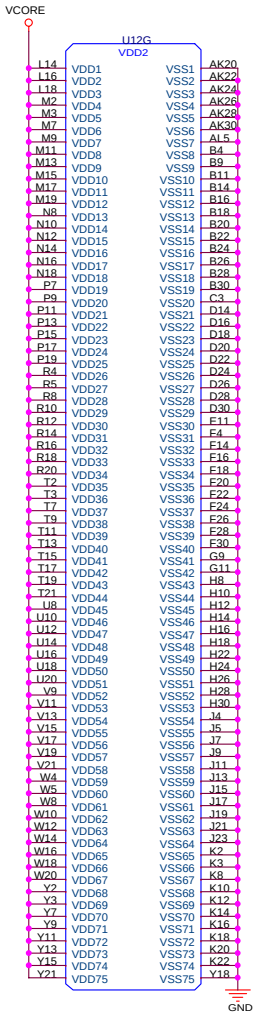


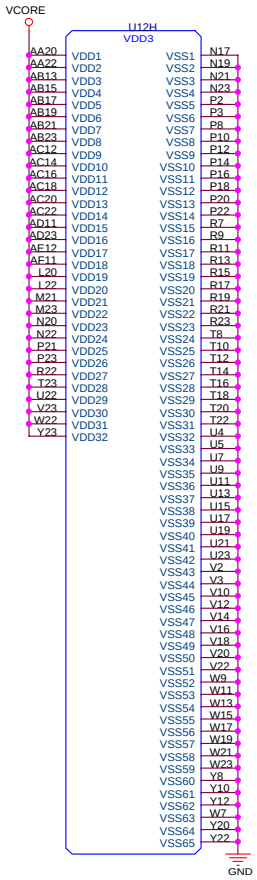
GIGABYTE CORP.		
Title: CPU DDRII MEMORY		
Size: Custom	Document Number: GA-M55S-S3	Rev: 2.02
Date: 星期二, 一月 09, 2007	Sheet 5 of 41	

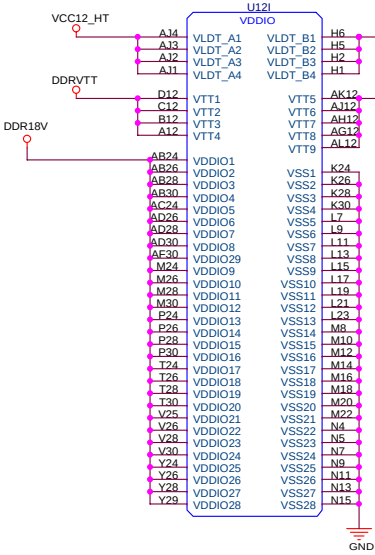

DDR18V
-CPURST_C R123 330/4
CPU_PWRGD_C R124 330/4
HTSTOP_L_C R121 330/4
-CPURST R120 1K/4/X
CPU_PWRGD R114 1K/4/X
HTSTOP_L R122 1K/4/X
VDDA25
2.5V/0.11A
FB3 30/8/4A/S
C83 4.7U/8/Y5V/10V/Z
C87 3.3N/4/X7R/50V/K
C88 0.22U/6/Y5V/16V/Z
GND
[11] CPUCLK0_H CPUCLK0_H C81 3.9N/4/X7R/50V/K CLKIN_H
[11] CPUCLK0_L CPUCLK0_L C80 3.9N/4/X7R/50V/K CLKIN_L
R154 169/6/1
CPU_PWRGD_C
HTSTOP_L_C
-CPURST_C
CPU_PRESENT_L
U12D
MISC
VDDA1
VDDA2
CLKIN_H
CLKIN_L
PWROK
LDTSTOP_L
RESET_L
CPU_PRESENT_L
VID(5)
VID(4)
VID(3)
VID(2)
VID(1)
VID(0)
RESERVE
RN14 330/8P4R/X
R115 330/4
R175 330/4
TP2
U7A SN74LVC07ADR/SO14/X
C60 0.1U/4/Y5V/16V/Z
RN11
CPU_VID0 VID0
CPU_VID1 VID1
CPU_VID2 VID2
CPU_VID3 VID3
0/8P4R/6
CPU_VID4 R113 0/4 VID4
THERMTRIP_CPU_L R106 0/4/X THERMTRIP_CPU_L-1
U7B
U7C
U7D
U7E
PULL HIGH 3VDUAL ==>
VID4 [28]
VID3 [28]
VID2 [28]
VID1 [28]
VID0 [28]
U8A SN74LVC07ADR/SO14/X
C266 0.1U/4/Y5V/16V/Z
[11] CPU_PWRGD
CPU_PWRGD_C
[16] SIC
[16] SID
R173 330/4
R165 330/4
SIC
SID
THERMTRIP_L
PROCHOT_L
THERMTRIP_L
R459 0/6/SHT/X
THERMTRIP_CPU_L [11]
U7F
THERMTRIP_CPU_L-1
TP16
TP17
TP19
TP10
TP7
TDI
TRST_L
TCK
TMS
TDO
TP18
DBREQ_L
DBRDY
TP6
[28,41] COREFB+
[28,41] COREFB-
VDD_FB_H
VDD_FB_L
VDDIO_FB_H
VDDIO_FB_L
[31]
DDRVTT
R160 0/6/SHT/X
VTT_SENSE
PSI_L
TP1
CPU_M_VREF
VCC12_HT
R172 39.2/6/1
R179 39.2/6/1
M_VREF
M_ZN
M_ZP
HTREF1
HTREF0
R155 44.2/6/1
R166 44.2/6/1
U8B
U8C
[11] -CPURST
[11] HTSTOP_L
-CPURST_C
HTSTOP_L_C
CPU_PWRGD_C
C330 100P/4/NPO/50V/J/X
CPU_TEST25_H
CPU_TEST25_L
TEST25_H
TEST25_L
TEST19
TEST18
TEST13
TEST9
TEST29_H
TEST29_L
C11
D11
R153 80.6/6/1
R152 330/4
R149 330/4
R118 330/4
-PROCHOT
Route as 80-Ohm differential impedance
Keep trace to resistor less than 1" from CPU pin
TP8
TP9
TP20
TP5
TP14
TEST17
TEST16
TEST15
TEST14
TEST12
TEST24
TEST23
TEST22
TEST21
TEST20
CPU_TEST21
TP13
TP11
TP15
TP12
RN15
[11] CPU_PWRGD
[11] HTSTOP
[11] -CPURST
CPU_PWRGD_C
HTSTOP_L_C
-CPURST_C
0/8P4R/6
R65 0/4/X
[35] THERMN
[35,36] TMPIN3
15/10/12/10/15
TEST7
TEST6
THERMDC
THERMDA
TEST3
TEST2
TEST28_H
TEST28_L
TEST27
TEST26
TEST10
TEST8
CPU_TEST26
LAYOUT: Route trace 50 mils wide and
500 to 750 mils long between these caps.
Erratum 133, Revision Guide for
AMD NPT 0Fh Processors
CPU_TEST26 R178 330/4
CPU_PRESENT_L R171 1K/4
CPU_TEST25_H R150 510/4
CPU_TEST25_L R151 510/4
CPU_TEST21 R177 330/4
Erratum 133, Revision Guide for
AMD NPT 0Fh Processors
U12E
INTERNAL MISC
RSVD1
RSVD2
RSVD3
RSVD4
RSVD5
RSVD6
RSVD7
RSVD8
RSVD9
RSVD10
RSVD11
RSVD12
RSVD13
RSVD14
RSVD15
RSVD16
RSVD17
RSVD18
RSVD19
RSVD20
RSVD21
RSVD22
RSVD23
RSVD24
RSVD25
RSVD26
RSVD27
RSVD28
RSVD29
RSVD30
RSVD31
RSVD32
RSVD33
RSVD34
RSVD35
RSVD36
RSVD37
RSVD38
CPUVREF
20/15/20 (< 6")
CPU_M_VREF
R143 16.9/6/1
R147 16.9/6/1
C76 1U/6/Y5V/10V/Z
[28,41] COREFB-
[28,41] COREFB+
BC63 0.1U/4/Y5V/16V/Z
SC1 0.1U/4/Y/10V/X
U8D
U8E
U8F
RESERVED
R196 4.7K/6/X
5VSB
VCC
C111 0.1U/6/Y5V/25V/Z/X
U13B
KA393D/SO8
R188 1K/4/X
R195 8.2K/4/X
R187 8.2K/4/X
R186 8.2K/4/X
C112 1U/6/Y5V/10V/Z/X
CPUVDD_EN [16,28]
Q18 2N7002/SOT23/60pF/5/X
-PWRBTSW [34,35]
Q19 2N7002/SOT23/60pF/5/X
Q17 PMBT2222A/SOT23/600mA/40/X
SOT23
-CPURST R117 8.2K/4/X
THERMTRIP_CPU_L-1
R191 100K/6/X
VCC3
RS2 CLOSE CPU VR MOSFET
asserted at 131 degree
deasserted at 116 degree
R193 6.98K/6/1
R194 15K/6/1
R197 1.2K/6/1
R189 680/6/X
Q10 2N7002/SOT23/60pF/5
R192 1K/6/1
C116 0.1U/6/Y5V/25V/Z
RS2 100K/1/6/S
Plase at PH4 copper
GIGABYTE CORP.
Title
CPU CONTROL
Size Custom
Document Number GA-M55S-S3
Rev 2.02
Date: 星期二, 一月 09, 2007
Sheet 6 of 41

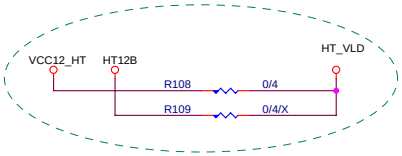
VLDT_RUN_B is connected to the VLDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.

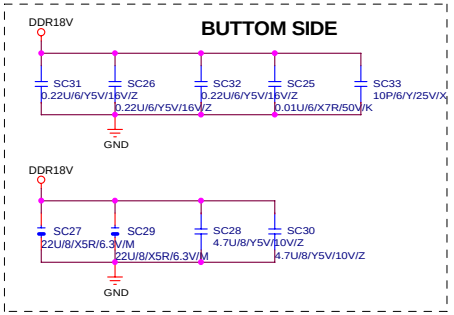


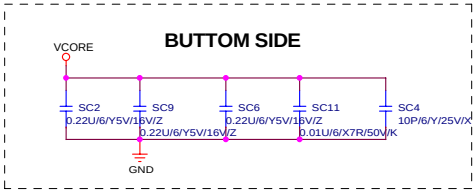


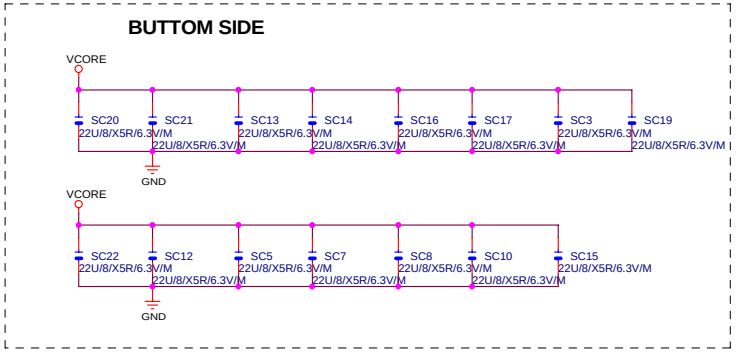


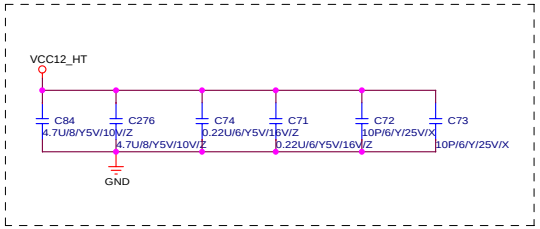


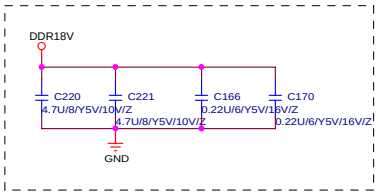


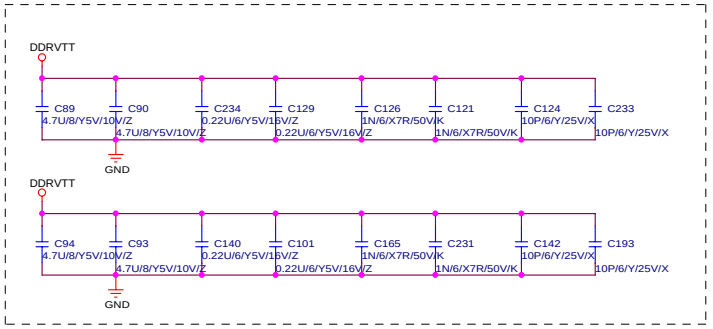


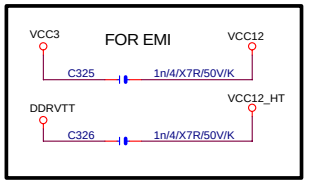










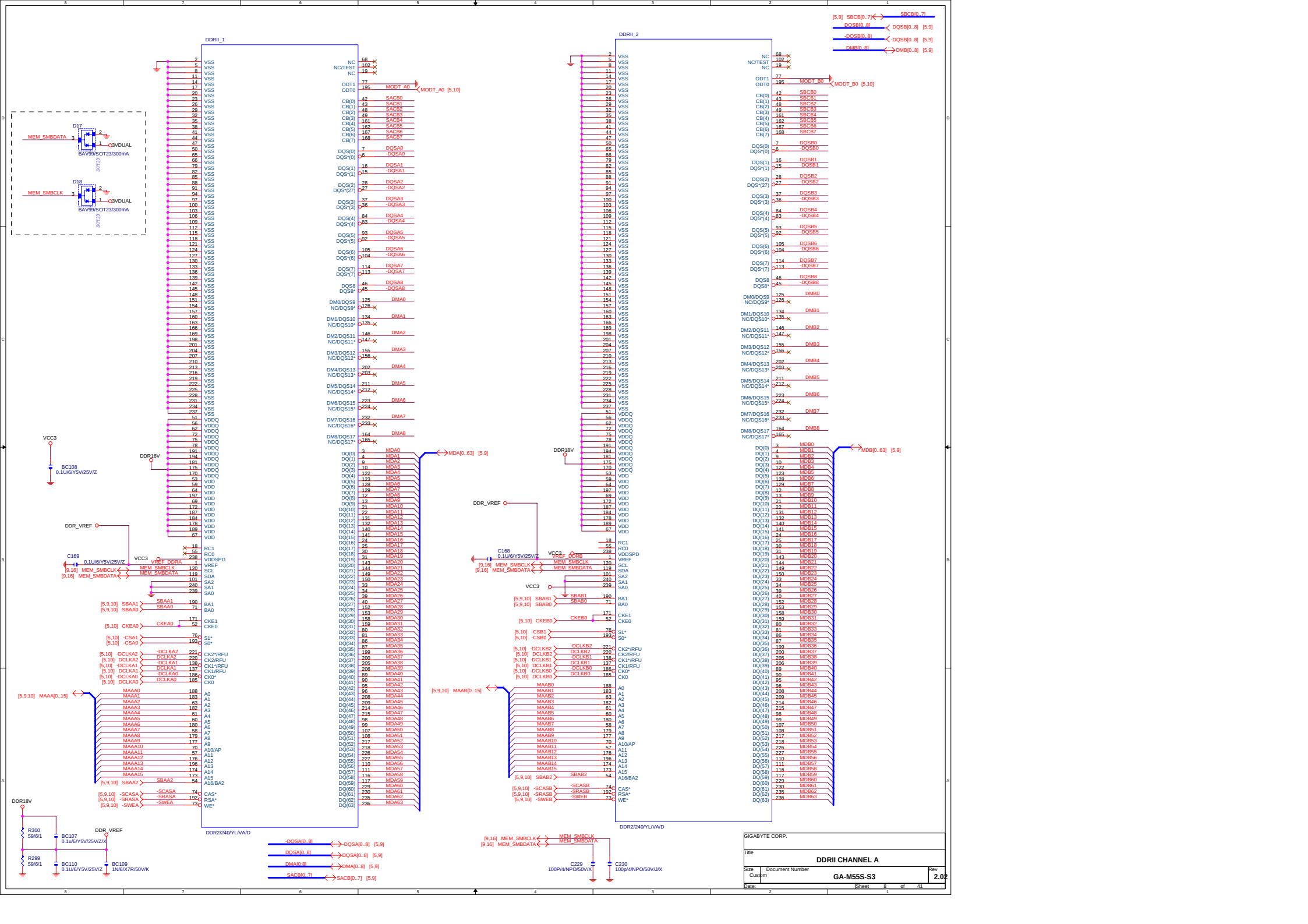


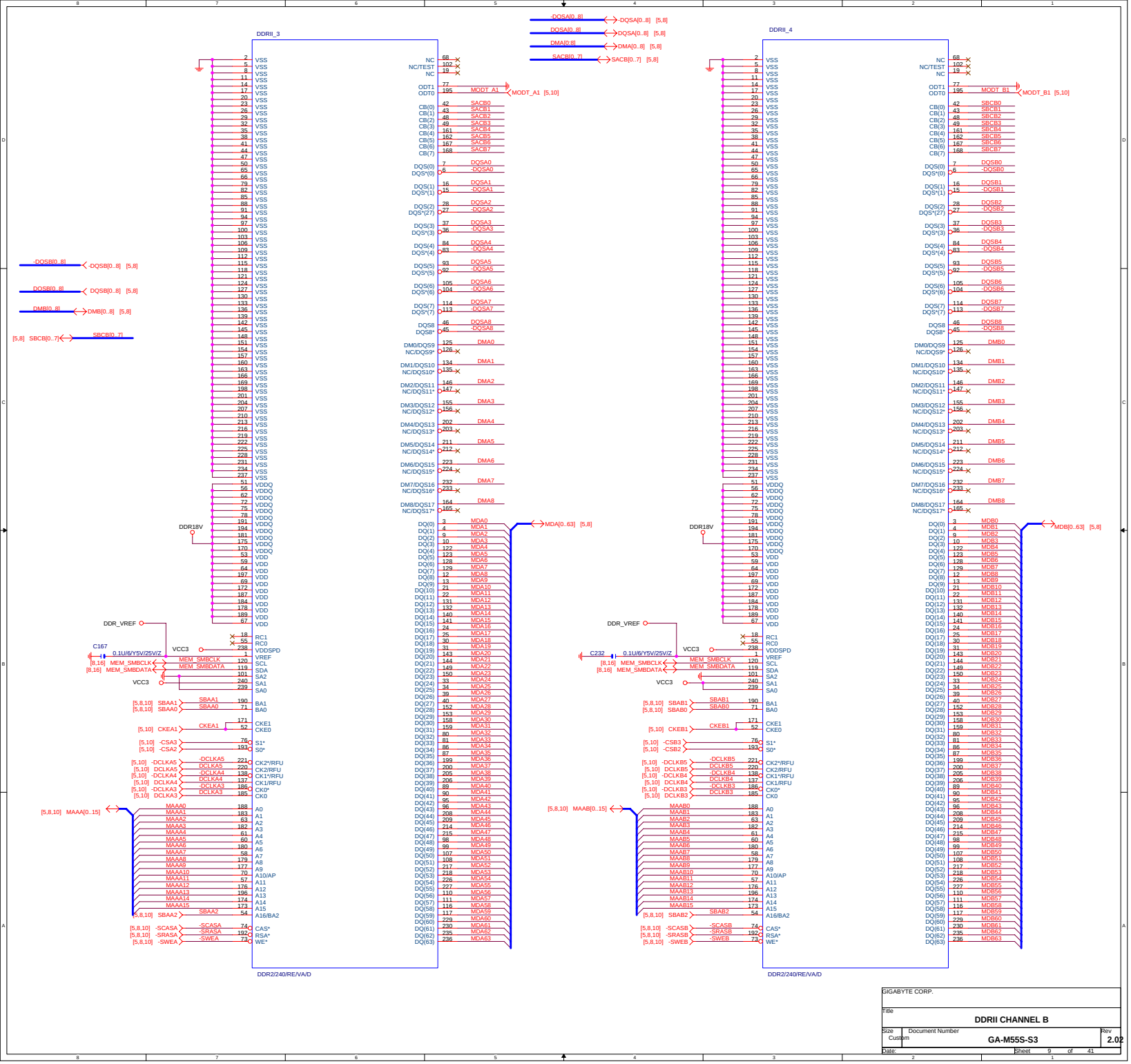
GIGABYTE CORP.

Title: CPU POWER & GND

Size	Document Number	Rev
Custom	GA-M55S-S3	2.02

Date: 星期二, 一月 09, 2007 Sheet 7 of 41


DDRII_1
DDRII_2
DDR2/240/YL/VA/D
DDR18V
VCC3
DDR_VREF
MEM_SMBDATA
MEM_SMBCLK
BAV99/SOT23/300mA
3VDUAL
D17
D18
BC108 0.1U/6/Y5V/25V/Z
BC107 0.1u/6/Y5V/25V/Z/X
BC110 0.1U/6/Y5V/25V/Z
BC109 1N/6/X7R/50V/K
C169 0.1U/6/Y5V/25V/Z
C168 0.1U/6/Y5V/25V/Z
C229 100P/4/NPO/50V/X
C230 100p/4/NPO/50V/J/X
R300 59/6/1
R299 59/6/1
MODT_A0 [5,10]
MODT_B0 [5,10]
MDA[0..63] [5,9]
MDB[0..63] [5,9]
SBCB[0..7] [5,9]
DQSB[0..8] [5,9]
DMB[0..8] [5,9]
-DQSA[0..8] [5,9]
DQSA[0..8] [5,9]
DMA[0..8] [5,9]
SACB[0..7] [5,9]
MAAA[0..15] [5,9,10]
MAAB[0..15] [5,9,10]
GIGABYTE CORP.
DDRII CHANNEL A
GA-M55S-S3
2.02
Custom
Sheet 8 of 41

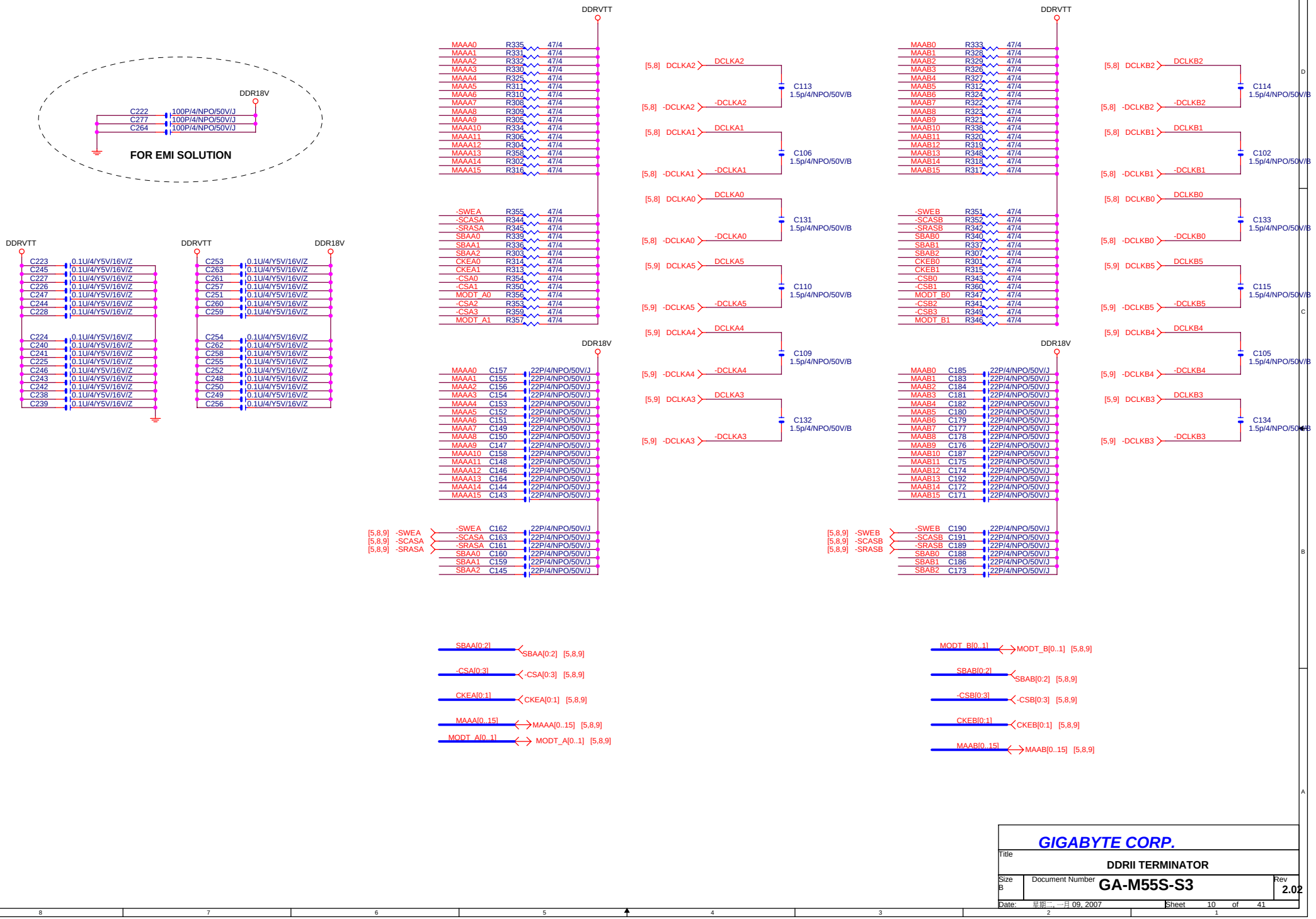


GIGABYTE CORP.

Title: **DDRII CHANNEL B**

Size	Document Number	Rev
Custom	GA-M55S-S3	2.02

Date: | Sheet 9 of 41


DDR18V
C222 100P/4/NPO/50V/J
C277 100P/4/NPO/50V/J
C264 100P/4/NPO/50V/J
FOR EMI SOLUTION
DDRVTT
C223 0.1U/4/Y5V/16V/Z
C245 0.1U/4/Y5V/16V/Z
C227 0.1U/4/Y5V/16V/Z
C226 0.1U/4/Y5V/16V/Z
C247 0.1U/4/Y5V/16V/Z
C244 0.1U/4/Y5V/16V/Z
C228 0.1U/4/Y5V/16V/Z
C224 0.1U/4/Y5V/16V/Z
C240 0.1U/4/Y5V/16V/Z
C241 0.1U/4/Y5V/16V/Z
C225 0.1U/4/Y5V/16V/Z
C246 0.1U/4/Y5V/16V/Z
C243 0.1U/4/Y5V/16V/Z
C242 0.1U/4/Y5V/16V/Z
C238 0.1U/4/Y5V/16V/Z
C239 0.1U/4/Y5V/16V/Z
DDRVTT
DDR18V
C253 0.1U/4/Y5V/16V/Z
C263 0.1U/4/Y5V/16V/Z
C261 0.1U/4/Y5V/16V/Z
C257 0.1U/4/Y5V/16V/Z
C251 0.1U/4/Y5V/16V/Z
C260 0.1U/4/Y5V/16V/Z
C259 0.1U/4/Y5V/16V/Z
C254 0.1U/4/Y5V/16V/Z
C262 0.1U/4/Y5V/16V/Z
C258 0.1U/4/Y5V/16V/Z
C255 0.1U/4/Y5V/16V/Z
C252 0.1U/4/Y5V/16V/Z
C248 0.1U/4/Y5V/16V/Z
C250 0.1U/4/Y5V/16V/Z
C249 0.1U/4/Y5V/16V/Z
C256 0.1U/4/Y5V/16V/Z
DDRVTT
MAAA0 R335 47/4
MAAA1 R331 47/4
MAAA2 R332 47/4
MAAA3 R330 47/4
MAAA4 R325 47/4
MAAA5 R311 47/4
MAAA6 R310 47/4
MAAA7 R308 47/4
MAAA8 R309 47/4
MAAA9 R305 47/4
MAAA10 R334 47/4
MAAA11 R306 47/4
MAAA12 R304 47/4
MAAA13 R358 47/4
MAAA14 R302 47/4
MAAA15 R316 47/4
-SWEA R355 47/4
-SCASA R344 47/4
-SRASA R345 47/4
SBAA0 R339 47/4
SBAA1 R336 47/4
SBAA2 R303 47/4
CKEA0 R314 47/4
CKEA1 R313 47/4
-CSA0 R354 47/4
-CSA1 R350 47/4
MODT_A0 R356 47/4
-CSA2 R353 47/4
-CSA3 R359 47/4
MODT_A1 R357 47/4
DDR18V
MAAA0 C157 22P/4/NPO/50V/J
MAAA1 C155 22P/4/NPO/50V/J
MAAA2 C156 22P/4/NPO/50V/J
MAAA3 C154 22P/4/NPO/50V/J
MAAA4 C153 22P/4/NPO/50V/J
MAAA5 C152 22P/4/NPO/50V/J
MAAA6 C151 22P/4/NPO/50V/J
MAAA7 C149 22P/4/NPO/50V/J
MAAA8 C150 22P/4/NPO/50V/J
MAAA9 C147 22P/4/NPO/50V/J
MAAA10 C158 22P/4/NPO/50V/J
MAAA11 C148 22P/4/NPO/50V/J
MAAA12 C146 22P/4/NPO/50V/J
MAAA13 C164 22P/4/NPO/50V/J
MAAA14 C144 22P/4/NPO/50V/J
MAAA15 C143 22P/4/NPO/50V/J
[5,8,9] -SWEA -SCASA -SRASA
-SWEA C162 22P/4/NPO/50V/J
-SCASA C163 22P/4/NPO/50V/J
-SRASA C161 22P/4/NPO/50V/J
SBAA0 C160 22P/4/NPO/50V/J
SBAA1 C159 22P/4/NPO/50V/J
SBAA2 C145 22P/4/NPO/50V/J
[5,8] DCLKA2
[5,8] -DCLKA2
[5,8] DCLKA1
[5,8] -DCLKA1
[5,8] DCLKA0
[5,8] -DCLKA0
[5,9] DCLKA5
[5,9] -DCLKA5
[5,9] DCLKA4
[5,9] -DCLKA4
[5,9] DCLKA3
[5,9] -DCLKA3
DCLKA2
-DCLKA2
DCLKA1
-DCLKA1
DCLKA0
-DCLKA0
DCLKA5
-DCLKA5
DCLKA4
-DCLKA4
DCLKA3
-DCLKA3
C113 1.5p/4/NPO/50V/B
C106 1.5p/4/NPO/50V/B
C131 1.5p/4/NPO/50V/B
C110 1.5p/4/NPO/50V/B
C109 1.5p/4/NPO/50V/B
C132 1.5p/4/NPO/50V/B
DDRVTT
MAAB0 R333 47/4
MAAB1 R328 47/4
MAAB2 R329 47/4
MAAB3 R326 47/4
MAAB4 R327 47/4
MAAB5 R312 47/4
MAAB6 R324 47/4
MAAB7 R322 47/4
MAAB8 R323 47/4
MAAB9 R321 47/4
MAAB10 R338 47/4
MAAB11 R320 47/4
MAAB12 R319 47/4
MAAB13 R348 47/4
MAAB14 R318 47/4
MAAB15 R317 47/4
-SWEB R351 47/4
-SCASB R352 47/4
-SRASB R342 47/4
SBAB0 R340 47/4
SBAB1 R337 47/4
SBAB2 R307 47/4
CKEB0 R301 47/4
CKEB1 R315 47/4
-CSB0 R343 47/4
-CSB1 R360 47/4
MODT_B0 R347 47/4
-CSB2 R341 47/4
-CSB3 R349 47/4
MODT_B1 R346 47/4
DDR18V
MAAB0 C185 22P/4/NPO/50V/J
MAAB1 C183 22P/4/NPO/50V/J
MAAB2 C184 22P/4/NPO/50V/J
MAAB3 C181 22P/4/NPO/50V/J
MAAB4 C182 22P/4/NPO/50V/J
MAAB5 C180 22P/4/NPO/50V/J
MAAB6 C179 22P/4/NPO/50V/J
MAAB7 C177 22P/4/NPO/50V/J
MAAB8 C178 22P/4/NPO/50V/J
MAAB9 C176 22P/4/NPO/50V/J
MAAB10 C187 22P/4/NPO/50V/J
MAAB11 C175 22P/4/NPO/50V/J
MAAB12 C174 22P/4/NPO/50V/J
MAAB13 C192 22P/4/NPO/50V/J
MAAB14 C172 22P/4/NPO/50V/J
MAAB15 C171 22P/4/NPO/50V/J
[5,8,9] -SWEB -SCASB -SRASB
-SWEB C190 22P/4/NPO/50V/J
-SCASB C191 22P/4/NPO/50V/J
-SRASB C189 22P/4/NPO/50V/J
SBAB0 C188 22P/4/NPO/50V/J
SBAB1 C186 22P/4/NPO/50V/J
SBAB2 C173 22P/4/NPO/50V/J
[5,8] DCLKB2
[5,8] -DCLKB2
[5,8] DCLKB1
[5,8] -DCLKB1
[5,8] DCLKB0
[5,8] -DCLKB0
[5,9] DCLKB5
[5,9] -DCLKB5
[5,9] DCLKB4
[5,9] -DCLKB4
[5,9] DCLKB3
[5,9] -DCLKB3
DCLKB2
-DCLKB2
DCLKB1
-DCLKB1
DCLKB0
-DCLKB0
DCLKB5
-DCLKB5
DCLKB4
-DCLKB4
DCLKB3
-DCLKB3
C114 1.5p/4/NPO/50V/B
C102 1.5p/4/NPO/50V/B
C133 1.5p/4/NPO/50V/B
C115 1.5p/4/NPO/50V/B
C105 1.5p/4/NPO/50V/B
C134 1.5p/4/NPO/50V/B
SBAA[0:2] SBAA[0:2] [5,8,9]
-CSA[0:3] -CSA[0:3] [5,8,9]
CKEA[0:1] CKEA[0:1] [5,8,9]
MAAA[0..15] MAAA[0..15] [5,8,9]
MODT_A[0..1] MODT_A[0..1] [5,8,9]
MODT_B[0..1] MODT_B[0..1] [5,8,9]
SBAB[0:2] SBAB[0:2] [5,8,9]
-CSB[0:3] -CSB[0:3] [5,8,9]
CKEB[0:1] CKEB[0:1] [5,8,9]
MAAB[0..15] MAAB[0..15] [5,8,9]
GIGABYTE CORP.
Title
DDRII TERMINATOR
Size B
Document Number GA-M55S-S3
Rev 2.02
Date: 星期三, 一月 09, 2007
Sheet 10 of 41

N.B HEATSINK or FANSINK

U5G1A PBGA776-NVIDIA-MCP55
MCP55S
NF550-N-A2
SEC 1 OF 9

HS2 HS1
FAN SINK/X
HEAT SINK/[12SP2-01A002-81R_12SP2-01A002-82R]

[4] L0_CADOUT_L[0..15] L0_CADOUT_L[0..15]
L0_CADOUT_H0 AK32 HT_MCP_RXD0_P
L0_CADOUT_H1 AJ32 HT_MCP_RXD1_P
L0_CADOUT_H2 AH32 HT_MCP_RXD2_P
L0_CADOUT_H3 AH30 HT_MCP_RXD3_P
L0_CADOUT_H4 AF31 HT_MCP_RXD4_P
L0_CADOUT_H5 AE32 HT_MCP_RXD5_P
L0_CADOUT_H6 AD32 HT_MCP_RXD6_P
L0_CADOUT_H7 AD30 HT_MCP_RXD7_P
L0_CADOUT_H8 AG27 HT_MCP_RXD8_P
L0_CADOUT_H9 AF27 HT_MCP_RXD9_P
L0_CADOUT_H10 AD26 HT_MCP_RXD10_P
L0_CADOUT_H11 AE29 HT_MCP_RXD11_P
L0_CADOUT_H12 AB23 HT_MCP_RXD12_P
L0_CADOUT_H13 AB26 HT_MCP_RXD13_P
L0_CADOUT_H14 AB28 HT_MCP_RXD14_P
L0_CADOUT_H15 AA28 HT_MCP_RXD15_P

[4] L0_CADOUT_H[0..15] L0_CADOUT_H[0..15]
L0_CADOUT_L0 AK31 HT_MCP_RXD0_N
L0_CADOUT_L1 AJ31 HT_MCP_RXD1_N
L0_CADOUT_L2 AH31 HT_MCP_RXD2_N
L0_CADOUT_L3 AH29 HT_MCP_RXD3_N
L0_CADOUT_L4 AE30 HT_MCP_RXD4_N
L0_CADOUT_L5 AE31 HT_MCP_RXD5_N
L0_CADOUT_L6 AD31 HT_MCP_RXD6_N
L0_CADOUT_L7 AD29 HT_MCP_RXD7_N
L0_CADOUT_L8 AG28 HT_MCP_RXD8_N
L0_CADOUT_L9 AF28 HT_MCP_RXD9_N
L0_CADOUT_L10 AD25 HT_MCP_RXD10_N
L0_CADOUT_L11 AE28 HT_MCP_RXD11_N
L0_CADOUT_L12 AB24 HT_MCP_RXD12_N
L0_CADOUT_L13 AB25 HT_MCP_RXD13_N
L0_CADOUT_L14 AB27 HT_MCP_RXD14_N
L0_CADOUT_L15 AA29 HT_MCP_RXD15_N

HT_MCP_TXD0_P R29 L0_CADIN_H0
HT_MCP_TXD1_P T29 L0_CADIN_H1
HT_MCP_TXD2_P T31 L0_CADIN_H2
HT_MCP_TXD3_P U31 L0_CADIN_H3
HT_MCP_TXD4_P W29 L0_CADIN_H4
HT_MCP_TXD5_P Y29 L0_CADIN_H5
HT_MCP_TXD6_P Y31 L0_CADIN_H6
HT_MCP_TXD7_P AA31 L0_CADIN_H7
HT_MCP_TXD8_P R24 L0_CADIN_H8
HT_MCP_TXD9_P T28 L0_CADIN_H9
HT_MCP_TXD10_P U28 L0_CADIN_H10
HT_MCP_TXD11_P T25 L0_CADIN_H11
HT_MCP_TXD12_P V27 L0_CADIN_H12
HT_MCP_TXD13_P V26 L0_CADIN_H13
HT_MCP_TXD14_P Y28 L0_CADIN_H14
HT_MCP_TXD15_P Y26 L0_CADIN_H15
L0_CADIN_H[0..15] L0_CADIN_H[0..15] [4]

HT_MCP_TXD0_N R30 L0_CADIN_L0
HT_MCP_TXD1_N T30 L0_CADIN_L1
HT_MCP_TXD2_N T32 L0_CADIN_L2
HT_MCP_TXD3_N U32 L0_CADIN_L3
HT_MCP_TXD4_N W30 L0_CADIN_L4
HT_MCP_TXD5_N Y30 L0_CADIN_L5
HT_MCP_TXD6_N Y32 L0_CADIN_L6
HT_MCP_TXD7_N AA32 L0_CADIN_L7
HT_MCP_TXD8_N T24 L0_CADIN_L8
HT_MCP_TXD9_N T27 L0_CADIN_L9
HT_MCP_TXD10_N U29 L0_CADIN_L10
HT_MCP_TXD11_N T26 L0_CADIN_L11
HT_MCP_TXD12_N V28 L0_CADIN_L12
HT_MCP_TXD13_N V25 L0_CADIN_L13
HT_MCP_TXD14_N Y27 L0_CADIN_L14
HT_MCP_TXD15_N Y25 L0_CADIN_L15
L0_CADIN_L[0..15] L0_CADIN_L[0..15] [4]

COUPON1 COUPON1 1 2 COUPON/X
COUPON2 COUPON2 1 2 COUPON/X
VCC

[4] L0_CLKOUT_H0 L0_CLKOUT_H0 AG30 HT_MCP_RX_CLK0_P
[4] L0_CLKOUT_L0 L0_CLKOUT_L0 AG29 HT_MCP_RX_CLK0_N
[4] L0_CLKOUT_H1 L0_CLKOUT_H1 AD27 HT_MCP_RX_CLK1_P
[4] L0_CLKOUT_L1 L0_CLKOUT_L1 AD28 HT_MCP_RX_CLK1_N

HT_MCP_TX_CLK0_P V30 L0_CLKIN_H0
HT_MCP_TX_CLK0_N V31 L0_CLKIN_L0
HT_MCP_TX_CLK1_P V24 L0_CLKIN_H1
HT_MCP_TX_CLK1_N W24 L0_CLKIN_L1
L0_CLKIN_H0 [4]
L0_CLKIN_L0 [4]
L0_CLKIN_H1 [4]
L0_CLKIN_L1 [4]

[4] L0_CTLOUT_H0 L0_CTLOUT_H0 AC30 HT_MCP_RXCTL_P
[4] L0_CTLOUT_L0 L0_CTLOUT_L0 AC29 HT_MCP_RXCTL_N

HT_MCP_TXCTL_P AB30 L0_CTLIN_H0
HT_MCP_TXCTL_N AB31 L0_CTLIN_L0
L0_CTLIN_H0 [4]
L0_CTLIN_L0 [4]

HT_MCP_REQ P25 -HT_REQ R232 1K/4
HT_MCP_STOP P28 HTSTOP_L
HT_MCP_RST P27 -CPURST
HT_MCP_PWRGD P26 CPU_PWRGD
3VDUAL
HTSTOP_L [6]
-CPURST [6]
CPU_PWRGD [6]

R297 150/6/1 HT_COMP1 AG26 HT_MCP_COMP_GND1
R295 49.9/6/1 HT_COMP2 AG25 HT_MCP_COMP_GND2

CLKOUT0_CLKIN_200MHZ_P N32 SR3 0/6/SHT/X CPUCLK0_H
CLKOUT0_CLKIN_200MHZ_N N31 SR1 0/6/SHT/X CPUCLK0_L
CPUCLK0_H [6]
CPUCLK0_L [6]
CLKOUT1_200MHZ_P M30 SR_CLKOUT1_P 1 TP41
CLKOUT1_200MHZ_N M29 TP_CLKOUT1_N 1 TP42
CLKOUT2_200MHZ_P L30 TP_CLKOUT2_P 1 TP37
CLKOUT2_200MHZ_N L29 TP_CLKOUT2_N 1 TP36

[6] THERMTRIP_CPU_L THERMTRIP_CPU_L AJ29 THERMTRIP/GPIO*

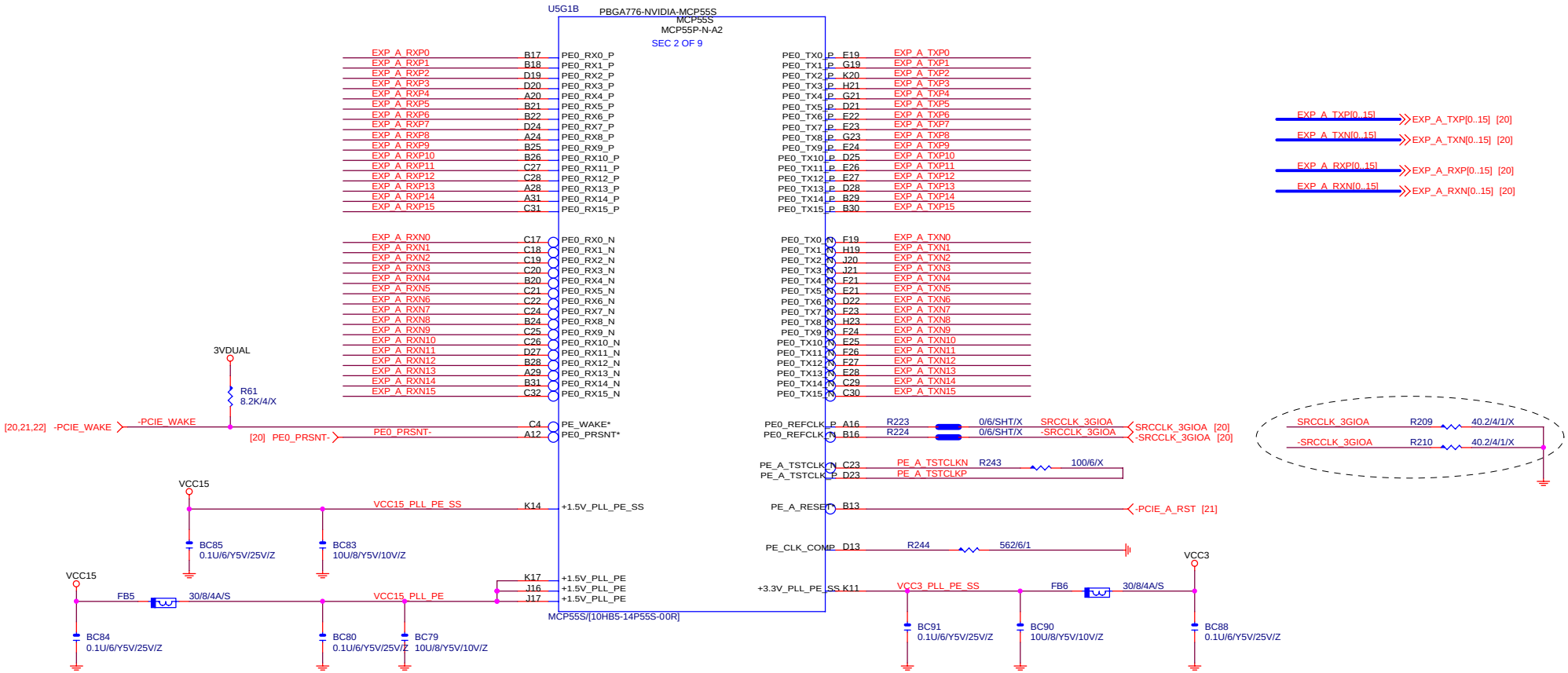
VCC15 P23 +1.5V_PLL_CPU_HT
VCC3 AC21 +3.3V_HT
AC22 +3.3V_PLL_CPU
AC23 +3.3V_PLL_HT
VCC12_HT
HT_VREF U23
CLKOUT_25MHZ N26 TP_CLKOUT_25M 1 TP45
CLK200_TERM_GND M28 R207 562/6/1
SC47 0.1U/4/Y5V/16V/Z

VCC3 FB9 30/8/4A/S VCC3_PLL_HT
C267 0.1U/6/Y5V/25V/Z
BC105 10U/8/Y5V/10V/Z
C217 0.1U/4/Y5V/16V/Z
C219 C194
0.1U/4/Y5V/16V/Z 0.1U/4/Y5V/16V/Z
MCP55S/[10HB5-14P55S-00R]

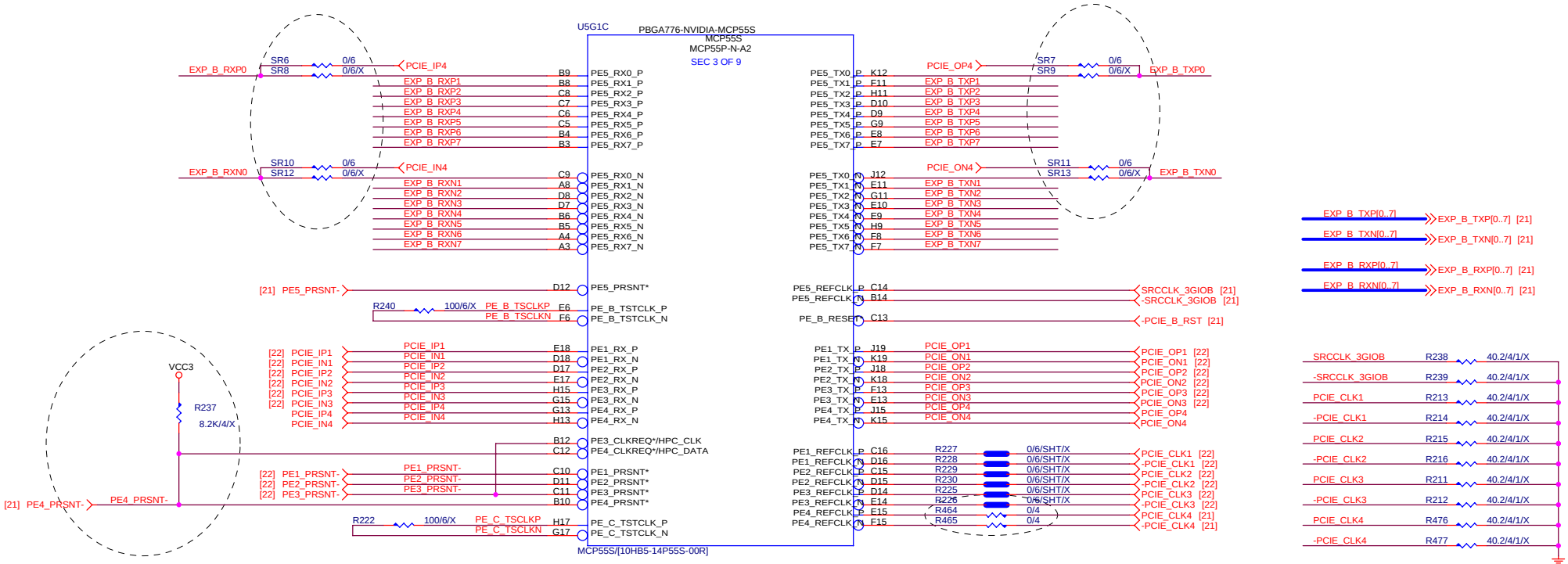
[20,21] -CK8PWOK
HTSTOP_L
Q25 2N7002/SOT23/60pF/5
CPU_PWRGD
Q22 2N7002/SOT23/60pF/5
-CPURST
Q27 2N7002/SOT23/60pF/5
3VDUAL
R233 8.2K/4
Q24 2N7002/SOT23/60pF/5
R201 0/6/SHT/X
[16,21,30] CK8_PWOK

GIGABYTE CORP.

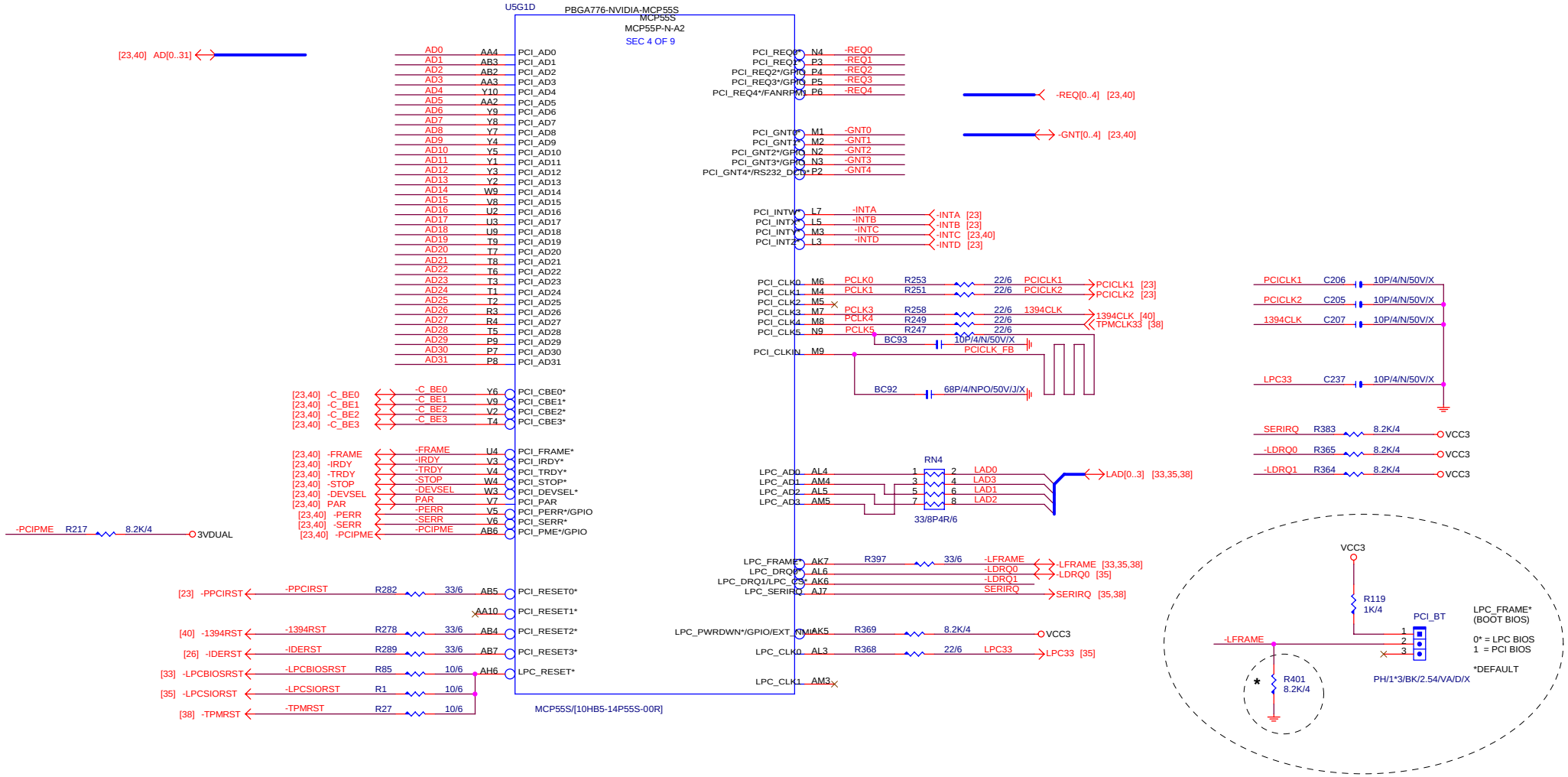
Title	MCP55 HT/CLK	
Size: Custom	Document Number: GA-M55S-S3	Rev: 2.02
Date: 星期二, 一月 09, 2007	Sheet 11 of 41	



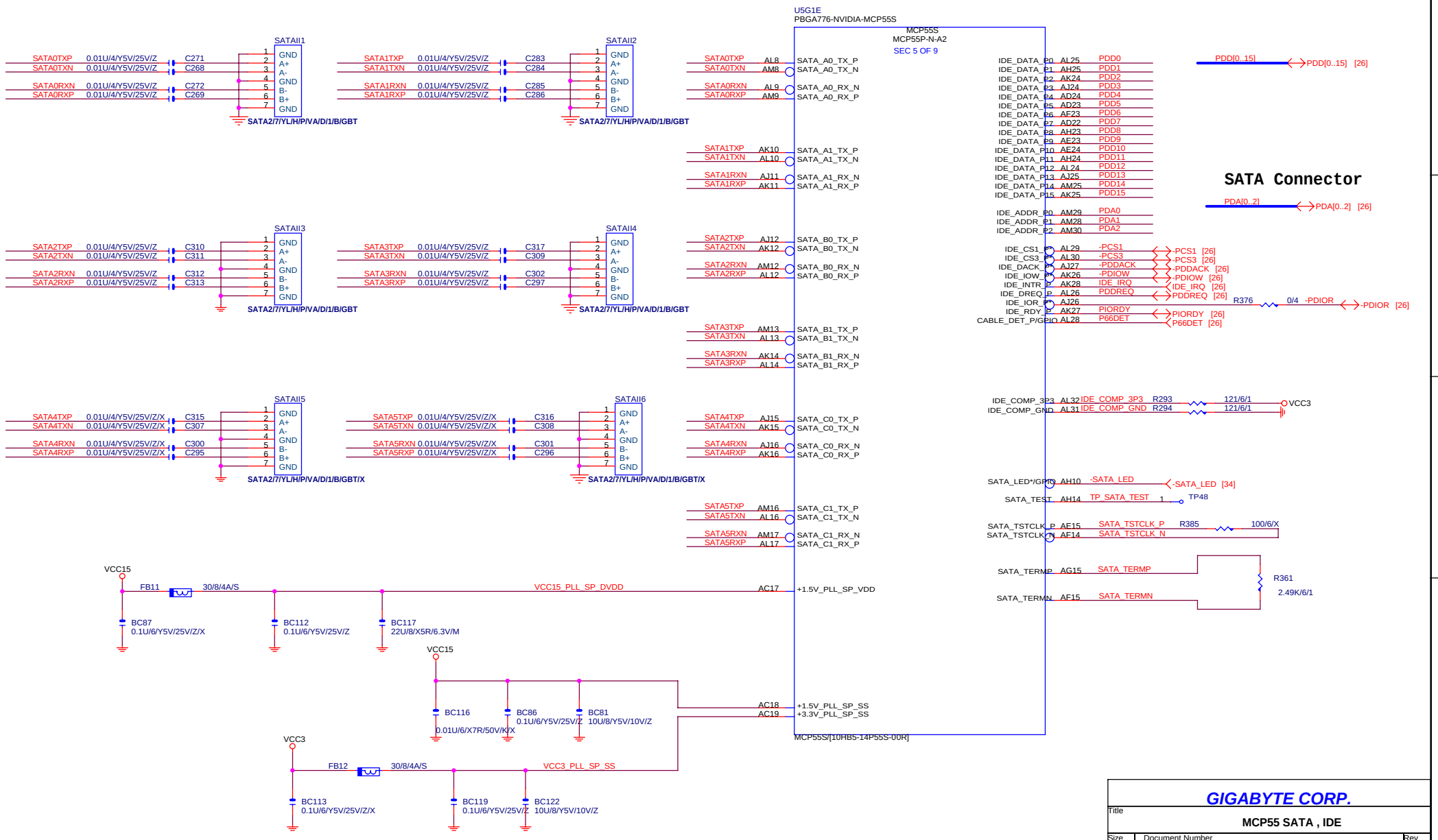
GIGABYTE CORP.		
Title: MCP55 PCIE X16		
Size: Custom	Document Number: GA-M55S-S3	Rev: 2.02
Date: 星期二, 一月 09, 2007	Sheet 12 of 41	

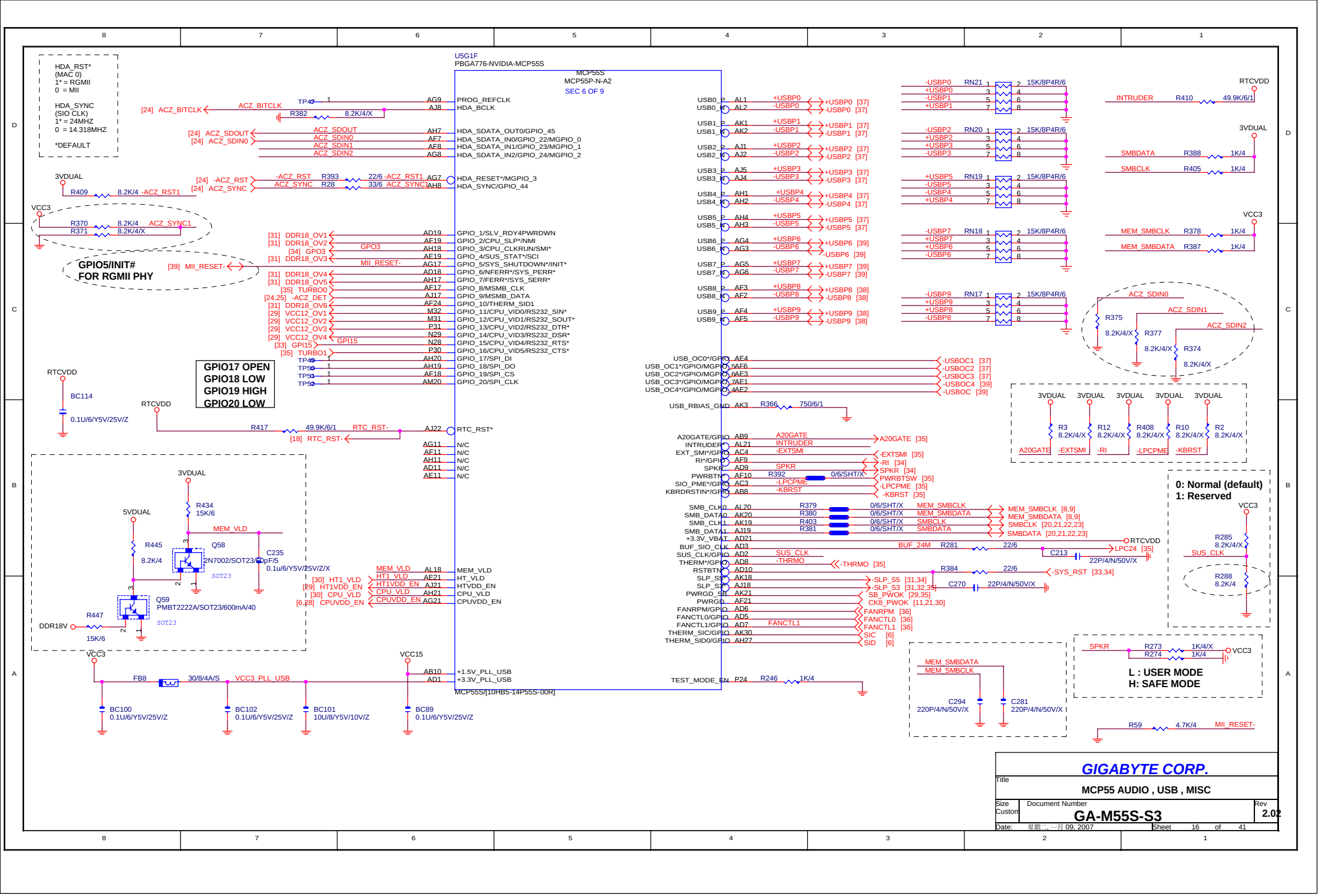


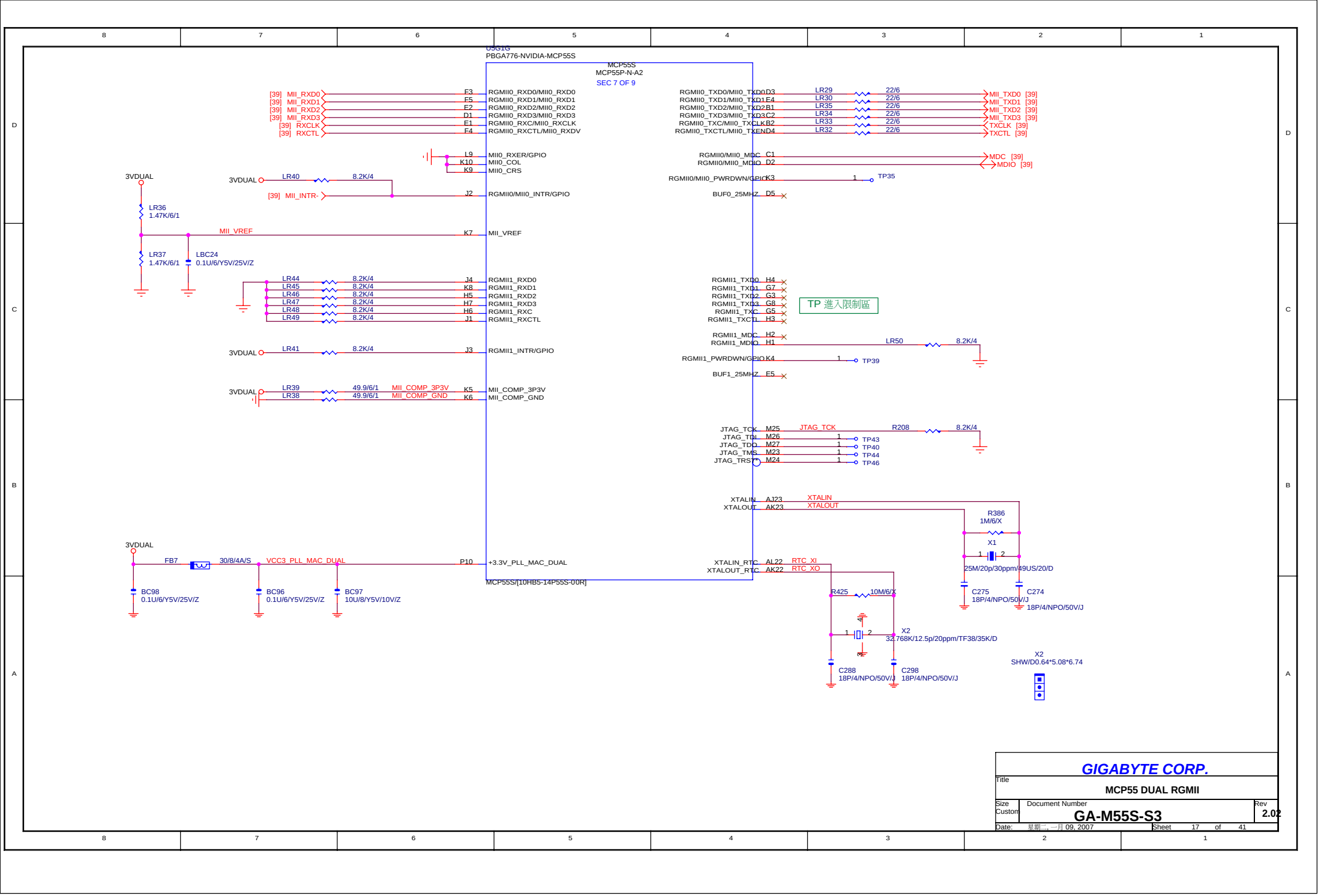
Company	GIGABYTE CORP.
Title	MCP55 PCIE X8 , X1
Size	Custom
Document Number	GA-M55S-S3
Rev	2.02
Date	星期二, 一月 09, 2007
Sheet	13 of 41

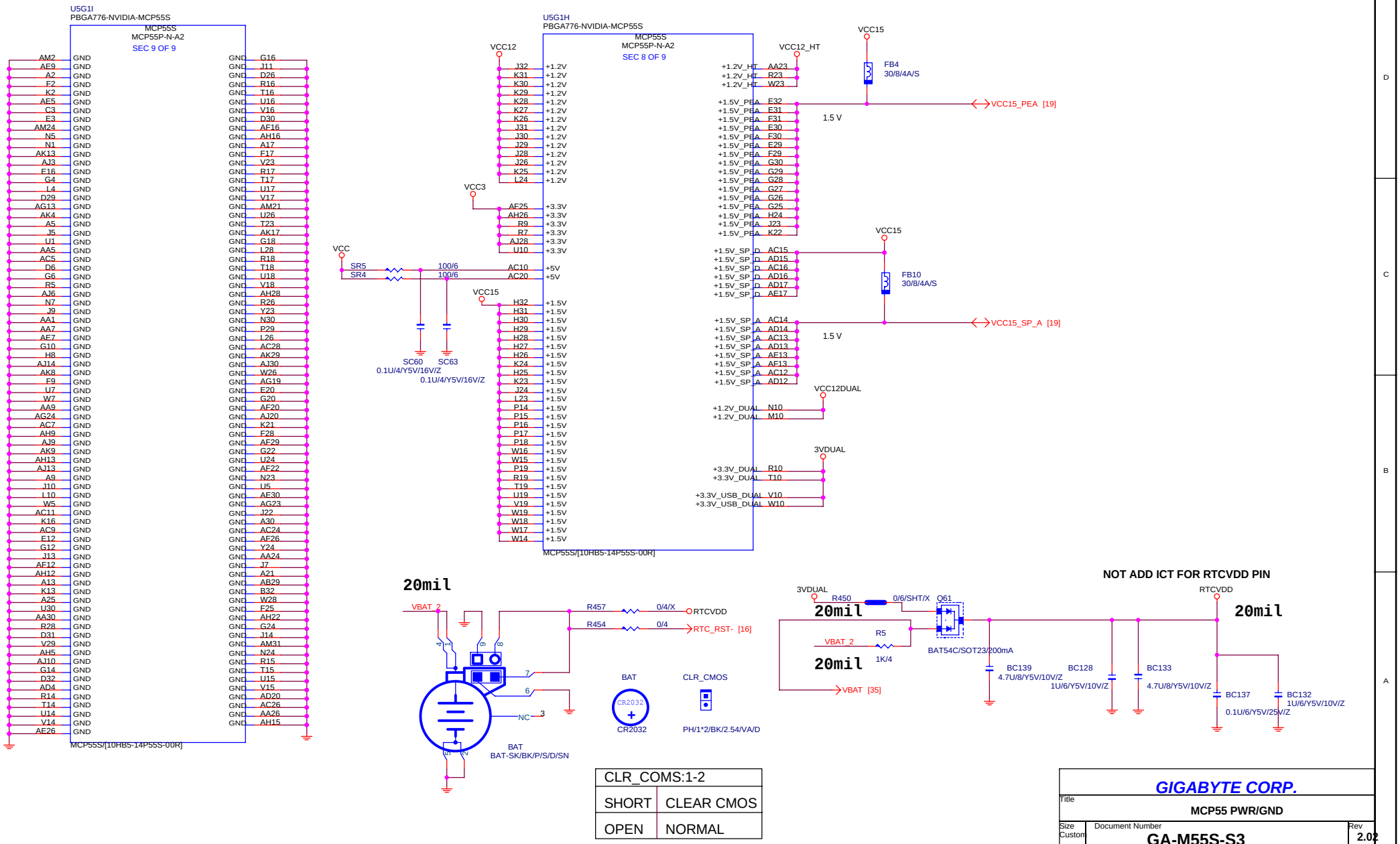


GIGABYTE CORP.		
Title: MCP55 PCI		
Size: Custom	Document Number: GA-M55S-S3	Rev: 2.02
Date: 星期二, 一月 09, 2007	Sheet 14 of 41	


U5G1E
PBGA776-NVIDIA-MCP55S
MCP55S
MCP55P-N-A2
SEC 5 OF 9
SATAII1
SATAII2
SATAII3
SATAII4
SATAII5
SATAII6
SATA2/7/YL/H/P/VA/D/1/B/GBT
SATA2/7/YL/H/P/VA/D/1/B/GBT/X
SATA Connector
PDD[0..15]
PDA[0..2]
VCC15
VCC3
FB11
FB12
30/8/4A/S
VCC15_PLL_SP_DVDD
VCC3_PLL_SP_SS
+1.5V_PLL_SP_VDD
+1.5V_PLL_SP_SS
+3.3V_PLL_SP_SS
MCP55S/[10HB5-14P55S-00R]
GIGABYTE CORP.
MCP55 SATA , IDE
GA-M55S-S3
2.02
Date: 星期二, 一月 09, 2007
Sheet 15 of 41


HDA_RST* (MAC 0) 1* = RGMII 0 = MII
HDA_SYNC (SIO CLK) 1* = 24MHZ 0 = 14.318MHZ
*DEFAULT
U5G1F
PBGA776-NVIDIA-MCP55S
MCP55S
MCP55P-N-A2
SEC 6 OF 9
GPIO5/INIT# FOR RGMII PHY
GPIO17 OPEN
GPIO18 LOW
GPIO19 HIGH
GPIO20 LOW
0: Normal (default)
1: Reserved
L : USER MODE
H: SAFE MODE
MCP55S/[10HB5-14P55S-00R]
GIGABYTE CORP.
MCP55 AUDIO , USB , MISC
GA-M55S-S3
2.02
Date: 星期二, 一月 09, 2007
Sheet 16 of 41


U5G1G
PBGA776-NVIDIA-MCP55S
MCP55S
MCP55P-N-A2
SEC 7 OF 9
[39] MII_RXD0
[39] MII_RXD1
[39] MII_RXD2
[39] MII_RXD3
[39] RXCLK
[39] RXCTL
F3 RGMII0_RXD0/MII0_RXD0
F5 RGMII0_RXD1/MII0_RXD1
E2 RGMII0_RXD2/MII0_RXD2
D1 RGMII0_RXD3/MII0_RXD3
E1 RGMII0_RXC/MII0_RXCLK
F4 RGMII0_RXCTL/MII0_RXDV
RGMII0_TXD0/MII0_TXD0 D3
RGMII0_TXD1/MII0_TXD1 E4
RGMII0_TXD2/MII0_TXD2 B1
RGMII0_TXD3/MII0_TXD3 C2
RGMII0_TXC/MII0_TXCLK B2
RGMII0_TXCTL/MII0_TXEND 4
LR29 LR30 LR35 LR34 LR33 LR32
22/6
MII_TXD0 [39]
MII_TXD1 [39]
MII_TXD2 [39]
MII_TXD3 [39]
TXCLK [39]
TXCTL [39]
L9 MII0_RXER/GPIO
K10 MII0_COL
K9 MII0_CRS
RGMII0/MII0_MDC C1
RGMII0/MII0_MDIO D2
MDC [39]
MDIO [39]
RGMII0/MII0_PWRDWN/GPIO K3
TP35
BUF0_25MHZ D5
3VDUAL
LR40 8.2K/4
[39] MII_INTR-
J2 RGMII0/MII0_INTR/GPIO
LR36 1.47K/6/1
MII_VREF
K7 MII_VREF
LR37 1.47K/6/1
LBC24 0.1U/6/Y5V/25V/Z
LR44 LR45 LR46 LR47 LR48 LR49 8.2K/4
J4 RGMII1_RXD0
K8 RGMII1_RXD1
H5 RGMII1_RXD2
H7 RGMII1_RXD3
H6 RGMII1_RXC
J1 RGMII1_RXCTL
RGMII1_TXD0 H4
RGMII1_TXD1 G7
RGMII1_TXD2 G3
RGMII1_TXD3 G8
RGMII1_TXC G5
RGMII1_TXCTL H3
TP 進入限制區
LR41 8.2K/4
J3 RGMII1_INTR/GPIO
RGMII1_MDC H2
RGMII1_MDIO H1
LR50 8.2K/4
RGMII1_PWRDWN/GPIO K4
TP39
BUF1_25MHZ E5
LR39 LR38 49.9/6/1
MII_COMP_3P3V
MII_COMP_GND
K5 MII_COMP_3P3V
K6 MII_COMP_GND
JTAG_TCK M25
JTAG_TDI M26
JTAG_TDO M27
JTAG_TMS M23
JTAG_TRST* M24
JTAG_TCK
R208 8.2K/4
TP43
TP40
TP44
TP46
XTALIN AJ23
XTALOUT AK23
XTALIN
XTALOUT
R386 1M/6/X
X1
25M/20p/30ppm/49US/20/D
C275 18P/4/NPO/50V/J
C274 18P/4/NPO/50V/J
FB7 30/8/4A/S
VCC3_PLL_MAC_DUAL
P10 +3.3V_PLL_MAC_DUAL
MCP55S/[10HB5-14P55S-00R]
BC98 0.1U/6/Y5V/25V/Z
BC96 0.1U/6/Y5V/25V/Z
BC97 10U/8/Y5V/10V/Z
XTALIN_RTC AL22
XTALOUT_RTC AK22
RTC_XI
RTC_XO
R425 10M/6/X
X2
32.768K/12.5p/20ppm/TF38/35K/D
C288 18P/4/NPO/50V/J
C298 18P/4/NPO/50V/J
X2
SHW/D0.64*5.08*6.74
GIGABYTE CORP.
Title
MCP55 DUAL RGMII
Size
Custom
Document Number
GA-M55S-S3
Rev
2.02
Date: 星期二, 一月 09, 2007
Sheet 17 of 41



CLR_COMS:1-2	
SHORT	CLEAR CMOS
OPEN	NORMAL

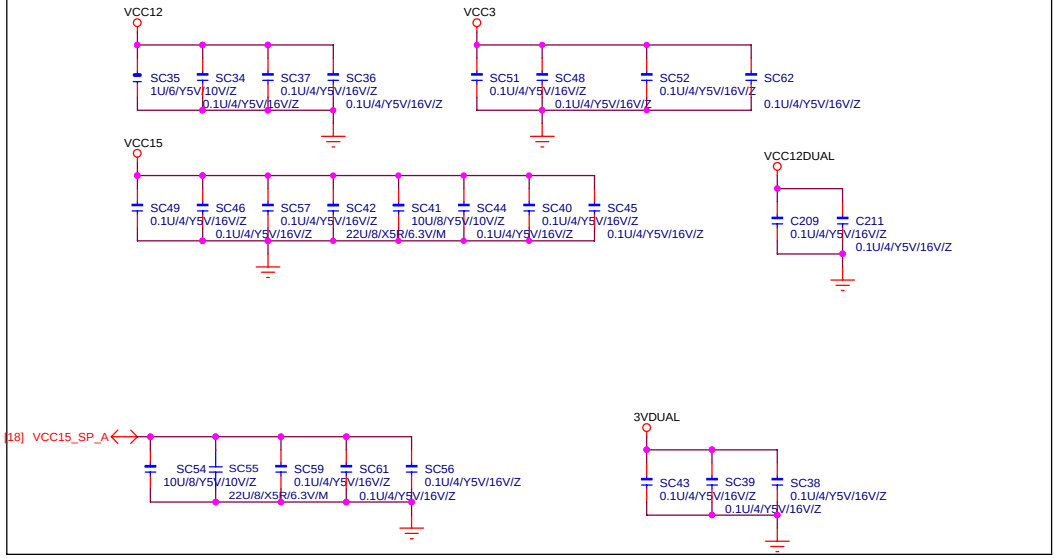
GIGABYTE CORP.

Title: MCP55 PWR/GND

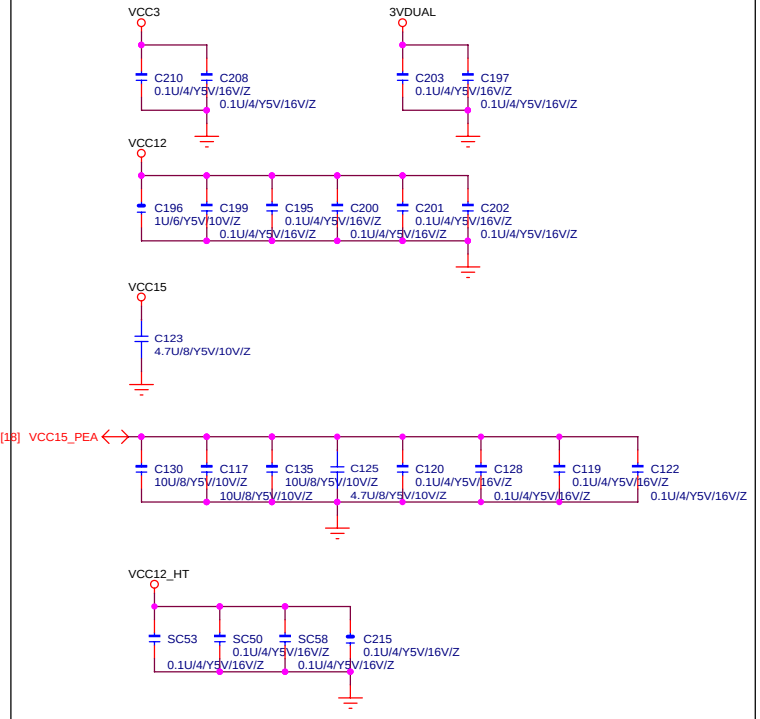
Size: Custom | Document Number: GA-M55S-S3 | Rev: 2.02

Date: 星期二, 一月 09, 2007 | Sheet 18 of 41

MCP55 BACK SIDE DECOUPLING



MCP55 TOP SIDE DECOUPLING



MCP55 INTERNAL PULL-UP/PULL-DOWN

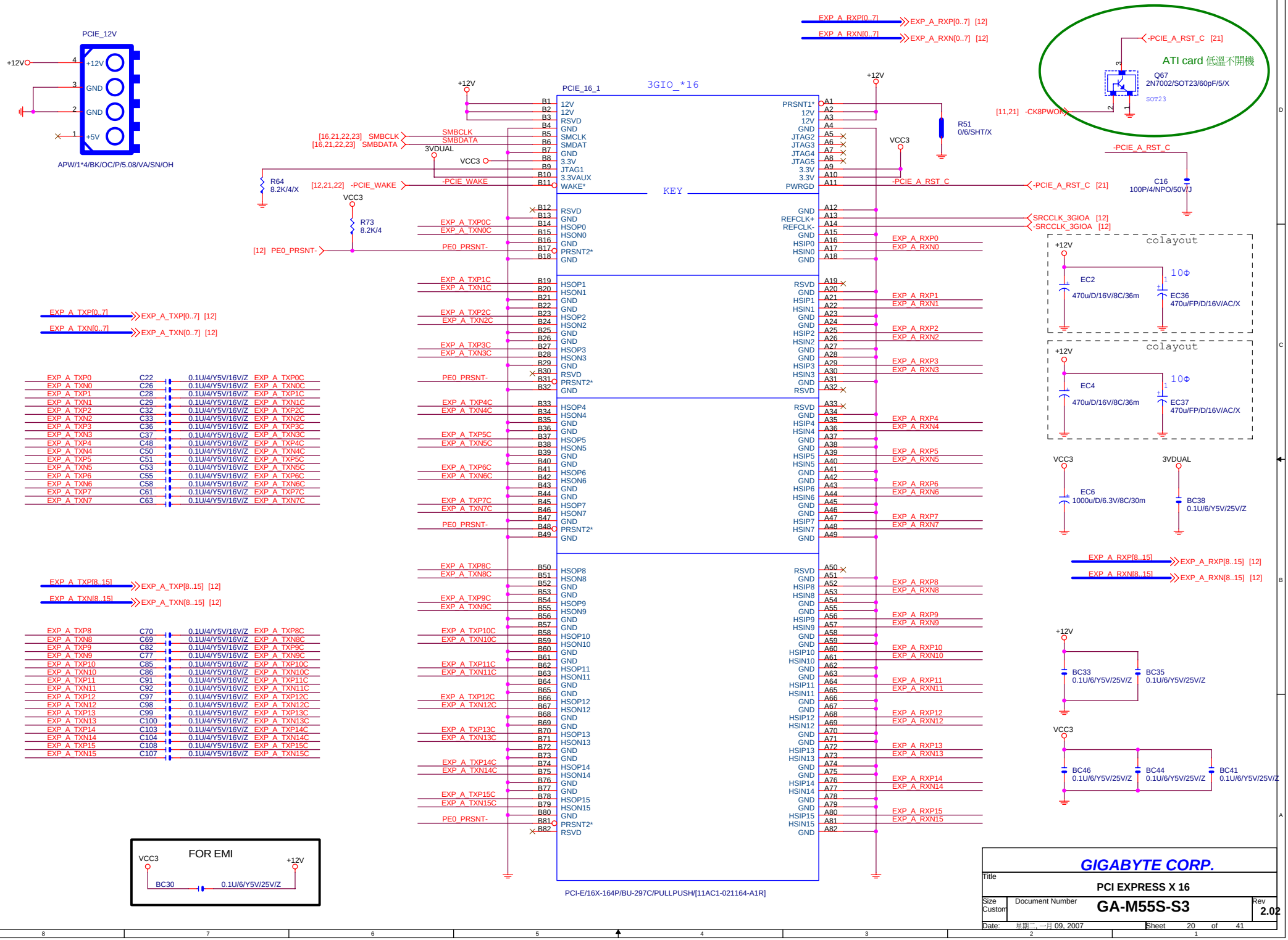
PIN	VOLTAGE
A20GATE/GPIO	+3.3V
EXT_SMI*/GPIO	+3.3V_DUAL
HDA_SDATA_IN0/GPIO_22/MGPIO_0	+3.3V_DUAL/GND
HDA_SDATA_IN1/GPIO_23/MGPIO_1	+3.3V_DUAL/GND
HDA_SDATA_IN2/GPIO_24/MGPIO_2	+3.3V_DUAL/GND
HDA_SDATA_OUT/GPIO_45	+3.3V_DUAL/GND
JTAG_TDI	+3.3V
JTAG_TMS	+3.3V
JTAG_TRST*	GND
KBRDRSTIN*/GPIO	+3.3V
PE_WAKE*	+3.3V_DUAL
SIO_PME*/GPIO	+3.3V_DUAL
THERM*/GPIO	+3.3V

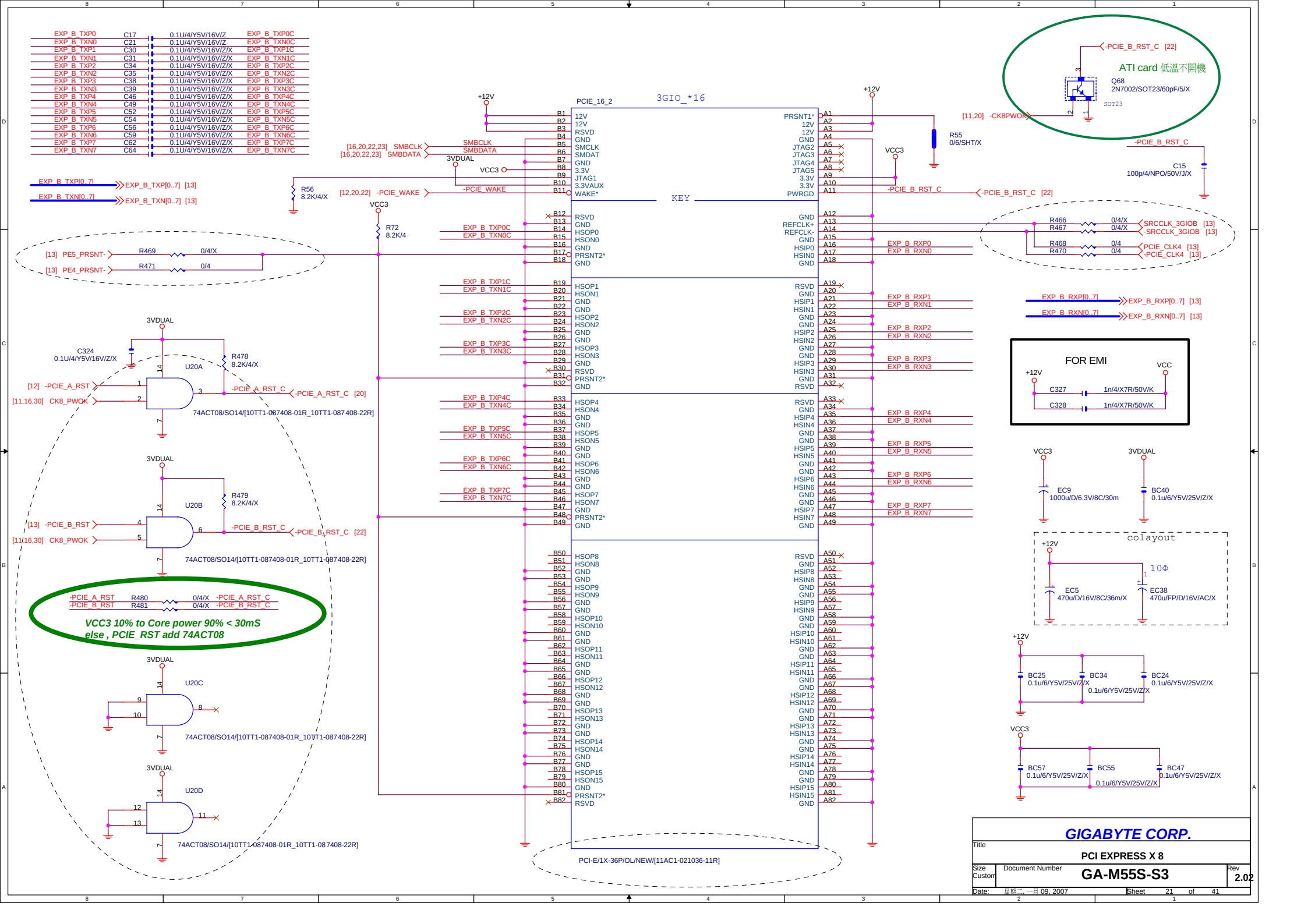
GIGABYTE CORP.

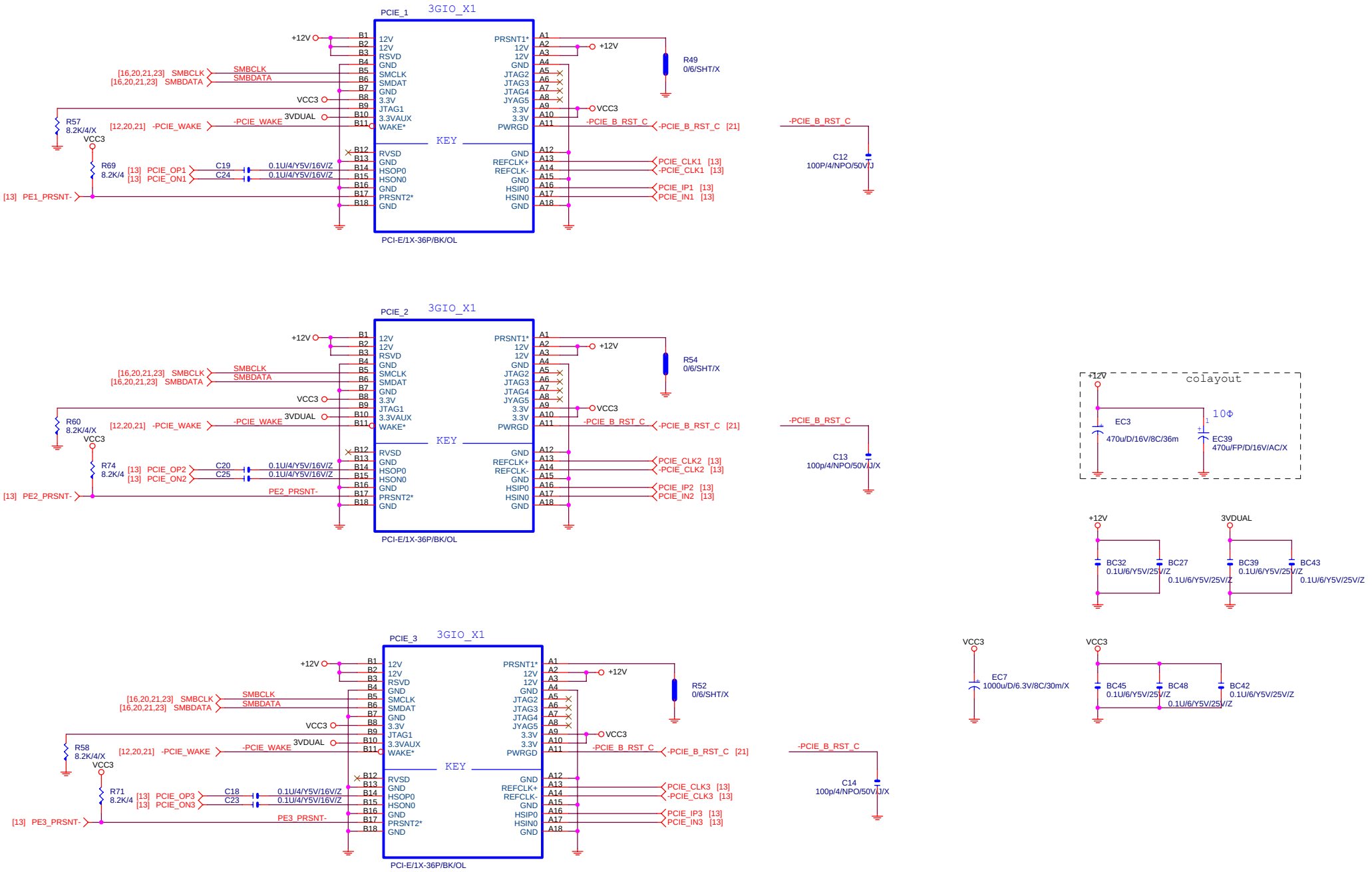
Title: MCP55 DECOUPLING

Size: Custom | Document Number: GA-M55S-S3 | Rev: 2.02

Date: 星期二, 一月 09, 2007 | Sheet 19 of 41

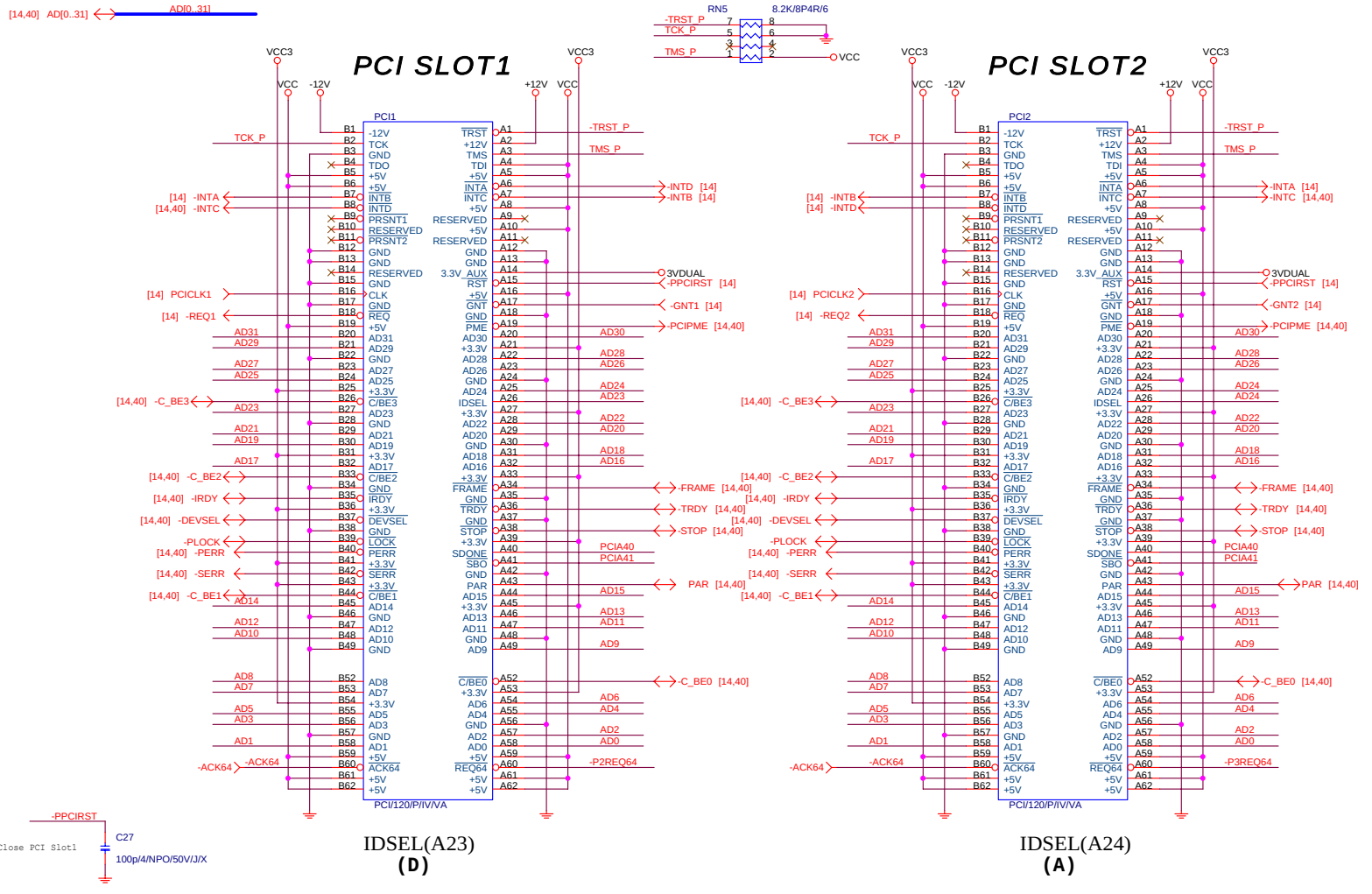

PCIE_12V
+12V
GND
GND
+5V
APW/1*4/BK/OC/P/5.08/VA/SN/OH
PCIE_16_1
3GIO_*16
KEY
EXP_A_RXP[0..7]
EXP_A_RXN[0..7]
EXP_A_TXP[0..7]
EXP_A_TXN[0..7]
EXP_A_TXP[8..15]
EXP_A_TXN[8..15]
SMBCLK
SMBDATA
3VDUAL
-PCIE_WAKE
PE0_PRSNT-
-PCIE_A_RST_C
-CK8PWOK
ATI card 低溫不開機
Q67
2N7002/SOT23/60pF/5/X
R51
0/6/SHT/X
R64
8.2K/4/X
R73
8.2K/4
C16
100P/4/NPO/50V/J
SRCCLK_3GIOA
-SRCCLK_3GIOA
colayout
EC2
470u/D/16V/8C/36m
EC36
470u/FP/D/16V/AC/X
EC4
EC37
EC6
1000u/D/6.3V/8C/30m
BC38
0.1U/6/Y5V/25V/Z
BC33
BC35
BC46
BC44
BC41
FOR EMI
BC30
0.1U/6/Y5V/25V/Z
PCI-E/16X-164P/BU-297C/PULLPUSH/[11AC1-021164-A1R]
GIGABYTE CORP.
PCI EXPRESS X 16
GA-M55S-S3
2.02
星期三, 一月 09, 2007
20
41

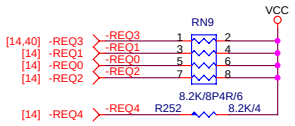

EXP_B_TXP0 C17 0.1U/4/Y5V/16V/Z EXP_B_TXP0C
EXP_B_TXN0 C21 0.1U/4/Y5V/16V/Z EXP_B_TXN0C
EXP_B_TXP1 C30 0.1U/4/Y5V/16V/Z/X EXP_B_TXP1C
EXP_B_TXN1 C31 0.1U/4/Y5V/16V/Z/X EXP_B_TXN1C
EXP_B_TXP2 C34 0.1U/4/Y5V/16V/Z/X EXP_B_TXP2C
EXP_B_TXN2 C35 0.1U/4/Y5V/16V/Z/X EXP_B_TXN2C
EXP_B_TXP3 C38 0.1U/4/Y5V/16V/Z/X EXP_B_TXP3C
EXP_B_TXN3 C39 0.1U/4/Y5V/16V/Z/X EXP_B_TXN3C
EXP_B_TXP4 C46 0.1U/4/Y5V/16V/Z/X EXP_B_TXP4C
EXP_B_TXN4 C49 0.1U/4/Y5V/16V/Z/X EXP_B_TXN4C
EXP_B_TXP5 C52 0.1U/4/Y5V/16V/Z/X EXP_B_TXP5C
EXP_B_TXN5 C54 0.1U/4/Y5V/16V/Z/X EXP_B_TXN5C
EXP_B_TXP6 C56 0.1U/4/Y5V/16V/Z/X EXP_B_TXP6C
EXP_B_TXN6 C59 0.1U/4/Y5V/16V/Z/X EXP_B_TXN6C
EXP_B_TXP7 C62 0.1U/4/Y5V/16V/Z/X EXP_B_TXP7C
EXP_B_TXN7 C64 0.1U/4/Y5V/16V/Z/X EXP_B_TXN7C
EXP_B_TXP[0..7] EXP_B_TXP[0..7] [13]
EXP_B_TXN[0..7] EXP_B_TXN[0..7] [13]
PCIE_16_2
3GIO_*16
KEY
+12V
VCC3
3VDUAL
[16,20,22,23] SMBCLK SMBCLK
[16,20,22,23] SMBDATA SMBDATA
R56 8.2K/4/X
[12,20,22] -PCIE_WAKE -PCIE_WAKE
R72 8.2K/4
[13] PE5_PRSNT- R469 0/4/X
[13] PE4_PRSNT- R471 0/4
C324 0.1U/4/Y5V/16V/Z/X
U20A
[12] -PCIE_A_RST
[11,16,30] CK8_PWOK
-PCIE_A_RST_C
-PCIE_A_RST_C [20]
R478 8.2K/4/X
74ACT08/SO14/[10TT1-087408-01R_10TT1-087408-22R]
U20B
[13] -PCIE_B_RST
[11,16,30] CK8_PWOK
-PCIE_B_RST_C
-PCIE_B_RST_C [22]
R479 8.2K/4/X
-PCIE_A_RST R480 0/4/X -PCIE_A_RST_C
-PCIE_B_RST R481 0/4/X -PCIE_B_RST_C
VCC3 10% to Core power 90% < 30mS
else , PCIE_RST add 74ACT08
U20C
U20D
PCI-E/1X-36P/OL/NEW/[11AC1-021036-11R]
[11,20] -CK8PWOK
R55 0/6/SHT/X
ATI card 低溫不開機
Q68 2N7002/SOT23/60pF/5/X
-PCIE_B_RST_C [22]
C15 100p/4/NPO/50V/J/X
R466 0/4/X SRCCLK_3GIOB [13]
R467 0/4/X -SRCCLK_3GIOB [13]
R468 0/4 PCIE_CLK4 [13]
R470 0/4 -PCIE_CLK4 [13]
EXP_B_RXP[0..7] EXP_B_RXP[0..7] [13]
EXP_B_RXN[0..7] EXP_B_RXN[0..7] [13]
FOR EMI
C327 1n/4/X7R/50V/K
C328 1n/4/X7R/50V/K
EC9 1000u/D/6.3V/8C/30m
BC40 0.1u/6/Y5V/25V/Z/X
colayout
10Φ
EC5 470u/D/16V/8C/36m/X
EC38 470u/FP/D/16V/AC/X
BC25 0.1u/6/Y5V/25V/Z/X
BC34 0.1u/6/Y5V/25V/Z/X
BC24 0.1u/6/Y5V/25V/Z/X
BC57 0.1u/6/Y5V/25V/Z/X
BC55 0.1u/6/Y5V/25V/Z/X
BC47 0.1u/6/Y5V/25V/Z/X
GIGABYTE CORP.
Title
PCI EXPRESS X 8
Size Custom
Document Number
GA-M55S-S3
Rev 2.02
Date: 星期三, 一月 09, 2007
Sheet 21 of 41

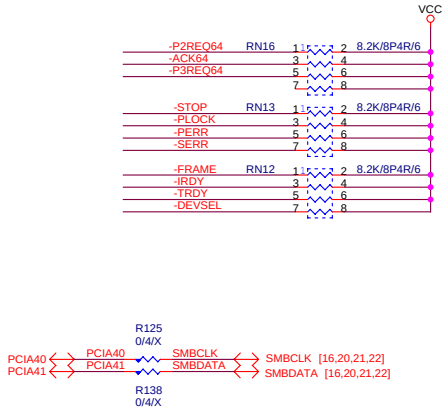


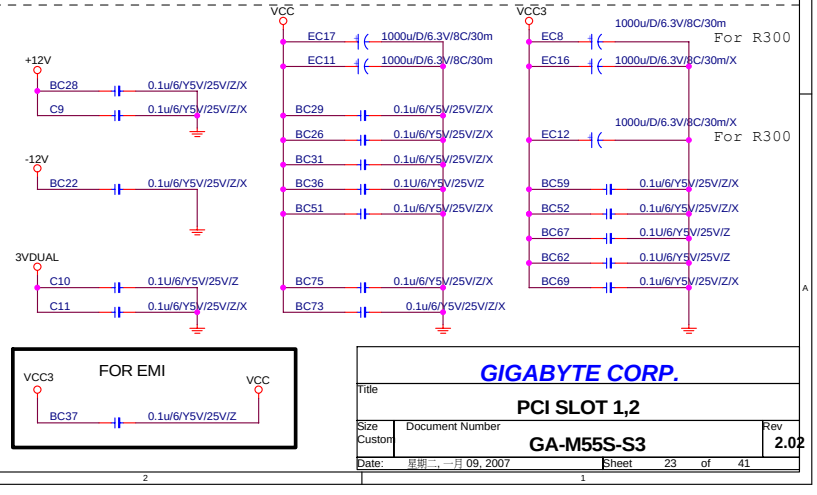
GIGABYTE CORP.		
Title: PCI E SLOT 1, 2		
Size: B	Document Number: GA-M55S-S3	Rev: 2.02
Date: 星期二, 一月 09, 2007	Sheet 22 of 41	

PCI SLOT 1,2



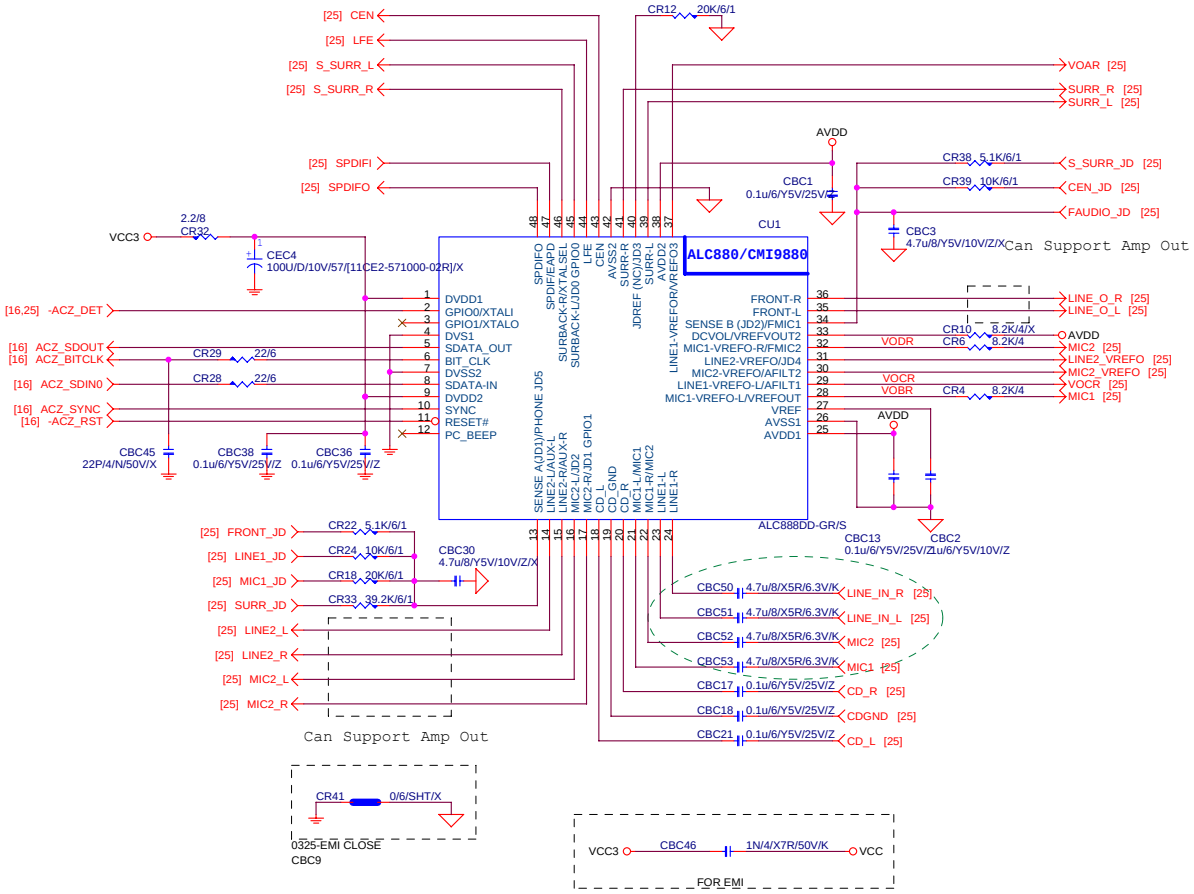






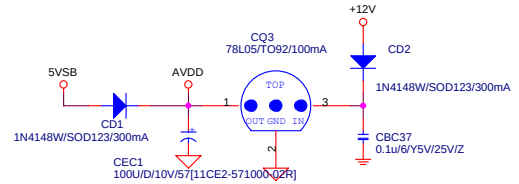
GIGABYTE CORP.		
Title: PCI SLOT 1,2		
Size: Custom	Document Number: GA-M55S-S3	Rev: 2.02
Date: 星期二, 一月 09, 2007	Sheet 23 of 41	

AZALIA CODEC

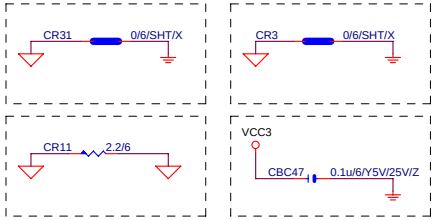


GIGABYTE CORP.		
Title: AZALIA-ALC888		
Size: Custom	Document Number: GA-M55S-S3	Rev: 2.02
Date: 星期二, 一月 09, 2007	Sheet 24 of 41	

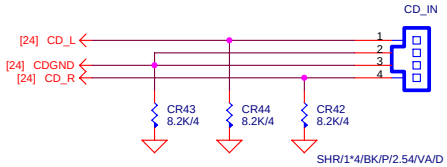
CODEC POWER/EMI PAD

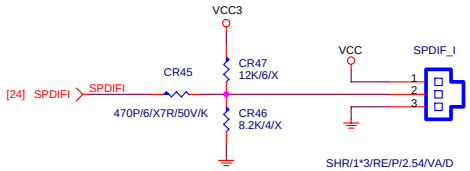


FOR EMI



CD IN





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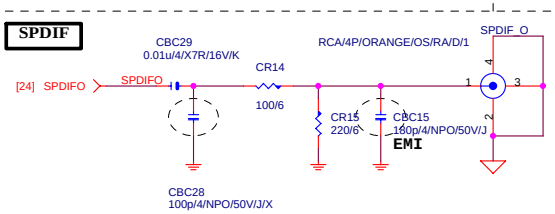
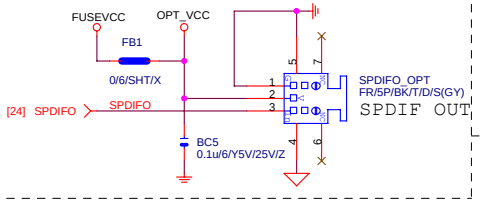
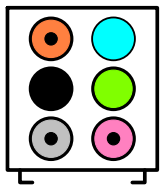




AZALIA JACK

BTX AZALIA CONNECTOR



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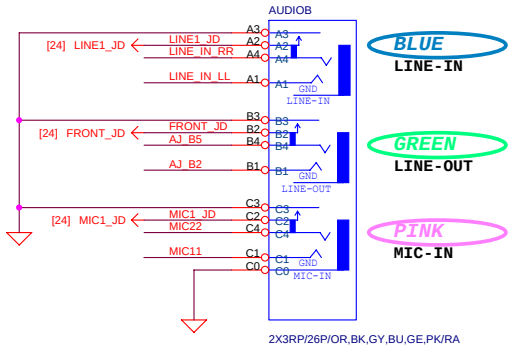
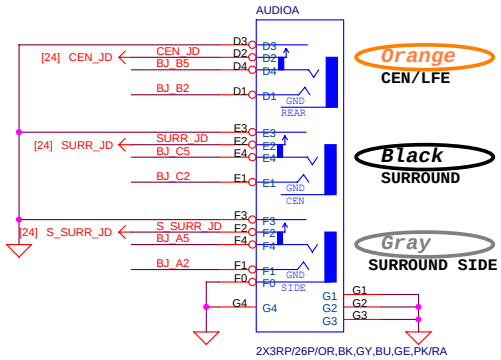
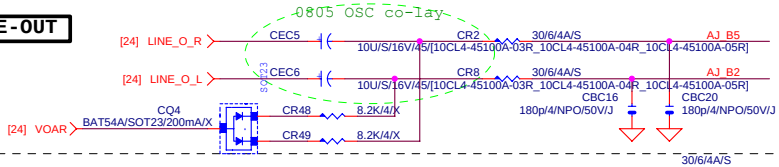
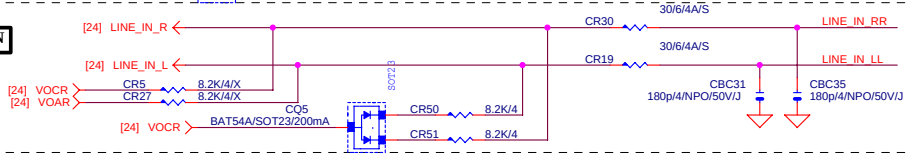




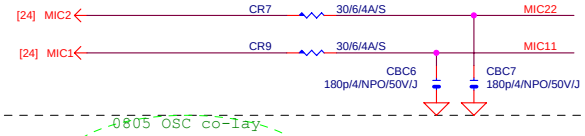
LINE-OUT



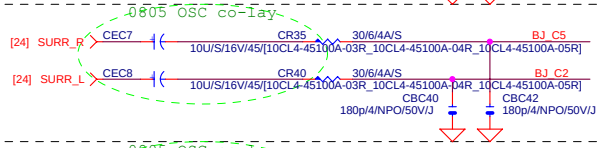
LINE-IN



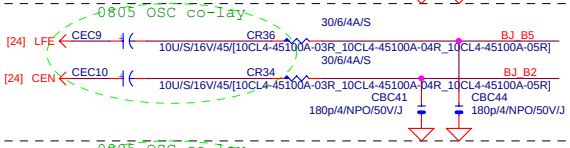
MIC-IN



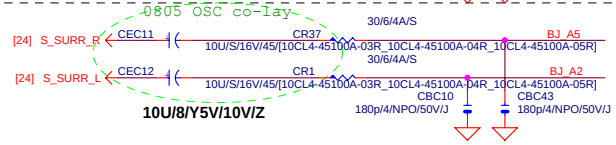
SURROUND



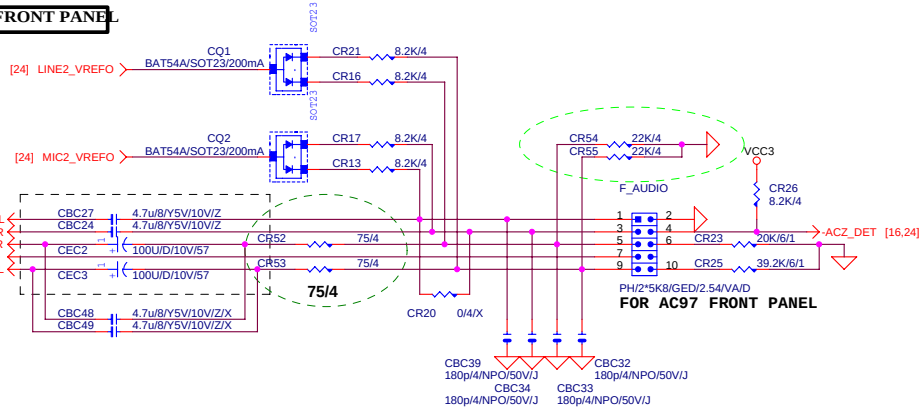
CEN/LFE



SURR BACK

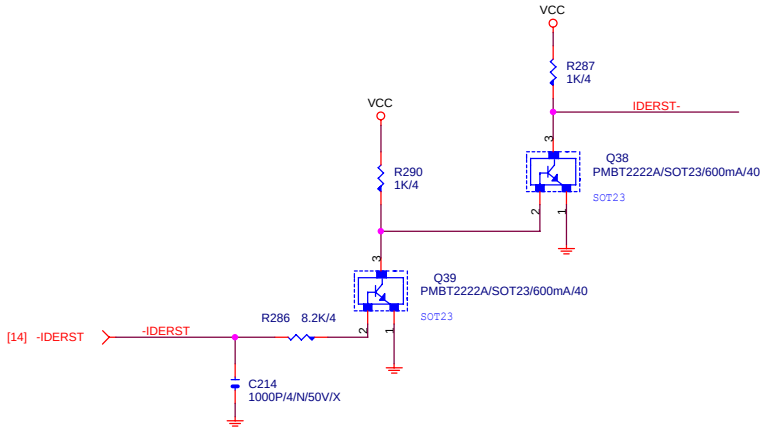


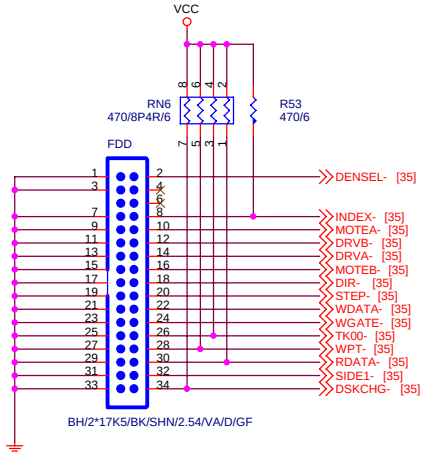
AZALIA FRONT PANEL

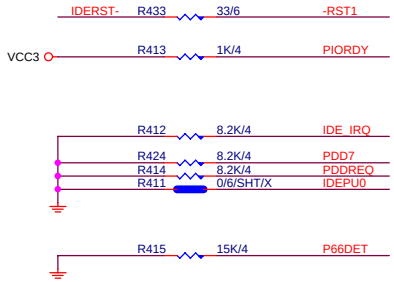


GIGABYTE CORP.

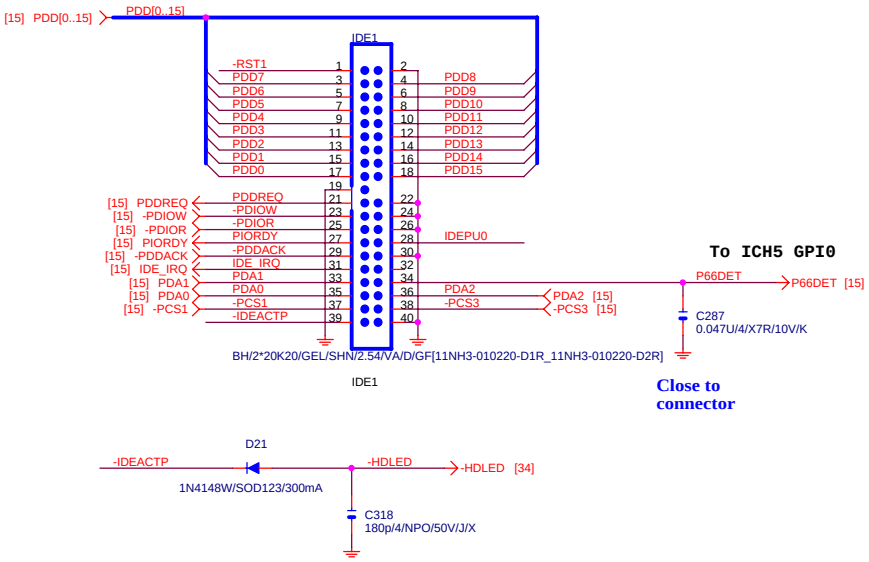
Title	AUDIO JACK	
Size: Custom	Document Number: GA-M55S-S3	Rev: 2.02
Date: 星期二, 一月 09, 2007	Sheet 25 of 41	





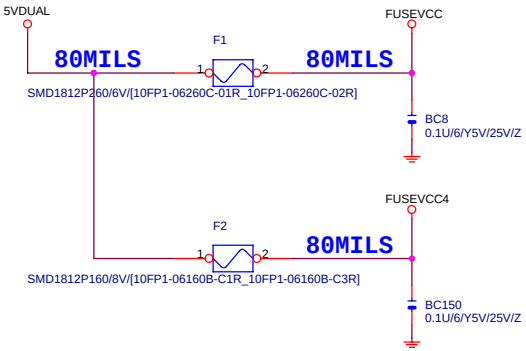


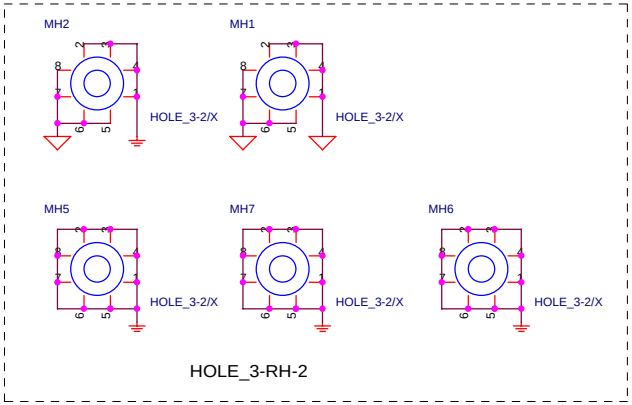
PRIMARY IDE CONNECTOR

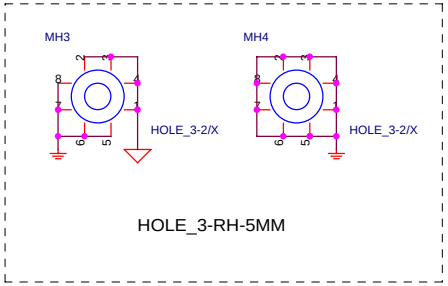


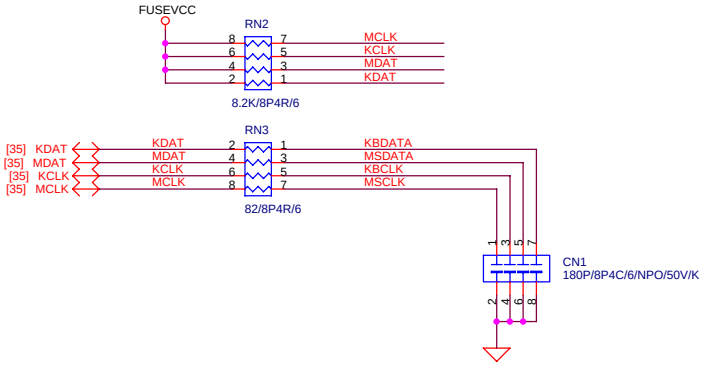
GIGABYTE CORP.

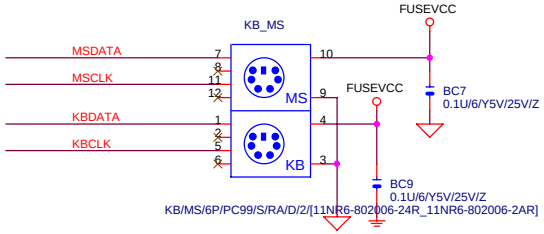
Title: IDE CONNECTOR		
Size: B	Document Number: GA-M55S-S3	Rev: 2.02
Date:	Sheet 26 of 41	



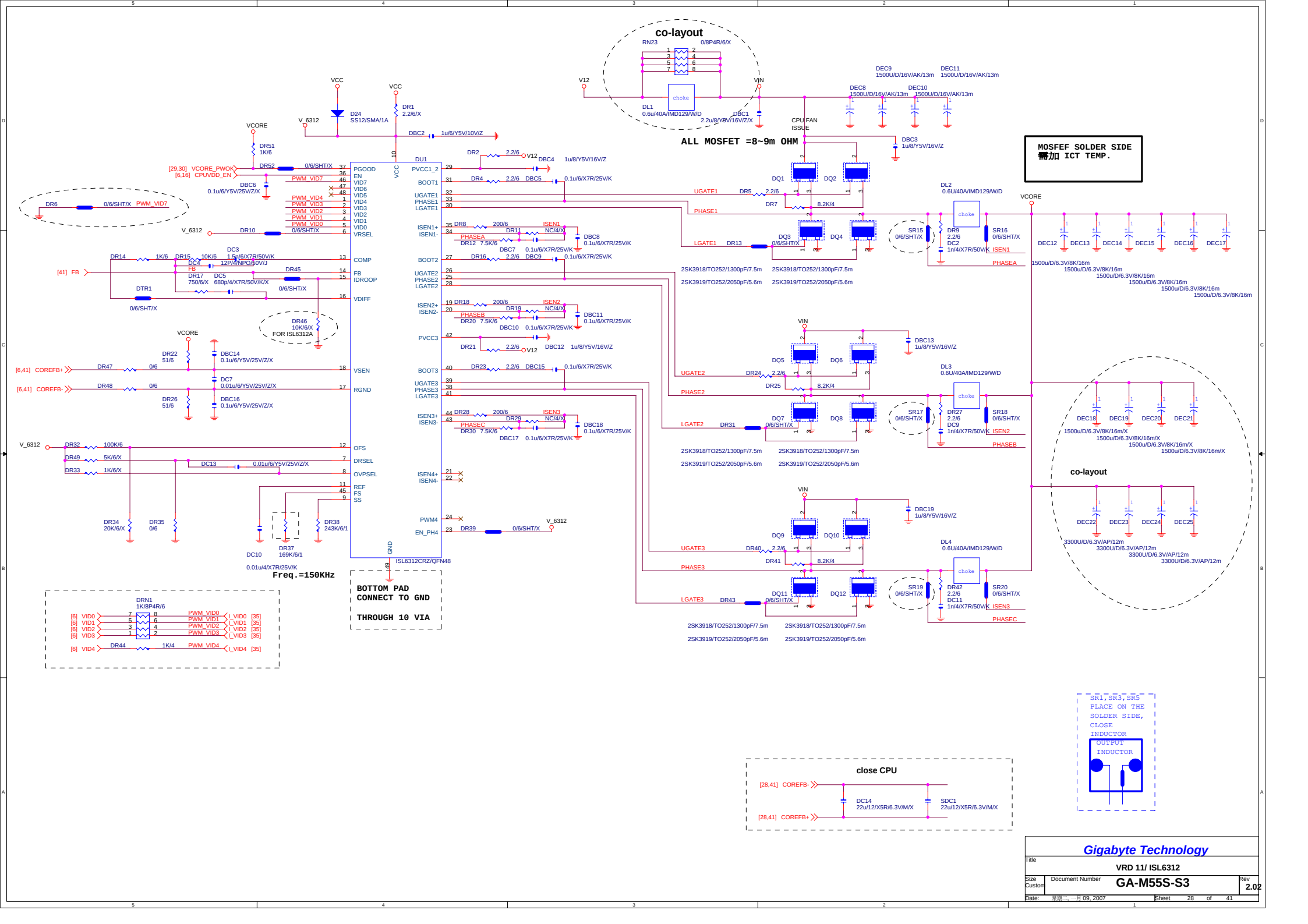


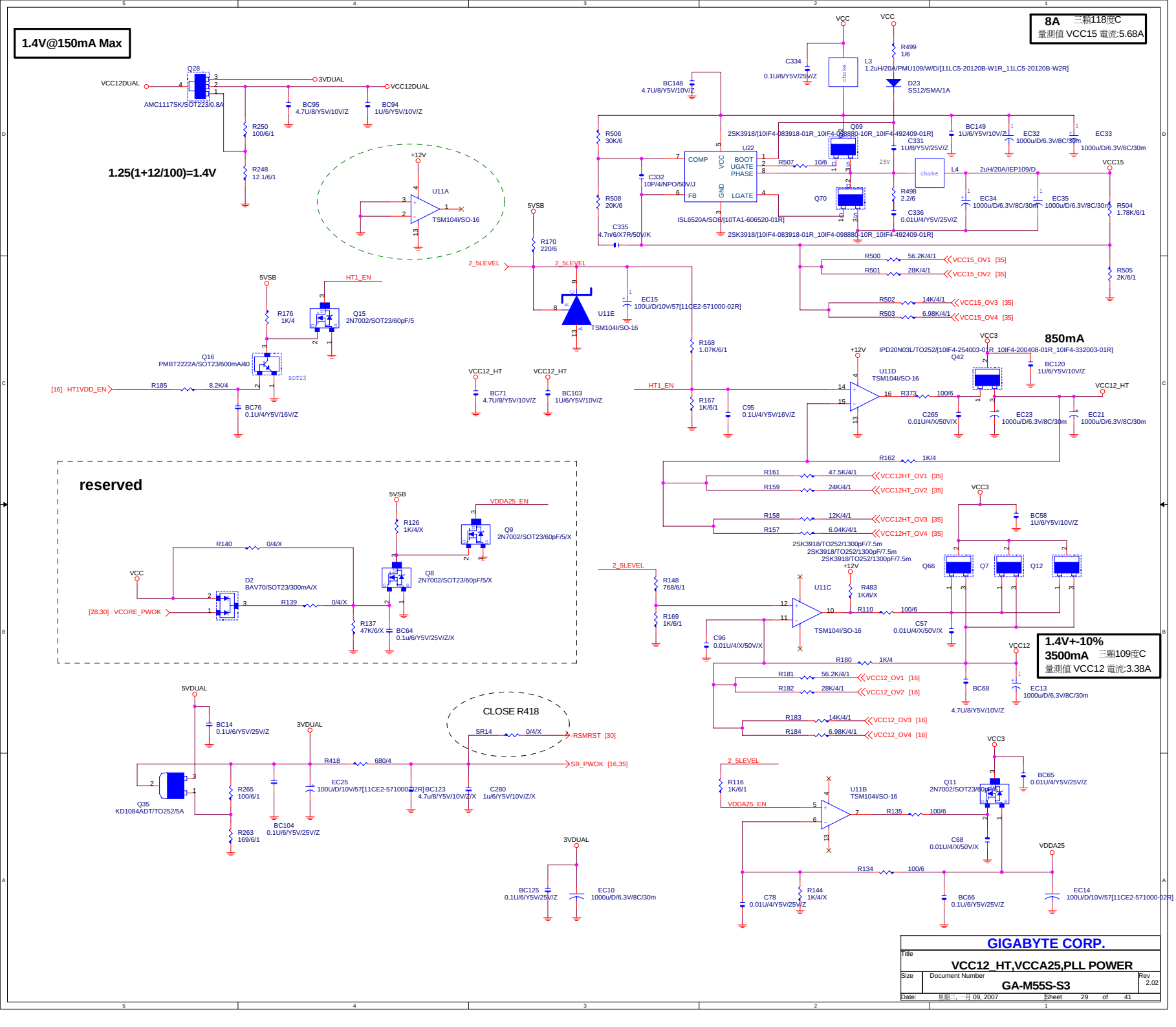


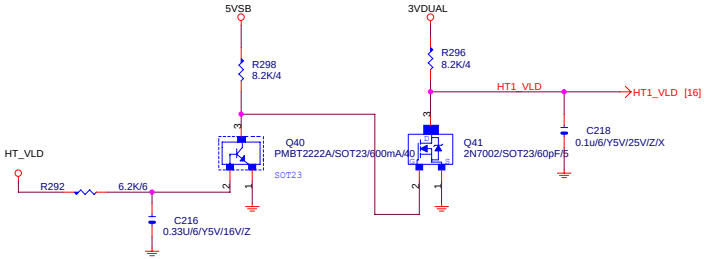


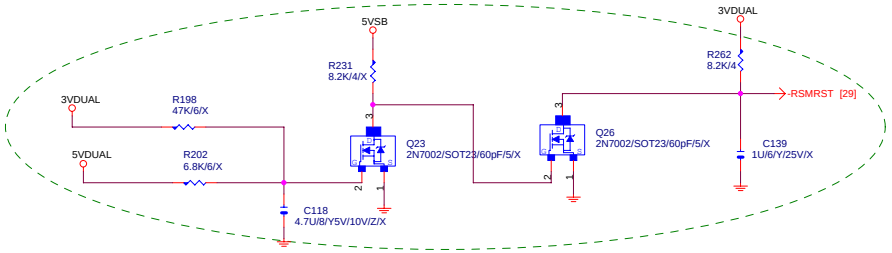


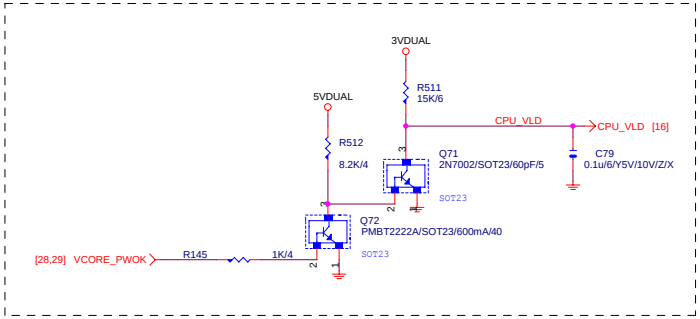
GIGABYTE CORP.		
Title: KB & PS2 MOUSE & IR		
Size: B	Document Number: GA-M55S-S3	Rev: 2.02
Date:	Sheet 27 of 41	

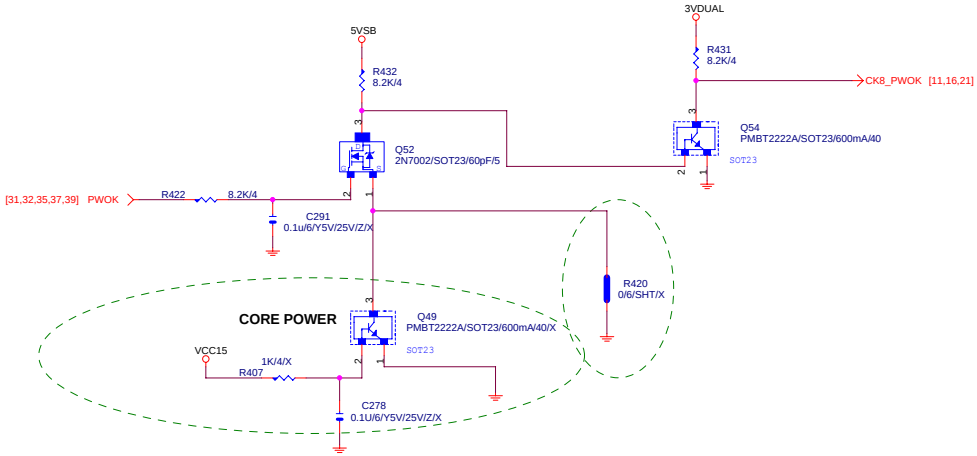

co-layout
RN23
0/8P4R/6/X
V12
VIN
choke
DL1
0.6u/40A/IMD129/W/D
DBC1
2.2u/8/Y5V/16V/Z/X
DEC8
1500U/D/16V/AK/13m
DEC9
1500U/D/16V/AK/13m
DEC10
1500U/D/16V/AK/13m
DEC11
1500U/D/16V/AK/13m
CPU FAN ISSUE
DBC3
1u/8/Y5V/16V/Z
ALL MOSFET =8~9m OHM
MOSFEF SOLDER SIDE
增加 ICT TEMP.
VCC
D24
SS12/SMA/1A
DR1
2.2/6/X
V_6312
DBC2
1u/6/Y5V/10V/Z
VCORE
DR51
1K/6
[29,30] VCORE_PWOK
[6,16] CPUVDD_EN
DR52
0/6/SHT/X
DBC6
0.1u/6/Y5V/25V/Z/X
DR6
0/6/SHT/X
PWM_VID7
PWM_VID4
PWM_VID3
PWM_VID2
PWM_VID1
PWM_VID0
DR10
DU1
PGOOD
EN
VID7
VID6
VID5
VID4
VID3
VID2
VID1
VID0
VRSEL
COMP
FB
IDROOP
VDIFF
VSEN
RGND
OFS
DRSEL
OVPSEL
REF
FS
SS
PVCC1_2
BOOT1
UGATE1
PHASE1
LGATE1
BOOT2
UGATE2
PHASE2
LGATE2
BOOT3
UGATE3
PHASE3
LGATE3
PVCC3
EN_PH4
GND
ISL6312CRZ/QFN48
DR2
2.2/6
DBC4
1u/8/Y5V/16V/Z
DR4
DBC5
0.1u/6/X7R/25V/K
DR8
200/6
DR11
ISEN1
NC/4/X
PHASEA
DR12 7.5K/6
DBC8
DR16
DBC9
DR18
DR19
ISEN2
PHASEB
DR20 7.5K/6
DBC10
DBC11
DR21
DBC12
DR23
DBC15
DR28
DR29
ISEN3
PHASEC
DR30 7.5K/6
DBC17
DBC18
ISEN1+
ISEN1-
ISEN2+
ISEN2-
ISEN3+
ISEN3-
ISEN4+
ISEN4-
PWM4
DR39
V_6312
DR14
1K/6
DR15
10K/6
DC3
1.5n/6/X7R/50V/K
DC4
12P/6/NPO/50V/J
[41] FB
DR17
750/6/X
DC5
680p/4/X7R/50V/K/X
DR45
DTR1
DR46
10K/6/X
FOR ISL6312A
DR22
51/6
DBC14
0.1u/6/Y5V/25V/Z/X
[6,41] COREFB+
DR47
0/6
DC7
0.01u/6/Y5V/25V/Z/X
[6,41] COREFB-
DR48
DR26
51/6
DBC16
0.1u/6/Y5V/25V/Z/X
DR32
100K/6
DR49
5K/6/X
DR33
1K/6/X
DC13
0.01u/6/Y5V/25V/Z/X
DR34
20K/6/X
DR35
0/6
DR37
169K/6/1
DR38
243K/6/1
DC10
0.01u/4/X7R/25V/K
Freq.=150KHz
BOTTOM PAD
CONNECT TO GND
THROUGH 10 VIA
DRN1
1K/8P4R/6
[6] VID0
[6] VID1
[6] VID2
[6] VID3
[6] VID4
DR44
1K/4
I_VID0 [35]
I_VID1 [35]
I_VID2 [35]
I_VID3 [35]
DQ1
DQ2
DR5
2.2/6
DR7
8.2K/4
DL2
0.6U/40A/IMD129/W/D
SR15
0/6/SHT/X
DQ3
DQ4
DR9
2.2/6
DC2
1n/4/X7R/50V/K
SR16
0/6/SHT/X
ISEN1
PHASEA
2SK3918/TO252/1300pF/7.5m
2SK3919/TO252/2050pF/5.6m
DEC12
DEC13
DEC14
DEC15
DEC16
DEC17
1500u/D/6.3V/8K/16m
DQ5
DQ6
DR24
2.2/6
DR25
8.2K/4
DL3
0.6U/40A/IMD129/W/D
SR17
0/6/SHT/X
DQ7
DQ8
DR27
2.2/6
DC9
1n/4/X7R/50V/K
SR18
0/6/SHT/X
ISEN2
PHASEB
DEC18
DEC19
DEC20
DEC21
1500u/D/6.3V/8K/16m/X
DQ9
DQ10
DR40
2.2/6
DR41
8.2K/4
DL4
0.6U/40A/IMD129/W/D
SR19
0/6/SHT/X
DQ11
DQ12
DR42
2.2/6
DC11
1n/4/X7R/50V/K
SR20
0/6/SHT/X
ISEN3
PHASEC
DEC22
DEC23
DEC24
DEC25
3300U/D/6.3V/AP/12m
close CPU
[28,41] COREFB-
[28,41] COREFB+
DC14
22u/12/X5R/6.3V/M/X
SDC1
22u/12/X5R/6.3V/M/X
SR1,SR3,SR5
PLACE ON THE
SOLDER SIDE,
CLOSE
INDUCTOR
OUTPUT
INDUCTOR
Gigabyte Technology
VRD 11/ ISL6312
GA-M55S-S3
2.02
Date: 星期二, 一月 09, 2007
Sheet 28 of 41


1.4V@150mA Max
8A 三顆118度C
量測值 VCC15 電流:5.68A
1.25(1+12/100)=1.4V
850mA
reserved
CLOSE R418
1.4V+-10%
3500mA 三顆109度C
量測值 VCC12 電流:3.38A
GIGABYTE CORP.
VCC12_HT,VCCA25,PLL POWER
GA-M55S-S3
2.02
29 of 41

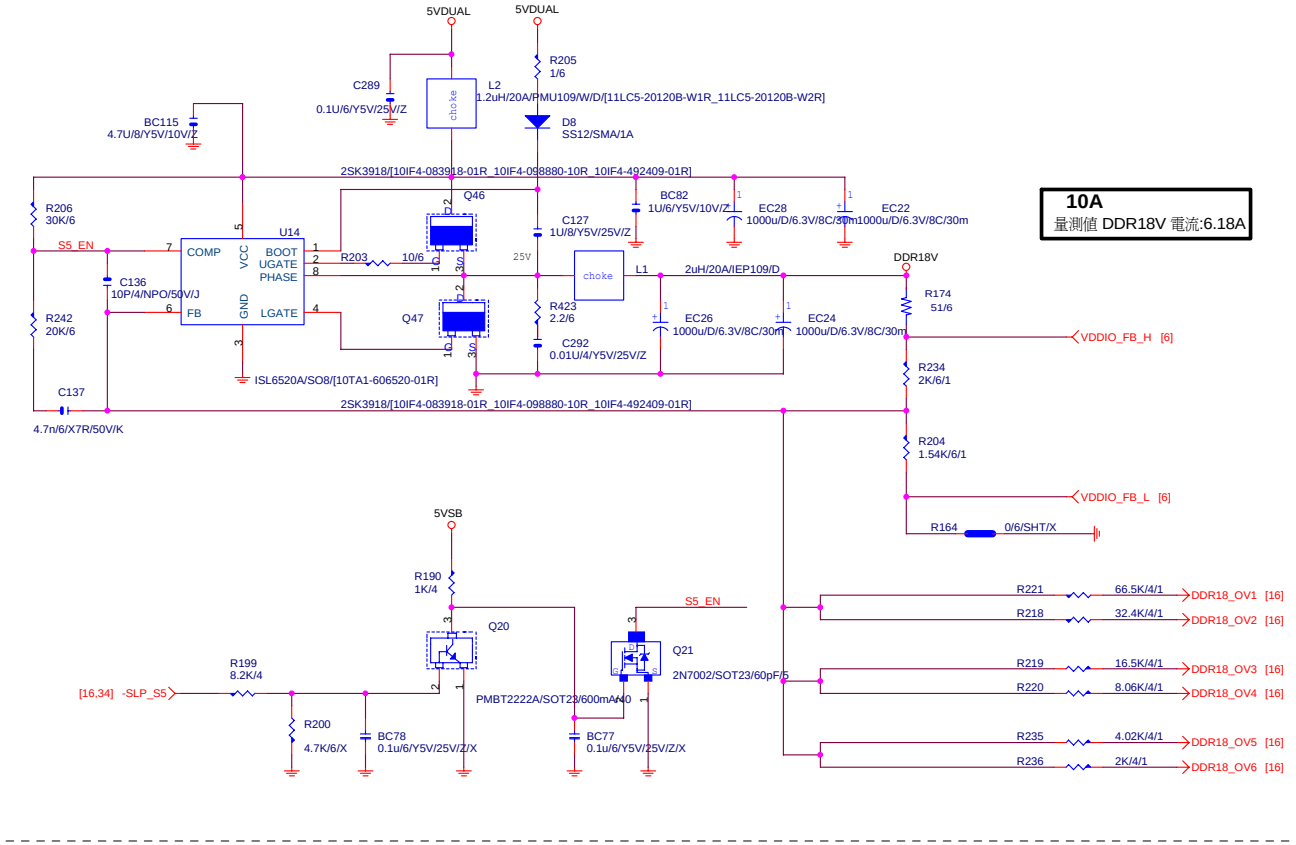


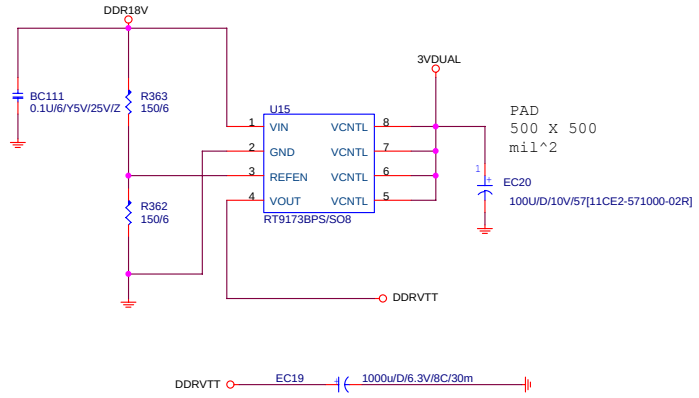


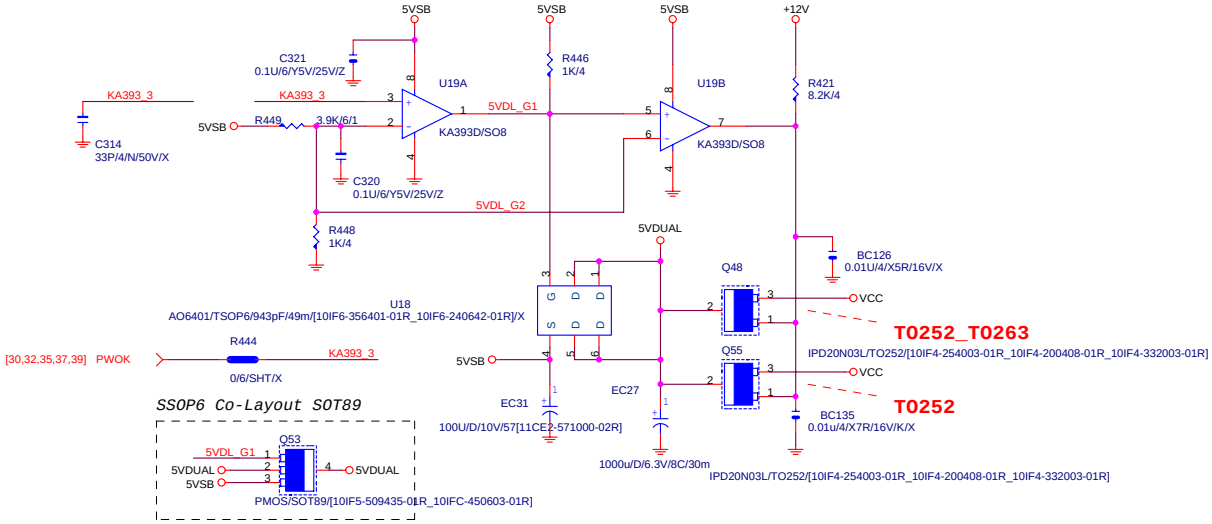


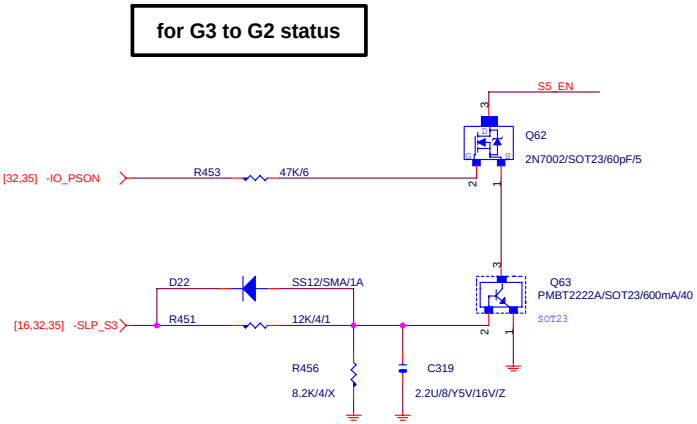


GIGABYTE CORP.		
Title: POWER SEQUENCE POWER		
Size	Document Number: GA-M55S-S3	Rev: 2.02
Date: 星期二, 一月 09, 2007	Sheet 30 of 41	









	G2	S5/S4	S3	S1/S0
-SLP_S5	H	L	H	H
-IO_PSON	H	H	H	L
-SLP_S3	H	L	L	H
DDR18V				

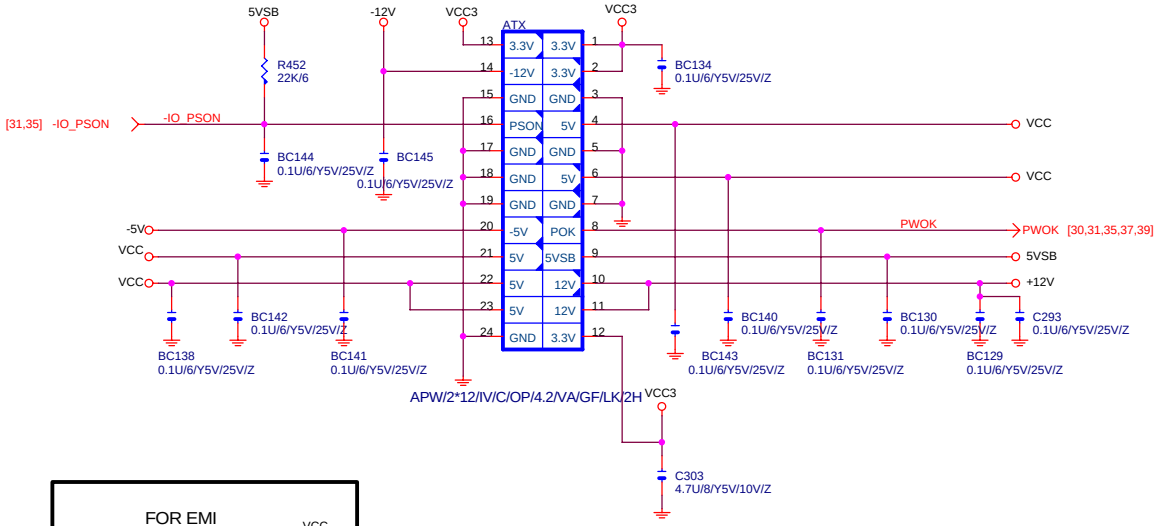
GIGABYTE CORP.

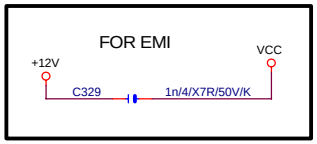
Title: DDR18 , DDRVTT , 5VDUAL

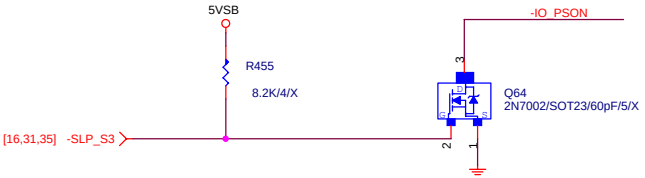
Size: Custom | Document Number: GA-M55S-S3 | Rev: 2.02

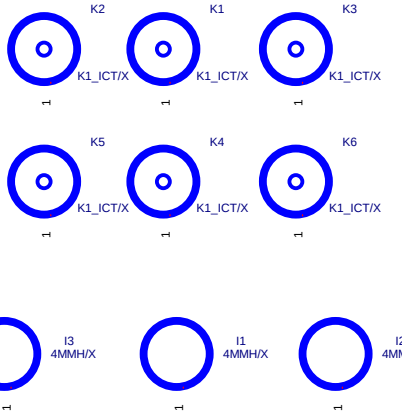
Date: 星期二, 一月 09, 2007 | Sheet 31 of 41

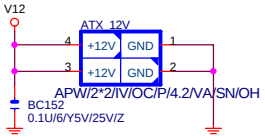
ATX POWER CONNECTOR



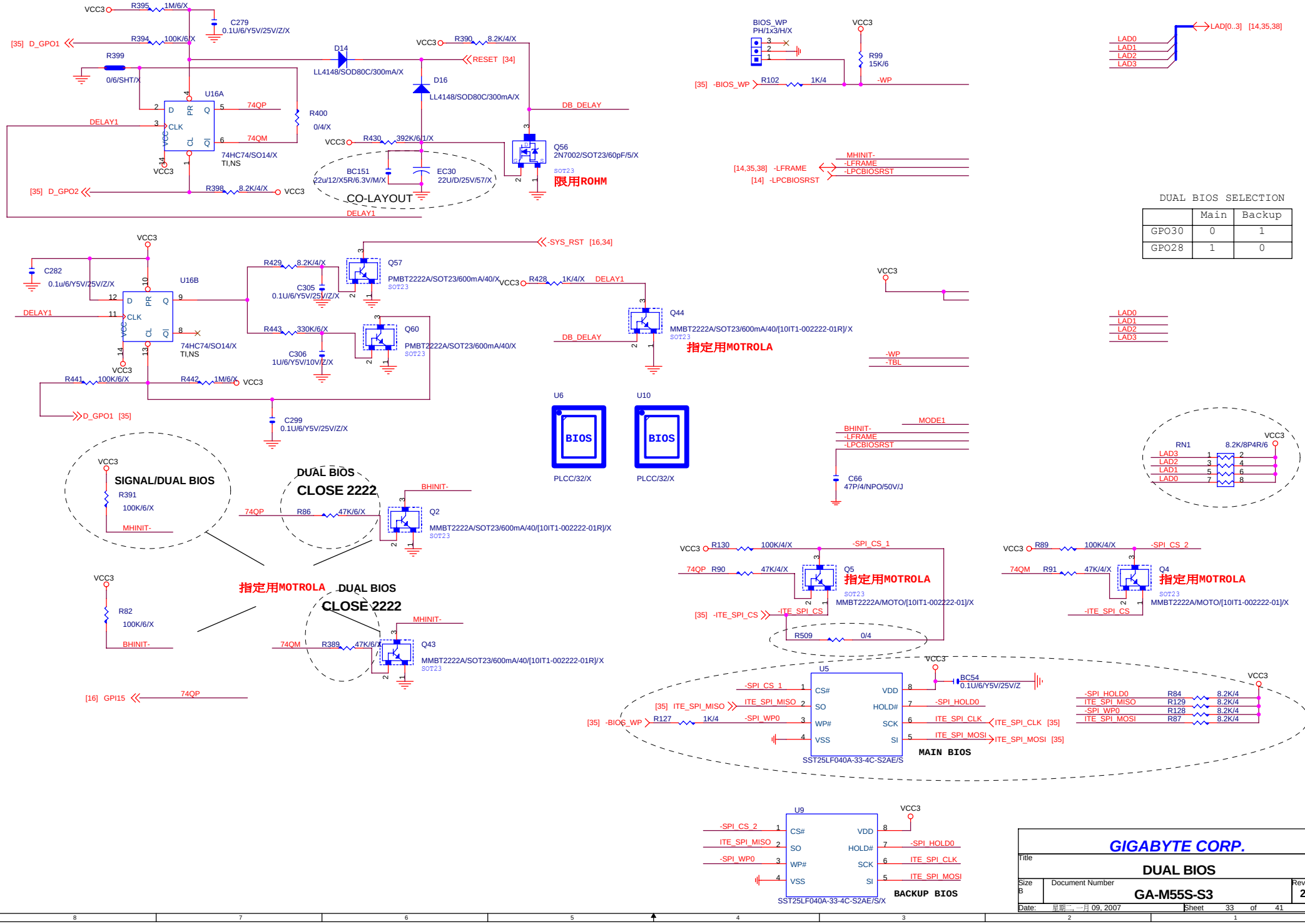


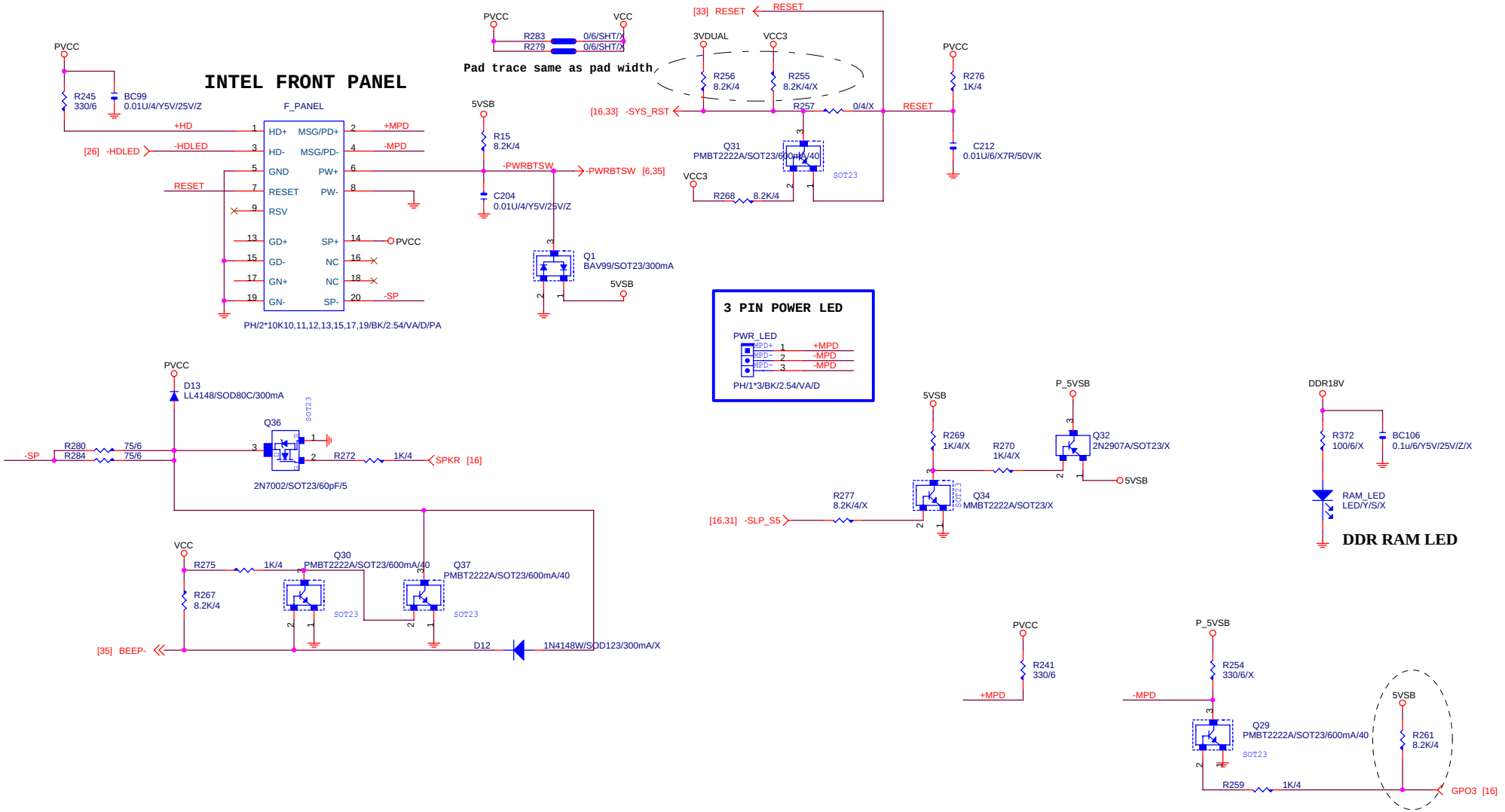




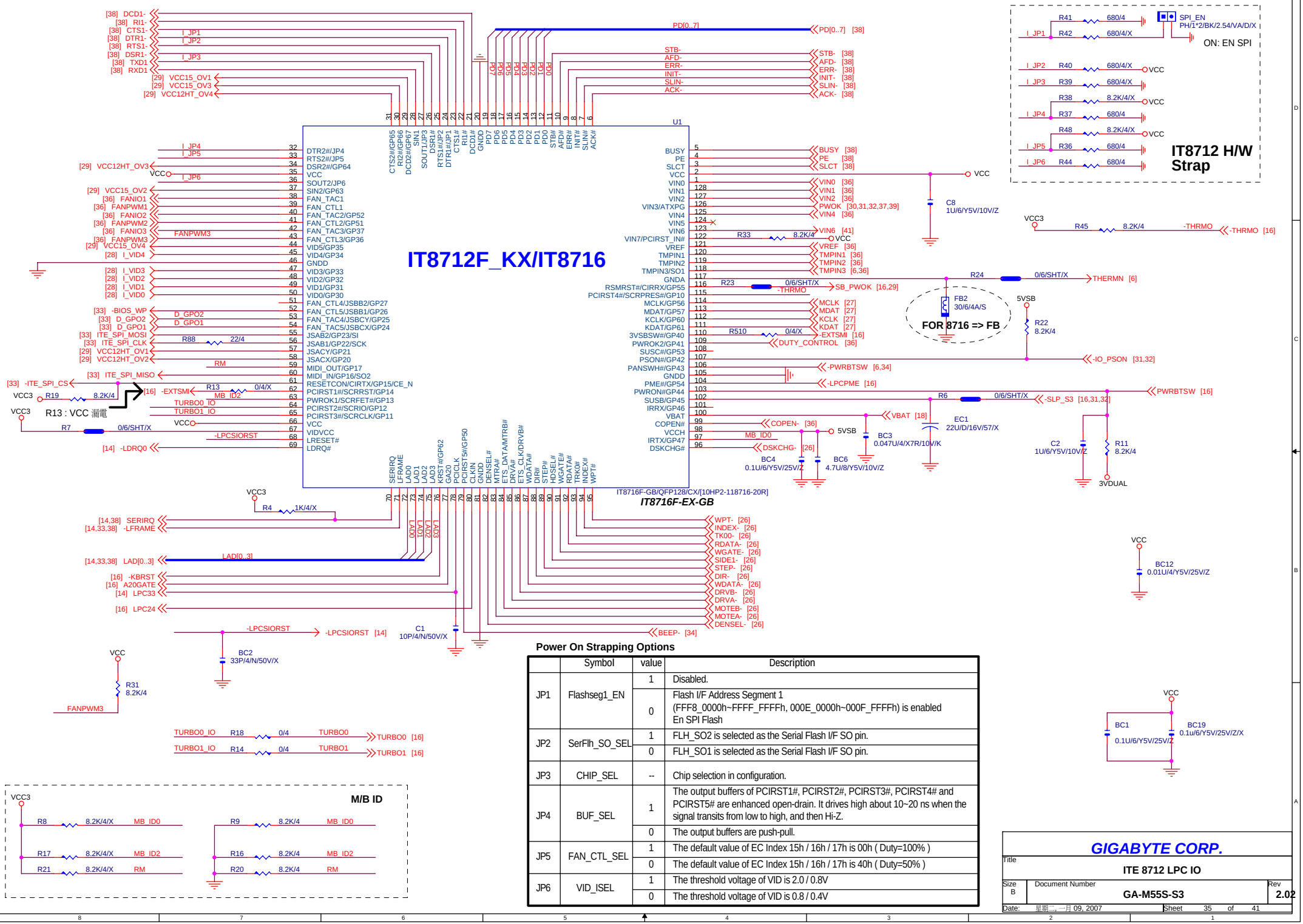


GIGABYTE CORP.		
Title: Misc. PWR & ATX CONN.		
Size: B	Document Number: GA-M55S-S3	Rev: 2.02
Date:	Sheet 32 of 41	


R395 1M/6/X
C279 0.1U/6/Y5V/25V/Z/X
[35] D_GPO1
R394 100K/6/X
R399 0/6/SHT/X
D14 LL4148/SOD80C/300mA/X
VCC3
R390 8.2K/4/X
RESET [34]
D16 LL4148/SOD80C/300mA/X
DB_DELAY
U16A
74QP
74QM
74HC74/SO14/X TI,NS
DELAY1
R400 0/4/X
R430 392K/6/1/X
BC151 22u/12/X5R/6.3V/M/X
EC30 22U/D/25V/57/X
Q56 2N7002/SOT23/60pF/5/X
限用ROHM
CO-LAYOUT
[35] D_GPO2
R398 8.2K/4/X
BIOS_WP PH/1x3/H/X
R99 15K/6
-WP
[35] -BIOS_WP
R102 1K/4
LAD[0..3] [14,35,38]
LAD0
LAD1
LAD2
LAD3
[14,35,38] -LFRAME
[14] -LPCBIOSRST
MHINIT-
-LFRAME
-LPCBIOSRST
DUAL BIOS SELECTION
Main
Backup
GPO30 0 1
GPO28 1 0
C282 0.1u/6/Y5V/25V/Z/X
U16B
74HC74/SO14/X TI,NS
R429 8.2K/4/X
Q57 PMBT2222A/SOT23/600mA/40/X
-SYS_RST [16,34]
C305 0.1U/6/Y5V/25V/Z/X
R428 1K/4/X
Q44 MMBT2222A/SOT23/600mA/40/[10IT1-002222-01R]/X
指定用MOTROLA
R443 330K/6/X
Q60 PMBT2222A/SOT23/600mA/40/X
C306 1U/6/Y5V/10V/Z/X
R441 100K/6/X
R442 1M/6/X
D_GPO1 [35]
C299 0.1U/6/Y5V/25V/Z/X
-WP
-TBL
U6
U10
BIOS
PLCC/32/X
BHINIT-
-LFRAME
-LPCBIOSRST
MODE1
C66 47P/4/NPO/50V/J
RN1 8.2K/8P4R/6
SIGNAL/DUAL BIOS
R391 100K/6/X
MHINIT-
DUAL BIOS CLOSE 2222
74QP
R86 47K/6/X
Q2 MMBT2222A/SOT23/600mA/40/[10IT1-002222-01R]/X
R82 100K/6/X
BHINIT-
指定用MOTROLA
DUAL BIOS CLOSE 2222
74QM
R389 47K/6/X
Q43 MMBT2222A/SOT23/600mA/40/[10IT1-002222-01R]/X
[16] GPI15
R130 100K/4/X
-SPI_CS_1
Q5 MMBT2222A/MOTO/[10IT1-002222-01]/X
[35] -ITE_SPI_CS
-ITE_SPI_CS
R509 0/4
R89 100K/4/X
-SPI_CS_2
Q4 MMBT2222A/MOTO/[10IT1-002222-01]/X
R91 47K/4/X
U5
SST25LF040A-33-4C-S2AE/S
MAIN BIOS
BC54 0.1U/6/Y5V/25V/Z
[35] ITE_SPI_MISO
R127 1K/4
-SPI_WP0
-SPI_HOLD0
ITE_SPI_CLK
ITE_SPI_MOSI
[35] ITE_SPI_CLK
[35] ITE_SPI_MOSI
R84 8.2K/4
R129 8.2K/4
R128 8.2K/4
R87 8.2K/4
U9
SST25LF040A-33-4C-S2AE/S/X
BACKUP BIOS
GIGABYTE CORP.
Title
DUAL BIOS
Size B
Document Number
GA-M55S-S3
Rev 2.02
Date: 星期二, 一月 09, 2007
Sheet 33 of 41

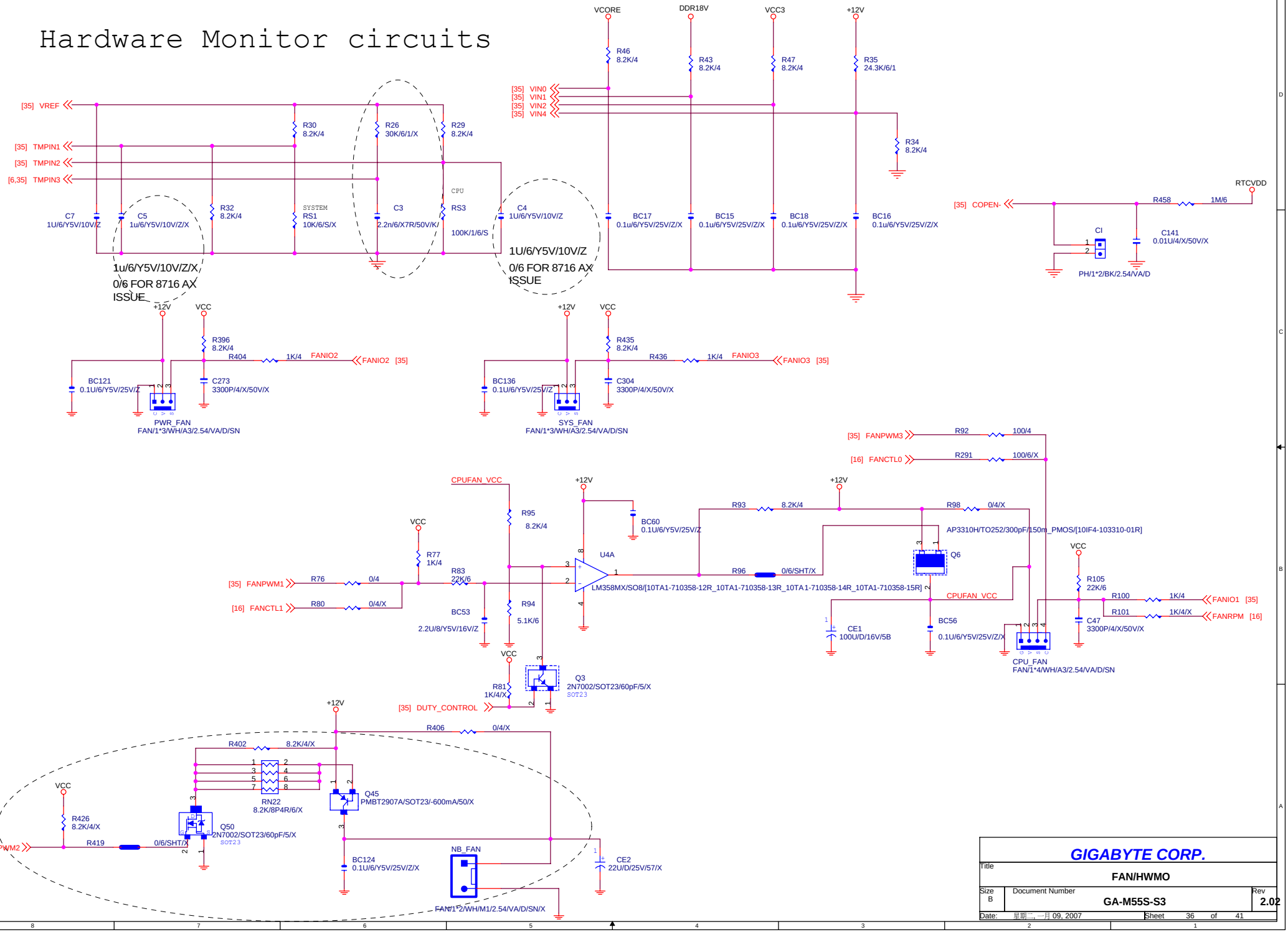


GIGABYTE CORP.		
Title: PANEL & STR LED & RI		
Size: B	Document Number: GA-M55S-S3	Rev: 2.02
Date:	Sheet 34 of 41	



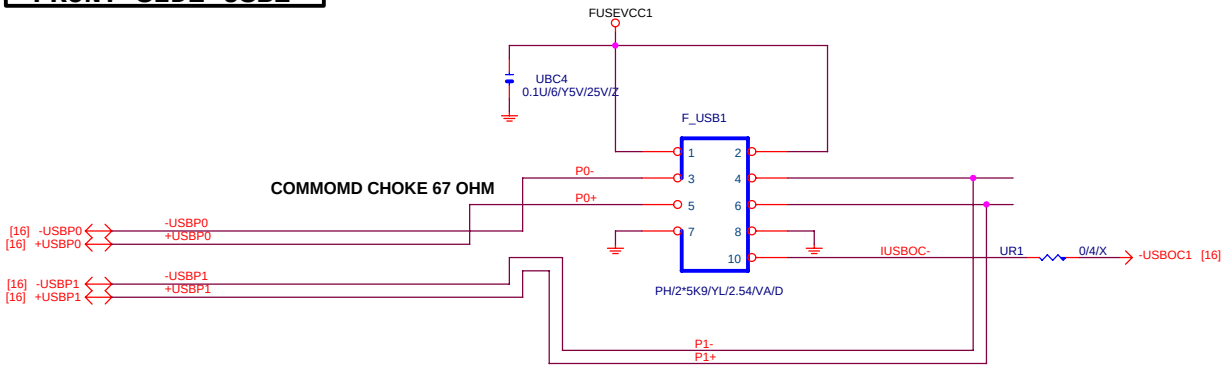
	Symbol	value	Description
JP1	Flashseg1_EN	1	Disabled.
		0	Flash I/F Address Segment 1 (FFF8_0000h~FFFF_FFFFh, 000E_0000h~000F_FFFFh) is enabled En SPI Flash
JP2	SerFlh_SO_SEL	1	FLH_SO2 is selected as the Serial Flash I/F SO pin.
		0	FLH_SO1 is selected as the Serial Flash I/F SO pin.
JP3	CHIP_SEL	--	Chip selection in configuration.
JP4	BUF_SEL	1	The output buffers of PCIRST1#, PCIRST2#, PCIRST3#, PCIRST4# and PCIRST5# are enhanced open-drain. It drives high about 10~20 ns when the signal transits from low to high, and then Hi-Z.
		0	The output buffers are push-pull.
JP5	FAN_CTL_SEL	1	The default value of EC Index 15h / 16h / 17h is 00h (Duty=100%)
		0	The default value of EC Index 15h / 16h / 17h is 40h (Duty=50%)
JP6	VID_ISEL	1	The threshold voltage of VID is 2.0 / 0.8V
		0	The threshold voltage of VID is 0.8 / 0.4V

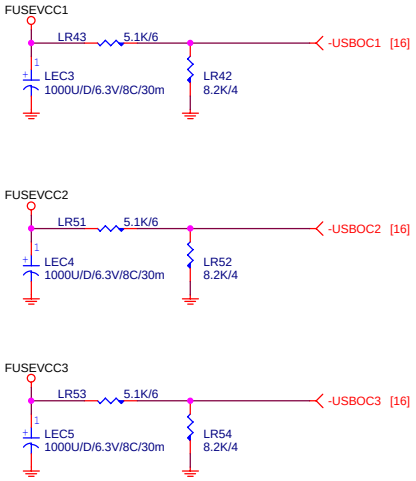
Hardware Monitor circuits

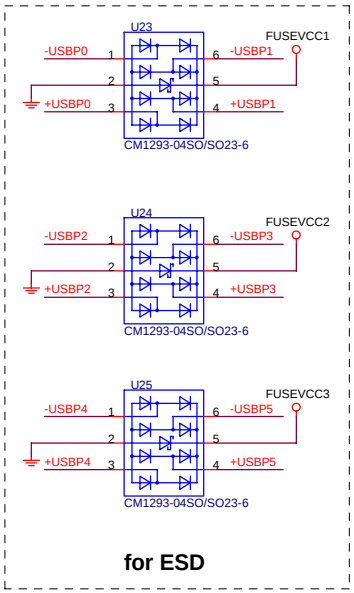


GIGABYTE CORP.		
Title: FAN/HWMO		
Size: B	Document Number: GA-M55S-S3	Rev: 2.02
Date: 星期二, 一月 09, 2007	Sheet 36 of 41	

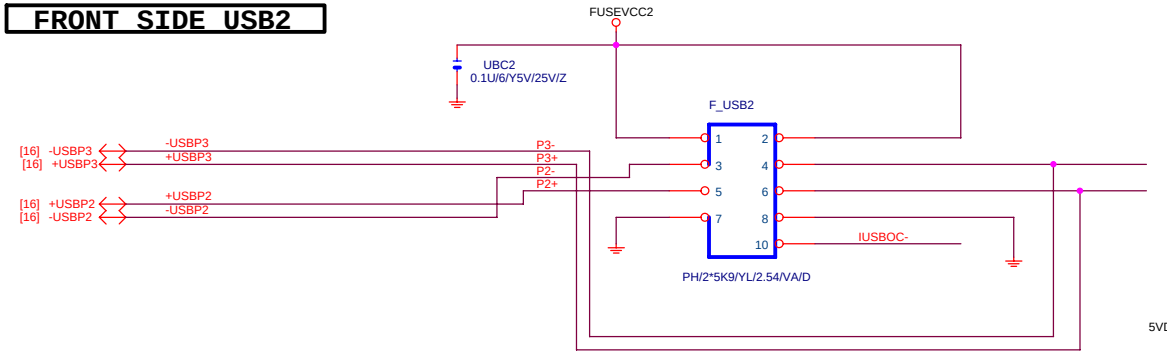
FRONT SIDE USB1

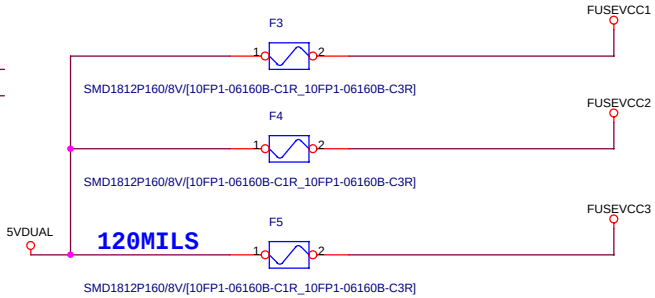




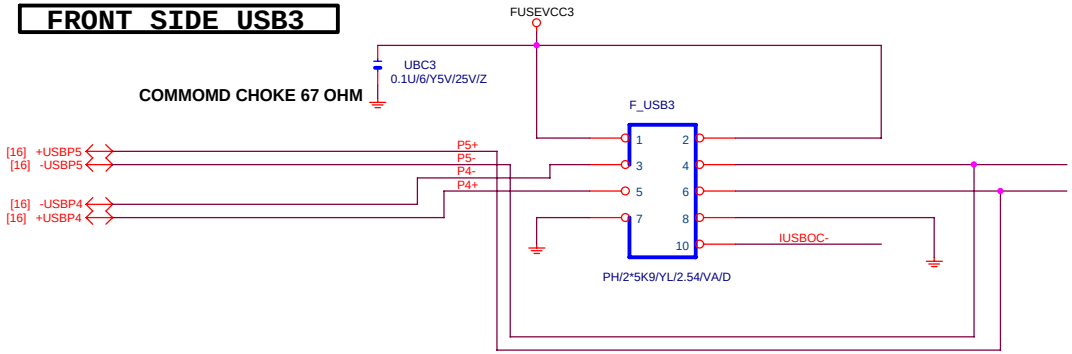


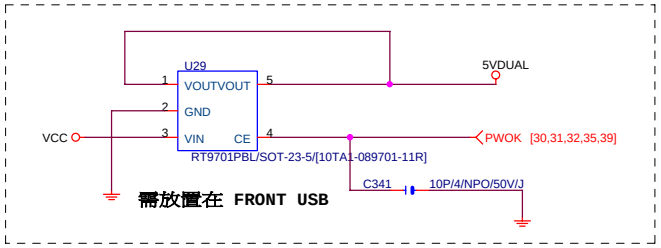
FRONT SIDE USB2

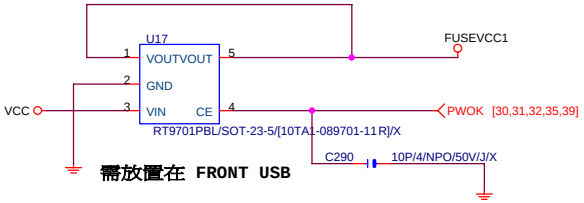


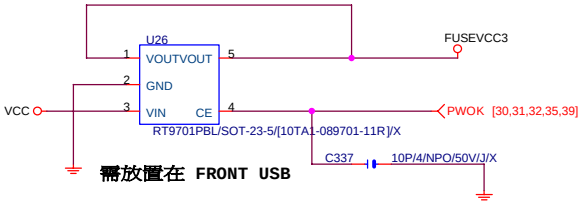


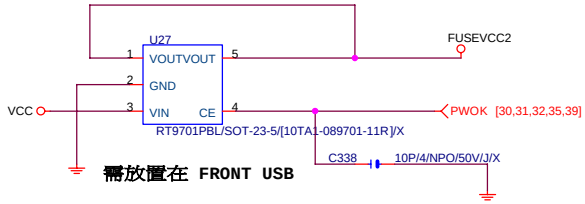
FRONT SIDE USB3





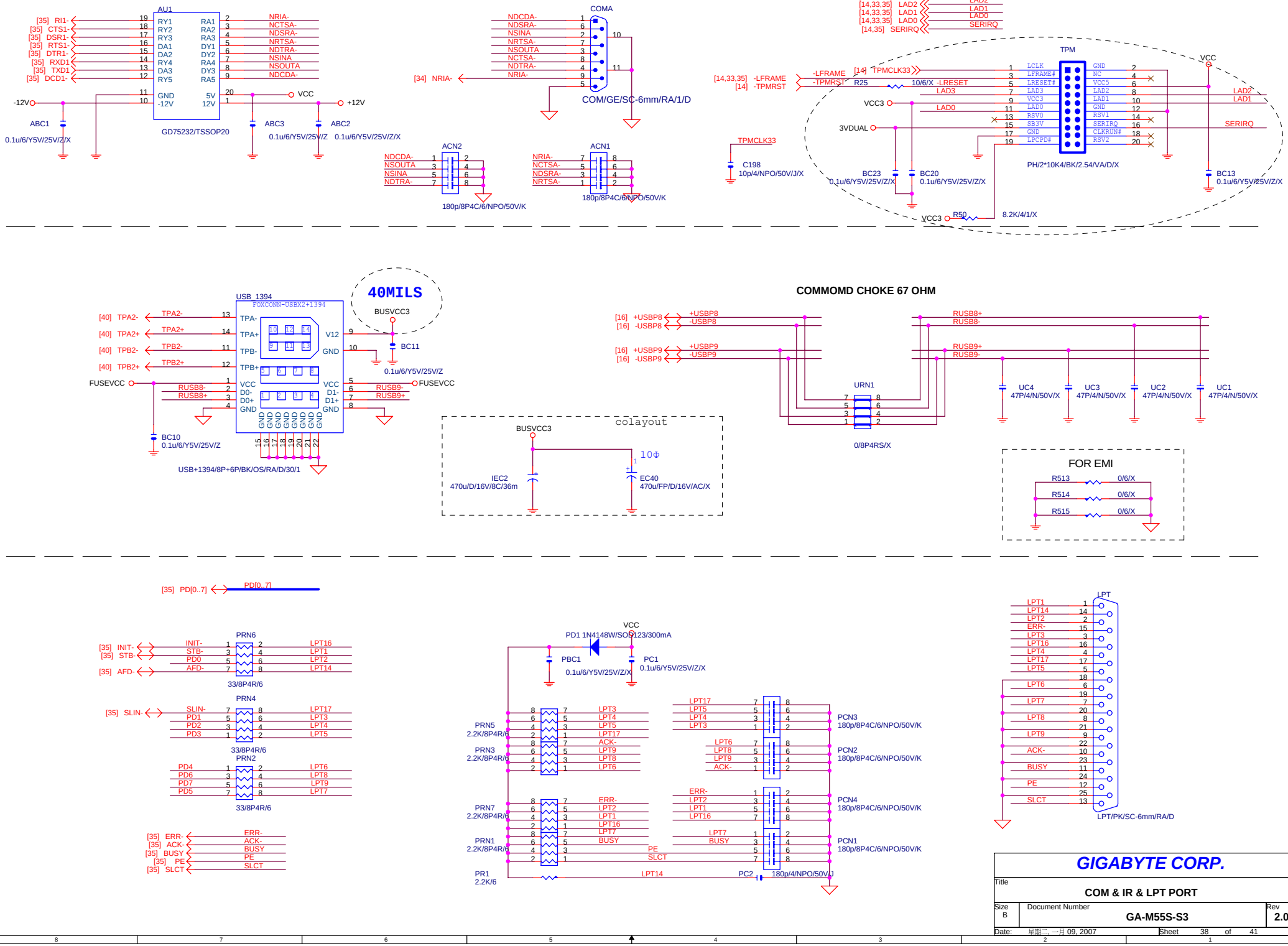






GIGABYTE CORP.

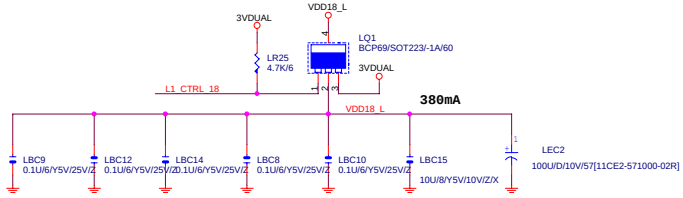
Title: USB PORT		
Size: B	Document Number: GA-M55S-S3	Rev: 2.02
Date:	Sheet 37 of 41	

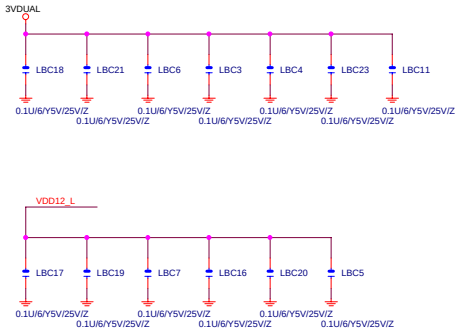

AU1
GD75232/TSSOP20
COMA
COM/GE/SC-6mm/RA/1/D
ACN2
180p/8P4C/6/NPO/50V/K
ACN1
180p/8P4C/6/NPO/50V/K
TPM
PH/2*10K4/BK/2.54/VA/D/X
ABC1
ABC2
ABC3
0.1u/6/Y5V/25V/Z/X
C198
10p/4/NPO/50V/J/X
BC23
BC20
BC13
R50
8.2K/4/1/X
USB_1394
FOXCONN-USBX2+1394
USB+1394/8P+6P/BK/OS/RA/D/30/1
40MILS
BUSVCC3
BC11
BC10
FUSEVCC
COMMOMD CHOKE 67 OHM
URN1
0/8P4RS/X
UC4
UC3
UC2
UC1
47P/4/N/50V/X
colayout
IEC2
470u/D/16V/8C/36m
EC40
470u/FP/D/16V/AC/X
FOR EMI
R513
R514
R515
0/6/X
PRN6
PRN4
PRN2
33/8P4R/6
PD1 1N4148W/SOD123/300mA
PBC1
PC1
PRN5
PRN3
PRN7
PRN1
2.2K/8P4R/6
PCN3
PCN2
PCN4
PCN1
180p/8P4C/6/NPO/50V/K
PR1
2.2K/6
PC2
180p/4/NPO/50V/J
LPT
LPT/PK/SC-6mm/RA/D
GIGABYTE CORP.
COM & IR & LPT PORT
GA-M55S-S3
2.02
星期二, 一月 09, 2007
38 of 41

E1116 use external 2.5V single power supply.
1.8V create by PNP and 1.2V use internal reg.

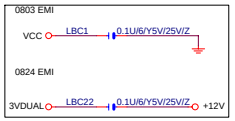
Hardware Configuration: See config _0:4

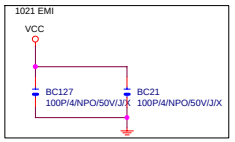
1. PHY address:00001
2. ENA_XC:Enable Auto-Crossover
3. RGMII_TX:Transmit clock not internally delayed
4. RGMII_RX:Receive clock transition when data transitions
5. Advertise all capabilities



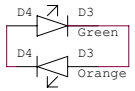


Bypass cap can share. User check it by layout consideration.

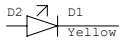


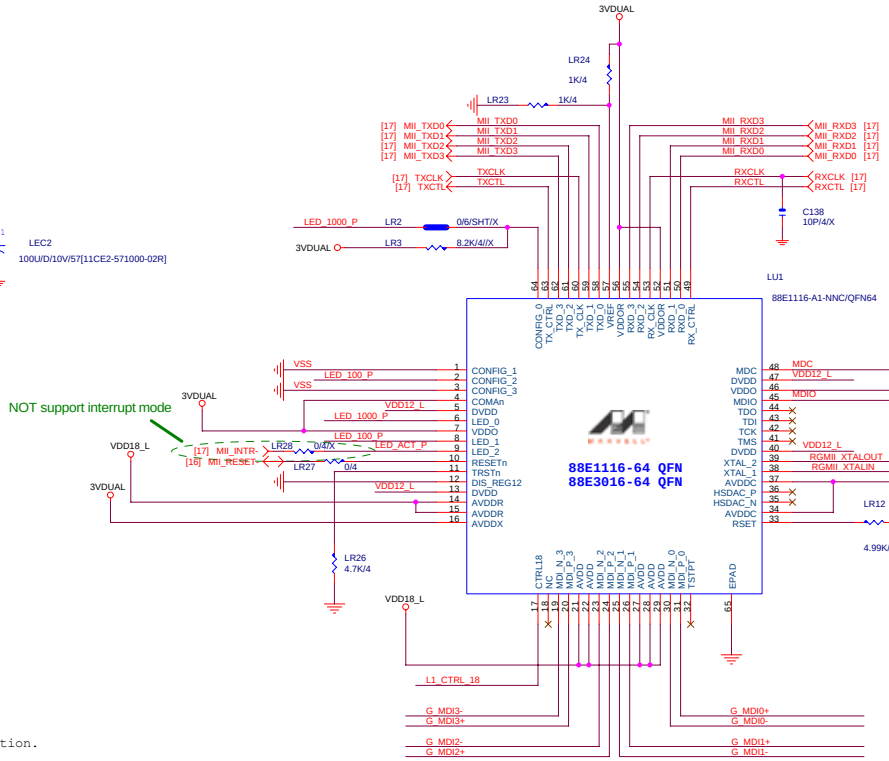


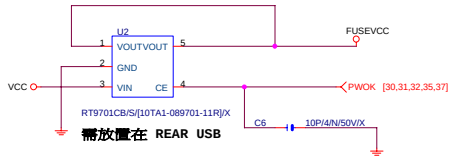
Dual Color LED



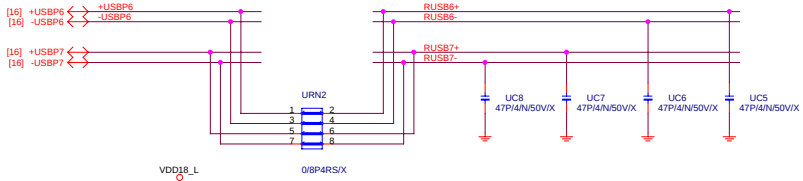
Single Color LED

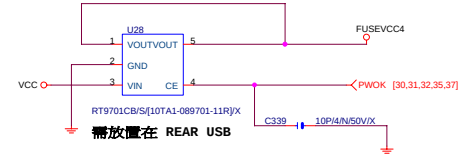


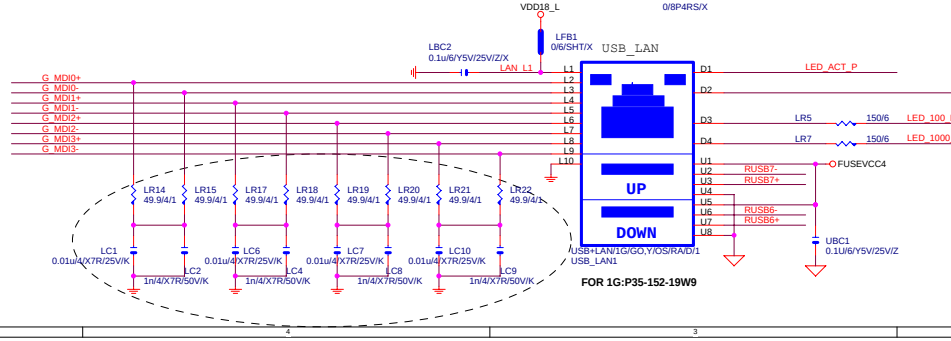


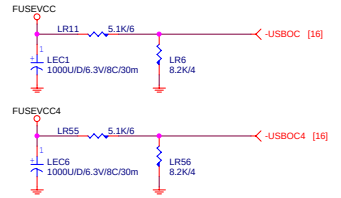


COMMOMD CHOKE 67 OHM

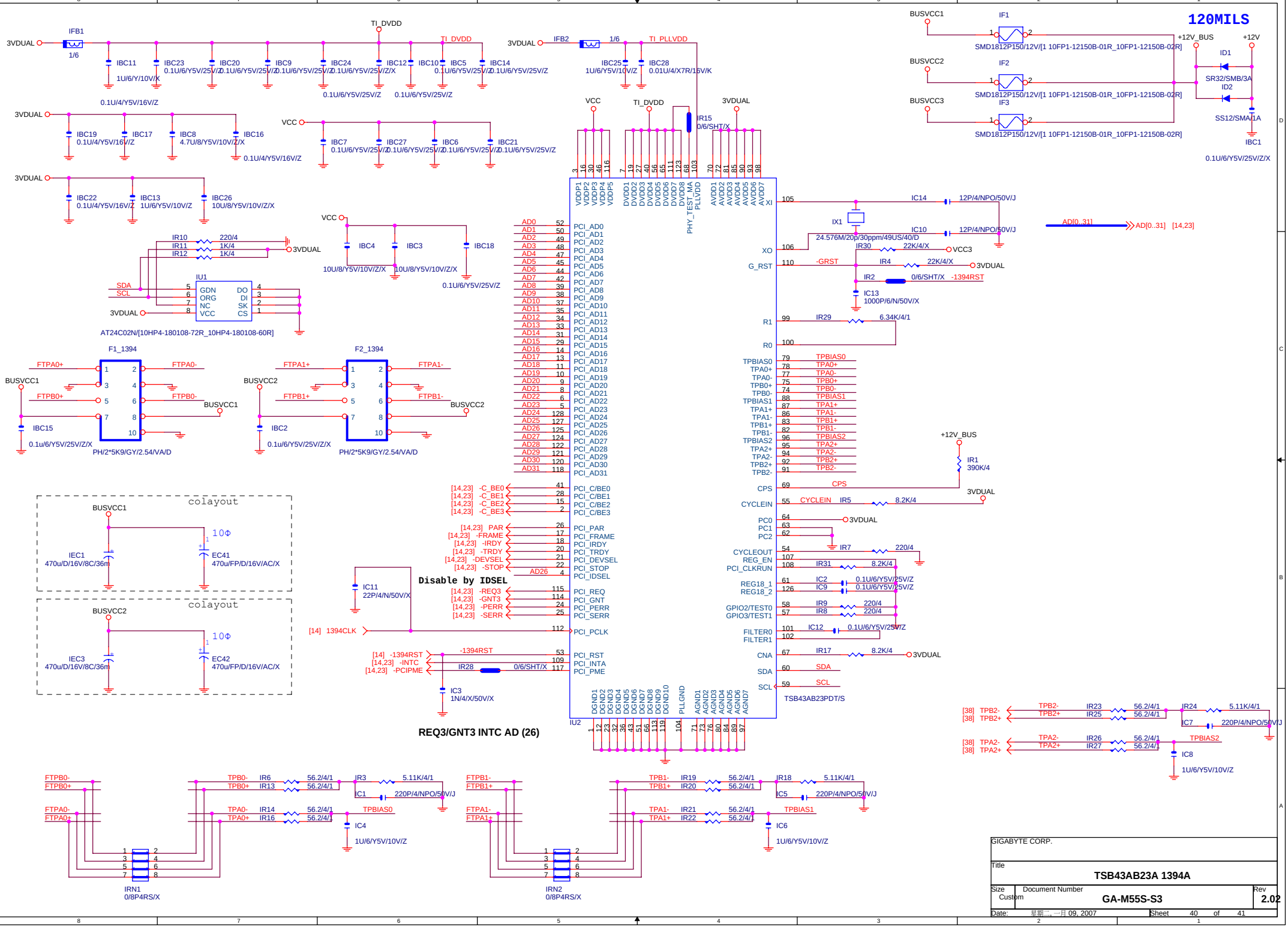


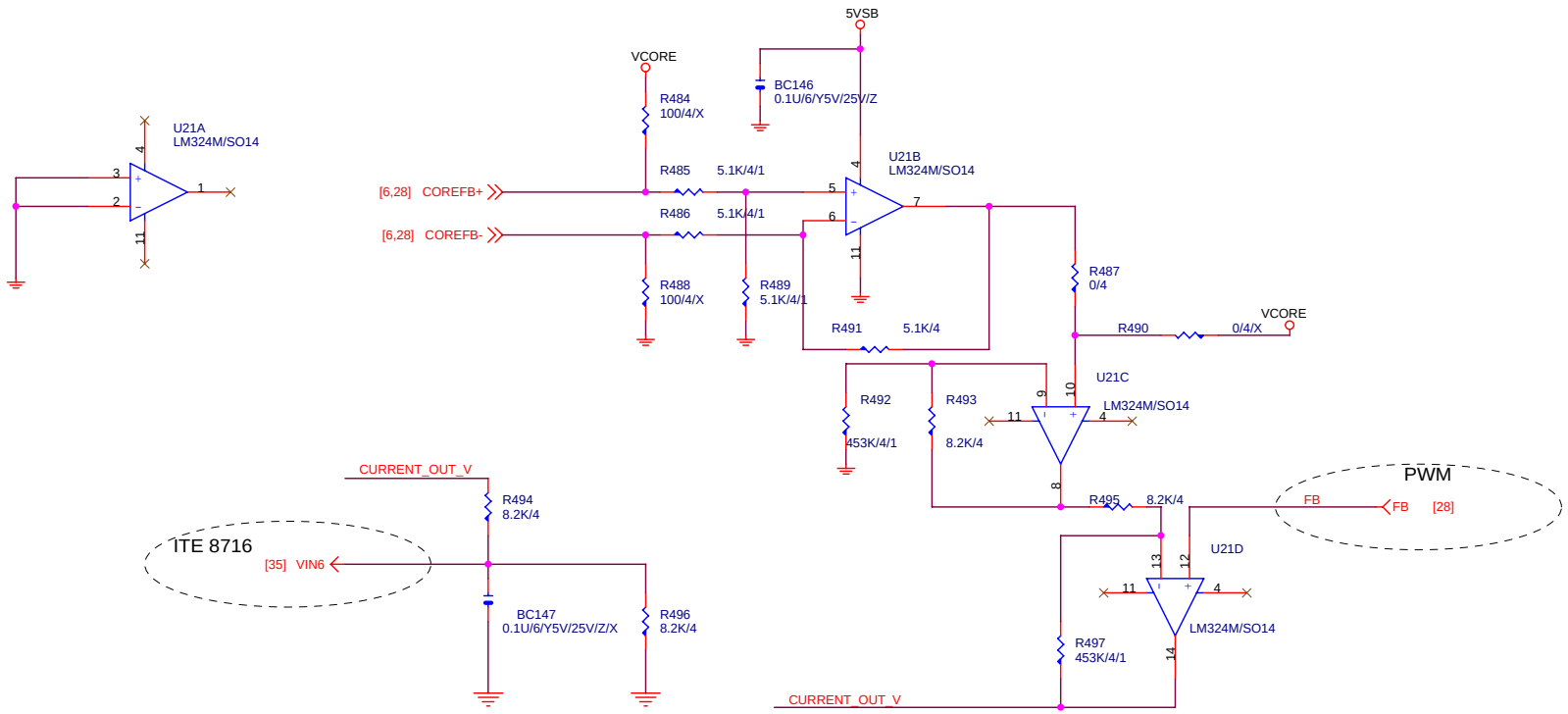






Title	Marvell_88E1115_88E1116_88E3016	
Size C	Document Number GA-M55S-S3	Rev 2.02
Date: 星期二, 一月 09, 2007	Sheet 39 of 41	


120MILS
TSB43AB23PDT/S
AT24C02N/[10HP4-180108-72R_10HP4-180108-60R]
PH/2*5K9/GY/2.54/VA/D
SMD1812P150/12V/[1 10FP1-12150B-01R_10FP1-12150B-02R]
SR32/SMB/3A
SS12/SMA/1A
Disable by IDSEL
REQ3/GNT3 INTC AD (26)
IRN1
0/8P4RS/X
IRN2
0/8P4RS/X
GIGABYTE CORP.
Title
TSB43AB23A 1394A
Size
Custom
Document Number
GA-M55S-S3
Rev
2.02
Date:
星期二, 一月 09, 2007
Sheet
40
of
41



GIGABYTE CORP.		
Title: CURRENT_OUT		
Size: B	Document Number: GA-M55S-S3	Rev: 2.02
Date: 星期二, 一月 09, 2007	Sheet 41 of 41	