GIGABYTE GA-M55S-S3 Schematics

Revision:1.11

SHEET	TITLE
01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	PROCESSOR HT INTERFACE
05	PROCESSOR DDR INTERFACE
06	PROCESSOR DDR INTERFACE
07	PROCESSOR CONTROL & DEBUG
08	DIMM A0,B0
09	DIMM A1,B1
10	DIMM TERMINATION
11	MCP55 HT/CLK
12	MCP55 PCIE X16
13	MCP55 PCIE X8 X1
14	MCP55 PCI
15	MCP55 SATA , IDE
16	MCP55 AUDIO , USB , MISC
17	MCP55 DUAL RGMII
18	MCP55 PWR/GND
19	MCP55 DECOUPLING
20	PCI EXPRESS X16 SLOT
21	PCI EXPRESS X8 SLOT
22	PCI EXPRESS X1 SLOT1,2,3
23	PCI 1,2 SLOT
24	CODEC 883
25	AUDIO JACK, L_OUT, F_AUDIO

SHEET	TITLE
26	IDE1/FDD
27	KB_MS/FUSEVCC
28	VCORE POWER
29	VCC12_HT,VCCA25,PLL POWER
30	PWR SEQUENCE PWR
31	DDR18 , DDRVTT , 5VDUAL
32	ATX POWER CONNCTOR,VCC15
33	DUAL BIOS
34	FRONT PANEL
35	ITE 8716F (GB)
36	FAN/HW MONITOR
37	F_USB1/F_USB2/F_USB3 CONNECTOR
38	COMA , LPT , TPM , R_USB
39	MARVELL 1116 RGMII PHY -A
40	TI TSB43AB23 1394A
41	
42	
43	
44	

GIGABYTE CORP.

Title: BLOCK DIAGRAM

Size: Custom | Document Number: GA-M55S-S3 | Rev: 1.11

Date: Thursday, August 17, 2006 | Sheet 1 of 41

Model Name: GA-M55S-S3

Version: 1.11

Component value change history

Date	Change Item	Reason
REV0.1 2006/03/27	First release.	
	REV1.0A	
2006/05/10	First PVT	
	REV1.1A	
2006/05/16	Update M2 CPU 風扇新機構	
	REV1.1B	
2006/05/25	R182 建新料時料號規則錯誤,修正	
	REV1.1C	
2006/06/01	改 VCC15 & CPU 機構	
	REV1.1D	
2006/06/26	EC9 1000U (low temperature 3D hang up)	
	remove R13 (VCC current leakage issue)	
	R451 12K/4/1 for STR margin	
	REV1.11D	
2006/07/13	BC117 10U=> 22U SATA ISSUE	
	ADD DL1 (POWER ISSUE)	
	REV1.11E	
2006/08/16	SC42,SC55 更改成 22uF	

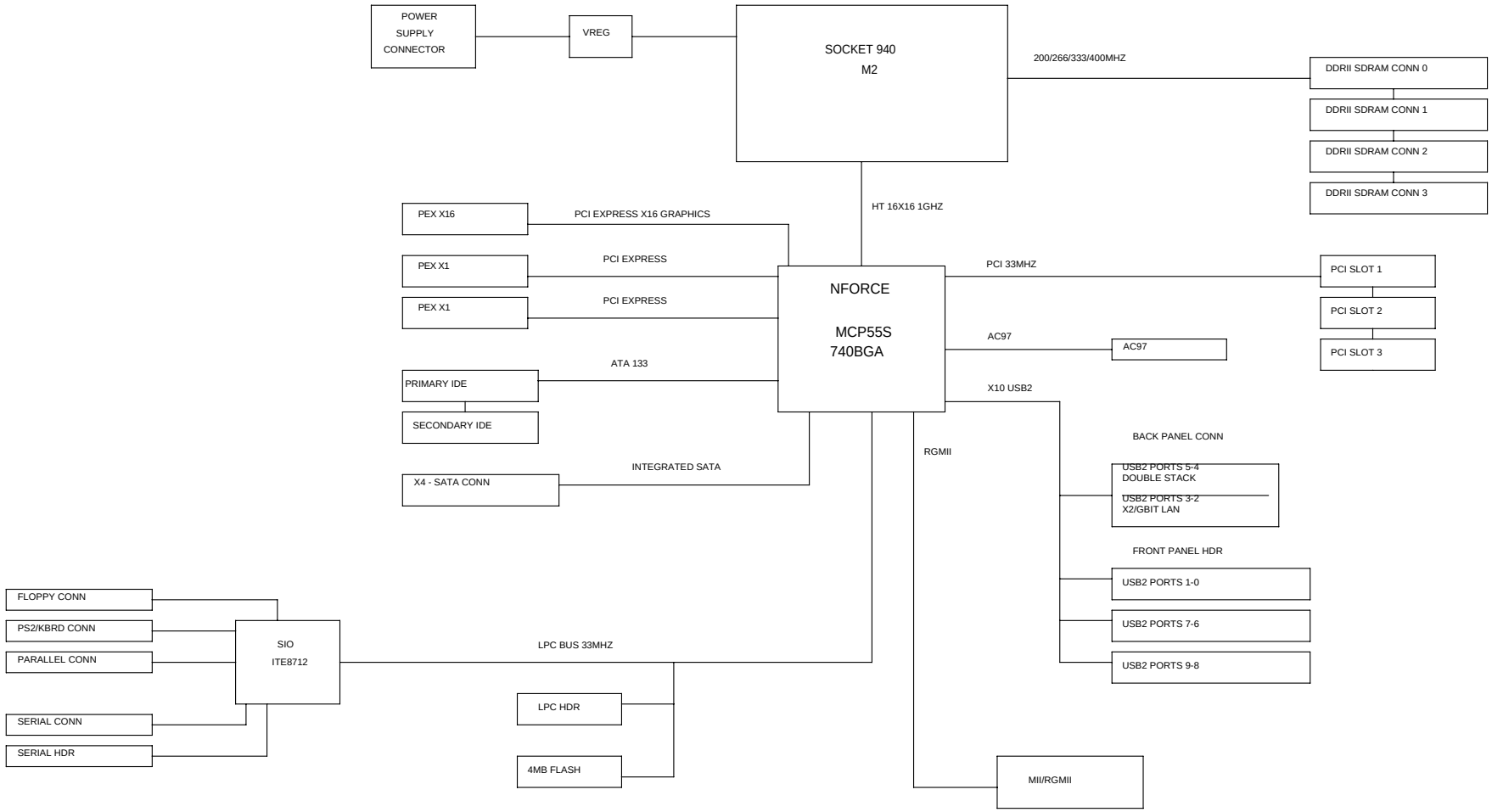
Circuit or PCB layout change for next version

Date	Change Item	Reason
REV0.1 2006/03/27	First release.	
	REV1.1	
2006/06/01	改 VCC15 & CPU 機構	

GIGABYTE CORP.

Title	BOM & PCB MODIFY HISTORY	
Size: Custom	Document Number: GA-M55S-S3	Rev: 1.11
Date: Thursday, August 17, 2006	Sheet 2 of 41	

BLOCK DIAGRAM



GIGABYTE CORP.

Title: BLOCK DIAGRAM		
Size: Custom	Document Number: GA-M55S-S3	Rev: 1.11
Date: Thursday, August 17, 2006	Sheet 3 of 41	

L0_CADIN_L[0..15] L0_CADIN_L[0..15] [11]
L0_CADIN_H[0..15] L0_CADIN_H[0..15] [11]
L0_CLKIN_L[0..1] L0_CLKIN_L[0..1] [11]
L0_CLKIN_H[0..1] L0_CLKIN_H[0..1] [11]
L0_CADOUT_L[0..15] L0_CADOUT_L[0..15] [11]
L0_CADOUT_H[0..15] L0_CADOUT_H[0..15] [11]
L0_CLKOUT_L[0..1] L0_CLKOUT_L[0..1] [11]
L0_CLKOUT_H[0..1] L0_CLKOUT_H[0..1] [11]

CPU_VDDA_RUN = VDDA25
CPU_VDDIO_SUS = DDR18V
CPU_VTT_SUS = DDRVTT

CPU_VDD_RUN = VCORE

VLDT_RUN = VCC12_HT

VLDT_A = VCC12_HT
VLDT_B = HT12B

VCORE
SC24 0.01U/4/Y5V/25V/Z
SC23 0.01U/4/Y5V/25V/Z
SC18 0.01U/4/Y5V/25V/Z

CLOSE CHIPSET & CROSSING BOUNDARY

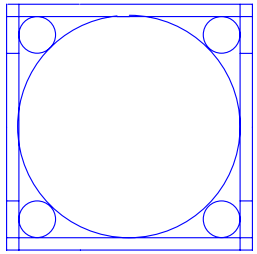
U12A

HYPERTRANSPORT

L0_CLKIN_H1	N6	L0_CLKIN_H(1)	L0_CLKOUT_H(1)	AD5	L0_CLKOUT_H1
L0_CLKIN_L1	P6	L0_CLKIN_L(1)	L0_CLKOUT_L(1)	AD4	L0_CLKOUT_L1
L0_CLKIN_H0	N3	L0_CLKIN_H(0)	L0_CLKOUT_H(0)	AD1	L0_CLKOUT_H0
L0_CLKIN_L0	N2	L0_CLKIN_L(0)	L0_CLKOUT_L(0)	AC1	L0_CLKOUT_L0
		L0_CTLIN_H(1)	L0_CTLOUT_H(1)	Y6	1 TP3
		L0_CTLIN_L(1)	L0_CTLOUT_L(1)	W6	1 TP4
L0_CTLIN_H0	U1	L0_CTLIN_H(0)	L0_CTLOUT_H(0)	W2	L0_CTLOUT_H0 [11]
L0_CTLIN_L0	V1	L0_CTLIN_L(0)	L0_CTLOUT_L(0)	W3	L0_CTLOUT_L0 [11]
L0_CADIN_H15	U6	L0_CADIN_H(15)	L0_CADOUT_H(15)	Y5	L0_CADOUT_H15
L0_CADIN_L15	V6	L0_CADIN_L(15)	L0_CADOUT_L(15)	Y4	L0_CADOUT_L15
L0_CADIN_H14	T4	L0_CADIN_H(14)	L0_CADOUT_H(14)	AB6	L0_CADOUT_H14
L0_CADIN_L14	T5	L0_CADIN_L(14)	L0_CADOUT_L(14)	AA6	L0_CADOUT_L14
L0_CADIN_H13	R6	L0_CADIN_H(13)	L0_CADOUT_H(13)	AB5	L0_CADOUT_H13
L0_CADIN_L13	T6	L0_CADIN_L(13)	L0_CADOUT_L(13)	AB4	L0_CADOUT_L13
L0_CADIN_H12	P4	L0_CADIN_H(12)	L0_CADOUT_H(12)	AD6	L0_CADOUT_H12
L0_CADIN_L12	P5	L0_CADIN_L(12)	L0_CADOUT_L(12)	AC6	L0_CADOUT_L12
L0_CADIN_H11	M4	L0_CADIN_H(11)	L0_CADOUT_H(11)	AE6	L0_CADOUT_H11
L0_CADIN_L11	M5	L0_CADIN_L(11)	L0_CADOUT_L(11)	AE6	L0_CADOUT_L11
L0_CADIN_H10	L6	L0_CADIN_H(10)	L0_CADOUT_H(10)	AF5	L0_CADOUT_H10
L0_CADIN_L10	M6	L0_CADIN_L(10)	L0_CADOUT_L(10)	AF4	L0_CADOUT_L10
L0_CADIN_H9	K4	L0_CADIN_H(9)	L0_CADOUT_H(9)	AH6	L0_CADOUT_H9
L0_CADIN_L9	K5	L0_CADIN_L(9)	L0_CADOUT_L(9)	AG6	L0_CADOUT_L9
L0_CADIN_H8	J6	L0_CADIN_H(8)	L0_CADOUT_H(8)	AH5	L0_CADOUT_H8
L0_CADIN_L8	K6	L0_CADIN_L(8)	L0_CADOUT_L(8)	AH4	L0_CADOUT_L8
L0_CADIN_H7	U3	L0_CADIN_H(7)	L0_CADOUT_H(7)	Y1	L0_CADOUT_H7
L0_CADIN_L7	U2	L0_CADIN_L(7)	L0_CADOUT_L(7)	W1	L0_CADOUT_L7
L0_CADIN_H6	R1	L0_CADIN_H(6)	L0_CADOUT_H(6)	AA2	L0_CADOUT_H6
L0_CADIN_L6	T1	L0_CADIN_L(6)	L0_CADOUT_L(6)	AA3	L0_CADOUT_L6
L0_CADIN_H5	R3	L0_CADIN_H(5)	L0_CADOUT_H(5)	AB1	L0_CADOUT_H5
L0_CADIN_L5	R2	L0_CADIN_L(5)	L0_CADOUT_L(5)	AA1	L0_CADOUT_L5
L0_CADIN_H4	N1	L0_CADIN_H(4)	L0_CADOUT_H(4)	AC2	L0_CADOUT_H4
L0_CADIN_L4	P1	L0_CADIN_L(4)	L0_CADOUT_L(4)	AC3	L0_CADOUT_L4
L0_CADIN_H3	L1	L0_CADIN_H(3)	L0_CADOUT_H(3)	AE2	L0_CADOUT_H3
L0_CADIN_L3	M1	L0_CADIN_L(3)	L0_CADOUT_L(3)	AE3	L0_CADOUT_L3
L0_CADIN_H2	L3	L0_CADIN_H(2)	L0_CADOUT_H(2)	AF1	L0_CADOUT_H2
L0_CADIN_L2	L2	L0_CADIN_L(2)	L0_CADOUT_L(2)	AE1	L0_CADOUT_L2
L0_CADIN_H1	J1	L0_CADIN_H(1)	L0_CADOUT_H(1)	AG2	L0_CADOUT_H1
L0_CADIN_L1	K1	L0_CADIN_L(1)	L0_CADOUT_L(1)	AG3	L0_CADOUT_L1
L0_CADIN_H0	J3	L0_CADIN_H(0)	L0_CADOUT_H(0)	AH1	L0_CADOUT_H0
L0_CADIN_L0	J2	L0_CADIN_L(0)	L0_CADOUT_L(0)	AG1	L0_CADOUT_L0

VCC12_HT R156 49.9/6/1 V4
GND R163 49.9/6/1 V5
[11] L0_CTLIN_H0
[11] L0_CTLIN_L0

SOCKET_M2
M2_RM/PLASTICS/[12KRC-04K807-41R]

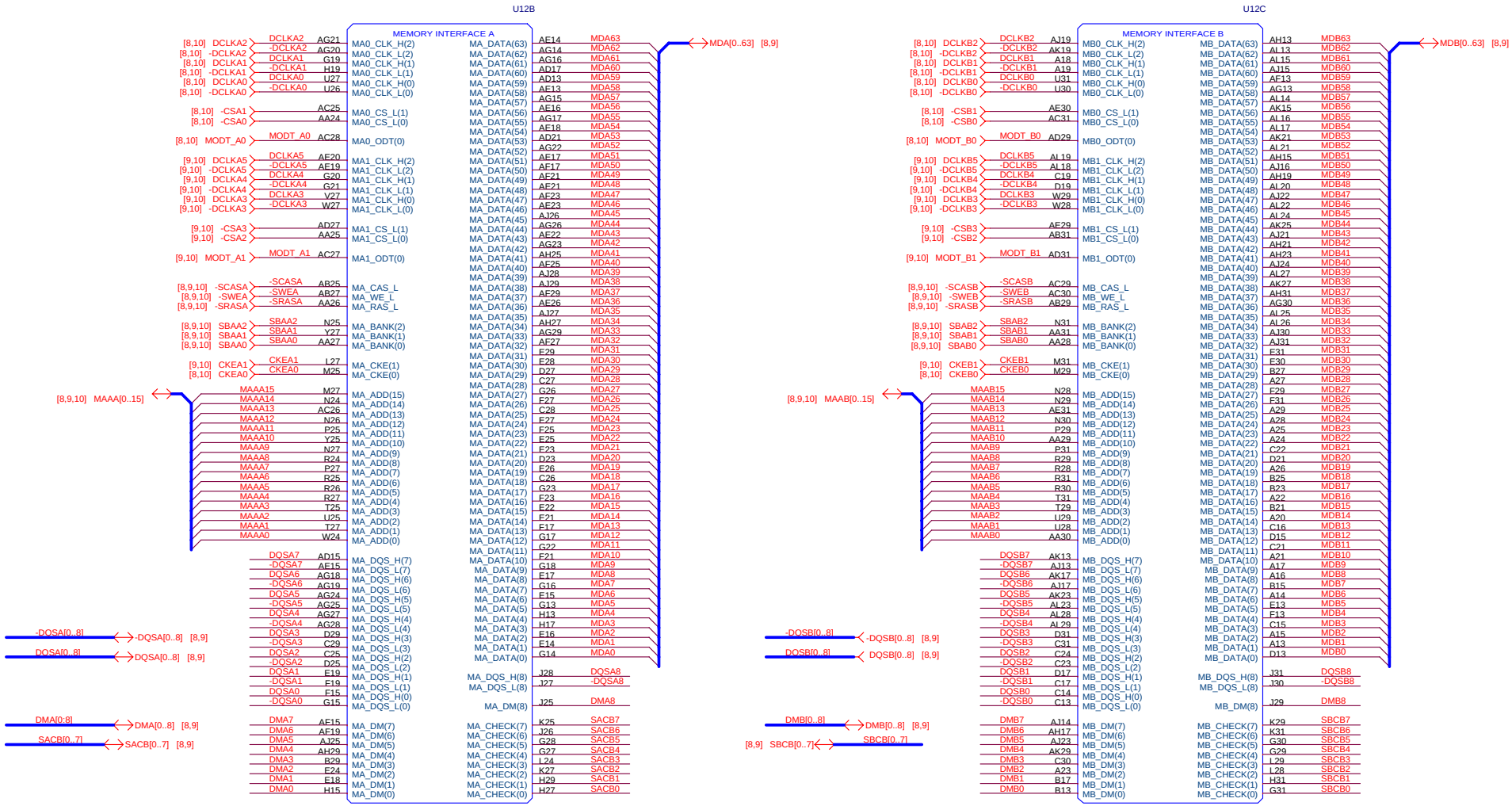


GIGABYTE CORP.

Title: CPU HYPER TRANSPORT

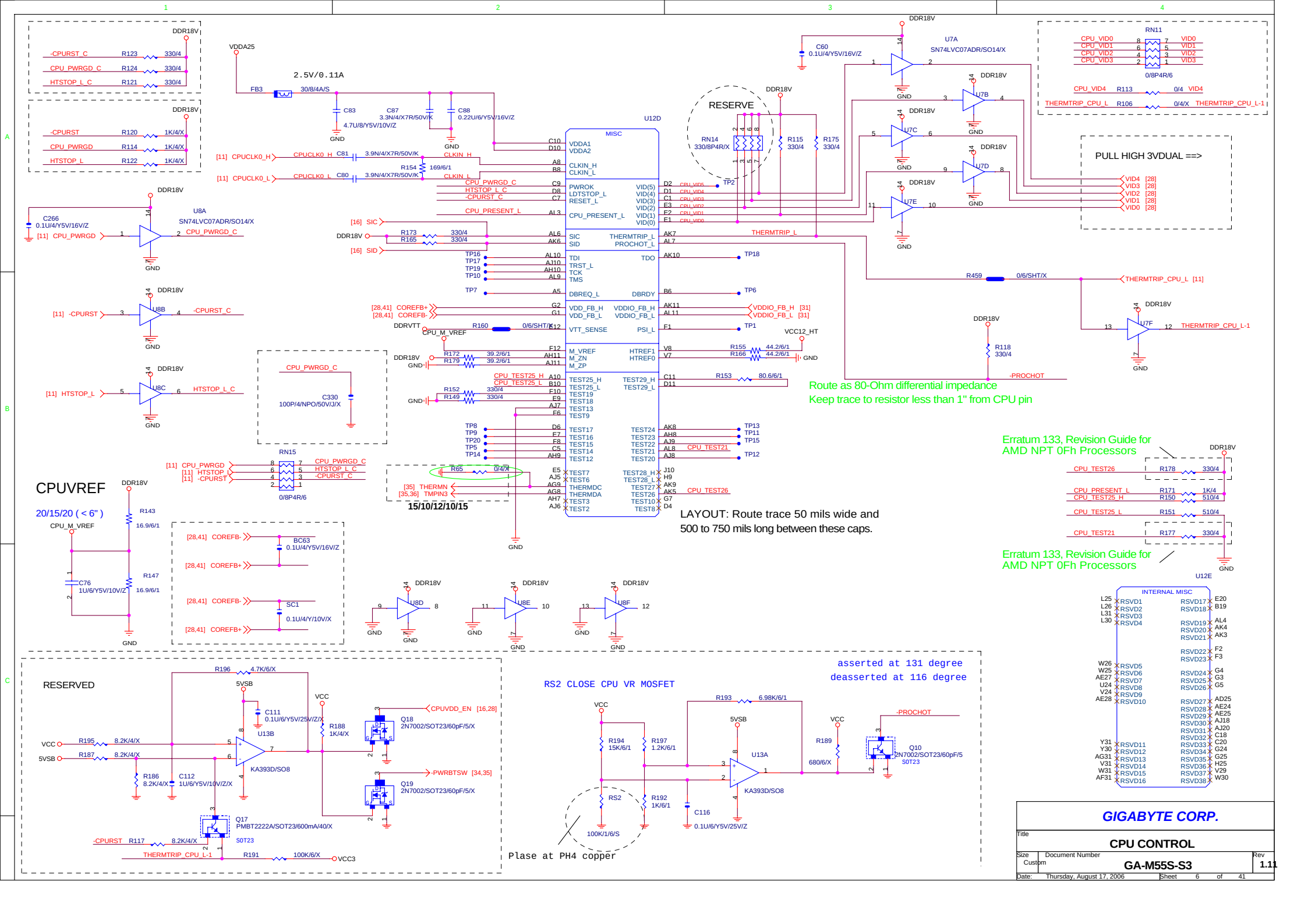
Size: Custom | Document Number: GA-M55S-S3 | Rev: 1.11

Date: Thursday, August 17, 2006 | Sheet 4 of 41

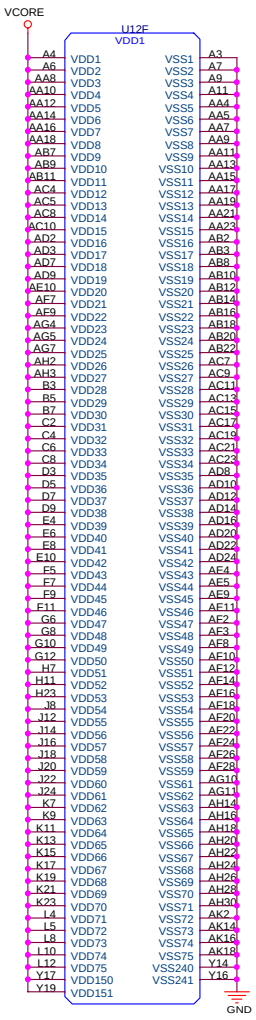


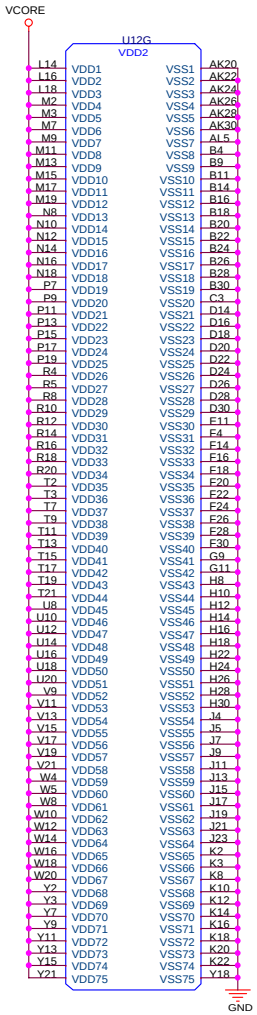
GIGABYTE CORP.

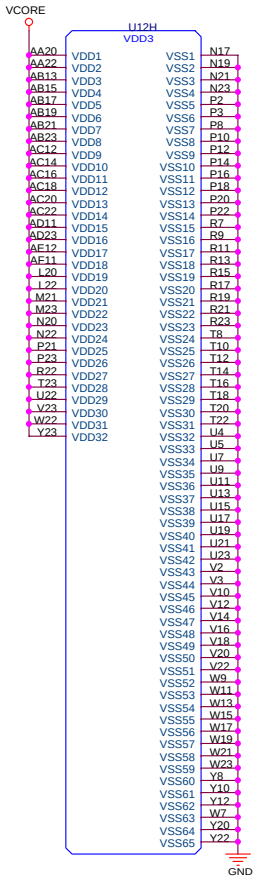
Title	CPU DDRII MEMORY	
Size: Custom	Document Number: GA-M55S-S3	Rev: 1.11
Date: Thursday, August 17, 2006	Sheet 5 of 41	

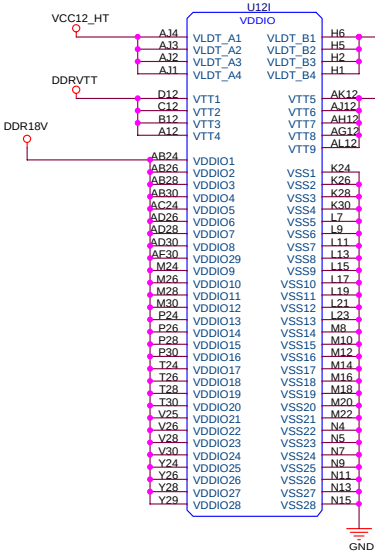

DDR18V
-CPURST_C R123 330/4
CPU_PWRGD_C R124 330/4
HTSTOP_L_C R121 330/4
-CPURST R120 1K/4/X
CPU_PWRGD R114 1K/4/X
HTSTOP_L R122 1K/4/X
VDDA25
2.5V/0.11A
FB3 30/8/4A/S
C83 4.7U/8/Y5V/10V/Z
C87 3.3N/4/X7R/50V/K
C88 0.22U/6/Y5V/16V/Z
GND
[11] CPUCLK0_H CPUCLK0_H C81 3.9N/4/X7R/50V/K CLKIN_H
[11] CPUCLK0_L CPUCLK0_L C80 3.9N/4/X7R/50V/K CLKIN_L
R154 169/6/1
CPU_PWRGD_C
HTSTOP_L_C
-CPURST_C
CPU_PRESENT_L
U12D
MISC
VDDA1
VDDA2
CLKIN_H
CLKIN_L
PWROK
LDTSTOP_L
RESET_L
CPU_PRESENT_L
VID(5)
VID(4)
VID(3)
VID(2)
VID(1)
VID(0)
SIC
SID
THERMTRIP_L
PROCHOT_L
TDI
TRST_L
TCK
TMS
TDO
DBREQ_L
DBRDY
VDD_FB_H
VDD_FB_L
VDDIO_FB_H
VDDIO_FB_L
VTT_SENSE
PSI_L
M_VREF
M_ZN
M_ZP
HTREF1
HTREF0
TEST25_H
TEST25_L
TEST19
TEST18
TEST13
TEST9
TEST29_H
TEST29_L
TEST17
TEST16
TEST15
TEST14
TEST12
TEST24
TEST23
TEST22
TEST21
TEST20
TEST7
TEST6
THERMDC
THERMDA
TEST3
TEST2
TEST28_H
TEST28_L
TEST27
TEST26
TEST10
TEST8
RESERVE
RN14 330/8P4R/X
R115 330/4
R175 330/4
TP2
CPU_VID5
CPU_VID4
CPU_VID3
CPU_VID2
CPU_VID1
CPU_VID0
U7A SN74LVC07ADR/SO14/X
U7B
U7C
U7D
U7E
C60 0.1U/4/Y5V/16V/Z
RN11
CPU_VID0 VID0
CPU_VID1 VID1
CPU_VID2 VID2
CPU_VID3 VID3
0/8P4R/6
CPU_VID4 R113 0/4 VID4
THERMTRIP_CPU_L R106 0/4/X THERMTRIP_CPU_L-1
PULL HIGH 3VDUAL ==>
VID4 [28]
VID3 [28]
VID2 [28]
VID1 [28]
VID0 [28]
U8A SN74LVC07ADR/SO14/X
C266 0.1U/4/Y5V/16V/Z
[11] CPU_PWRGD
CPU_PWRGD_C
[16] SIC
[16] SID
R173 330/4
R165 330/4
TP16
TP17
TP19
TP10
TP7
TP18
TP6
TP1
TP13
TP11
TP15
TP12
[28,41] COREFB+
[28,41] COREFB-
DDRVTT
R160 0/6/SHT/X
CPU_M_VREF
R172 39.2/6/1
R179 39.2/6/1
R152 330/4
R149 330/4
CPU_TEST25_H
CPU_TEST25_L
CPU_TEST21
CPU_TEST26
VCC12_HT
R155 44.2/6/1
R166 44.2/6/1
R153 80.6/6/1
R118 330/4
-PROCHOT
R459 0/6/SHT/X
THERMTRIP_CPU_L [11]
THERMTRIP_CPU_L-1
U8B
U8C
U7F
[11] -CPURST
[11] HTSTOP_L
HTSTOP_L_C
C330 100P/4/NPO/50V/J/X
RN15
[11] CPU_PWRGD
[11] HTSTOP
[11] -CPURST
0/8P4R/6
R65 0/4/X
[35] THERMN
[35,36] TMPIN3
15/10/12/10/15
LAYOUT: Route trace 50 mils wide and 500 to 750 mils long between these caps.
Route as 80-Ohm differential impedance
Keep trace to resistor less than 1" from CPU pin
Erratum 133, Revision Guide for AMD NPT 0Fh Processors
CPU_TEST26 R178 330/4
CPU_PRESENT_L R171 1K/4
CPU_TEST25_H R150 510/4
CPU_TEST25_L R151 510/4
CPU_TEST21 R177 330/4
Erratum 133, Revision Guide for AMD NPT 0Fh Processors
U12E
INTERNAL MISC
CPUVREF
20/15/20 (< 6")
R143 16.9/6/1
R147 16.9/6/1
C76 1U/6/Y5V/10V/Z
BC63 0.1U/4/Y5V/16V/Z
SC1 0.1U/4/Y/10V/X
U8D
U8E
U8F
RESERVED
R196 4.7K/6/X
C111 0.1U/6/Y5V/25V/Z/X
U13B
KA393D/SO8
R188 1K/4/X
R195 8.2K/4/X
R187 8.2K/4/X
R186 8.2K/4/X
C112 1U/6/Y5V/10V/Z/X
Q17 PMBT2222A/SOT23/600mA/40/X
S0T23
-CPURST R117 8.2K/4/X
THERMTRIP_CPU_L-1 R191 100K/6/X
VCC3
CPUVDD_EN [16,28]
Q18 2N7002/SOT23/60pF/5/X
-PWRBTSW [34,35]
Q19 2N7002/SOT23/60pF/5/X
RS2 CLOSE CPU VR MOSFET
asserted at 131 degree
deasserted at 116 degree
R193 6.98K/6/1
R194 15K/6/1
R197 1.2K/6/1
R192 1K/6/1
C116 0.1U/6/Y5V/25V/Z
R189 680/6/X
Q10 2N7002/SOT23/60pF/5
S0T23
RS2 100K/1/6/S
Plase at PH4 copper
GIGABYTE CORP.
Title
CPU CONTROL
Size Custom
Document Number GA-M55S-S3
Rev 1.11
Date: Thursday, August 17, 2006
Sheet 6 of 41

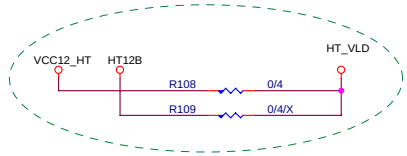
VLDT_RUN_B is connected to the VLDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.

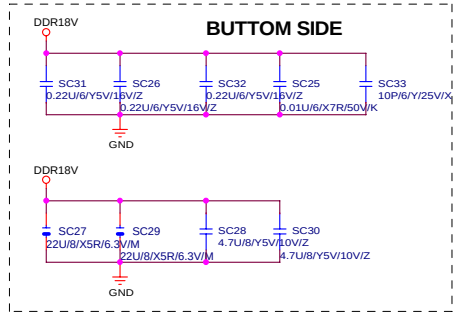


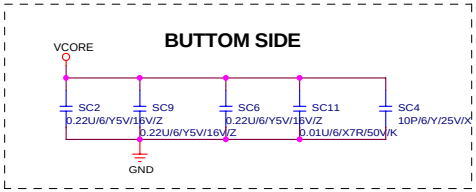


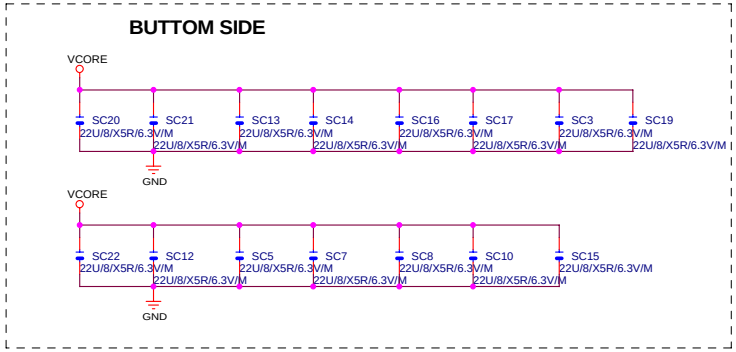


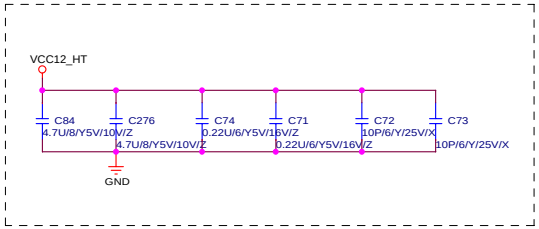


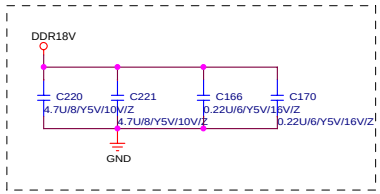


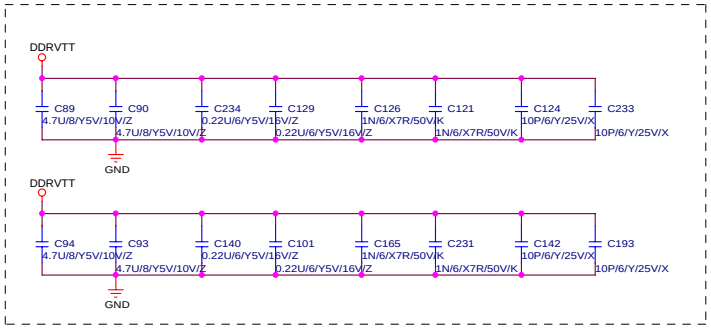


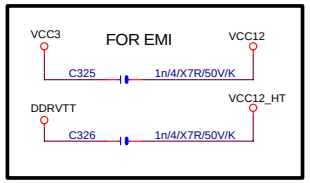










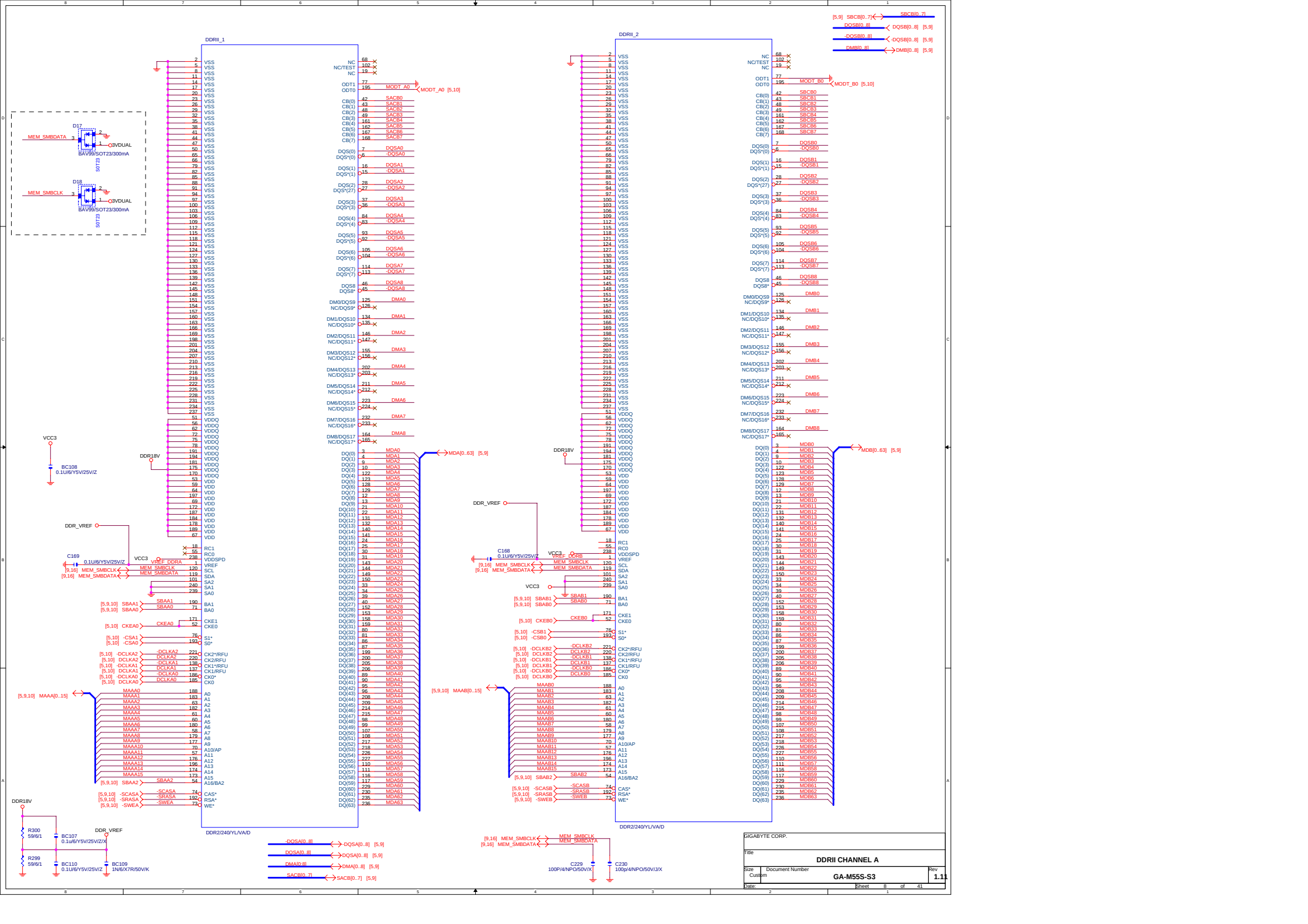


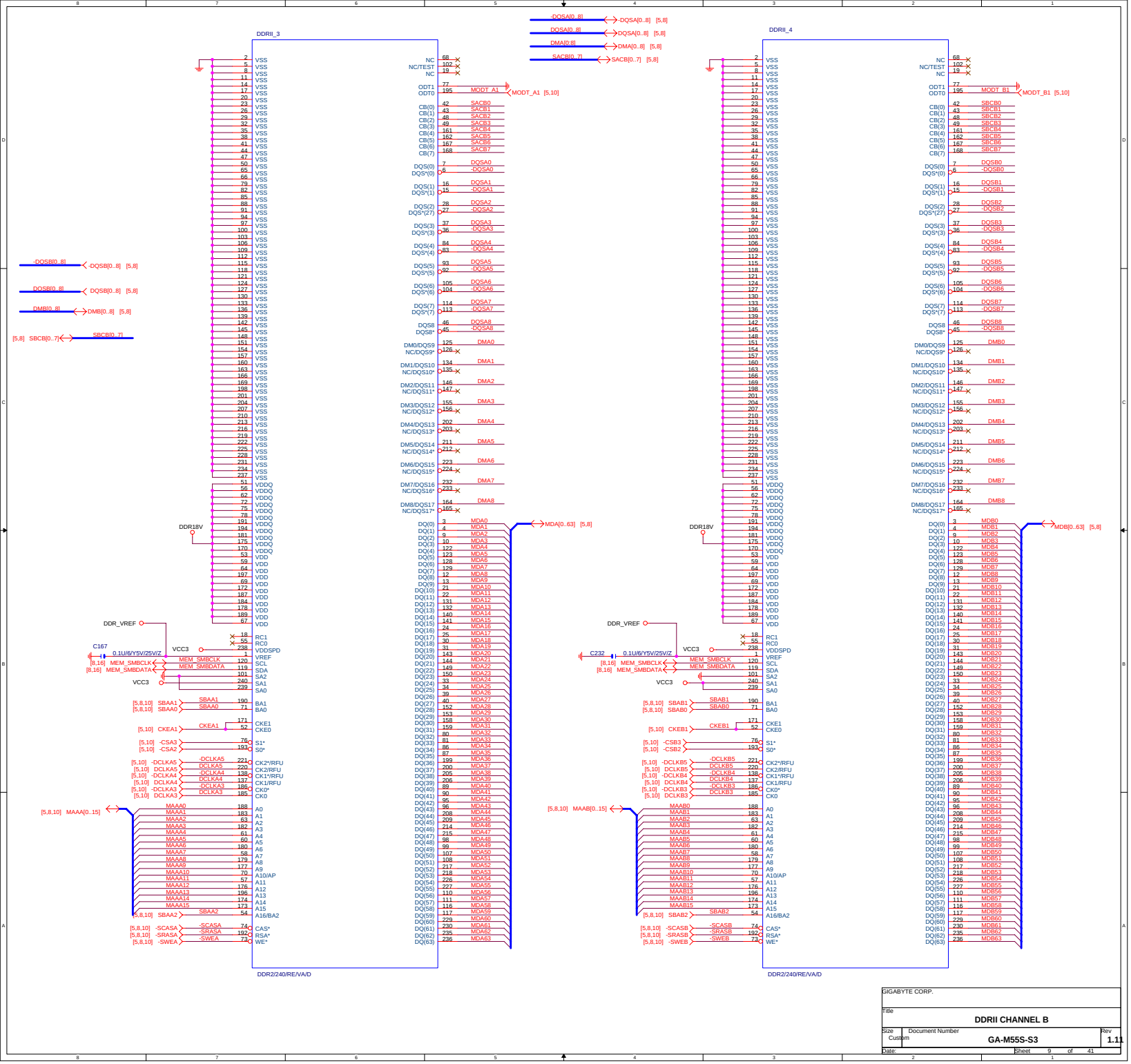
GIGABYTE CORP.

Title: **CPU POWER & GND**

Size	Document Number	Rev
Custom	GA-M55S-S3	1.11

Date: Thursday, August 17, 2006 Sheet 7 of 41


DDRII_1
DDRII_2
DDR2/240/YL/VA/D
DDR18V
VCC3
DDR_VREF
BC108 0.1U/6/Y5V/25V/Z
C169 0.1U/6/Y5V/25V/Z
C168 0.1U/6/Y5V/25V/Z
BC107 0.1u/6/Y5V/25V/Z/X
BC110 0.1U/6/Y5V/25V/Z
BC109 1N/6/X7R/50V/K
R300 59/6/1
R299 59/6/1
C229 100P/4/NPO/50V/X
C230 100p/4/NPO/50V/J/X
D17
D18
MEM_SMBDATA
MEM_SMBCLK
BAV99/SOT23/300mA
SOT23
3VDUAL
MODT_A0 [5,10]
MODT_B0 [5,10]
SBCB[0..7]
DQSB[0..8]
-DQSB[0..8]
DMB[0..8]
MDA[0..63] [5,9]
MDB[0..63] [5,9]
MAAA[0..15] [5,9,10]
MAAB[0..15] [5,9,10]
-DQSA[0..8] [5,9]
DQSA[0..8] [5,9]
DMA[0..8] [5,9]
SACB[0..7] [5,9]
GIGABYTE CORP.
DDRII CHANNEL A
GA-M55S-S3
1.11
Custom
Sheet 8 of 41

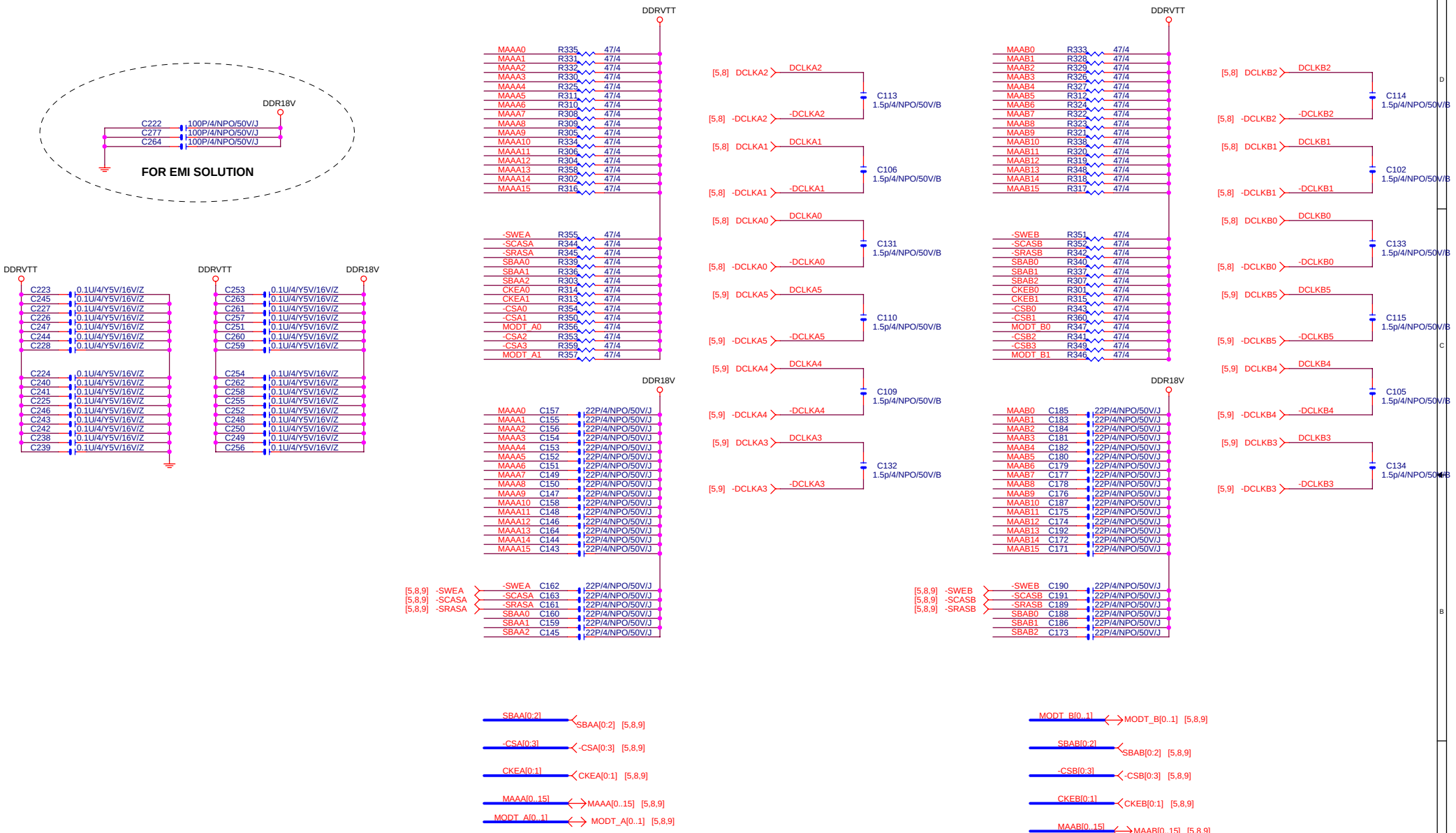


GIGABYTE CORP.

Title: **DDRII CHANNEL B**

Size	Document Number	Rev
Custom	GA-M55S-S3	1.11

Date: | Sheet 9 of 41



GIGABYTE CORP.

Title: DDRII TERMINATOR

Size: B | Document Number: GA-M55S-S3 | Rev: 1.11

Date: Thursday, August 17, 2006 | Sheet 10 of 41

N.B HEATSINK or FANSINK

U5G1A PBGA776-NVIDIA-MCP55
MCP55
MCP55P-N-A1
SEC 1 OF 9

HS2 HS1
FAN SINK/X
HEAT SINK/[12SP2-01A002-81R_12SP2-01A002-82R]

[4] L0_CADOUT_L[0..15] L0_CADOUT_L[0..15]
L0_CADOUT_H0 AK32 HT_MCP_RXD0_P
L0_CADOUT_H1 AJ32 HT_MCP_RXD1_P
L0_CADOUT_H2 AH32 HT_MCP_RXD2_P
L0_CADOUT_H3 AH30 HT_MCP_RXD3_P
L0_CADOUT_H4 AF31 HT_MCP_RXD4_P
L0_CADOUT_H5 AE32 HT_MCP_RXD5_P
L0_CADOUT_H6 AD32 HT_MCP_RXD6_P
L0_CADOUT_H7 AD30 HT_MCP_RXD7_P
L0_CADOUT_H8 AG27 HT_MCP_RXD8_P
L0_CADOUT_H9 AF27 HT_MCP_RXD9_P
L0_CADOUT_H10 AD26 HT_MCP_RXD10_P
L0_CADOUT_H11 AE29 HT_MCP_RXD11_P
L0_CADOUT_H12 AB23 HT_MCP_RXD12_P
L0_CADOUT_H13 AB26 HT_MCP_RXD13_P
L0_CADOUT_H14 AB28 HT_MCP_RXD14_P
L0_CADOUT_H15 AA28 HT_MCP_RXD15_P

[4] L0_CADOUT_H[0..15] L0_CADOUT_H[0..15]
L0_CADOUT_L0 AK31 HT_MCP_RXD0_N
L0_CADOUT_L1 AJ31 HT_MCP_RXD1_N
L0_CADOUT_L2 AH31 HT_MCP_RXD2_N
L0_CADOUT_L3 AH29 HT_MCP_RXD3_N
L0_CADOUT_L4 AE30 HT_MCP_RXD4_N
L0_CADOUT_L5 AE31 HT_MCP_RXD5_N
L0_CADOUT_L6 AD31 HT_MCP_RXD6_N
L0_CADOUT_L7 AD29 HT_MCP_RXD7_N
L0_CADOUT_L8 AG28 HT_MCP_RXD8_N
L0_CADOUT_L9 AF28 HT_MCP_RXD9_N
L0_CADOUT_L10 AD25 HT_MCP_RXD10_N
L0_CADOUT_L11 AE28 HT_MCP_RXD11_N
L0_CADOUT_L12 AB24 HT_MCP_RXD12_N
L0_CADOUT_L13 AB25 HT_MCP_RXD13_N
L0_CADOUT_L14 AB27 HT_MCP_RXD14_N
L0_CADOUT_L15 AA29 HT_MCP_RXD15_N

HT_MCP_TXD0_P R29 L0_CADIN_H0
HT_MCP_TXD1_P T29 L0_CADIN_H1
HT_MCP_TXD2_P T31 L0_CADIN_H2
HT_MCP_TXD3_P U31 L0_CADIN_H3
HT_MCP_TXD4_P W29 L0_CADIN_H4
HT_MCP_TXD5_P Y29 L0_CADIN_H5
HT_MCP_TXD6_P Y31 L0_CADIN_H6
HT_MCP_TXD7_P AA31 L0_CADIN_H7
HT_MCP_TXD8_P R24 L0_CADIN_H8
HT_MCP_TXD9_P T28 L0_CADIN_H9
HT_MCP_TXD10_P U28 L0_CADIN_H10
HT_MCP_TXD11_P T25 L0_CADIN_H11
HT_MCP_TXD12_P V27 L0_CADIN_H12
HT_MCP_TXD13_P V26 L0_CADIN_H13
HT_MCP_TXD14_P Y28 L0_CADIN_H14
HT_MCP_TXD15_P Y26 L0_CADIN_H15
L0_CADIN_H[0..15] L0_CADIN_H[0..15] [4]

HT_MCP_TXD0_N R30 L0_CADIN_L0
HT_MCP_TXD1_N T30 L0_CADIN_L1
HT_MCP_TXD2_N T32 L0_CADIN_L2
HT_MCP_TXD3_N U32 L0_CADIN_L3
HT_MCP_TXD4_N W30 L0_CADIN_L4
HT_MCP_TXD5_N Y30 L0_CADIN_L5
HT_MCP_TXD6_N Y32 L0_CADIN_L6
HT_MCP_TXD7_N AA32 L0_CADIN_L7
HT_MCP_TXD8_N T24 L0_CADIN_L8
HT_MCP_TXD9_N T27 L0_CADIN_L9
HT_MCP_TXD10_N U29 L0_CADIN_L10
HT_MCP_TXD11_N T26 L0_CADIN_L11
HT_MCP_TXD12_N V28 L0_CADIN_L12
HT_MCP_TXD13_N V25 L0_CADIN_L13
HT_MCP_TXD14_N Y27 L0_CADIN_L14
HT_MCP_TXD15_N Y25 L0_CADIN_L15
L0_CADIN_L[0..15] L0_CADIN_L[0..15] [4]

COUPON1 COUPON1 1 2 COUPON/X
COUPON2 COUPON2 1 2 COUPON/X
VCC

[4] L0_CLKOUT_H0 L0_CLKOUT_H0 AG30 HT_MCP_RX_CLK0_P
[4] L0_CLKOUT_L0 L0_CLKOUT_L0 AG29 HT_MCP_RX_CLK0_N
[4] L0_CLKOUT_H1 L0_CLKOUT_H1 AD27 HT_MCP_RX_CLK1_P
[4] L0_CLKOUT_L1 L0_CLKOUT_L1 AD28 HT_MCP_RX_CLK1_N

HT_MCP_TX_CLK0_P V30 L0_CLKIN_H0
HT_MCP_TX_CLK0_N V31 L0_CLKIN_L0
HT_MCP_TX_CLK1_P V24 L0_CLKIN_H1
HT_MCP_TX_CLK1_N W24 L0_CLKIN_L1
L0_CLKIN_H0 [4]
L0_CLKIN_L0 [4]
L0_CLKIN_H1 [4]
L0_CLKIN_L1 [4]

[4] L0_CTLOUT_H0 L0_CTLOUT_H0 AC30 HT_MCP_RXCTL_P
[4] L0_CTLOUT_L0 L0_CTLOUT_L0 AC29 HT_MCP_RXCTL_N

HT_MCP_TXCTL_P AB30 L0_CTLIN_H0
HT_MCP_TXCTL_N AB31 L0_CTLIN_L0
L0_CTLIN_H0 [4]
L0_CTLIN_L0 [4]

HT_MCP_REQ P25 -HT_REQ R232 1K/4 3VDUAL
HT_MCP_STOP P28 HTSTOP_L HTSTOP_L [6]
HT_MCP_RST P27 -CPURST -CPURST [6]
HT_MCP_PWRGD P26 CPU_PWRGD CPU_PWRGD [6]

R297 150/6/1 HT_COMP1 AG26 HT_MCP_COMP_GND1
R295 49.9/6/1 HT_COMP2 AG25 HT_MCP_COMP_GND2

CLKOUT0_CLKIN_200MHZ_P N32 SR3 0/6/SHT/X CPUCLK0_H CPUCLK0_H [6]
CLKOUT0_CLKIN_200MHZ_N N31 SR1 0/6/SHT/X CPUCLK0_L CPUCLK0_L [6]
CLKOUT1_200MHZ_P M30 SR_CLKOUT1_P 1 TP41
CLKOUT1_200MHZ_N M29 TP_CLKOUT1_N 1 TP42
CLKOUT2_200MHZ_P L30 TP_CLKOUT2_P 1 TP37
CLKOUT2_200MHZ_N L29 TP_CLKOUT2_N 1 TP36

[6] THERMTRIP_CPU_L THERMTRIP_CPU_L AJ29 THERMTRIP/GPIO*

VCC15 P23 +1.5V_PLL_CPU_HT
VCC3 AC21 +3.3V_HT
AC22 +3.3V_PLL_CPU
AC23 +3.3V_PLL_HT
VCC12_HT
HT_VREF U23
CLKOUT_25MHZ N26 TP_CLKOUT_25M 1 TP45
CLK200_TERM_GND M28 R207 562/6/1
SC47 0.1U/4/Y5V/16V/Z

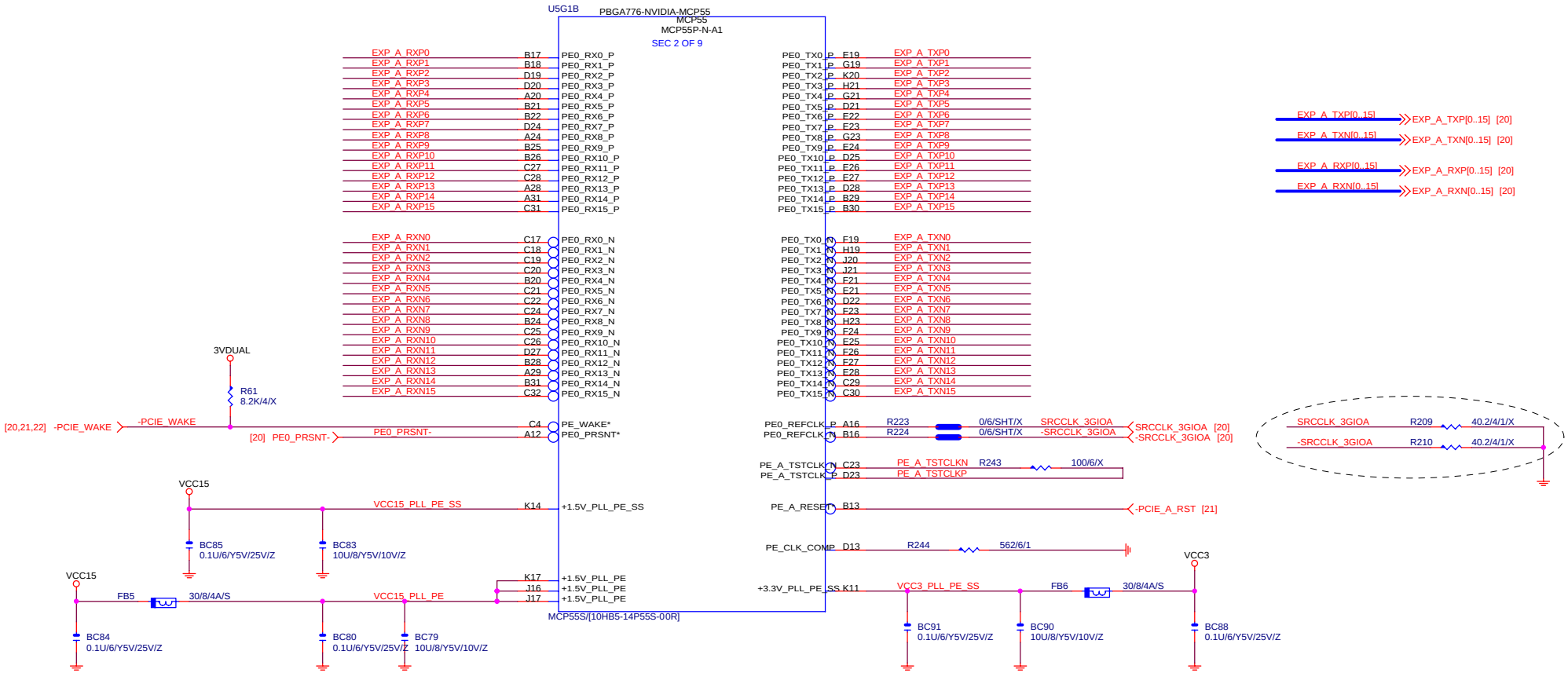
VCC3 FB9 30/8/4A/S VCC3_PLL_HT
C267 0.1U/6/Y5V/25V/Z
BC105 10U/8/Y5V/10V/Z
C217 0.1U/4/Y5V/16V/Z
C219 C194
0.1U/4/Y5V/16V/Z 0.1U/4/Y5V/16V/Z

MCP55S/[10HB5-14P55S-00R]

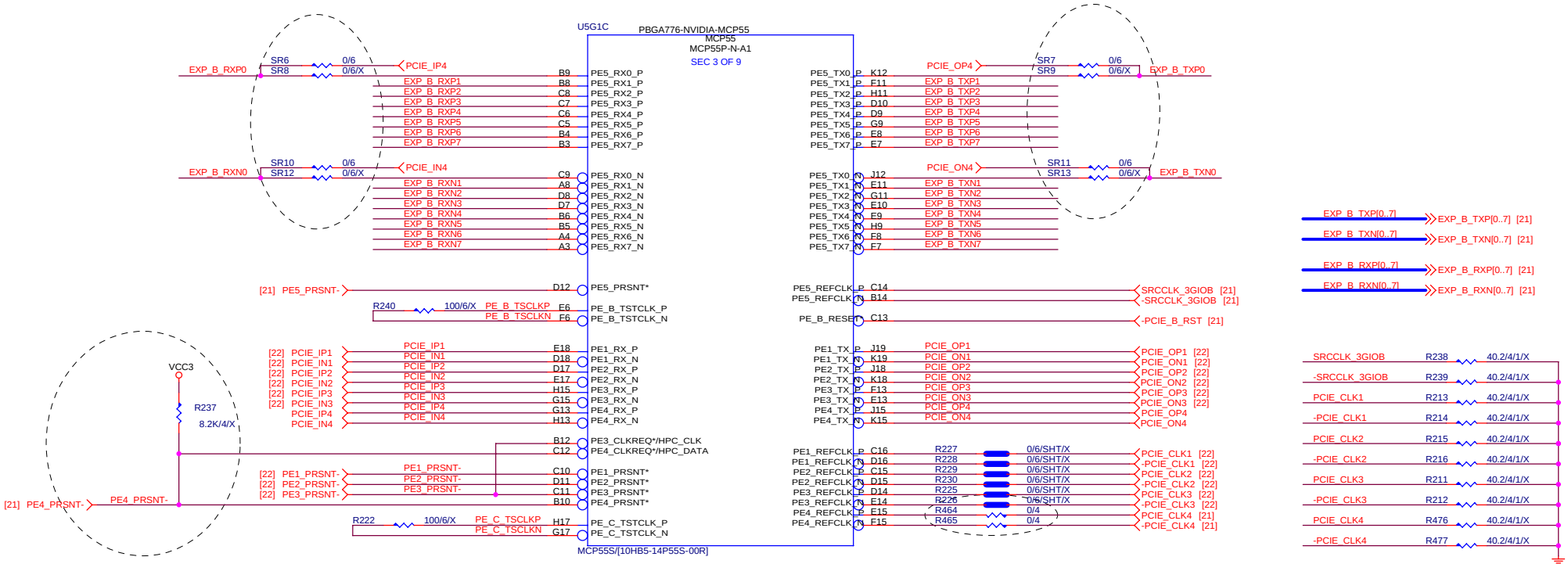
HTSTOP_L
[20,21] -CK8PWOK Q25 2N7002/SOT23/60pF/5 S0T23
CPU_PWRGD
Q22 2N7002/SOT23/60pF/5 S0T23
-CPURST
Q27 2N7002/SOT23/60pF/5 S0T23
3VDUAL
R233 8.2K/4
Q24 2N7002/SOT23/60pF/5
R201
[16,21,30] CK8_PWOK
0/6/SHT/X

GIGABYTE CORP.

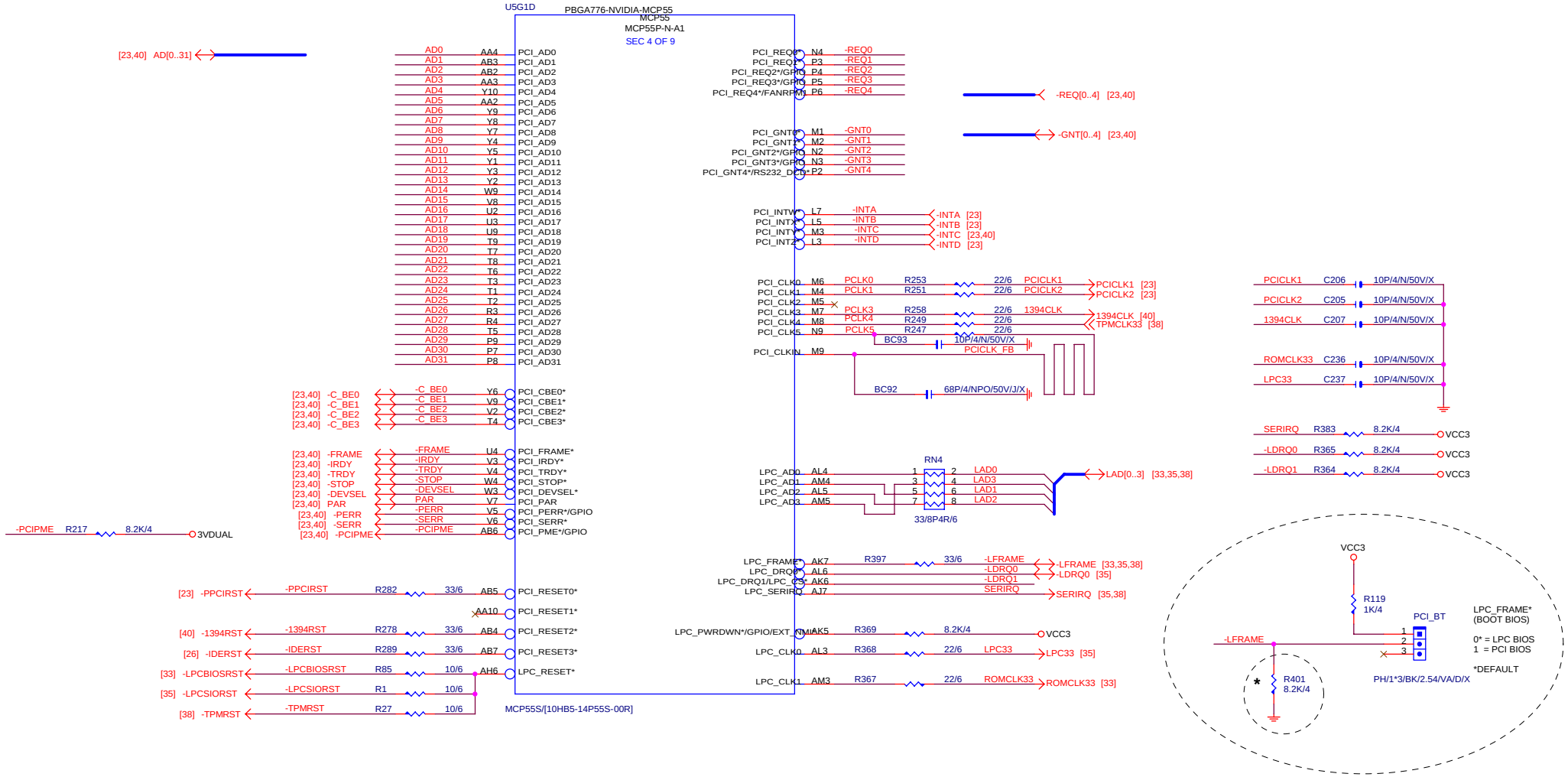
Title	MCP55 HT/CLK	
Size: Custom	Document Number: GA-M55S-S3	Rev: 1.11
Date: Thursday, August 17, 2006	Sheet 11 of 41	



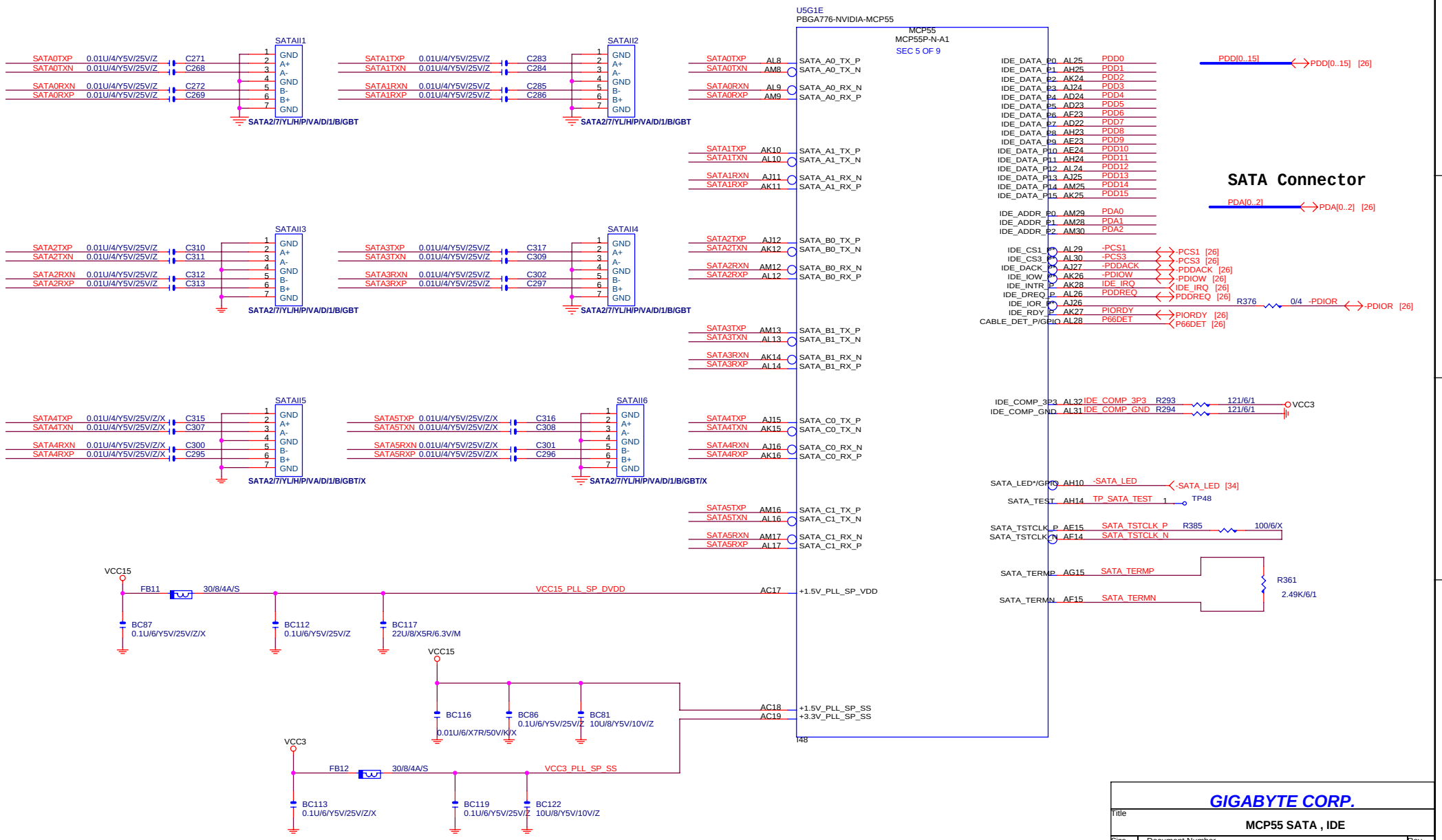
GIGABYTE CORP.		
Title: MCP55 PCIE X16		
Size: Custom	Document Number: GA-M55S-S3	Rev: 1.11
Date: Thursday, August 17, 2006	Sheet 12 of 41	



Company	GIGABYTE CORP.
Title	MCP55 PCIE X8 , X1
Size	Custom
Document Number	GA-M55S-S3
Rev	1.11
Date	Thursday, August 17, 2006
Sheet	13 of 41

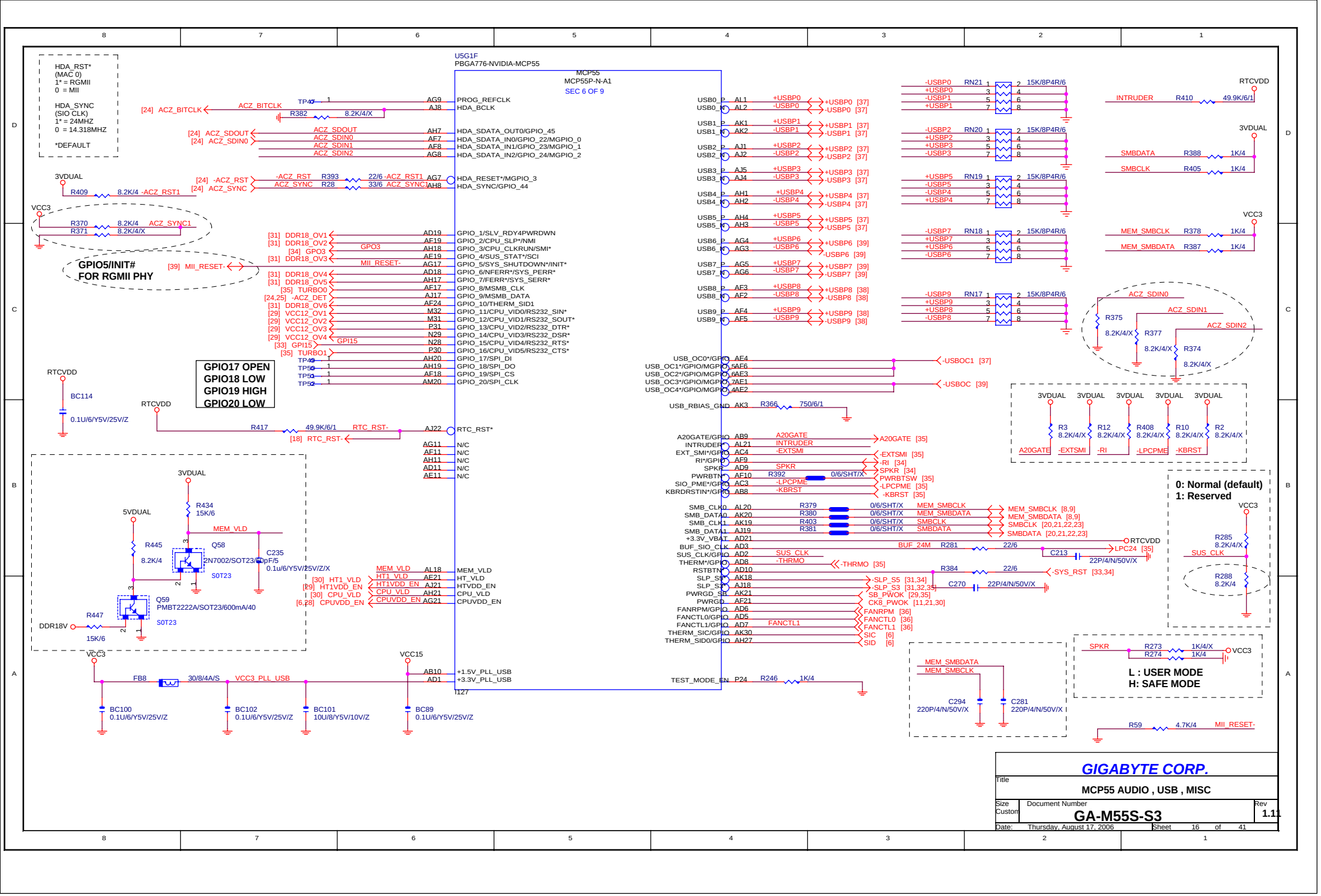


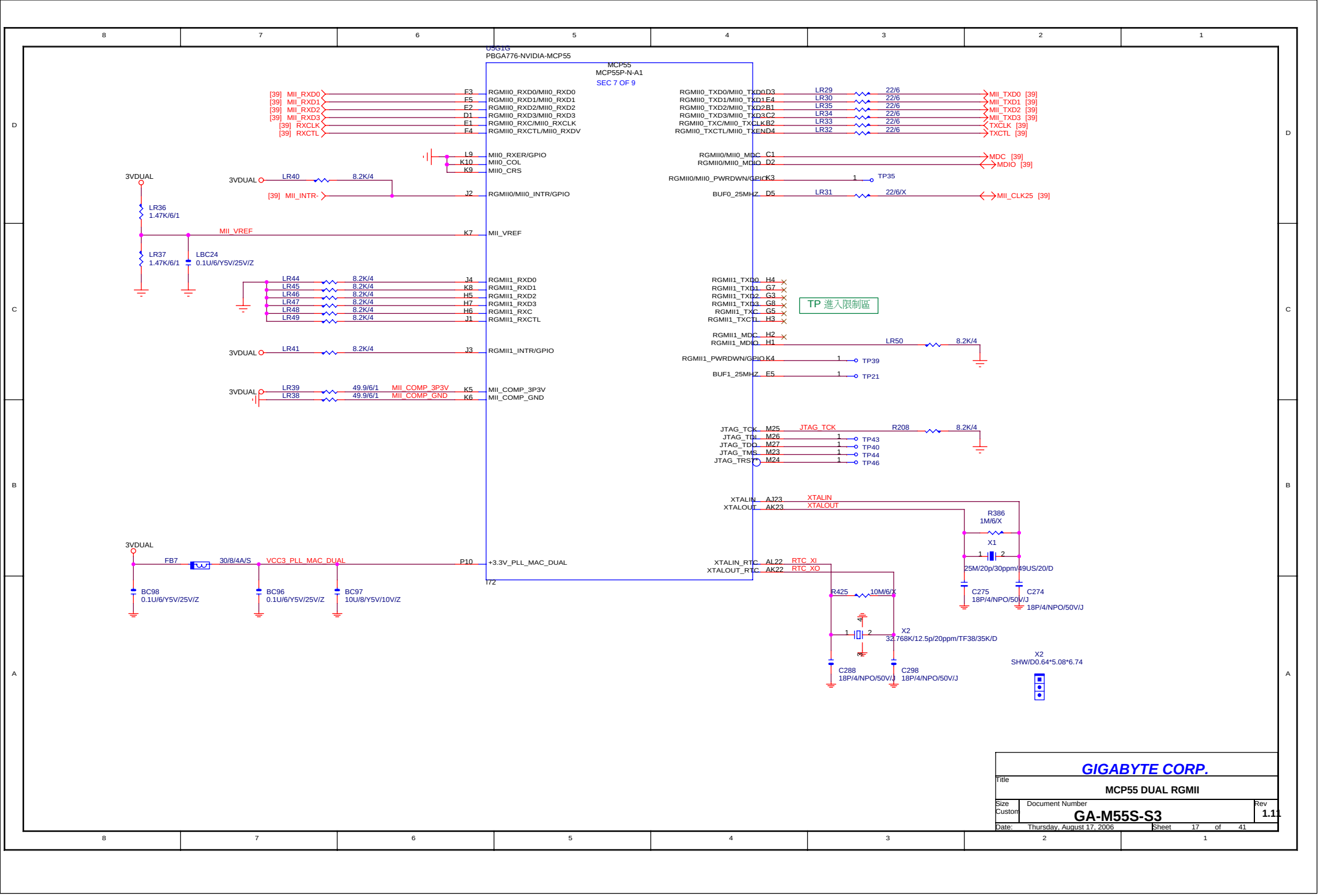
GIGABYTE CORP.		
Title: MCP55 PCI		
Size: Custom	Document Number: GA-M55S-S3	Rev: 1.11
Date: Thursday, August 17, 2006	Sheet 14 of 41	

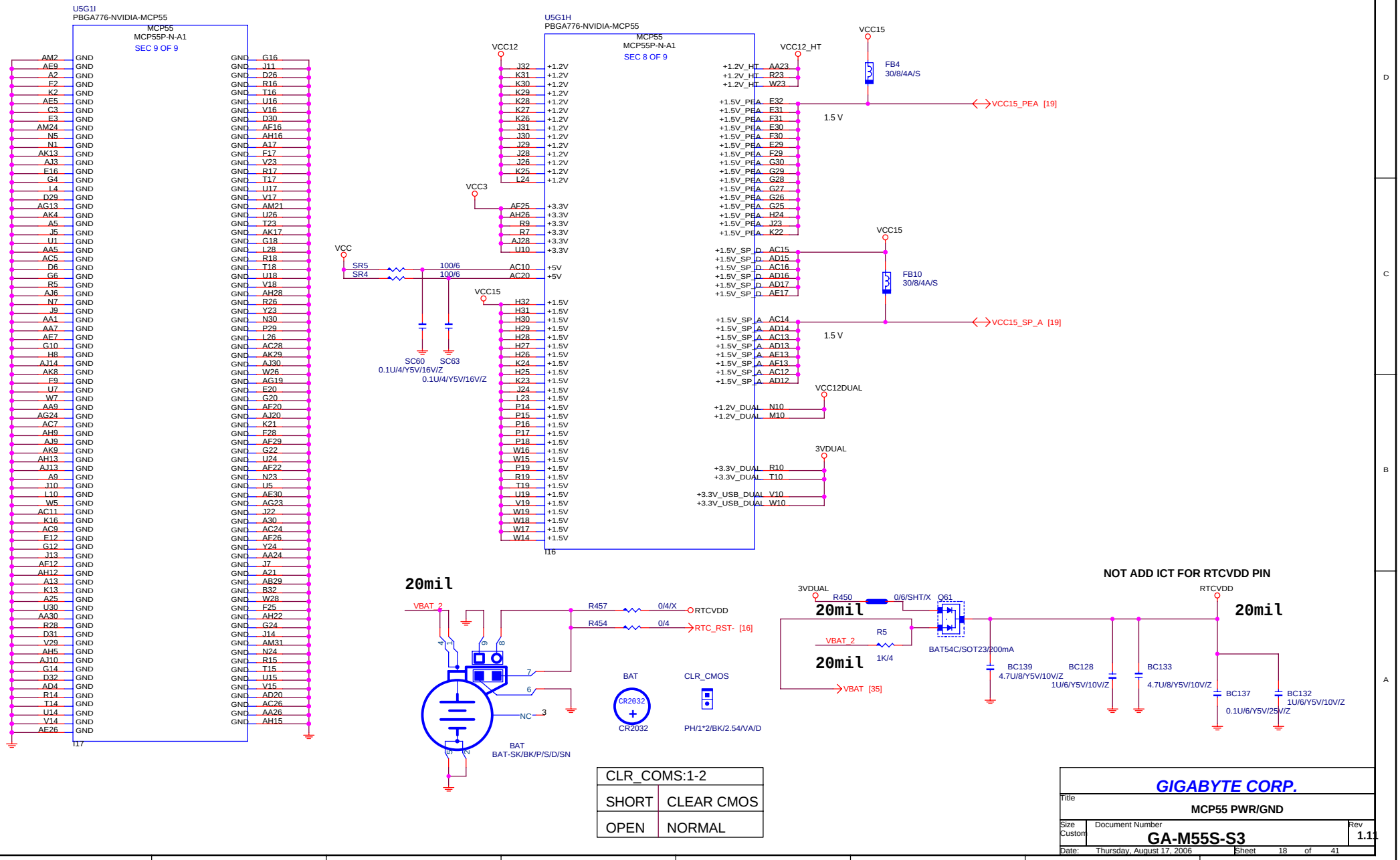


Title	MCP55 SATA , IDE
Size	Custom
Document Number	GA-M55S-S3
Rev	1.11
Date:	Thursday, August 17, 2006
Sheet	15 of 41

GIGABYTE CORP.


HDA_RST* (MAC 0) 1* = RGMII 0 = MII
HDA_SYNC (SIO CLK) 1* = 24MHZ 0 = 14.318MHZ
*DEFAULT
U5G1F
PBGA776-NVIDIA-MCP55
MCP55
MCP55P-N-A1
SEC 6 OF 9
GPIO5/INIT# FOR RGMII PHY
GPIO17 OPEN
GPIO18 LOW
GPIO19 HIGH
GPIO20 LOW
0: Normal (default)
1: Reserved
L : USER MODE
H: SAFE MODE
GIGABYTE CORP.
MCP55 AUDIO , USB , MISC
GA-M55S-S3
1.11
Thursday, August 17, 2006
16 of 41


U5G1G
PBGA776-NVIDIA-MCP55
MCP55
MCP55P-N-A1
SEC 7 OF 9
[39] MII_RXD0
[39] MII_RXD1
[39] MII_RXD2
[39] MII_RXD3
[39] RXCLK
[39] RXCTL
F3 RGMII0_RXD0/MII0_RXD0
F5 RGMII0_RXD1/MII0_RXD1
E2 RGMII0_RXD2/MII0_RXD2
D1 RGMII0_RXD3/MII0_RXD3
E1 RGMII0_RXC/MII0_RXCLK
F4 RGMII0_RXCTL/MII0_RXDV
L9 MII0_RXER/GPIO
K10 MII0_COL
K9 MII0_CRS
3VDUAL
LR40 8.2K/4
[39] MII_INTR-
J2 RGMII0/MII0_INTR/GPIO
LR36 1.47K/6/1
MII_VREF
K7 MII_VREF
LR37 1.47K/6/1
LBC24 0.1U/6/Y5V/25V/Z
LR44 8.2K/4
LR45 8.2K/4
LR46 8.2K/4
LR47 8.2K/4
LR48 8.2K/4
LR49 8.2K/4
J4 RGMII1_RXD0
K8 RGMII1_RXD1
H5 RGMII1_RXD2
H7 RGMII1_RXD3
H6 RGMII1_RXC
J1 RGMII1_RXCTL
LR41 8.2K/4
J3 RGMII1_INTR/GPIO
LR39 49.9/6/1 MII_COMP_3P3V
LR38 49.9/6/1 MII_COMP_GND
K5 MII_COMP_3P3V
K6 MII_COMP_GND
FB7 30/8/4A/S
VCC3_PLL_MAC_DUAL
P10 +3.3V_PLL_MAC_DUAL
172
BC98 0.1U/6/Y5V/25V/Z
BC96 0.1U/6/Y5V/25V/Z
BC97 10U/8/Y5V/10V/Z
RGMII0_TXD0/MII0_TXD0 D3
RGMII0_TXD1/MII0_TXD1 E4
RGMII0_TXD2/MII0_TXD2 B1
RGMII0_TXD3/MII0_TXD3 C2
RGMII0_TXC/MII0_TXCLK B2
RGMII0_TXCTL/MII0_TXEND 4
LR29 22/6
LR30 22/6
LR35 22/6
LR34 22/6
LR33 22/6
LR32 22/6
MII_TXD0 [39]
MII_TXD1 [39]
MII_TXD2 [39]
MII_TXD3 [39]
TXCLK [39]
TXCTL [39]
RGMII0/MII0_MDC C1
RGMII0/MII0_MDIO D2
MDC [39]
MDIO [39]
RGMII0/MII0_PWRDWN/GPIO K3
TP35
BUF0_25MHZ D5
LR31 22/6/X
MII_CLK25 [39]
RGMII1_TXD0 H4
RGMII1_TXD1 G7
RGMII1_TXD2 G3
RGMII1_TXD3 G8
RGMII1_TXC G5
RGMII1_TXCTL H3
TP 進入限制區
RGMII1_MDC H2
RGMII1_MDIO H1
LR50 8.2K/4
RGMII1_PWRDWN/GPIO K4
TP39
BUF1_25MHZ E5
TP21
JTAG_TCK M25
JTAG_TDI M26
JTAG_TDO M27
JTAG_TMS M23
JTAG_TRST* M24
JTAG_TCK
R208 8.2K/4
TP43
TP40
TP44
TP46
XTALIN AJ23
XTALOUT AK23
XTALIN
XTALOUT
R386 1M/6/X
X1
25M/20p/30ppm/49US/20/D
C275 18P/4/NPO/50V/J
C274 18P/4/NPO/50V/J
XTALIN_RTC AL22
XTALOUT_RTC AK22
RTC_XI
RTC_XO
R425 10M/6/X
X2 32.768K/12.5p/20ppm/TF38/35K/D
C288 18P/4/NPO/50V/J
C298 18P/4/NPO/50V/J
X2 SHW/D0.64*5.08*6.74
GIGABYTE CORP.
Title
MCP55 DUAL RGMII
Size Custom
Document Number
GA-M55S-S3
Rev 1.11
Date: Thursday, August 17, 2006
Sheet 17 of 41



CLR_COMS:1-2	
SHORT	CLEAR CMOS
OPEN	NORMAL

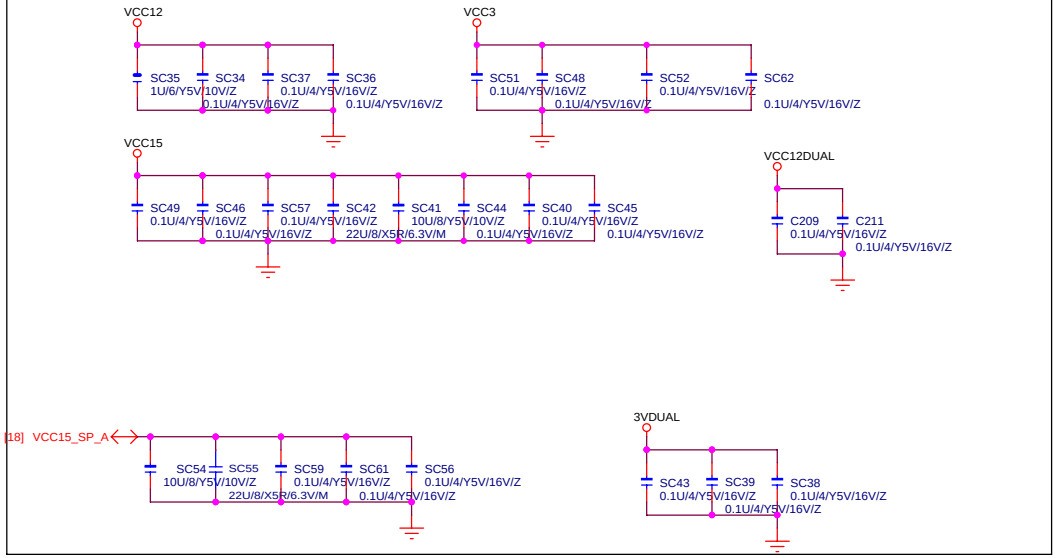
GIGABYTE CORP.

Title: MCP55 PWR/GND

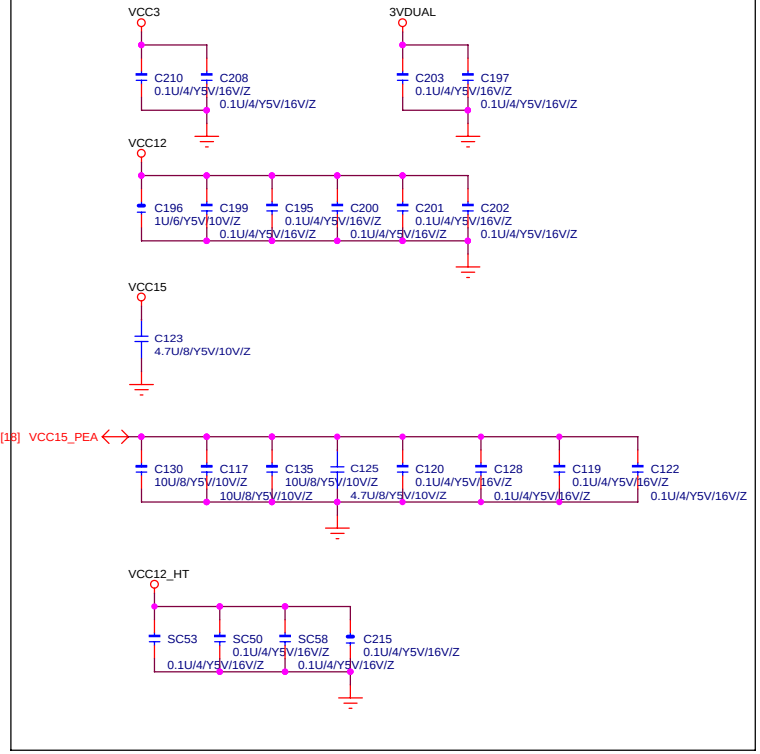
Size: Custom | Document Number: GA-M55S-S3 | Rev: 1.11

Date: Thursday, August 17, 2006 | Sheet 18 of 41

MCP55 BACK SIDE DECOUPLING



MCP55 TOP SIDE DECOUPLING



MCP55 INTERNAL PULL-UP/PULL-DOWN

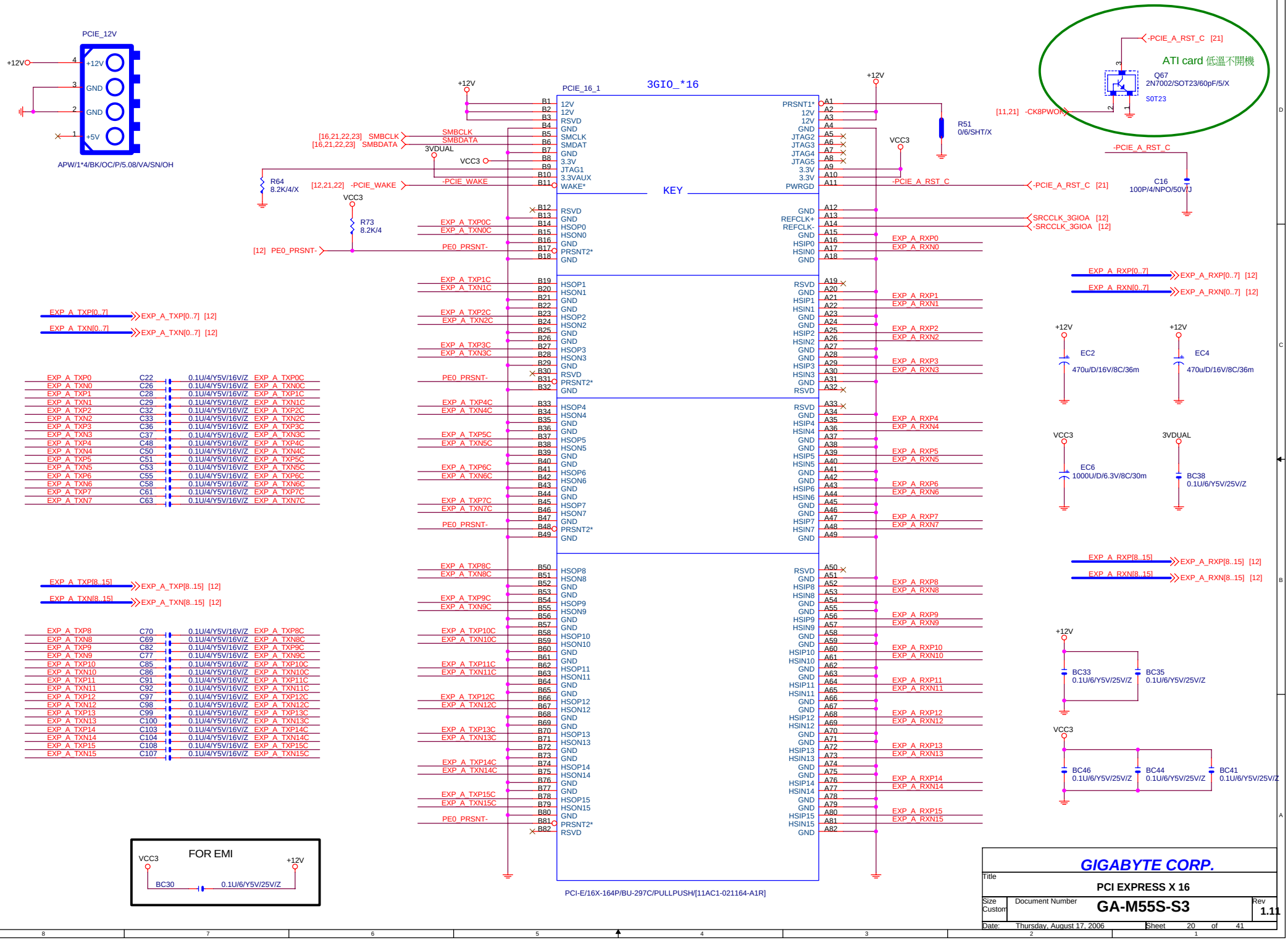
PIN	VOLTAGE
A20GATE/GPIO	+3.3V
EXT_SMI*/GPIO	+3.3V_DUAL
HDA_SDATA_IN0/GPIO_22/MGPIO_0	+3.3V_DUAL/GND
HDA_SDATA_IN1/GPIO_23/MGPIO_1	+3.3V_DUAL/GND
HDA_SDATA_IN2/GPIO_24/MGPIO_2	+3.3V_DUAL/GND
HDA_SDATA_OUT/GPIO_45	+3.3V_DUAL/GND
JTAG_TDI	+3.3V
JTAG_TMS	+3.3V
JTAG_TRST*	GND
KBRDRSTIN*/GPIO	+3.3V
PE_WAKE*	+3.3V_DUAL
SIO_PME*/GPIO	+3.3V_DUAL
THERM*/GPIO	+3.3V

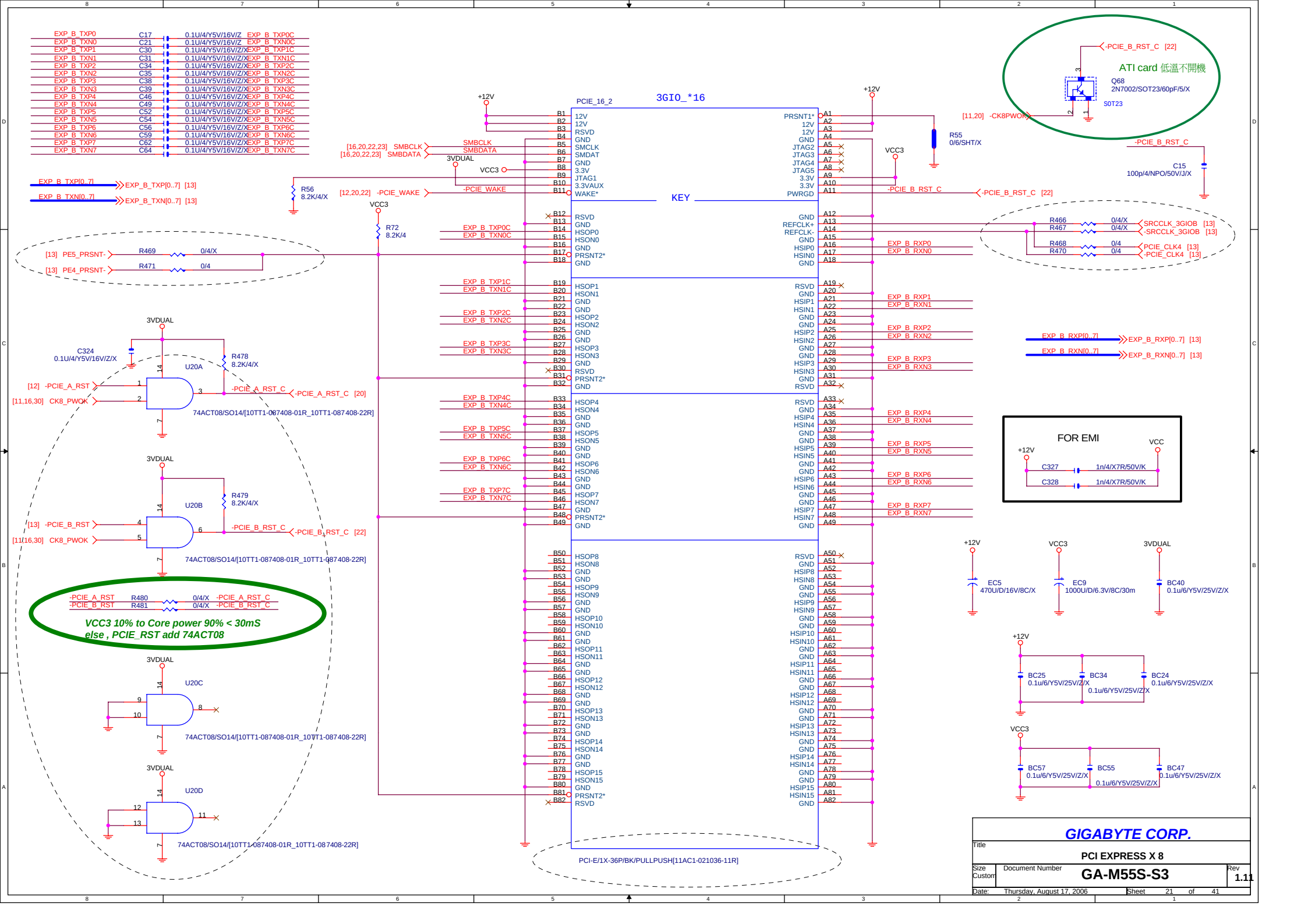
GIGABYTE CORP.

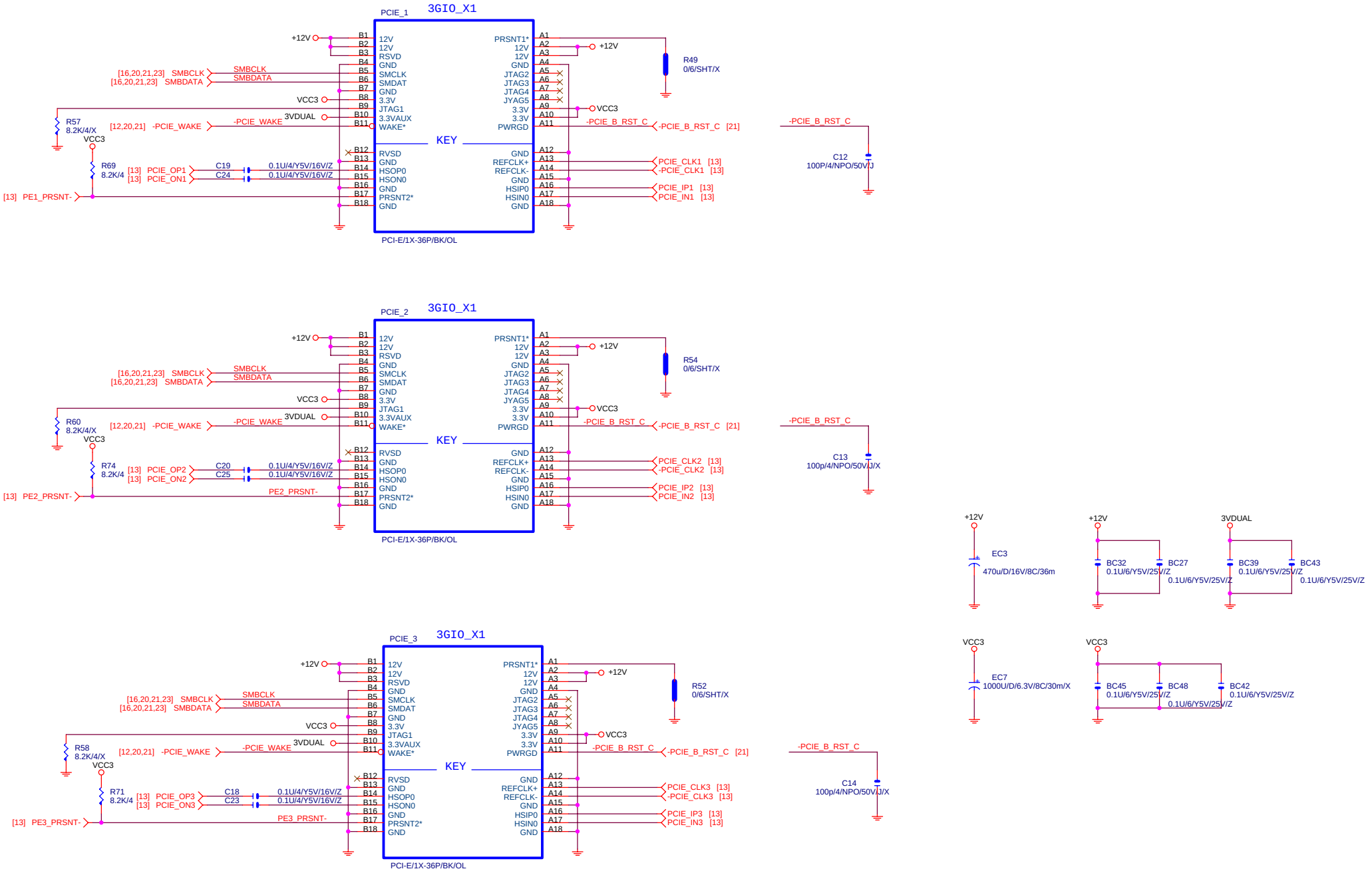
Title: MCP55 DECOUPLING

Size: Custom | Document Number: GA-M55S-S3 | Rev: 1.11

Date: Thursday, August 17, 2006 | Sheet 19 of 41

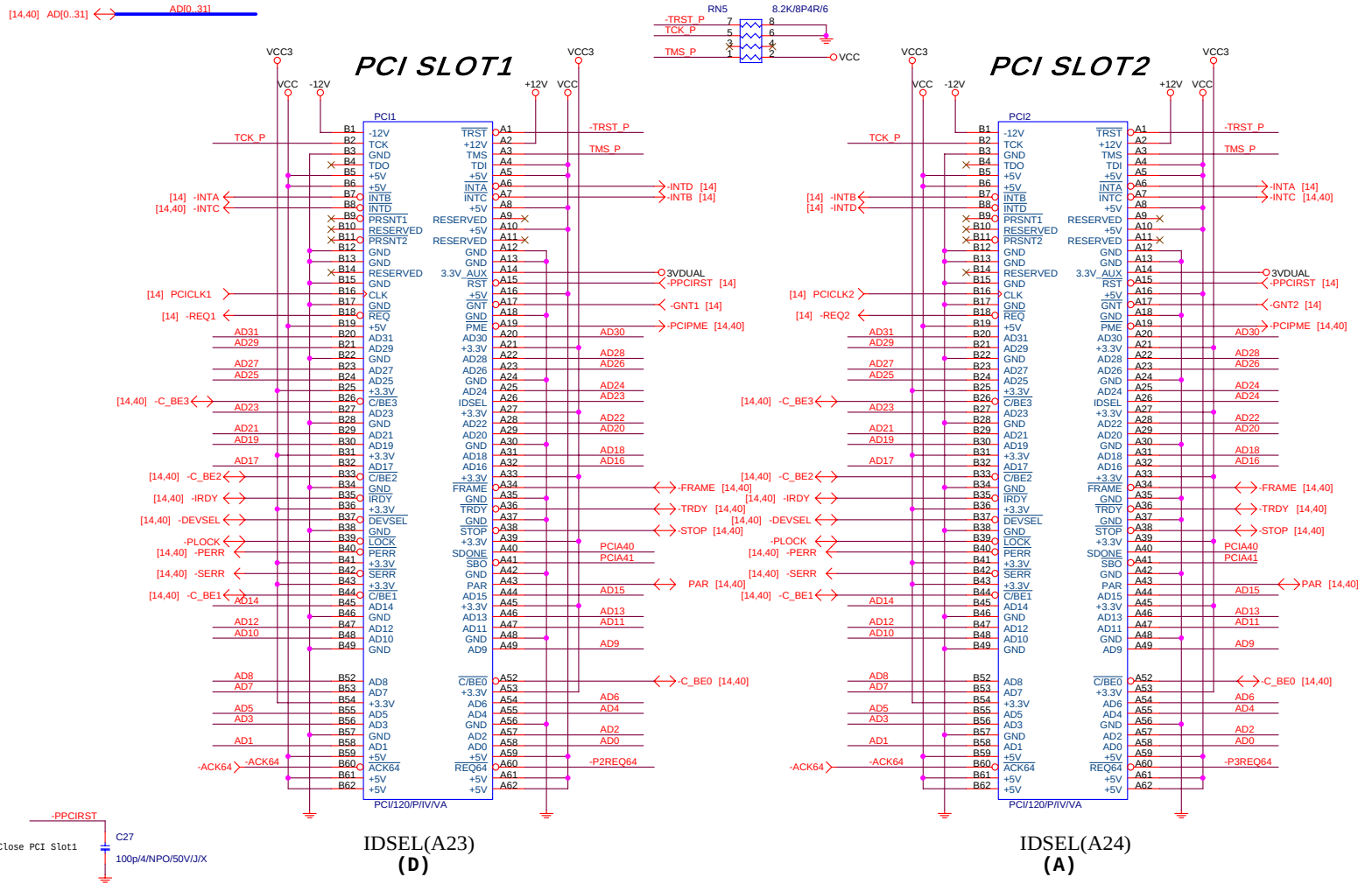

PCIE_12V
+12V
GND
GND
+5V
APW/1*4/BK/OC/P/5.08/VA/SN/OH
PCIE_16_1
3GIO_*16
KEY
ATI card 低溫不開機
Q67
2N7002/SOT23/60pF/5/X
S0T23
-PCIE_A_RST_C [21]
[11,21] -CK8PWOK
R51
0/6/SHT/X
-PCIE_A_RST_C
C16
100P/4/NPO/50V/J
SMBCLK
SMBDATA
3VDUAL
VCC3
-PCIE_WAKE
R64
8.2K/4/X
R73
8.2K/4
PE0_PRSNT-
SRCCLK_3GIOA [12]
-SRCCLK_3GIOA [12]
EXP_A_RXP[0..7]
EXP_A_RXN[0..7]
EXP_A_TXP[0..7]
EXP_A_TXN[0..7]
EC2
470u/D/16V/8C/36m
EC4
470u/D/16V/8C/36m
EC6
1000U/D/6.3V/8C/30m
BC38
0.1U/6/Y5V/25V/Z
EXP_A_RXP[8..15]
EXP_A_RXN[8..15]
EXP_A_TXP[8..15]
EXP_A_TXN[8..15]
BC33
0.1U/6/Y5V/25V/Z
BC35
0.1U/6/Y5V/25V/Z
BC46
0.1U/6/Y5V/25V/Z
BC44
0.1U/6/Y5V/25V/Z
BC41
0.1U/6/Y5V/25V/Z
FOR EMI
BC30
0.1U/6/Y5V/25V/Z
PCI-E/16X-164P/BU-297C/PULLPUSH/[11AC1-021164-A1R]
GIGABYTE CORP.
Title
PCI EXPRESS X 16
Size
Custom
Document Number
GA-M55S-S3
Rev
1.11
Date:
Thursday, August 17, 2006
Sheet
20
of
41


EXP_B_TXP0 C17 0.1U/4/Y5V/16V/Z EXP_B_TXP0C
EXP_B_TXN0 C21 0.1U/4/Y5V/16V/Z EXP_B_TXN0C
EXP_B_TXP1 C30 0.1U/4/Y5V/16V/Z/X EXP_B_TXP1C
EXP_B_TXN1 C31 0.1U/4/Y5V/16V/Z/X EXP_B_TXN1C
EXP_B_TXP2 C34 0.1U/4/Y5V/16V/Z/X EXP_B_TXP2C
EXP_B_TXN2 C35 0.1U/4/Y5V/16V/Z/X EXP_B_TXN2C
EXP_B_TXP3 C38 0.1U/4/Y5V/16V/Z/X EXP_B_TXP3C
EXP_B_TXN3 C39 0.1U/4/Y5V/16V/Z/X EXP_B_TXN3C
EXP_B_TXP4 C46 0.1U/4/Y5V/16V/Z/X EXP_B_TXP4C
EXP_B_TXN4 C49 0.1U/4/Y5V/16V/Z/X EXP_B_TXN4C
EXP_B_TXP5 C52 0.1U/4/Y5V/16V/Z/X EXP_B_TXP5C
EXP_B_TXN5 C54 0.1U/4/Y5V/16V/Z/X EXP_B_TXN5C
EXP_B_TXP6 C56 0.1U/4/Y5V/16V/Z/X EXP_B_TXP6C
EXP_B_TXN6 C59 0.1U/4/Y5V/16V/Z/X EXP_B_TXN6C
EXP_B_TXP7 C62 0.1U/4/Y5V/16V/Z/X EXP_B_TXP7C
EXP_B_TXN7 C64 0.1U/4/Y5V/16V/Z/X EXP_B_TXN7C
EXP_B_TXP[0..7] EXP_B_TXP[0..7] [13]
EXP_B_TXN[0..7] EXP_B_TXN[0..7] [13]
R56 8.2K/4/X
[12,20,22] -PCIE_WAKE
-PCIE_WAKE
SMBCLK
SMBDATA
[16,20,22,23] SMBCLK
[16,20,22,23] SMBDATA
3VDUAL
VCC3
+12V
PCIE_16_2
3GIO_*16
KEY
12V
RSVD
GND
SMCLK
SMDAT
JTAG1
3.3VAUX
WAKE*
PRSNT1*
JTAG2
JTAG3
JTAG4
JTAG5
3.3V
PWRGD
REFCLK+
REFCLK-
HSOP0
HSON0
PRSNT2*
HSIP0
HSIN0
HSOP1
HSON1
HSIP1
HSIN1
HSOP2
HSON2
HSIP2
HSIN2
HSOP3
HSON3
HSIP3
HSIN3
HSOP4
HSON4
HSIP4
HSIN4
HSOP5
HSON5
HSIP5
HSIN5
HSOP6
HSON6
HSIP6
HSIN6
HSOP7
HSON7
HSIP7
HSIN7
HSOP8
HSON8
HSIP8
HSIN8
HSOP9
HSON9
HSIP9
HSIN9
HSOP10
HSON10
HSIP10
HSIN10
HSOP11
HSON11
HSIP11
HSIN11
HSOP12
HSON12
HSIP12
HSIN12
HSOP13
HSON13
HSIP13
HSIN13
HSOP14
HSON14
HSIP14
HSIN14
HSOP15
HSON15
HSIP15
HSIN15
PCI-E/1X-36P/BK/PULLPUSH[11AC1-021036-11R]
R55 0/6/SHT/X
[11,20] -CK8PWOK
-PCIE_B_RST_C [22]
ATI card 低溫不開機
Q68 2N7002/SOT23/60pF/5/X
S0T23
C15 100p/4/NPO/50V/J/X
-PCIE_B_RST_C
VCC3
R72 8.2K/4
R466 0/4/X SRCCLK_3GIOB [13]
R467 0/4/X -SRCCLK_3GIOB [13]
R468 0/4 PCIE_CLK4 [13]
R470 0/4 -PCIE_CLK4 [13]
[13] PE5_PRSNT- R469 0/4/X
[13] PE4_PRSNT- R471 0/4
C324 0.1U/4/Y5V/16V/Z/X
R478 8.2K/4/X
U20A
[12] -PCIE_A_RST
[11,16,30] CK8_PWOK
-PCIE_A_RST_C
-PCIE_A_RST_C [20]
74ACT08/SO14/[10TT1-087408-01R_10TT1-087408-22R]
R479 8.2K/4/X
U20B
[13] -PCIE_B_RST
[11,16,30] CK8_PWOK
-PCIE_B_RST_C
-PCIE_B_RST_C [22]
-PCIE_A_RST R480 0/4/X -PCIE_A_RST_C
-PCIE_B_RST R481 0/4/X -PCIE_B_RST_C
VCC3 10% to Core power 90% < 30mS
else , PCIE_RST add 74ACT08
U20C
U20D
EXP_B_RXP0
EXP_B_RXN0
EXP_B_RXP1
EXP_B_RXN1
EXP_B_RXP2
EXP_B_RXN2
EXP_B_RXP3
EXP_B_RXN3
EXP_B_RXP4
EXP_B_RXN4
EXP_B_RXP5
EXP_B_RXN5
EXP_B_RXP6
EXP_B_RXN6
EXP_B_RXP7
EXP_B_RXN7
EXP_B_RXP[0..7] EXP_B_RXP[0..7] [13]
EXP_B_RXN[0..7] EXP_B_RXN[0..7] [13]
FOR EMI
VCC
C327 1n/4/X7R/50V/K
C328 1n/4/X7R/50V/K
EC5 470U/D/16V/8C/X
EC9 1000U/D/6.3V/8C/30m
BC40 0.1u/6/Y5V/25V/Z/X
BC25 0.1u/6/Y5V/25V/Z/X
BC34 0.1u/6/Y5V/25V/Z/X
BC24 0.1u/6/Y5V/25V/Z/X
BC57 0.1u/6/Y5V/25V/Z/X
BC55 0.1u/6/Y5V/25V/Z/X
BC47 0.1u/6/Y5V/25V/Z/X
GIGABYTE CORP.
Title
PCI EXPRESS X 8
Size Custom
Document Number
GA-M55S-S3
Rev 1.11
Date: Thursday, August 17, 2006
Sheet 21 of 41

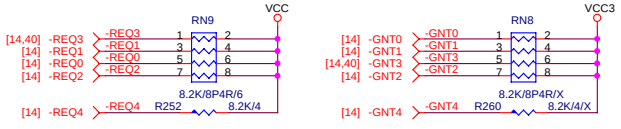


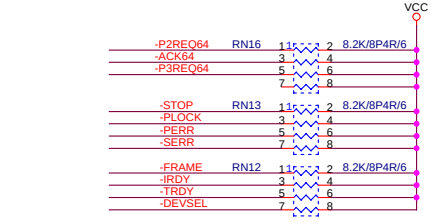
GIGABYTE CORP.		
Title: PCI E SLOT 1, 2		
Size: B	Document Number: GA-M55S-S3	Rev: 1.11
Date: Thursday, August 17, 2006	Sheet 22 of 41	

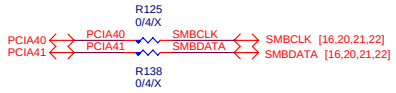
PCI SLOT 1,2

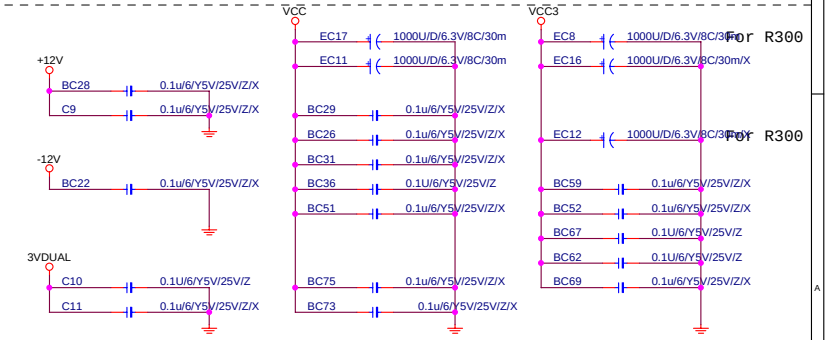


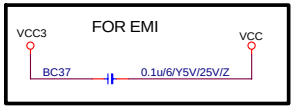
-PPCIRST
Close PCI Slot1
C27
100p/4/NPO/50V/J/X







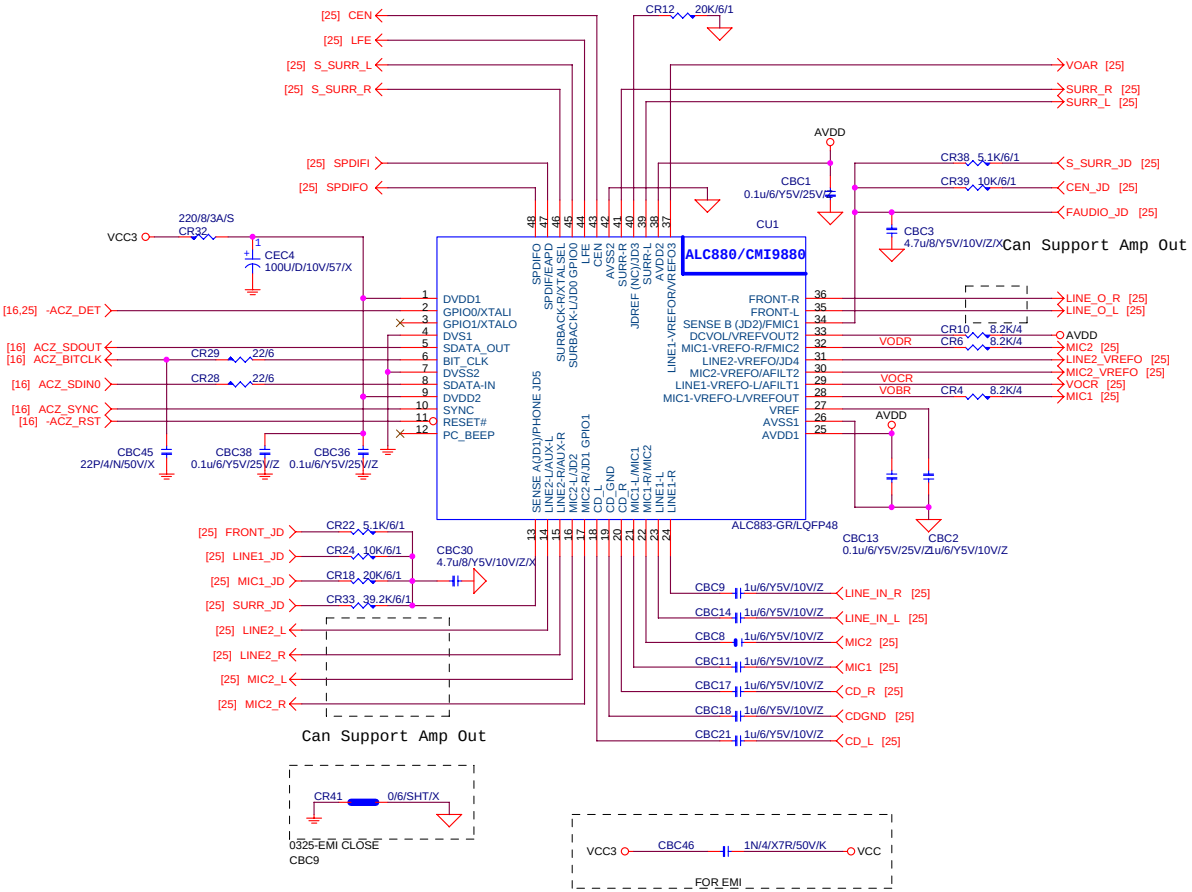




GIGABYTE CORP.

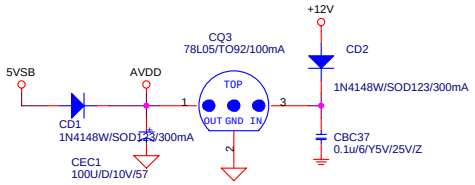
Title	PCI SLOT 1,2	
Size: Custom	Document Number: GA-M55S-S3	Rev: 1.11
Date: Thursday, August 17, 2006	Sheet 23 of 41	

AZALIA CODEC

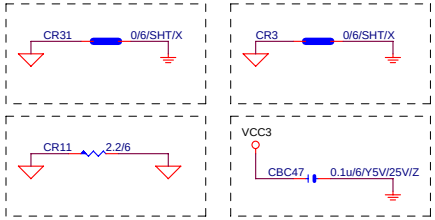


GIGABYTE CORP.		
Title: AZALIA-ALC883		
Size: Custom	Document Number: GA-M55S-S3	Rev: 1.11
Date: Thursday, August 17, 2006	Sheet 24 of 41	

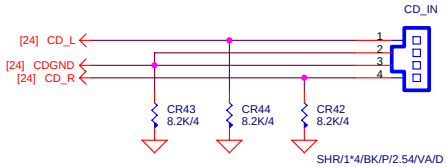
CODEC POWER/EMI PAD

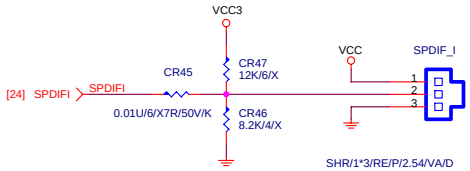


FOR EMI

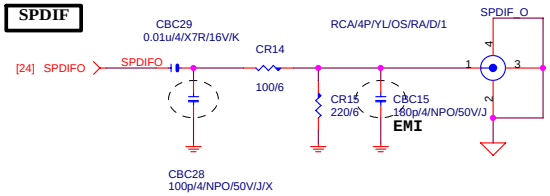


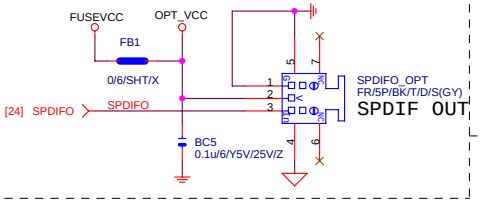
CD IN





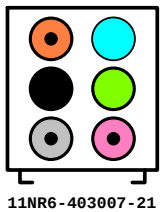
SPDIF



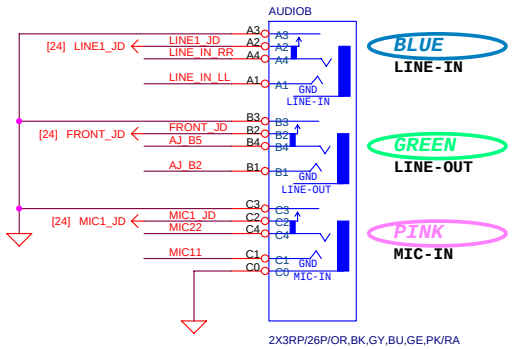


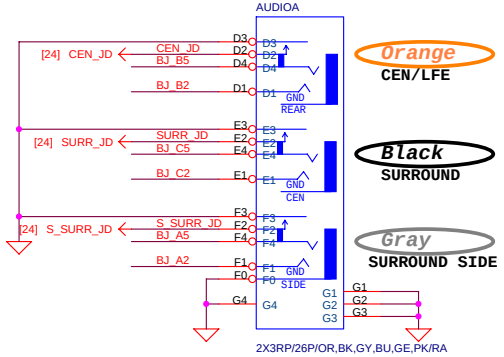
AZALIA JACK

BTX AZALIA CONNECTOR

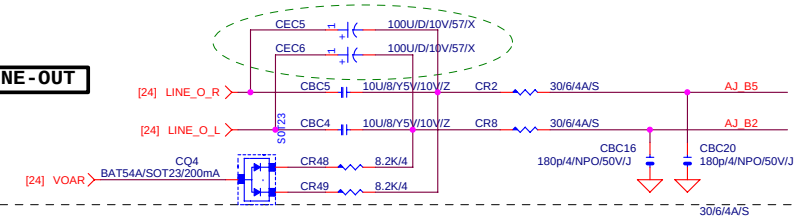


11NR6-403007-21

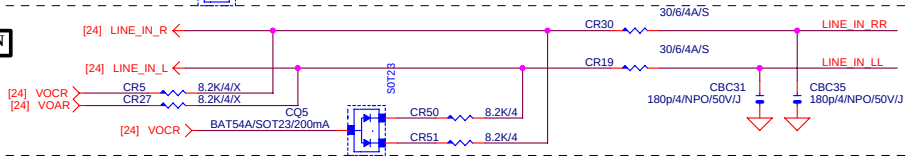




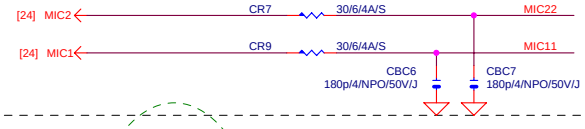
LINE-OUT



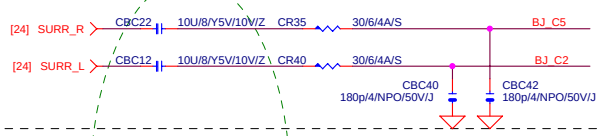
LINE-IN



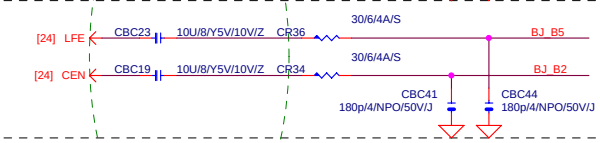
MIC-IN



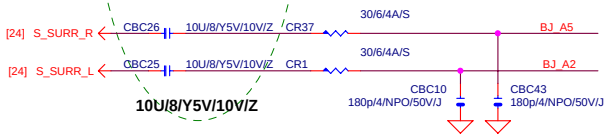
SURROUND



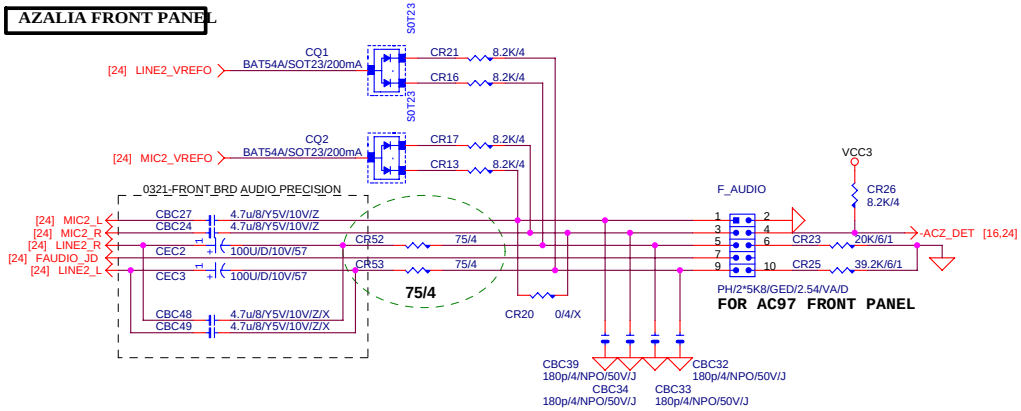
CEN/LFE



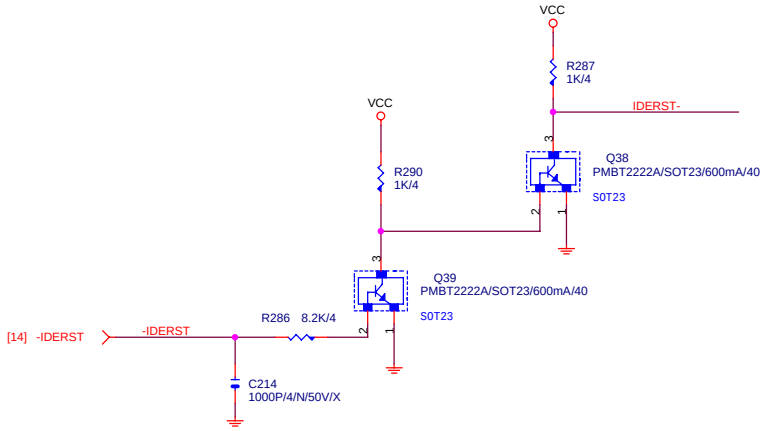
SURR BACK

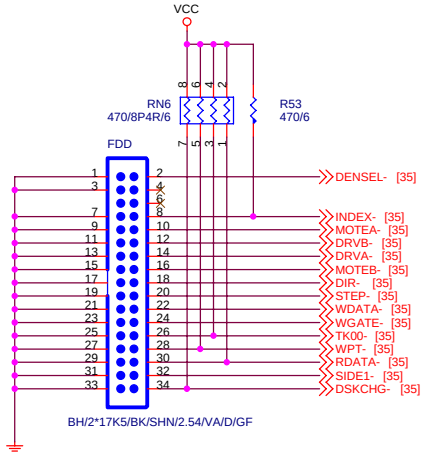


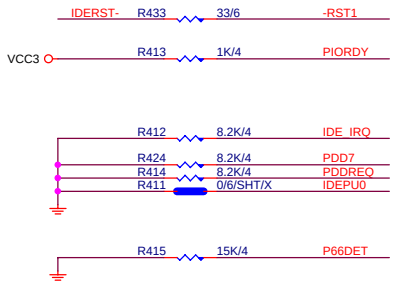
AZALIA FRONT PANEL



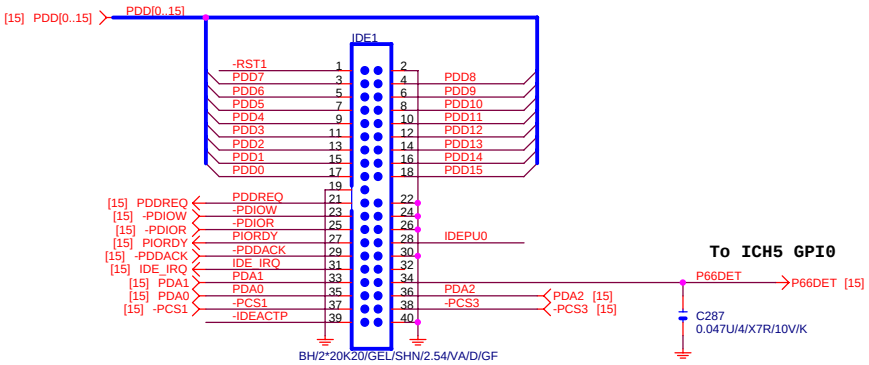
GIGABYTE CORP.			
Title: AUDIO JACK			
Size: Custom	Document Number: GA-M55S-S3		Rev: 1.11
Date: Thursday, August 17, 2006	Sheet 25 of 41		





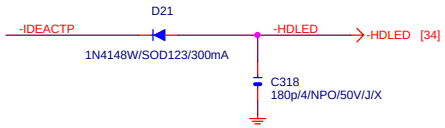


PRIMARY IDE CONNECTOR



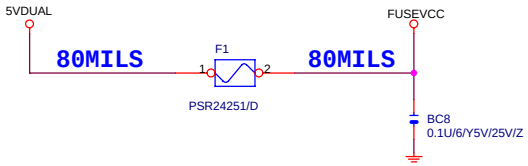
To ICH5 GPI0

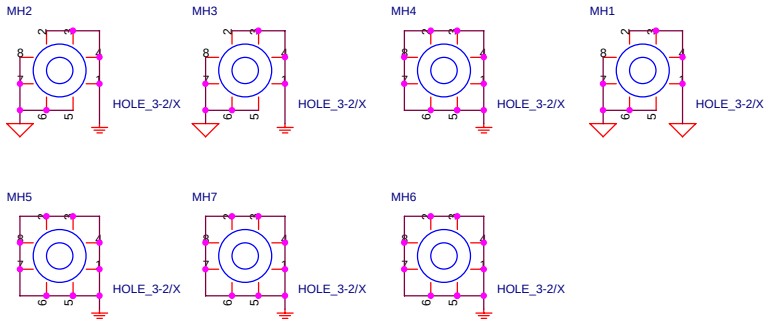
Close to connector

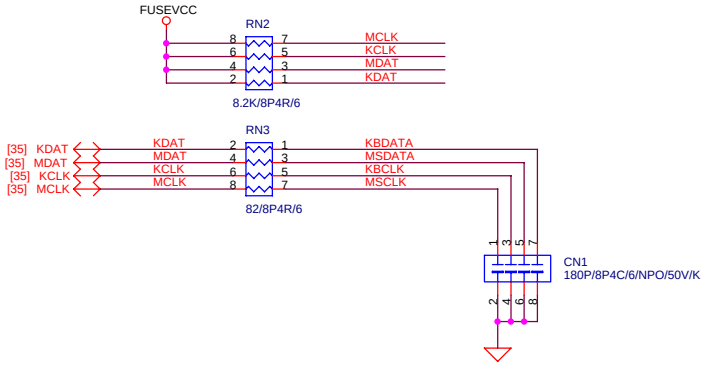


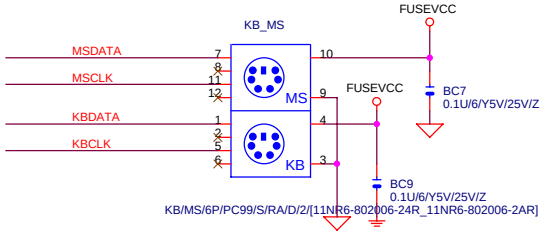
GIGABYTE CORP.

Title: IDE CONNECTOR		
Size: B	Document Number: GA-M55S-S3	Rev: 1.11
Date:	Sheet 26 of 41	



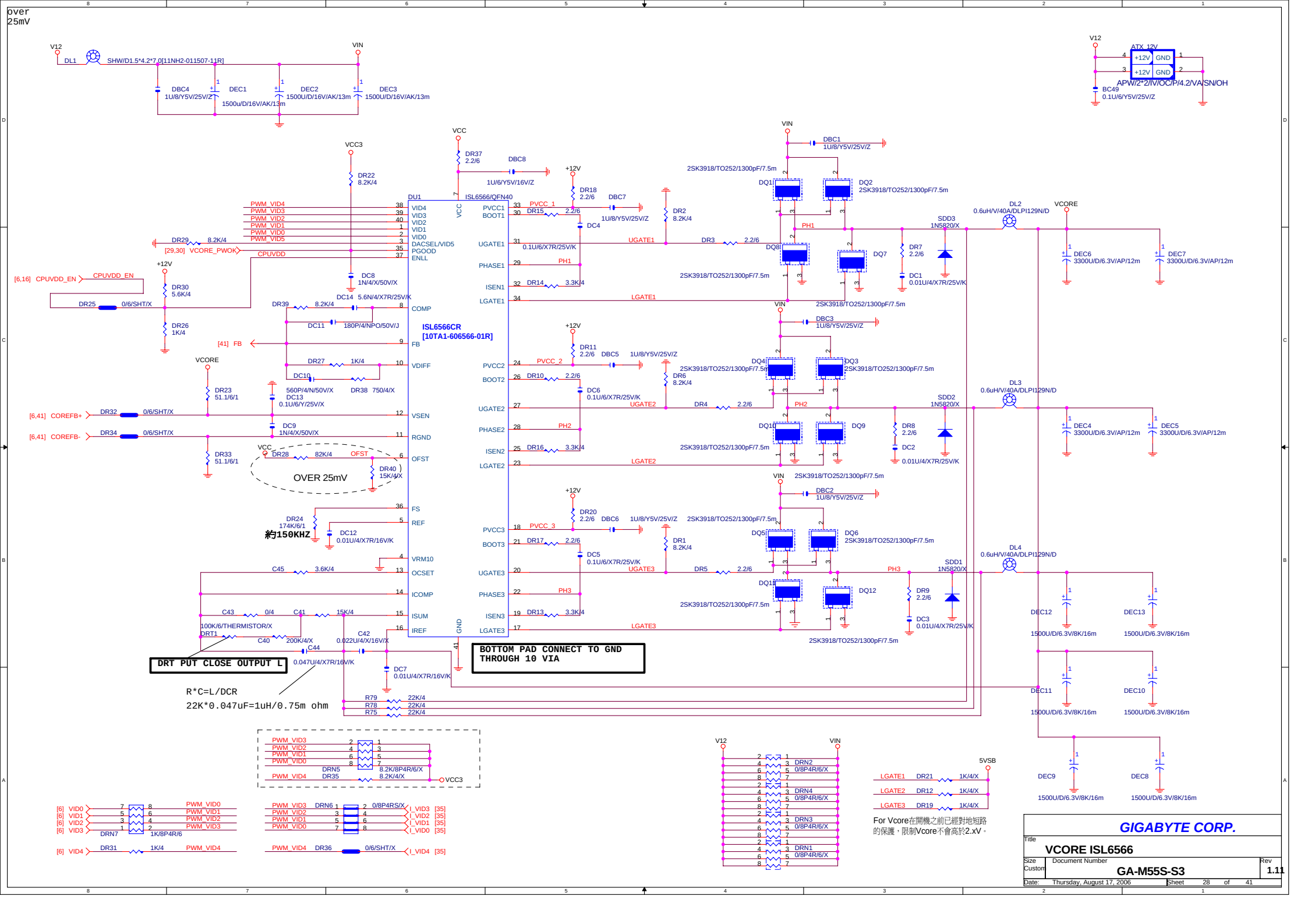


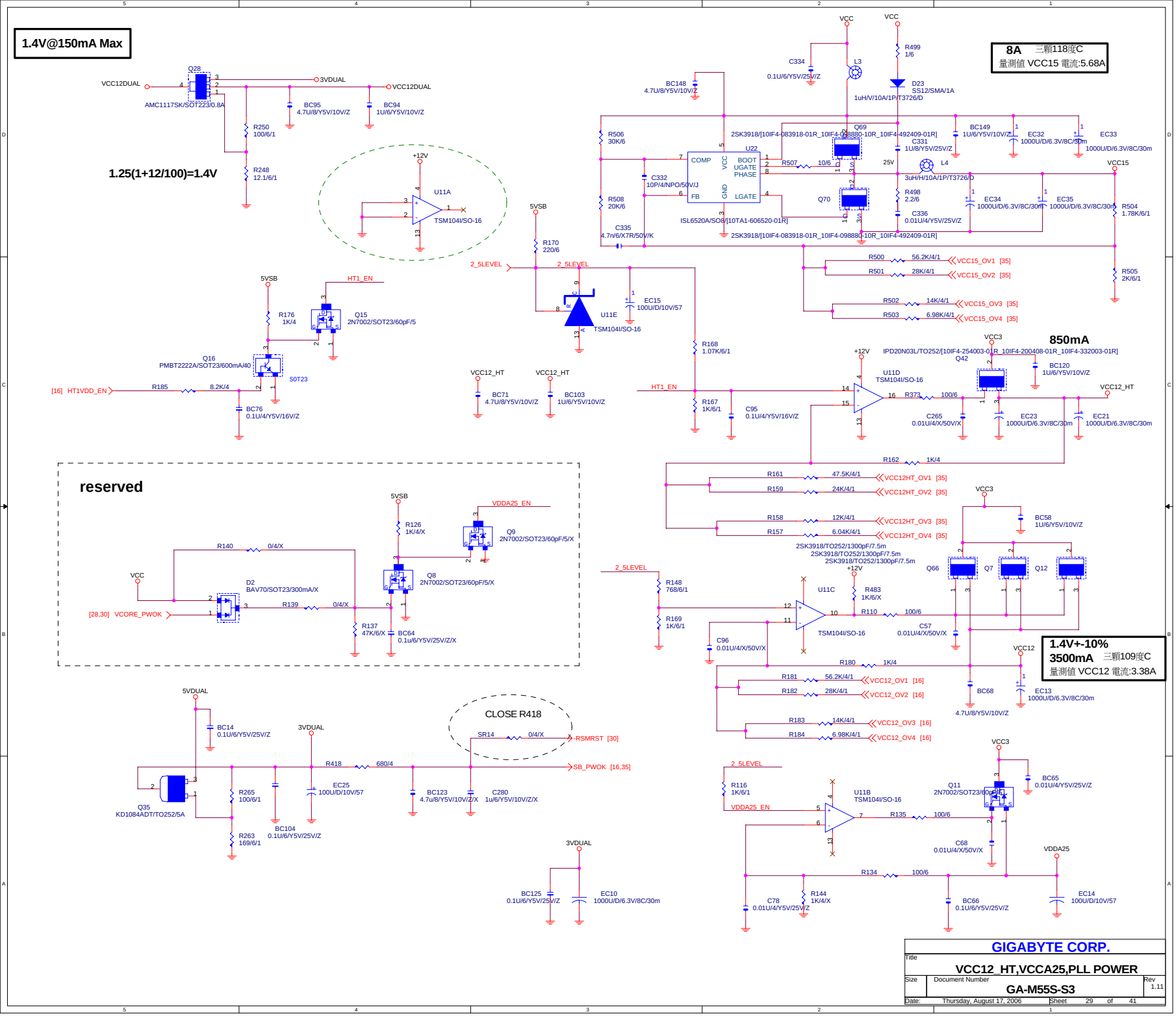


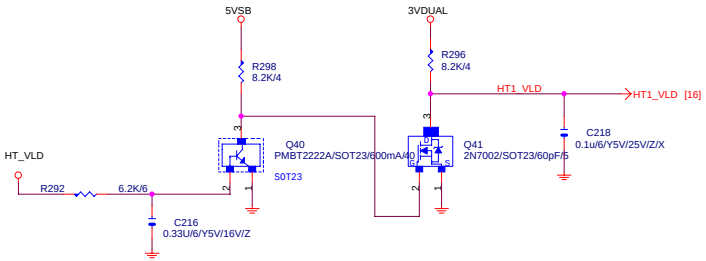


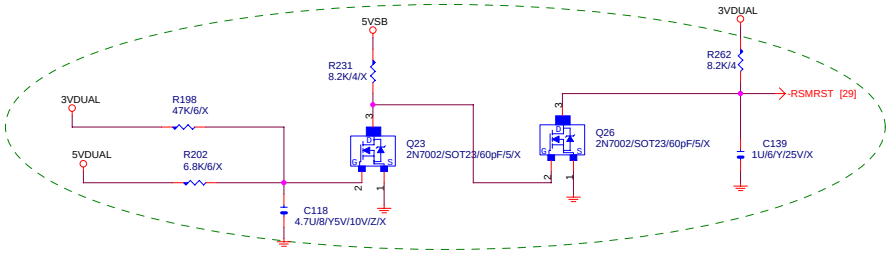
GIGABYTE CORP.

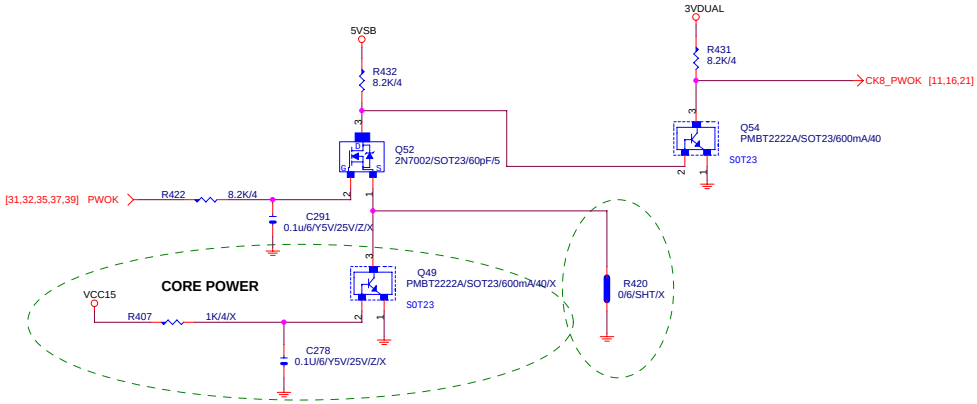
Title	KB & PS2 MOUSE & IR	
Size: B	Document Number: GA-M55S-S3	Rev: 1.11
Date:	Sheet 27 of 41	


over
25mV
ISL6566CR
[10TA1-606566-01R]
ISL6566/QFN40
OVER 25mV
約150KHZ
DRT PUT CLOSE OUTPUT L
BOTTOM PAD CONNECT TO GND
THROUGH 10 VIA
R*C=L/DCR
22K*0.047uF=1uH/0.75m ohm
APW/2*2/IV/OC/P/4.2/VA/SN/OH
For Vcore在開機之前已經對地短路
的保護，限制Vcore不會高於2.xV。
GIGABYTE CORP.
VCORE ISL6566
GA-M55S-S3
1.11
Thursday, August 17, 2006
Sheet 28 of 41

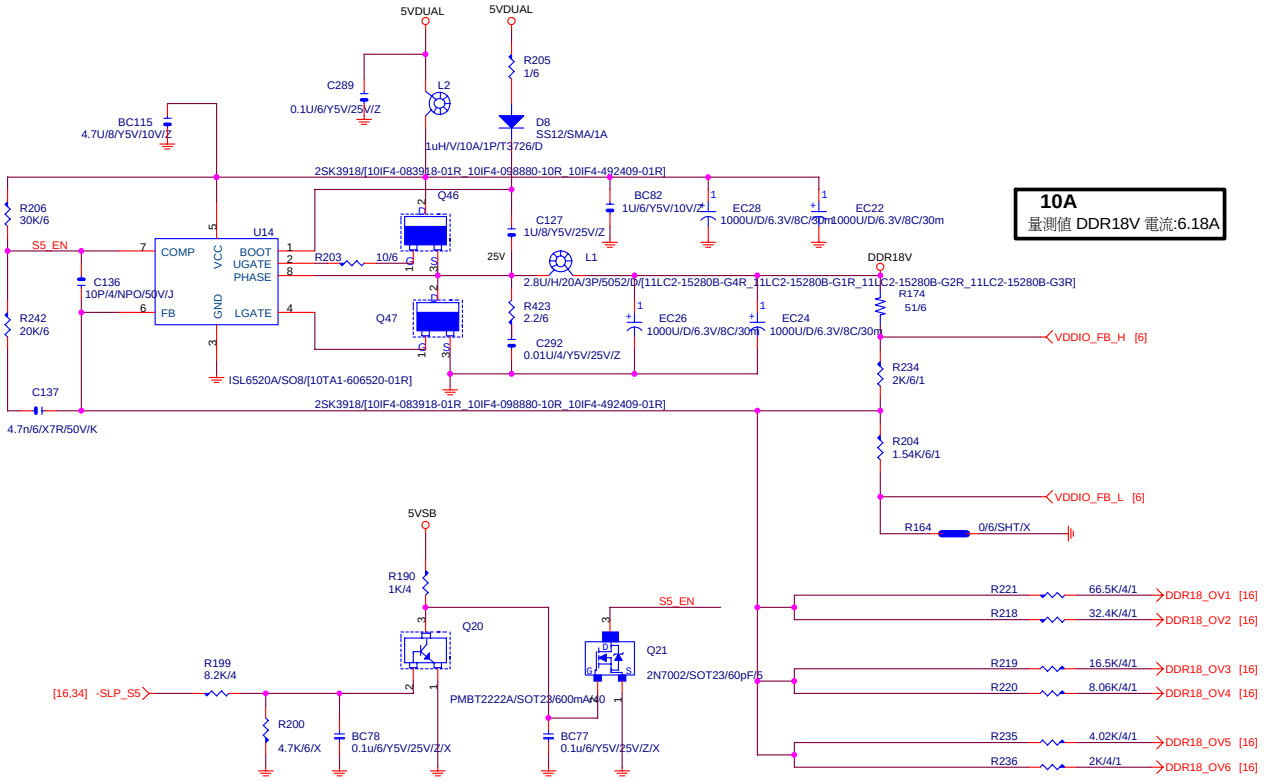

1.4V@150mA Max
VCC12DUAL
Q28
AMC1117SK/SOT223/0.8A
3VDUAL
VCC12DUAL
BC95
4.7U/8/Y5V/10V/Z
BC94
1U/6/Y5V/10V/Z
R250
100/6/1
R248
12.1/6/1
1.25(1+12/100)=1.4V
+12V
U11A
TSM104I/SO-16
5VSB
R170
220/6
2_5LEVEL
U11E
TSM104I/SO-16
EC15
100U/D/10V/57
C335
4.7n/6/X7R/50V/K
R506
30K/6
R508
20K/6
C332
10P/4/NPO/50V/J
U22
ISL6520A/SO8/[10TA1-606520-01R]
2SK3918/[10IF4-083918-01R_10IF4-088880-10R_10IF4-492409-01R]
R507
10/6
Q69
Q70
C331
1U/8/Y5V/25V/Z
C336
0.01U/4/Y5V/25V/Z
25V
L4
3uH/H/10A/1P/T3726/D
R498
2.2/6
VCC15
EC34
1000U/D/6.3V/8C/30m
EC35
1000U/D/6.3V/8C/30m
R504
1.78K/6/1
R505
2K/6/1
R500
56.2K/4/1
VCC15_OV1 [35]
R501
28K/4/1
VCC15_OV2 [35]
R502
14K/4/1
VCC15_OV3 [35]
R503
6.98K/4/1
VCC15_OV4 [35]
L3
1uH/V/10A/1P/T3726/D
D23
SS12/SMA/1A
R499
1/6
C334
0.1U/6/Y5V/25V/Z
BC148
4.7U/8/Y5V/10V/Z
BC149
1U/6/Y5V/10V/Z
EC32
1000U/D/6.3V/8C/30m
EC33
1000U/D/6.3V/8C/30m
8A 三顆118度C
量測值 VCC15 電流:5.68A
5VSB
HT1_EN
R176
1K/4
Q15
2N7002/SOT23/60pF/5
Q16
PMBT2222A/SOT23/600mA/40
S0T23
[16] HT1VDD_EN
R185
8.2K/4
BC76
0.1U/4/Y5V/16V/Z
VCC12_HT
BC71
4.7U/8/Y5V/10V/Z
VCC12_HT
BC103
1U/6/Y5V/10V/Z
R168
1.07K/6/1
HT1_EN
R167
1K/6/1
C95
0.1U/4/Y5V/16V/Z
+12V
U11D
TSM104I/SO-16
IPD20N03L/TO252/[10IF4-254003-01R_10IF4-200408-01R_10IF4-332003-01R]
Q42
850mA
VCC3
BC120
1U/6/Y5V/10V/Z
VCC12_HT
R373
100/6
C265
0.01U/4/X/50V/X
EC23
1000U/D/6.3V/8C/30m
EC21
1000U/D/6.3V/8C/30m
R162
1K/4
R161
47.5K/4/1
VCC12HT_OV1 [35]
R159
24K/4/1
VCC12HT_OV2 [35]
R158
12K/4/1
VCC12HT_OV3 [35]
R157
6.04K/4/1
VCC12HT_OV4 [35]
2SK3918/TO252/1300pF/7.5m
2SK3918/TO252/1300pF/7.5m
2SK3918/TO252/1300pF/7.5m
VCC3
BC58
1U/6/Y5V/10V/Z
Q66
Q7
Q12
reserved
5VSB
R126
1K/4/X
VDDA25_EN
Q9
2N7002/SOT23/60pF/5/X
R140
0/4/X
VCC
D2
BAV70/SOT23/300mA/X
[28,30] VCORE_PWOK
R139
0/4/X
Q8
2N7002/SOT23/60pF/5/X
R137
47K/6/X
BC64
0.1u/6/Y5V/25V/Z/X
2_5LEVEL
R148
768/6/1
R169
1K/6/1
C96
0.01U/4/X/50V/X
+12V
U11C
TSM104I/SO-16
R483
1K/6/X
R110
100/6
C57
0.01U/4/X/50V/X
1.4V+-10%
3500mA 三顆109度C
量測值 VCC12 電流:3.38A
VCC12
R180
1K/4
R181
56.2K/4/1
VCC12_OV1 [16]
R182
28K/4/1
VCC12_OV2 [16]
R183
14K/4/1
VCC12_OV3 [16]
R184
6.98K/4/1
VCC12_OV4 [16]
BC68
4.7U/8/Y5V/10V/Z
EC13
1000U/D/6.3V/8C/30m
5VDUAL
BC14
0.1U/6/Y5V/25V/Z
3VDUAL
CLOSE R418
SR14
0/4/X
RSMRST [30]
R418
680/4
SB_PWOK [16,35]
Q35
KD1084ADT/TO252/5A
R265
100/6/1
R263
169/6/1
BC104
0.1U/6/Y5V/25V/Z
EC25
100U/D/10V/57
BC123
4.7u/8/Y5V/10V/Z/X
C280
1u/6/Y5V/10V/Z/X
3VDUAL
BC125
0.1U/6/Y5V/25V/Z
EC10
1000U/D/6.3V/8C/30m
2_5LEVEL
R116
1K/6/1
VDDA25_EN
U11B
TSM104I/SO-16
R135
100/6
Q11
2N7002/SOT23/60pF
VCC3
BC65
0.01U/4/Y5V/25V/Z
C68
0.01U/4/X/50V/X
VDDA25
R134
100/6
C78
0.01U/4/Y5V/25V/Z
R144
1K/4/X
BC66
0.1U/6/Y5V/25V/Z
EC14
100U/D/10V/57
GIGABYTE CORP.
Title
VCC12_HT,VCCA25,PLL POWER
Size
Document Number
GA-M55S-S3
Rev
1.11
Date: Thursday, August 17, 2006
Sheet 29 of 41

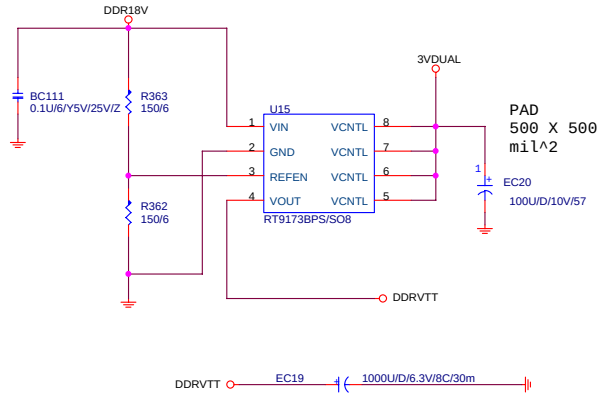


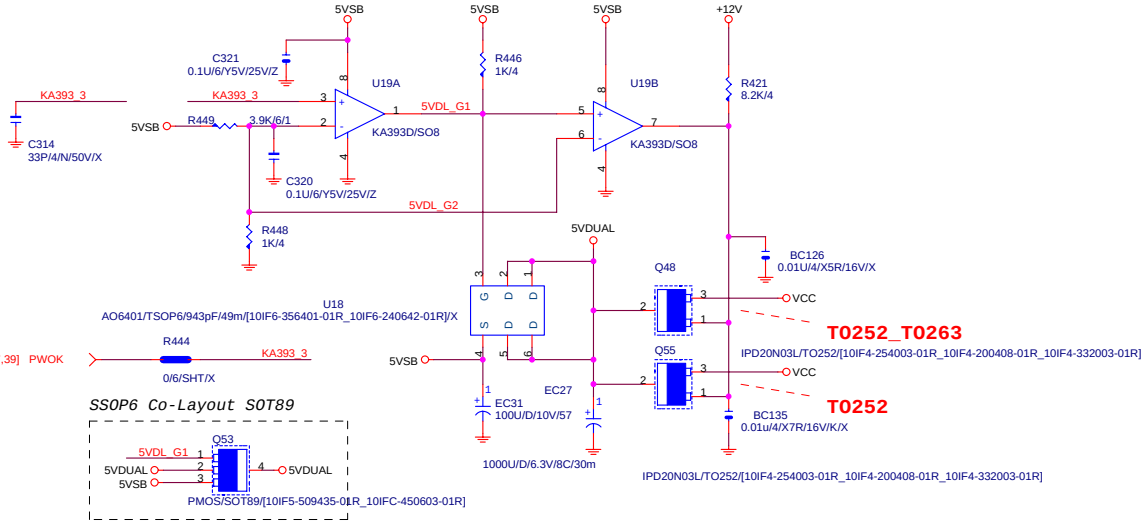




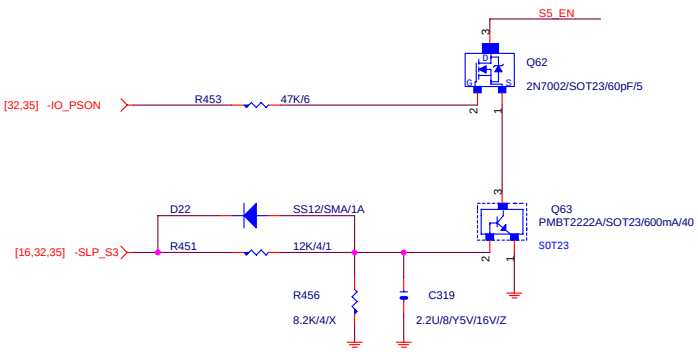
GIGABYTE CORP.		
Title: POWER SEQUENCE POWER		
Size	Document Number: GA-M55S-S3	Rev: 1.11
Date: Thursday, August 17, 2006	Sheet 30 of 41	







for G3 to G2 status



	G2	S5/S4	S3	S1/S0
-SLP_S5	H	L	H	H
-IO_PSON	H	H	H	L
-SLP_S3	H	L	L	H
DDR18V				

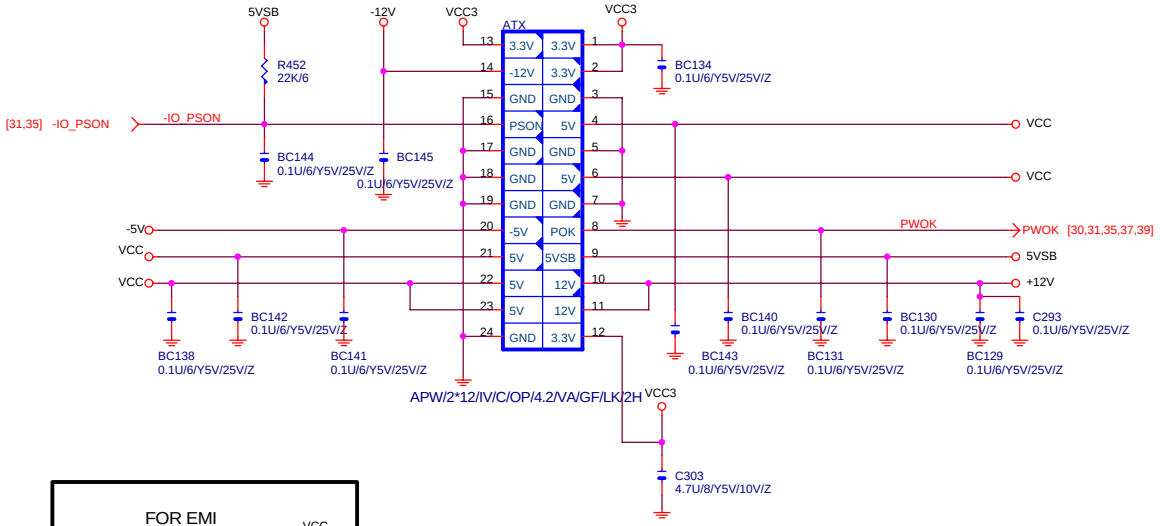
GIGABYTE CORP.

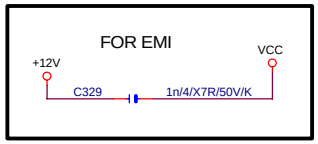
Title: DDR18 , DDRVTT , 5VDUAL

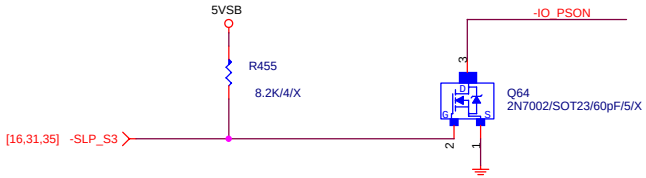
Size: Custom | Document Number: GA-M55S-S3 | Rev: 1.11

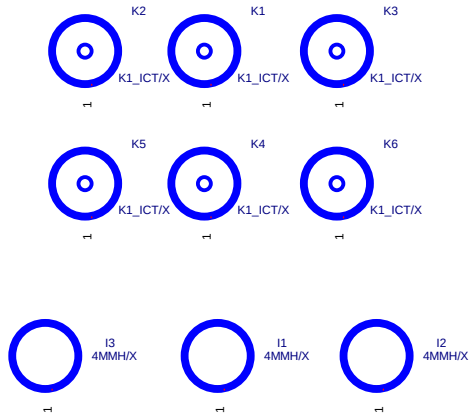
Date: Thursday, August 17, 2006 | Sheet 31 of 41

ATX POWER CONNECTOR



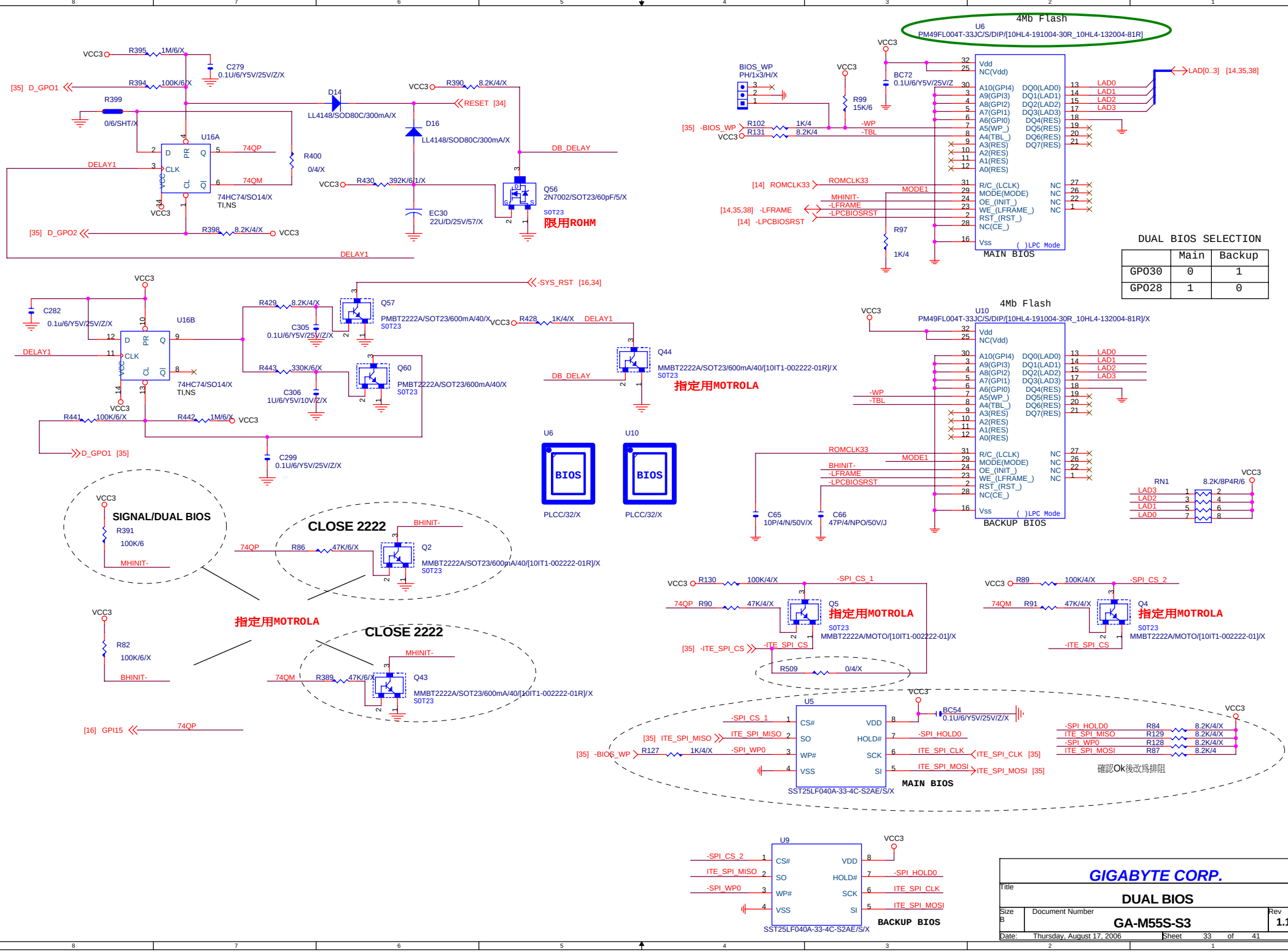


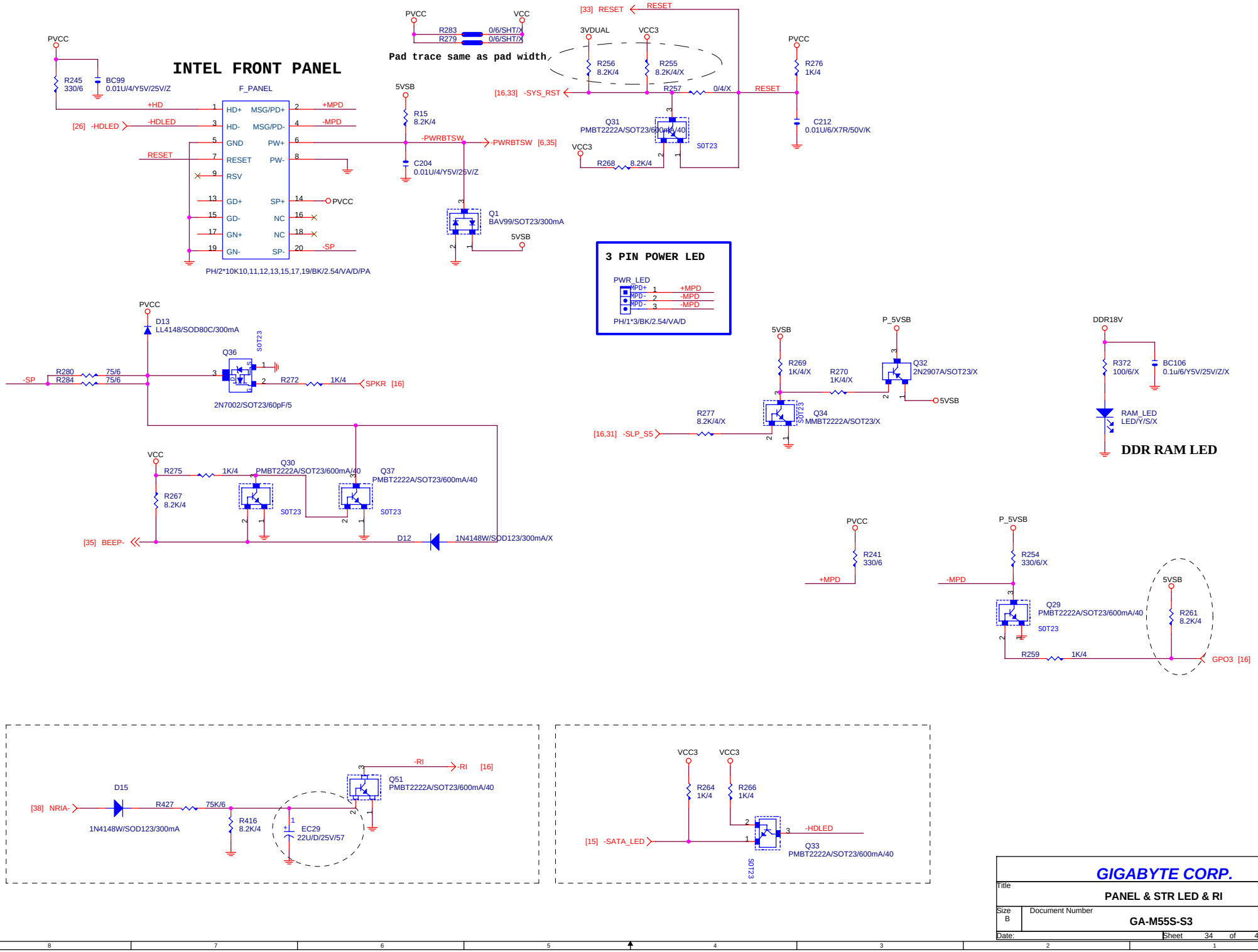




GIGABYTE CORP.

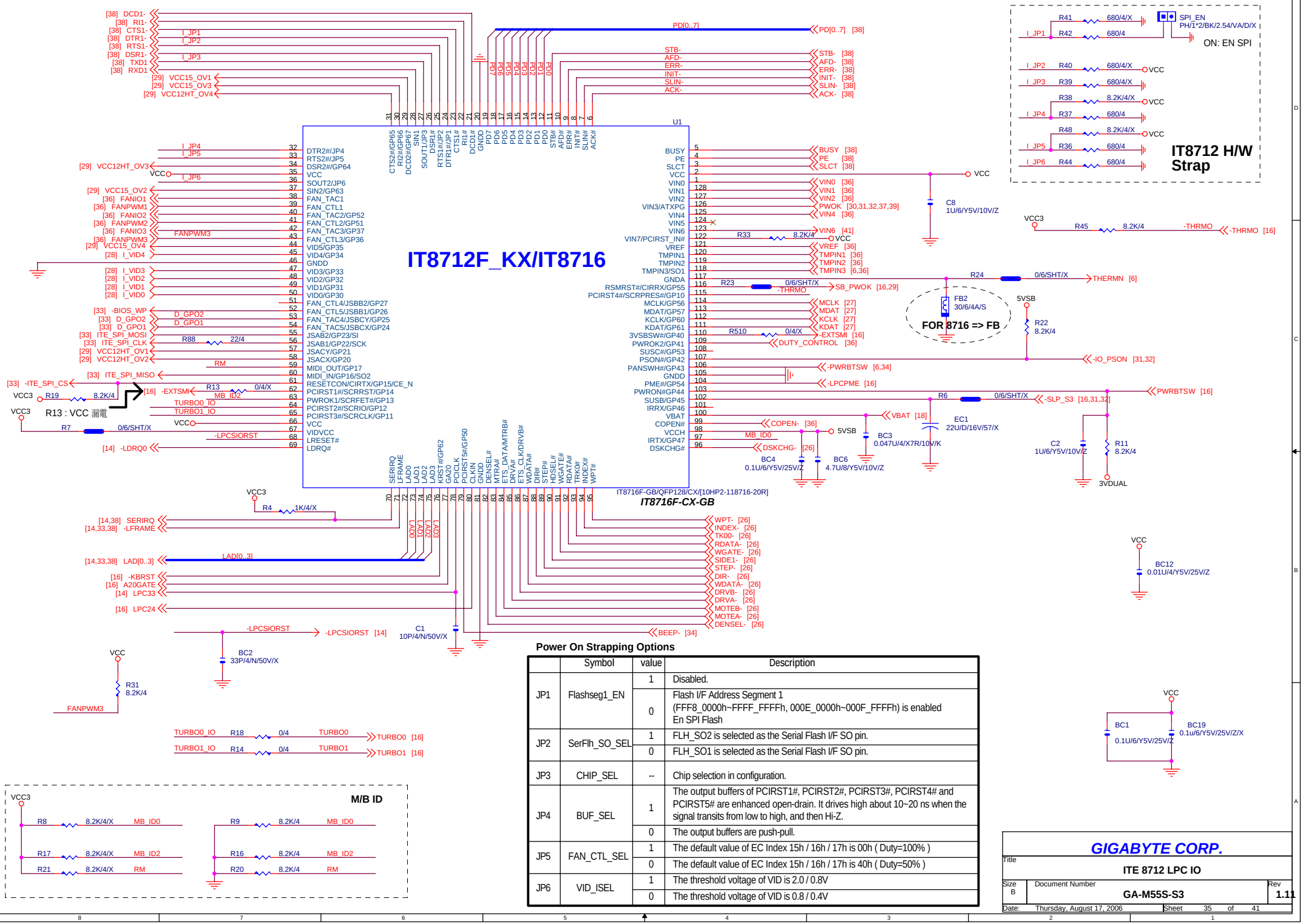
Title: Misc. PWR & ATX CONN.		
Size: B	Document Number: GA-M55S-S3	Rev: 1.11
Date:	Sheet 32 of 41	


4Mb Flash
U6
PM49FL004T-33JC/S/DIP/[10HL4-191004-30R_10HL4-132004-81R]
MAIN BIOS
DUAL BIOS SELECTION
Main
Backup
GPO30
0
1
GPO28
1
0
4Mb Flash
U10
PM49FL004T-33JC/S/DIP/[10HL4-191004-30R_10HL4-132004-81R]/X
BACKUP BIOS
限用ROHM
指定用MOTROLA
SIGNAL/DUAL BIOS
CLOSE 2222
MAIN BIOS
BACKUP BIOS
SST25LF040A-33-4C-S2AE/S/X
確認Ok後改爲排阻
GIGABYTE CORP.
DUAL BIOS
GA-M55S-S3
1.11
Thursday, August 17, 2006
33 of 41



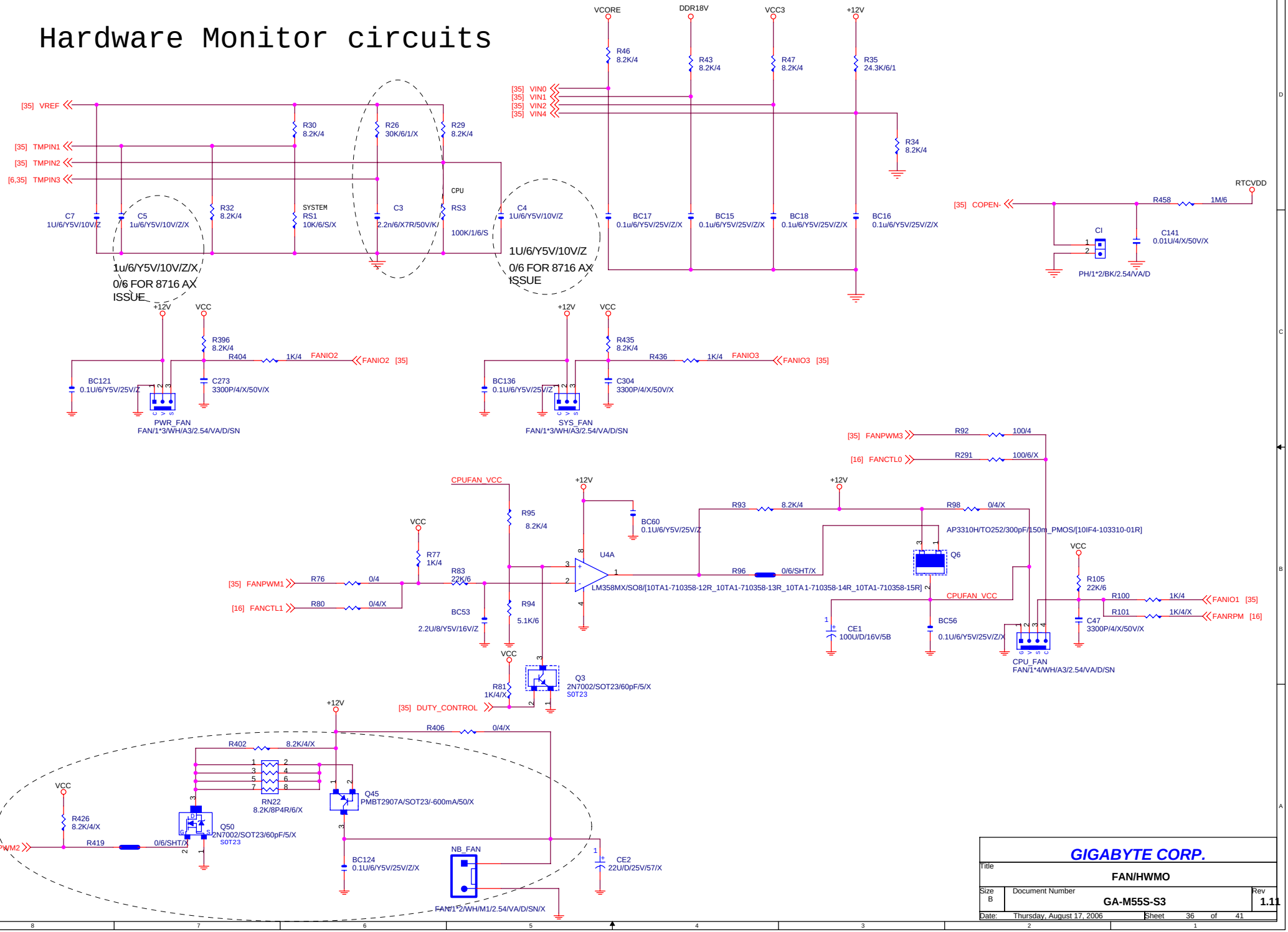
GIGABYTE CORP.

Title	PANEL & STR LED & RI	
Size B	Document Number GA-M55S-S3	Rev 1.11
Date:	Sheet 34 of 41	



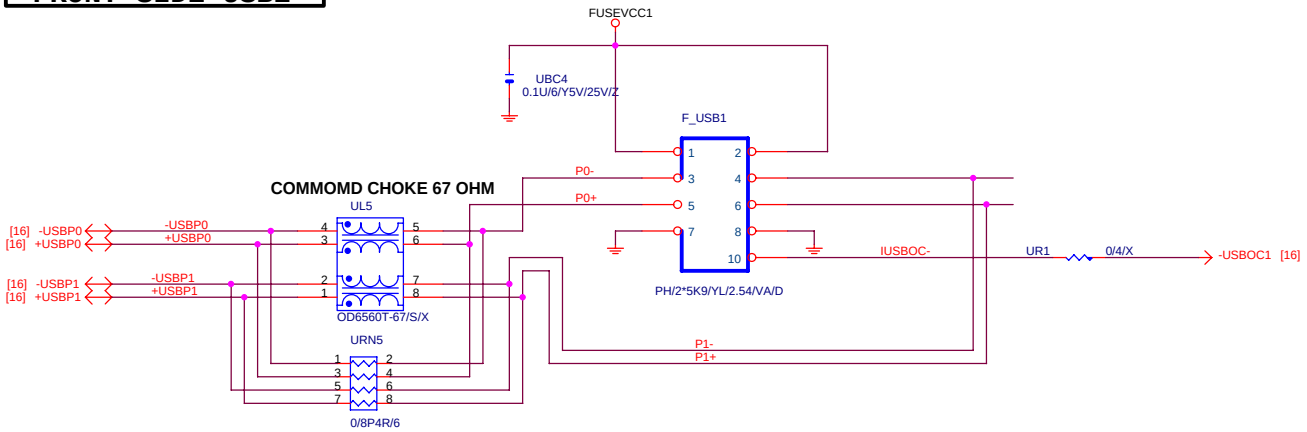
	Symbol	value	Description
JP1	Flashseg1_EN	1	Disabled.
		0	Flash I/F Address Segment 1 (FFF8_0000h~FFFF_FFFFh, 000E_0000h~000F_FFFFh) is enabled En SPI Flash
JP2	SerFlh_SO_SEL	1	FLH_SO2 is selected as the Serial Flash I/F SO pin.
		0	FLH_SO1 is selected as the Serial Flash I/F SO pin.
JP3	CHIP_SEL	--	Chip selection in configuration.
JP4	BUF_SEL	1	The output buffers of PCIRST1#, PCIRST2#, PCIRST3#, PCIRST4# and PCIRST5# are enhanced open-drain. It drives high about 10~20 ns when the signal transits from low to high, and then Hi-Z.
		0	The output buffers are push-pull.
JP5	FAN_CTL_SEL	1	The default value of EC Index 15h / 16h / 17h is 00h (Duty=100%)
		0	The default value of EC Index 15h / 16h / 17h is 40h (Duty=50%)
JP6	VID_ISEL	1	The threshold voltage of VID is 2.0 / 0.8V
		0	The threshold voltage of VID is 0.8 / 0.4V

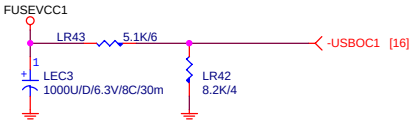
Hardware Monitor circuits



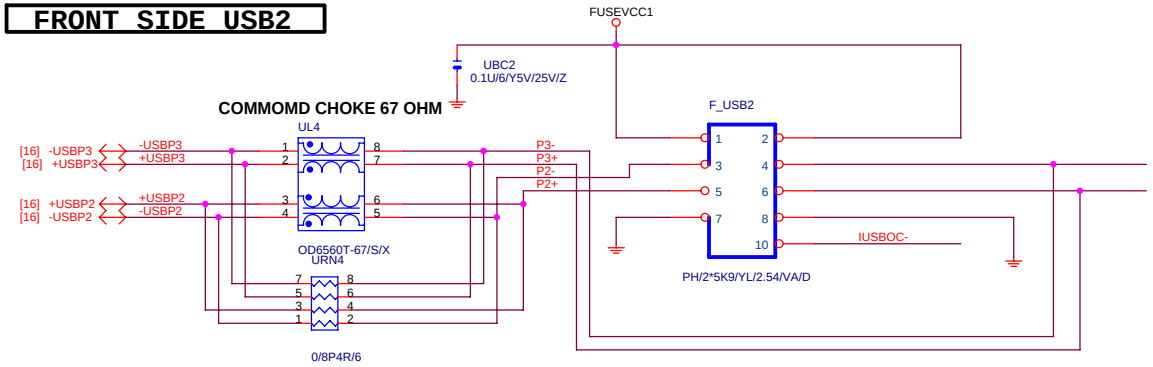
GIGABYTE CORP.		
Title: FAN/HWMO		
Size: B	Document Number: GA-M55S-S3	Rev: 1.11
Date: Thursday, August 17, 2006	Sheet 36 of 41	

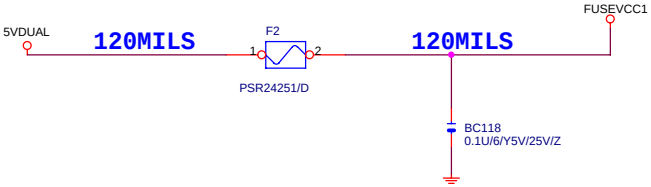
FRONT SIDE USB1



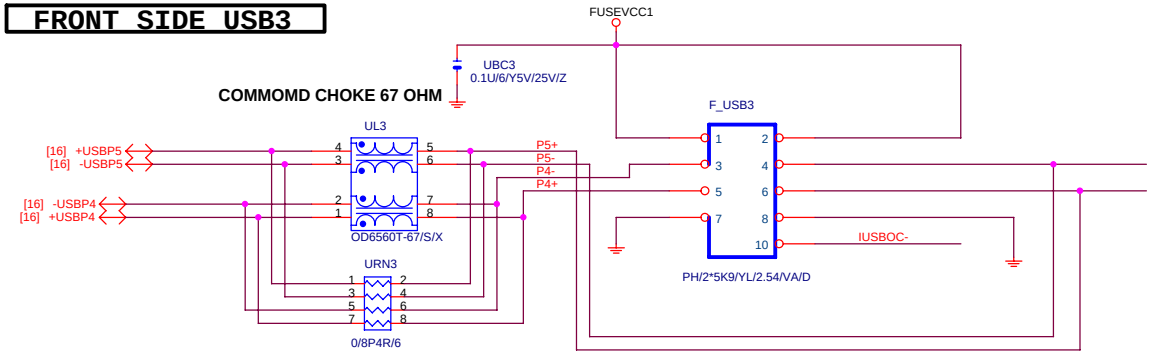


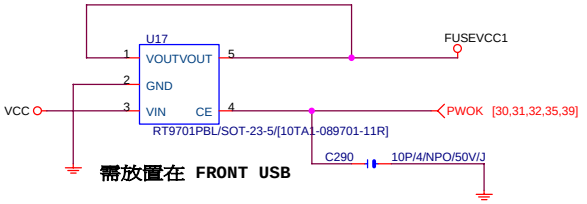
FRONT SIDE USB2



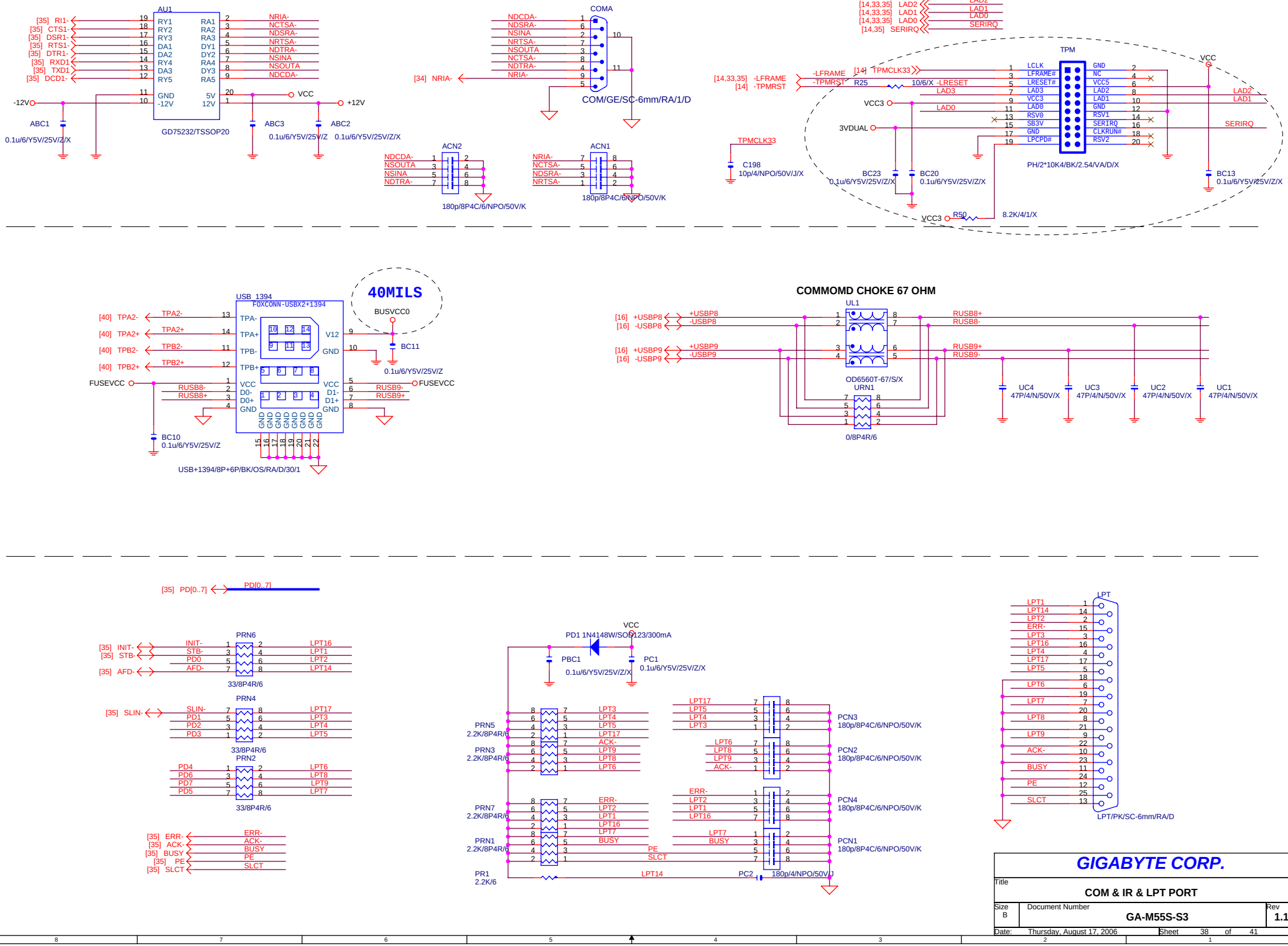


FRONT SIDE USB3





GIGABYTE CORP.		
Title: USB PORT		
Size: B	Document Number: GA-M55S-S3	Rev: 1.11
Date:	Sheet 37 of 41	

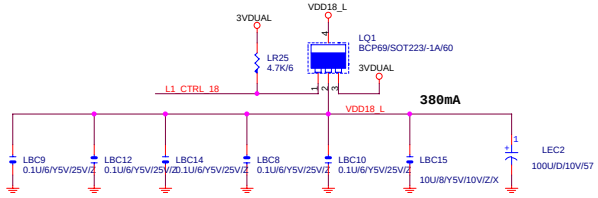


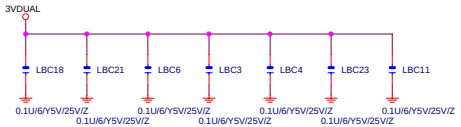
GIGABYTE CORP.		
Title	COM & IR & LPT PORT	
Size B	Document Number GA-M55S-S3	Rev 1.11
Date: Thursday, August 17, 2006	Sheet 38 of 41	

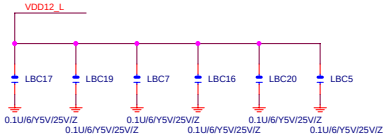
E1116 use external 2.5V single power supply.
1.8V create by PNP and 1.2V use internal reg.

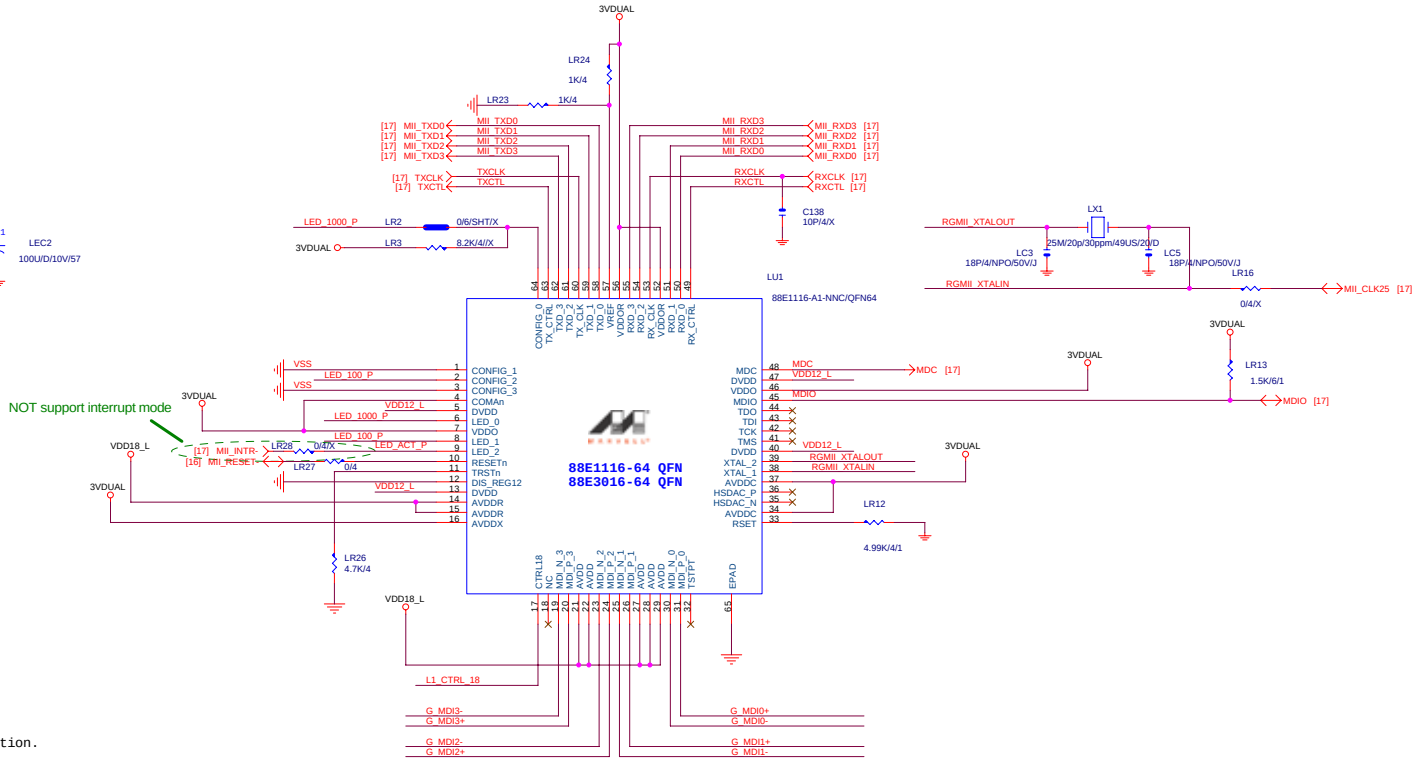
Hardware Configuration: See config _0:4

1. PHY address:00001
2. ENA_XC:Enable Auto-Crossover
3. RGMII_TX:Transmit clock not internally delayed
4. RGMII_RX:Receive clock transition when data transitions
5. Advertise all capabilities



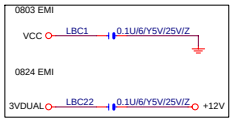


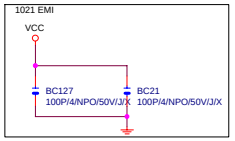




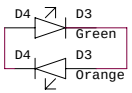
NOT support interrupt mode

Bypass cap can share. User check it by layout consideration.

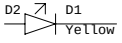


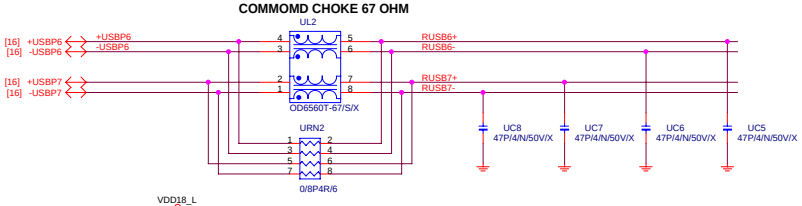


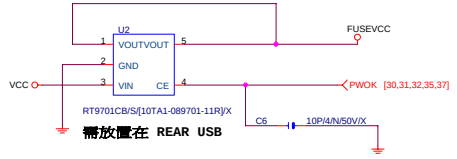
Dual Color LED



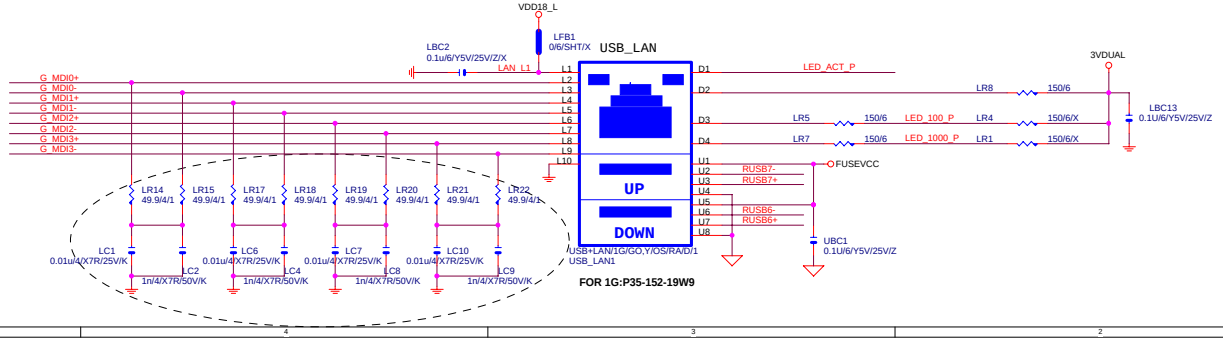
Single Color LED

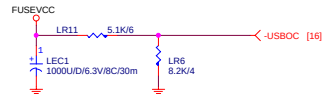




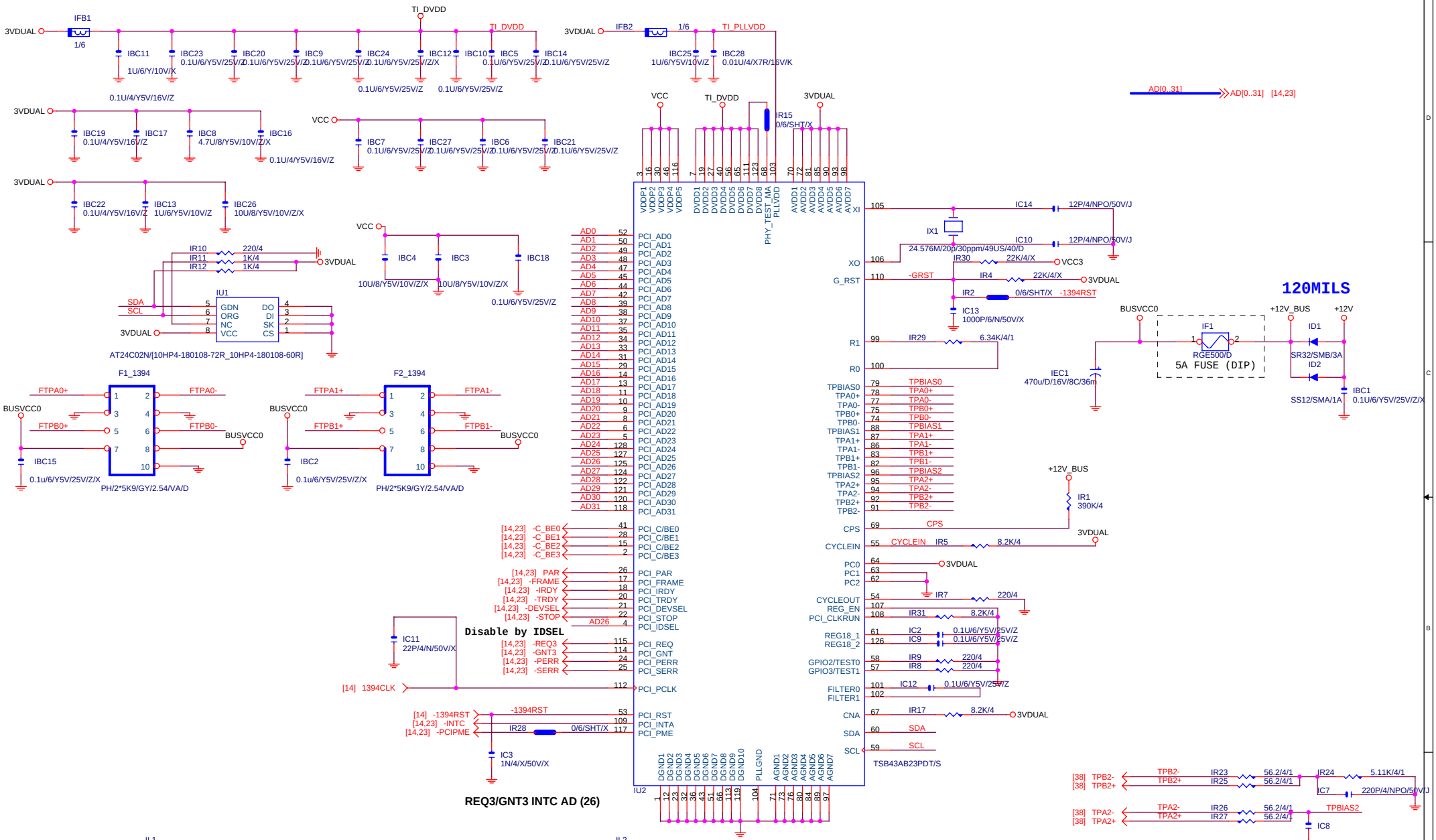


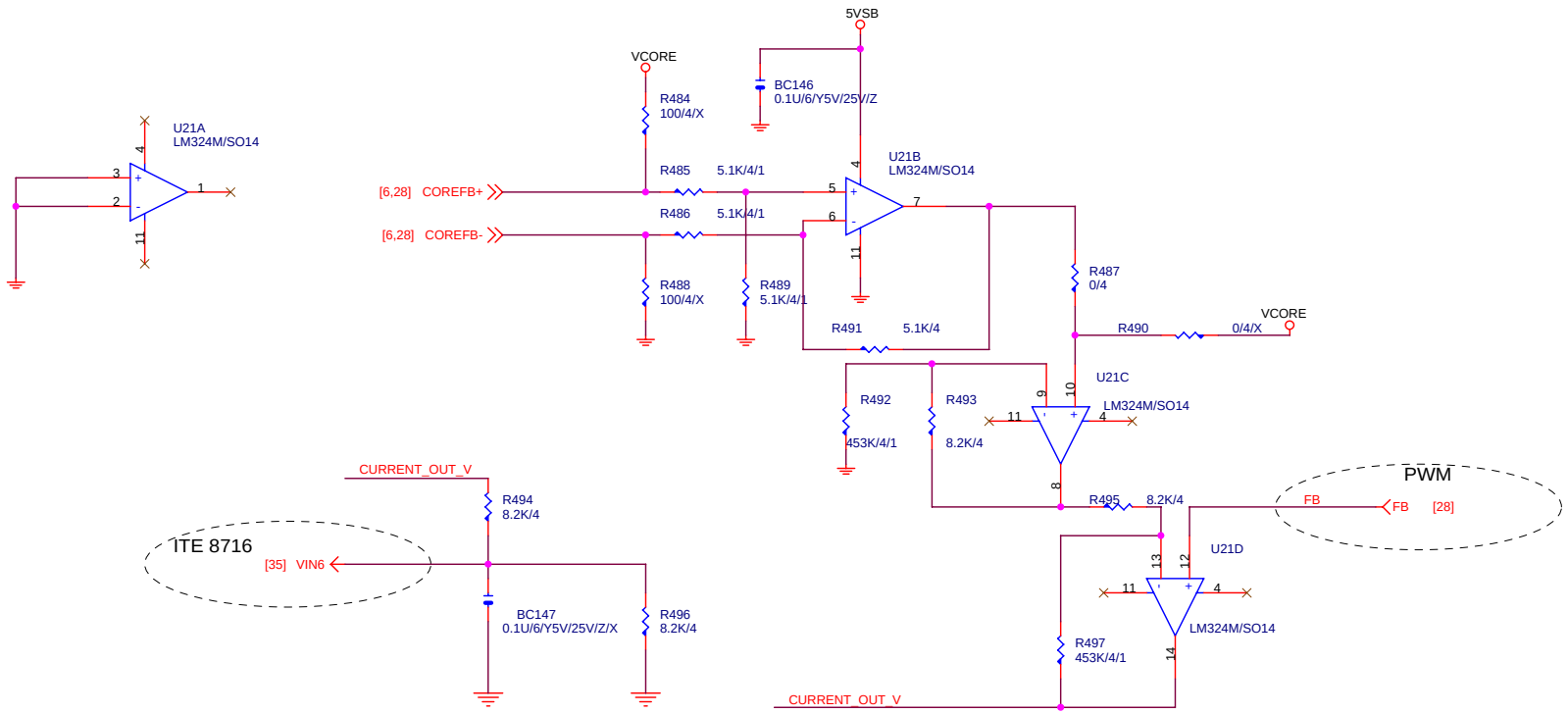
暫放置在 REAR USB





Title	Marvell_88E1115_88E1116_88E3016	
Size C	Document Number GA-M55S-S3	Rev 1.11
Date: Thursday, August 17, 2006	Sheet 39 of 41	


TSB43AB23PDT/S
IU2
AT24C02N/[10HP4-180108-72R_10HP4-180108-60R]
IU1
F1_1394
F2_1394
PH/2*5K9/GY/2.54/VA/D
IRN1
0/8P4RS/X
IRN2
OD6560-T-E601T/S/X
IL1
IL2
Disable by IDSEL
REQ3/GNT3 INTC AD (26)
AD[0..31]
AD[0..31] [14,23]
120MILS
5A FUSE (DIP)
RGE500/D
SS12/SMA/1A
SR32/SMB/3A
24.576M/20p/30ppm/49US/40/D
1000P/6/N/50V/X
470u/D/16V/8C/36m
GIGABYTE CORP.
Title
TSB43AB23A 1394A
Size
Custom
Document Number
GA-M55S-S3
Rev
1.11
Date:
Thursday, August 17, 2006
Sheet
40
of
41



GIGABYTE CORP.		
Title: CURRENT_OUT		
Size: B	Document Number: GA-M55S-S3	Rev: 1.11
Date: Thursday, August 17, 2006	Sheet 41 of 41	